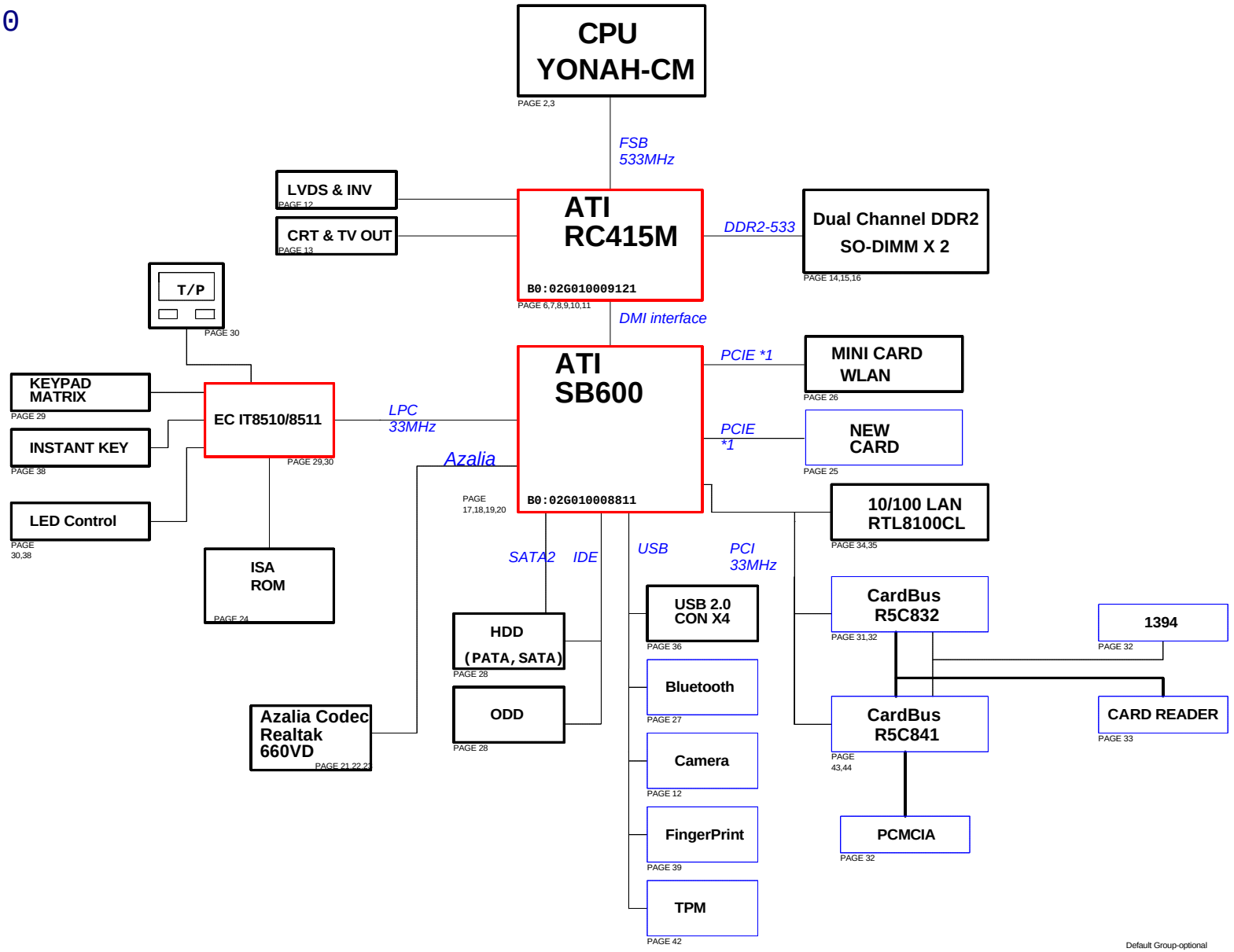
T12R Block Diagram

V2.0



PAGE 5

DISCHARGER CIRCUIT
PAGE 37

Power On Sequence
PAGE 40

DC/BATT IN
PAGE 41

CPU VCORE
PAGE 50

SYSTEM PWR
PAGE 51

BAT & CHARGER
PAGE 57

Default Group-optional

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 1 of 63

+VCCP_AGTL+ JP201 @ +VCCP
SHORT_PIN
2.5A

+VCCP +VCCP 5,6,10,17,19,20,52
+VCCP_AGTL+ +VCCP_AGTL+ 3

6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]

12G011204792==>12G04600479A

V1.1 ME

T202

U201A

ADDR GROUP 0
H_A#3 J4 A[3]#
H_A#4 L4 A[4]#
H_A#5 M3 A[5]#
H_A#6 K5 A[6]#
H_A#7 M1 A[7]#
H_A#8 N2 A[8]#
H_A#9 J1 A[9]#
H_A#10 N3 A[10]#
H_A#11 P5 A[11]#
H_A#12 P2 A[12]#
H_A#13 L1 A[13]#
H_A#14 P4 A[14]#
H_A#15 P1 A[15]#
H_A#16 R1 A[16]#
6 H_ADSTB#0 L2 ADSTB[0]#

H_REQ#0 K3 REQ[0]#
H_REQ#1 H2 REQ[1]#
H_REQ#2 K2 REQ[2]#
H_REQ#3 J3 REQ[3]#
H_REQ#4 L5 REQ[4]#

ADDR GROUP 1
H_A#17 Y2 A[17]#
H_A#18 U5 A[18]#
H_A#19 R3 A[19]#
H_A#20 W6 A[20]#
H_A#21 U4 A[21]#
H_A#22 Y5 A[22]#
H_A#23 U2 A[23]#
H_A#24 R4 A[24]#
H_A#25 T5 A[25]#
H_A#26 T3 A[26]#
H_A#27 W3 A[27]#
H_A#28 W5 A[28]#
H_A#29 Y4 A[29]#
H_A#30 W2 A[30]#
H_A#31 Y1 A[31]#
6 H_ADSTB#1 V4 ADSTB[1]#

THERM
17 H_A20M# A6 A20M#
17 H_FERR# A5 FERR#
17 H_IGNNE# C4 IGNNE#
THERMTRIP# C7 PM_THRMTRIP# 19

HCLK
17 H_STPCLK# D5 STPCLK#
17 H_INTR C6 LINT0
17 H_NMI B4 LINT1
17 H_SMI# A3 SMI#
A22 CLK_CPU_BCLK
A21 CLK_CPU_BCLK# 5
BCLK[0] CLK_CPU_BCLK 5
BCLK[1] CLK_CPU_BCLK# 5

RESERVED
AA1 RSVD[1]
AA4 RSVD[2]
AB2 RSVD[3]
AA3 RSVD[4]
M4 RSVD[5]
N5 RSVD[6]
T2 RSVD[7]
V3 RSVD[8]
B2 RSVD[9]
C3 RSVD[10]
B25 RSVD[11]
T22 RSVD[12]
A2 RSVD[A2]
D2 RSVD[13]
F6 RSVD[14]
D3 RSVD[15]
C1 RSVD[16]
AE1 RSVD[17]
D22 RSVD[18]
C23 RSVD[19]
C24 RSVD[20]

CONTROL
ADS# H1 H_ADS# H_ADS# 6
BNR# E2 H_BNR# H_BNR# 6
BPRI# G5 H_BPRI# H_BPRI# 6
H5 H_DEFER# H_DEFER# 6
DRDY# F21 H_DRDY# H_DRDY# 6
DBSY# E1 H_DBSY# H_DBSY# 6
BR0# F1 H_BR0# H_BR0# 6
IERR# D20 H_IERR#
INIT# B3 H_INIT# H_INIT# 17
LOCK# H4 H_LOCK# H_LOCK# 6
RESET# B1 H_CPURST# H_CPURST# 6
RS[0]# F3 H_RS#0 H_RS#0 6
RS[1]# E4 H_RS#1 H_RS#1 6
RS[2]# G3 H_RS#2 H_RS#2 6
TRDY# G2 H_TRDY# H_TRDY# 6
HIT# G6 H_HIT# H_HIT# 6
HITM# E4 H_HITM# H_HITM# 6

R201 56Ohm +VCCP_AGTL+
R202 54.9Ohm @ +VCCP_AGTL+
T201

XDP/ITP SIGNALS
BPM[0]# AD4
BPM[1]# AD3
BPM[2]# AD1
BPM[3]# AC4
PRDY# AC2
PREQ# AC1 H_PREQ# R203 56Ohm @ T203
TCK AC5 H_TCK 1 R204 2 56Ohm
TDI AA6 H_TDI 1 R205 2 56Ohm
TDO AB3 H_TDO R206 56Ohm @
TMS AB5 H_TMS 1 R207 2 56Ohm
TRST# AB6 H_TRST# 1 R208 2 56Ohm
DBR# C20 CPU_DBR# 1 T204 TPC28T
+VCCP_AGTL+
GND

PROCHOT# D21 H_PROCHOT_S#
THERMDA A24 CPU_THRM_DA CPU_THRM_DA 4
THERMDC A25 CPU_THRM_DC CPU_THRM_DC 4

U201B

DATA GRP 0
H_D#0 E22 D[0]# AA23 H_D#32
H_D#1 F24 D[1]# AB24 H_D#33
H_D#2 E26 D[2]# V24 H_D#34
H_D#3 H22 D[3]# V26 H_D#35
H_D#4 F23 D[4]# W25 H_D#36
H_D#5 G25 D[5]# U23 H_D#37
H_D#6 E25 D[6]# U25 H_D#38
H_D#7 F23 D[7]# U22 H_D#39
H_D#8 K24 D[8]# AB25 H_D#40
H_D#9 G24 D[9]# W22 H_D#41
H_D#10 J24 D[10]# Y23 H_D#42
H_D#11 J23 D[11]# AA26 H_D#43
H_D#12 H26 D[12]# Y26 H_D#44
H_D#13 F26 D[13]# Y22 H_D#45
H_D#14 K22 D[14]# AC26 H_D#46
H_D#15 H25 D[15]# AA24 H_D#47
6 H_DSTBN#0 H23 DSTBN[0]# W24 H_DSTBN#2 DSTBN[2]# H_DSTBN#2 6
6 H_DSTBP#0 G22 DSTBP[0]# Y25 H_DSTBP#2 DSTBP[2]# H_DSTBP#2 6
6 H_DINV#0 J26 DINV[0]# V23 H_DINV#2 DINV[2]# H_DINV#2 6

DATA GRP 1
H_D#16 N22 D[16]# AC22 H_D#48
H_D#17 K25 D[17]# AC23 H_D#49
H_D#18 P26 D[18]# AB22 H_D#50
H_D#19 R23 D[19]# AA21 H_D#51
H_D#20 L25 D[20]# AB21 H_D#52
H_D#21 L22 D[21]# AC25 H_D#53
H_D#22 L23 D[22]# AD20 H_D#54
H_D#23 M23 D[23]# AE22 H_D#55
H_D#24 P25 D[24]# AF23 H_D#56
H_D#25 P22 D[25]# AD24 H_D#57
H_D#26 P23 D[26]# AE21 H_D#58
H_D#27 T24 D[27]# AD21 H_D#59
H_D#28 R24 D[28]# AE25 H_D#60
H_D#29 L26 D[29]# AE25 H_D#61
H_D#30 T25 D[30]# AF22 H_D#62
H_D#31 N24 D[31]# AF26 H_D#63
6 H_DSTBN#1 M24 DSTBN[1]# AD23 H_DSTBN#3 DSTBN[3]# H_DSTBN#3 6
6 H_DSTBP#1 N25 DSTBP[1]# AE24 H_DSTBP#3 DSTBP[3]# H_DSTBP#3 6
6 H_DINV#1 M26 DINV[1]# AC20 H_DINV#3 DINV[3]# H_DINV#3 6

H_D#[0..63] 6

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

MISC
GTL_REF AD26
GTLREF
TEST1 C26 TEST1
TEST2 D25 TEST2
BSEL[0] B22 CPU_BSEL0
BSEL[1] B23 CPU_BSEL1
BSEL[2] C21 CPU_BSEL2
COMP[0] R26 H_COMP0 R210 1 2 27.4Ohm 1%
COMP[1] U26 H_COMP1 R211 1 2 54.9Ohm 1%
COMP[2] U1 H_COMP2 R212 1 2 27.4Ohm 1%
COMP[3] V1 H_COMP3 R215 1 2 54.9Ohm 1%
GND
DPRSTP# E5 H_DPRSTP# H_DPRSTP# 17,50
DPSLP# B5 H_DPSLP# H_DPSLP# 17
DPWR# D24 H_DPWR# H_DPWR# 6
PWRGOOD D6 H_PWRGD H_PWRGD 17
SLP# D7
PSI# AE6 H_CPUSLP# PM_PSI# H_SLP# 6,17 PM_PSI# 50
T205

+VCCP_AGTL+
R209 1KOhm 1% 6 H_DSTBN#1 6 H_DSTBP#1 6 H_DINV#1
<500 mil (55 Ohm) T/B trace 5 Space 25
C201 0.1UF/10V @
R213 2KOhm 1%
@R214 1KOhm
R216 51Ohm
GND
5 CPU_BSEL0 5 CPU_BSEL1 5 CPU_BSEL2

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

12G04600479A
12G04600479A

12G04600479A

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

H_PROCHOT_S# R217 56Ohm +VCCP_AGTL+

Default Group-optional

Title : YONAH CPU (1)
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12R | Rev: 2.0
Date: Wednesday, August 09, 2006 | Sheet 2 of 63

+VCCP_AGTL+ → +VCCP_AGTL+ 2
+VCORE → +VCORE 50
+1.5VO → +1.5VO 54

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

U201C

12G04600479A

JP301 1MM_OPEN_5MIL @

120mA / 20mil
Close to Pin B26
C301 10UF/10V
C318 0.01UF/25V
checklist suggests 10uF POSCAP

R301 100Ohm
R302 100Ohm

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

U201D

12G04600479A

1215---PWR comp
CE301 330UF/2V N/A
Place the cap on North of Secondary side

Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

Place these upper side inside socket cavity on L1
C302 C303 C304 C305 C306 C307 22UF/6.3V

Place these lower side inside socket cavity on L1
C308 C309 C310 C311 C312 C313 22UF/6.3V

Place these upper side inside socket cavity on L6
C314 C315 C316 C317 22UF/6.3V

Place these lower side inside socket cavity on L6
C319 C320 C321 C322 22UF/6.3V

+1.05V Decoupling Capacitor
Place near CPU
C323 C324 C325 C326 C327 C328 c0402 0.1UF/10V
CE302 100UF/2.5V

V1.1 EMI
C332 C333 c0402 0.1UF/10V

Default Group-optional

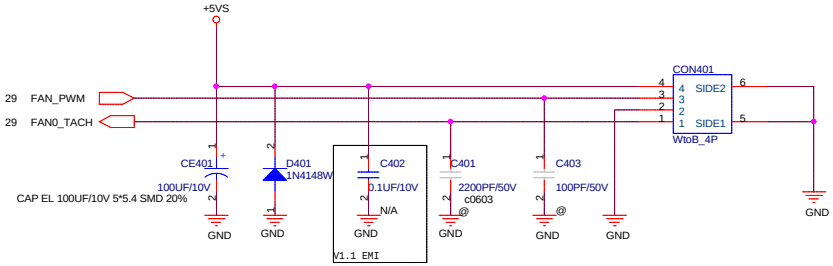
Title : Yonah CPU (2)
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12R | Rev: 2.0
Date: Wednesday, August 09, 2006 | Sheet 3 of 63

+5VS +5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS +3VS 5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

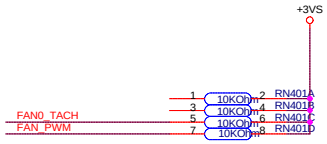
Fan Speed Control

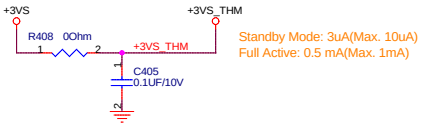
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



COULD BE CLOSED TO EC

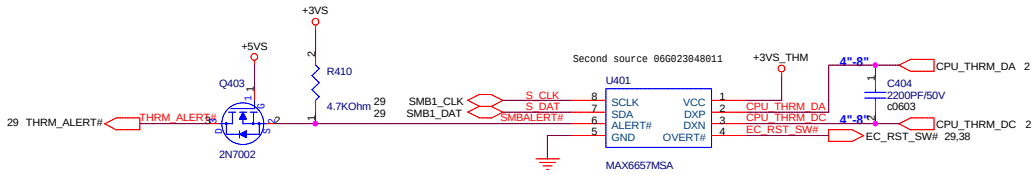




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



Default Group-optional

ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

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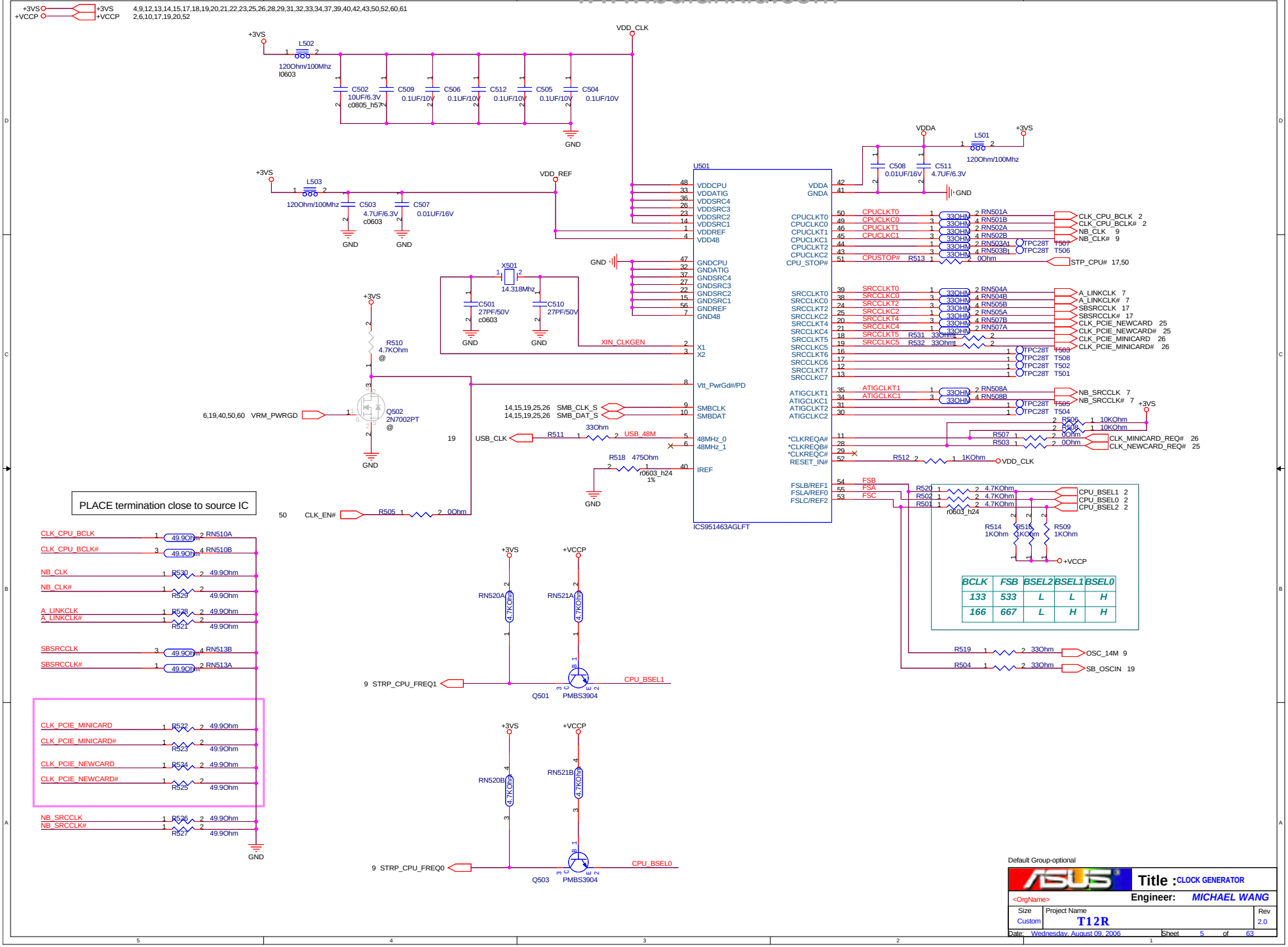

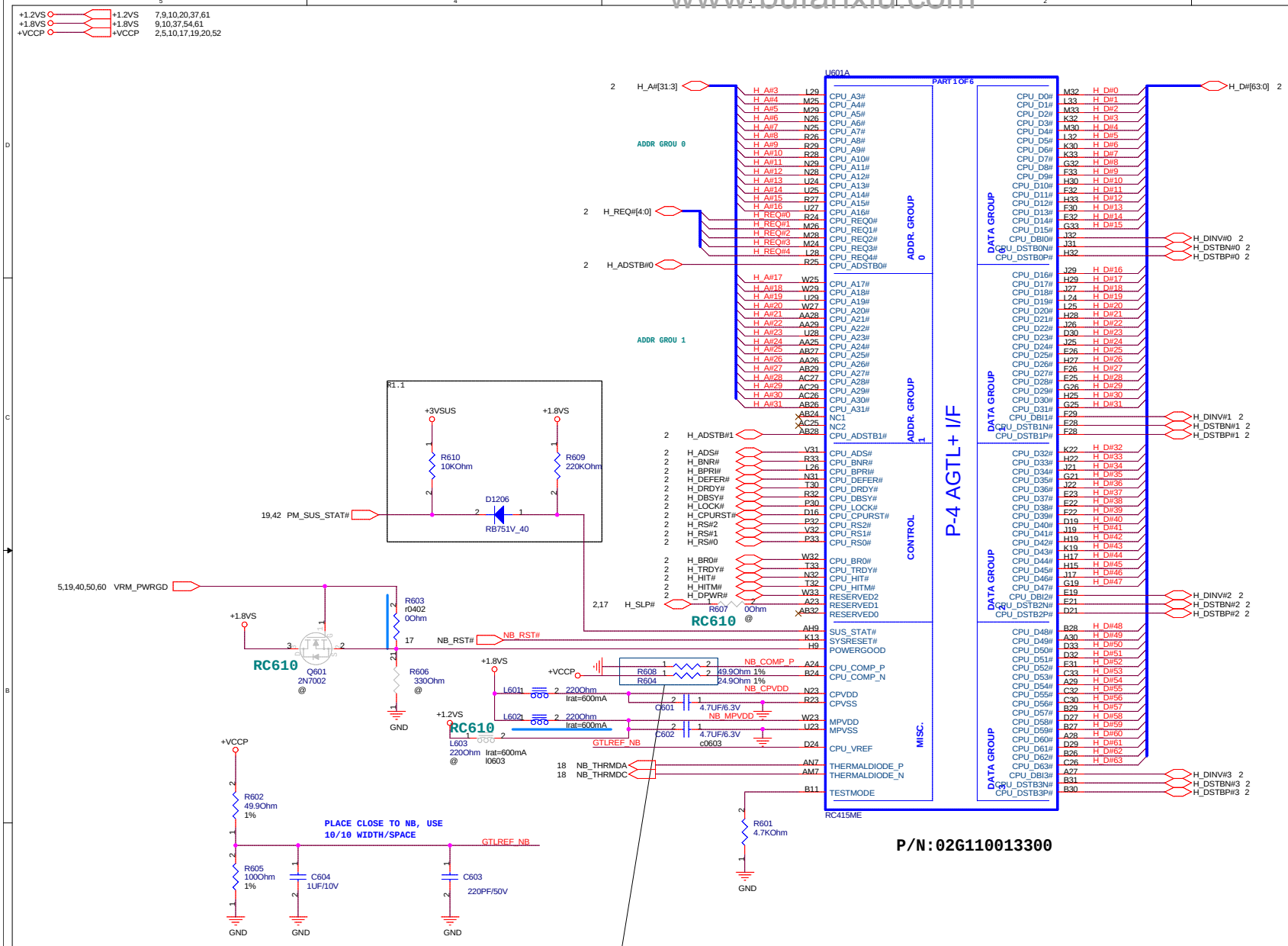

RC610/RC515	RC610	RC415
R0608	53.6(10G21**********)	49.9(10G21249R914030)
R0604	21 (10G21**********)	24.9(10G21224R914040)

Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title : NBRC415M(HOST)

Engineer:

Size	Project Name	Rev
Custom	T12R	2.0

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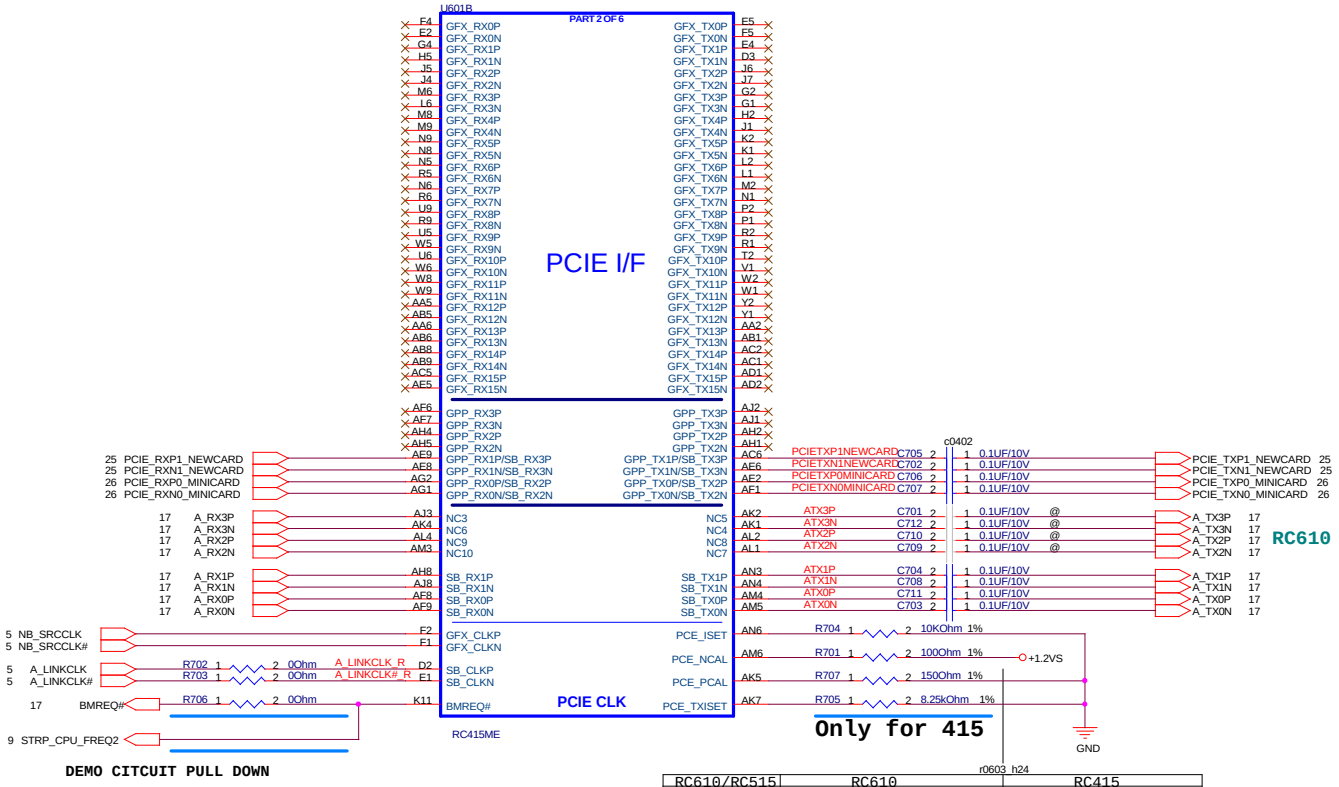
+1.2VS ⟶ +1.2VS 6,9,10,20,37,61



RC610/RC515	RC610	RC415
R0704	1.47K(10G21**********)	10K(10G213100213030)
R0701	2K (10G21**********)	100(10G213100013010)
R0707	562 (10G21**********)	150(10G213150013030)

Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title : NB-945PM(DMI & CFG)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 7 of 63

+1.8V +1.8V 10,14,15,16,37,53

U601C

PART3OF6

MEM_B I/F

M_A_A0	AN20	MEM_A0
M_A_A1	AJ19	MEM_A1
M_A_A2	AM19	MEM_A2
M_A_A3	AN19	MEM_A3
M_A_A4	AK18	MEM_A4
M_A_A5	AM18	MEM_A5
M_A_A6	AN18	MEM_A6
M_A_A7	AM16	MEM_A7
M_A_A8	AL16	MEM_A8
M_A_A9	AH15	MEM_A9
M_A_A10	AM20	MEM_A10
M_A_A11	AJ15	MEM_A11
M_A_A12	AN15	MEM_A12
M_A_A13	AM24	MEM_A13
M_A_A14	AK15	MEM_A14
M_A_A15	AM21	MEM_A15
M_A_A16	AK20	MEM_A16
M_A_A17	AM15	MEM_A17
M_A_DM0	AJ13	MEM_DM0
M_A_DM1	AM10	MEM_DM1
M_A_DM2	AH17	MEM_DM2
M_A_DM3	AF23	MEM_DM3
M_A_DM4	AH28	MEM_DM4
M_A_DM5	AM29	MEM_DM5
M_A_DM6	AK33	MEM_DM6
M_A_DM7	AE32	MEM_DM7
	AL21	MEM_RAS#
	AN23	MEM_CAS#
	AM23	MEM_WE#
M_A_DQS0	AE12	MEM_DQS0P
M_A_DQS1	AN11	MEM_DQS1P
M_A_DQS2	AE19	MEM_DQS2P
M_A_DQS3	AJ23	MEM_DQS3P
M_A_DQS4	AF27	MEM_DQS4P
M_A_DQS5	AN30	MEM_DQS5P
M_A_DQS6	AJ33	MEM_DQS6P
M_A_DQS7	AD33	MEM_DQS7P
M_A_DQS#0	AD12	MEM_DQS0N
M_A_DQS#1	AM11	MEM_DQS1N
M_A_DQS#2	AF17	MEM_DQS2N
M_A_DQS#3	AH23	MEM_DQS3N
M_A_DQS#4	AF26	MEM_DQS4N
M_A_DQS#5	AM30	MEM_DQS5N
M_A_DQS#6	AJ32	MEM_DQS6N
M_A_DQS#7	AD32	MEM_DQS7N
	AC24	MEM_CK0N
	AE25	MEM_CK0P
	AE15	MEM_CK1N
	AF15	MEM_CK1P
	AF29	MEM_CK2N
	AE30	MEM_CK2P
	AF23	MEM_CK3N
	AD23	MEM_CK3P
	AD15	MEM_CK4N
	AD17	MEM_CK4P
	AF27	MEM_CK5N
	AE26	MEM_CK5P
	AN14	MEM_CKE0
	AM14	MEM_CKE1
	AN13	MEM_CKE2
	AK13	MEM_CKE3
	AN22	MEM_CS0#
	AN24	MEM_CS1#
	AN22	MEM_CS2#
	AM25	MEM_CS3#
	AK24	MEM_ODT0
	AK26	MEM_ODT1
	AL25	MEM_ODT2
	AN26	MEM_ODT3
	AM26	MEM_COMPN
	AM27	MEM_COMPP
	AJ26	MEM_VMODE
	AN27	MEM_VREF

MEM_DQ0	AH11	M_A_DQ0
MEM_DQ1	AG12	M_A_DQ1
MEM_DQ2	AE13	M_A_DQ2
MEM_DQ3	AF13	M_A_DQ3
MEM_DQ4	AJ11	M_A_DQ4
MEM_DQ5	AJ12	M_A_DQ5
MEM_DQ6	AH12	M_A_DQ6
MEM_DQ7	AG13	M_A_DQ7
MEM_DQ8	AM9	M_A_DQ8
MEM_DQ9	AN10	M_A_DQ9
MEM_DQ10	AM12	M_A_DQ10
MEM_DQ11	AM13	M_A_DQ11
MEM_DQ12	AN9	M_A_DQ12
MEM_DQ13	AK9	M_A_DQ13
MEM_DQ14	AK11	M_A_DQ14
MEM_DQ15	AL12	M_A_DQ15
MEM_DQ16	AE19	M_A_DQ16
MEM_DQ17	AH19	M_A_DQ17
MEM_DQ18	AJ21	M_A_DQ18
MEM_DQ19	AK22	M_A_DQ19
MEM_DQ20	AE17	M_A_DQ20
MEM_DQ21	AJ17	M_A_DQ21
MEM_DQ22	AF21	M_A_DQ22
MEM_DQ23	AE21	M_A_DQ23
MEM_DQ24	AF22	M_A_DQ24
MEM_DQ25	AJ22	M_A_DQ25
MEM_DQ26	AG25	M_A_DQ26
MEM_DQ27	AH25	M_A_DQ27
MEM_DQ28	AH21	M_A_DQ28
MEM_DQ29	AG22	M_A_DQ29
MEM_DQ30	AG23	M_A_DQ30
MEM_DQ31	AJ25	M_A_DQ31
MEM_DQ32	AG26	M_A_DQ32
MEM_DQ33	AJ29	M_A_DQ33
MEM_DQ34	AH29	M_A_DQ34
MEM_DQ35	AJ30	M_A_DQ35
MEM_DQ36	AH26	M_A_DQ36
MEM_DQ37	AJ28	M_A_DQ37
MEM_DQ38	AF28	M_A_DQ38
MEM_DQ39	AF29	M_A_DQ39
MEM_DQ40	AM28	M_A_DQ40
MEM_DQ41	AL29	M_A_DQ41
MEM_DQ42	AL31	M_A_DQ42
MEM_DQ43	AM31	M_A_DQ43
MEM_DQ44	AK28	M_A_DQ44
MEM_DQ45	AN28	M_A_DQ45
MEM_DQ46	AK30	M_A_DQ46
MEM_DQ47	AN31	M_A_DQ47
MEM_DQ48	AL32	M_A_DQ48
MEM_DQ49	AK32	M_A_DQ49
MEM_DQ50	AH33	M_A_DQ50
MEM_DQ51	AH32	M_A_DQ51
MEM_DQ52	AM32	M_A_DQ52
MEM_DQ53	AL33	M_A_DQ53
MEM_DQ54	AG33	M_A_DQ54
MEM_DQ55	AG32	M_A_DQ55
MEM_DQ56	AF32	M_A_DQ56
MEM_DQ57	AE33	M_A_DQ57
MEM_DQ58	AC32	M_A_DQ58
MEM_DQ59	AB33	M_A_DQ59
MEM_DQ60	AG30	M_A_DQ60
MEM_DQ61	AF31	M_A_DQ61
MEM_DQ62	AC30	M_A_DQ62
MEM_DQ63	AB31	M_A_DQ63

RC415ME

M_A_DQ[63..0] M_A_DQ[63..0] 14,15

14,15,16 M_A_A[17..0] M_A_A[17..0]

14,15 M_A_DM[7..0] M_A_DM[7..0]

14,15,16 M_A_RAS#
14,15,16 M_A_CAS#
14,15,16 M_A_WE#

14,15 M_A_DQS[7..0] M_A_DQS[7..0]

14,15 M_A_DQS#[7..0] M_A_DQS#[7..0]

14 M_CLK_DDR#0
14 M_CLK_DDR0
14 M_CLK_DDR#1
14 M_CLK_DDR1

15 M_CLK_DDR#3
15 M_CLK_DDR3
15 M_CLK_DDR#4
15 M_CLK_DDR4

14,16 M_CKE0
14,16 M_CKE1
15,16 M_CKE2
15,16 M_CKE3

14,16 M_CS#0
14,16 M_CS#1
15,16 M_CS#2
15,16 M_CS#3

14,16 M_ODT0
15,16 M_ODT1
14,16 M_ODT2
15,16 M_ODT3

+1.8V
MEM_COMPN — 61.9Ohm — R804 1% r0603_h24
MEM_COMPP — 61.9Ohm — R805 1%
MEM_MODE — 4.7KOhm — R803 r0603_h24 — GND
MEM_VREF

+1.8V
R801 1KOhm 1% — C801 0.1UF/16V
R802 1KOhm 1% — C802 0.1UF/16V
GND

RC610/RC515	RC610	RC415
R07??/R07??	40.2(10G21*********)	61.9(10G213100213030)

Default Group-optional

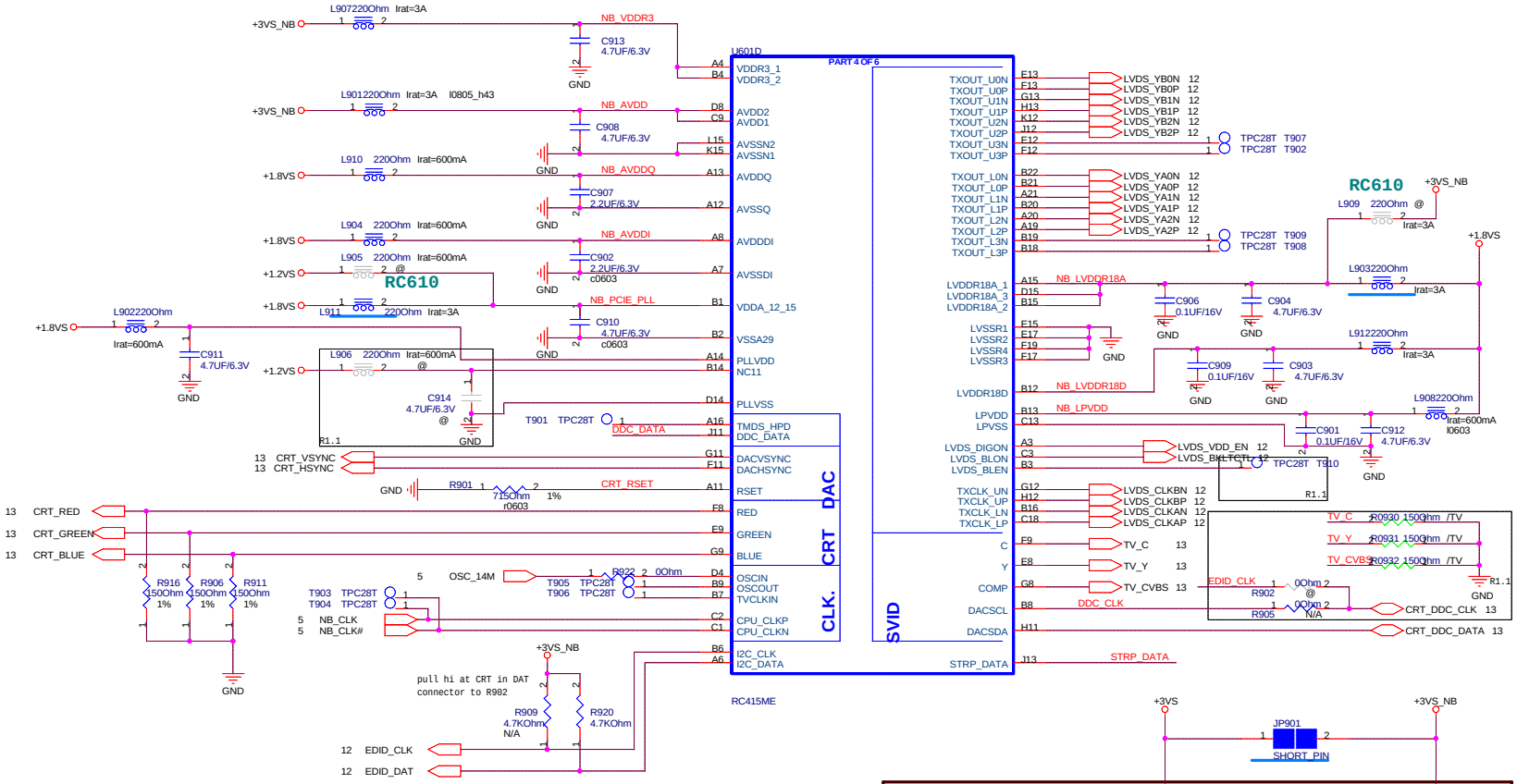
Title : NB_945PM(PCI-E)

ASUSTeK COMPUTER INC. NB1 Engineer: MICHAEL WANG

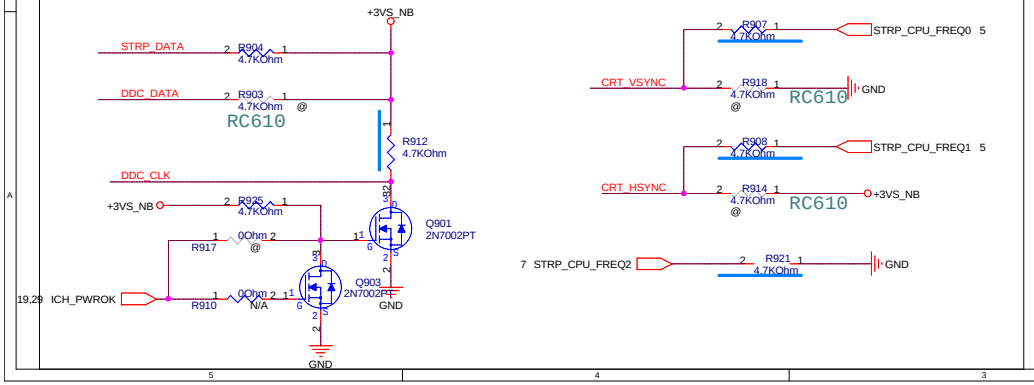
Size	Project Name	Rev
Custom	T12R	2.0

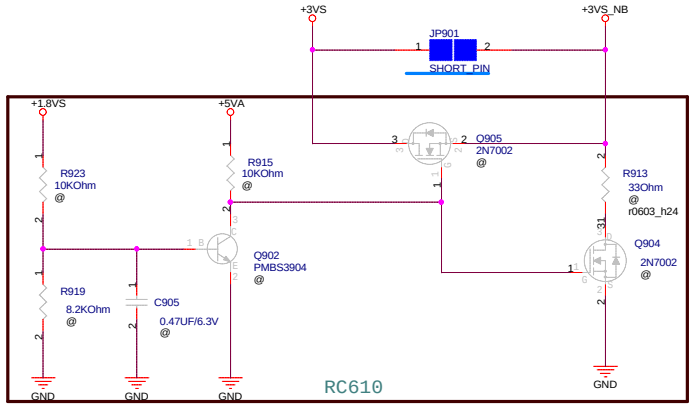
Date: Wednesday, August 09, 2006 Sheet 8 of 63

+3VS 4,5,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.8VS 6,10,37,54,61
+1.2VS 6,7,10,20,37,61



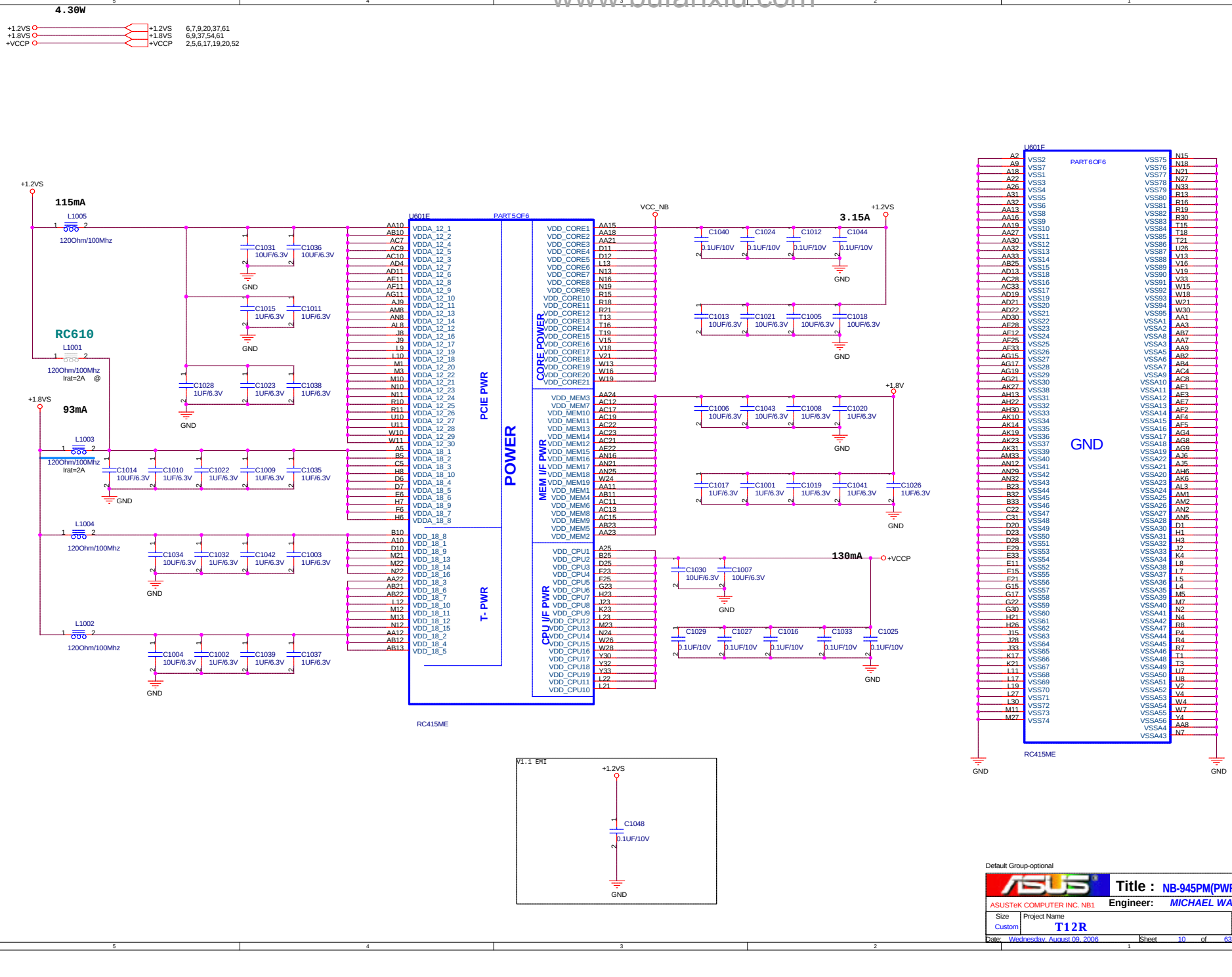
STRAPS





Default Group-optional

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(DDR2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 9 of 63	



Default Group-optional

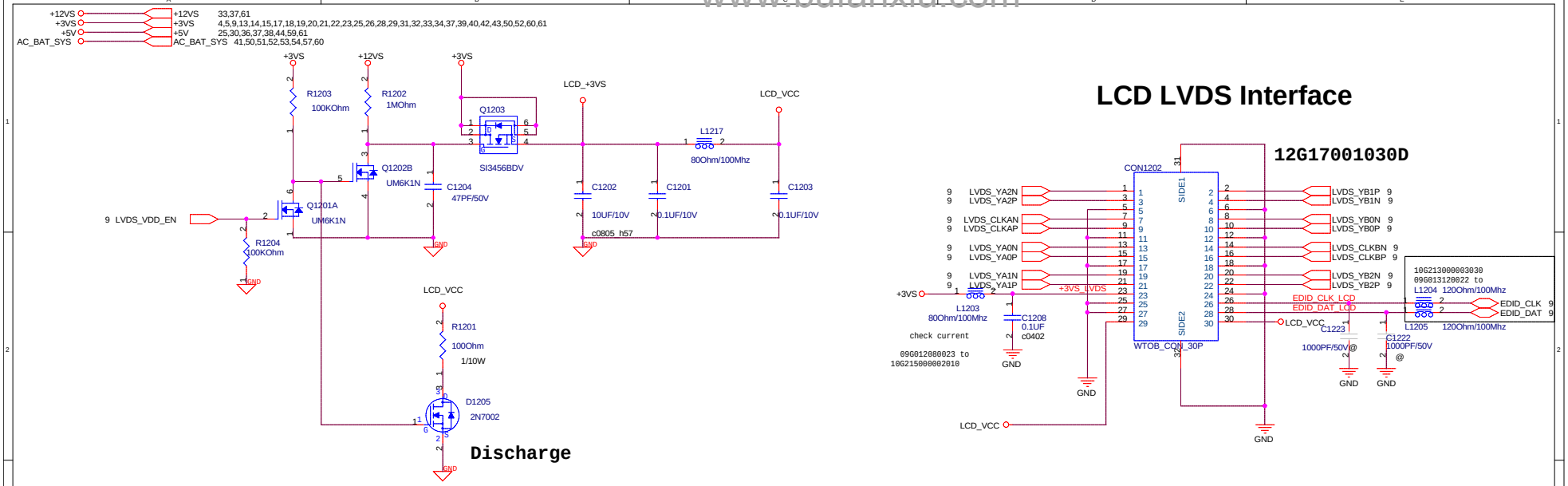
Title : HISTORY

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 11 of 63



LCD LVDS Interface

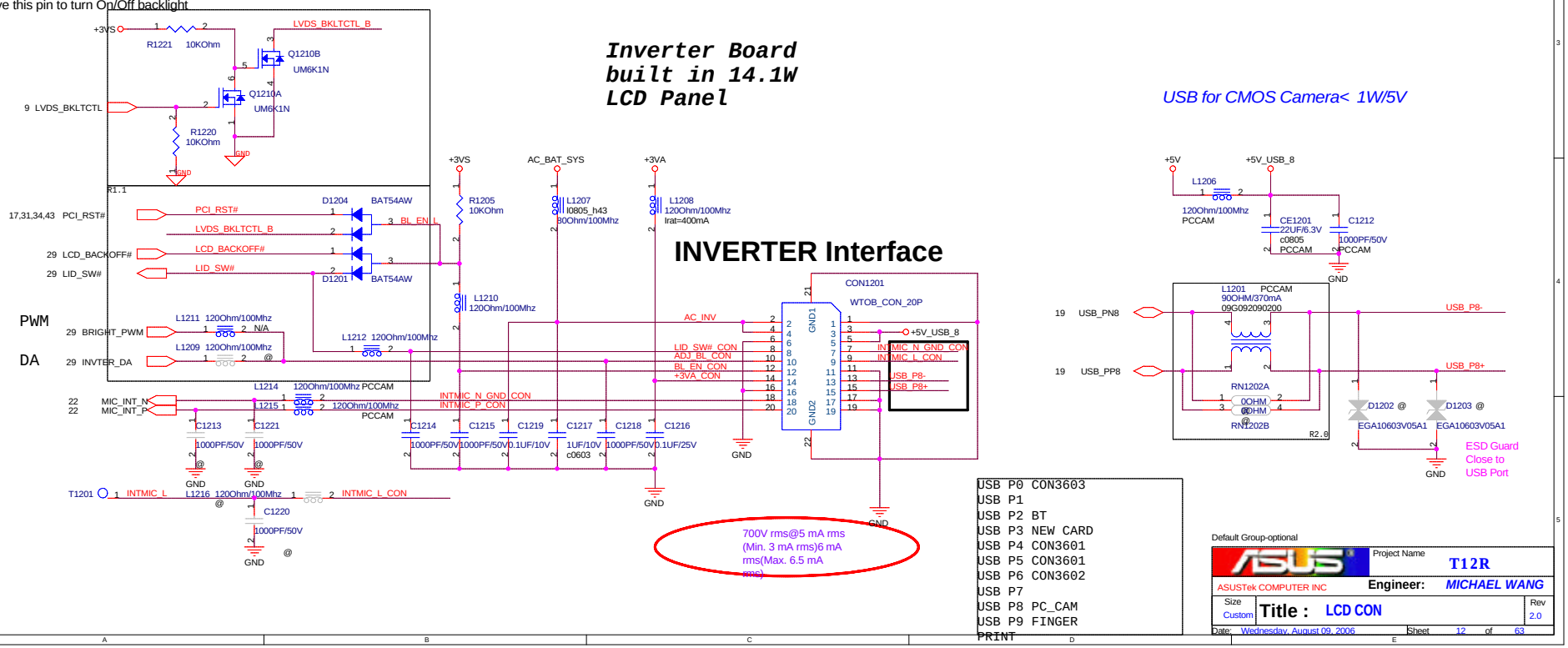
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

Inverter Board built in 14.1W LCD Panel

USB for CMOS Camera< 1W/5V

INVERTER Interface



USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT

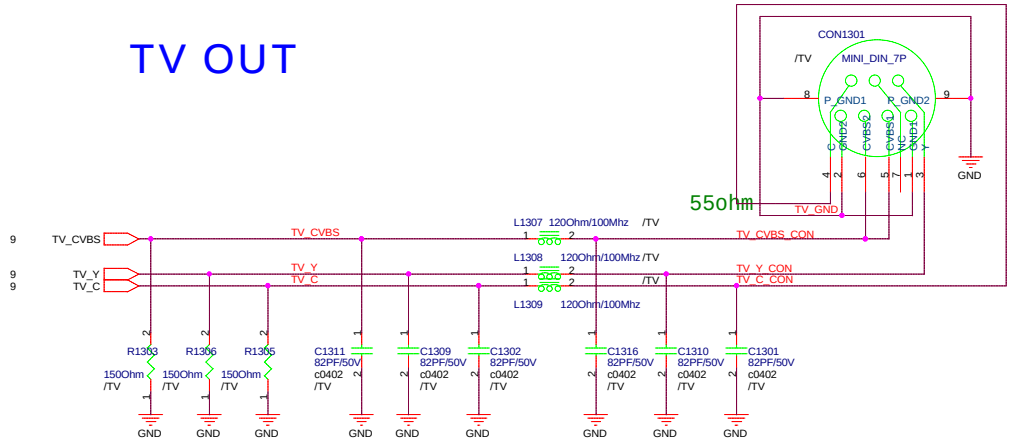
Default Group-optional

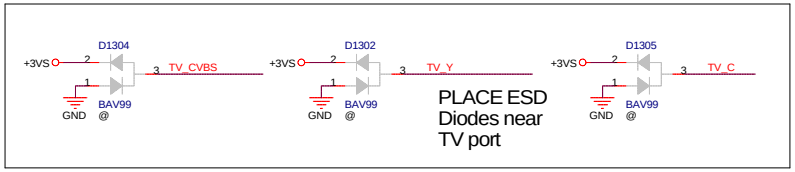
ASUSTek COMPUTER INC	Project Name: T12R	Engineer: MICHAEL WANG
Size: Custom	Title : LCD CON	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 12 of 63	

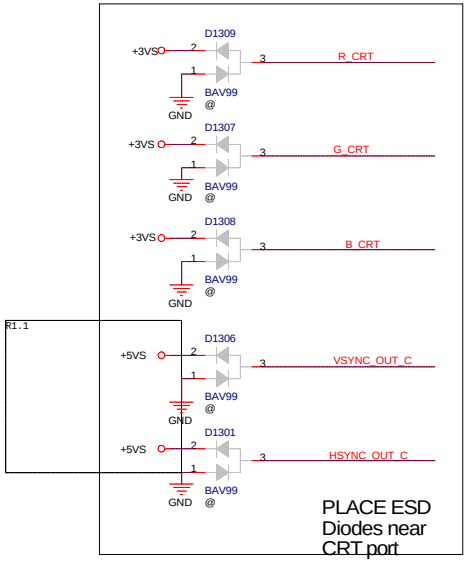
+5VS → +5VS 4,20,22,23,28,29,30,37,38,50,61
+3VS → +3VS 4,5,9,12,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

12G141011076

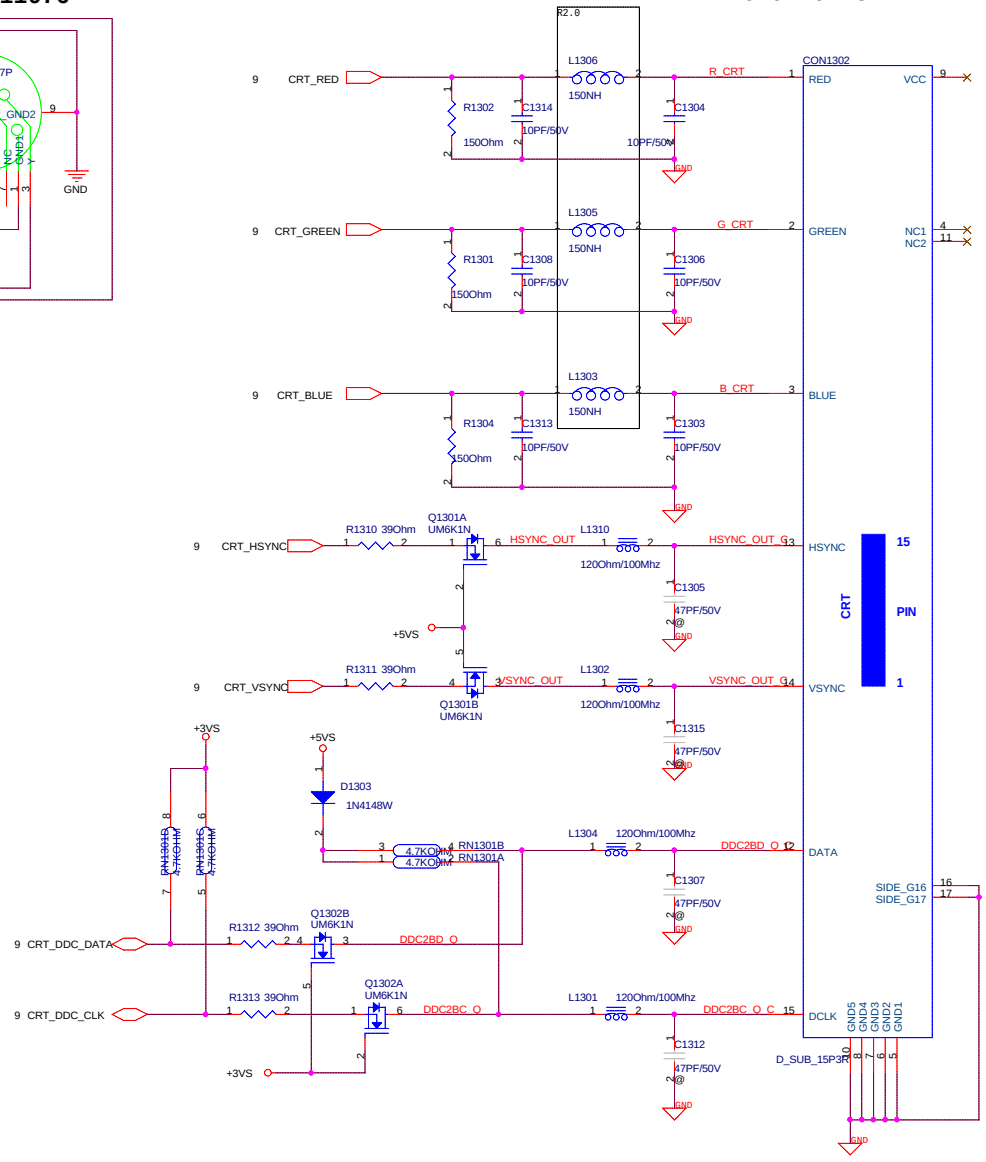
TV OUT







12G101102152
=>12G10110215A



Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	Engineer: MICHAEL WANG
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 13 of 63	

+3VS
+1.8V
+3VS
+1.8V
4,5,9,12,13,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,15,16,37,53

FRON

PN:12G02502200E==>12G025022004
V1.1 ME second source

M_CLK_DDR0
C1401
10PF/50V
@
M_CLK_DDR#0

M_CLK_DDR1
C1402
10PF/50V
@
M_CLK_DDR#1

CON1401A

8,15,16 M_A_A[17:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A17 M_A_A15 M_A_A16
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2 BA0 BA1

8,16 M_CS#0
8,16 M_CS#1
8 M_CLK_DDR1
8 M_CLK_DDR#1
8 M_CLK_DDR0
8 M_CLK_DDR#0
8,16 M_CKE0
8,16 M_CKE1
8,15,16 M_A_CAS#
8,15,16 M_A_RAS#
8,15,16 M_A_WE#
S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

5,15,19,25,26 SMB_CLK_S
5,15,19,25,26 SMB_DAT_S
SA0 SA1 SCL SDA

8,16 M_ODT0
8,16 M_ODT2
8,15 M_A_DM[7:0]
ODT0 ODT1
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

8,15 M_A_DQS[7:0]
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

8,15 M_A_DQS#[7:0]
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

M_A_DQ[63..0] 8,15
M_A_DQ0 M_A_DQ1 M_A_DQ6 M_A_DQ5 M_A_DQ2 M_A_DQ3 M_A_DQ0 M_A_DQ4 M_A_DQ10 M_A_DQ14 M_A_DQ9 M_A_DQ11 M_A_DQ15 M_A_DQ13 M_A_DQ12 M_A_DQ8 M_A_DQ23 M_A_DQ20 M_A_DQ17 M_A_DQ19 M_A_DQ16 M_A_DQ22 M_A_DQ21 M_A_DQ18 M_A_DQ30 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ31 M_A_DQ38 M_A_DQ39 M_A_DQ33 M_A_DQ35 M_A_DQ32 M_A_DQ36 M_A_DQ37 M_A_DQ34 M_A_DQ45 M_A_DQ41 M_A_DQ42 M_A_DQ46 M_A_DQ40 M_A_DQ44 M_A_DQ47 M_A_DQ53 M_A_DQ49 M_A_DQ50 M_A_DQ54 M_A_DQ48 M_A_DQ52 M_A_DQ55 M_A_DQ51 M_A_DQ56 M_A_DQ60 M_A_DQ58 M_A_DQ63 M_A_DQ57 M_A_DQ61 M_A_DQ62 M_A_DQ59
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

DDR2_DIMM_200P

+1.8V
C1403 2.2UF/6.3V
C1404 2.2UF/6.3V
C1405 2.2UF/6.3V
C1406 2.2UF/6.3V
C1407 2.2UF/6.3V
C1408 0.1UF/10V
C1409 0.1UF/10V
C1410 0.1UF/10V
C1411 0.1UF/10V
+3VS
C1412 2.2UF/6.3V
C1413 0.1UF/10V
15,16 M_VREF_DIMM0
C1414 2.2UF/6.3V
C1415 0.1UF/10V

CON1401B
112 111 117 96 95 118 81 82 87 103 88 104 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12
199 VDDSPD
83 120 50 69 163 NC1 NC2 NC3 NC4 NCTEST
1 VREF
201 202 GND0 GND1
203 204 NP_NC1 NP_NC2
47 133 183 77 12 48 184 78 71 72 121 122 196 193 8 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15
18 24 41 53 42 54 59 65 60 66 127 139 128 145 165 171 172 177 187 178 190 9 21 33 155 34 132 144 156 168 2 3 15 27 39 149 161 28 40 138 150 162 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

DDR2_DIMM_200P

Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title : DDR2 SO-DIMM1
Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 14 of 63

+3VS
+1.8V
+3VS
+1.8V
4,5,9,12,13,14,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,14,16,37,53

M_CLK_DDR4
C1501
10PF/50V
@
M_CLK_DDR#4

M_CLK_DDR3
C1502
10PF/50V
@
M_CLK_DDR#3

PN:12G025C22000=>12G025C22004
V2.0 ME

CON1501A

8,14,16 M_A_A[17:0]
M_A_A0 102
M_A_A1 101
M_A_A2 100
M_A_A3 99
M_A_A4 98
M_A_A5 97
M_A_A6 94
M_A_A7 92
M_A_A8 93
M_A_A9 91
M_A_A10 105
M_A_A11 90
M_A_A12 89
M_A_A13 116
M_A_A14 86
M_A_A17 84 85
M_A_A15 107
M_A_A16 106
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2
BA0 BA1

+3VS
R1501
10KOhm

8,16 M_CS#2 115
8,16 M_CS#3 30
8 M_CLK_DDR3 32
8 M_CLK_DDR#3 164
8 M_CLK_DDR4 166
8 M_CLK_DDR#4 79
8,16 M_CKE2 80
8,16 M_CKE3 113
8,14,16 M_A_CAS# 108
8,14,16 M_A_RAS# 109
8,14,16 M_A_WE# 198
S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

SA0 200
SA1 197
5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S
SCL SDA

8,16 M_ODT1 114
8,16 M_ODT3 119
ODT0 ODT1

8,14 M_A_DM[7:0]
M_A_DM0 10
M_A_DM1 26
M_A_DM2 52
M_A_DM3 67
M_A_DM4 130
M_A_DM5 147
M_A_DM6 170
M_A_DM7 185
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

8,14 M_A_DQS[7:0]
M_A_DQS0 13
M_A_DQS1 31
M_A_DQS2 51
M_A_DQS3 70
M_A_DQS4 131
M_A_DQS5 148
M_A_DQS6 169
M_A_DQS7 188
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

8,14 M_A_DQS#[7:0]
M_A_DQS#0 11
M_A_DQS#1 29
M_A_DQS#2 49
M_A_DQS#3 68
M_A_DQS#4 129
M_A_DQS#5 146
M_A_DQS#6 167
M_A_DQS#7 186
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

DQ0 5 M_A_DQ7
DQ1 7 M_A_DQ3
DQ2 17 M_A_DQ4
DQ3 19 M_A_DQ0
DQ4 4 M_A_DQ2
DQ5 6 M_A_DQ1
DQ6 14 M_A_DQ6
DQ7 16 M_A_DQ5
DQ8 23 M_A_DQ10
DQ9 25 M_A_DQ14
DQ10 35 M_A_DQ9
DQ11 37 M_A_DQ11
DQ12 20 M_A_DQ15
DQ13 22 M_A_DQ13
DQ14 36 M_A_DQ12
DQ15 38 M_A_DQ8
DQ16 43 M_A_DQ23
DQ17 45 M_A_DQ20
DQ18 55 M_A_DQ17
DQ19 57 M_A_DQ19
DQ20 44 M_A_DQ16
DQ21 46 M_A_DQ22
DQ22 56 M_A_DQ21
DQ23 58 M_A_DQ18
DQ24 61 M_A_DQ30
DQ25 63 M_A_DQ24
DQ26 73 M_A_DQ25
DQ27 75 M_A_DQ26
DQ28 62 M_A_DQ28
DQ29 64 M_A_DQ29
DQ30 74 M_A_DQ27
DQ31 76 M_A_DQ31
DQ32 123 M_A_DQ38
DQ33 125 M_A_DQ39
DQ34 135 M_A_DQ33
DQ35 137 M_A_DQ35
DQ36 124 M_A_DQ32
DQ37 126 M_A_DQ36
DQ38 134 M_A_DQ37
DQ39 136 M_A_DQ34
DQ40 141 M_A_DQ45
DQ41 143 M_A_DQ41
DQ42 151 M_A_DQ42
DQ43 153 M_A_DQ46
DQ44 140 M_A_DQ40
DQ45 142 M_A_DQ44
DQ46 152 M_A_DQ47
DQ47 154 M_A_DQ43
DQ48 157 M_A_DQ53
DQ49 159 M_A_DQ49
DQ50 173 M_A_DQ50
DQ51 175 M_A_DQ54
DQ52 158 M_A_DQ48
DQ53 160 M_A_DQ52
DQ54 174 M_A_DQ55
DQ55 176 M_A_DQ51
DQ56 179 M_A_DQ56
DQ57 181 M_A_DQ60
DQ58 189 M_A_DQ58
DQ59 191 M_A_DQ63
DQ60 180 M_A_DQ57
DQ61 182 M_A_DQ61
DQ62 192 M_A_DQ59
DQ63 194 M_A_DQ62

DDR_DIMM_200P

M_A_DQ[63..0] 8,14

+1.8V
C1503 2.2UF/6.3V
C1504 2.2UF/6.3V
C1505 2.2UF/6.3V
C1506 2.2UF/6.3V
C1507 2.2UF/6.3V
C1508 0.1UF/10V
C1509 0.1UF/10V
C1510 0.1UF/10V
C1511 0.1UF/10V
+3VS
C1512 2.2UF/6.3V
C1513 0.1UF/10V
14,16 M_VREF_DIMM1
C1514 2.2UF/6.3V
C1515 0.1UF/10V

CON1501B

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199
NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163
VREF 1
GND0 201
GND1 202
NP_NC1 203
NP_NC2 204
VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8
VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR_DIMM_200P

Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title : DDR2 SO-DIMM1
Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 15 of 63

+0.9VS +0.9VS 37,53

8,14,15 M_A_A[17:0]

+0.9VS

Follow A5 & W1 Design

+0.9VS L1401 120Ohm/100Mhz M_VREF_MCH 14,15 M_VREF_DIMM0 14,15 M_VREF_DIMM1 14,15

+1.8V C1416 1UF/6.3V M_VREF_MCH R1410 1KOhm R1411 1KOhm

M_A_A4 M_A_A6 M_A_A17 M_A_A7 M_CKE2 M_A_A11 M_A_A14 M_CKE3 — 56Ohm — RN1401A RN1401B RN1401C RN1401D RN1401E RN1401F RN1401G RN1401H — 0.1UF/25V — CN1401A CN1401D CN1401B CN1401C

+1.8V C1430 0.1UF/16V

8,14,15 M_A_RAS#

M_A_A3 M_A_RAS# M_A_A0 M_A_A5 M_A_A2 M_A_A8 M_A_A9 M_A_A12 — 56Ohm — RN1402A RN1402B RN1402C RN1402D RN1402E RN1402F RN1402G RN1402H — 0.1UF/25V — CN1402D CN1402A CN1402B CN1402C

+1.8V C1431 0.1UF/16V

M_ODT0 M_ODT2 M_CS#1 M_CS#0 M_CKE0 M_CKE1 — 56Ohm — RN1403A RN1403B RN1403C RN1403D RN1403E RN1403F RN1403G RN1403H — 0.1UF/25V — CN1403D CN1403A CN1403B CN1403C

8,14,15 M_CKE[0:3]

+1.8V C1432 0.1UF/16V

8,14,15 M_CS#[0:3]

8,14,15 M_A_WE#

M_ODT1 M_A_A13 M_CS#2 M_A_A15 M_A_A10 M_A_A1 M_A_A16 — 56Ohm — RN1404A RN1404B RN1404C RN1404D RN1404E RN1404F RN1404G RN1404H — 0.1UF/25V — CN1404D CN1404A CN1404B CN1404C

+1.8V C1433 0.1UF/16V

8,14,15 M_ODT[0:3]

8,14,15 M_A_CAS#

M_ODT3 M_CS#3 — 56Ohm — RN1405A RN1405B RN1405C RN1405D — 0.1UF/25V — CN1405D CN1405A CN1405B CN1405C

V1.1 EMI

+0.9VS C1444 0.1UF/16V N/A

+1.8V C1443 C1442 C1441 C1440 C1439 C1438 C1437 C1436 C1435 C1434 0.1UF/16V N/A

V2.0 EMI

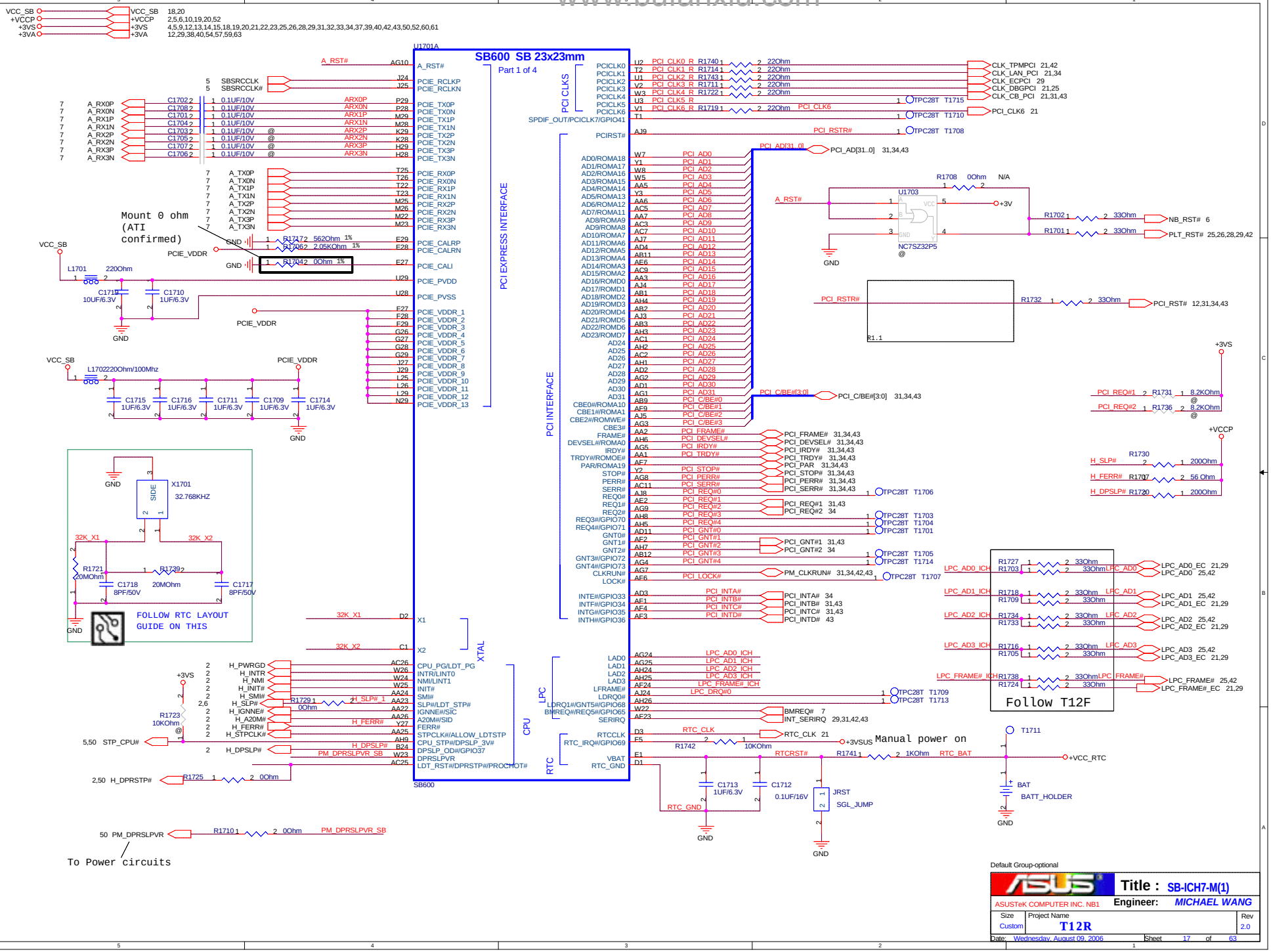
Default Group-optional

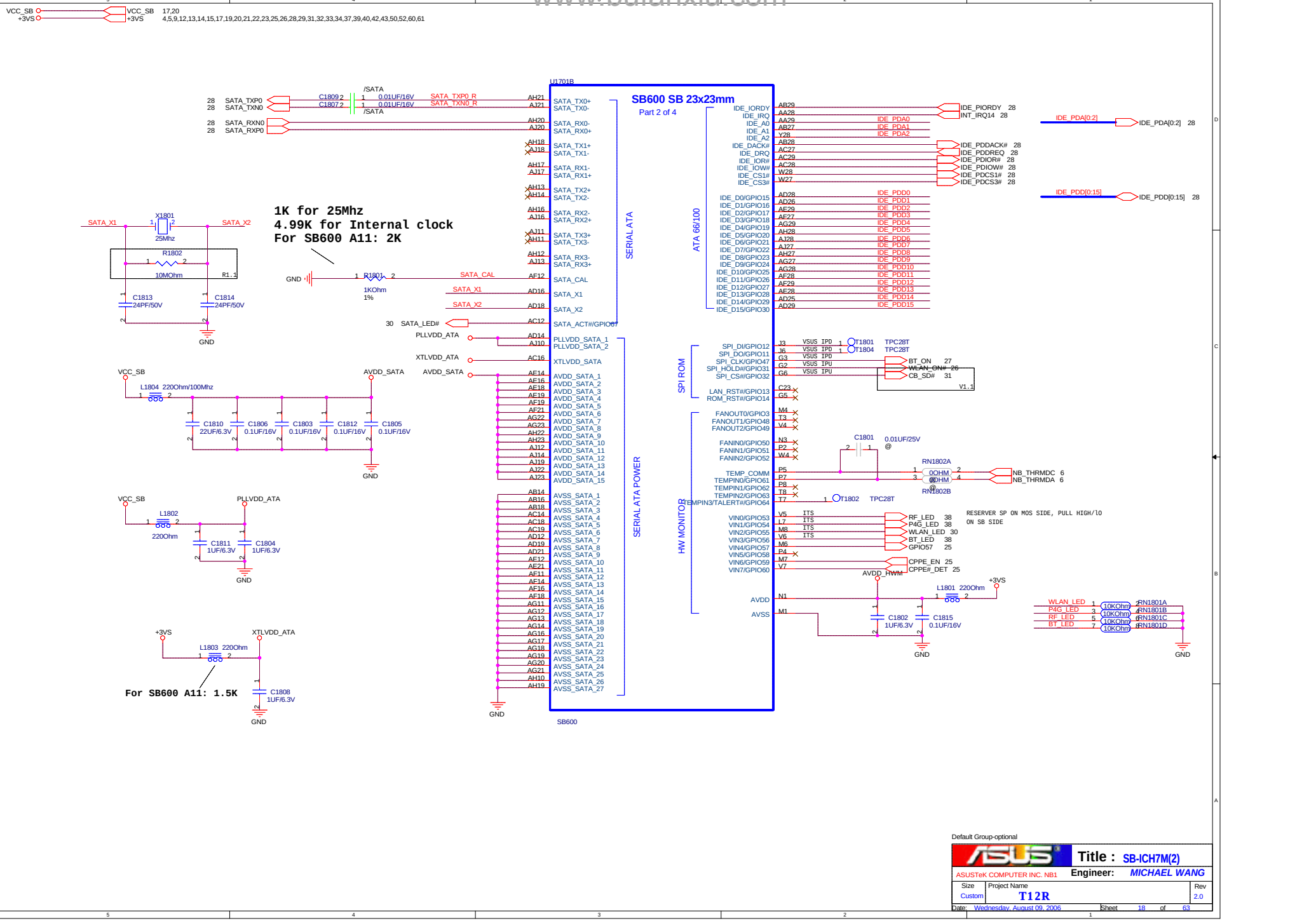
Title : DDR2 TERMINATION

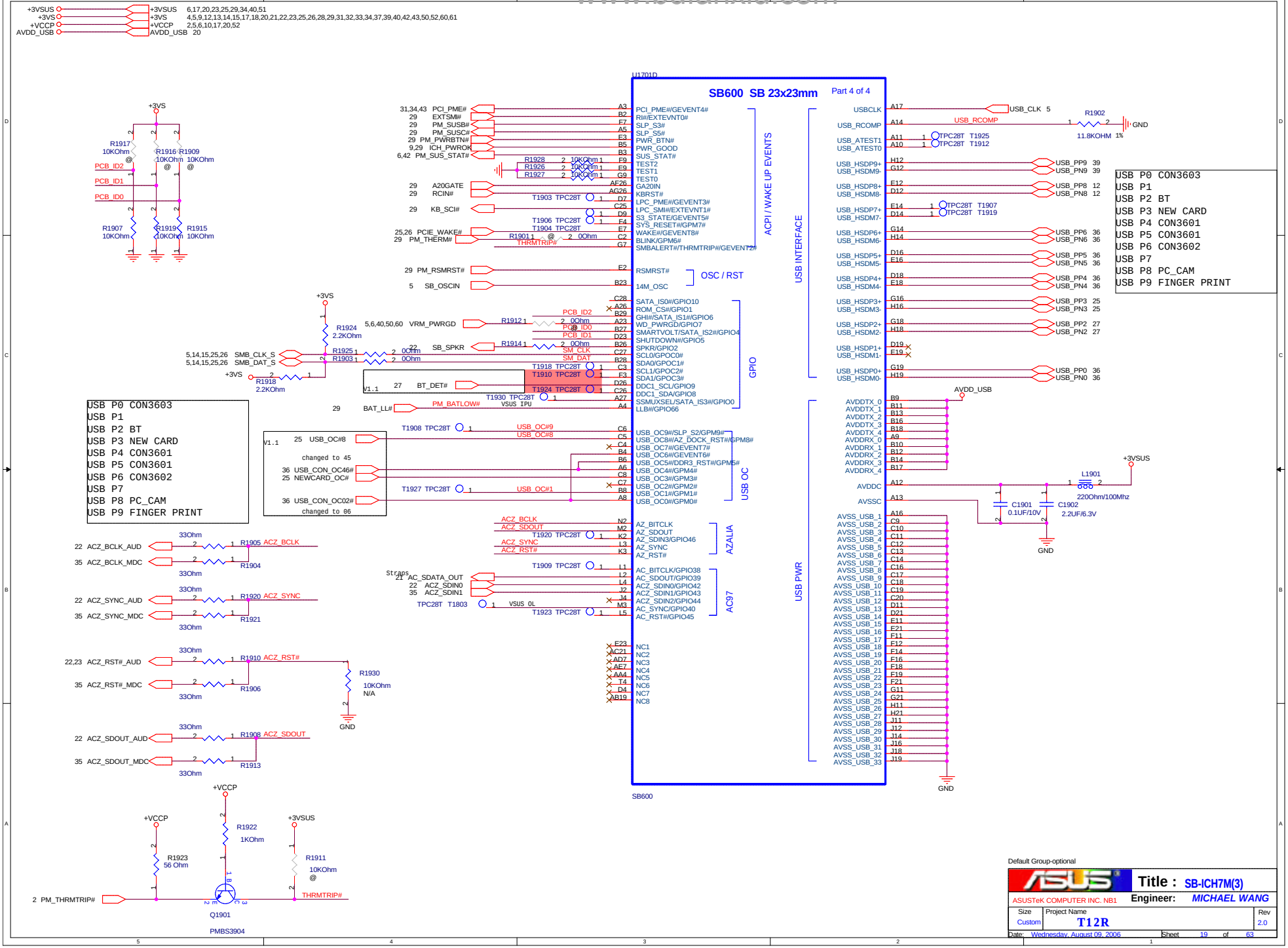
ASUSTeK COMPUTER INC. NB1 Engineer: MICHAEL WANG

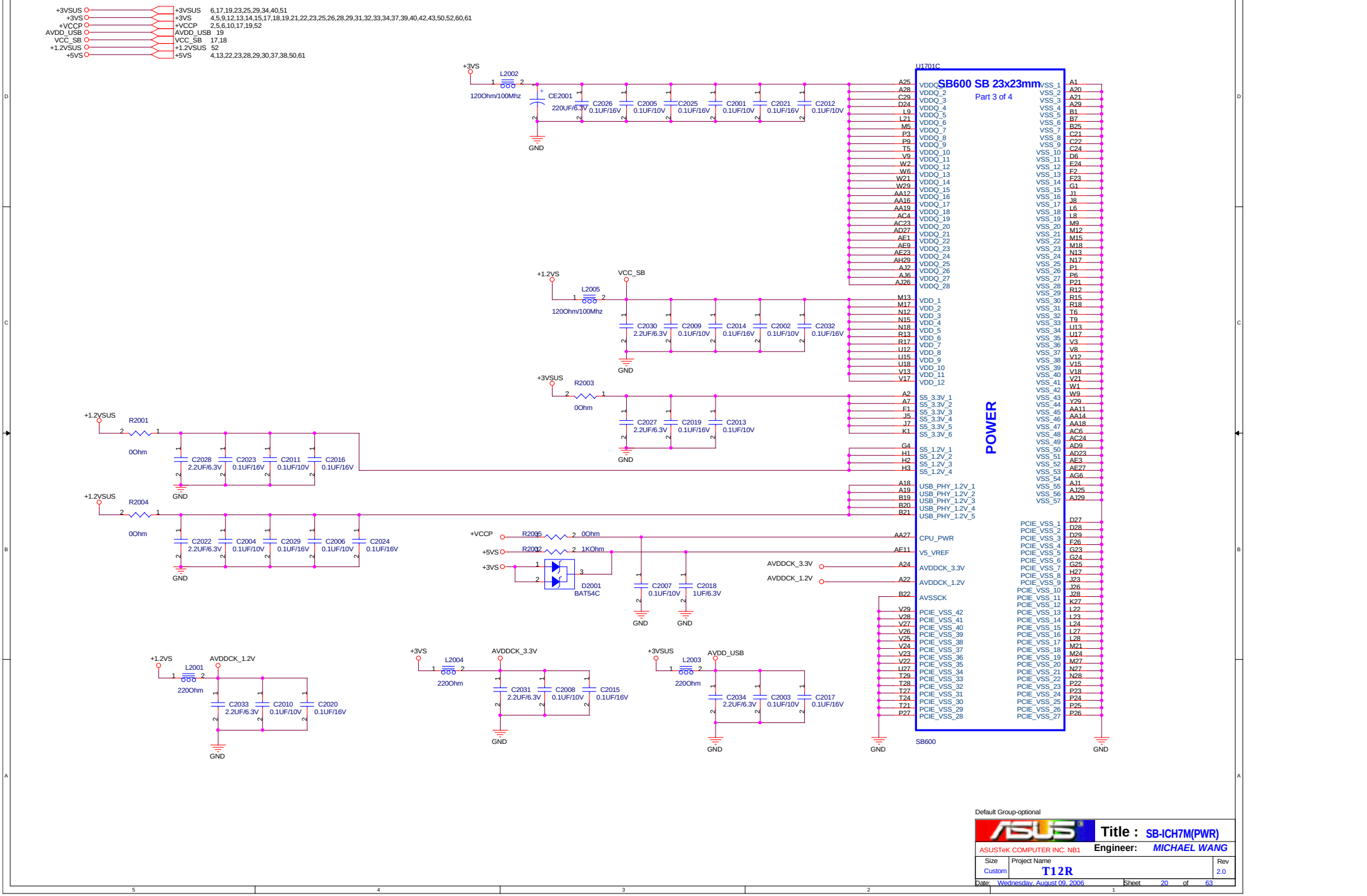
Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 16 of 63



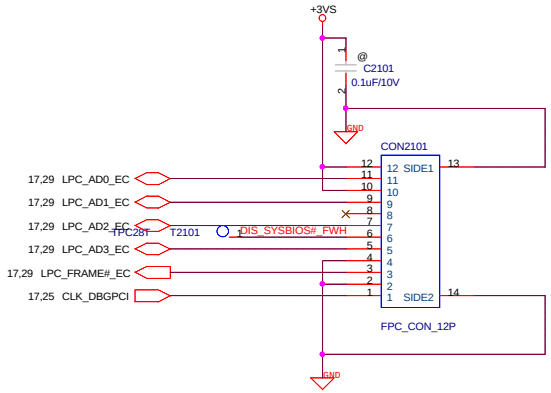






Default Group-optional

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(PWR)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 20 of 63	



19 AC_SDATA_OUT — R2101 1 — 2 2.2KOhm — +3VS

Ignore Debug Straps (Default)

17 RTC_CLK — 1 — TPC28T T2102

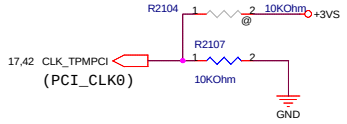
RTC_CLK has 15K internal pull up (Default): Uses Internal RTC

17,31,43 CLK_CB_PCI — R2106 2 — 1 10KOhm — GND

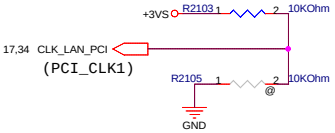
PCI_CLK4(CLK_CB_PCI) Pull-Low uses external 48Mhz(Default)

17 PCI_CLK6 — R2102 2 — 1 10KOhm — GND

PCI_CLK6 Pull-Low uses Intel P4(Default)



(PCI_CLK0)



(PCI_CLK1)

PCI_CLK0	PCI_CLK1	(ROM Type)	
H	H	PCI ROM	
H	L	SPI ROM	
L	H	LPC ROM	(Default)
L	L	FWH ROM	

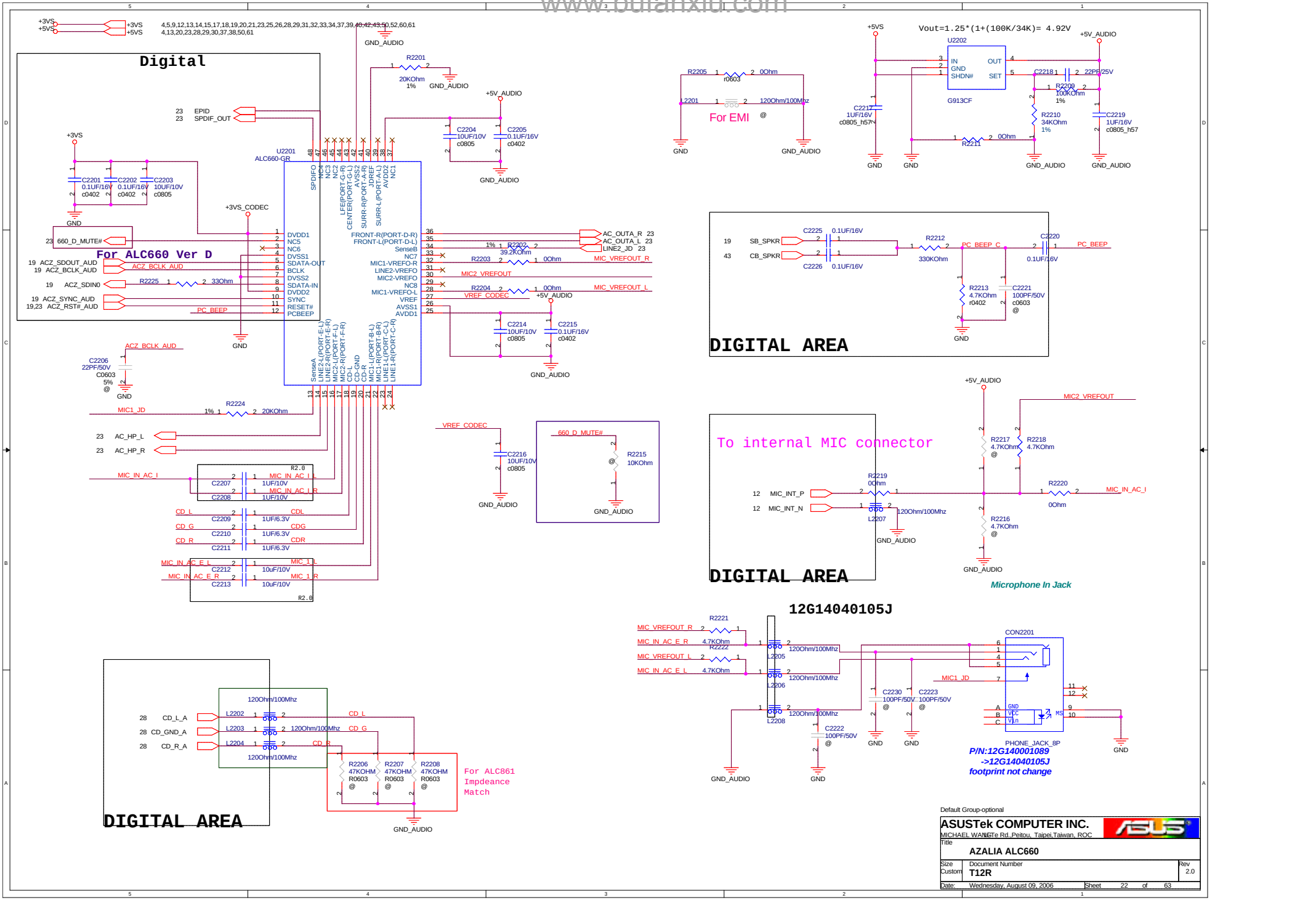
Default Group-optional

Title : BLOCK DIAGRAM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 21 of 63



Default Group-optional

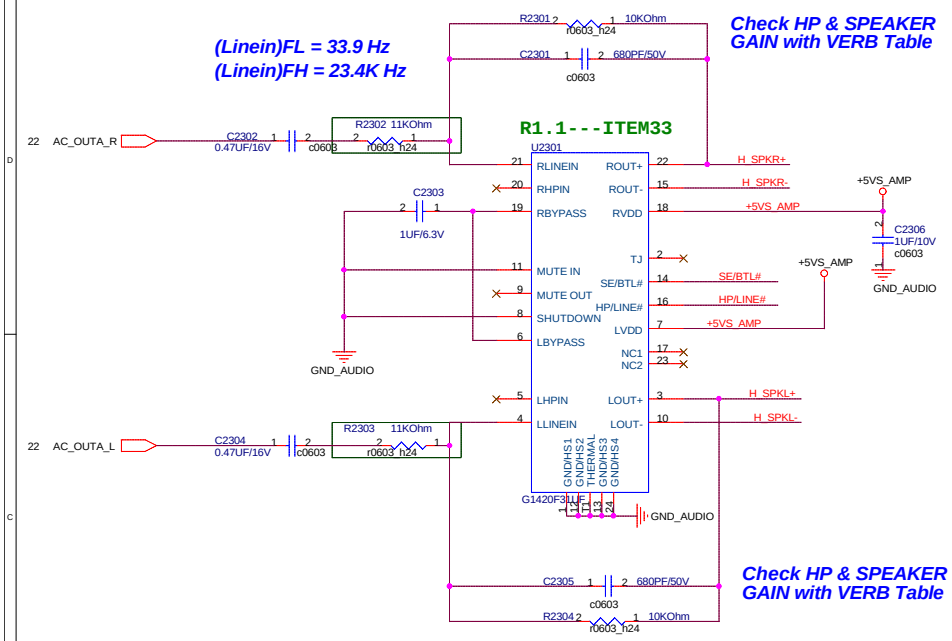
ASUSTek COMPUTER INC.

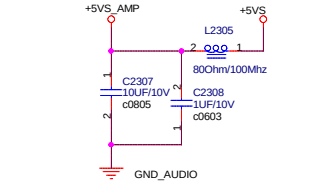
MICHAEL WANG 15 Te Rd.,Peitou, Taipei,Taiwan, ROC

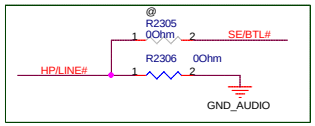
Title: **AZALIA ALC660**

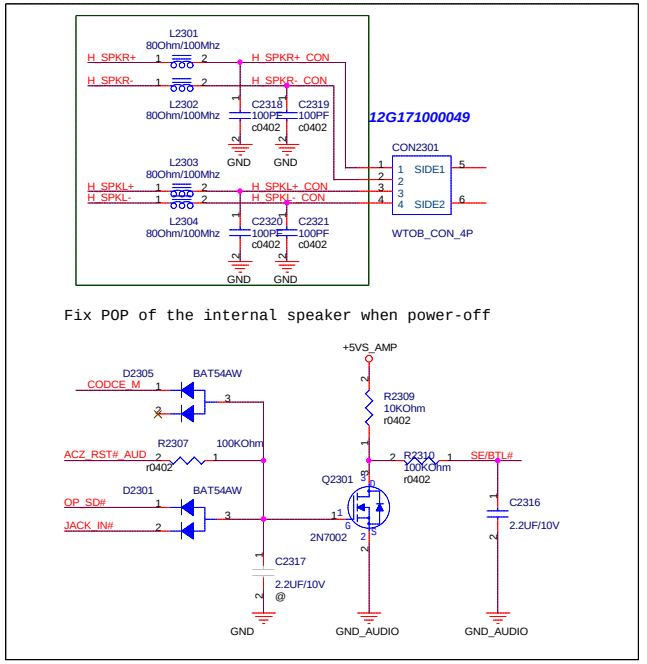
Size	Document Number	Rev
Custom	T12R	2.0

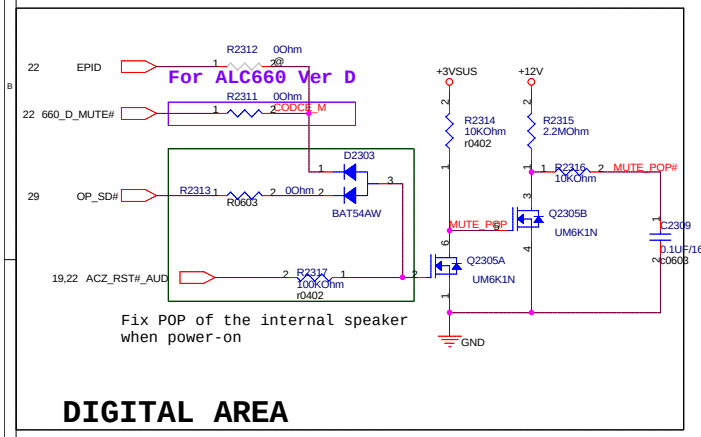
Date: Wednesday, August 09, 2006 Sheet 22 of 63





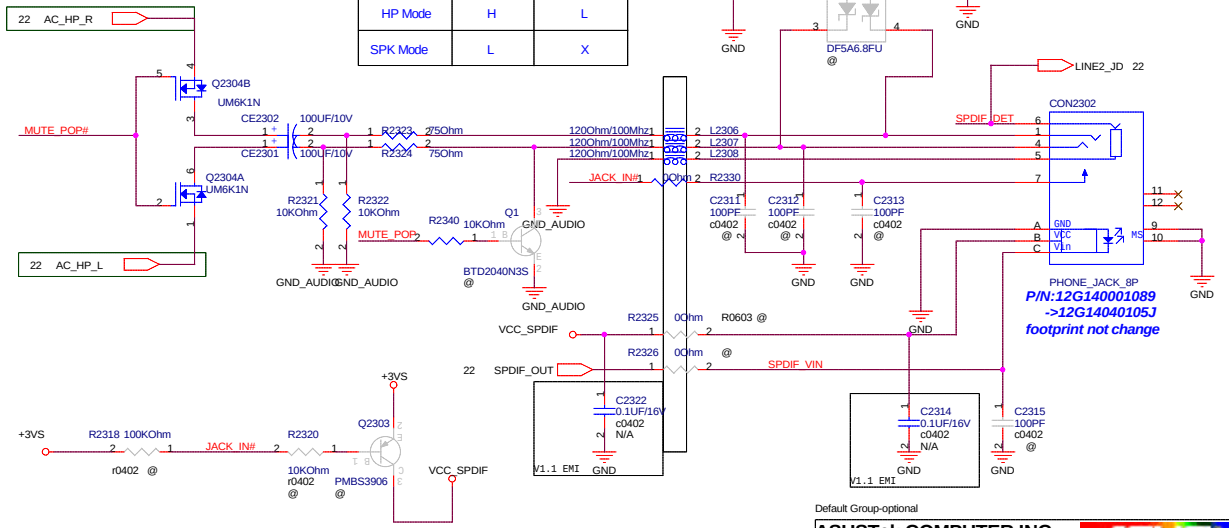






JACK_IN

	SE/BTL#	SPDIF_DET
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X



+3VS	+3VS	4,5,9,12,13,14,15,17,18,19,20,21,22,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS	+5VS	4,13,20,22,28,29,30,37,38,50,61
+5V_AUDIO	+5V_AUDIO	22
+3VSUS	+3VSUS	6,17,19,20,25,29,34,40,51
+12V	+12V	37,54,61

Default Group-optional

ASUSTek COMPUTER INC.
MICHAEL WANG 15 Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: **Audio AMP**

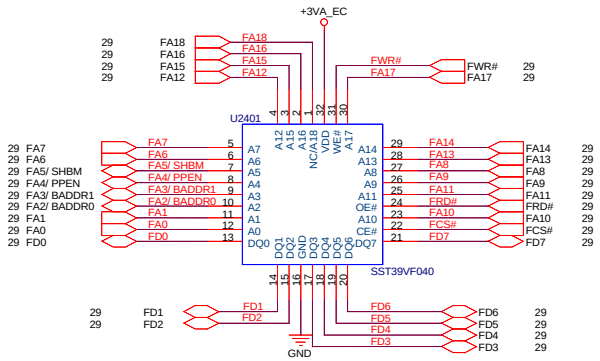
Size	Document Number	Rev
Custom	T12R	2.0

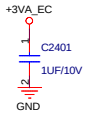
Date: Wednesday, August 09, 2006 Sheet 23 of 63

+3VA_EC +3VA_EC 26,29

ISA ROM

0.01A

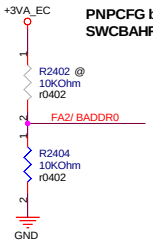


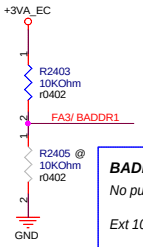


EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

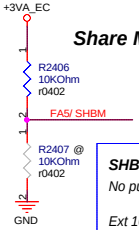




BADDR[1:0]

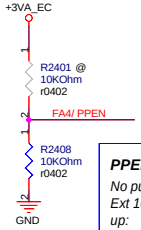
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

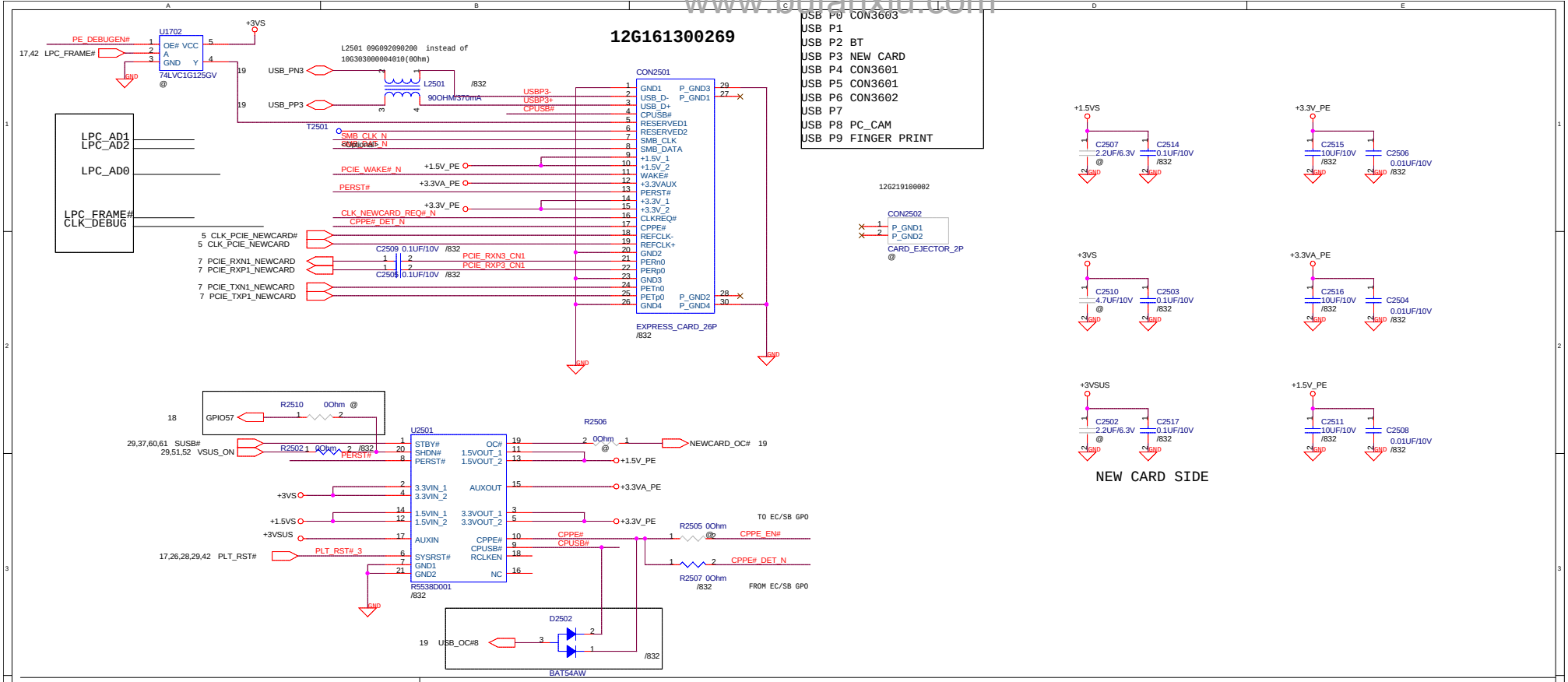


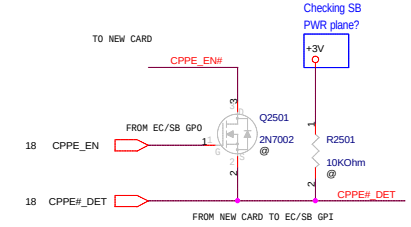
PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

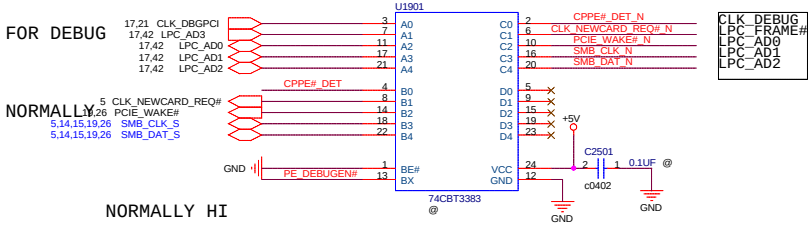
Default Group-optional

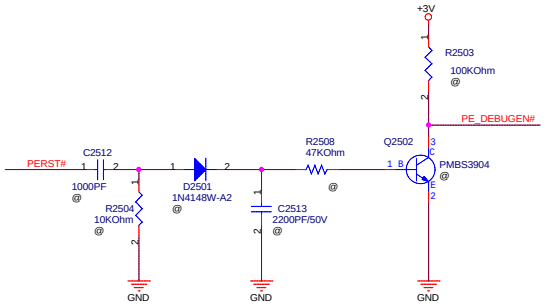
ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 24 of 63	



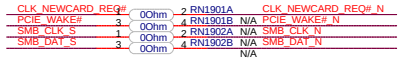


New card debug function





Reserve to remove PCIE debug function



Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	Engineer: MICHAEL WANG
Size: Custom	Title : New Card	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 25 of 63	

+3V +3V 17,25,27,31,35,37,42,43,44,61
+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.5VS +1.5VS 25,37,54
+3VA_EC +3VA_EC 24,29

12G030000526

CLKREQ#(output) CLOCK REQUEST could be pull low

CON2602

19,25 PCIE_WAKE#	1	WAKE#	3.3V_1	2	
27 CH_DATA	3	Reserved1	GND7	4	
27 CH_CLK	5	Reserved2	1.5V_1	6	
5 CLK_MINICARD_REQ#	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	
5 CLK_PCIE_MINICARD#	11	REFCLK-	UIM_CLK	12	
5 CLK_PCIE_MINICARD	13	REFCLK+	UIM_RESET	14	
	15	GND2	UIM_VPP	16	
	17	Reserved/UIM_C8	GND8	18	
	19	Reserved/UIM_C4W_DISABLE#		20	WIRELESS_LAN_ON/OFF#
	21	GND3	PERST#	22	PLT_RST# 17,25,28,29,42
7 PCIE_RXN0_MINICARD	23	PERn0	+3.3Vaux	24	
7 PCIE_RXP0_MINICARD	25	PERp0	GND9	26	
	27	GND4	1.5V_2	28	
	29	GND5	SMB_CLK	30	R2603 1 2 0Ohm @ SMB_CLK_S 5,14,15,19,25
7 PCIE_TXN0_MINICARD	31	PETn0	SMB_DATA	32	R2601 1 2 0Ohm @ SMB_DAT_S 5,14,15,19,25
7 PCIE_TXP0_MINICARD	33	PETp0	GND10	34	
	35	GND6	USB_D-	36	
	37	Reserved3	USB_D+	38	
	39	Reserved4	GND11	40	
	41	Reserved5	LED_WWAN#	42	
	43	Reserved6	LED_WLAN#	44	WL_LED# 1 T260 PC28t
	45	Reserved7	LED_WPAN#	46	
	47	Reserved8	1.5V_3	48	
	49	Reserved9	GND12	50	
	51	Reserved10	3.3V_2	52	
	53	GND13	NP_NC2	56	
	54	GND14	NP_NC1	55	

MINI_CARD_LATCH_52P

GND GND

+3VS
C2602 0.1UF/10V GND
C2605 0.1UF/10V GND
C2606 10UF/6.3V GND
3.003V~3.597V
Max= 750 mA

+1.5VS
C2608 0.1UF/10V GND
C2601 0.1UF/10V GND
C2603 10UF/6.3V GND
1.425V~1.575V
Max= 375 mA

+3V
C2607 0.1UF/10V GND
C2604 1UF/6.3V GND
3.003V~3.597V
Max= 250 mA

CON2601
MINI_PCI_LATCH_5P
MINI PCI-E LATCH 5P
GND

12G162210052

+3VA_EC
PULL HIGH ON SB SIDE AND IT INTERNAL PULL HIGH
INTERNAL PU
R2602 47KOhm @
WIRELESS_LAN_ON/OFF#
18 WLAN_ON#
Q2601 2N7002
GND

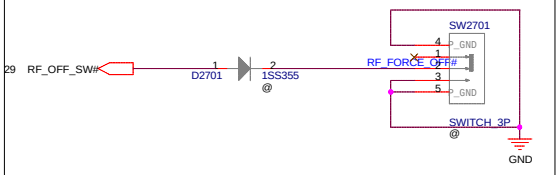
Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : MINI PCI	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 26 of 63	

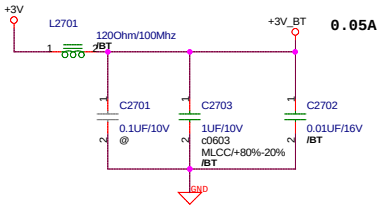
+3V +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

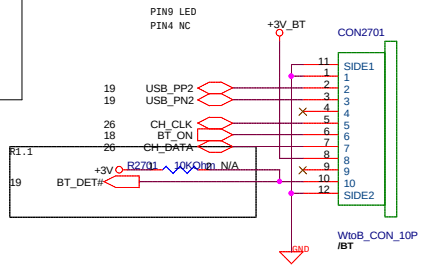
RESERVED RF SWITCH



Bluetooth Module CN



12G17101010L



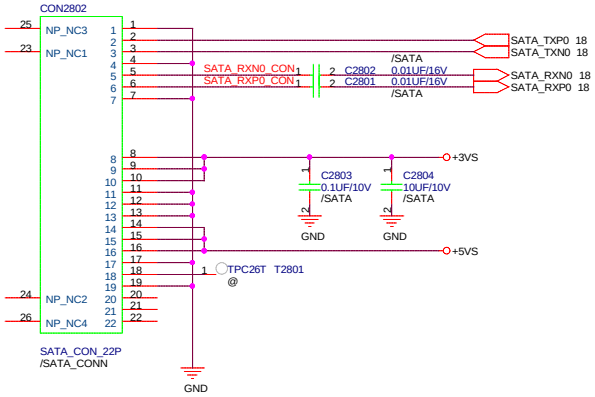

```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
```

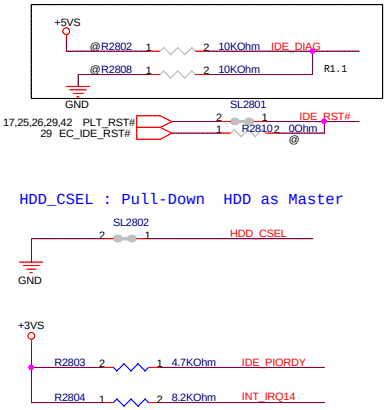
Default Group-optional

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 27 of 63	

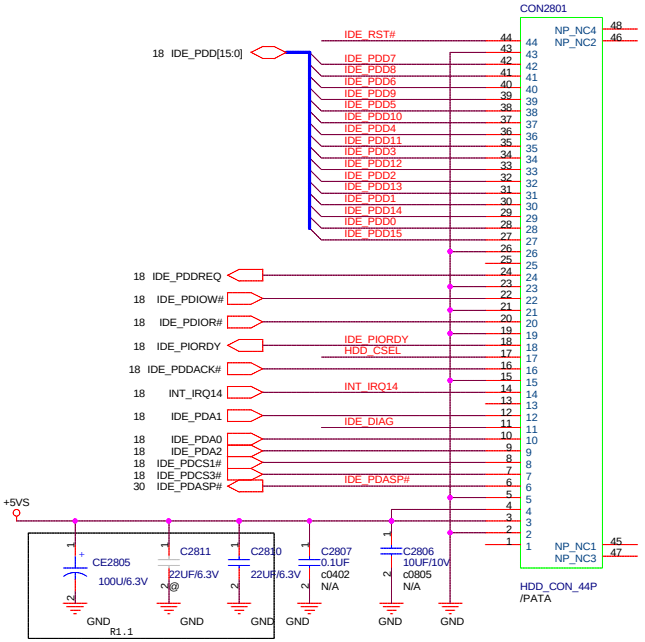
+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS +5VS 4,13,20,22,23,29,30,37,38,50,61

12G15100022F





12G161520447

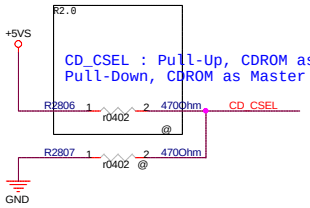


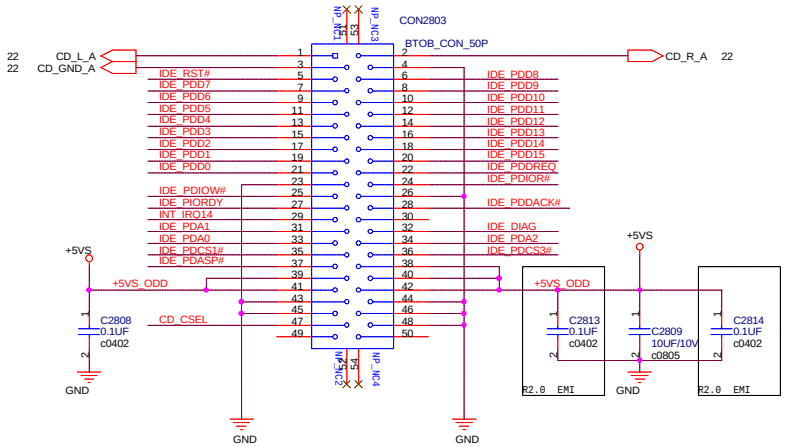
SATA HDD

PATA HDD

CD-ROM

12G161210504





Default Group-optional

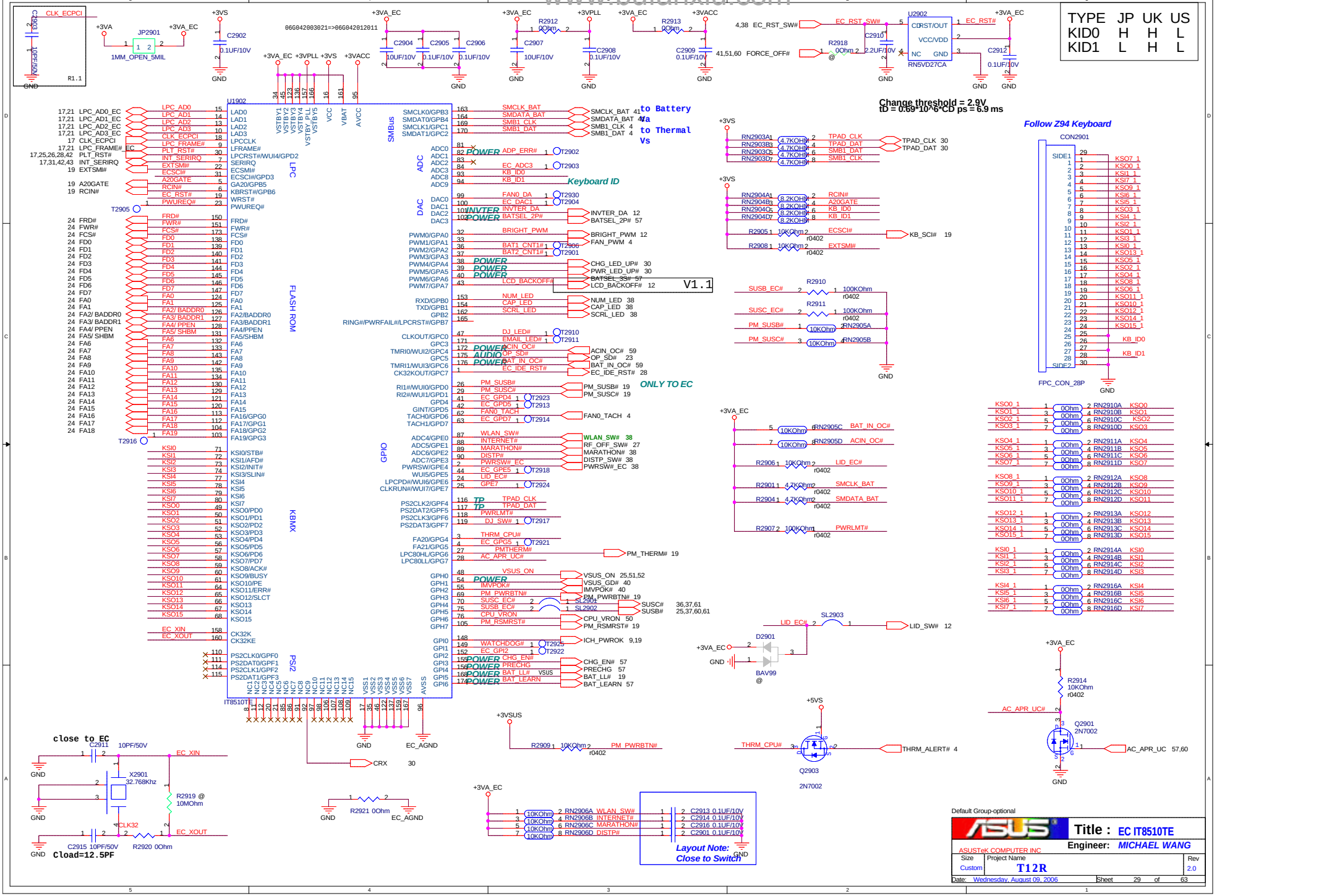
ASUSTeK COMPUTER INC. NB1

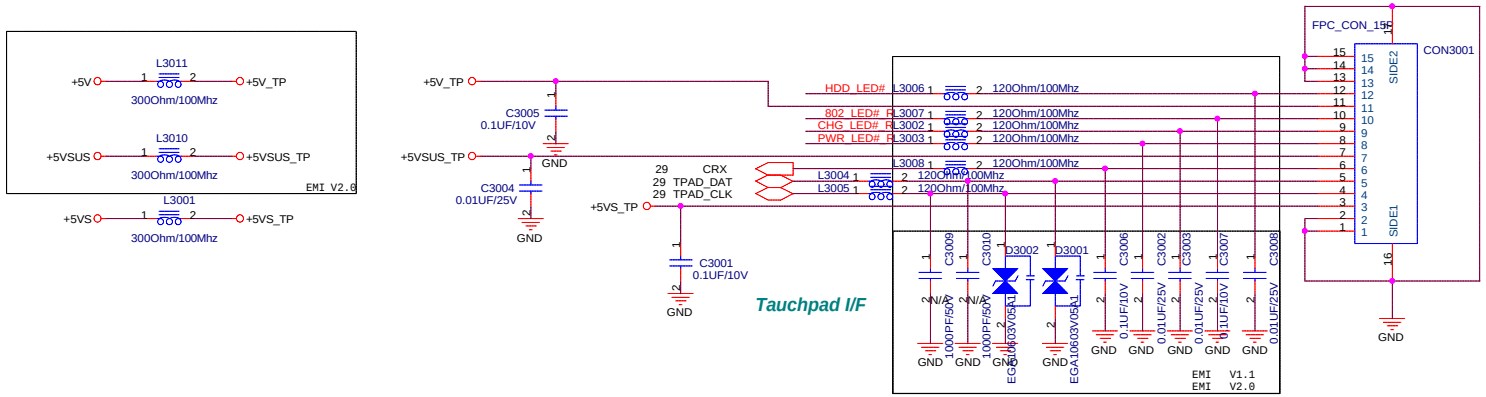
Title : PATA-SATA & ODD

Engineer:

Size	Project Name	Rev
Custom	T12R	2.0

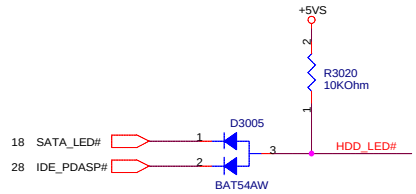
Date: Wednesday, August 09, 2006 Sheet 28 of 63



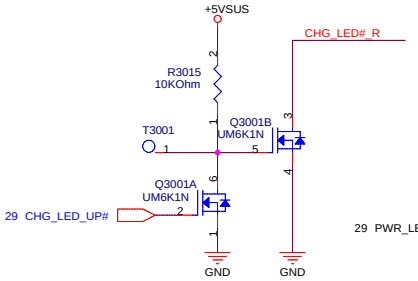


Touchpad

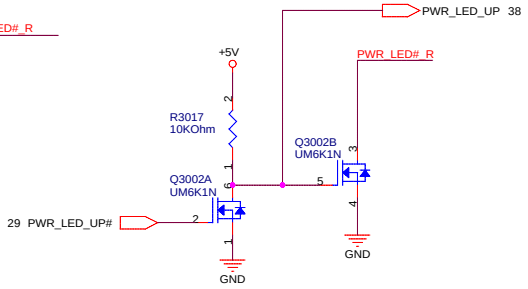
HDD LED



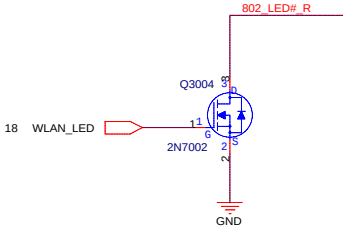
CHARGE LED



POWER LED



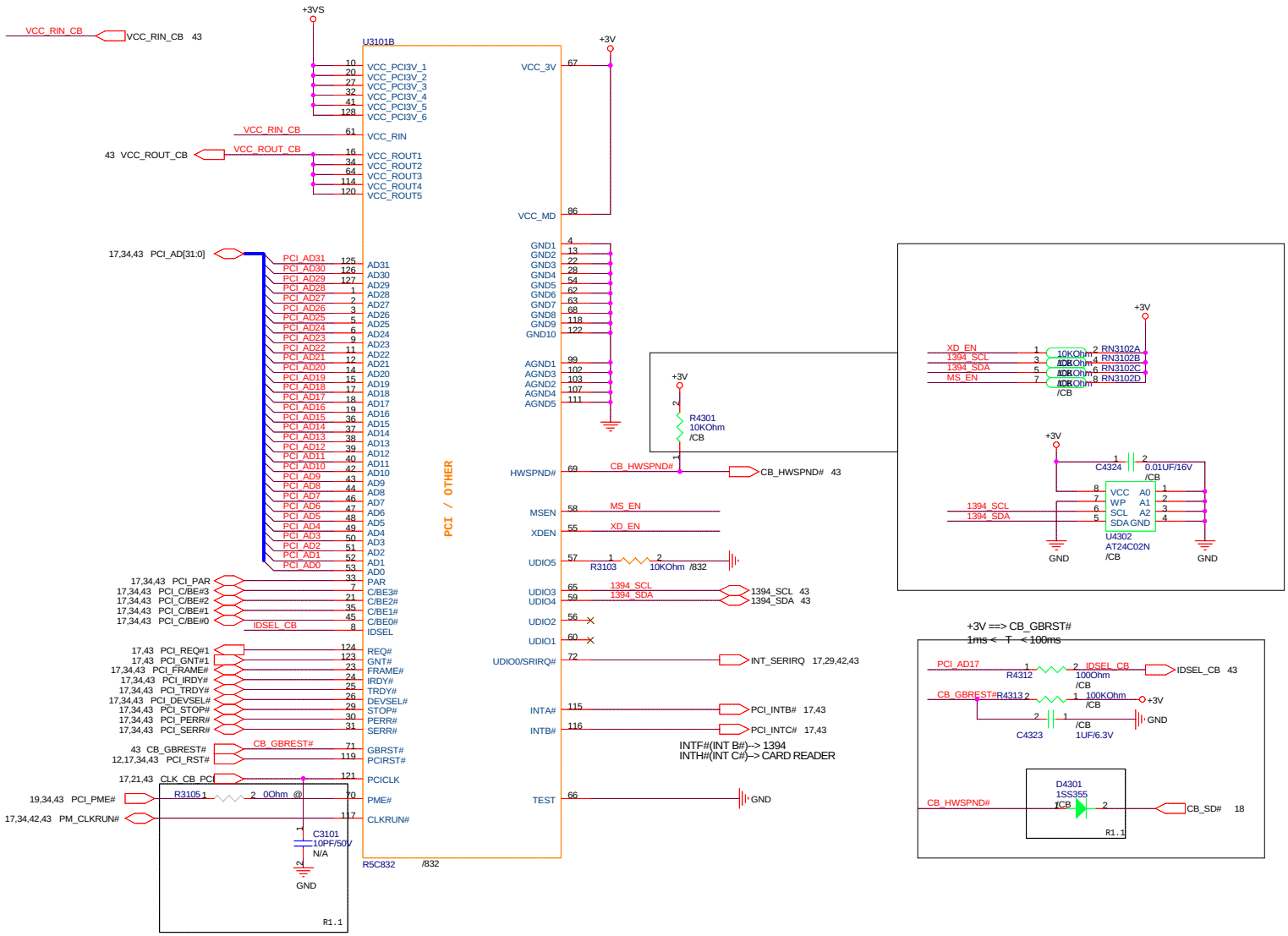
WLAN LED



Default Group-optional

Title : EC IT8510TE(2/2)		
Engineer: MICHAEL WANG		
ASUSTeK COMPUTER INC		
Size: A3	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 30 of 63	

+3V +3V 17,25,26,27,35,37,42,43,44,61
+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,32,33,34,37,39,40,42,43,50,52,60,61



Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title :CARD1394-R5C832(1)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 31 of 63

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,33,34,37,39,40,42,43,50,52,60,61

U3101A

IEEE1394/SD

AVCC_PHY3V_1 98
AVCC_PHY3V_2 106
AVCC_PHY3V_3 110
AVCC_PHY3V_4 112

+3VS_832
C3202 0.01UF/16V /CB
C3203 0.1UF/10V /CB
C3204 10UF/10V /CB
L3203 120Ohm/100Mhz /CB
+3VS
GND

TPBIAS0 113 TPBIAS0 TPBIAS0 44

44 XIN_1394 XIN_1394 94 XI
44 XOUT_1394 XOUT_1394 95 XO
44 1394_FIL 1394_FIL 96 FIL0
44 1394_REXT 1394_REXT 101 REXT
44 1394_VREF 1394_VREF 100 VREF

TPBN0 104 TPB0- TPB0- 44
TPBP0 105 TPB0+ TPB0+ 44
TPAN0 108 TPA0- TPA0- 44
TPAP0 109 TPA0+ TPA0+ 44

MDIO17 87 MDIO17_XDDAT7 33,43
MDIO16 92 MDIO16_XDDAT6 33,43
MDIO15 89 MDIO15_XDDAT5 33,43
MDIO14 91 MDIO14_XDDAT4 33,43
MDIO13 90 MDIO13_SD/MS/XDDAT3 33,43
MDIO12 93 MDIO12_SD/MS/XDDAT2 33,43
MDIO11 81 MDIO11_SD/MS/XDDAT1 33,43
MDIO10 82 MDIO10_SD/MS/XDDAT0 33,43
MDIO05 75 MDIO05_XDWP# 33,43
MDIO08 88 MDIO08_SDCMD_MSBS_XDWE# 33,43
MDIO19 83 MDIO19_XDALE 33,43
MDIO18 85 MDIO18_XDCLE 33,43
MDIO02 78 MDIO02_XDCE# 33,43
MDIO03 77 MDIO03_SDWP_XDR/B# 33,43
MDIO00 80 MDIO00_SDCD#_XDCD# 33,43
MDIO01 79 MDIO01_MSCD#_XDCD# 33,43
MDIO09 84 MDIO09_SD/MSCLK_XDRE# 33,43
MDIO04 76 MDIO04_SD/MS/XDPWR 33,43
MDIO06 74 MDIO06 T3201 /832 TPC26T
MDIO07 73 GND

SHIELD GND
R3207 r0402 0Ohm
/832

97 RSV

R5C832 /832

Closed to 1394 Controller

TPBIAS0
R4405 56Ohm /CB
R4406 56Ohm /CB
C4424 0.01UF/16V /CB
C4425 0.33UF/16V /CB
GND
TPA0+
TPA0-

TPB0-
TPB0+
R4407 56Ohm /CB
R4408 56Ohm /CB
5.1KOhm /CB R4409
270PF/50V /CB C4426
GND

Closed to 1394 Connector

TPB0+ LTPB0+ L3201 90OHM/370mA /CB
TPB0- LTPB0-
TPA0+ LTPA0+ L3202 90OHM/370mA /CB
TPA0- LTPA0-

CON4401
LTPB0-
LTPB0+
LTPA0-
LTPA0+
P_GND1 P_GND3 P_GND4 P_GND2
IEEE1394_CON_4P /CB
GND

Closed to 1394 Controller

XIN_1394 X4401 XOUT_1394
C4422 15PF/50V /CB
24.576Mhz /CB
C4423 15PF/50V /CB
GND

Closed to 1394 Controller

1394_FIL C4407 0.01UF/25V /CB GND
1394_REXT R4403 10KOhm /CB GND
1394_VREF C4412 0.01UF/25V /CB GND

Default Group-optional

Title : CARD1394-R5C832(2)
ASUSTeK COMPUTER INC. NB1
Engineer: MICHAEL WANG
Size: Custom
Project Name: T12R
Rev: 2.0
Date: Wednesday, August 09, 2006
Sheet 32 of 63

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

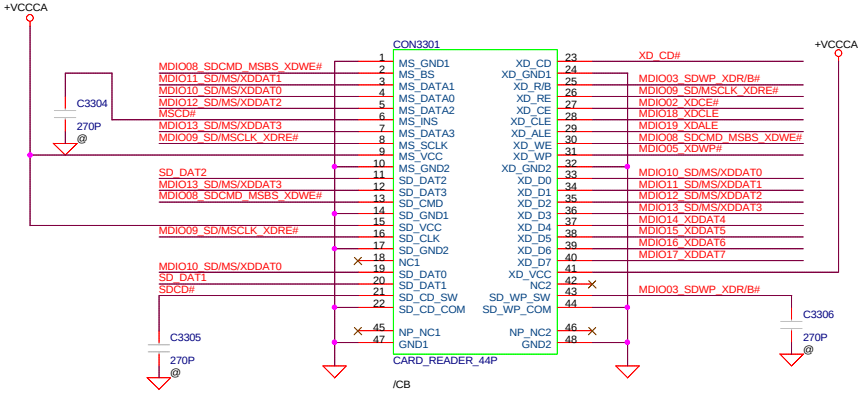
SD/MMC/MS/MS-PRO Card Reader Socket

32,43 MDIO17_XDDAT7 — MDIO17_XDDAT7
32,43 MDIO16_XDDAT6 — MDIO16_XDDAT6
32,43 MDIO15_XDDAT5 — MDIO15_XDDAT5
32,43 MDIO14_XDDAT4 — MDIO14_XDDAT4
32,43 MDIO13_SD/MS/XDDAT3 — MDIO13_SD/MS/XDDAT3
32,43 MDIO12_SD/MS/XDDAT2 — MDIO12_SD/MS/XDDAT2
32,43 MDIO11_SD/MS/XDDAT1 — MDIO11_SD/MS/XDDAT1
32,43 MDIO10_SD/MS/XDDAT0 — MDIO10_SD/MS/XDDAT0

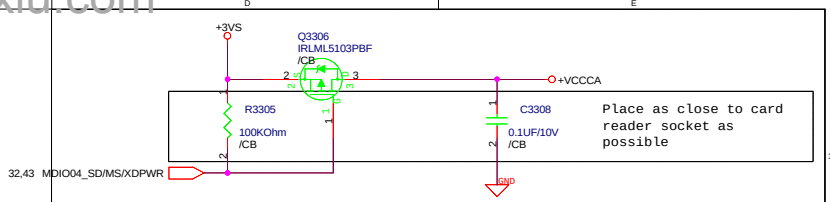
32,43 MDIO05_XDWP# — MDIO05_XDWP#
32,43 MDIO08_SDCMD_MSBS_XDWE# — MDIO08_SDCMD_MSBS_XDWE#
32,43 MDIO19_XDALE — MDIO19_XDALE
32,43 MDIO18_XDCLE — MDIO18_XDCLE
32,43 MDIO02_XDCE# — MDIO02_XDCE#

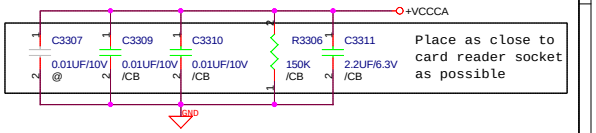
32,43 MDIO03_SDWP_XDR/B# — MDIO03_SDWP_XDR/B#
32,43 MDIO00_SDCD#_XDCD# — MDIO00_SDCD#_XDCD#
32,43 MDIO01_MSCD#_XDCD# — MDIO01_MSCD#_XDCD#
32,43 MDIO09_SD/MSCLK_XDRE# — MDIO09_SD/MSCLK_XDRE#

12G340004402

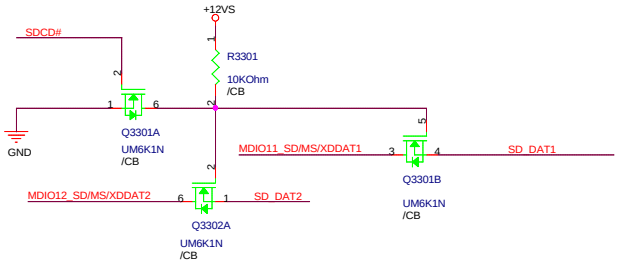


+12VS +3VS — +12VS +3VS — 12,37,61 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61

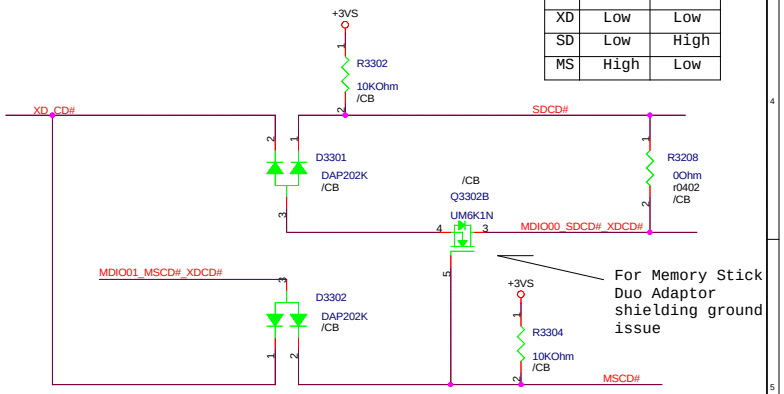




To coorect the problem when MS Duo adaptor is in use.

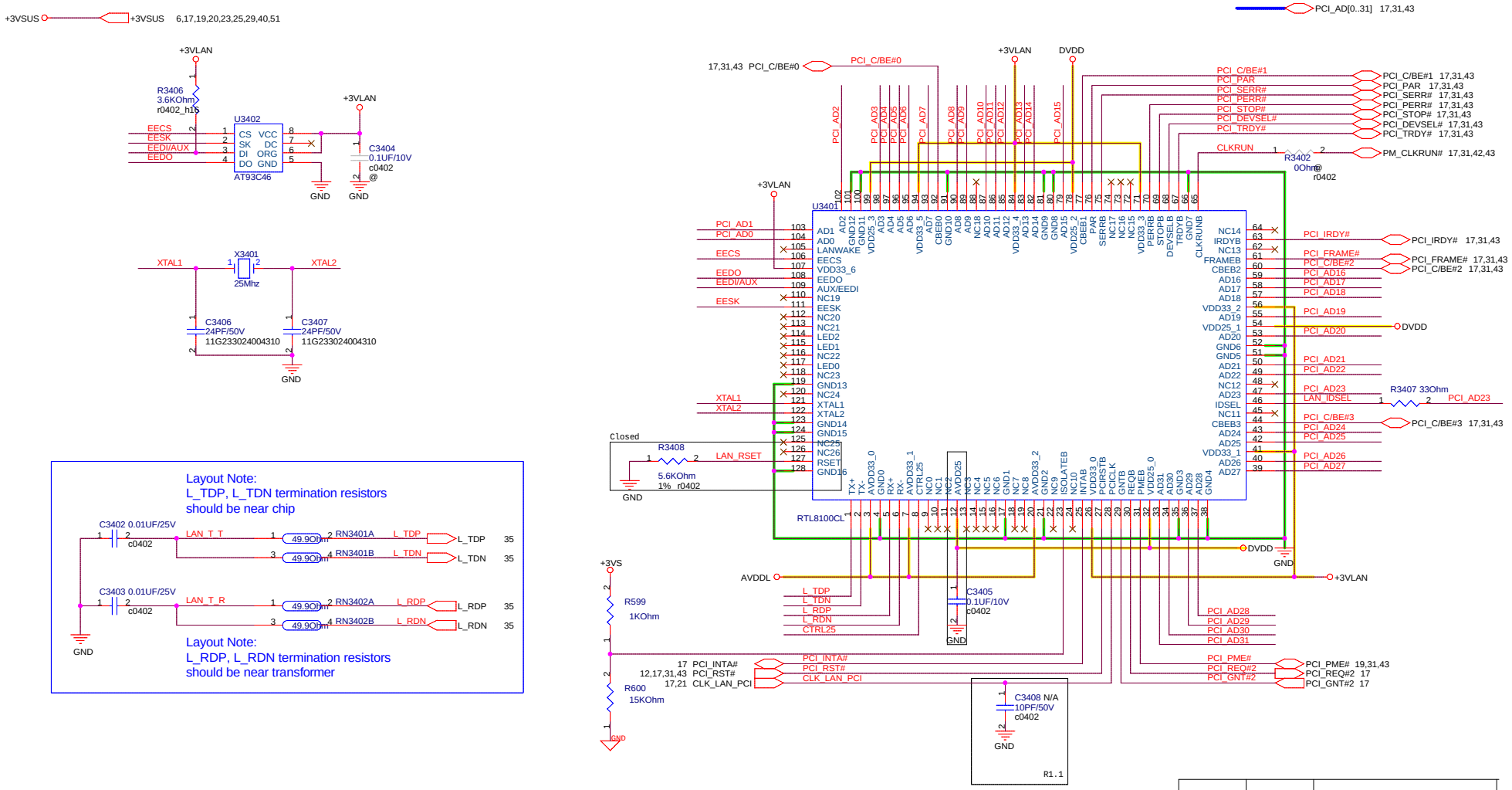


Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	Engineer: MICHAEL WANG
Size: Custom	Title : CardReader	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 33 of 63	



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/ 84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

<65mA 3.3V
<25mA 2.5V

Default Group-optional

ASUSTeK COMPUTER INC

Title : LAN_RTL8100CL

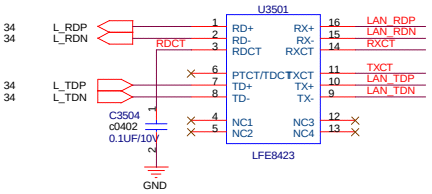
Engineer: MICHAEL WANG

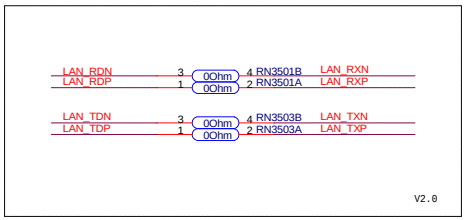
Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 34 of 63

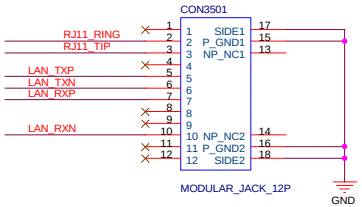
+3V +3V 17,25,26,27,31,37,42,43,44,61

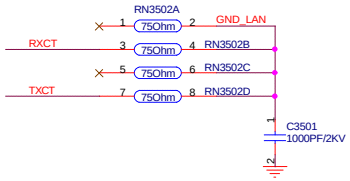
LAN PORT





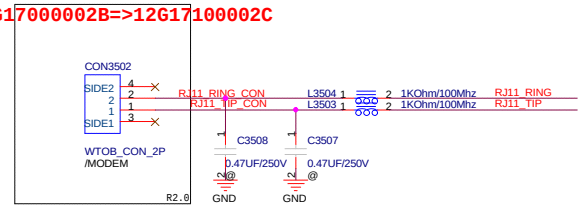
12G142111120



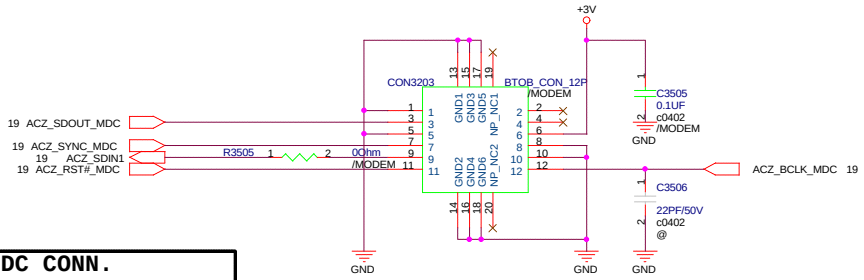


MDC CONNECTOR

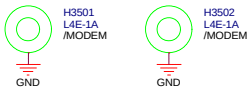
12G17000002B=>12G17100002C



12G161200124



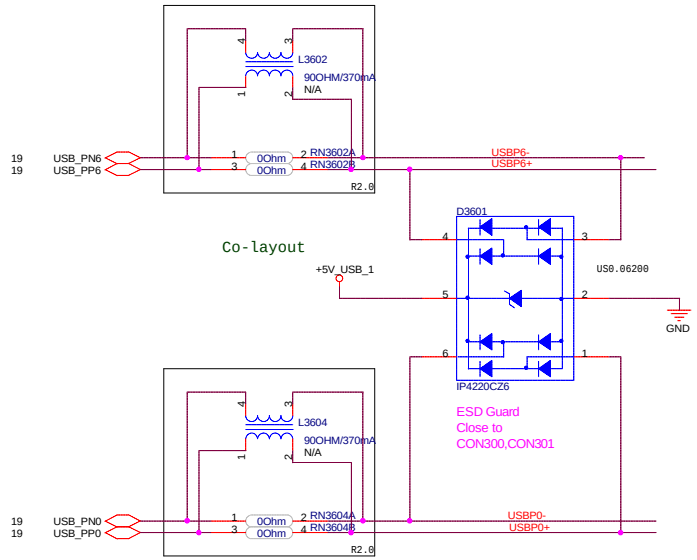
For MDC CONN.

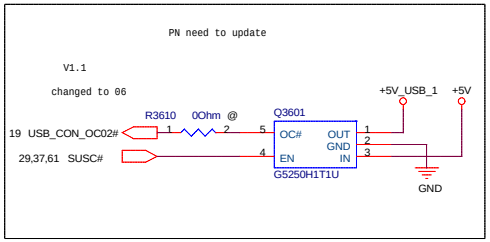


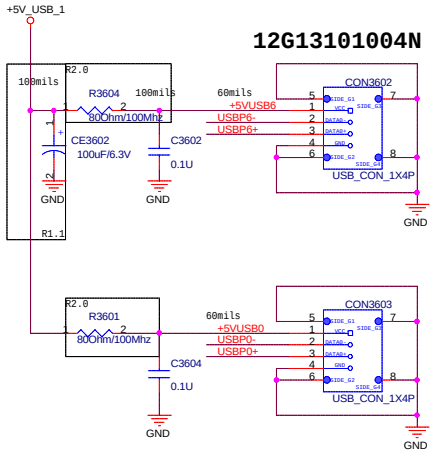
Must change to 13GN7510M270

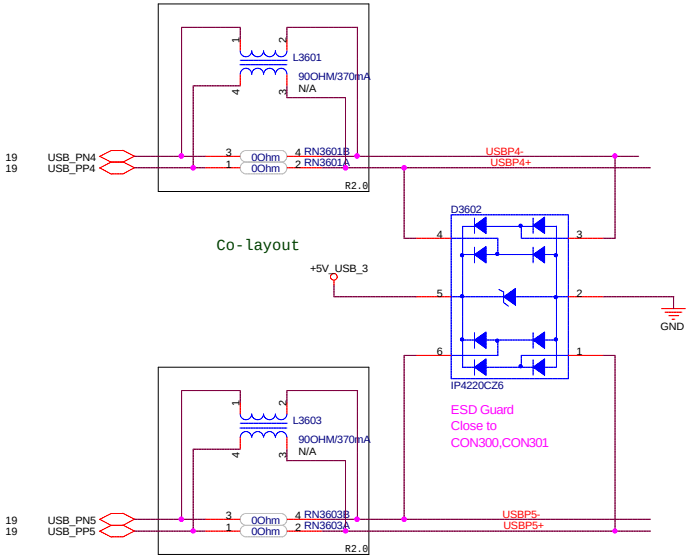
Default Group-optional

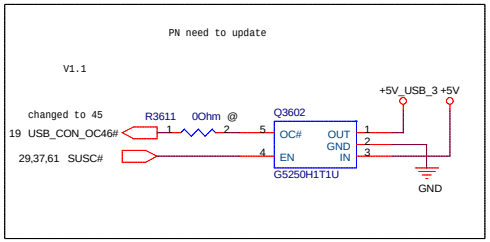
ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 35 of 63	

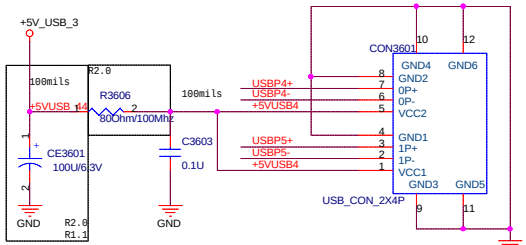






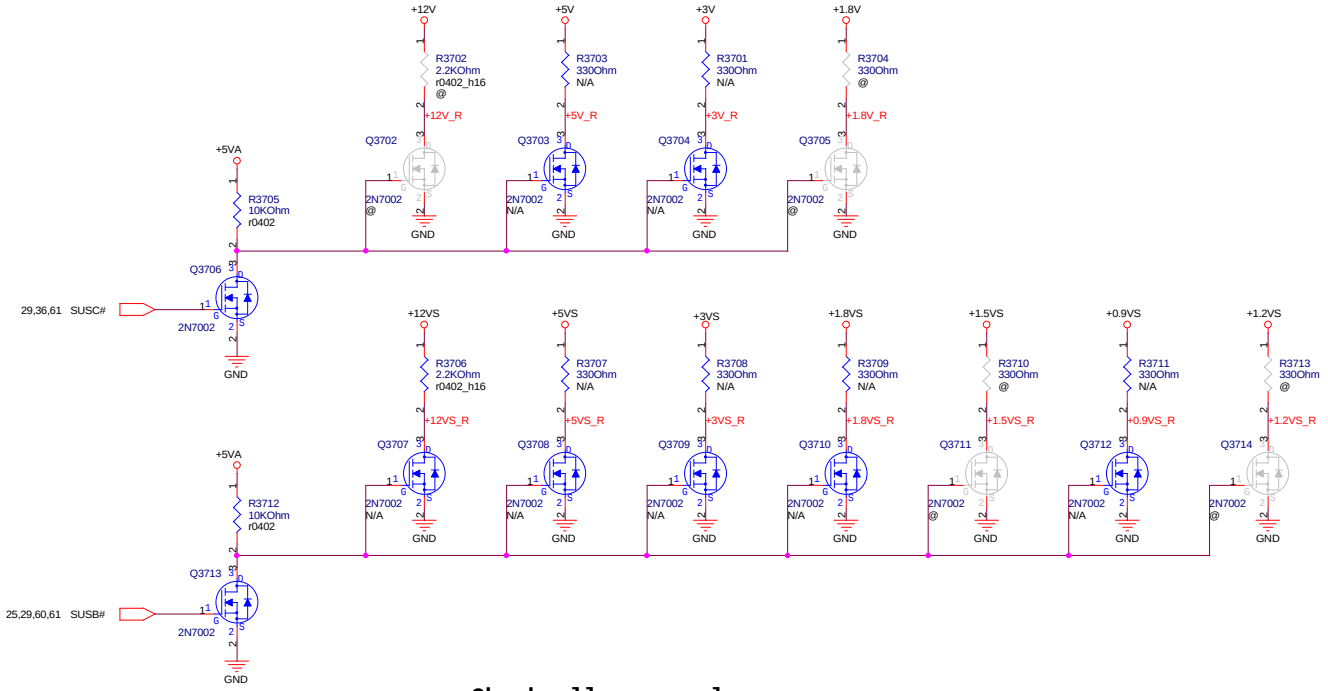






Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 36 of 63	



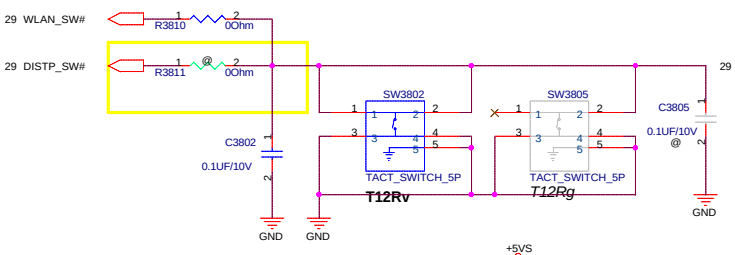
Check all power plan

Default Group-optional

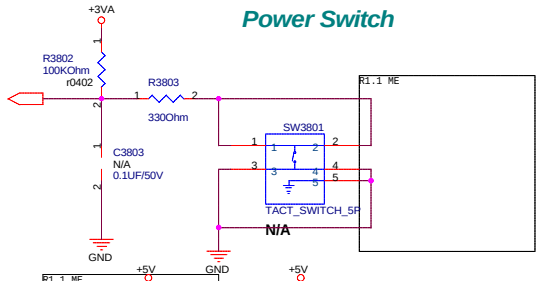
ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 37 of 63	

Main Board SW & LED

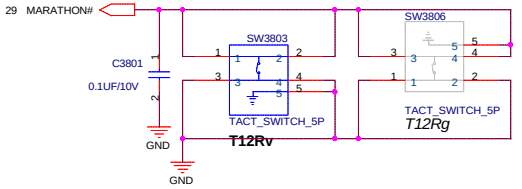
RF/Touchpad Disable



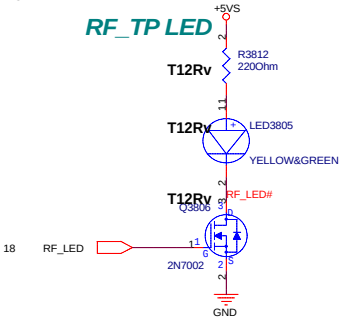
Power Switch



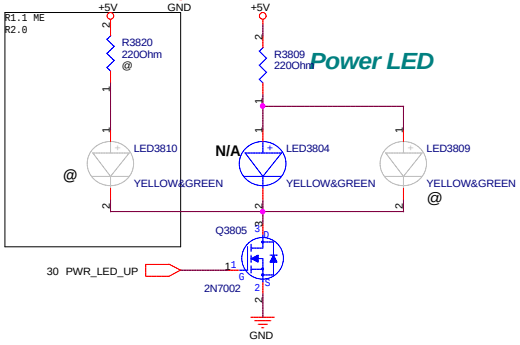
Power4 Gear



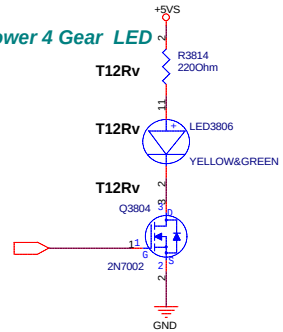
RF_TP LED



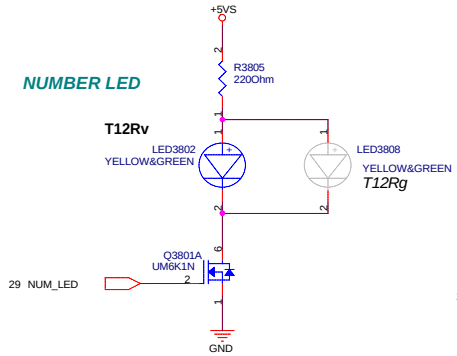
Power LED



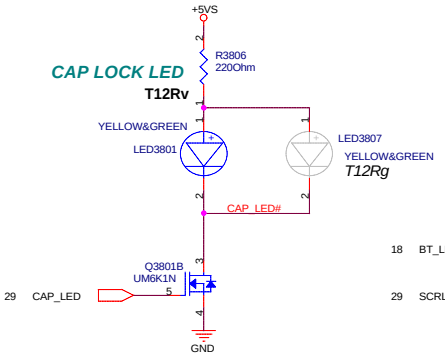
Power 4 Gear LED



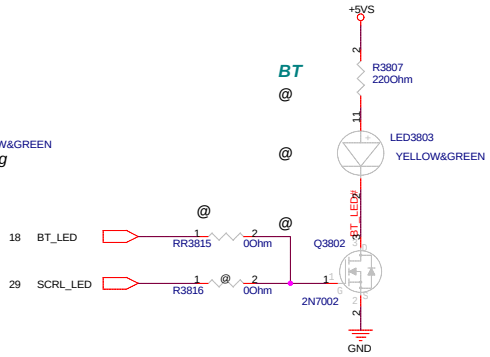
NUMBER LED



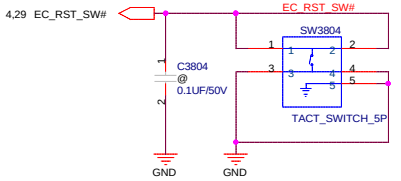
CAP LOCK LED



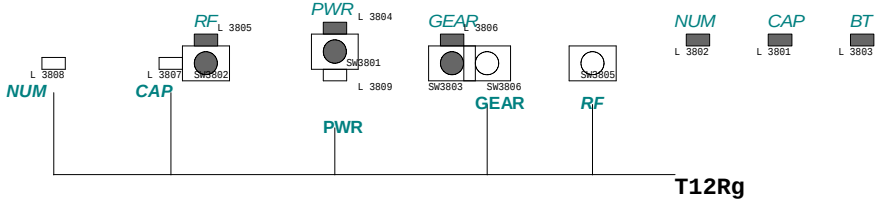
BT



Reset Switch



Pleacemant LED&SW



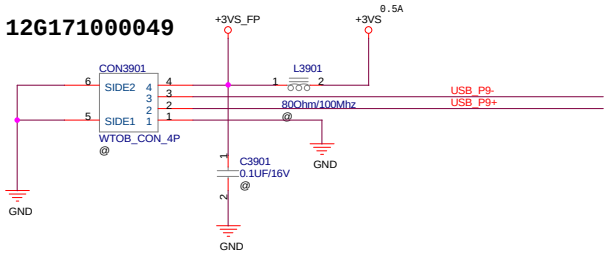
Default Group-optional

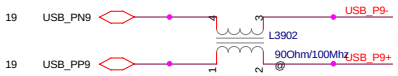
Title :	SW/LED
Engineer:	MICHAEL WANG
ASUSTeK COMPUTER INC	
Size: Custom	Project Name: T12R
Rev:	2.0
Date: Wednesday, August 09, 2006	Sheet 38 of 63

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT





Default Group-optional

ASUSTeK COMPUTER INC

Title : FINGER PRINT

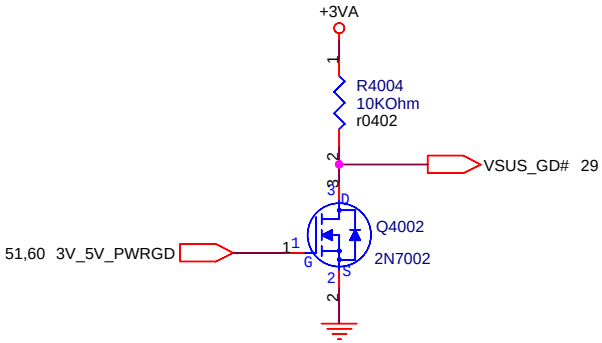
Engineer: MICHAEL WANG

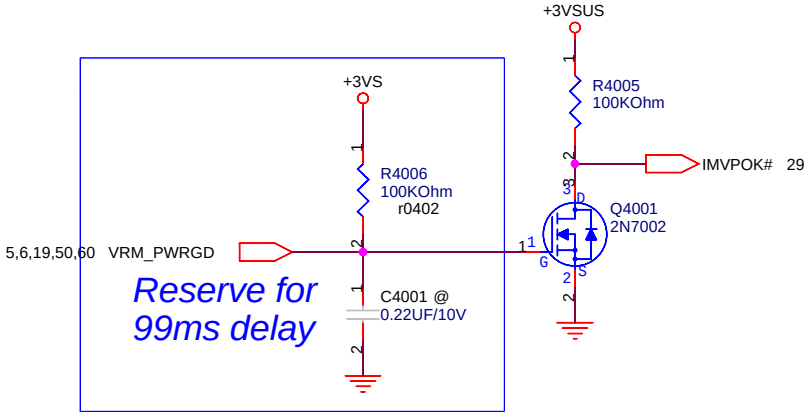
Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 39 of 63

+3VA
+3VS
+3VSUS

+3VA 12,29,38,54,57,59,63
+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,42,43,50,52,60,61
+3VSUS 6,17,19,20,23,25,29,34,51





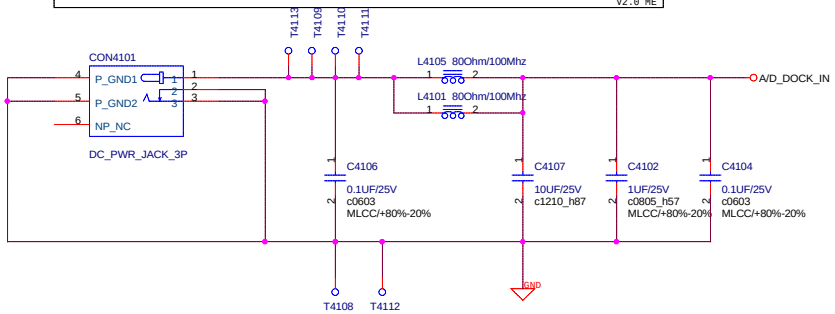
Default Group-optional

ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: MICHAEL WANG	
Size: A4	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 40 of 63	

A/D_DOCK_IN — A/D_DOCK_IN 57,59
BAT_CON — BAT_CON 57
AC_BAT_SYS — AC_BAT_SYS 12,50,51,52,53,54,57,60

12G145002034=>12G14530103E

V2.0 ME



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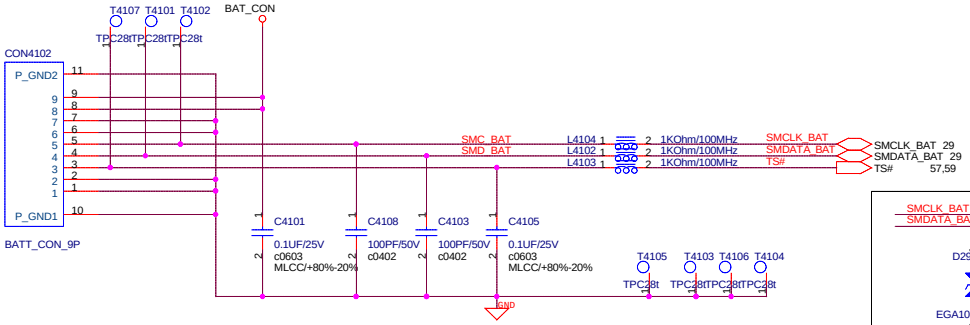
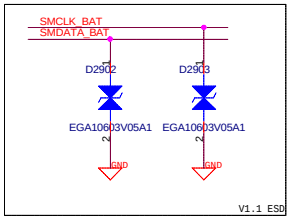
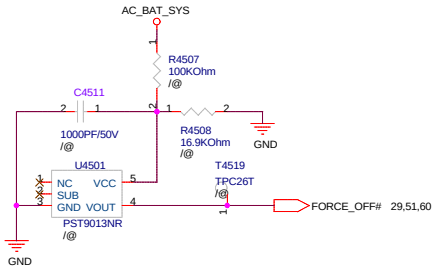




Without Battery & Pull out Adapter RESERVED



Default Group-optional

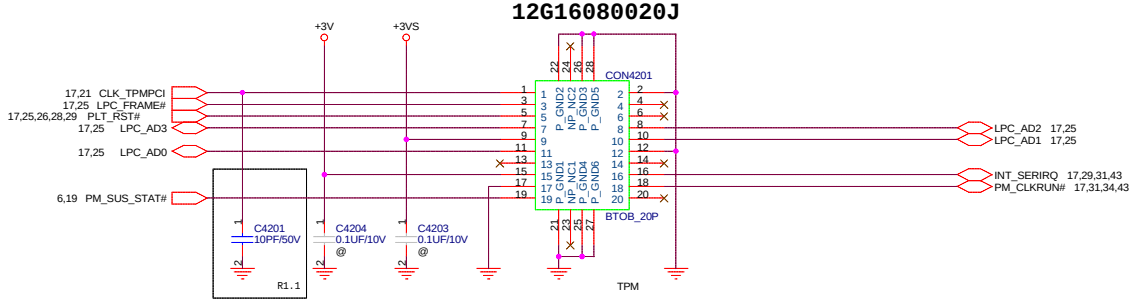
ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : DC IN	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 41 of 63	

+3VS → +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

+3V → +3V 17,25,26,27,31,35,37,43,44,61

TPM Module CON
RESERVED

12G16080020J



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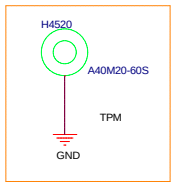
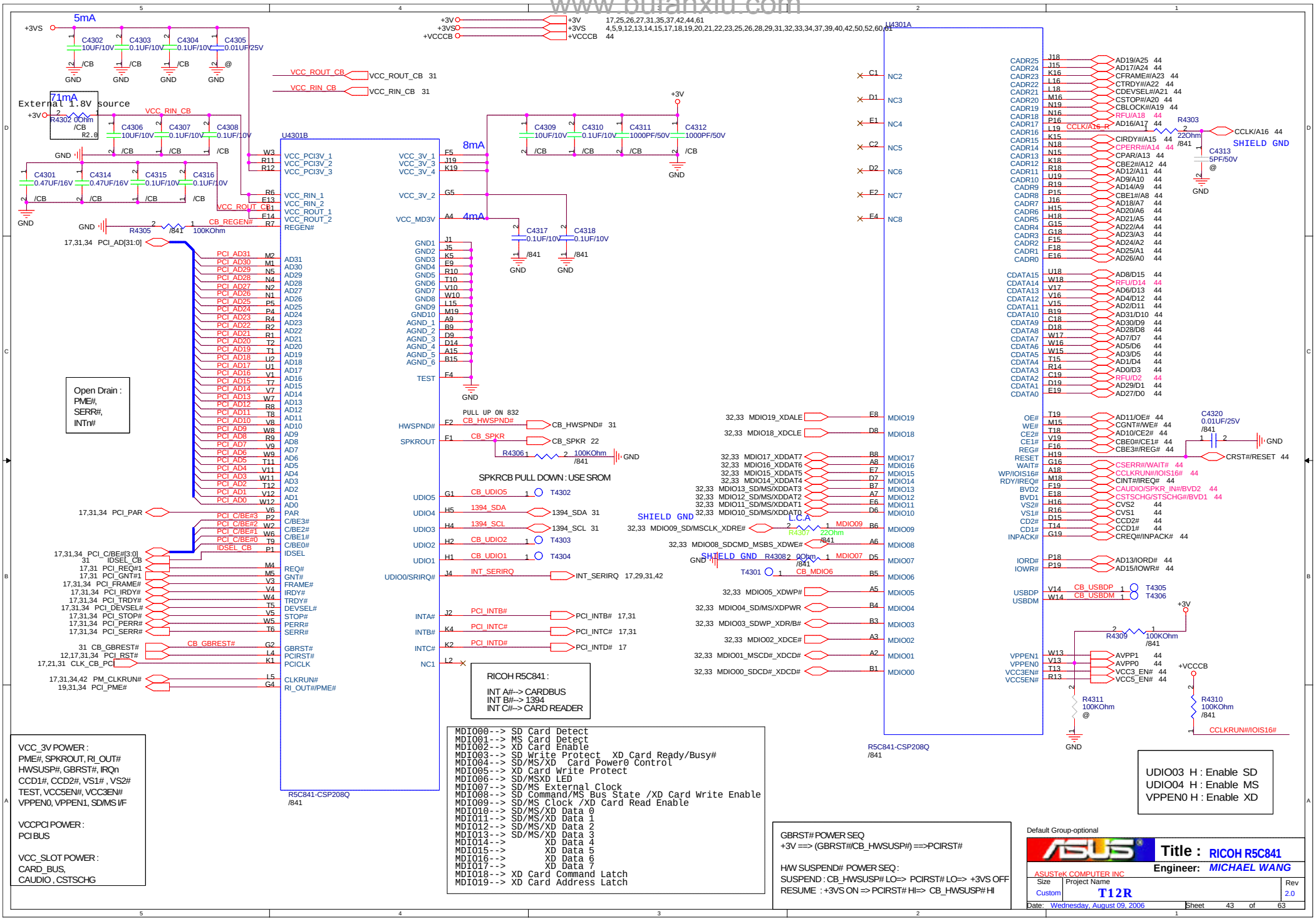


For TPM CONN.

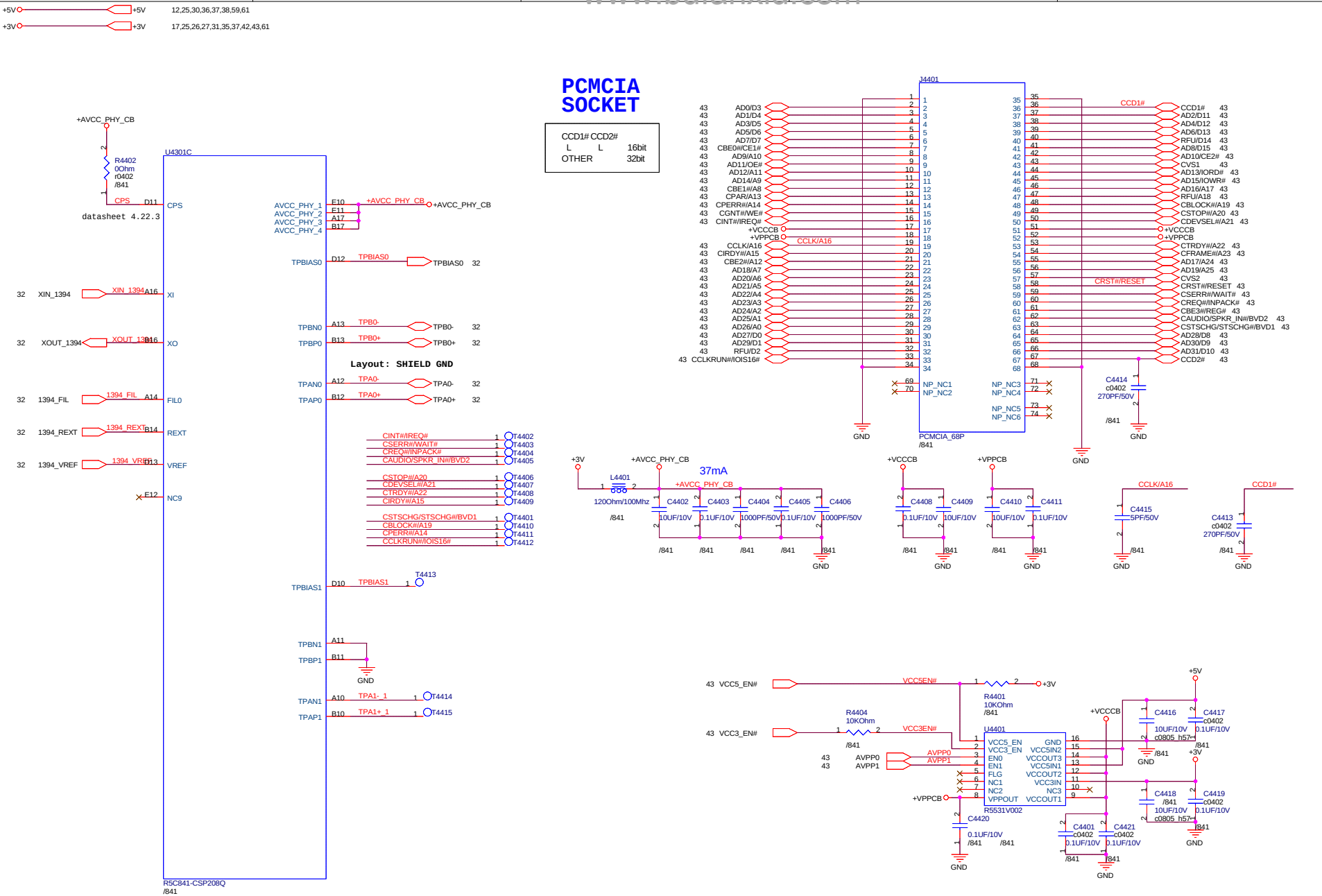
Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 42 of 63	



PCMCIA SOCKET

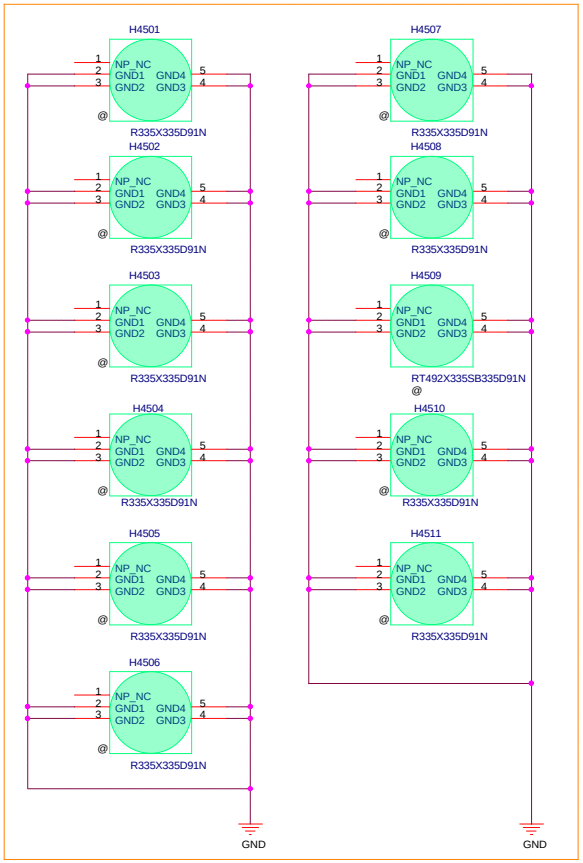
CCD1#	CCD2#	
L	L	16bit
OTHER		32bit



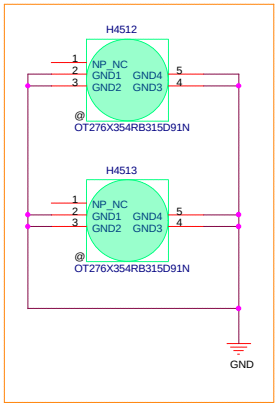
Default Group-optional

ASUSTeK COMPUTER INC	Title : CARDBUS SOCKET	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 44 of 63	

ABCDH



E



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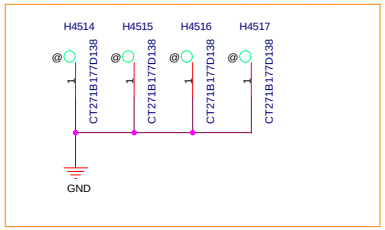
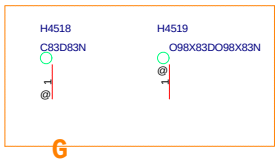
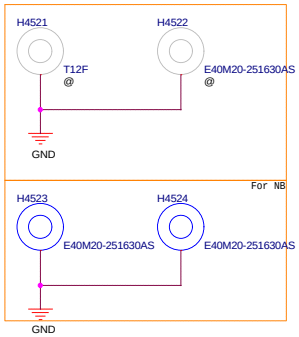


固定孔



G



Default Group-optional

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 45 of 63	

Default Group-optional

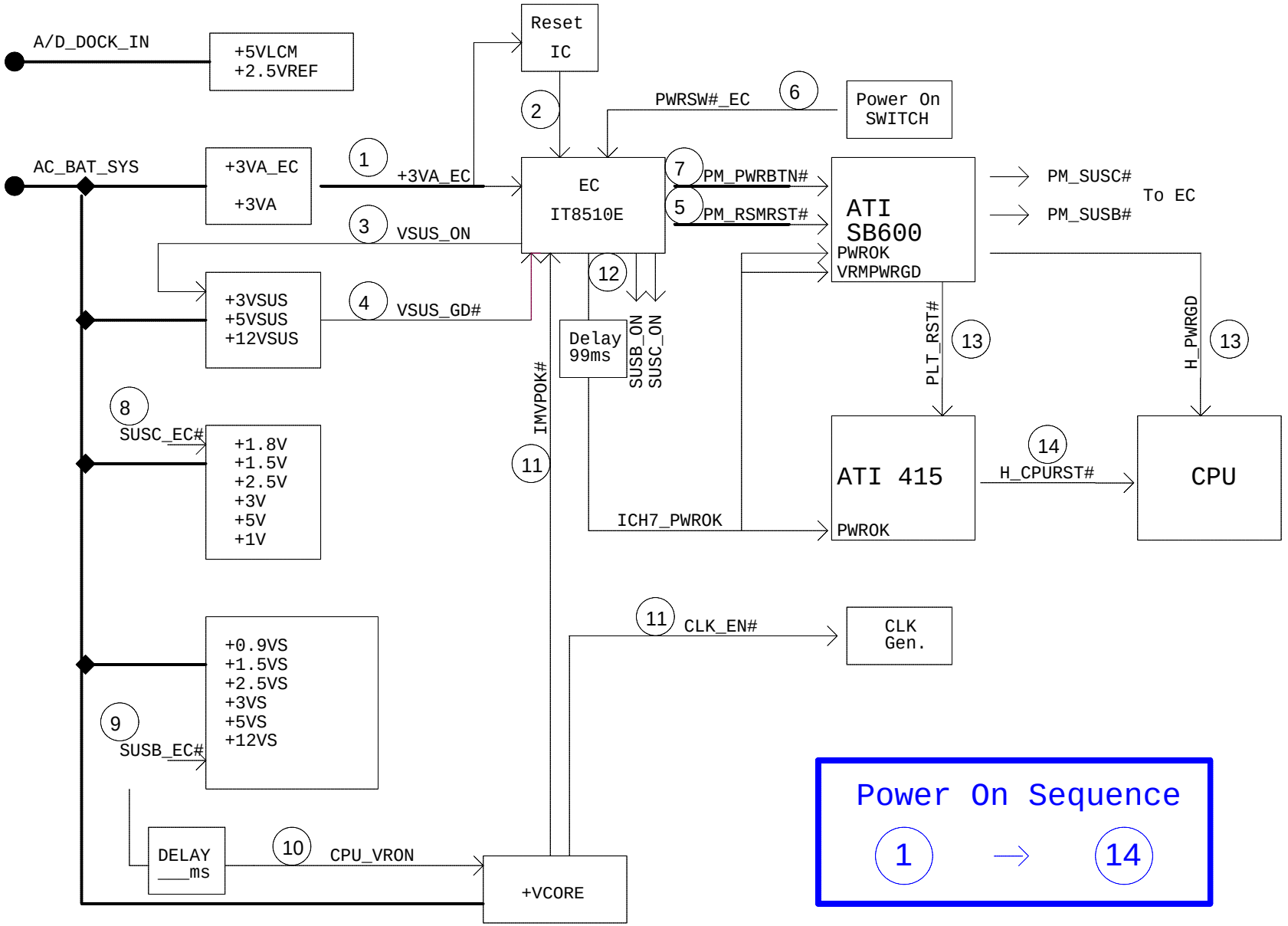
Title : HISTORY

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 46 of 63



Default Group-optional

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 47 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

Default Group-optional

Title : GPIO Setting

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

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T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9.All PCI clock added 6.8 pF to decrease skew.
10.PWM connected to EC and back-light connected to NB
11.D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12.page 19, added BT_DET# to detect BT.
13.Page 19, adjust USB OC ping to correspond USB port
14.Page 25, modification NEW CARD debug circuit to correspond new debug card
15.page 28, we used correctly capacity for customer request.
16.page 36, we used LDO with over current protect IC
17.page 41, DC in connector add 2nd source.

ME modify

1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加螺絲鎖付記號

6.DDR2 added 2nd source
  P/N :12G025022004
  DDR2 DIMM 200P,1.8V,H:4mm,STD
  FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.連版圖修改

T12R V2.0 Modify History

1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 10U with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006~3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

Default Group-optional

ASUS	Title : HISTORY	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12R	Rev: 2.0
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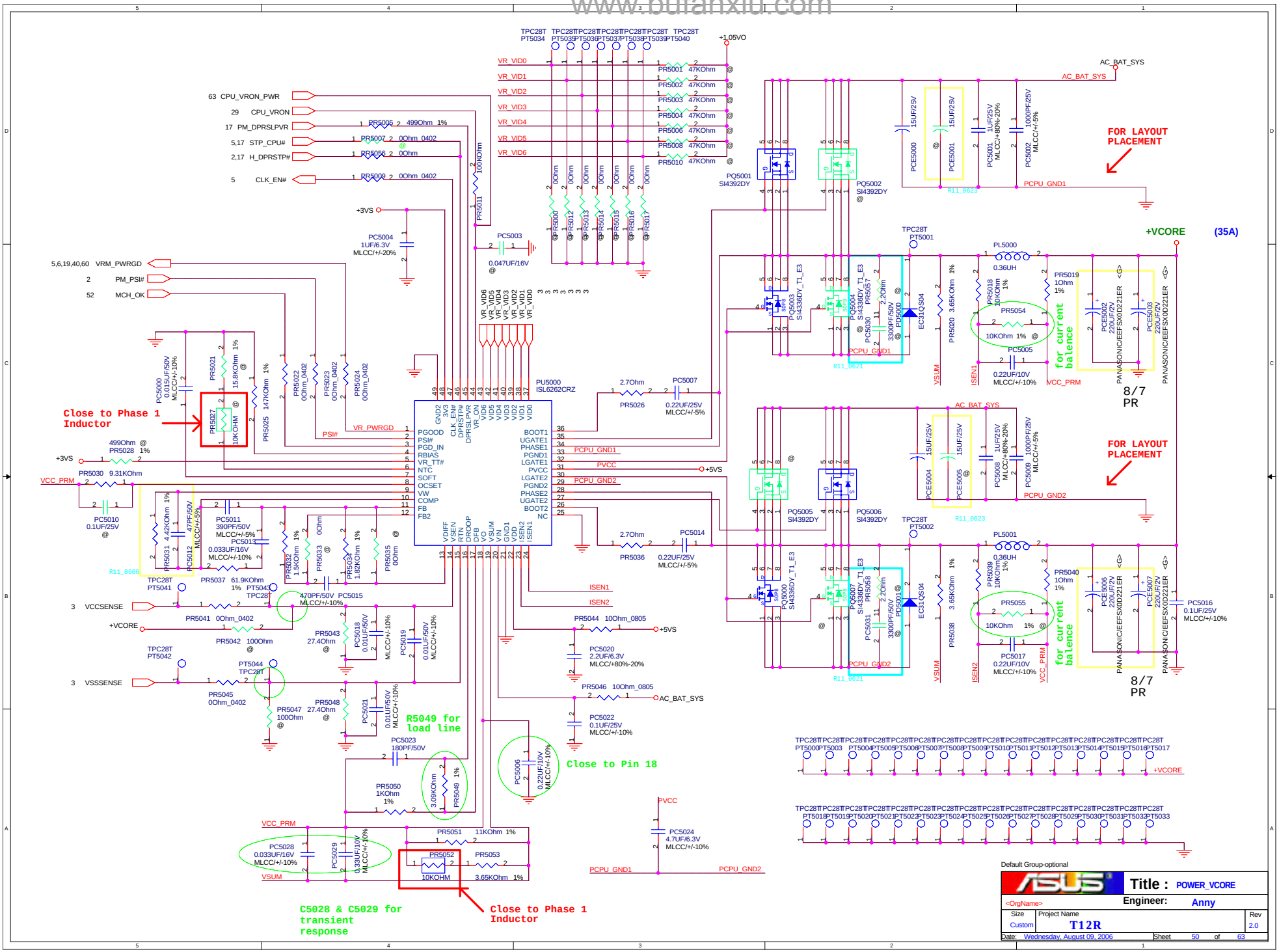
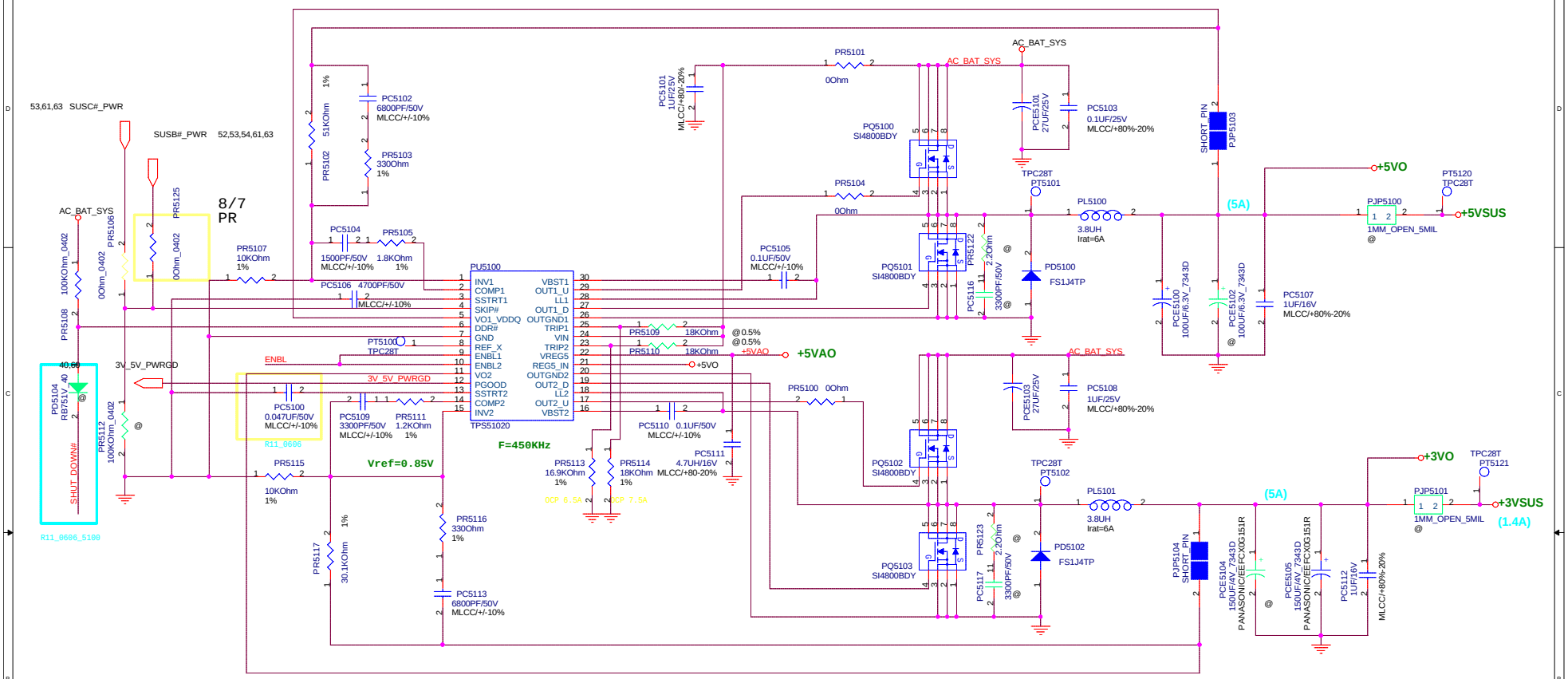
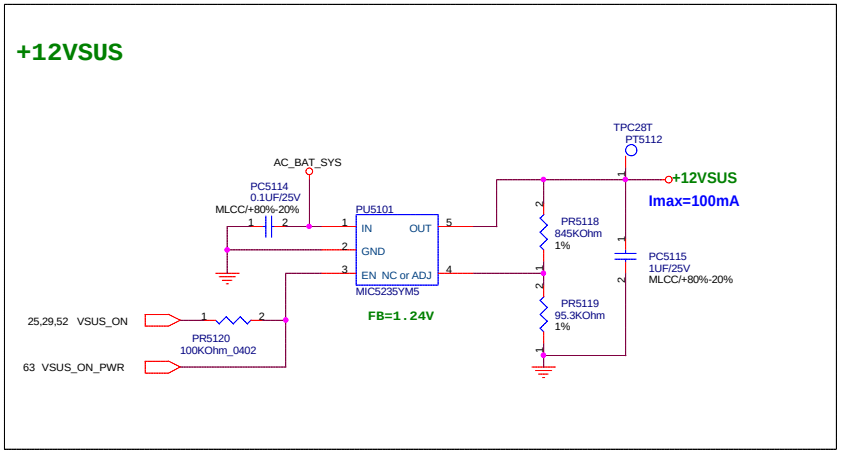
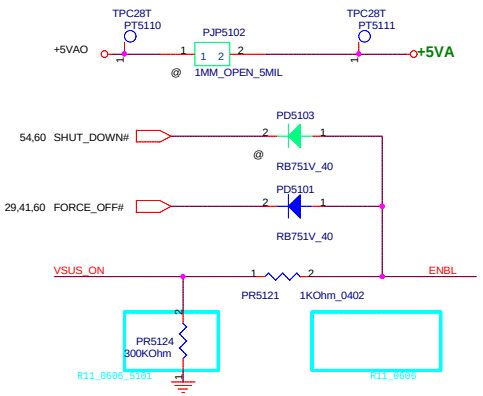
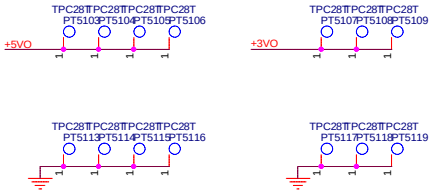




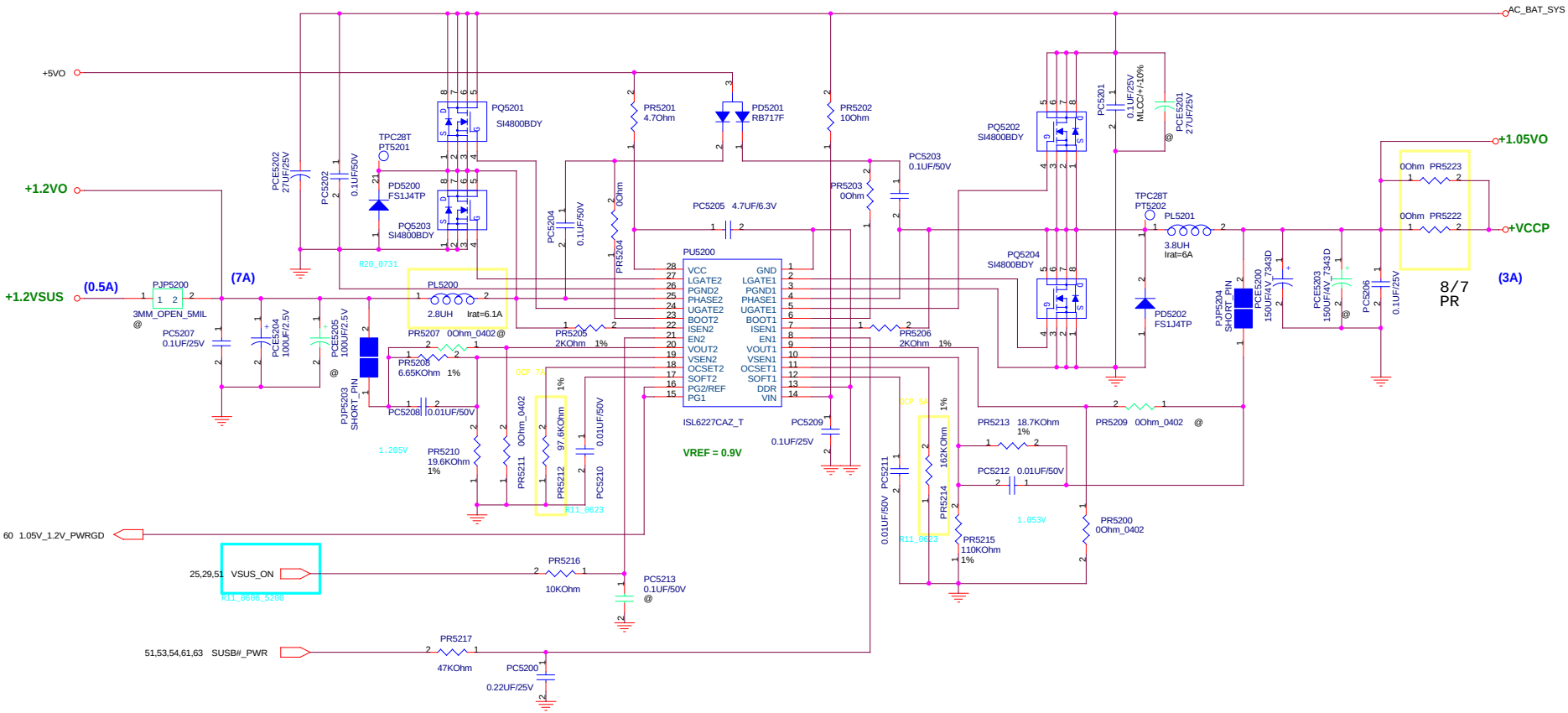






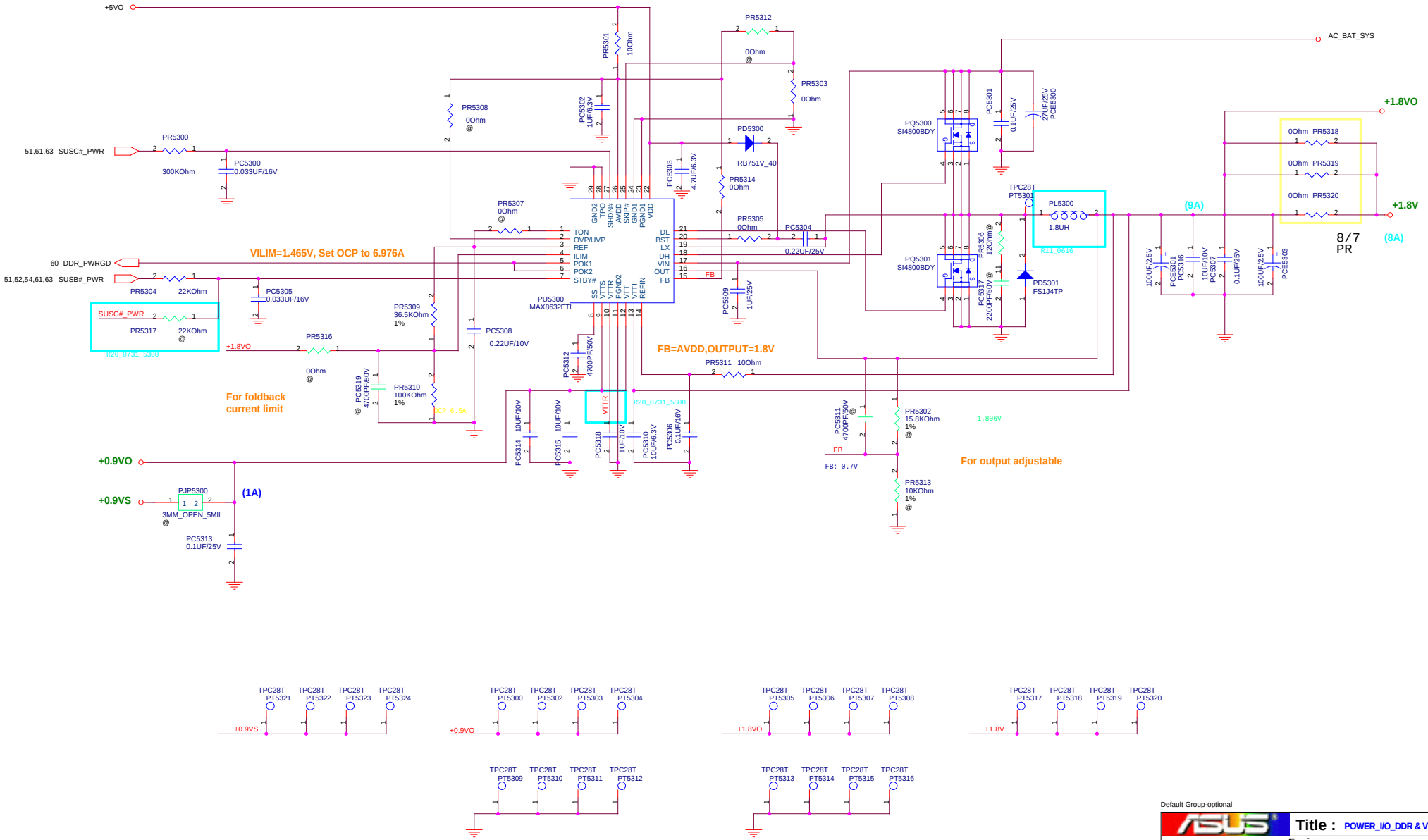
Default Group-optional

ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 51 of 63	



Default Group-optional

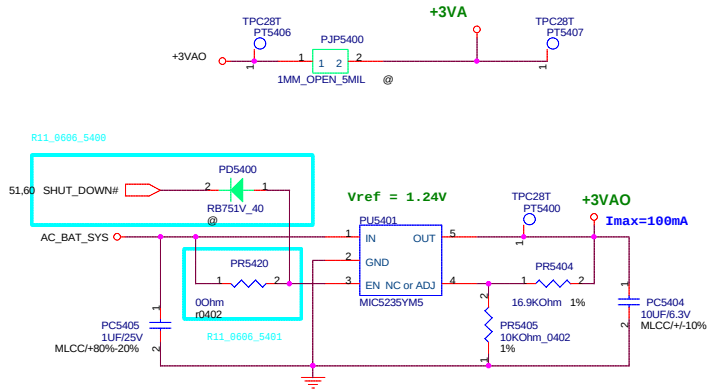
ASUS	Title : POWER_I/O_1.2VS & 1.05VS	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 52 of 63	



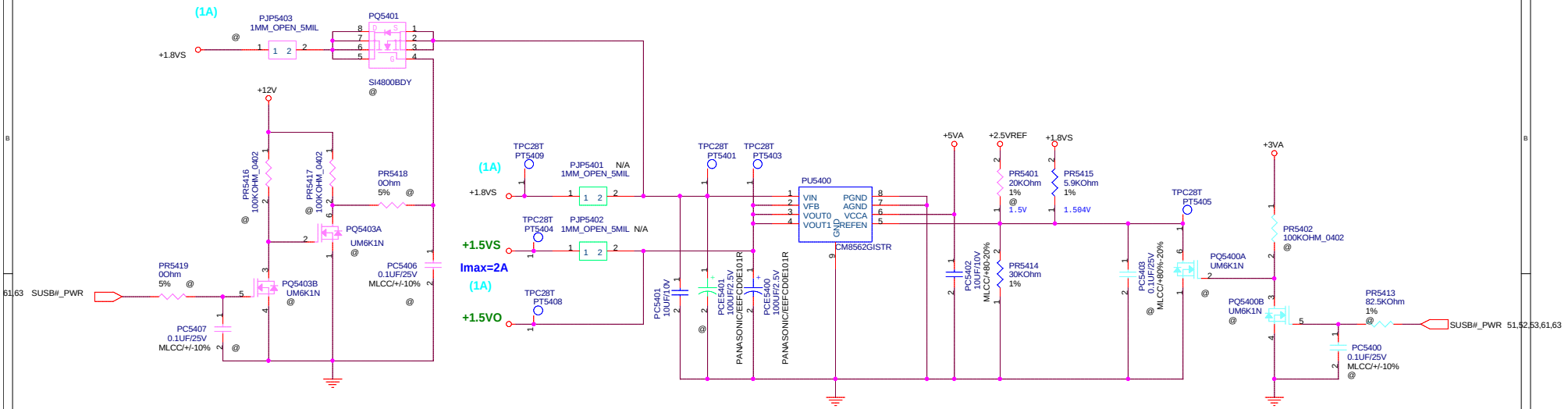
Default Group-optional

Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 53 of 63	

+3VA0

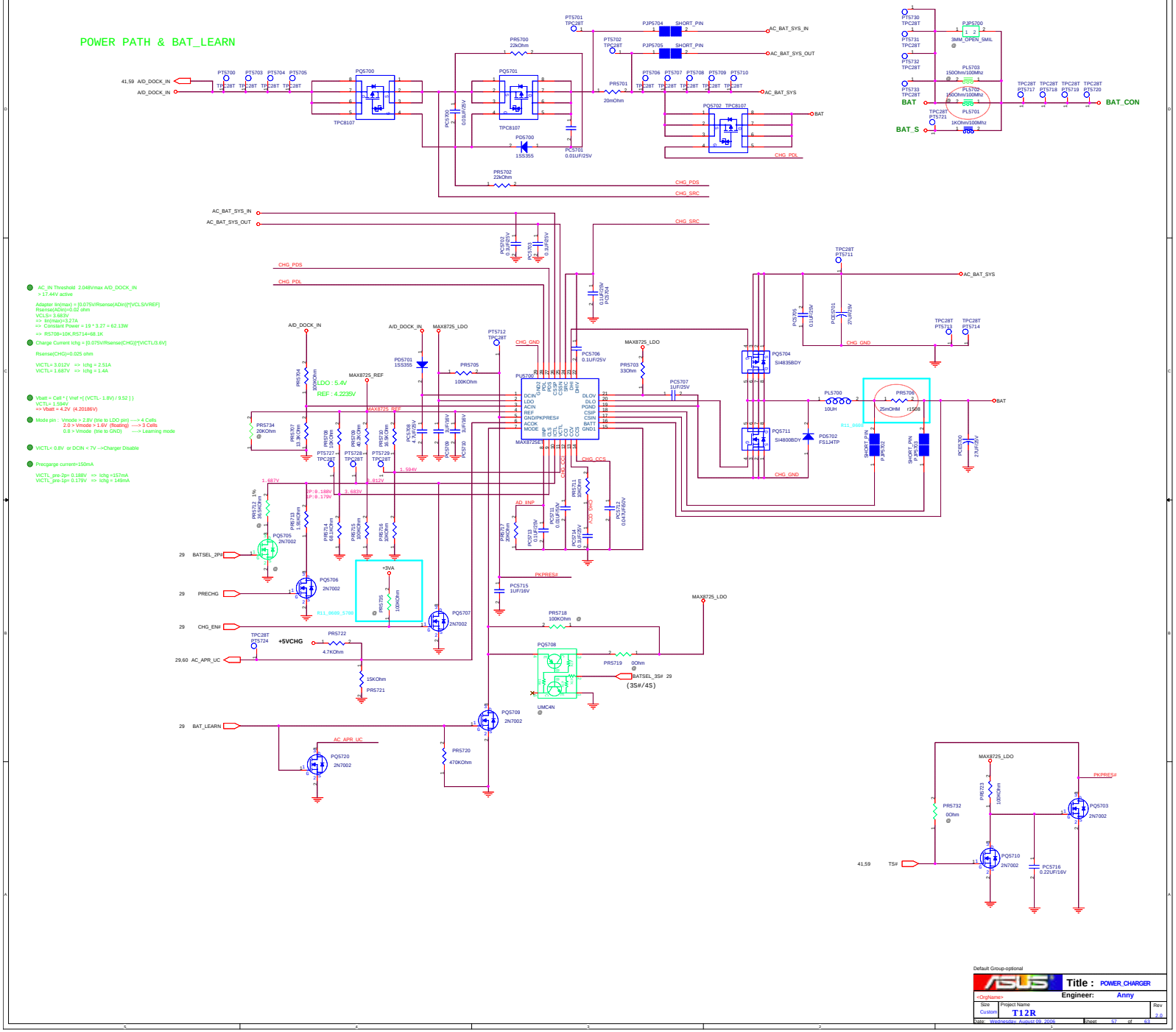


+2.5VS

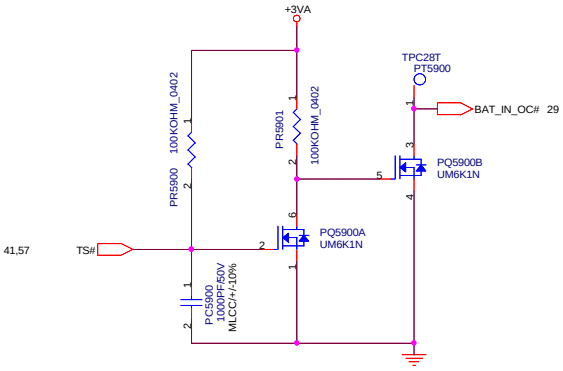


Default Group-optional

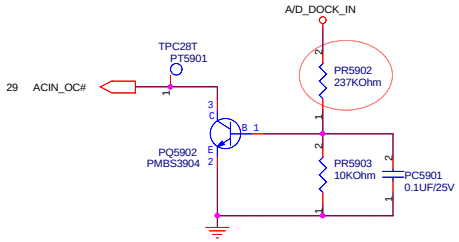
ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 54 of 63	



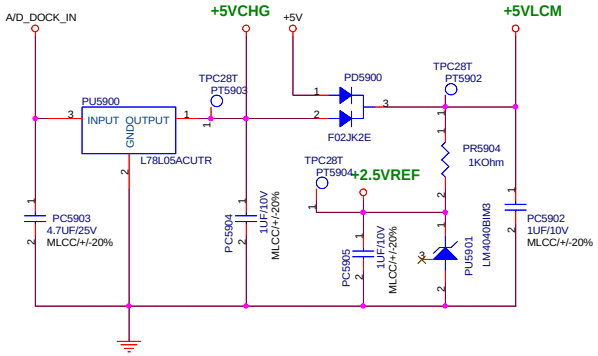
BATTERY IN DETECT



ADAPTER IN DETECT

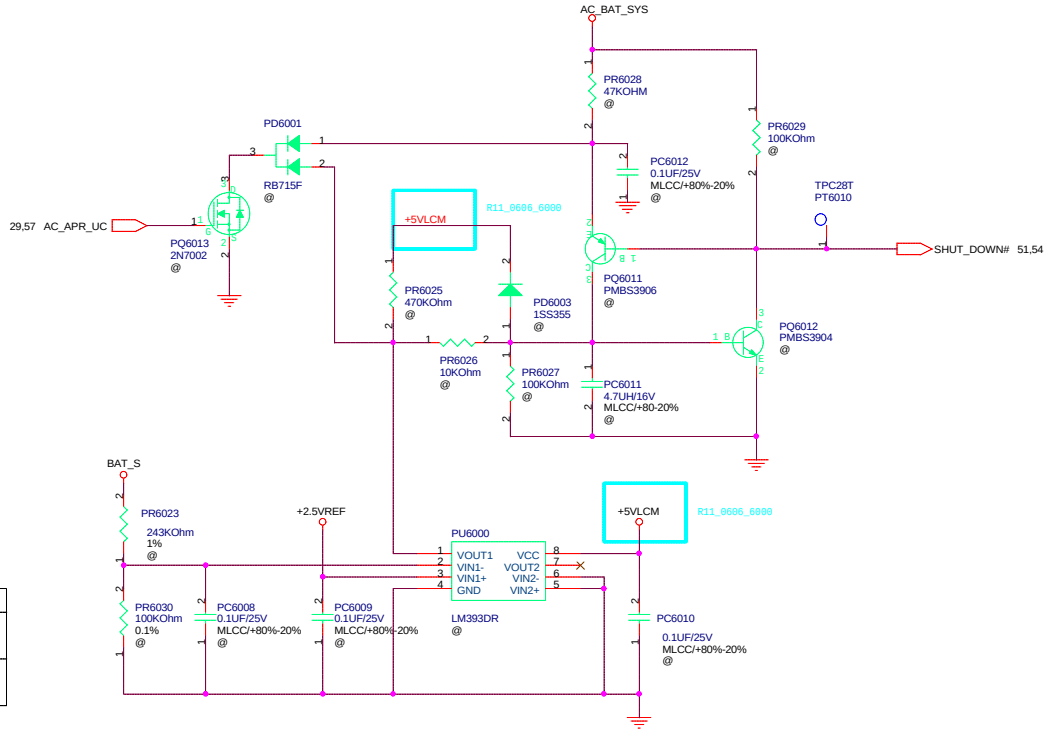


+5VLCM, +5VCHG & +2.5VREF



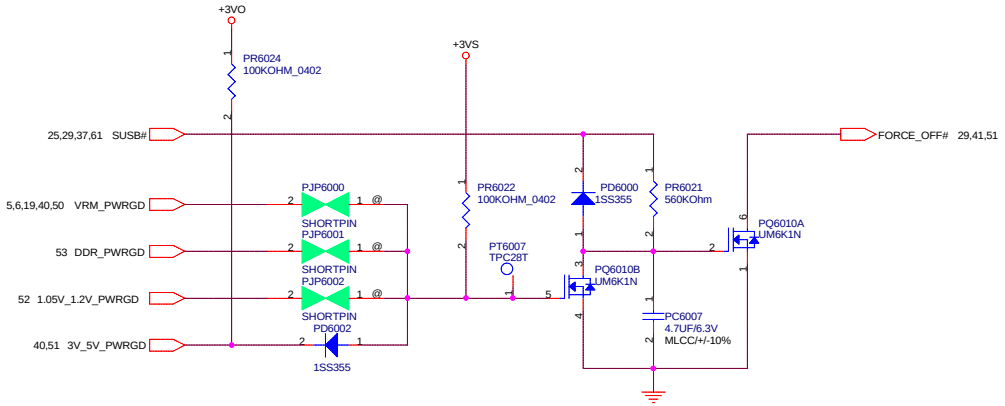
Default Group-optional

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 59 of 63	



	8.575V	11.625V
R6023	243KOhm 10G213243313030 1%	365KOhm 10G213365313010 1%
R6024	100KOhm 10G213100323010 0.1%	100KOhm 10G213100323010 0.1%

POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD

TPC28T PT6004 1 DDR_PWRGD

TPC28T PT6005 1 3V_5V_PWRGD

TPC28T PT6006 1 1.05V_1.2V_PWRGD

Default Group-optional

Title : POWER_PROTECT

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12R	2.0

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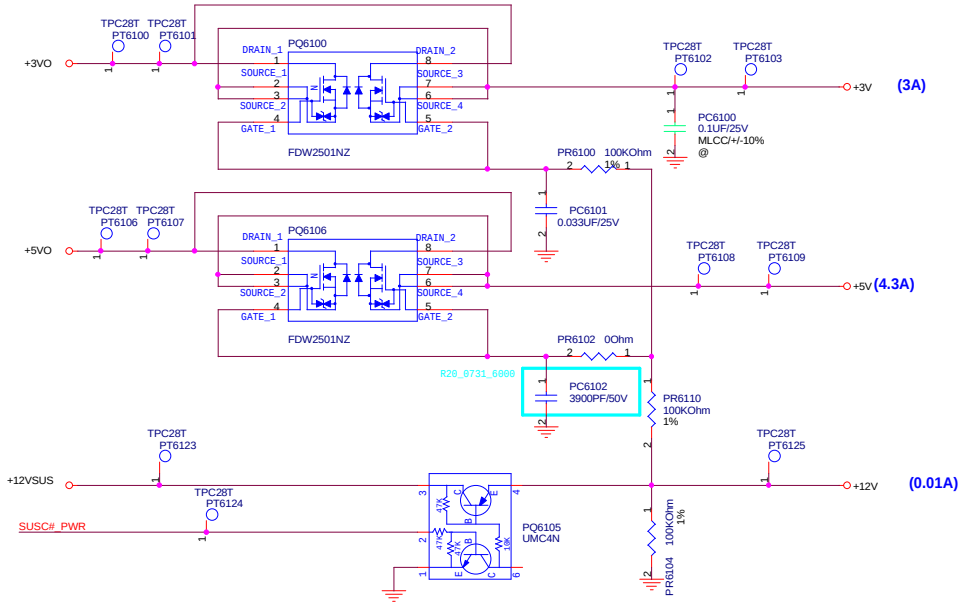
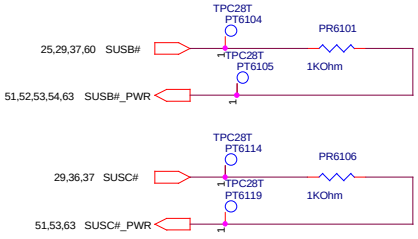
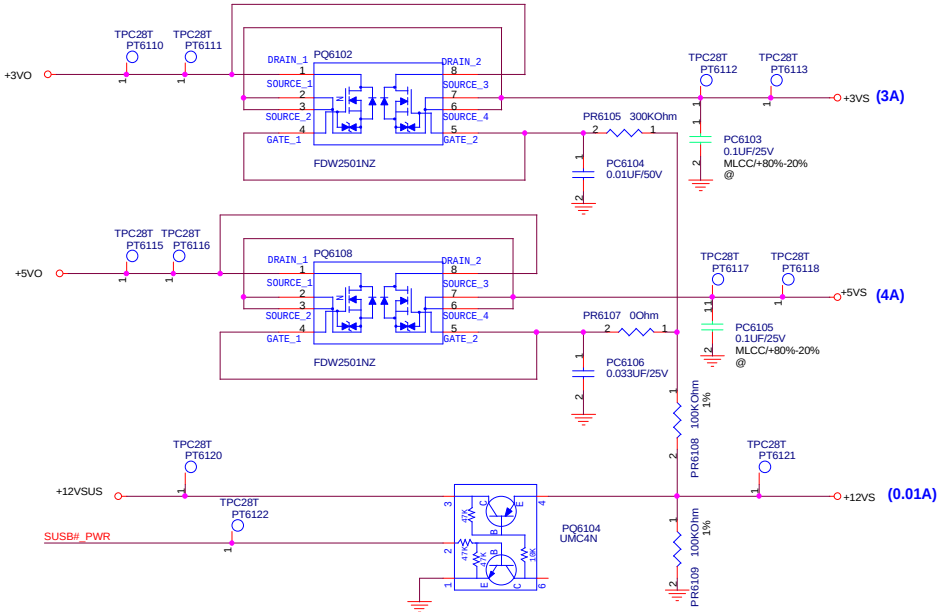
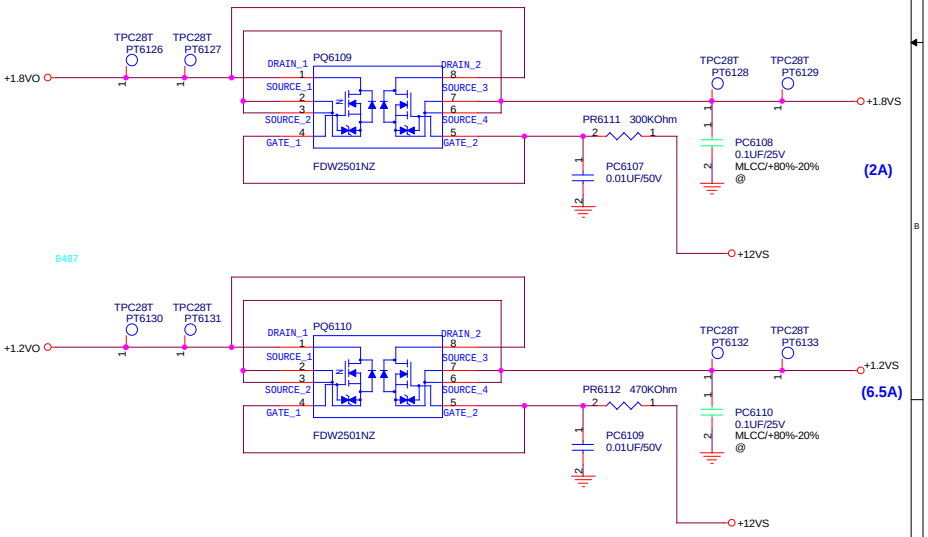
SUSC#_PWR POWER





SUSB#_PWR POWER





Default Group-optional

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 61 of 63	

AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57,60

+3VA → +3VA 12,29,38,40,54,57,59

+5VA → +5VA 9,37,51,54

+5VO → +5VO 51,52,53,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 6,17,19,20,23,25,29,34,40,51

+5VSUS → +5VSUS 30,51

+3V → +3V 17,25,26,27,31,35,37,42,43,44,61

+3VS → +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 23,37,54,61

+12VS → +12VS 12,33,37,61

+5V → +5V 12,25,30,36,37,38,44,59,61

+5VS → +5VS 4,13,20,22,23,28,29,30,37,38,50,61

+1.2VO → +1.2VO 52,61

+1.2VSUS → +1.2VSUS 20,52

+1.2VS → +1.2VS 6,7,9,10,20,37,61

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,10,14,15,16,37,53

+VCCP → +VCCP 2,5,6,10,17,19,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3

+VCCP_GMCH → +VCCP_GMCH

+VCCP_ICH → +VCCP_ICH

+0.9VS → +0.9VS 16,37,53

BAT → BAT 57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 59,60

+2.5VREF → +2.5VREF 54,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST

+3VA → PJP6300 (1 | 1 2 | 2) SGL_JUMP @ → CPU_VRON_PWR 50

+3VA → PJP6301 (1 | 1 2 | 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,61

+3VA → PJP6302 (1 | 1 2 | 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 51,53,61

+3VA → PJP6303 (1 | 1 2 | 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

Default Group-optional

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 63 of 63	

R1.1

Item	Before	After	Reason	Owner	Date
R11_0606_5100		Add PD5104	for shutdown application		2006.06.06
R11_0606	PC5100: 0.01uF	PC5100 change to 0.047uF	for EE timing request		2006.06.06
R20_0606_5101		add PR5124	Pull ground to avoid vsus_on is float.		2006.06.06
R11_0606_5200	VSUS_ON_PWR	VSUS_ON			2006.06.06
R11_0609_5700		Add PR5735 to +3VA on CHG_EN# pin	To avoid CHG_EN# pin floating in initial		2006.06.06

R2.0

Item	Before	After	Reason	Owner	Date
R20_0731_6000	0.047uF	3900pF	for EE timing request		2006.07.31
R20_0731_5300	None	VTTR	For DDR Vref		2006.07.31

R2.0

Item	Before	After	Reason	Owner	Date

Default Group-optional

ASUS Title : POWER_PIC

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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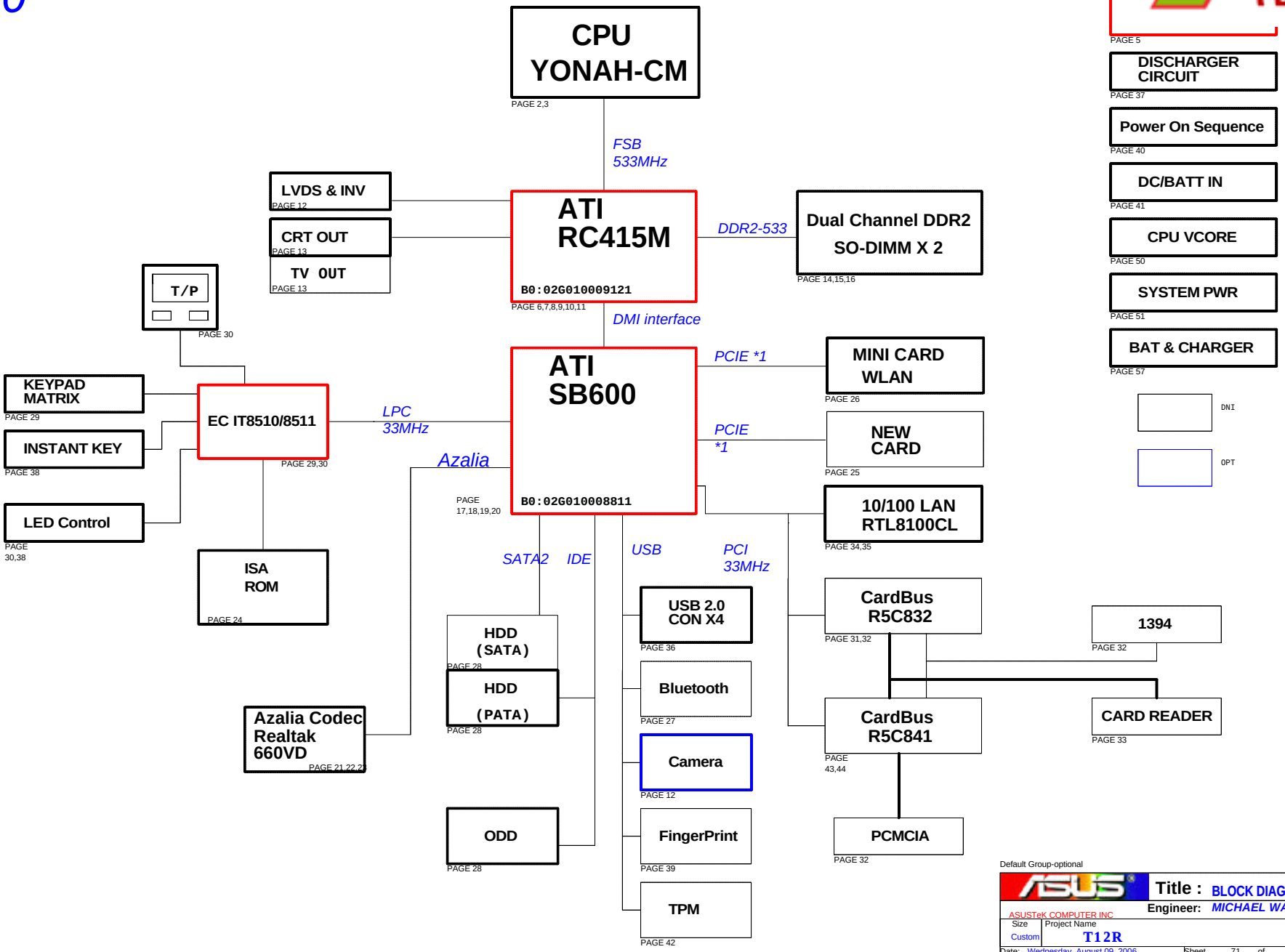
T12Rv Block Diagram V2.0



Default Group-optional

Title : BLOCK DIAGRAM

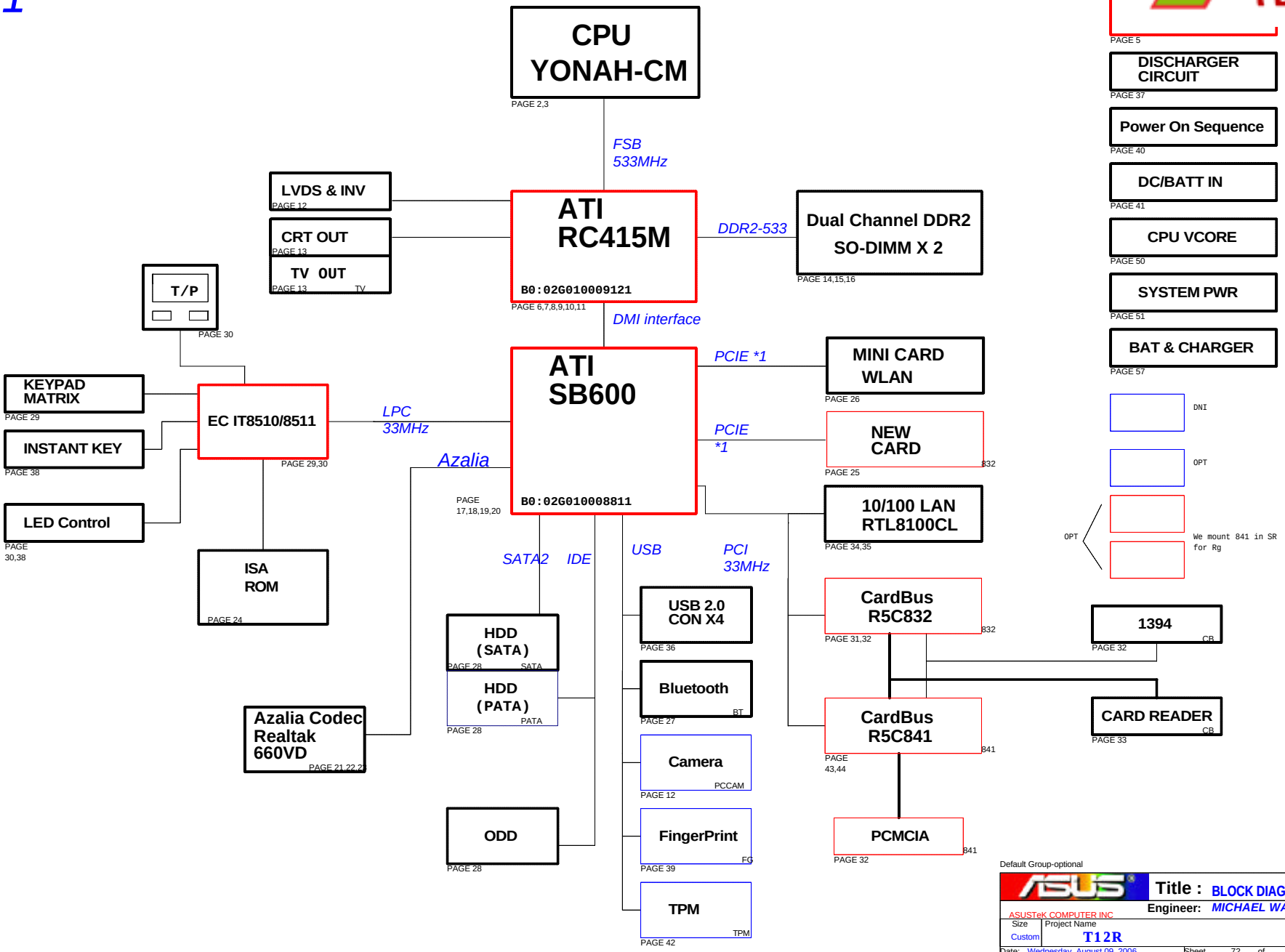
Engineer: MICHAEL WANG

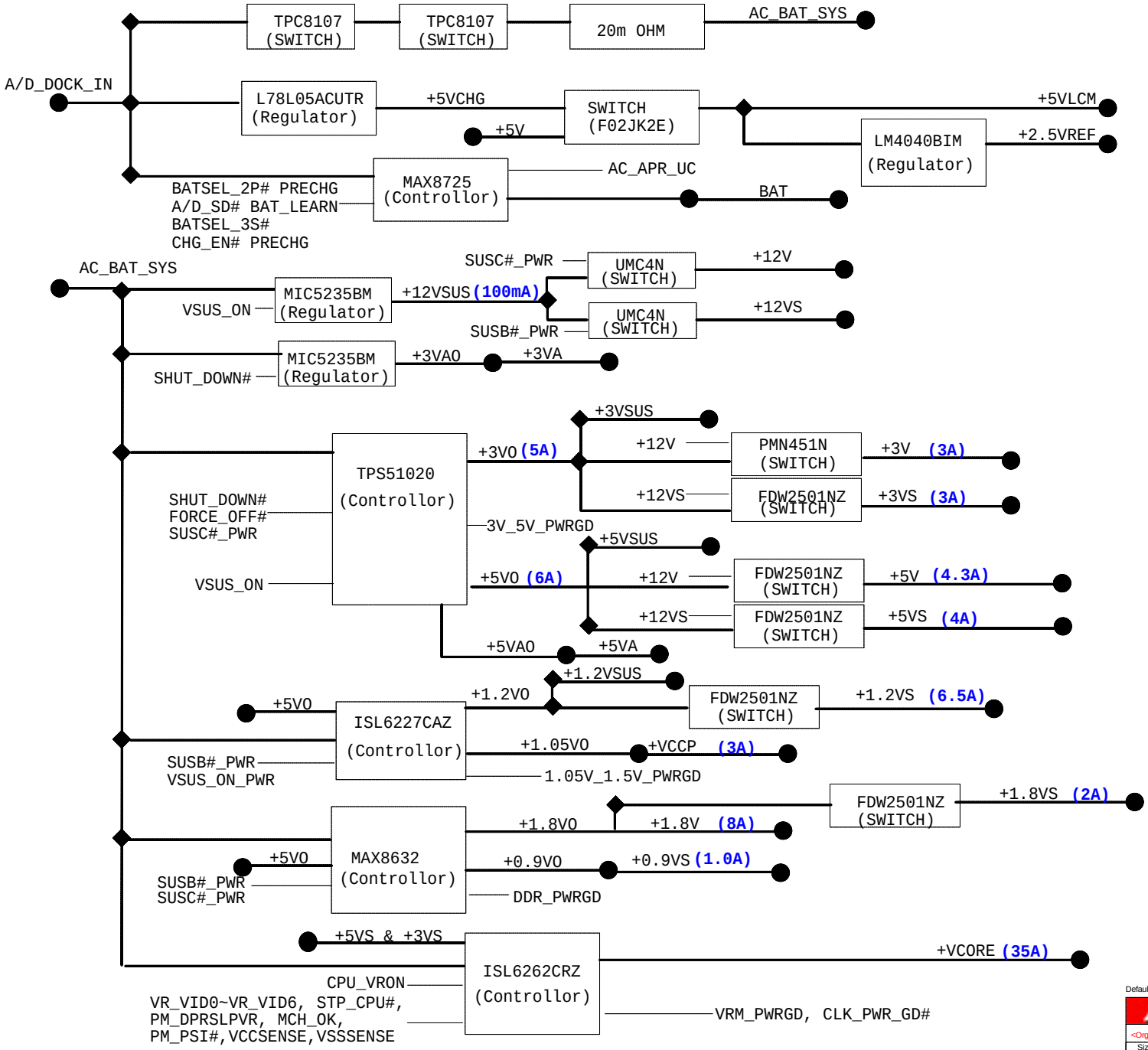
ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 71 of 63

T12Rg Block Diagram V1.1





Default Group-optional

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 87 of 89	