T13Fv SCHEMATIC R1.11

SYSTEM PAGE REF.

POWER PAGE REF.

<Variant Name>

ASUSTeK COMPUTER INC

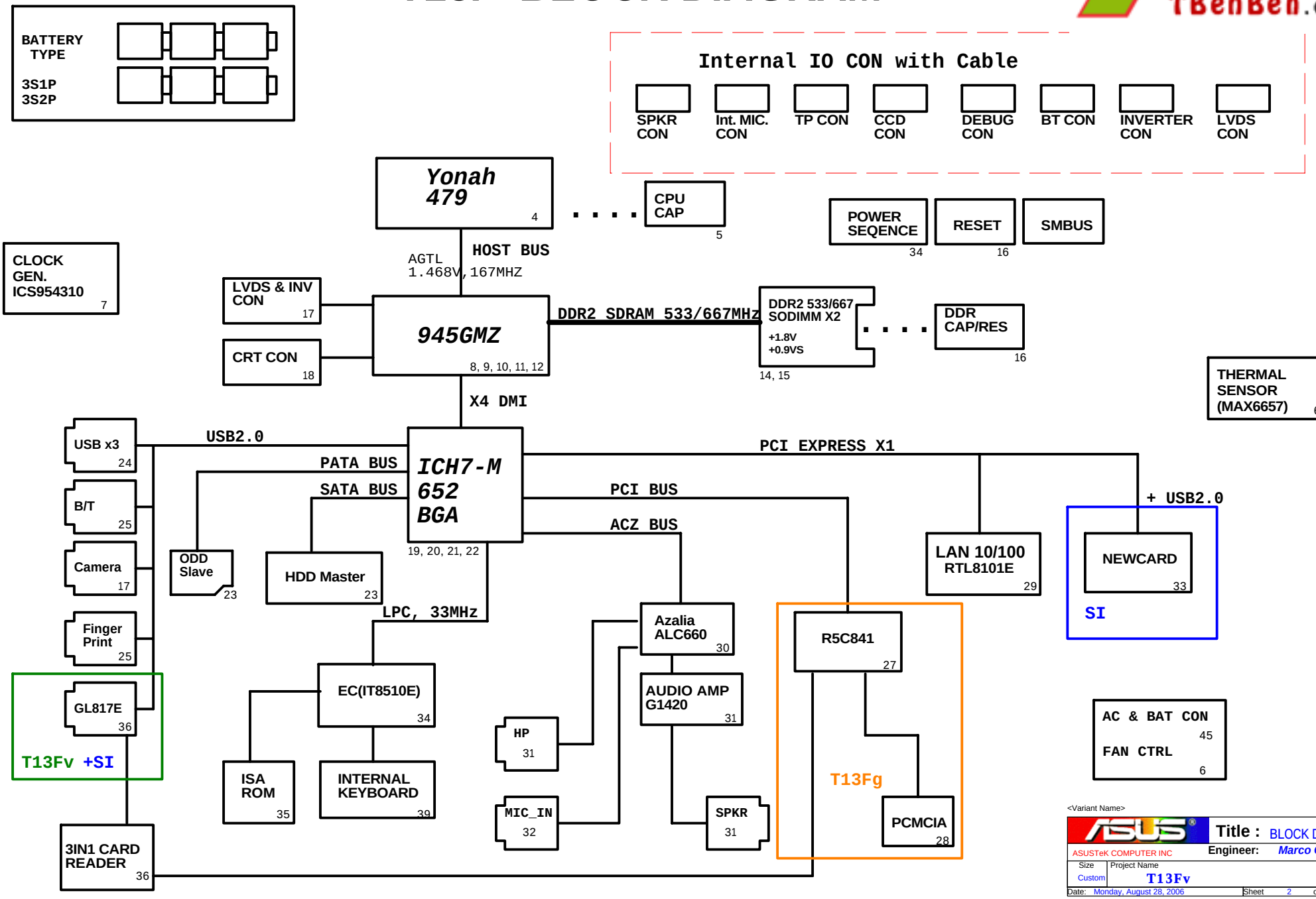
Title : PAGE REF.

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 1 of 63

T13F BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 2 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	CR_DRIVER#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	CR_POWER#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	PWRLMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

ICH7M_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

ICH7M_PCI_DEVICE:

PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

ICH7M_GPIO

Pin		Use As	Signal Name	
GPIO 00	i	GPI	PM_BMBUSY#	
GPIO 01	i	GPI	PCI_REQ#5	
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	
GPIO 06	i	GPO	BT_LED_EN	
GPIO 07	i	GPI	N/A	+3VS
GPIO 08	i	GPI	EXTSMI#	+3VSUS
GPIO 09	i	GPI	N/A	+3VSUS
GPIO 10	i	GPI	N/A	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KBC_SCI#	+3VSUS
GPIO 13	i	GPI	N/A	+3VSUS
GPIO 14	i	GPI	N/A	+3VSUS
GPIO 15	i	GPO	802_LED_EN	+3VSUS
GPIO 16	O	0 GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1 GPO	PCI_GNT#5	+3VS
GPIO 18	O	1 GPO	STP_PCI#	+3VS
GPIO 19	i	1 GPI	N/A	+3VS
GPIO 20	O	1 GPO	STP_CPU#	+3VS
GPIO 21	i	1 GPO	N/A	+3VS
GPIO 22	i	1 Native	PCI_REQ#4	+3VS
GPIO 23	i	1 Native	N/A	+3VS
GPIO 24	O	0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1 GPO	CB_SD#	+3VSUS
GPIO 26	O	0 GPO	BT_ON#	+3VSUS
GPIO 27	O	0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0 GPO	MEMROM/YONAH#	+3VSUS
GPIO 29	i	0 Native	USB_OC#5	+3VSUS
GPIO 30	i	0 Native	USB_OC#6	+3VSUS
GPIO 31	i	0 Native	USB_OC#7	+3VSUS
GPIO 32	O	1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1 GPO	N/A	+3VS
GPIO 34	O	0 GPO	CPU_Select	+3VS
GPIO 35	O	0 GPO	N/A	+3VS
GPIO 36	i	0 GPO	N/A	+3VS
GPIO 37	i	0 GPI	PCB_ID0	+3VS
GPIO 38	i	0 GPI	PCB_ID1	+3VS
GPIO 39	i	0 GPI	PCB_ID2	+3VS
GPIO [40:47]		NA	NA	NA
GPIO 48		Native	PCI_GNT#4	+3VS
GPIO 49		Native	H_PWRGD	+VCORE

<Variant Name>

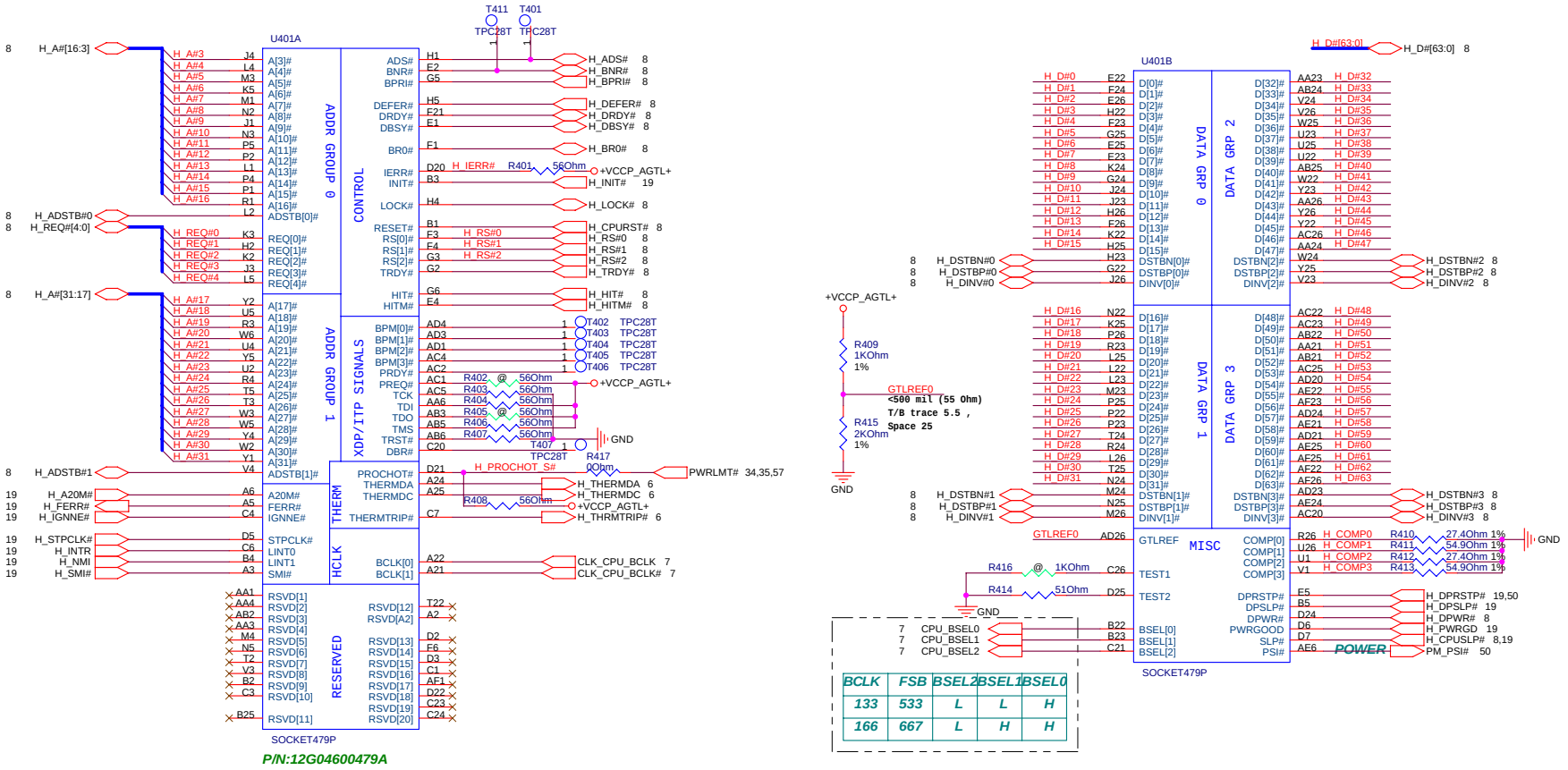
ASUSTeK COMPUTER INC

Title : Schematic data

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 3 of 63



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<Variant Name>

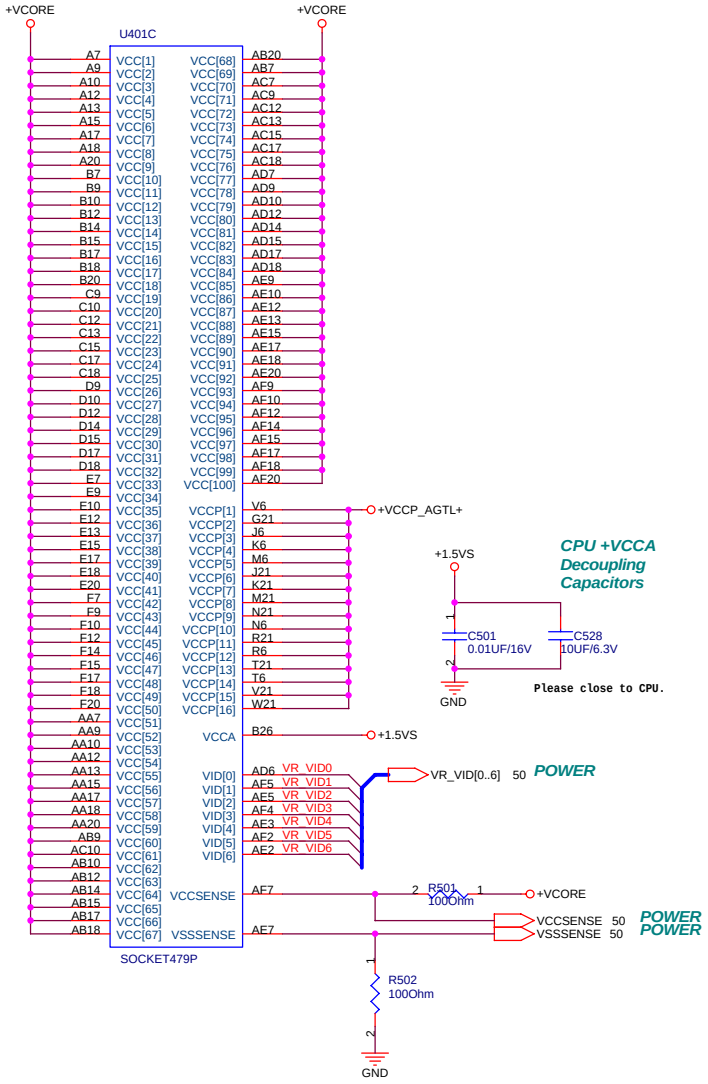
ASUSTeK COMPUTER INC

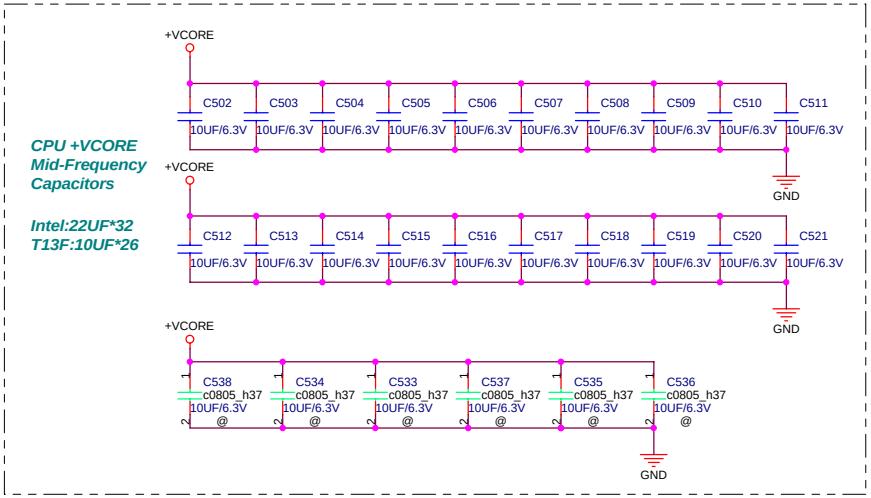
Title : YONAH CPU (1)

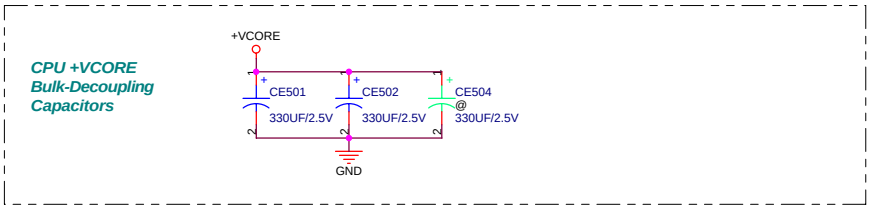
Engineer: Marco Chen

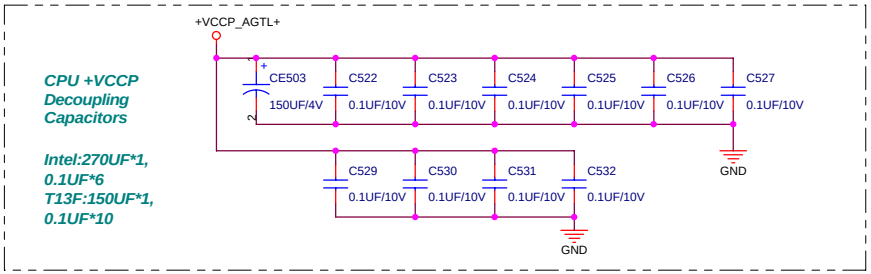
Size	Project Name	Rev
Custom	T13Fv	1.11

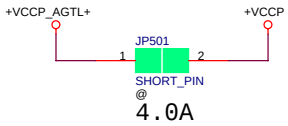
Date: Monday, August 28, 2006 Sheet 4 of 63

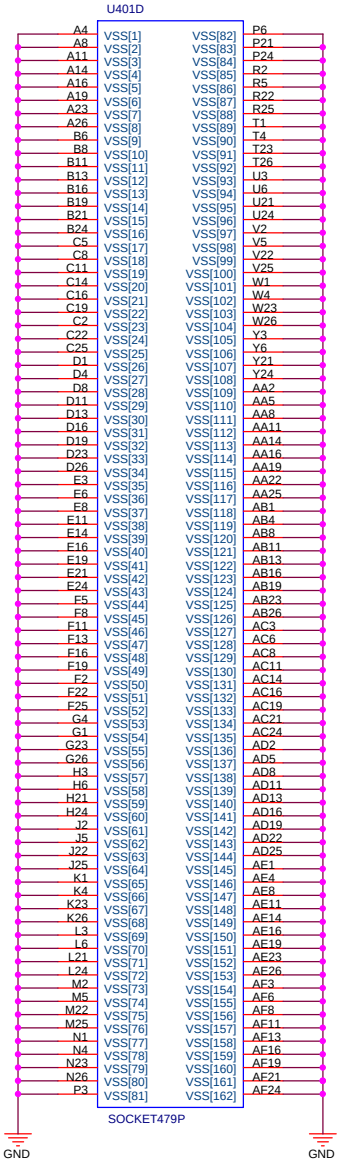












<Variant Name>

Title : YONAH CPU (2)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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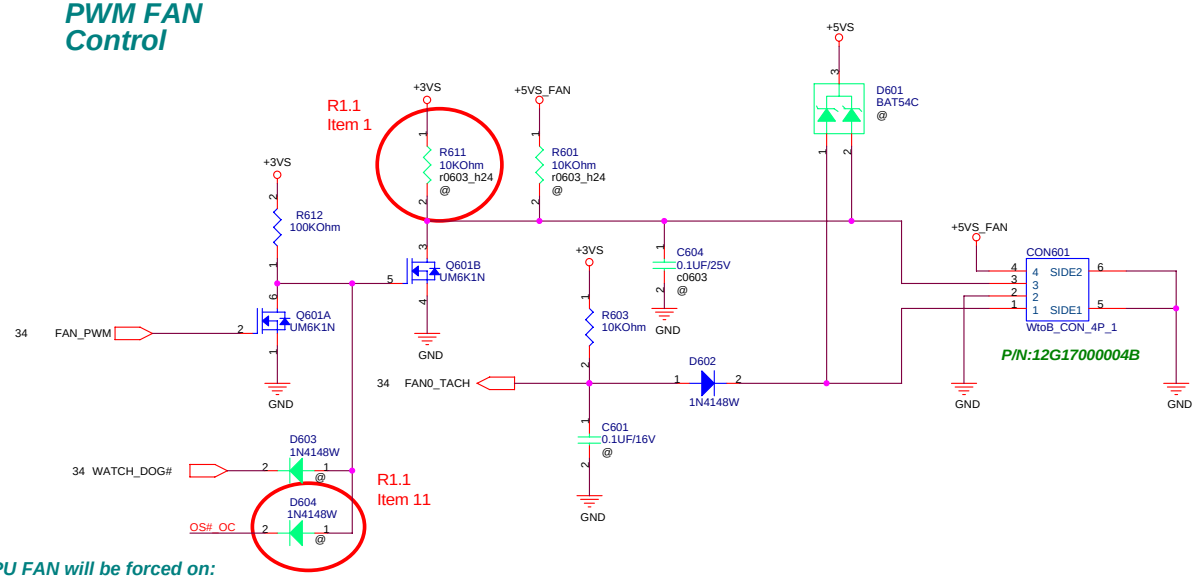
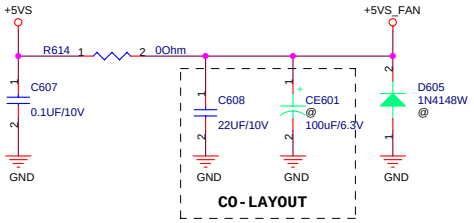
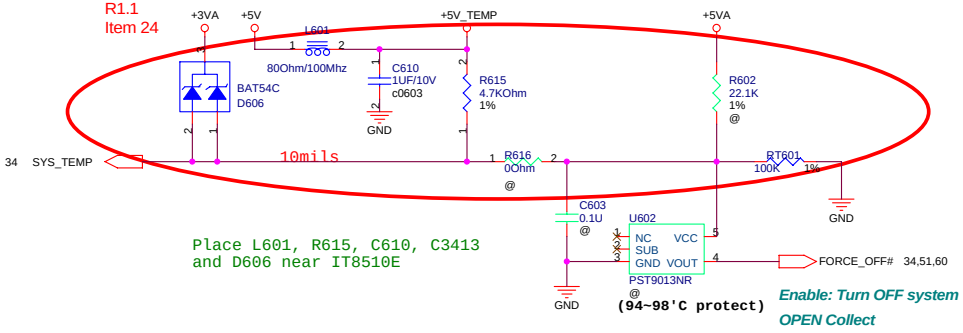
PWM FAN Control

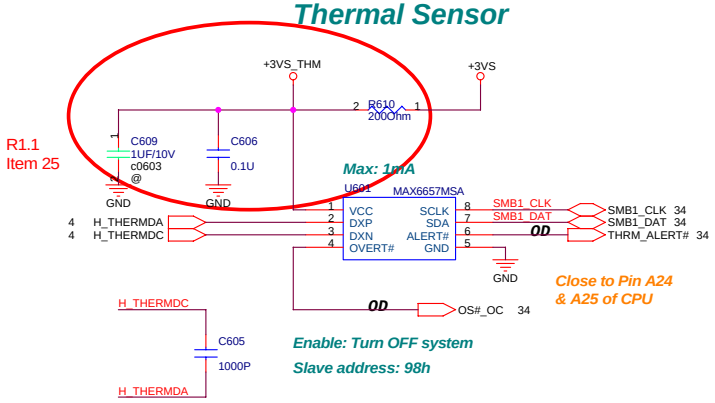


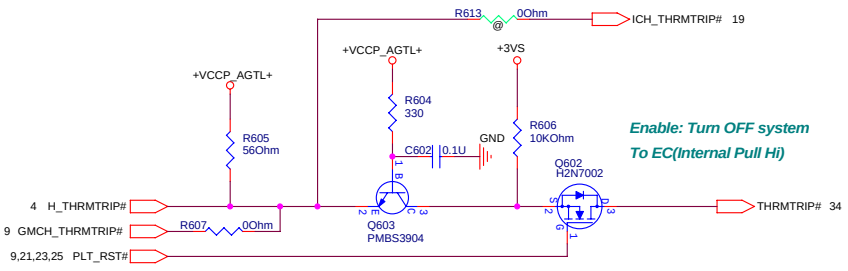


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

Thermal Sensor







<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thernal	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 6 of 63	

CPU_BSEL0 R701 1KOhm MCH_BSEL0 9
CPU_BSEL1 R702 1KOhm MCH_BSEL1 9
CPU_BSEL2 R705 1KOhm MCH_BSEL2 9

FSLC FSLB FSLA

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

PLACE termination close to source IC

CLK_MCH_BCLK R703 49.9Ohm 1%
CLK_MCH_BCLK# R704 49.9Ohm 1%
CLK_CPU_BCLK R706 49.9Ohm 1%
CLK_CPU_BCLK# R708 49.9Ohm 1%
CLK_PCIE_MINICARD R709 49.9Ohm 1%
CLK_PCIE_MINICARD# R710 49.9Ohm 1%
CLK_MCH_3GPLL R713 49.9Ohm 1%
CLK_MCH_3GPLL# R715 49.9Ohm 1%
CLK_PCIE_ICH R717 49.9Ohm 1%
CLK_PCIE_ICH# R718 49.9Ohm 1%
CLK_PCIE_NEWCARD R763 @ 49.9Ohm 1%
CLK_PCIE_NEWCARD# R750 @ 49.9Ohm 1%
CLK_PCIE_LAN R769 49.9Ohm 1%
CLK_PCIE_LAN# R770 49.9Ohm 1%
CLK_SATA_ICH R726 49.9Ohm 1%
CLK_SATA_ICH# R728 49.9Ohm 1%
DREFCLKIN R737 49.9Ohm 1%
DREFCLKIN# R741 49.9Ohm 1%
DREFSSCLKIN R744 49.9Ohm 1%
DREFSSCLKIN# R746 49.9Ohm 1%

U701 ICS954310CGLFT

VDDPCIEX1 VDDPCIEX2 VDDPCIEX3 VDDPCI1 VDDPCI2 VDD48 VDDREF
PWRSAVE# PCI/PCIEX_STOP# CPU_STOP#
VDDCPU VDDA GNDA X1 X2
27FIX/LCD_SSCGT/PCIEX0T 27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5 PCICLK4 PCICLK3 PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1 ITP_EN/PCICLK_F0 SCLK SDATA IREF
GND1 GND2 GND3 GND4 GND5 GND6 GND7
CPUCLKT1 CPUCLKC1 CPUCLKT0 CPUCLKC0 CPUCLKT2_ITP/PCIEXT8 CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7 PEREQ2#/PCIEXC7
PCIEXT6 PCIEXC6 PCIEXT5 PCIEXC5 PCIEXT4 PCIEXC4
PCIEXT3 PCIEXC3 PCIEXT2 PCIEXC2 PCIEXT1 PCIEXC1
SATACLKT SATACLKC DOTT_96MHz DOTC_96MHz
PEREQ3# PEREQ4# Vtt_PwrGd#/PD REF1/FSLC/TEST_SEL REF0

Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64

Latched Input Select

/	PIN9	PIN5	PIN17	PIN18
*	0	X	27FIX	27SS
	1	0	96MSS_T	96MSS_C
	1	1	PCIEX0_T	PCIEX0_C

From Power

PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

<Variant Name>

ASUSTeK COMPUTER INC
Title : ICS954310
Engineer: Marco Chen
Size: Custom | Project Name: T13Fv | Rev: 1.11
Date: Monday, August 28, 2006 | Sheet 7 of 63

RCOMP

For Calibrating FSB I/O Buffer

H_XRCOMP — R801 24.9Ohm 1% — GND (10/20mils)

H_YRCOMP — R802 24.9Ohm 1% — GND (10/20mils)

SCOMP

For Slew Rate Compensation on the FSB

+VCCP_AGTL+ — R804 54.9Ohm 1% — H_XSCOMP (5.5/20 mils)

+VCCP_AGTL+ — R805 54.9Ohm 1% — H_YSCOMP (5.5/20 mils)

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit

+VCCP_AGTL+ — R807 221Ohm 1% — H_XSWING (12/20mils) — R808 100Ohm 1% — GND; C801 0.1UF/16V — GND

+VCCP_AGTL+ — R809 221Ohm 1% — H_YSWING (12/20mils) — R811 100Ohm 1% — GND; C803 0.1UF/16V — GND

4 H_D#[0..63] — H_D#[0..63]

H_A#[3..31] — H_A#[3..31] 4

U801A

HOST

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	
H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
7 CLK_MCH_BCLK	AG2	H_CLKIN	
7 CLK_MCH_BCLK#	AG1	H_CLKIN#	

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
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H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
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H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	
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H_AVREF	J13	H_VREF	
H_BNR#	C6	H_BNR#	4
H_BPRI#	F6	H_BPRI#	4
H_BREQ#0	C7	H_BR0#	4
H_CPURST#	B7	H_CPURST#	4
H_DBSY#	A7	H_DBSY#	4
H_DEFER#	C3	H_DEFER#	4
H_DPWR#	J9	H_DPWR#	4
H_DRDY#	H8	H_DRDY#	4
H_DVREF	K13		
H_DINV#_0	J7	H_DINV#0	4
H_DINV#_1	W8	H_DINV#1	4
H_DINV#_2	U3	H_DINV#2	4
H_DINV#_3	AB10	H_DINV#3	4
H_DSTBN#_0	K4	H_DSTBN#0	4
H_DSTBN#_1	T7	H_DSTBN#1	4
H_DSTBN#_2	Y5	H_DSTBN#2	4
H_DSTBN#_3	AC4	H_DSTBN#3	4
H_DSTBP#_0	K3	H_DSTBP#0	4
H_DSTBP#_1	T6	H_DSTBP#1	4
H_DSTBP#_2	AA5	H_DSTBP#2	4
H_DSTBP#_3	AC5	H_DSTBP#3	4
H_HIT#	D3	H_HIT#	4
H_HITM#	D4	H_HITM#	4
H_LOCK#	B3	H_LOCK#	4
H_REQ#_0	D8	H_REQ#0	
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	
H_RS#_0	B4	H_RS#0	
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	
H_SLPCPU#	E3	R810 0Ohm	H_CPUSLP# 4,19
H_TRDY#	E7		H_TRDY# 4

H_REQ#[4..0] 4

H_RS#[0..2] 4

H_CPURST# 1 — T801 TPC28T

AGTL+ I/O Voltage Reference

+VCCP_AGTL+ — R803 100Ohm 1% — H_VREF — R806 200Ohm 1% — GND; C802 0.1UF/16V — GND

<500 mil (55 Ohm) T/B trace 5.5 , Space 25

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--CPU

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 8 of 63

011=667MHz
001=533MHz

U801B

RSVD
RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 TV_DCONSEL_0 TV_DCONSEL_1 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15

CFG
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM
PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 PM_THRMTRIP# PWROK RSTIN#

MISC
SDVO_CTRLCLK SDVO_CTRLDATA ICH_SYNC# CLK_REQ#

NC
NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

DDR MUXING
SM_CK_0 SM_CK_1 SM_CK_2 SM_CK_3 → M_CLK_DDR0 14, M_CLK_DDR1 14, M_CLK_DDR2 15, M_CLK_DDR3 15
SM_CK#_0 SM_CK#_1 SM_CK#_2 SM_CK#_3 → M_CLK_DDR#0 14, M_CLK_DDR#1 14, M_CLK_DDR#2 15, M_CLK_DDR#3 15
SM_CKE_0 SM_CKE_1 SM_CKE_2 SM_CKE_3 → M_CKE[0..3] 14,15,16
SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 → M_CS#[0..3] 14,15,16
SM_OCDCOMP_0 SM_OCDCOMP_1 → M_OCDCOMP0 R906 @ 40.2Ohm 1%, M_OCDCOMP1 R907 @ 40.2Ohm 1% → GND
SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 → M_ODT[0..3] 14,15,16
SM_RCOMP# SM_RCOMP → M_RCOMP# R908 80.6Ohm 1%, M_RCOMP R909 80.6Ohm 1% → GND
SM_VREF_0 SM_VREF_1 → VTT_REF

Layout Note: Route as short as possible.

+1.8V

CLK
G_CLKIN# G_CLKIN D_REFCLKIN# D_REFCLKIN D_REFSSCLKIN# D_REFSSCLKIN
→ CLK_MCH_3GPLL# 7, CLK_MCH_3GPLL 7, DREFCLKIN# 7, DREFCLKIN 7, DREFSSCLKIN# 7, DREFSSCLKIN 7

DMI
DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → DMI_TXN[0..3] 21
DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → DMI_TXP[0..3] 21
DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → DMI_RXN[0..3] 21
DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → DMI_RXP[0..3] 21

MCH_BSEL0 MCH_BSEL1 MCH_BSEL2
MCH_CFG_5 MCH_CFG_7 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_15 MCH_CFG_16 MCH_CFG_18 MCH_CFG_19
T901 TPC28T
PM_BMBUSY#
PM_EXTTS#0 PM_EXTTS#1
GMCH_THRMTRIP# 6
ICH7_PWROK 20,27,34
PLT_RST# 6,21,23,25
R901 100Ohm
T906 T907 T908 TPC28T
MCH_ICH_SYNC# 21

+3VS
R911 10KOhm PM_EXTTS#0
R912 10KOhm PM_EXTTS#1

VTT_REF
C901 1UF/6.3V
C902 0.1UF/16V
GND

+3VS
RN903B 10KOhm 8
RN903C 10KOhm 6
RN903D 10KOhm 4
RN903A 10KOhm 2
EDID_CLK 17
EDID_DAT 17
L_IBG
R905 1.5KOhm 1%
T902 TPC28T
L_BKLTEN_V 17
T905 TPC28T
L_VDD_EN 17
GND

U801C

LVDS
L_BKLTCTL L_BKLTEN L_CLK_CTLA L_DATA_CTLB L_DDC_CLK L_DDC_DATA L_IBG L_VBG L_VDDEN L_VREFH L_VREFL
LA_CLK# LA_CLK LB_CLK# LB_CLK
LVDS_LCLKN 17 LVDS_LCLKP 17
LA_DATA#_0 LA_DATA#_1 LA_DATA#_2
LVDS_L0N 17 LVDS_L1N 17 LVDS_L2N 17
LA_DATA_0 LA_DATA_1 LA_DATA_2
LVDS_L0P 17 LVDS_L1P 17 LVDS_L2P 17
LB_DATA#_0 LB_DATA#_1 LB_DATA#_2
LB_DATA_0 LB_DATA_1 LB_DATA_2

TV
+1.5VS
TV_DACA_OUT TV_DACB_OUT TV_DACC_OUT
TV_IREF TV_IRTNA TV_IRTNB TV_IRTNC

VGA
CRT_BLUE 18 CRT_GREEN 18 CRT_RED 18
CRT_BLUE CRT_BLUE# CRT_GREEN CRT_GREEN# CRT_RED CRT_RED#
GND
CRT_DDC_CLK 18 CRT_DDC_DATA 18 CRT_HSYNC 18 CRT_VSYNC 18
CRT_IREF
R910 255Ohm
GND

PCI-EXPRESS GRAPHICS
EXP_A_COMPI EXP_A_COMPO
PEG_COMP D40 D38 R904 24.9Ohm 1%
+1.5VS_PCIE
EXP_A_RXN_0 … EXP_A_RXN_15
EXP_A_RXP_0 … EXP_A_RXP_15
EXP_A_TXN_0 … EXP_A_TXN_15
EXP_A_TXP_0 … EXP_A_TXP_15

CRT_BLUE
CRT_GREEN
CRT_RED
+VCCP_GMCH
C905 33PF/50V c0402
C904 33PF/50V c0402
C903 33PF/50V c0402
C906 0.1UF/16V c0402 @
GND
R1.1
Item 27

Place C903, C904, C905 near NB

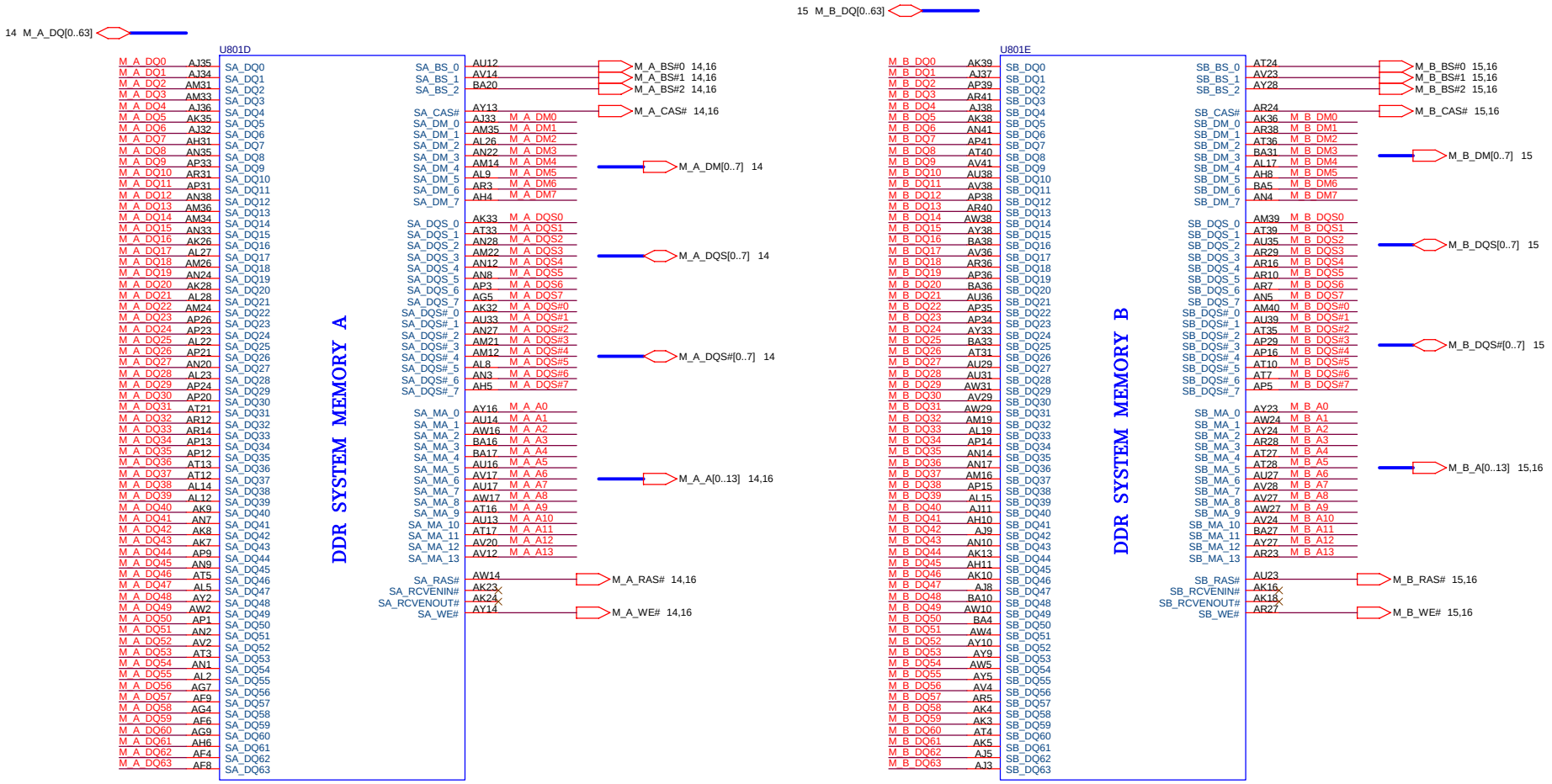
<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--PCIE
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 9 of 63



<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--DDR2

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 10 of 63

+2.5VS
C1101 10UF/6.3V
C1103 0.1UF/16V
C1104 0.022UF/16V
C1105 0.1UF/16V
GND

+1.5VS
L1101 80Ohm/100Mhz
CE1102 220UF/2V
C1106 10UF/6.3V
C1107 0.1UF/16V
+1.5VS_PCIE
GND

+1.5VS
L1102 120Ohm/100Mhz
+1.5VS_3GPLL
C1111 10UF/6.3V
C1112 0.1UF/16V
GND

+2.5VS
L1103 120Ohm/100Mhz
+VCCA_CRTDAC
C1113 0.022UF/16V
C1114 0.1UF/16V
GND

+1.5VS
C1118 0.1UF/16V
GND

+3VS
L1105 120Ohm/100Mhz
+VCCA_TVBG
C1121 0.022UF/16V
C1122 0.1UF/16V
GND

+2.5VS
R1101 10Ohm
D1101 RB717F
+VCCP_AGTL+

+3VS
R1102 10Ohm
D1102 RB717F
+1.5VS

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

+1.5VS
L1106 120Ohm/100Mhz
+1.5VS_DPLLA
C1125 10UF/10V
C1126 0.1UF/16V
GND
1.425V~1.575V
Max: 40mA

+1.5VS
L1108 120Ohm/100Mhz
+1.5VS_DPLLB
C1130 10UF/10V
C1131 0.1UF/16V
GND
1.425V~1.575V
Max: 40mA

+1.5VS
L1109 120Ohm/100Mhz
+1.5VS_HPLL
C1138 10UF/10V
C1139 0.1UF/16V
GND
1.425V~1.575V
Max: 45mA

+1.5VS
L1110 120Ohm/100Mhz
+1.5VS_MPLL
C1140 10UF/10V
C1141 0.1UF/16V
GND
1.425V~1.575V
Max: 45mA

+3VS
C1132 10UF/6.3V
C1133 0.1UF/16V
GND

+1.5VS
CE1101 220UF/2V
C1134 10UF/6.3V
C1135 0.1UF/16V
GND

NOTE:0.1UF CAPS USED IN +1.5VS, +3VS +2.5VS should be placed within 200 mils of edge.

+2.5VS
C1102 0.1UF/16V
GND

U801H

	H22	VCCSYNC	
+2.5VS	C30	VCC_TXLVDS0	
	B30	VCC_TXLVDS1	
	A30	VCC_TXLVDS2	
+1.5VS_PCIE	AJ41	VCC3G0	
	AB41	VCC3G1	
	Y41	VCC3G2	
	V41	VCC3G3	
	R41	VCC3G4	
	N41	VCC3G5	
	L41	VCC3G6	
+1.5VS_3GPLL	AC33	VCCA_3GPLL	
+2.5VS	G41	VCCA_3GBG	
GND	H41	VSSA_3GBG	
+VCCA_CRTDAC	F21	VCCA_CRTDAC0	
	E21	VCCA_CRTDAC1	
GND R1103 10Ohm	G21	VSSA_CRTDAC	
+1.5VS_DPLLA	B26	VCCA_DPLLA	
+1.5VS_DPLLB	C39	VCCA_DPLLB	
+1.5VS_HPLL	AF1	VCCA_HPLL	
+2.5VS	A38	VCCA_LVDS	
GND	B39	VSSA_LVDS	
+1.5VS_MPLL	AF2	VCCA_MPLL	
+1.5VS	H20	VCCA_TVBG	
GND	G20	VSSA_TVBG	
+1.5VS	E19	VCCA_TVDACA0	
	F19	VCCA_TVDACA1	
	C20	VCCA_TVDACB0	
	D20	VCCA_TVDACB1	
	E20	VCCA_TVDACC0	
	F20	VCCA_TVDACC1	
+1.5VS	AH1	VCCD_HMPLL0	
	AH2	VCCD_HMPLL1	
+1.5VS	A28	VCCD_LVDS0	
	B28	VCCD_LVDS1	
	C28	VCCD_LVDS2	
+1.5VS	D21	VCCD_TVDAC	
+3VS	A23	VCC_HV0	
	B23	VCC_HV1	
	B25	VCC_HV2	
+1.5VS	H19	VCCD_QTVDAC	
+1.5VS	AK31	VCCAUX0	
	AF31	VCCAUX1	
	AE31	VCCAUX2	
	AC31	VCCAUX3	
	AL30	VCCAUX4	
	AK30	VCCAUX5	
	AJ30	VCCAUX6	
	AH30	VCCAUX7	
	AG30	VCCAUX8	
	AF30	VCCAUX9	
	AE30	VCCAUX10	
	AD30	VCCAUX11	
	AC30	VCCAUX12	
	AG29	VCCAUX13	
	AF29	VCCAUX14	
	AE29	VCCAUX15	
	AD29	VCCAUX16	
	AC29	VCCAUX17	
	AG28	VCCAUX18	
	AF28	VCCAUX19	
	AE28	VCCAUX20	
	AH22	VCCAUX21	
	AJ21	VCCAUX22	
	AH21	VCCAUX23	
	AJ20	VCCAUX24	
	AH20	VCCAUX25	
	AH19	VCCAUX26	
	P19	VCCAUX27	
	P16	VCCAUX28	
	AH15	VCCAUX29	
	P15	VCCAUX30	
	AH14	VCCAUX31	
	AG14	VCCAUX32	
	AF14	VCCAUX33	
	AE14	VCCAUX34	
	Y14	VCCAUX35	
	AF13	VCCAUX36	
	AE13	VCCAUX37	
	AF12	VCCAUX38	
	AE12	VCCAUX39	
	AD12	VCCAUX40	

R1.1
Item 27

1.425V~1.575V
Max: 1.5A

POWER

+VCCP_AGTL+

VTT_0	AC14	
VTT_1	AB14	
VTT_2	W14	
VTT_3	Y14	
VTT_4	T14	
VTT_5	R14	
VTT_6	P14	
VTT_7	N14	
VTT_8	M14	
VTT_9	L14	
VTT_10	AD13	
VTT_11	AC13	
VTT_12	AB13	
VTT_13	AA13	
VTT_14	Y13	
VTT_15	W13	
VTT_16	V13	
VTT_17	U13	
VTT_18	T13	
VTT_19	R13	
VTT_20	N13	
VTT_21	M13	
VTT_22	L13	
VTT_23	AB12	
VTT_24	AA12	
VTT_25	Y12	
VTT_26	W12	
VTT_27	V12	
VTT_28	U12	
VTT_29	T12	
VTT_30	R12	
VTT_31	P12	
VTT_32	N12	
VTT_33	M12	
VTT_34	L12	
VTT_35	R11	
VTT_36	P11	
VTT_37	N11	
VTT_38	M11	
VTT_39	R10	
VTT_40	P10	
VTT_41	N10	
VTT_42	M10	
VTT_43	P9	
VTT_44	N9	
VTT_45	M9	
VTT_46	R8	
VTT_47	P8	
VTT_48	N8	
VTT_49	M8	
VTT_50	P7	
VTT_51	N7	
VTT_52	M7	
VTT_53	R6	
VTT_54	P6	
VTT_55	M6	
VTT_56	A6	VTTLF_CAP3
VTT_57	R5	
VTT_58	P5	
VTT_59	N5	
VTT_60	M5	
VTT_61	P4	
VTT_62	N4	
VTT_63	M4	
VTT_64	R3	
VTT_65	P3	
VTT_66	N3	
VTT_67	M3	
VTT_68	R2	
VTT_69	P2	
VTT_70	M2	
VTT_71	D2	VTTLF_CAP2
VTT_72	AB1	VTTLF_CAP1
VTT_73	R1	
VTT_74	P1	
VTT_75	N1	
VTT_76	M1	

C1129 0.47UF/16V GND

C1136 0.47UF/16V GND
C1137 0.1UF/16V GND

0.9475V~1.1025V
Max: 1.4A

PLACE IN CAVITY
C1108 0.47UF/16V
C1109 10UF/6.3V
GND

PLACE ON THE EDGE
+VCCP_AGTL+
C1110 0.1UF/16V
CE1103 220UF/2V
GND

<Variant Name>

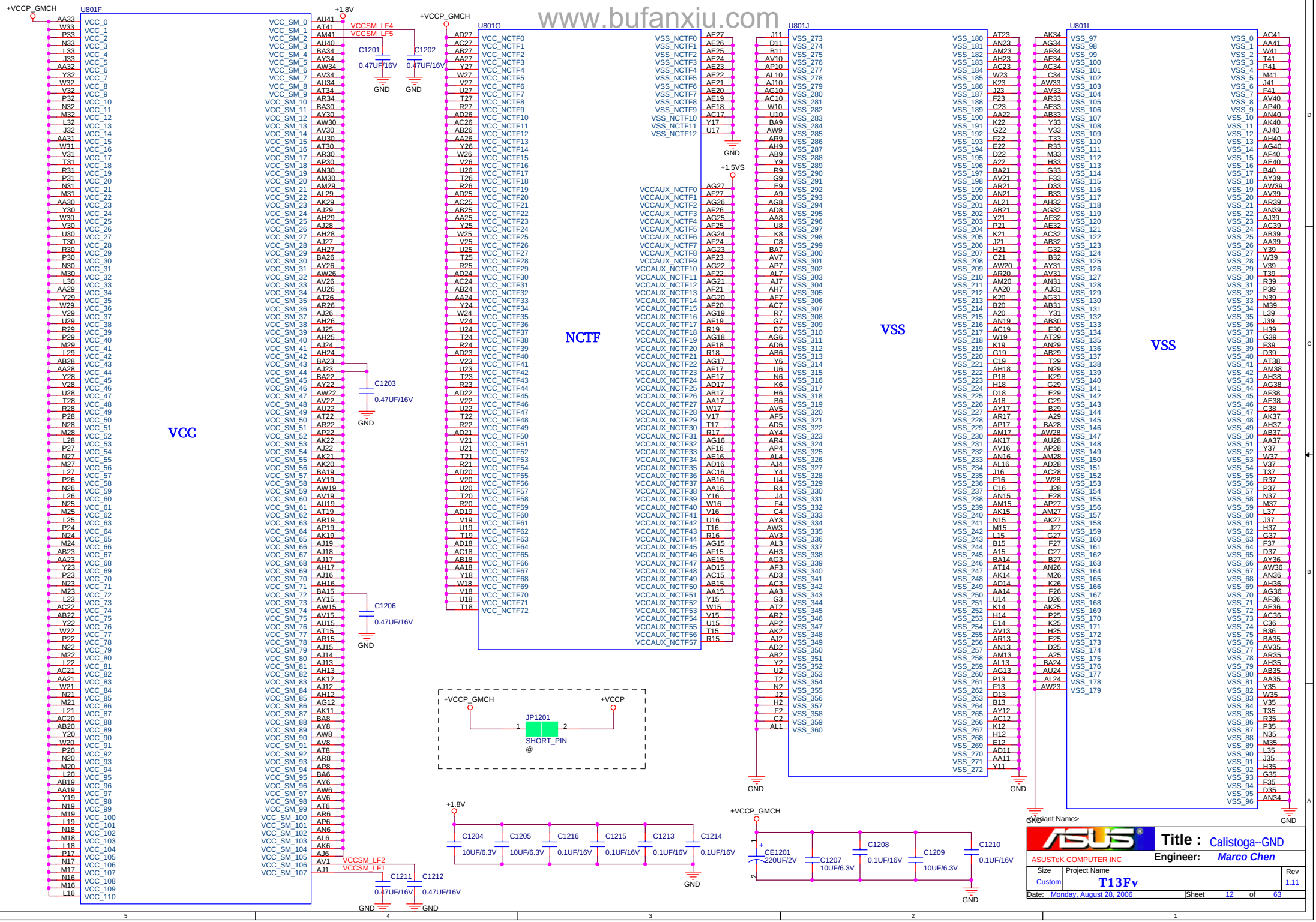
ASUSTeK COMPUTER INC

Title : Calistoga--POWER

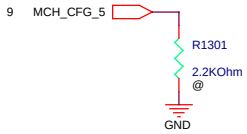
Engineer: *Marco Chen*

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 11 of 63

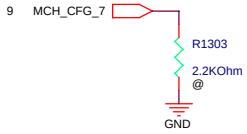


Variant Name>			
ASUSTeK COMPUTER INC	Title : Calistoga--GND		
	Engineer: Marco Chen		
Size: Custom	Project Name: T13Fv		Rev: 1.11
Date: Monday, August 28, 2006	Sheet 12 of 63		



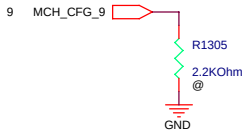
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



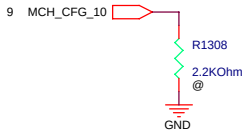
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



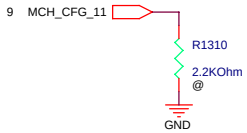
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

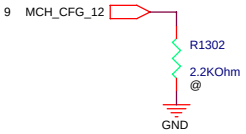
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

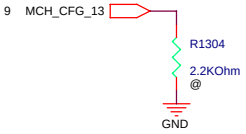
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

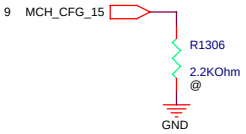
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG[13:12] : GMCH TEST MODE SELECT

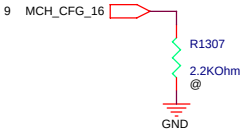
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)





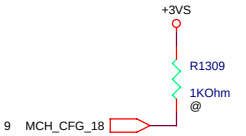
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



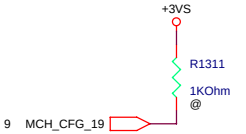
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga--Strap	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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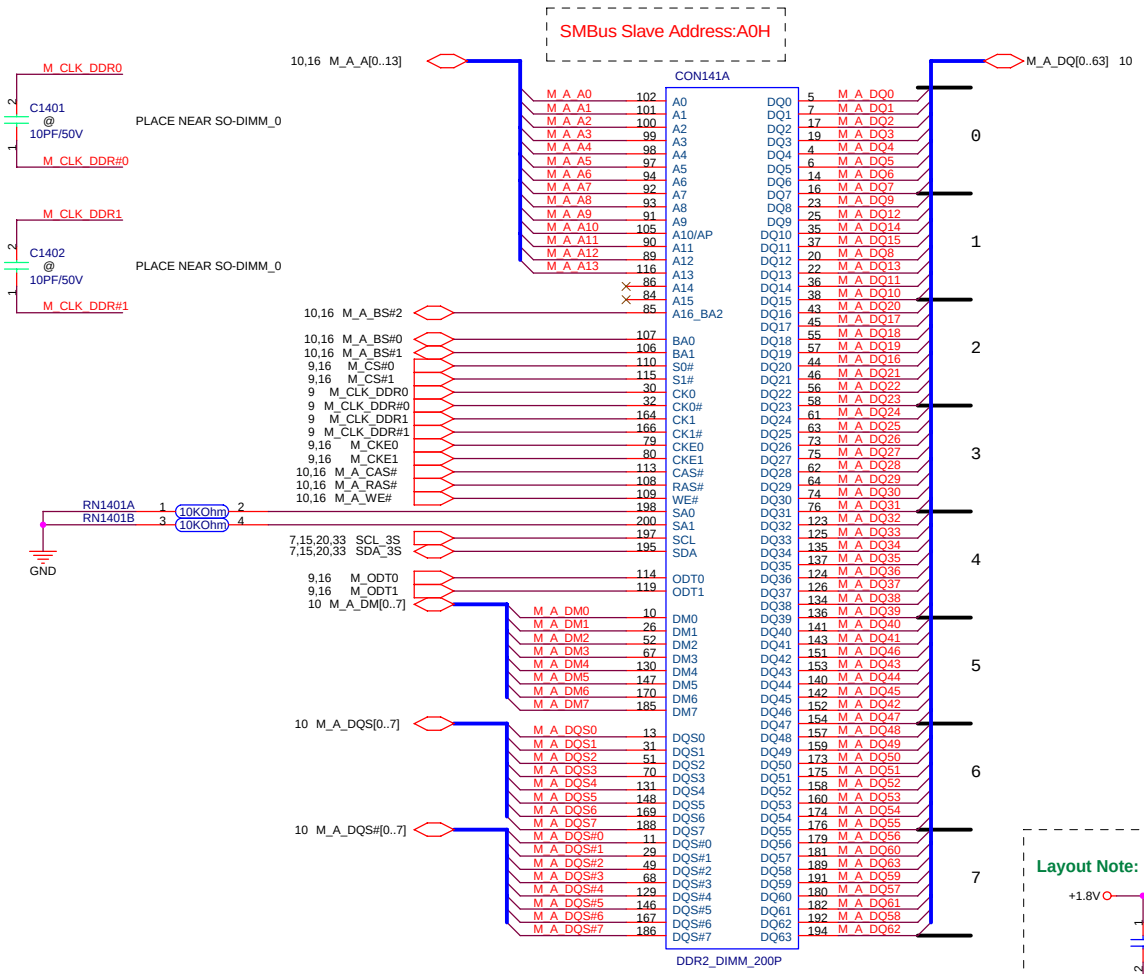
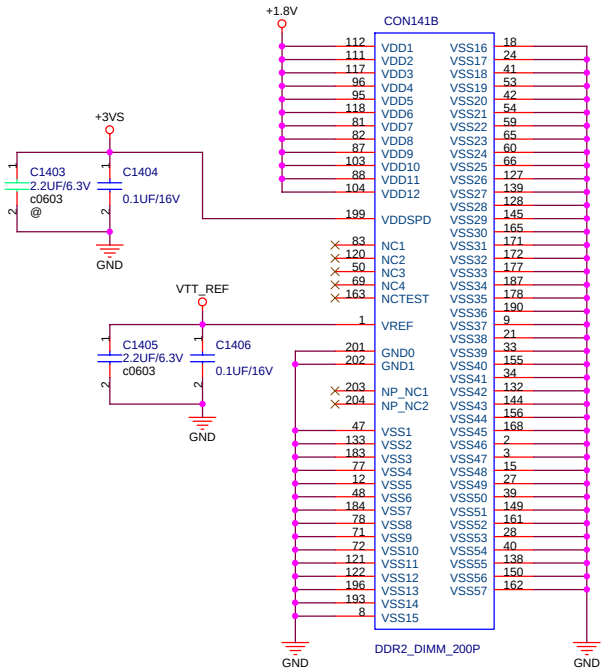
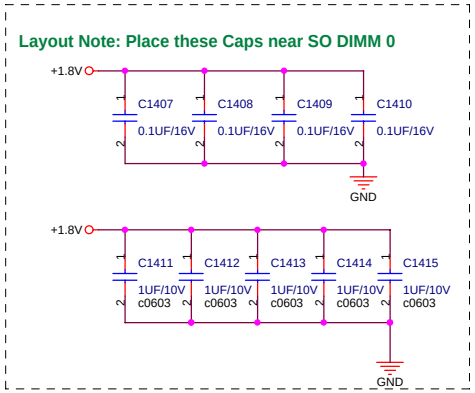
DDR2 HAD SWAPED.



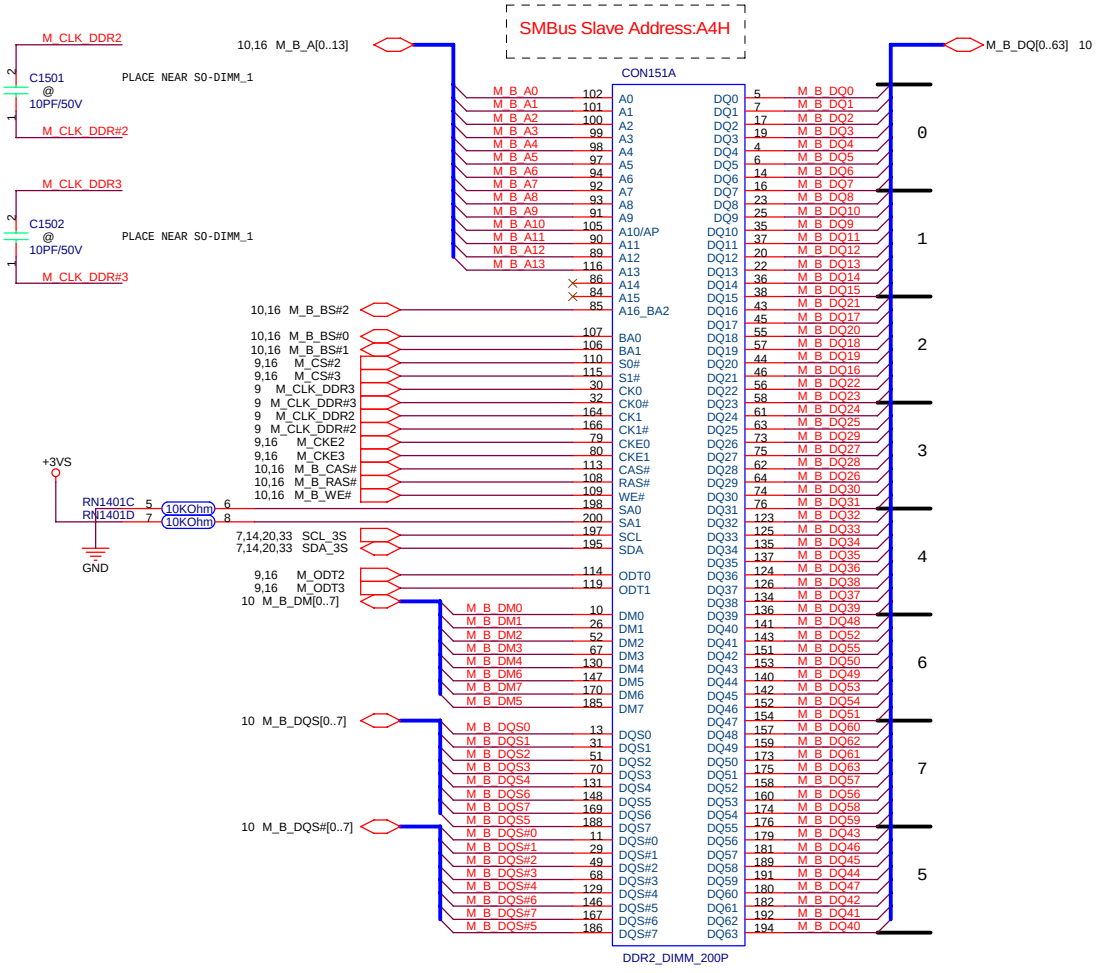




<Variant Name>

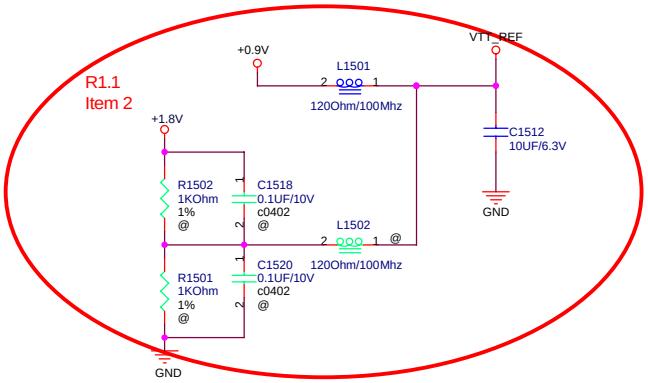
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 14 of 63	

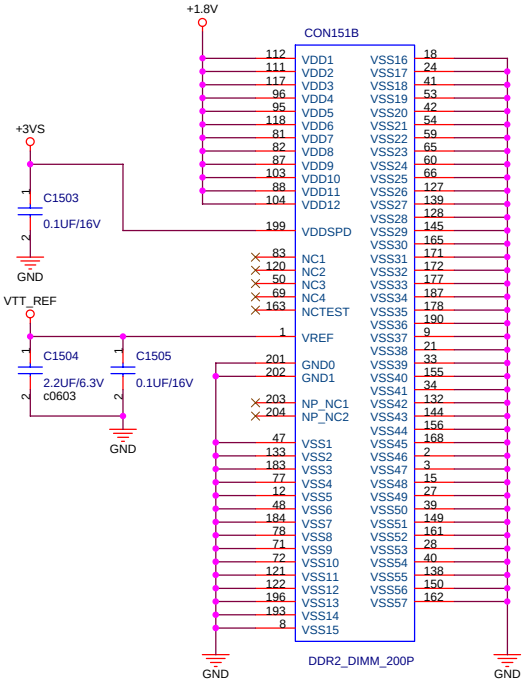
DDR2 HAD SWAPED.

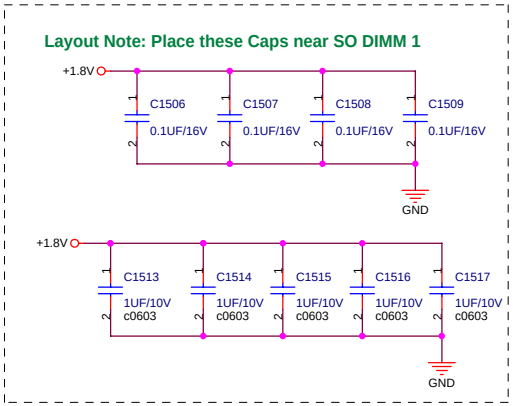


Hight: 9.2 mm

P/N:12G025C22004







<Variant Name>

ASUSTeK COMPUTER INC

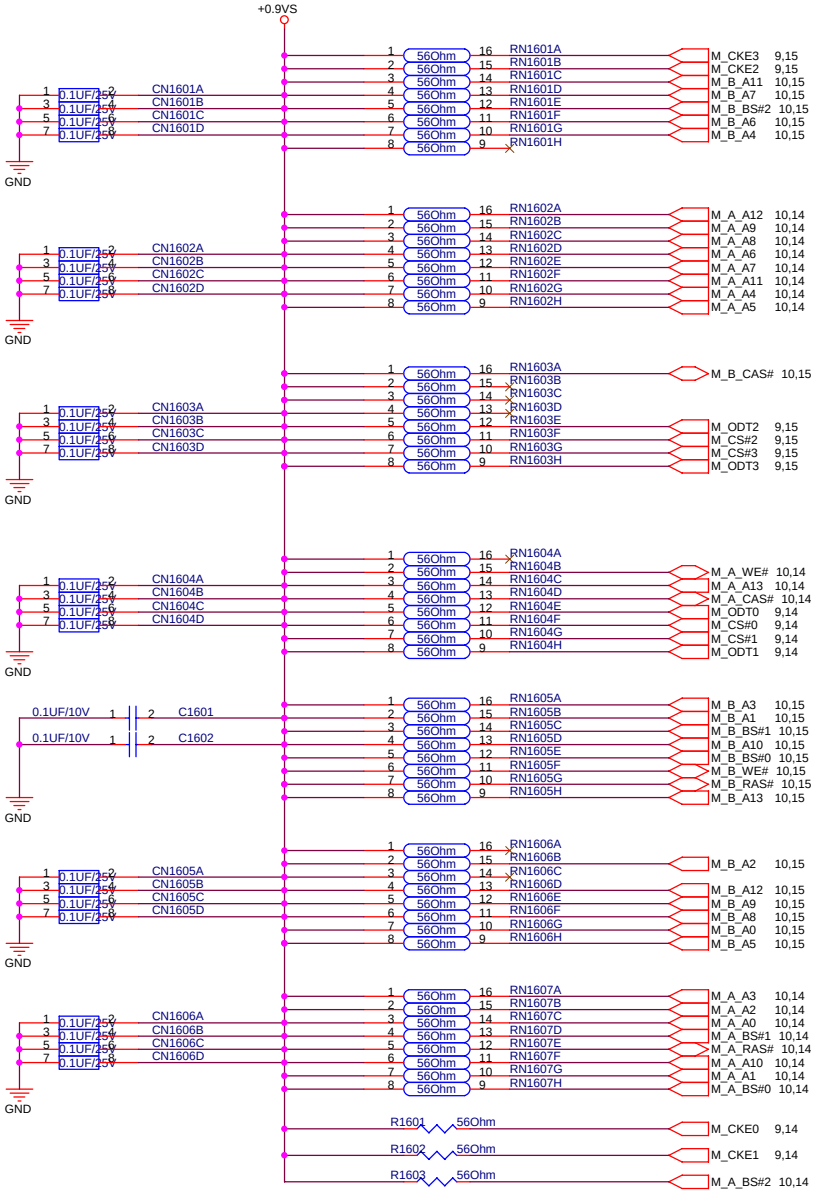
Title : DDR2 SO-DIMM_1

Engineer: *Marco Chen*

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 15 of 63

DDR2 HAD SWAPED.



Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 TERMINATION

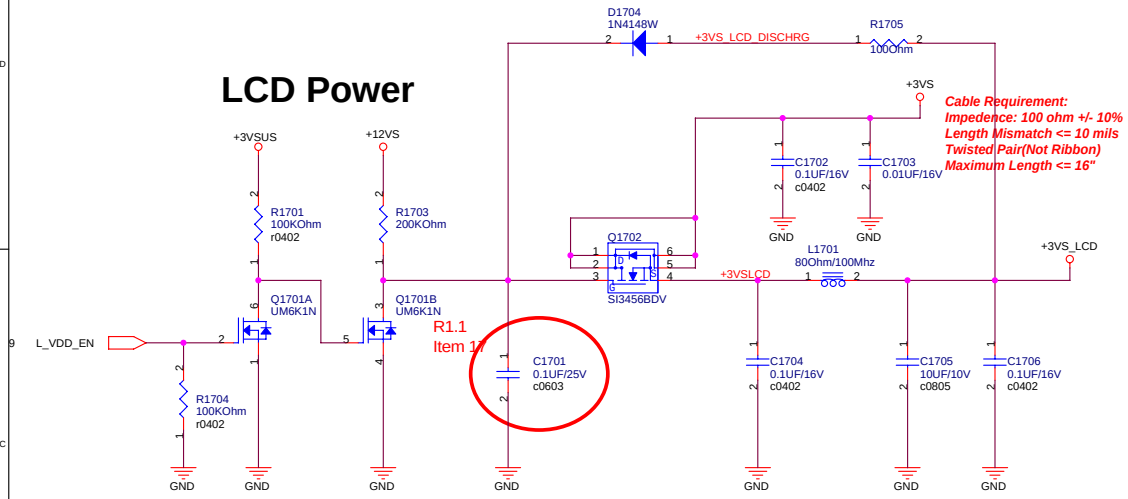
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 16 of 63

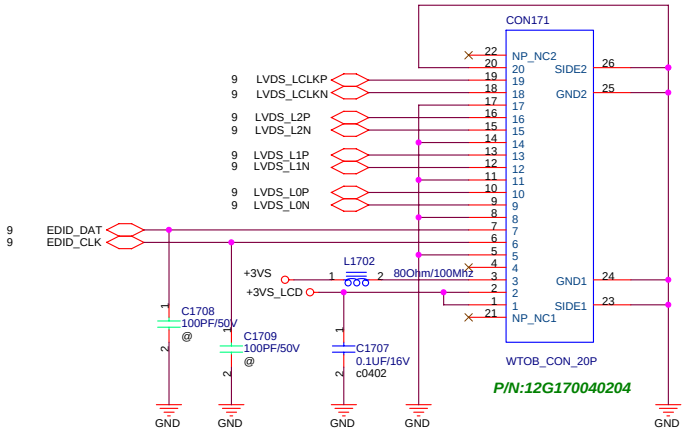
LCD Backlight Control

LCD Power

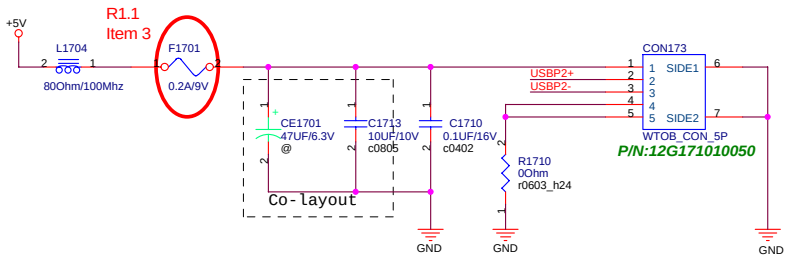


PR_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

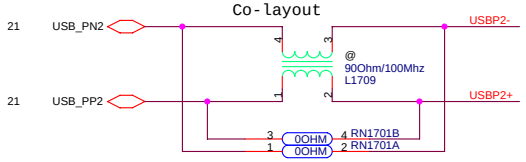
LCD LVDS Interface



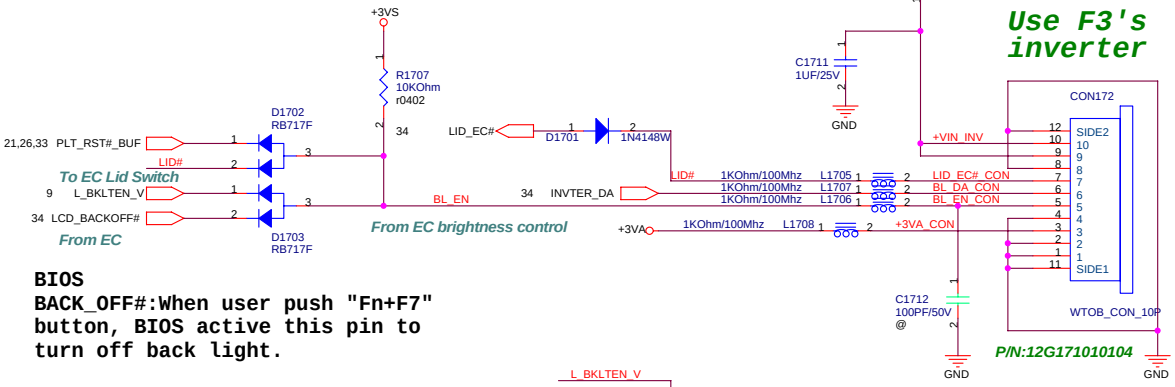
CCD connecter



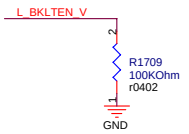
FOR EMI
Co-layout



Inverter connecter



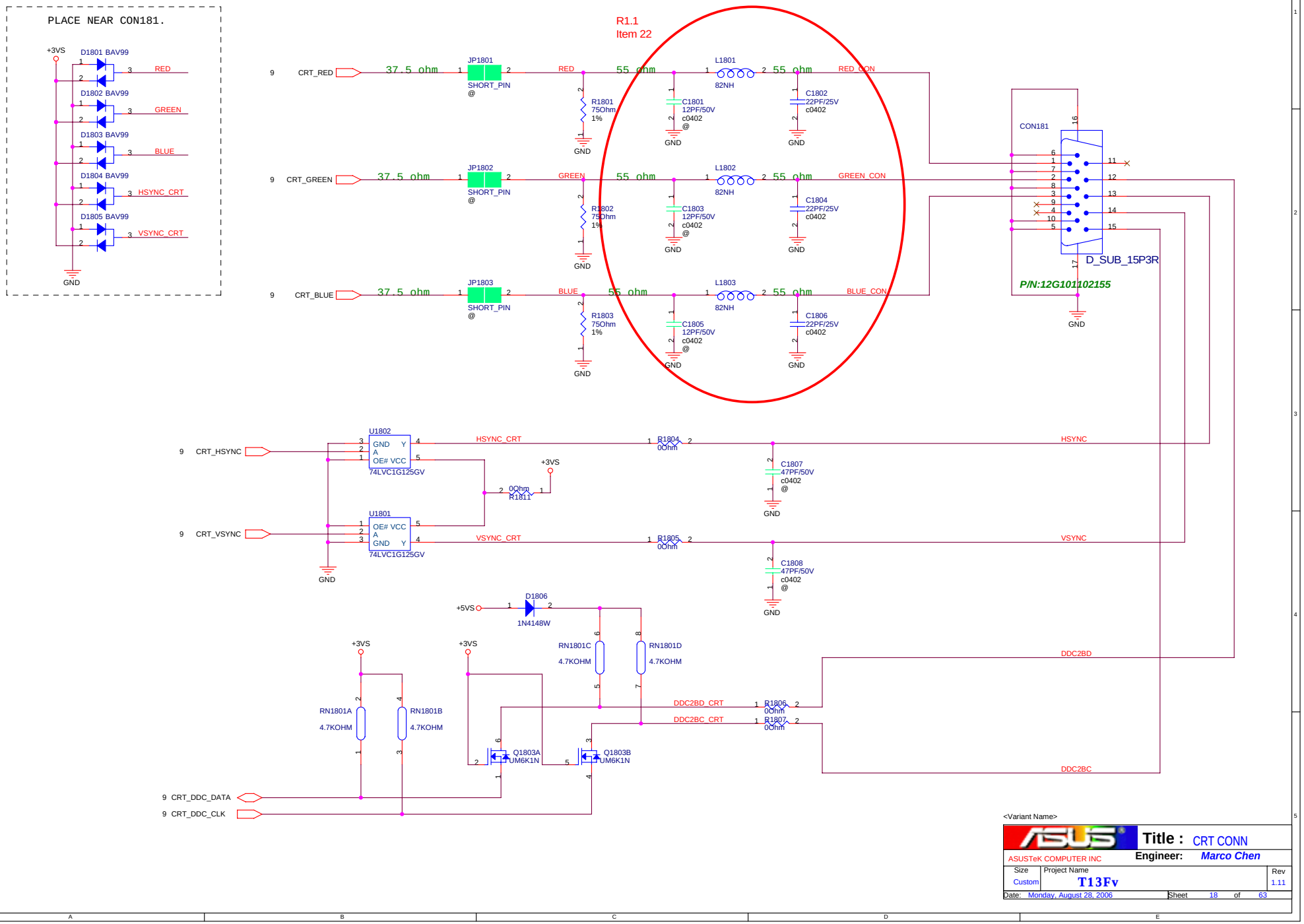
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



<Variant Name>

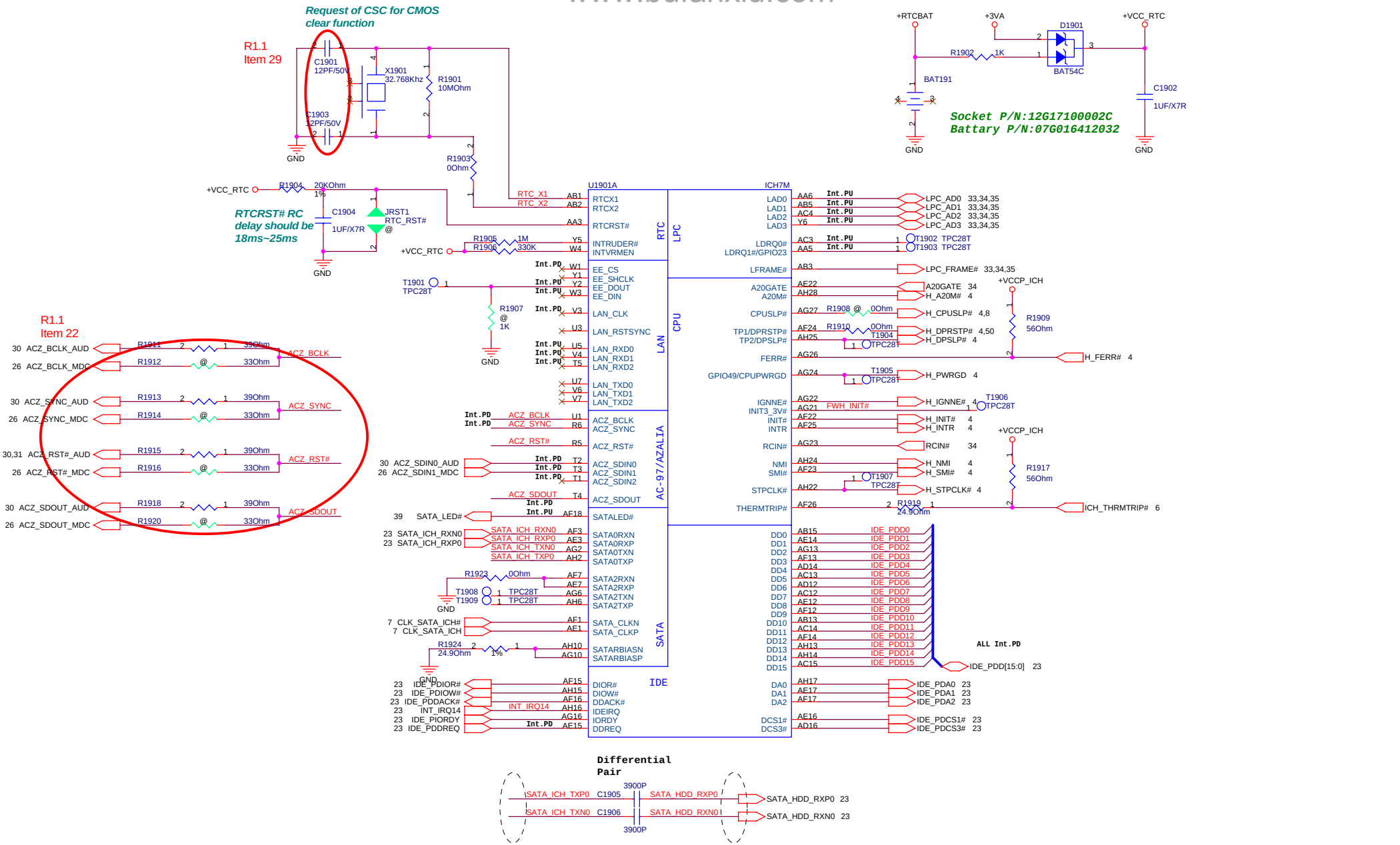
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 17 of 63	

CRT



<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT CONN	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 18 of 63	



<Variant Name>

ASUSTeK COMPUTER INC	Title : ICH7M (1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 19 of 63	

To new card check power plane

Clock Generator
DDR2 SO-DIMM

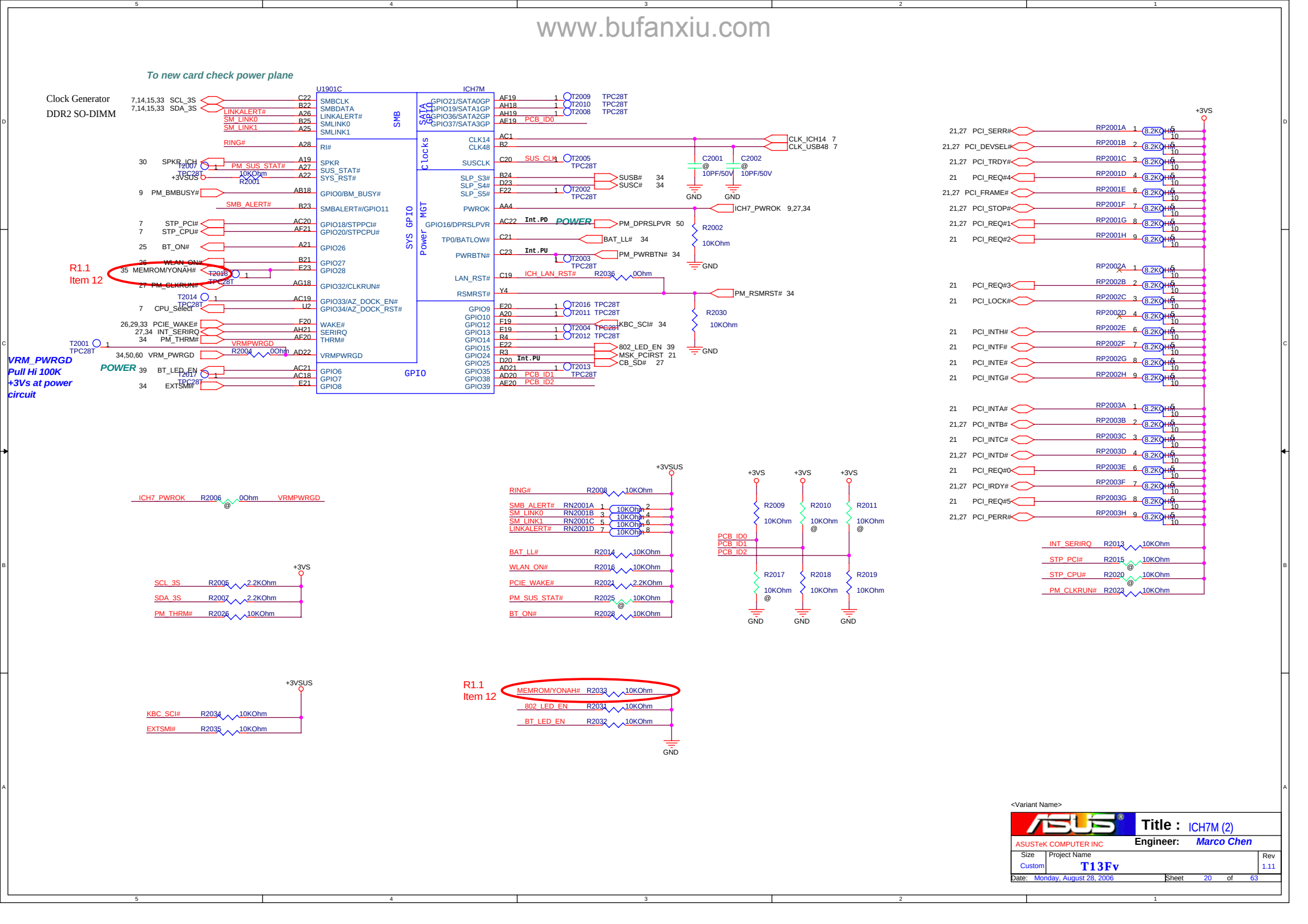
U1901C

ICH7M

R1.1
Item 12

VRM_PWRGD
Pull Hi 100K
+3Vs at power
circuit

POWER



<Variant Name>

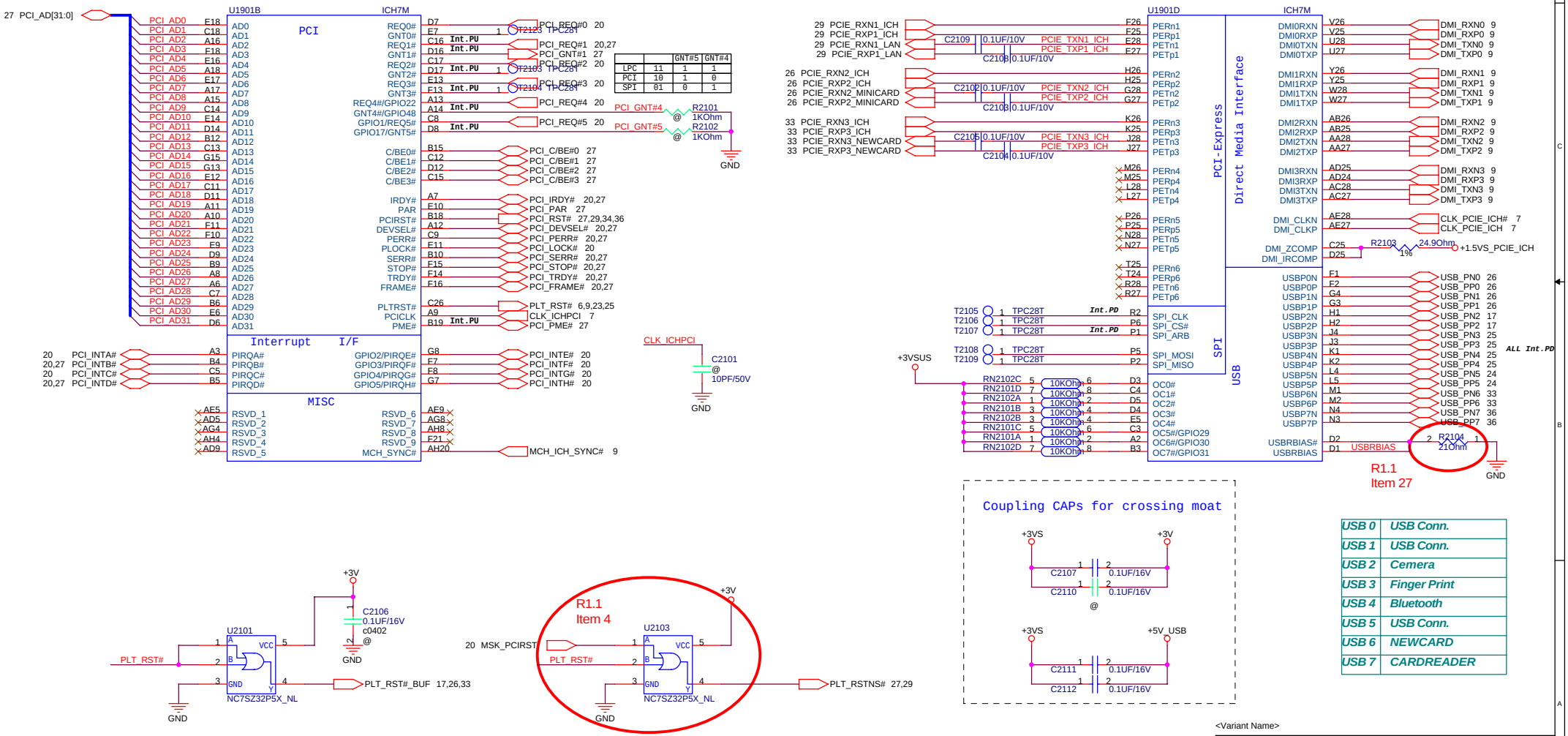
ASUSTeK COMPUTER INC

Title : ICH7M (2)

Engineer: *Marco Chen*

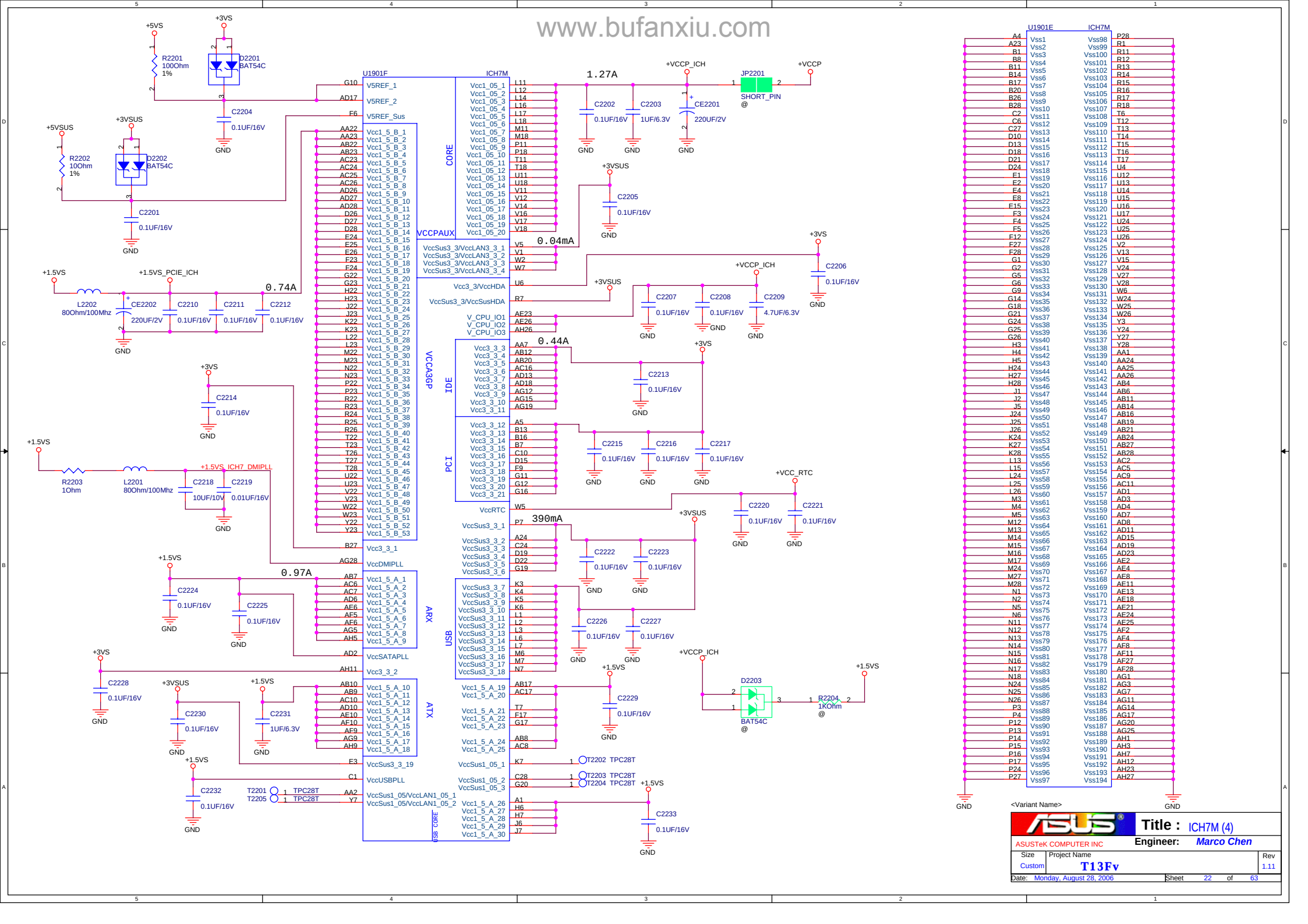
Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 20 of 63

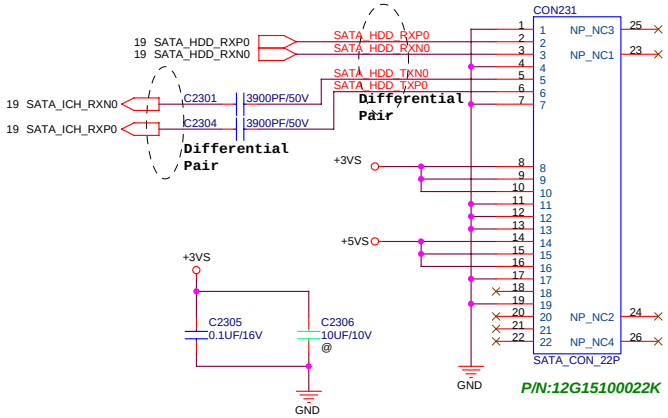


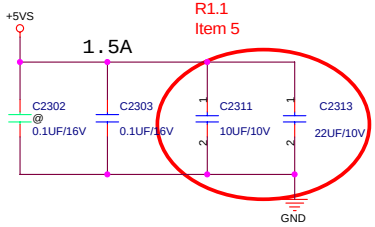
		GNT#5	GNT#4
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER

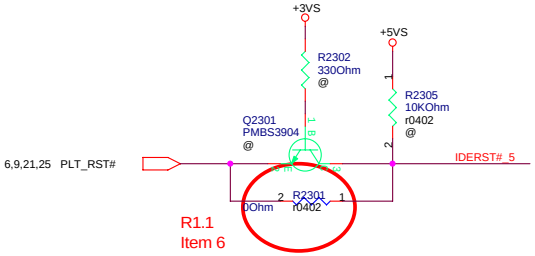


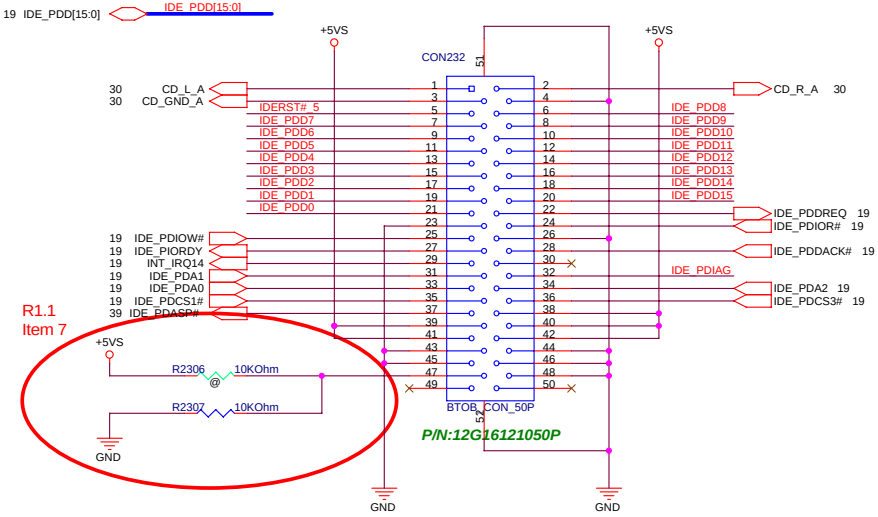
SATA HDD CON

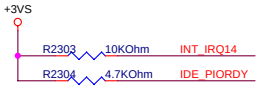


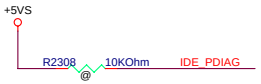


PATA ODD CON

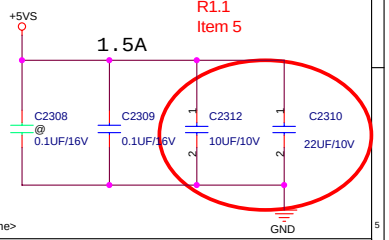






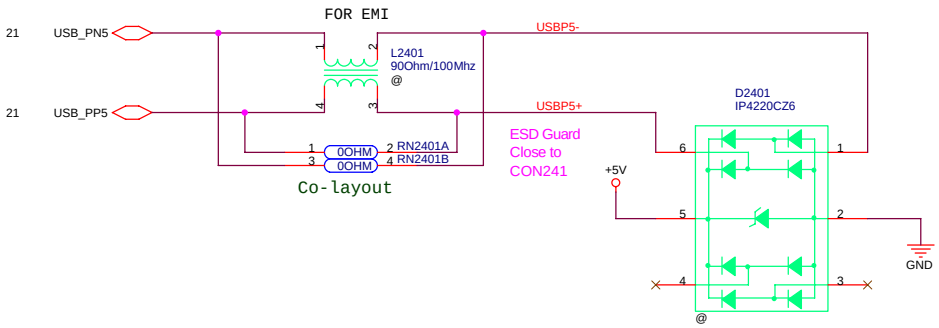


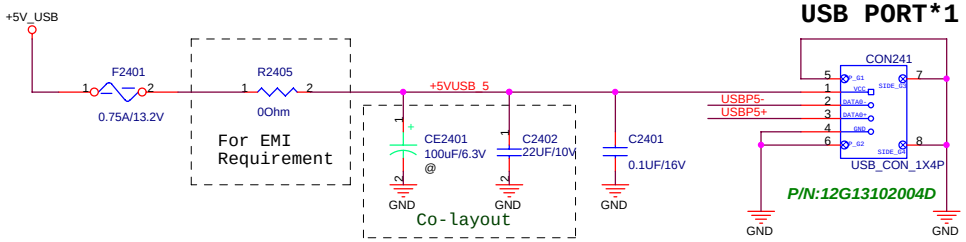
Normal type
High: Slave
Low : Master

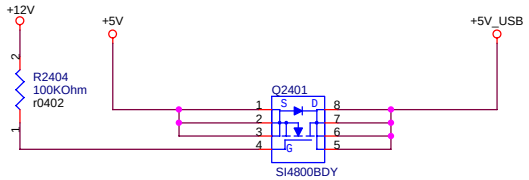


<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & ODD	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 23 of 63	

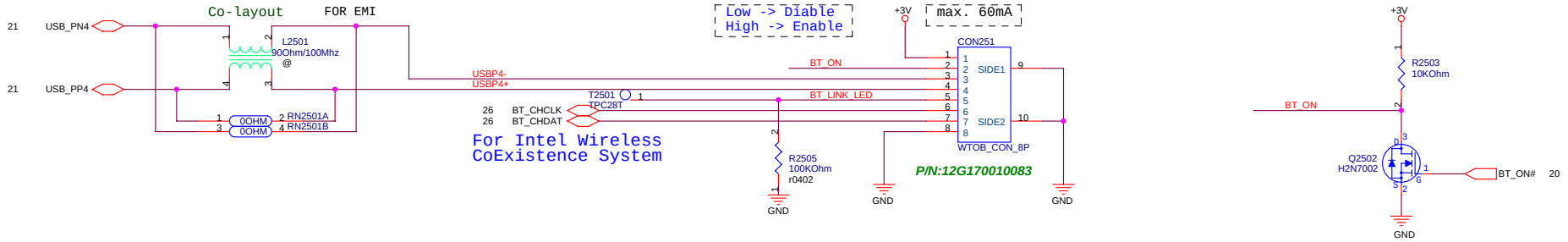




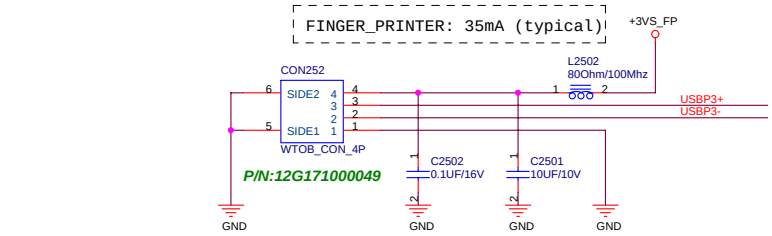


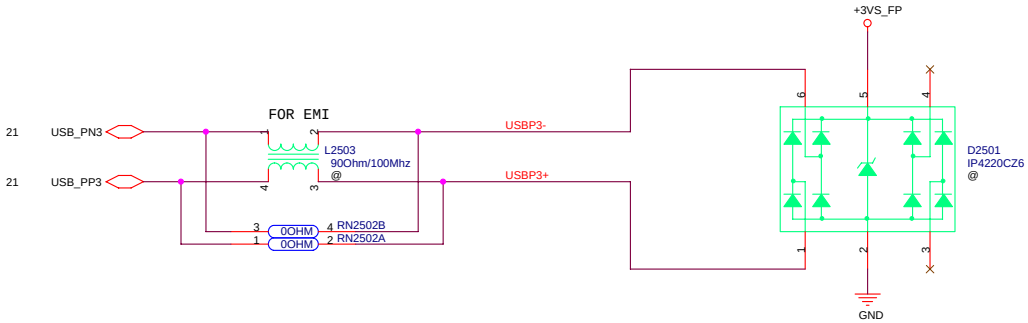
<Variant Name>

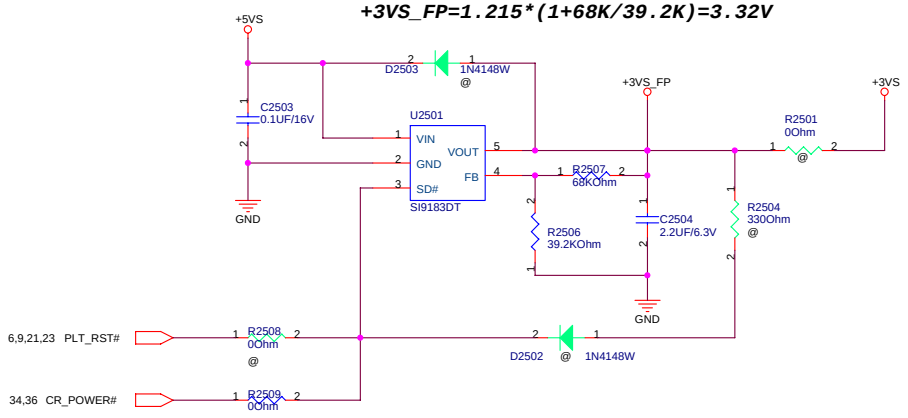
ASUSTeK COMPUTER INC	Title : USB PORT	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 24 of 63	



Finger Printer







<Variant Name>

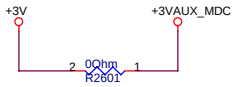
ASUSTeK COMPUTER INC	Title : BT & FP	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 25 of 63	

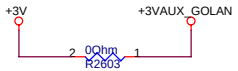
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

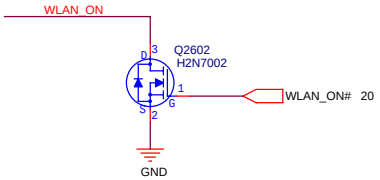
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA





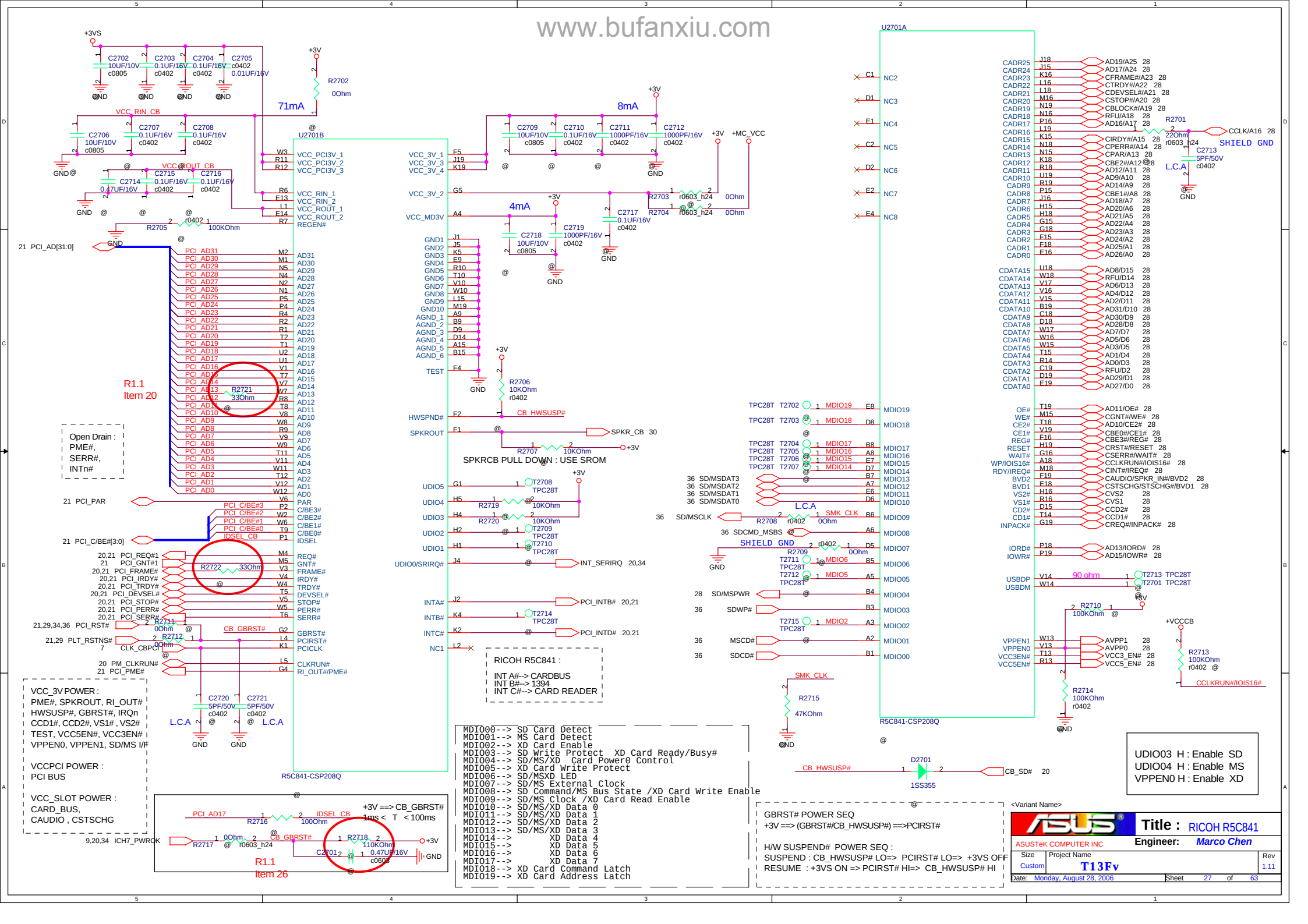
Intel SPEC(18780):Internal
Pull UP 110Kohm

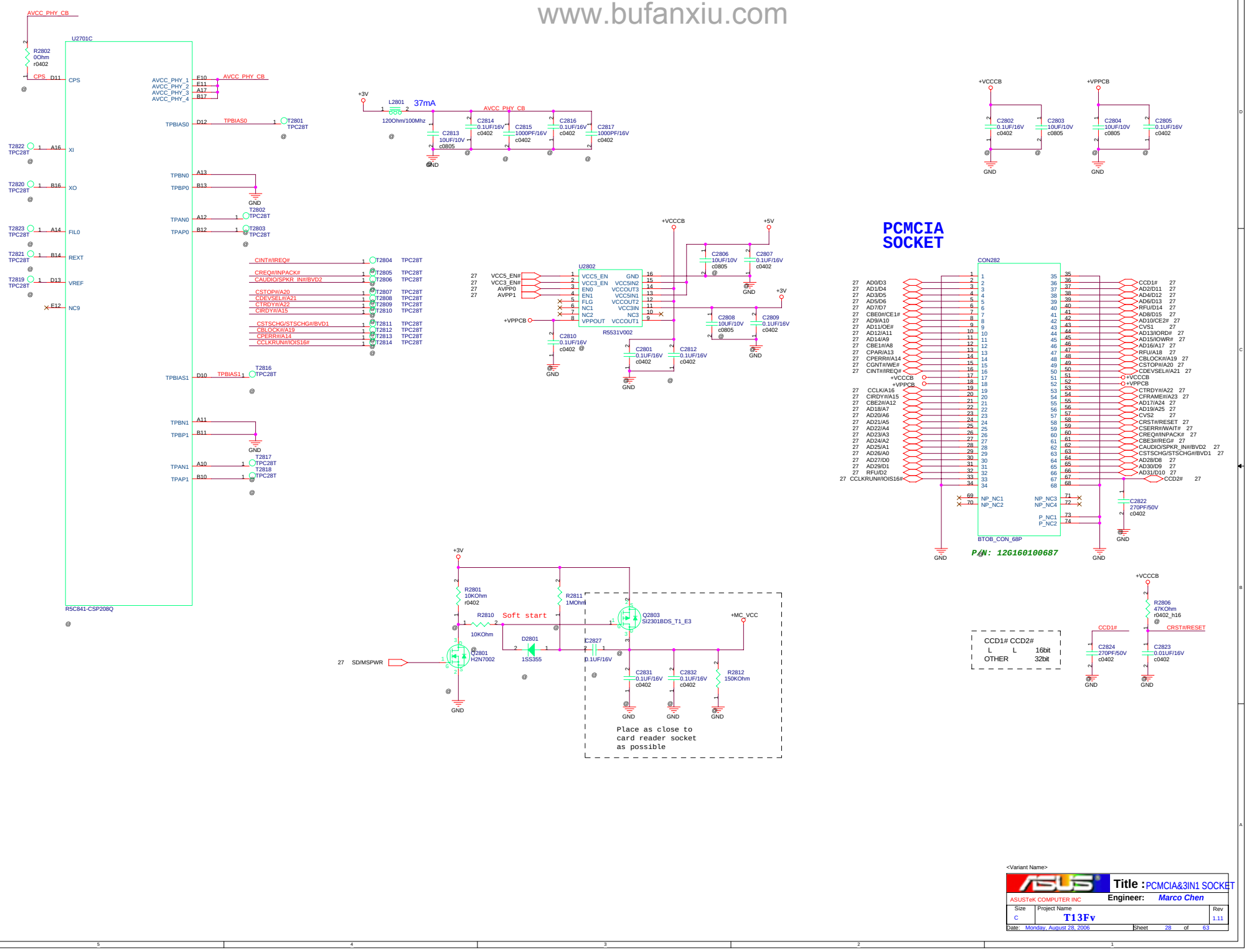


P/N:12G061200504

<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: *Marco Chen*	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 26 of 63	





<Variant Name>

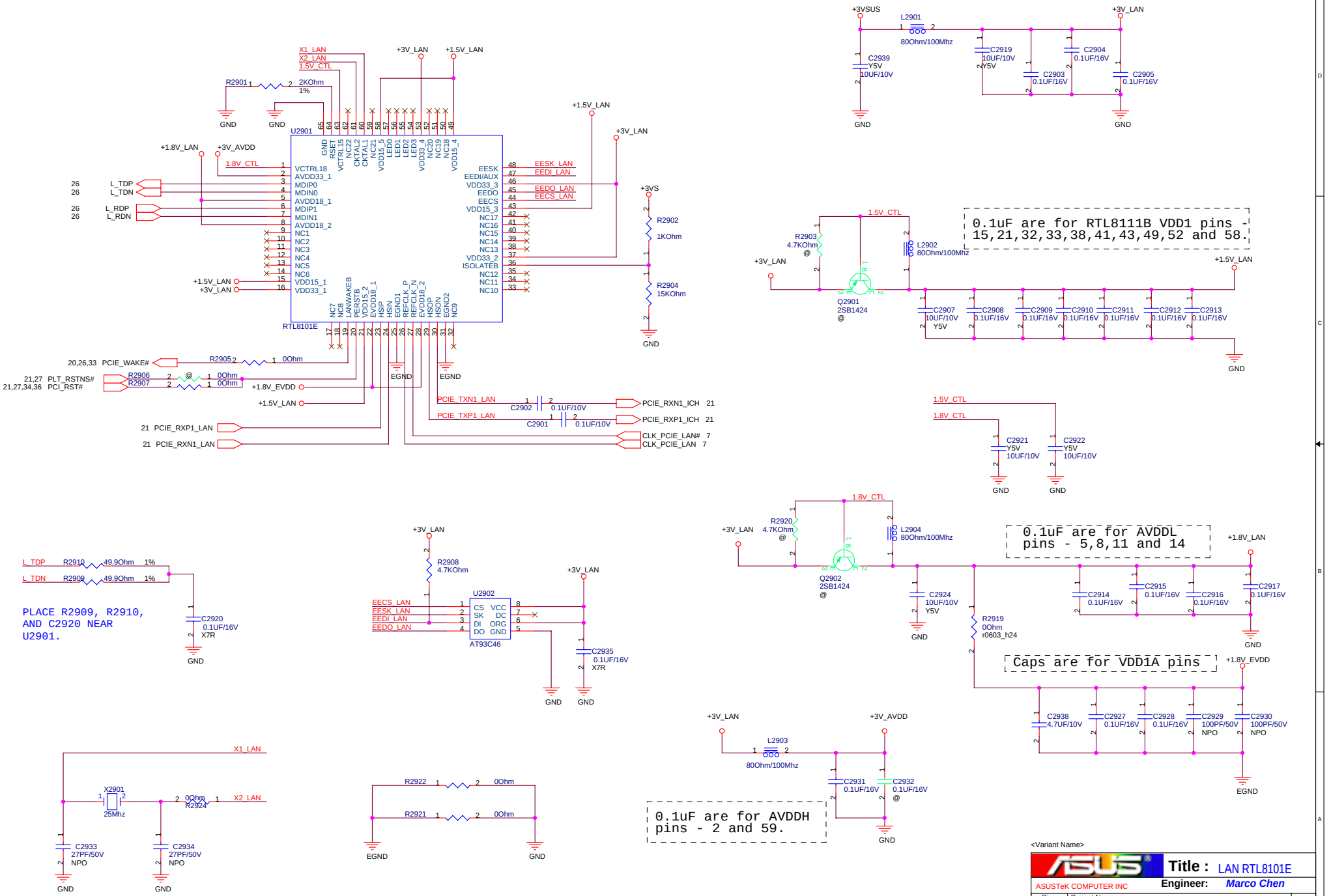
ASUSTeK COMPUTER INC

Title : PCMCIA&3IN1 SOCKET

Engineer: Marco Chen

Size	Project Name	Rev
C	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 28 of 63



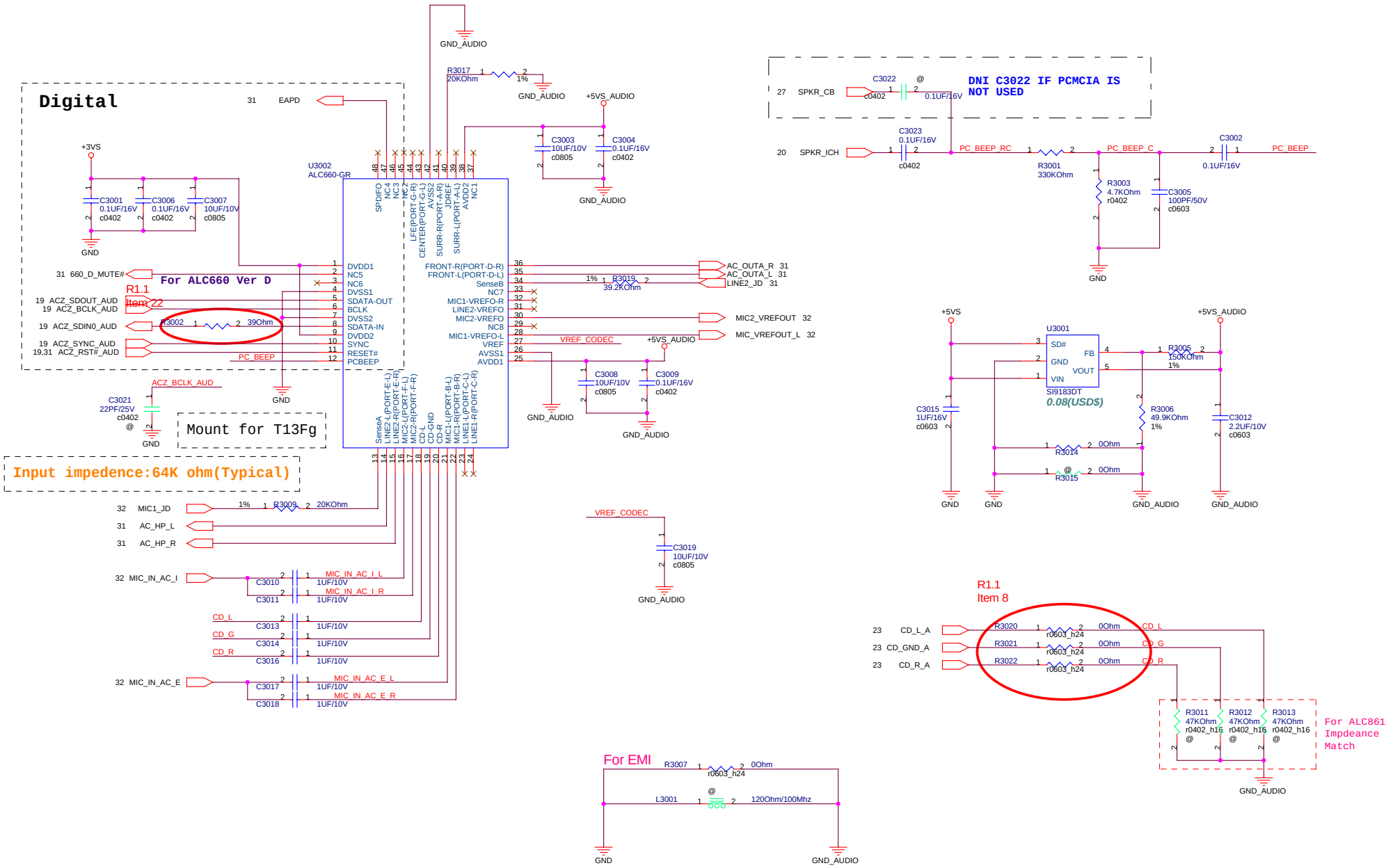
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.

0.1uF are for AVDDL pins - 5,8,11 and 14

Caps are for VDD1A pins

PLACE R2909, R2910, AND C2920 NEAR U2901.

0.1uF are for AVDDH pins - 2 and 59.



<Variant Name>

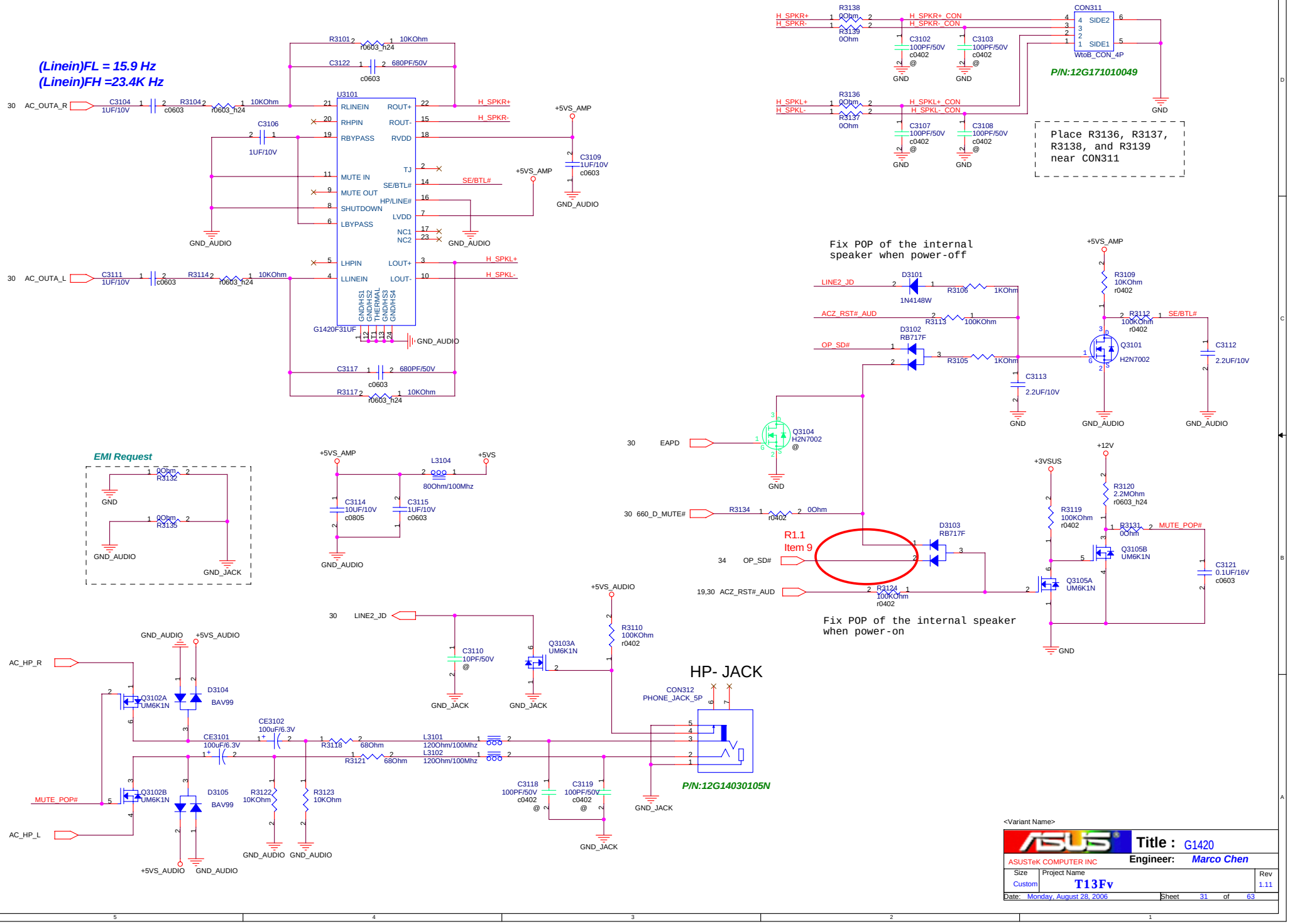
Title : ALC660-GR

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 30 of 63



<Variant Name>

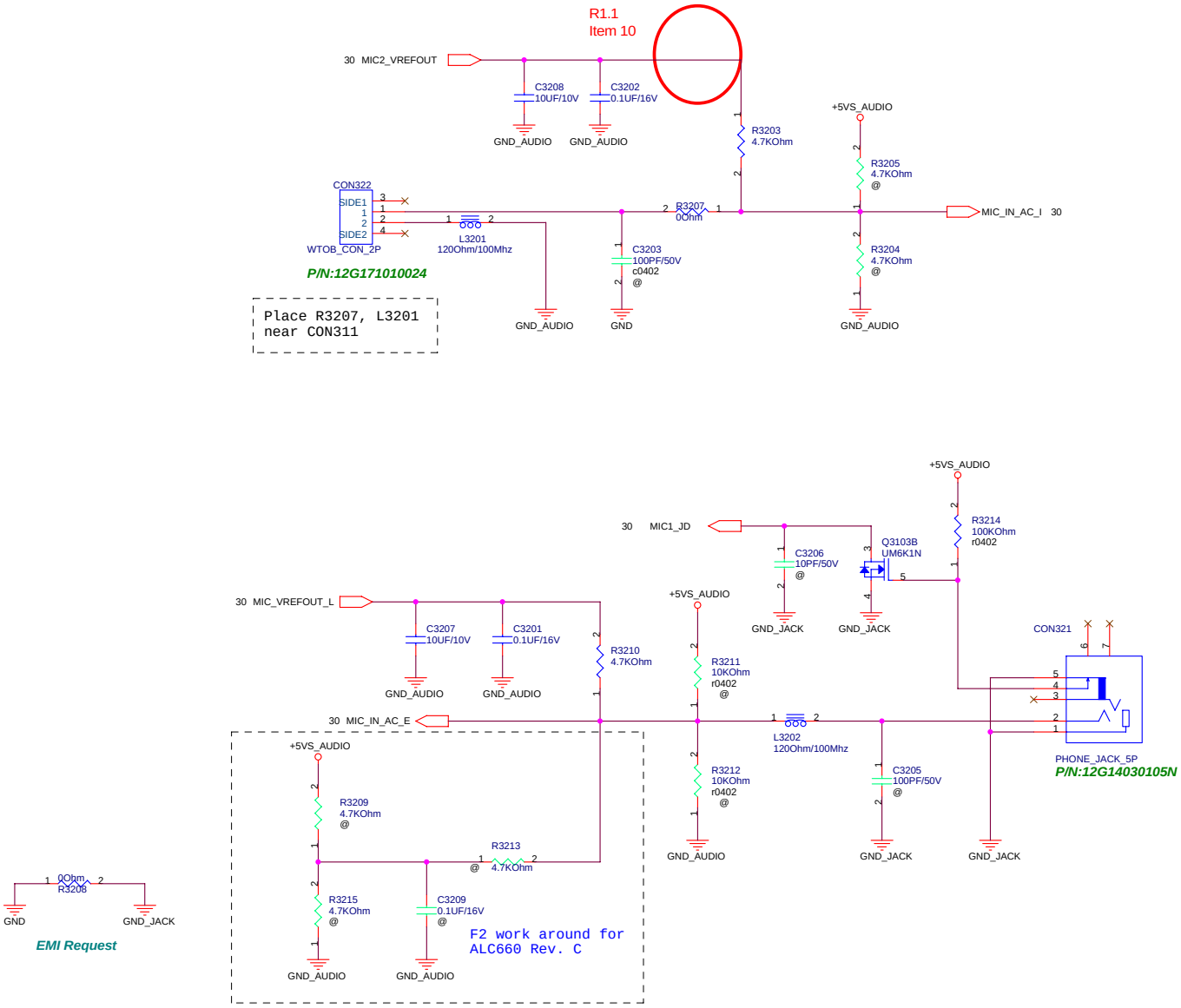
ASUSTeK COMPUTER INC

Title : G1420

Engineer: Marco Chen

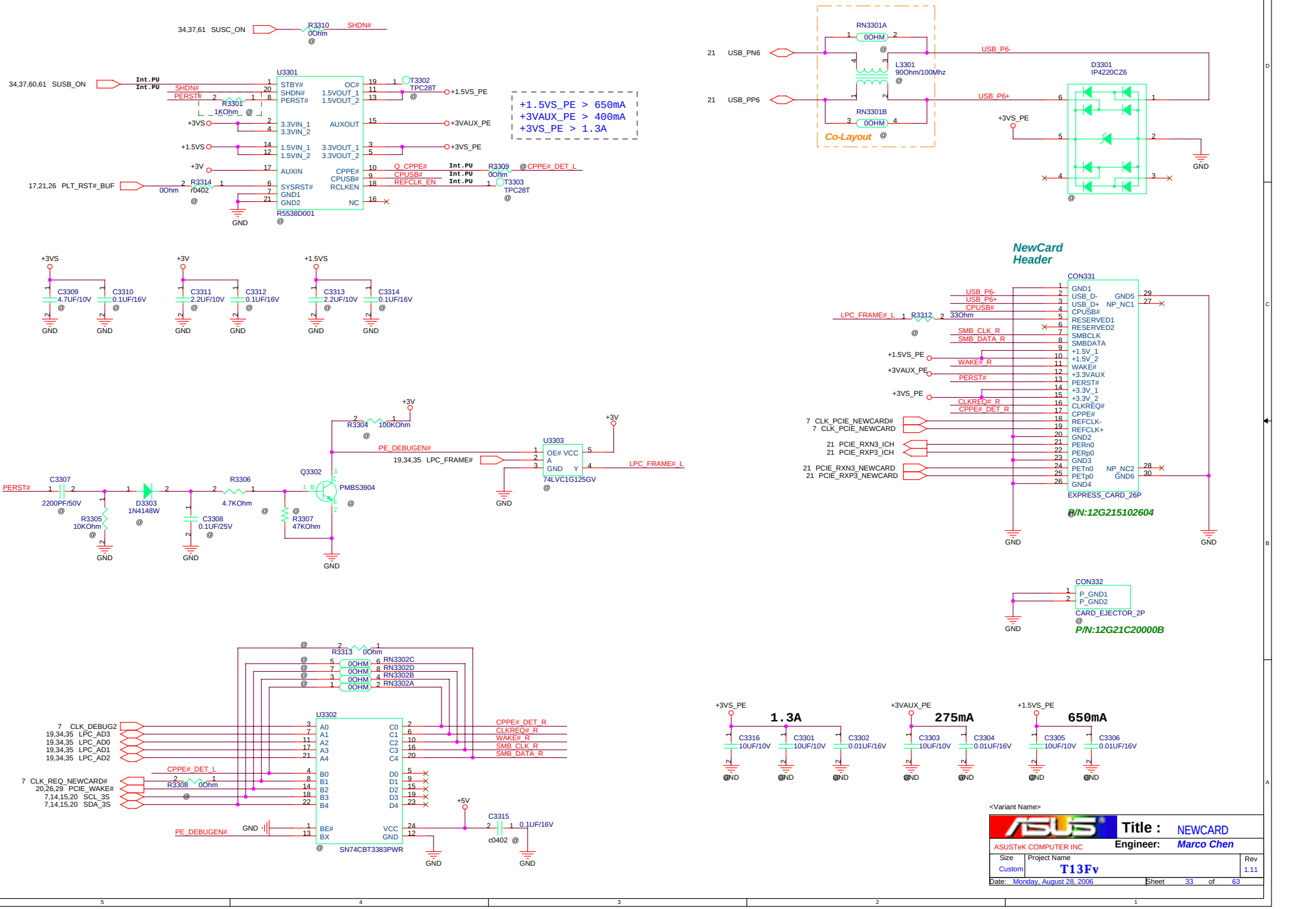
Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 31 of 63



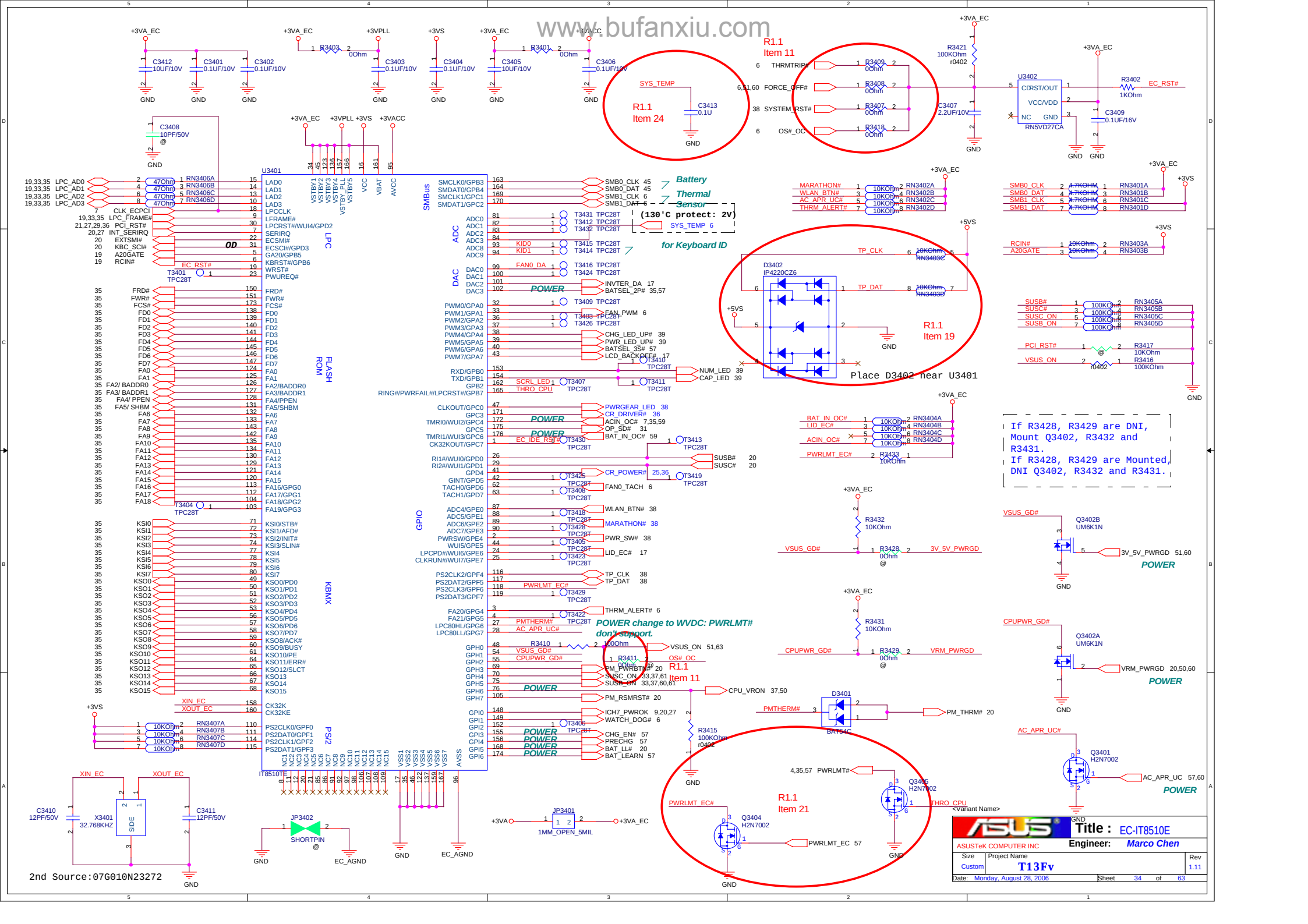
<variant_name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 32 of 63	



<Variant Name>

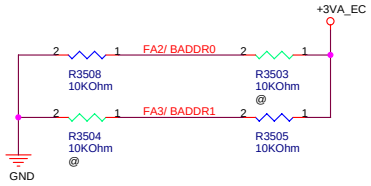
ASUSTeK COMPUTER INC	Title : NEWCARD	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 33 of 63	



EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

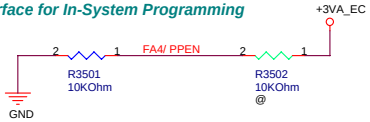
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

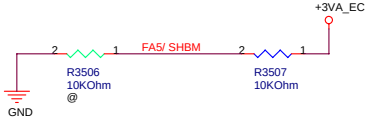
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

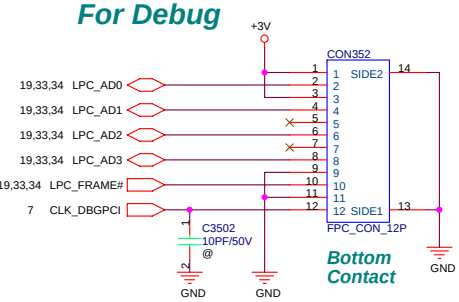


FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

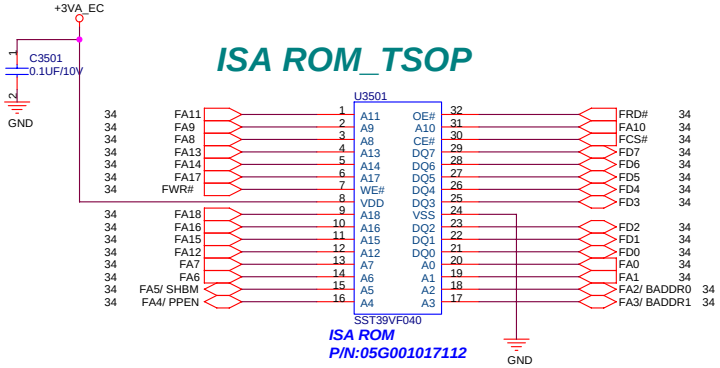


For Debug



P/N:12G183301208

ISA ROM_TSOP



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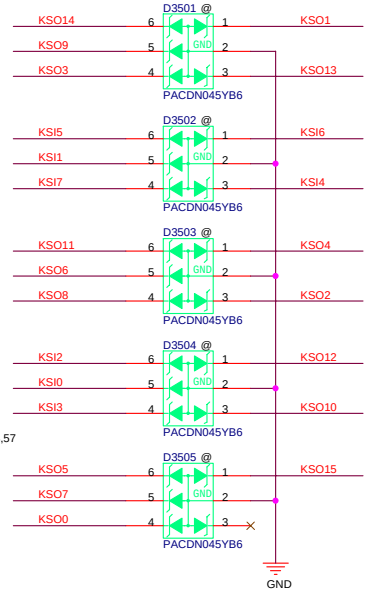
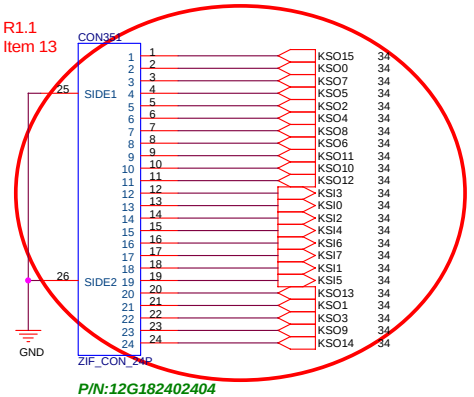


For Keyboard

R1.1
Item 13



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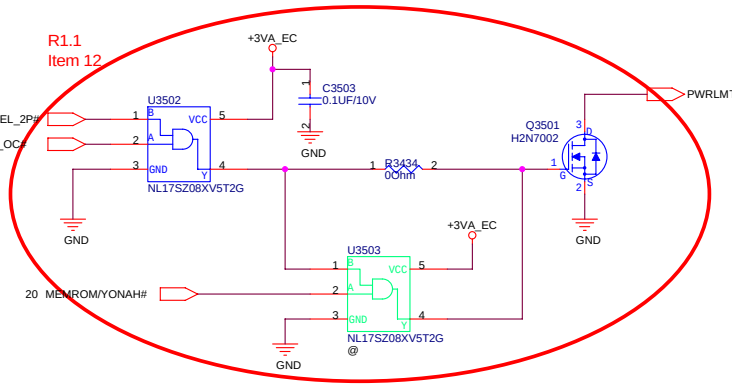
R1.1
Item 12



<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 35 of 63	

R1.1 Item 14

Original value:36K & 240K,
V=3.3*36k/(240k+36k)=2.87

Imax: 85mA

R1.1 Item 15

TRY POSSIBILITY FOR CHANGING FROM SI2301 TO PMBS3906

R1.1 Item 18

DNI RN3601, RN3602, RN3603, RN3604, RN3605, RN3606 BY USING GL817E.

Place RN3601, RN3602, RN3603, RN3604, RN3605, RN3606 near U3601

SD_CARD_19P
P/N:12G340001912

SD_PWRCTRL# / MS_PWRCTRL# have internal pull-up resistor => Min:39K Norm:65K Max:116K ohm and Each pin has 4KV ESD protect function.

MS PRO <= 100mA
MMC < 60mA
SD <= 35mA

<Variant Name>

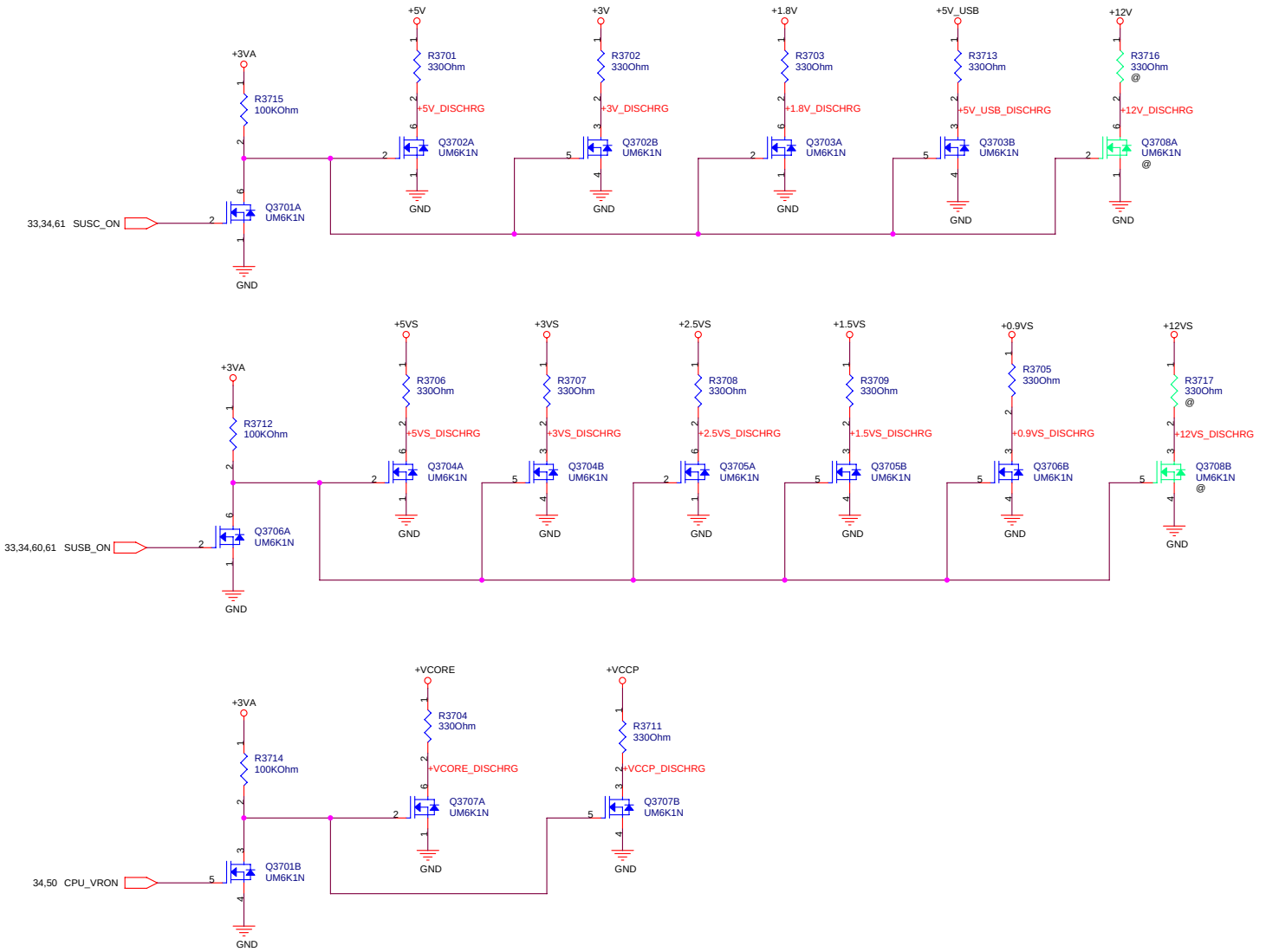
ASUSTeK COMPUTER INC

Title : 3IN1 CARD-READER

Engineer: Marco Chen

Size	Project Name	Rev
C	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 36 of 63



<Variant Name>

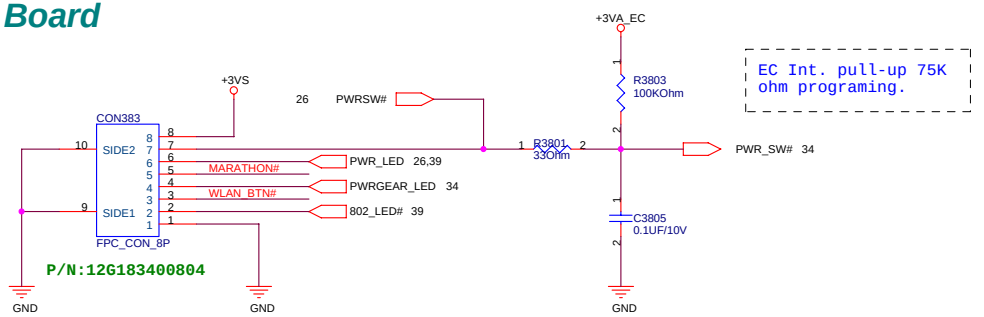
Title : DISCHARGE

ASUSTeK COMPUTER INC **Engineer:** *Marco Chen*

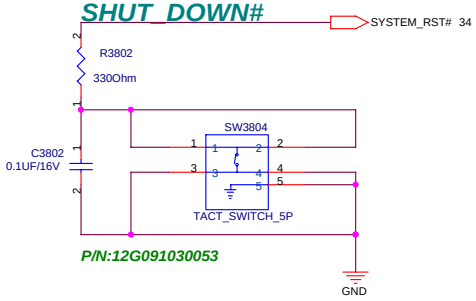
Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 37 of 63

FFC CONNECTER for T13Fv SW Board

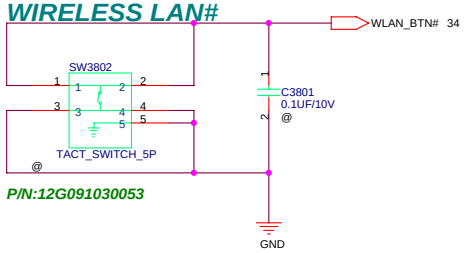


SHUT_DOWN#

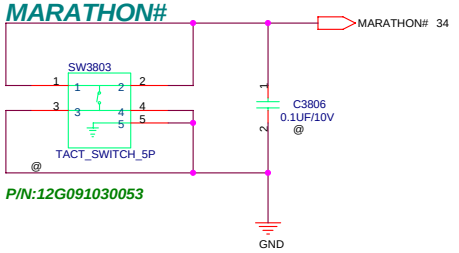


INSTANT KEY for T13Fg

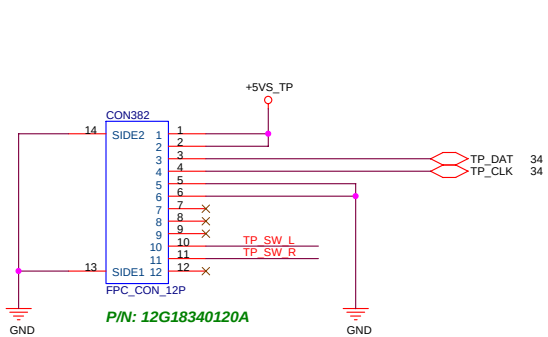
WIRELESS LAN#

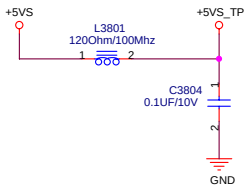


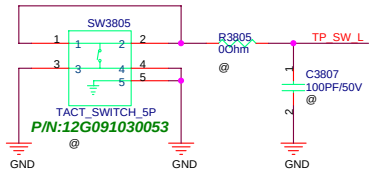
MARATHON#

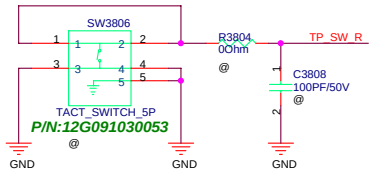


Select Button for T13Fg







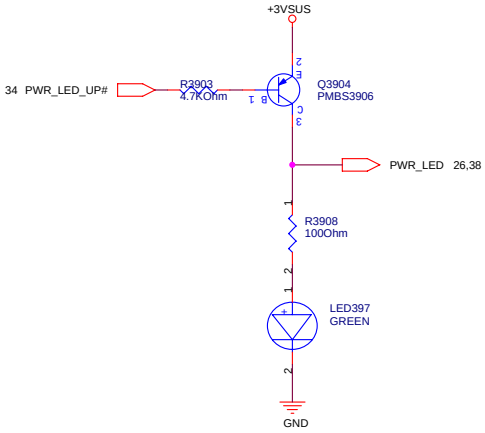


<Variant Name>

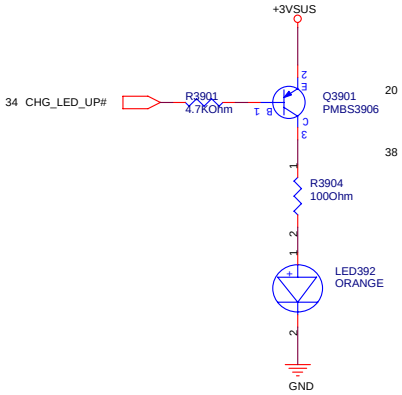
ASUSTeK COMPUTER INC	Title : Key & FFC CONN	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 38 of 63	

PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.

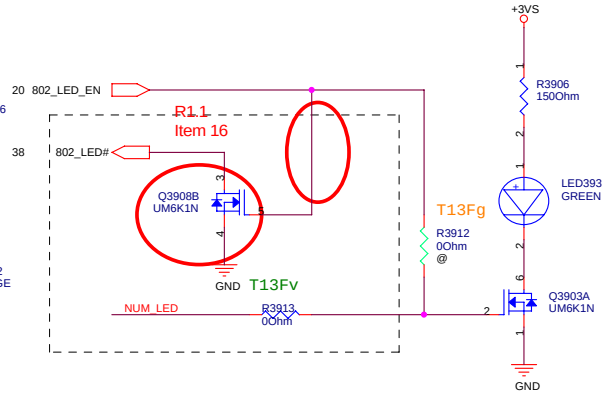
For POWER LED



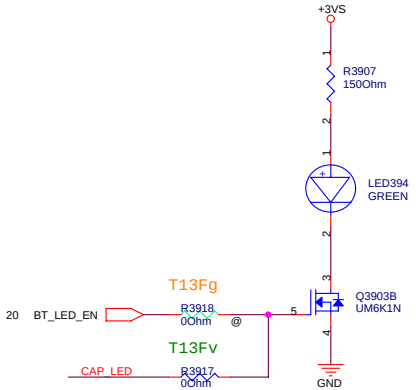
For BATTERY LED



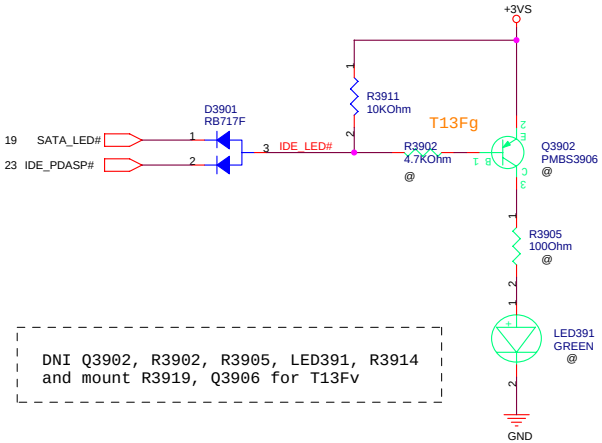
For WireLess LED



For BT LED

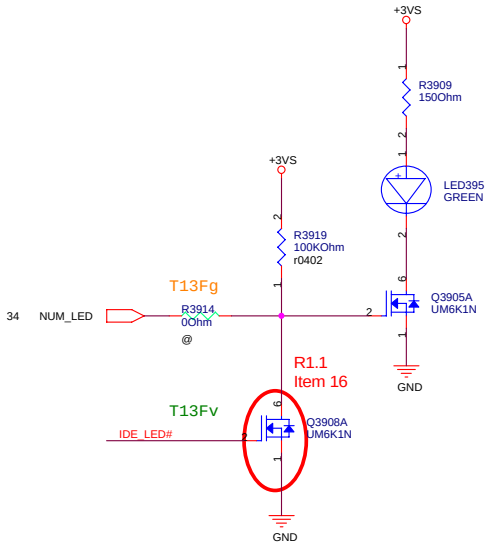


For SATA/IDE LED

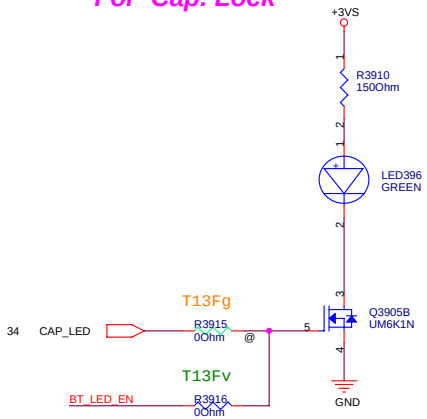


DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3906 for T13Fv

For Num Lock



For Cap. Lock



<Variant Name>

Title : LEDs

ASUSTeK COMPUTER INC Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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<Variant Name>

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 40 of 63	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 41 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 42 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 43 of 63

<Variant Name>

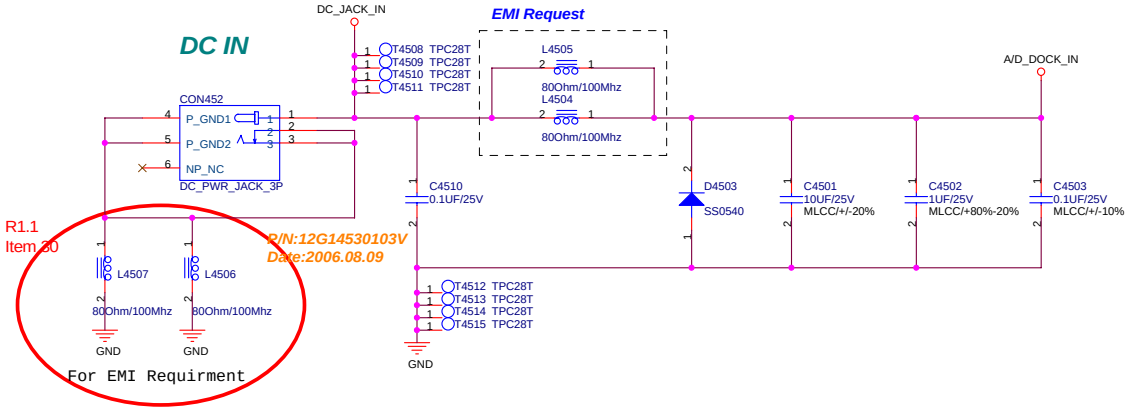
Title : EMPTY

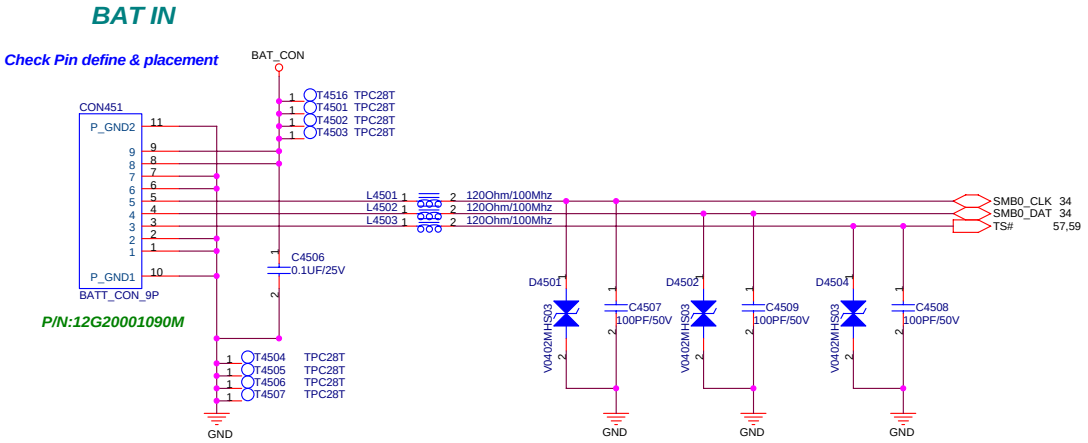
ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 44 of 63





<Variant Name>

Title : BAT&Adapter conn

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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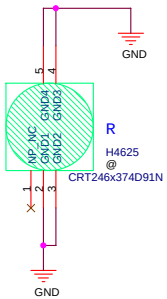

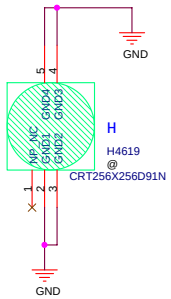

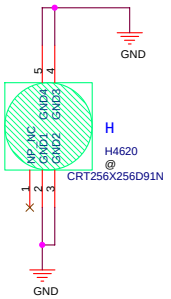

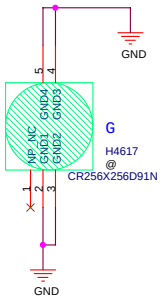

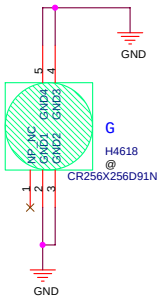

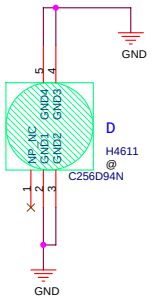

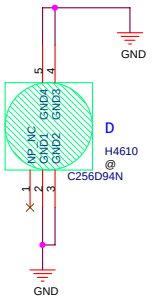

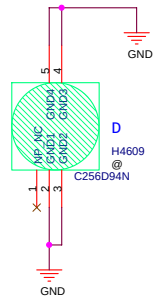

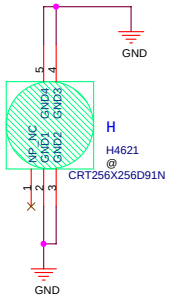

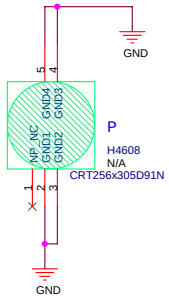

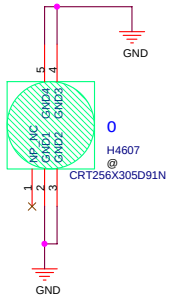

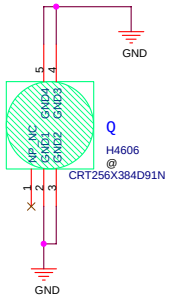

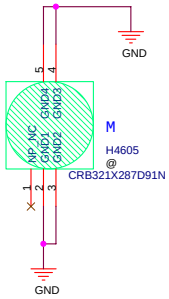

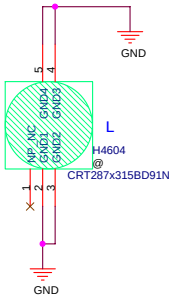

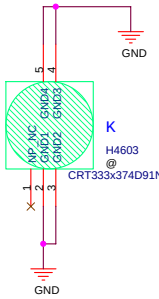

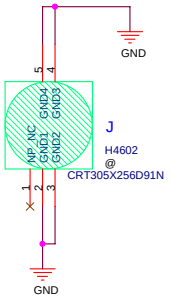

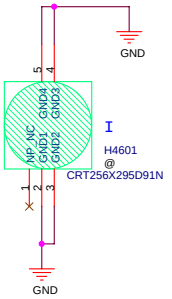

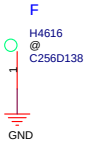

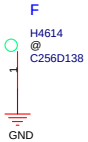

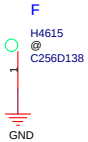

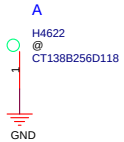

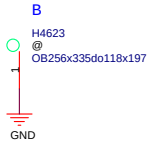

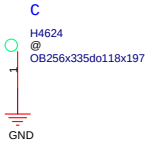

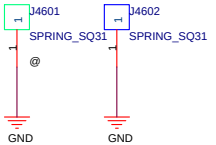

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Title : SCREW HOLE

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 46 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
C	T13Fv	1.11

Date: Monday, August 28, 2006 Sheet 47 of 63

R1.0 -> R1.1

1.Page 6: DNI R611 because Int. pull-up resister exists in FAN module.

2.Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

3.Page 17: Change reference name from F3602 to F1701.

4.Page 21: DNI U2103.

5.Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.

6.Page 23: Change R2301 size from 0603 to 0402.

7.Page 23: Add pull high resister R2306*DNI and pull down resister R2307*Mount for ODD cable select.

8.Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.

9.Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.Page 32: Delete R3201 and connect MIC2_VREFOUTto R3203.1 directly.

11.Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.

12.Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

13.Page 35: Change keyboard matrix.

14.Page 36: Change reference name from JP3403 to JP3601

15.Page 36: Change R3622 size from 0402 to 0603.

16.Page 39: Delete R3920 and change Q3906 and Q3907*2N7006 to Q3908*UM6K1N.

17.Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.

18.Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.

19.Page 34: Add ESD Protection*D3402 for Touch Pad.

20.Page 27: Add series resister 33 ohm for PCI_FRAME# and PCI_AD13

21.Page 34:Change Q3403**UM6K1N to Q3404, Q3405*2N7002.

22.Page 18: Change L1801, L1802, and L1803 from bead to inductor.

23.Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

24.Page 6: Change R615 pull up from +3VS to +5VS_AUDIO.

25.Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.

26.Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.

27.Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.

28.Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.

29.Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.

30.Page 45:Add L4506 and L4507 for EMI requirement.

<Variant Name>

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 48 of 63	

<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13Fv	1.11

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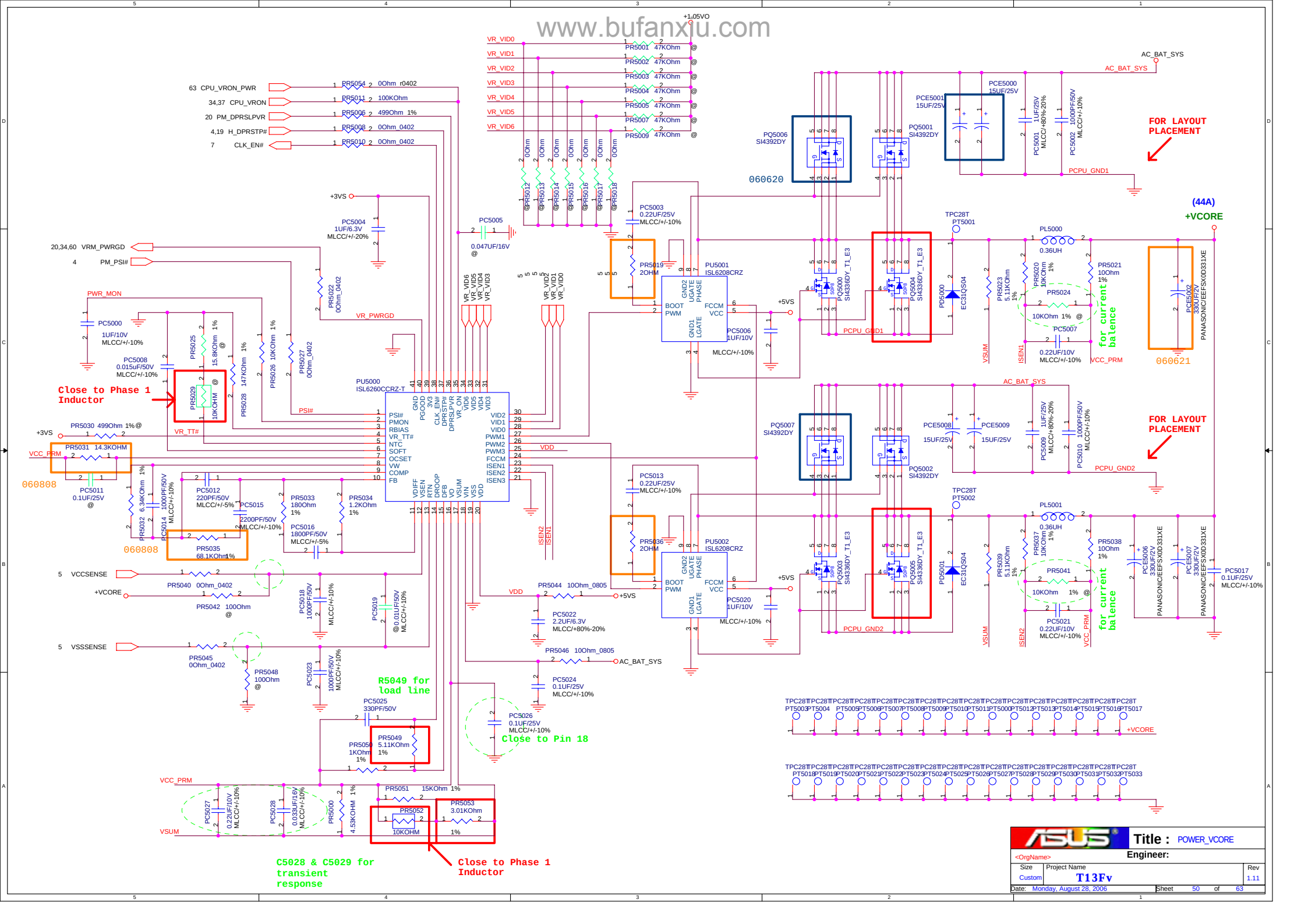
www.bufanxiu.com
+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5005 47KOhm
PR5007 47KOhm
PR5009 47KOhm
63 CPU_VRON_PWR
34,37 CPU_VRON
20 PM_DPRSLPVR
4,19 H_DPRSTP#
7 CLK_EN#
PR5054 0Ohm r0402
PR5011 100KOhm
PR5006 499Ohm 1%
PR5008 0Ohm_0402
PR5010 0Ohm_0402
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5005 0.047UF/16V @
20,34,60 VRM_PWRGD
4 PM_PSI#
PR5022 0Ohm_0402
PWR_MON
PC5000 1UF/10V MLCC/+/-10%
PC5008 0.015uF/50V MLCC/+/-10%
PR5025 15.8KOhm 1% @
PR5026 10KOhm 1%
PR5027 0Ohm_0402
PR5028 147KOhm 1%
PR5029 10KOHM 1% @
Close to Phase 1 Inductor
VR_PWRGD
PSI#
VR_TT#
PU5000 ISL6260CCRZ-T
PSI# PMON RBIAS VR_TT# NTC SOFT OCSET VW COMP FB
GND PGOOD 3V3 CLK_EN# DPRSTP# DPRSLPVR VR_ON VID6 VID5 VID4 VID3 VID2 VID1 VID0 PWM1 PWM2 PWM3 FCCM ISEN1 ISEN2 ISEN3
VDIFF VSEN RTN DROOP DFB VO VSUM VIN VSS VDD
PR5030 499Ohm 1%@
PR5031 14.3KOHM
VCC_PRM
060808
PC5011 0.1UF/25V @
PR5032 6.34KOhm 1%
PC5014 1000PF/50V MLCC/+/-10%
PC5012 220PF/50V MLCC/+/-5%
PC5015 2200PF/50V MLCC/+/-10%
PR5033 180Ohm 1%
PC5016 1800PF/50V MLCC/+/-5%
PR5034 1.2KOhm 1%
PR5035 68.1KOhm1%
5 VCCSENSE
+VCORE
PR5040 0Ohm_0402
PR5042 100Ohm @
PC5018 1000PF/50V MLCC/+/-10%
PC5019 @ 0.01UF/50V MLCC/+/-10%
5 VSSSENSE
PR5045 0Ohm_0402
PR5048 100Ohm @
PC5023 1000PF/50V MLCC/+/-10%
R5049 for load line
PC5025 330PF/50V
PR5049 5.11KOhm 1%
PR5050 1KOhm 1%
VCC_PRM
PC5027 0.22UF/10V MLCC/+/-10%
PC5028 0.033UF/16V MLCC/+/-10%
PR5000 4.53KOHM 1%
VSUM
PR5051 15KOhm 1%
PR5052 10KOHM
PR5053 3.01KOhm 1%
C5028 & C5029 for transient response
Close to Phase 1 Inductor
PC5026 0.1UF/25V MLCC/+/-10%
Close to Pin 18
PR5044 10Ohm_0805
PC5022 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
AC_BAT_SYS
PC5024 0.1UF/25V MLCC/+/-10%
VDD
ISEN2
ISEN1
PC5003 0.22UF/25V MLCC/+/-10%
PR5019 2OHM
PU5001 ISL6208CRZ
BOOT PWM GND2 UGATE PHASE FCCM VCC GND1 LGATE
PC5006 1UF/10V MLCC/+/-10%
+5VS
PC5013 0.22UF/25V MLCC/+/-10%
PR5036 2OHM
PU5002 ISL6208CRZ
PC5020 1UF/10V MLCC/+/-10%
PQ5006 SI4392DY
PQ5001 SI4392DY
060620
PCPU_GND1
PCE5001 15UF/25V
PCE5000 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/50V MLCC/+/-10%
FOR LAYOUT PLACEMENT
(44A) +VCORE
TPC28T PT5001
PL5000 0.36UH
PD5000 EC31QS04
PR5023 5.11KOhm 1%
PR5020 10KOhm 1%
PR5024 10KOhm 1% @
PC5007 0.22UF/10V MLCC/+/-10%
PR5021 10Ohm 1%
for current balence
PCE5002 330UF/2V PANASONIC/EEFSX0D331XE
060621
PQ5007 SI4392DY
PQ5002 SI4392DY
PCE5008 15UF/25V
PCE5009 15UF/25V
PC5009 1UF/25V MLCC/+80%-20%
PC5010 1000PF/50V MLCC/+/-10%
PCPU_GND2
TPC28T PT5002
PL5001 0.36UH
PD5001 EC31QS04
PR5039 5.11KOhm 1%
PR5037 10KOhm 1%
PR5041 10KOhm 1% @
PC5021 0.22UF/10V MLCC/+/-10%
PR5038 10Ohm 1%
PCE5006 330UF/2V PANASONIC/EEFSX0D331XE
PC5007 330UF/2V PANASONIC/EEFSX0D331XE
PC5017 0.1UF/25V MLCC/+/-10%
TPC28T PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5000 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
+VCORE
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
Engineer:
<OrgName>
Size Custom
Project Name T13Fv
Rev 1.11
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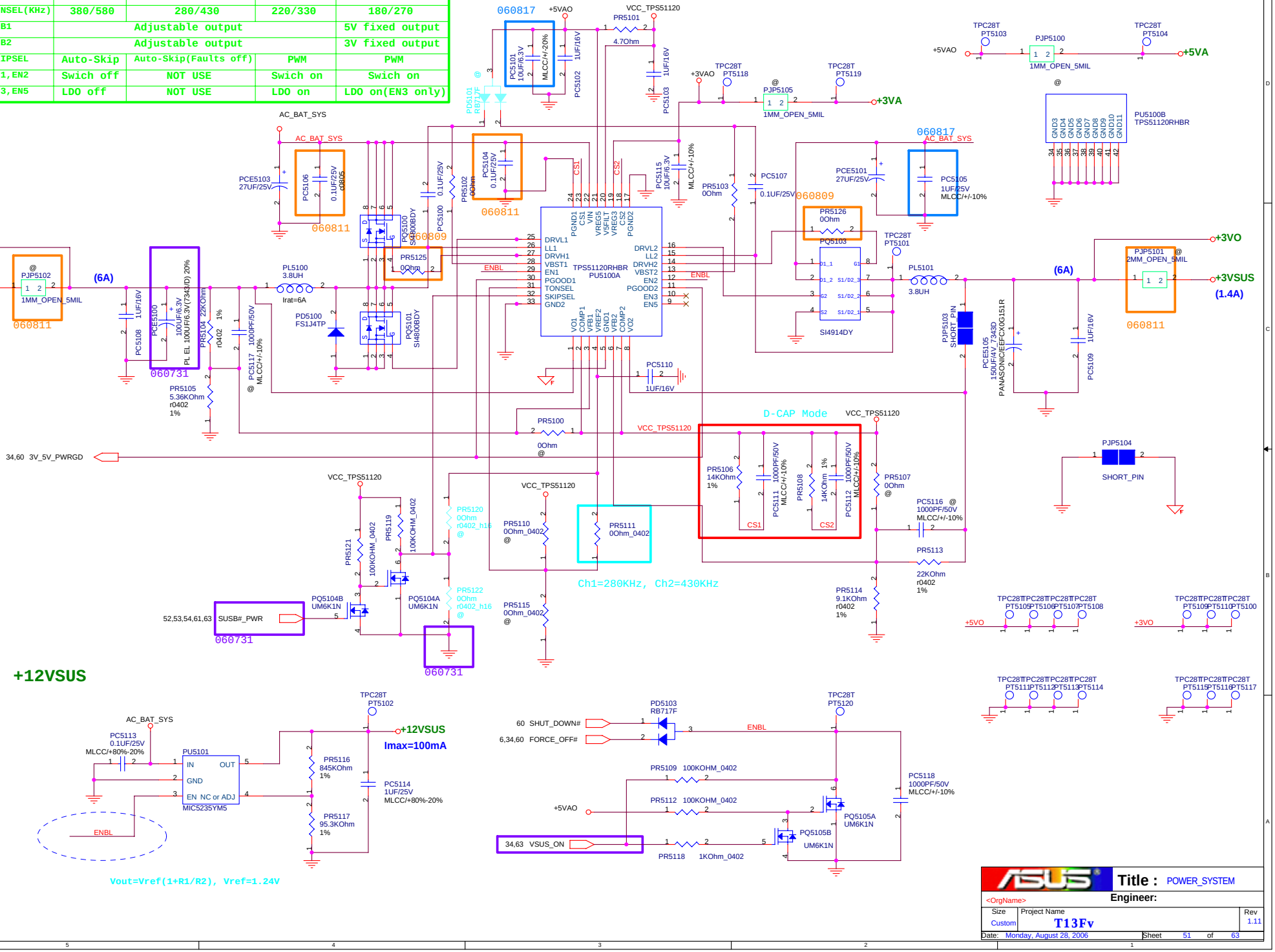
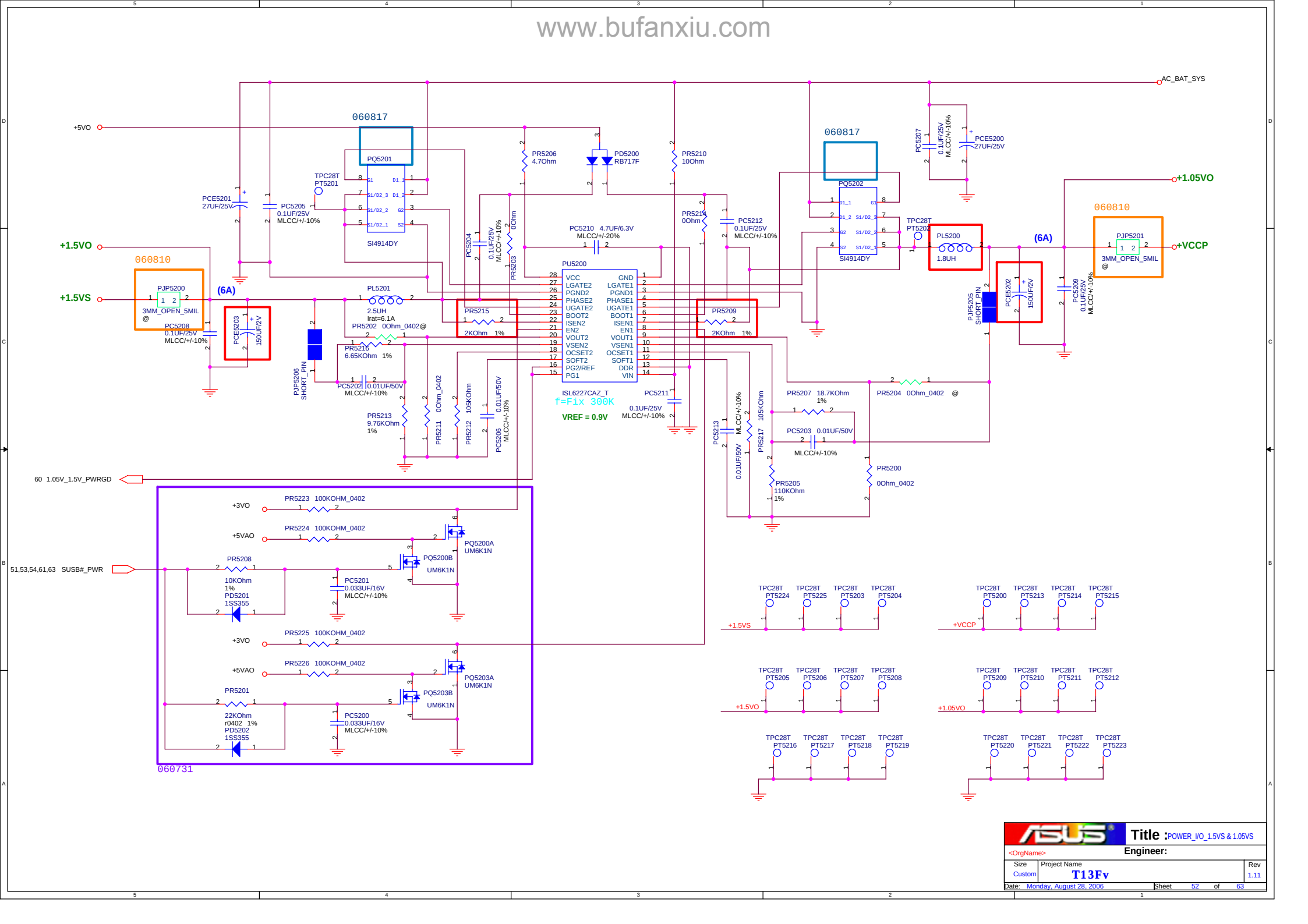
PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)

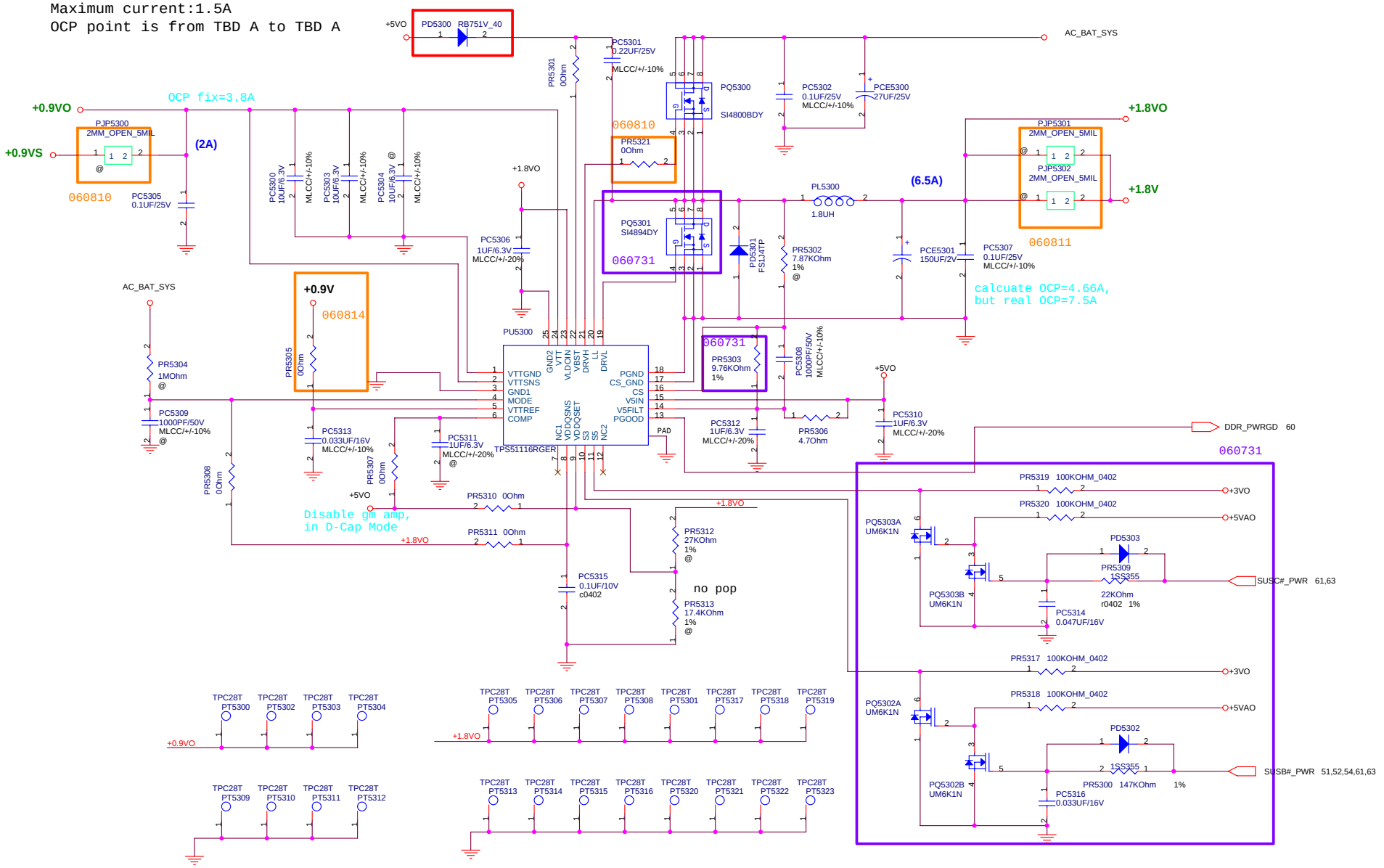




Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 52 of 63	

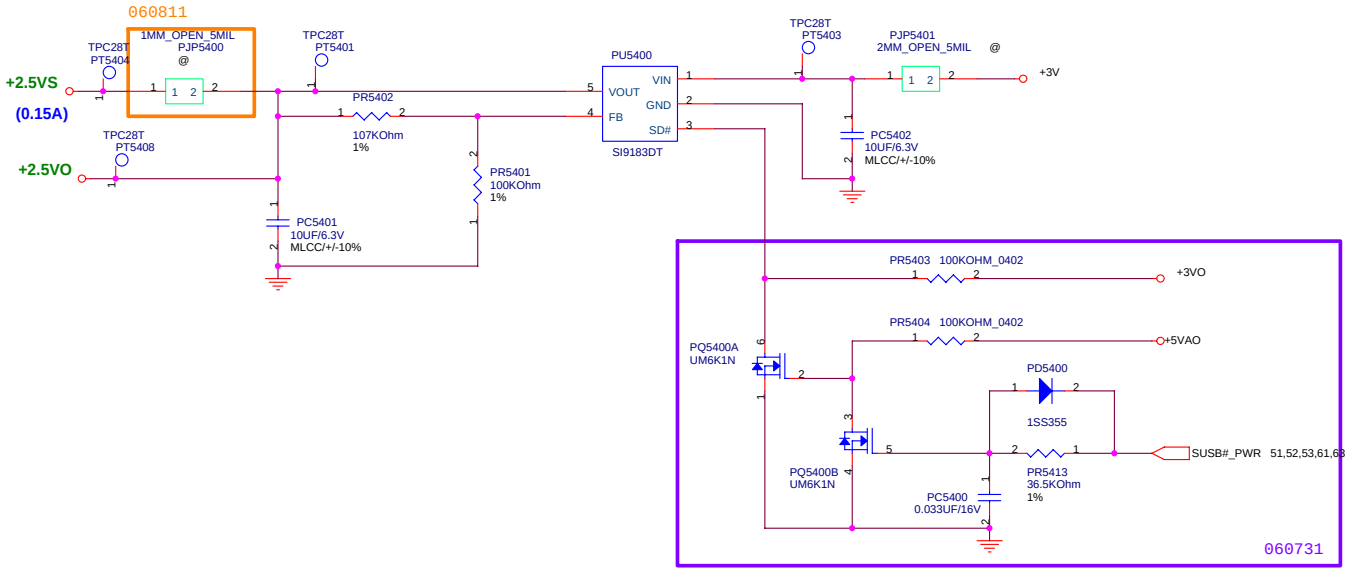
.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A



Title :	POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 53 of 14	

+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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Title : EMPTY			
<OrgName>	Engineer:		
Size: Custom	Project Name: T13Fv		Rev: 1.11
Date: Monday, August 28, 2006		Sheet 55 of 63	

Title : EMPTY				
<OrgName>	Engineer:			
Size: Custom	Project Name: T13Fv			Rev: 1.11
Date: Monday, August 28, 2006		Sheet 56 of 63		

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=1.805V
=> Iin(max)=3.205A
=> Constant Power = 19 * 3.205= 60.89W
=> R5708=40.2K,R5714=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] } = 12.603
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA

Power limit Circuit
Viinp=Iinput*RS*Glinp*R5717
Viinp=0.998, RS=10mohm, Glinp=3uA/mV,
R5717=10K----->Iinput=3.32A
Pinput=63.08W

Title : POWER_CHARGER			
<OrgName>	Engineer:		
Size: Custom	Project Name: T13Fv		Rev: 1.11
Date: Monday, August 28, 2006	Sheet 57 of 63		

Title : POWER_PIC			
<OrgName>	Engineer:		
Size: Custom	Project Name: T13Fv		Rev: 1.11
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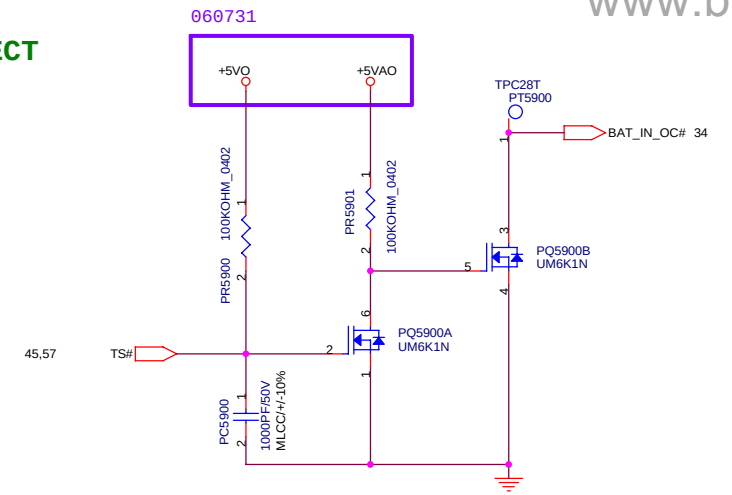
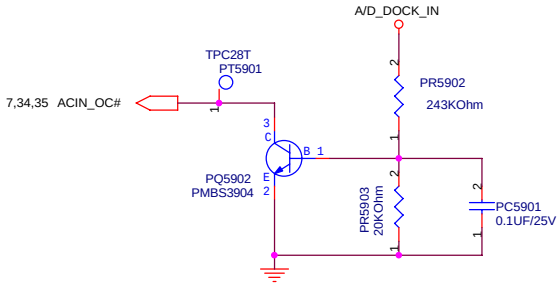
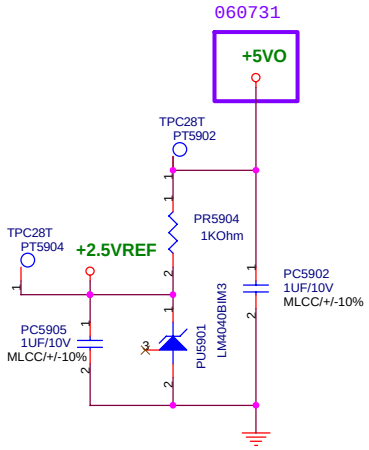
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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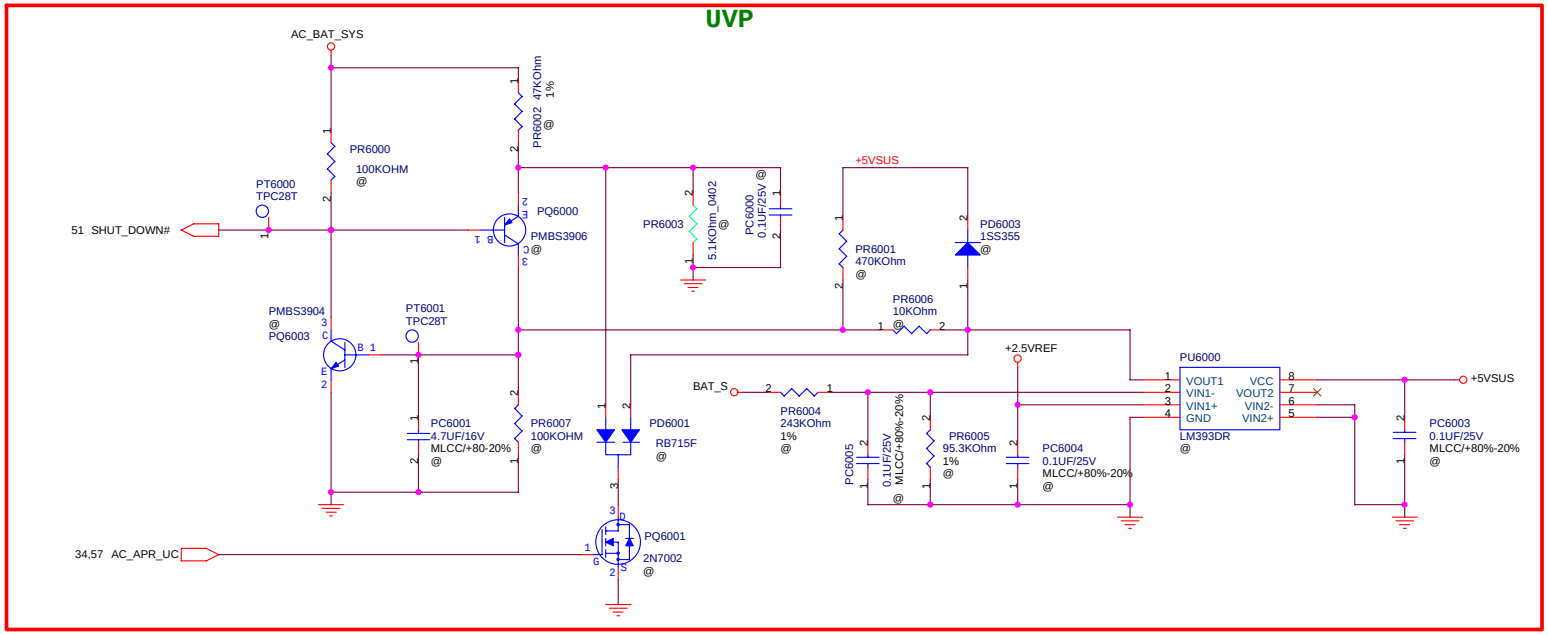
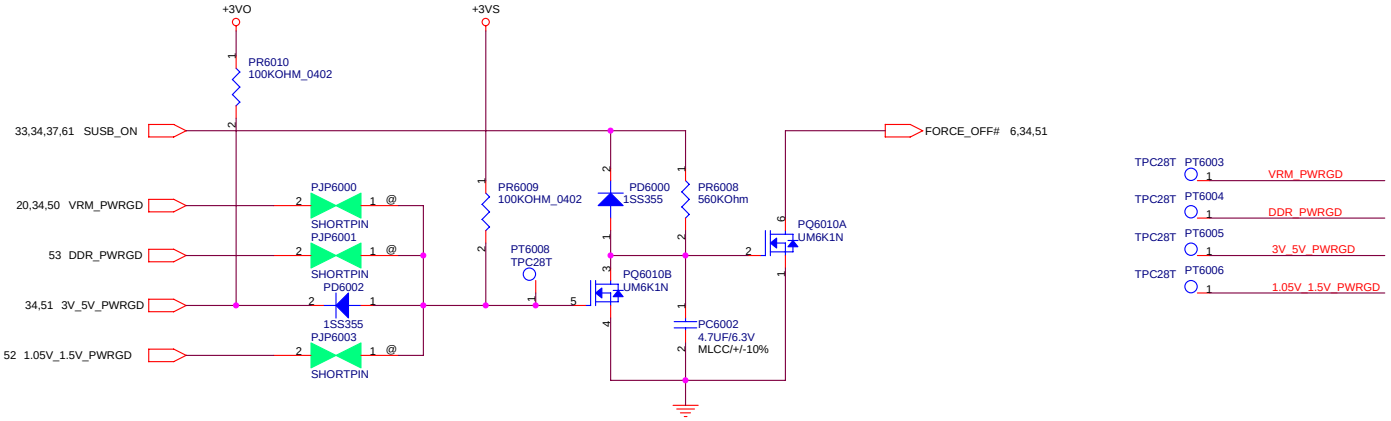
UVP

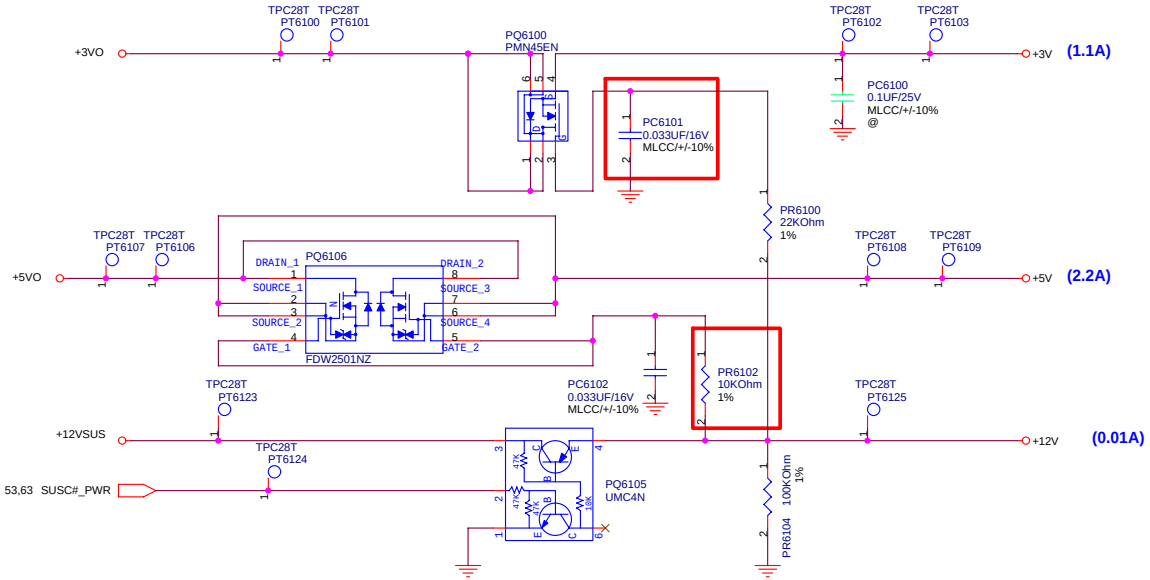


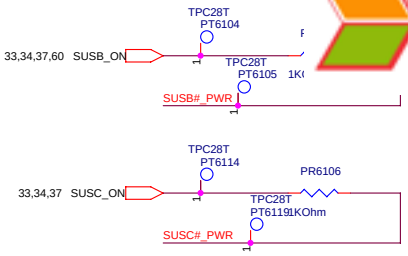
POWER GOOD DETECTER



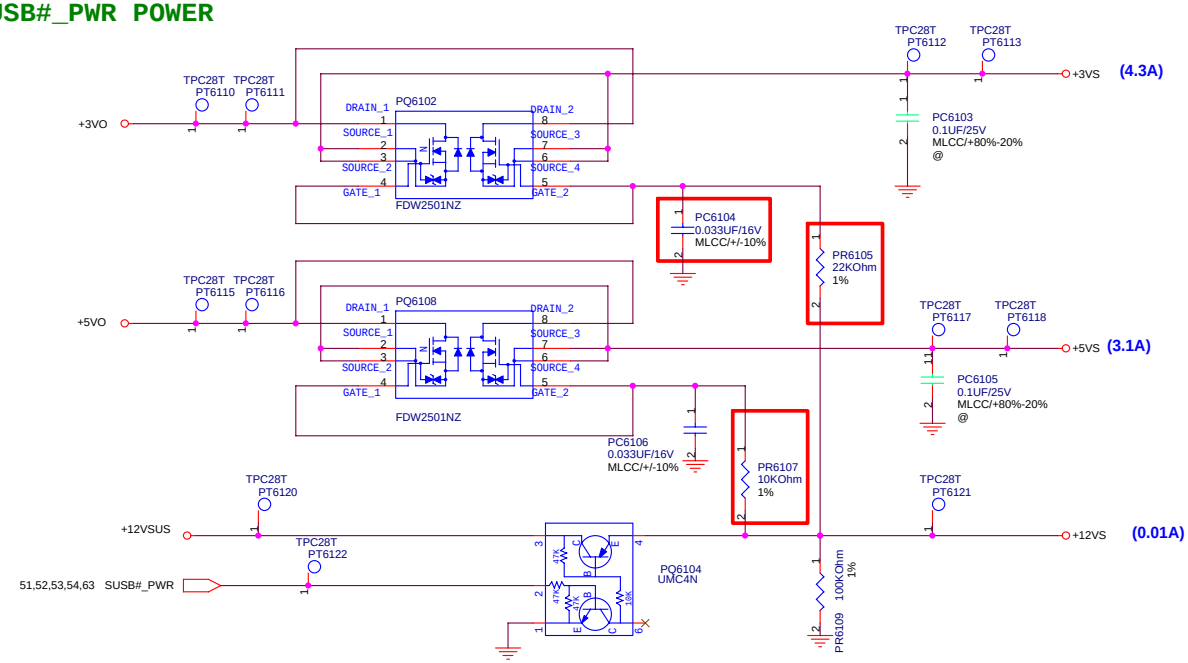
Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
Date: Monday, August 28, 2006	Sheet 60 of 63	

SUSC#_PWR POWER





SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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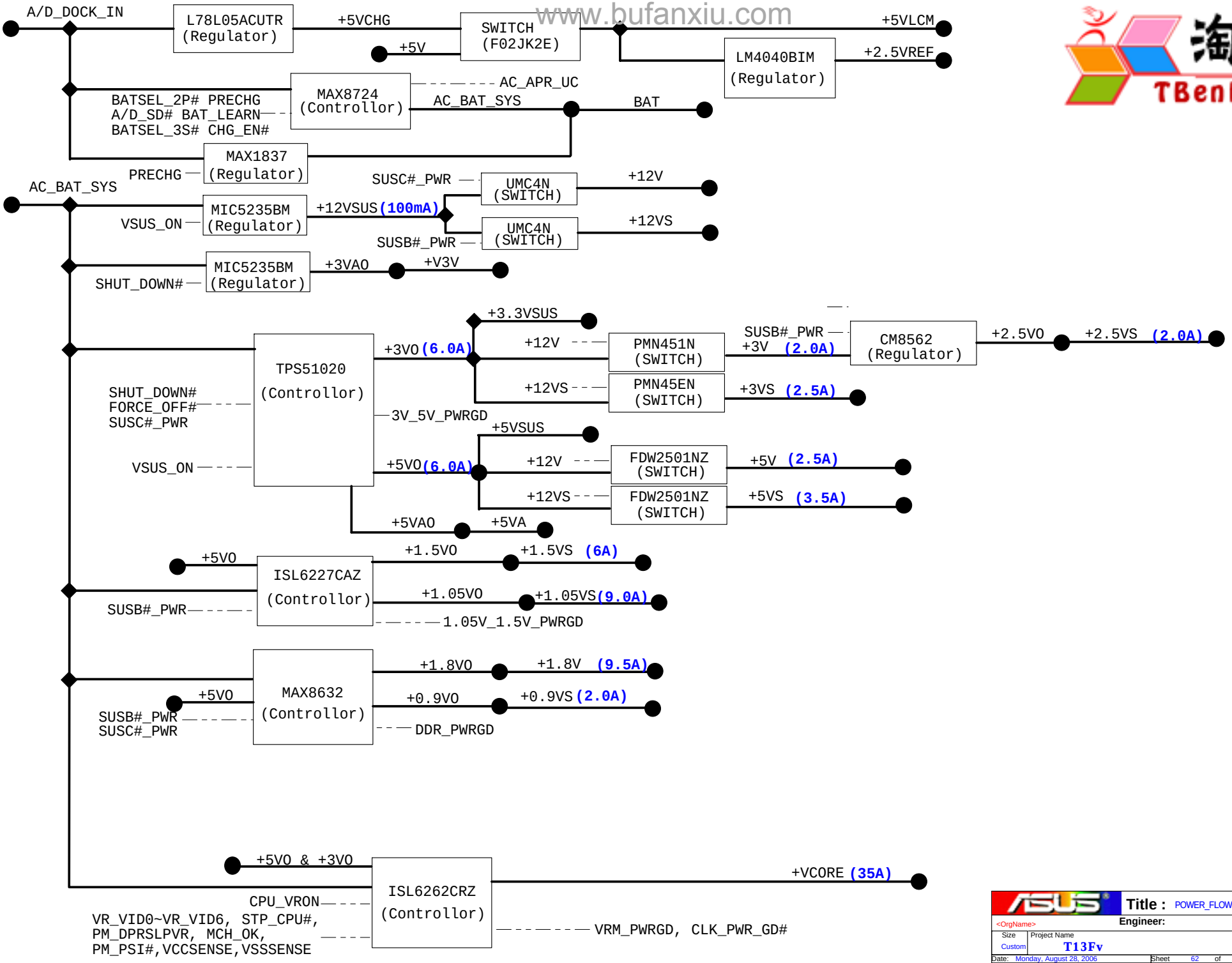

Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13Fv	Rev: 1.11
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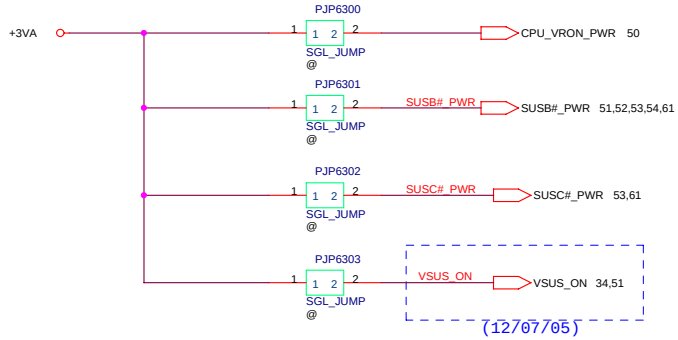
AC_BAT_SYS	AC_BAT_SYS	17,50,51,52,53,57,60
+3VA	+3VA	6,17,19,34,37,51
+5VA	+5VA	6,51
+5VO	+5VO	51,52,53,59,61
+3VO	+3VO	51,52,53,54,60,61
+3VSUS	+3VSUS	17,20,21,22,29,31,39,51
+5VSUS	+5VSUS	22,51,57,60
+3V	+3V	21,25,26,27,28,33,35,37,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,20,21,22,23,25,26,27,29,30,33,34,36,37,38,39,50,60,61
+12VSUS	+12VSUS	51,61
+12V	+12V	24,31,37,61
+12VS	+12VS	17,37,61
+5V	+5V	6,17,24,28,33,37,61
+5VS	+5VS	6,18,22,23,25,30,31,34,37,38,50,61
+2.5VO	+2.5VO	54
+2.5VS	+2.5VS	11,37,54
+1.8VO	+1.8VO	53
+1.8V	+1.8V	9,12,14,15,37,53
+VCCP	+VCCP	5,12,22,37,52
+0.9VS	+0.9VS	16,37,53
BAT	BAT	57
+2.5VREF	+2.5VREF	57,59,60
+VCORE	+VCORE	5,37,50
BAT_CON	BAT_CON	45,57

FOR POWER TEST



ASUS	Title : POWER_SIGNAL		
<OrgName>	Engineer:		
Size: Custom	Project Name: T13Fv		Rev: 1.11
Date: Monday, August 28, 2006	Sheet 63 of 63		