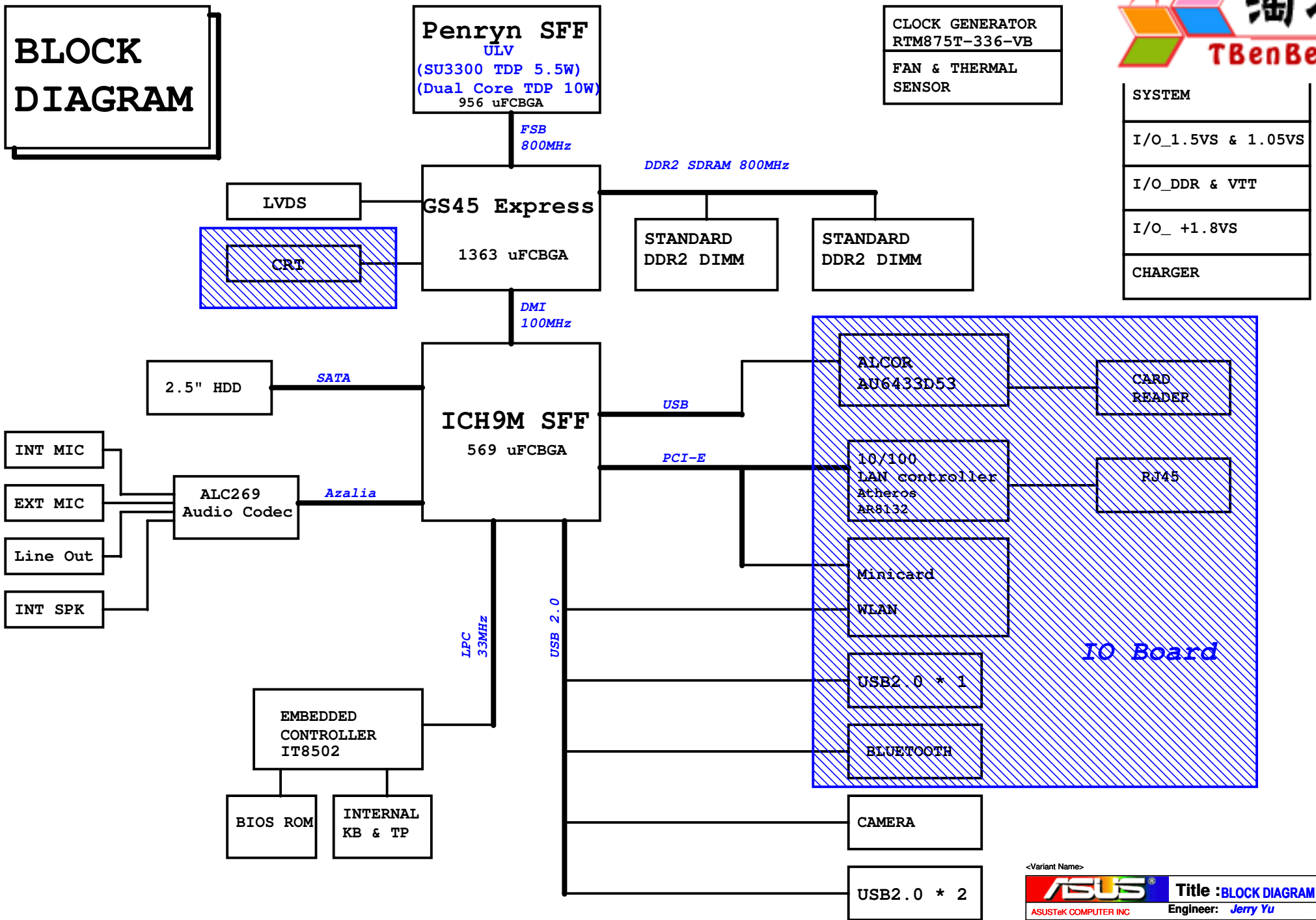


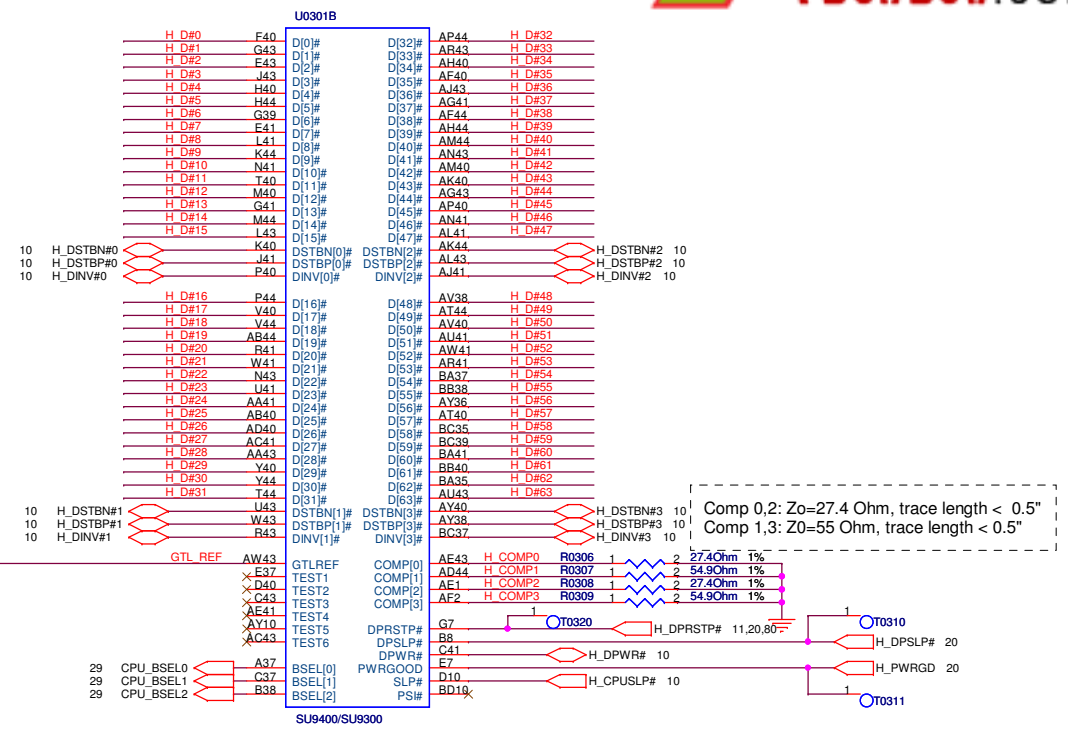
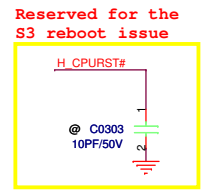
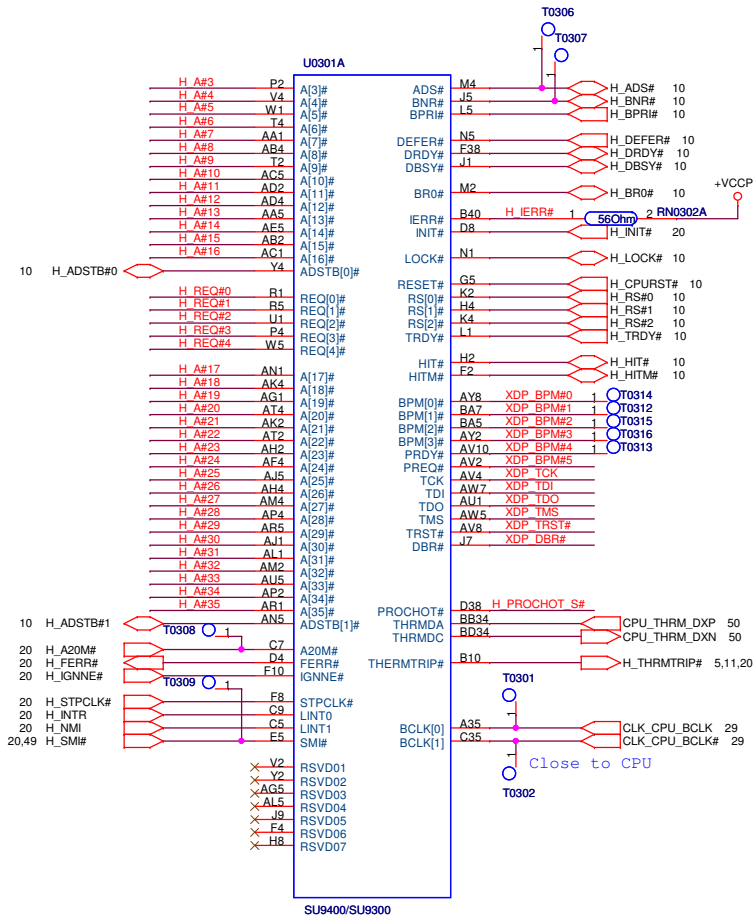
BLOCK DIAGRAM



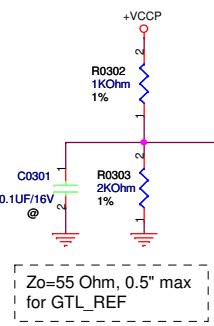
CLOCK GENERATOR
RTM875T-336-VB

FAN & THERMAL
SENSOR

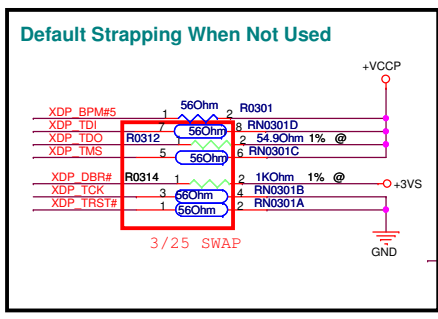
SYSTEM
I/O_1.5VS & 1.05VS
I/O_DDR & VTT
I/O_ +1.8VS
CHARGER



Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

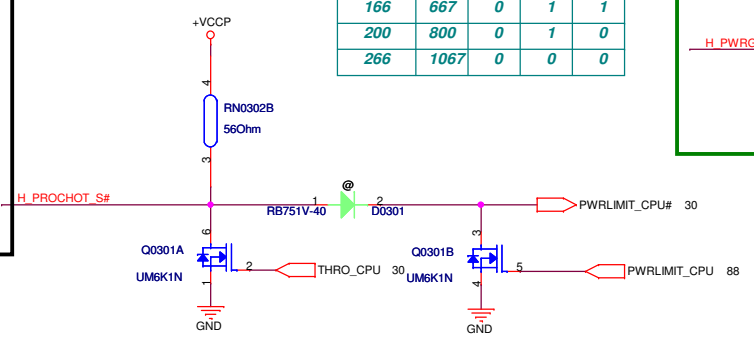
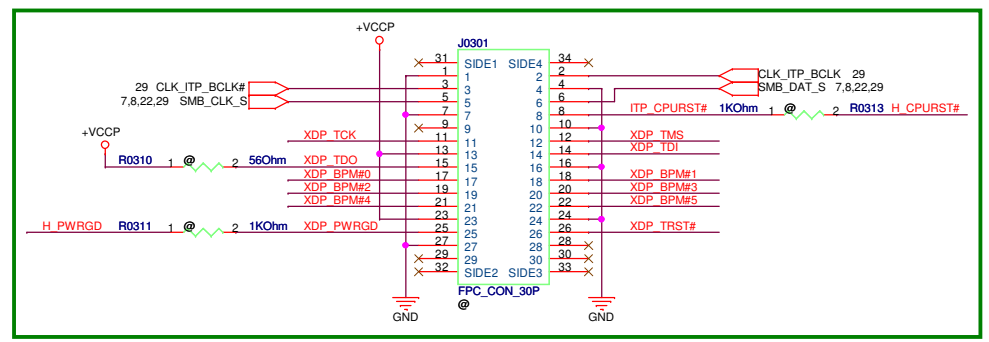


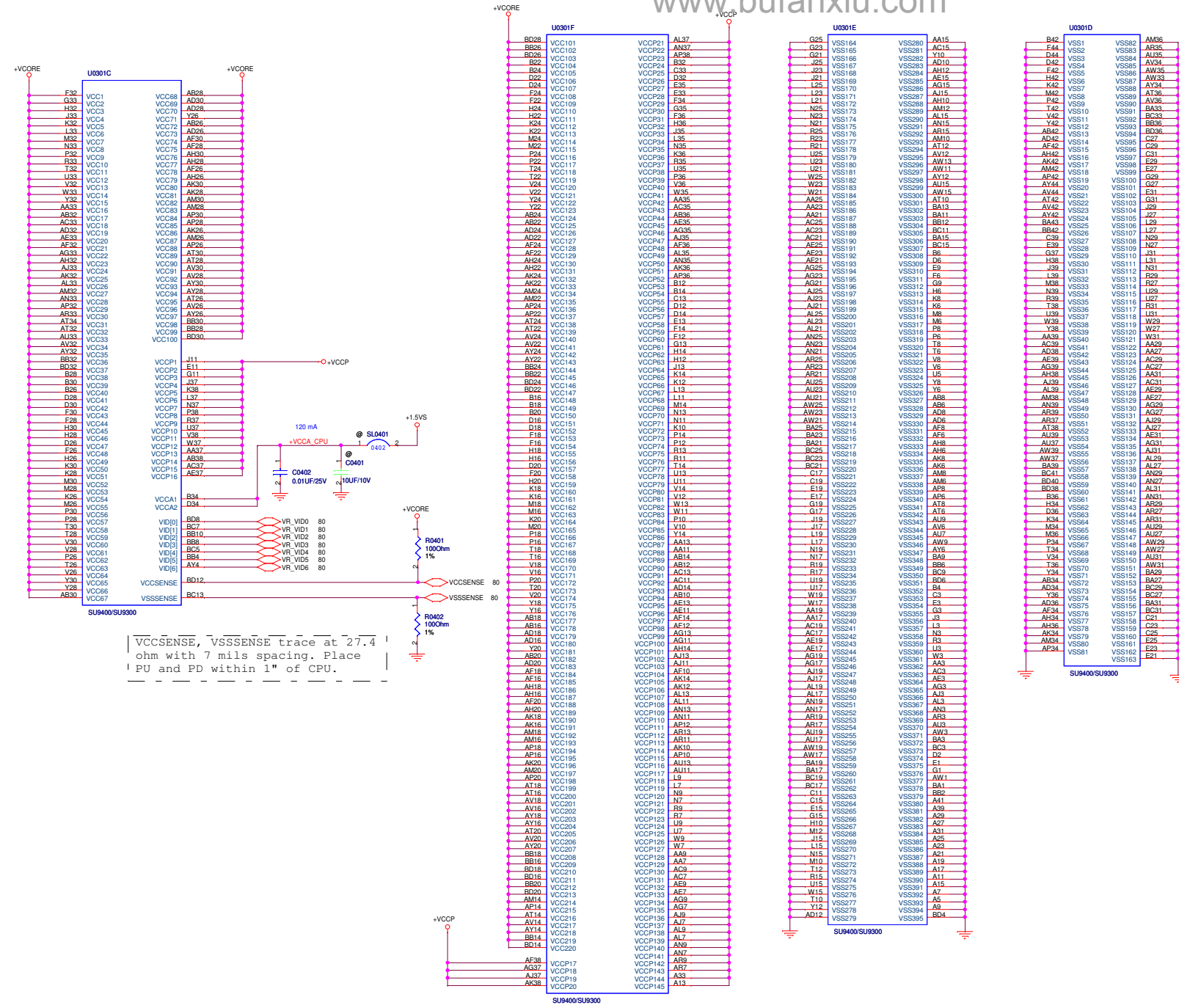
Zo=55 Ohm, 0.5" max for GTL_REF

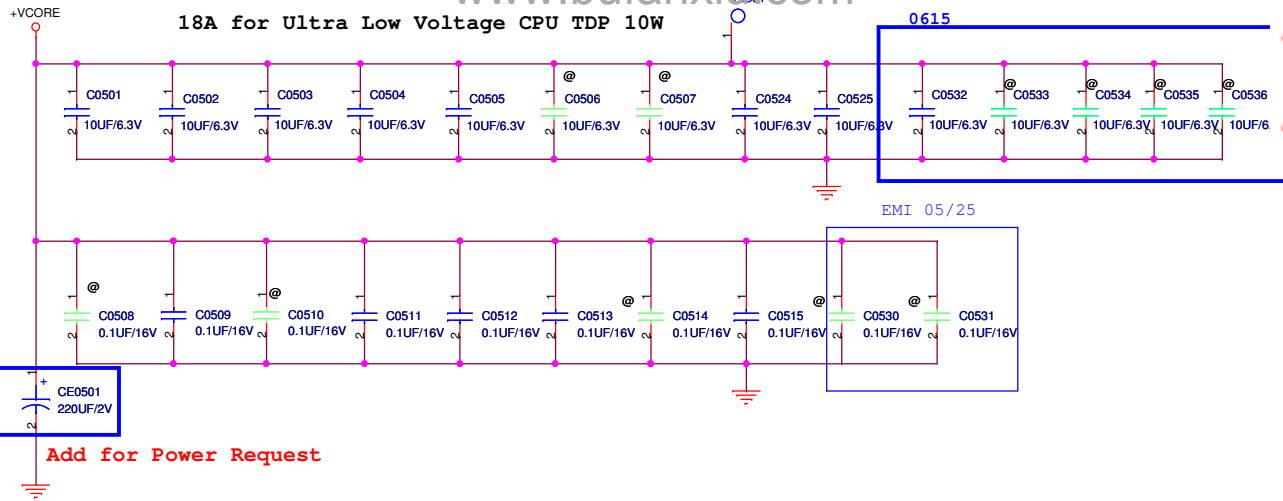


Place R0304 & R0306 for XDP function

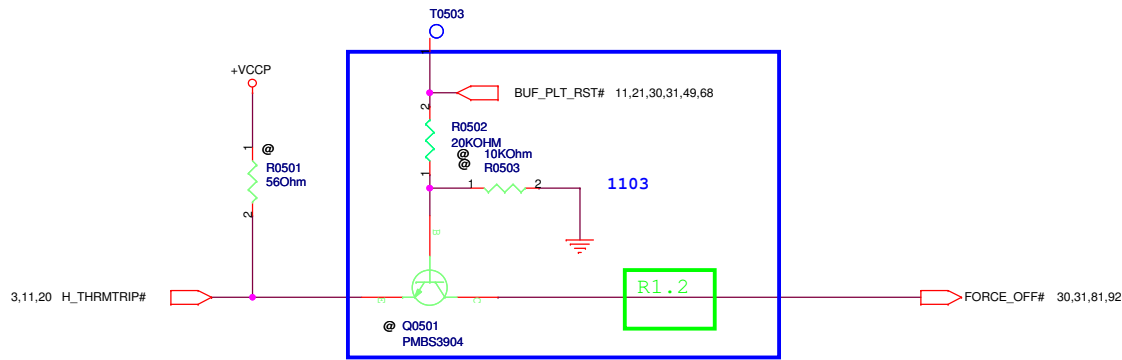
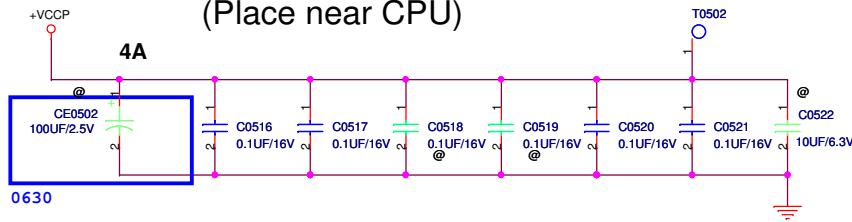
Table with columns BCLK, FSB, BSEL2, BSEL1, BSEL0 and rows of values (166, 200, 266).







+VCCP Decoupling Capacitor
(Place near CPU)



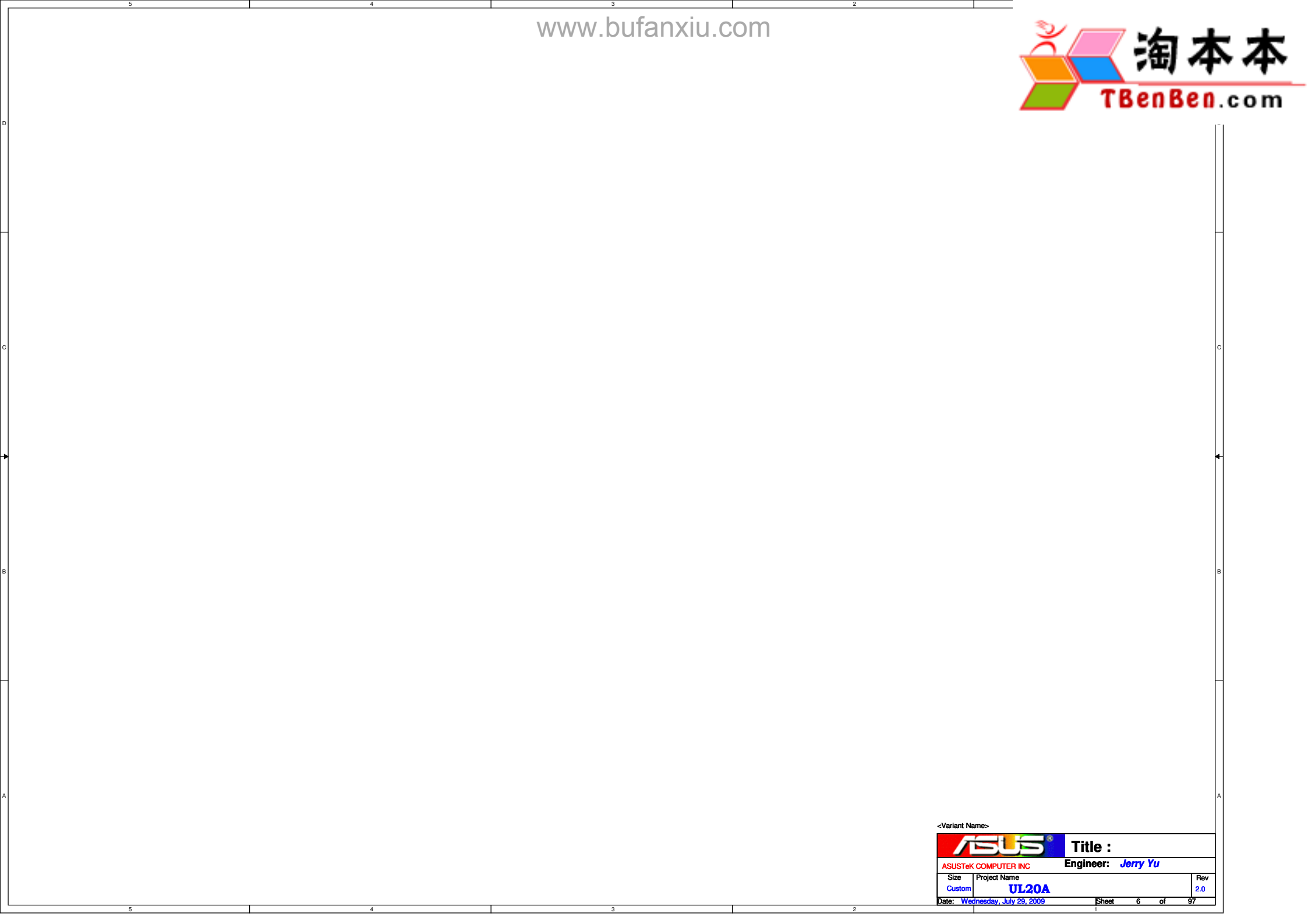
Thermal Trip signal (From CPU to ICH-9M and sequence)

Decoupling guide from Intel


VCCP	10uF mount	* 4pcs
VCCP	0.1uF mount	* 5pcs
VCCP	1uF	* 12pcs
VCCP	270uF	* 1pcs
VCCA	0.01uF	* 1 pcs
VCCA	10uF	* 1 pcs

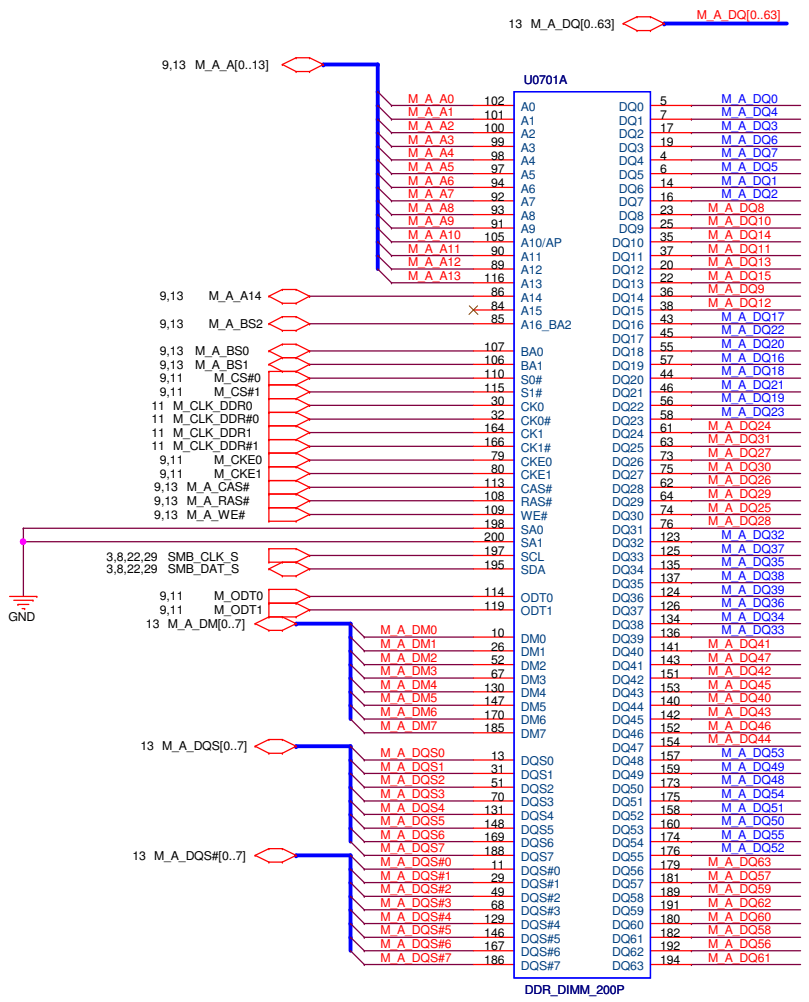
<Variant Name>

ASUS		Title :CPU CAPACITORS
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size	Project Name	Rev
Custom	UL20A	2.0
Date: Monday, August 03, 2009	Sheet	5 of 97



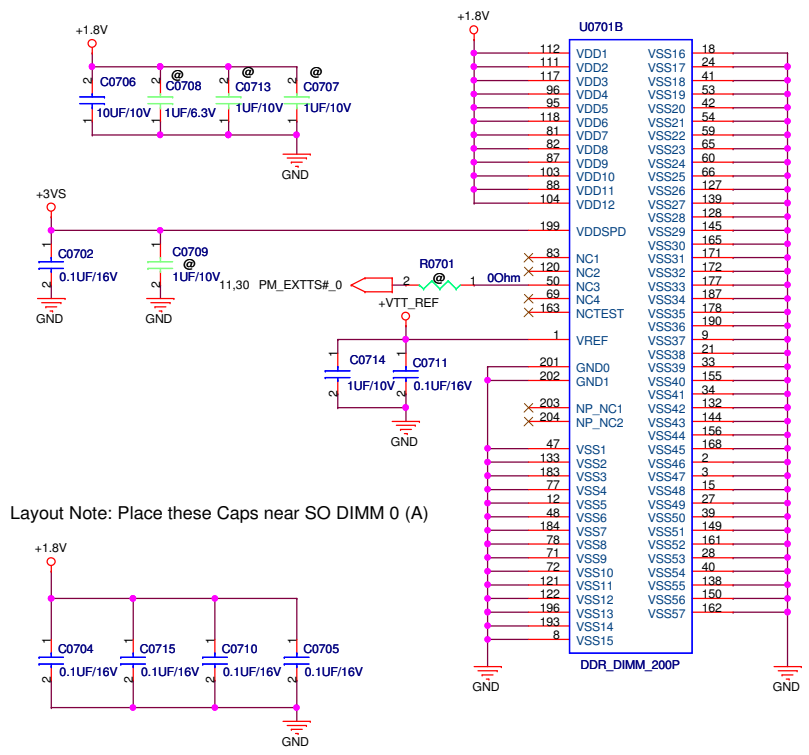
<Variant Name>

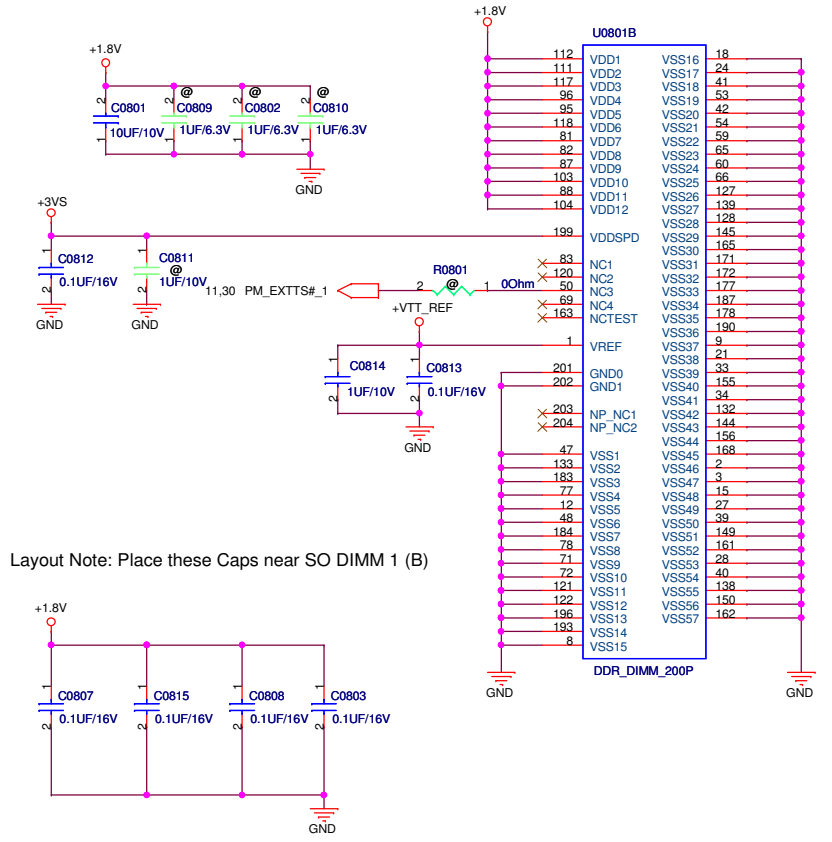
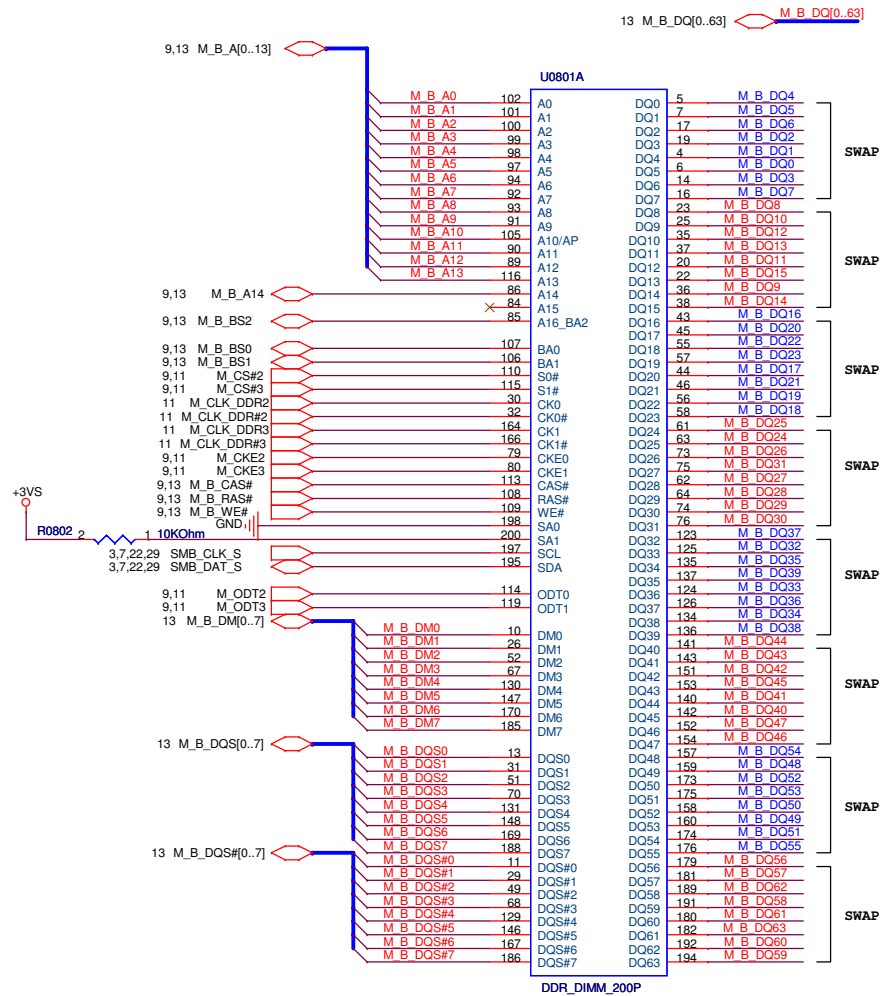
		Title :	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Wednesday, July 29, 2009		Sheet	6 of 97

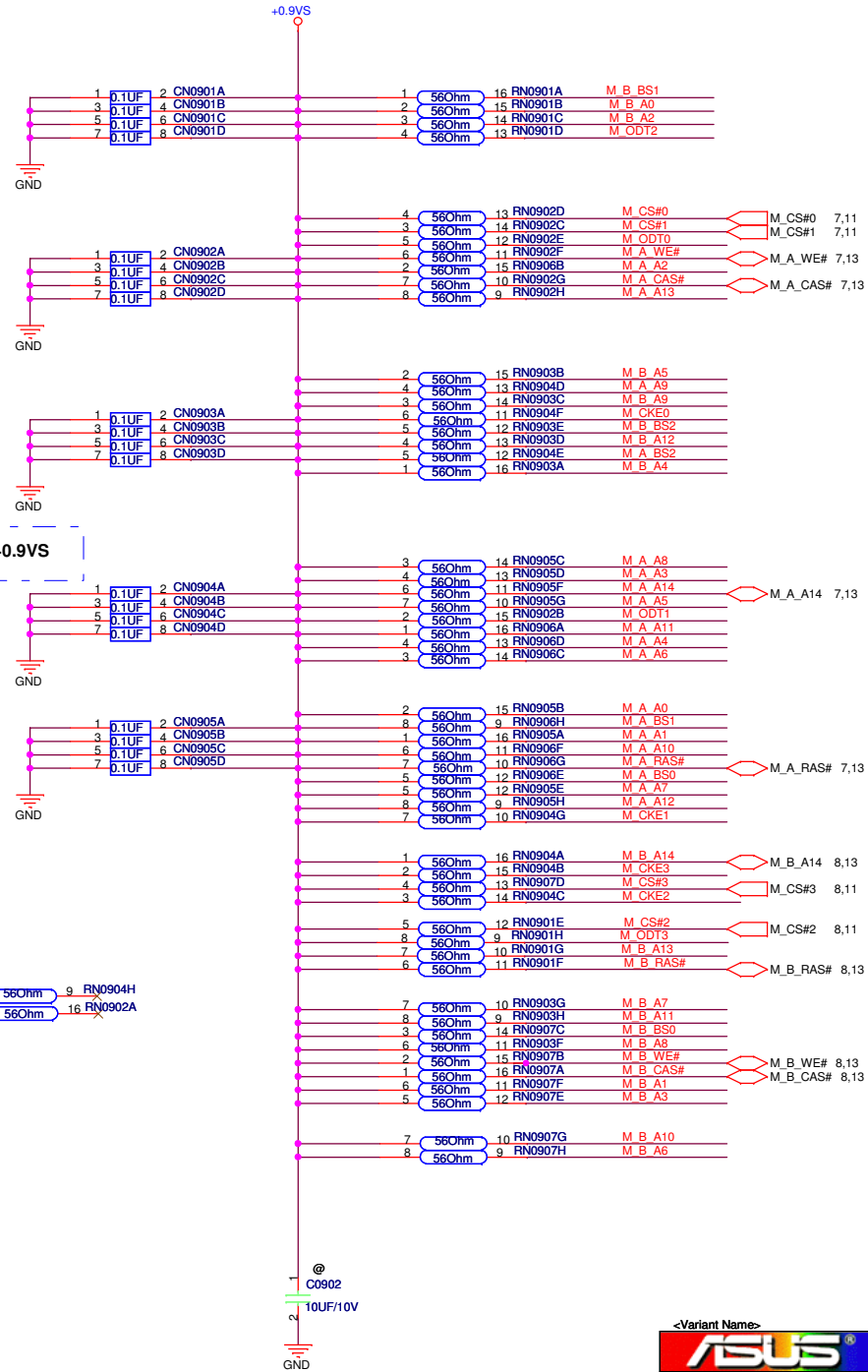
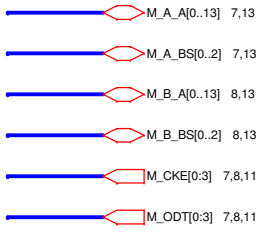


PN : 12G02533200E
STD

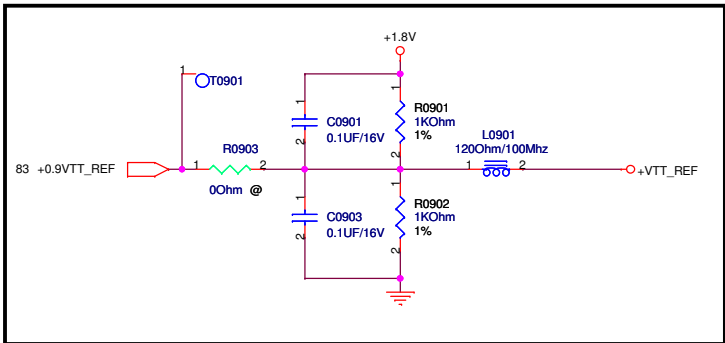
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP
SWAP



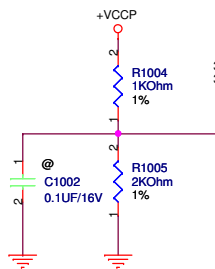
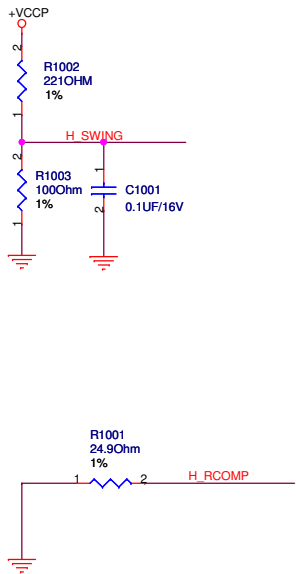




Layout note: Place array cap close to each pullup resistors terminated to +0.9VS



ASUS		Title : DIM DDR2 VREF	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Monday, August 03, 2009	Sheet 9 of 97		

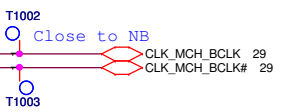
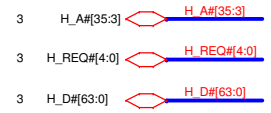


Place on Top
T1001

U1001A		
H_D#0	J7	H_D#_0
H_D#1	H6	H_D#_1
H_D#2	L11	H_D#_2
H_D#3	J3	H_D#_3
H_D#4	H4	H_D#_4
H_D#5	G3	H_D#_5
H_D#6	K10	H_D#_6
H_D#7	K12	H_D#_7
H_D#8	L1	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	M6	H_D#_10
H_D#11	N11	H_D#_11
H_D#12	L7	H_D#_12
H_D#13	K6	H_D#_13
H_D#14	M4	H_D#_14
H_D#15	K4	H_D#_15
H_D#16	F6	H_D#_16
H_D#17	W9	H_D#_17
H_D#18	V6	H_D#_18
H_D#19	V2	H_D#_19
H_D#20	P10	H_D#_20
H_D#21	W7	H_D#_21
H_D#22	N9	H_D#_22
H_D#23	P4	H_D#_23
H_D#24	U9	H_D#_24
H_D#25	V4	H_D#_25
H_D#26	U1	H_D#_26
H_D#27	W3	H_D#_27
H_D#28	V10	H_D#_28
H_D#29	U7	H_D#_29
H_D#30	W11	H_D#_30
H_D#31	U11	H_D#_31
H_D#32	AC11	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	Y4	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	AB6	H_D#_36
H_D#37	AA9	H_D#_37
H_D#38	AE10	H_D#_38
H_D#39	AA1	H_D#_39
H_D#40	AC3	H_D#_40
H_D#41	AC7	H_D#_41
H_D#42	AD12	H_D#_42
H_D#43	AB4	H_D#_43
H_D#44	Y6	H_D#_44
H_D#45	AD10	H_D#_45
H_D#46	AA11	H_D#_46
H_D#47	AB2	H_D#_47
H_D#48	AD4	H_D#_48
H_D#49	AE7	H_D#_49
H_D#50	AD2	H_D#_50
H_D#51	AE3	H_D#_51
H_D#52	AG9	H_D#_52
H_D#53	AG7	H_D#_53
H_D#54	AE11	H_D#_54
H_D#55	AK6	H_D#_55
H_D#56	AF6	H_D#_56
H_D#57	AF6	H_D#_57
H_D#58	AJ9	H_D#_58
H_D#59	AH6	H_D#_59
H_D#60	AE12	H_D#_60
H_D#61	AH4	H_D#_61
H_D#62	AJ7	H_D#_62
H_D#63	AE9	H_D#_63
H_SWING	B6	H_SWING
H_RCOMP	D4	H_RCOMP
H_CPURST#	J11	H_CPURST#
H_CPUSLP#	G9	H_CPUSLP#
H_AVREF	L17	H_AVREF
H_DVREF	K18	H_DVREF

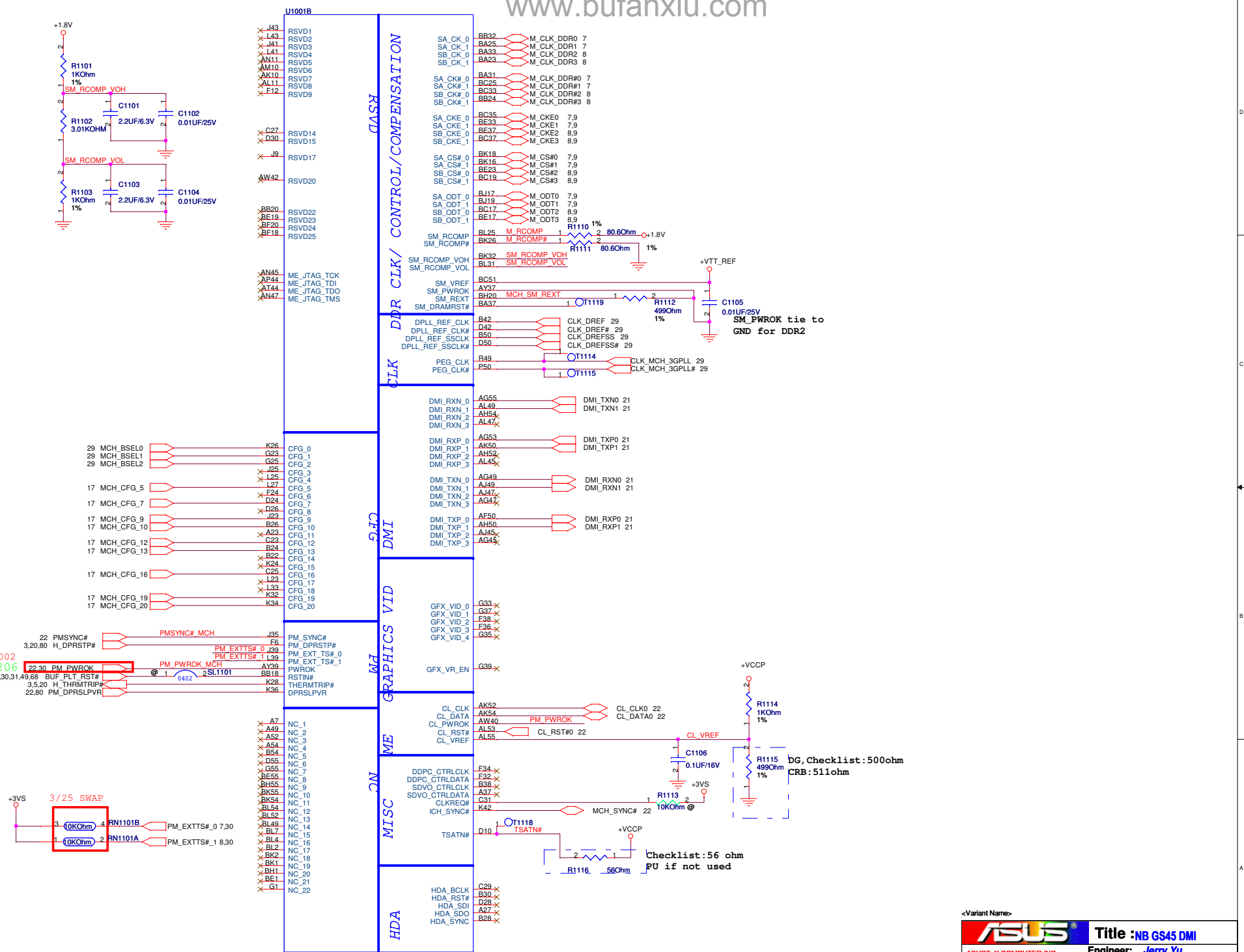
HOST

H_A#_3	L15	H_A#3
H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	E14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	D14	H_A#13
H_A#_14	K16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	B16	H_A#16
H_A#_17	C21	H_A#17
H_A#_18	D18	H_A#18
H_A#_19	J19	H_A#19
H_A#_20	J21	H_A#20
H_A#_21	B18	H_A#21
H_A#_22	D22	H_A#22
H_A#_23	G19	H_A#23
H_A#_24	J17	H_A#24
H_A#_25	L21	H_A#25
H_A#_26	L19	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	D20	H_A#28
H_A#_29	K22	H_A#29
H_A#_30	F18	H_A#30
H_A#_31	K20	H_A#31
H_A#_32	F20	H_A#32
H_A#_33	F22	H_A#33
H_A#_34	B20	H_A#34
H_A#_35	A19	H_A#35
H_ADS#	F10	H_ADS# 3
H_ADSTB#_0	A15	H_ADSTB#0 3
H_ADSTB#_1	C19	H_ADSTB#1 3
H_BNR#	G9	H_BNR# 3
H_BPRI#	B8	H_BPRI# 3
H_BREQ#	E5	H_BREQ# 3
H_DEFER#	D6	H_DEFER# 3
H_DBSY#	AH10	H_DBSY# 3
HPLL_CLK	AH11	CLK_MCH_BCLK 29
HPLL_CLK#	AH11	CLK_MCH_BCLK# 29
H_DPWR#	G11	H_DPWR# 3
H_DRDY#	H2	H_DRDY# 3
H_HIT#	C7	H_HIT# 3
H_HITM#	F8	H_HITM# 3
H_LOCK#	A11	H_LOCK# 3
H_TRDY#	D8	H_TRDY# 3
H_DINV#_0	L9	H_DINV#0 3
H_DINV#_1	N7	H_DINV#1 3
H_DINV#_2	AA7	H_DINV#2 3
H_DINV#_3	AG3	H_DINV#3 3
H_DSTBN#_0	K2	H_DSTBN#0 3
H_DSTBN#_1	N3	H_DSTBN#1 3
H_DSTBN#_2	AA3	H_DSTBN#2 3
H_DSTBN#_3	AF4	H_DSTBN#3 3
H_DSTBP#_0	L3	H_DSTBP#0 3
H_DSTBP#_1	M2	H_DSTBP#1 3
H_DSTBP#_2	Y2	H_DSTBP#2 3
H_DSTBP#_3	AF2	H_DSTBP#3 3
H_REQ#_0	J13	H_REQ#0
H_REQ#_1	L13	H_REQ#1
H_REQ#_2	C13	H_REQ#2
H_REQ#_3	G13	H_REQ#3
H_REQ#_4	G15	H_REQ#4
H_RS#_0	F4	H_RS#0 3
H_RS#_1	F2	H_RS#1 3
H_RS#_2	G7	H_RS#2 3

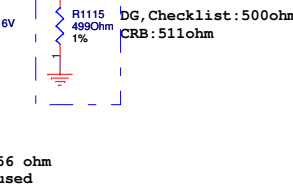
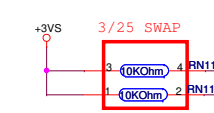


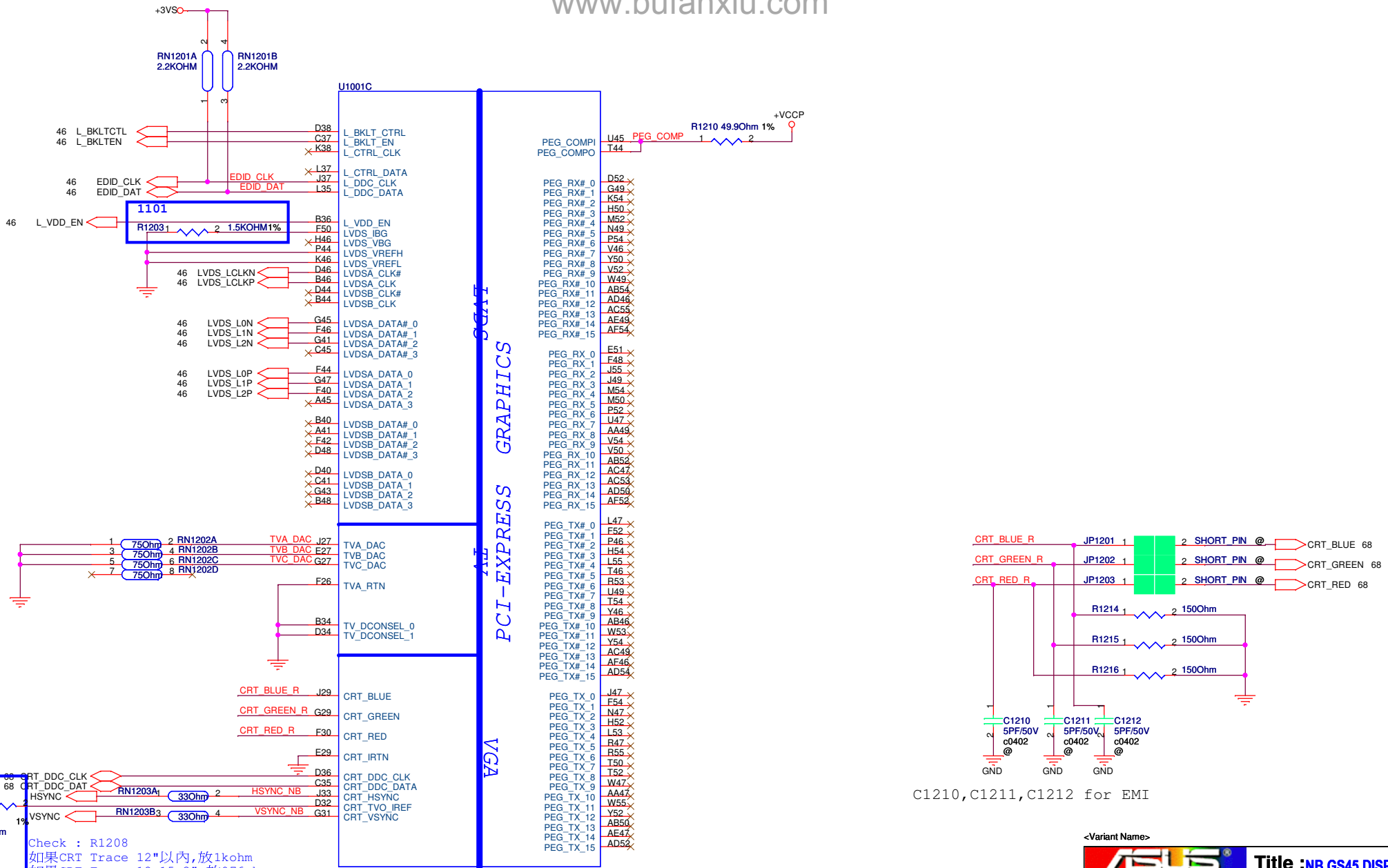
<Variant Name>

ASUS		Title :NB GS45 HOST	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name		
Custom	UL20A		
Date: Monday, August 03, 2009	Sheet	10	of 97
		Rev 2.0	



2002
1206





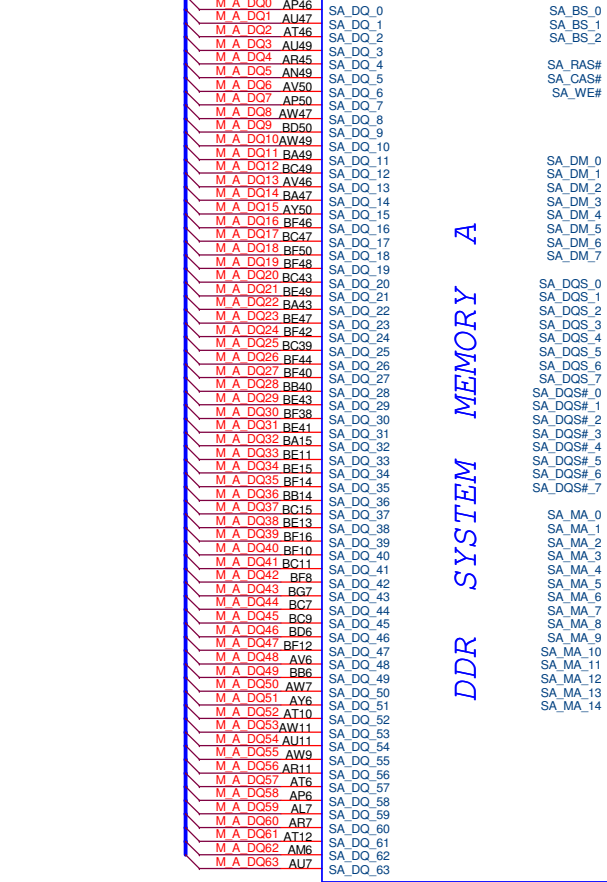
Check : R1208
 如果CRT Trace 12"以内,放1kohm
 如果CRT Trace 12~15.3",放976ohm

C1210, C1211, C1212 for EMI

<Variant Name>

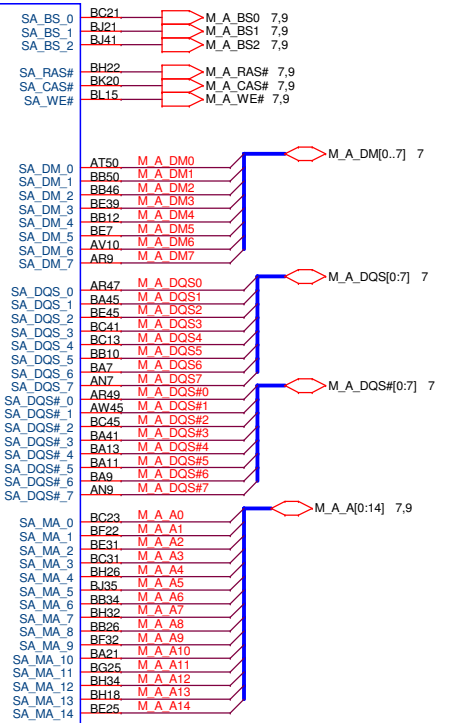
ASUS		Title :NB GS45 DISPLAY	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name		Rev
B	UL20A		2.0
Date: Monday, August 03, 2009	Sheet	12	of 97

7 M_A_DQ[0:63]

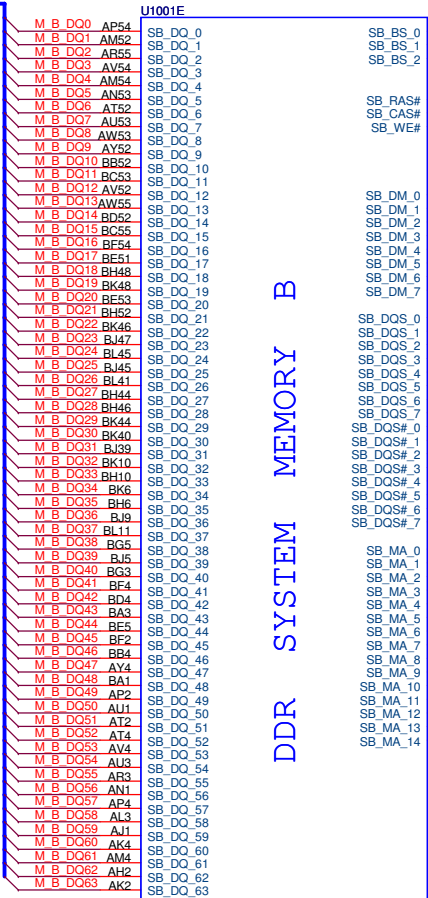


DDR SYSTEM MEMORY A

897605

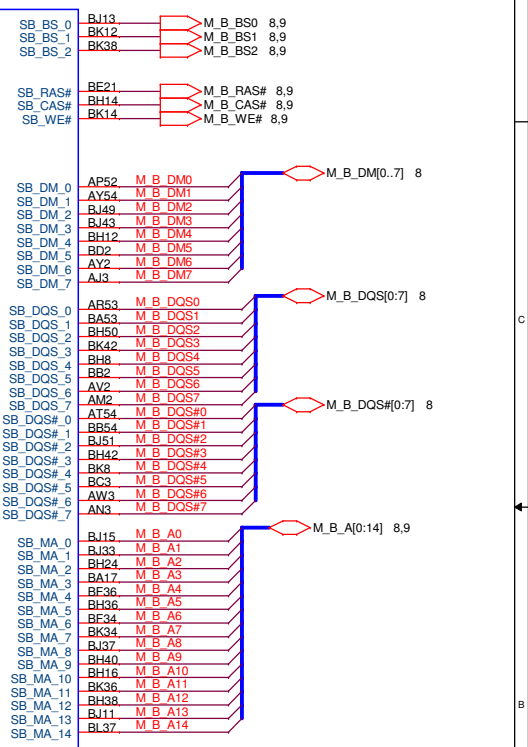


8 M_B_DQ[0:63]



DDR SYSTEM MEMORY B

897605

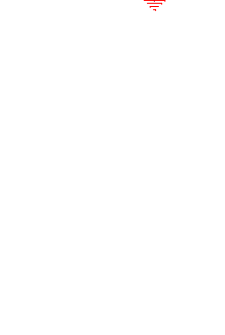
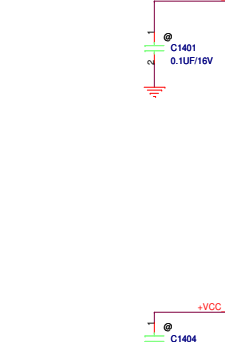


<Variant Name>

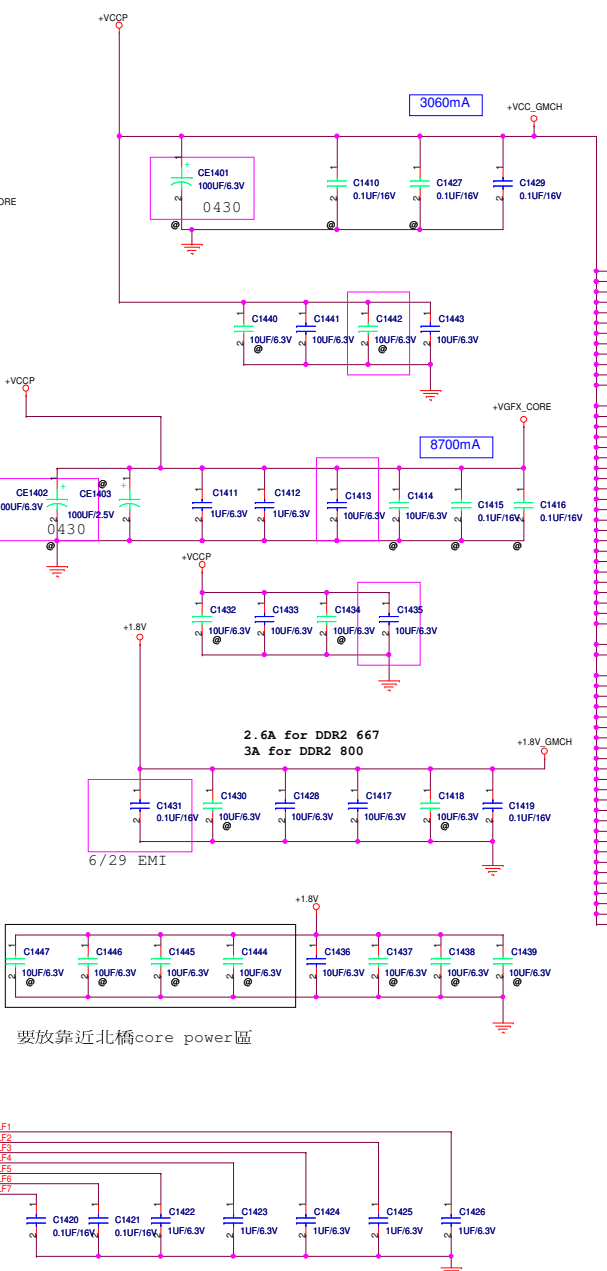
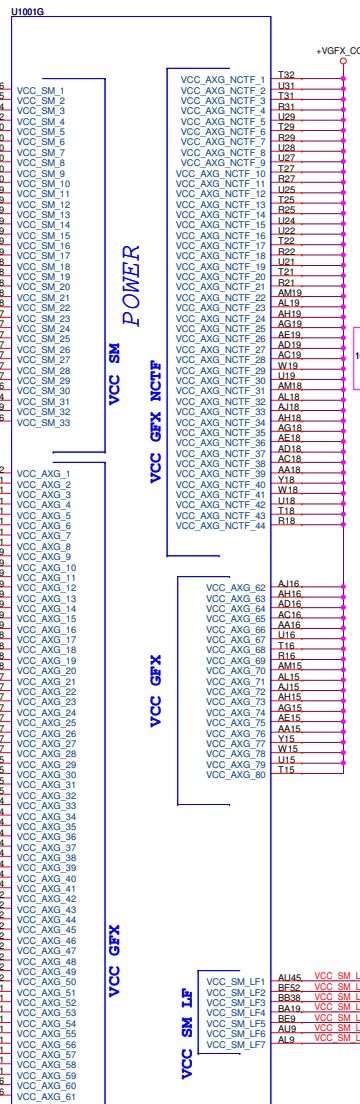
ASUS Title :NB GS45 DDR3 BUS
 ASUSTeK COMPUTER INC Engineer: Jerry Yu

Size	Project Name	Rev
Custom	UL20A	2.0
Date: Monday, August 03, 2009	Sheet	13 of 97

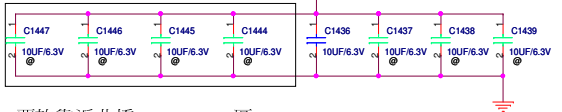
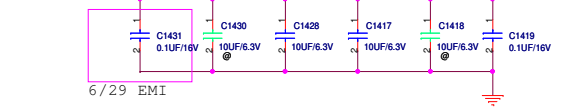
2.6A for DDR2 667
3A for DDR2 800



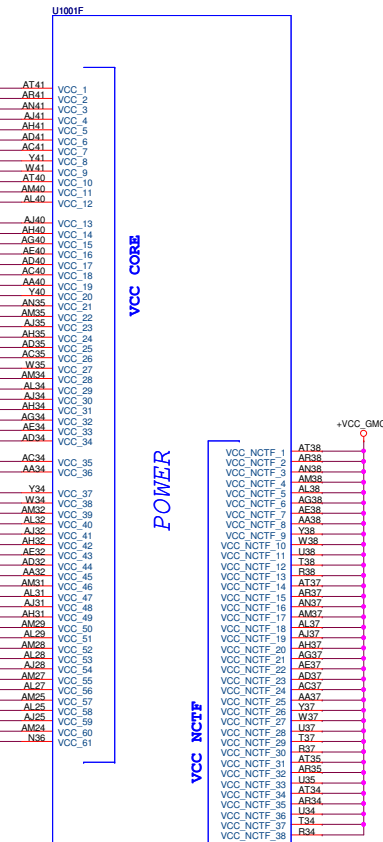
Route VCC AXG SENSE and VSS AXG SENSE differentially.

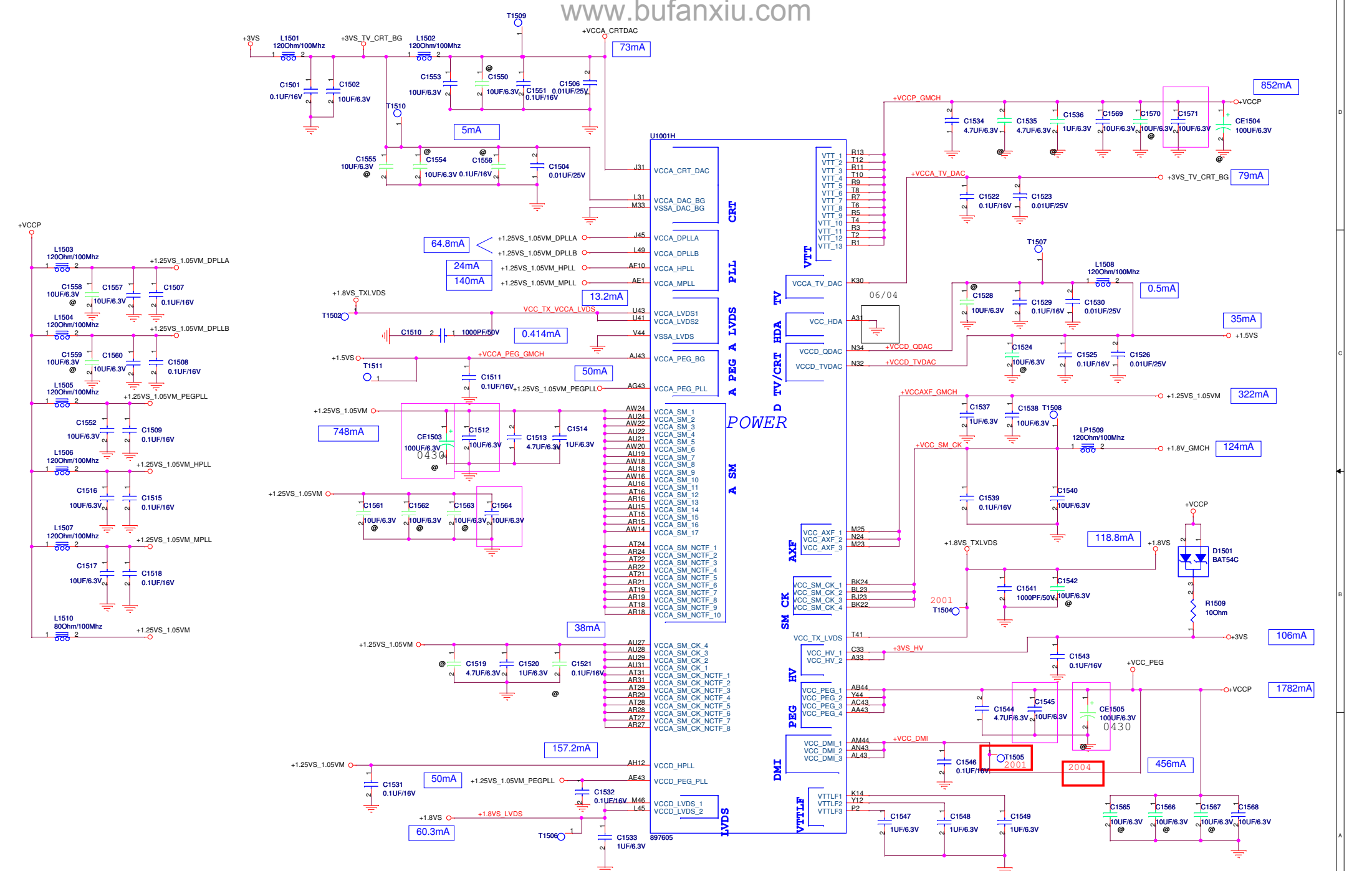


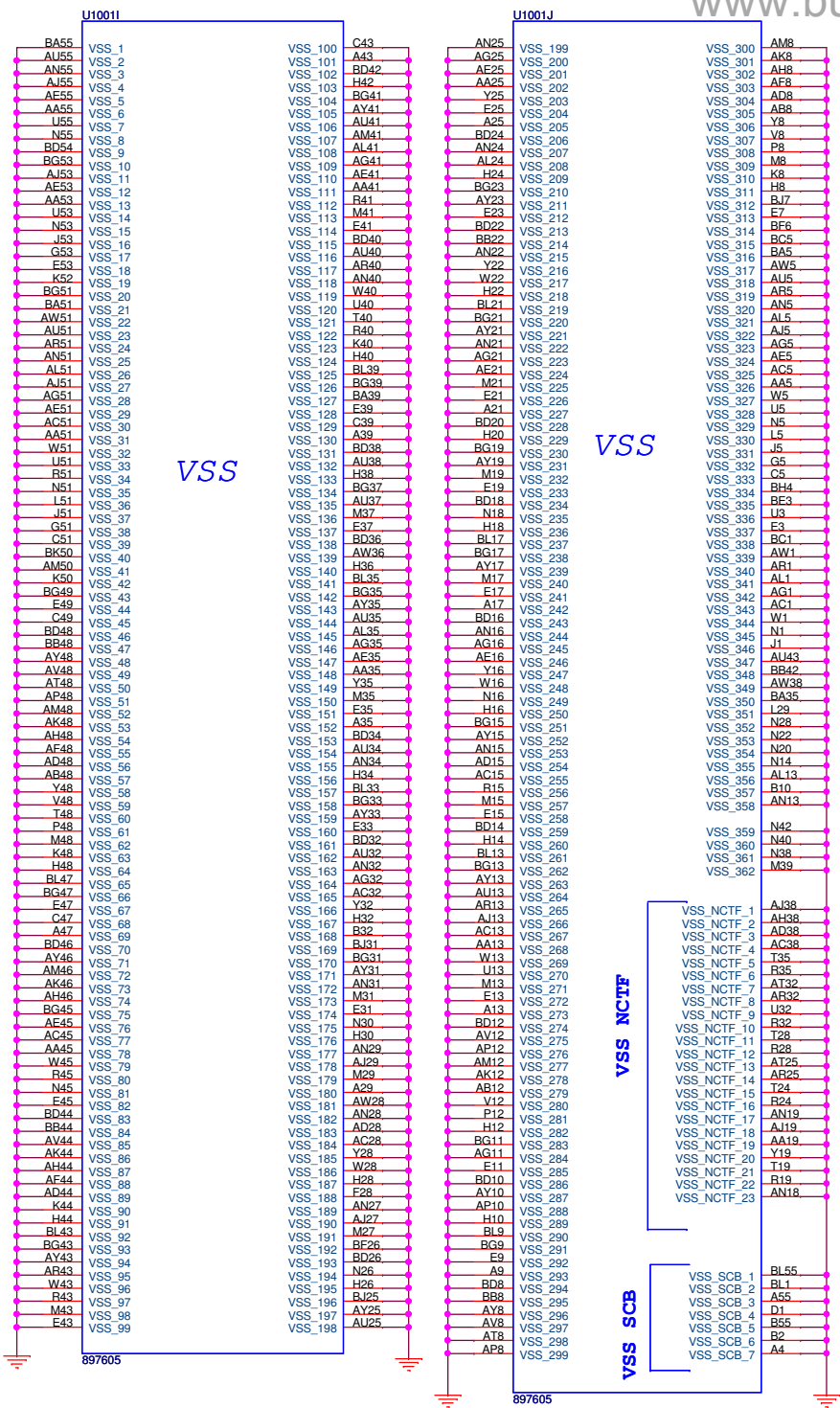
2.6A for DDR2 667
3A for DDR2 800



要放靠近北橋core power區

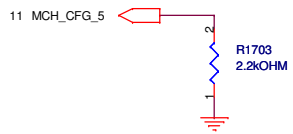






<Variant Name>

ASUS		Title :NB GS45 GND	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Wednesday, July 29, 2009	Sheet	16	of 97

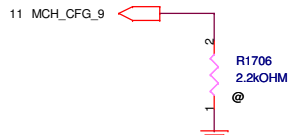


CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

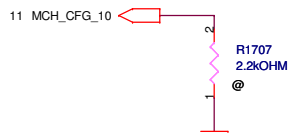
CFG6 : ITPM Host Interface
 (Relate to SPL_MOSI)
 H = ITPM Disable (Default)
 L = ITPM enable(Can disable by SW)



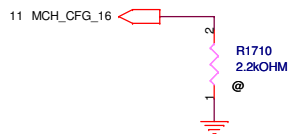
CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality



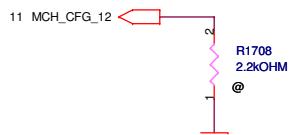
CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse



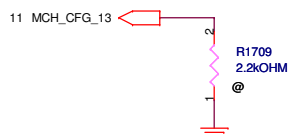
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable



CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

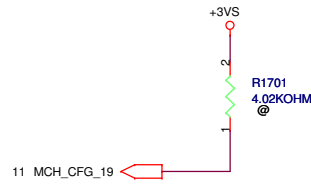


CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

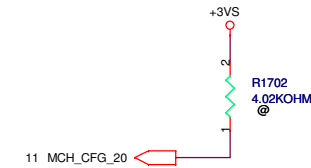


CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
 00 = Reserved
 01= XOR Mode Enabled
 10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)




CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>


ASUS		Title :NB GS45 STRAPPING	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size Custom	Project Name UL20A	Rev 2.0	
Date: Monday, August 03, 2009	Sheet	17	of 97

<Variant Name>

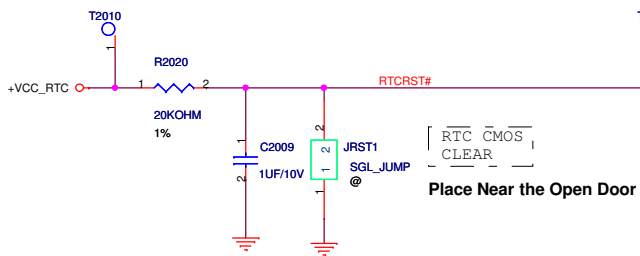
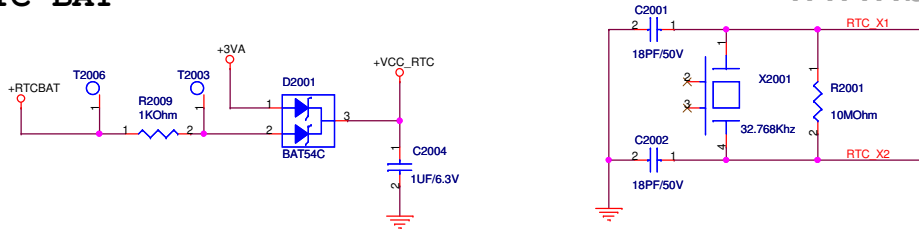
		Title :
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size	Project Name	Rev
C	UL20A	2.0
Date: Wednesday, July 29, 2009		Sheet 18 of 97

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

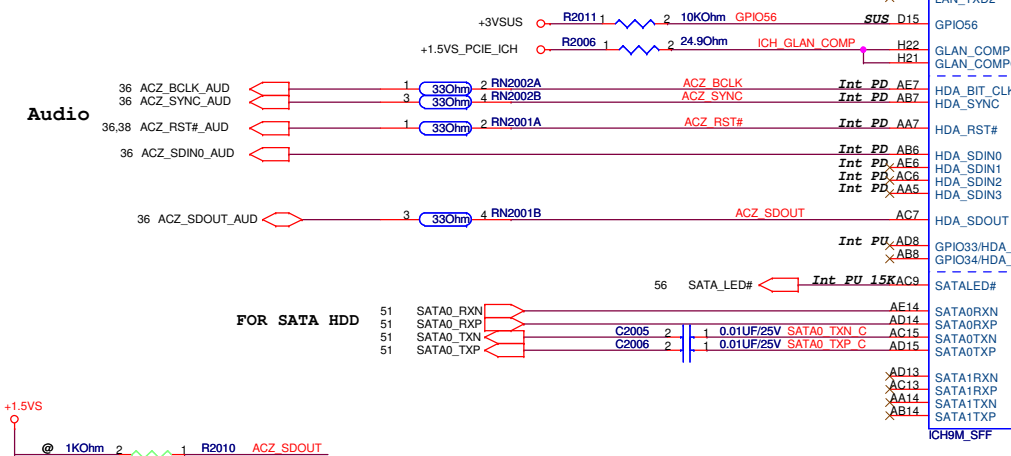
		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 19 of 97

RTC BAT



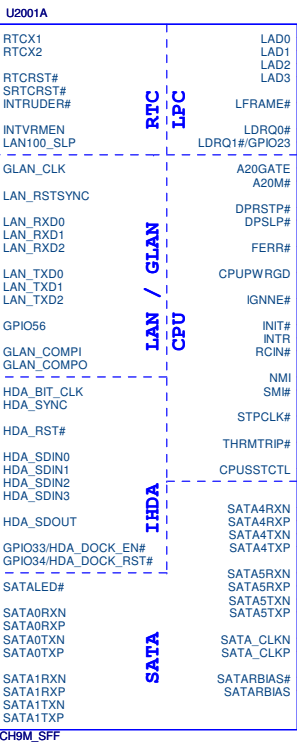
Check Intruder # 可不用1MOhm
并由332K改成100KOhm

LCI/GLCI disable guidelines
Design guide 4.19

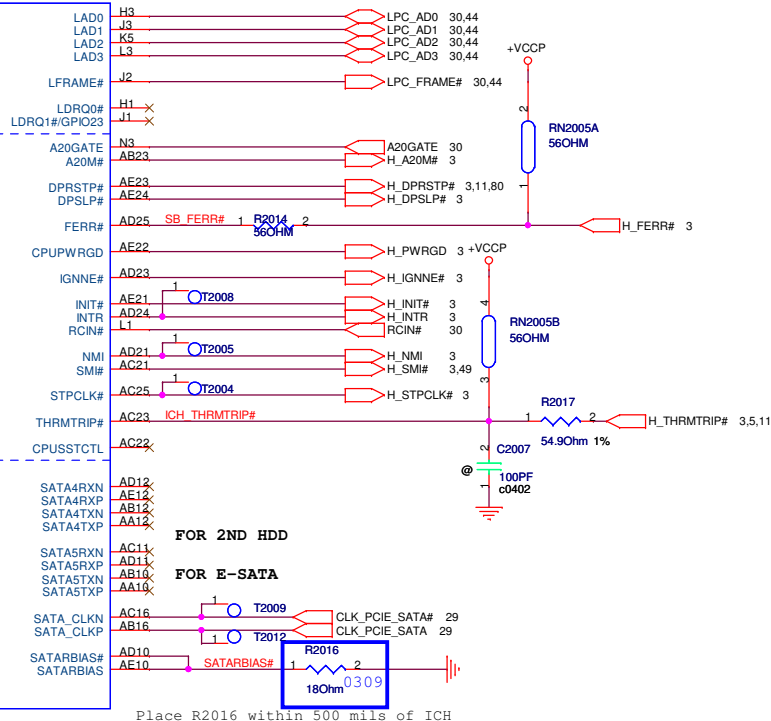


[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1

GPIO33:Flash Descriptor Security
Override
High = Enable (Default)
Low = Overriden



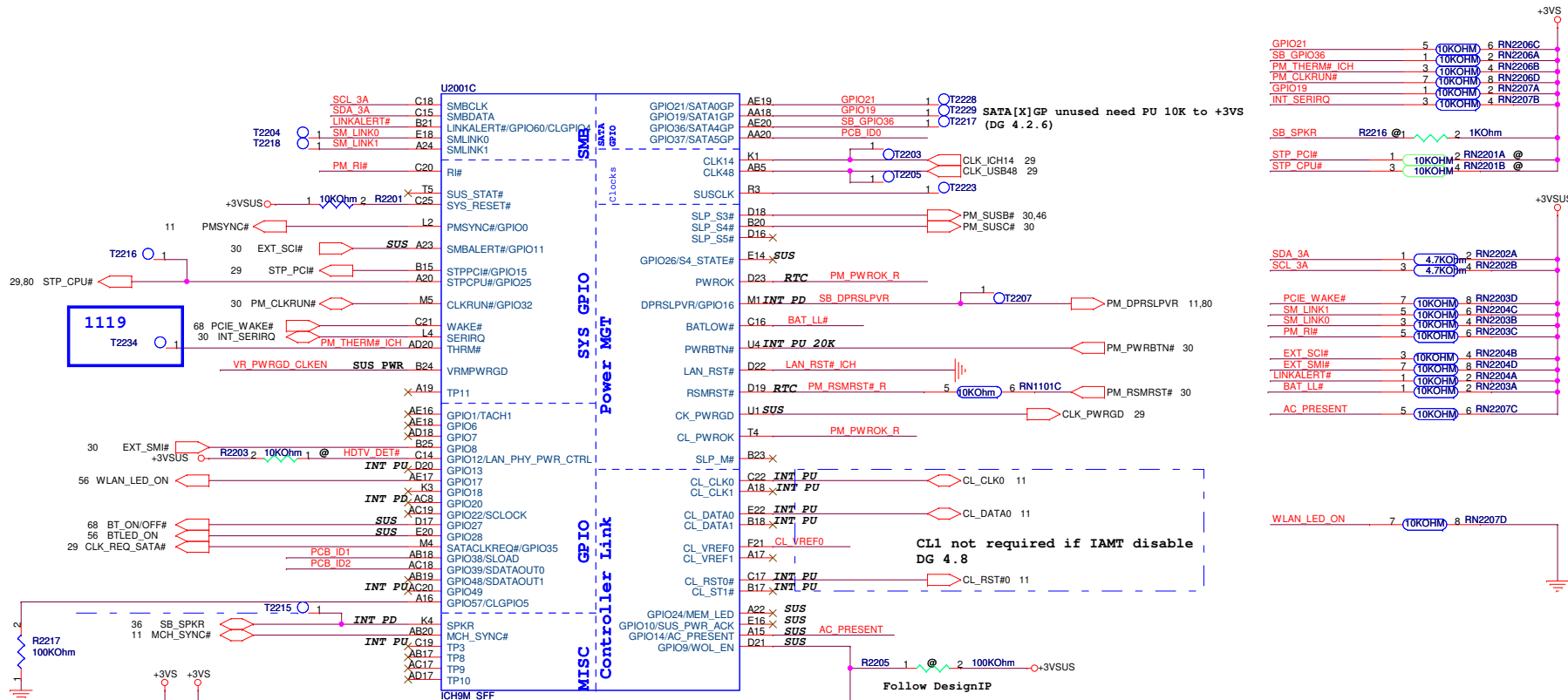
LAD[0:3] INT PU 20K



Place R2016 within 500 mils of ICH

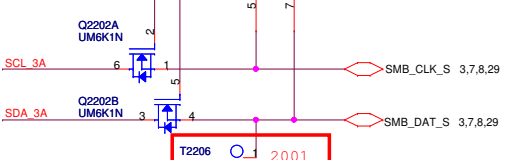
<Variant Name>

ASUS SB ICH9M PCI-PCIe DMI-USB
Title :
ASUSTeK COMPUTER INC Engineer: Jerry Yu
Size Project Name Rev
Custom UL20A 2.0
Date: Monday, August 03, 2009 Sheet 20 of 97



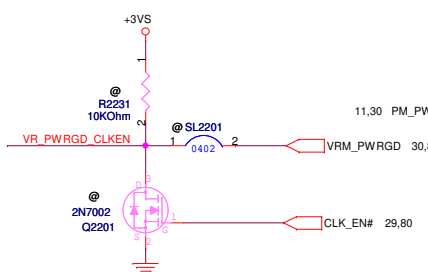
SR Check
Q2202可否直接SHORT

SPKR
No Reboot Strap
Low = Default
High = No Reboot

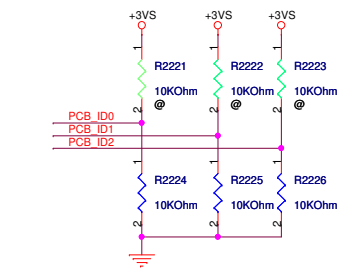


PCB ID	GPIO37 PCB_ID0	GPIO38 PCB_ID1	GPIO39 PCB_ID2
MBR1.0	0	0	0
MBR1.2	0	0	1
MBR2.0	0	1	0

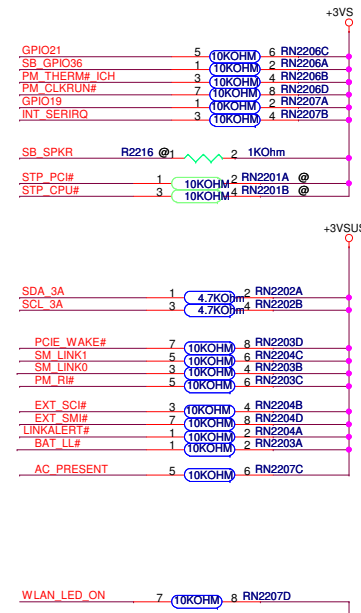
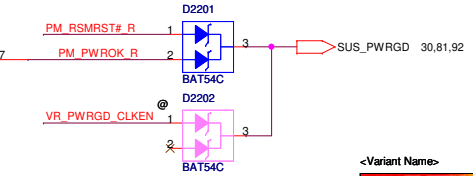
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max

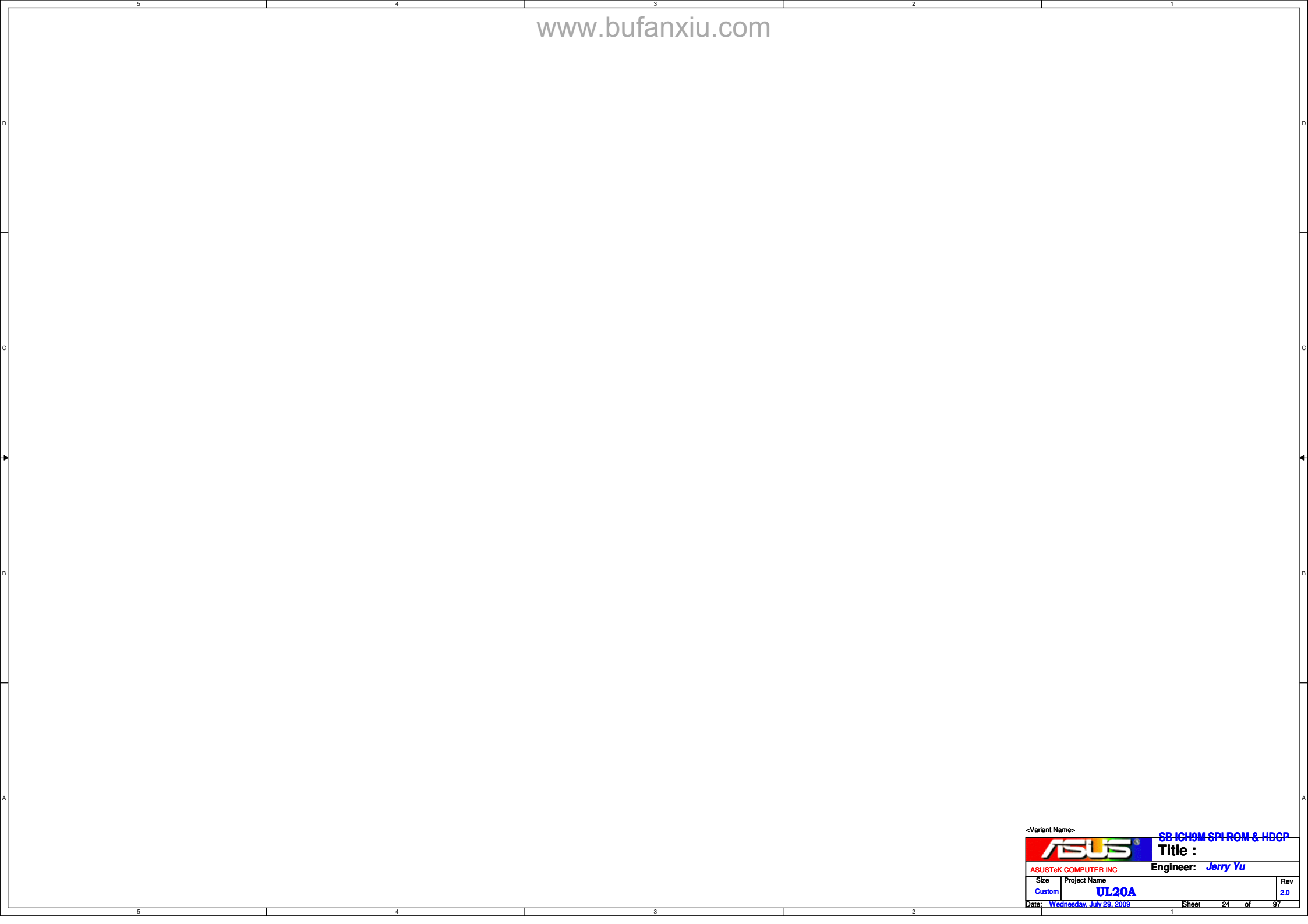


1206 2002




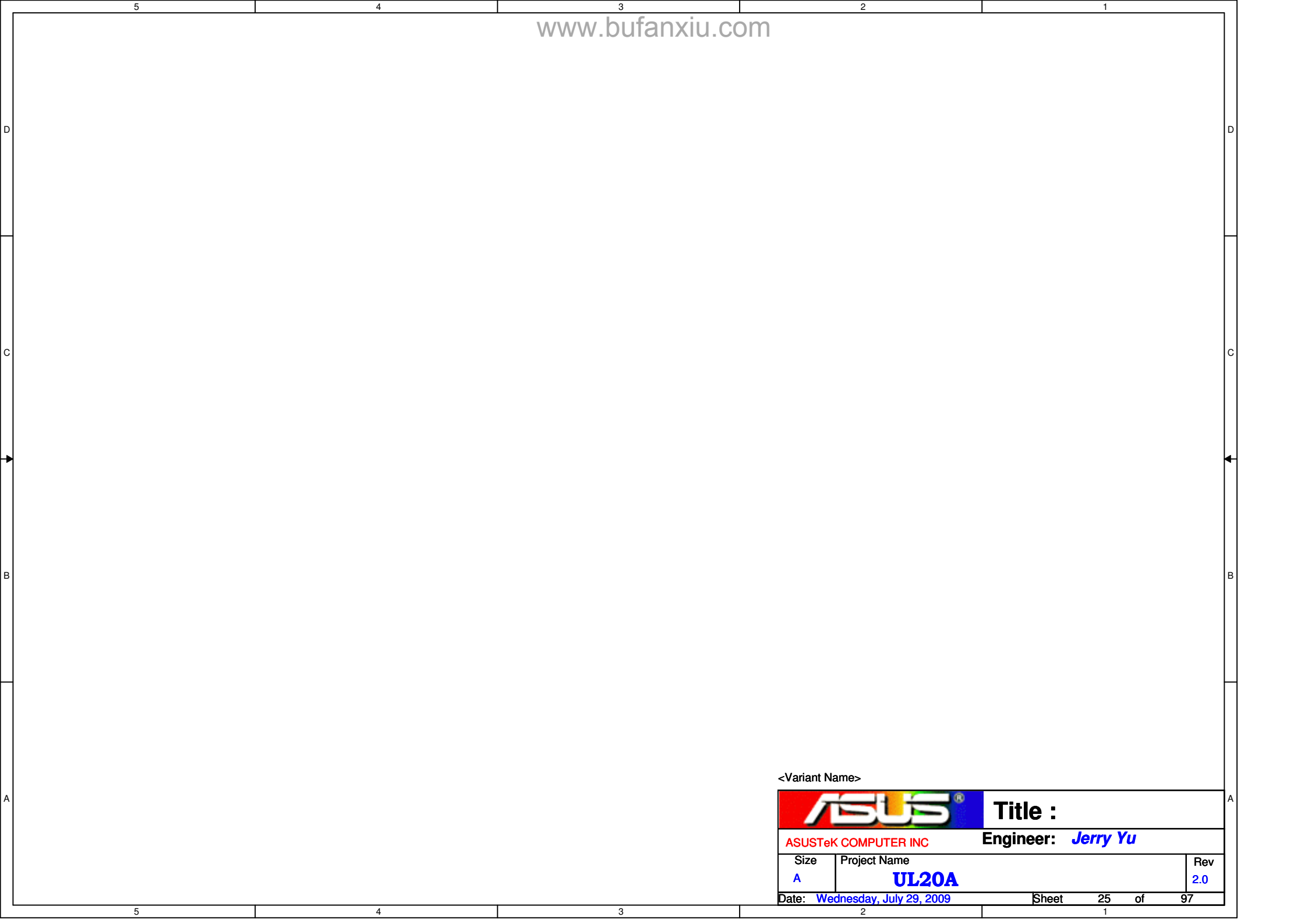
1203






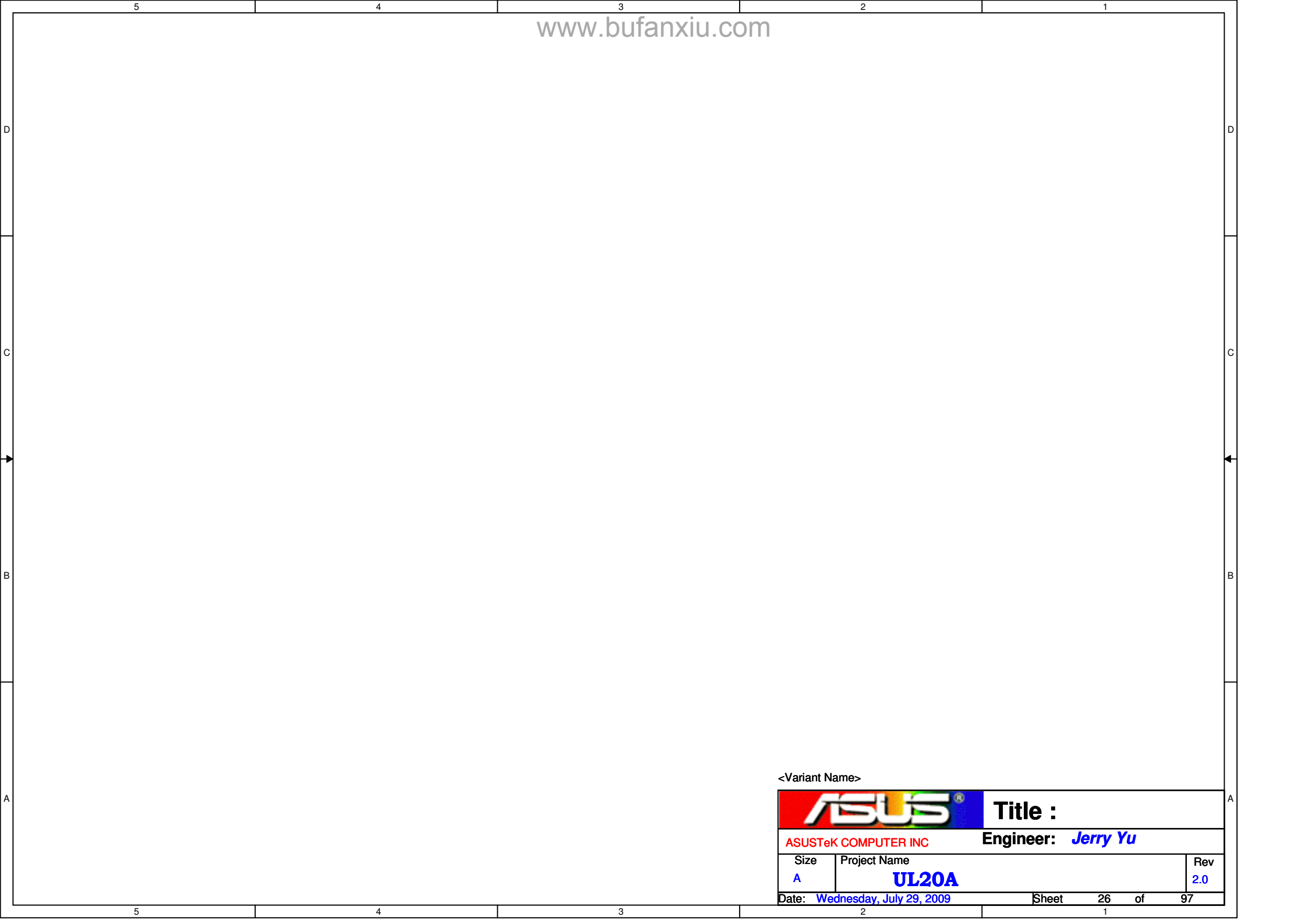
<Variant Name>

		SB ICH9M SPI-ROM & HDCP	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Wednesday, July 29, 2009		Sheet	24 of 97




<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	25 of 97




<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <i>Wednesday, July 29, 2009</i>		Sheet 26 of 97


5	4	3	2	1
D				D
C				C
B				B
A				A

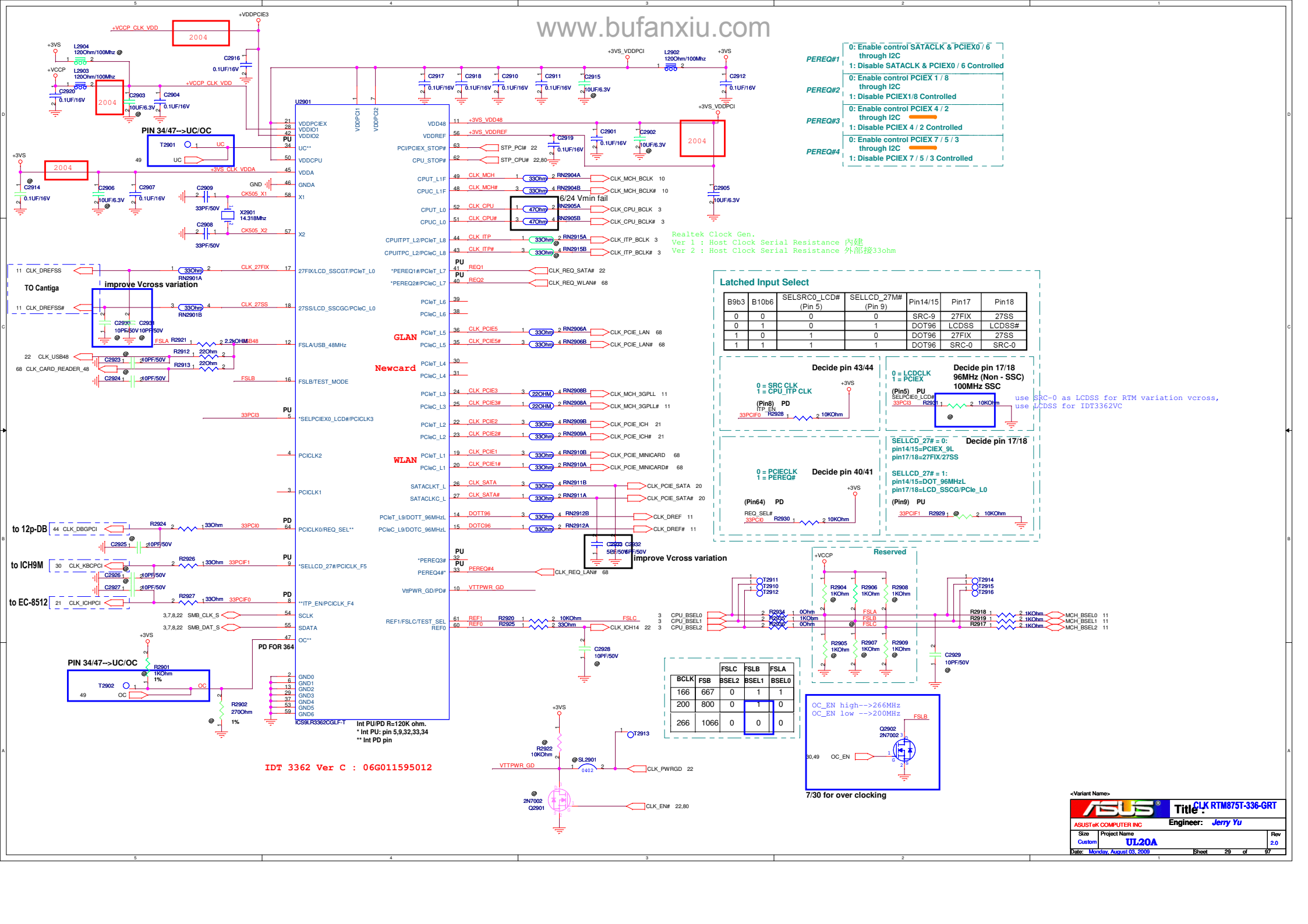
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	27 of 97

5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	28 of 97

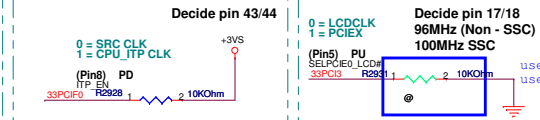


- PEREQ#1: 0: Enable control SATACLK & PCIeX0 / 6 through I2C; 1: Disable SATACLK & PCIeX0 / 6 Controlled
- PEREQ#2: 0: Enable control PCIeX 1 / 8 through I2C; 1: Disable PCIeX1/8 Controlled
- PEREQ#3: 0: Enable control PCIeX 4 / 2 through I2C; 1: Disable PCIeX 4 / 2 Controlled
- PEREQ#4: 0: Enable control PCIeX 7 / 5 / 3 through I2C; 1: Disable PCIeX 7 / 5 / 3 Controlled

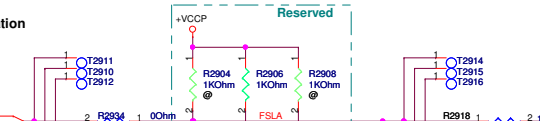
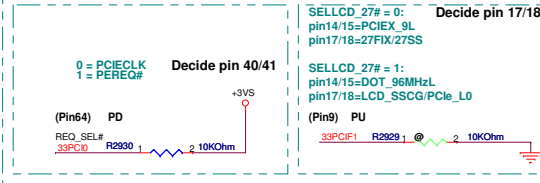
Realtek Clock Gen.
Ver 1 : Host Clock Serial Resistance 內建
Ver 2 : Host Clock Serial Resistance 外部接330hm

Latched Input Select

B9b3	B10b6	SELSRC0_LCD# (Pin 5)	SELLCD_27M# (Pin 9)	Pin14/15	Pin17	Pin18
0	0	0	0	SRC-9	27FIX	27SS
0	1	0	1	DOT96	LCDSS	LCDSS#
1	0	1	0	DOT96	27FIX	27SS
1	1	1	1	DOT96	SRC-0	SRC-0



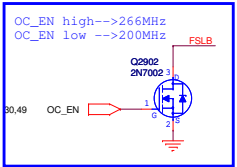
use SRC-0 as LCDSS for RTM variation vcross, use LCDSS for IDT3362VC



improve Vcross variation



BCLK	FSB	FSLC	FSLB	FSLA	BSEL2	BSEL1	BSEL0
166	667	0	1	1			
200	800	0	1	0			
266	1066	0	0	0			

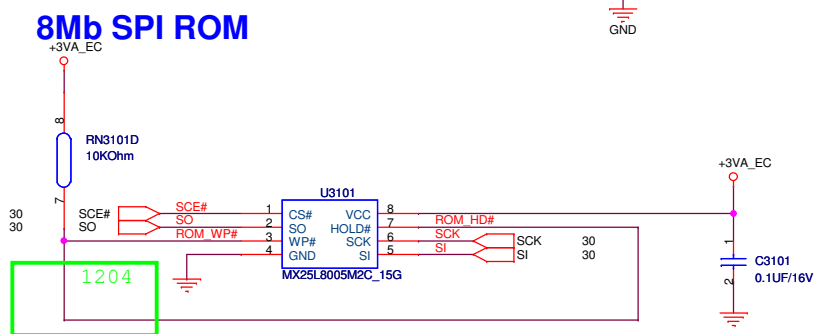
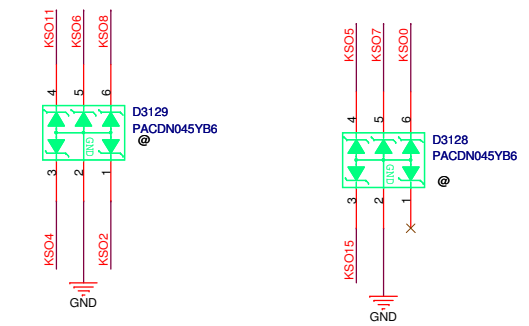
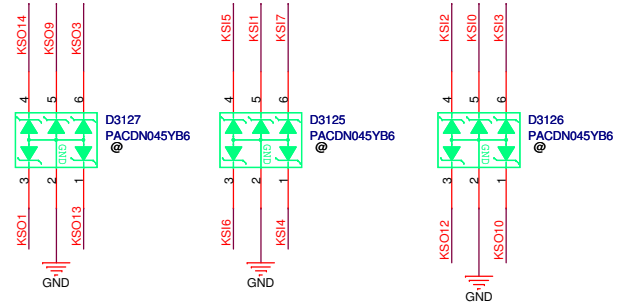
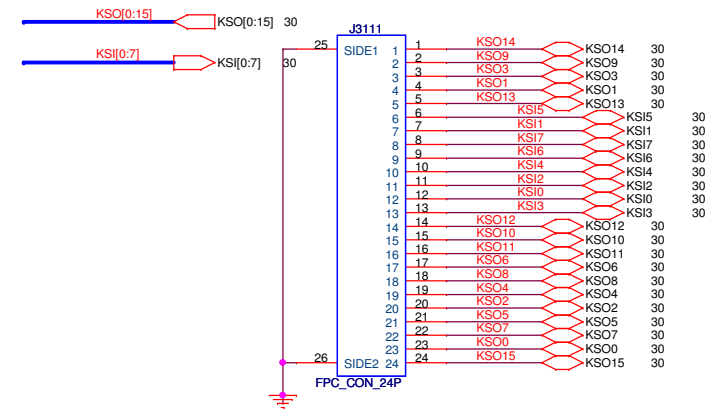
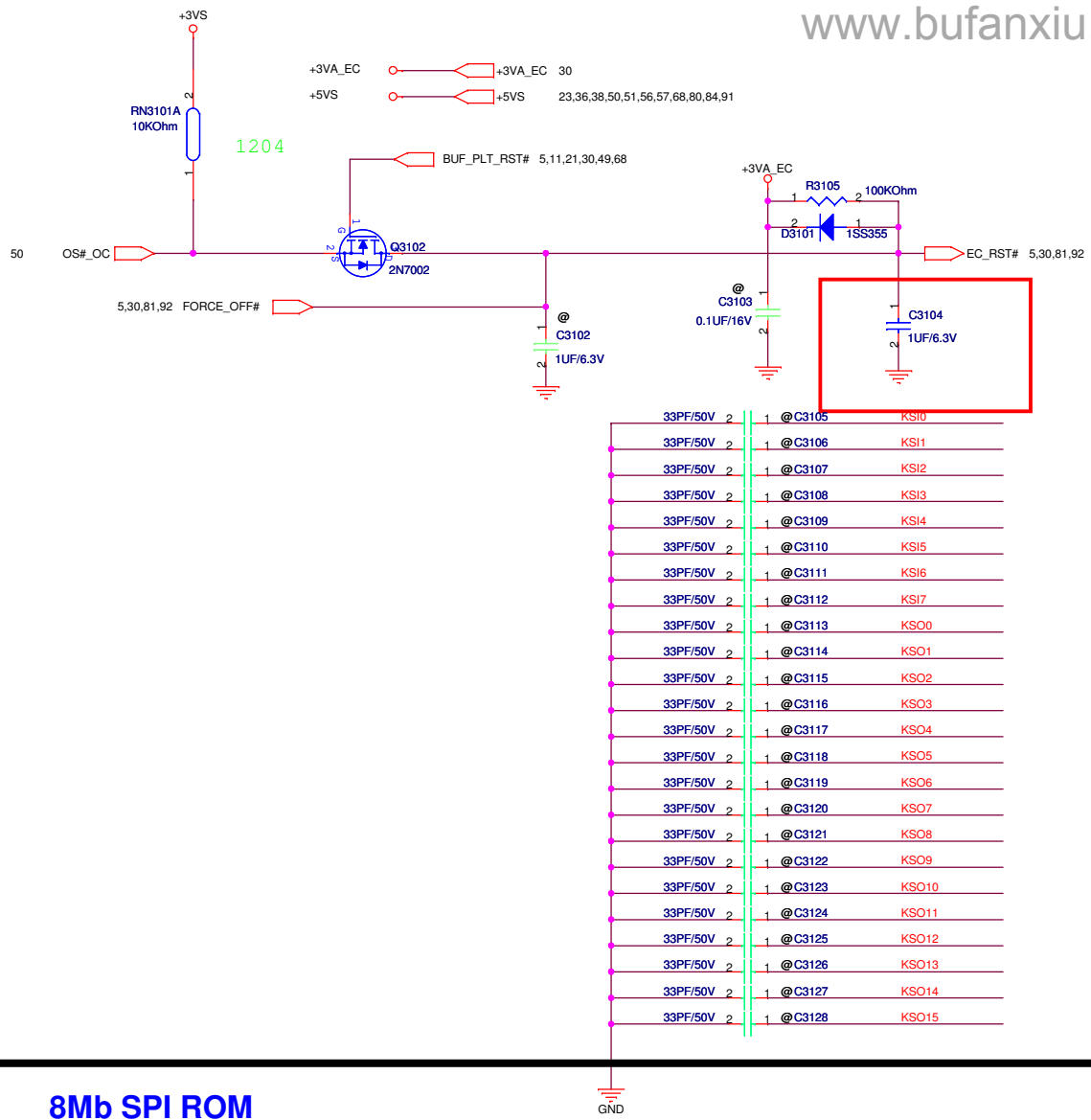


7/30 for over clocking

IDT 3362 Ver C : 06G011595012

Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin

Internal Keyboard



<Variant Name> **ROM FLASH ROM TOUCH PAD KB**

ASUS Title : _____


ASUSTeK COMPUTER INC Engineer: **Jerry Yu**

Size	Project Name	Rev
Custom	UL20A	2.0
Date: Monday, August 03, 2009	Sheet 31 of 97	


Parade PS8101T: Optional /PS
Stuff: R3216 R3219 R3201 R3215
No stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202
R3210 R3208 R3209 R3206 Q3201.

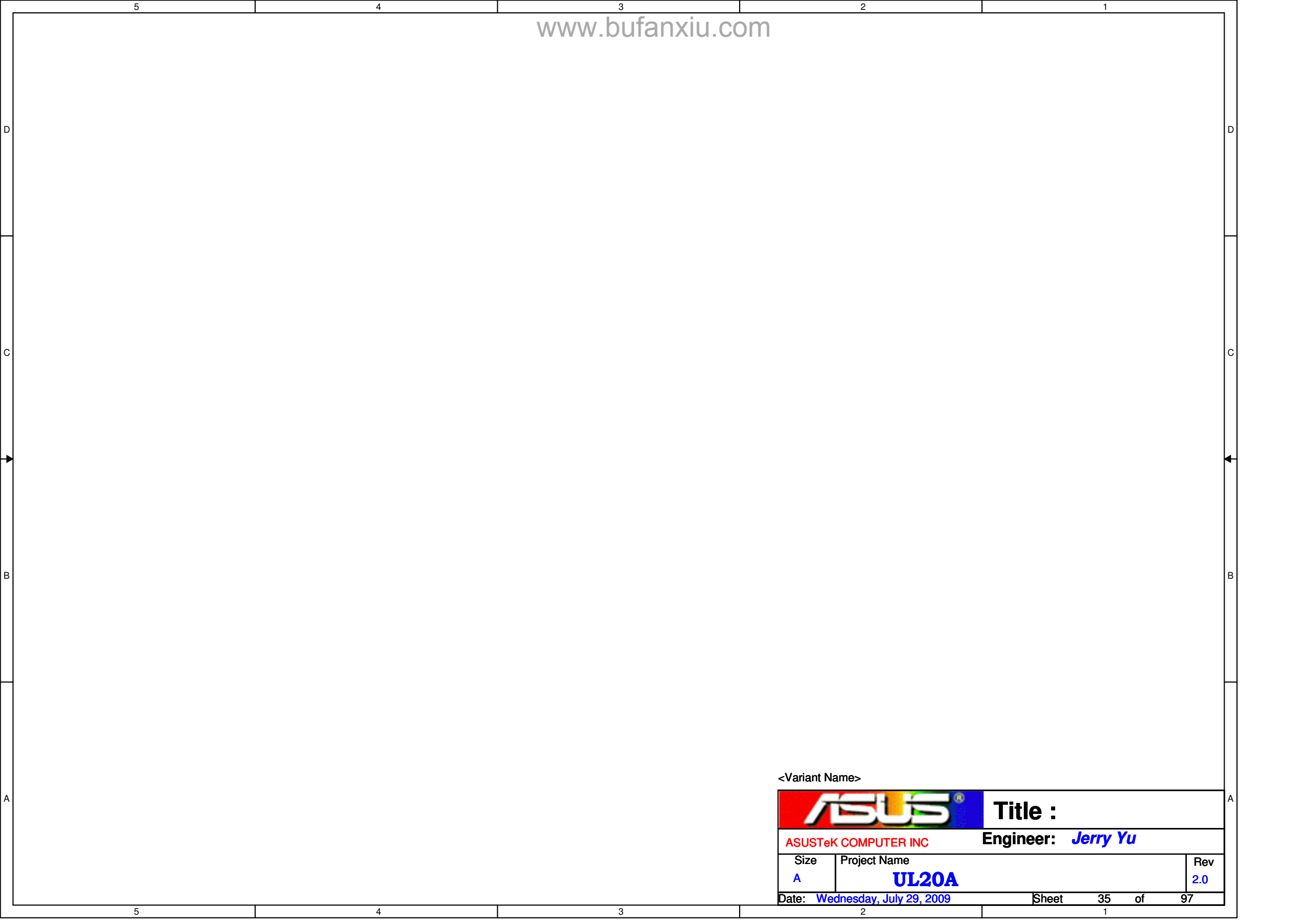
PERICOM PI3VDP411LSZDE: Optional /PI
No stuff: R3216 R3219 R3201 R3215
Stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202
R3210 R3208 R3209 R3206 Q3201.

<Variant Name>


		Title :AR8131 LAN
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size B	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 33 of 97

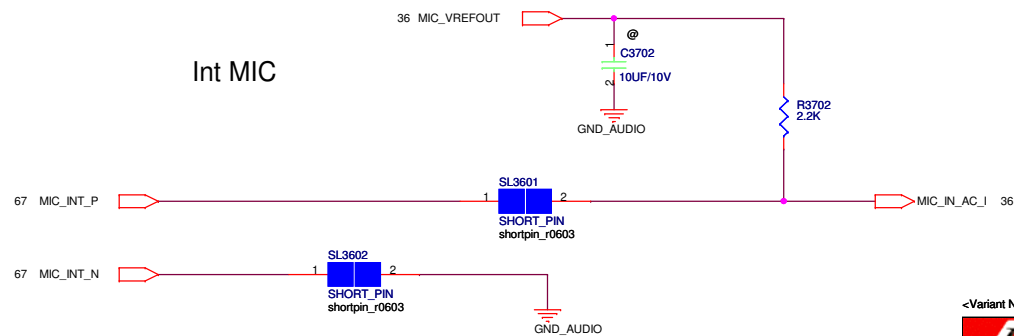
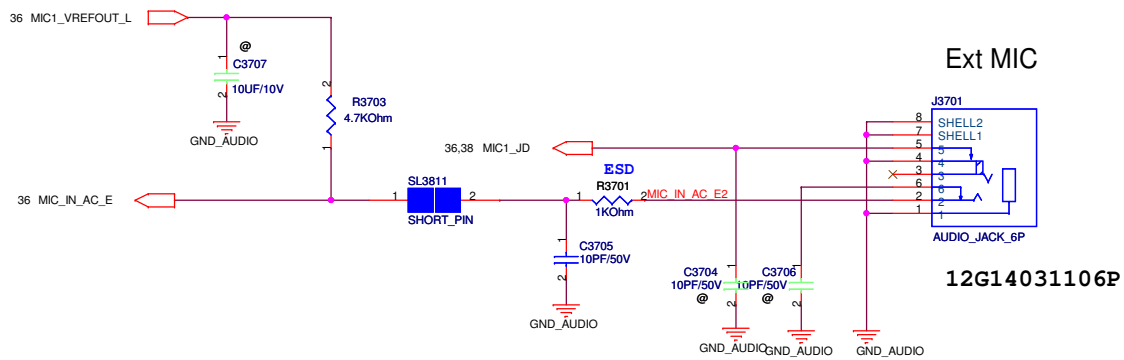
<Variant Name>

		Title : LAN RJ45 CONN
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size Custom	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 34 of 97



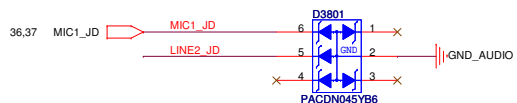
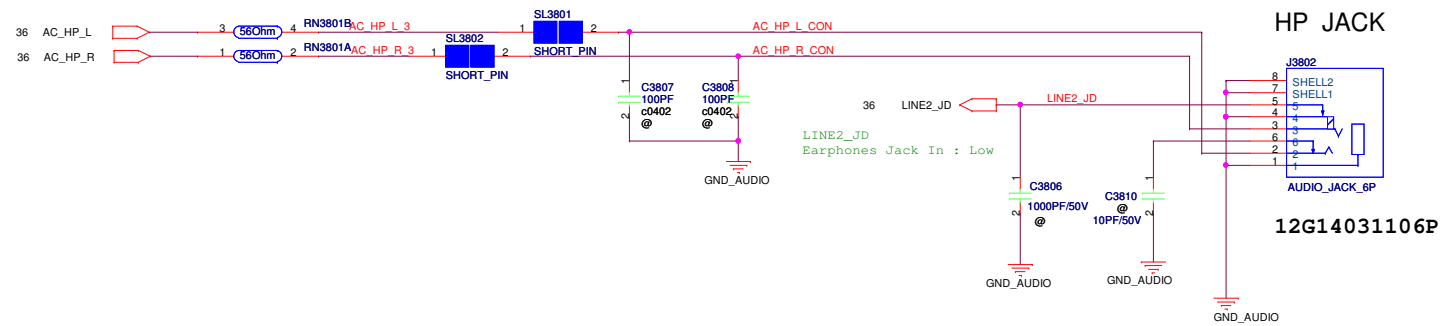
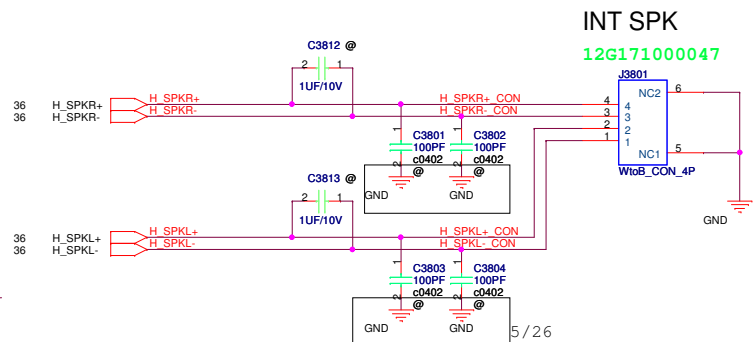
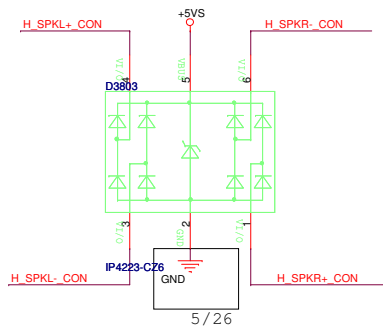
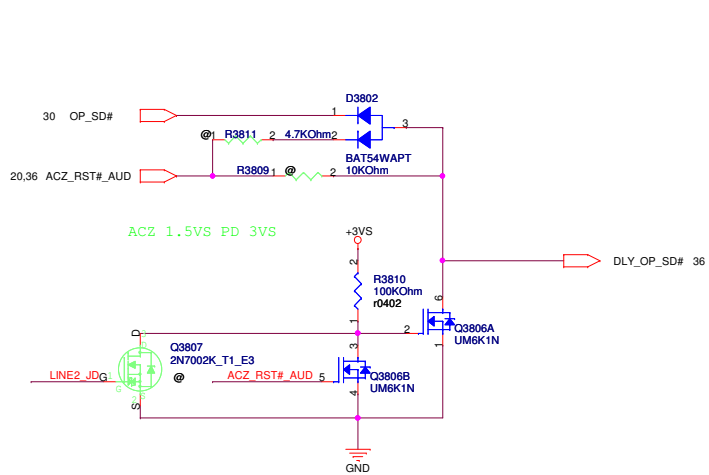
<Variant Name>

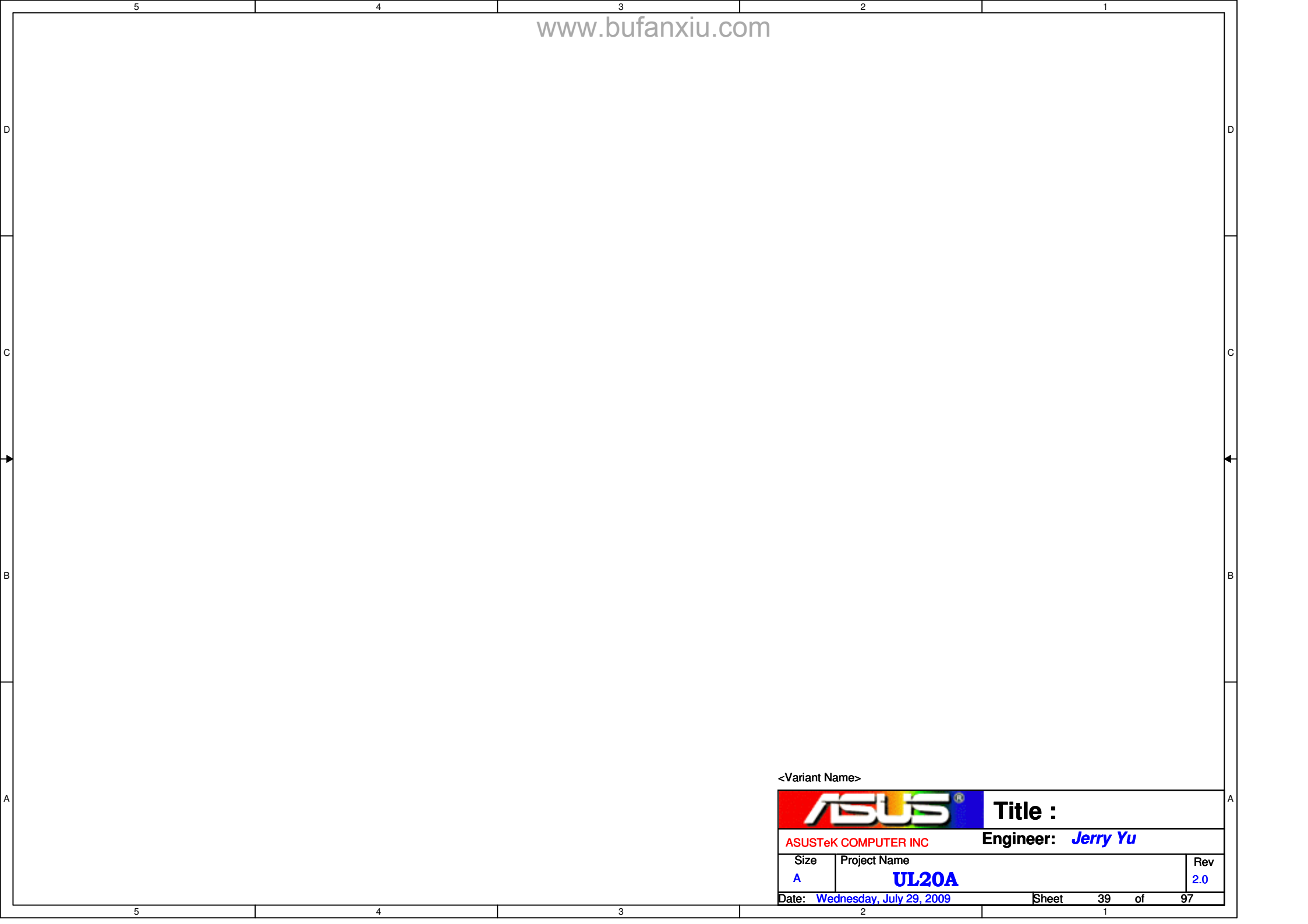
		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size	Project Name	Rev
A	UL20A	2.0
Date: Wednesday, July 29, 2009		Sheet 35 of 97




<Variant Name>

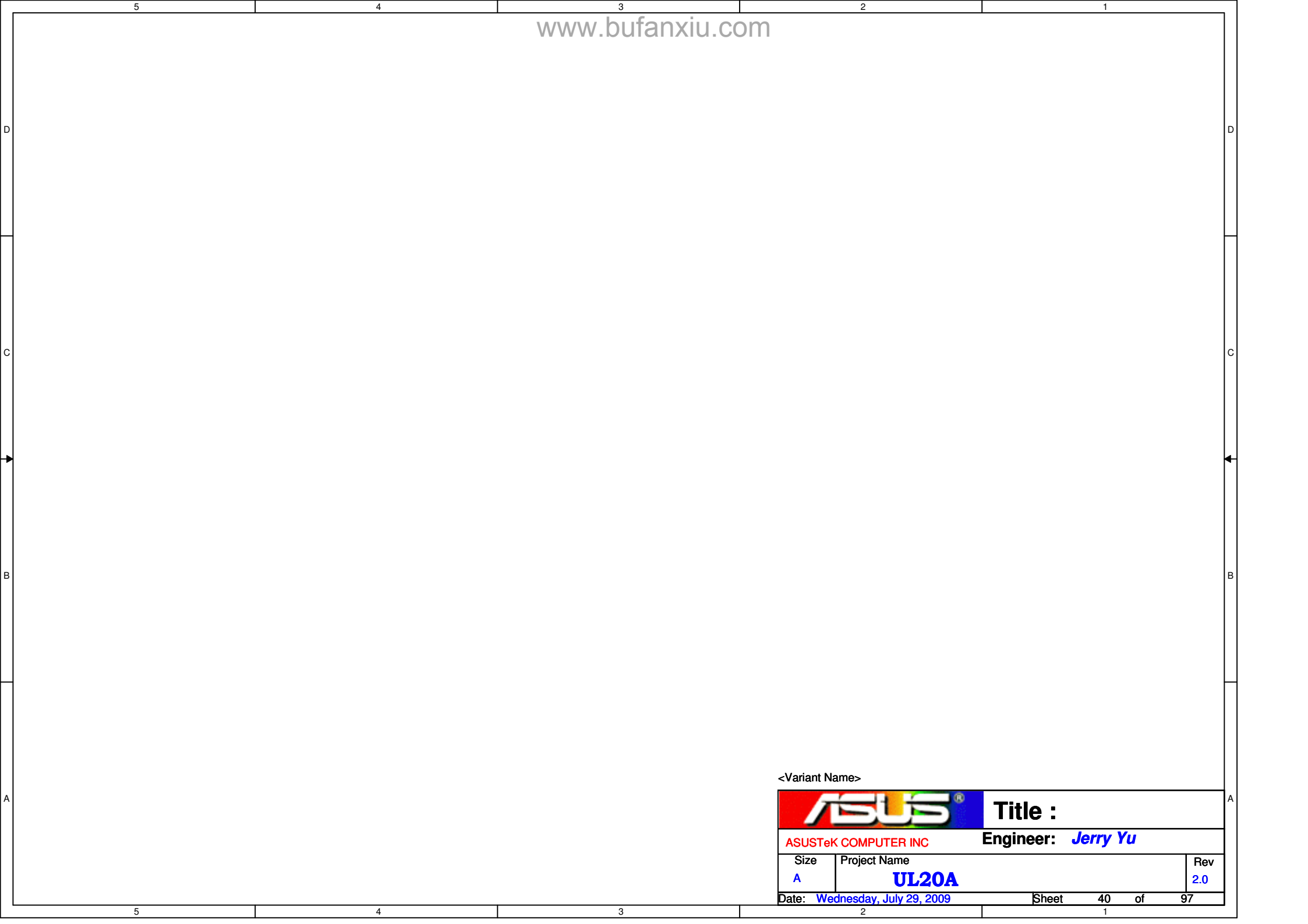
ASUS		Title : AUD MIC CONN	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size Custom	Project Name UL20A	Rev 2.0	
Date: Monday, August 03, 2009	Sheet 37	of 97	






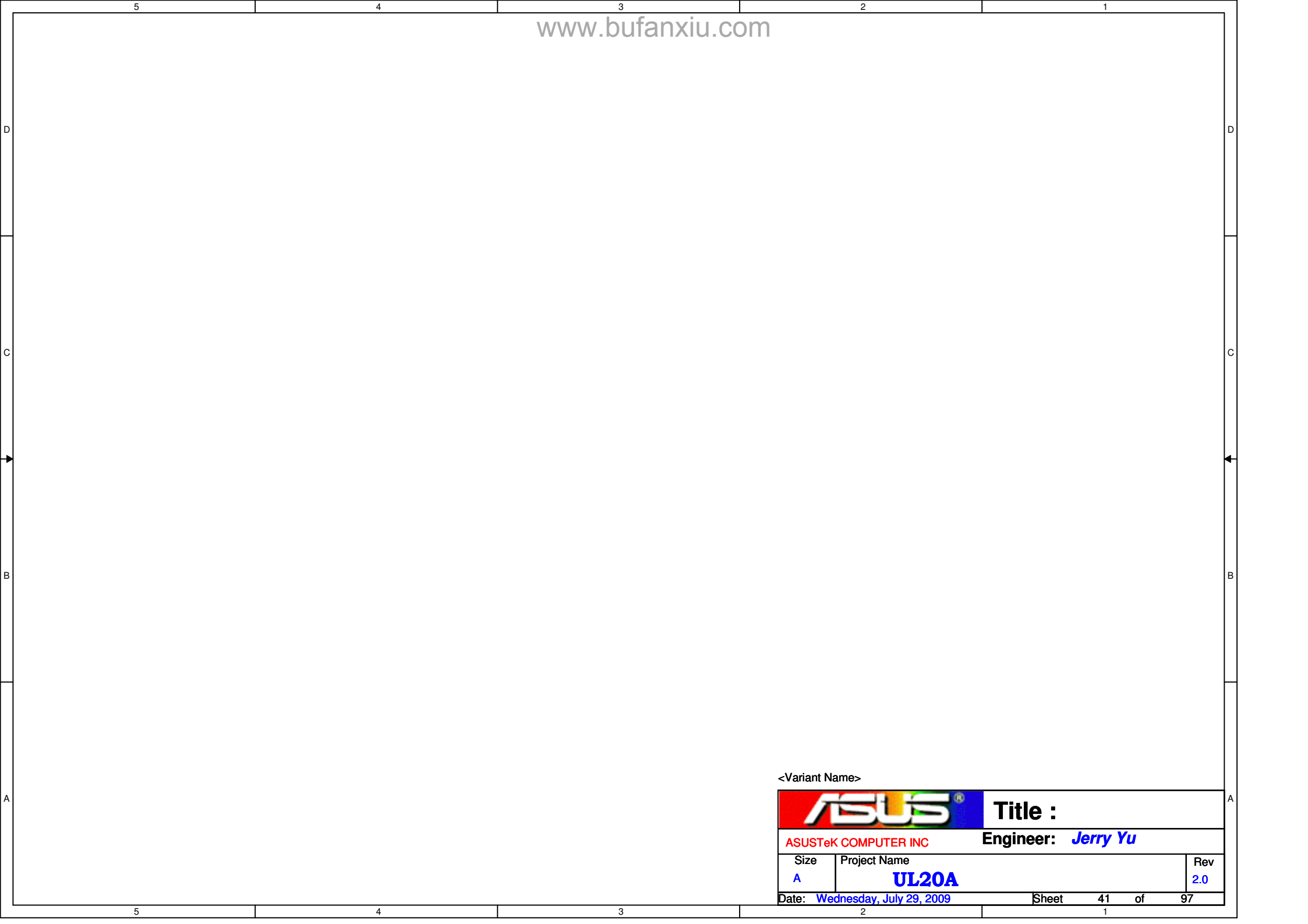
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 39 of 97




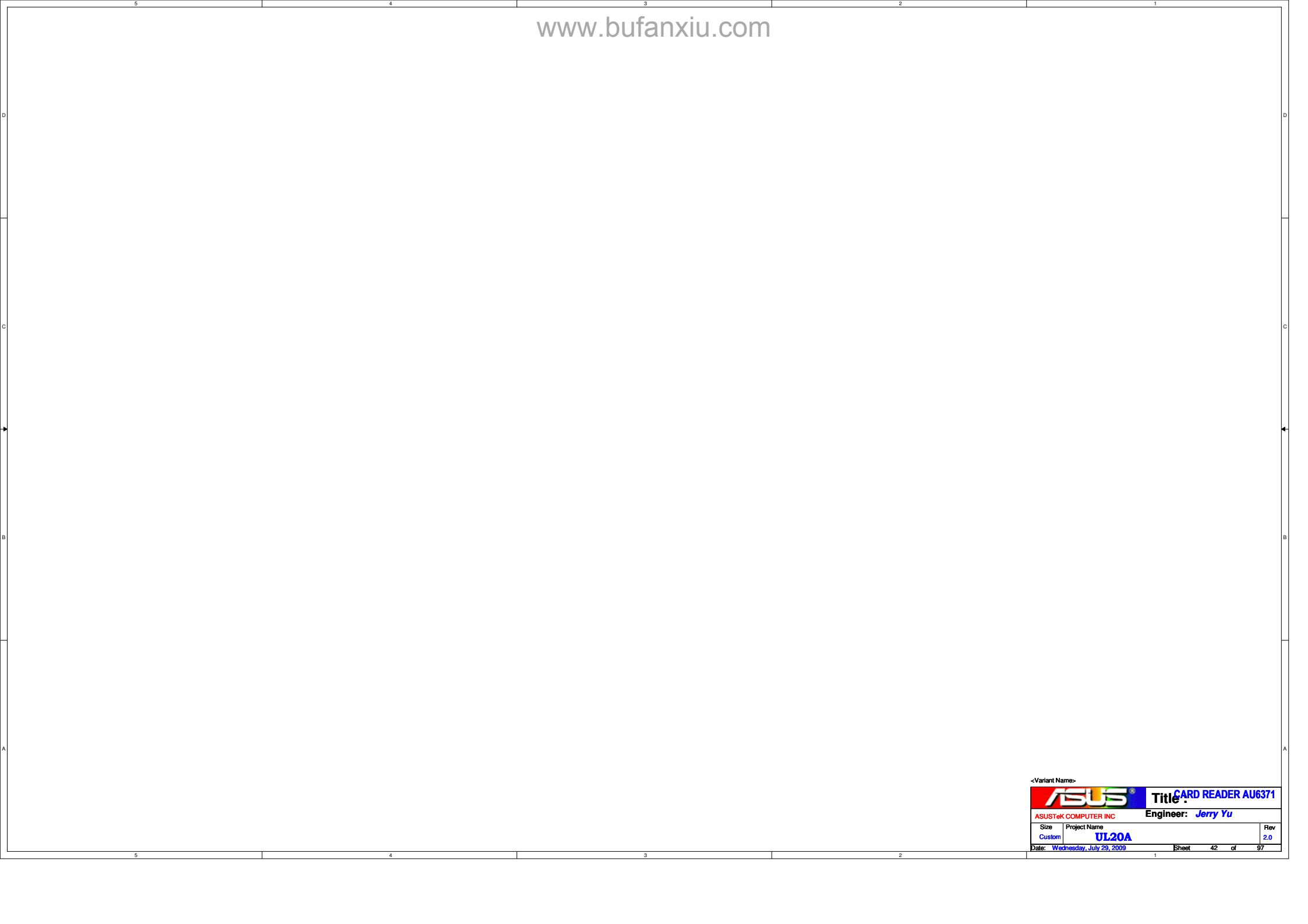
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 40 of 97




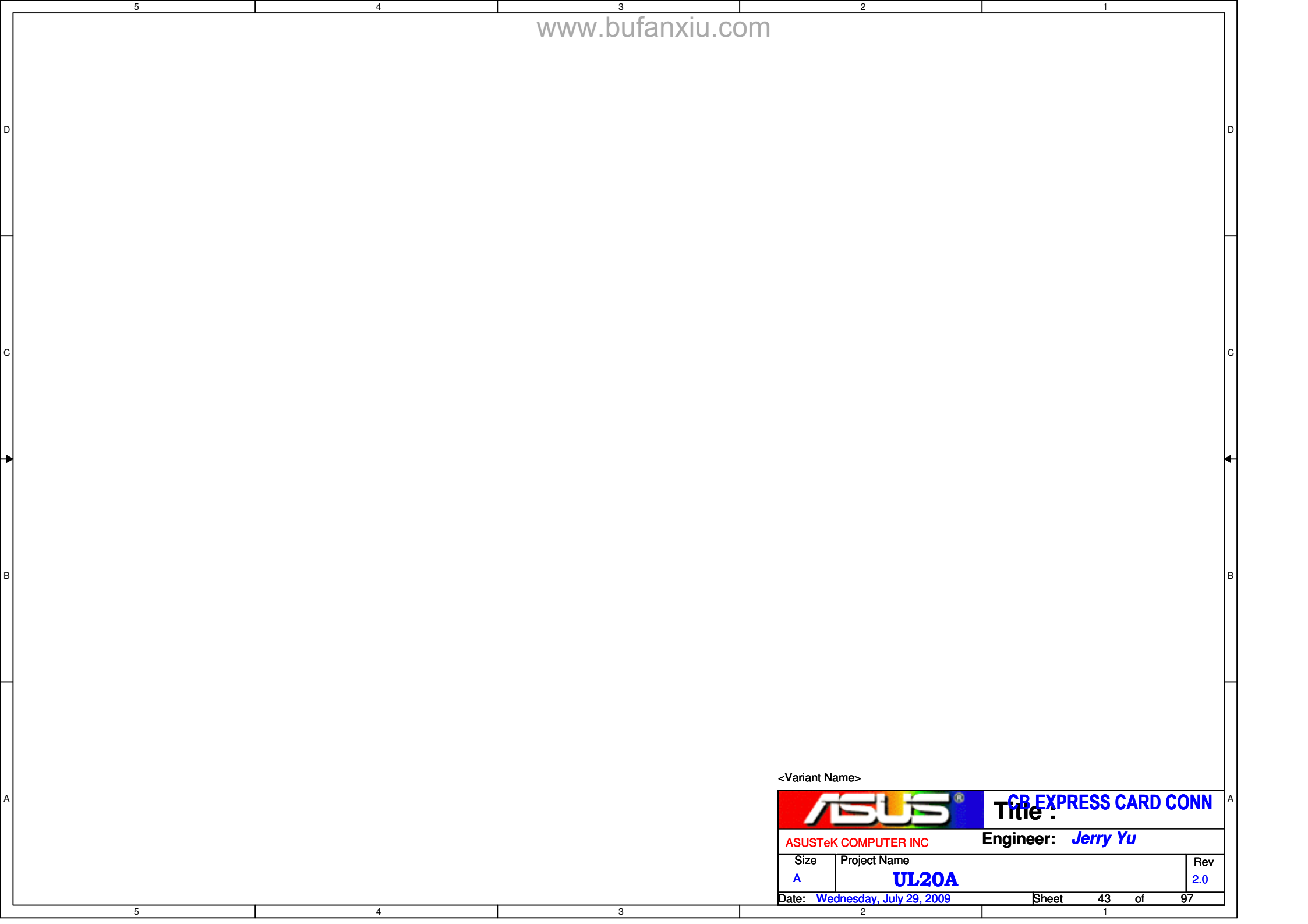
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 41 of 97




<Variant Name>

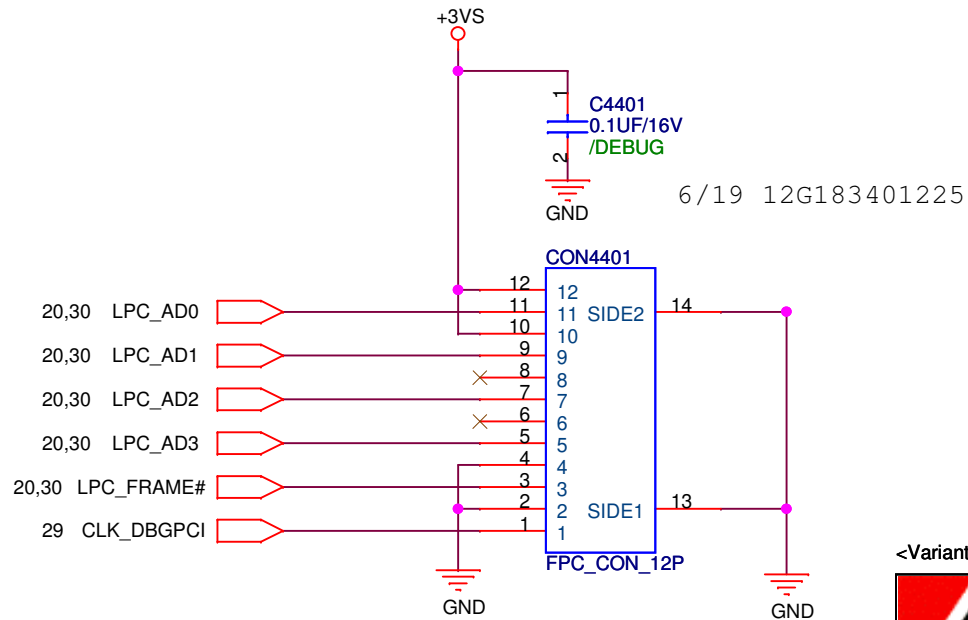
		Title: CARD READER AU6371	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Wednesday, July 29, 2009		Sheet	42 of 97




<Variant Name>

		Title : CB EXPRESS CARD CONN
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 43 of 97


LPC DEBUG PORT



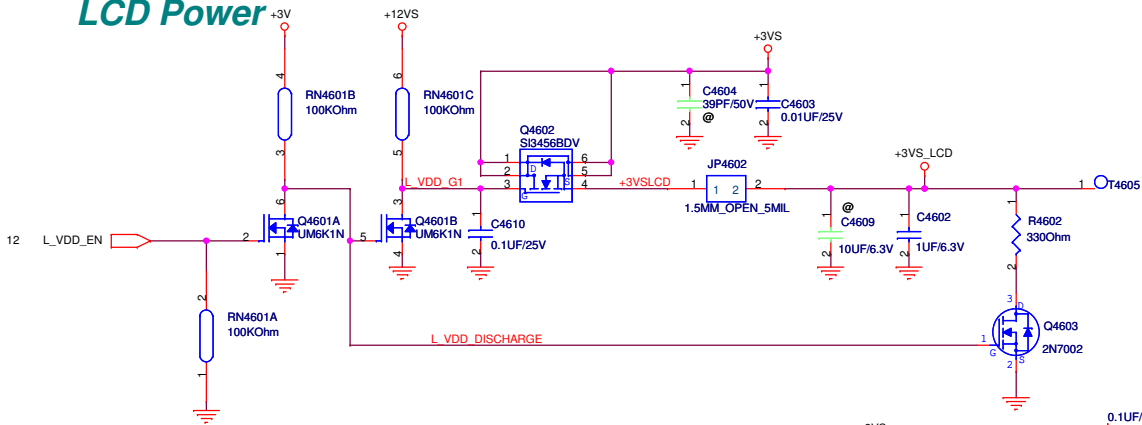
<Variant Name>

		Title :BUG DEBUG PORT
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size A	Project Name UL20A	Rev 2.0
Date: Monday, August 03, 2009		Sheet 44 of 97

<Variant Name>

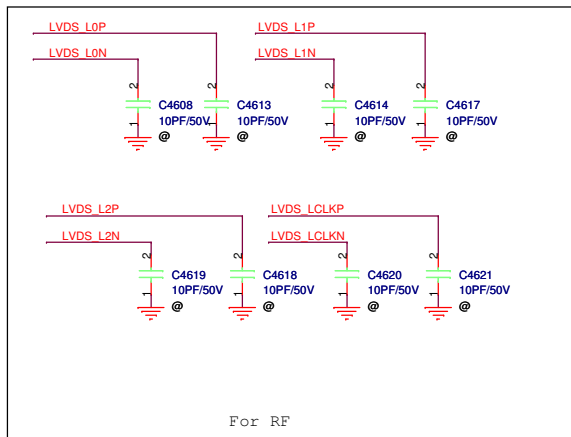
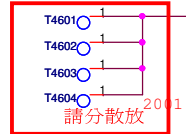
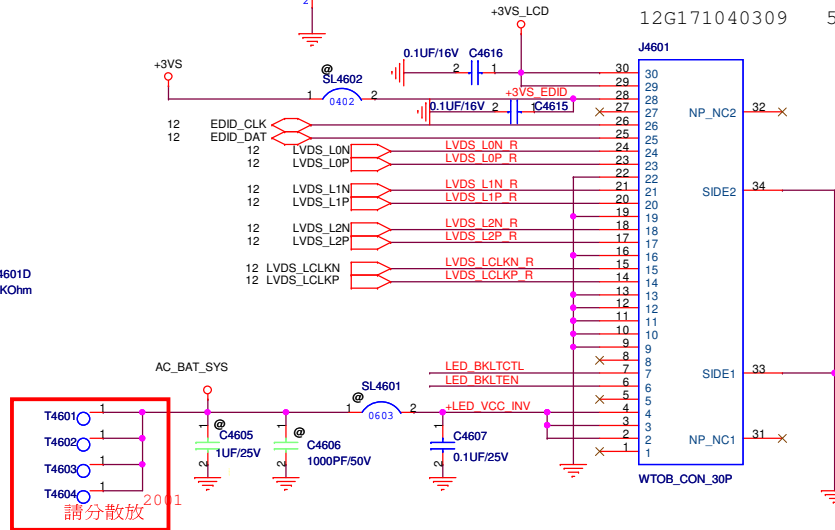
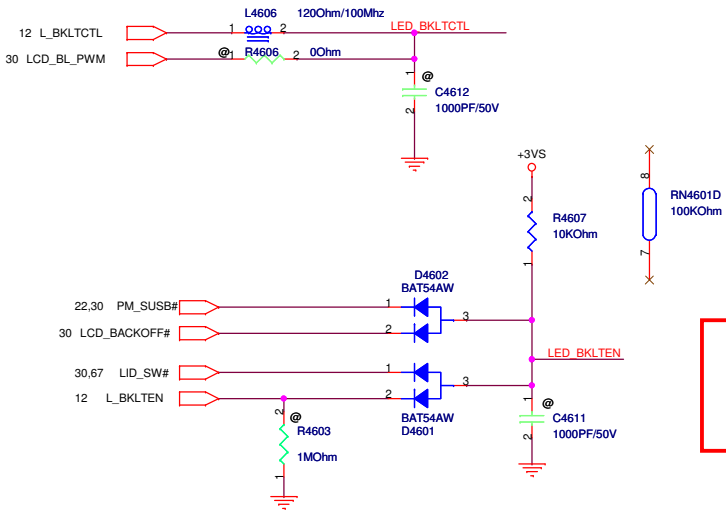
		Title : HDMI CONN
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size C	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 45 of 97

LCD Power



LVDS CONN

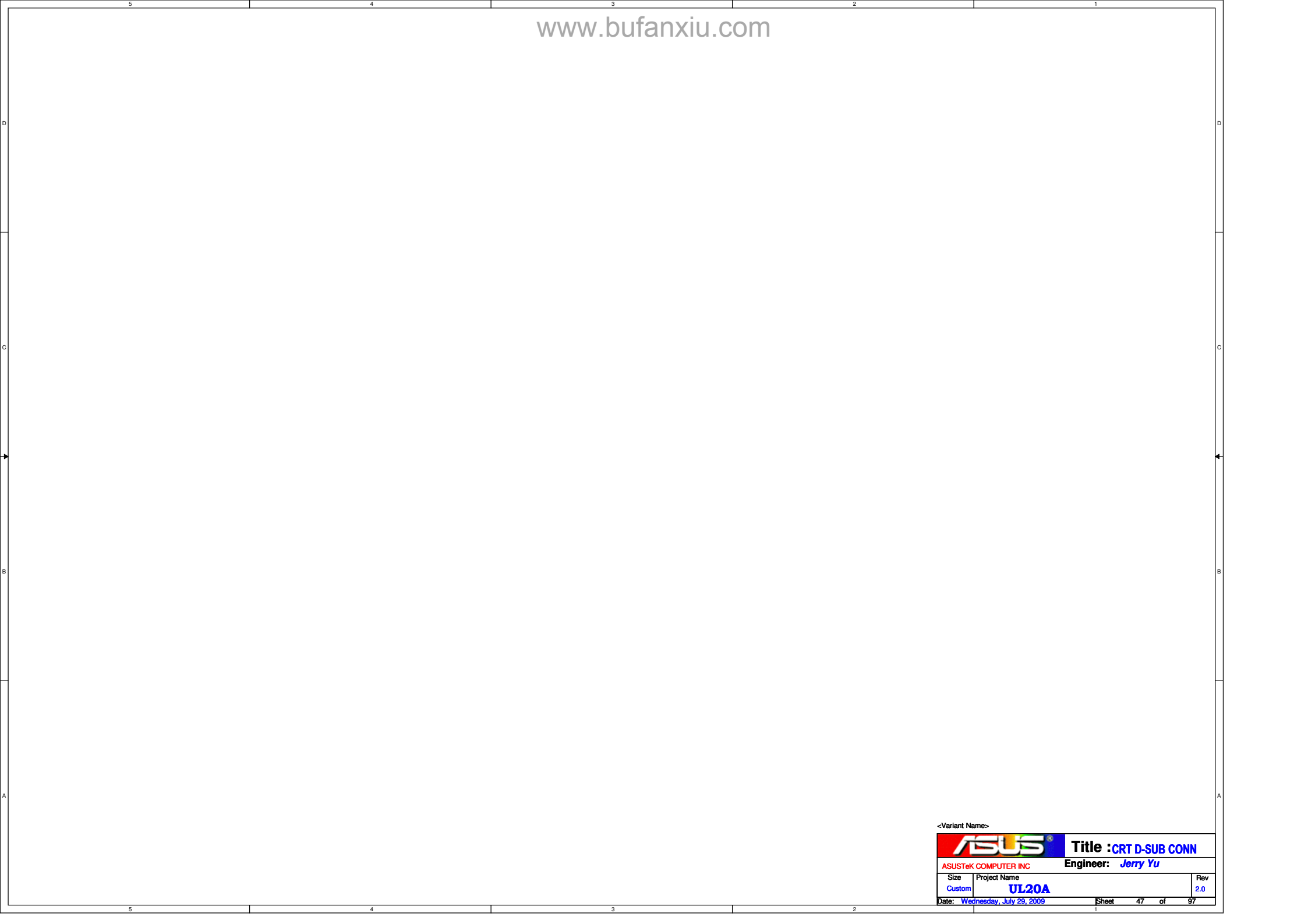
12G171040309 5/19




<Variant Name>

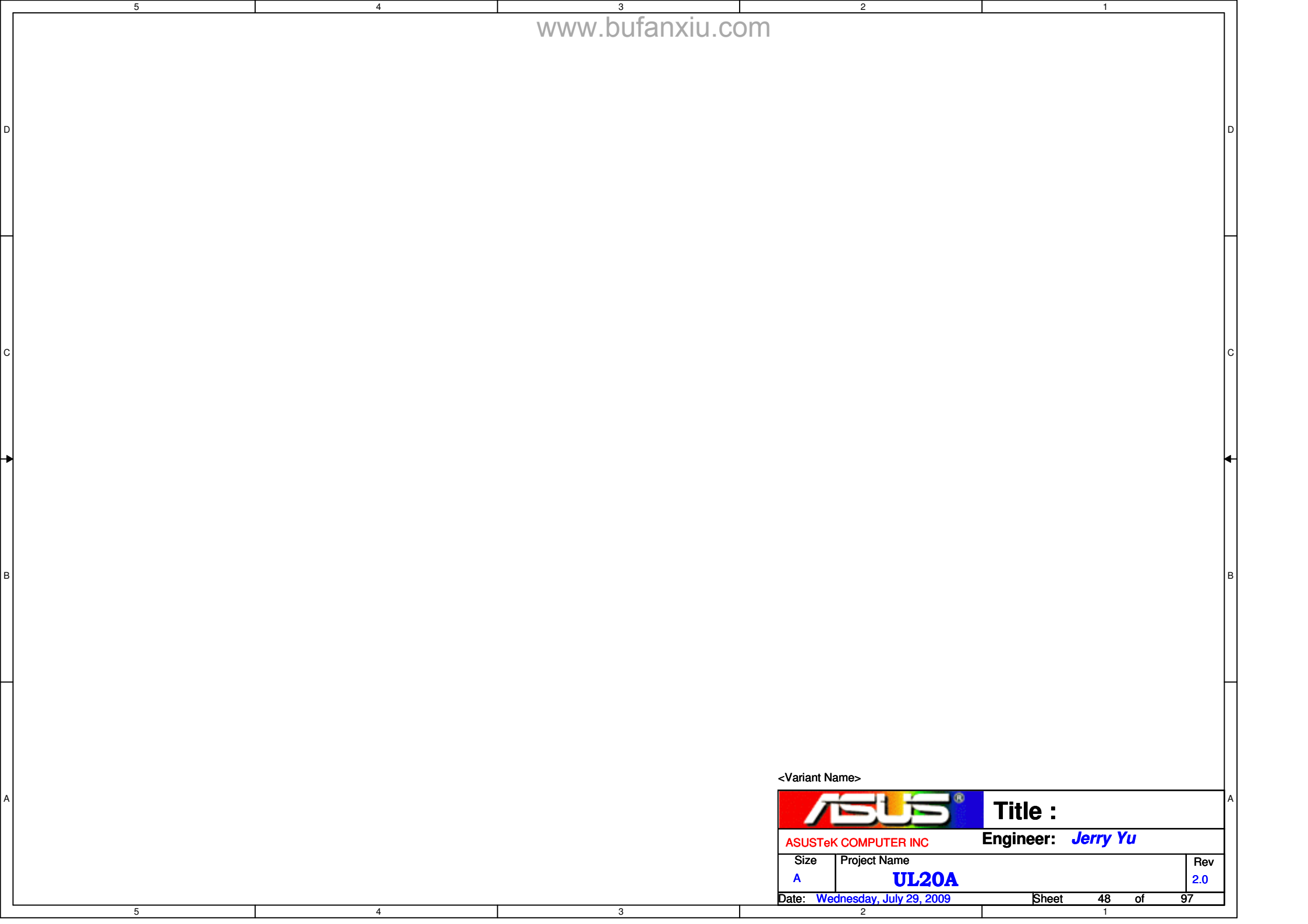
ASUS		Title : LVDS CONN	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Monday, August 03, 2009	Sheet	46	of 97

FOR REF




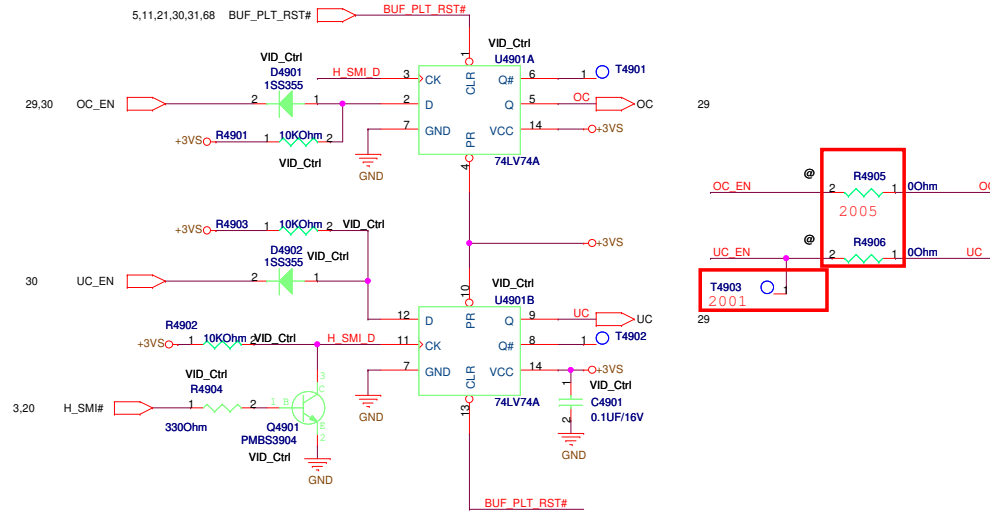
<Variant Name>

		Title : CRT D-SUB CONN
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size Custom	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>	Sheet 47 of 97	



<Variant Name>




		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 48 of 97

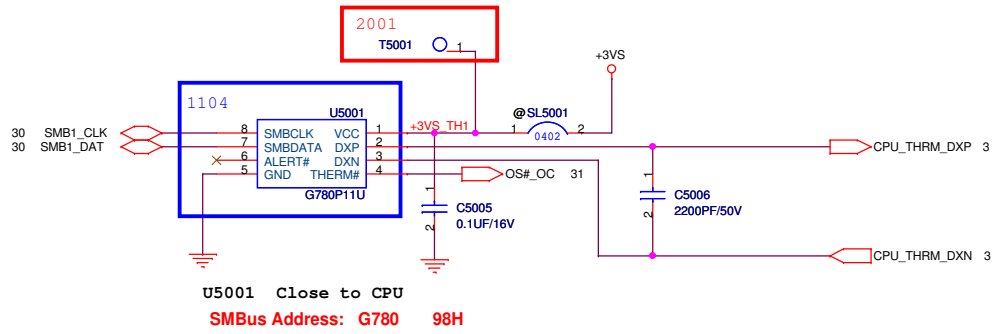


<Variant Name>

ASUS		Title : CRT D-SUB CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Monday, August 03, 2009	Sheet	49	of 97

Thermal Seneor

- +3VS  +3VS 3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,51,56,57,68,69,80,91,92
- +V CORE  +V CORE 4,5,69,80
- +5VS  +5VS 23,36,38,51,56,57,68,80,84,91



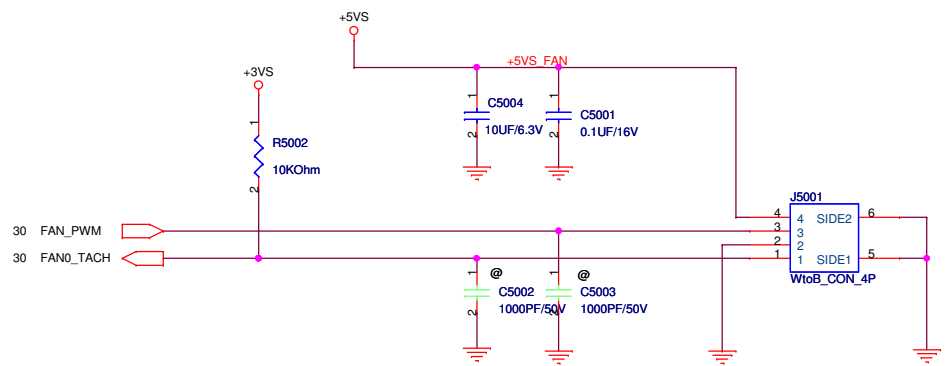
Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

```

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS
    
```

Avoid FSB,Power

FAN CONN

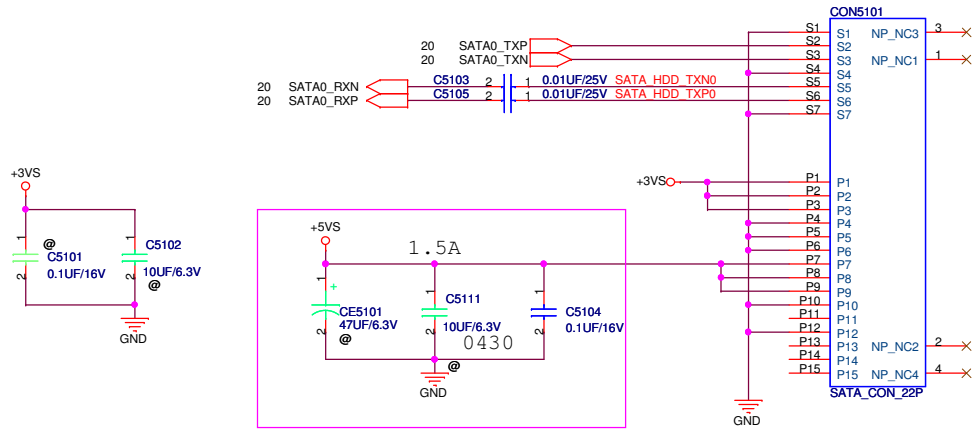


<Variant Name> **FAN THERMAL SENSOR FAN CONN**

ASUS Title : **ASUSTeK COMPUTER INC** Engineer: **Jerry Yu**

Size	Project Name	Rev
Custom	UL20A	2.0
Date: Monday, August 03, 2009	Sheet 50 of 97	

SATA HDD

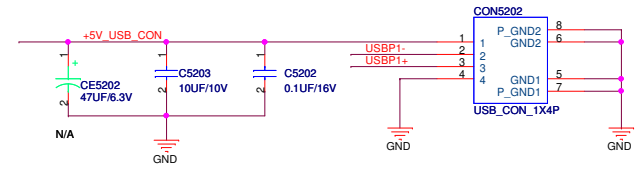
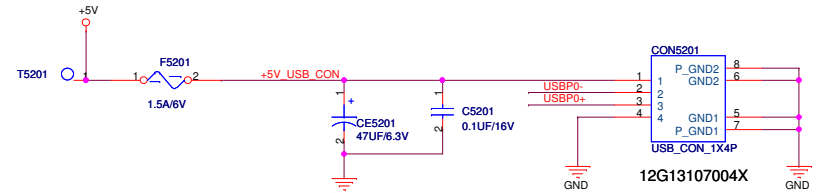
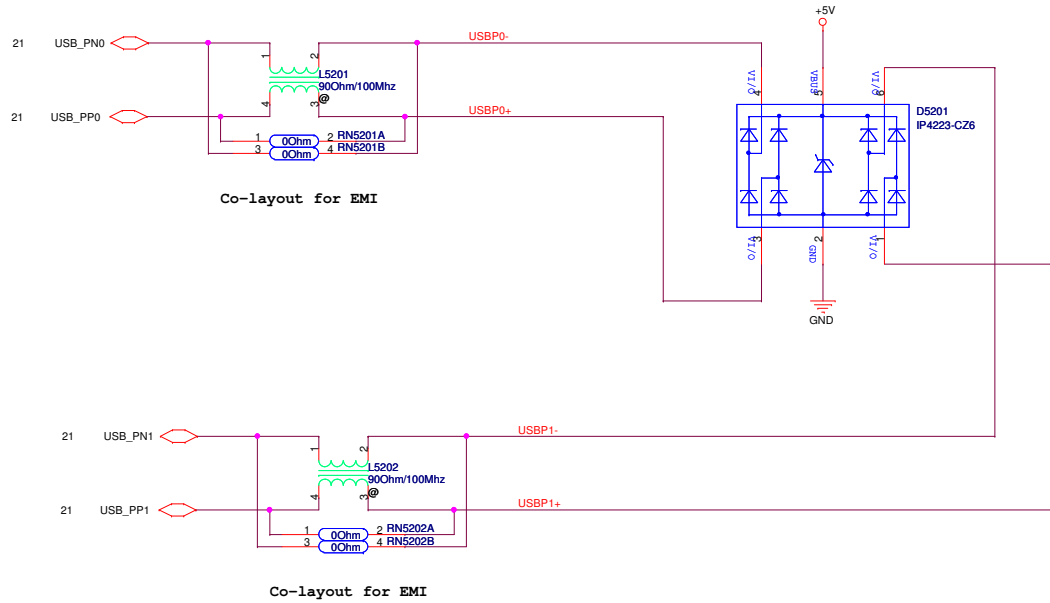


<Variant Name>

ASUS		Title: XDD SATA HDD CONN	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size Custom	Project Name UL20A	Rev 2.0	
Date: Monday, August 03, 2009		Sheet	51 of 97

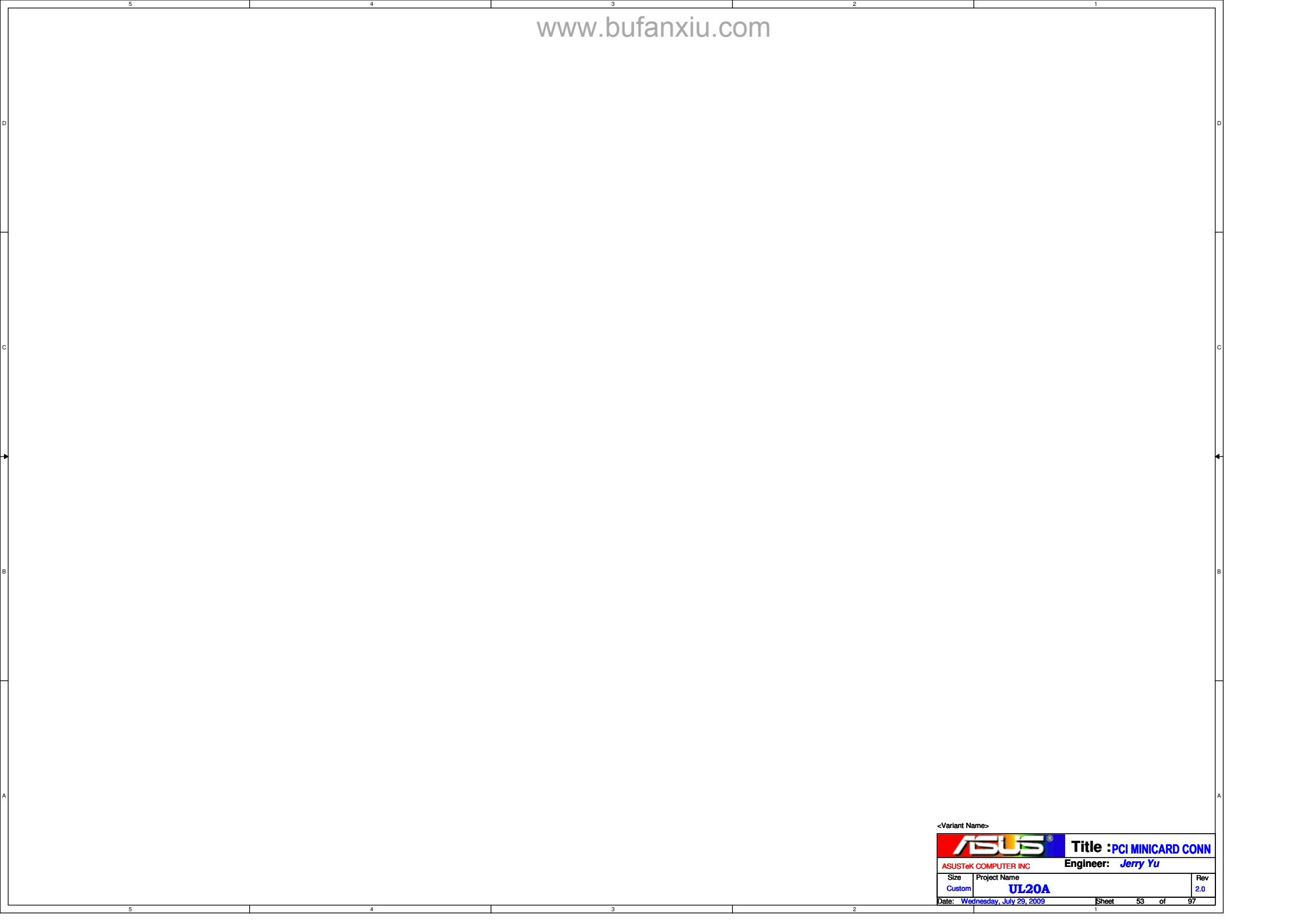
USB CONN *2

USB : MB




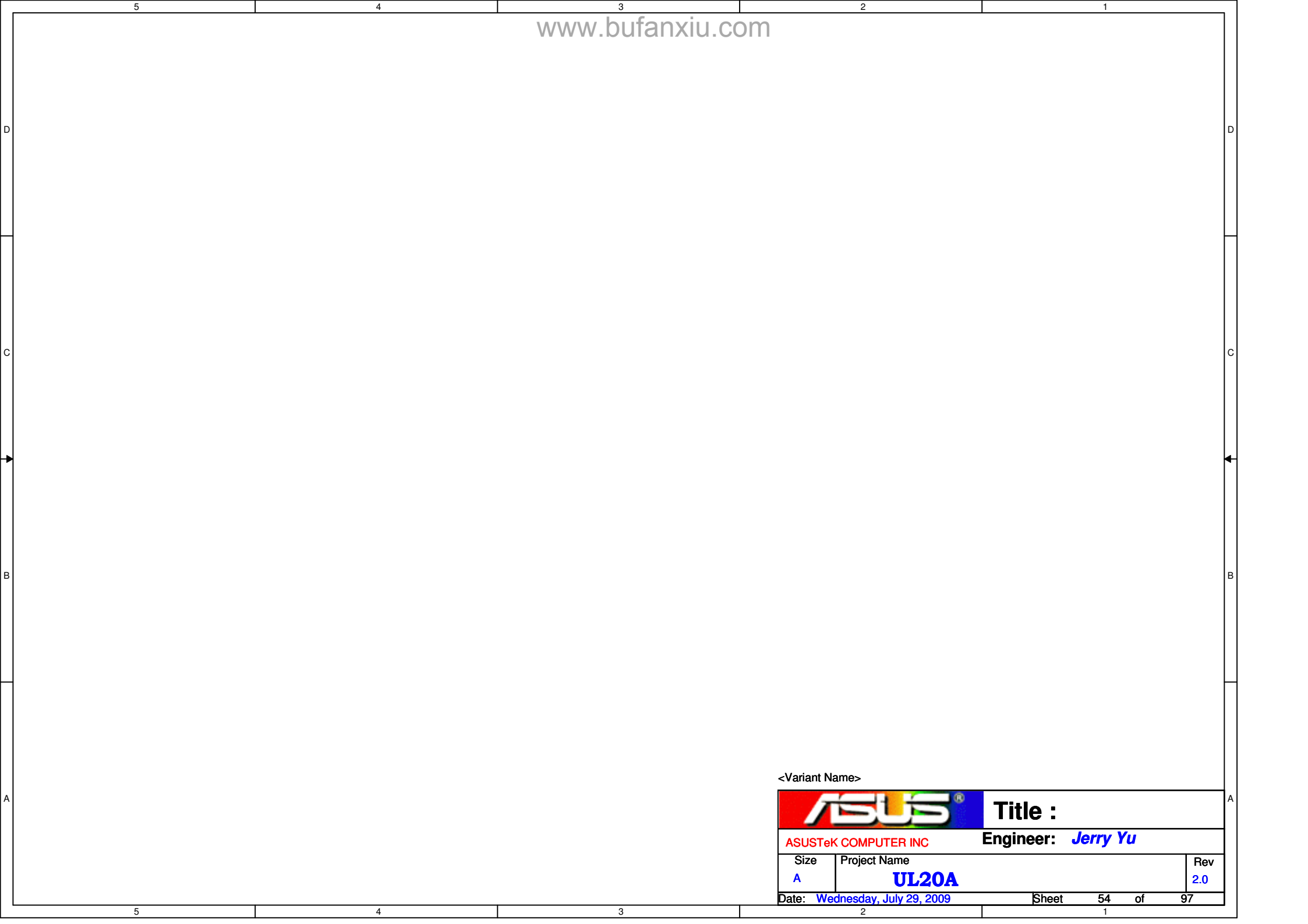
<Variant Name>

ASUS		Title :USB 2.0 CONN*2	
ASUSTek COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Monday, August 03, 2009	Sheet	52	of 97




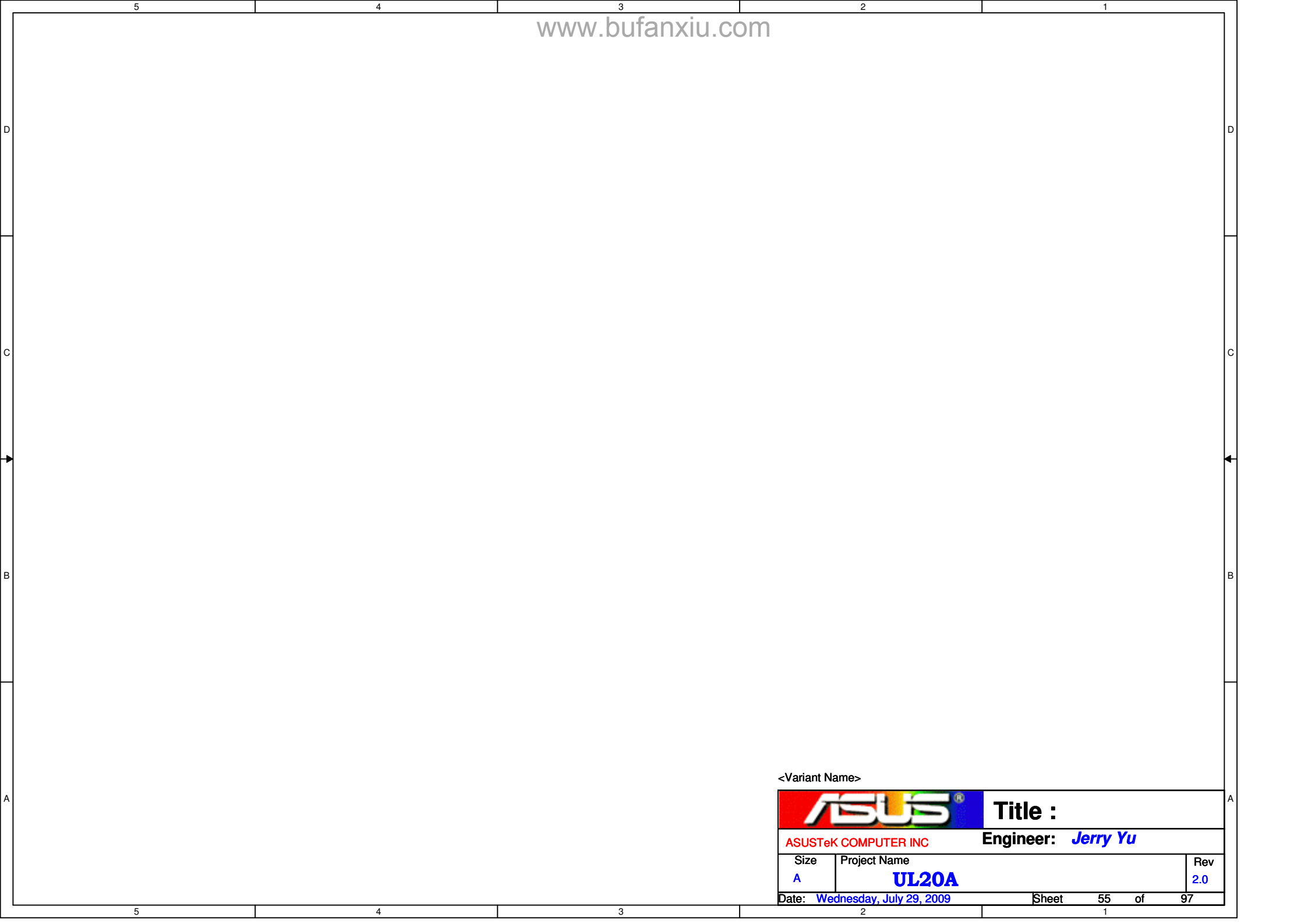
<Variant Name>

		Title :PCI MINICARD CONN
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size Custom	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>	Sheet 53 of	97




<Variant Name>

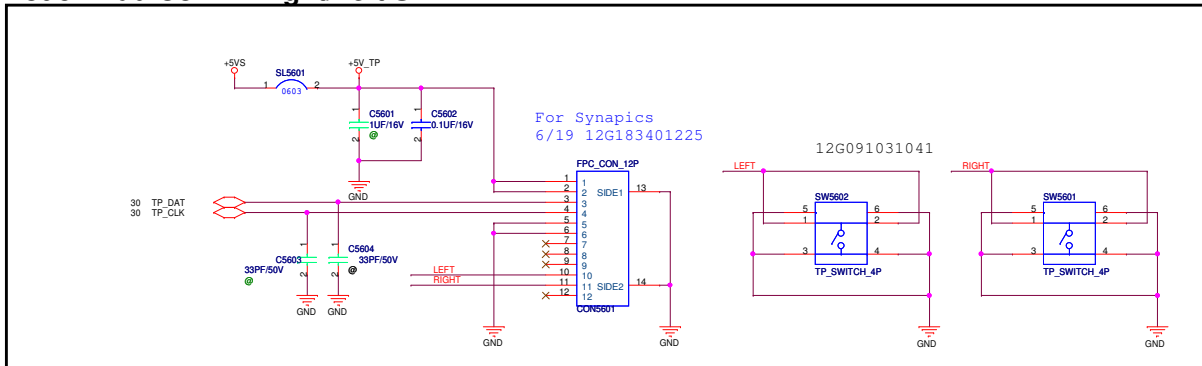
		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 54 of 97



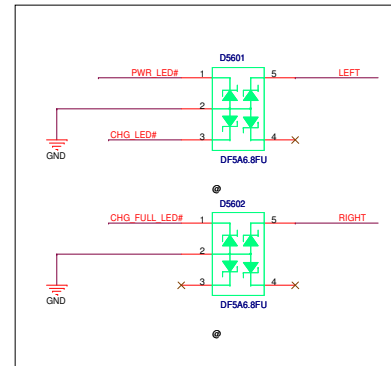
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 55 of 97

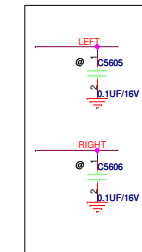
Touch-Pad Conn. Right/Left SW.



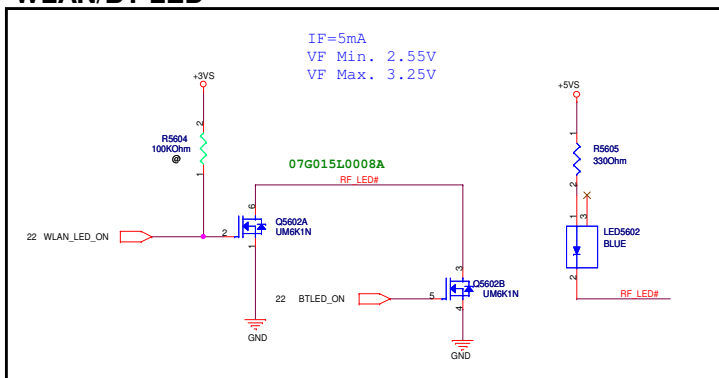
6/22 for ESD



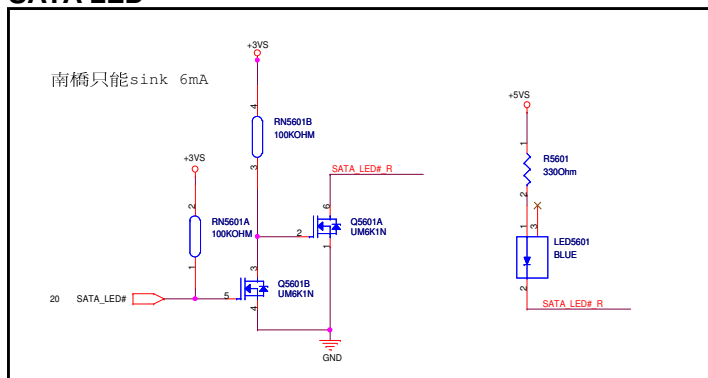
6/30 EMI near BTN



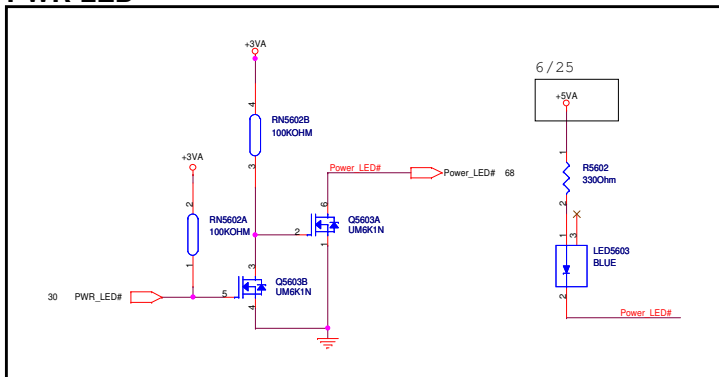
WLAN/BT LED



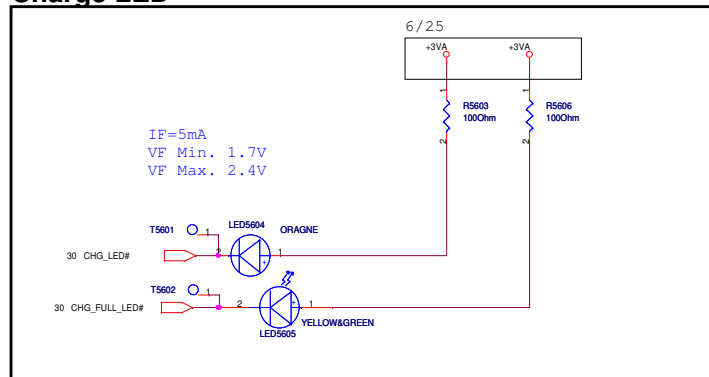
SATA LED



PWR LED

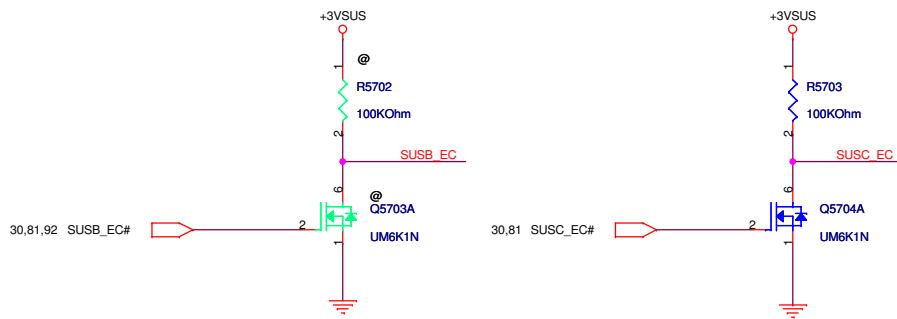
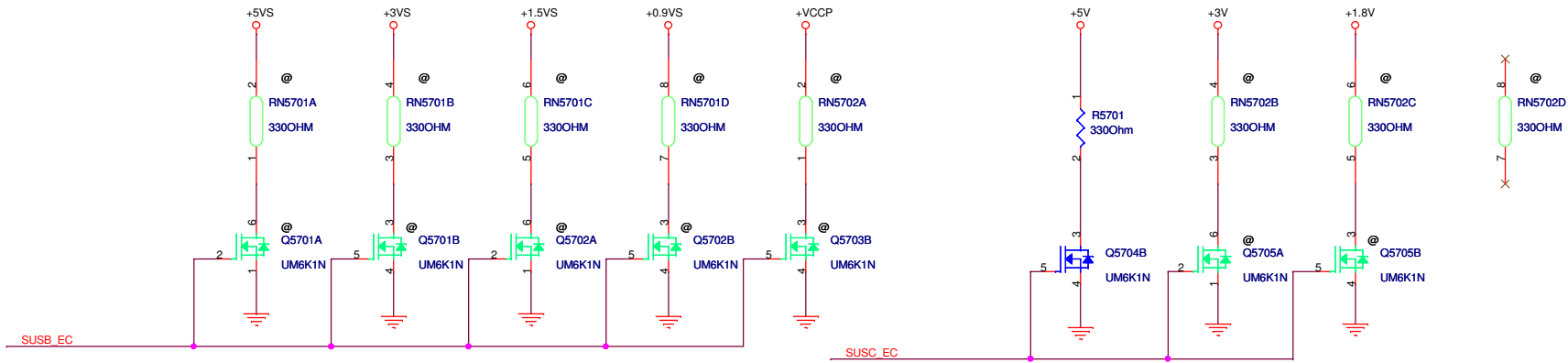


Charge LED



Discharge Circuit

+5VS		+5VS	23,36,38,50,51,56,68,80,84,91
+3VS		+3VS	3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,68,69,80,91,92
+1.5VS		+1.5VS	4,15,20,23,36,68,69,84
+VCCP		+VCCP	3,4,5,10,11,12,14,15,20,23,29,69,82
+5V		+5V	52,67,68,91
+3V		+3V	46,68,91
+1.8V		+1.8V	7,8,9,11,14,15,83,84,91
+0.9VS		+0.9VS	9,83
+3VSUS		+3VSUS	20,21,22,23,30,68,69,80,81,91,92




<Variant Name>

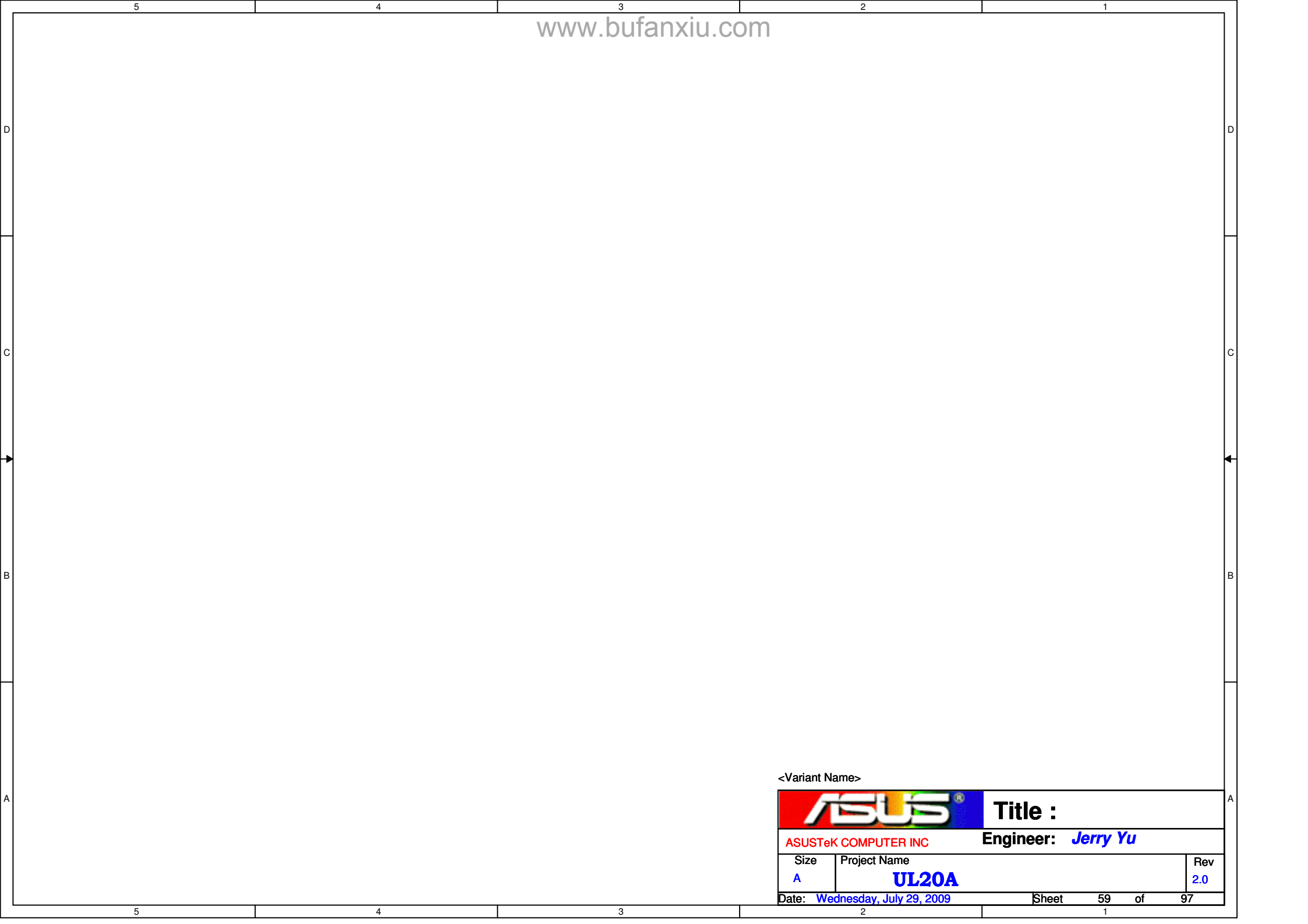
DSG-DISCHARGE CIRCUIT

		Title :
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size Custom	Project Name UL20A	Rev 2.0
Date: Monday, August 03, 2009	Sheet 57 of 97	


5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

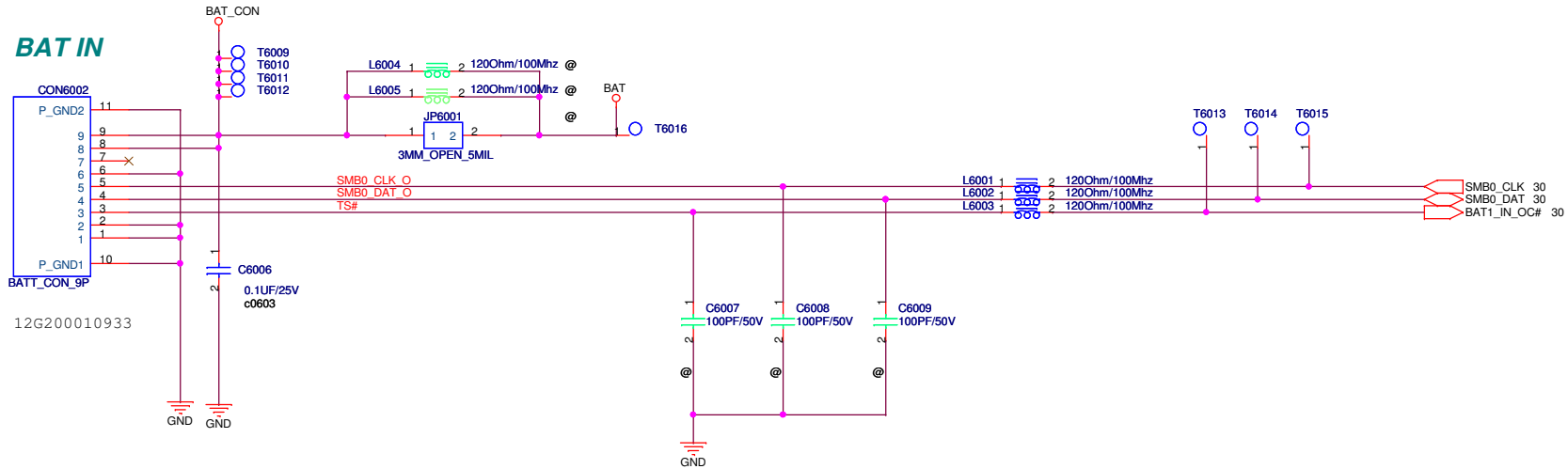
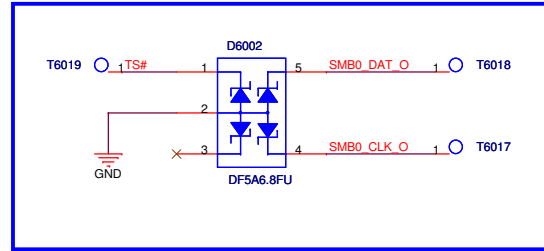
		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	58 of 97



<Variant Name>

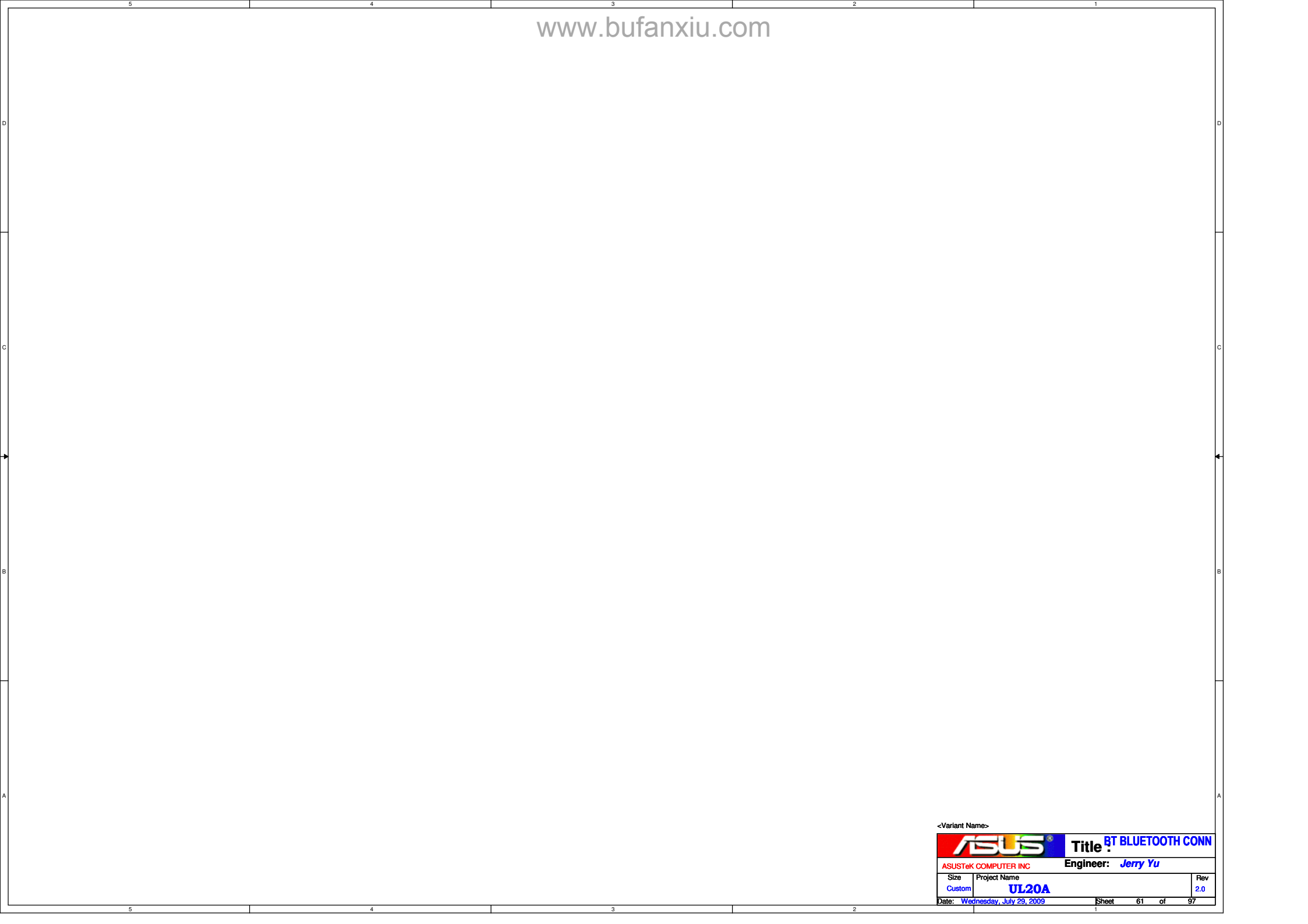
		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 59 of 97

6/22 change part




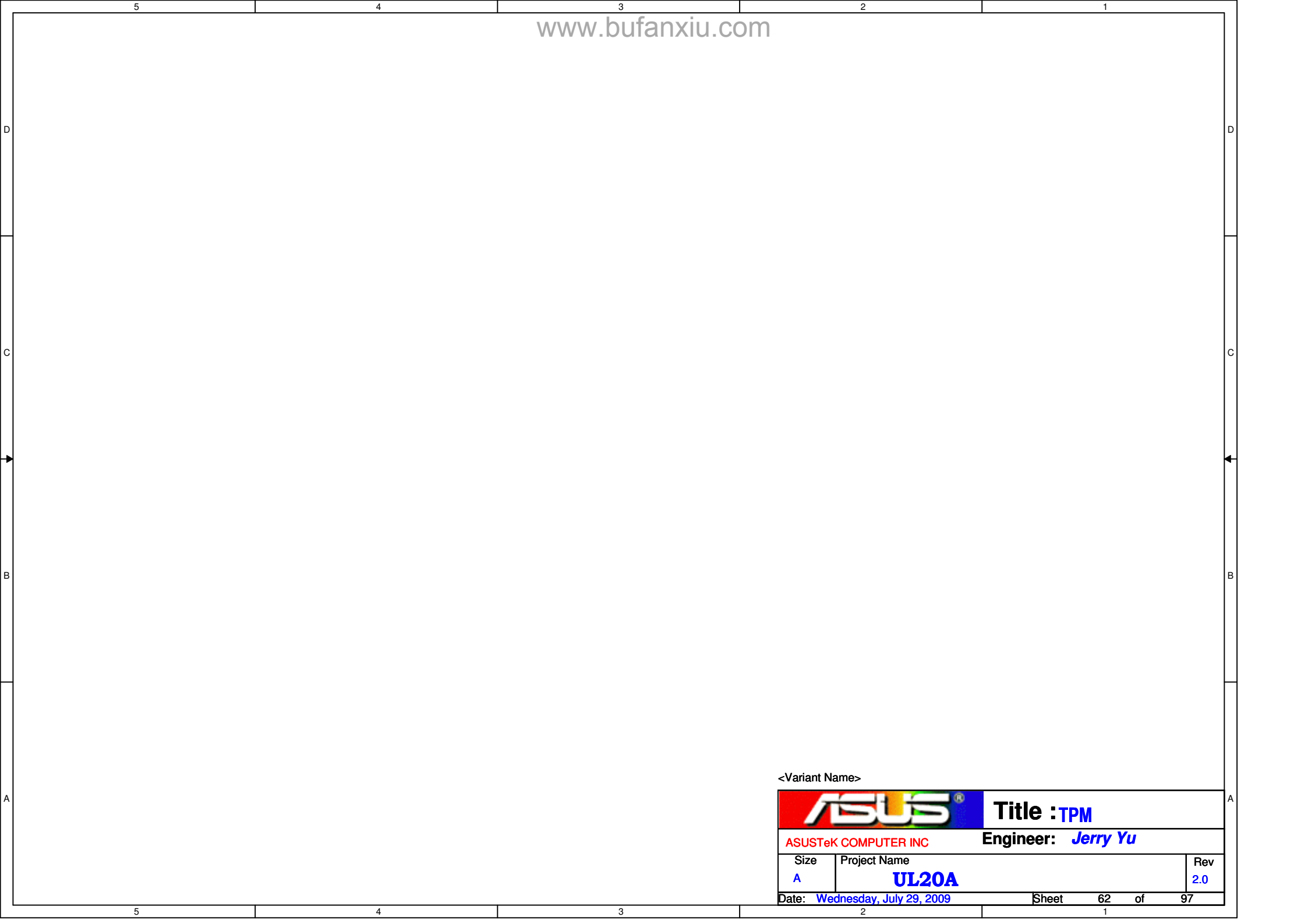
<Variant Name>

ASUS		Title :DC DC&BATT CONN	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name	Rev	
Custom	UL20A	2.0	
Date: Monday, August 03, 2009	Sheet	60	of 97




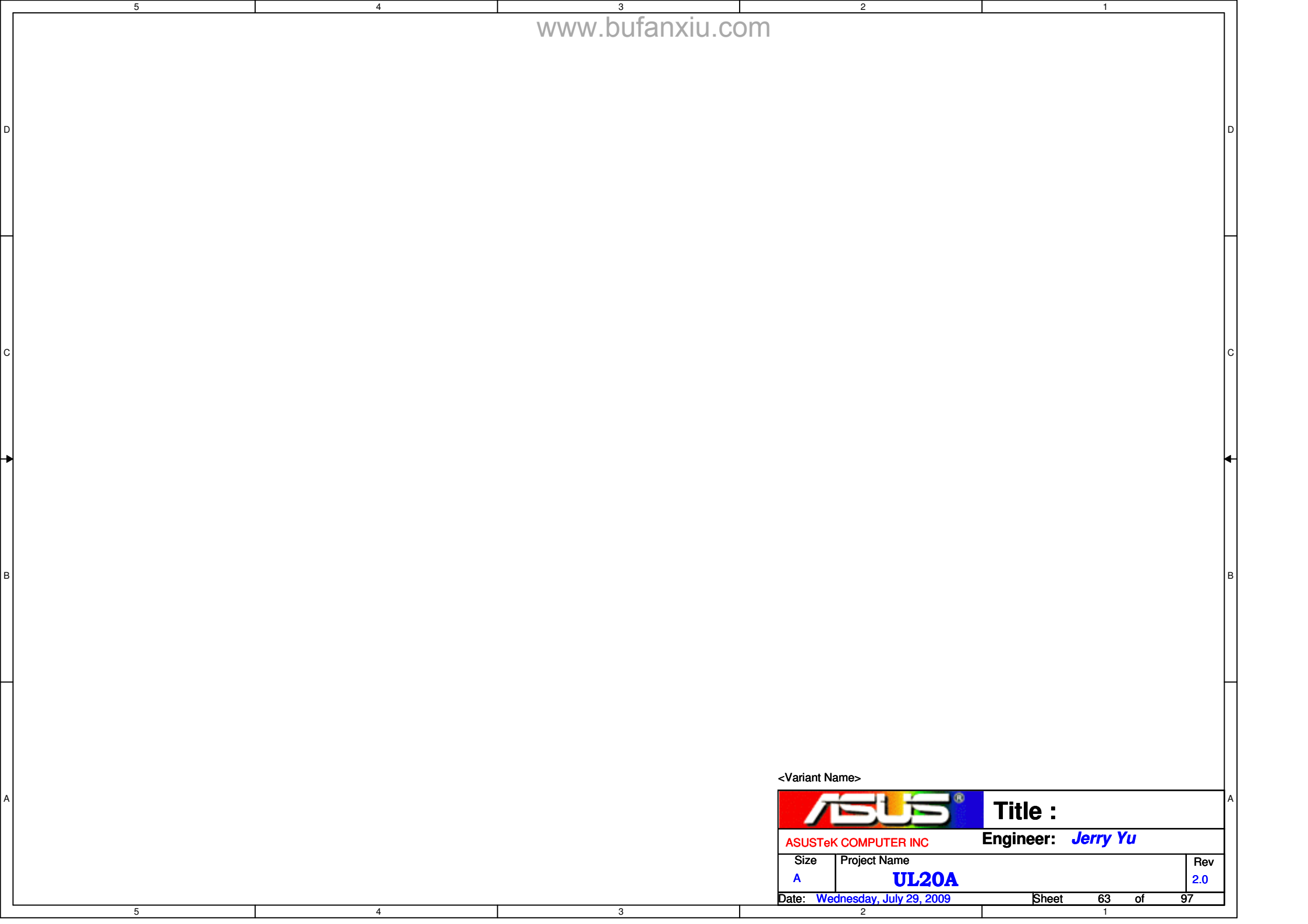
<Variant Name>

		Title: BT BLUETOOTH CONN
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size Custom	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 61 of 97




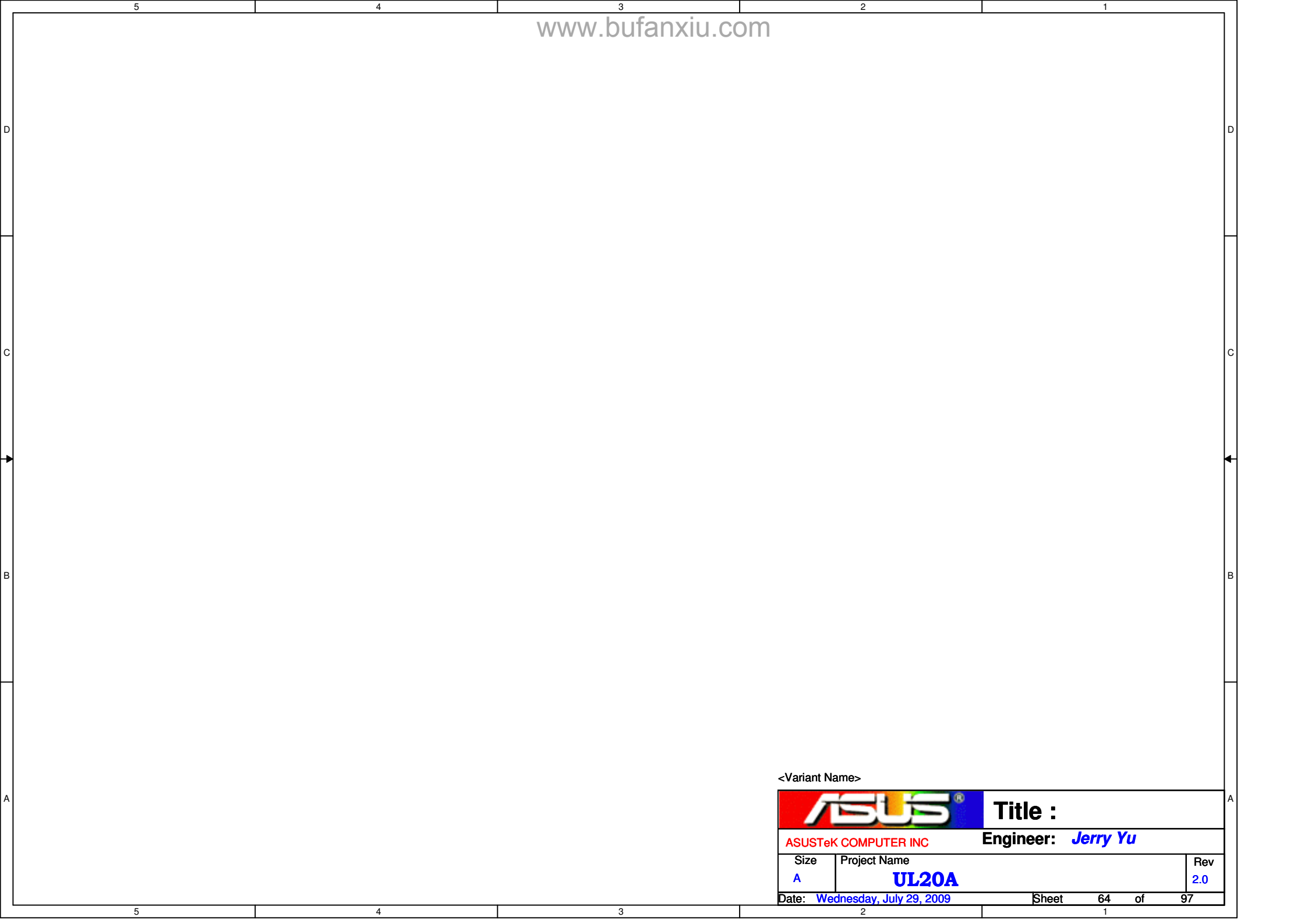
<Variant Name>

		Title :TPM
ASUSTeK COMPUTER INC		Engineer: Jerry Yu
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 62 of 97




<Variant Name>

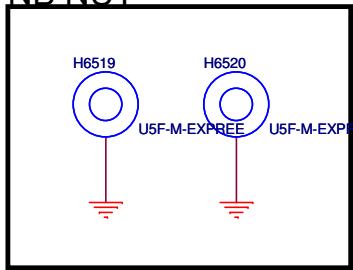
		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 63 of 97



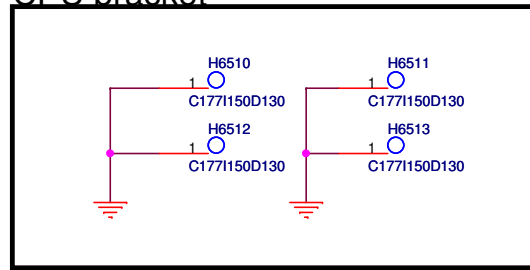
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	64 of 97

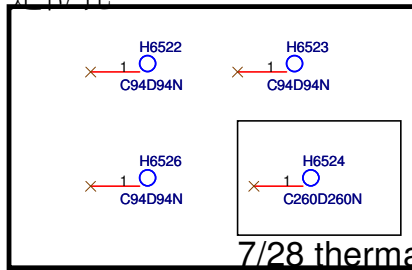
NB NUT



CPU bracket

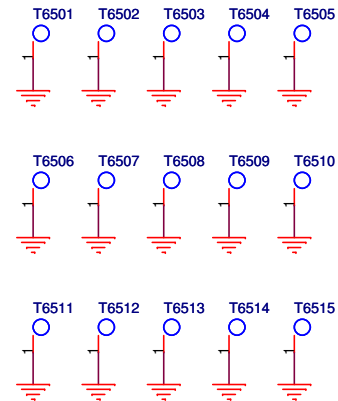
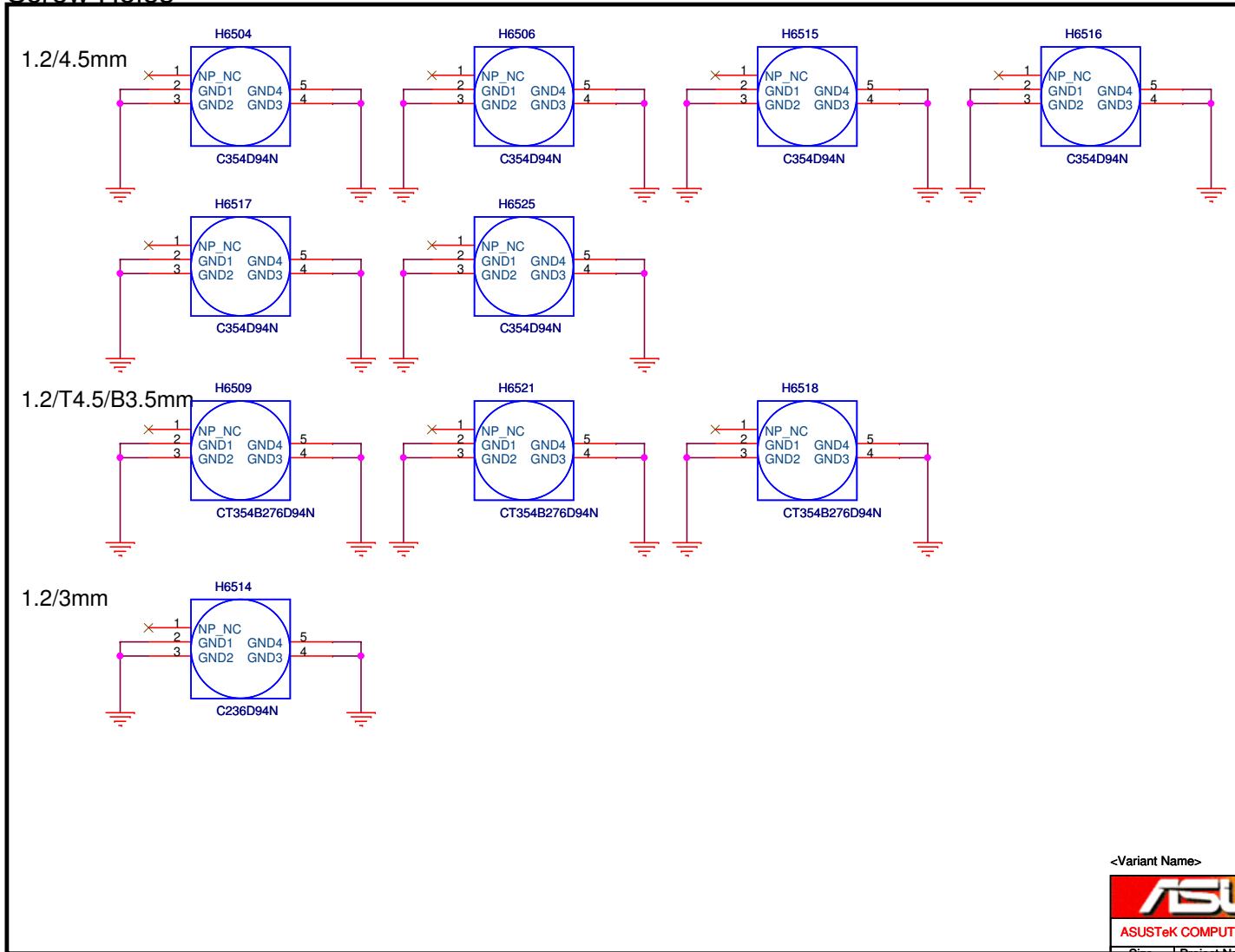


定位孔



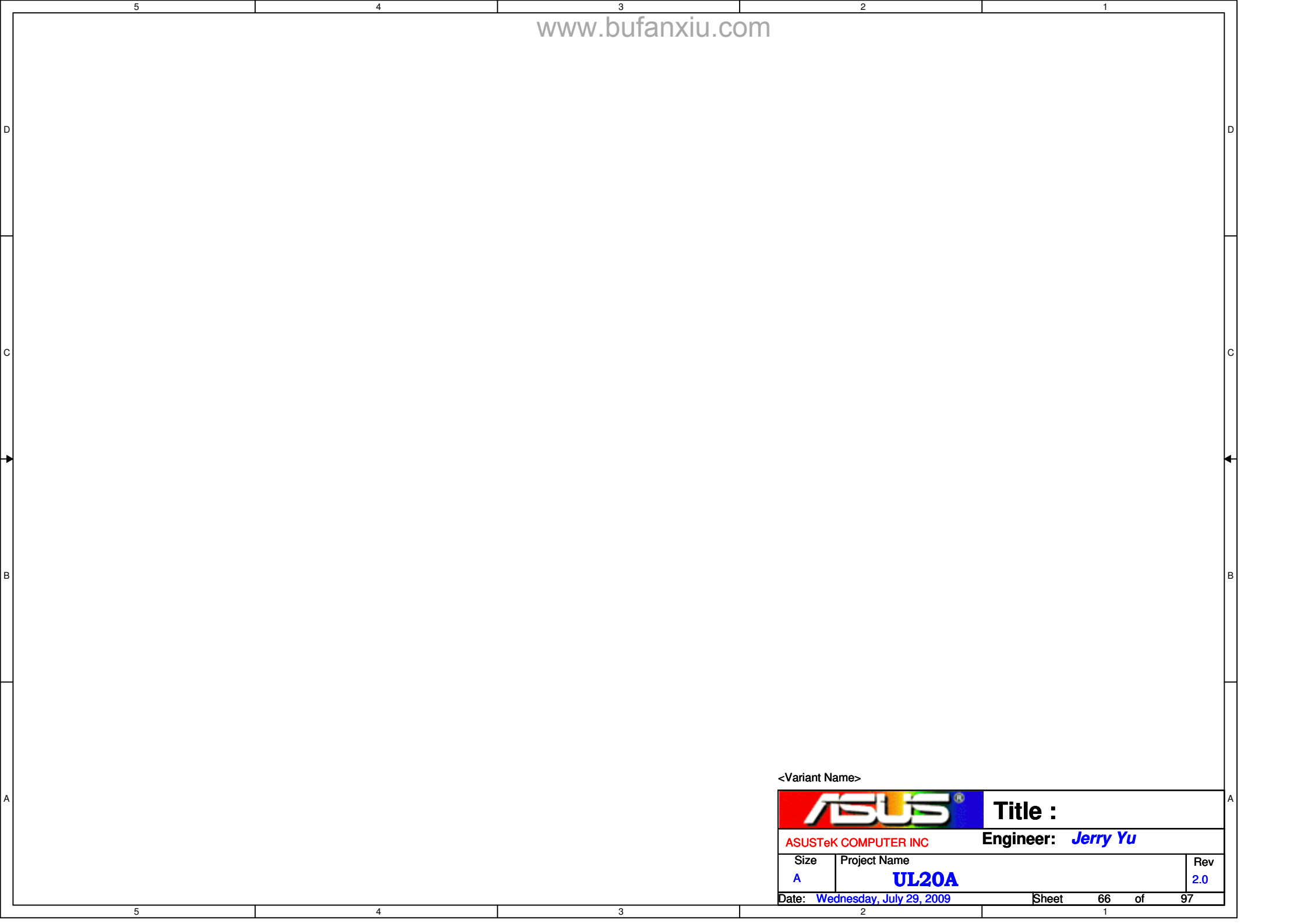
7/28 thermal request

Screw Holes




<Variant Name>

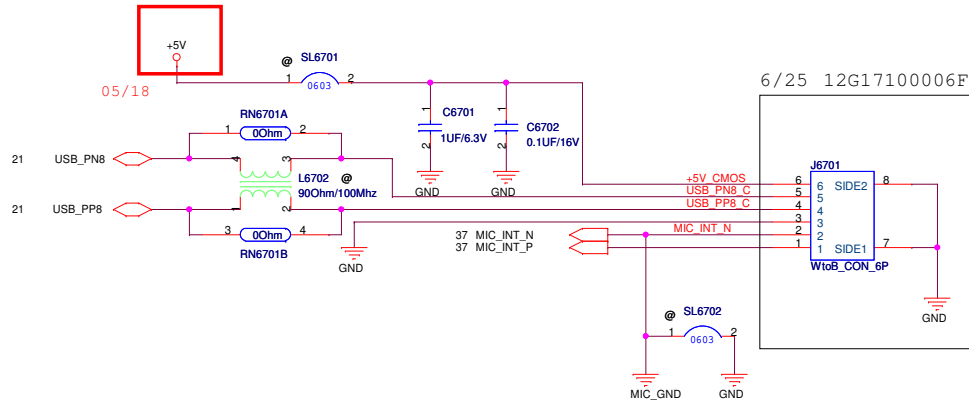
ASUS		ME SCREW HOLE AMT NUT	
ASUSTeK COMPUTER INC		Title :	
Custom		Engineer: Jerry Yu	
Date: Wednesday, July 29, 2009		Rev 2.0	
Project Name: UL20A		Sheet 65 of 97	



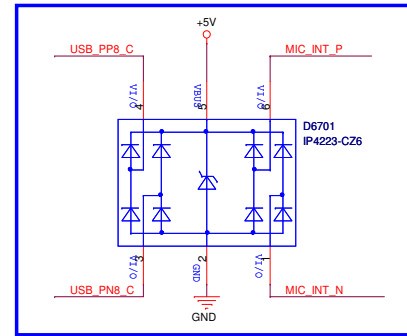
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	66 of 97

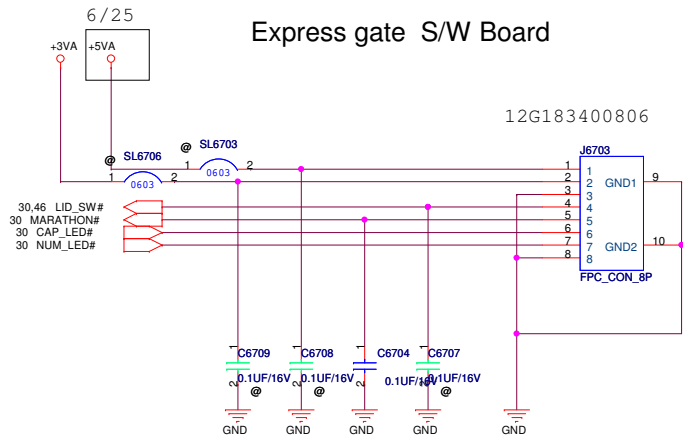
Camera Module & Mic.



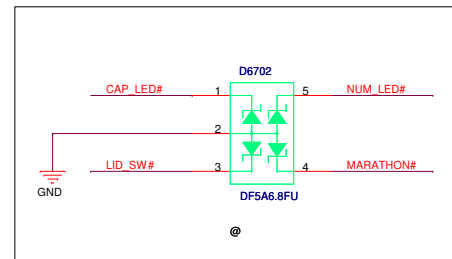
D6701 Close to J6701

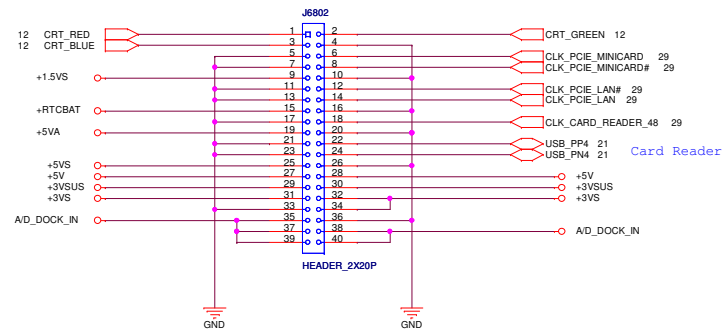
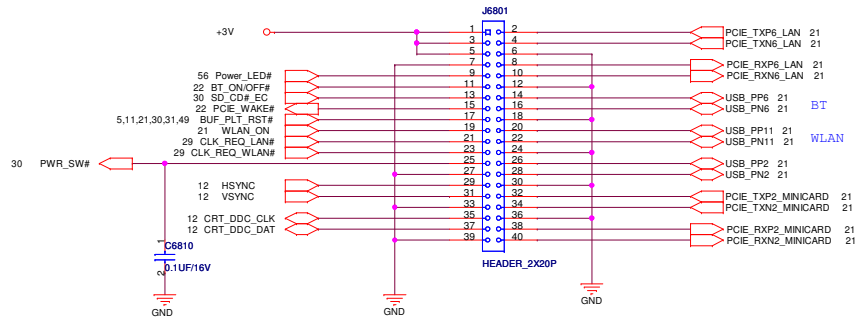


Express gate S/W Board



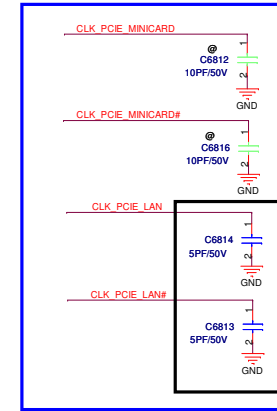
6/22 for ESD



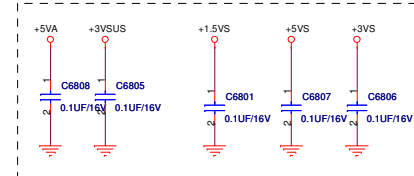


每一根估0.5A, connector spec 1A

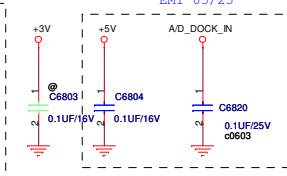
For Clock signal quality



EMI 07/03



EMI 05/25



<Variant Name>

ASUS		Title : B TO B CONN	
ASUSTEK COMPUTER INC		Engineer: Jerry Yu	
Size	Project Name		Rev
Custom	UL20A		2.0
Date: Monday, August 03, 2009		Sheet	68 of 97

SYSTEM

- +VCCP ○ —◇— +VCCP 3,4,5,10,11,12,14,15,20,23,29,57,82
- +VCC_GMCH ○ —◇— +VCC_GMCH 3,4,5,10,11,12,14,15,20,23,29,57,82
- +VGFX_CORE ○ —◇— +VGFX_CORE 3,4,5,10,11,12,14,15,20,23,29,57,82

- +3VS ○ —◇— +3VS 3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,57,68,80,91,92
- +VCORE ○ —◇— +VCORE 4,5,80
- +1.5VS ○ —◇— +1.5VS 4,15,20,23,36,57,68,84
- +1.8V ○ —◇— +1.8V 7,8,9,11,14,15,57,83,84,91
- +5V ○ —◇— +5V 52,57,67,68,91

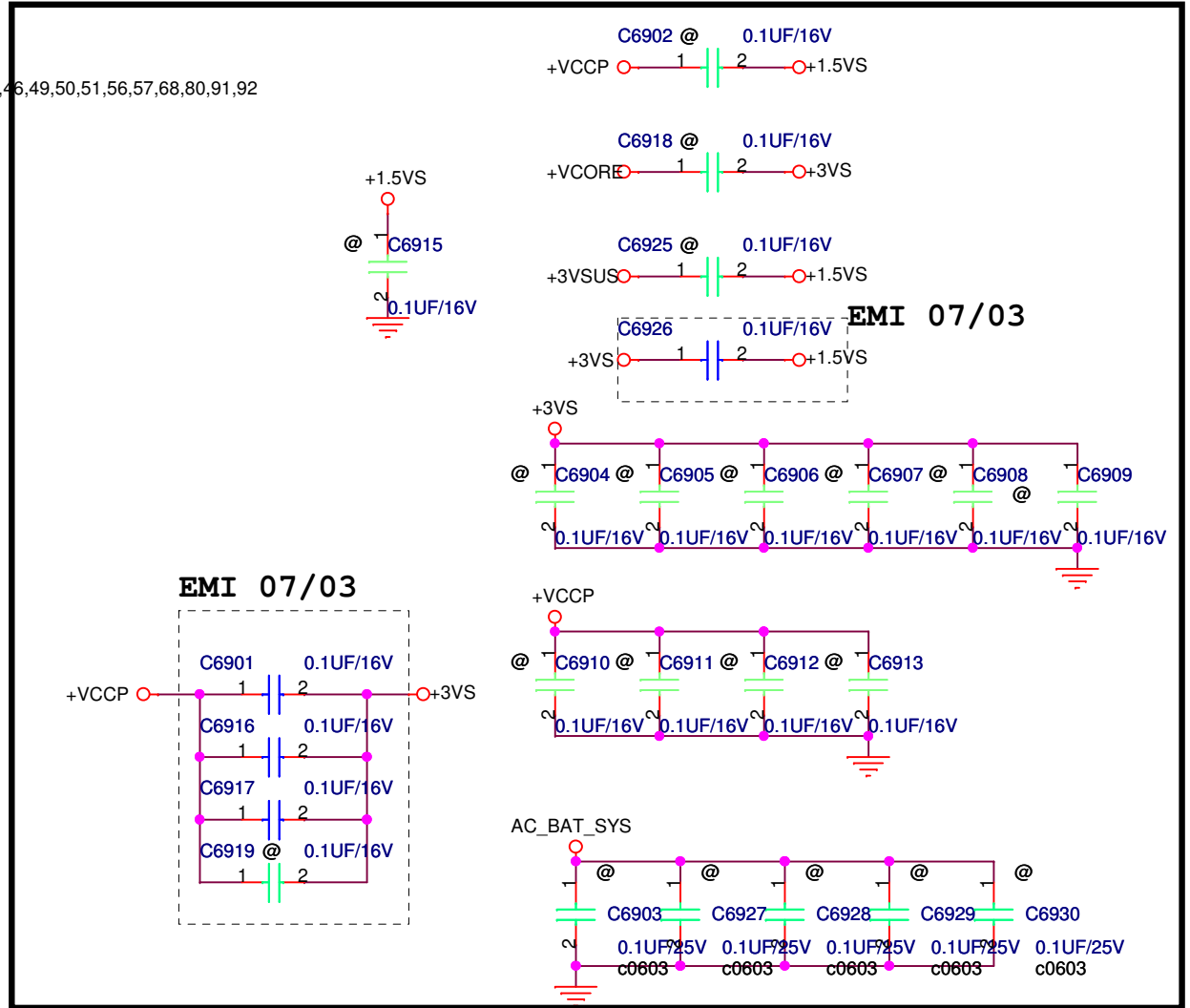
- +5VS ○ —◇— +5VS 23,36,38,50,51,56,57,68,80,84,91
- +3VA ○ —◇— +3VA 20,30,56,67,81,88
- +VCC_RTC ○ —◇— +VCC_RTC 20,23
- +3V ○ —◇— +3V 46,57,68,91
- +3VSUS ○ —◇— +3VSUS 20,21,22,23,30,57,68,80,81,91,92
- +5VSUS ○ —◇— +5VSUS 23,80,81,82,83,88,91
- +3VPLL ○ —◇— +3VPLL 30,31
- +3VACC ○ —◇— +3VACC 30
- +3VA_EC ○ —◇— +3VA_EC 30,31

- +5VS_AMP ○ —◇— +5VS_AMP 36
- +12V ○ —◇— +12V 91
- +12VS ○ —◇— +12VS 22,46,91

- AC_BAT_SYS ○ —◇— AC_BAT_SYS 46,80,81,82,83,88

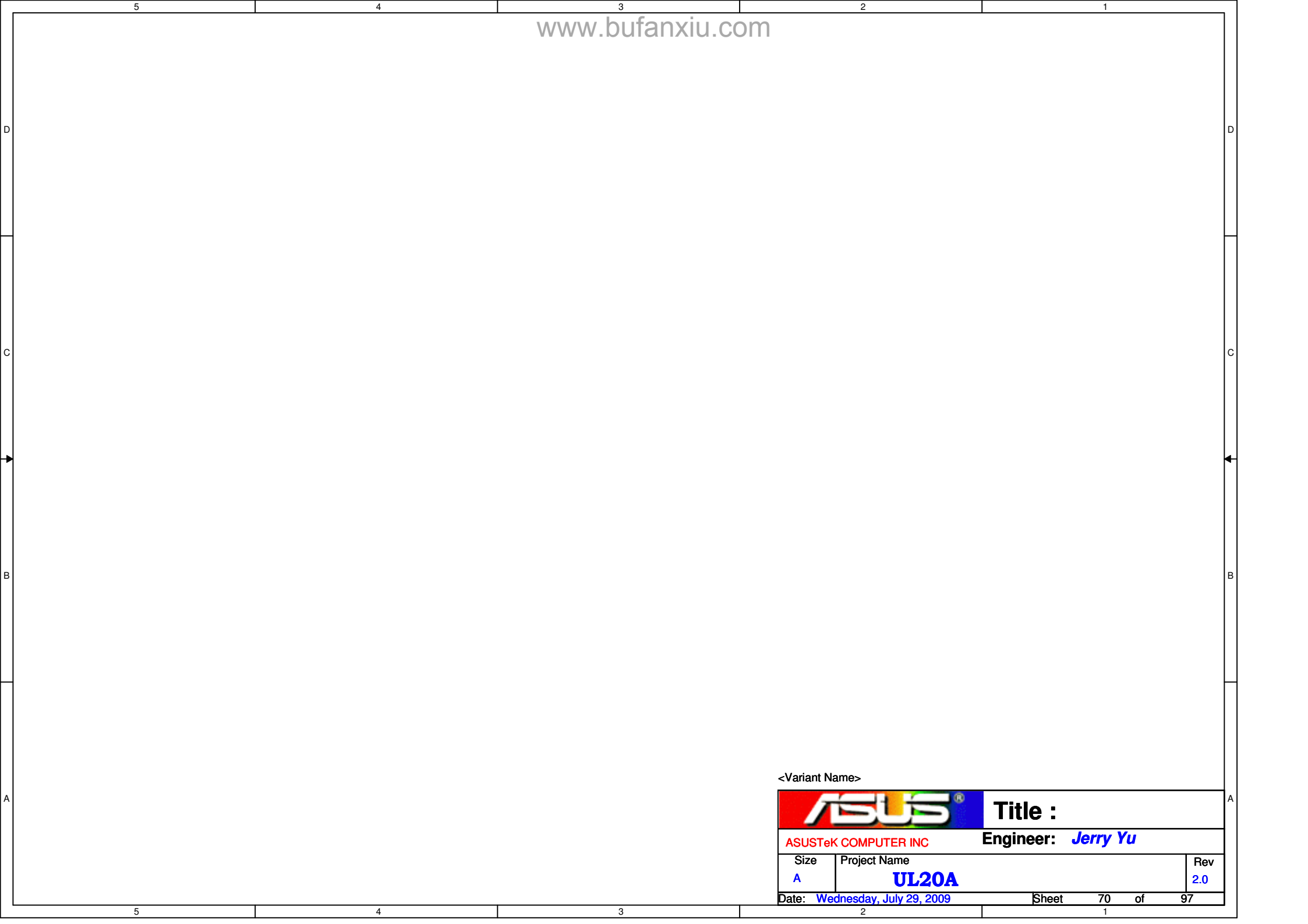
- +5VA ○ —◇— +5VA 56,67,68,81

EMI 05/25




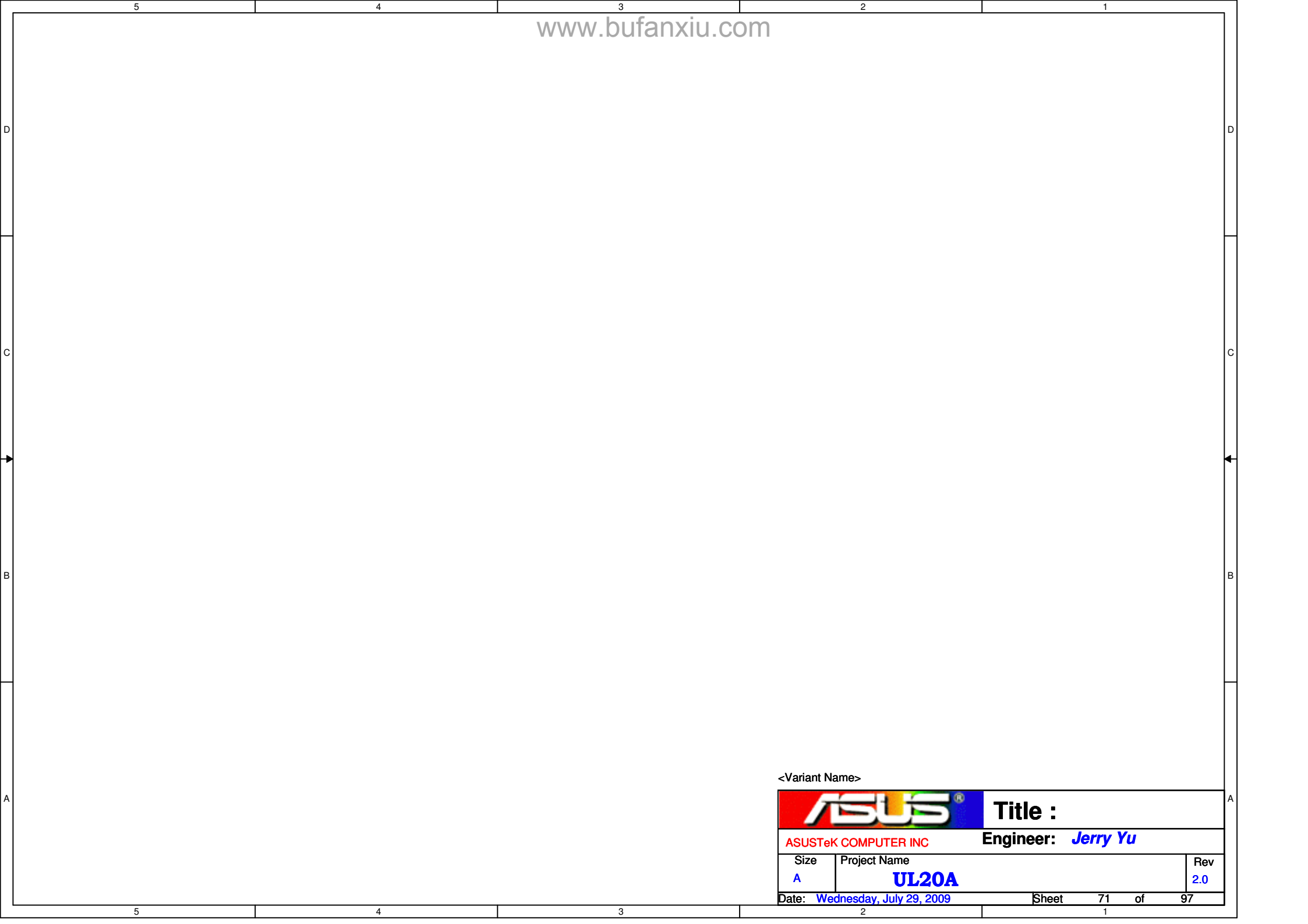
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size A	Project Name UL20A	Rev 2.0	
Date: Monday, August 03, 2009		Sheet 69 of 97	




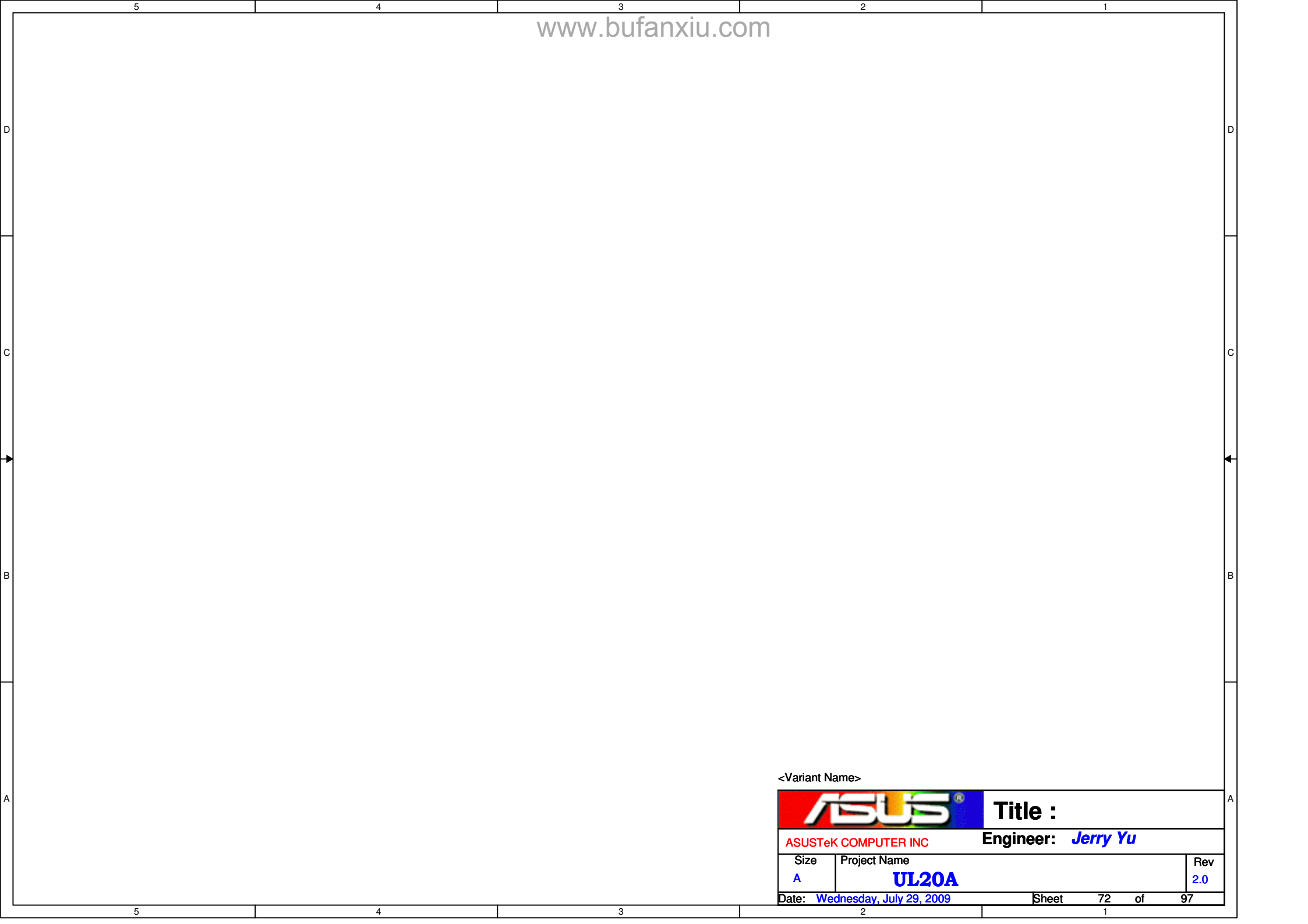
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 70 of 97




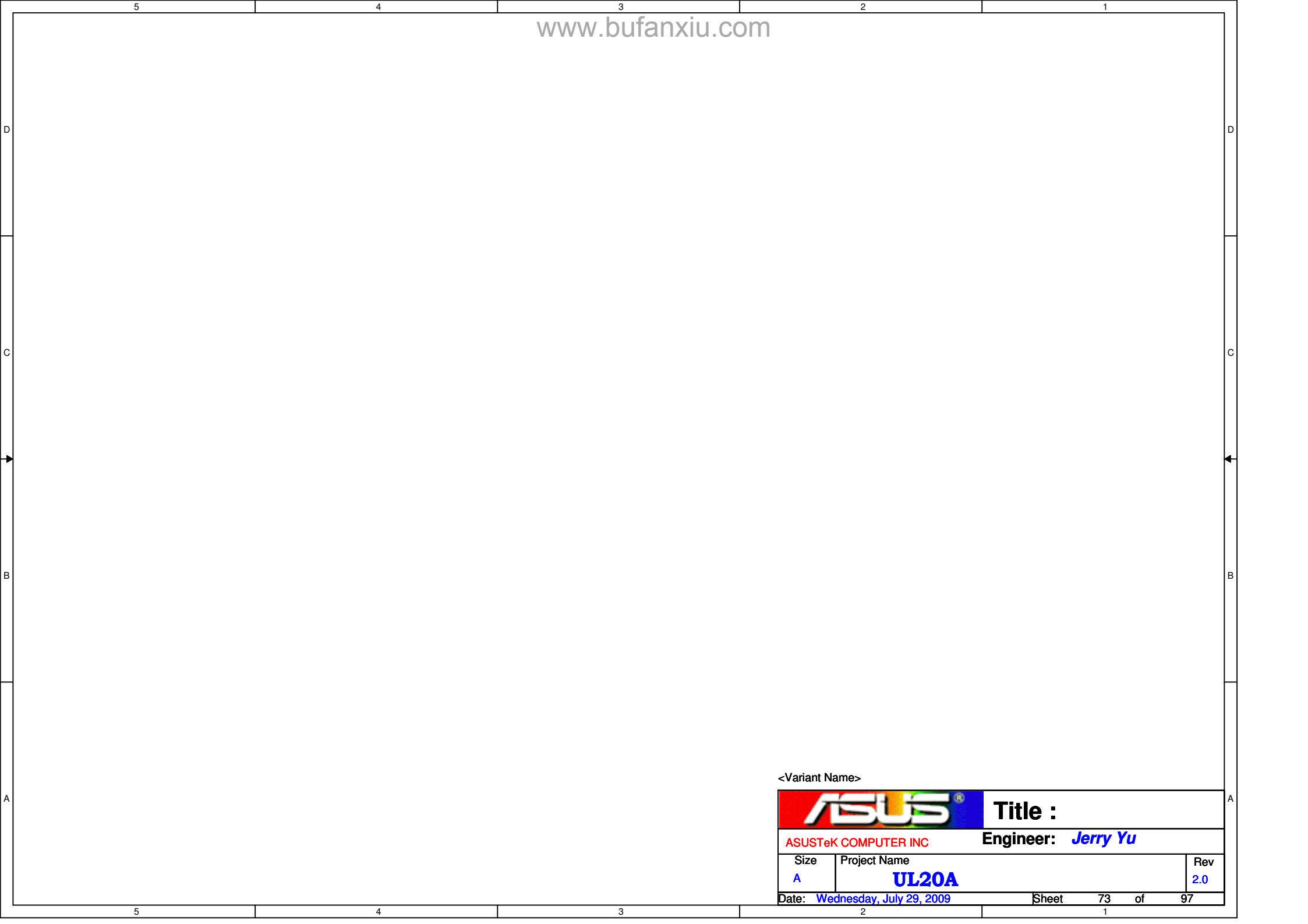
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <i>Wednesday, July 29, 2009</i>		Sheet 71 of 97




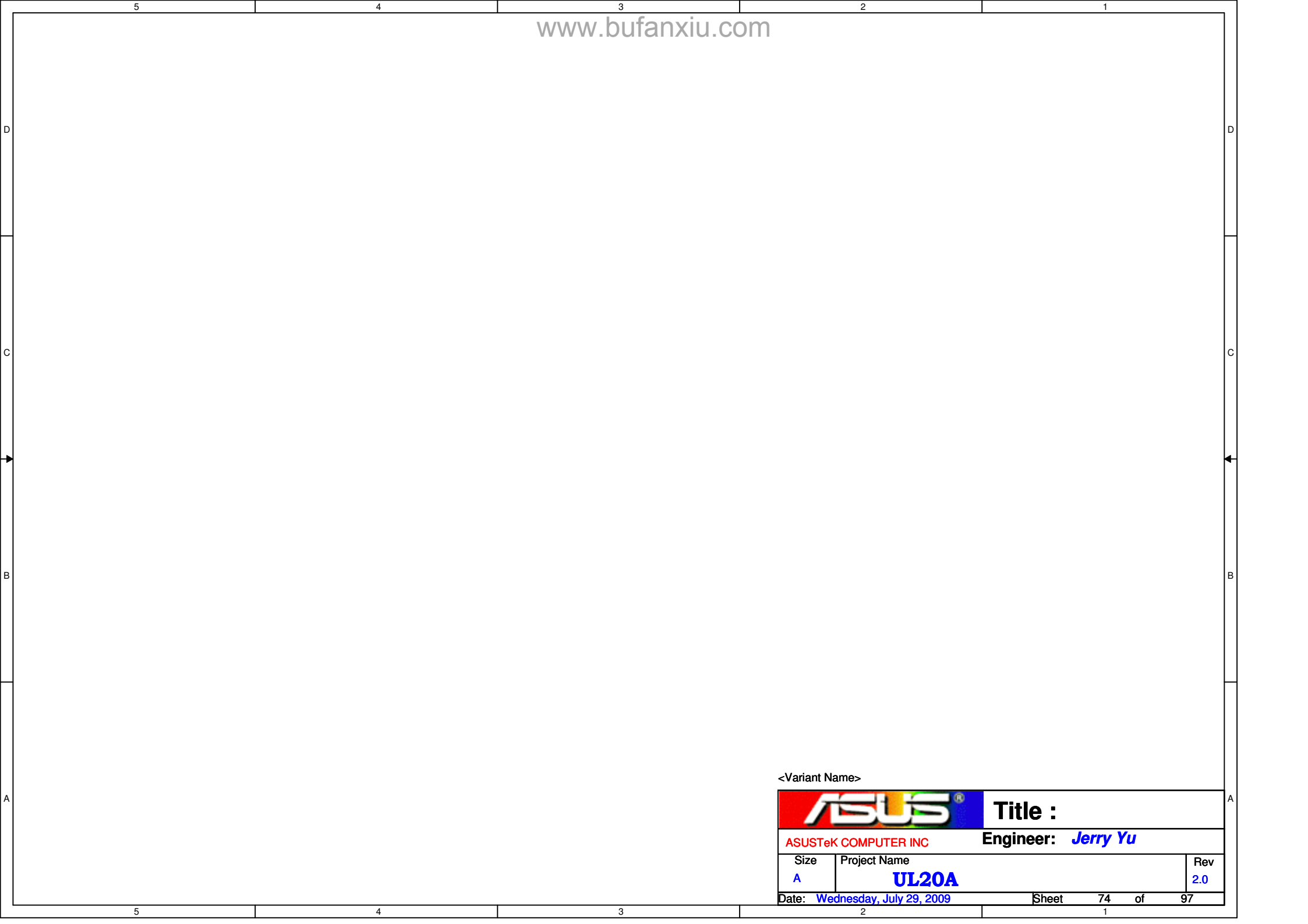
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 72 of 97




<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 73 of 97




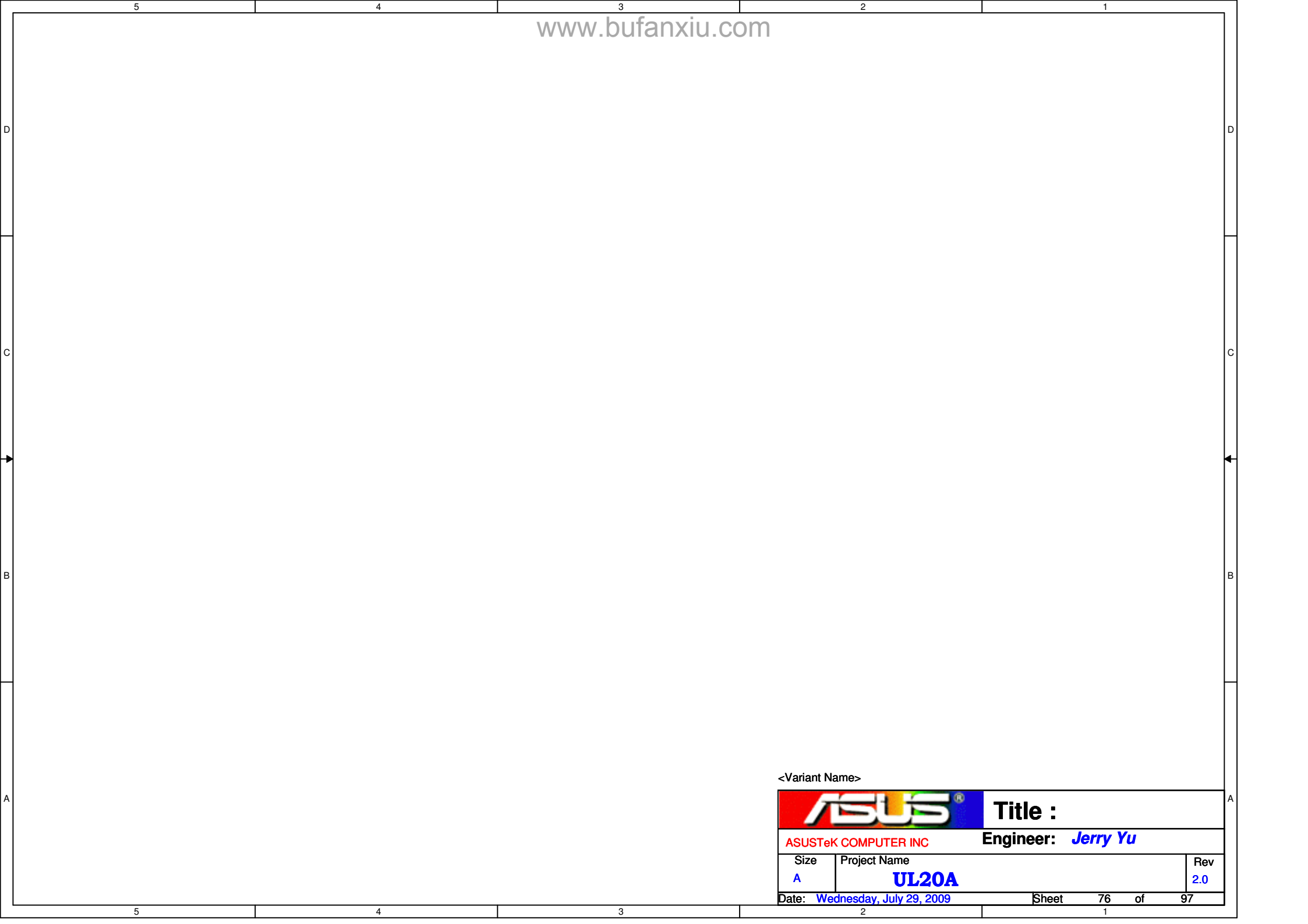
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 74 of 97


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	75 of 97




<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 76 of 97


5	4	3	2	1
D				D
C				C
B				B
A				A

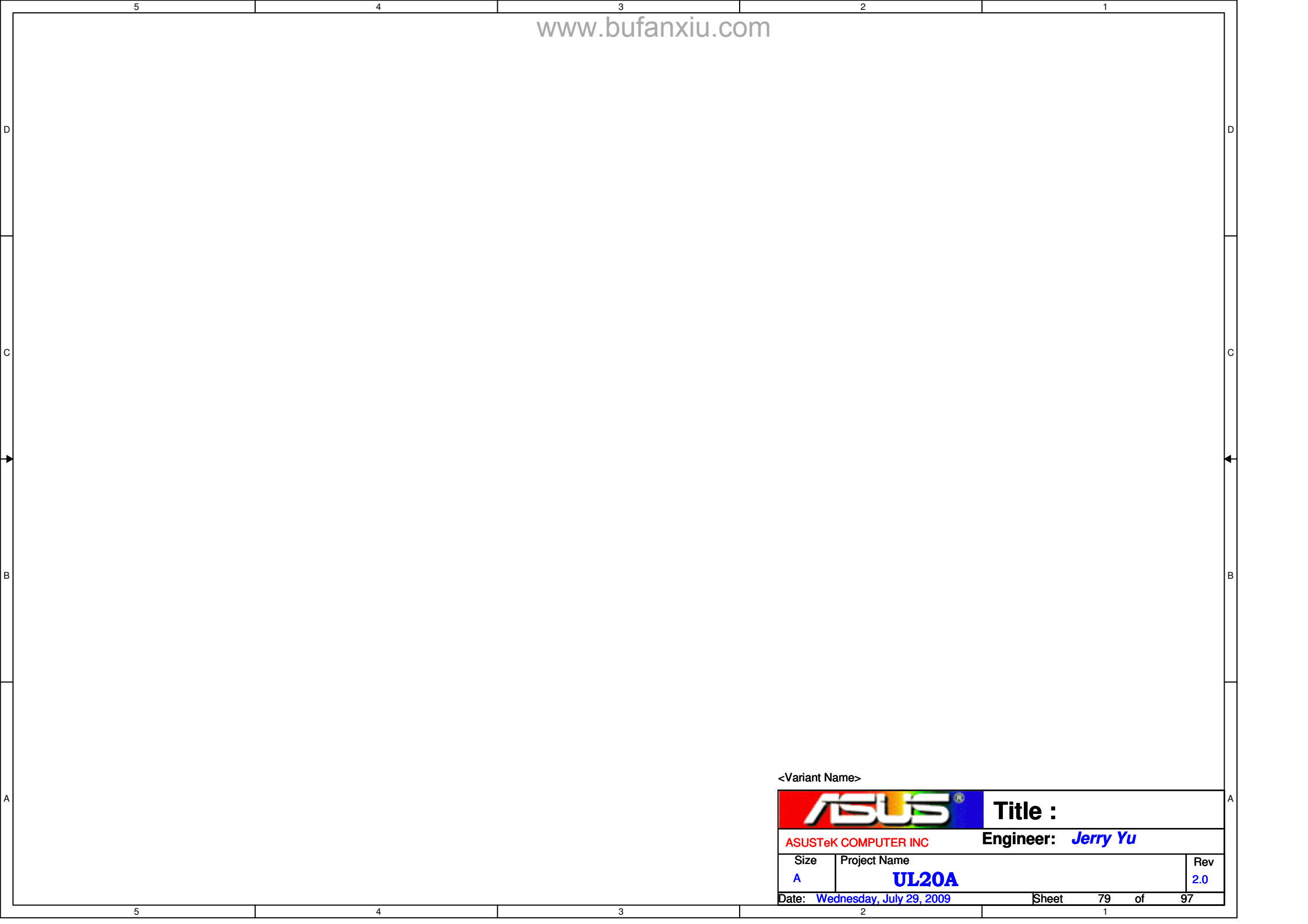
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: Wednesday, July 29, 2009		Sheet 77 of 97


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name	Rev	
A	UL20A	2.0	
Date: <u>Wednesday, July 29, 2009</u>		Sheet	78 of 97

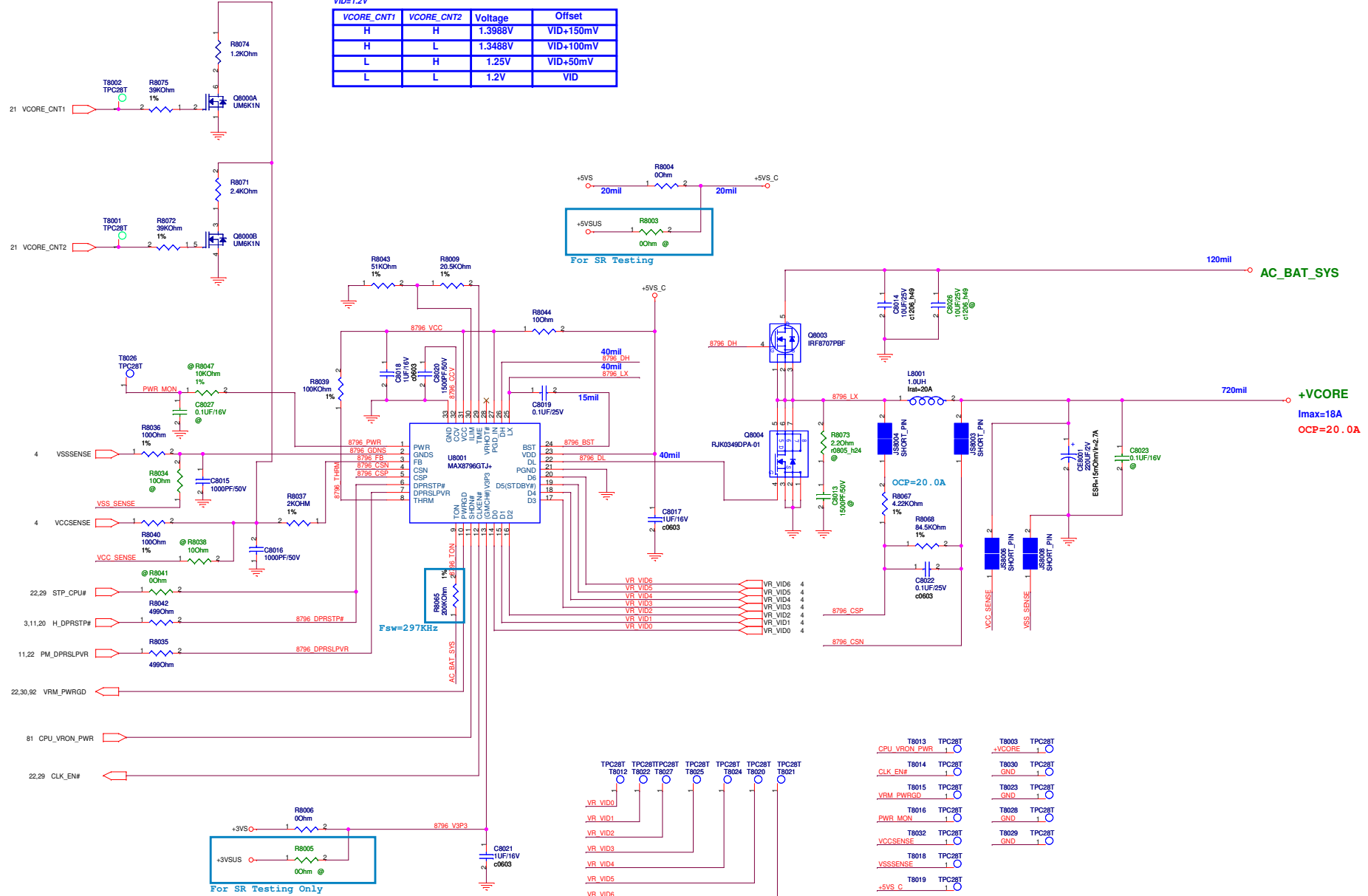


<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>
Size A	Project Name UL20A	Rev 2.0
Date: <u>Wednesday, July 29, 2009</u>		Sheet 79 of 97

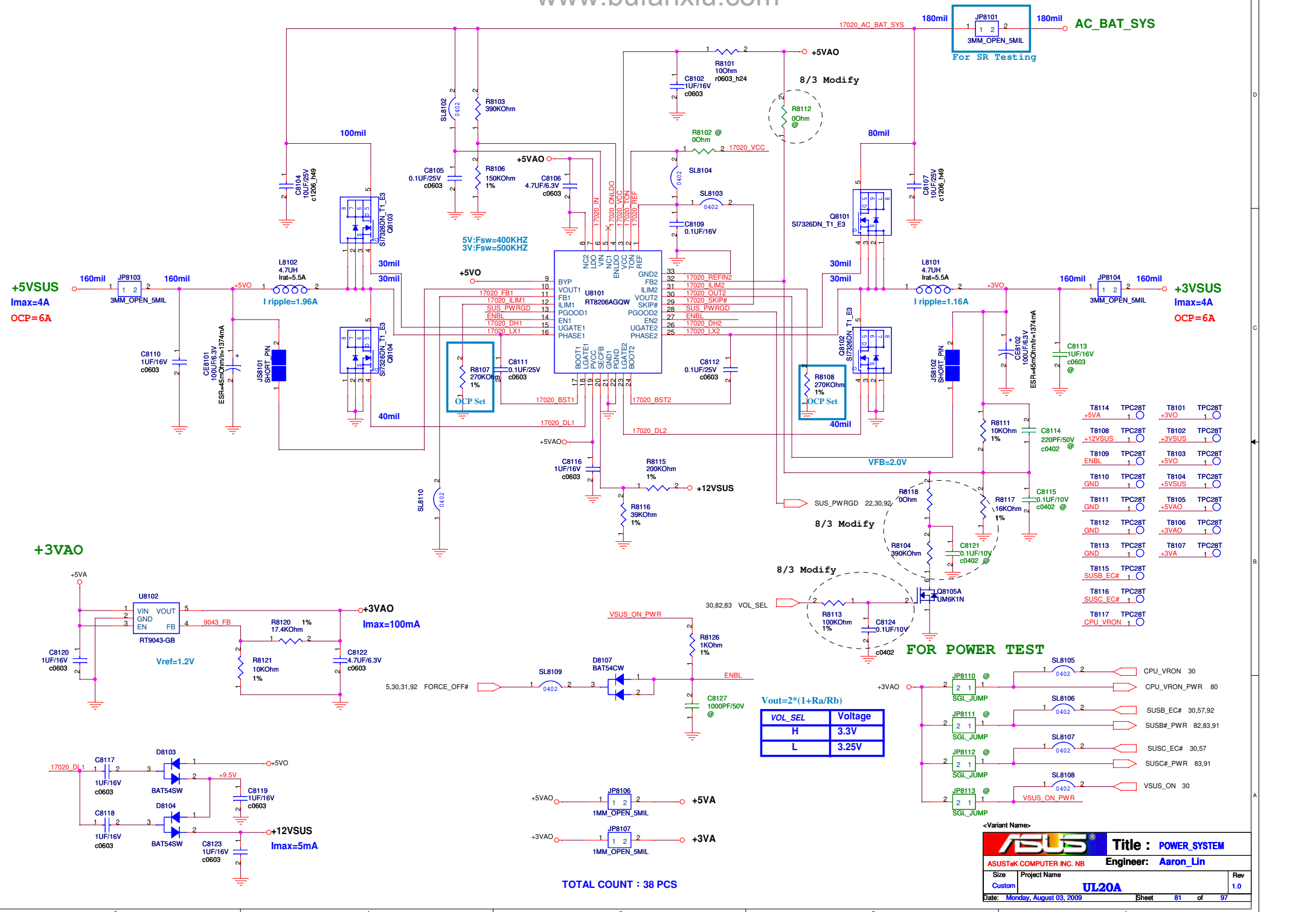
CPU
VID=1.2V

VCORE_CNT1	VCORE_CNT2	Voltage	Offset
H	H	1.3988V	VID+150mV
H	L	1.3488V	VID+100mV
L	H	1.25V	VID+50mV
L	L	1.2V	VID



TOTAL COUNT : 29 PCS

- T8013 TPC28T CPU_VRON_PWR
- T8014 TPC28T CLK_EN#
- T8015 TPC28T VRM_PWRGD
- T8016 TPC28T PWR_MON
- T8032 TPC28T VCCSENSE
- T8018 TPC28T VSSSENSE
- T8019 TPC28T -5VS_C
- T8031 TPC28T STP_CPU#
- T8033 TPC28T H_DPRSTP#
- T8034 TPC28T PM_DPRSLPVR
- T8003 TPC28T -VCORE
- T8030 TPC28T GND
- T8023 TPC28T GND
- T8028 TPC28T GND
- T8029 TPC28T GND
- T8000 TPC28T GND
- T8001 TPC28T GND
- T8002 TPC28T GND
- T8004 TPC28T GND
- T8005 TPC28T GND
- T8006 TPC28T GND
- T8007 TPC28T GND
- T8008 TPC28T GND
- T8009 TPC28T GND
- T8010 TPC28T GND
- T8011 TPC28T GND
- T8012 TPC28T GND
- T8020 TPC28T GND
- T8021 TPC28T GND
- T8022 TPC28T GND
- T8024 TPC28T GND
- T8025 TPC28T GND
- T8026 TPC28T GND
- T8027 TPC28T GND



$V_{out} = 2 * (1 + R_a / R_b)$

VOL_SEL	Voltage
H	3.3V
L	3.25V

- T8114 TPC28T T8101 TPC28T
- 5VA 1 1 -3VO 1
- T8108 TPC28T T8102 TPC28T
- +12VSUS 1 1 -3VSUS 1
- T8109 TPC28T T8103 TPC28T
- ENBL 1 1 +5VO 1
- T8110 TPC28T T8104 TPC28T
- GND 1 1 -5VSUS 1
- T8111 TPC28T T8105 TPC28T
- GND 1 1 -5VAO 1
- T8112 TPC28T T8106 TPC28T
- GND 1 1 -3VAO 1
- T8113 TPC28T T8107 TPC28T
- GND 1 1 -3VA 1
- T8115 TPC28T
- SUSB_EC# 1 1
- T8116 TPC28T
- SUSC_EC# 1 1
- T8117 TPC28T
- CPU_VRON 1 1

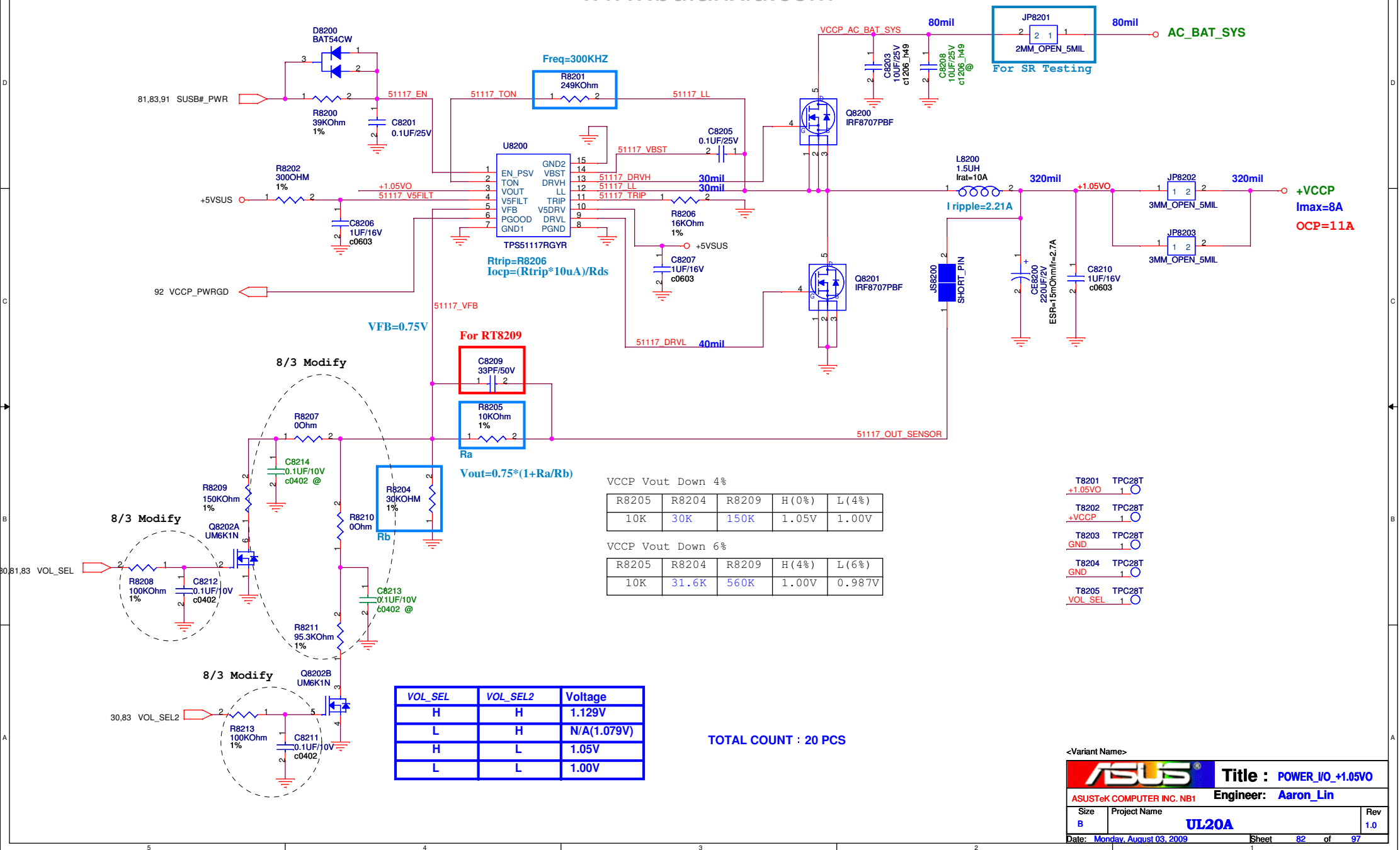
ASUS Title : POWER_SYSTEM

ASUSTek COMPUTER INC. NB Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UL20A	1.0

Date: Monday, August 03, 2009 Sheet 81 of 97

TOTAL COUNT : 38 PCS



For RT8209
 $V_{out} = 0.75 * (1 + R_a/R_b)$

VCCP Vout Down 4%

R8205	R8204	R8209	H (0%)	L (4%)
10K	30K	150K	1.05V	1.00V

VCCP Vout Down 6%

R8205	R8204	R8209	H (4%)	L (6%)
10K	31.6K	560K	1.00V	0.987V

VOL_SEL	VOL_SEL2	Voltage
H	H	1.129V
L	H	N/A(1.079V)
H	L	1.05V
L	L	1.00V

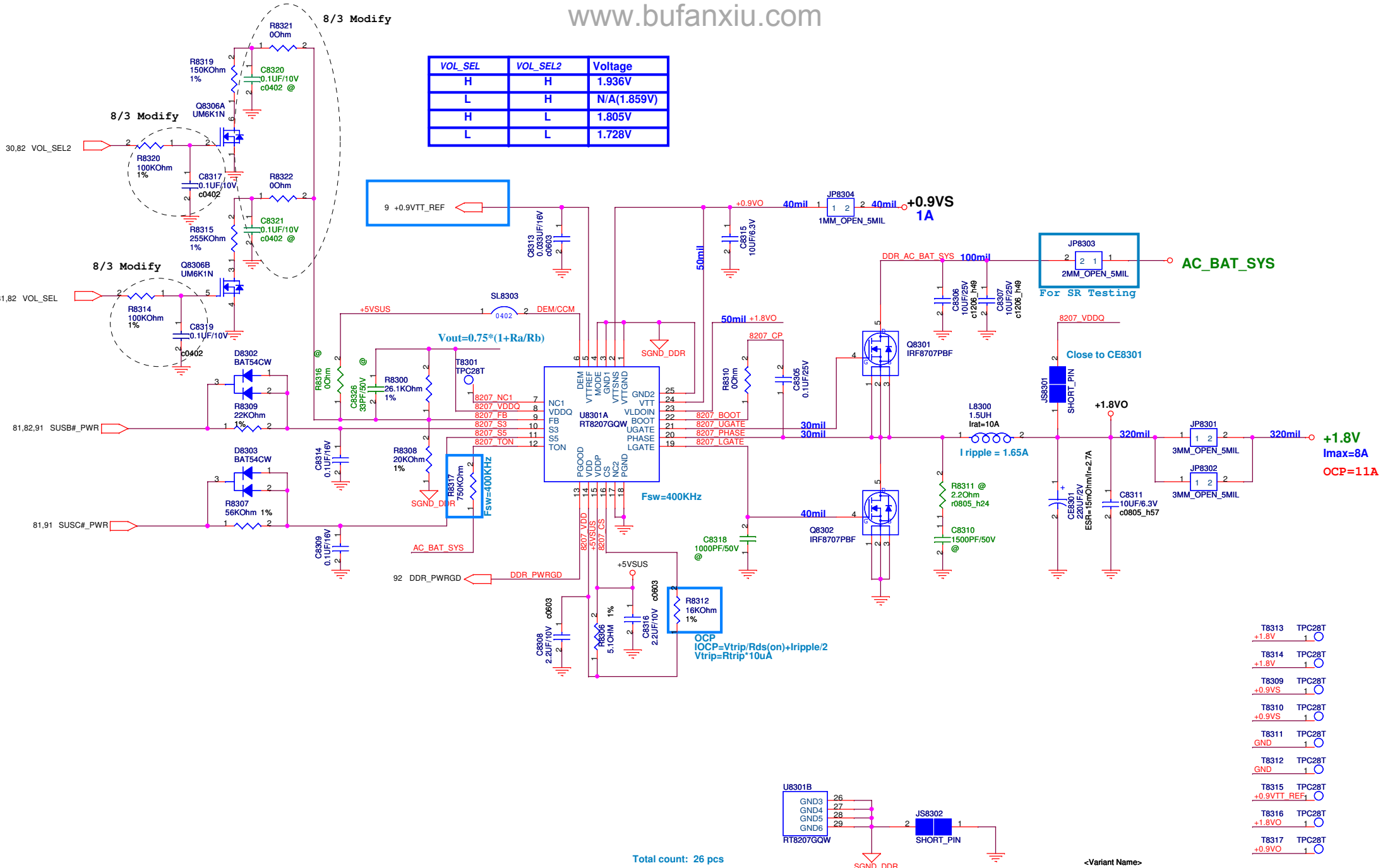
TOTAL COUNT : 20 PCS

- T8201 TPC28T +1.05VO 1
- T8202 TPC28T +VCCP 1
- T8203 TPC28T GND 1
- T8204 TPC28T GND 1
- T8205 TPC28T VOL_SEL 1

<Variant Name>

ASUS		Title : POWER_IO_+1.05VO
ASUSTeK COMPUTER INC. NB1		Engineer: Aaron_Lin
Size B	Project Name UL20A	Rev 1.0
Date: Monday, August 03, 2009	Sheet 82	of 97

VOL_SEL	VOL_SEL2	Voltage
H	H	1.936V
L	H	N/A(1.859V)
H	L	1.805V
L	L	1.728V



9 +0.9VTT_REF

+0.9V 1A

AC_BAT_SYS

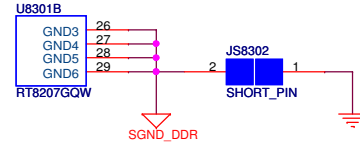
+1.8V
Imax=8A
OCP=11A

$V_{out} = 0.75 * (1 + R_a/R_b)$

Fsw=400KHz

Total count: 26 pcs

- T8313 TPC28T +1.8V 1
- T8314 TPC28T +1.8V 1
- T8309 TPC28T +0.9VS 1
- T8310 TPC28T +0.9VS 1
- T8311 TPC28T GND 1
- T8312 TPC28T GND 1
- T8315 TPC28T +0.9VTT_REF 1
- T8316 TPC28T +1.8V 1
- T8317 TPC28T +0.9V 1



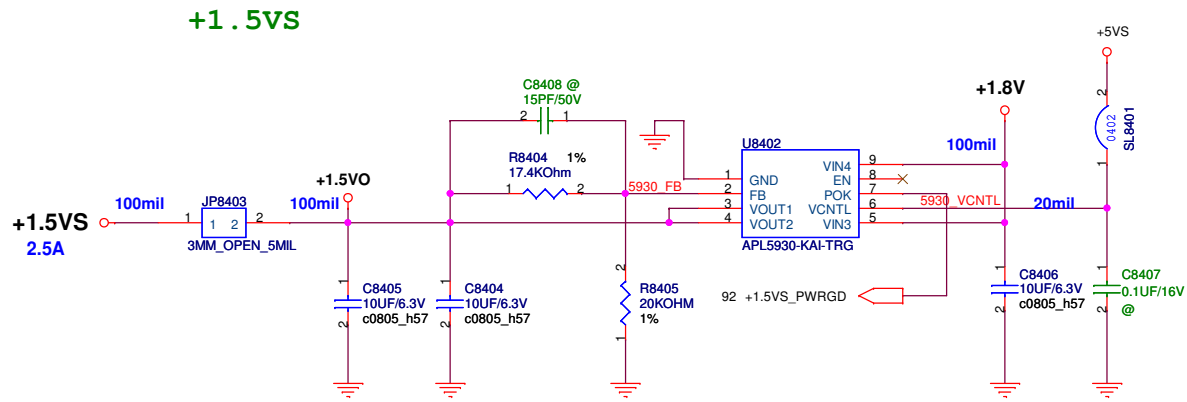
<Variant Name>

ASUS Title : POWER_I/O_DDR & VTT

ASUSTeK COMPUTER INC. NB Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	UL20A	1.0

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T8405	TPC28T	
+1.5VO	1	○
T8406	TPC28T	
+1.5VS	1	○
T8407	TPC28T	
GND	1	○
T8408	TPC28T	
GND	1	○

Total count: 6 pcs


<Variant Name>

		Title : POWER_I/O_+1.8VS	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
B	UL20A	1.0	
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<-Variant Name>

		Title : +MCP_VDD_CORE	
ASUSTek COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
Date: Monday, August 03, 2009		Sheet	85 of 97

<Variant Name>

		Title : N/A
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin
Size B	Project Name UL20A	Rev 1.0
Date: Monday, August 03, 2009		Sheet 86 of 97

<Variant Name>

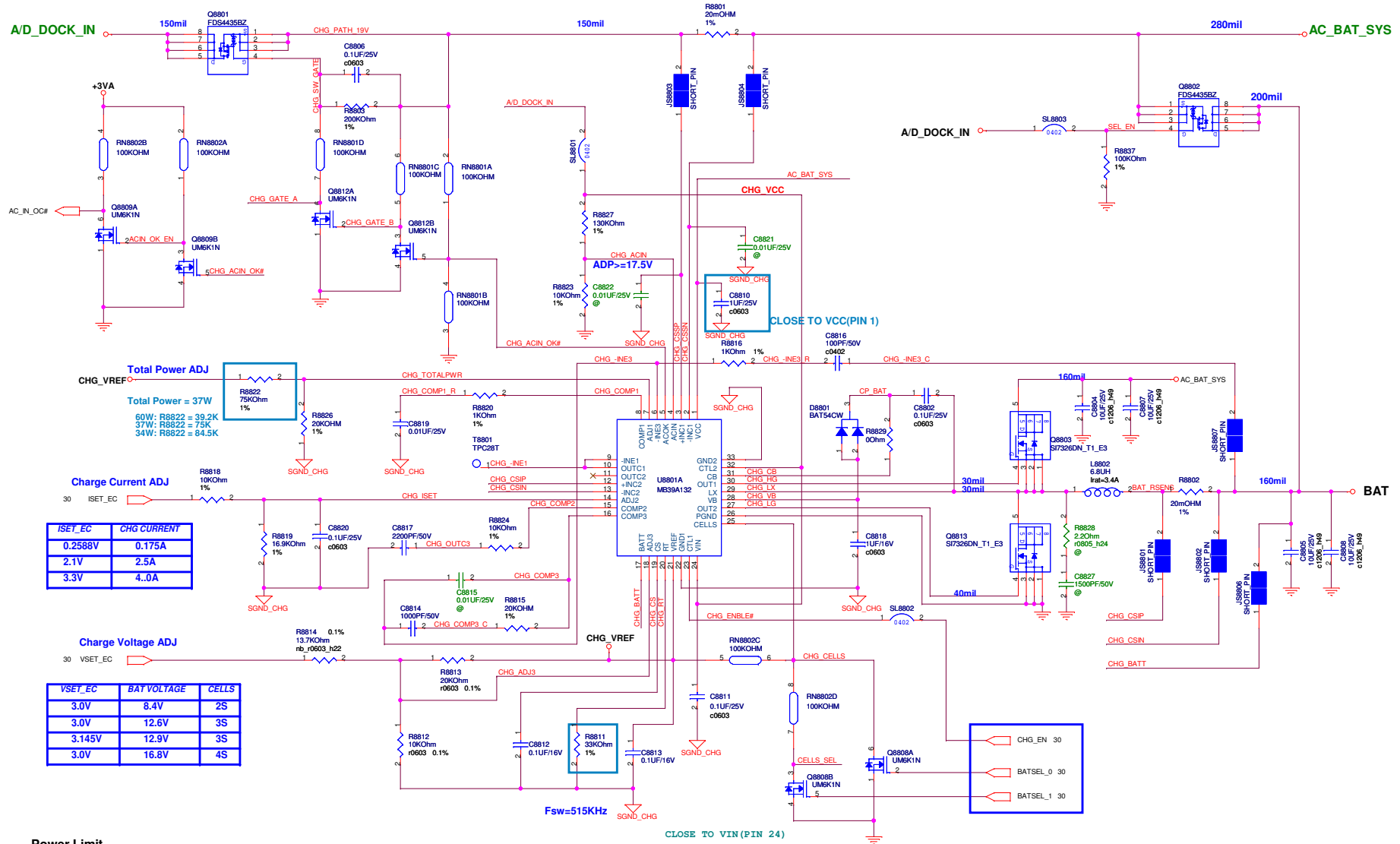
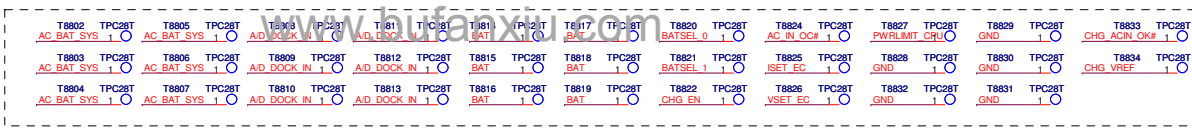
		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
Date: Monday, August 03, 2009		Sheet	87 of 97

N31 Adaptor : 19V/2.1A (40W)

Adaptor 65W
Power Limit 63W
Total Power 60W

Adaptor 40W
Power Limit 39W
Total Power 37W

Adaptor 36W
Power Limit 35W
Total Power 34W



Total Power ADJ

Total Power = 37W

60W: R8822 = 39.2K
37W: R8822 = 75K
34W: R8822 = 84.5K

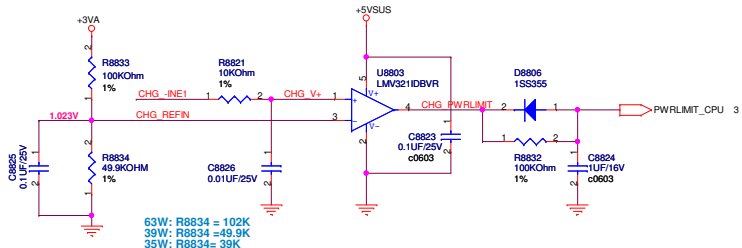
Charge Current ADJ

ISET_EC	CHG CURRENT
0.2588V	0.175A
2.1V	2.5A
3.3V	4.0A

Charge Voltage ADJ

VSET_EC	BAT VOLTAGE	CELLS
3.0V	8.4V	2S
3.0V	12.6V	3S
3.145V	12.9V	3S
3.0V	16.8V	4S

Power Limit
Power Limit = 39W




TOTAL COUNT : 58 PCS

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202


<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
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BATTERY IN DETECT

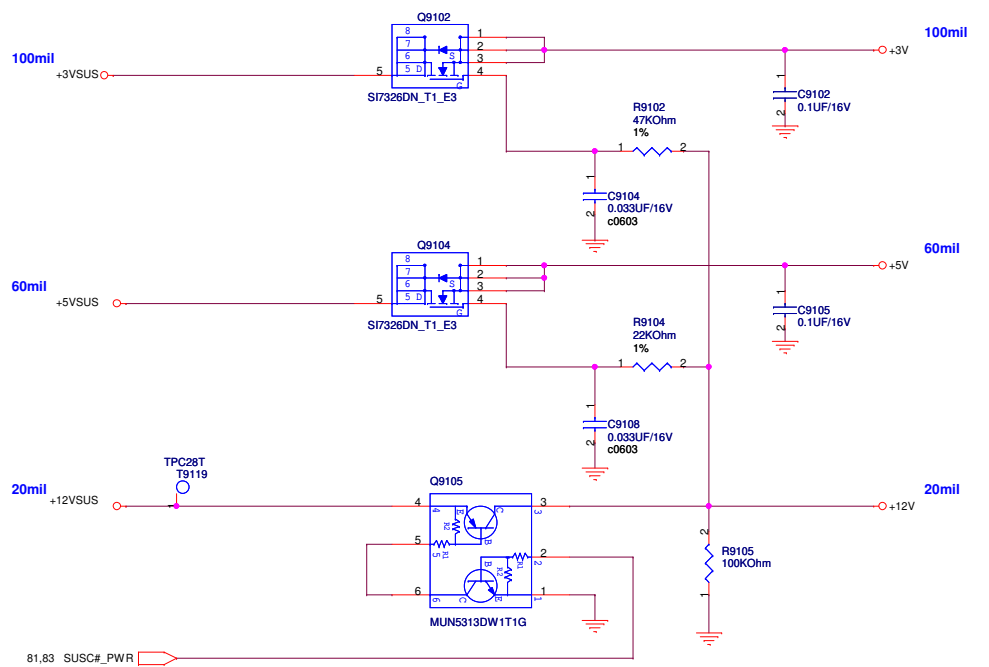
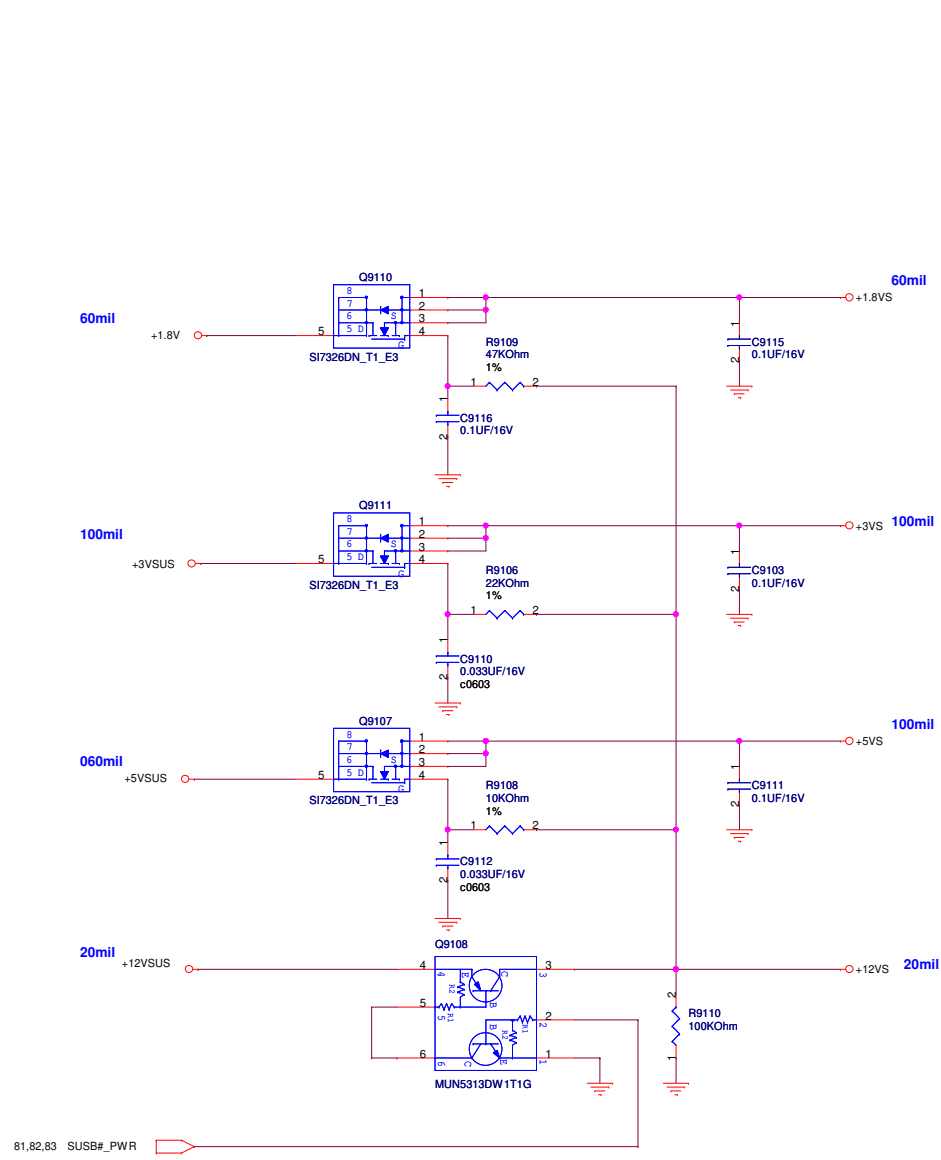
ADAPTER IN DETECT

<Variant Name>

		Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
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SUSB#_PWR POWER

SUSC#_PWR POWER



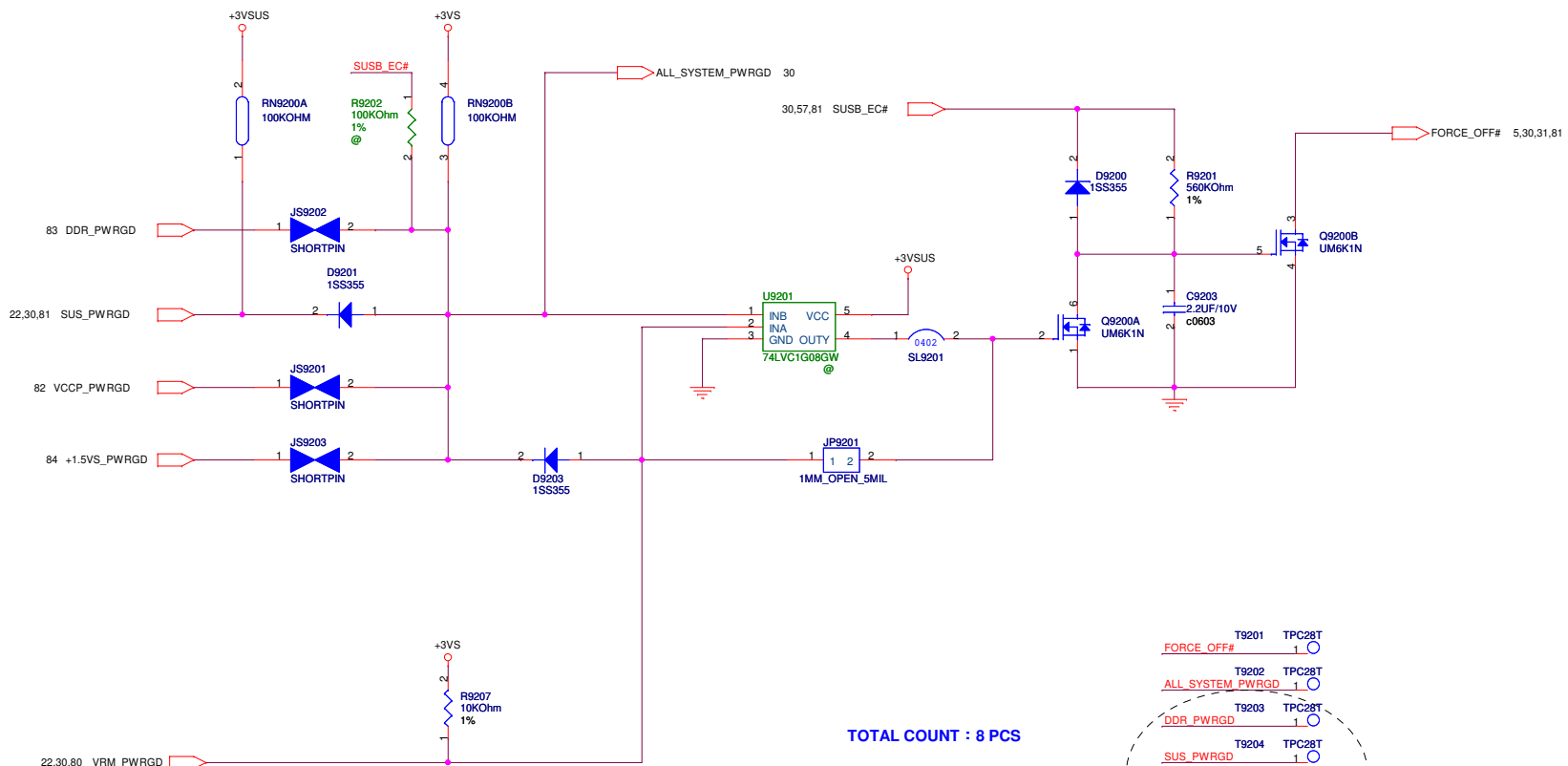
T9101	TPC28T	T9111	TPC28T
+12VSUS	1	+3VSUS	1
T9102	TPC28T	T9113	TPC28T
+12VS	1	+3VS	1
T9103	TPC28T	T9115	TPC28T
+12V	1	+3V	1
T9104	TPC28T	T9120	TPC28T
+5VSUS	1	+1.8V	1
T9106	TPC28T	T9121	TPC28T
+5VS	1	+1.8VS	1
T9110	TPC28T	T9123	TPC28T
+5V	1	SUSB#_PWR1	1
		T9114	TPC28T
		SUSC#_PWR1	1

TOTAL COUNT : 19 PCS

<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
ASUSTek COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
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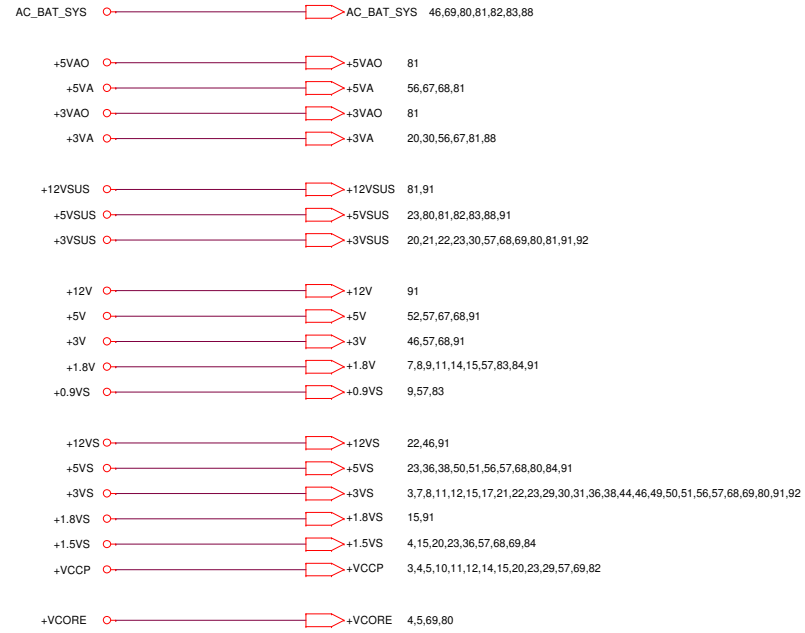
POWER GOOD DETECTOR




TOTAL COUNT : 8 PCS

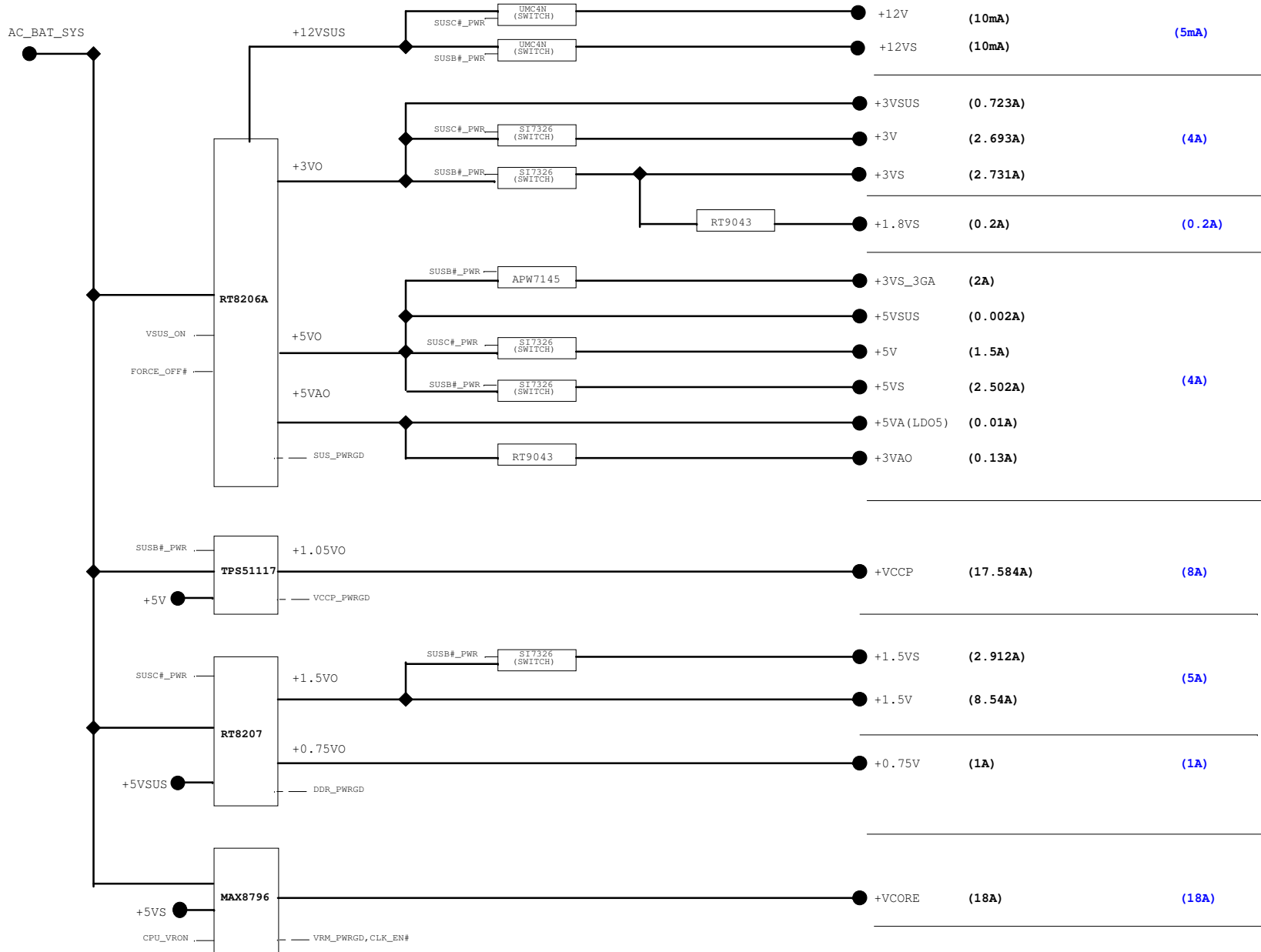
- T9201 TPC28T FORCE_OFF# 1
- T9202 TPC28T ALL_SYSTEM_PWRGD 1
- T9203 TPC28T DDR_PWRGD 1
- T9204 TPC28T SUS_PWRGD 1
- T9205 TPC28T VCCP_PWRGD 1
- T9206 TPC28T +1.5VS_PWRGD 1

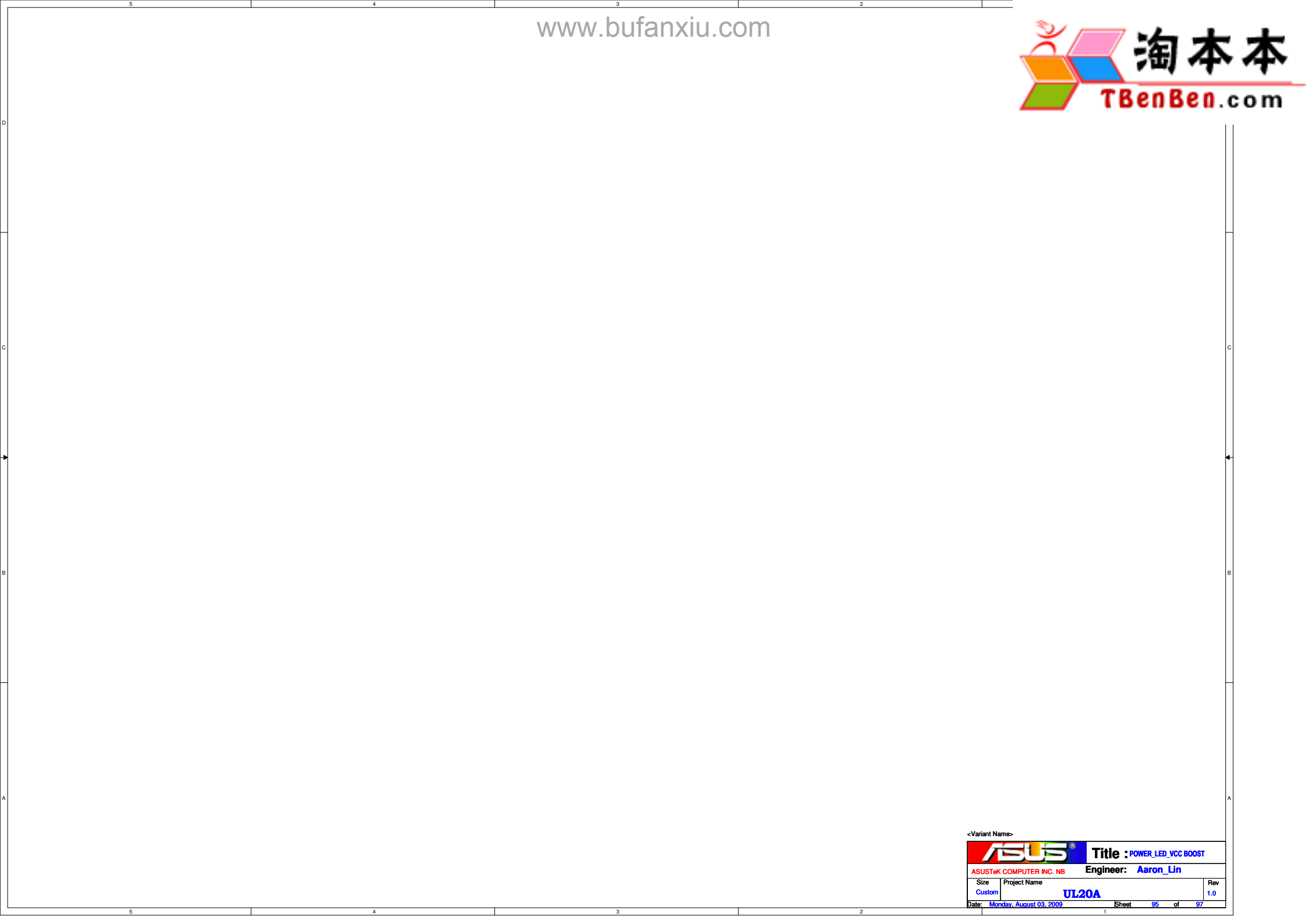
7/20 Modify




<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
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<Variant Name>

		Title : POWER_LED_VCC BOOST	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
Size	Project Name	Rev	
Custom	UL20A	1.0	
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Rev	Date	Description
1.2a	2009/06/15	Item 1 remove CE0502 220uF, C0501,C0503,C0504 10uF/10V (0805) add C0532,C0533,C0534,C0535,C0536,C0501,C0503,C0504 10uF/6.3V(0603) Item 2 connect SW5601,SW5602 pin5&6 to GND Item 3 change TP/DeBUG conn to 12G183401225 ME request Item 4 unmount R3602,R3603,C3603 disable PC beep function
1.2b	2009/06/22	Item 1 change D6002 to 07G001023010 Item 2 add D5601,D5602,D6702 for ESD Item 3 add R3001 to reduce xtal DL Item 4 EA CLK: RN2905->47ohm, C2932=C2933=C6813=C6814->5pF Item 5 EA CRT: R1208->1k ohm Item 6 change Camera conn to 12G17100006F for cost down Item 7 charge/PWR LED connect from VSUS to VA (P.56), cap/num lock LED connect from VS to VA (P.67)
1.2c	2009/06/29	Item 1 update PWR schematic 0701 Item 2 change audio 5V LDO 06G029330020 by designIP (P.36) Item 3 restore CE0502 220uF Item 4 EMI: add C5605, C5606 0.1uF on Left/Right Item 5 Thermal: change H6524 to 2.4mm hole
1.2	2009/07/03	Item 1 EMI: mount C6801,C6804,C6805,C6806,C6807,C6808,C6820,C6901,C6916,C6917, C6926,C1431,C3601,C3621
2.0a	2009/07/20	Item 1 change J6802.19 to +5VA
2.0b	2009/07/28	Item 1 Thermal: change H6524 to 6.6mm hole Item 2 update PWR circuit: 1.8V low voltage circuit Item 3 add vol_sel2 on EC GPH3 Item 4 update PWR circuit: Vcore/Vccp/1.8V/3.3V voltage control Item 5 add BSEL strap Q2902 circuit for over clocking (P.29)
2.0	2009/08/03	Item 1 PWR: update 3.3V/VCCP/DDR power control circuit

Rev	Date	Description

