

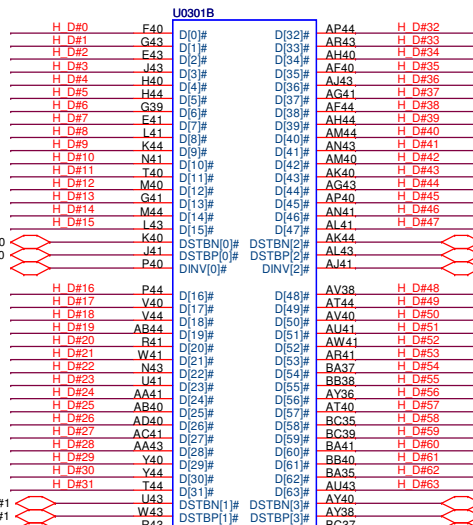
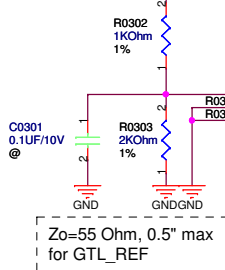
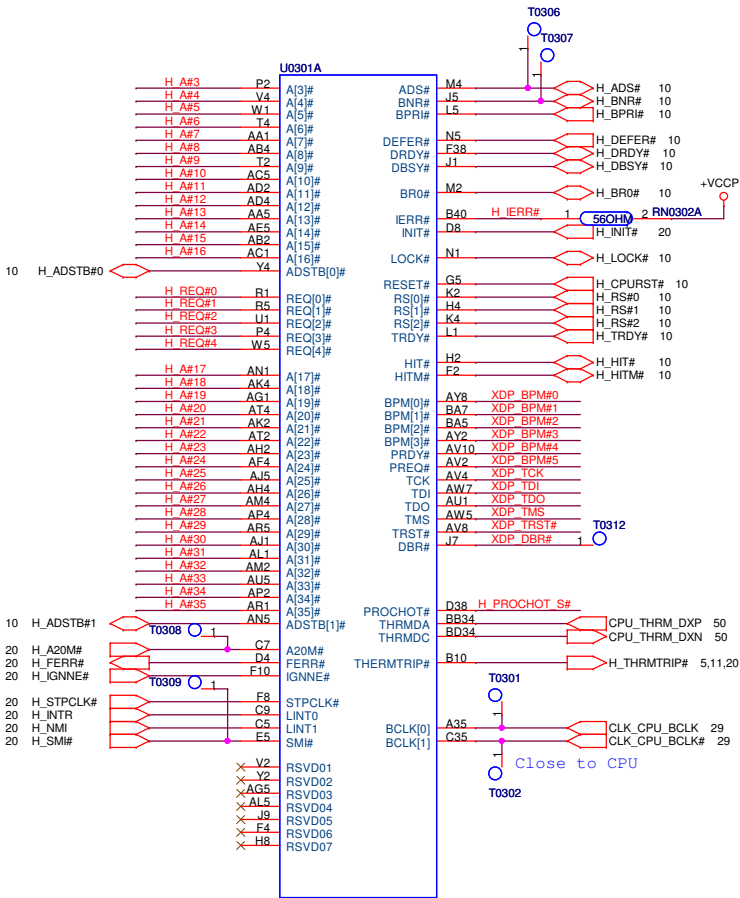
CLOCK GENERATOR RTM875T-336
FAN & THERMAL SENSOR

## POWER

VCORE
SYSTEM
I/O_1.5VS & 1.05VS
I/O_DDR & VTT
I/O_ +1.8VS
CHARGER
LCD DRIVER



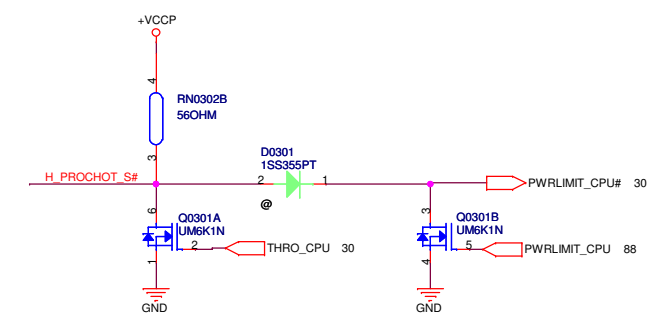
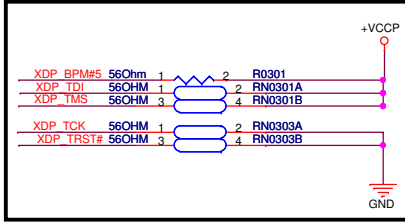
- 10 H\_D#[63:0] H\_D#[63:0]
- 10 H\_A#[35:3] H\_A#[35:3]
- 10 H\_REQ#[4:0] H\_REQ#[4:0]



Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"  
 Comp 1,3: Z0=55 Ohm, trace length < 0.5"

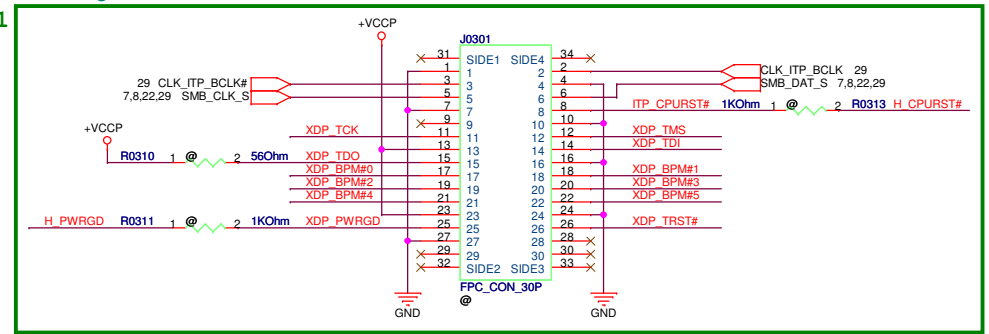
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

### Default Strapping When Not Used



### ITP Debug Port

R1.1



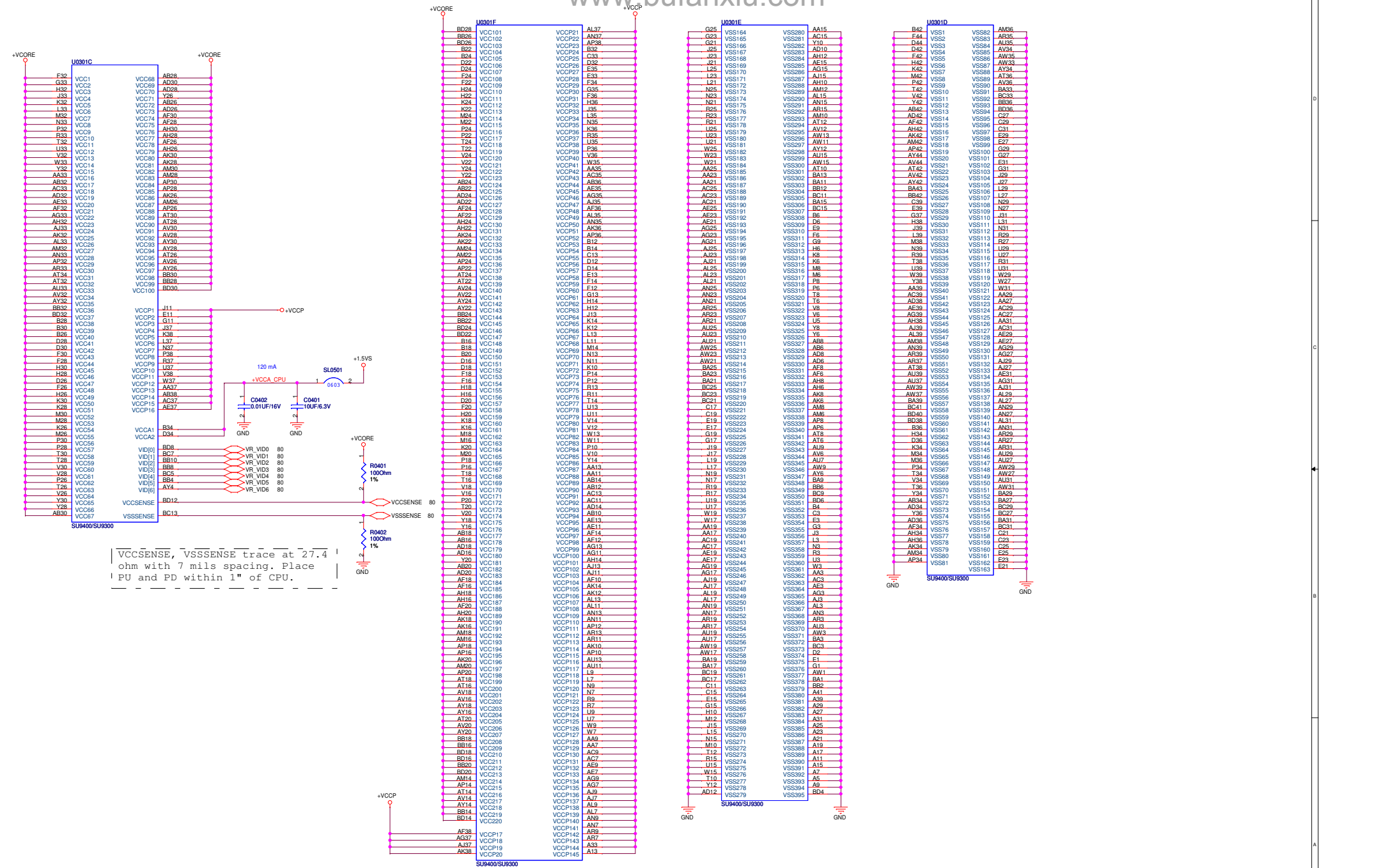
ASUS Logo

Title: CPU PENRYN ULV FSB

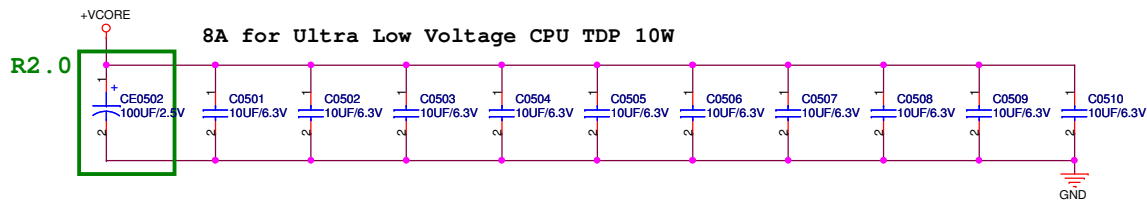
ASUSTek COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

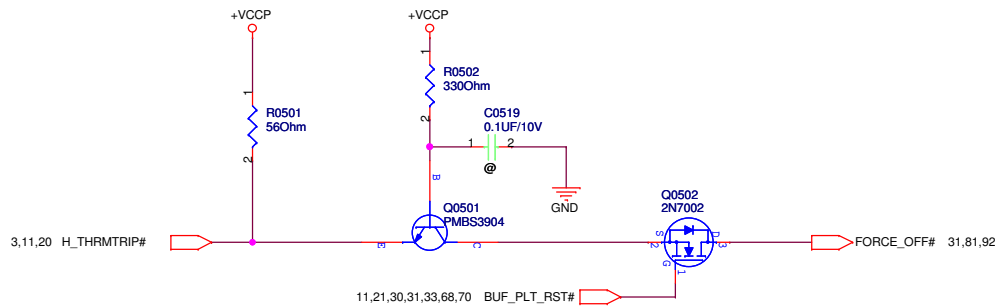
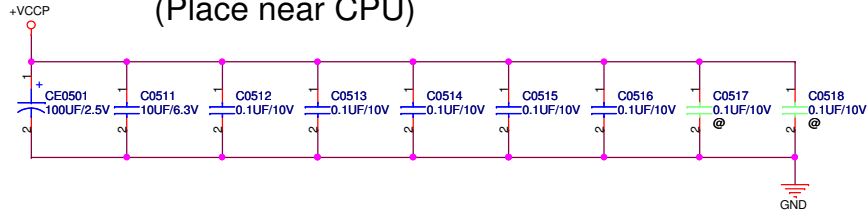
Date: Tuesday, March 31, 2009 Sheet 3 of 97



VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place PU and PD within 1" of CPU.



**+VCCP Decoupling Capacitor  
(Place near CPU)**

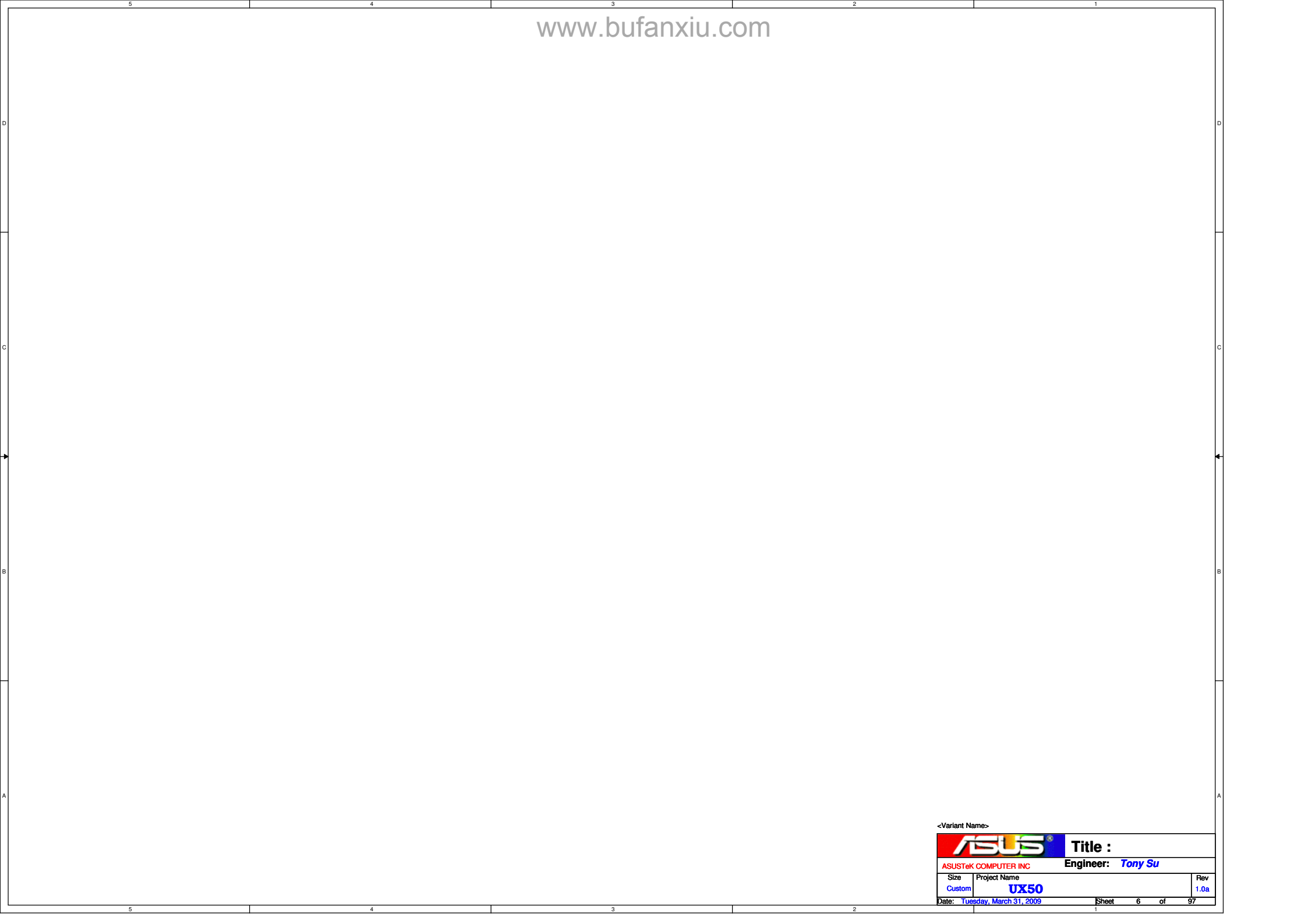


**Decoupling guide from Intel**


V CORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	*12pcs
	270uF	*1pcs
VCCA	0.01uF	*1 pcs
	10uF	*1 pcs

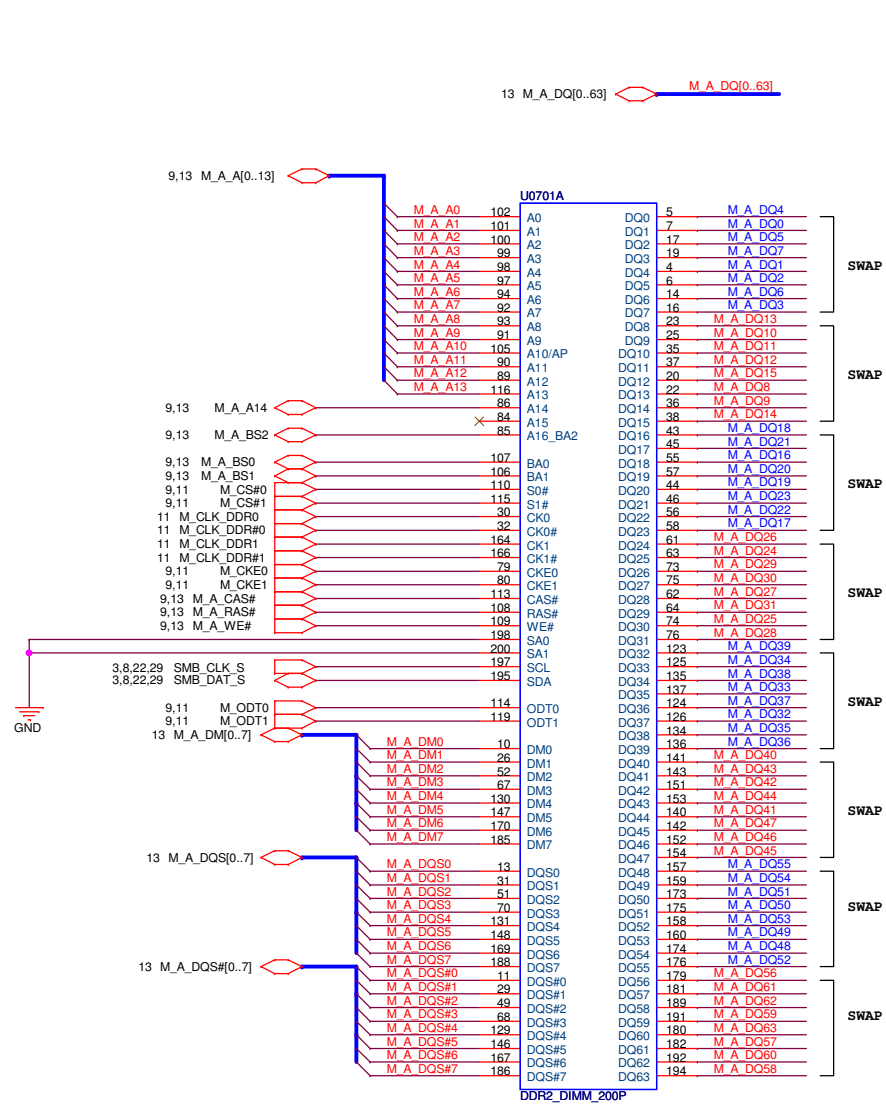
<Variant Name>

<b>ASUS</b>		<b>Title :CPU CAPACITORS</b>
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>
Size Custom	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>	Sheet	5 of 97

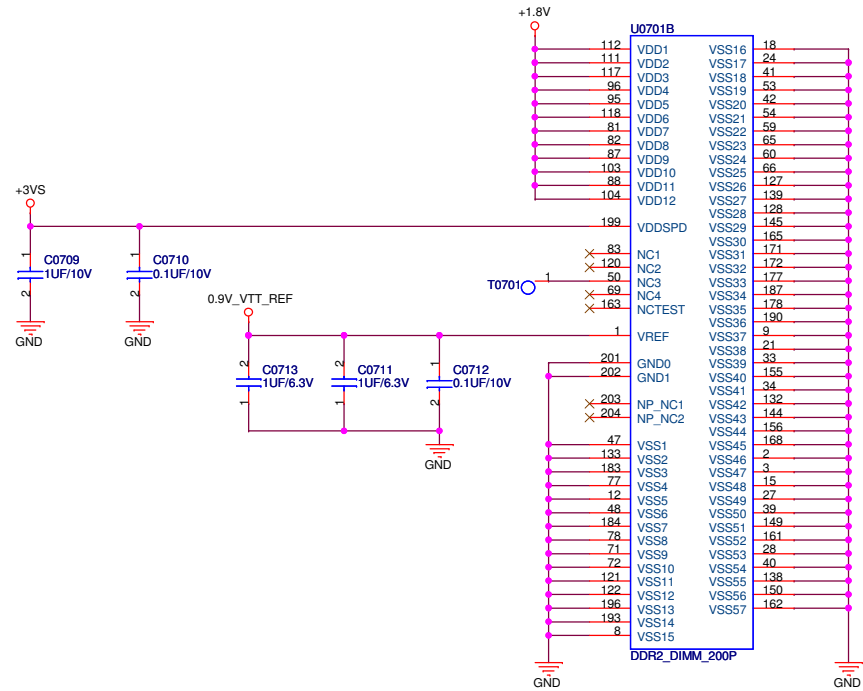
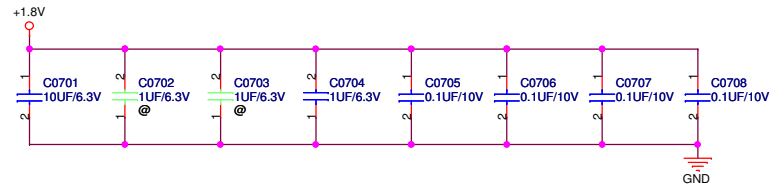


<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer: Tony Su</b>
Size Custom	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 6 of 97

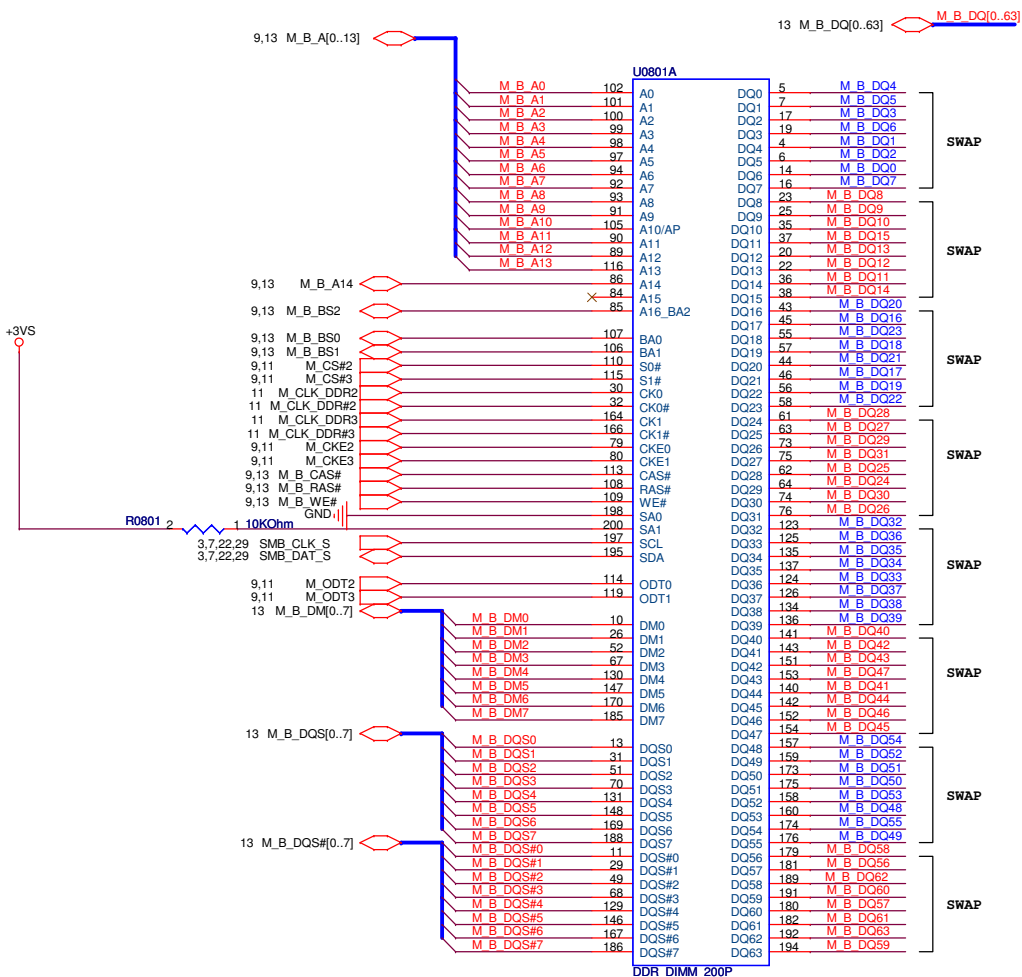


PN : 12G02512200Y (STD Type)

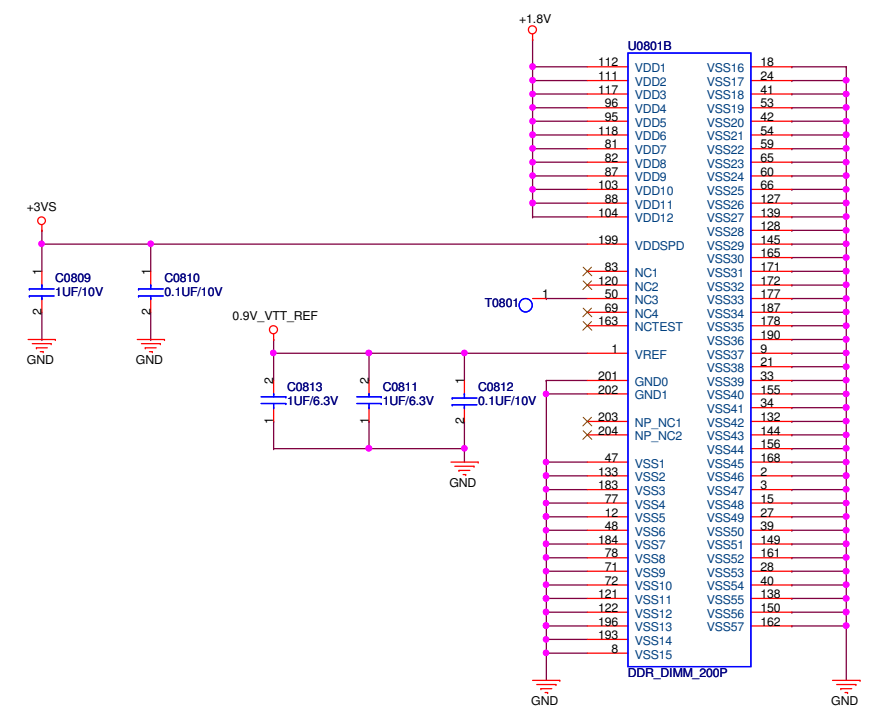
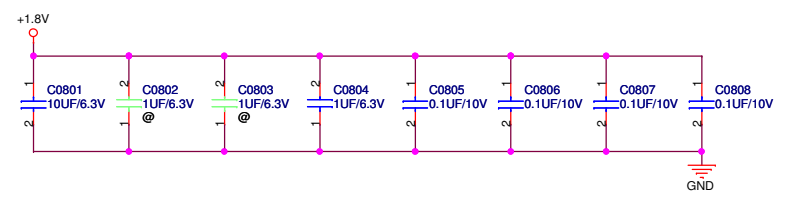


<Variant Name>

<b>ASUS</b>		<b>R2-60 DIMM CHANNEL A</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>	
Size	Project Name		Rev
Custom	<b>UX50</b>		1.0a
Date: Tuesday, March 31, 2009	Sheet	7	of 97



PN: 12G02512200G (REV. Type)



<Variant Name>

**ASUS** Title: **SP-DIMM CHANNEL B**

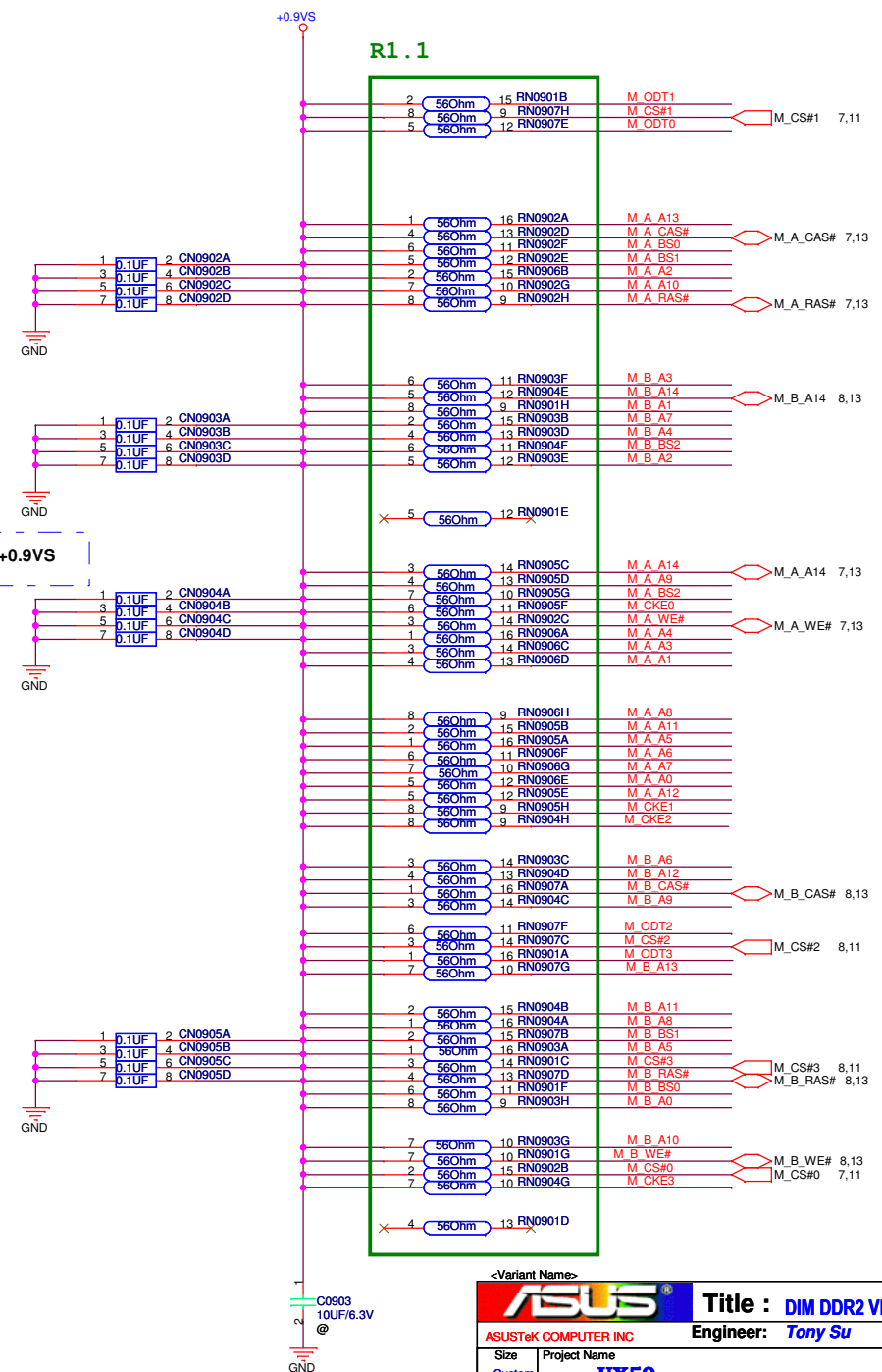
ASUSTek COMPUTER INC Engineer: **Tony Su**

Size	Project Name	Rev
Custom	<b>UX50</b>	1.0a
Date: Tuesday, March 31, 2009	Sheet	8 of 97



- M\_A\_A[0..13] 7,13
- M\_A\_BS[0..2] 7,13
- M\_B\_A[0..13] 8,13
- M\_B\_BS[0..2] 8,13
- M\_CKE[0:3] 7,8,11
- M\_ODT[0:3] 7,8,11

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

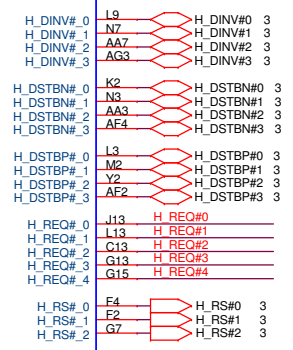
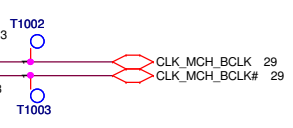
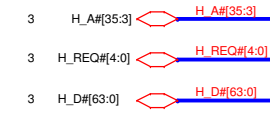
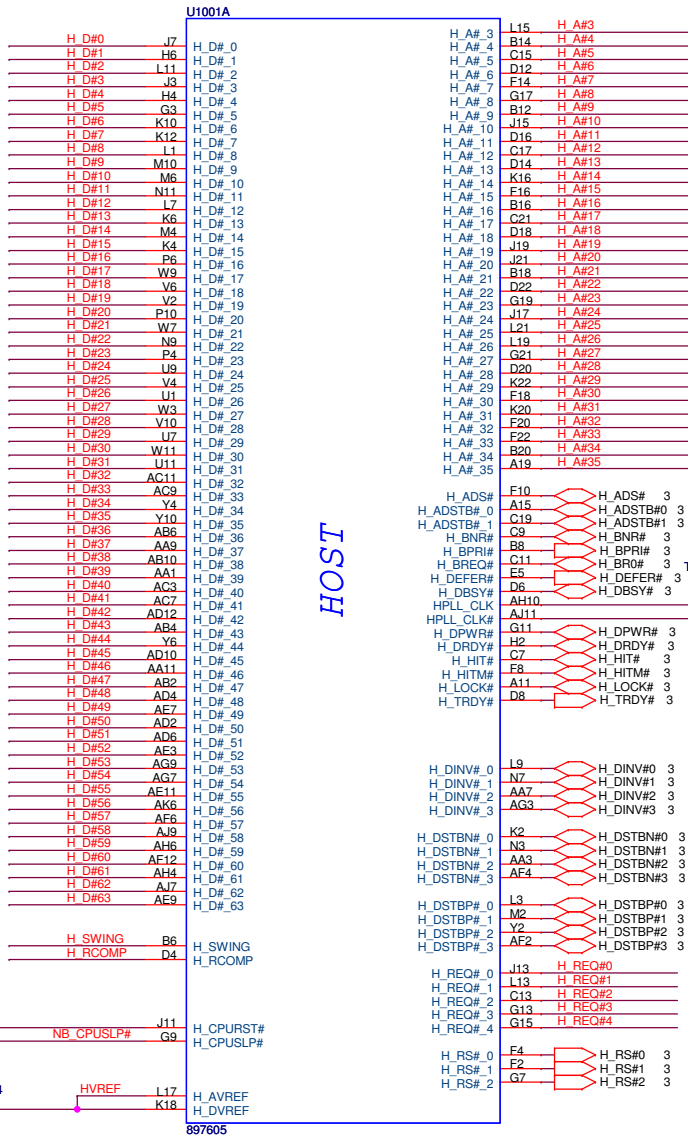
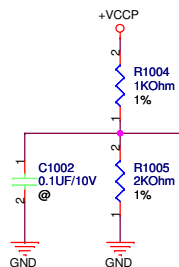
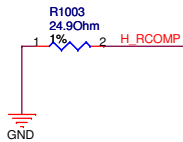
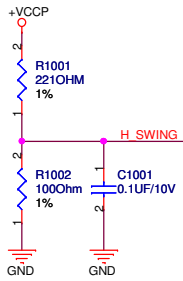


<Variant Name>

**ASUS** Title : DIM DDR2 VREF

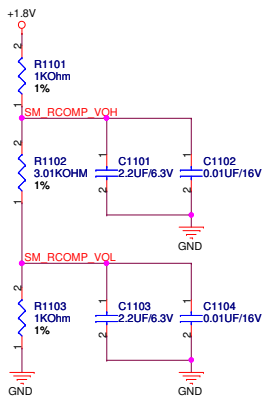
ASUSTeK COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet	9 of 97



<Variant Name>

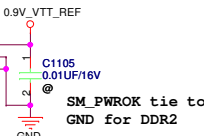
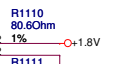
<b>ASUS</b>		<b>Title :NB GS45 HOST</b>	
ASUSTek COMPUTER INC		Engineer: <b>Tony Su</b>	
Size Custom	Project Name <b>UX50</b>		Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet	10	of 97



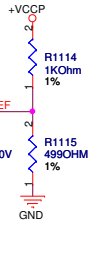
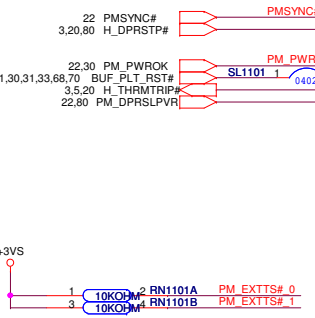
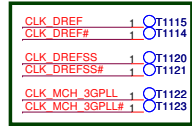
U1001B	RSVD1	RSVD
X J43	RSVD2	
X L43	RSVD3	
X J41	RSVD4	
X L41	RSVD5	
X AN11	RSVD6	
X AM10	RSVD7	
X AK10	RSVD8	
X AL11	RSVD9	
X F12		
X C27	RSVD14	
X D30	RSVD15	
X J8	RSVD17	
X W42	RSVD20	
X BB20	RSVD22	
X BE19	RSVD23	
X BF20	RSVD24	
X BF19	RSVD25	
AN45	ME_JTAG_TCK	
AP44	ME_JTAG_TDI	
AT44	ME_JTAG_TDO	
AN47	ME_JTAG_TMS	

RSVD  
DDR CLK/ CONTROL/COMPENSATION  
CLK  
DMI  
CFM  
GRAPHICS VID  
PM  
MISC  
CN  
HDA

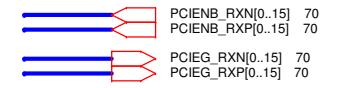
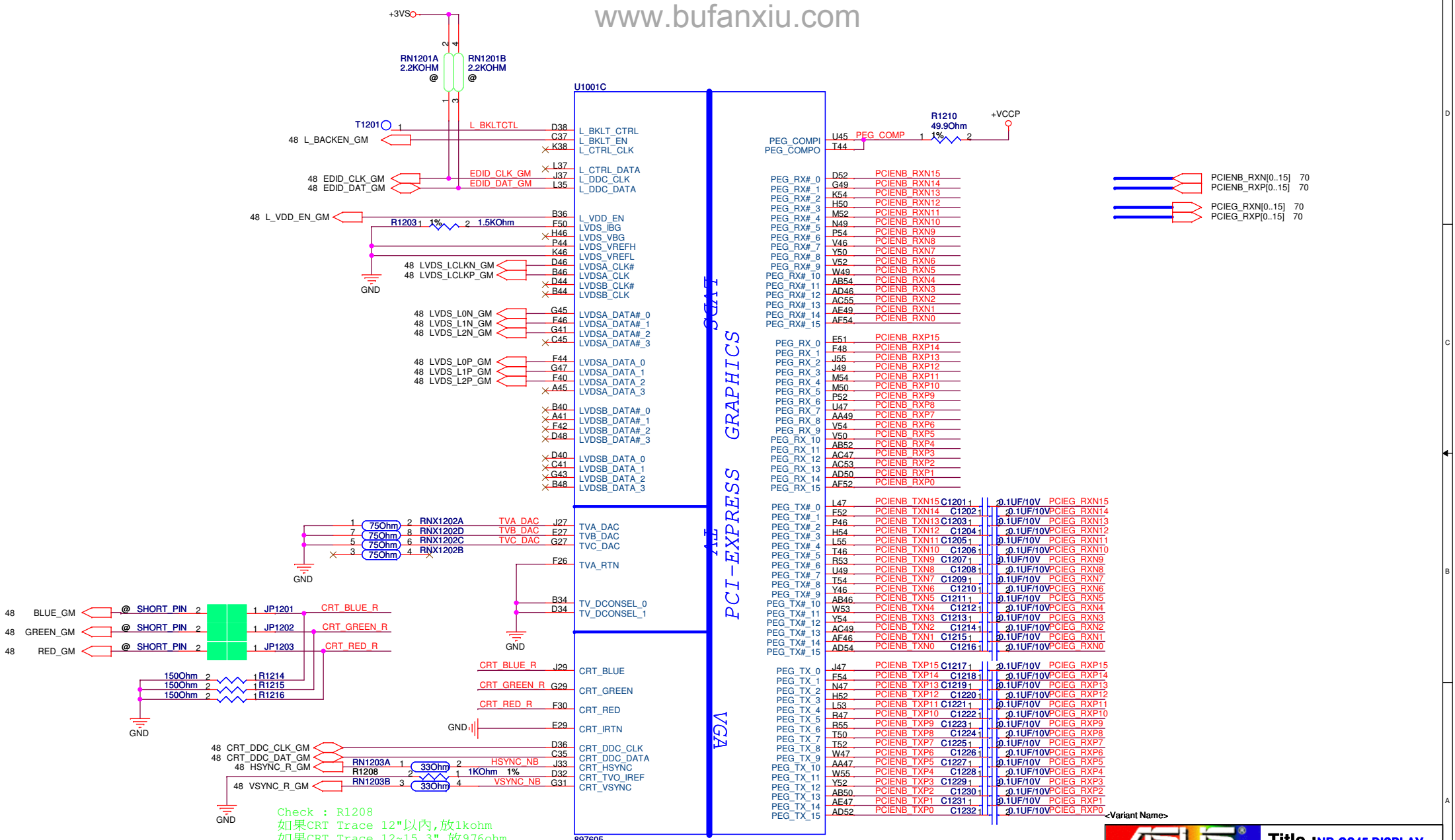
SA_CK_0	BB32	M_CLK_DDR0	7
SA_CK_1	BA25	M_CLK_DDR1	7
SB_CK_0	BA33	M_CLK_DDR2	8
SB_CK_1	BA23	M_CLK_DDR3	8
SA_CK#_0	BA31	M_CLK_DDR#0	7
SA_CK#_1	BC25	M_CLK_DDR#1	7
SB_CK#_0	BC33	M_CLK_DDR#2	8
SB_CK#_1	BB24	M_CLK_DDR#3	8
SA_CKE_0	BC35	M_CKE0	7.9
SA_CKE_1	BE33	M_CKE1	7.9
SB_CKE_0	BE37	M_CKE2	8.9
SB_CKE_1	BC37	M_CKE3	8.9
SA_CS#_0	BK18	M_CS#0	7.9
SA_CS#_1	DK16	M_CS#1	7.9
SB_CS#_0	BE23	M_CS#2	8.9
SB_CS#_1	BC19	M_CS#3	8.9
SA_ODT_0	BJ17	M_ODT0	7.9
SA_ODT_1	BJ19	M_ODT1	7.9
SB_ODT_0	D427	M_ODT2	8.9
SB_ODT_1	BE17	M_ODT3	8.9
SM_RCAMP	BL25	M_RCAMP	1
SM_RCMP#	BK26	M_RCAMP#	1
SM_VREF	BC51		
SM_PWROK	AY37		
SM_REXT	BA37		
SM_DRAMRST#	BA37		
DPLL_REF_CLK	B42	CLK_DREF	29
DPLL_REF_CLK#	D42	CLK_DREF#	29
DPLL_REF_SSCLK	B50	CLK_DREFSS	29
DPLL_REF_SSCLK#	D50	CLK_DREFSS#	29
PEG_CLK	R49	CLK_MCH_3GPLL	29
PEG_CLK#	P50	CLK_MCH_3GPLL#	29
DMI_RXN_0	AG55	DMI_TXN0	21
DMI_RXN_1	AL49	DMI_TXN1	21
DMI_RXN_2	AH54	DMI_TXN2	21
DMI_RXN_3	AL47	DMI_TXN3	21
DMI_RXP_0	AG53	DMI_TXP0	21
DMI_RXP_1	AK50	DMI_TXP1	21
DMI_RXP_2	AH52	DMI_TXP2	21
DMI_RXP_3	AL45	DMI_TXP3	21
DMI_TXN_0	AG49	DMI_RXN0	21
DMI_TXN_1	AJ49	DMI_RXN1	21
DMI_TXN_2	AJ47	DMI_RXN2	21
DMI_TXN_3	AG47	DMI_RXN3	21
DMI_TXP_0	AF50	DMI_RXP0	21
DMI_TXP_1	AH50	DMI_RXP1	21
DMI_TXP_2	AJ45	DMI_RXP2	21
DMI_TXP_3	AG45	DMI_RXP3	21
GFX_VID_0	G33		
GFX_VID_1	G37		
GFX_VID_2	F38		
GFX_VID_3	F36		
GFX_VID_4	G35		
GFX_VR_EN	G39		
CL_CLK	AK52	CL_CLK0	22
CL_DATA	AK54	CL_DATA0	22
CL_PWROK	AW40		
CL_RST#	AL53	CL_RST#0	22
CL_VREF	AL55		
DDPC_CTRLCLK	F34	DDPC_CTRLCLK	1
DDPC_CTRLDATA	F32	DDPC_CTRLDATA	1
SDVO_CTRLCLK	R38		
SDVO_CTRLDATA	A37		
CLKREQ#	C31		
ICH_SYNC#	K42	MCH_SYNC#	22
TSATN#	D10	TSATN#	2
HDA_BCLK	C25		
HDA_RST#	B30		
HDA_SDI	D28		
HDA_SDO	A27		
HDA_SYNC	B28		



For Clock measurement



DG, Checklist: 500ohm  
CRB: 511ohm



Check : R1208  
 如果CRT Trace 12"以内,放1kohm  
 如果CRT Trace 12~15.3",放976ohm

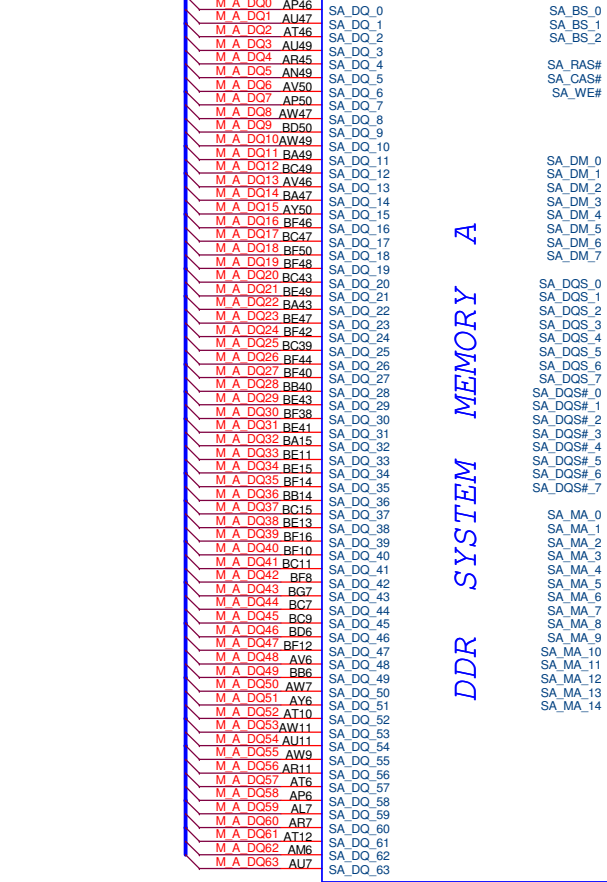
ASUS Title :NB GS45 DISPLAY

ASUSTeK COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
B	UX50	1.0a

Date: Friday, April 03, 2009 Sheet 12 of 97

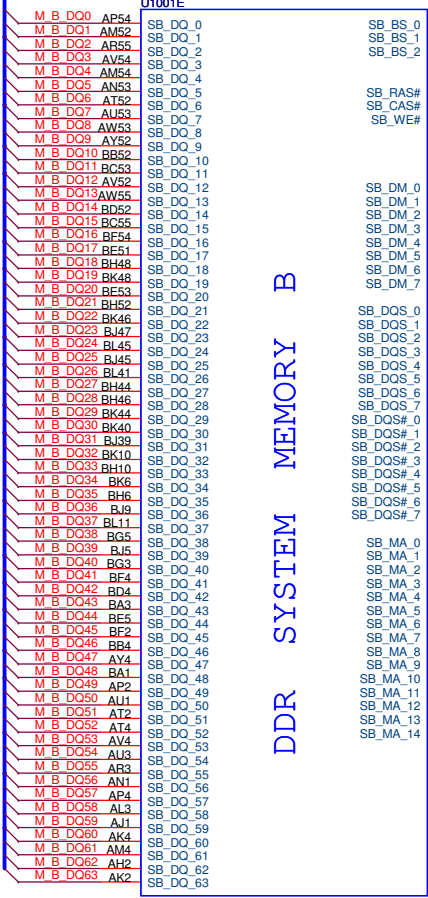
7 M\_A\_DQ[0:63]



DDR SYSTEM MEMORY A

897605

8 M\_B\_DQ[0:63]



DDR SYSTEM MEMORY B

897605

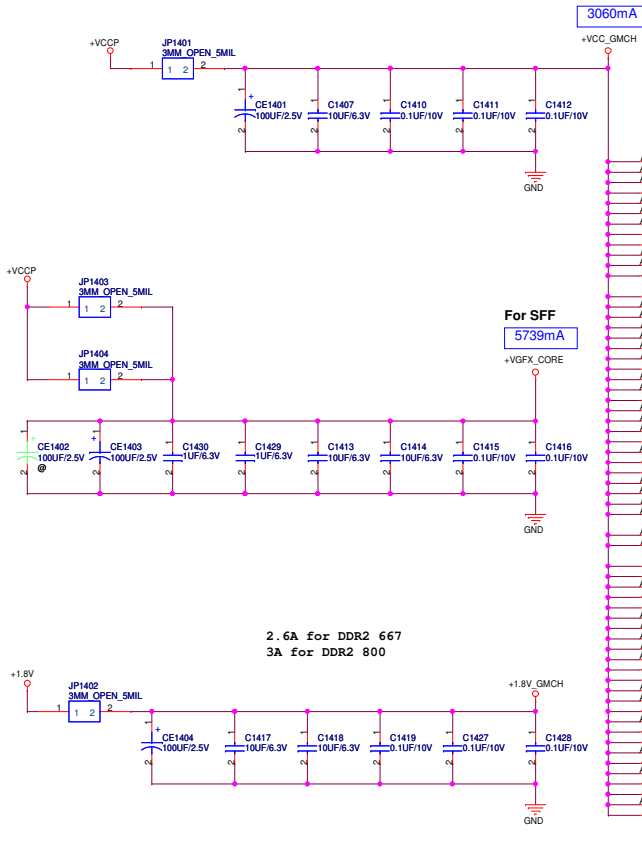
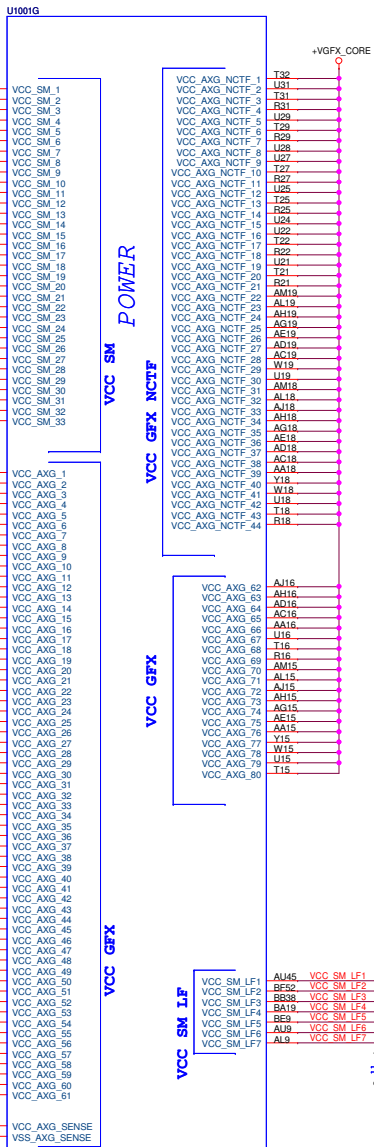
<Variant Name>



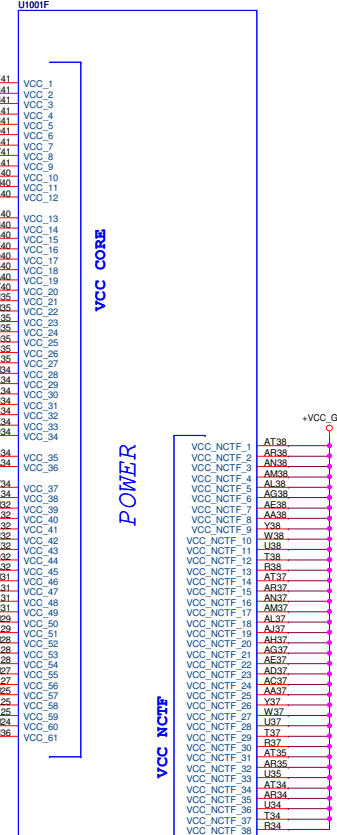
ASUSTeK COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet	13 of 97

2.6A for DDR2 667  
3A for DDR2 800



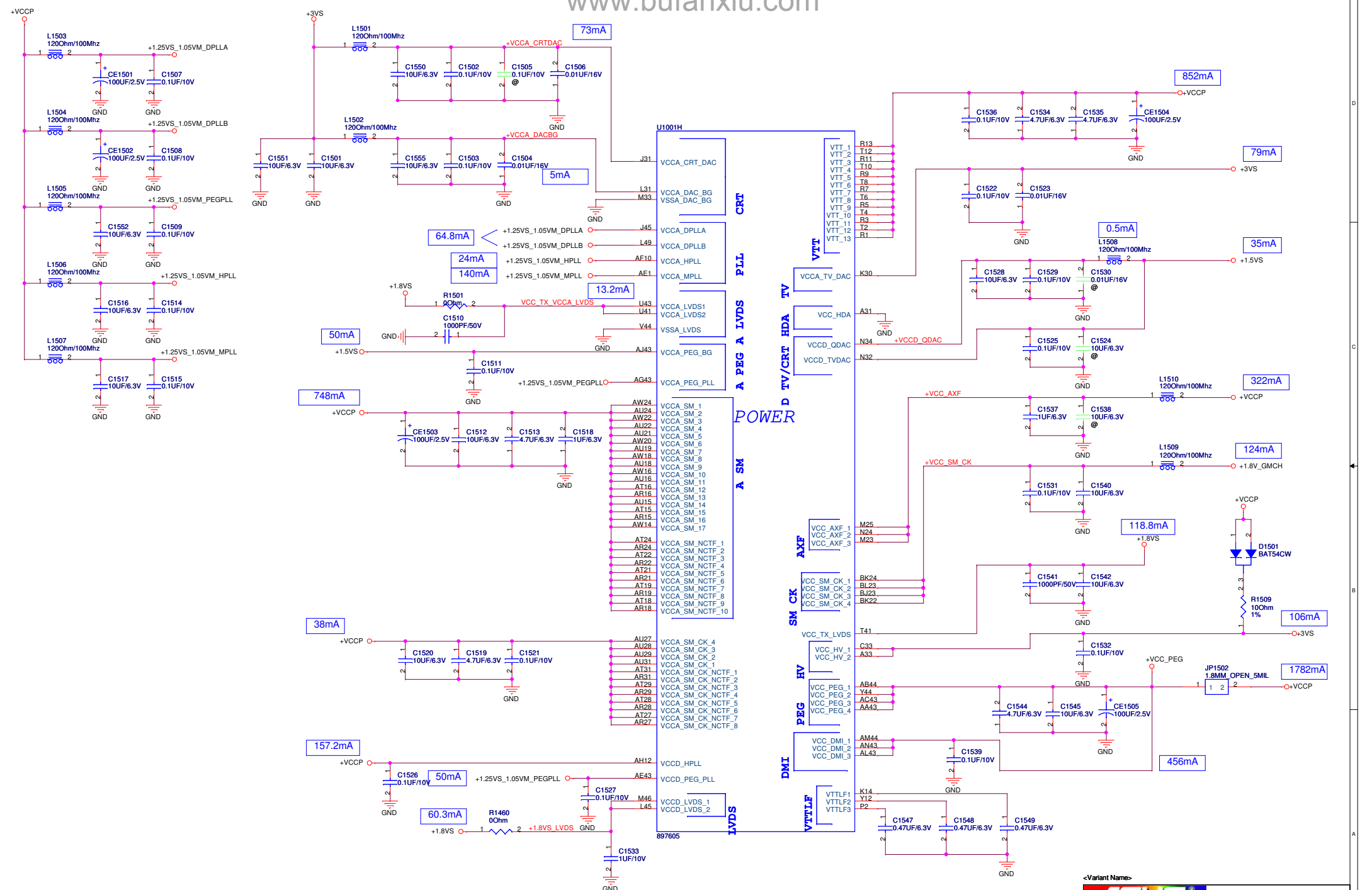
2.6A for DDR2 667  
3A for DDR2 800

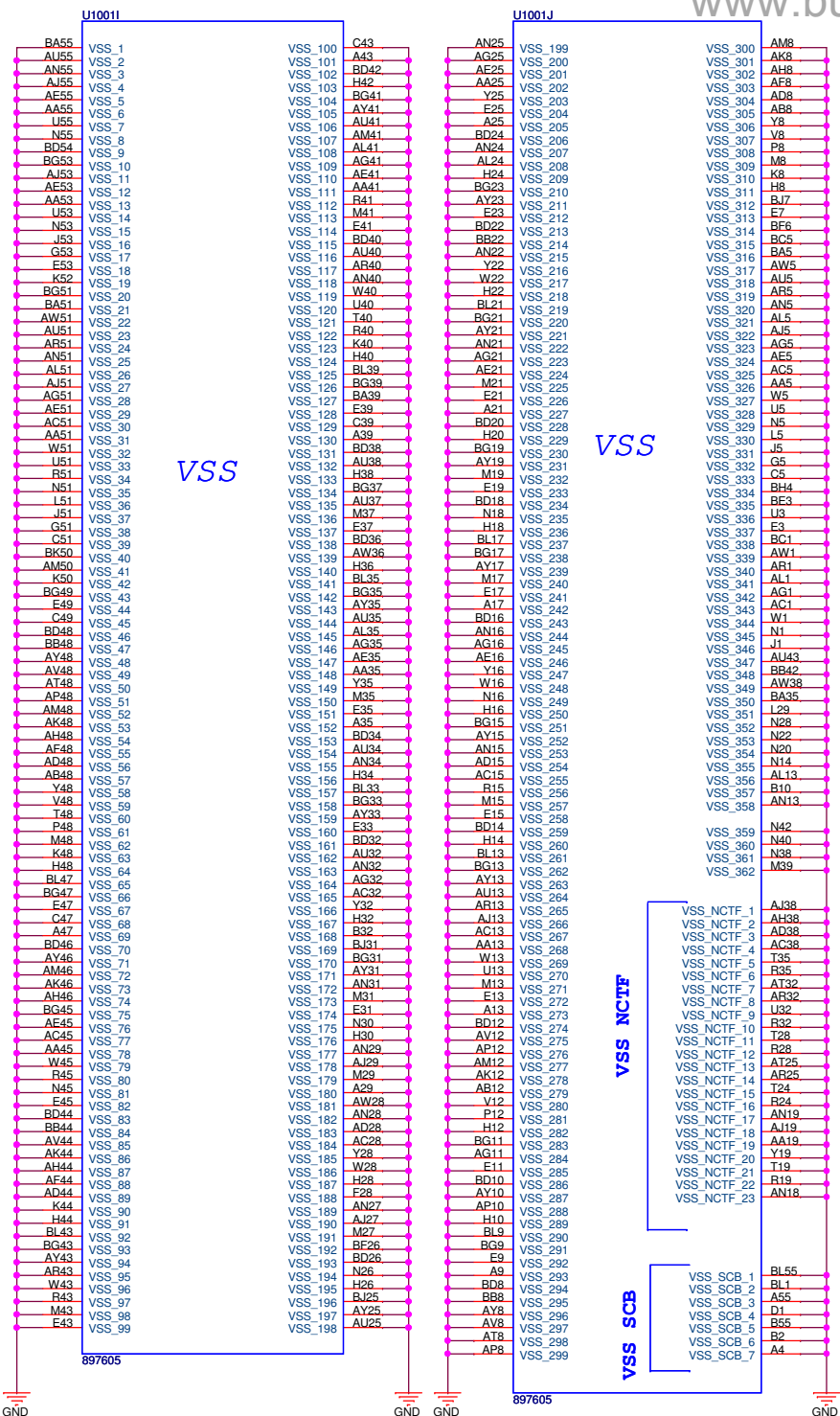


T1401 1 VCC\_AXG\_SENSE AG13 VCC\_AXG\_SENSE  
T1402 1 VSS\_AXG\_SENSE AE13 VSS\_AXG\_SENSE

Route VCC\_AXG\_SENSE and VSS\_AXG\_SENSE differentially.

ASUS Logo  
Title : NB GS45 POWER  
ASUSTeK COMPUTER INC Engineer: Tony Su  
Size C Project Name UX50 Rev 1.0a  
Date: Tuesday, March 31, 2009 Sheet 14 of 97



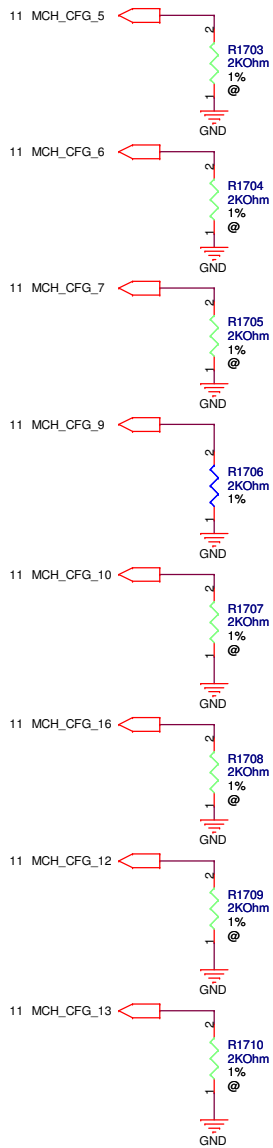


AN25	VSS_199	AM8
AG25	VSS_200	AK8
AE25	VSS_201	AH8
AA25	VSS_202	AF8
Y25	VSS_203	AD8
AY41	VSS_204	AB8
AU41	VSS_205	Y8
AM41	VSS_206	V8
AN24	VSS_207	P8
AL24	VSS_208	M8
AG41	VSS_209	K8
AE41	VSS_210	H8
AA41	VSS_211	B7
R41	VSS_212	E7
E23	VSS_213	BF6
BD22	VSS_214	BC5
BB22	VSS_215	BA5
AY23	VSS_216	AW5
E23	VSS_217	AU5
BD22	VSS_218	AR5
BB22	VSS_219	AN5
AY21	VSS_220	AL5
K40	VSS_221	AJ5
AG21	VSS_222	AG5
AE21	VSS_223	AE5
BL39	VSS_224	AC5
M21	VSS_225	AA5
BA39	VSS_226	W5
E39	VSS_227	U5
A21	VSS_228	N5
BD20	VSS_229	L5
A39	VSS_230	J5
BD38	VSS_231	G5
AU38	VSS_232	C5
H38	VSS_233	B4
BG37	VSS_234	BE3
AL37	VSS_235	U3
M37	VSS_236	E3
E37	VSS_237	BC1
BD36	VSS_238	AW1
AW36	VSS_239	AR1
H36	VSS_240	AL1
BL35	VSS_241	AG1
BG35	VSS_242	AC1
E17	VSS_243	W1
A17	VSS_244	N1
BD16	VSS_245	J1
AN16	VSS_246	AU43
AG16	VSS_247	AB42
AE16	VSS_248	AW38
AY16	VSS_249	BA35
W16	VSS_250	L29
N16	VSS_251	N28
H16	VSS_252	N22
BG15	VSS_253	N20
AY15	VSS_254	N14
AN15	VSS_255	VSS_355
AL15	VSS_256	VSS_356
AC15	VSS_257	VSS_357
R15	VSS_258	VSS_358
M15	VSS_259	N42
E15	VSS_260	N40
BD14	VSS_261	N38
H14	VSS_262	M39
AL13	VSS_263	
BG13	VSS_264	
AY13	VSS_265	AJ38
AU13	VSS_266	AH38
AC32	VSS_267	AD38
Y32	VSS_268	AC38
H32	VSS_269	VSS_NCTF_4
B32	VSS_270	VSS_NCTF_5
BU31	VSS_271	VSS_NCTF_6
W13	VSS_272	VSS_NCTF_7
U13	VSS_273	VSS_NCTF_8
M13	VSS_274	VSS_NCTF_9
E13	VSS_275	VSS_NCTF_10
A13	VSS_276	VSS_NCTF_11
BD12	VSS_277	VSS_NCTF_12
H30	VSS_278	VSS_NCTF_13
AP12	VSS_279	VSS_NCTF_14
AM12	VSS_280	VSS_NCTF_15
AK12	VSS_281	VSS_NCTF_16
AB12	VSS_282	VSS_NCTF_17
V12	VSS_283	VSS_NCTF_18
P12	VSS_284	VSS_NCTF_19
H12	VSS_285	VSS_NCTF_20
BG11	VSS_286	VSS_NCTF_21
AG11	VSS_287	VSS_NCTF_22
E11	VSS_288	VSS_NCTF_23
BD10	VSS_289	
F28	VSS_290	BL55
AY10	VSS_291	BL1
AP10	VSS_292	A55
H10	VSS_293	D1
M27	VSS_294	B55
BG9	VSS_295	B2
E9	VSS_296	A4
BD26	VSS_297	
N26	VSS_298	
H26	VSS_299	
BJ25		
AV8		
ATR		
AP8		

<Variant Name>

<b>ASUS</b>		<b>Title :NB GS45 GND</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>	
Size	Project Name		Rev
Custom	<b>UX50</b>		1.0a
Date: Tuesday, March 31, 2009	Sheet	16	of 97





**CFG5 : DMI STRAP**  
 H = DMI X 4 (Default)  
 L = DMI X 2

**CFG6 : ITPM Host Interface**  
 (Relate to SPL\_MOSI)  
 H = ITPM Disable (Default)  
 L = ITPM enable(Can disable by SW)

**CFG7 : Intel ME Crypto Strap**  
 H = With confidentiality (Default)  
 L = Without confidentiality

**CFG9 : PCIE Graphic Lane Reverse**  
 H = Normal (Default)  
 L = Lanes Reverse

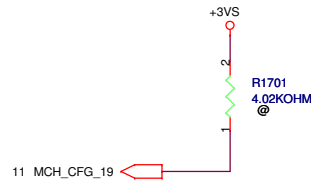
**CFG10 : PCIE Loopback**  
 H = Disable (Default)  
 L = Enable

**CFG16 : FSB Dynamic ODT**  
 H =Enable (Default)  
 L = Disable

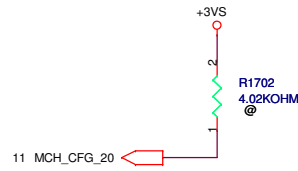
**CFG12 : ALL-Z Mode**  
 H =Disable (Default)  
 L = Enable

**CFG13 : XOR Mode**  
 H = Disable (Default)  
 L = Enable

**CFG [13:12] : XOR/ALL-Z**  
 00 = Reserved  
 01= XOR Mode Enabled  
 10= All-Z Mode Enabled  
 11= Normal Operation (Default)



**CFG19 : DMI Lane Reversal**  
 H =DMI Lane Reversal  
 L = Normal (Default)




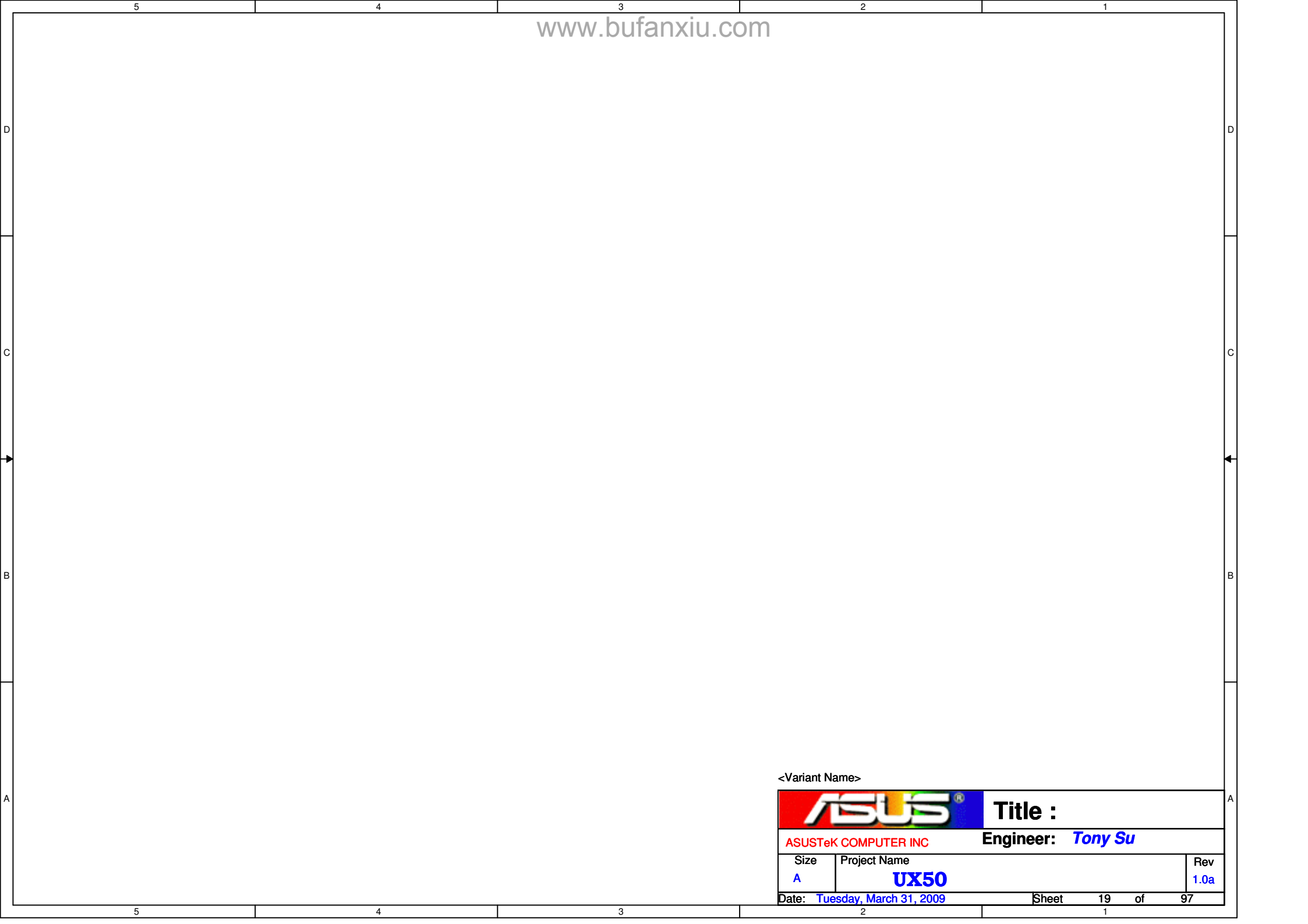
**CFG20 : SDVO/PCIE CONCURRENT MODE**  
 L = Only Digital display port or PCIE is Operational (Default)  
 H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>


<b>ASUS</b>		<b>Title :NB GS45 STRAPPING</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>	
Size Custom	Project Name <b>UX50</b>		Rev 1.0a
Date: Monday, April 06, 2009	Sheet	17	of 97

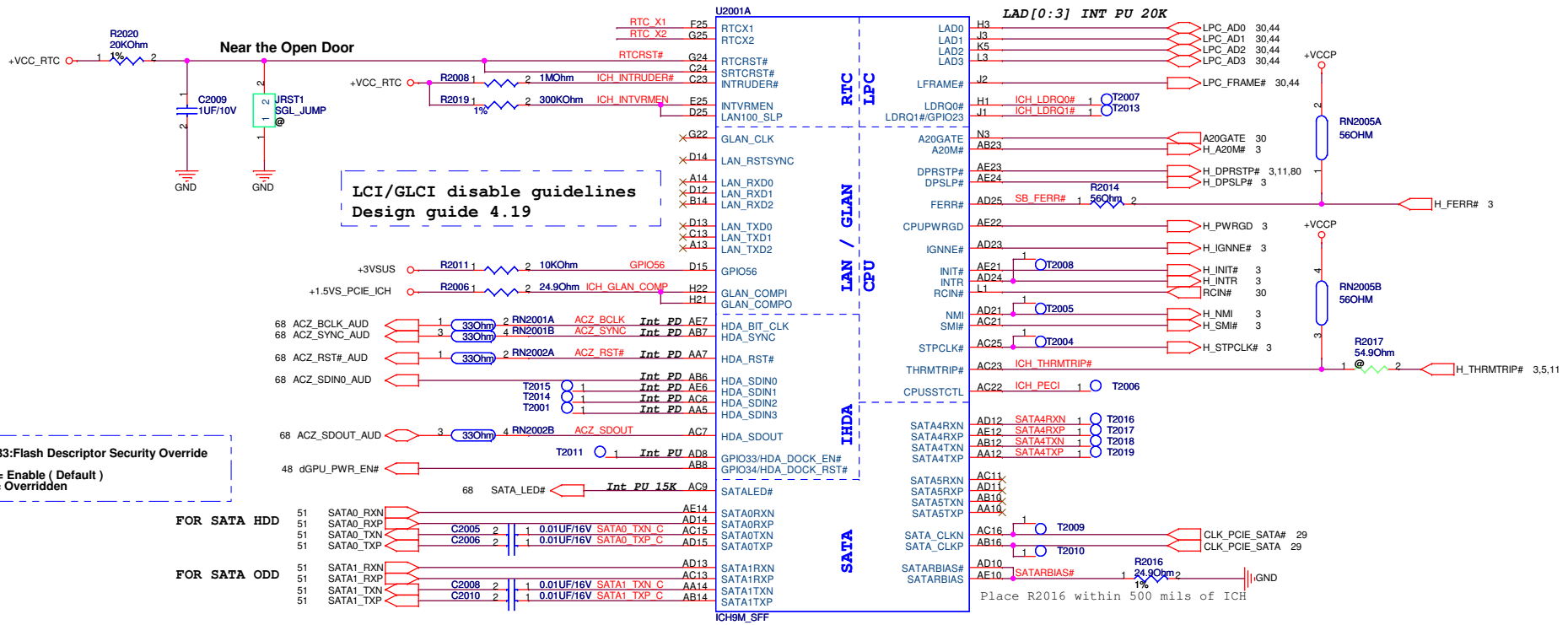
<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size	Project Name	Rev
C	<b>UX50</b>	1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 18 of 97



<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 19 of 97

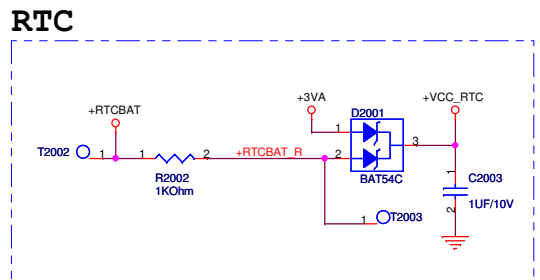
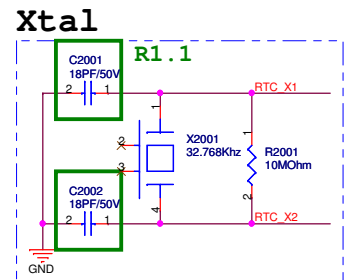


LCI/GLCI disable guidelines  
Design guide 4.19

GPIO33:Flash Descriptor Security Override  
High = Enable ( Default )  
Low = Overridden

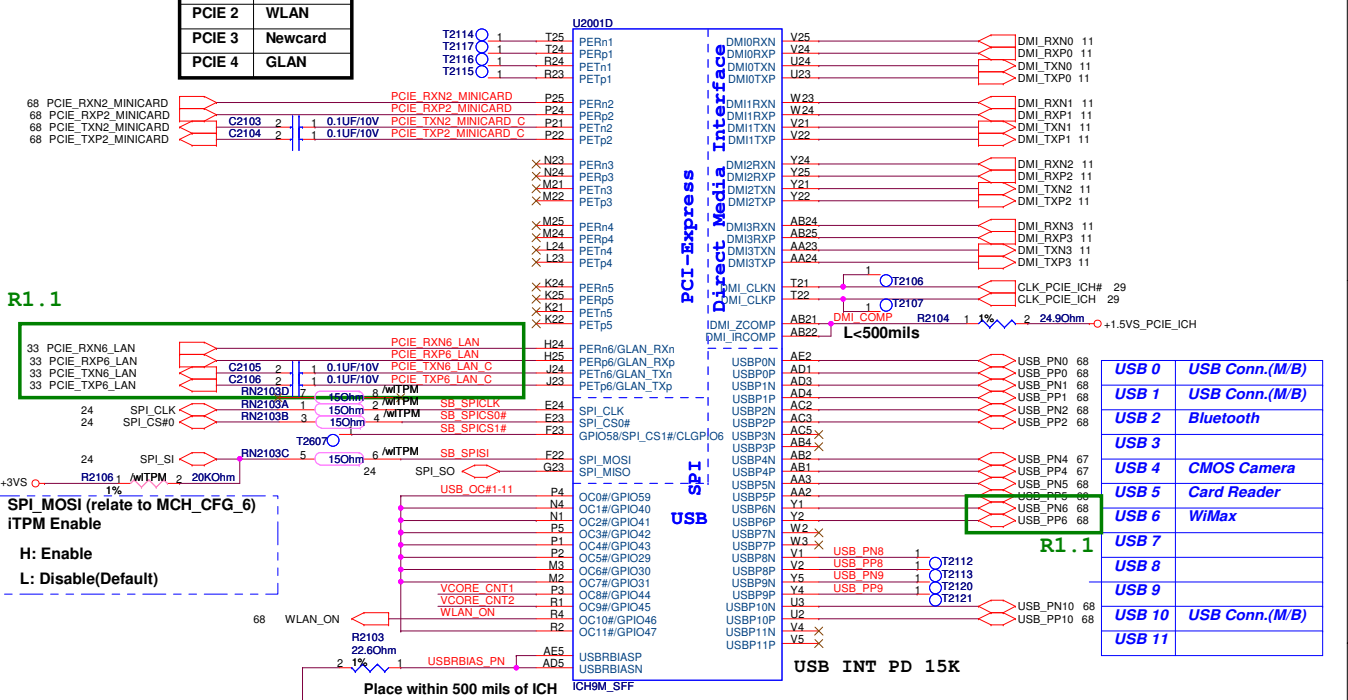
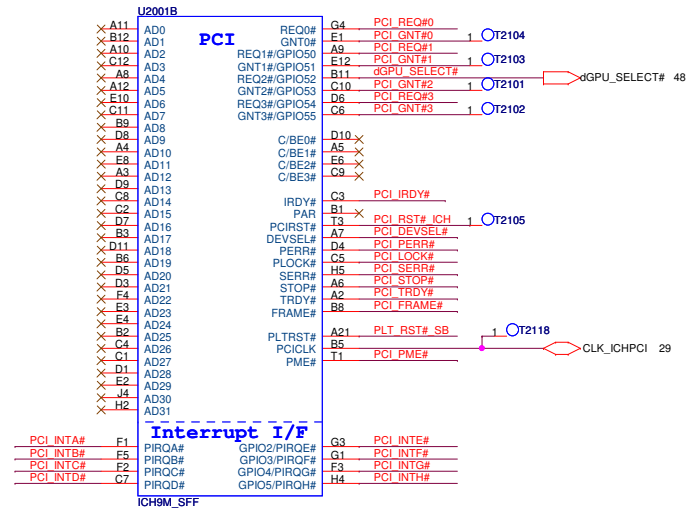
FOR SATA HDD

FOR SATA ODD



[ICH\_TP3, ACZ\_SDOUT] : XOR Chain Entrance Strap  
00 = Reserved  
01 = Enter XOR Chain  
10 = Normal Operation (Default)  
11 = Set PCIe Port Config Bit 1

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	GLAN



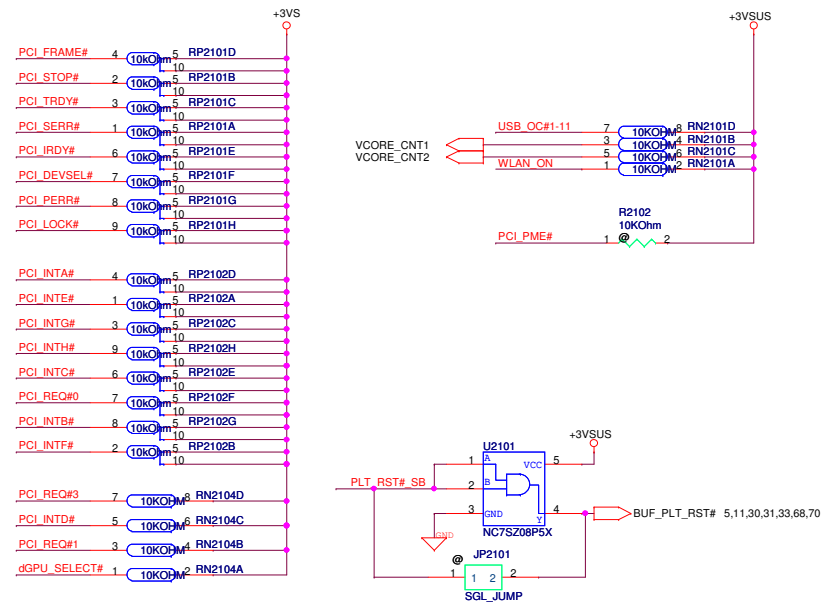
R1.1

SPI\_MOSI (relate to MCH\_CFG\_6)  
 ITPM Enable  
 H: Enable  
 L: Disable(Default)

Place within 500 mils of ICH

ICH9M BIOS select

		GNT#0	SPICS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	



SR Check可否Short過去?

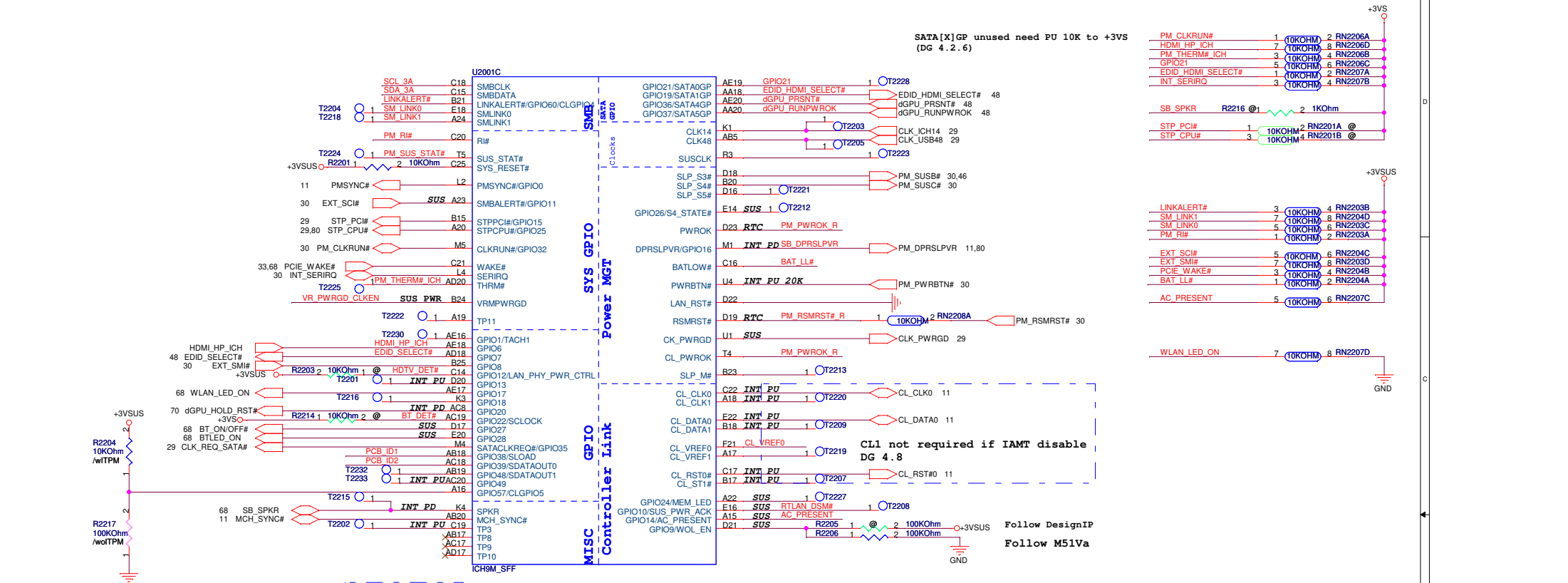
<Variant Name>

**ASUS** Title: SB ICH9M(2)

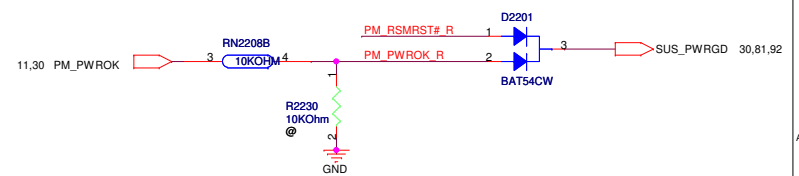
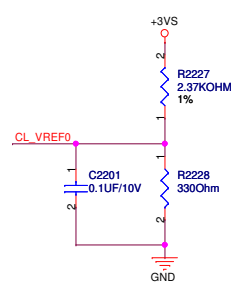
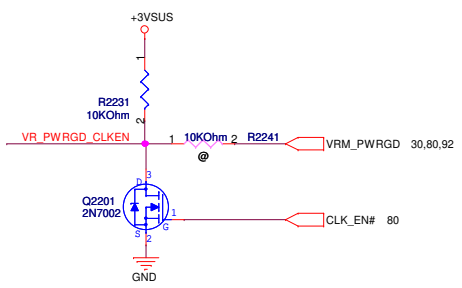
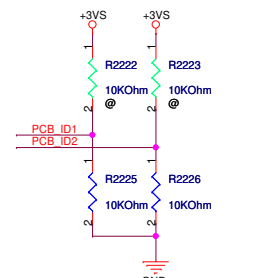
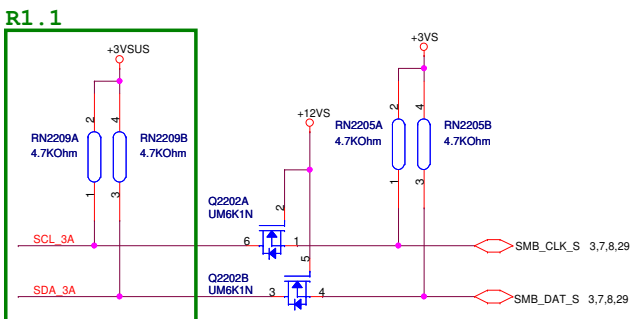
ASUSTek COMPUTER INC Engineer: Tony Su

Size Project Name  
 Custom **UX50**

Date: Tuesday, March 31, 2009 Sheet 21 of 97



**SPKR**  
No Reboot Strap  
Low = Default  
High = No Reboot



PCB ID	GPIO38	GPIO39
MBR1.0	0	0
MBR1.1	0	1
MBR2.0	1	0

**CL\_VREF0 routing rules**  
Width = 12 mils min  
Spacing = 12 mils min  
Break-out = 5 mils on 5 mils for 300 mils max

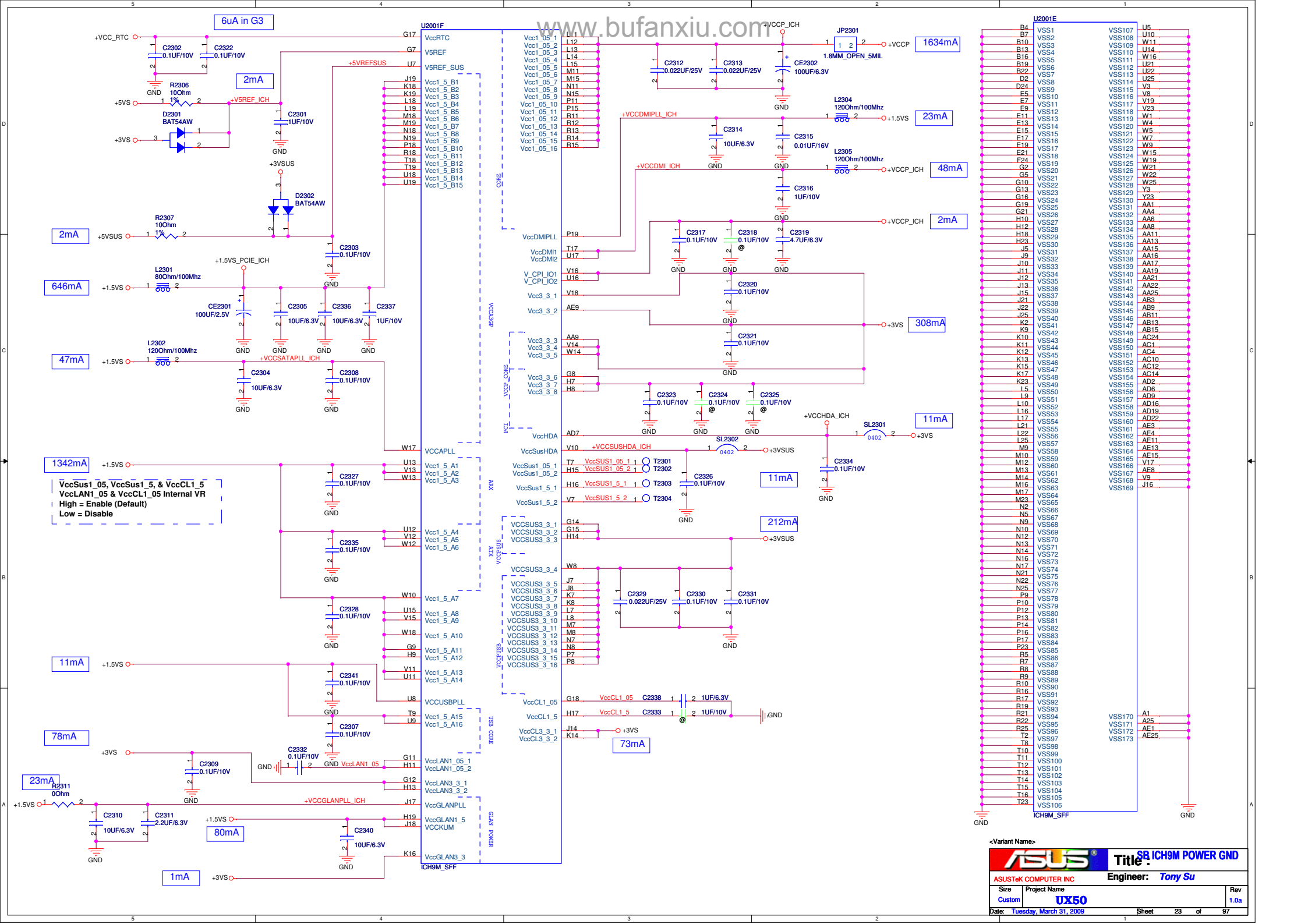
<Variant Name>

**ASUS** Title: **SB ICH9M GPIO PMGT**

ASUSTek COMPUTER INC Engineer: **Tony Su**

Size	Project Name	Rev
Custom	<b>UX50</b>	1.0a

Date: Monday, April 06, 2009 Sheet 22 of 97



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6uA in G3

2mA

2mA

646mA

47mA

1342mA

11mA

78mA

23mA

1mA

1634mA

23mA

48mA

2mA

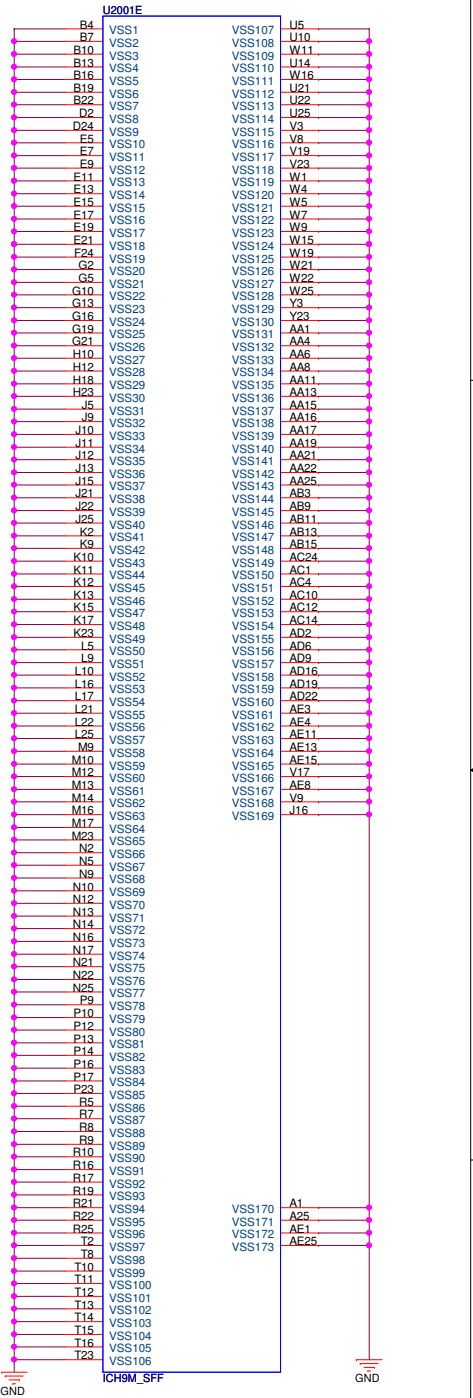
308mA

11mA

11mA

212mA

73mA



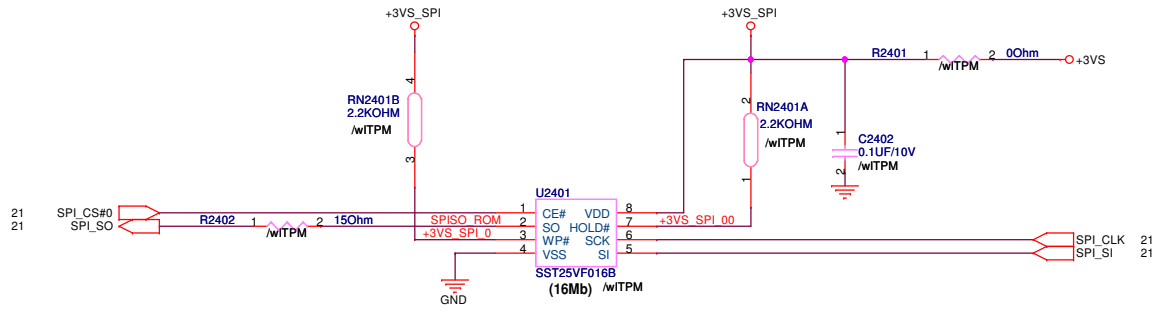
<Variant Name>

**ASUS** Title: **S8 ICH9M POWER GND**

ASUSTeK COMPUTER INC Engineer: **Tony Su**


Size	Project Name	Rev
Custom	<b>UX50</b>	1.0a

Date: **Tuesday, March 31, 2009** Sheet **23** of **97**

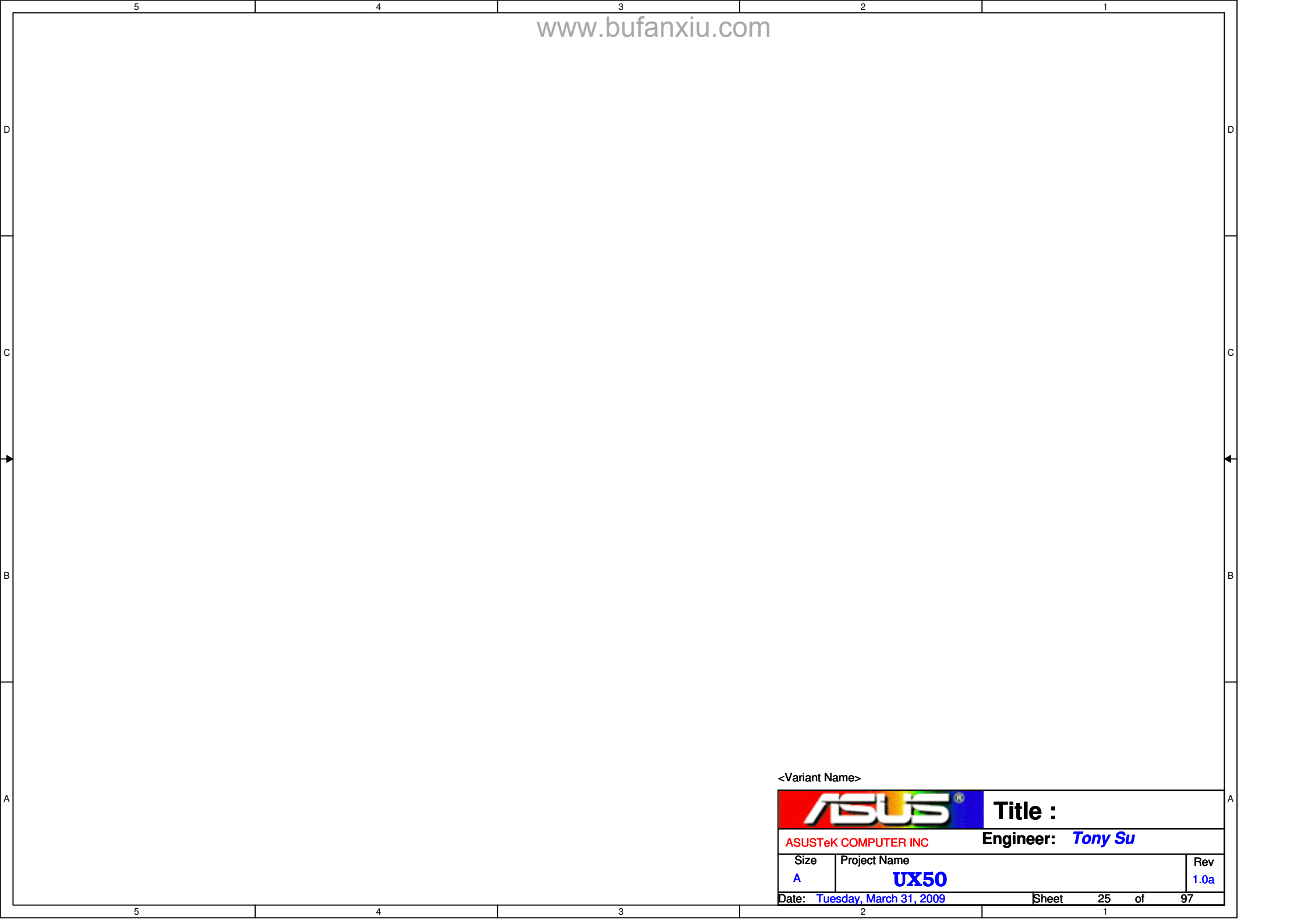


FOR iTPM


<Variant Name>

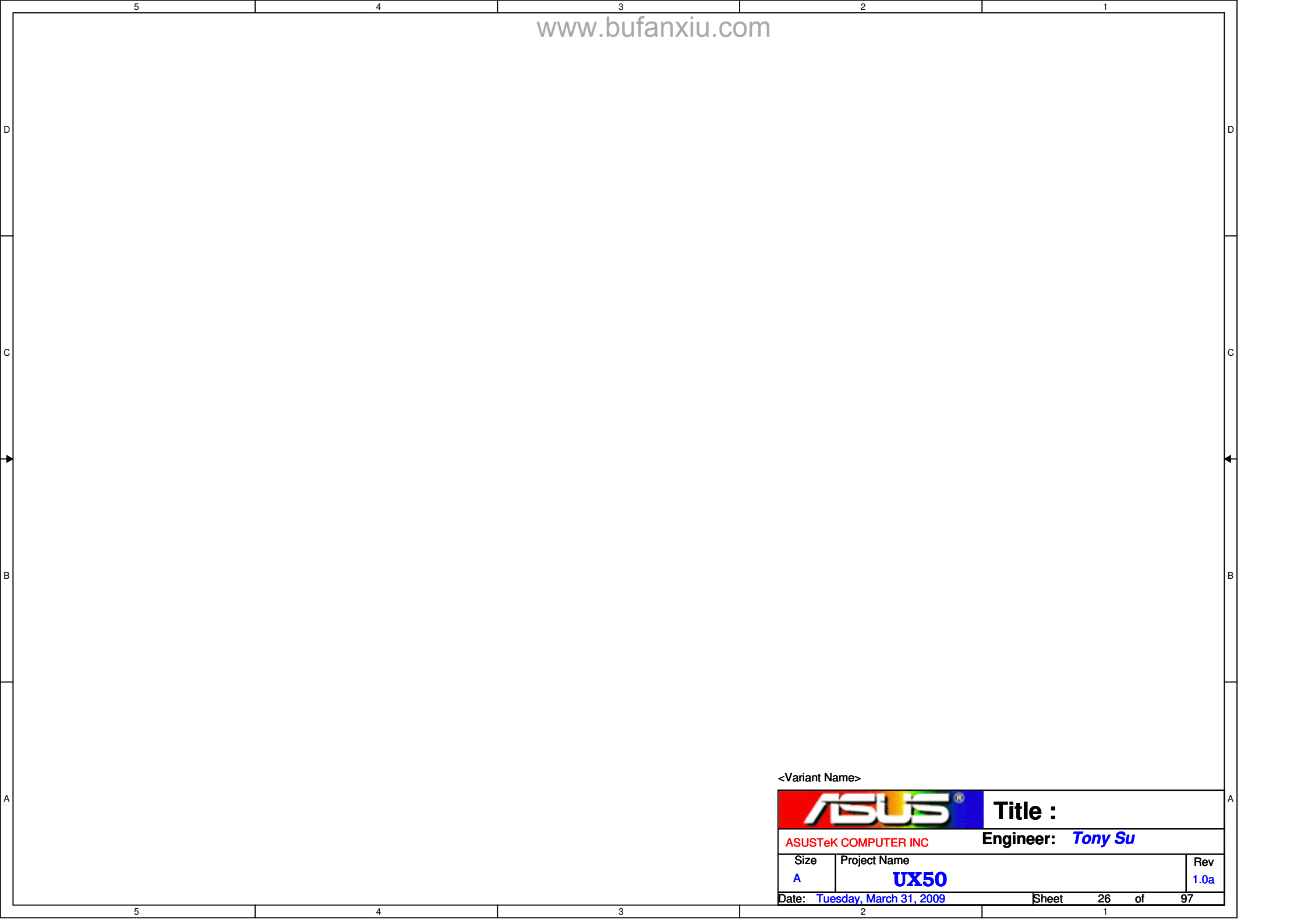
		<b>SB ICH9M SPI ROM &amp; HDPC</b>	
		<b>Title :</b>	
ASUSTeK COMPUTER INC		<b>Engineer: Tony Su</b>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0a	
Date:	Tuesday, March 31, 2009	Sheet	24 of 97






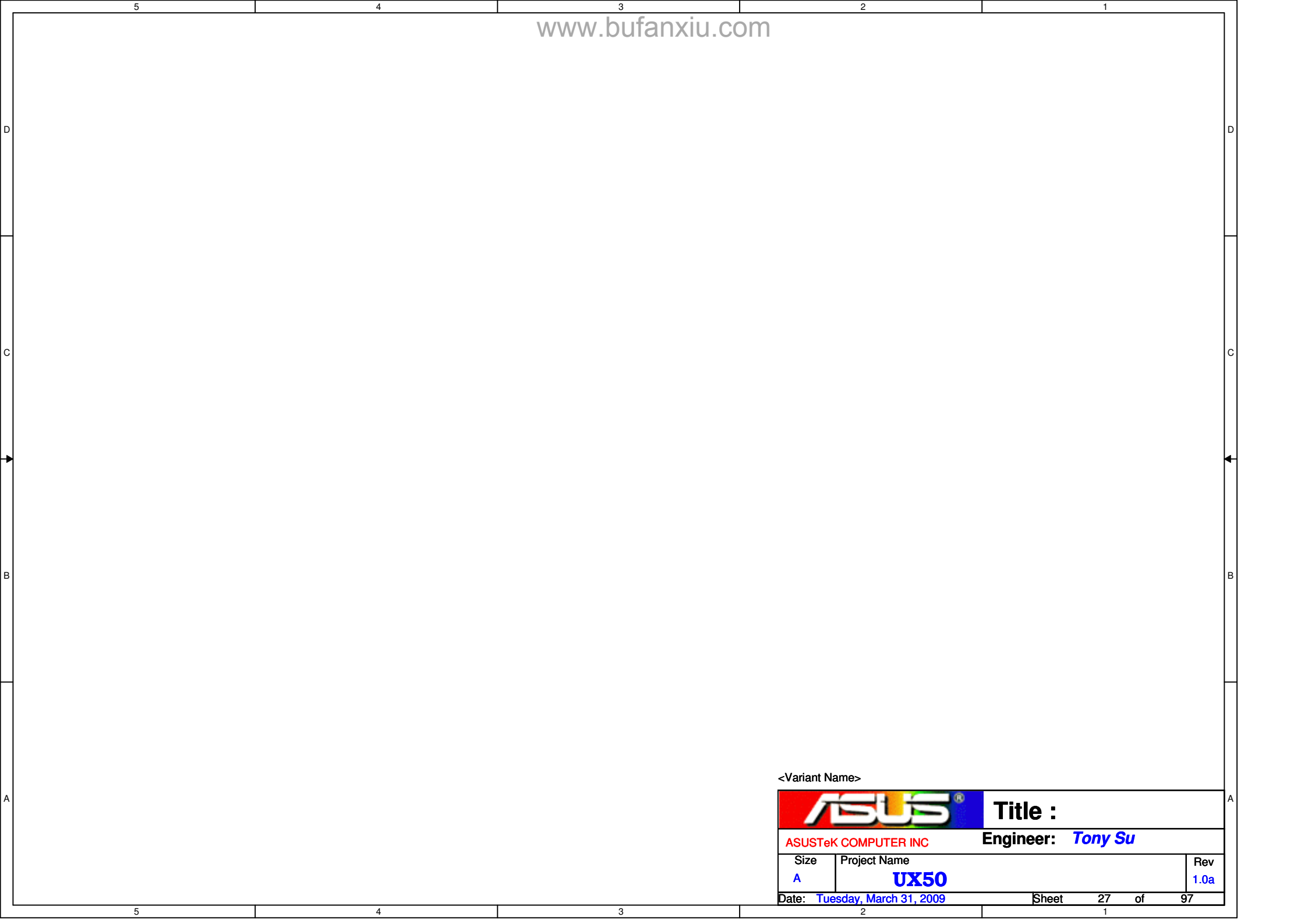
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		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 25 of 97




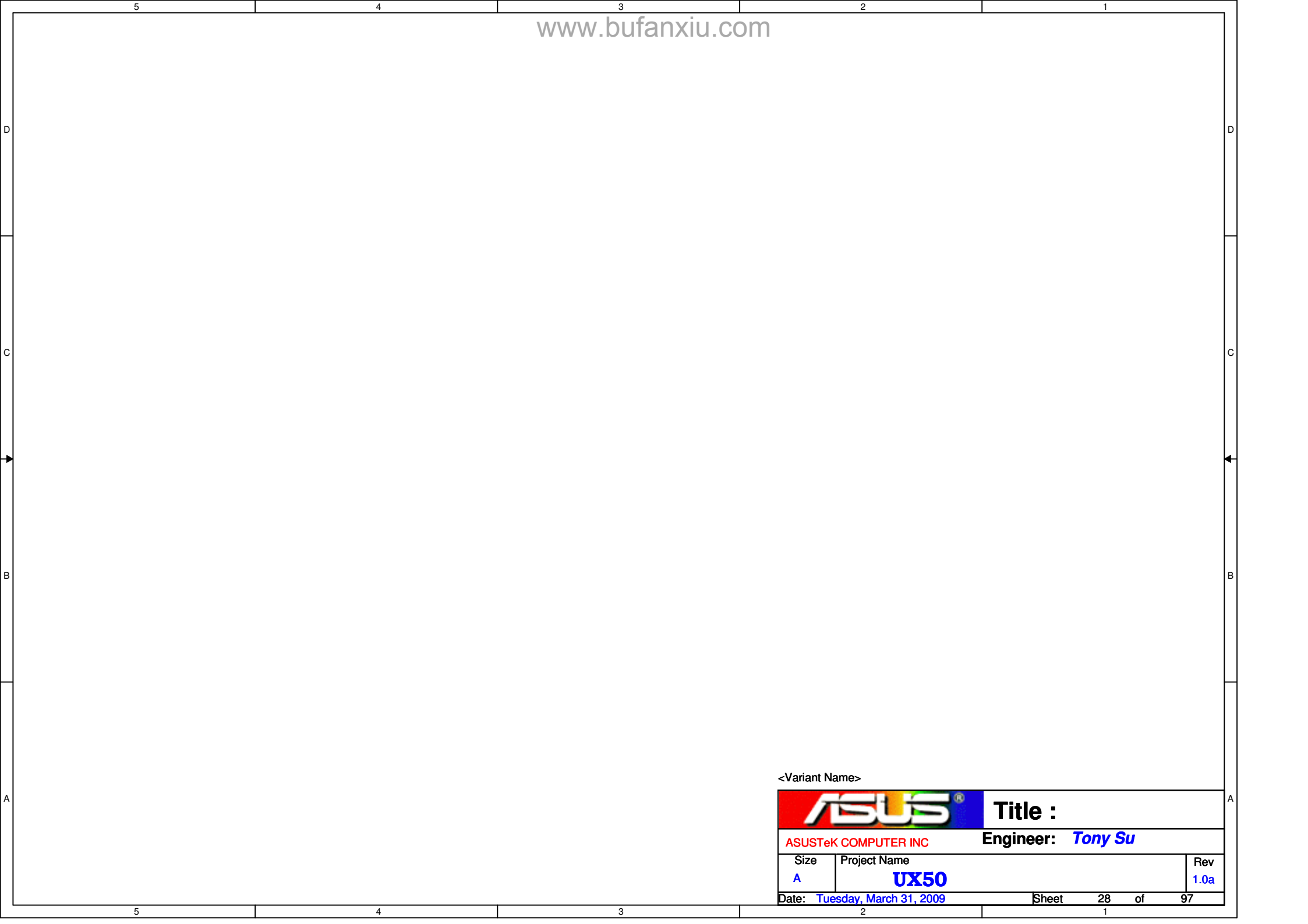
<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 26 of 97




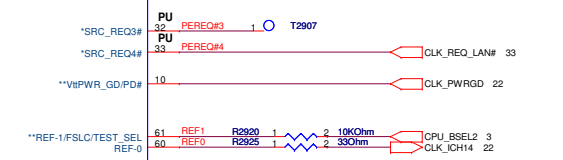
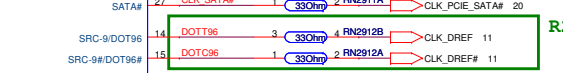
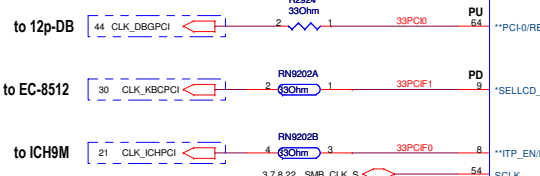
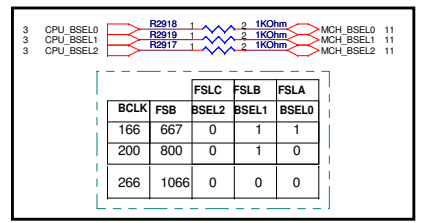
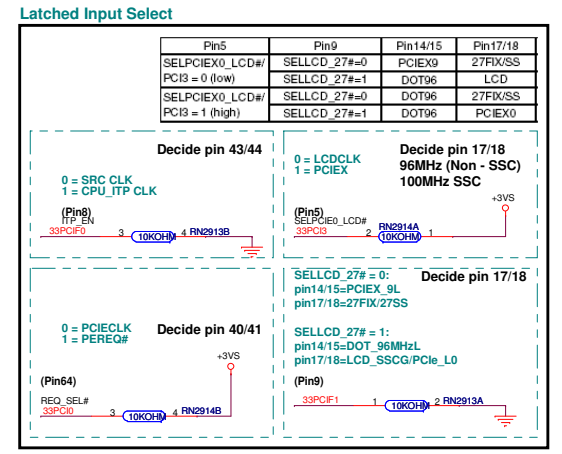
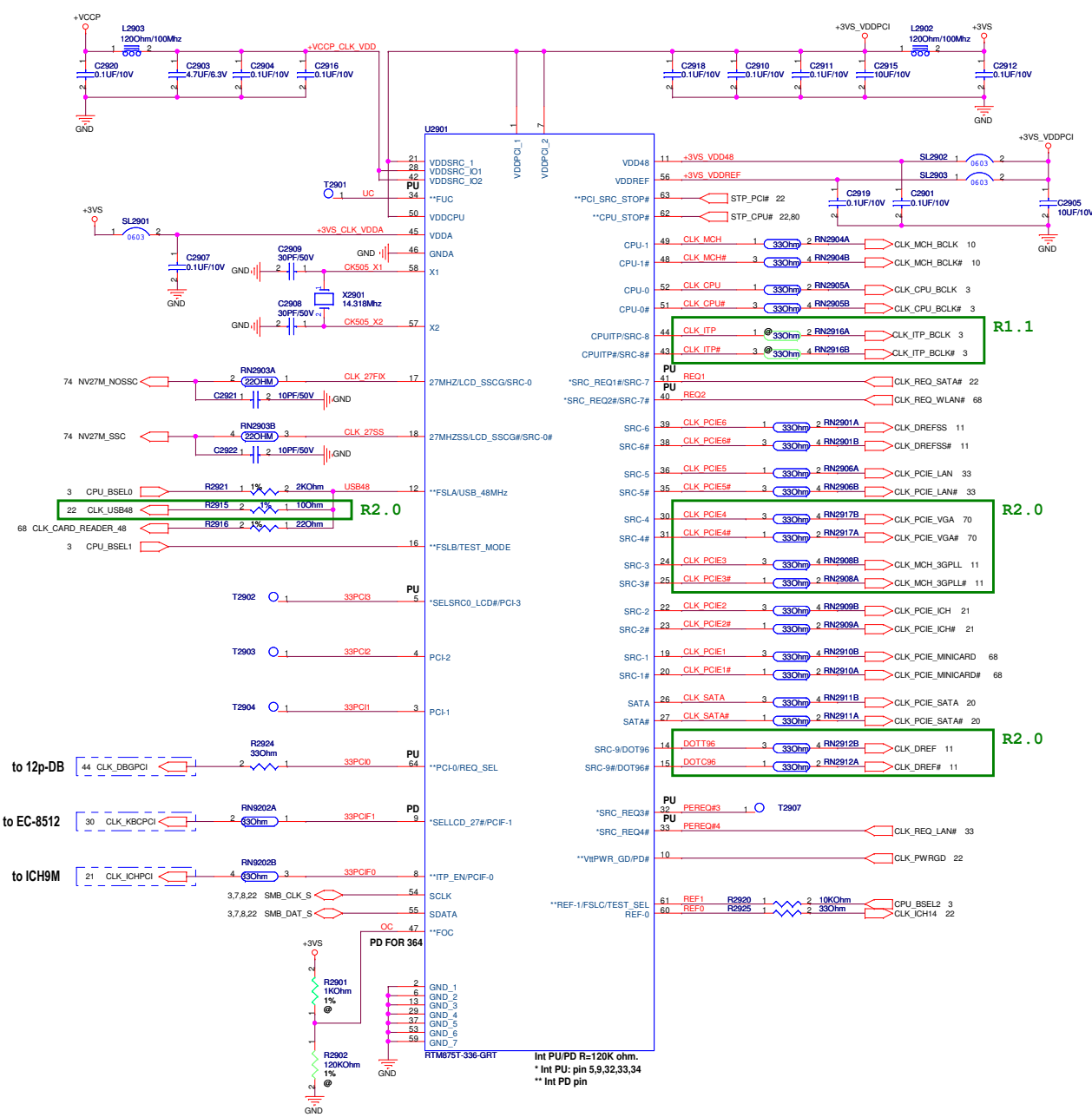
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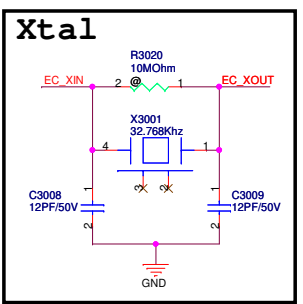
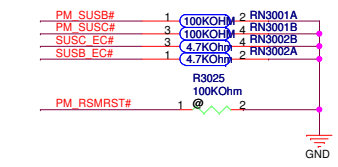
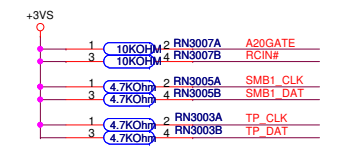
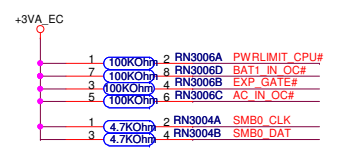
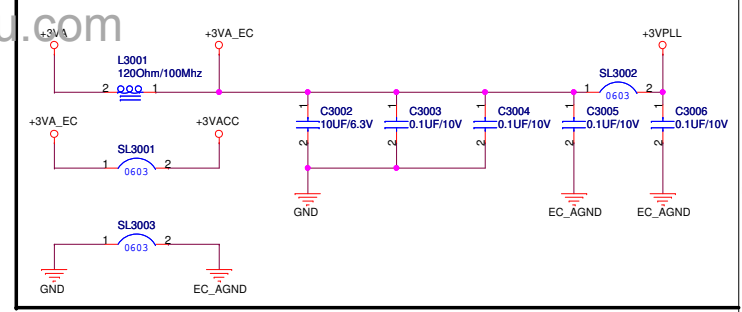
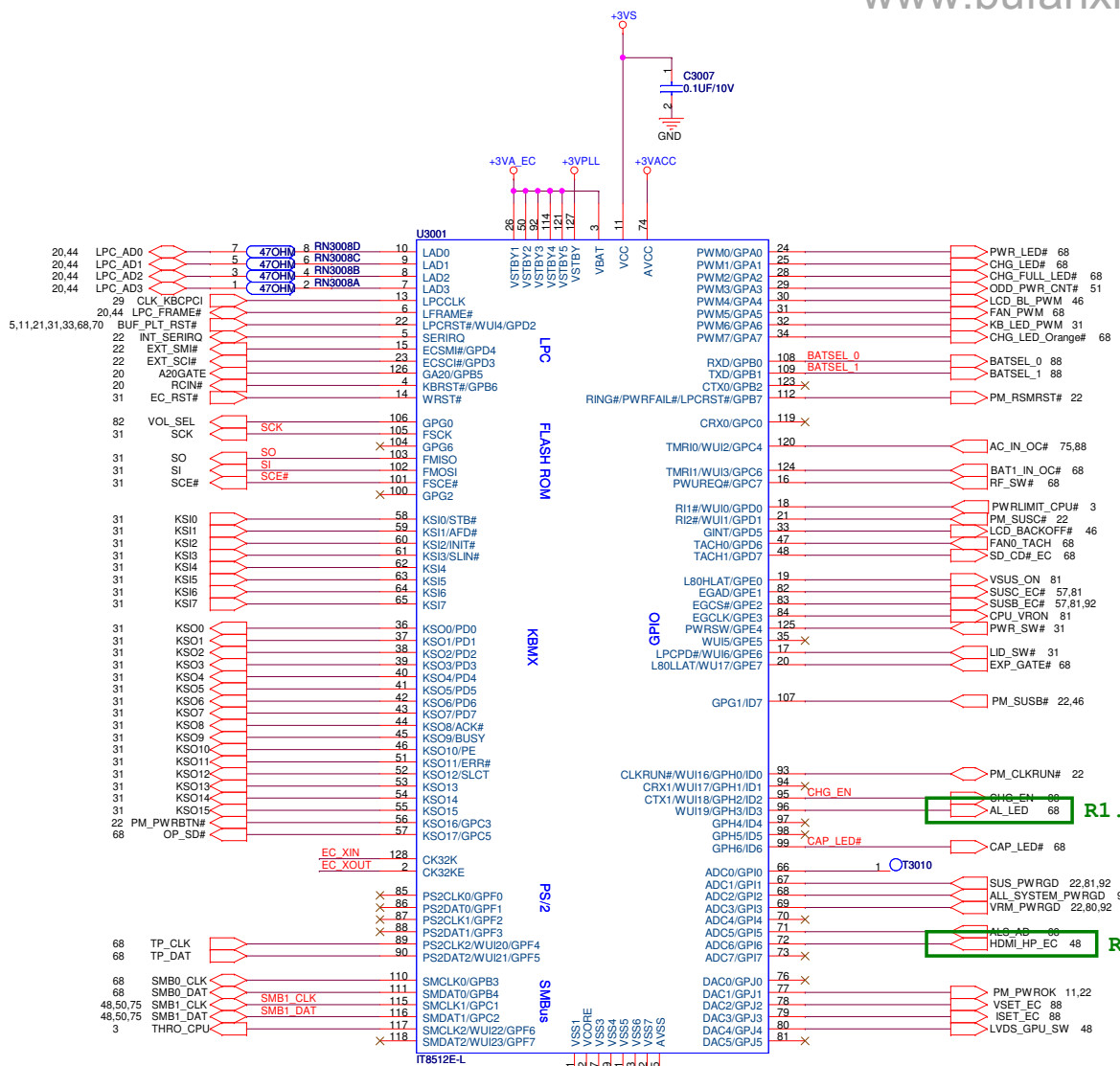
		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 27 of 97



<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 28 of 97





R1.1

R2.0

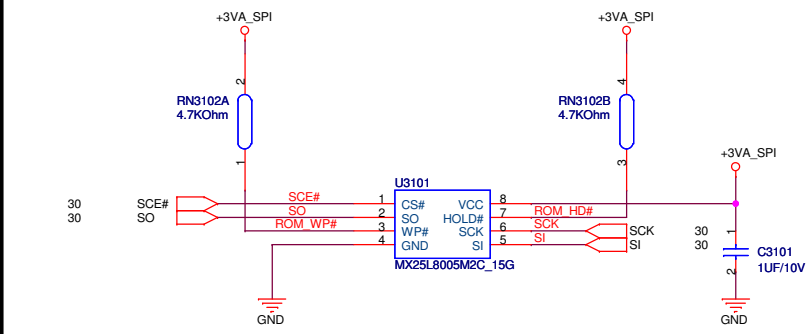
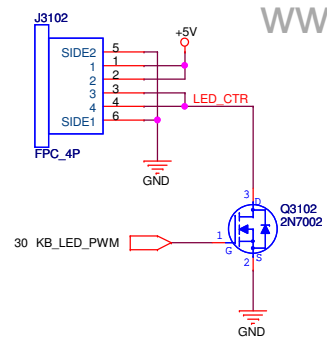
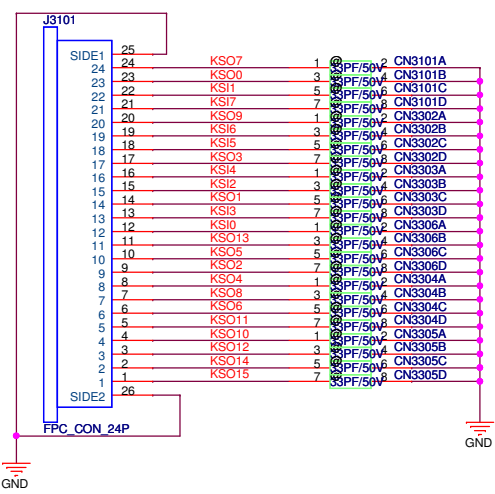
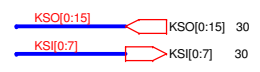
<Variant Name>

**ASUS** Title: **KBC ITE8512**  
 ASUSTeK COMPUTER INC Engineer: **Tony Su**

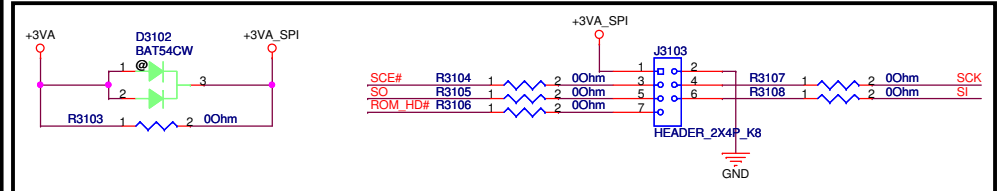
Size	Project Name	Rev
Custom	<b>UX50</b>	1.0a
Date: Wednesday, April 01, 2009	Sheet	30 of 97

# Internal Keyboard

www.8mb.com SPI ROM

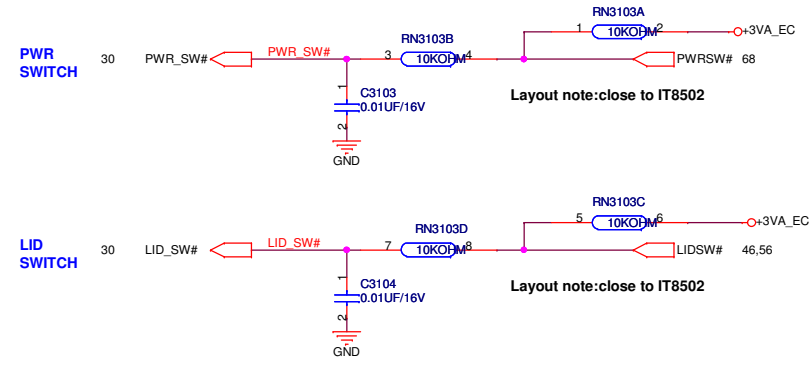
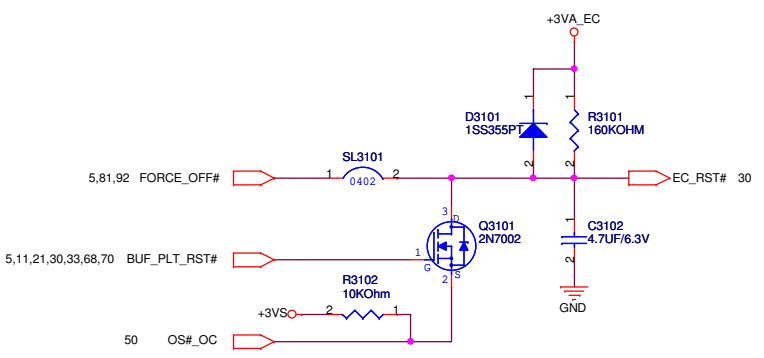


## For SPI Flash Debug



# EC RST


# For Switch



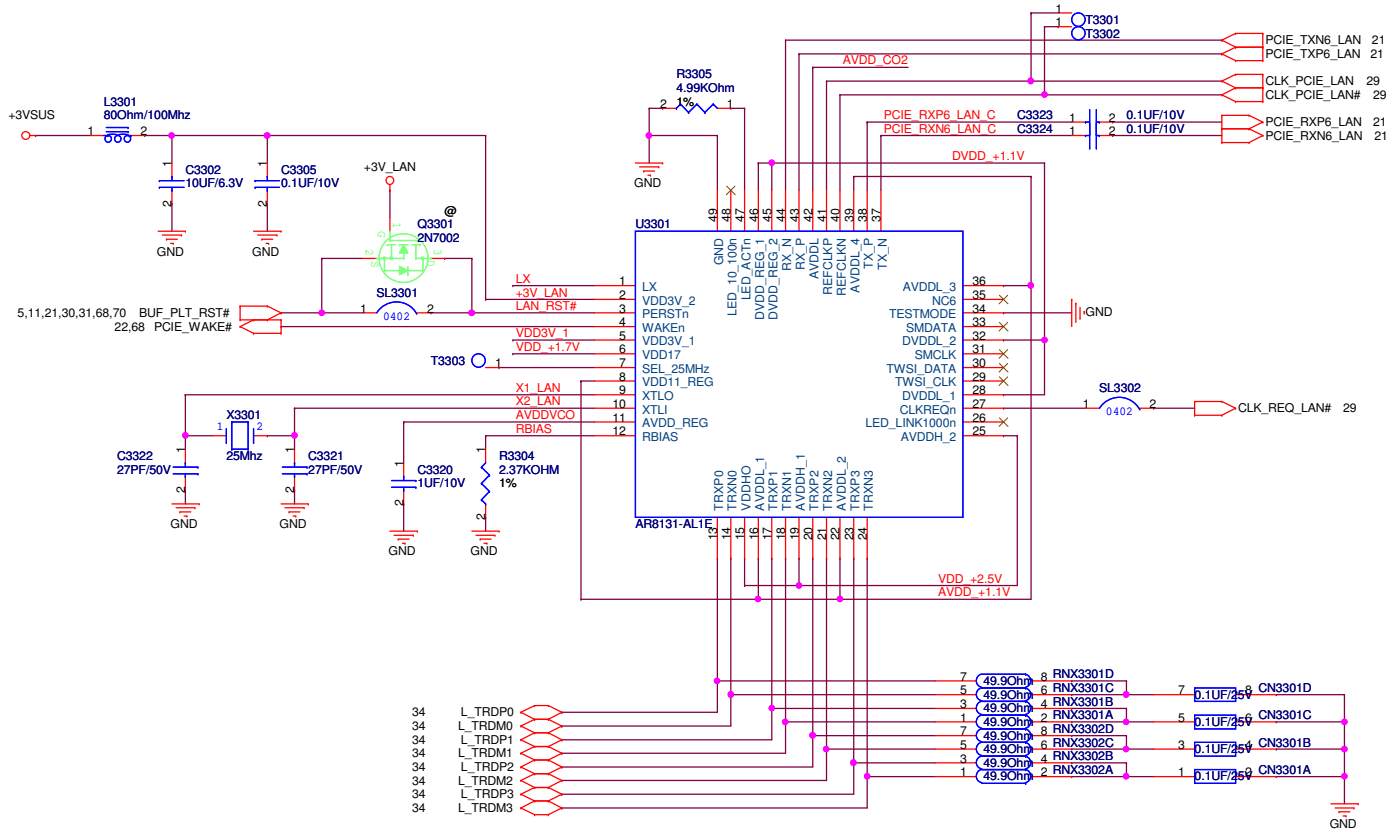
<Variant Name> ROM FLASH ROM TOUCH PAD KB

<b>ASUS</b>		<b>Title :</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name <b>UX50</b>	Rev 1.0a	
Date: Monday, April 06, 2009	Sheet	31	of 97

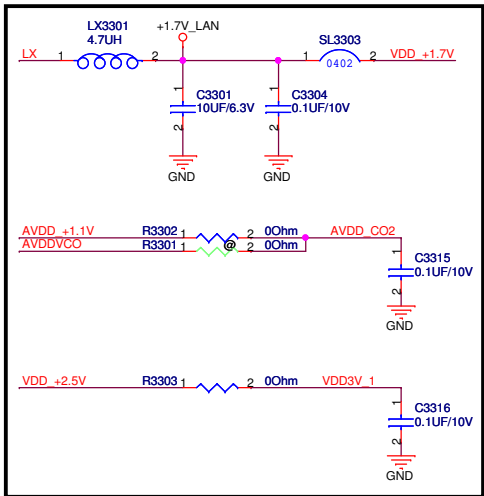
<Variant Name>

		<b>Title: UVA LEVEL SHIFTERS</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
C	<b>UX50</b>	1.0a	
Date: <u>Tuesday, March 31, 2009</u>		Sheet	32 of 97

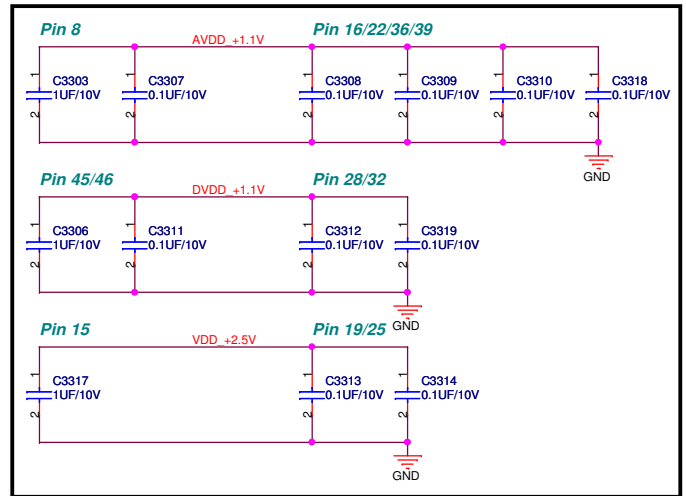




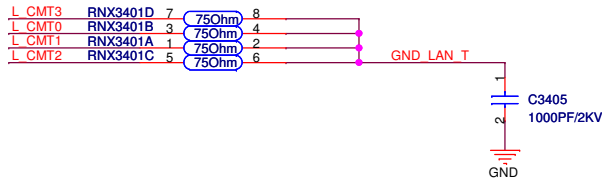
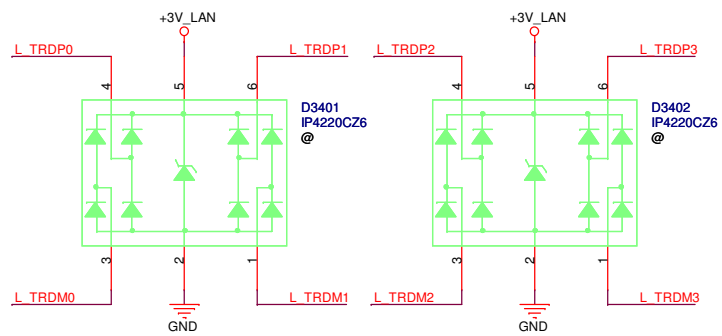
**Power**



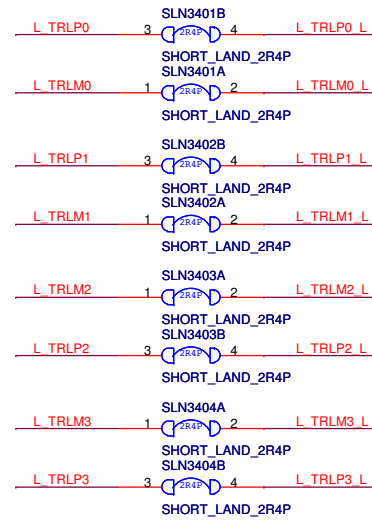
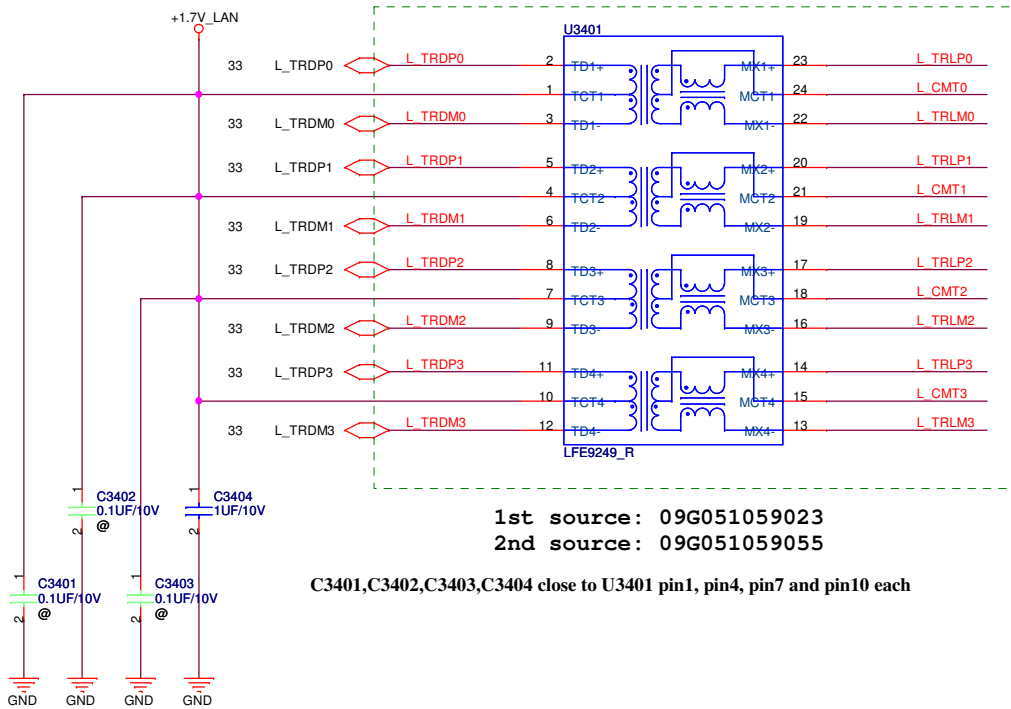
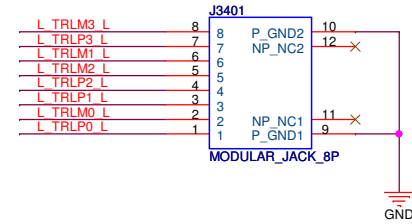
**Cap.**



<b>ASUS</b>		<b>Title : LAN-AR8131-AR812</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Tony Su</b>	
Size	Project Name	<b>UX50</b>	Rev
Custom			1.00
Date: Wednesday, April 08, 2009		Sheet	33 of 97

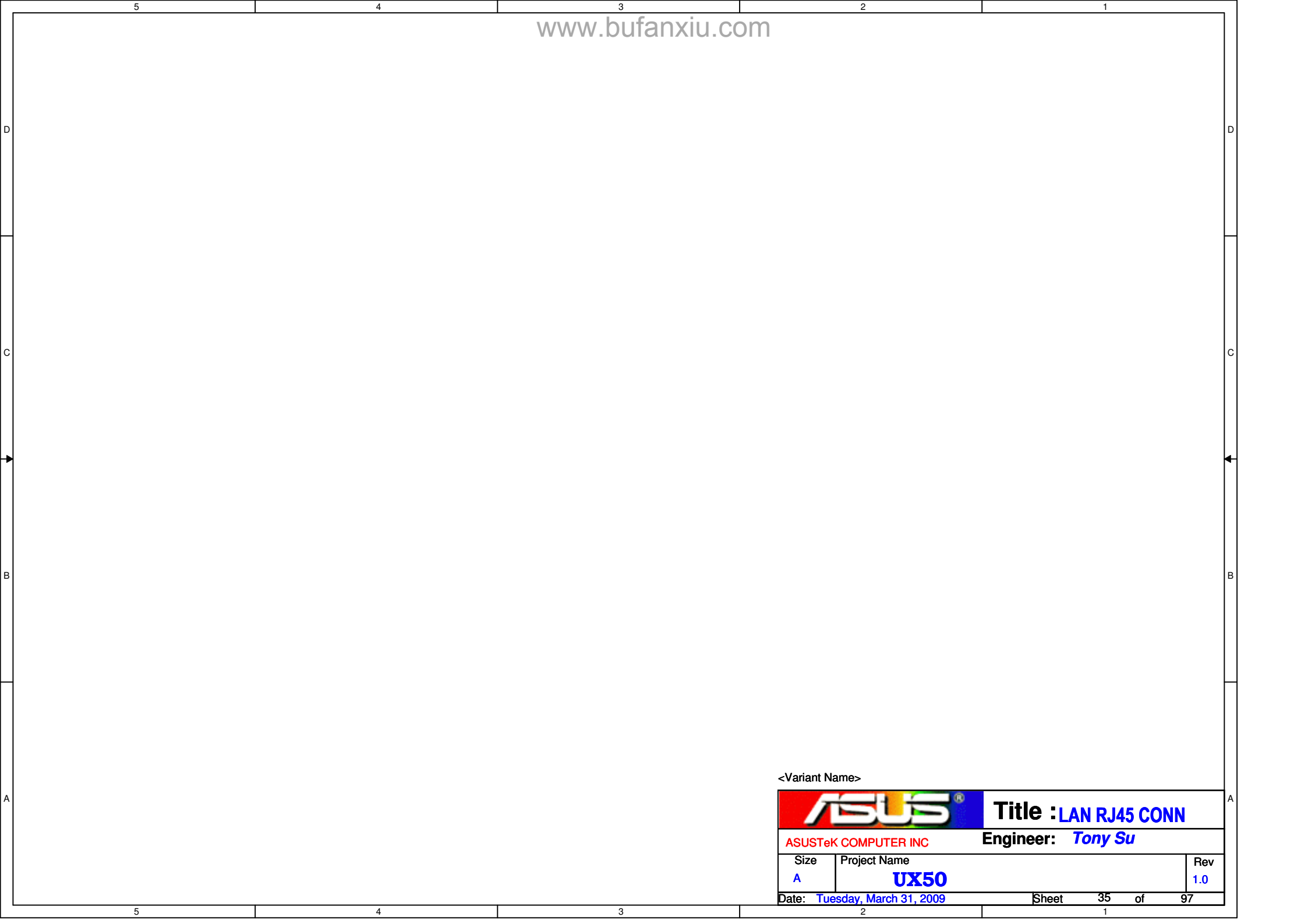


For RJ-45




<Variant Name>


<b>ASUS</b>		<b>Title :LAN RJ45 CONN</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0	
Date: Tuesday, March 31, 2009		Sheet	34 of 97

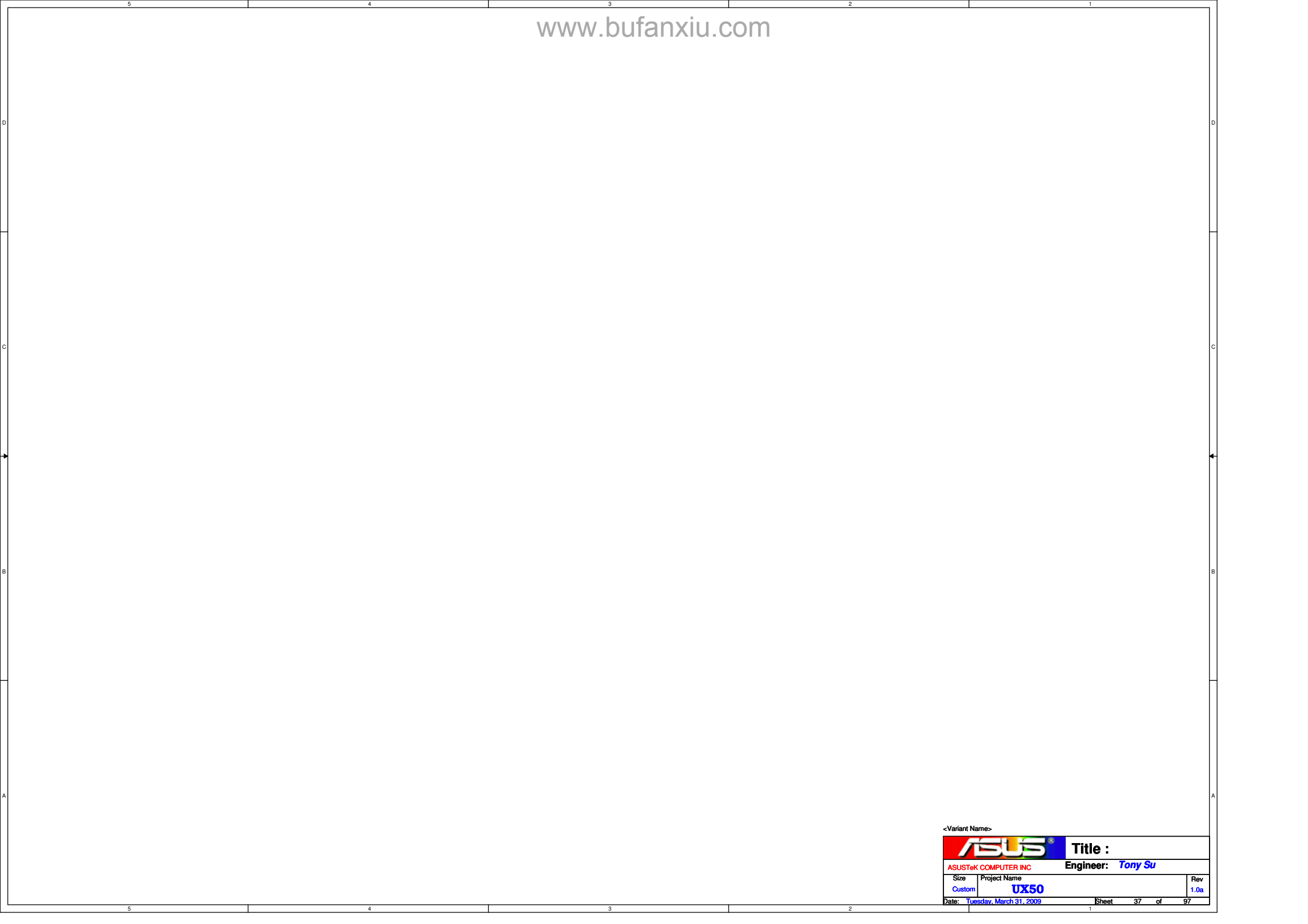


<Variant Name>


		<b>Title : LAN RJ45 CONN</b>
ASUSTeK COMPUTER INC		<b>Engineer: Tony Su</b>
Size A	Project Name <b>UX50</b>	Rev 1.0
Date: <b>Tuesday, March 31, 2009</b>		Sheet <b>35</b> of <b>97</b>

<Variant Name>

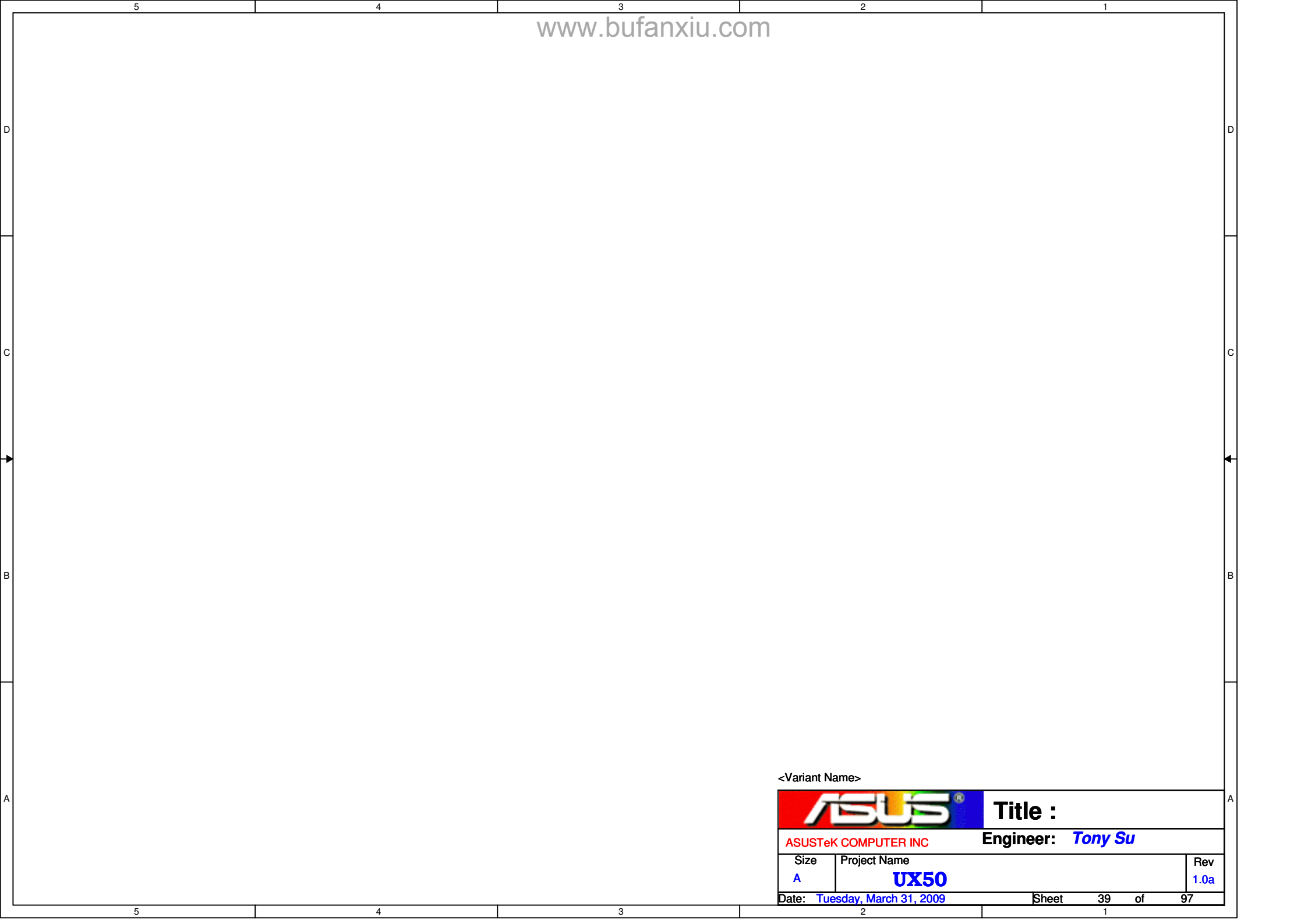
		<b>Title :AUD ALC269</b>	
ASUSTeK COMPUTER INC		<b>Engineer: Tony Su</b>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0a	
Date: Tuesday, March 31, 2009			
		Sheet	36 of 97




<Variant Name>

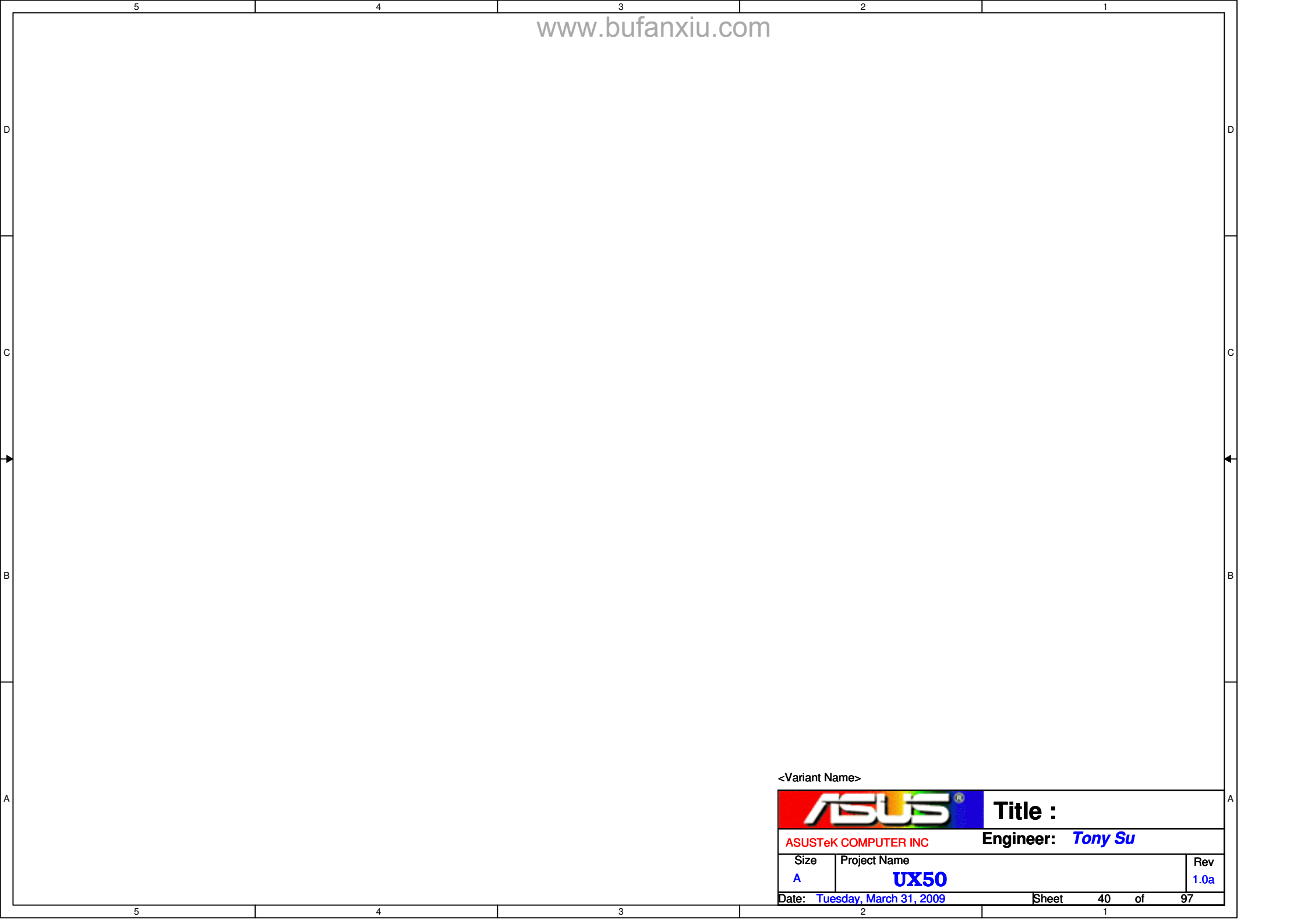
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ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
Custom	<b>UX50</b>		1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet	37 of 97






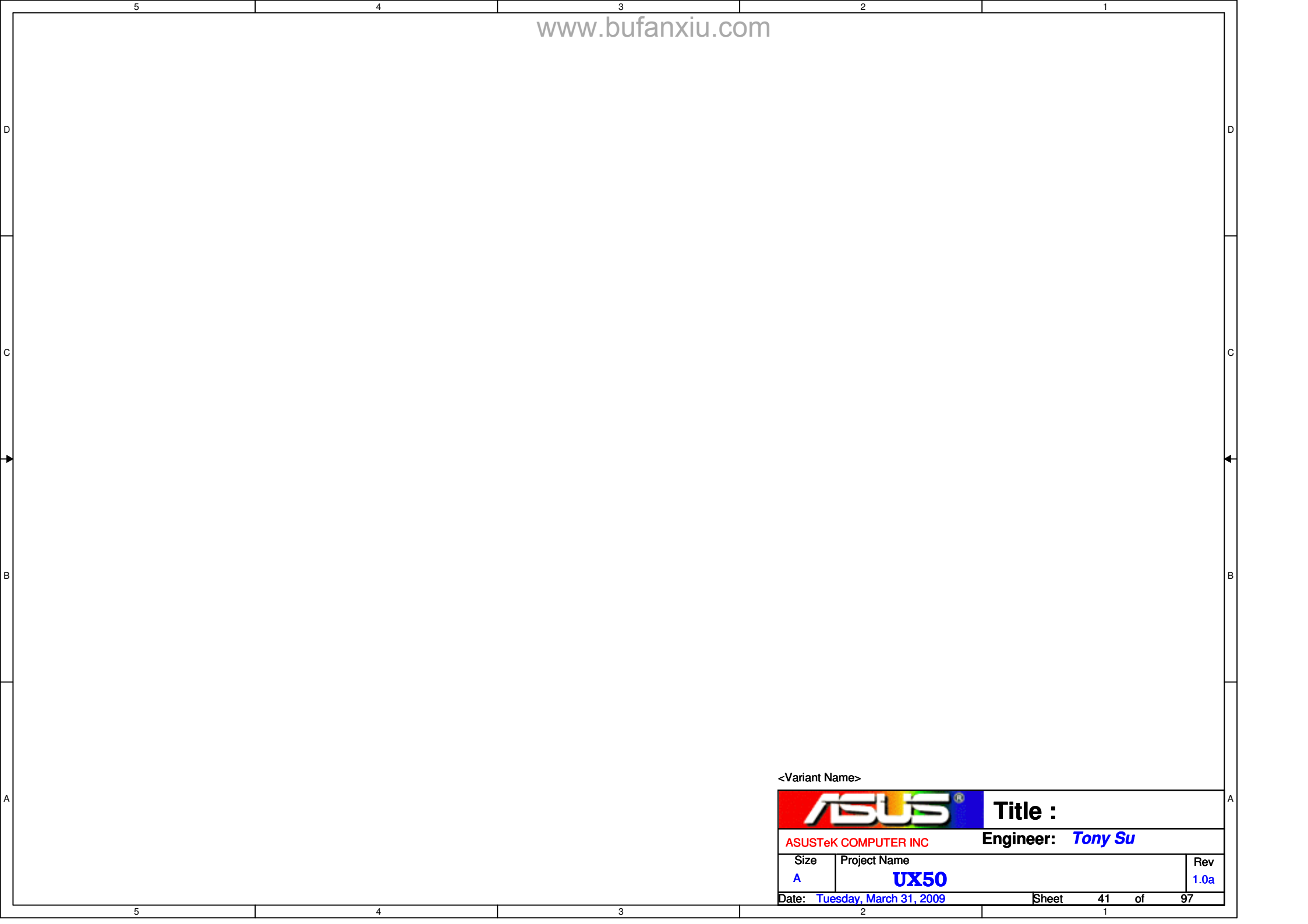
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		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 39 of 97




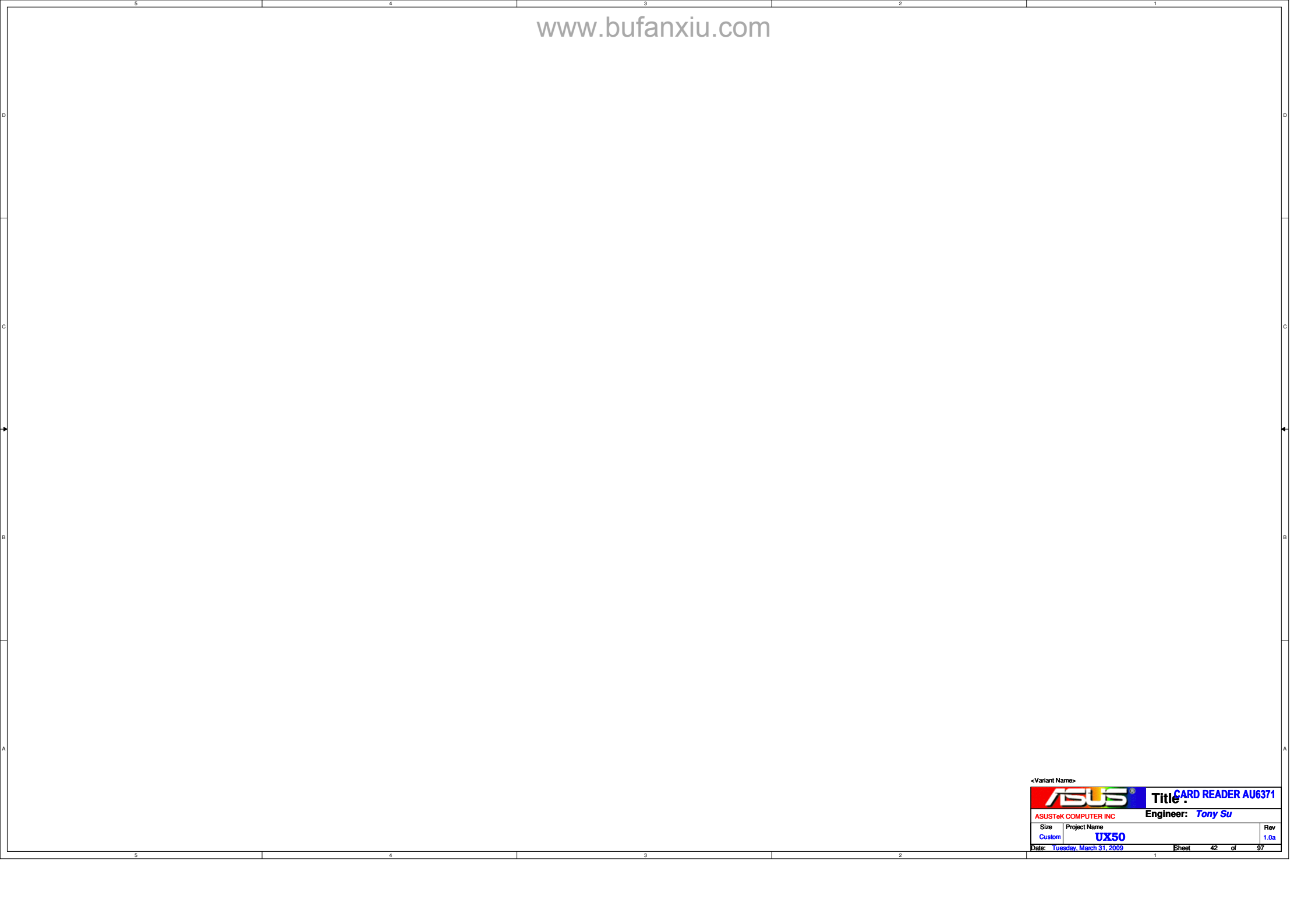
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ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 40 of 97






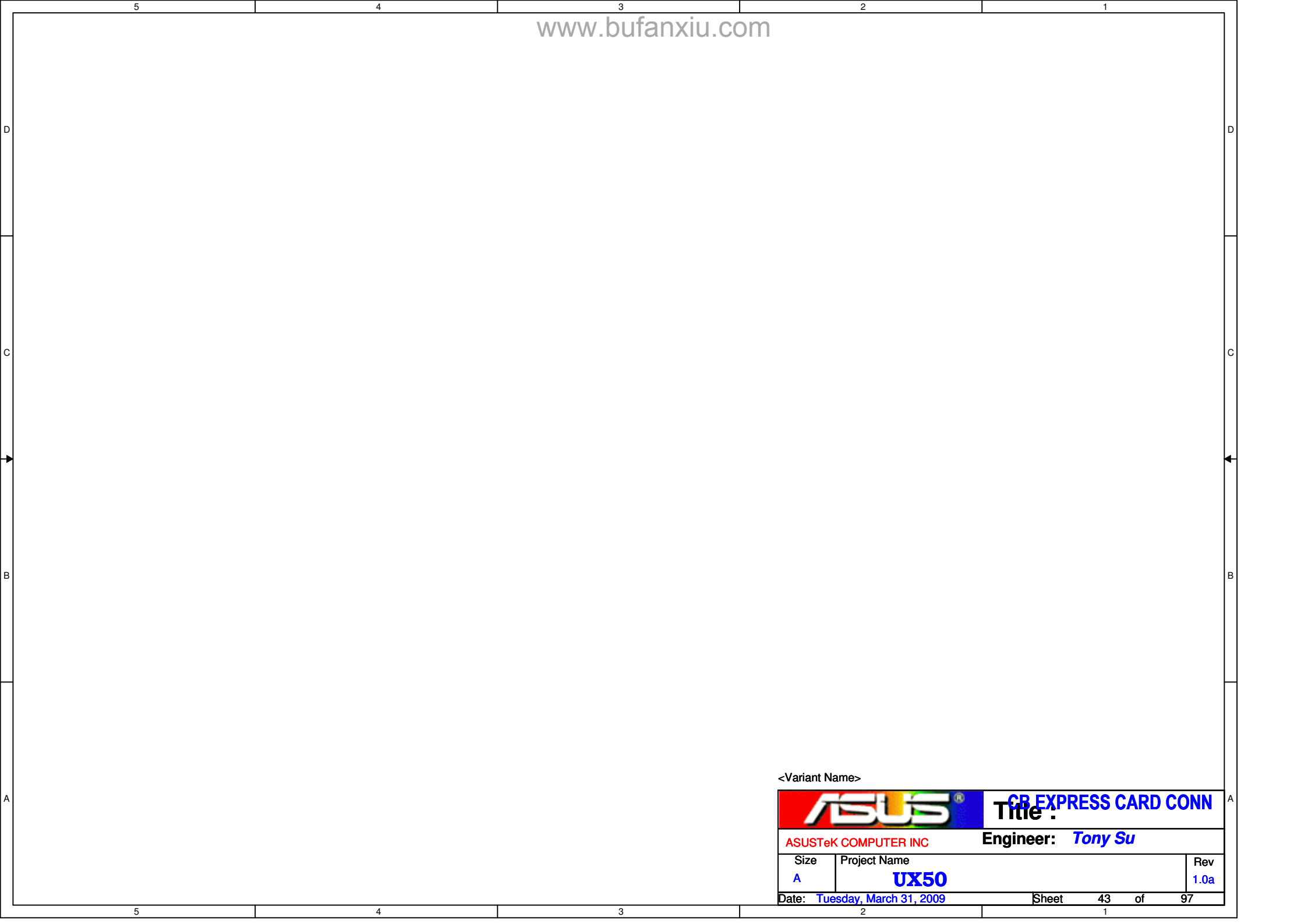
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		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 41 of 97




<Variant Name>

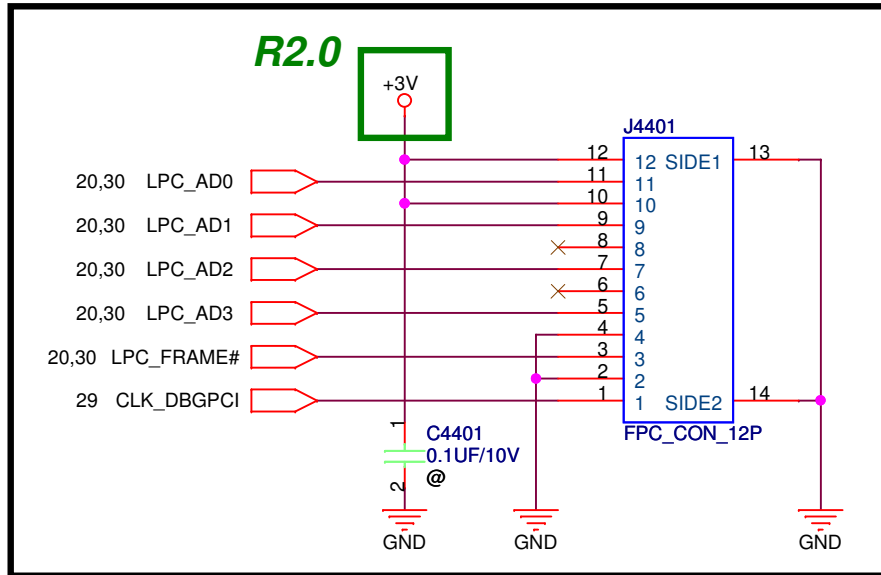
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ASUSTeK COMPUTER INC		<b>Engineer:</b> Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009		Sheet	42 of 97



<Variant Name>

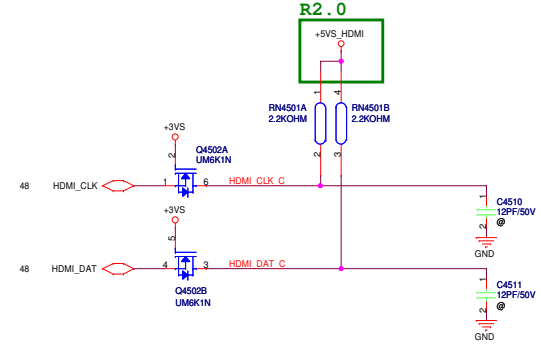
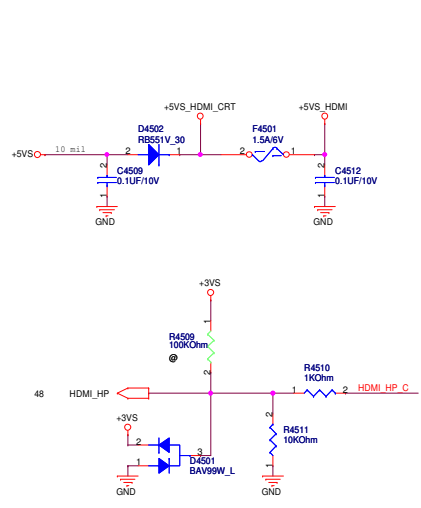
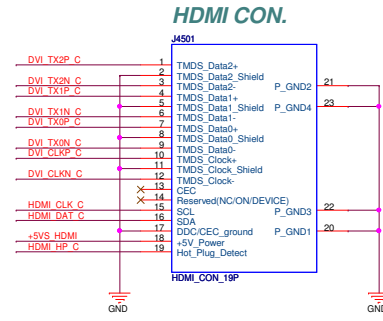
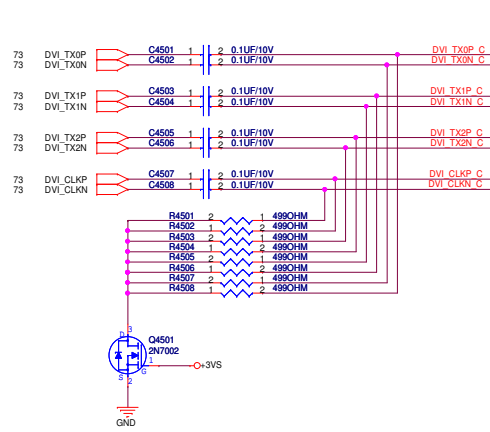
		<b>Title :</b> CB EXPRESS CARD CONN
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 43 of 97

# LPC DEBUG PORT

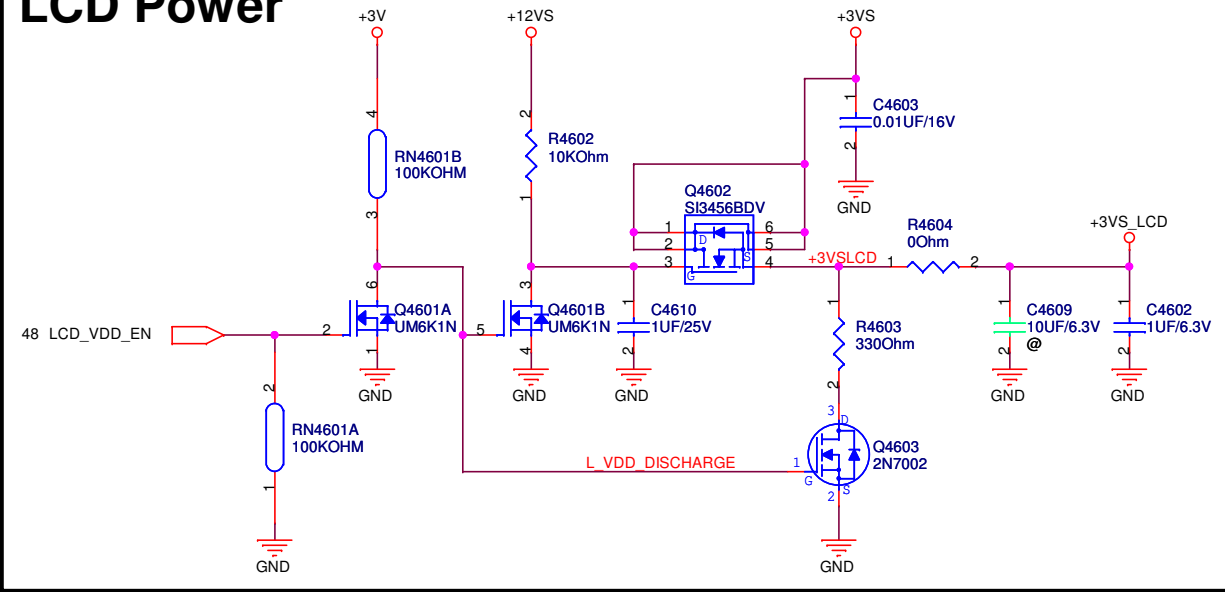


<Variant Name>

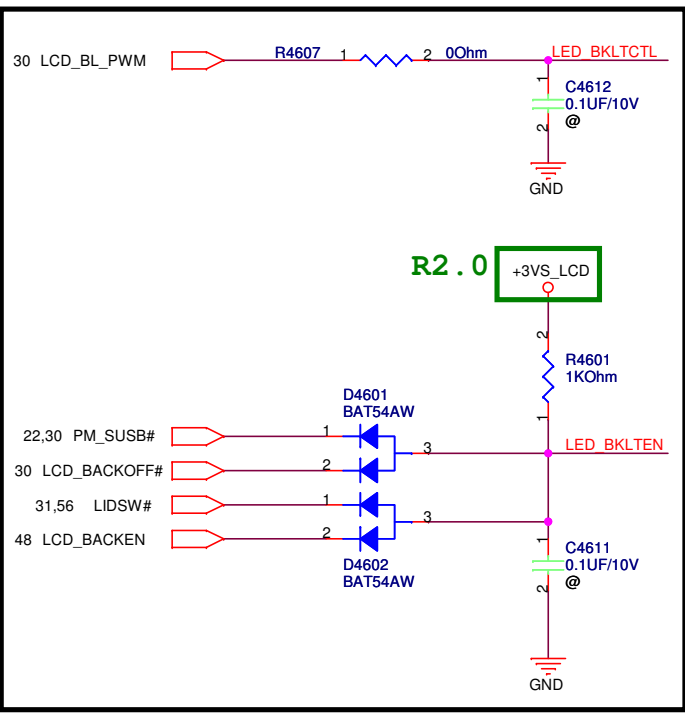
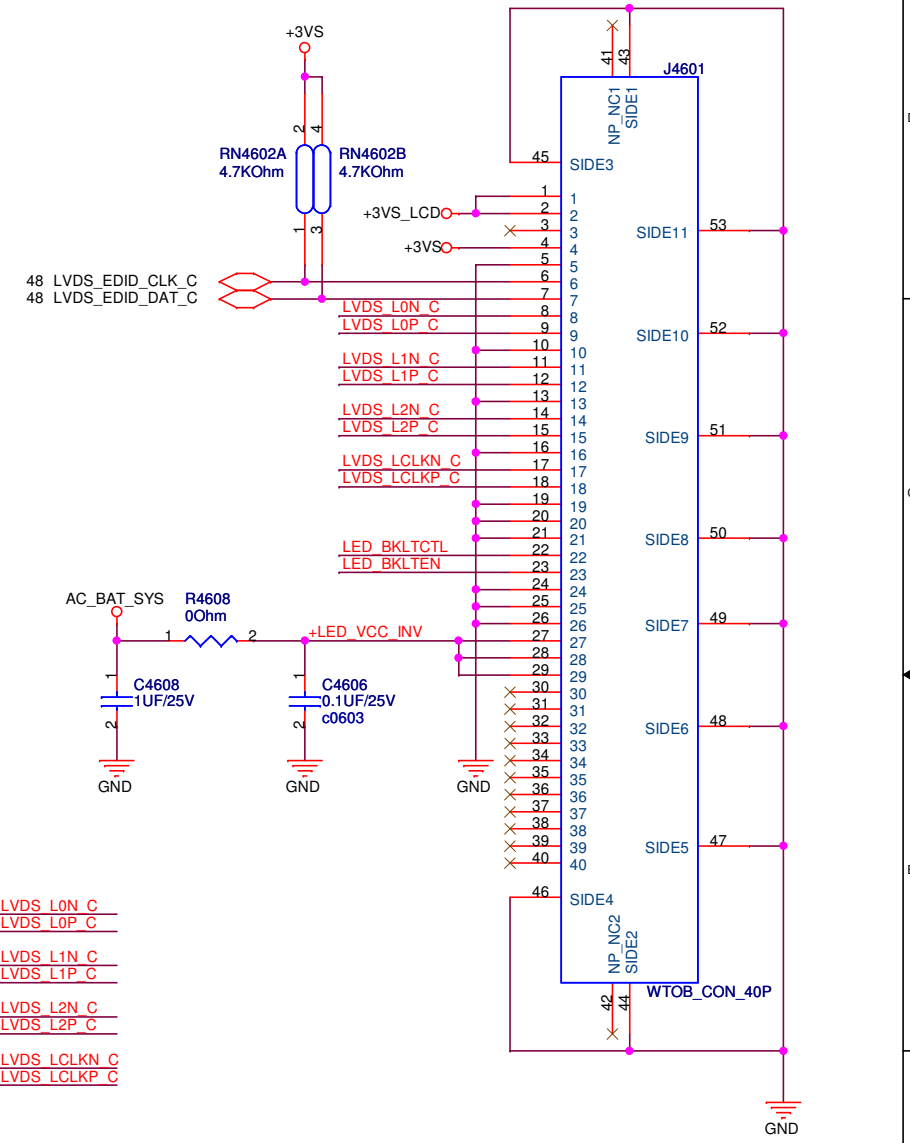
		<b>Title :BUG DEBUG PORT</b>
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 44 of 97



# LCD Power



# LVDS CONN

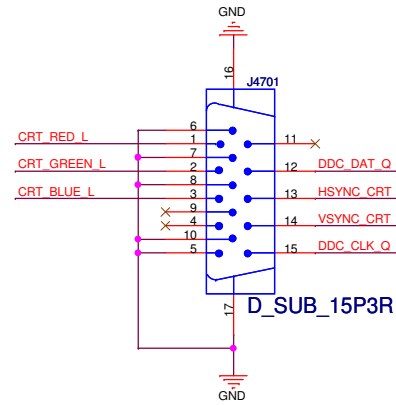
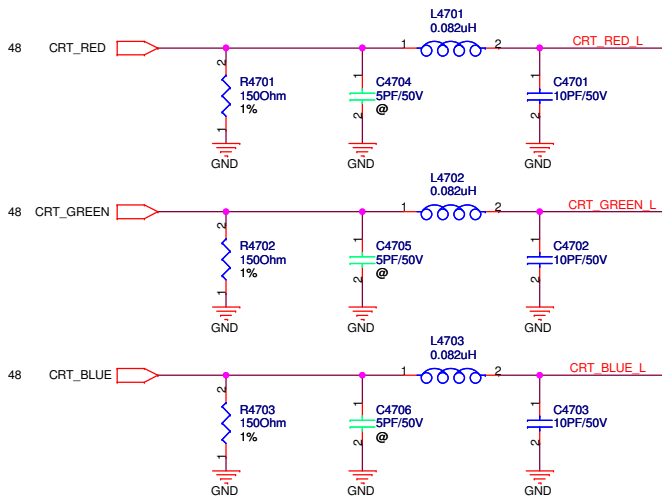


48 LVDS_L0N	1	2R4P	2	SLN4601A	LVDS_L0N_C
48 LVDS_L0P	3	2R4P	4	SLN4601B	LVDS_L0P_C
48 LVDS_L1N	1	2R4P	2	SLN4602A	LVDS_L1N_C
48 LVDS_L1P	3	2R4P	4	SLN4602B	LVDS_L1P_C
48 LVDS_L2N	1	2R4P	2	SLN4603A	LVDS_L2N_C
48 LVDS_L2P	3	2R4P	4	SLN4603B	LVDS_L2P_C
48 LVDS_LCLKN	1	2R4P	2	SLN4604A	LVDS_LCLKN_C
48 LVDS_LCLKP	3	2R4P	4	SLN4604B	LVDS_LCLKP_C

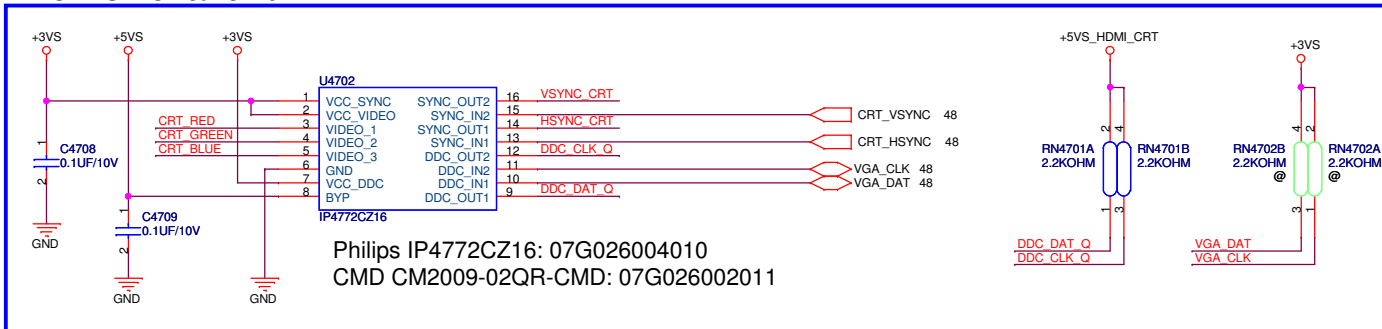
<Variant Name>

<b>ASUS</b>		<b>Title :CRT LVDS CONN</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0a	
Date: Tuesday, March 31, 2009		Sheet	46 of 97

# CRT Connector



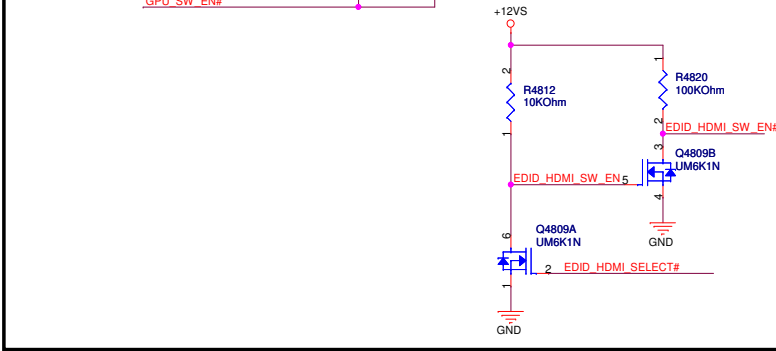
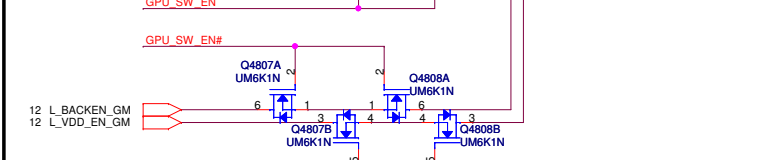
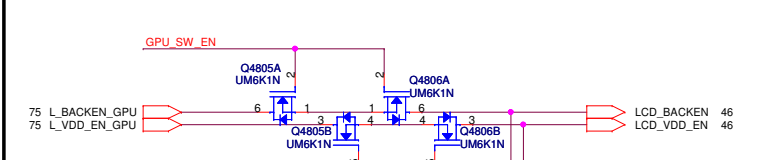
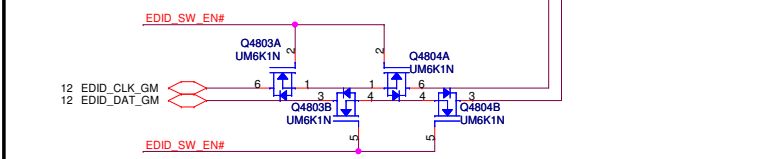
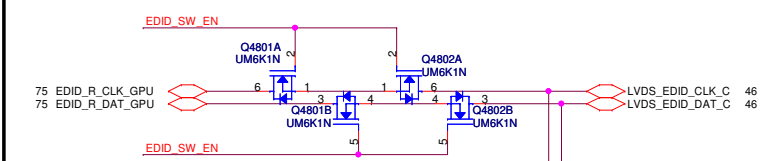
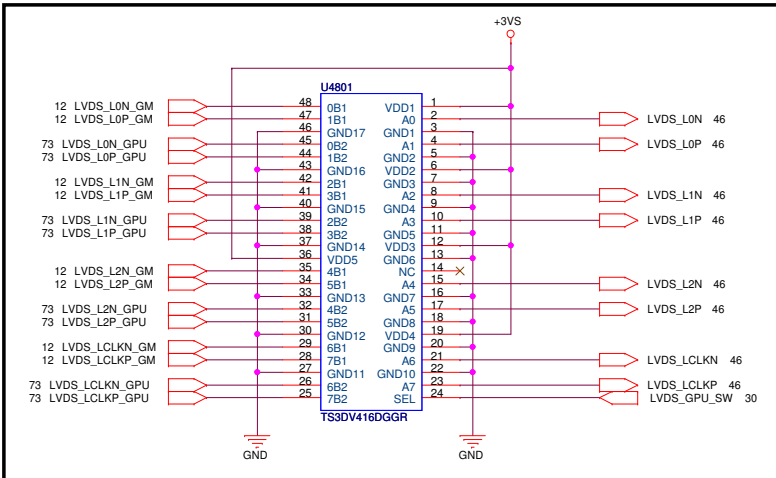
## PLACE ESD IC near J4701



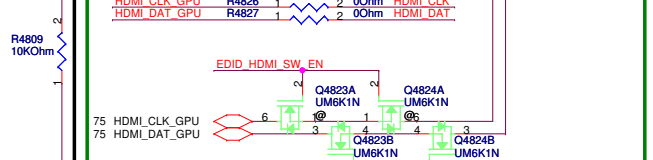
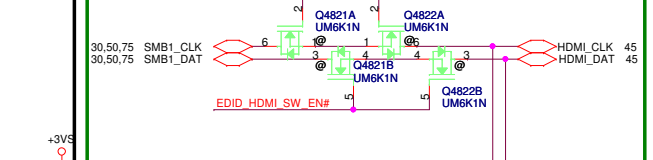
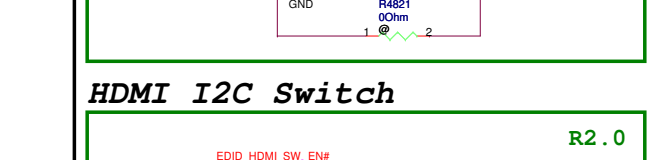
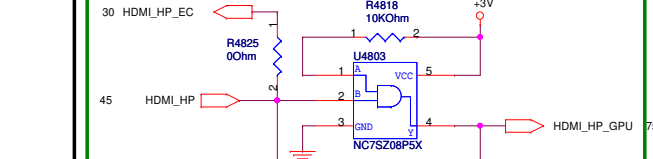
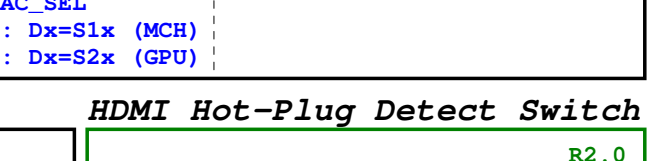
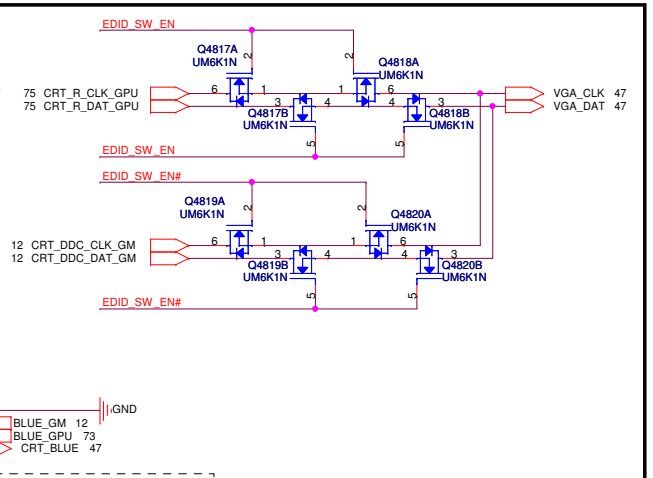
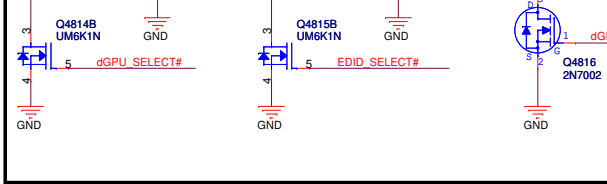
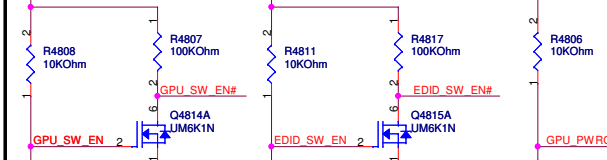
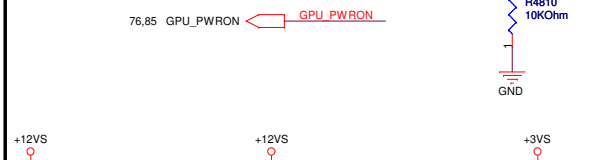
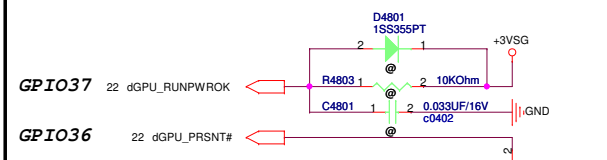
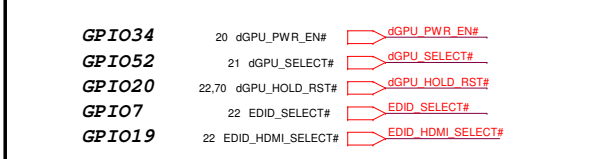
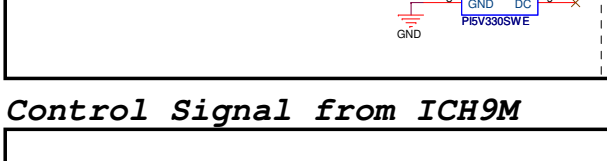
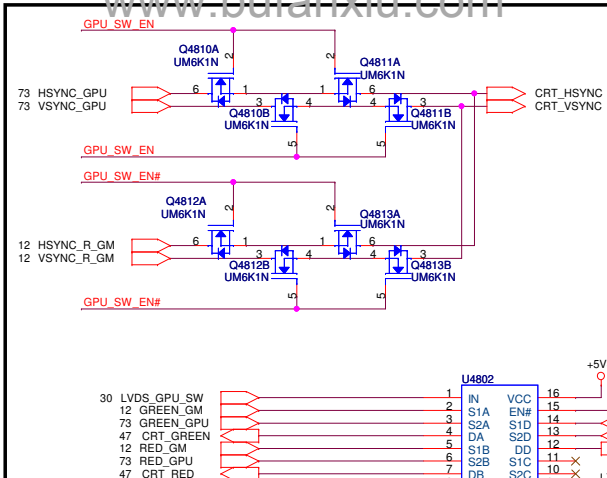
<Variant Name>

<b>ASUS</b>		<b>Title :CRT D-SUB CONN</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size Custom	Project Name <b>UX50</b>	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet 47	of 97	

# LVDS Switch

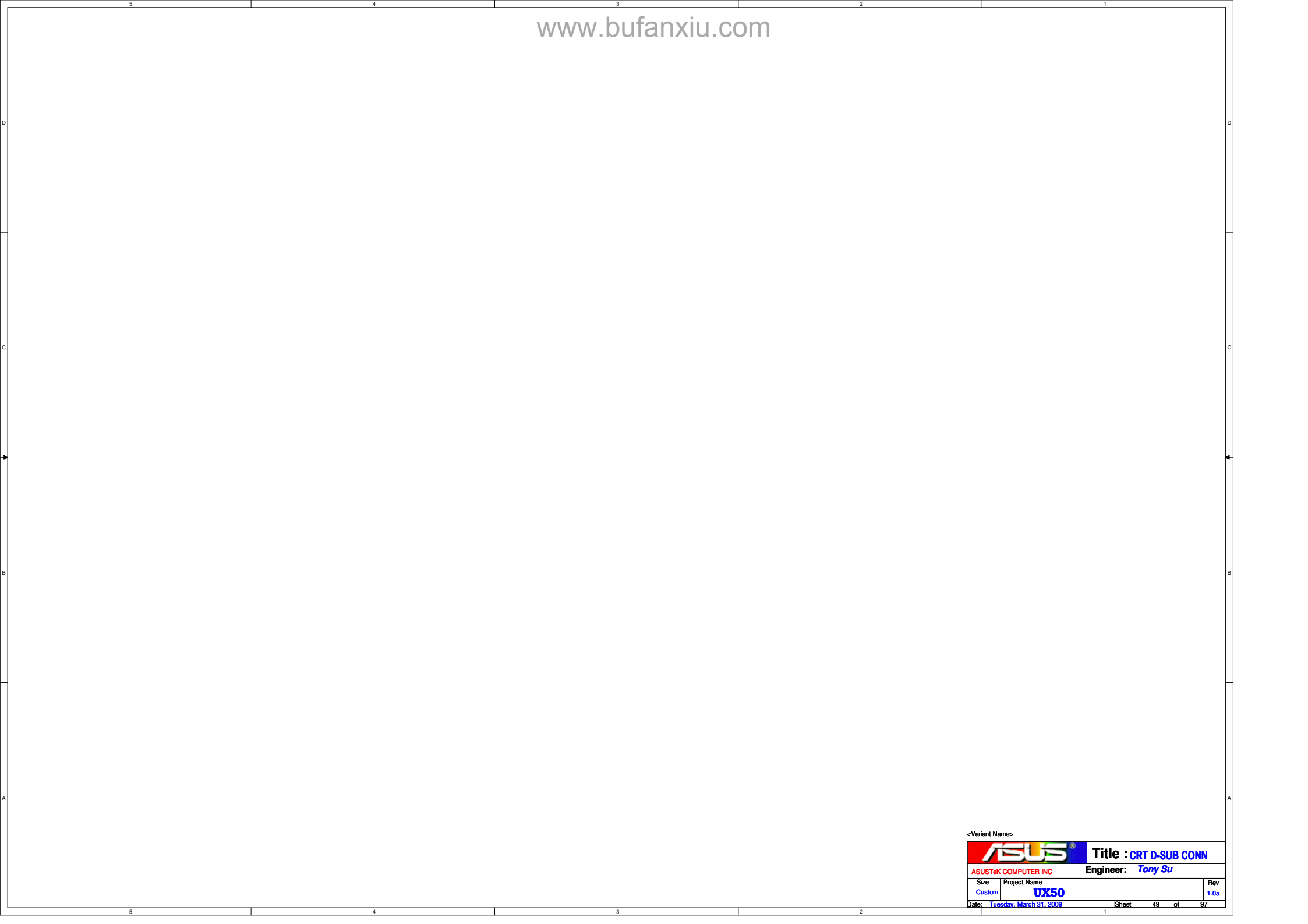


# CRT Switch




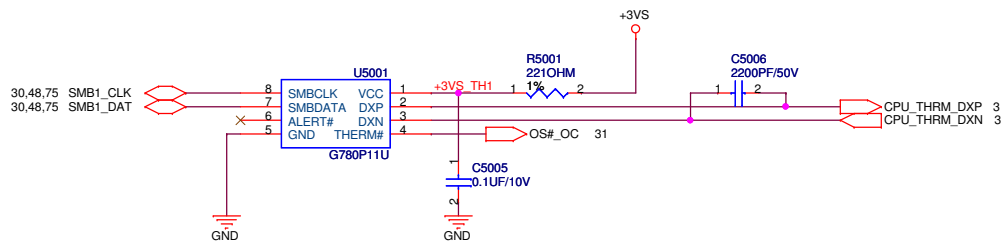
**ASUS** Title: Hybrid Switch  
ASUSTek COMPUTER INC Engineer: Tony Su  
Size: Project Name  
Custom: UX50  
Date: Tuesday, March 31, 2009 Sheet: 48 of 97





<Variant Name>

		<b>Title : CRT D-SUB CONN</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0a	
Date: <u>Tuesday, March 31, 2009</u>		Sheet	49 of 97



1nd: 06G023096010 G780P11U SOP-8  
 2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU\_THRM\_DA , CPU\_THRM\_DC and MEM\_THERM\_DA , MEM\_THERM\_DC on the same layer

```

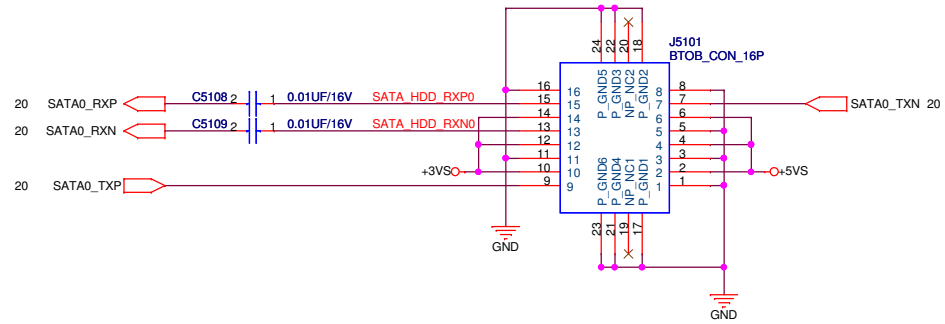
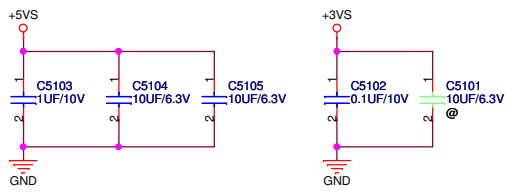
-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS
    
```

Avoid FSB,Power

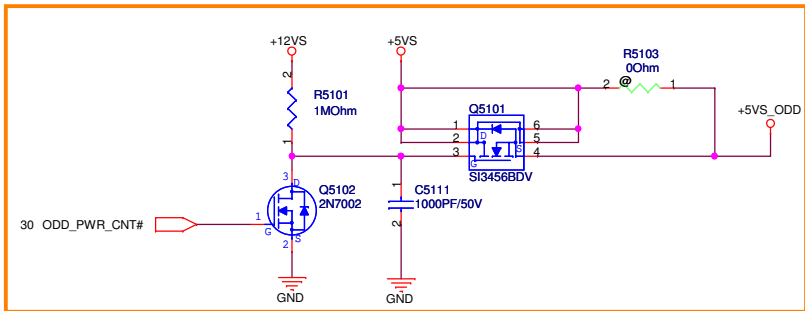
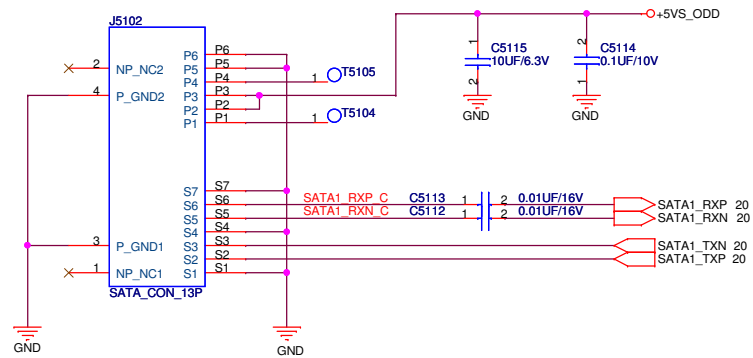
<Variant Name>

<b>ASUS</b>		<b>FAN THERMAL SENSOR FAN CONN</b>	
<b>ASUSTeK COMPUTER INC</b>		<b>Title :</b>	
<b>Engineer: Tony Su</b>			
Size Custom	Project Name <b>UX50</b>	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet 50 of 97		

### SATA HDD




### SATA ODD

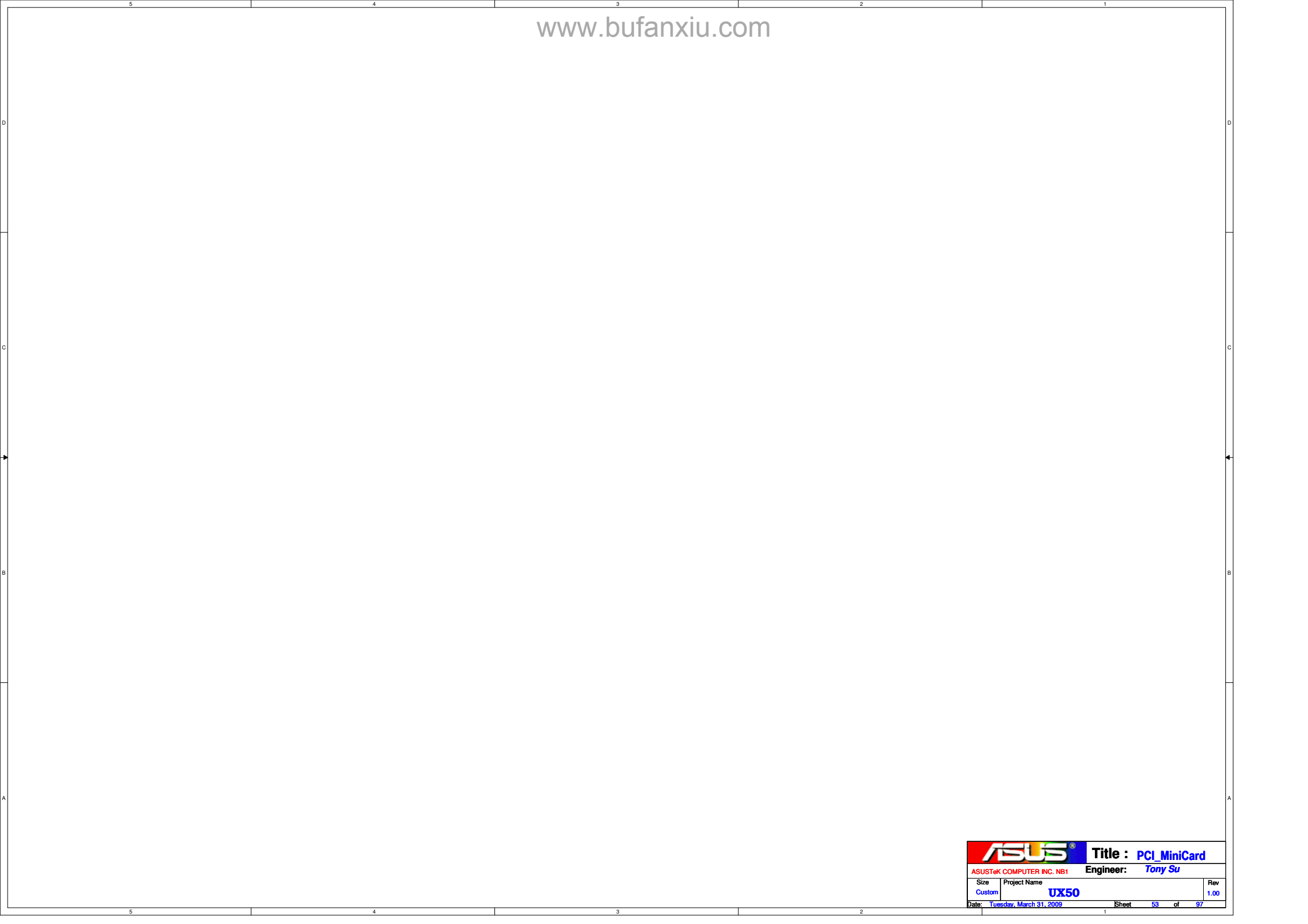



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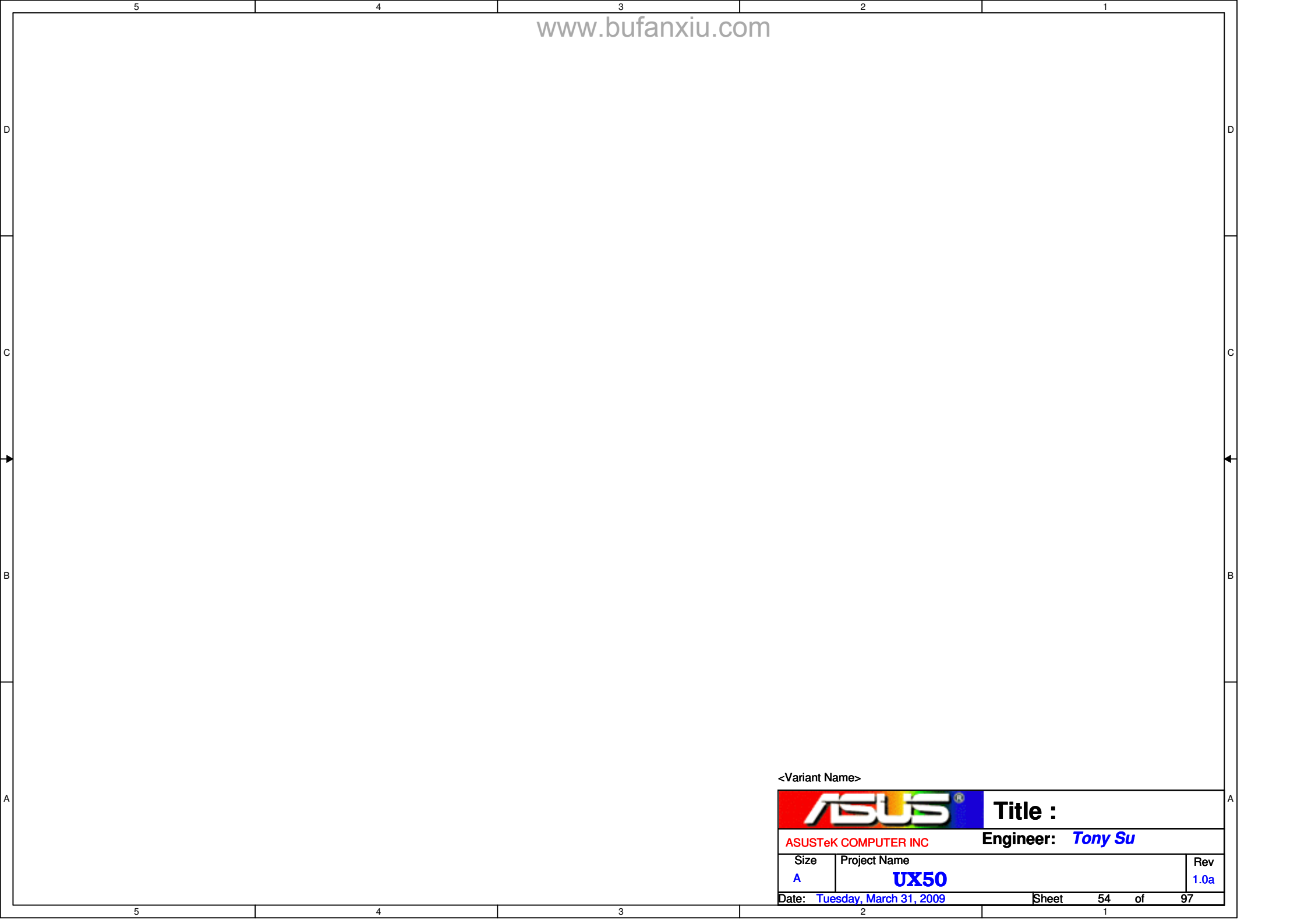
<b>ASUS</b>		<b>Title: YDD SATA HDD CONN</b>	
ASUSTeK COMPUTER INC		Engineer: <b>Tony Su</b>	
Size Custom	Project Name <b>UX50</b>	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet 51 of 97		

<Variant Name>


		<b>Title :USB 2.0 CONN*1</b>
ASUSTek COMPUTER INC		Engineer: <i>Tony Su</i>
Size Custom	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 52 of 97

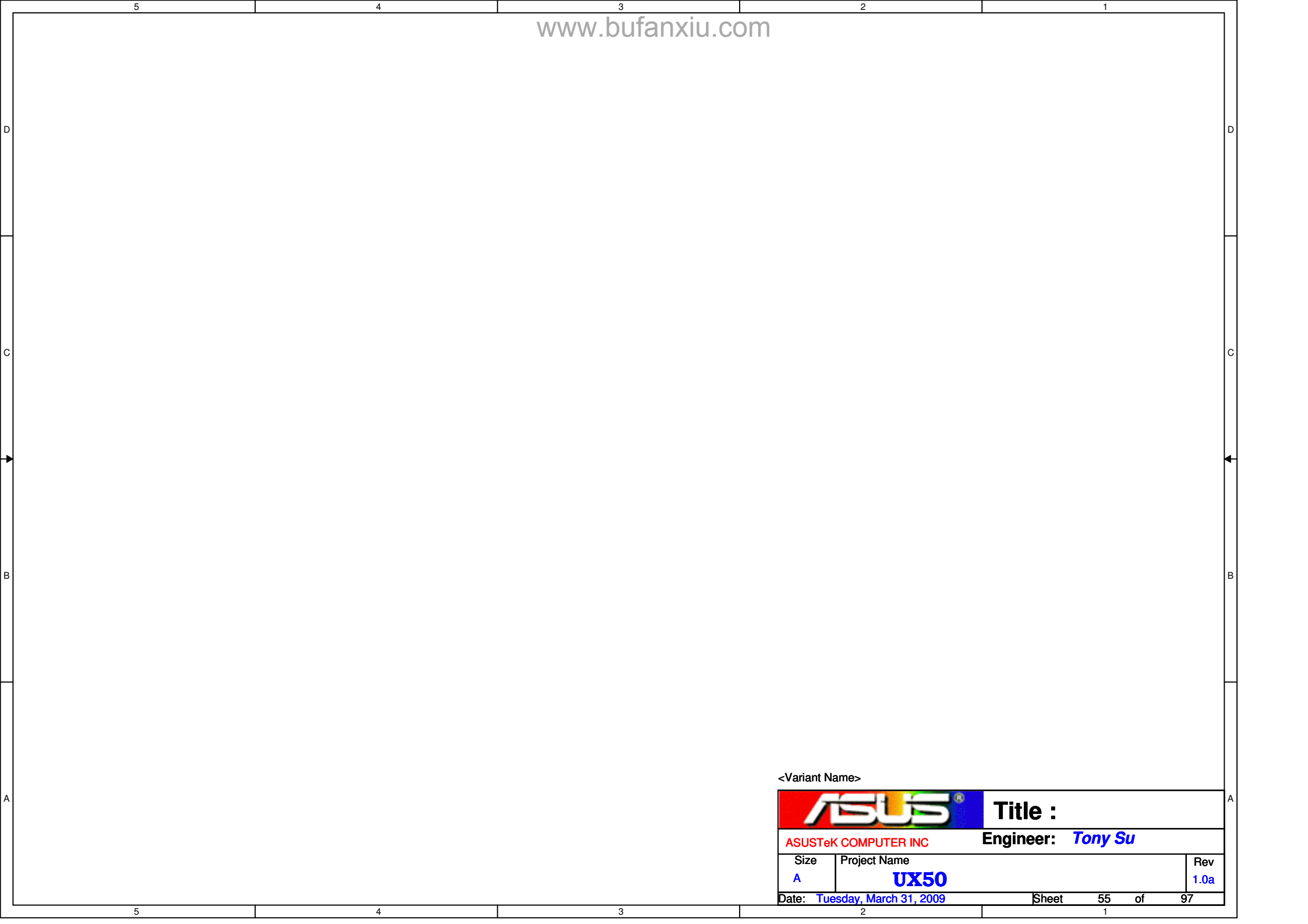


		<b>Title : PCI_Minicard</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer: Tony Su</b>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.00	
Date: Tuesday, March 31, 2009		Sheet	53 of 97




<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 54 of 97



<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 55 of 97

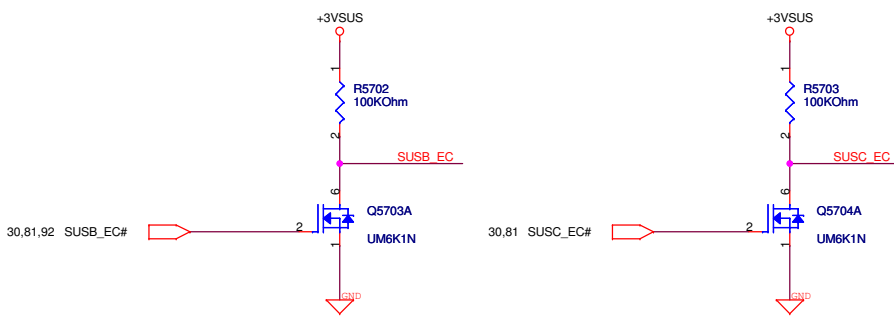
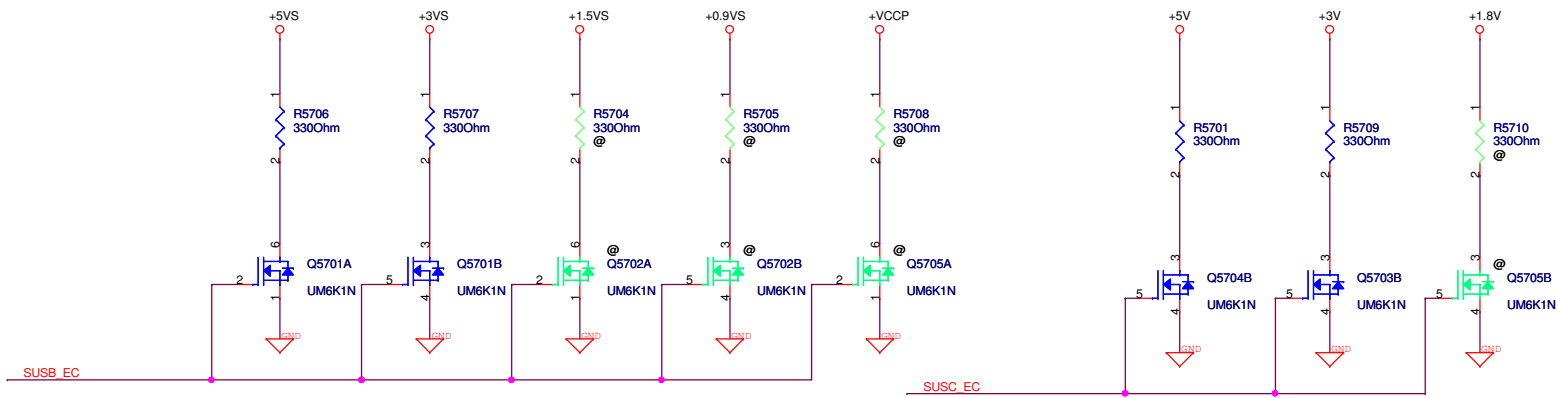
### LID SENSER

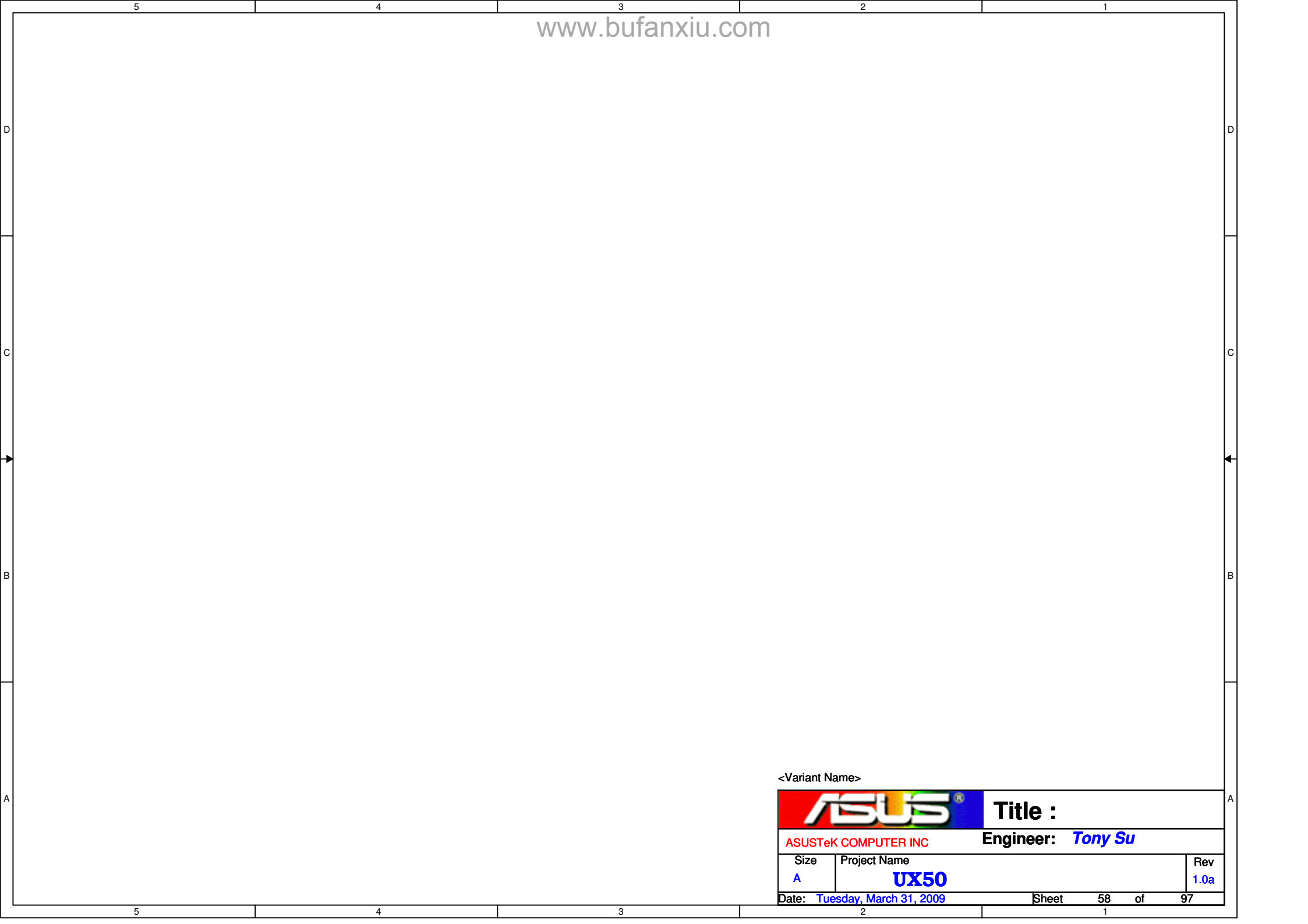


Hall Sensor Second Source  
06G036012010 Cheap  
06G036013010  
06G036009011  
06G051001012




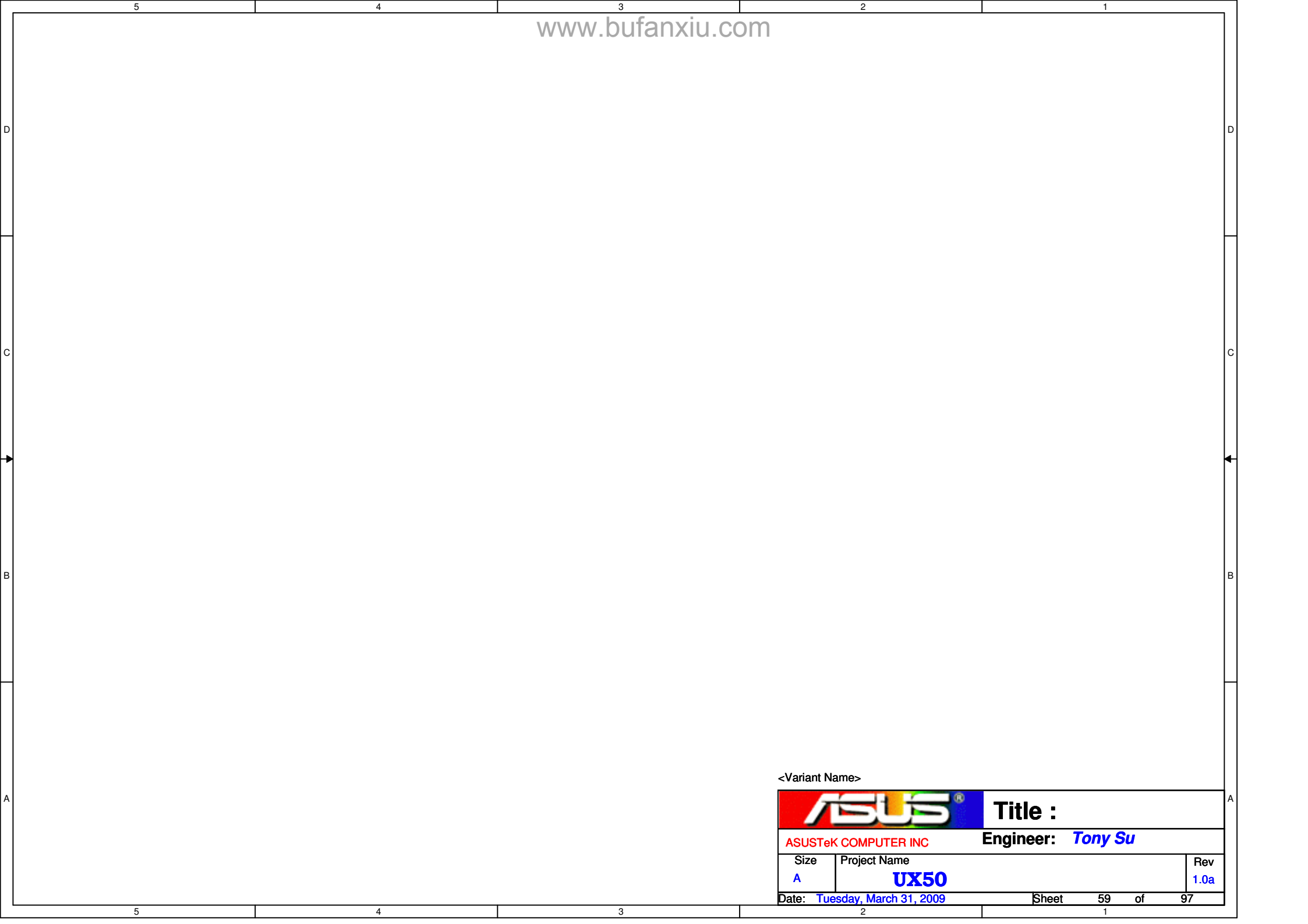
# Discharge Circuit






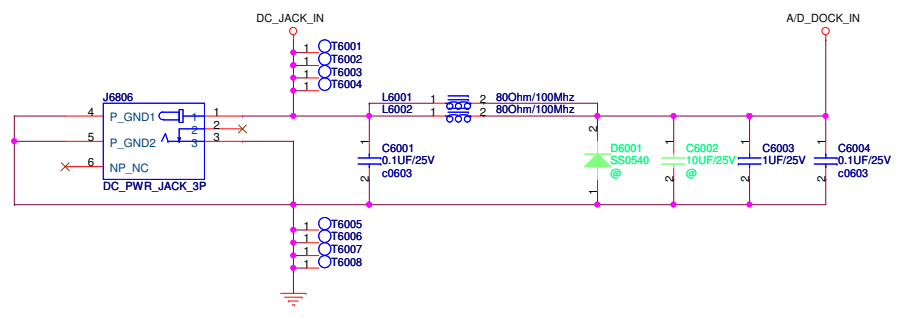
<Variant Name>

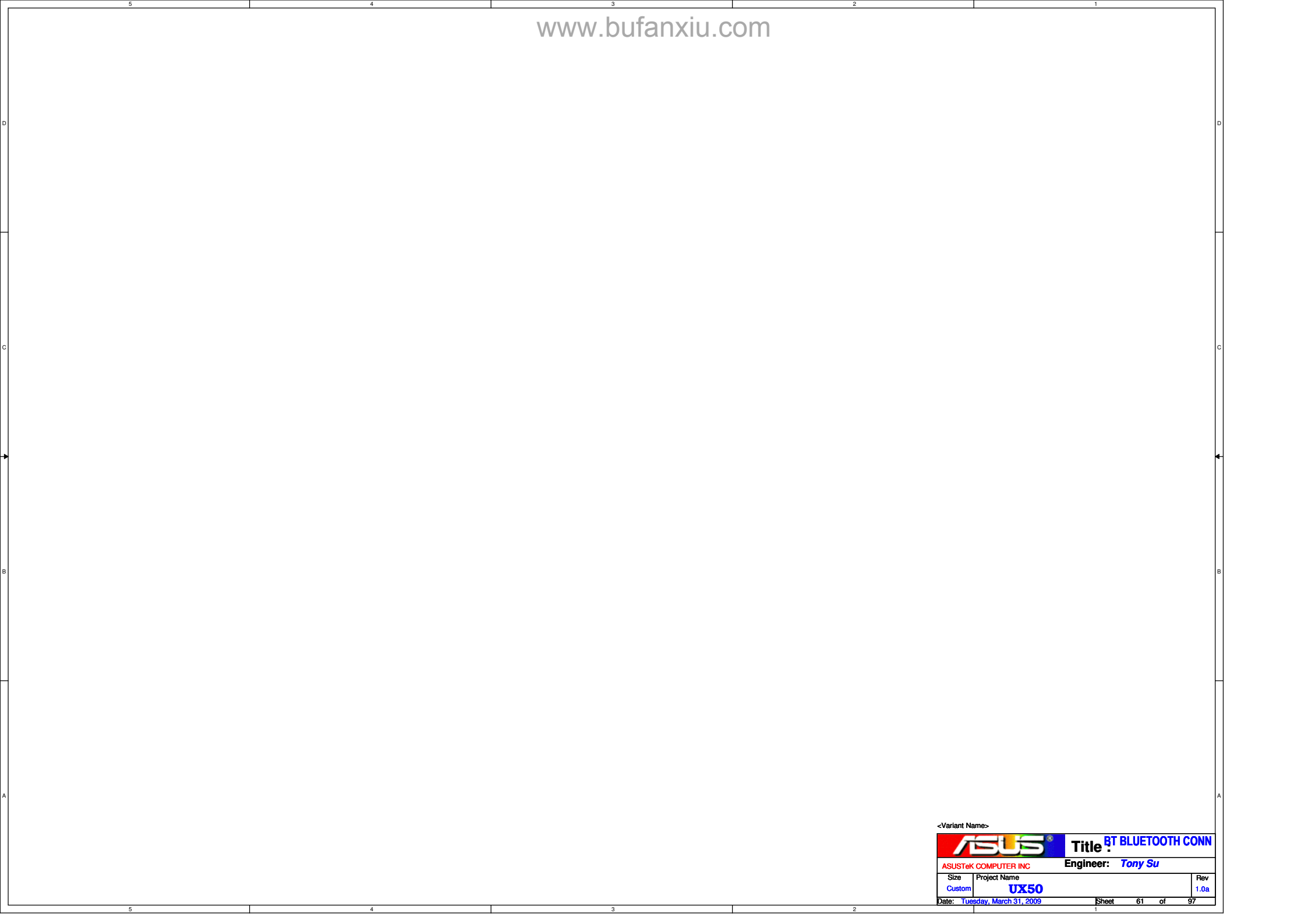
		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 58 of 97




<Variant Name>

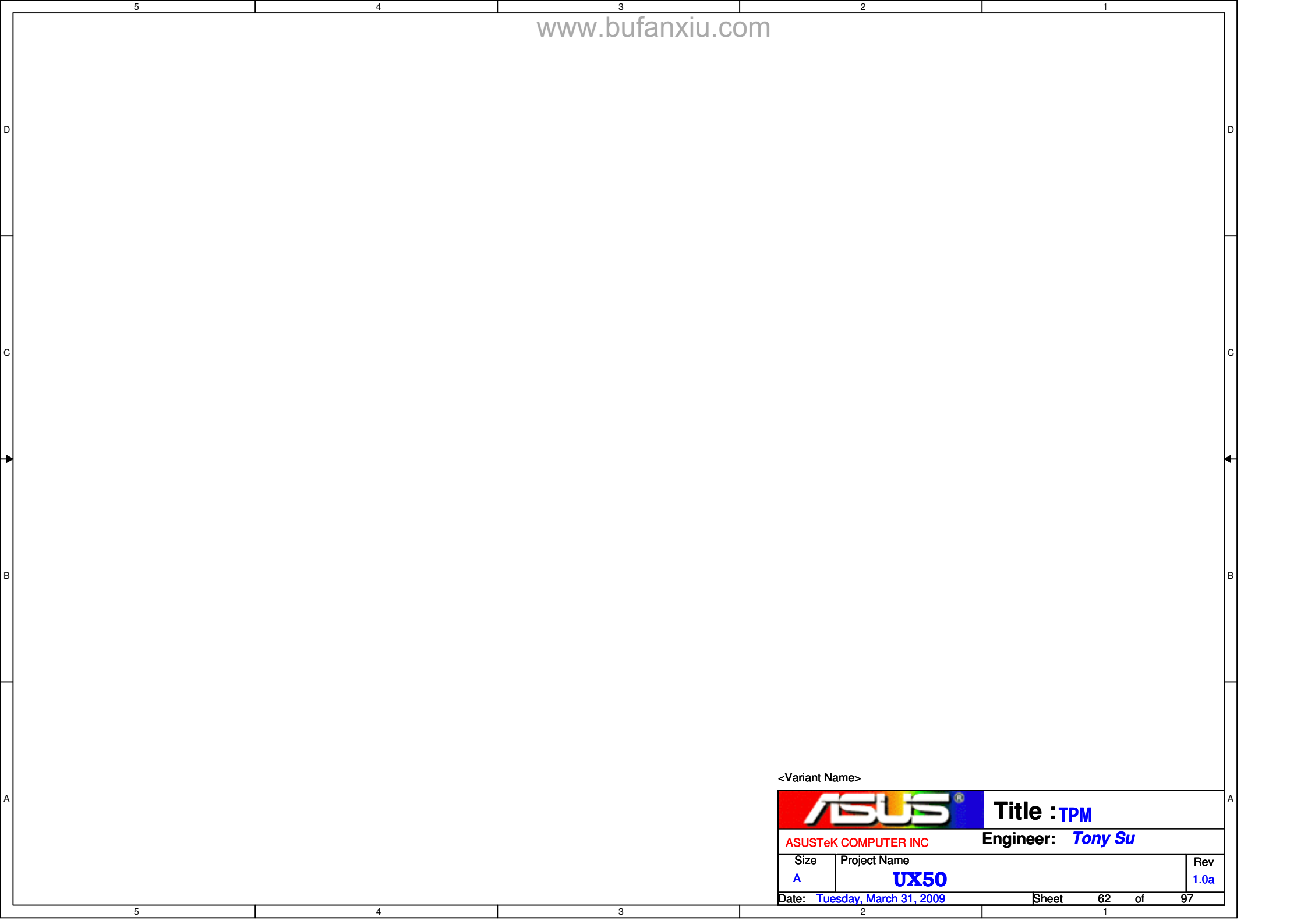
		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 59 of 97






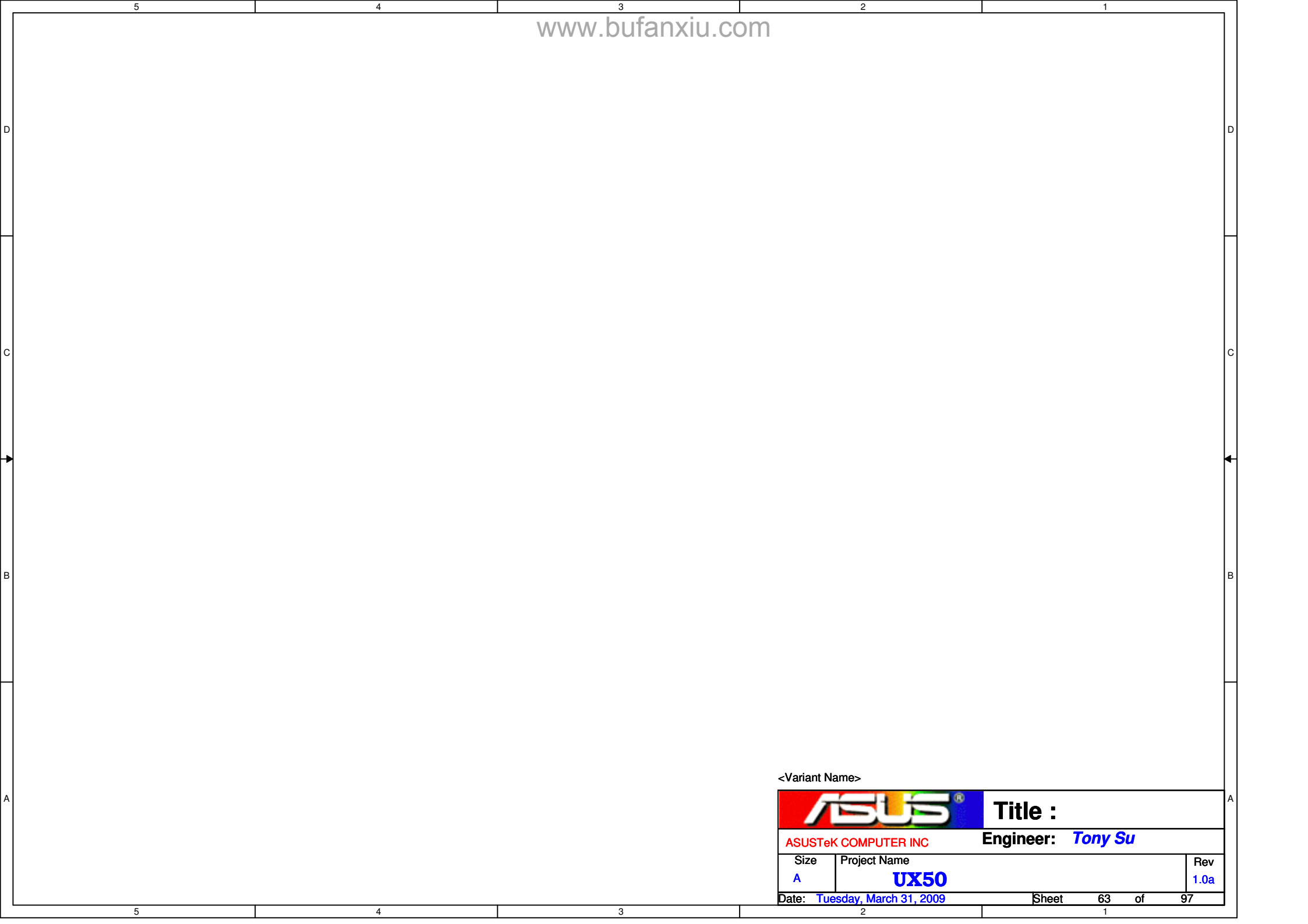
<Variant Name>

		<b>Title:</b> BT BLUETOOTH CONN
ASUSTeK COMPUTER INC		<b>Engineer:</b> Tony Su
Size Custom	Project Name <b>UX50</b>	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 61 of 97




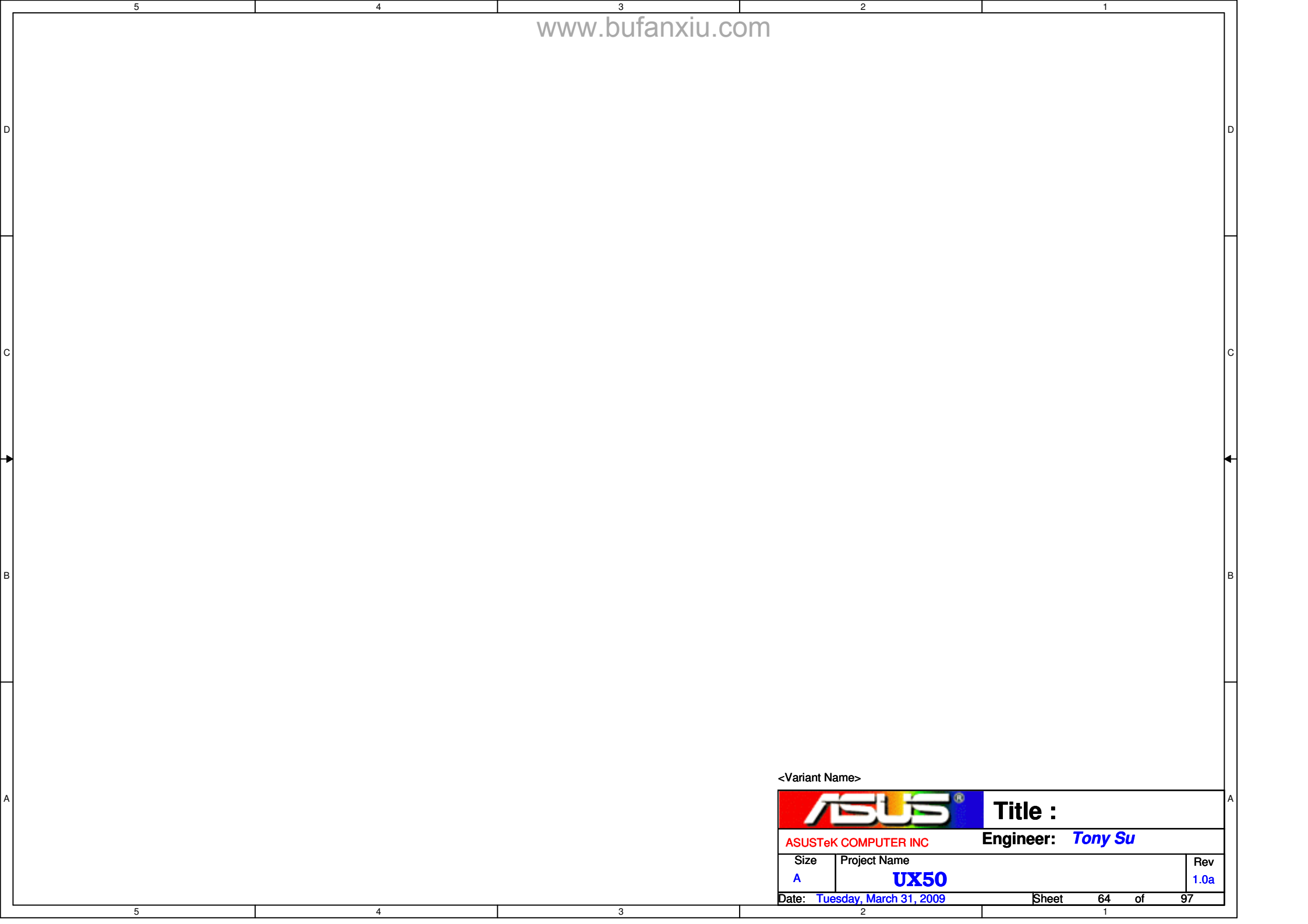
<Variant Name>

		<b>Title :TPM</b>
ASUSTeK COMPUTER INC		<b>Engineer: Tony Su</b>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 62 of 97




<Variant Name>

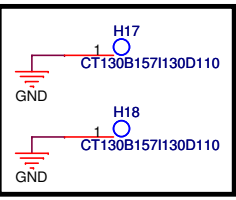
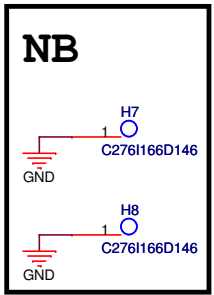
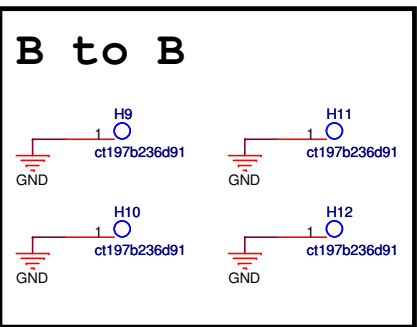
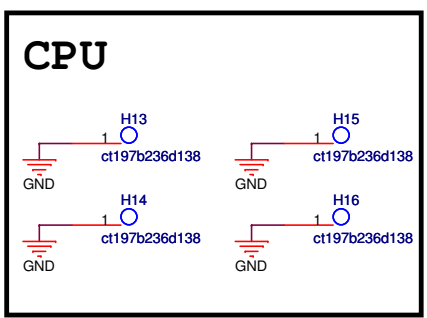
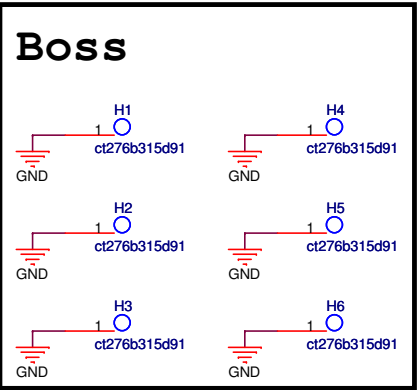
		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 63 of 97



<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <b>Tuesday, March 31, 2009</b>		Sheet 64 of 97





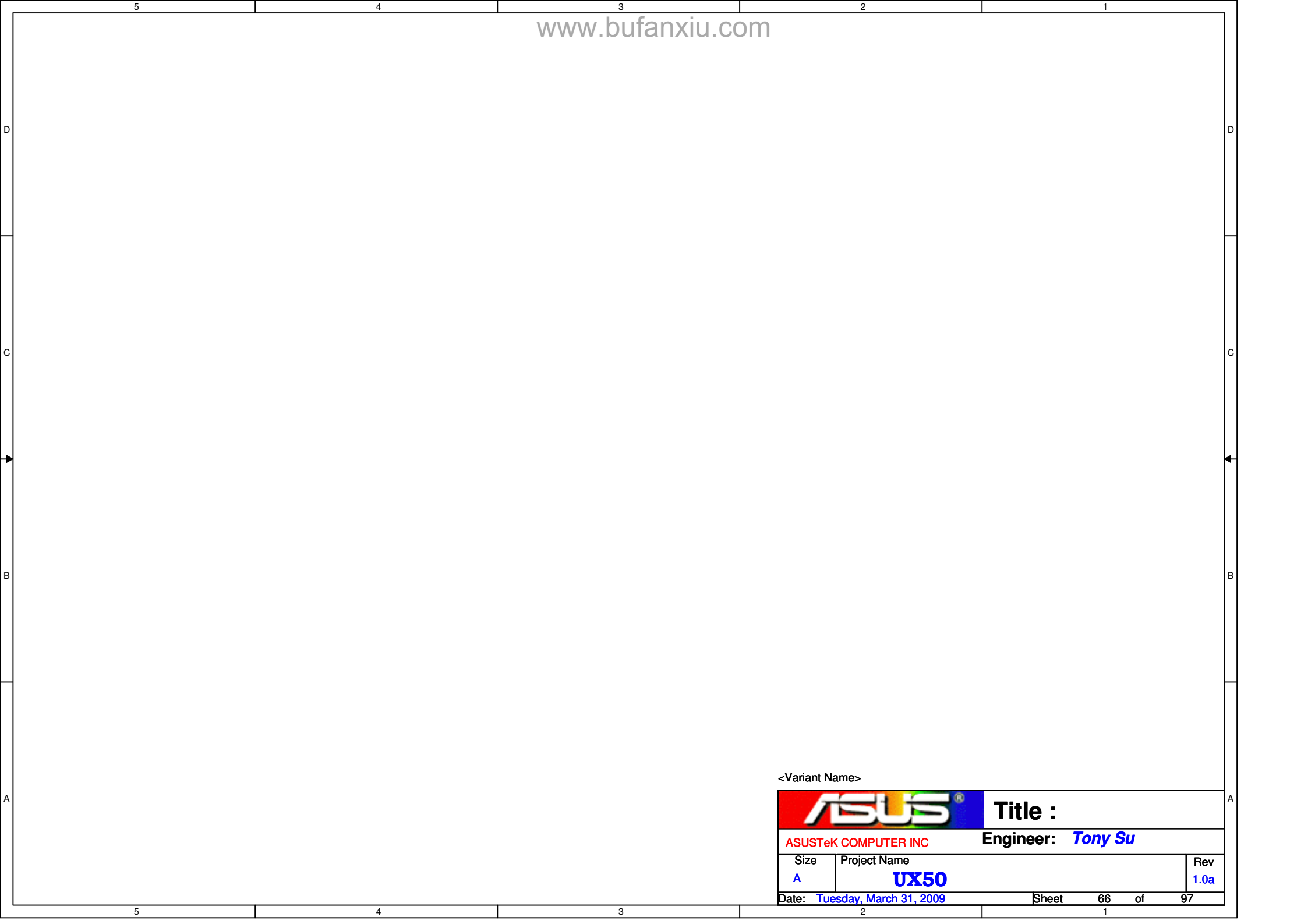
<Variant Name>

**ASUS** **ME SCREW HOLE AMT NUT**  
**Title :**


ASUSTeK COMPUTER INC **Engineer: Tony Su**

Size	Project Name	Rev
Custom	<b>UX50</b>	1.0a

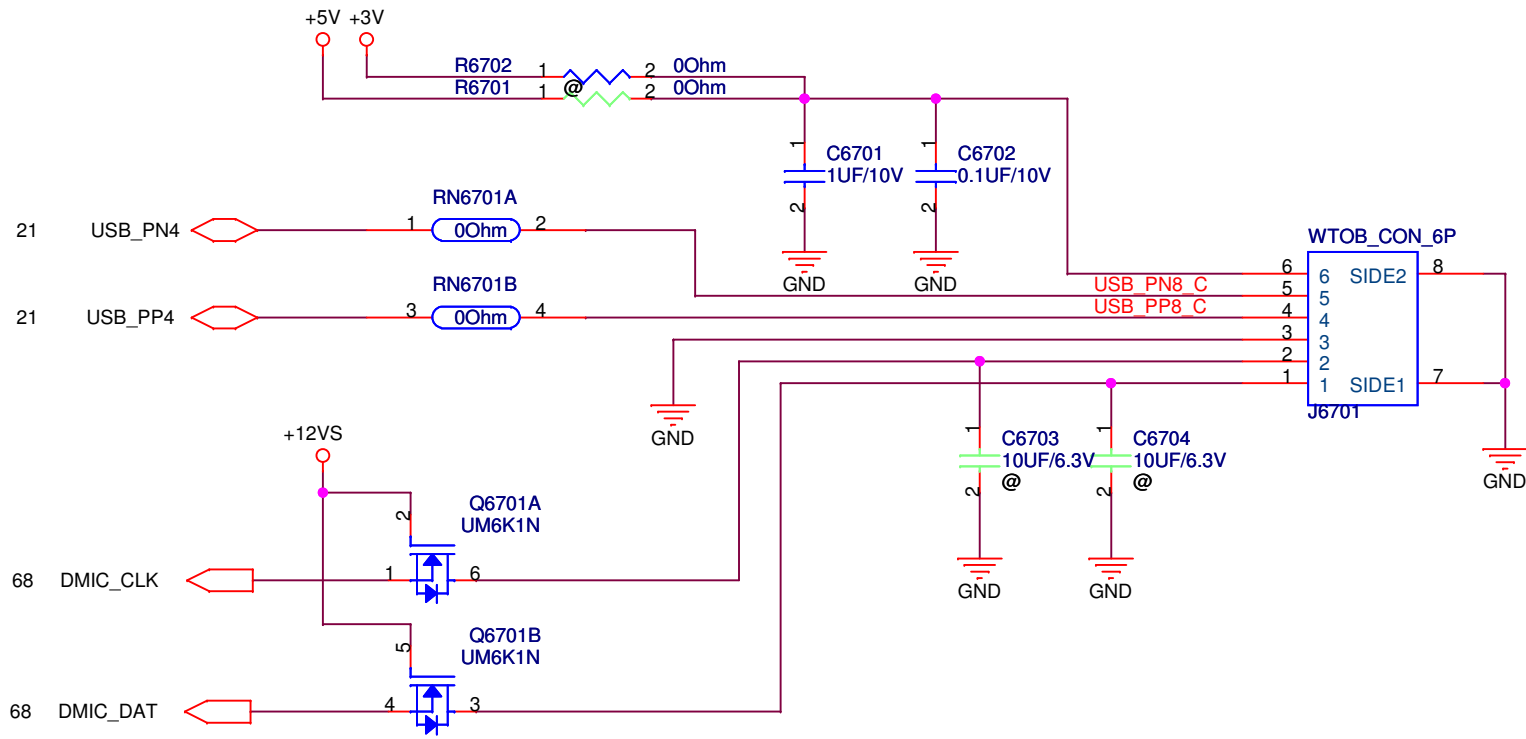
Date: **Tuesday, March 31, 2009** Sheet 65 of 97




<Variant Name>

		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 66 of 97

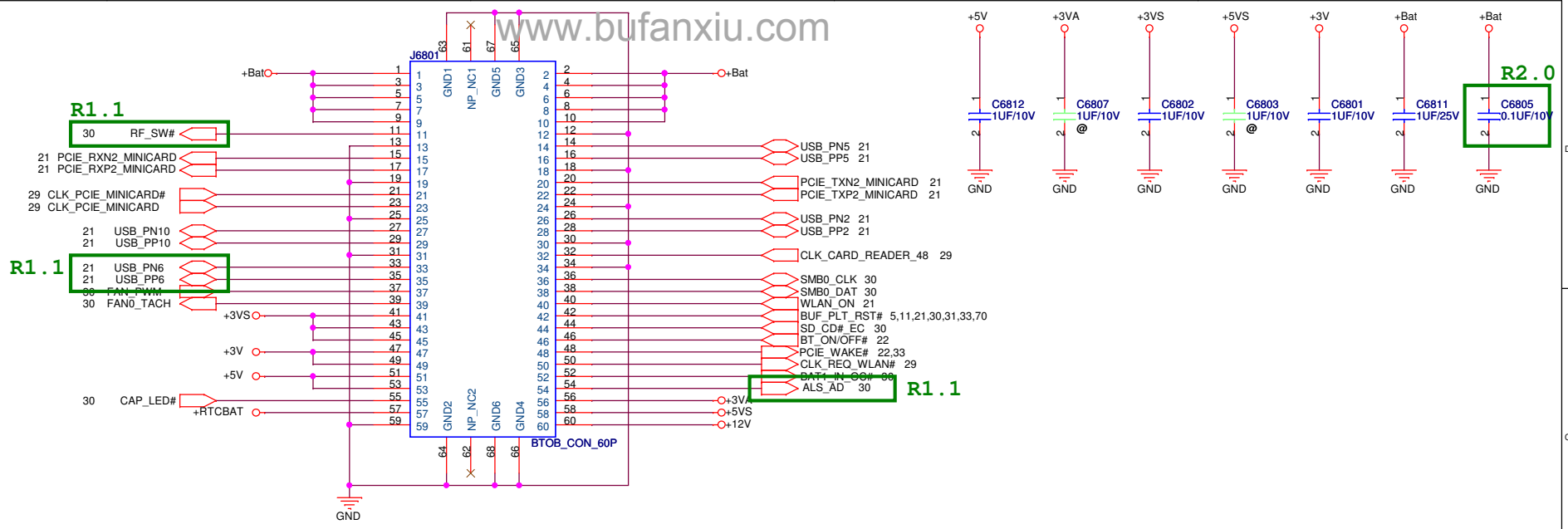
# Camera Module



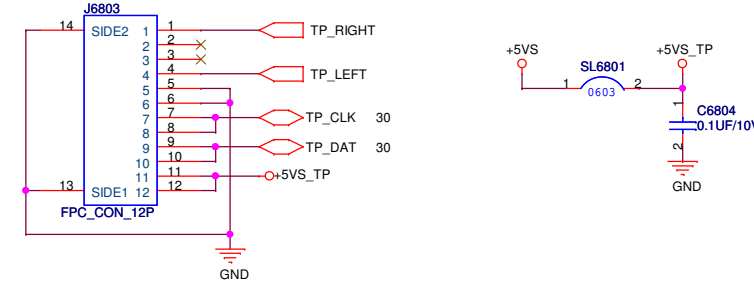
<Variant Name>

		<b>Title :</b> CMOS CAMERA
ASUSTeK COMPUTER INC		<b>Engineer:</b> Tony Su
Size A	Project Name <b>UX50</b>	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 67 of 97

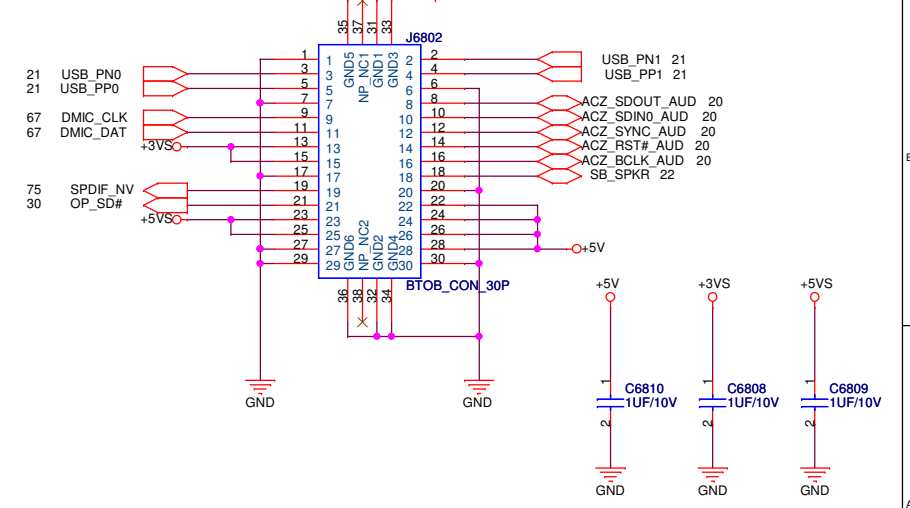
# CR Board



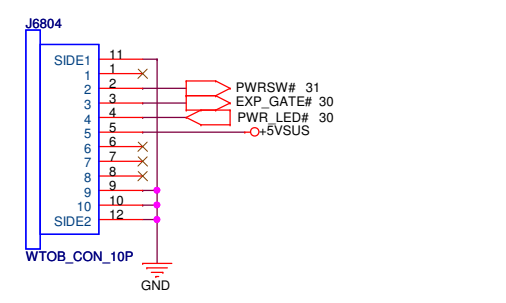
# Touch Pad Board



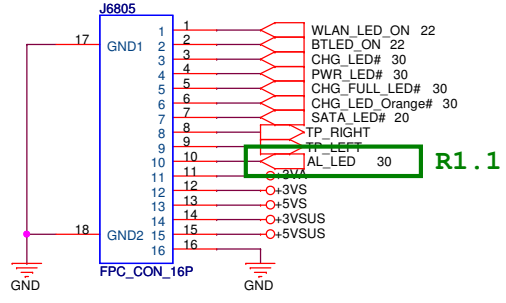
# Audio Board



# Switch Board



# LED Board



<Variant Name>

**ASUS** Title: **B TO B CONN**

ASUSTeK COMPUTER INC Engineer: **Tony Su**

Size	Project Name	Rev
B	UX50	1.0a



Date: Tuesday, March 31, 2009 Sheet 68 of 97



# SYSTEM

+VCCP   +VCCP 3,4,5,10,11,12,14,15,20,23,29,57,76,82



+VCC\_GMCH   +VCC\_GMCH 14

+VGFX\_CORE   +VGFX\_CORE 14



+3VS   +3VS 7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92

+12VS   +12VS 22,46,48,51,67,91



+VCORE   +VCORE 4,5,80

+1.5VS   +1.5VS 4,15,20,23,57,84

AC\_BAT\_SYS   AC\_BAT\_SYS 46,80,81,82,83,85,86,88

+5V   +5V 31,57,67,68,91

+5VS   +5VS 23,45,47,48,51,57,68,80,84,91



+3VA   +3VA 20,30,31,56,68,81,88

+VCC\_RTC   +VCC\_RTC 20,23

+3V   +3V 44,46,48,57,67,68,70,91

+5VA   +5VA 81

+3VSUS   +3VSUS 20,21,22,23,30,33,57,68,76,81,85,91,92

+5VSUS   +5VSUS 23,68,80,81,82,83,85,86,88,91

+3VPLL   +3VPLL 30

+3VACC   +3VACC 30

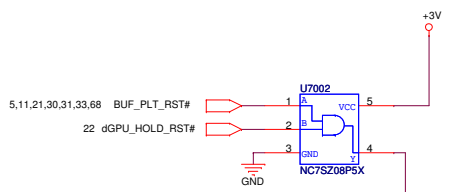
+3VA\_ECO   +3VA\_EC 30,31

+12V   +12V 68,91

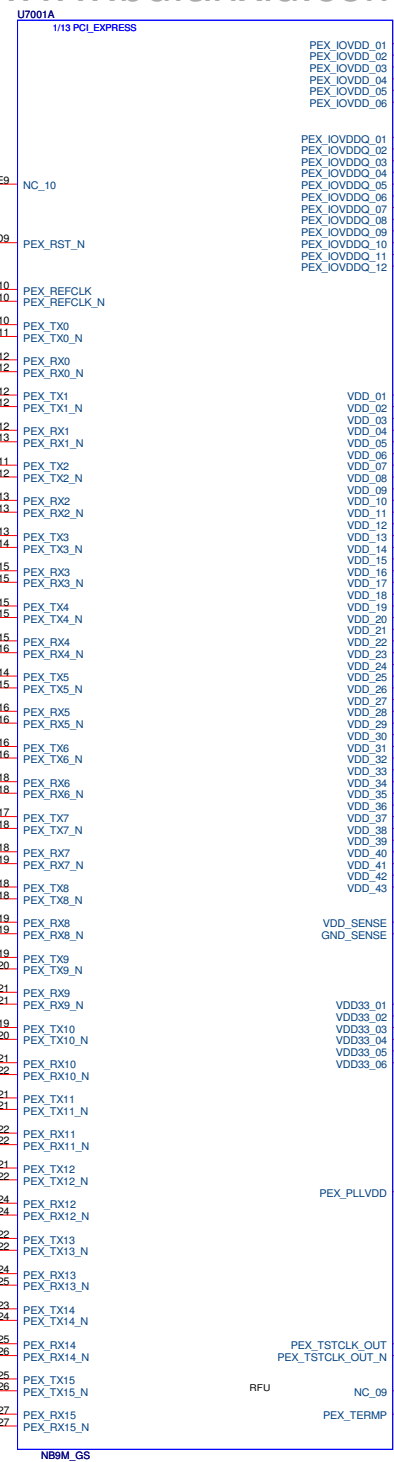
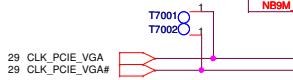
<Variant Name>

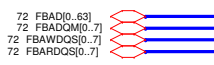
		<b>Title :</b>	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size A	Project Name <b>UX50</b>	Rev 1.0a	
Date: <b>Tuesday, March 31, 2009</b>		Sheet	69 of 97

PCIEG\_RXP[0..15] 12  
 PCIEG\_RXN[0..15] 12  
 PCIEB\_RXP[0..15] 12  
 PCIEB\_RXN[0..15] 12



PCIEB_RXN15	C7046	1	2	0.1UF/10V	PCIEG_TXN15
PCIEB_RXP15	C7062	1	2	0.1UF/10V	PCIEG_TXP15
PCIEB_RXN14	C7047	1	2	0.1UF/10V	PCIEG_TXN14
PCIEB_RXP14	C7063	1	2	0.1UF/10V	PCIEG_TXP14
PCIEB_RXN13	C7048	1	2	0.1UF/10V	PCIEG_TXN13
PCIEB_RXP13	C7064	1	2	0.1UF/10V	PCIEG_TXP13
PCIEB_RXN12	C7049	1	2	0.1UF/10V	PCIEG_TXN12
PCIEB_RXP12	C7065	1	2	0.1UF/10V	PCIEG_TXP12
PCIEB_RXN11	C7050	1	2	0.1UF/10V	PCIEG_TXN11
PCIEB_RXP11	C7066	1	2	0.1UF/10V	PCIEG_TXP11
PCIEB_RXN10	C7051	1	2	0.1UF/10V	PCIEG_TXN10
PCIEB_RXP10	C7067	1	2	0.1UF/10V	PCIEG_TXP10
PCIEB_RXN9	C7052	1	2	0.1UF/10V	PCIEG_TXN9
PCIEB_RXP9	C7068	1	2	0.1UF/10V	PCIEG_TXP9
PCIEB_RXN8	C7053	1	2	0.1UF/10V	PCIEG_TXN8
PCIEB_RXP8	C7069	1	2	0.1UF/10V	PCIEG_TXP8
PCIEB_RXN7	C7054	1	2	0.1UF/10V	PCIEG_TXN7
PCIEB_RXP7	C7070	1	2	0.1UF/10V	PCIEG_TXP7
PCIEB_RXN6	C7055	1	2	0.1UF/10V	PCIEG_TXN6
PCIEB_RXP6	C7071	1	2	0.1UF/10V	PCIEG_TXP6
PCIEB_RXN5	C7056	1	2	0.1UF/10V	PCIEG_TXN5
PCIEB_RXP5	C7072	1	2	0.1UF/10V	PCIEG_TXP5
PCIEB_RXN4	C7057	1	2	0.1UF/10V	PCIEG_TXN4
PCIEB_RXP4	C7073	1	2	0.1UF/10V	PCIEG_TXP4
PCIEB_RXN3	C7058	1	2	0.1UF/10V	PCIEG_TXN3
PCIEB_RXP3	C7074	1	2	0.1UF/10V	PCIEG_TXP3
PCIEB_RXN2	C7059	1	2	0.1UF/10V	PCIEG_TXN2
PCIEB_RXP2	C7075	1	2	0.1UF/10V	PCIEG_TXP2
PCIEB_RXN1	C7060	1	2	0.1UF/10V	PCIEG_TXN1
PCIEB_RXP1	C7076	1	2	0.1UF/10V	PCIEG_TXP1
PCIEB_RXN0	C7061	1	2	0.1UF/10V	PCIEG_TXN0
PCIEB_RXP0	C7077	1	2	0.1UF/10V	PCIEG_TXP0

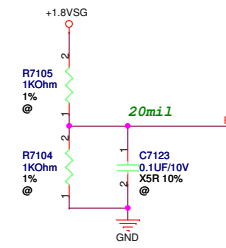
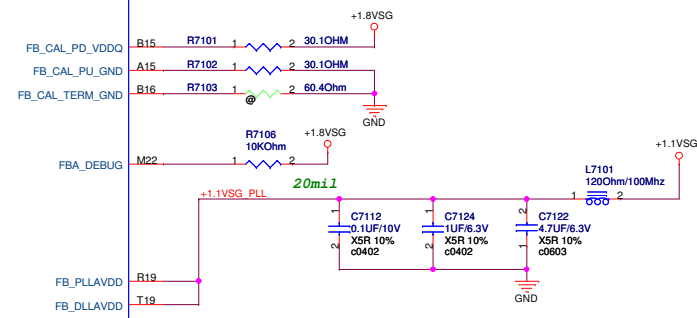
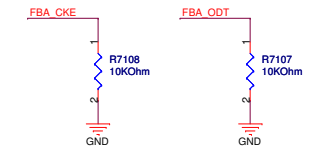
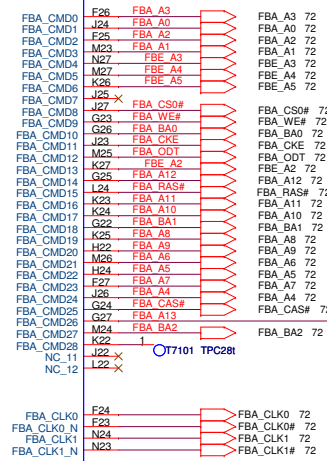
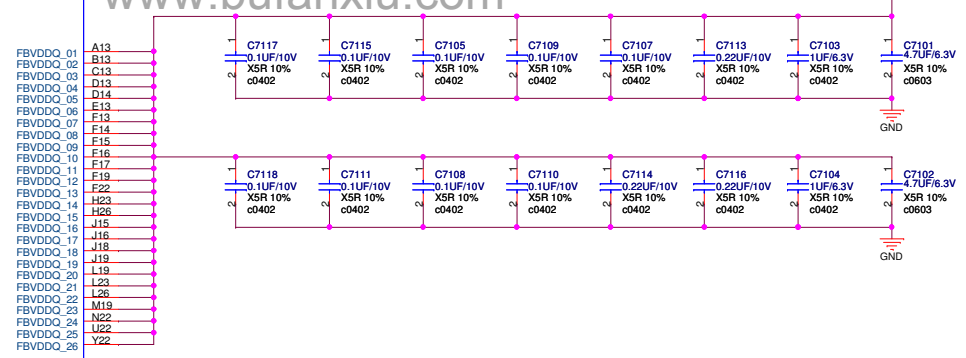


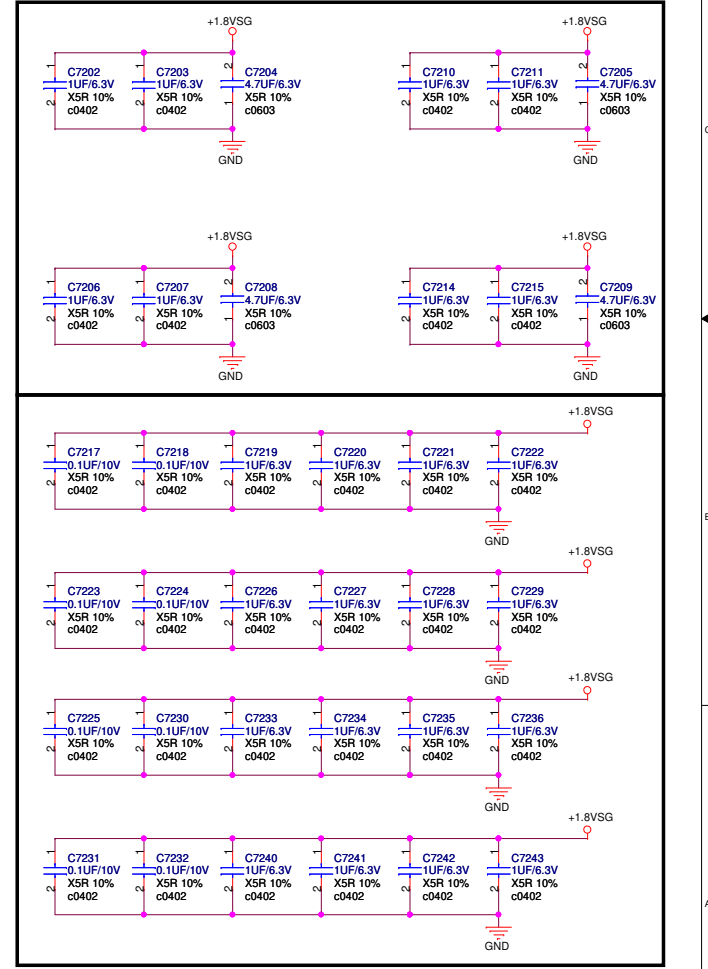
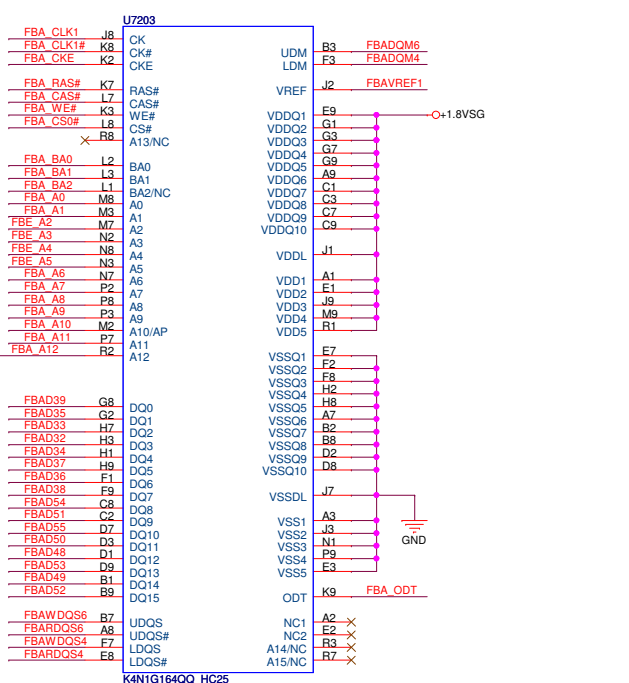
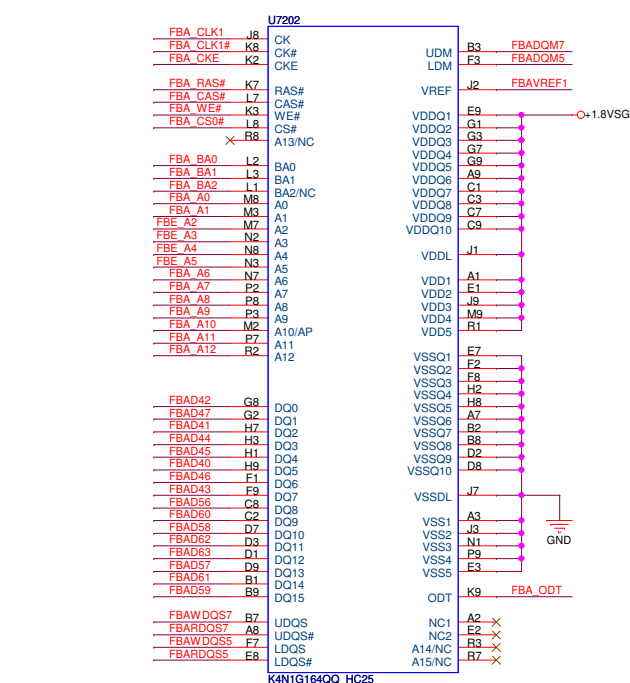
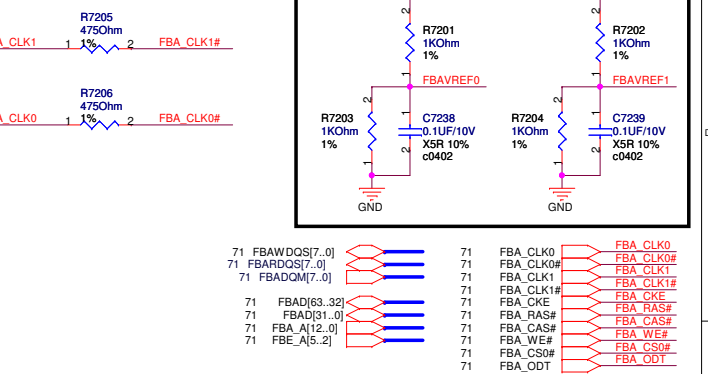
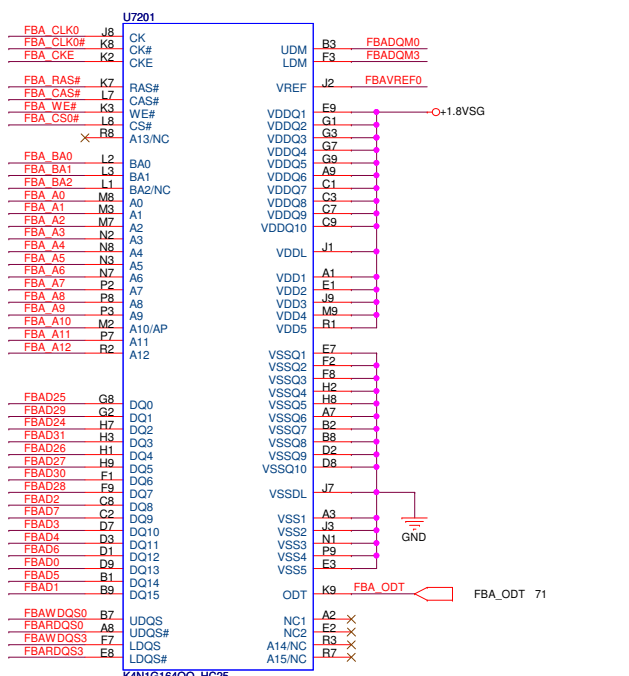
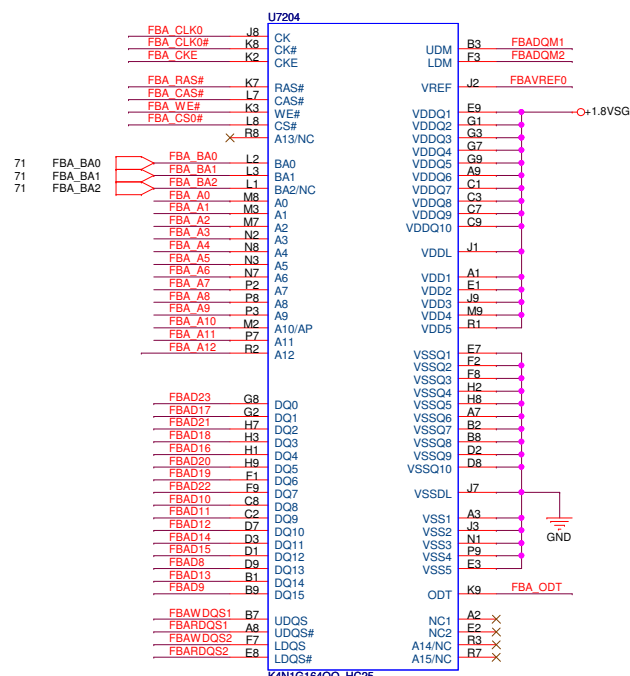


U7001B 2/13 FRAME\_BUFFER

- Pin list for U7001B: FBA\_D0 to FBA\_D63, FBA\_CMD0 to FBA\_CMD28, FBA\_CMD29 to FBA\_CMD38, FBA\_CMD39 to FBA\_CMD47, FBA\_CMD48 to FBA\_CMD57, FBA\_CMD58 to FBA\_CMD62, FBA\_CMD25 to FBA\_CMD28, FBA\_CMD29 to FBA\_CMD38, FBA\_CMD39 to FBA\_CMD47, FBA\_CMD48 to FBA\_CMD57, FBA\_CMD58 to FBA\_CMD62.

- Pin list for FBADQM and FBARDQS: FBADQM0 to FBADQM7, FBARDQS0 to FBARDQS7, FBA\_DQS\_WP0 to FBA\_DQS\_WP7, FBA\_DQS\_RN0 to FBA\_DQS\_RN7.





**ASUS** Title :  
ASUSTek COMPUTER INC. NB1 Engineer: Tony Su

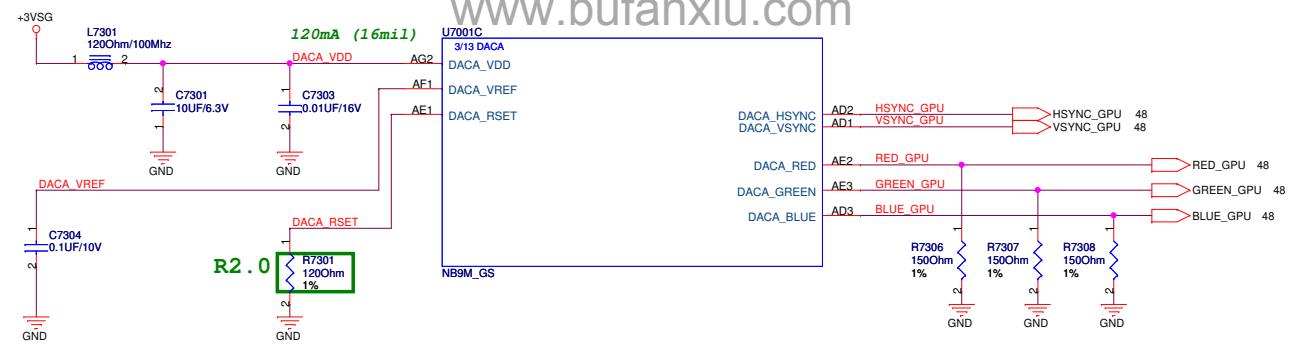
Size Project Name  
Custom UX50

Date: Monday, April 06, 2009 Sheet 72 of 97

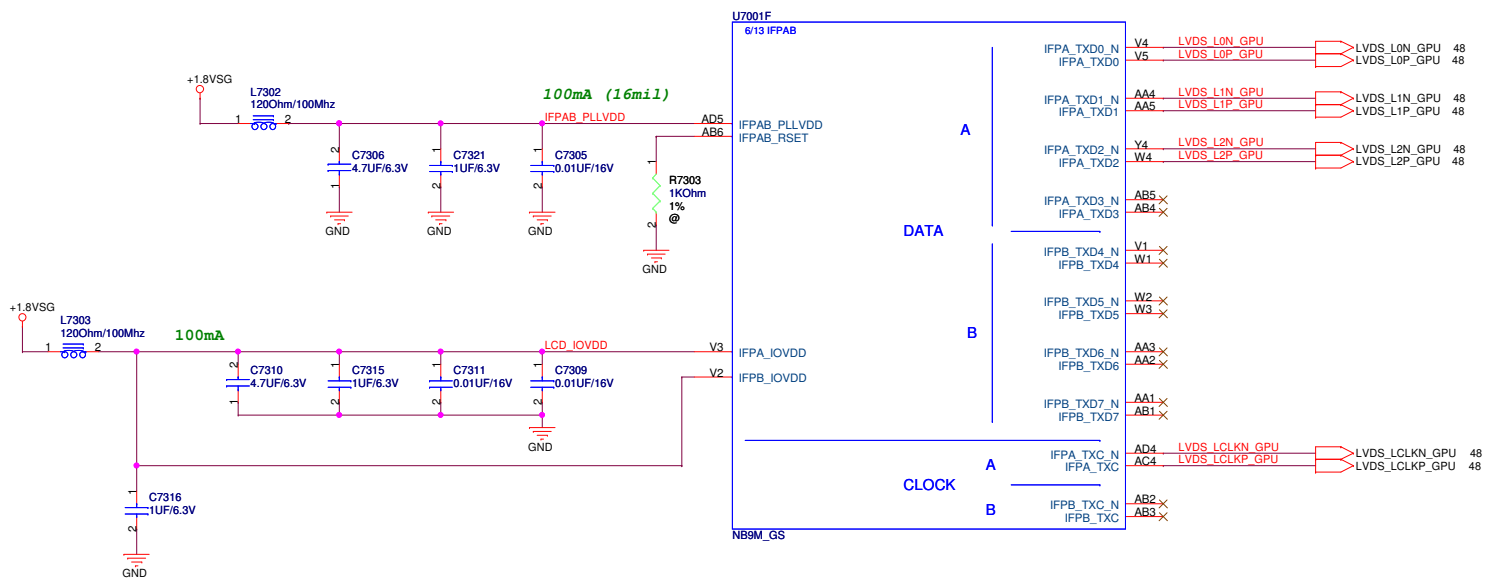
Rev 2.2



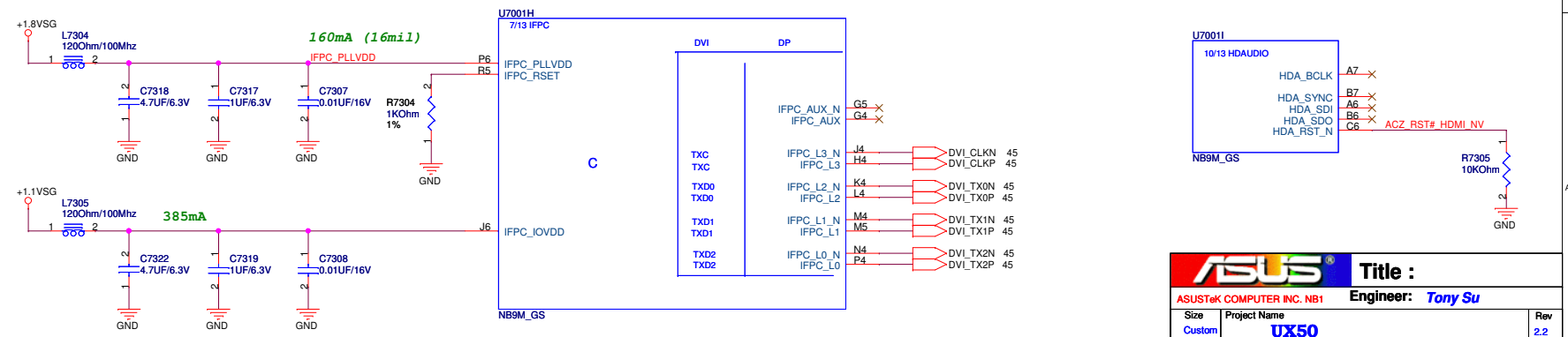
### VGA



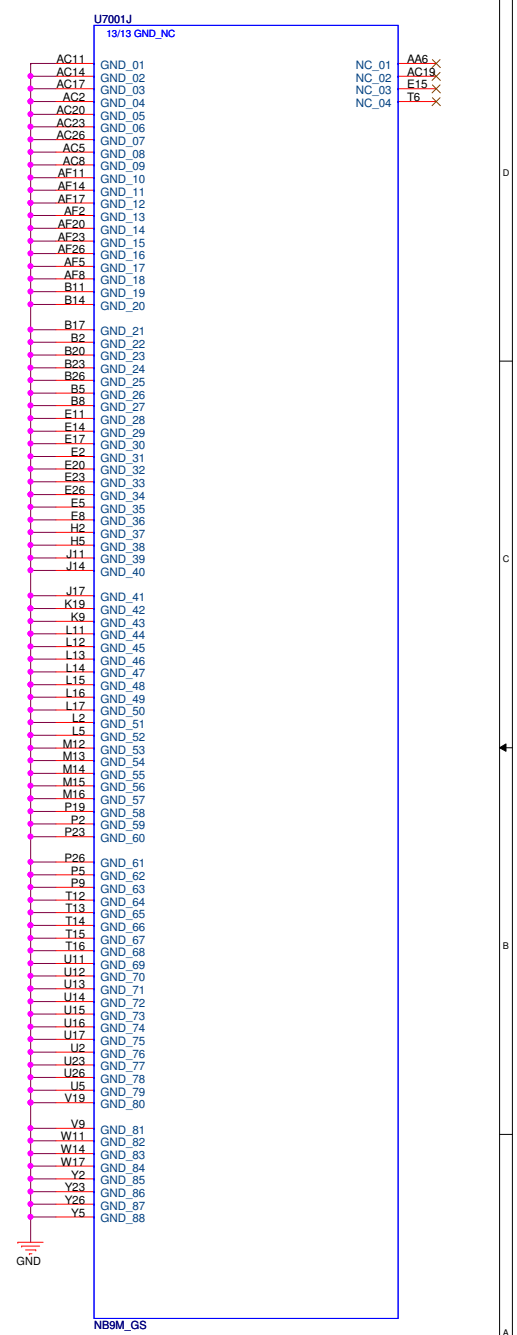
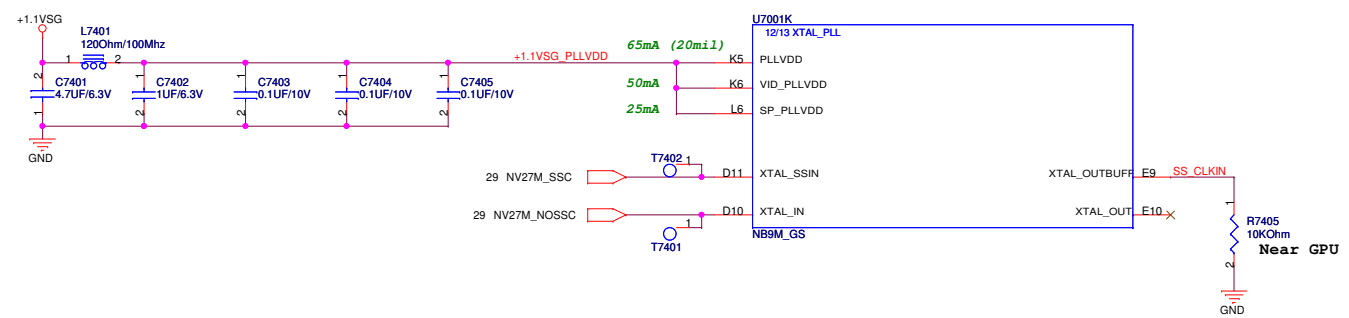
### LVDS



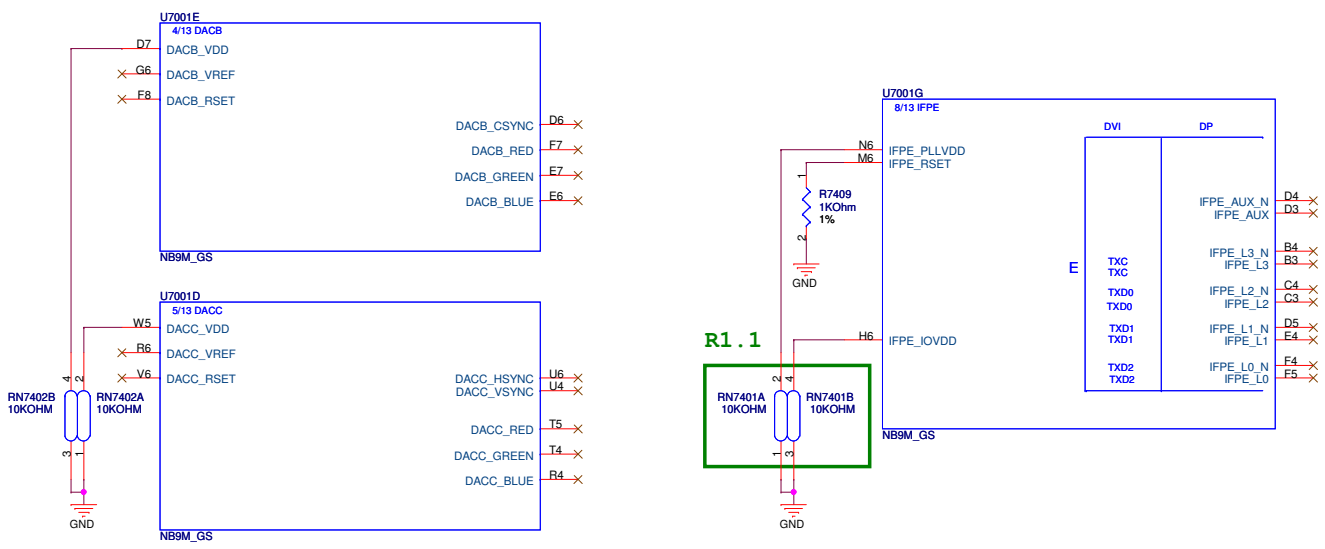
### HDMI



### Xtal

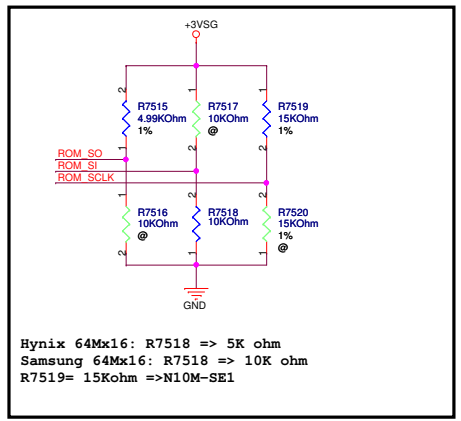
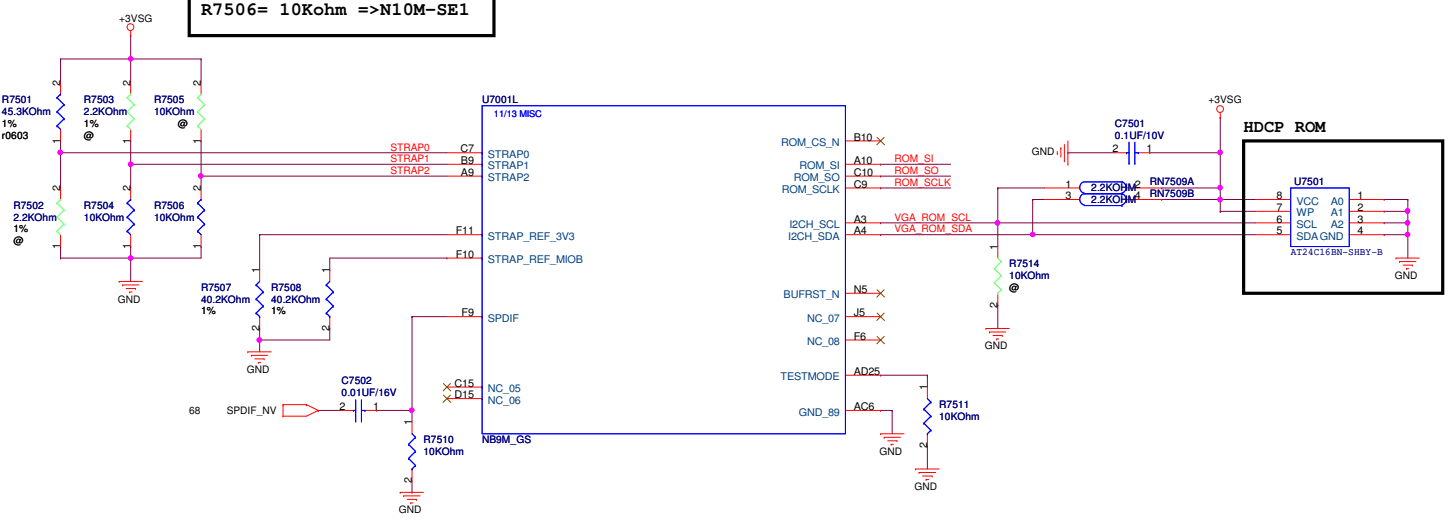


### Other



ROM

R7506= 10Kohm =>N10M-SE1

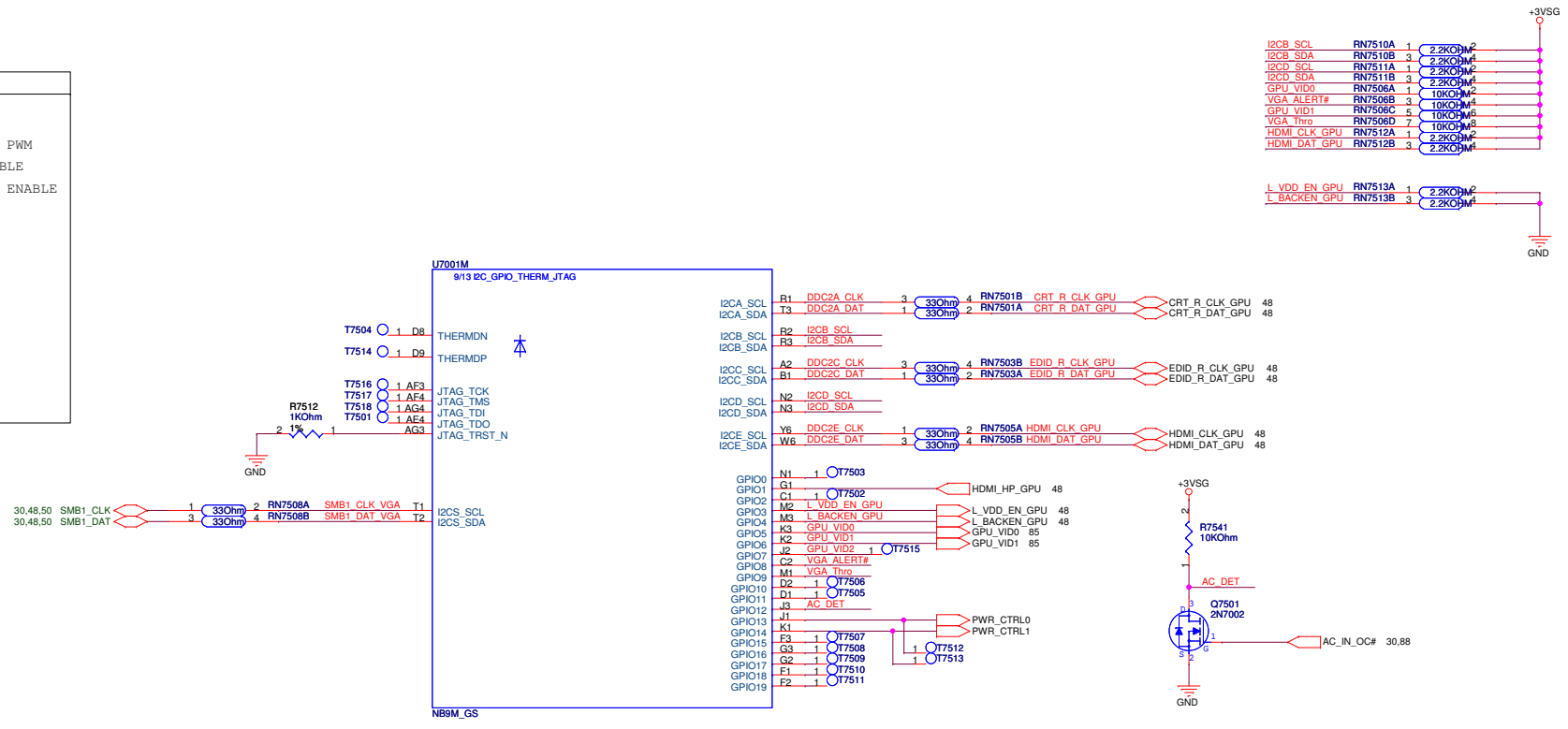


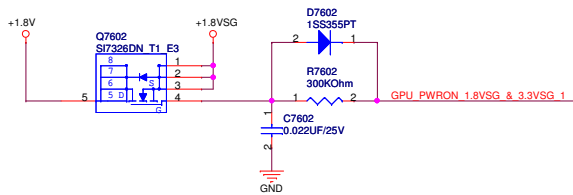
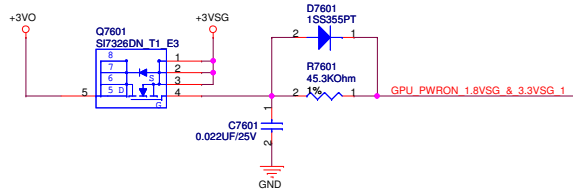
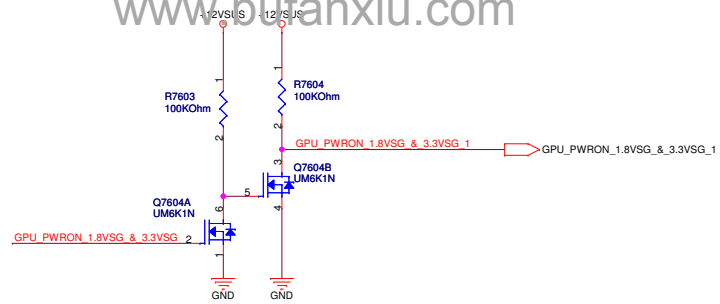
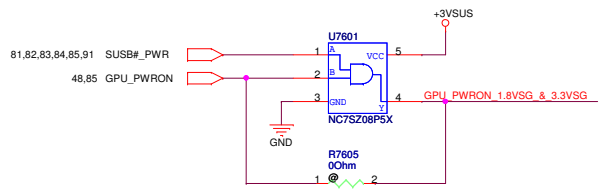
Hynix 64Mx16: R7518 => 5K ohm  
 Samsung 64Mx16: R7518 => 10K ohm  
 R7519= 15Kohm =>N10M-SE1

GPIO

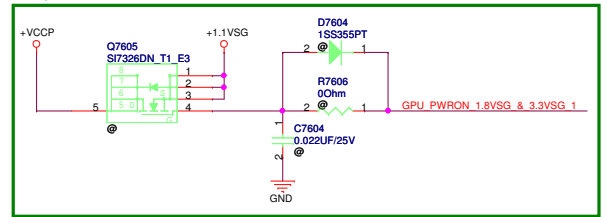
GPIO ASSIGNMENTS

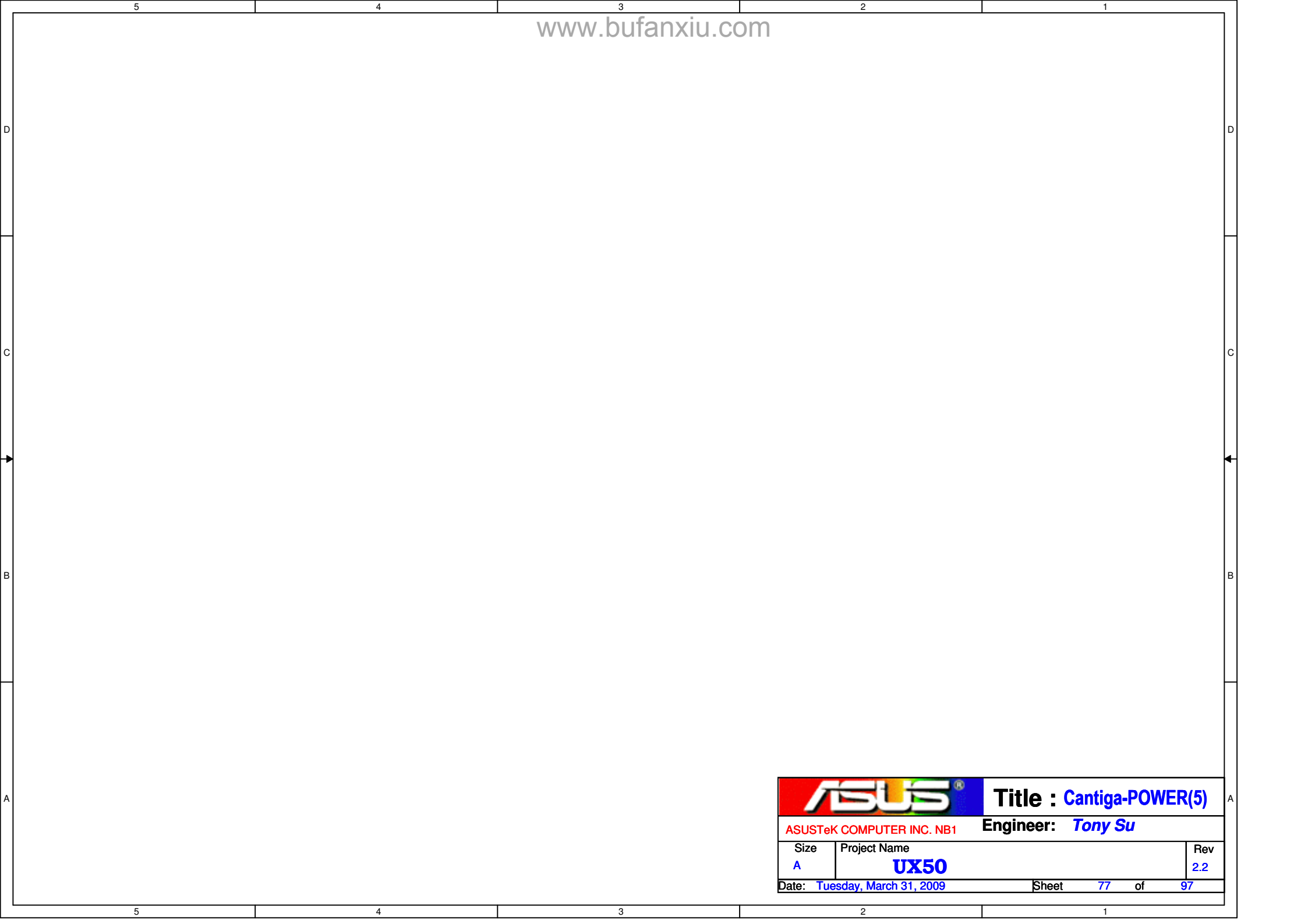
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL




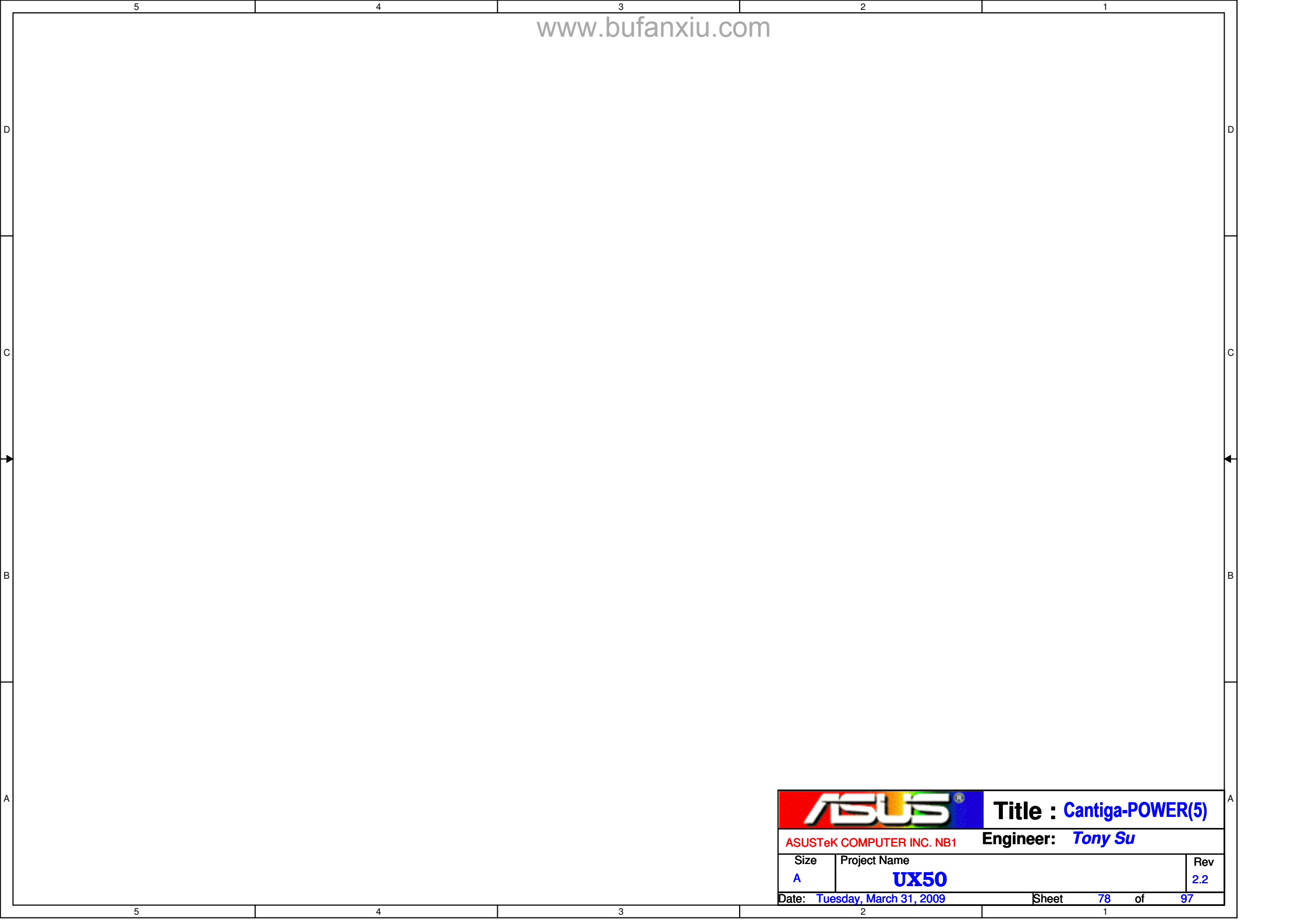



R1.1

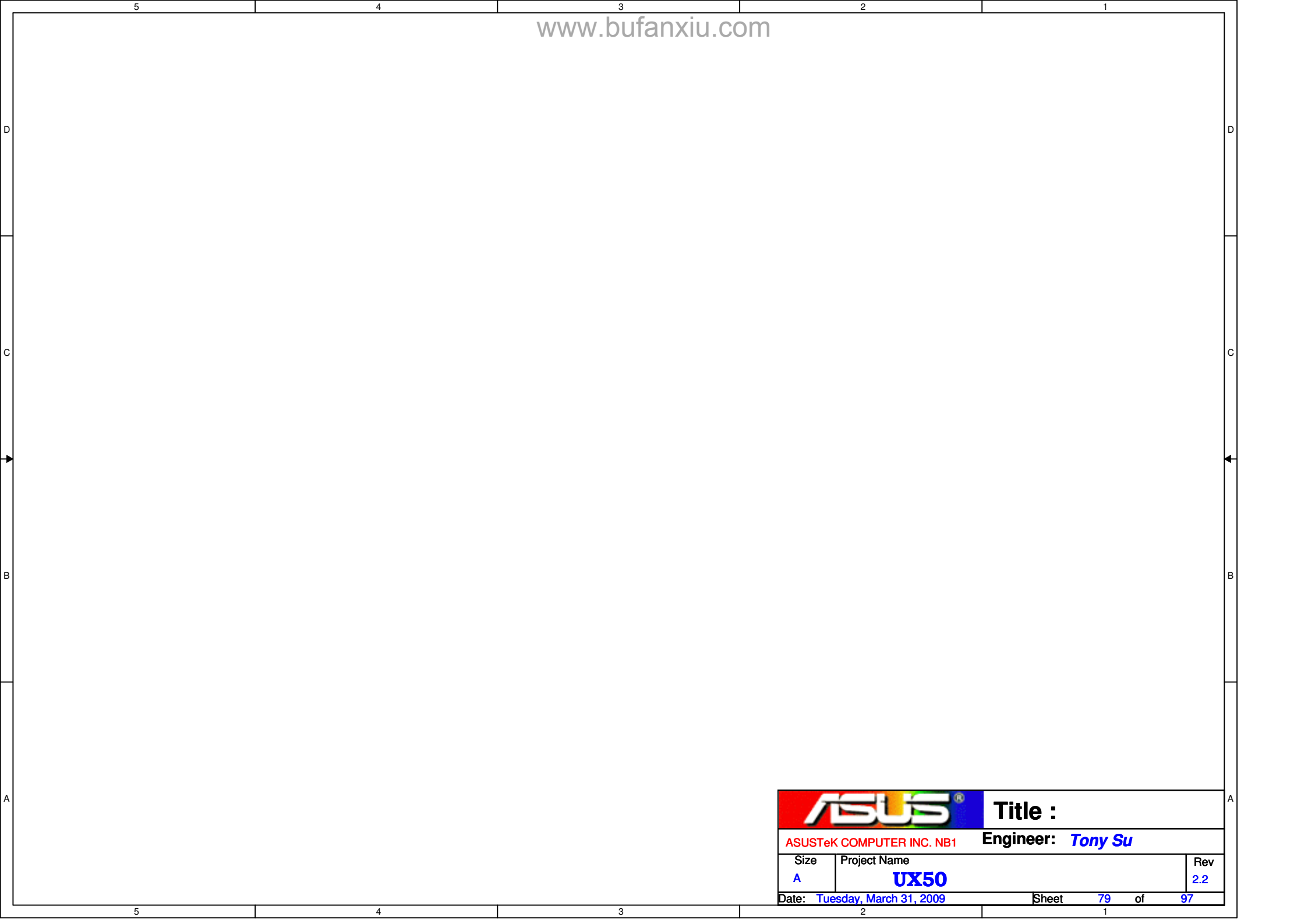





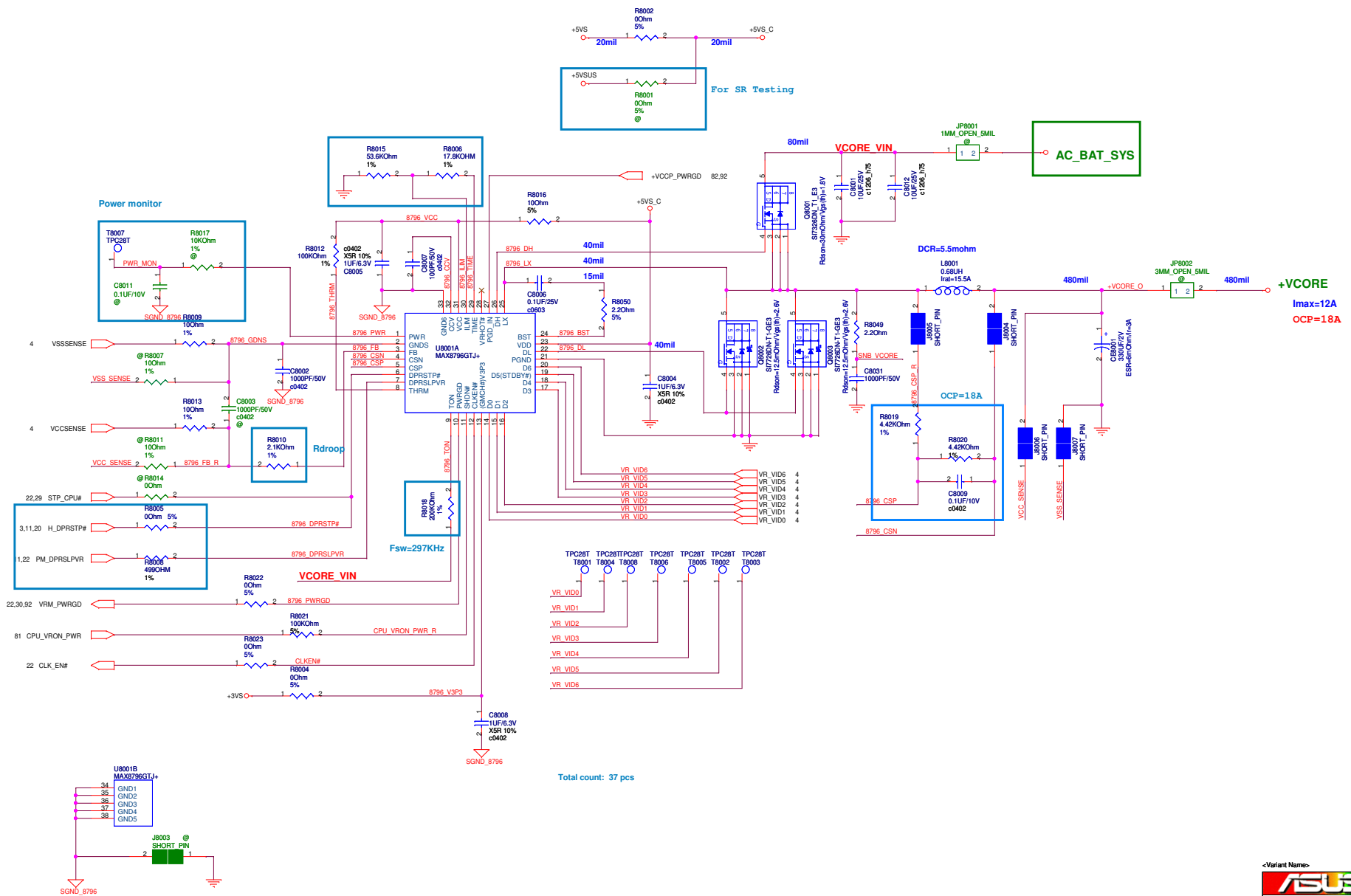
		<b>Title : Cantiga-POWER(5)</b>
ASUSTeK COMPUTER INC. NB1		<b>Engineer: Tony Su</b>
Size A	Project Name <b>UX50</b>	Rev 2.2
Date: <b>Tuesday, March 31, 2009</b>		Sheet <b>77</b> of <b>97</b>



		<b>Title :</b> Cantiga-POWER(5)
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <i>Tony Su</i>
Size A	Project Name <b>UX50</b>	Rev 2.2
Date: <b>Tuesday, March 31, 2009</b>		Sheet <b>78</b> of <b>97</b>



		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <i>Tony Su</i>	
Size	Project Name	Rev	
A	<b>UX50</b>	2.2	
Date: <i>Tuesday, March 31, 2009</i>		Sheet	79 of 97

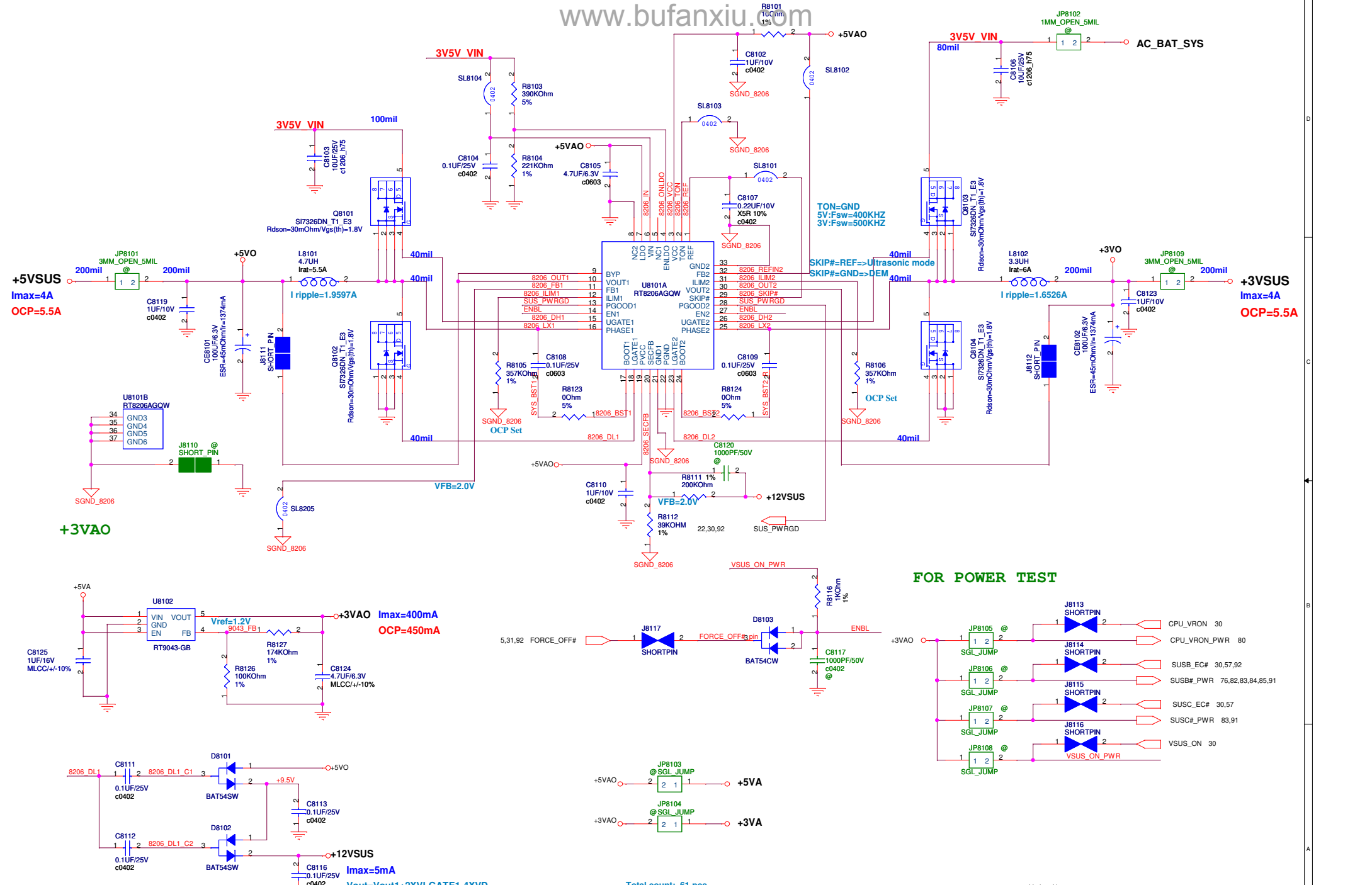


Total count: 37 pcs

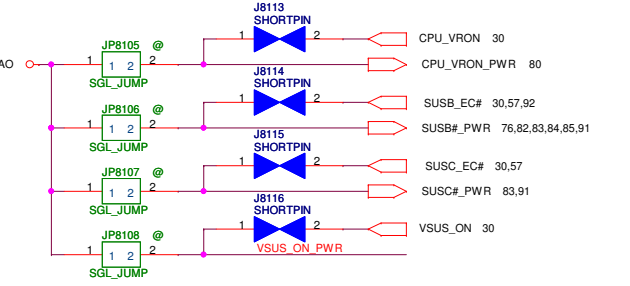
<Variant Names>

<b>ASUS</b>		<b>Title : +Vcore</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: Morris/Eric	
Size	Project Name	Rev	
Custom	UX50	1.0	
Date: Tuesday, March 31, 2009	Sheet	80	of 97

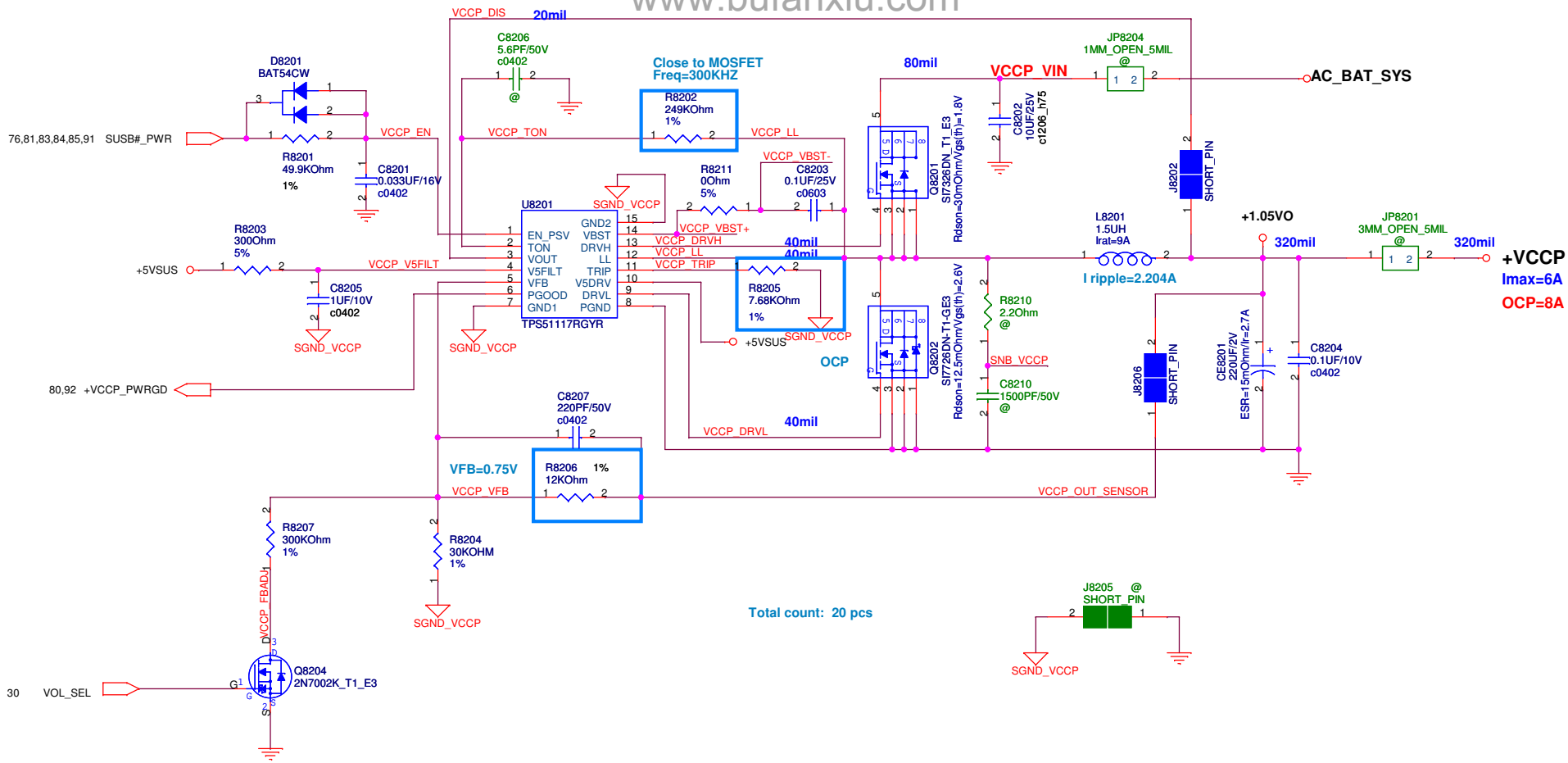




FOR POWER TEST



Total count: 61 pcs

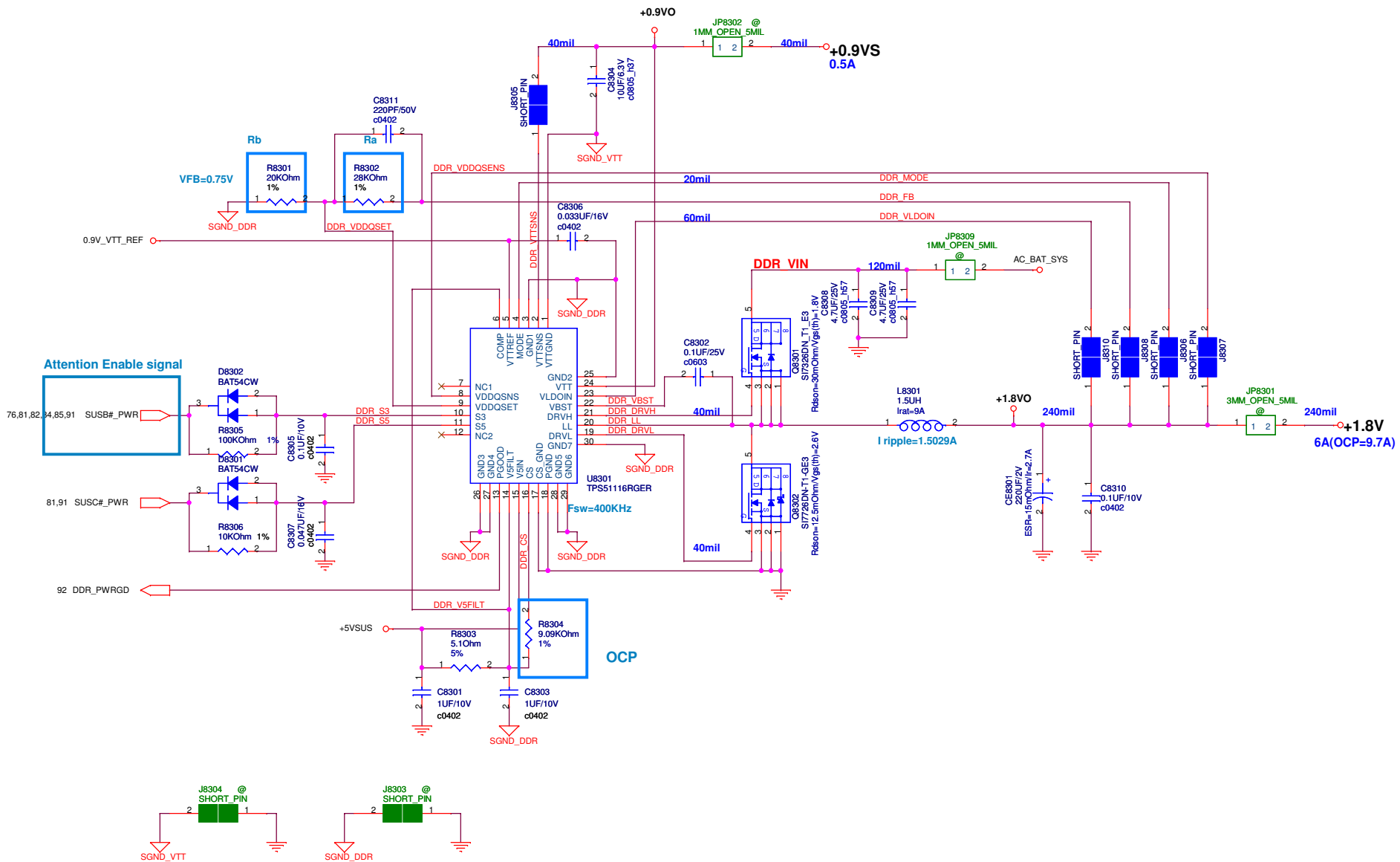


Total count: 20 pcs

VOL\_SEL:High VOLTAGE=1.080V  
 VOL\_SEL:Low VOLTAGE=1.050V

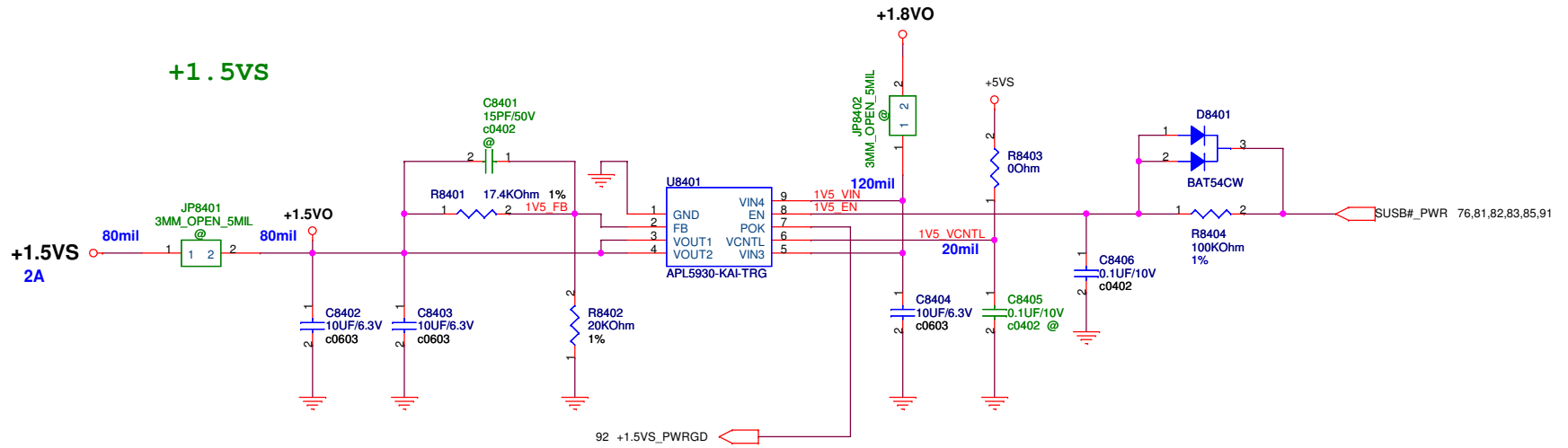
<Variant Name>

<b>ASUS</b>		<b>Title :POWER_IO_+VCCP</b>	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size B	Project Name <b>UX50</b>	Rev 1.0	
Date: Tuesday, March 31, 2009		Sheet 82 of 97	



<Variant Name>

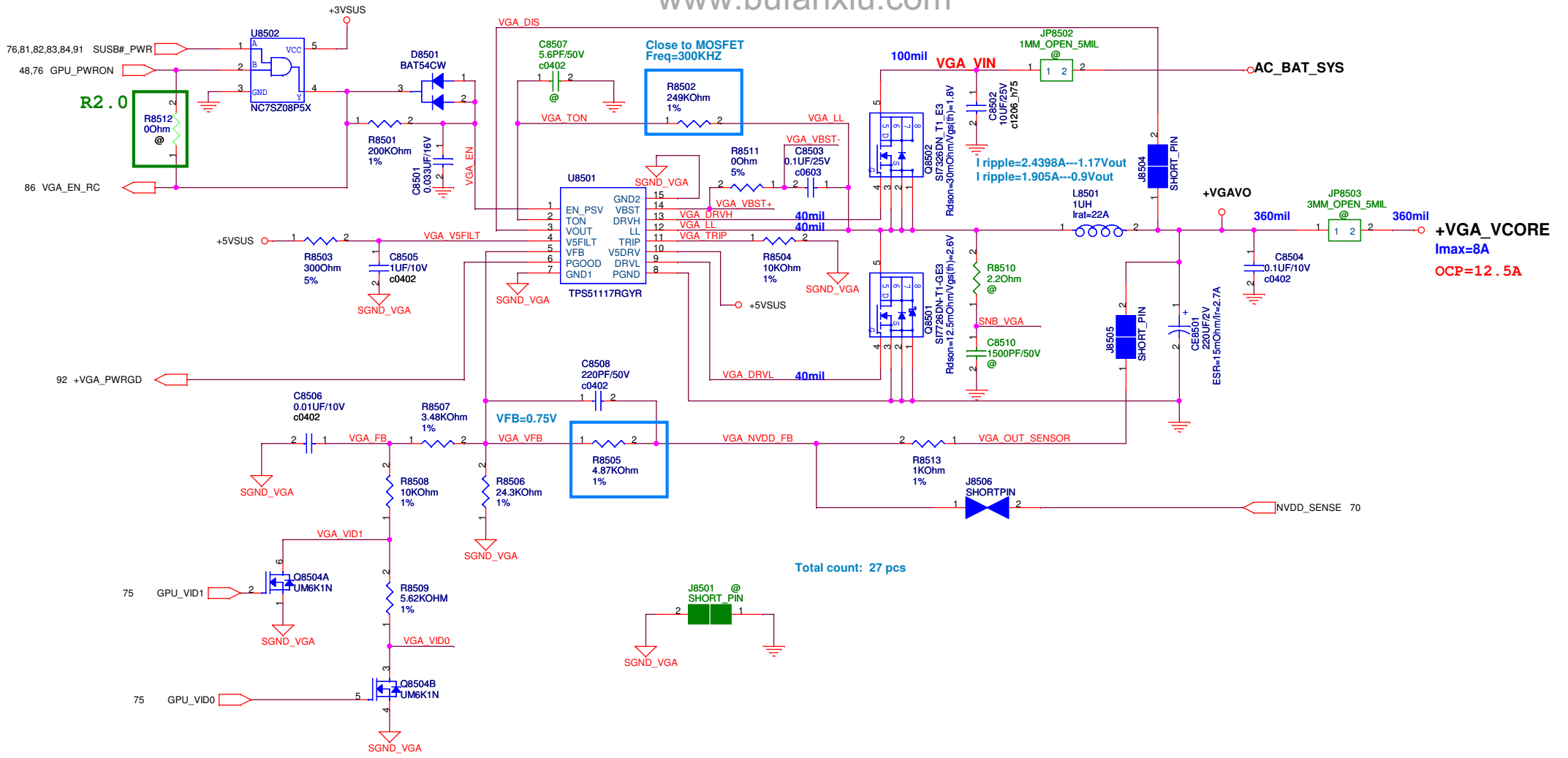
		Title : POWER_I/O_DDR & VTT	
ASUSTek COMPUTER INC. NB		Engineer: Morris/Eric	
Size Custom	Project Name <b>UX50</b>	Rev 1.0	
Date: Tuesday, March 31, 2009	Sheet	83	of 97



Total count: 12 pcs

LDO Second source APL5913-KAC-TRL

<Variant Name>		
		Title :POWER_I/O_+1.5VS
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric
Size	Project Name	Rev
B	UX50	1.0
Date: Tuesday, March 31, 2009		Sheet 84 of 97

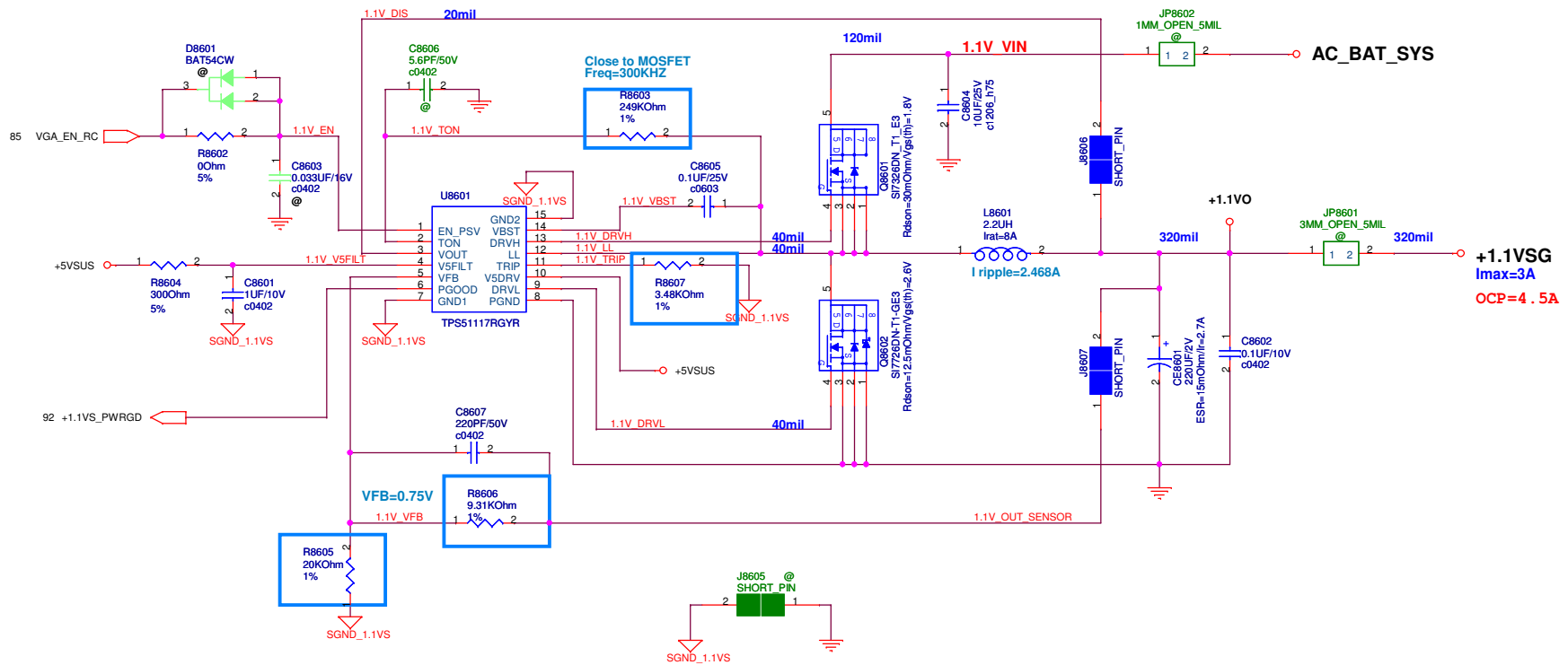


Total count: 27 pcs

GPU_VID0	GPU_VID1	+VGA_VCORE
H	H	1.17V
H	L	1.09V
L	L	0.9V
L	H	1.17V

<Variant Name>

<b>ASUS</b>		<b>Title :POWER_I/O_VGA</b>
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric
Size B	Project Name <b>UX50</b>	Rev 1.0
Date: Tuesday, March 31, 2009		Sheet 85 of 97



<Variant Name>

		<b>Title : POWER_I/O_1.1VS</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris/Eric</i>	
Size	Project Name	UX50	Rev
Custom			1.0
Date: Tuesday, March 31, 2009		Sheet	86 of 97

5

4

3

2

1

D

D

C

C

B

B

A

A



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, March 31, 2009	Sheet 87 of 97

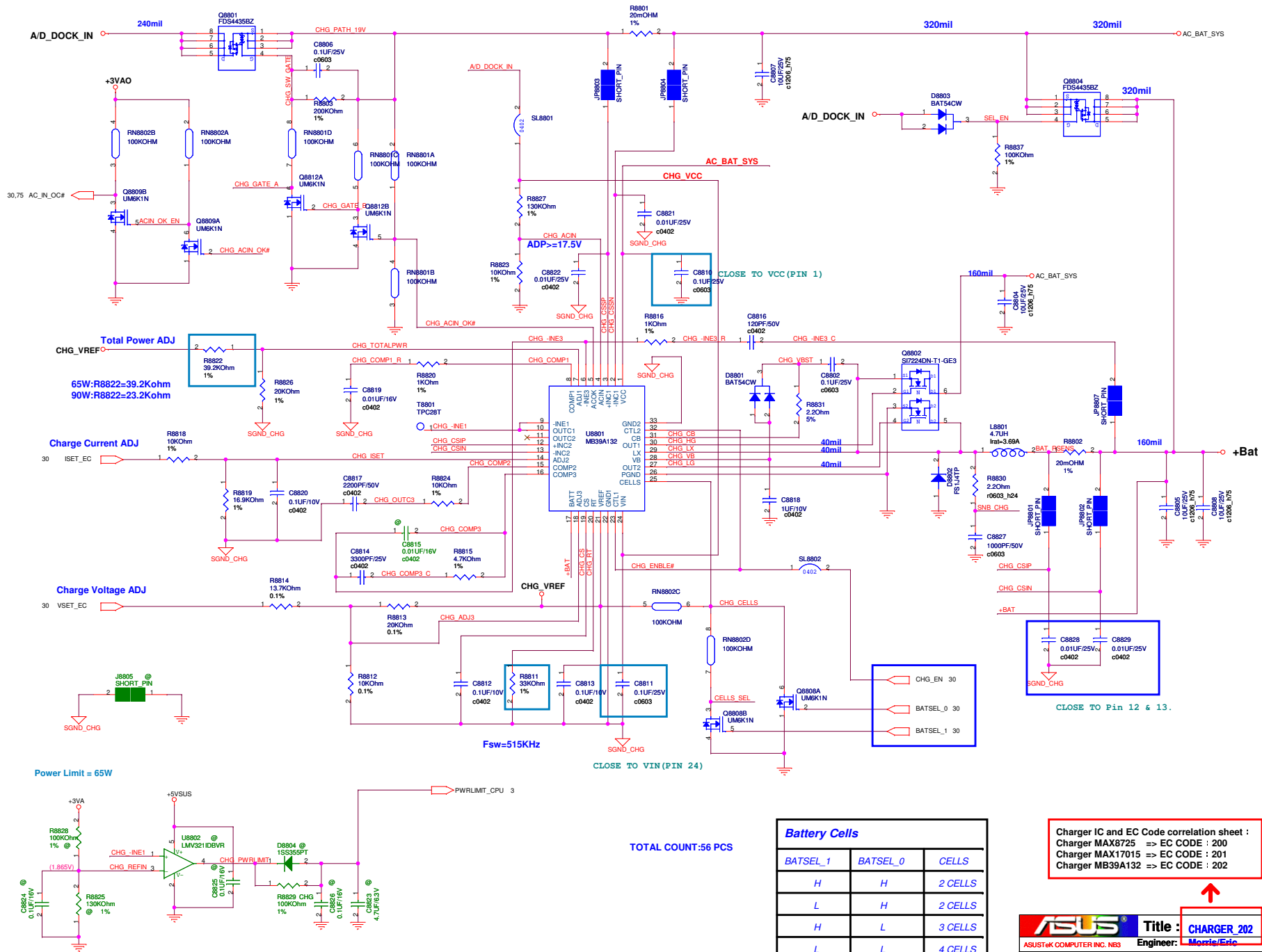
5

4

3

2

1



**Battery Cells**

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS


Charger IC and EC Code correlation sheet :  
 Charger MAX8725 => EC CODE : 200  
 Charger MAX17015 => EC CODE : 201  
 Charger MB39A132 => EC CODE : 202



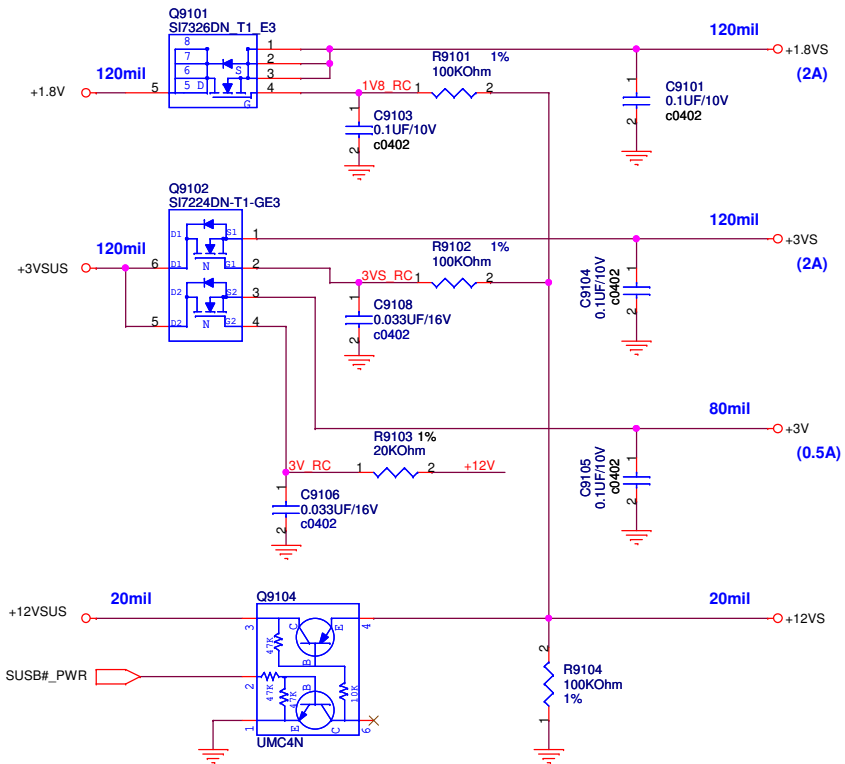


BATTERY IN DETECT

<Variant Name>

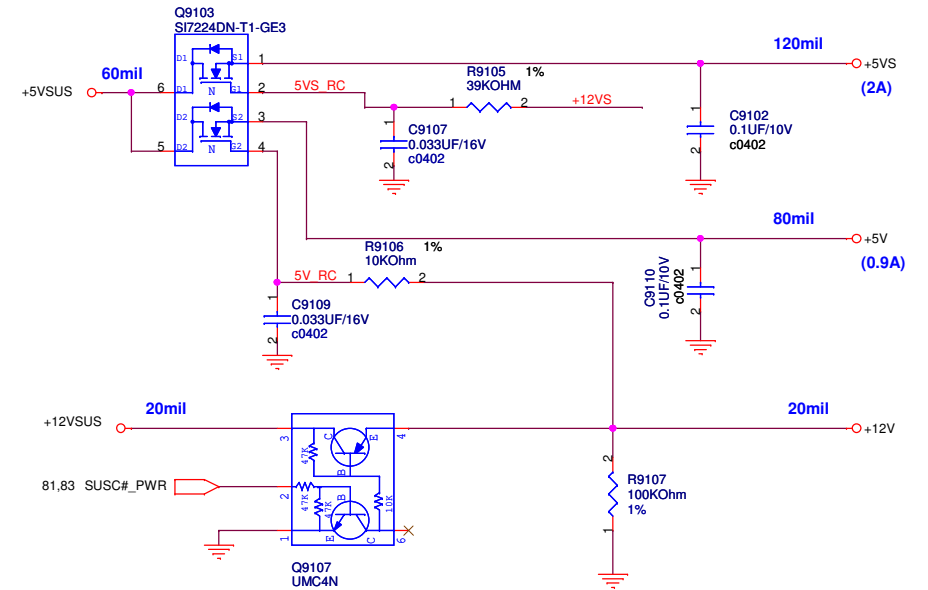
		<b>Title : POWER_DETECT</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris/Eric</i>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0	
Date: <i>Tuesday, March 31, 2009</i>		Sheet	90 of 97

SUSB#\_PWR POWER



Total count: 20 pcs

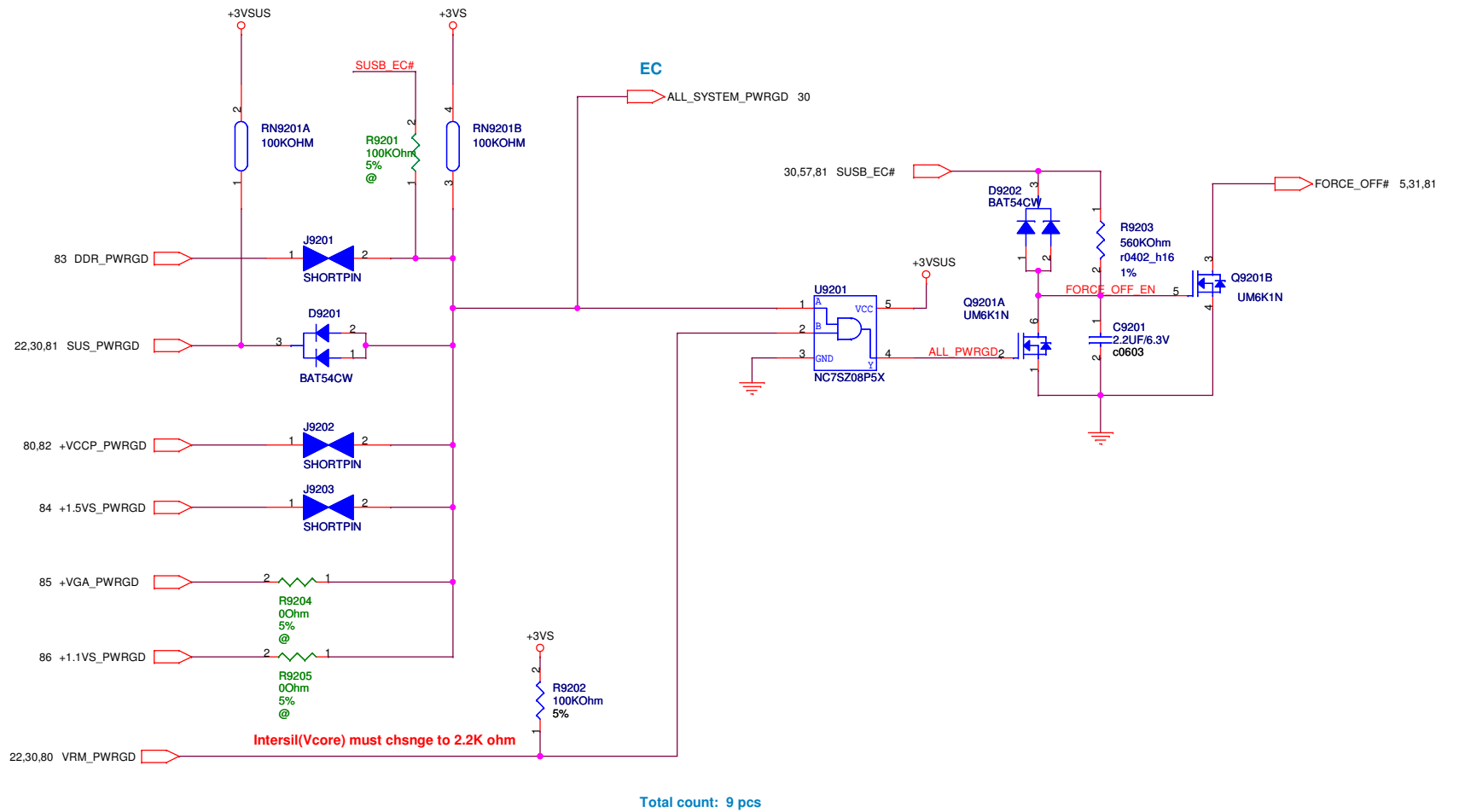
SUSC#\_PWR POWER



<Variant Name>

<b>ASUS</b>		<b>Title :POWER_LOAD SWITCH</b>	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size B	Project Name UX50	Date Tuesday, March 31, 2009	Rev 1.0
		Sheet 91	of 97

# POWER GOOD DETECTOR




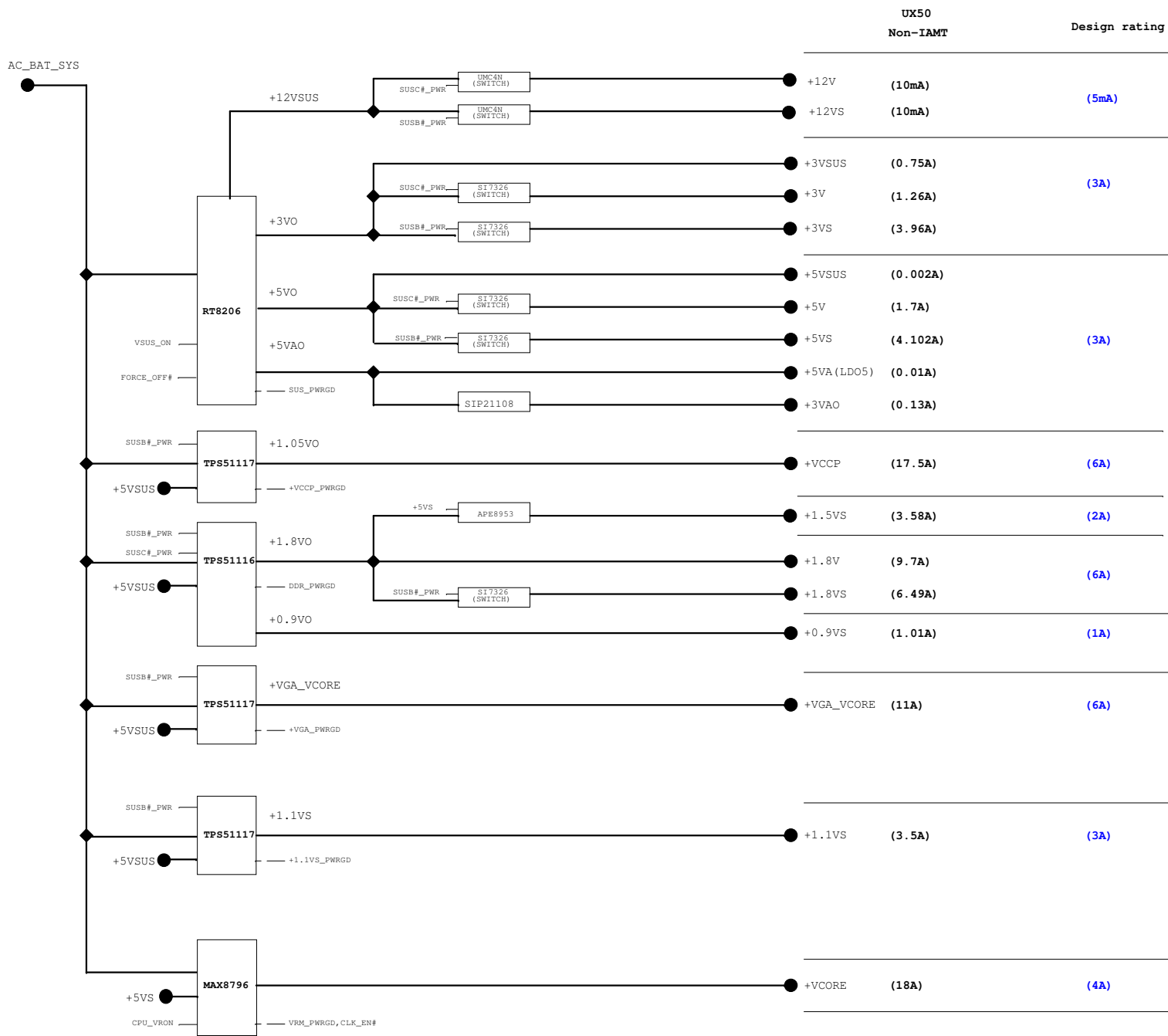
<Variant Name>		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size	Project Name	Rev	
B	UX50	1.0	
Date: Tuesday, March 31, 2009		Sheet 92 of 97	

AC_BAT_SYS	AC_BAT_SYS	46,80,81,82,83,85,86,88
+BAT	+BAT	68,88
+3VAO	+3VAO	81,88
+5VA	+5VA	81
+3VA	+3VA	20,30,31,56,68,81,88
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	23,68,80,81,82,83,85,86,88,91
+5V	+5V	31,57,67,68,91
+5VS	+5VS	23,45,47,48,51,57,68,80,84,91
+3VO	+3VO	76,81
+3VSUS	+3VSUS	20,21,22,23,30,33,57,68,76,81,85,91,92
+3V	+3V	44,46,48,57,67,68,70,91
+3VS	+3VS	7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92
+12VSUS	+12VSUS	76,81,91
+12V	+12V	68,91
+12VS	+12VS	22,46,48,51,67,91
+1.8VO	+1.8VO	83,84
+1.8V	+1.8V	7,8,11,14,57,76,83,91
+1.8VS	+1.8VS	15,91
+0.9VS	+0.9VS	9,57,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	82
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,76,82
+1.5VO	+1.5VO	84
+1.5VS	+1.5VS	4,15,20,23,57,84
+VCORE	+VCORE	4,5,80
+VCCP	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,76,82
+1.05VO	+1.05VO	82
+1.1VSG	+1.1VSG	70,71,73,74,76,86
+VGA_VCORE	+VGA_VCORE	70,85
A/D_DOCK_IN	A/D_DOCK_IN	60,88

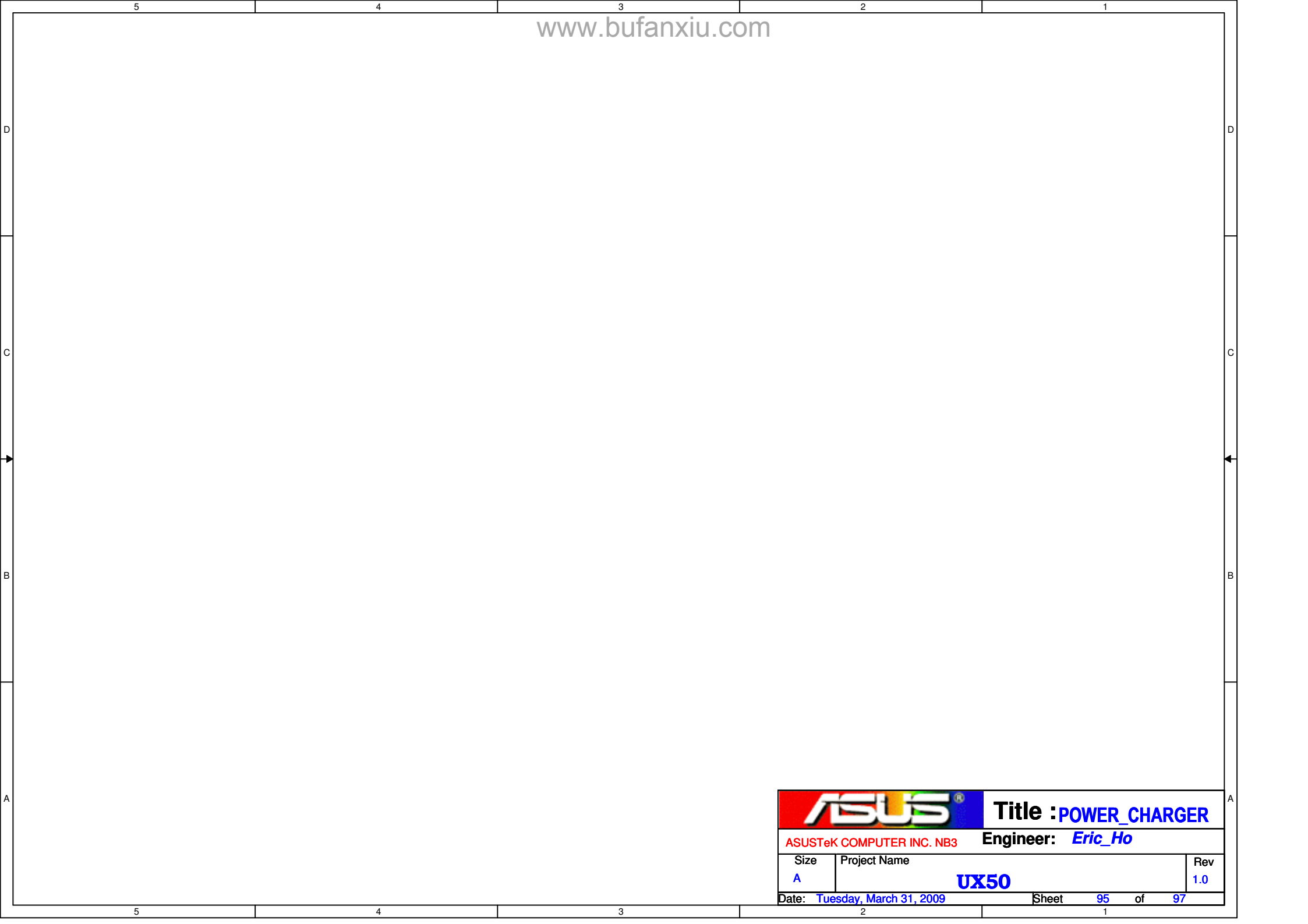
Total sum count: 236 pcs


<Variant Name>

		<b>Title : POWER_SIGNAL</b>	
ASUS COMPUTER INC. NB		Engineer: <i>Morris/Eric</i>	
Size	Project Name	Rev	
Custom	<b>UX50</b>	1.0	
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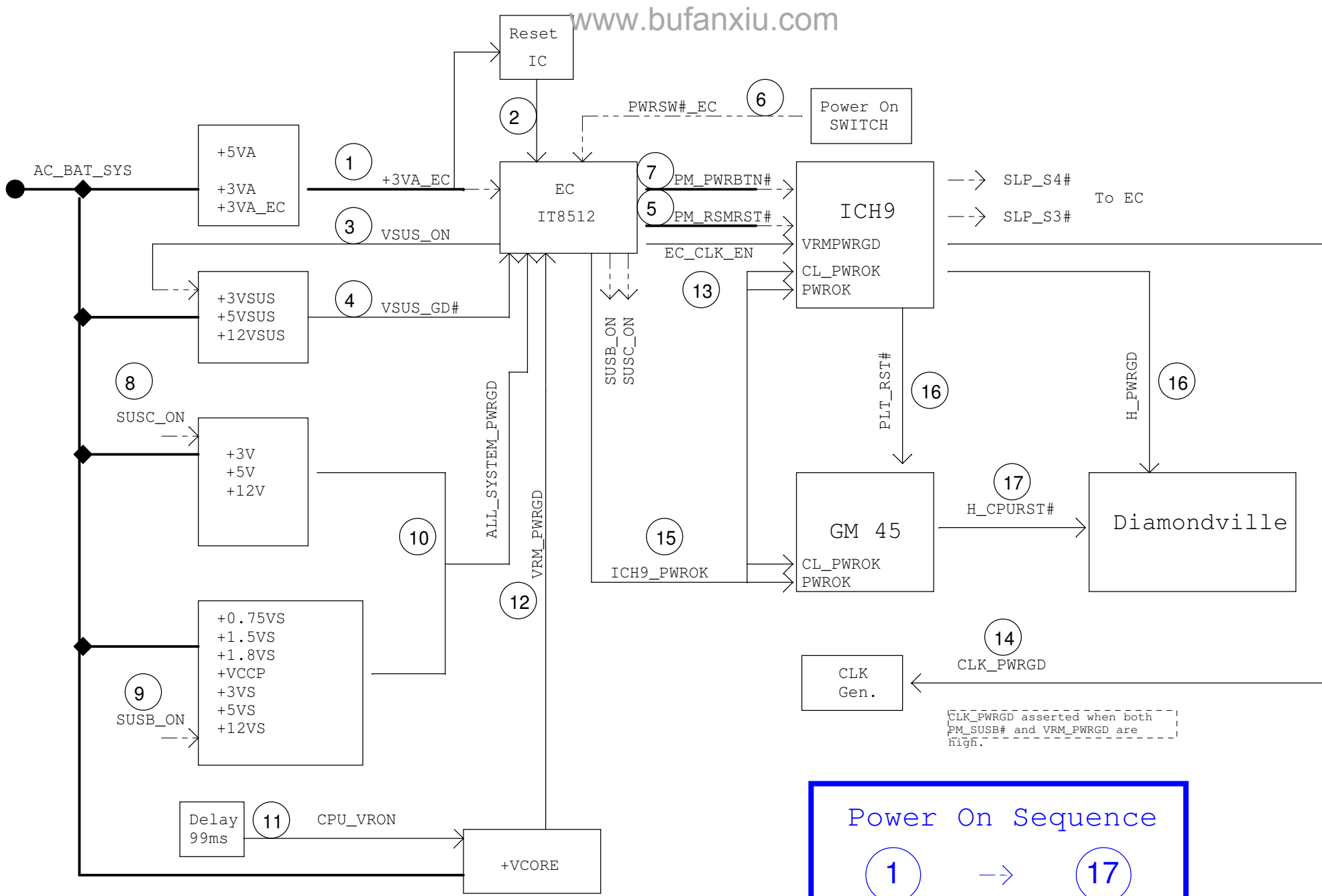
VR\_VID0-VR\_VID6, H\_DPRSTP#,  
MCH\_OK, PM\_DPRSLEPVR, PM\_PSI#,  
VCCSENSE, VSSSENSE, STP\_CPU#,  
PWR\_MON



		<b>Title :POWER_CHARGER</b>
ASUSTeK COMPUTER INC. NB3		<b>Engineer: Eric_Ho</b>
Size A	Project Name <b>UX50</b>	Rev 1.0
Date: <b>Tuesday, March 31, 2009</b>		Sheet <b>95</b> of <b>97</b>

Rev	Date	Description
1.00		First Release!
1.10	02/08/2009	1. Change net ALS_AD to J6801. (Page 68) 2. Change RTC circuit from small board to M/B. (Page 20) 3. Add net CLK_PCIE_VGA and CLK_PCIE_VGA#.(Page 29) 4. Add pull-up for SMBus.(Page 22) 5. Add ITP connector. (Page 03,29) 6. Add MOS for dGPU power. (Page 76)
	02/10/2009	7. Change LAN PCIE to port 6. (Page 21) 8. Add AL_LED# to control ambient light LED. (Page 30,68) 9. Change C7036 to 4.7UF. (Page 70) 10. Swapping DDR2 nets (Page 09,29,74)
	02/11/2009	11. Add USB port for WiMax (Page 68,21) 12. Remove test point for layout. (Page 30)
	02/16/2009	13. Change 8pF cap for 32.768KHz crystal. (Page 20,30)
	02/17/2009	14. Swap J6801 BAT pins (Page 68)
2.00	03/04/2009	1. Remove D4503 for HDA issue. (Page 45)
	03/09/2009	2. Add HDMI hot plug detect in iGPU mode. (Page 48)
	03/09/2009	3. Add C6805 for EMI. (Page 68)
	03/12/2009	4. Change HDMI hot plug detect pin to EC GPI6. (Page 30,48)
	03/12/2009	5. Add CE0502 for CPU SU9600 hang issue. (Page 5)
	03/12/2009	6. Pull up backligh enable pin tto +3VS_LCD from +3VS. (Page 46)
	03/16/2009	7. Swap RN2917. (Page 29)
	03/18/2009	8. Change R7301 to 120ohm. (Page 73)





Power On Sequence

1 → 17

CLK\_PWRGD asserted when both PM\_SUSB# and VRM\_PWRGD are high.