V6J SCHEMATIC V2.0

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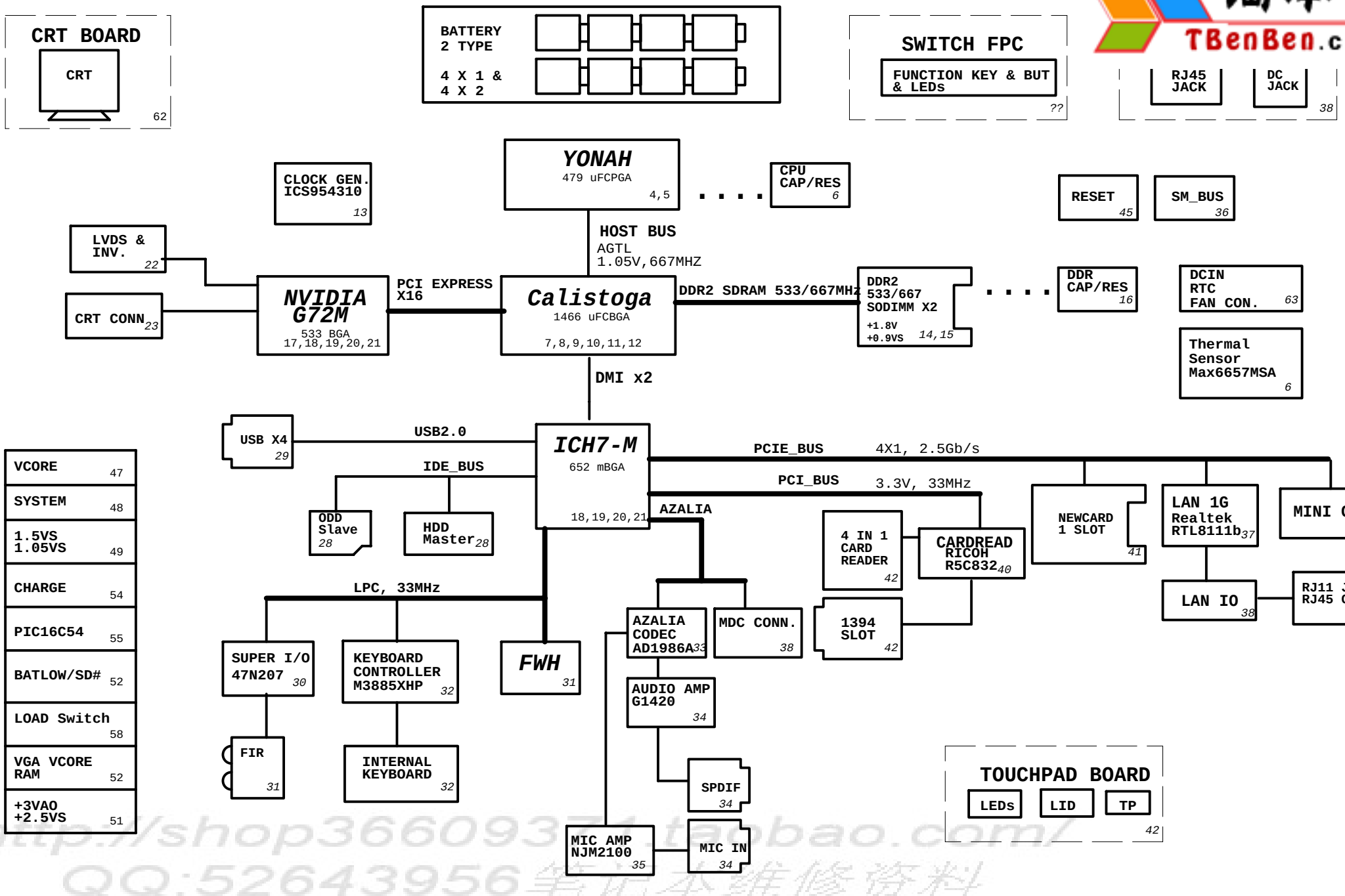
PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: Content & History	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Feng Lin
		SHEET 1 OF 63		RELEASE DATE :	

V6J: YONAH/Calistoga/G72M BLOCK DIAGRAM



ASUS PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005 SHEET 2 OF 63	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : Feng Lin

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	B	
CardBus	AD17	1	B	
1394	AD17	1	A	
4 IN 1		1	C	

AZALIA : PC
USB 0,1 : PC
USB 2,3 : PC
USB 4,5 : PC

CLK =
DDR_SODIMM0 :
DDR_SODIMM1 = 1010000x (A0)
THERMAL = 1001100x (98)
TPM = TBD

SMBUS ADDRESS :

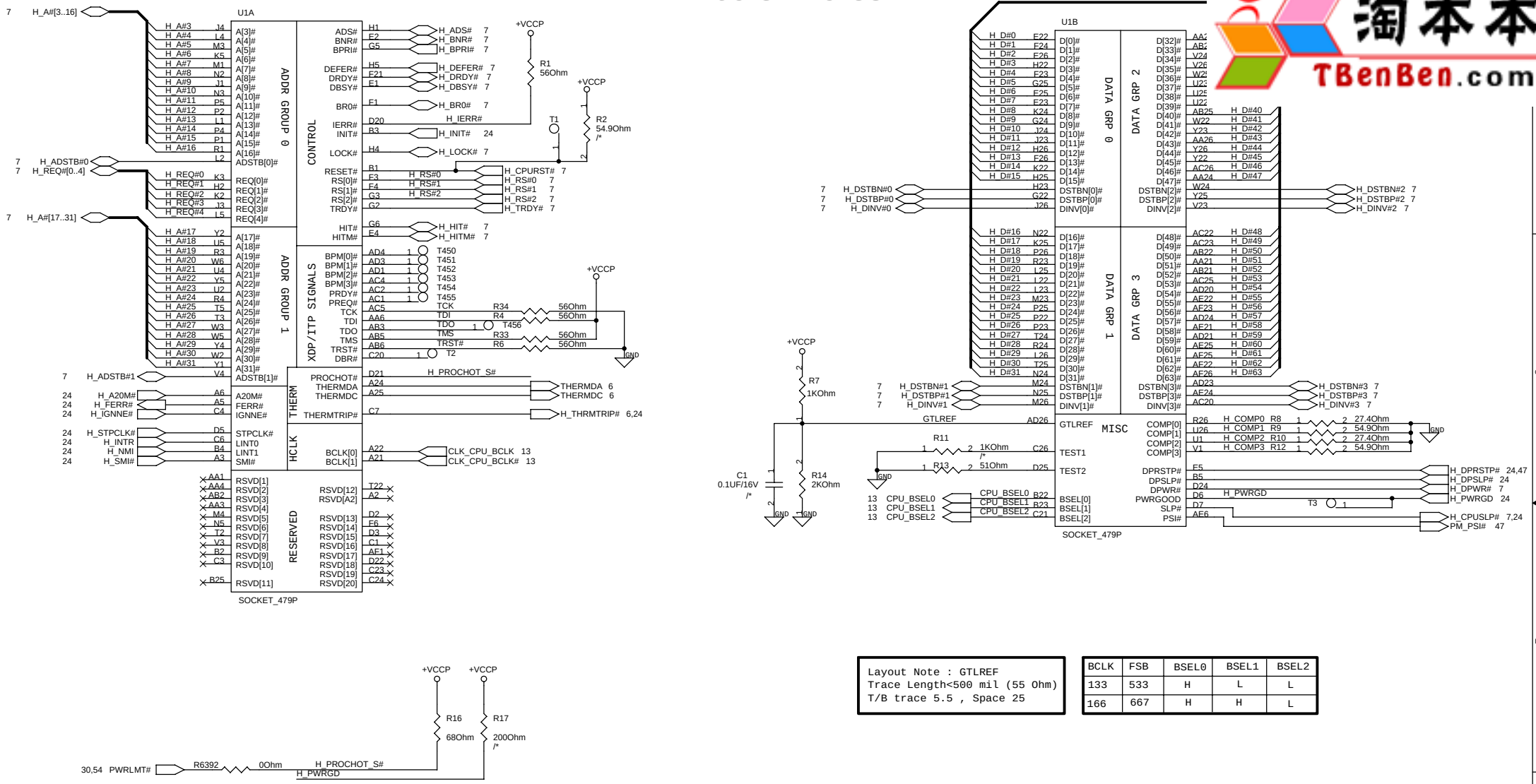
ICH7M_GPIO	Use As	Signal Name	Power
GPIO00	GPI	PM_BMBUSY#	+3VS
GPIO01	GPI	PCI_REQ#5	+3VS
GPIO02	GPI	G72M_THRM#(reserve)	+3VS
GPIO[3:5]	GPI	PCI_INT[E:H]	+3VS
GPIO06	GPO	BACK_OFF#	+3VS
GPIO07	GPI	WIRLESS_#	+3VS
GPIO08	GPI	EXTSMI#_3A	+3VSUS
GPIO09	GPI	ACIN_OC_ICH(reserve)	+3VSUS
GPIO10	GPI	CHG_FULL_OC	+3VSUS
GPIO11	NATIVE	SMBALERT#	+3VSUS
GPIO12	GPI	KBCSCI_3	+3VSUS
GPIO13	GPI	BATIN_OC#_ICH(reserve)	+3VSUS
GPIO14	GPO	LID_ICH#_3A(reserve)	+3VSUS
GPIO15	GPI	802_LED#	+3VSUS
GPIO16	GPO	PM_DPRSLPVR	+3VSUS
GPIO17	GPO	PCI_GNT#5	+3VSUS
GPIO18	GPO	STP_PCI#	+3VSUS
GPIO19	GPI	SATA_DET_#1	+3VSUS
GPIO20	GPO	STP_CPU#	+3VS
GPIO21	GPI	BATSEL_2P(reserve)	+3VS
GPIO22	NATIVE	PCI_REQ#4	+3VS
GPIO23	NATIVE	LDRQ1#	+3VS
GPIO24	GPO		+3VSUS
GPIO25	GPO		+3VSUS
GPIO26	GPO	OP_SD#	+3VSUS
GPIO27	GPO	**WLAN_ON**	+3VSUS
GPIO28	GPO	**PWR_1HZ**	+3VSUS
GPIO29	NATIVE	USB_OC#45	+3VSUS
GPIO30	NATIVE	USB_OC#67	+3VSUS
GPIO31	NATIVE	USB_OC#67	+3VSUS
GPIO32	GPO	PM_CLKRUN#	+3VSUS
GPIO33	GPO	BT_ON	+3VS
GPIO34	GPO	FWH_WP#	+3VS
GPIO35	GPO		+3VS
GPIO36	GPO	BT_LED#	+3VS
GPIO37	GPI	PCB_VID0	+3VS
GPIO38	GPI	PCB_VID1	+3VS
GPIO39	GPI	PCB_VID2	+3VS
GPIO[40:47]	N/A	N/A	N/A
GPIO48	NATIVE	**FWH_TBL#**	+3VS
GPIO49	NATIVE	H_PWRGD	+3VS

M38857_GPIO	Use As	Signal Name
P20	GPO	KBCRSM
P21	GPI	
P22	GPO	BAT_LEARN
P23	GPO	**CPPE_EN**
P24	GPO	SET_PCIRSTNS#
P25	GPO	CAP_LED#
P26	GPO	NUM_LED#
P27	GPO	SCROLL_LED#
P40	GPO	KBC_EXTSMI
P41	GPO	**PANLOCK_LED#**
P42	GPO	WATCHDOG
P43	GPO	CHG_FULL_KBC(reserve)
P44	GPO	KBDCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LOW#_KBC
P51	GPO	
P52	GPI	KBDDT0
P53	GPI	KBDDT1
P54	GPI	LID_ICH#_3A
P55	GPI	BAT_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	**BLUETOOTH_#**
P61	GPI	INTERNET#
P62	GPI	**CPPE#**
P63	GPI	
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPI	PANLOCK_#
P67	GPI	
P76	GPI/O	SMD_BAT
P77	GPI/O	SMC_BAT

G72M_GPIO	Use As	Signal Name
GPIO00	GPI	
GPIO01	GPI	
GPIO02	GPO	
GPIO03	GPO	LCD_VDD_EN#
GPIO04	GPO	LCD_BACKEN
GPIO05	GPO	
GPIO06	GPO	
GPIO07	GPO	
GPIO08	GPI	GPIO8/ALERT#
GPIO09	GPO	
GPIO10	GPIO	G72M_GPIO12
GPIO11	GPO	
GPIO12	GPO	

47N207_GPIO	Use As	Signal Name
GP10	GPIO	
GP11	GPIO	
GP12	GPO	
GP13	GPO	
GP14	GPO	FIR_SEL
GP15	GPIO	**PWR_THRO#**
GP16	GPIO	**ODD_DIS#**
GP17	GPIO	**RST#_XCARD**
GP30	GPIO	PID0
GP31	GPIO	
GP32	GPIO	**G72M_THRO#**
GP33	GPIO	CPUFAN_SPD_A
GP34	GPIO	SW_RST#
GP35	GPIO	
GP36	GPIO	
GP37	GPIO	

PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005 SHEET 3 OF 63	DESCRIPTION: SYSTEM INFO.	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER : Feng Lin



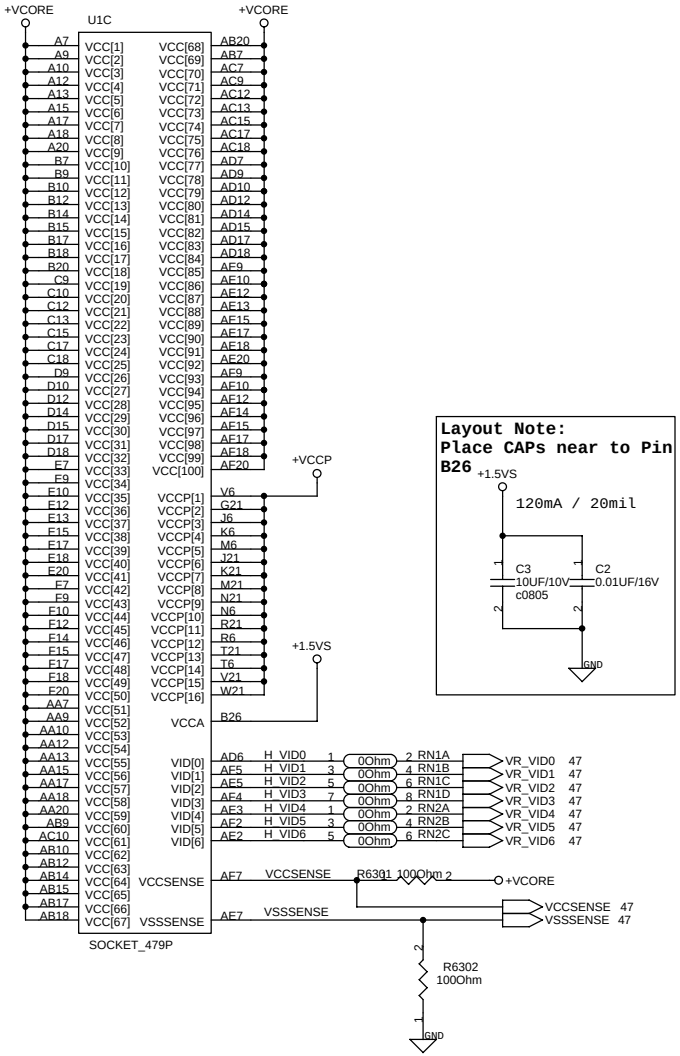
Layout Note : GTLREF
Trace Length<500 mil (55 Ohm)
T/B trace 5.5 , Space 25

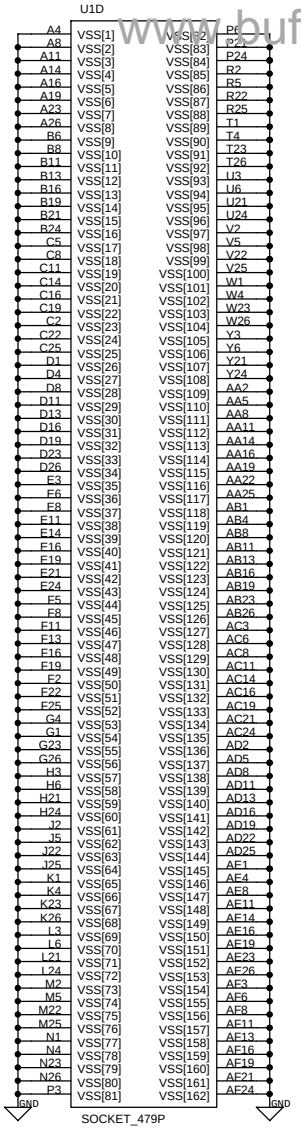
BCLK	FSB	BSEL0	BSEL1	BSEL2
133	533	H	L	L
166	667	H	H	L

PROJECT: V6J	REVISION 2.0	DATE: Friday, November 25, 2005	DESCRIPTION: YONAH CPU (1)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Feng Lin
		SHEET 4 OF 63		RELEASE DATE :	

YONAH FSB667			
	LFM	TYP	HFM
CPU State	C4	C3	C0
VCC	1.14V	1.2V	1.356V
ICC	0.9A	7.59A	27A

YONAH FSB667			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
ICCP			2.5A





MOBILE YONAH

VID[6..0]	Voltage	VID[6..0]	Voltage				
0 0 0 0 0 0 0	1.5000V	0 1 0 0 0 0 0	1.1000V	1 0		1 1 0 0 0 0 1	0.2875V
0 0 0 0 0 0 1	1.4875V	0 1 0 0 0 0 1	1.0875V	1 0 0 0 0 0 1	0.6875V	1 1 0 0 0 1 0	0.2750V
0 0 0 0 0 1 0	1.4750V	0 1 0 0 0 1 0	1.0750V	1 0 0 0 0 1 0	0.6750V	1 1 0 0 0 1 1	0.2650V
0 0 0 0 0 1 1	1.4625V	0 1 0 0 0 1 1	1.0625V	1 0 0 0 0 1 1	0.6625V	1 1 0 0 1 0 0	0.2500V
0 0 0 0 1 0 0	1.4500V	0 1 0 0 1 0 0	1.0500V	1 0 0 0 1 0 0	0.6500V	1 1 0 0 1 0 1	0.2375V
0 0 0 0 1 0 1	1.4375V	0 1 0 0 1 0 1	1.0375V	1 0 0 0 1 0 1	0.6375V	1 1 0 0 1 1 0	0.2250V
0 0 0 0 1 1 0	1.4250V	0 1 0 0 1 1 0	1.0250V	1 0 0 0 1 1 0	0.6250V	1 1 0 0 1 1 1	0.2125V
0 0 0 0 1 1 1	1.4125V	0 1 0 0 1 1 1	1.0125V	1 0 0 0 1 1 1	0.6125V	1 1 0 1 0 0 0	0.2000V
0 0 0 1 0 0 0	1.4000V	0 1 0 1 0 0 0	1.0000V	1 0 0 1 0 0 0	0.6000V	1 1 0 1 0 0 1	0.1875V
0 0 0 1 0 0 1	1.3875V	0 1 0 1 0 0 1	0.9875V	1 0 0 1 0 0 1	0.5875V	1 1 0 1 0 1 0	0.1750V
0 0 0 1 0 1 0	1.3750V	0 1 0 1 0 1 0	0.9750V	1 0 0 1 0 1 0	0.5750V	1 1 0 1 0 1 1	0.1625V
0 0 0 1 0 1 1	1.3625V	0 1 0 1 0 1 1	0.9625V	1 0 0 1 0 1 1	0.5625V	1 1 0 1 1 0 0	0.1500V
0 0 0 1 1 0 0	1.3500V	0 1 0 1 1 0 0	0.9500V	1 0 0 1 1 0 0	0.5500V	1 1 0 1 1 0 1	0.1375V
0 0 0 1 1 0 1	1.3375V	0 1 0 1 1 0 1	0.9375V	1 0 0 1 1 0 1	0.5375V	1 1 0 1 1 1 0	0.1250V
0 0 0 1 1 1 0	1.3250V	0 1 0 1 1 1 0	0.9250V	1 0 0 1 1 1 0	0.5250V	1 1 0 1 1 1 1	0.1125V
0 0 0 1 1 1 1	1.3125V	0 1 0 1 1 1 1	0.9125V	1 0 0 1 1 1 1	0.5125V	1 1 1 0 0 0 0	0.1000V
0 0 1 0 0 0 0	1.3000V	0 1 1 0 0 0 0	0.9000V	1 0 1 0 0 0 0	0.5000V	1 1 1 0 0 0 1	0.0875V
0 0 1 0 0 0 1	1.2875V	0 1 1 0 0 0 1	0.8875V	1 0 1 0 0 0 1	0.4875V	1 1 1 0 0 1 0	0.0750V
0 0 1 0 0 1 0	1.2750V	0 1 1 0 0 1 0	0.8750V	1 0 1 0 0 1 0	0.4750V	1 1 1 0 0 1 1	0.0625V
0 0 1 0 0 1 1	1.2625V	0 1 1 0 0 1 1	0.8625V	1 0 1 0 0 1 1	0.4625V	1 1 1 0 1 0 0	0.0500V
0 0 1 0 1 0 0	1.2500V	0 1 1 0 1 0 0	0.8500V	1 0 1 0 1 0 0	0.4500V	1 1 1 0 1 0 1	0.0375V
0 0 1 0 1 0 1	1.2375V	0 1 1 0 1 0 1	0.8375V	1 0 1 0 1 0 1	0.4375V	1 1 1 0 1 1 0	0.0250V
0 0 1 0 1 1 0	1.2250V	0 1 1 0 1 1 0	0.8250V	1 0 1 0 1 1 0	0.4250V	1 1 1 0 1 1 1	0.0125V
0 0 1 0 1 1 1	1.2125V	0 1 1 0 1 1 1	0.8125V	1 0 1 0 1 1 1	0.4125V	1 1 1 1 0 0 0	0.0000V
0 0 1 1 0 0 0	1.2000V	0 1 1 1 0 0 0	0.8000V	1 0 1 1 0 0 0	0.4000V	1 1 1 1 0 0 1	0.0000V
0 0 1 1 0 0 1	1.1875V	0 1 1 1 0 0 1	0.7875V	1 0 1 1 0 0 1	0.3875V	1 1 1 1 0 1 0	0.0000V
0 0 1 1 0 1 0	1.1750V	0 1 1 1 0 1 0	0.7750V	1 0 1 1 0 1 0	0.3750V	1 1 1 1 0 1 1	0.0000V
0 0 1 1 0 1 1	1.1625V	0 1 1 1 0 1 1	0.7625V	1 0 1 1 0 1 1	0.3625V	1 1 1 1 1 0 0	0.0000V
0 0 1 1 1 0 0	1.1500V	0 1 1 1 1 0 0	0.7500V	1 0 1 1 1 0 0	0.3500V	1 1 1 1 1 0 1	0.0000V
0 0 1 1 1 0 1	1.1375V	0 1 1 1 1 0 1	0.7375V	1 0 1 1 1 0 1	0.3375V	1 1 1 1 1 1 0	0.0000V
0 0 1 1 1 1 0	1.1250V	0 1 1 1 1 1 0	0.7250V	1 0 1 1 1 1 0	0.3250V	1 1 1 1 1 1 1	0.0000V
0 0 1 1 1 1 1	1.1125V	0 1 1 1 1 1 1	0.7125V	1 0 1 1 1 1 1	0.3125V		

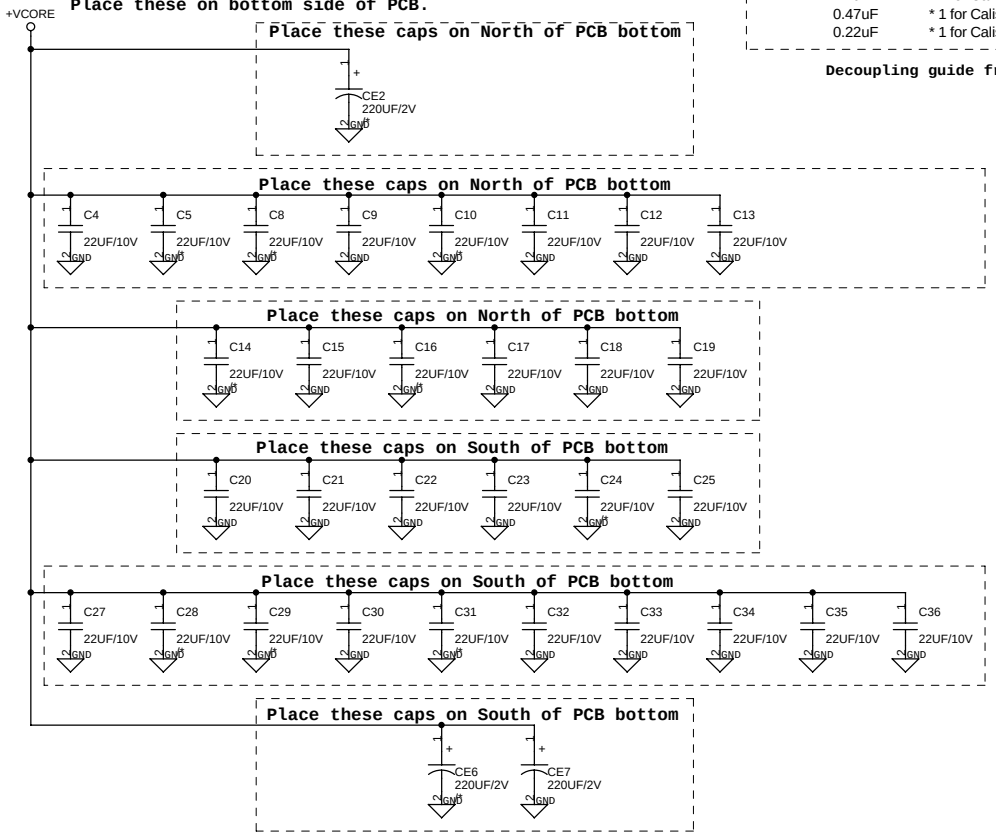
YONAH VID TABLE							
CPU FREQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.8G	C3/C4
2.13G/B1	1.372V					0.988V	0.726V
2.0G/B1	1.356V					0.988V	0.726V
1.87G/B1	1.356V					0.988V	0.726V
1.73G/B1	1.356V					0.988V	0.726V
1.6G/B1	1.356V					0.988V	0.726V
1.6G/A2	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V

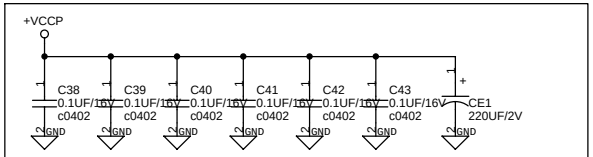
PROJECT: V6J	REVISION	DATE: Friday, November 25, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.0	SHEET 5 OF 63	YONAH CPU (2)	RELEASE DATE :		Feng Lin

VCORE	22uF/6.3V	* 20
	330uF/2V	* 6
VCCP	0.1uF	* 5 for CPU
	220uF	* 1 for CPU
	220uF	* 1 for Calistoga
	4.7uF	* 1 for Calistoga
	2.2uF	* 1 for Calistoga
	0.47uF	* 1 for Calistoga
	0.22uF	* 1 for Calistoga

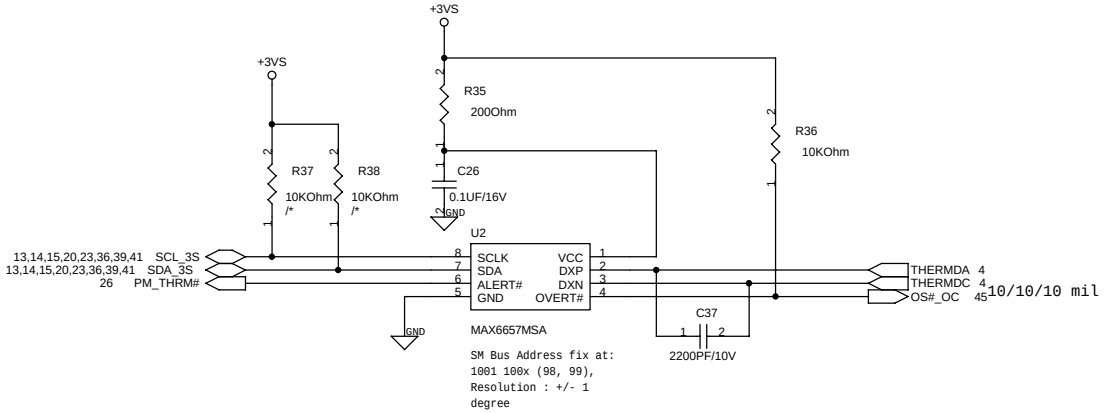
Decoupling guide from INTEL

Layout Note :
All of VCore Decoupling Caps
Place these on bottom side of PCB.

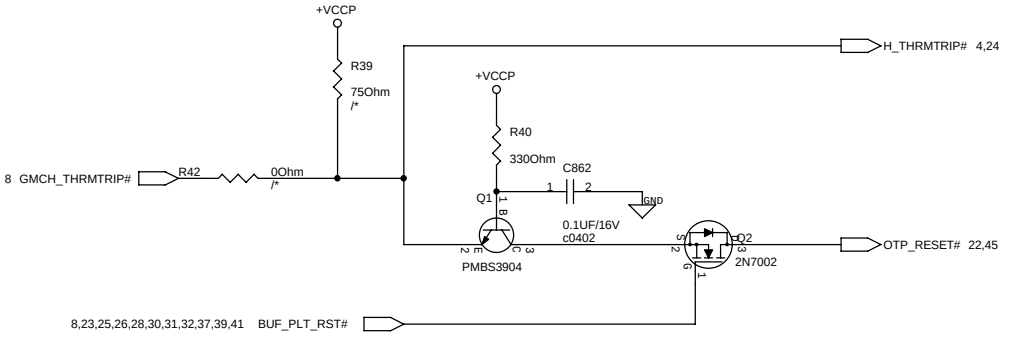




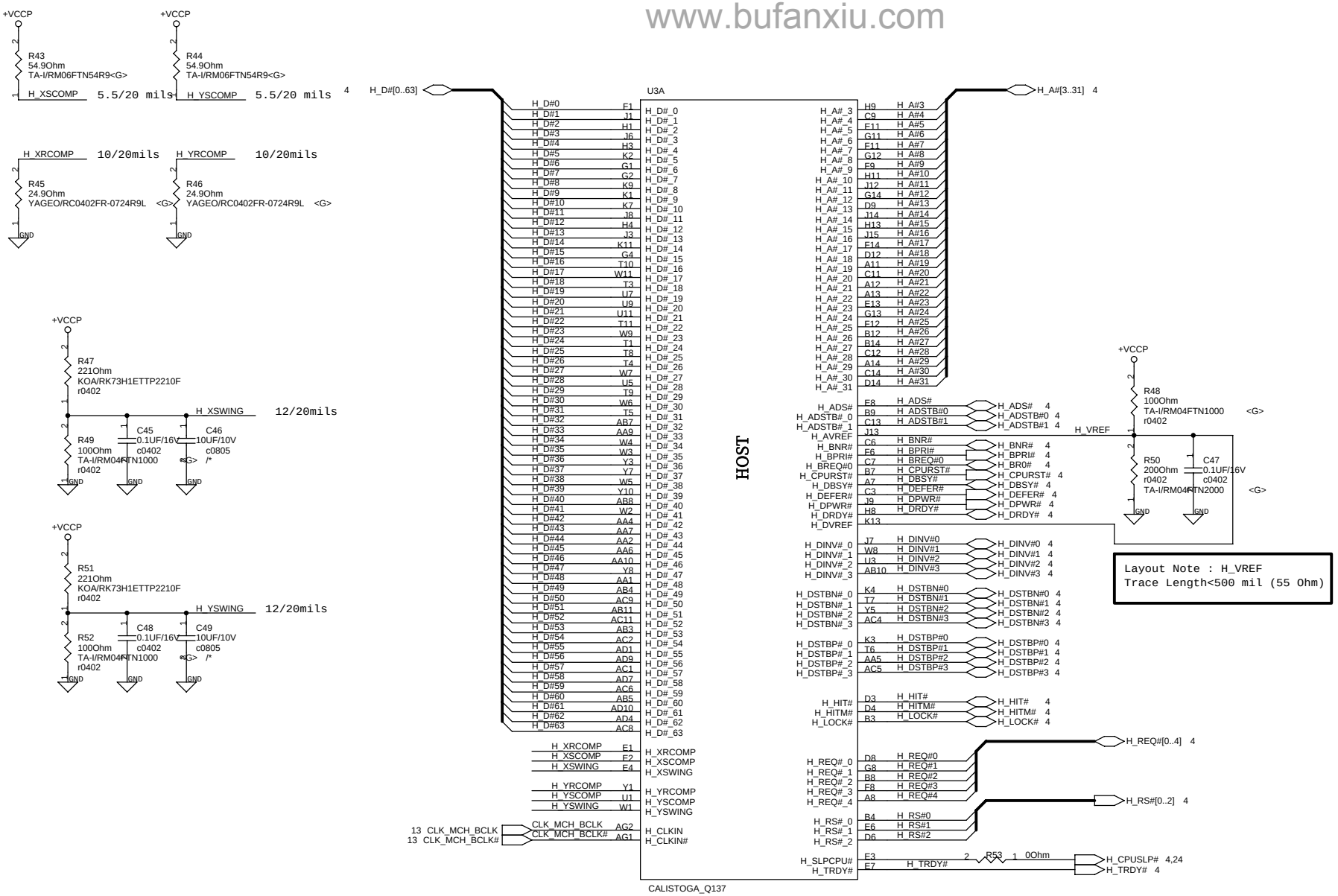
Layout Note :
+V1.05S (VCCP) Decoupling Capacitor
(Place near CPU)



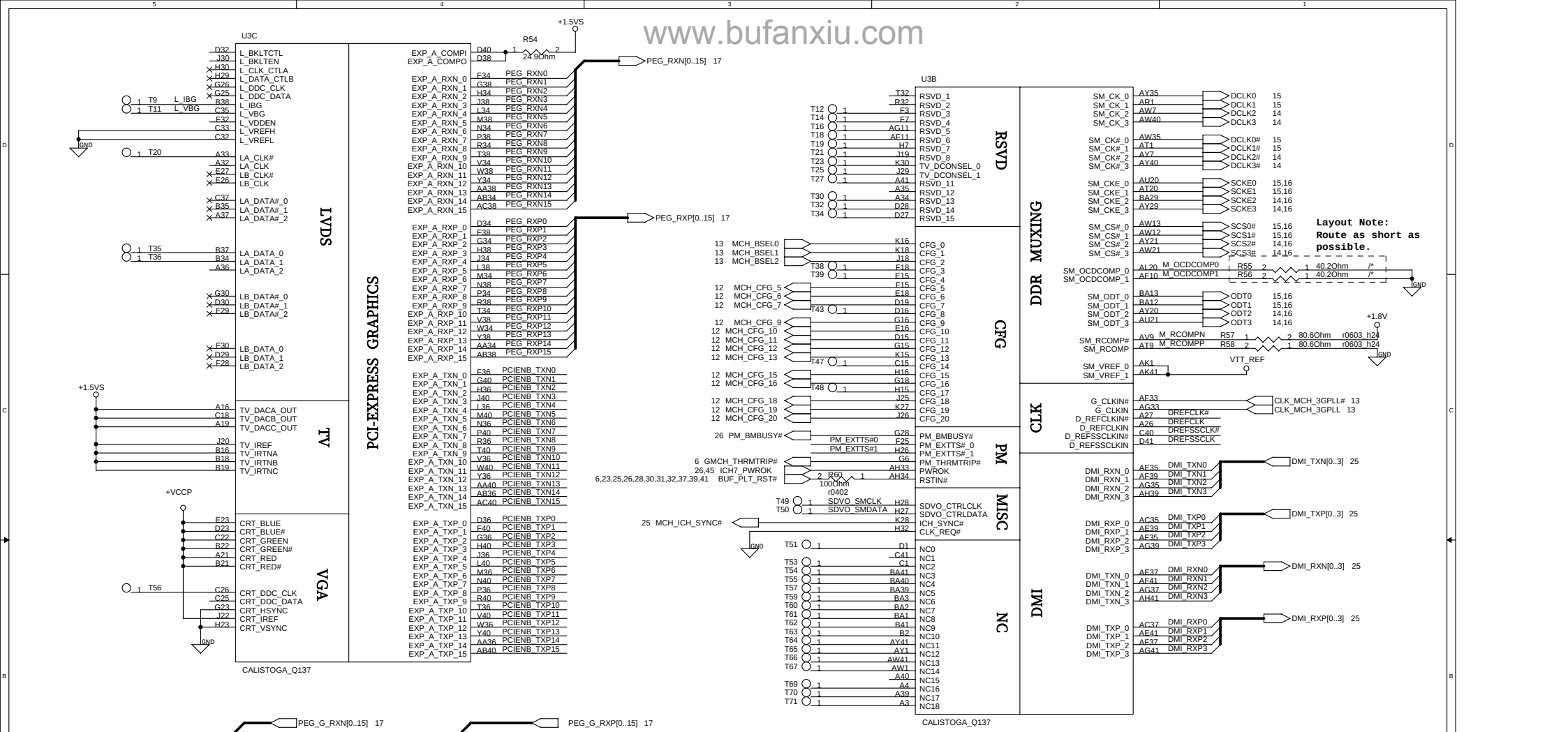
THERMAL SENSOR



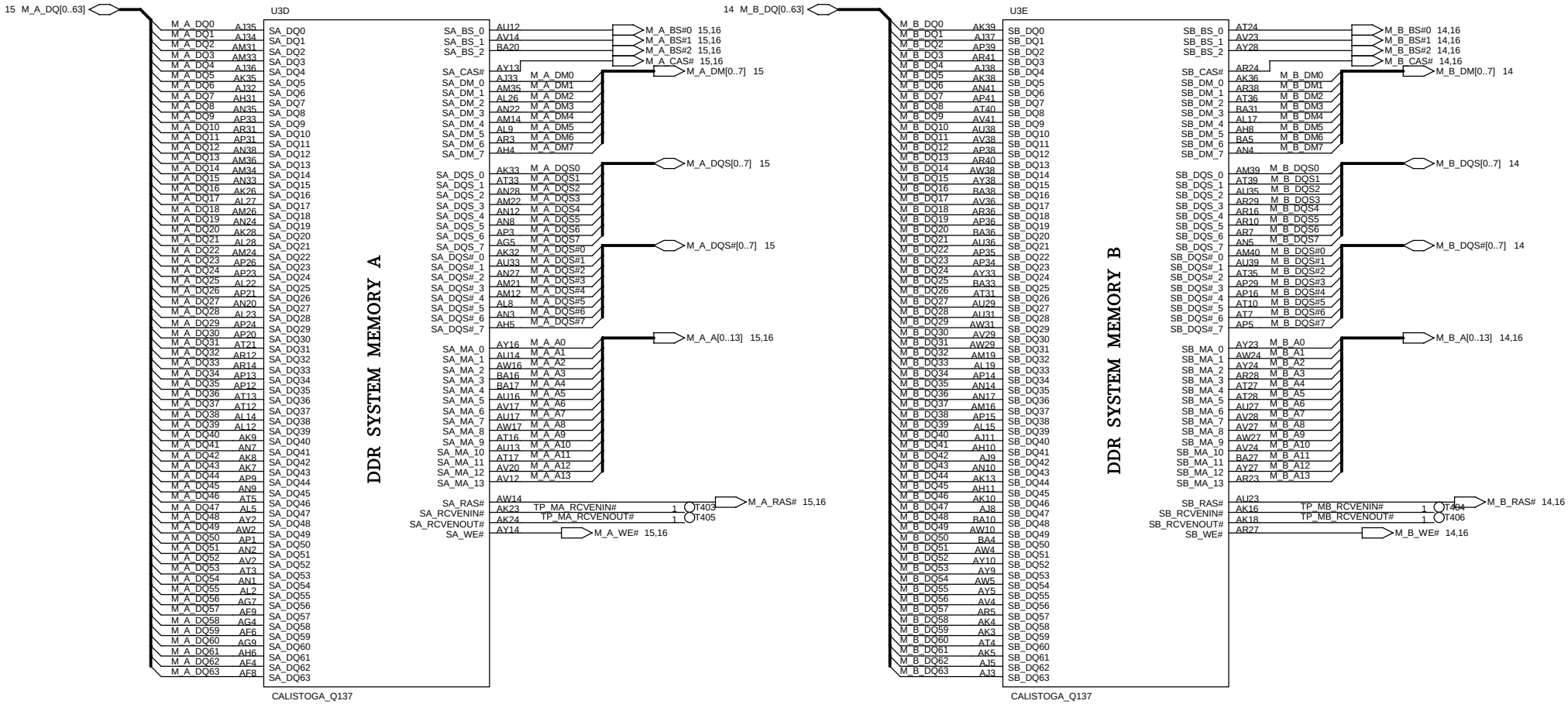
ASUS PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **6** OF **63**	DESCRIPTION: ***Caps & THERMAL & ITP***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **7** OF **63**	DESCRIPTION: ***MCH : CPU***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***

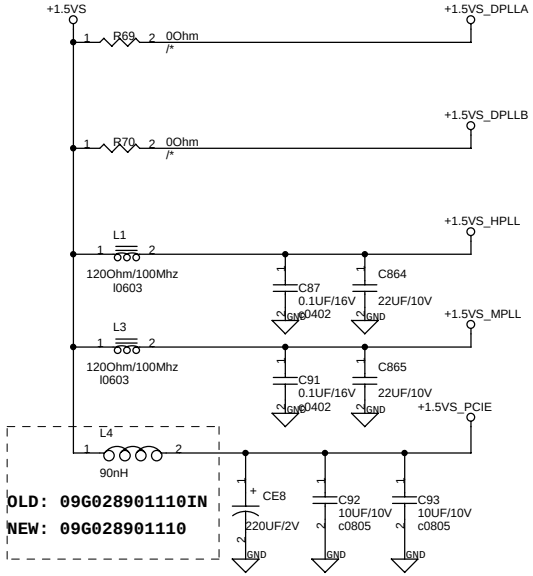


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **8** OF **63**	DESCRIPTION: ***MCH: PCIE/DMI/DDR2***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***

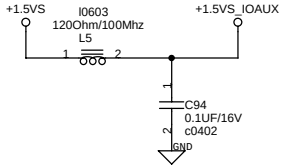


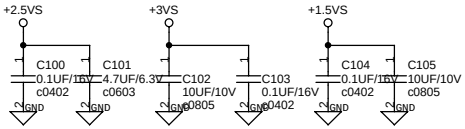
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **9** OF **63**	DESCRIPTION: ***Calistoga DDR2 (3)***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

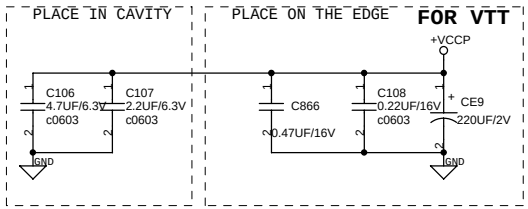


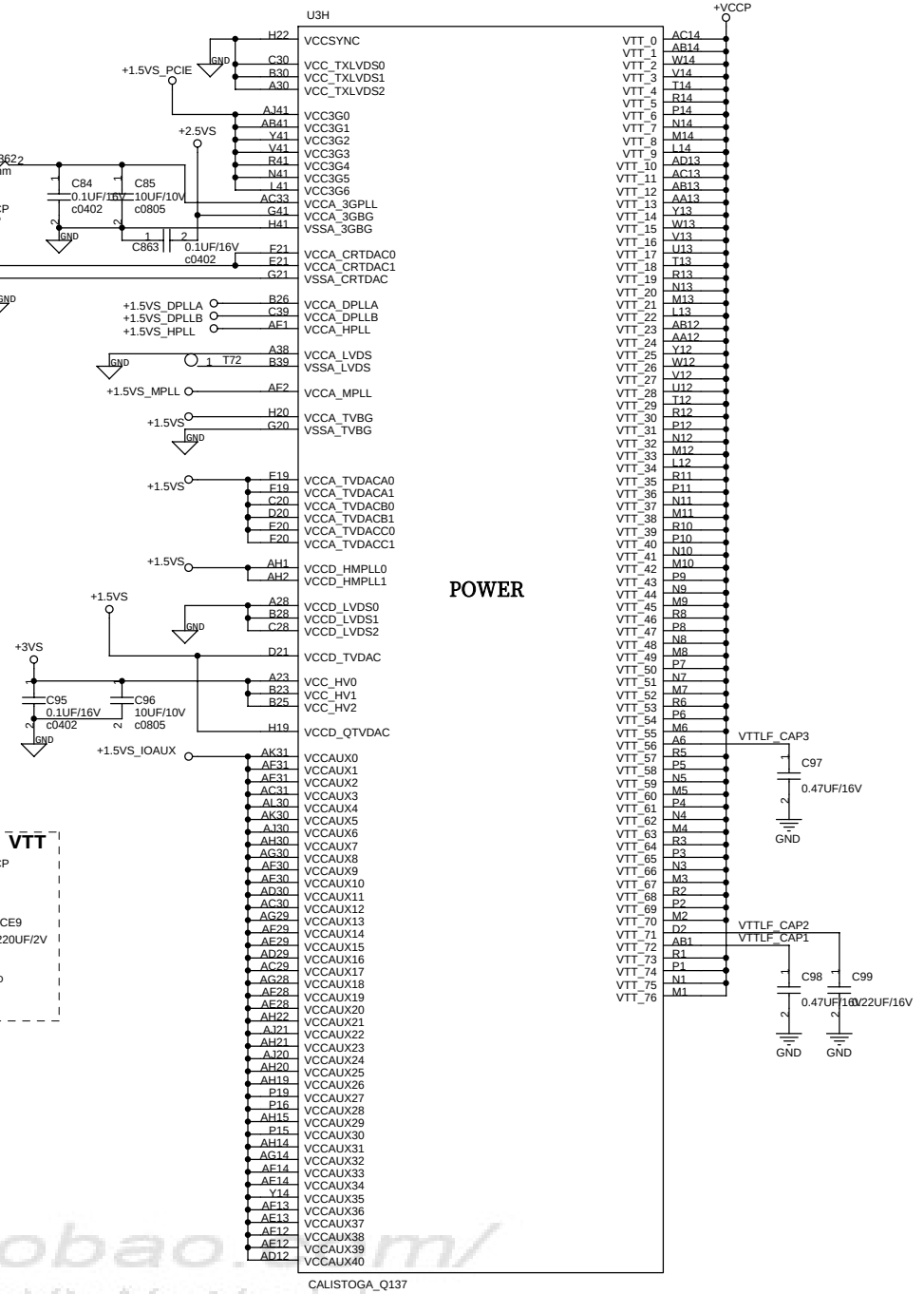
OLD: 09G028901110IN
NEW: 09G028901110





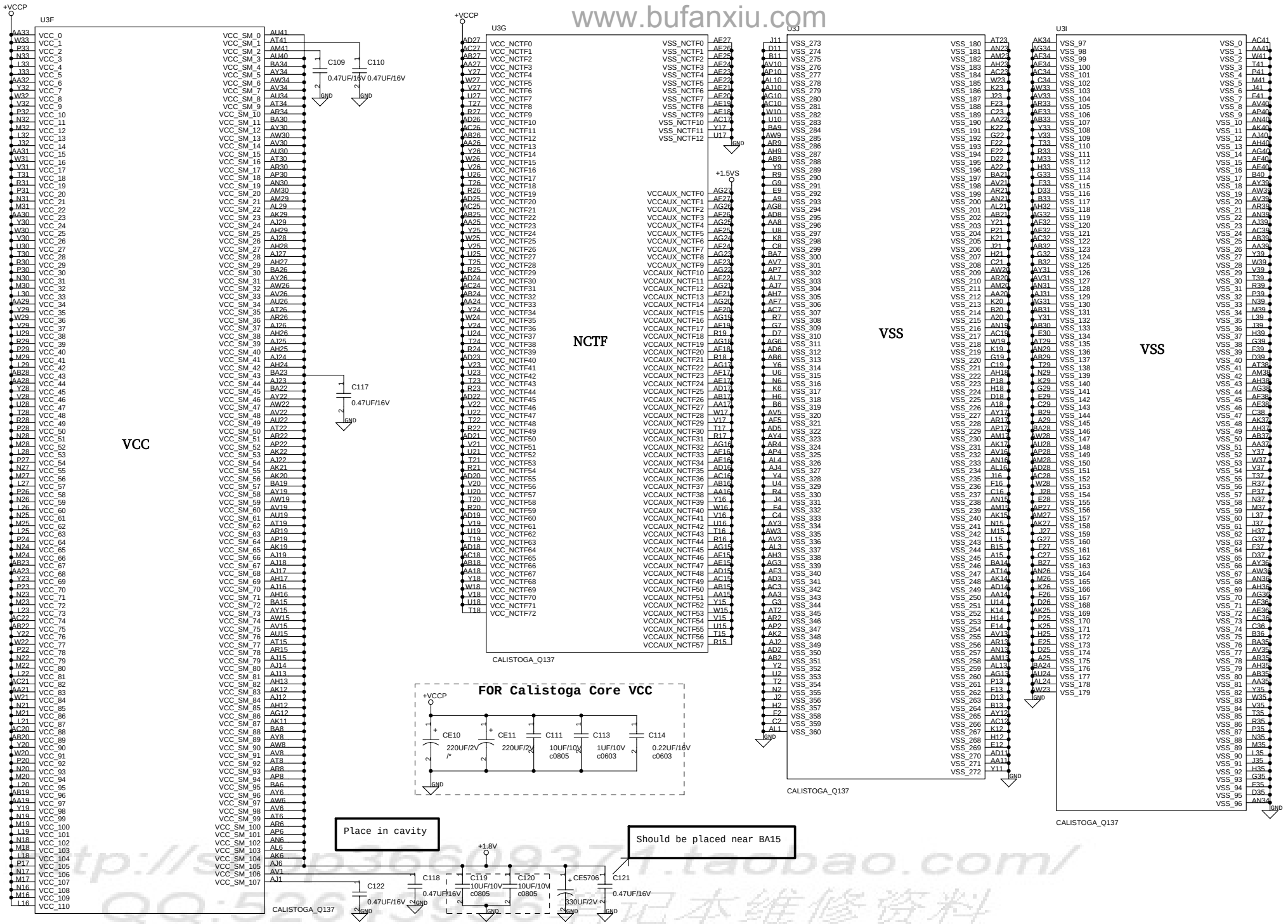
NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.



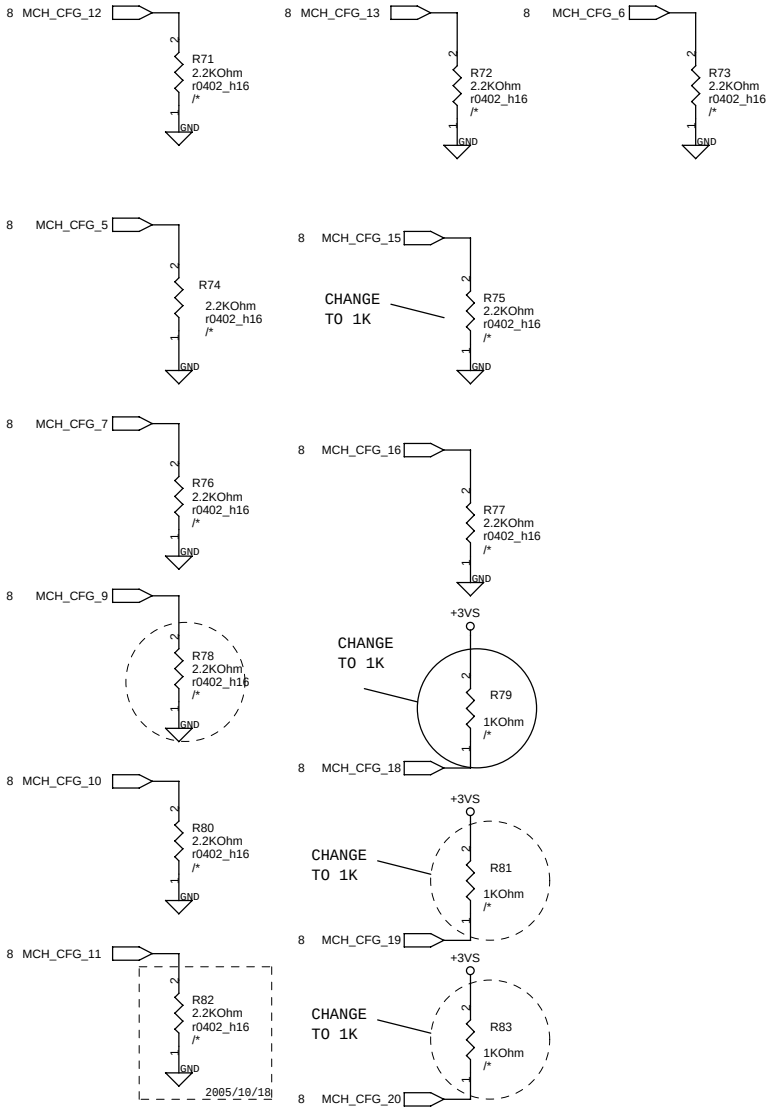


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **10** OF **63**	DESCRIPTION: ***MCH: Power***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***Feng Lin***



PROJECT: **V6J**	REVISION: **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***MCH: GND/NCTF***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Feng Lin***
		SHEET **11** OF **63**		RELEASE DATE:	



Signal Name	Configuration	Notes
CFG[2:0]	011= 667 FSB 001= 533 FSB	Selection the FSB freqency
CFG5	0= DMIx2 1= DMIx4	Selection between DMIx2 and DMIx4
CFG7	0= Reserved 1= Mobil Yonah	Control the target processor
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG[13:12]	01= XOR 10= Z 11= Normal Operation	
CFG16	0= Dynamic ODT DIS 1= Dynamic ODT EN	Control FSB Dynamic ODT
CFG18	0= 1.05V 1= 1.5V	Control GMCH Vcore level
CFG19	0= Normal Operation 1= DMI Lane Revesal EN	
SDVOCTRL_DATA	0= No SDVO device 1= SDVO device present	

Intel Demo Circuit

CFG6	0= Moby Dick 1= Calistoga	
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG11	0= Reserved 1= 8x Enable	PSB 4x CLK Enable
CFG20	0= Only SDVO or PCIE x1 (Default) 1= SDVO and PCIE x1 are operating	

CFG[2..0] need external pullup resistors.
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **12** OF **63**	DESCRIPTION: ***MCH: Strapping***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Feng Lin***

Bclk	FSB	FSLC	FSLB	FSLA
		BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

PLACE termination close to source IC

CLK_CPU_BCLK R91 49.9Ohm
CLK_CPU_BCLK# R92 49.9Ohm
CLK_MCH_BCLK R96 49.9Ohm
CLK_MCH_BCLK# R97 49.9Ohm
CLK_PCIE_ICH R98 49.9Ohm
CLK_PCIE_ICH# R100 49.9Ohm
CLK_MCH_3GPLL R102 49.9Ohm
CLK_MCH_3GPLL# R103 49.9Ohm
CLK_PCIE_NEWCARD R6376 49.9Ohm
CLK_PCIE_NEWCARD# R6377 49.9Ohm
CLK_PCIE_LAN R110 49.9Ohm
CLK_PCIE_LAN# R111 49.9Ohm
CLK_PCIE_MINICARD R112 49.9Ohm
CLK_PCIE_MINICARD# R114 49.9Ohm
CLK_PCIE_PEG R115 49.9Ohm
CLK_PCIE_PEG# R116 49.9Ohm

U4 ICS954310BGLFT

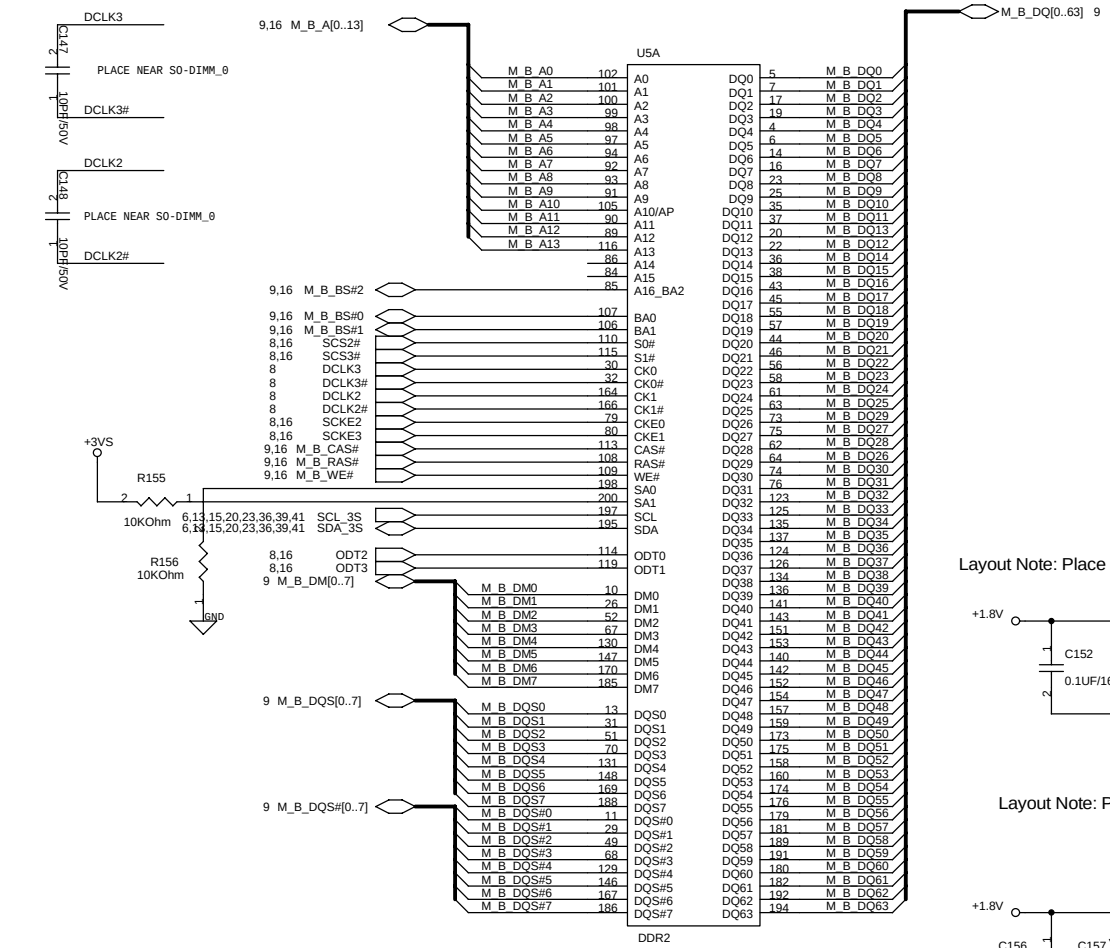
ICS 954310 FREQUENCY TABLE

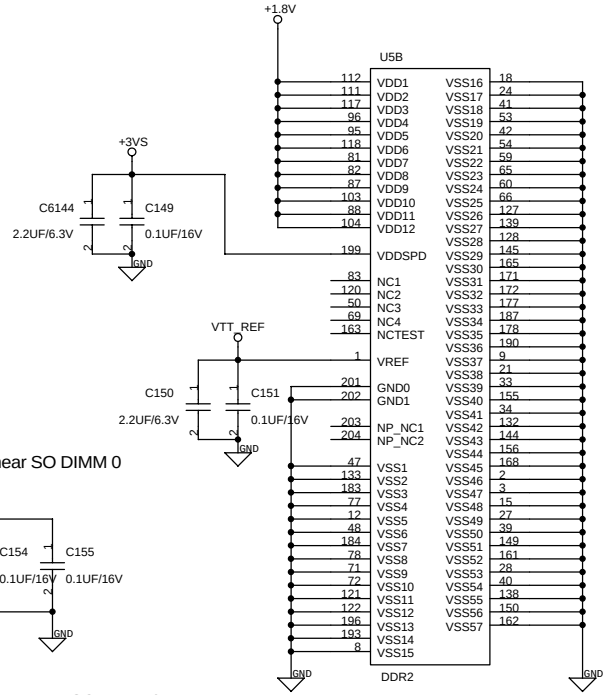
FS_C	FS_B	FS_A	CPU MHz	PCIE MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266	100	33.33	14.318	48.00	96.00
0	0	1	133	100	33.33	14.318	48.00	96.00
0	1	0	200	100	33.33	14.318	48.00	96.00
0	1	1	166	100	33.33	14.318	48.00	96.00
1	0	0	333	100	33.33	14.318	48.00	96.00
1	0	1	100	100	33.33	14.318	48.00	96.00
1	1	0	400	100	33.33	14.318	48.00	96.00
1	1	1	200	100	33.33	14.318	48.00	96.00

Internal Pull-Up
PIN 5,9,32,33,34
Internal Pull-Down
PIN 64

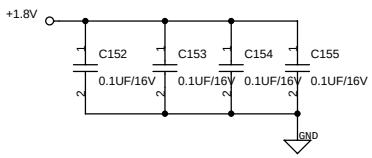
Pin9	Pin8	Pin17	Pin18
0	x	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIEX0T	PCIEX0C

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***CLOCK GEN.***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **13** OF **63**		RELEASE DATE :	

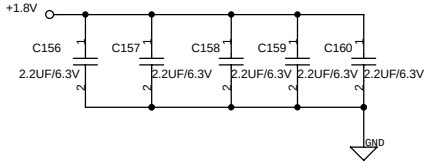




Layout Note: Place these Caps near SO DIMM 0

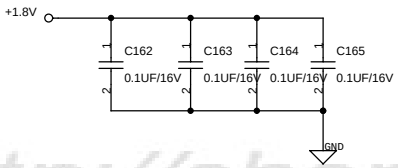


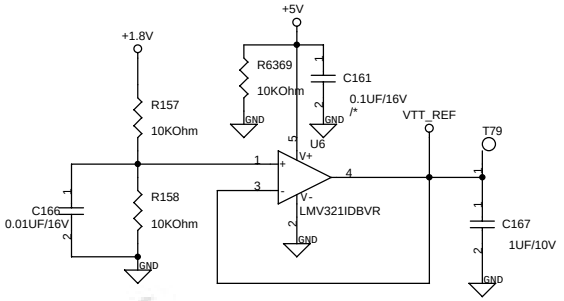
Layout Note: Place these Caps near SO DIMM 0



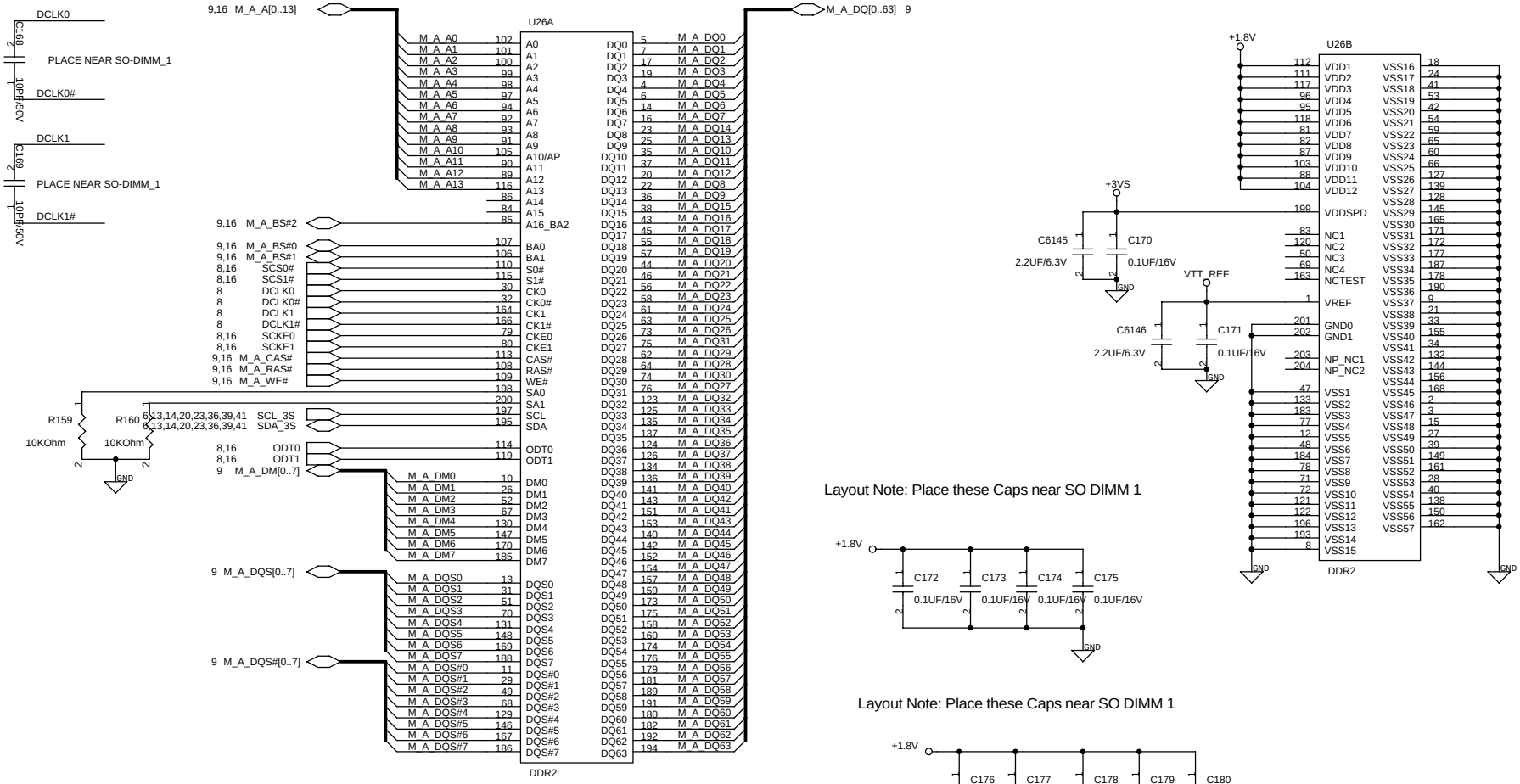
SO-DIMM Part is QUASAR
BOM is TYCO

Layout Note: Place these High-Freq decoupling Caps near the GMCH



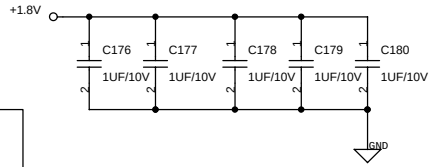


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **14** OF **63**	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**
					DESIGN ENGINEER : ***Feng Lin***



Layout Note: Place these Caps near SO DIMM 1

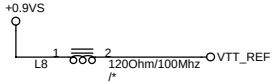
Layout Note: Place these Caps near SO DIMM 1



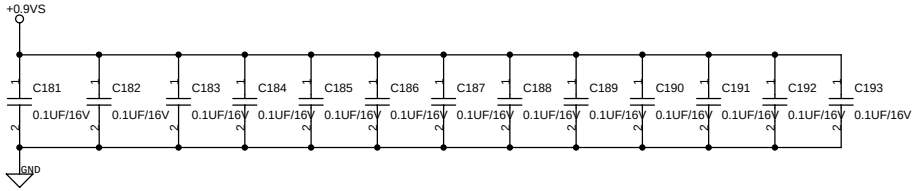
SO-DIMM Part is QUASAR
BOM is TYCO

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

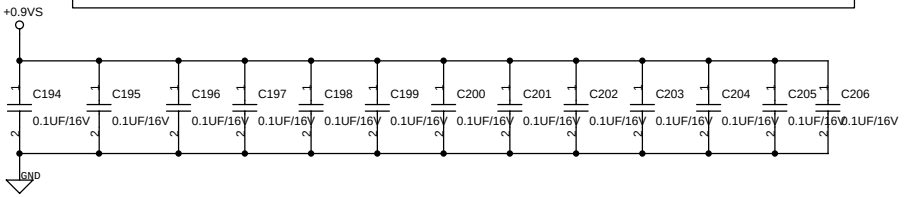
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***DDR2 SO-DIMM (2)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **15** OF **63**		RELEASE DATE :		



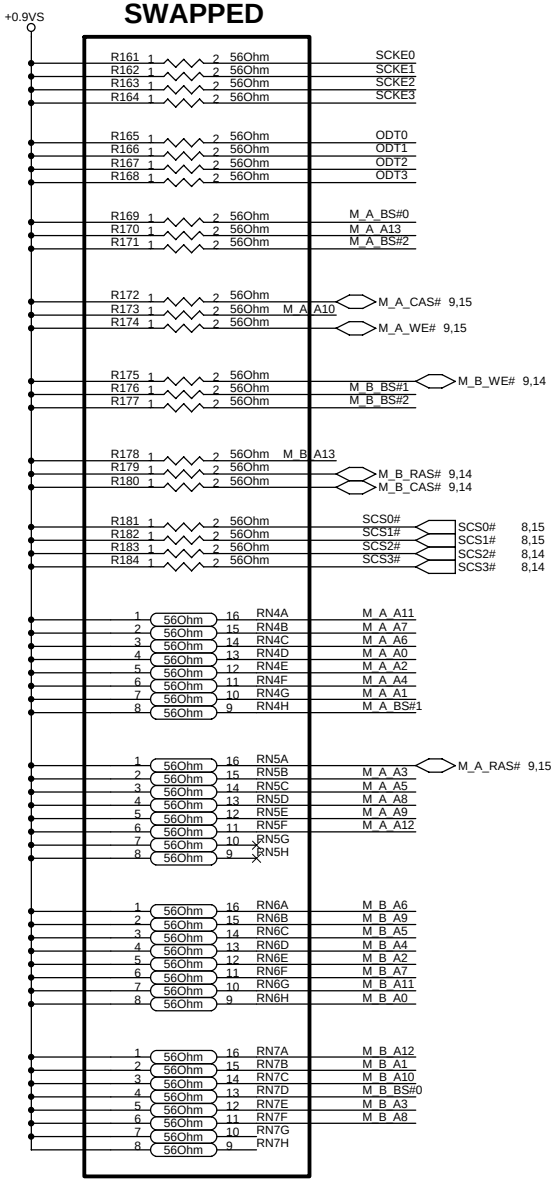
M_A_A[0..13] 9,15
M_A_BS#[0..2] 9,15
M_B_A[0..13] 9,14
M_B_BS#[0..2] 9,14
SCKE[0:3] 8,14,15
ODT[0:3] 8,14,15



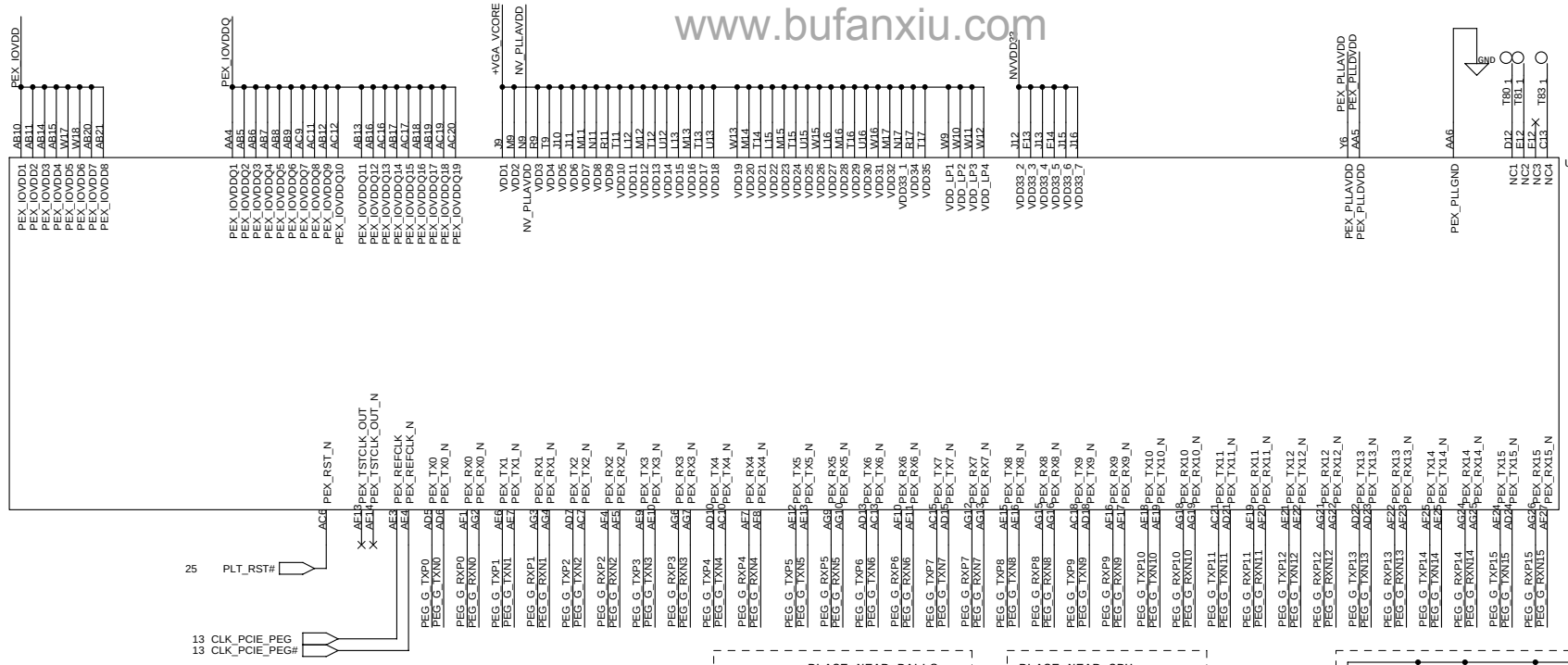
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

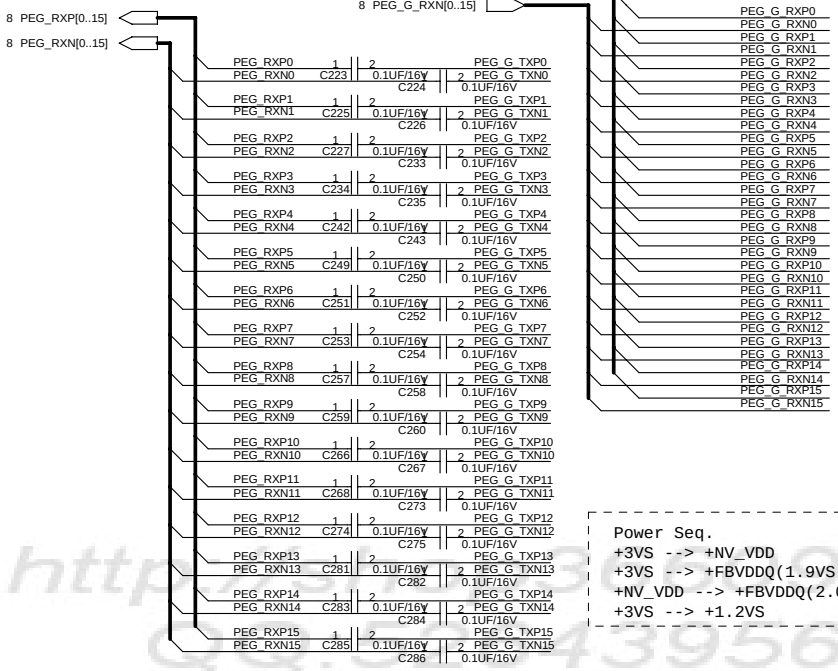


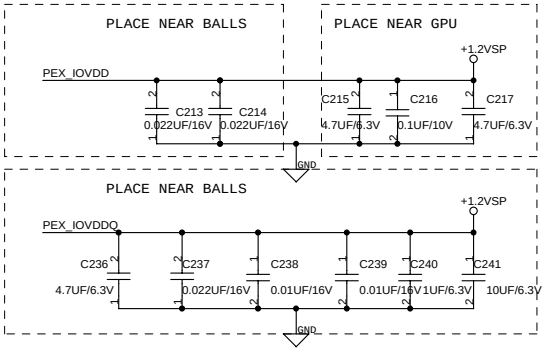
SWAPPED

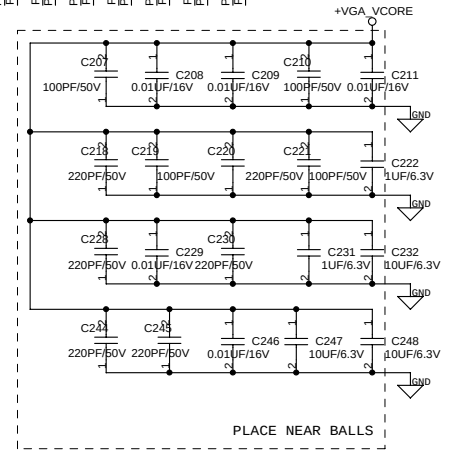


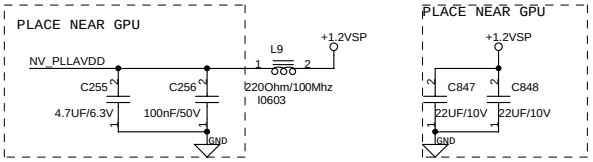
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***DDR2 Res***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **16** OF **63**		RELEASE DATE :	

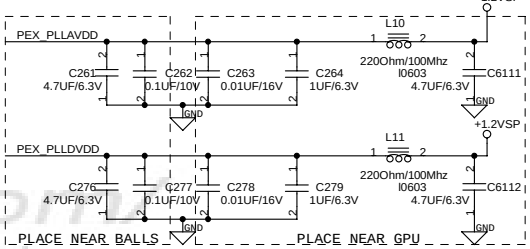




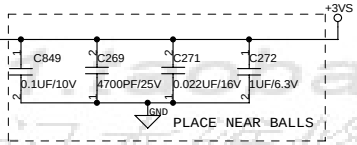




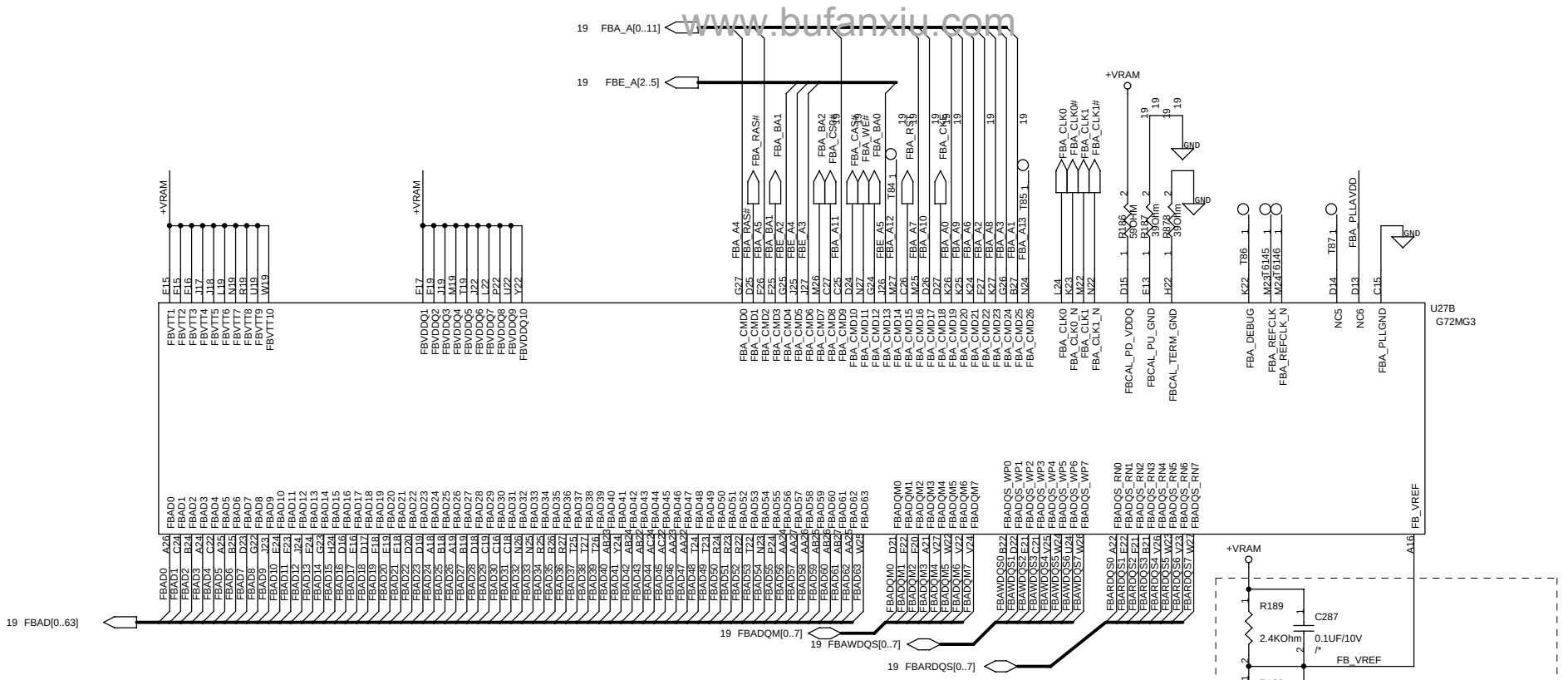




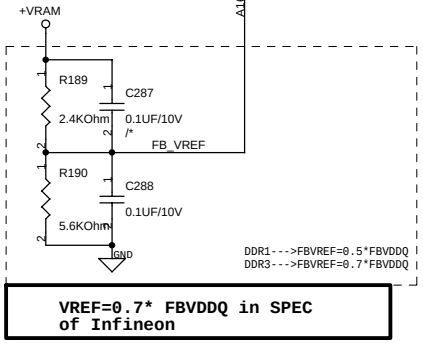
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS

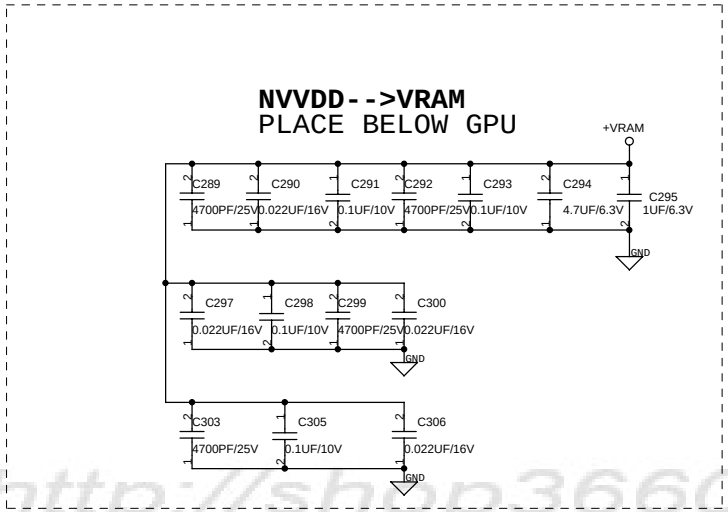


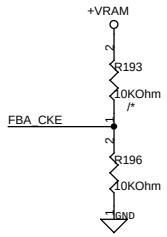
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***G72M64: PCIE***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **17** OF **63**		RELEASE DATE :	

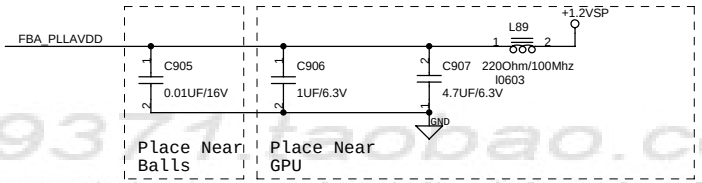


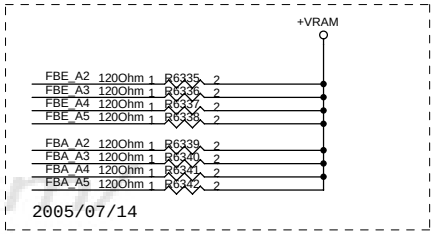
GDDR3 8x32 FBVDDQ 2.0V 144PIN



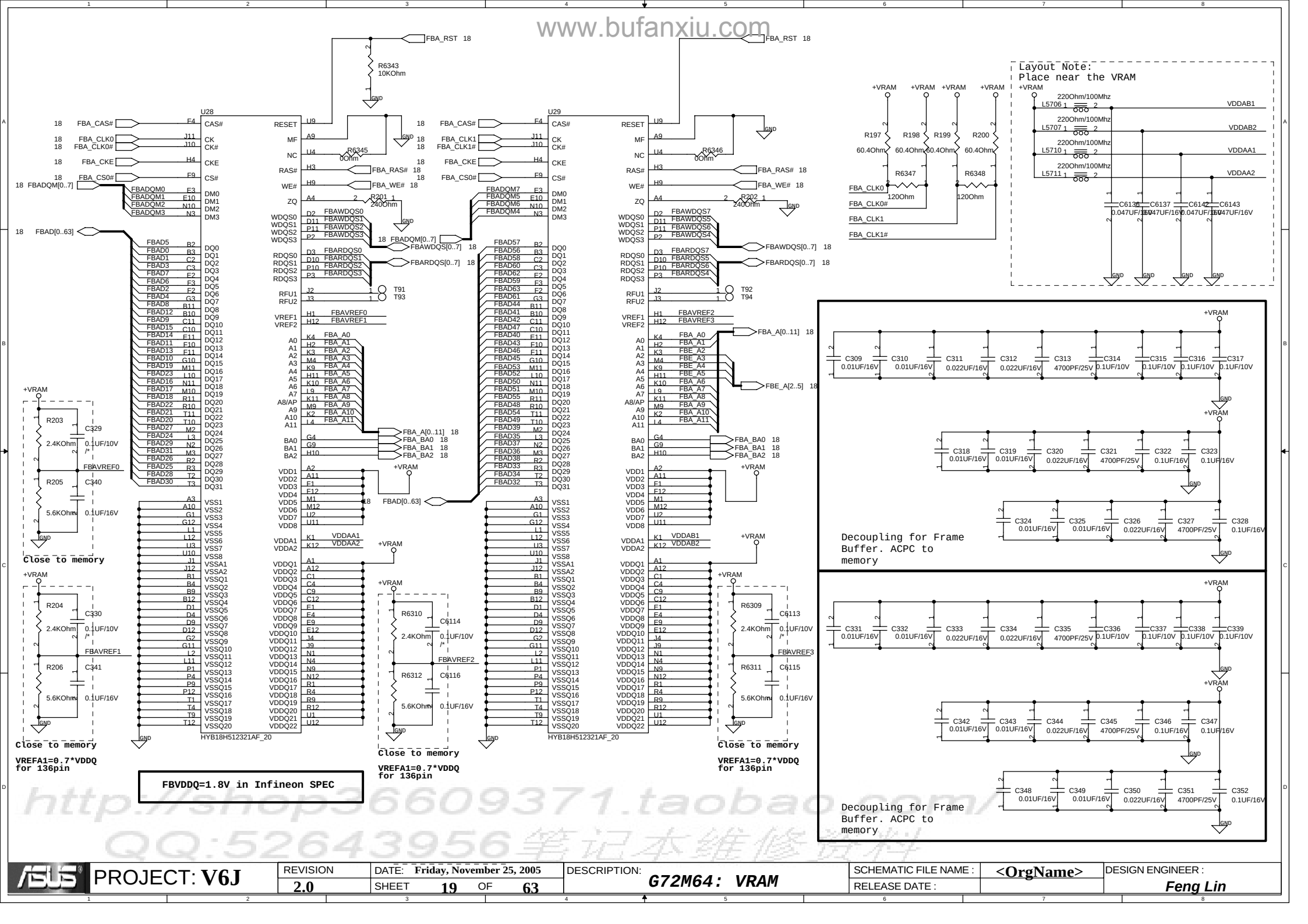








PROJECT: V6J	REVISION	DATE: Friday, November 25, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.0	SHEET 18 OF 63	G72M64: FB	RELEASE DATE :		Feng Lin



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **19** OF **63**	DESCRIPTION: ***G72M64: VRAM***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***Feng Lin***

VGA

U27C G72MG3

DACA_VDD AE2, DACA_VREF AB4, DACA_RSET AD3

I2CA_SCL D10 via R210 33Ohm → DDC2BC 23
I2CA_SDA E10 via R212 33Ohm → DDC2BD 23

DACA_HSYNC AD4 → DAC_HSYNC
DACA_VSYNC AC4 → DAC_VSYNC

DACA_RED AE1 → DAC_R 23
DACA_GREEN AD1 → DAC_G 23
DACA_BLUE AD2 → DAC_B 23

DACA_IDUMP U9 → GND

+3VS → L12 220Ohm/100Mhz → DACA_VDD
C354 4.7UF/6.3V
C355 1UF/6.3V
C356 1UF/6.3V
C357 4700PF/25V
C358 470PF/50V
C359 1UF/6.3V

DACA_VREF, DACA_RSET
R221 137Ohm, R222 124Ohm /*
Adjust RGB signal quality

TV-OUT

U27D G72MG3

DACB_VDD F8, DACB_VREF E7, DACB_RSET D6
R856 10KOhm → GND

I2CB_SCL F9
I2CB_SDA F10

DACB_HSYNC F6
DACB_VSYNC F5

DACB_RED F4 via R857 75Ohm
DACB_GREEN F4 via R858 75Ohm
DACB_BLUE D5 via R862 75Ohm

DACB_IDUMP L9 → GND

LVDS

U27E G72MG3

IFPAB_VPROBE N6 ← C367 0.1UF/16V /*

IFPA_TXD0_N N5 → LVDS_YA0M 22
IFPA_TXD0 N4 → LVDS_YA0P 22
IFPA_TXD1_N R4 → LVDS_YA1M 22
IFPA_TXD1 R5 → LVDS_YA1P 22
IFPA_TXD2_N T6 → LVDS_YA2M 22
IFPA_TXD2 T5 → LVDS_YA2P 22
IFPA_TXD3_N P6
IFPA_TXD3 R6

IFPB_TXD4_N W2 → LVDS_YB0M 22
IFPB_TXD4 W3 → LVDS_YB0P 22
IFPB_TXD5_N AA3 → LVDS_YB1M 22
IFPB_TXD5 AA2 → LVDS_YB1P 22
IFPB_TXD6_N AA1 → LVDS_YB2M 22
IFPB_TXD6 AB1 → LVDS_YB2P 22
IFPB_TXD7_N AB2
IFPB_TXD7 AB3

IFPA_TXC_N U4 → LVDS_CLKAM 22
IFPA_TXC T4 → LVDS_CLKAP 22
IFPB_TXC_N W6 → LVDS_CLKBM 22
IFPB_TXC W5 → LVDS_CLKBP 22

IFPAB_PLLVDD V5, IFPAB_RSET U6
+2.5VS → L14 220Ohm/100Mhz
C368 4.7UF/6.3V
C370 1UF/6.3V
C371 4700PF/25V
C372 470PF/50V
R239 1KOhm /*
IFPAB_PLLGND V6

+LCD_VCC=1.8V

+1.8VS → L15 220Ohm/100Mhz → LCD_IOVDD
C374 4.7UF/6.3V
C375 4.7UF/6.3V
C376 0.01UF/16V
C377 0.022UF/16V
C378 4700PF/25V
C379 220PF/50V
C380 1UF/6.3V
C381 1UF/6.3V

IFPA_IOVDD W4
IFPB_IOVDD Y4

U27F G72MG3

VGA_THERMDC → C353 2200PF/10V → C9 THERMDN
VGA_THERMDA → B9 THERMDP

+3VS
R6358 10KOhm, R6359 10KOhm /*
T99
JTAG_TCK AE27
JTAG_TMS AD26
JTAG_TDI AD27
JTAG_TDO AE26
JTAG_TRST_N AD25
R6360 10KOhm
R6361 10KOhm /*

NC22 D11

I2CC_SCL E9 via R213 33Ohm → DDCC_CLK_MXM
I2CC_SDA D8 via R214 33Ohm → DDCC_DATA_MXM

+3VS +3VS
R208 2.2KOhm
R211 2.2KOhm

R219 10KOhm → GND

GPIO0 A9 → T96
GPIO1 D9 → T97
GPIO2 A10 → T98
GPIO3 B10 → LCD_VDD_EN 22
GPIO4 C10 → LCD_BACKEN 22
GPIO5 C12 GPU_VID0 → GPU_VID 52
GPIO6 B12 GPU_VID1 → T101
GPIO7 A12 GPU_VID2 → T102
GPIO8 A13 G72M_GPIO8
GPIO9 B13 → T413
GPIO10 B15 → T6130
GPIO11 A15 → T414
GPIO12 B16 → T6135

R220 10KOhm → GND

DAC_R R223 150Ohm → GND
DAC_G R224 150Ohm → GND
DAC_B R227 150Ohm → GND
NEAR GPU

Internal Pull-down
GPIO 0,1,2,4,5,6,7

U27G G72MG3

ROMCS_N D1 → T397
ROM_SI F3
ROM_SO D3
ROM_SCLK D2
I2CH_SCL C7 → T428
I2CH_SDA B7 → T429
BUFRST_N A6 → T110
STERED F7
SWAPRDY A7 → T445
TESTMODE D7 via R238 10KOhm
GND AC8

U27H G72MG3

+3VS
C908 0.1UF/10V
C909 0.1UF/10V
NC7 F6
NC8 G6
NC9 J6

NC10 A2 MIOAD0
NC11 B3 MIOAD1
NC12 A3 MIOAD2 → T430
NC13 D4 MIOAD3 → T431
NC14 A4 MIOAD4 → T432
NC15 B4 MIOAD5 → T433
NC16 B6 MIOAD6
NC17 P4
NC18 C6 MIOAD8
NC19 G5 MIOAD9
NC20 V4
NC21 C4 MIOA_HSYNC → T436

R942 2KOhm MIOAD1
R943 2KOhm MIOA_HSYNC
MIOAD6 R944 2KOhm /*
MIOAD8 R945 2KOhm /*
MIOAD9 R946 2KOhm /*
MIOAD0 R947 2KOhm /*

```
MIOAD0----PEX_PLL_EN_TERM

MIOAD1----SUB_VENDOR

MIOAD7-----TVMODE0
MIOAD10----TVMODE1

MIOAD2----USER0
MIOAD3----USER1
MIOAD4----USER2
MIOAD5----USER3

MIOAD6----GPIO_PADCFG0+
MIOAD8----GPIO_PADCFG1+
MIOAD9----GPIO_PADCFG2+
```

+5VS

DAC_VSYNC → U32 74LVC1G32GV → VSYNC_5 23
DAC_HSYNC → U33 74LVC1G32GV → HSYNC_5 23
R252 0Ohm /*
R250 0Ohm /*

Layout Note: Place near the GPU

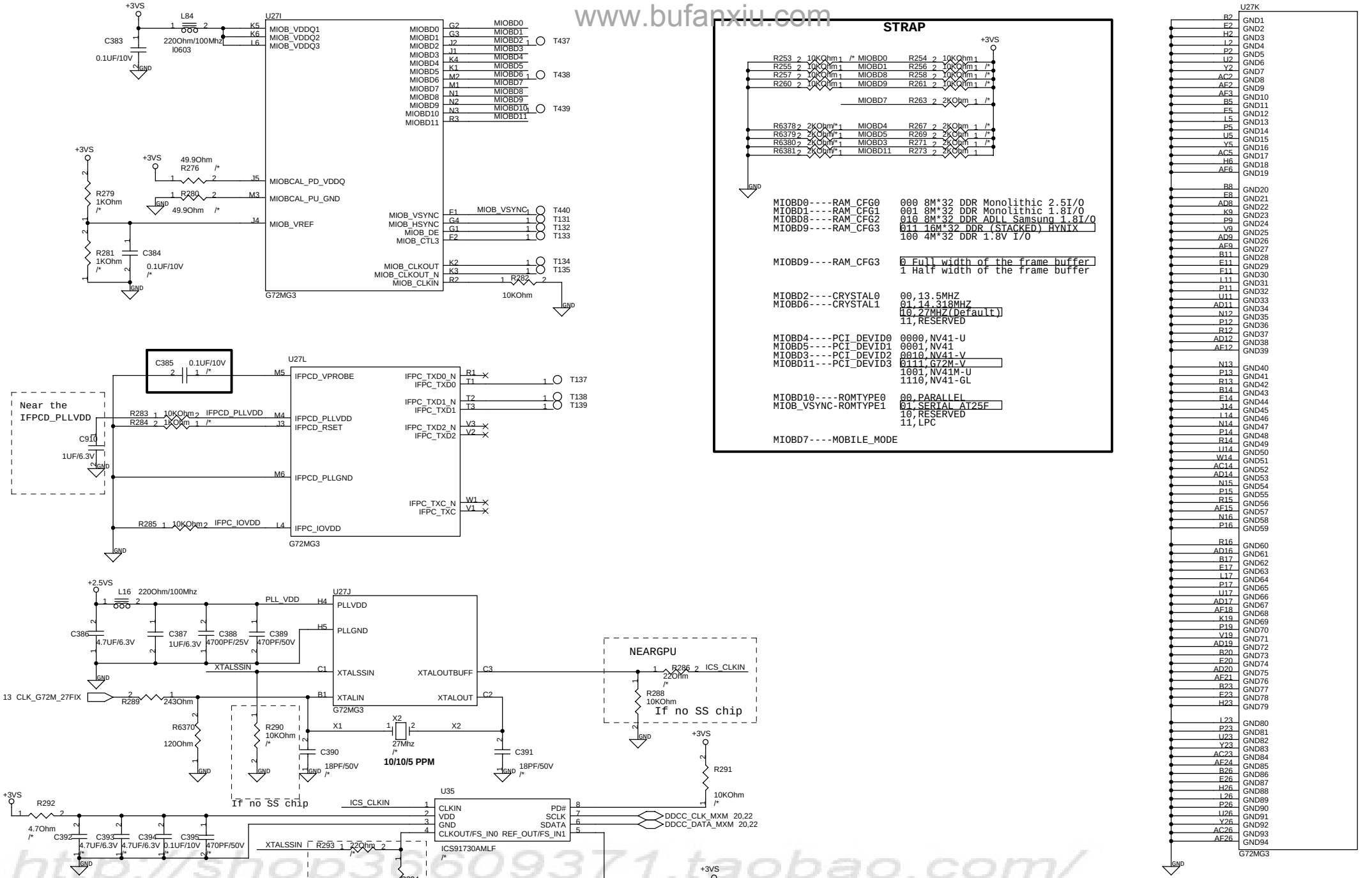
+3VS → R242 200Ohm → C382 1UF/10V

U34 MAX6657MSA
VGA_THERMDA
VGA_THERMDC
VCC, DXP, DXN, OVERT#, SCLK, SDA, ALERT#, GND
R893 /* 0Ohm → 25,26 G72M_THRM#
R226 10KOhm → +3VS

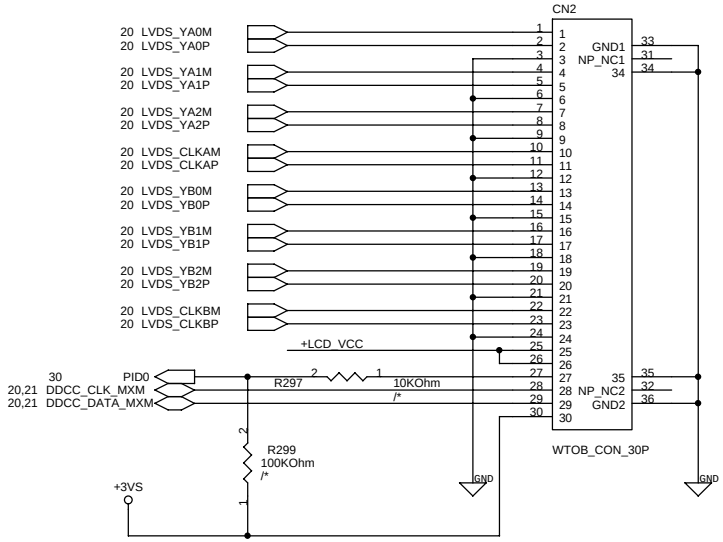
SMB_CLK R243 0Ohm /* → SCL_3S 6,13,14,15,23,36,39,41
SMB_DAT R244 0Ohm /* → SDA_3S 6,13,14,15,23,36,39,41

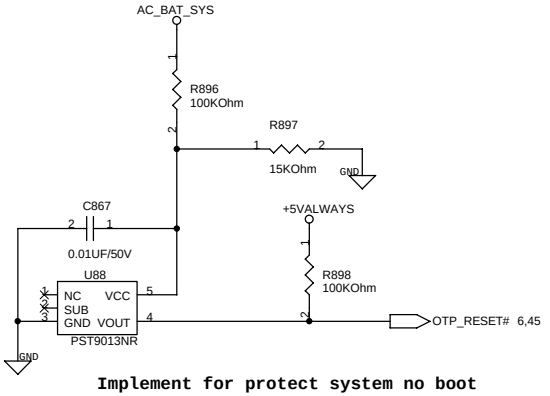
R245 0Ohm DDCC_CLK_MXM → DDCC_CLK_MXM 21,22
R247 0Ohm DDCC_DATA_MXM → DDCC_DATA_MXM 21,22
R948 0Ohm G72M_GPIO8
R6382 10KOhm → +3VS
R6383 /* 0Ohm → G72M_THRO# 30

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **20** OF **63**	DESCRIPTION: ***G72M64: RGB/LCD/ROM/GPIO***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***

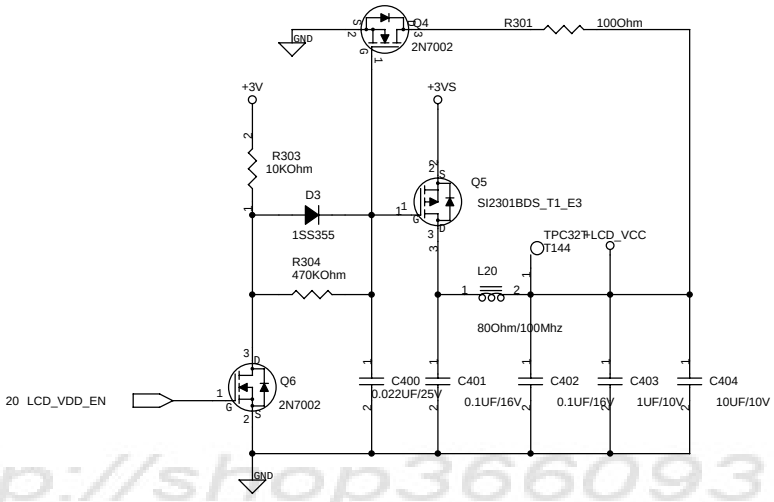


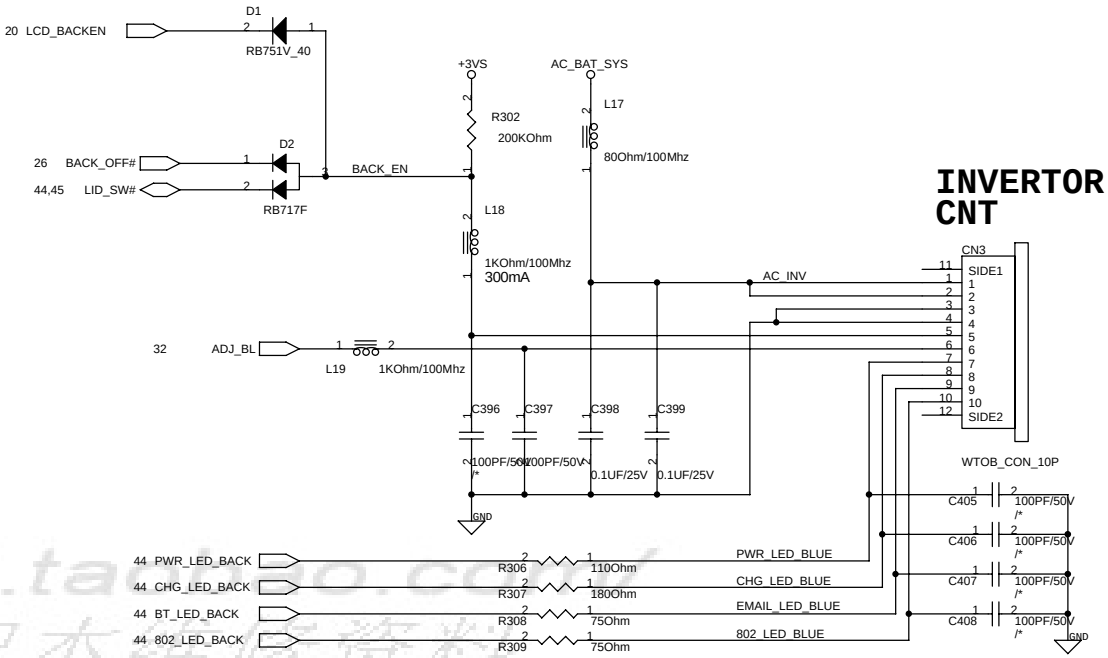
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***G72M64: MIOB/CRYSTAL/TMDS***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **21** OF **63**		RELEASE DATE :	





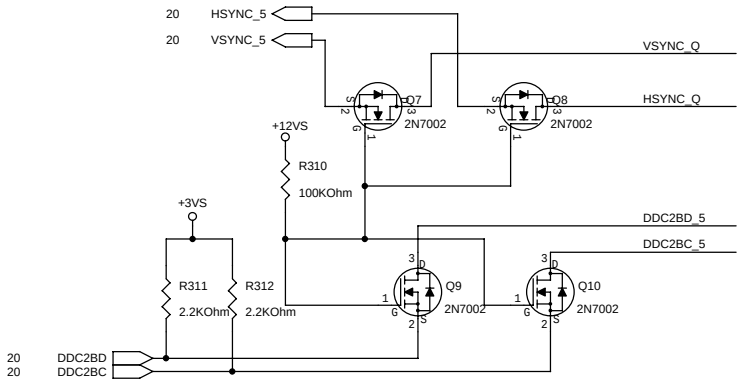
Implement for protect system no boot

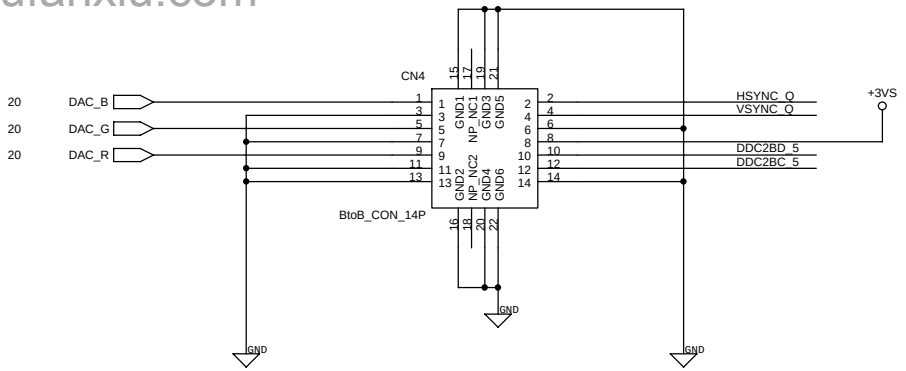


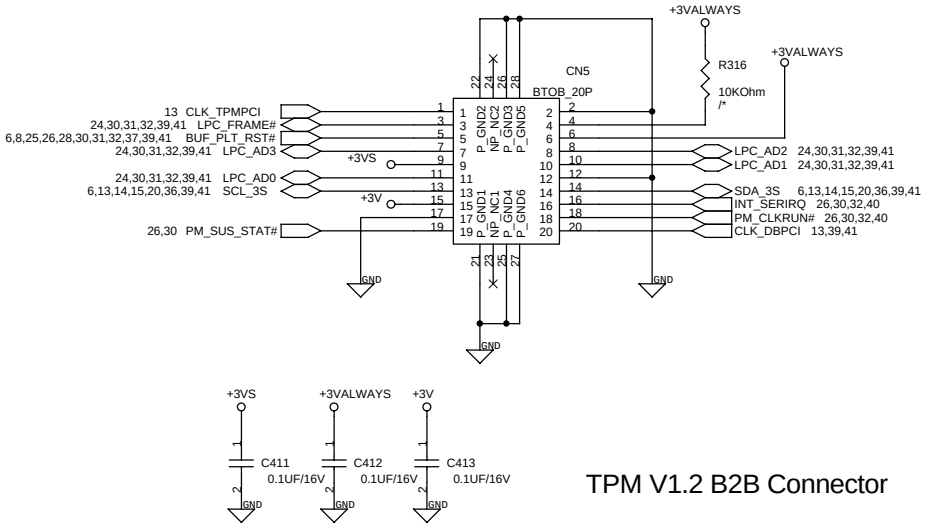


INVERTOR CNT

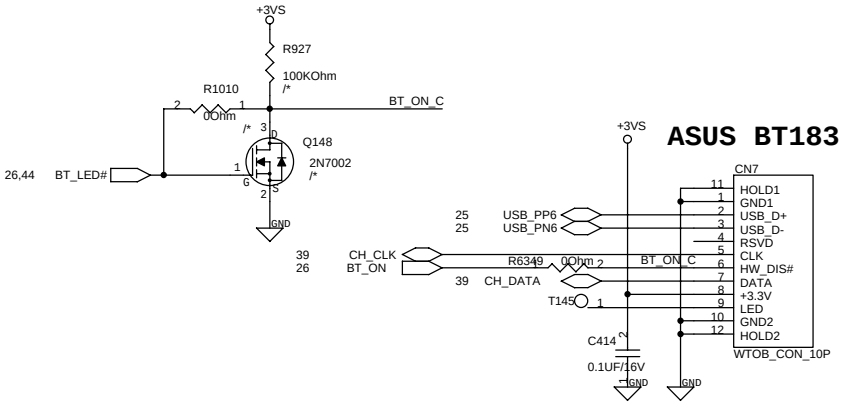
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***LVDS & INVERTER***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **22** OF **63**		RELEASE DATE :		





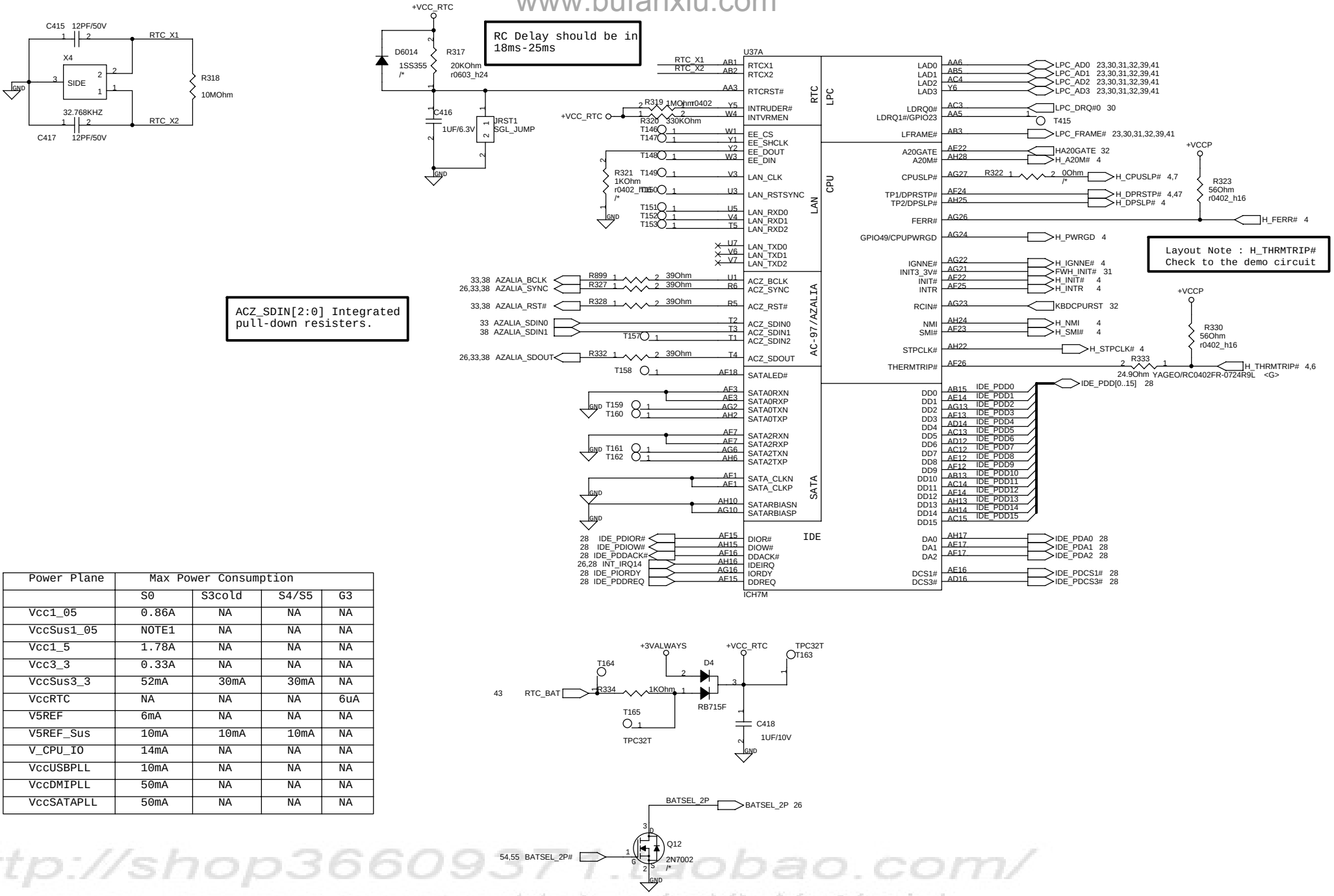


TPM V1.2 B2B Connector



BT B2B Connector

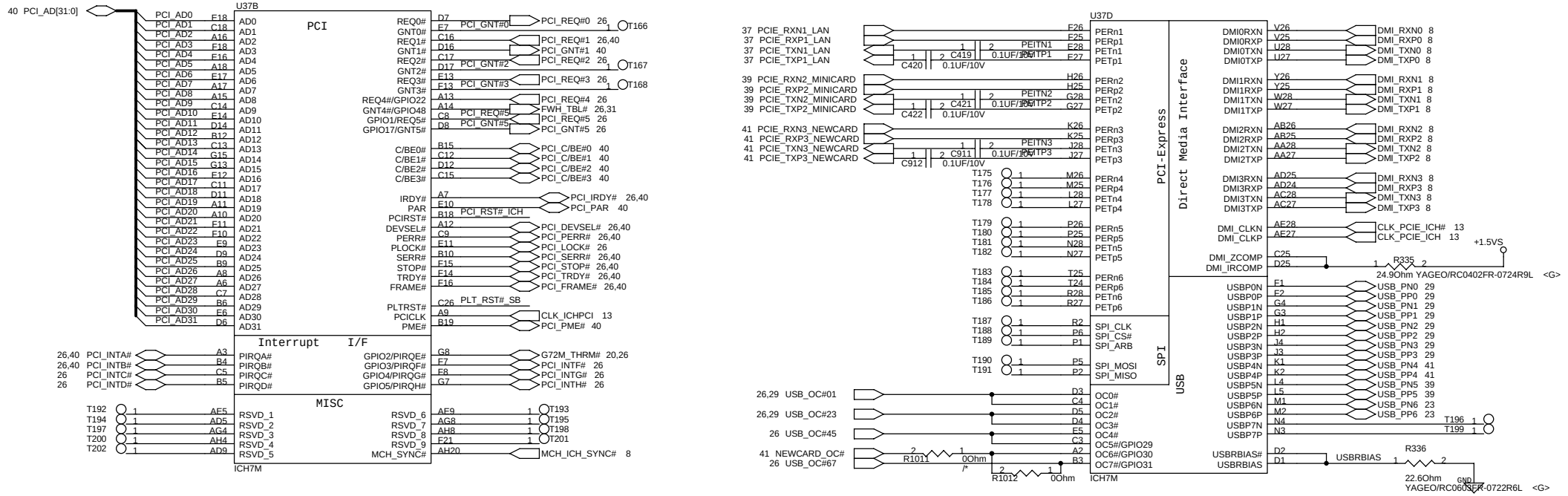
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **23** OF **63**	DESCRIPTION: ***CRT & TPM & BT***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***



Power Plane	Max Power Consumption			
	S0	S3cold	S4/S5	G3
Vcc1_05	0.86A	NA	NA	NA
VccSus1_05	NOTE1	NA	NA	NA
Vcc1_5	1.78A	NA	NA	NA
Vcc3_3	0.33A	NA	NA	NA
VccSus3_3	52mA	30mA	30mA	NA
VccRTC	NA	NA	NA	6uA
V5REF	6mA	NA	NA	NA
V5REF_Sus	10mA	10mA	10mA	NA
V_CPU_IO	14mA	NA	NA	NA
VccUSBPLL	10mA	NA	NA	NA
VccDMIPLL	50mA	NA	NA	NA
VccSATAPLL	50mA	NA	NA	NA

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **24** OF **63**	DESCRIPTION: ***ICH7: IDE/AC97/LPC/RTC***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***Feng Lin***



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **25** OF **63**	DESCRIPTION: ***ICH7: PCI/INT/DMI/USB***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***Feng Lin***

U37C

ICH7M

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SYS GPIO: RI#, SPKR, SUS_STAT#, SYS_RST#, GPIO0/BM_BUSY#, SMBALERT#/GPIO11, GPIO18/STPPCI#, GPIO20/STPCPU#, GPIO26, GPIO27, GPIO28, GPIO32/CLKRUN#, GPIO33/AZ_DOCK_EN#, GPIO34/AZ_DOCK_RST#, WAKE#, SERIRQ, THRM#, VRMPWRGD

GPIO: GPIO6, GPIO7, GPIO8

SATA GPIO: GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA2GP, GPIO37/SATA3GP

Clocks: CLK14, CLK48, SUSCLK

Power MGT: GPIO16/DPRSLPVR, TP0/BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, GPIO24, GPIO25, GPIO35, GPIO38, GPIO39

SCL_3A, SDA_3A, LINKALERT#, SM_LINK0, SM_LINK1, RING#, ICH_SPKR, PM_SUS_STAT#, SYS_RST#, PM_BMBUSY#, SMBALERT#, STP_PCI#, STP_CPU#, OP_SD#, WLAN_ON, PWR_1HZ, PM_CLKRUN#, BT_ON, FWH_WP#, PX_WK#, INT_SERIRQ, PM_THRM#, VRMPWRGD, ICH7_PWROK, BACK_OFF#, WIRELESS_#, EXTSMI#_3A

BATSEL_2P, SATA_DET_#1, PCB_VID0, CLK_ICH14, CLK_USB48, T205, SLP_S3#, SLP_S4#, SLP_S5#, T206, SUSB#, SUSC#, PWROK, ICH7_PWROK, AC22, PM_DPRSLPVR, PM_BATLOW#, R349 0Ohm, BAT_LLOW#_OC, PM_PWRBTN#, R902 r0402 100KOhm +3VSUS, BUF_PLT_RST#, Y4, PM_RSMRST#, ACIN_OC#_ICH, KBDSCI_3, BATIN_OC#_ICH, R4 GPIO14 R6303 0Ohm, LID_ICH#_3A, 802_LED#, R3 T416, D20 T6136, AD21 T214, PCB_VID1, PCB_VID2

C430 10PF/50V c0603 /*

R351 10KOhm r0402

PWROK active no sooner than 100ms after Vcc3_3 and Vcc1_5

+3VS

INTERNAL PULL-DOWN
PULL-UP : PCI Express
Port config bit 1
R359 10KOhm /* → AZALIA_SDOUT 24,33,38

INTERNAL PULL-DOWN
PULL-UP : PCI Express
Port config bit 0
R361 10KOhm /* → AZALIA_SYNC 24,33,38

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT
R363 1KOhm /* ICH_SPKR

+3VSUS

R358 r0402 10KOhm SYS_RST# → 45 AUXPWROK

45,47,57 VRM_PWRGD — R903 0Ohm /* — VRMPWRGD

R364 1KOhm /* → FWH_TBL# 25,31

INTERNAL PULL-UP
PULL-DOWN : Boot BIOS
destination select

R366 1KOhm /* → PCI_GNT#5 25

INTERNAL PULL-UP
PULL-DOWN : Boot BIOS
destination select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

INTERNAL PULL-DOWN SIGNALS :

AC_BITCLK, AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , PDDREQ , SPKR , USB[7:0][P,N], SPI_ARB, SPI_CLK, GPIO[16]

INTERNAL PULL-UP SIGNALS :

EE_DIN , EE_DOUT , EE_CS , GPIO[17] , LAD[3:0]# , LDRQ[0:1] , LAN_RXD[2:0] , PME# , PWRBTN# , TP3 , SATALED# , GNT[5:0]

+3V

Q136 2N7002 /*

32,56 BAT_IN_OC# → BATIN_OC#_ICH

Q137 2N7002 /*

32,45,56 ACIN_OC# → ACIN_OC#_ICH

+3VSUS

PWR_1HZ R6417 100KOhm /*
PX_WK# R6366 1KOhm
WLAN_ON R6350 10KOhm /*
802_LED# R6304 8.2KOhm
SCL_3A R356 2.2KOhm
SDA_3A R357 2.2KOhm
GPIO14, BATIN_OC#_ICH → RN19A, RN19B, RN19C, RN19D
SM_LINK0, SM_LINK1, PM_BATLOW#, LINKALERT# → RN8A, RN8B, RN8C, RN8D

+3VS

20,25 G72M_THRM#
25 PCI_INTF#
25 PCI_INTG#
25 PCI_INTH#
→ RN17A, RN17B, RN17C, RN17D

24,28 INT_IRQ14 — R904 10KOhm
23,44 BT_LED# — R6351 10KOhm

PM_SUS_STAT# R370 4.7KOhm /*

FWH_WP# R373 100KOhm
OP_SD# R375 10KOhm /*
ICH7_PWROK R6363 10KOhm

+3VS

25,40 PCI_FRAME#
25,40 PCI_IRDY#
25,40 PCI_TRDY#
25,40 PCI_STOP#
25,40 PCI_SERR#
25,40 PCI_DEVSEL#
25,40 PCI_PERR#
25 PCI_LOCK#
→ RP1A–RP1H (8.2KOhm)

INT_SERIRQ, PM_THRM#, 25 PCI_REQ#0, 25,40 PCI_REQ#1, 25 PCI_REQ#2, 25 PCI_REQ#3, 25 PCI_REQ#4, 25 PCI_REQ#5, 25 PCI_INTD#, 25 PCI_INTC#, 25,40 PCI_INTA#, 25,40 PCI_INTB# → RP2A–RP3D (8.2KOhm)

BATSEL_2P, SATA_DET_#1, PM_CLKRUN#, 32,55 CHG_FULL_OC → RP3E–RP3H (8.2KOhm)

C431 0.1UF/16V

+3VSUS

KBDSCI_3, RING#, ACIN_OC#_ICH, 25,29 USB_OC#01, 25,29 USB_OC#23, 25 USB_OC#45, 25 USB_OC#67, SMBALERT# → RP4A–RP4H (10kOhm)

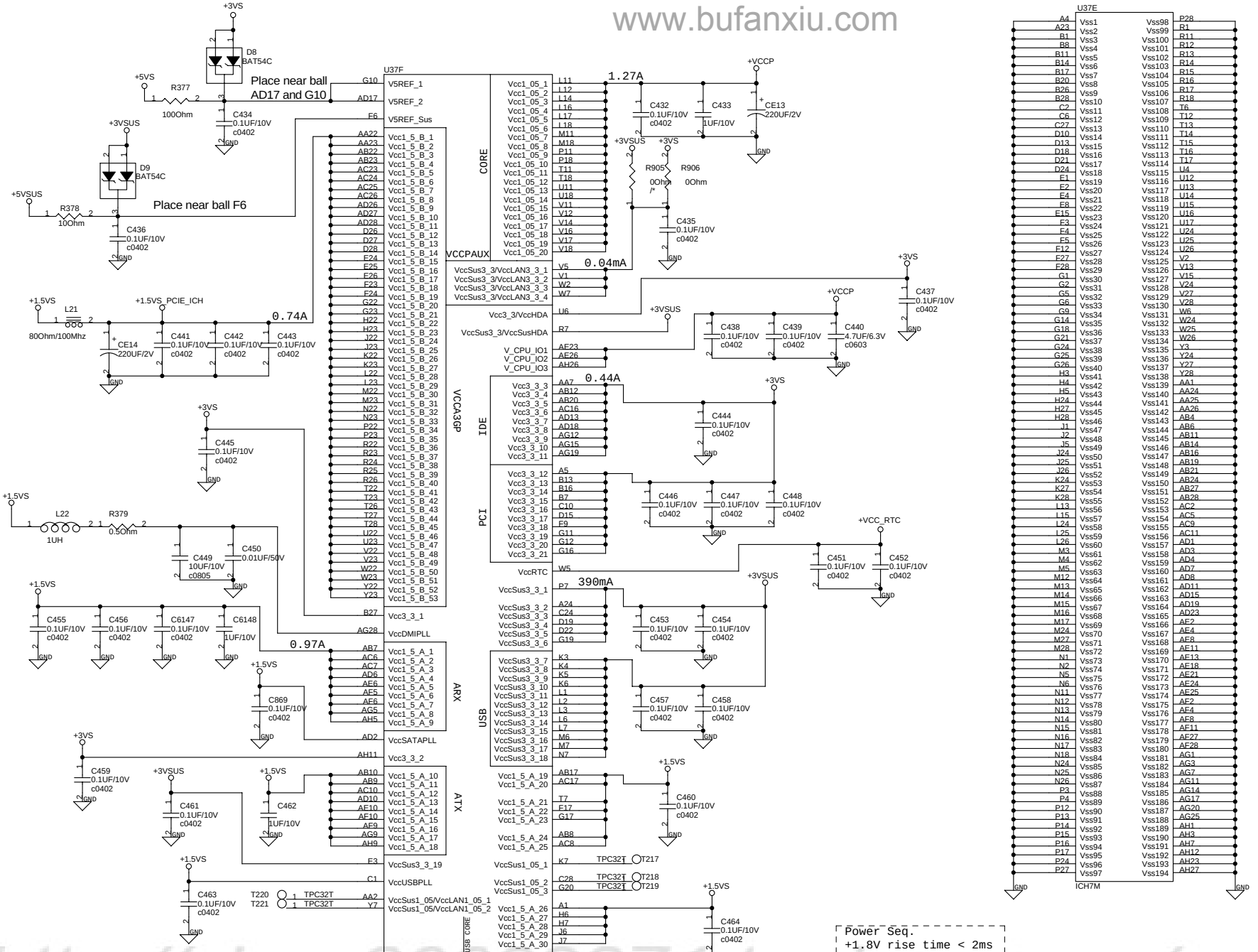
+3VS

R410 R411 R412 100KOhm /*
PCB_VID0, PCB_VID1, PCB_VID2
R413 R414 R415 10KOhm /*

0 0 0 : V1.0
0 0 1 : V1.1
1 0 0 : V2.0

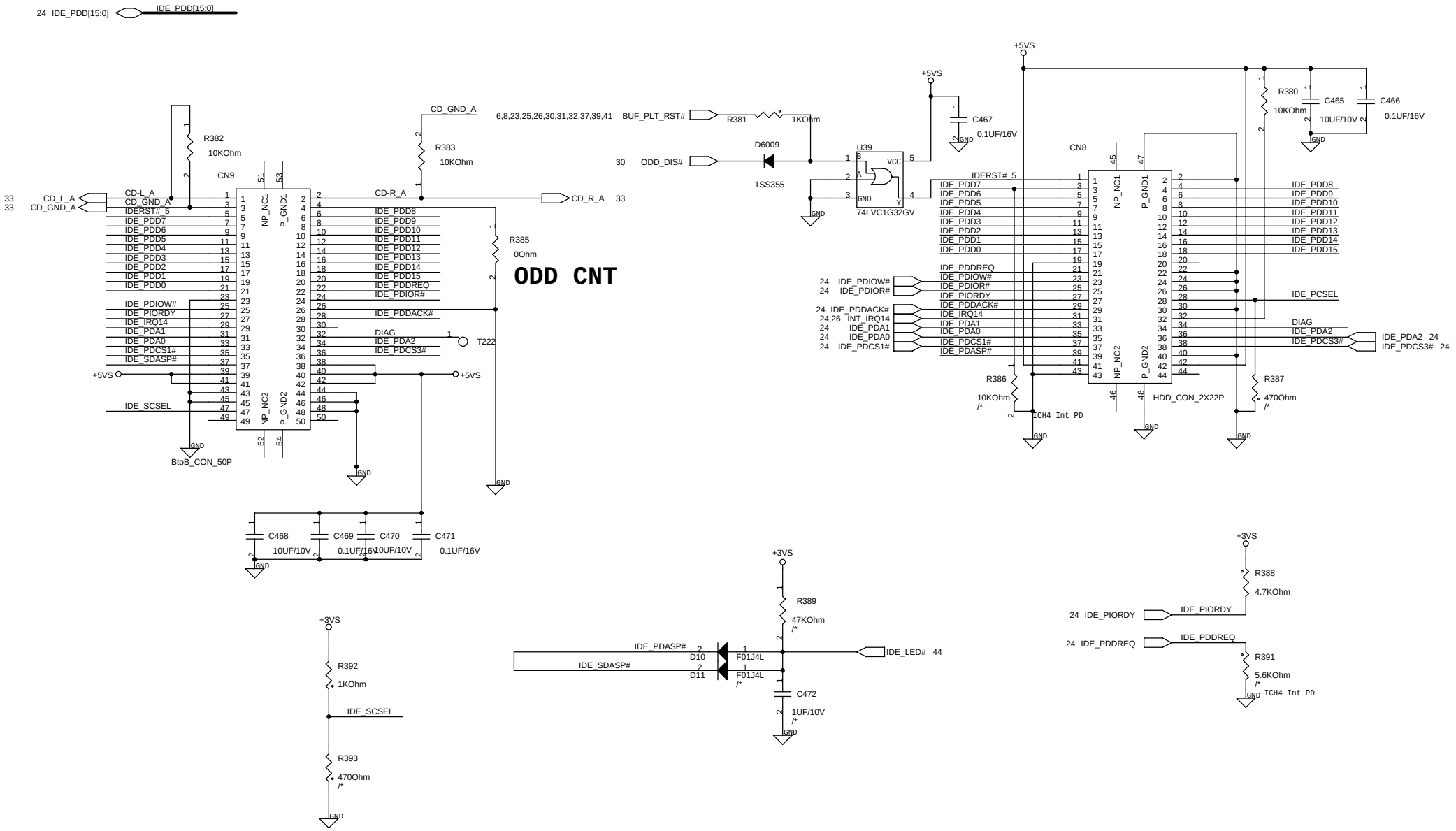
PCB_VID2	PCB_VID1	PCB_VID0
X	X	X

PROJECT: V6J	REVISION: 2.0	DATE: Friday, November 25, 2005	SHEET 26 OF 63	DESCRIPTION: ICH7: SMB/PWR/CLK/GPIO	SCHEMATIC FILE NAME: <OrgName>	RELEASE DATE:	DESIGN ENGINEER: Feng Lin

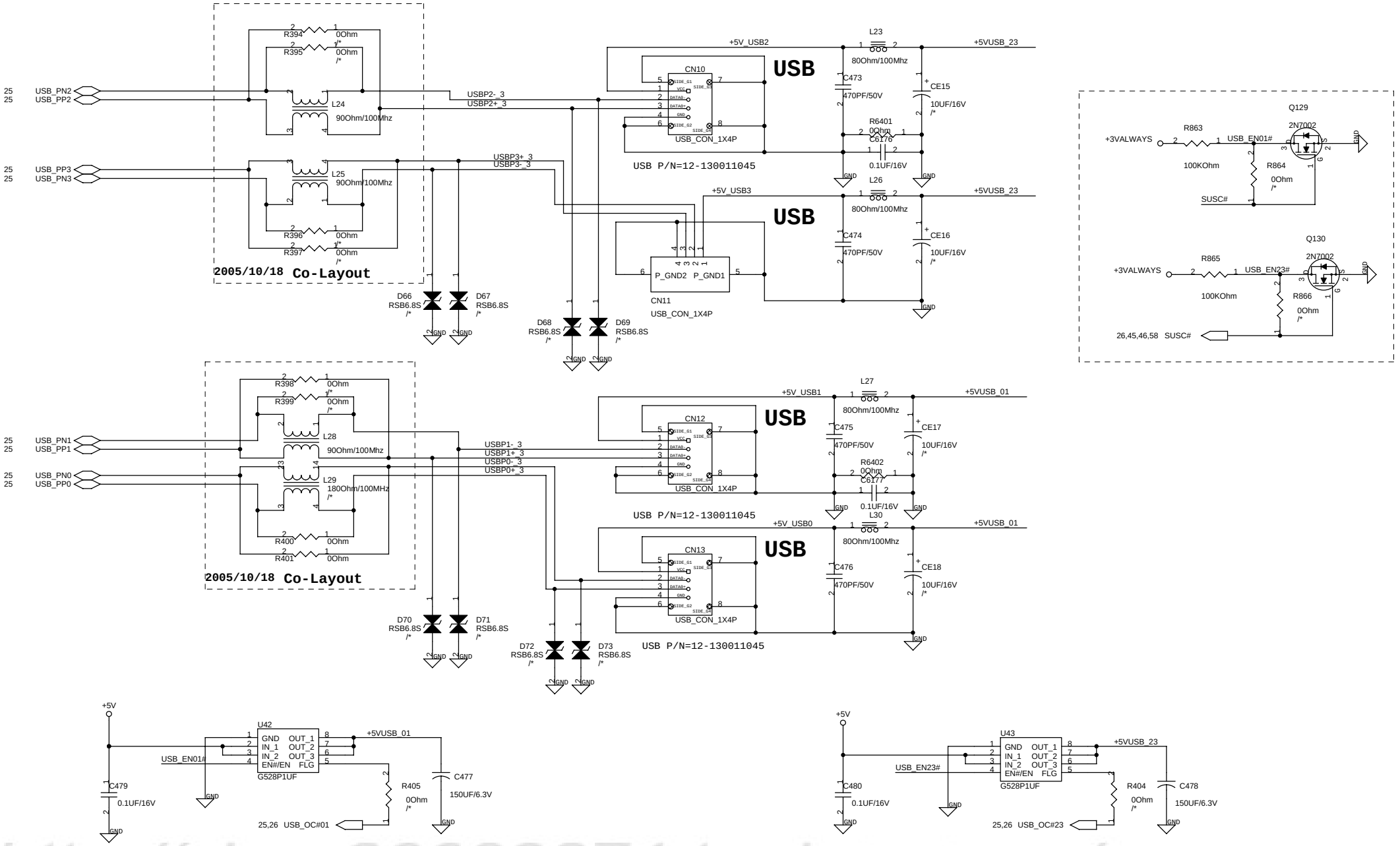


Power Seq.
+1.8V rise time < 2ms
+1.5VS --> +VCCP
+5VS --> +3VS
+5VSUS --> +3VSUS

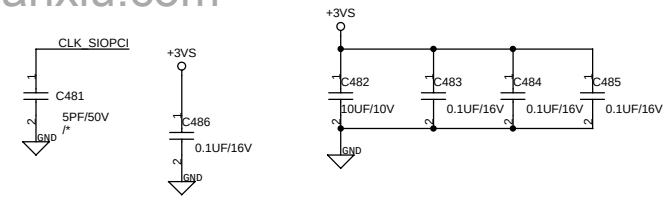
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***ICH7: PWR/Caps***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **27** OF **63**		RELEASE DATE :	

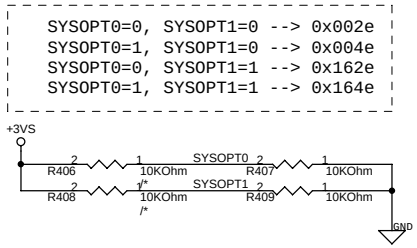


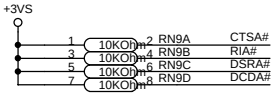
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***HDD & ODD CONN.***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **28** OF **63**		RELEASE DATE :	



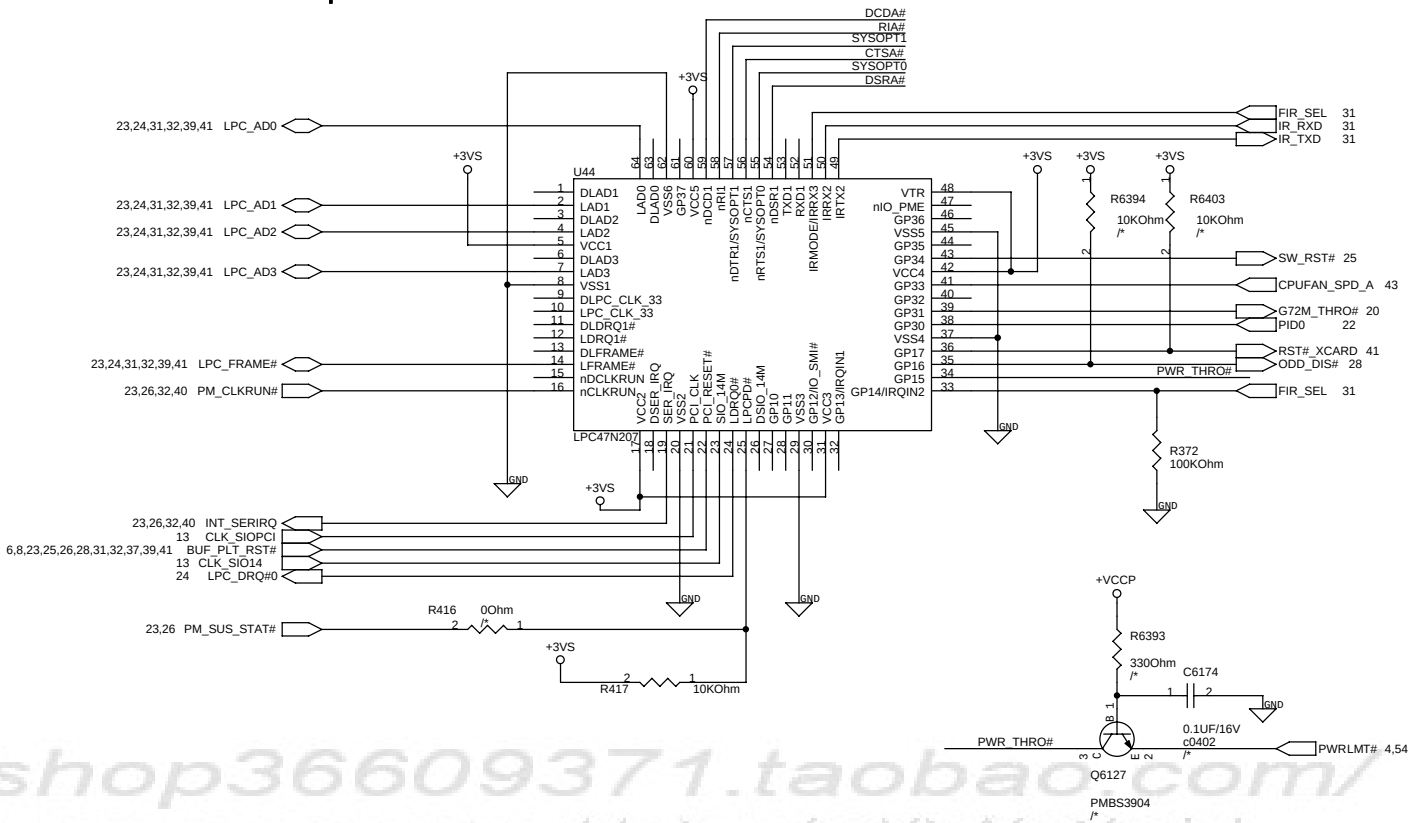
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***USB PORTS***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **29** OF **63**		RELEASE DATE :	



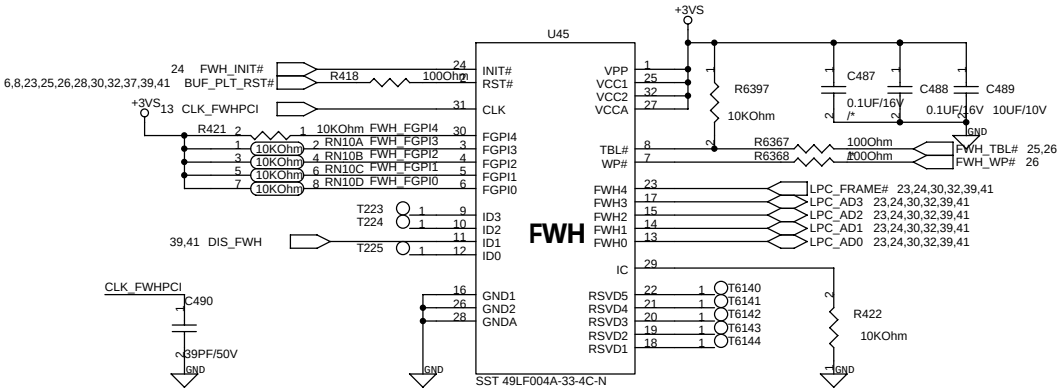




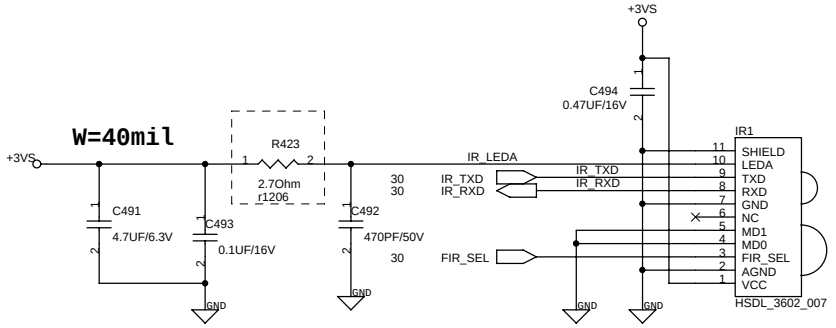
Super I/O



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **30** OF **63**	DESCRIPTION: ***SUPER I/O 47N207***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE : DESIGN ENGINEER : ***Julian Kuo***



PLCC32 Socket Part Number :
12G04300032F,12-043000321
,12-043000323,12-04300032J



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **31** OF **63**	DESCRIPTION: ***FIR & FWH***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

U47 M38857 80mA

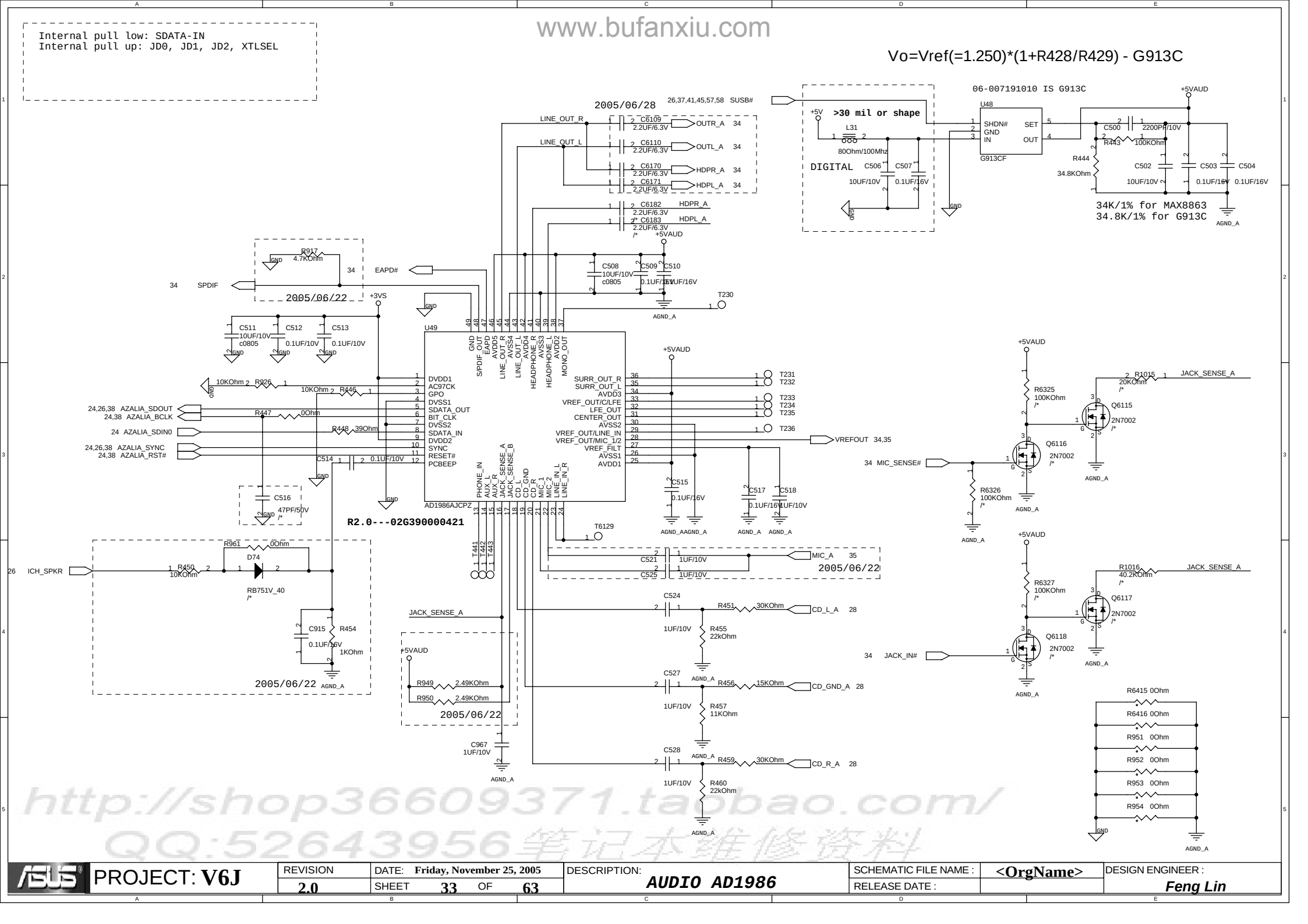
CN14 FPC_CON_28P

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **32** OF **63**	DESCRIPTION: ***KBC M38857***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Julian Kuo***

Internal pull low: SDATA-IN
Internal pull up: JD0, JD1, JD2, XTLSEL

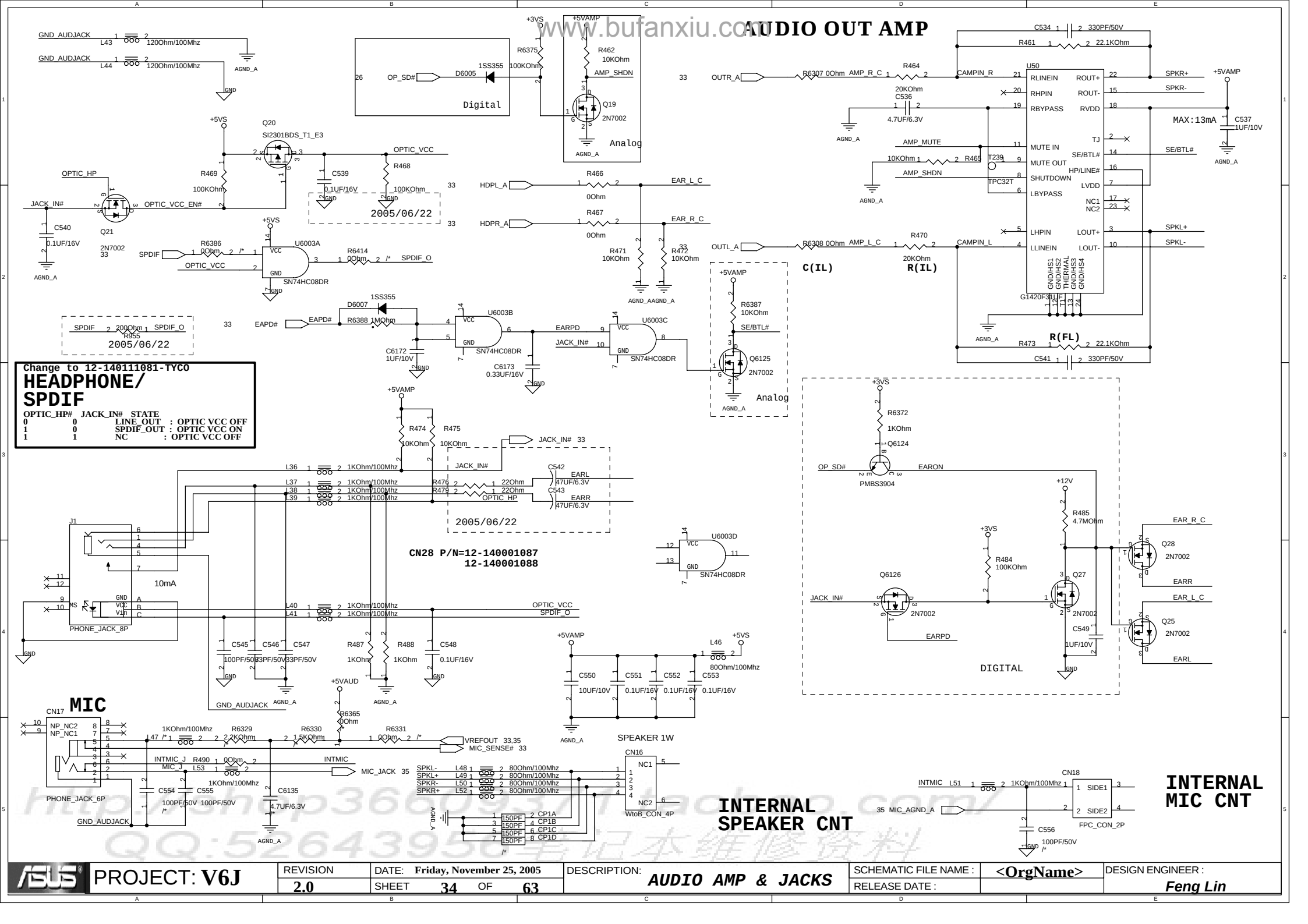
Vo=Vref(=1.250)*(1+R428/R429) - G913C



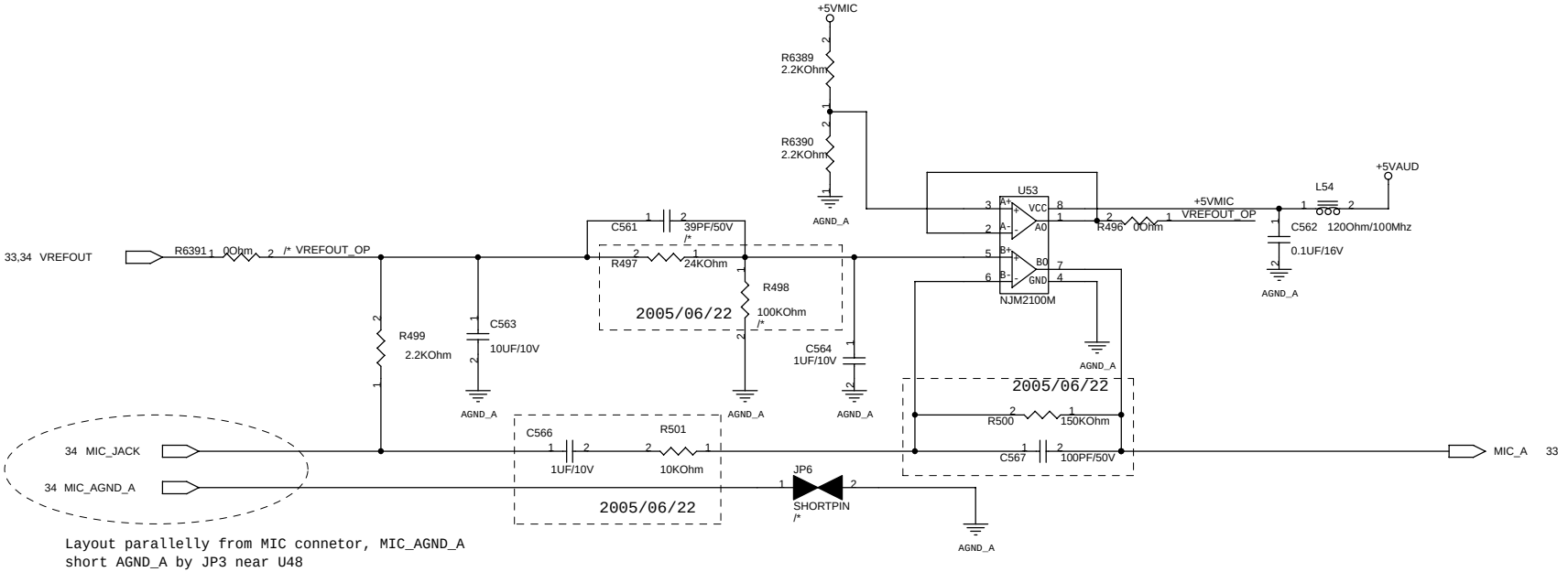
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **33** OF **63**	DESCRIPTION: ***AUDIO AD1986***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***Feng Lin***

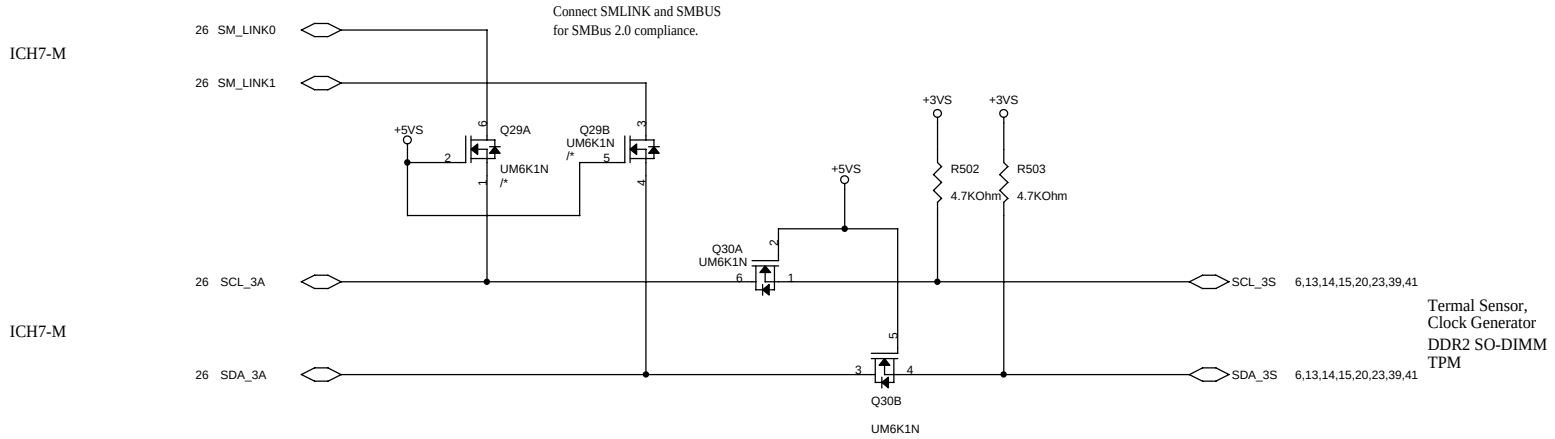
AUDIO OUT AMP



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***AUDIO AMP & JACKS***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **34** OF **63**		RELEASE DATE :	



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **35** OF **63**	DESCRIPTION: ***MIC AMP***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
				RELEASE DATE :		



+3VALWAYS +3VALWAYS 23,24,29,32,44,45,46,51,60
+3VSUS +3VSUS 26,27,32,37,41,45,48
+5VALWAYS +5VALWAYS 22,48,51,54
+5VSUS +5VSUS 27,44,48
+3V +3V 22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+5V +5V 14,29,33,41,44,46,56,58
+12V +12V 34,42,58
+3VS +3VS 6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+5VS +5VS 20,27,28,32,34,39,43,44,45,46,47,58
+12VS +12VS 23,44,58
VTT_REF VTT_REF 8,14,15,16
+2.5VS +2.5VS 10,20,21,46,51
+1.8VS +1.8VS 20,46,58
+0.9VS +0.9VS 16,50
+1.5VS +1.5VS 5,8,10,11,25,27,39,41,46,49
+VCC_RTC +VCC_RTC 24,27
+1.8V +1.8V 8,11,14,15,46,50
+3VA +3VALWAYS 23,24,29,32,44,45,46,51,60
+5VA +5VALWAYS 22,48,51,54
+5VAUD +5VAUD 33,34,35
VTT_REF VTT_REF 8,14,15,16
A/D_DOCK_IN A/D_DOCK_IN 43,54,56,57
+3VSUS_PE +3VSUS_PE 41
+3VS_PE +3VS_PE 41
+1.5VS_PE +1.5VS_PE 41

NEWCARD

YONAH

+VCCP +VCCP 4,5,6,7,8,10,11,24,27,30,46,49
+VCORE +VCORE 5,6,46,47
+1.5VS +1.5VS 5,8,10,11,25,27,39,41,46,49

Calistoga

+VCCP +VCCP 4,5,6,7,8,10,11,24,27,30,46,49
+1.5VS +1.5VS 5,8,10,11,25,27,39,41,46,49
+3VS +3VS 6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+1.8VS +1.8VS 20,46,58
VTT_REF VTT_REF 8,14,15,16
+2.5VS +2.5VS 10,20,21,46,51
+1.8V +1.8V 8,11,14,15,46,50

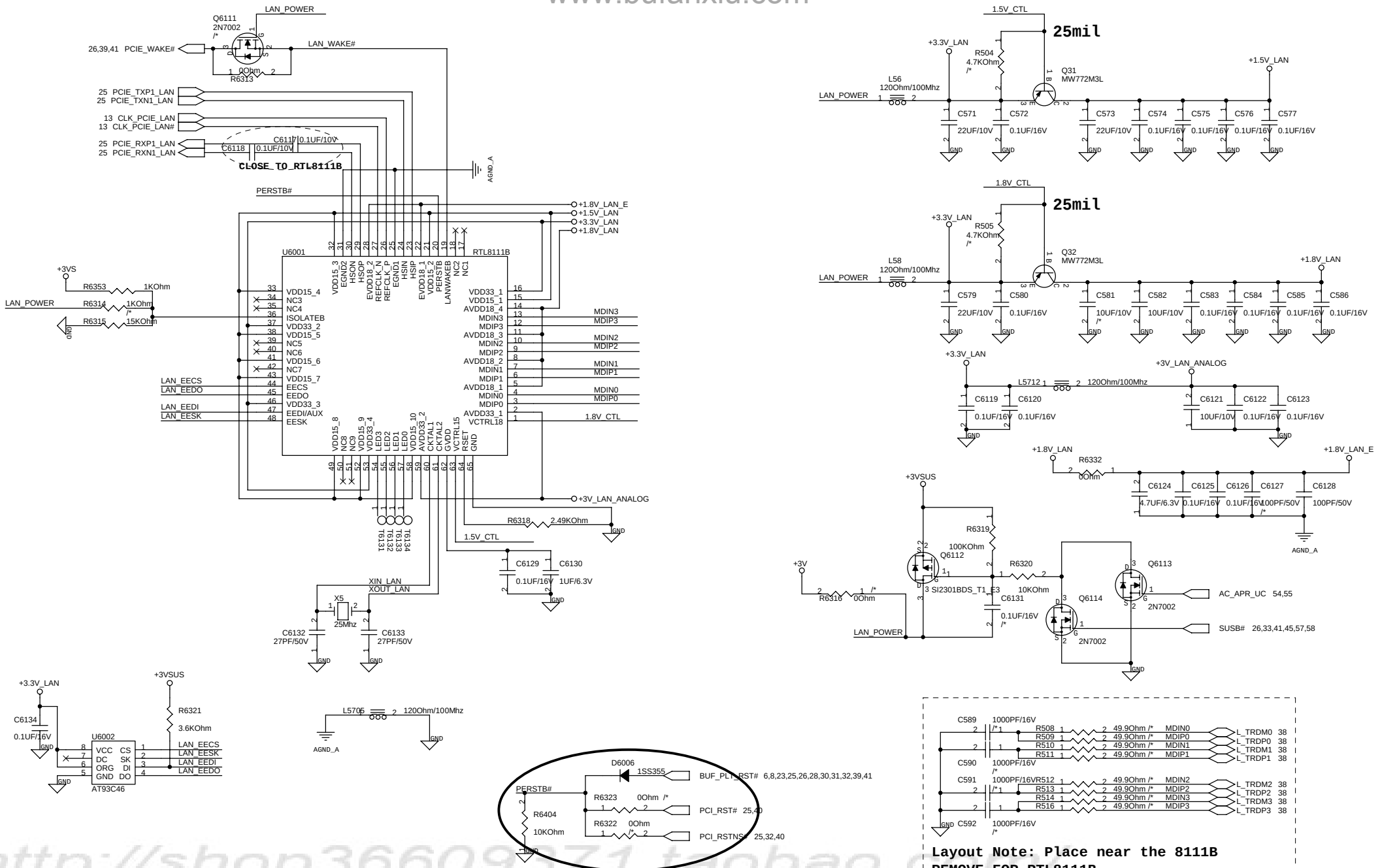
G72M G3-64

+VGA_VCORE +VGA_VCORE 17,46,52
+1.2VSP +1.2VSP 17,18,46,53
+3VS +3VS 6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+VRAM +VRAM 18,19,46,52
+2.5VS +2.5VS 10,20,21,46,51
+1.8VS +1.8VS 20,46,58
+5VS +5VS 20,27,28,32,34,39,43,44,45,46,47,58

ICH7

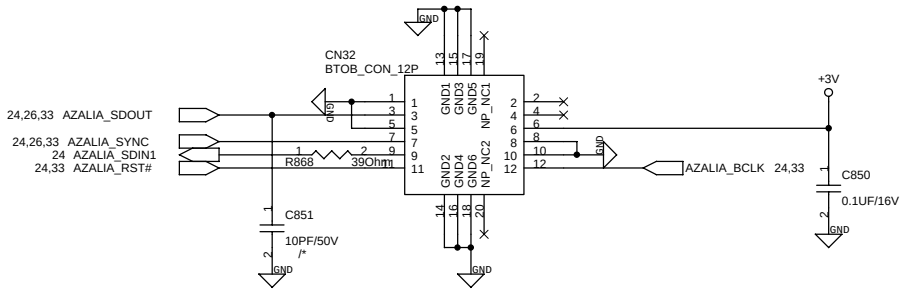
+VCC_RTC +VCC_RTC 24,27
+VCCP +VCCP 4,5,6,7,8,10,11,24,27,30,46,49
+3V +3V 22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+1.5VS +1.5VS 5,8,10,11,25,27,39,41,46,49
+3VSUS +3VSUS 26,27,32,37,41,45,48
+5VSUS +5VSUS 27,44,48

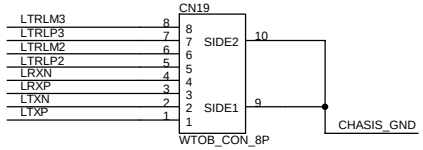
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***SMBUS***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **36** OF **63**		RELEASE DATE :		



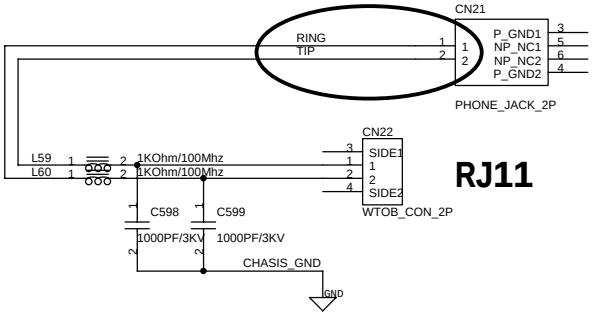
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***LAN_RTL8111B***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **37** OF **63**		RELEASE DATE :	

MDC CNT

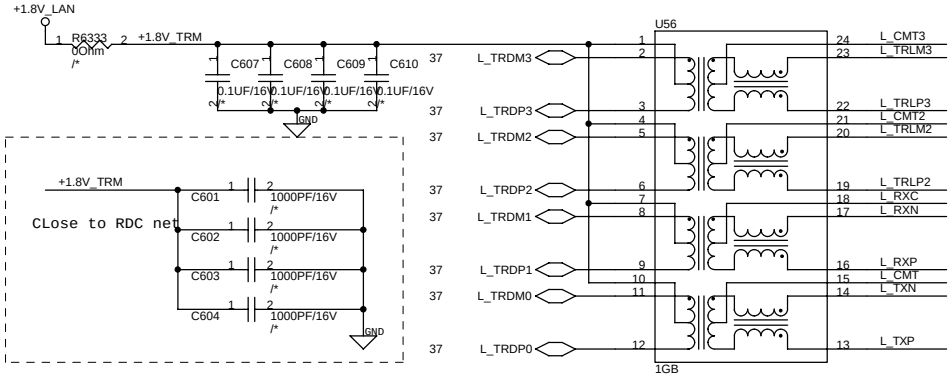




RJ45



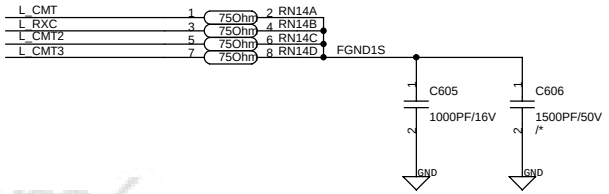
RJ11



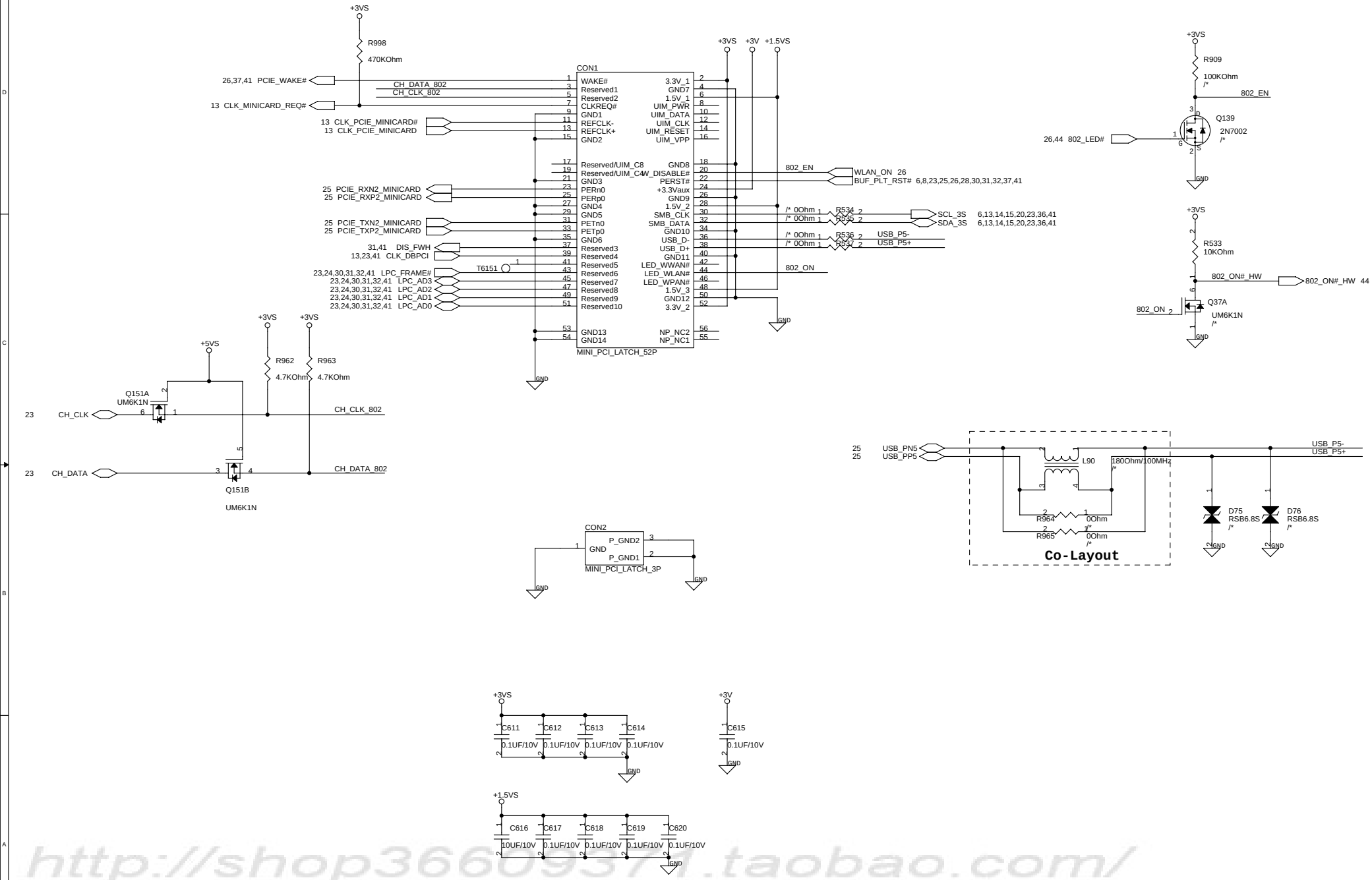
Change to LFE9209A
09-05102307 is BOTHHAND
24HST1041-2
PLACE NEAR TRANSFORMER

L_TRLP2	LTRLP2
L_TRLM2	LTRLM2
L_TRLP3	LTRLP3
L_TRLM3	LTRLM3

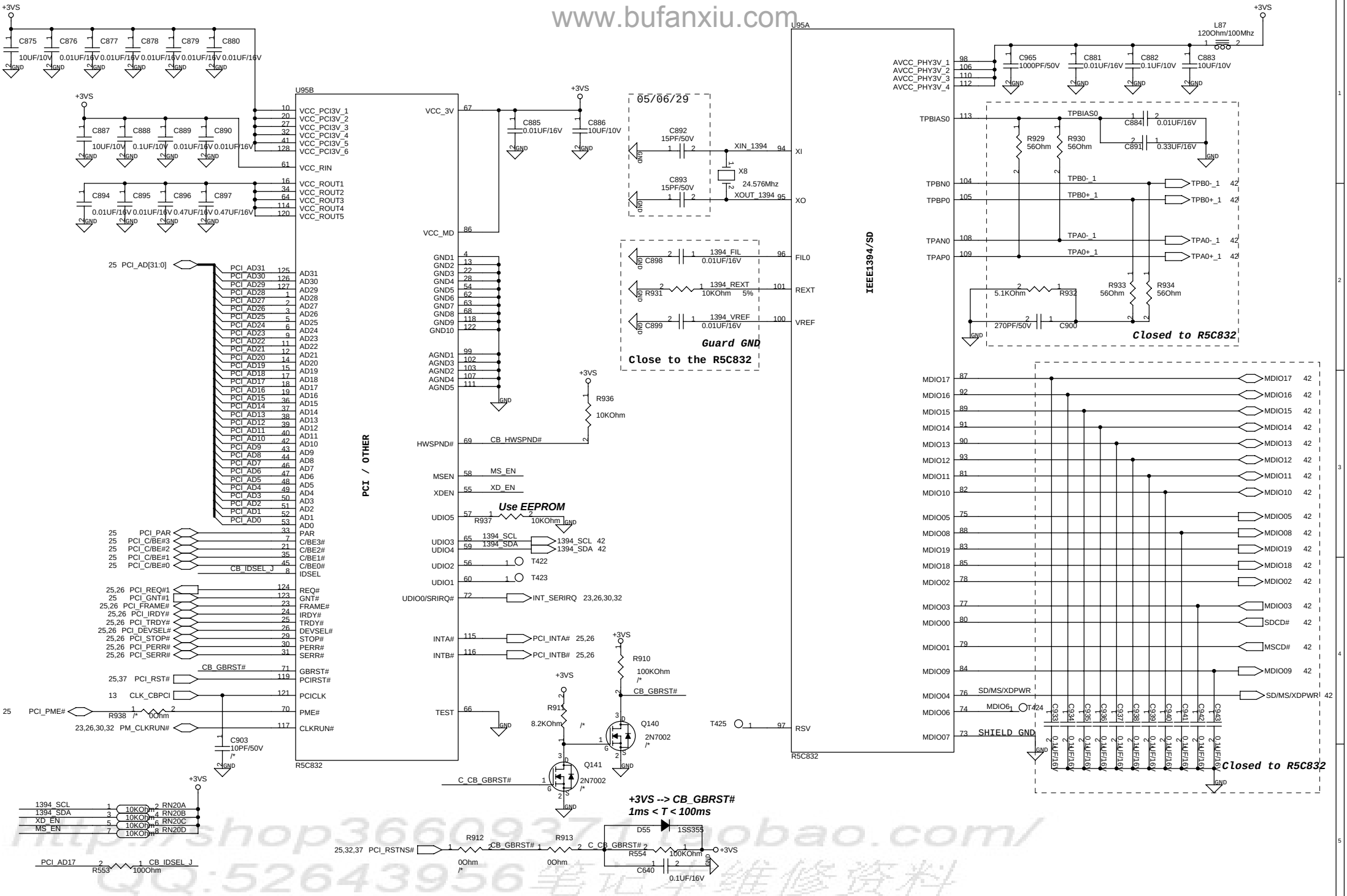
L_TXP	LTXP
L_TXN	LTXN
L_RXP	LRXP
L_RXN	LRXN



PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***RJ45/RJ11/MDC***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **38** OF **63**		RELEASE DATE :	

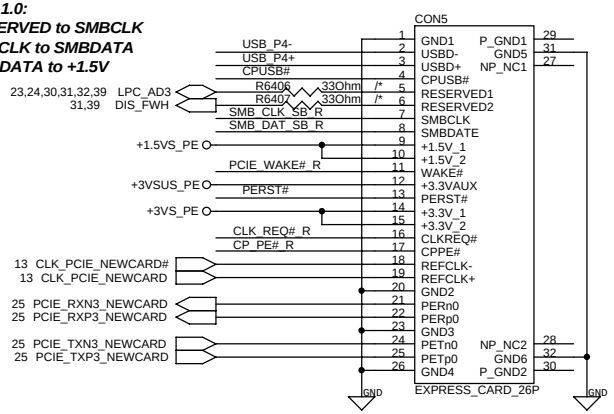


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***MINICARD***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **39** OF **63**		RELEASE DATE :	

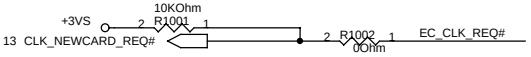


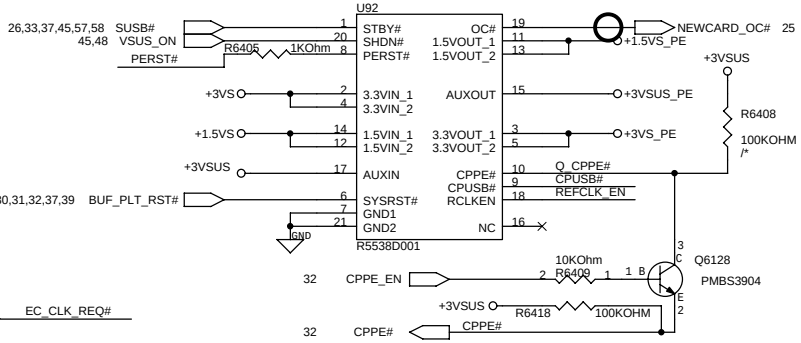
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***RICOH R5C832***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **40** OF **63**		RELEASE DATE :		

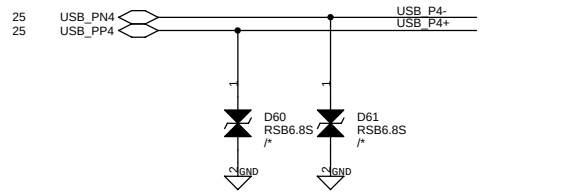
!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

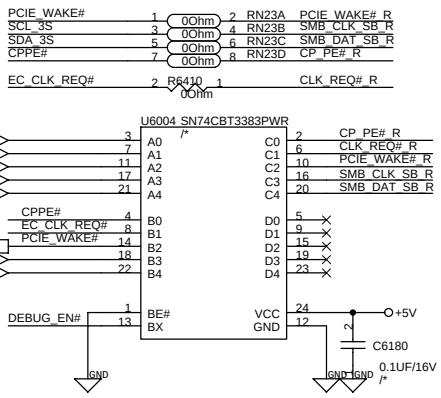


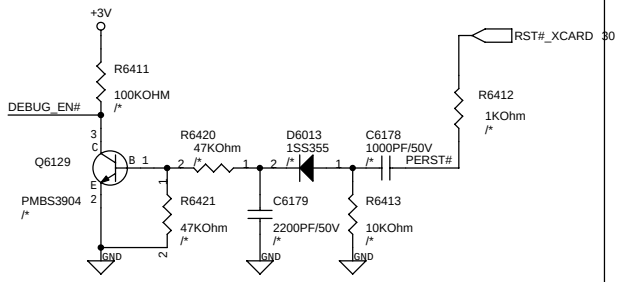
NEWCARD

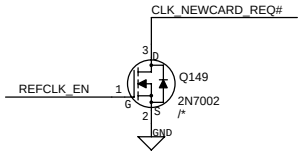


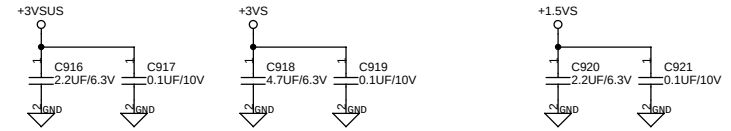


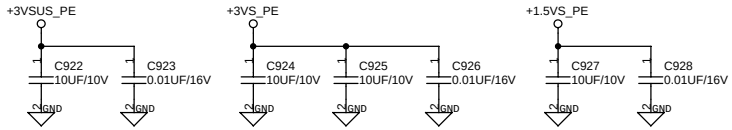






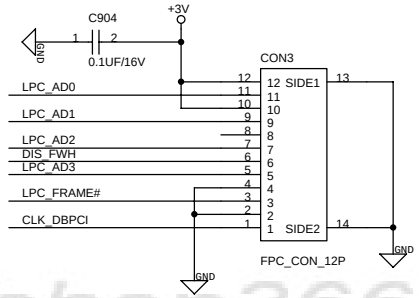






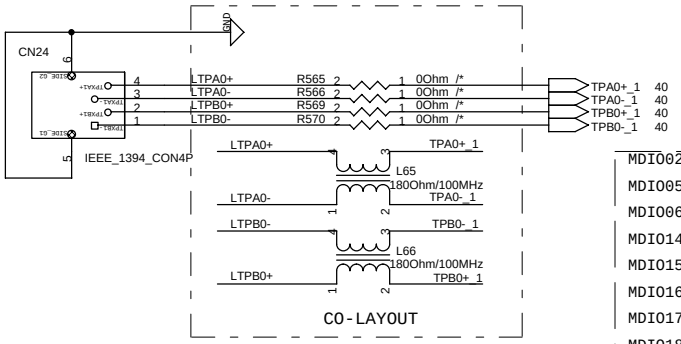
LPC Connector (Debug)

Note: Layout defined
Pin1--->Pin12



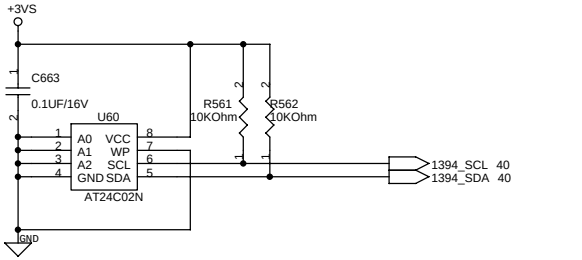
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **41** OF **63**	DESCRIPTION: ***NEWCARD***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**
					DESIGN ENGINEER : ***Feng Lin***

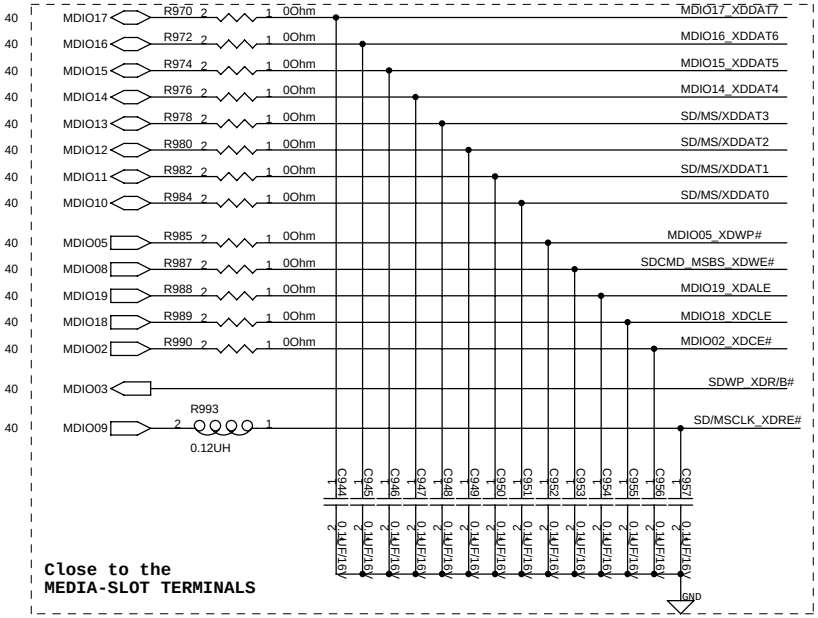
1394A

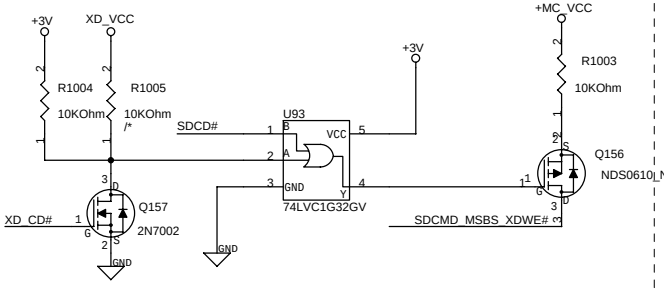


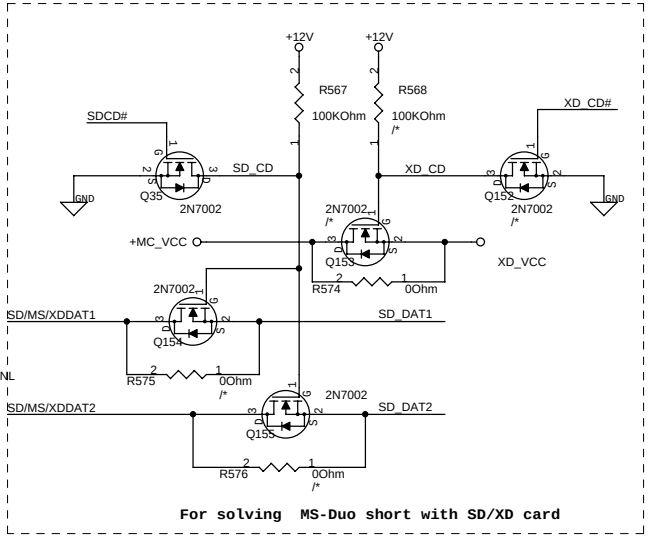
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

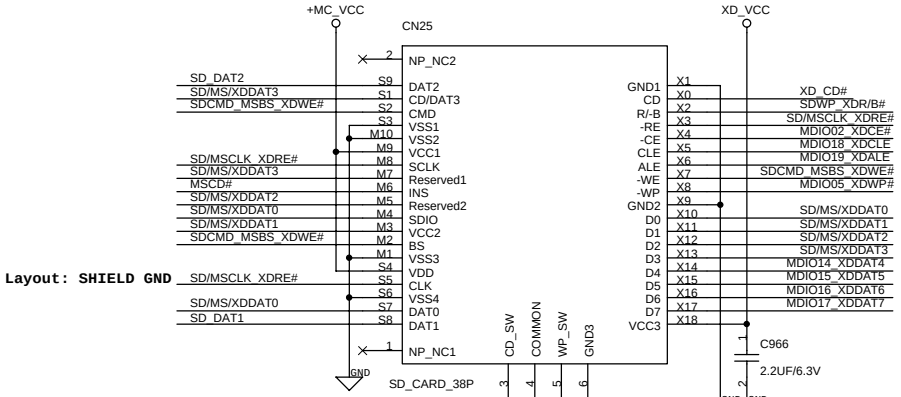
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

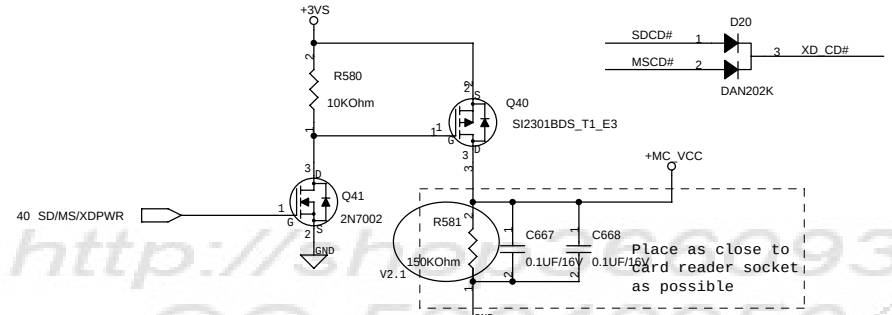


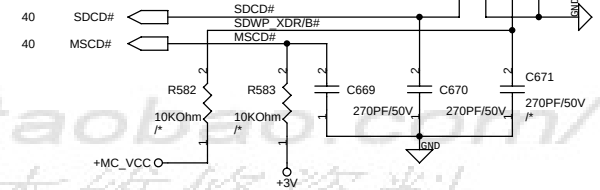




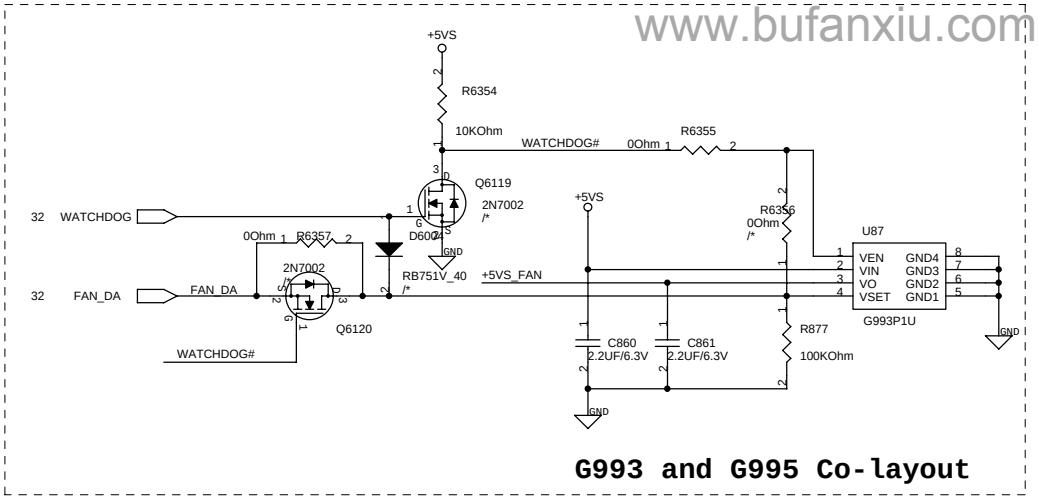






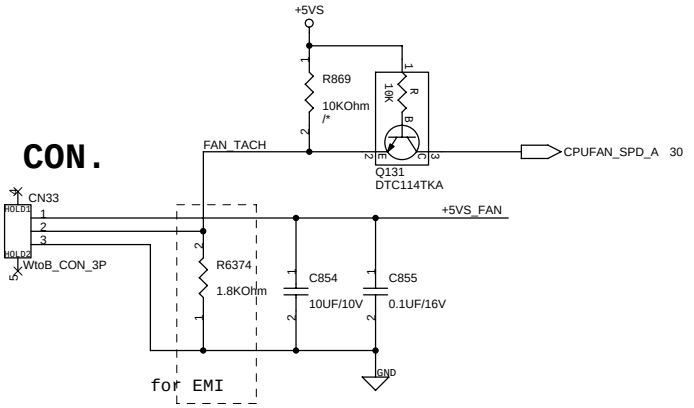


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***1394 & 4 IN 1***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **42** OF **63**		RELEASE DATE :	

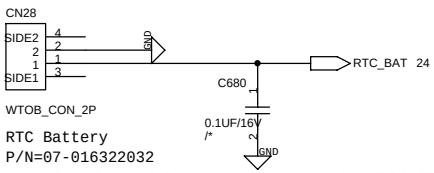


G993 and G995 Co-layout

FAN CON.

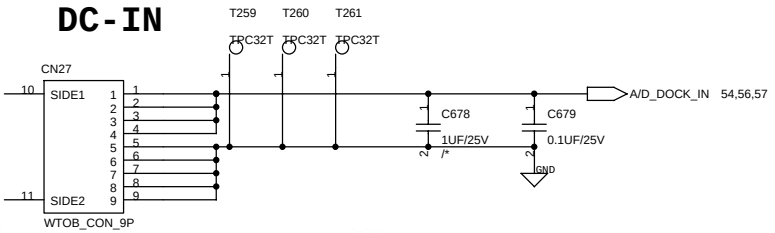


RTC BAT

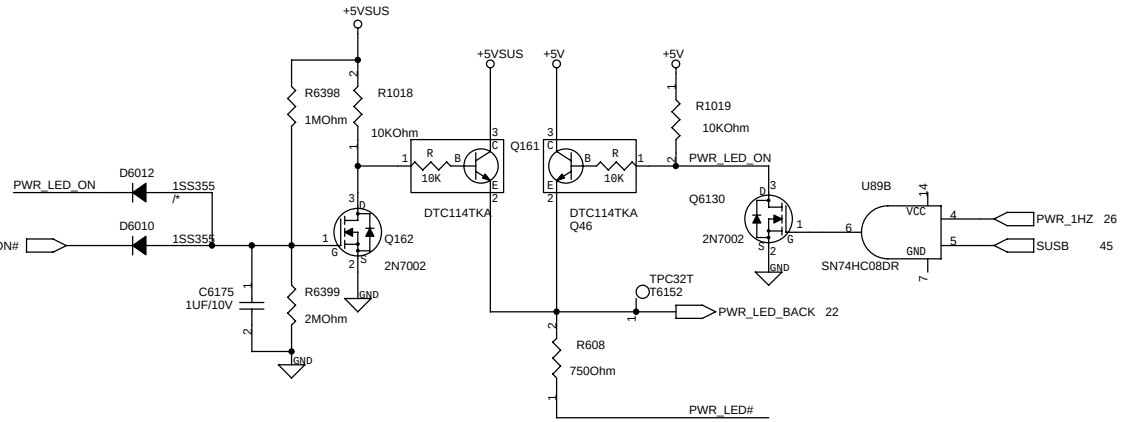


RTC Battery
P/N=07-016322032

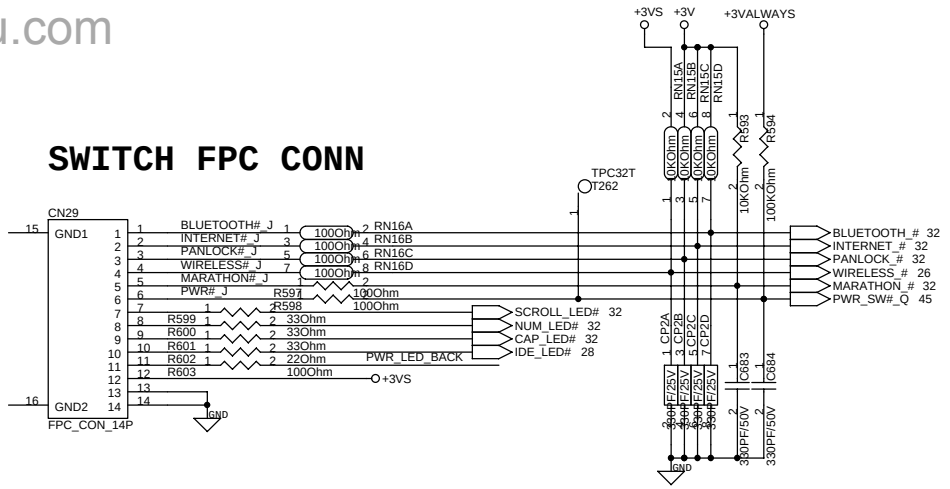
DC-IN

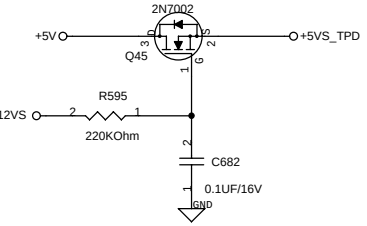


PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***FAN CONTROL & DC IN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **43** OF **63**		RELEASE DATE :		

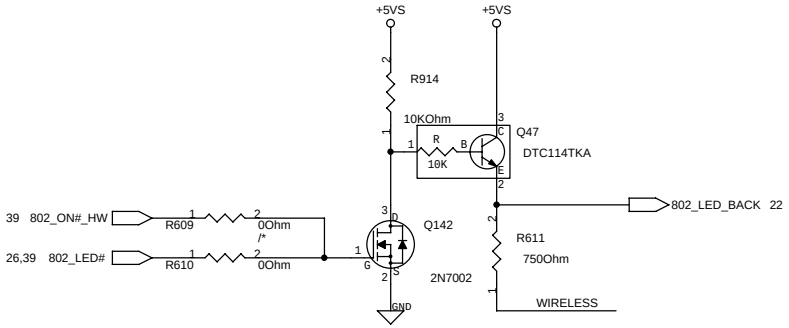


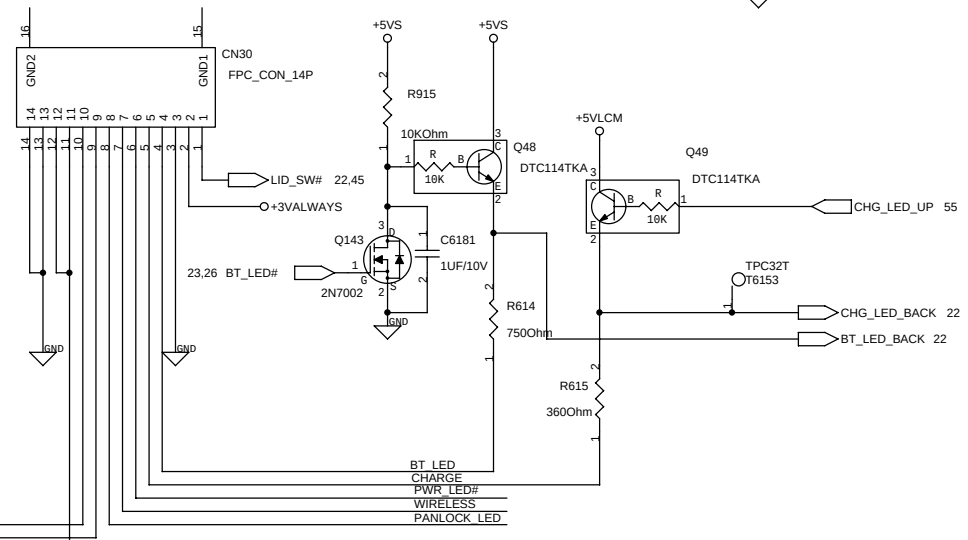
SWITCH FPC CONN

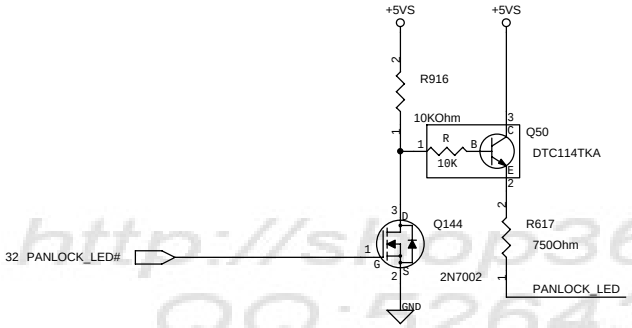


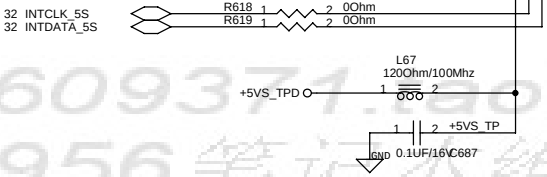


TOUCH PAD CNT

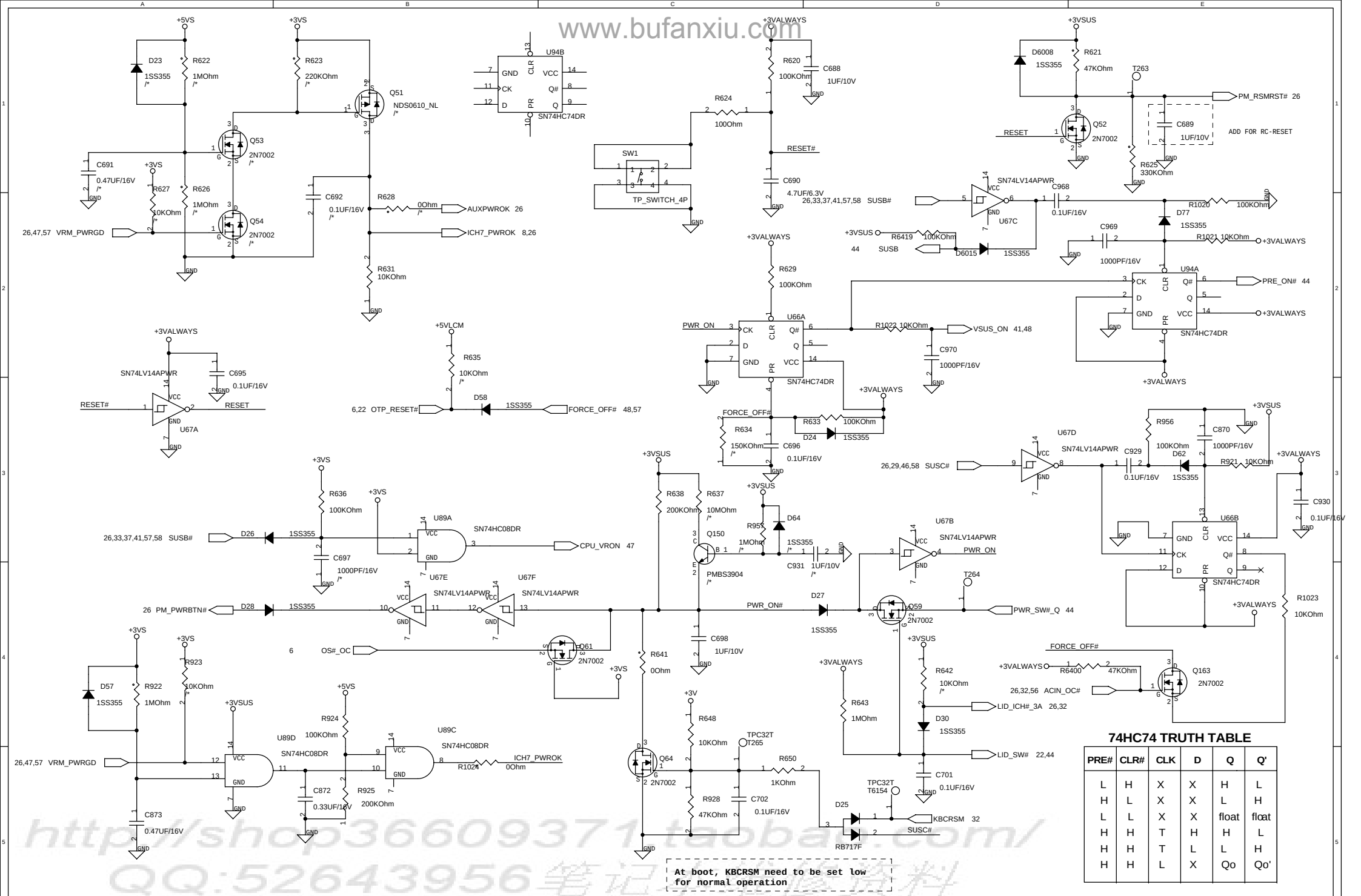








PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***INSTANT KEY & TP CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **44** OF **63**		RELEASE DATE :		

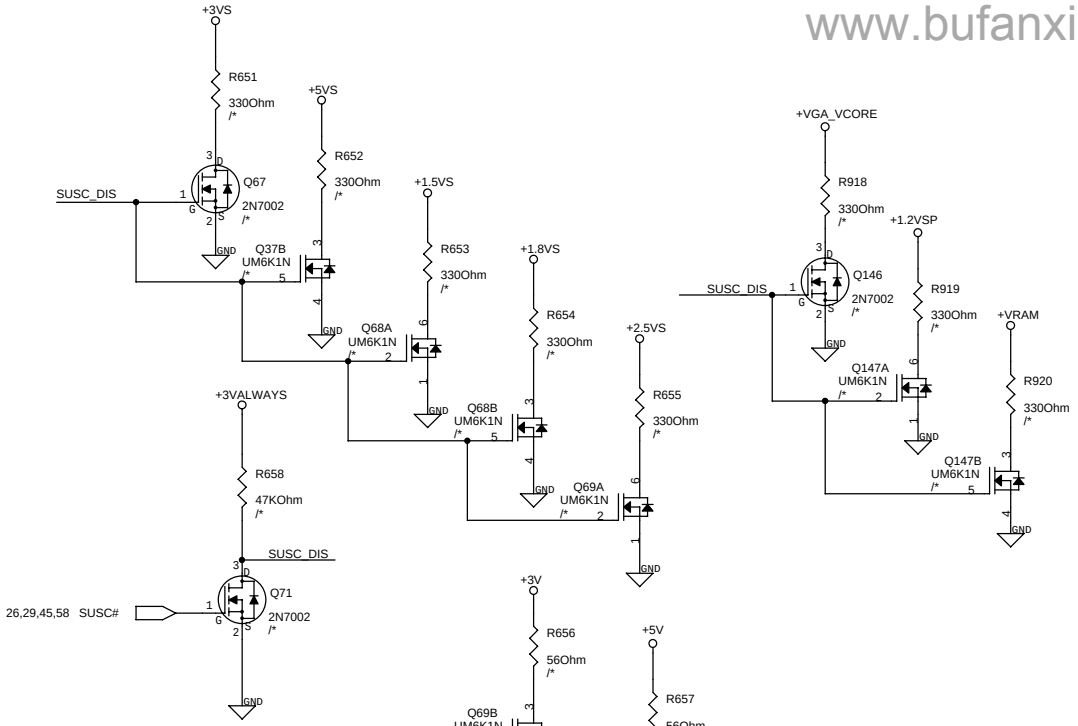


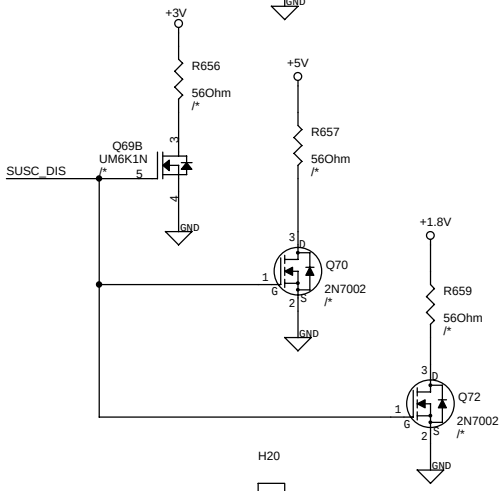
74HC74 TRUTH TABLE

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

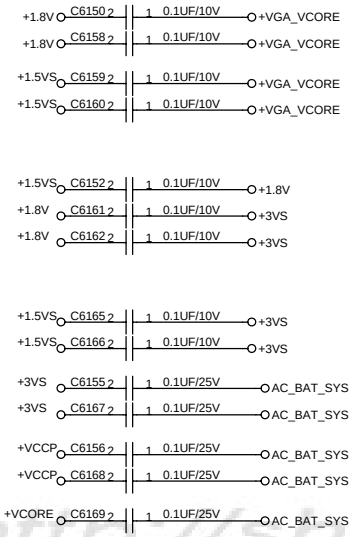
At boot, KBCRSM need to be set low for normal operation

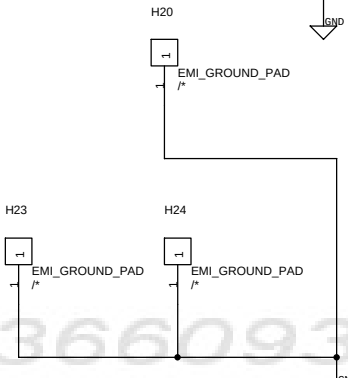
PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***POWER ON SEQUENCE***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Feng Lin***
		SHEET **45** OF **63**		RELEASE DATE :	

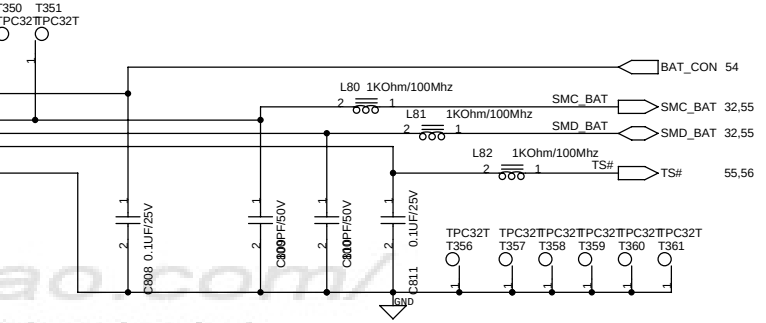




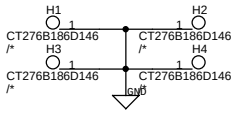
CROSS MOD



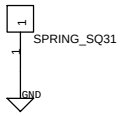




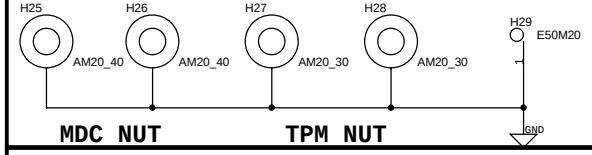
P.T.H for CPU Socket



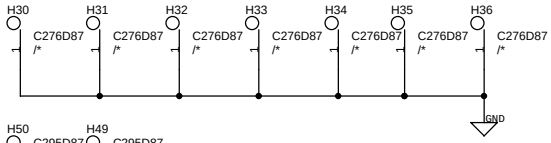
USB



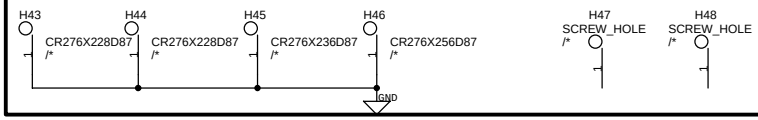
NUT on board

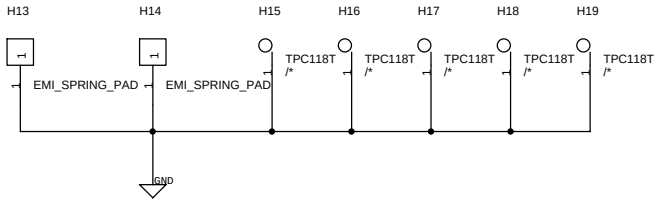


Screw Hole

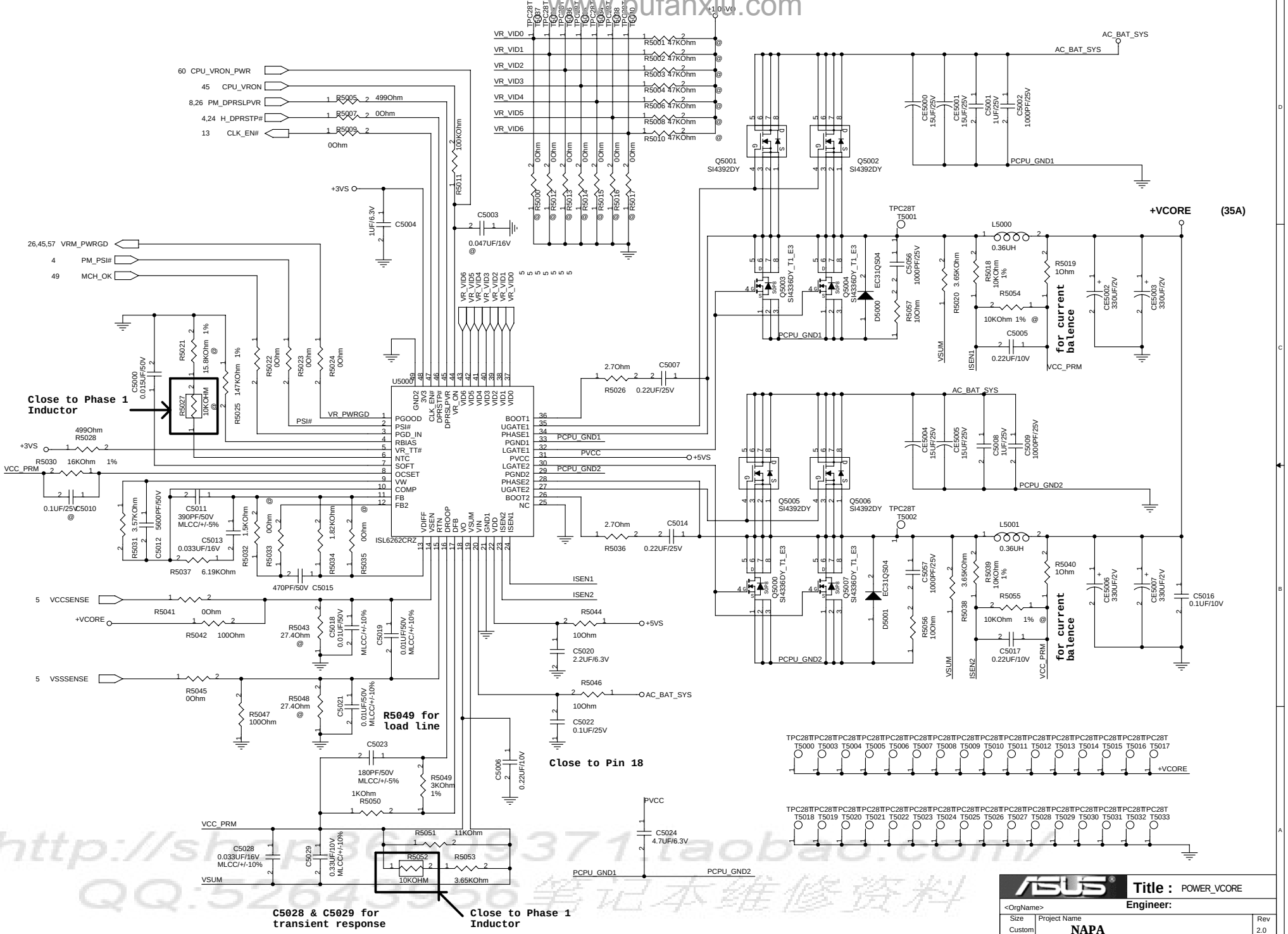


U-shaped screw hole





PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005**	DESCRIPTION: ***DISCHARGE & HOLE & BATCON***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Julian Kuo***
		SHEET **46** OF **63**		RELEASE DATE :	



ASUS	Title : POWER_VCORE	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
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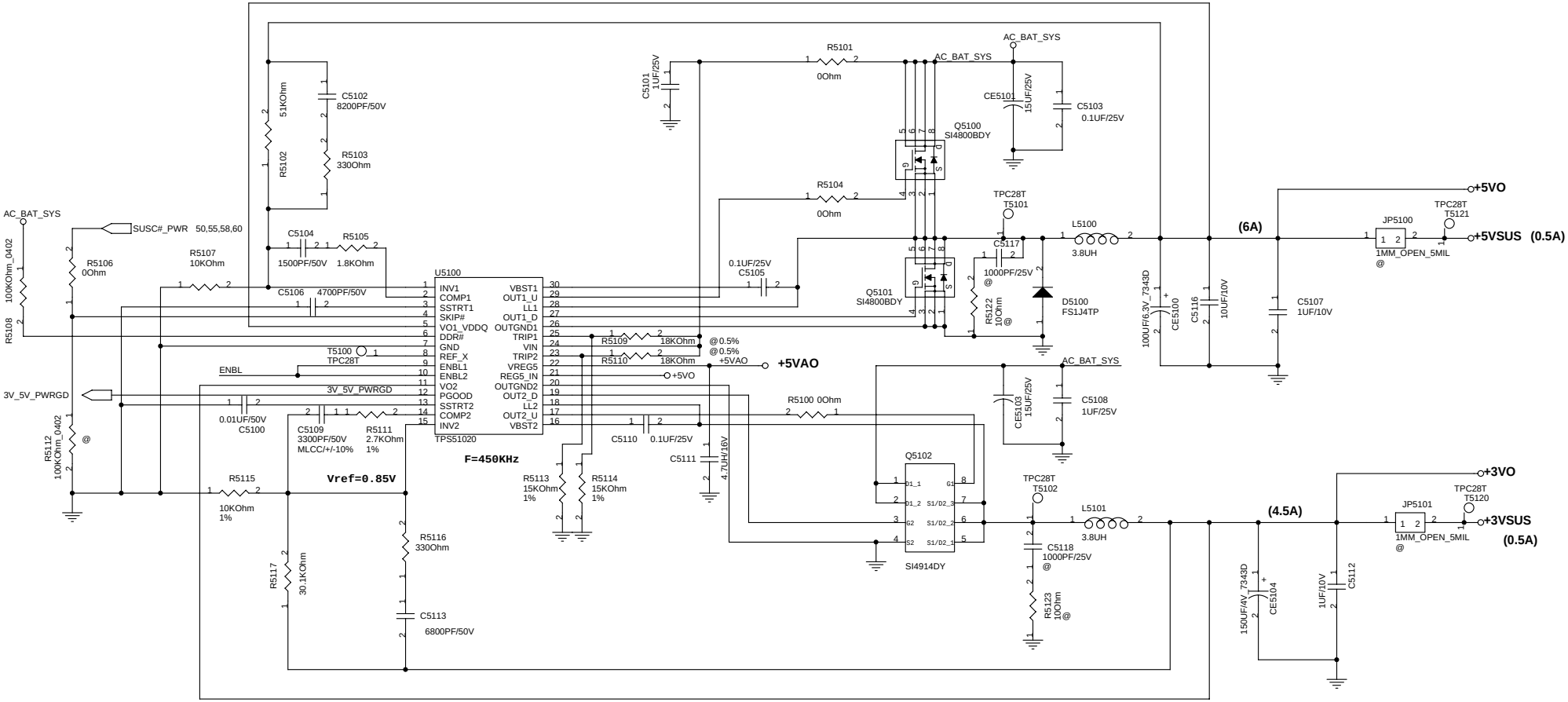

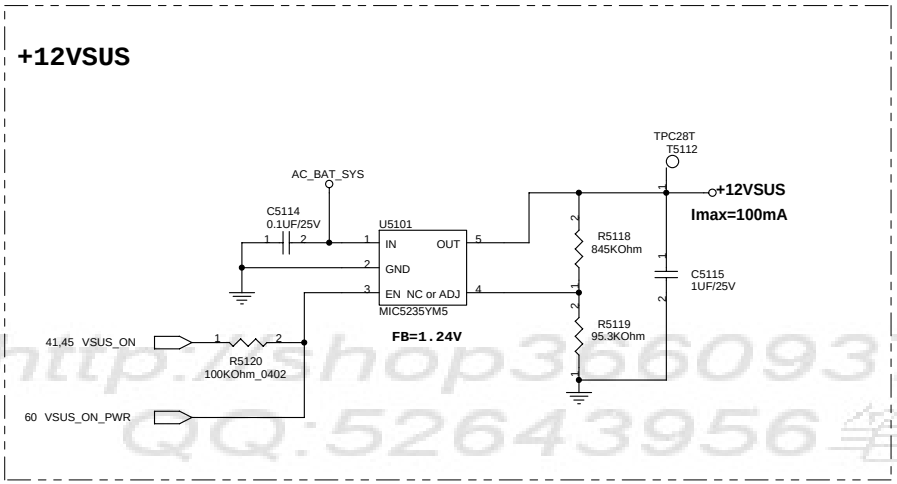

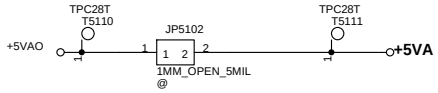

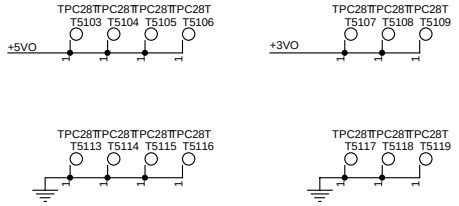

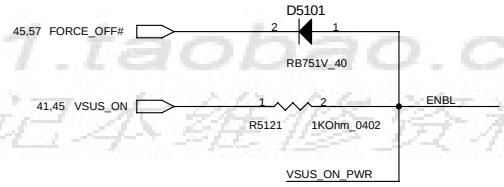

ASUS

Title : POWER_SYSTEM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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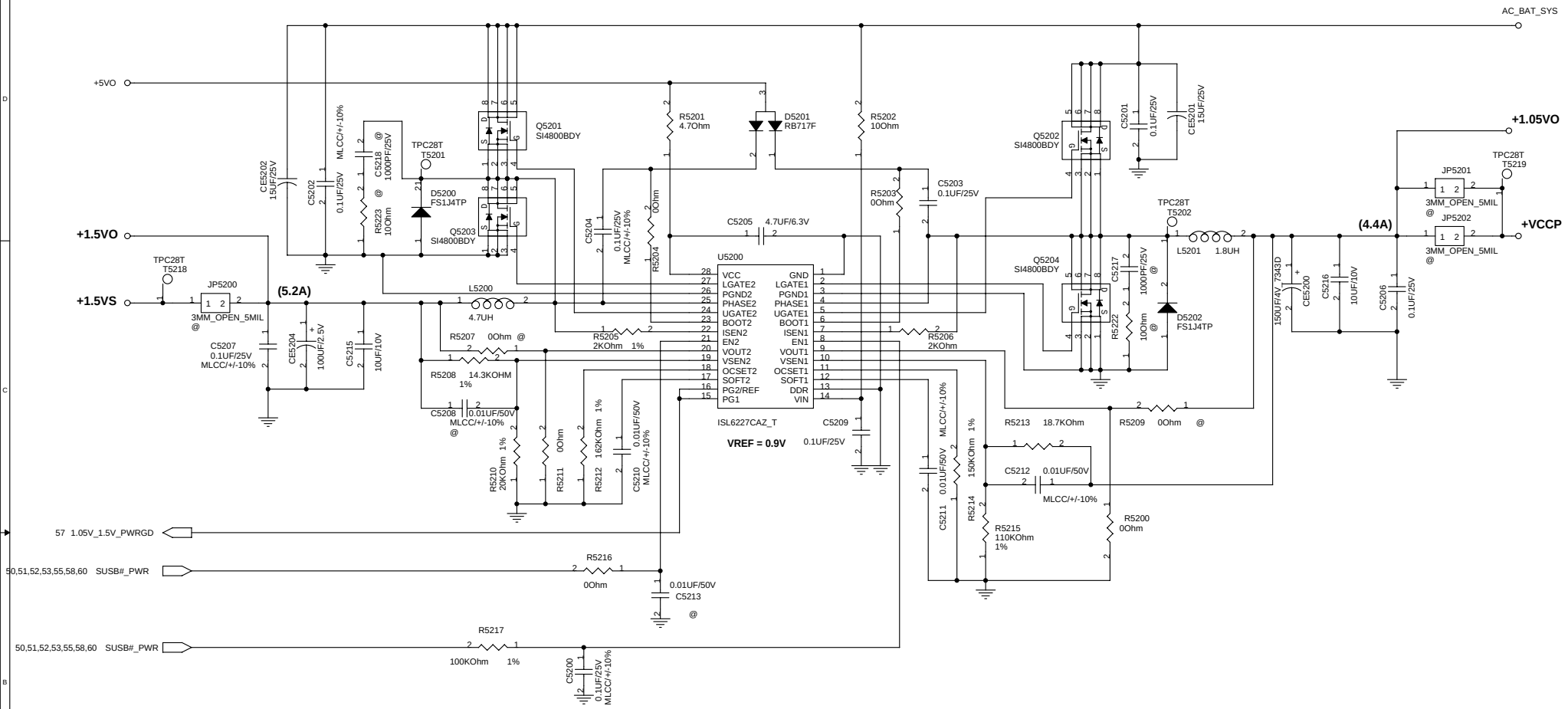
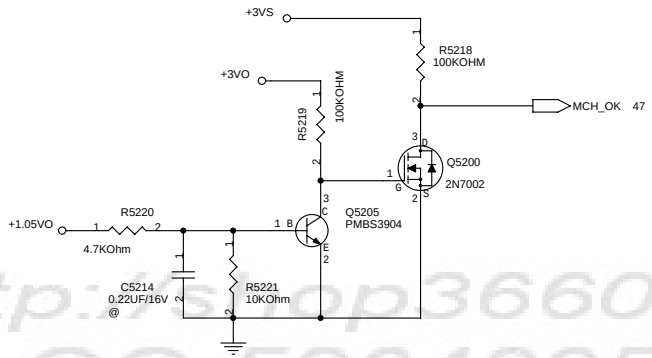
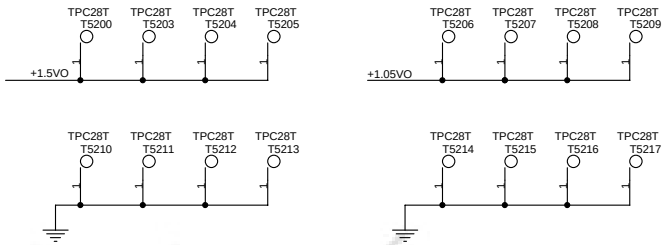
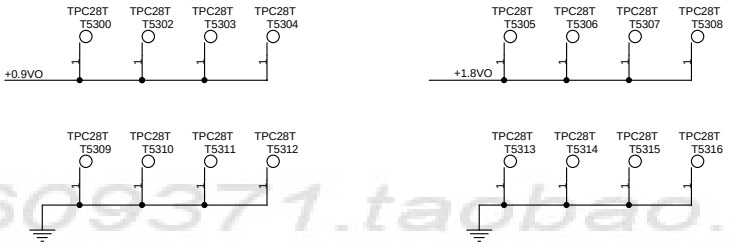




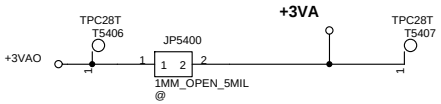


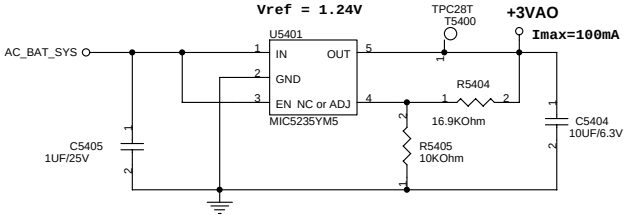
ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 49 of 63	



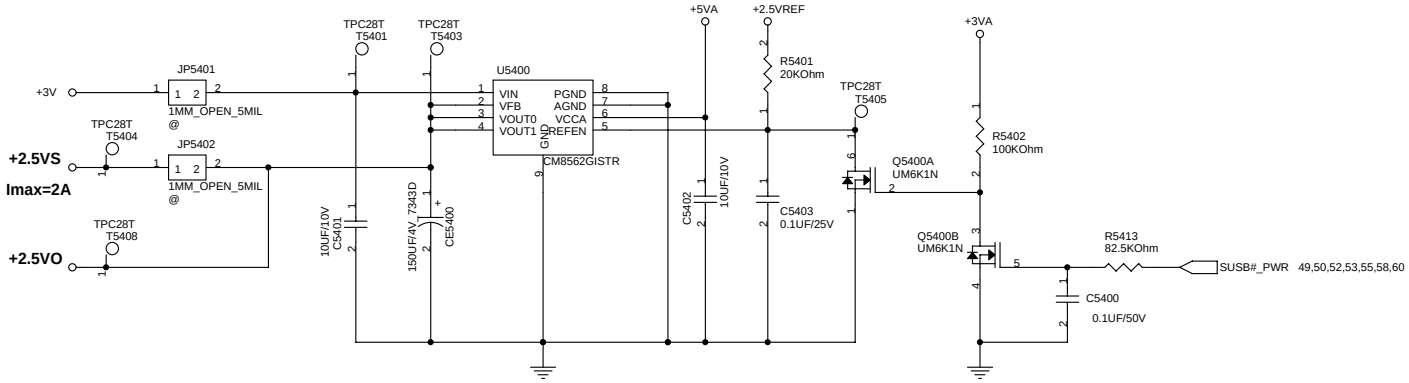
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 50 of 63	

+3VA0

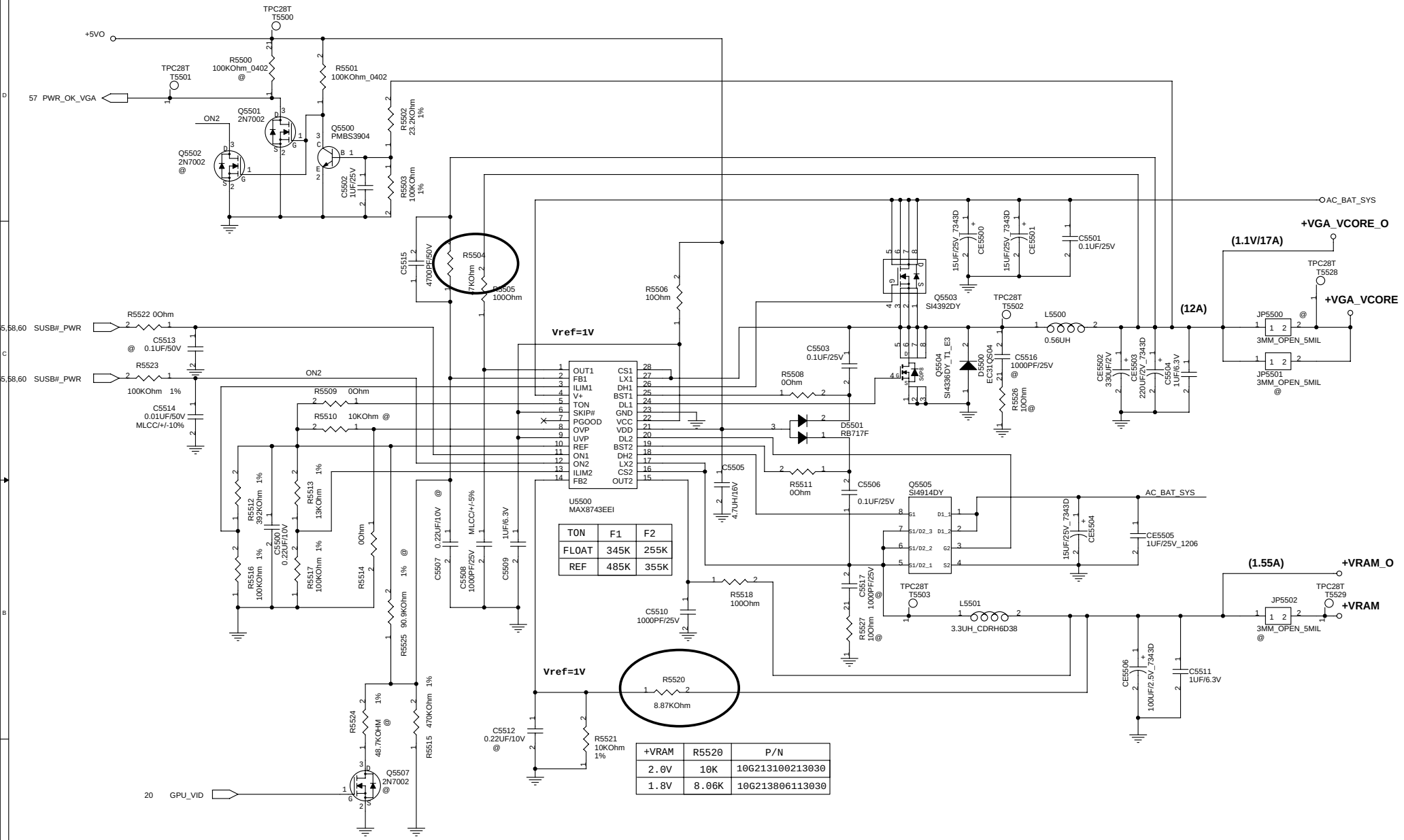




+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 51 of 63	



+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

TPC28T T5504 T5505 T5506 T5507 T5508 T5509 T5510 T5511 +VGA_VCORE_O

TPC28T T5520 T5521 T5522 T5523 T5524 T5525 T5526 T5527

TPC28T T5512 T5513 T5514 T5515 +VRAM_O

TPC28T T5516 T5517 T5518 T5519

ASUS

Title: POWER_VGA_CORE & RAM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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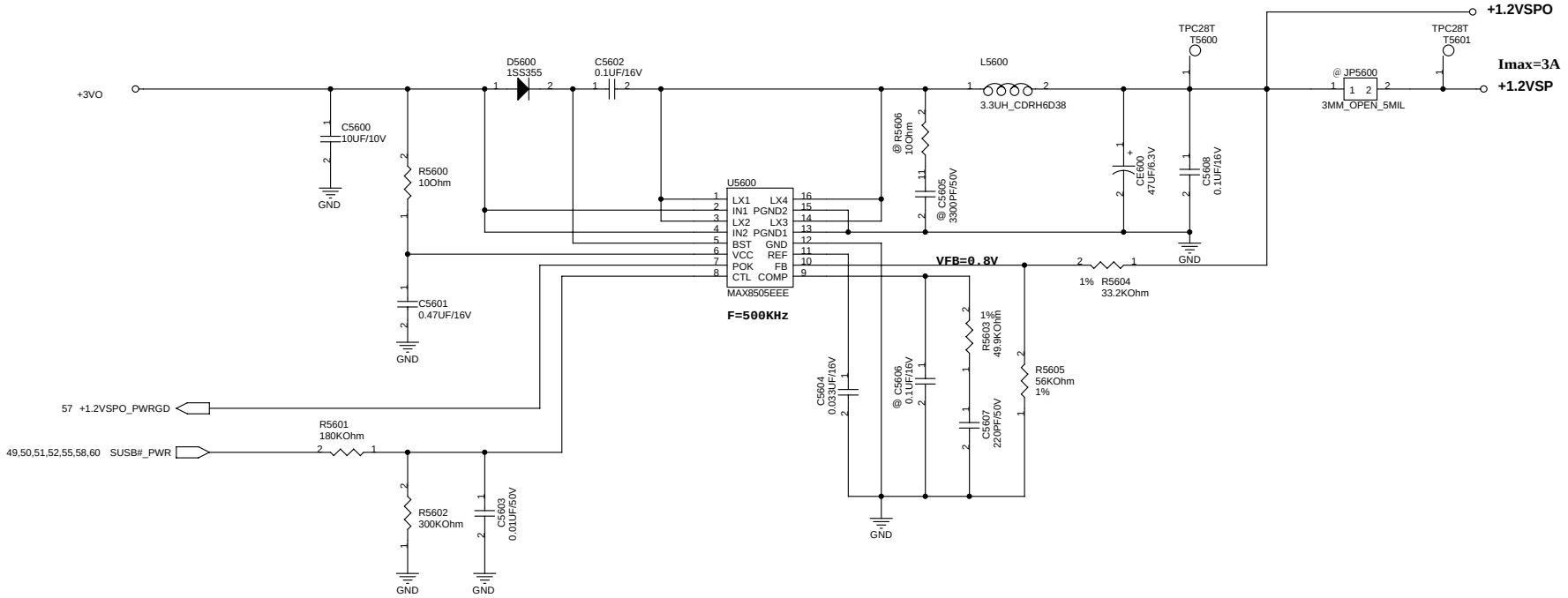
+1.2VSP



<Variant Name>

Title : POWER_VGA_+1.2VSP

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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TOTAL POWER=65W
-->3.42A

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A

Vref = 4.096V
VLDO = 5.4V

Vbatt = Cell * { 4V +[0.4 X (VCTL/REFIN)] }
VCTL= LDO
=> Vbatt = 4.2V X CELLS

VICTL= 1.728V

VREFIN = 3.54V

Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

PRE_CHARGE CIRCUIT

Pre-charge voltage 10V@3S
Pre-charge voltage 13.04V@4S

ASUS	Title : POWER_CHARGER	
<OrgName>	Engineer:	
Size: C	Project Name: NAPA	Rev: 2.0
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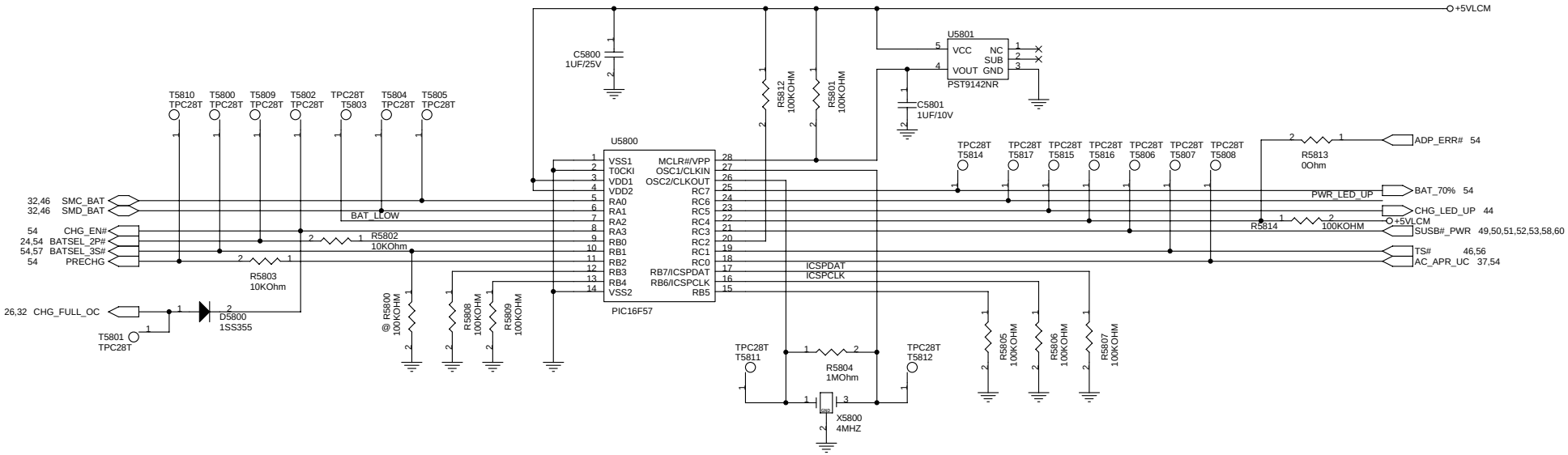
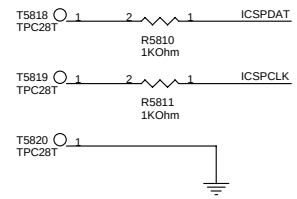
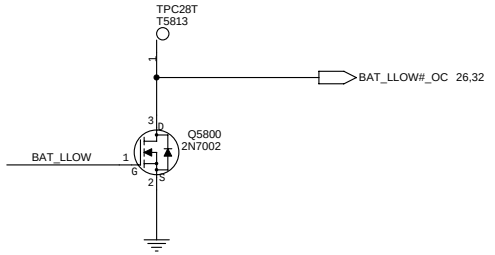
PIC16F57



For PIC reflash





ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
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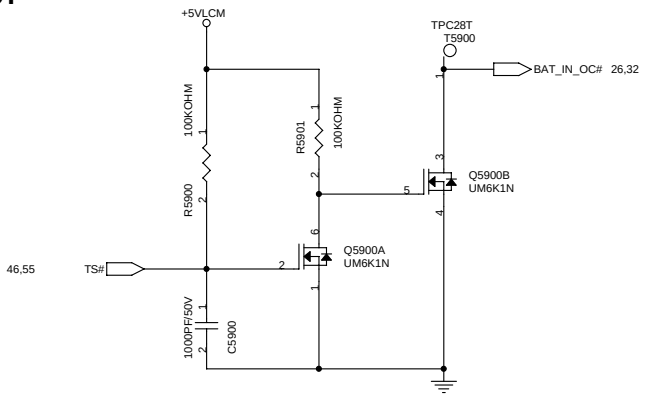
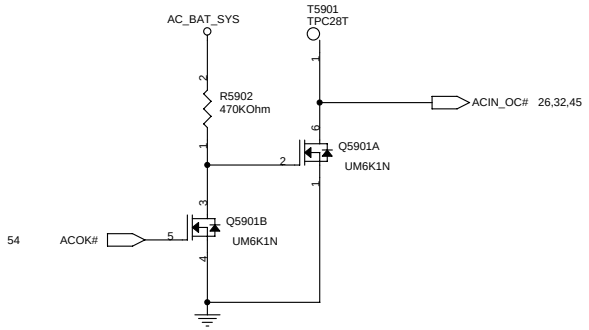
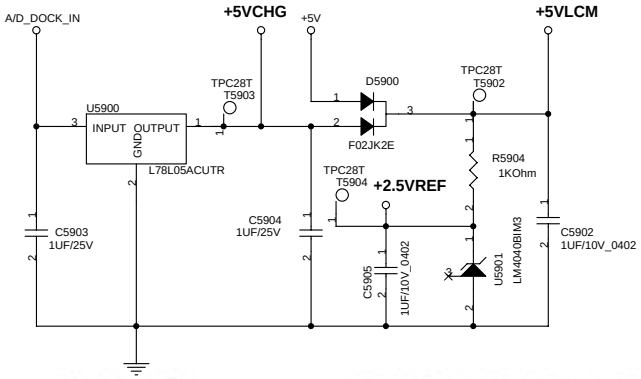
BATTERY IN DETECT



ADAPTER IN DETECT

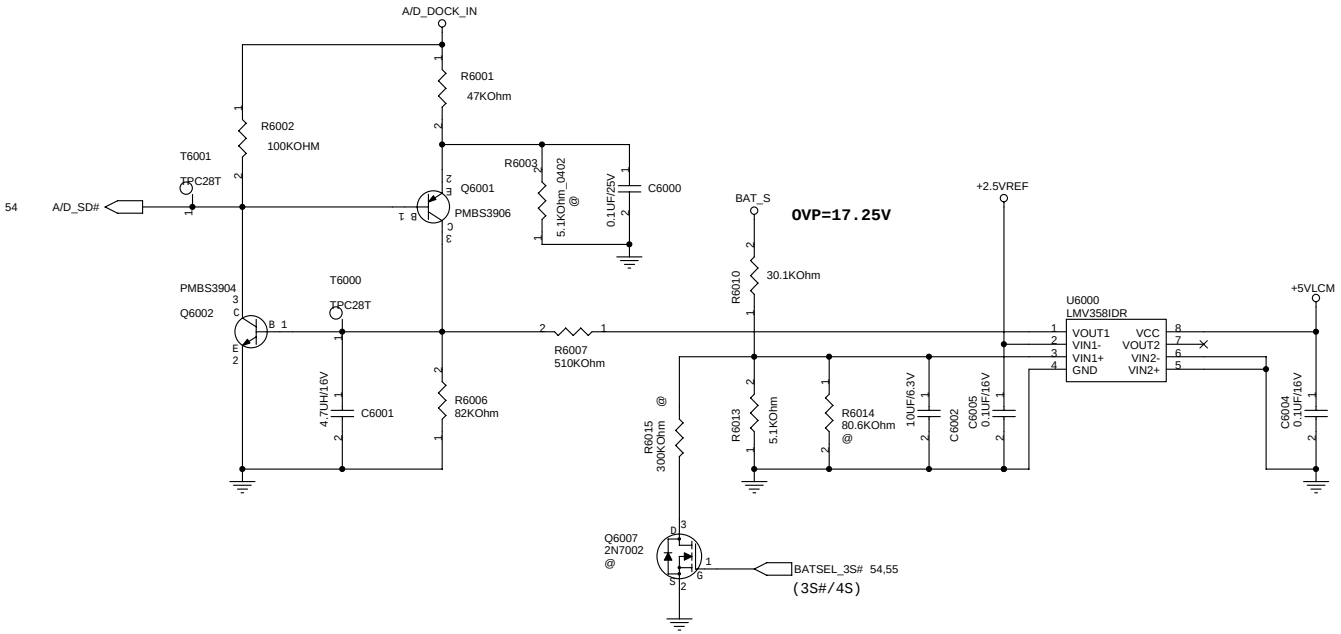


+5VLCM, +5VCHG & +2.5VREF

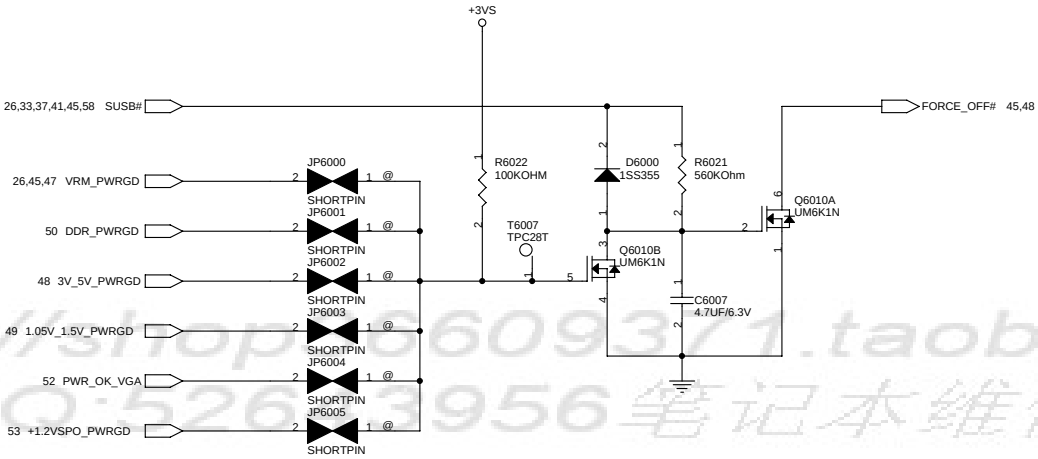


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 56 of 63	

BATTERY A/D_SD# (0VP)



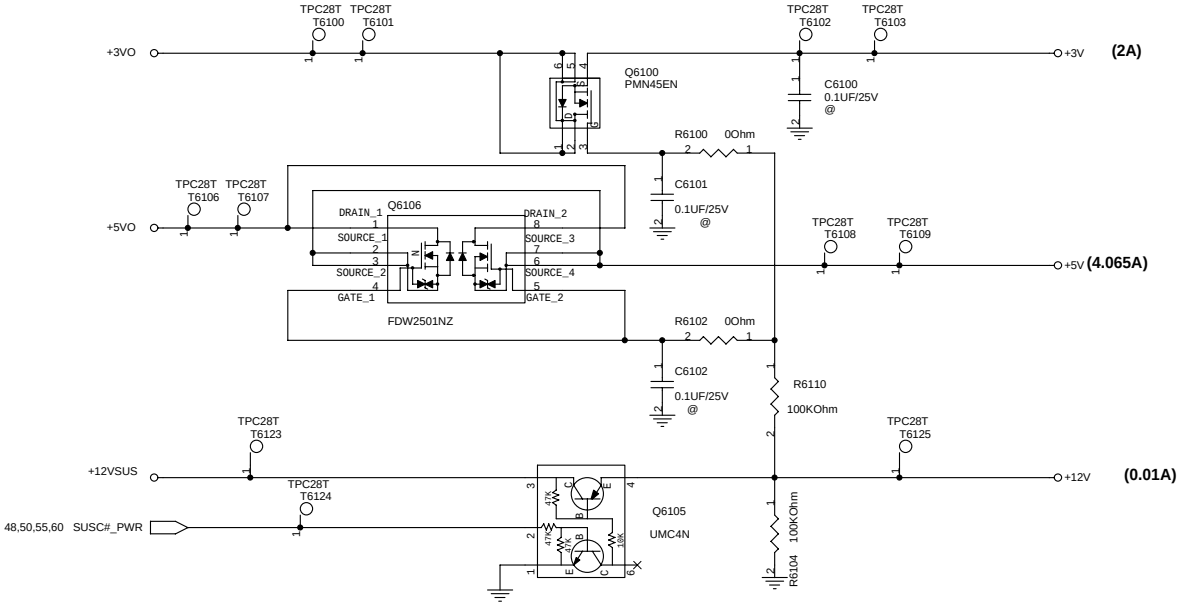
POWER GOOD DETECTER

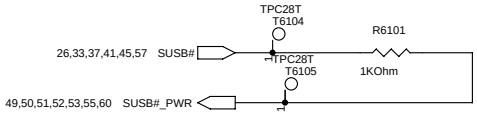


TPC28T T6003 — VRM_PWRGD
TPC28T T6004 — DDR_PWRGD
TPC28T T6005 — 3V_5V_PWRGD
TPC28T T6006 — 1.05V_1.5V_PWRGD

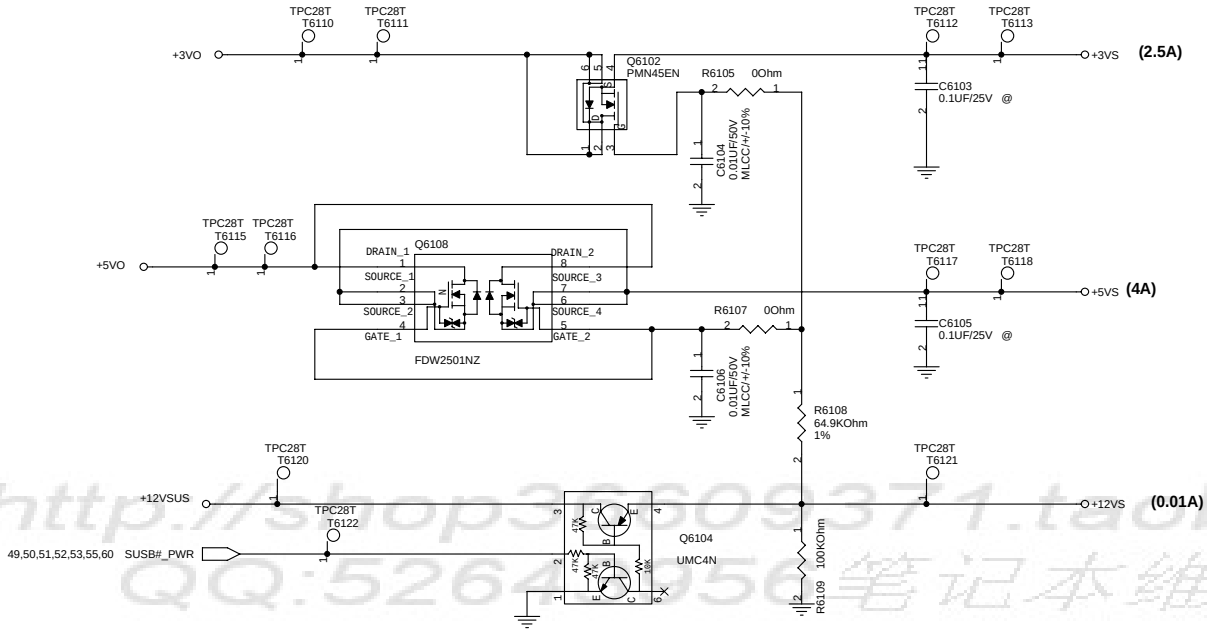
ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: Friday, November 25, 2005	Sheet 57 of 63	

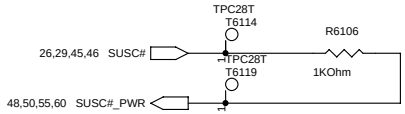
SUSC#_PWR POWER

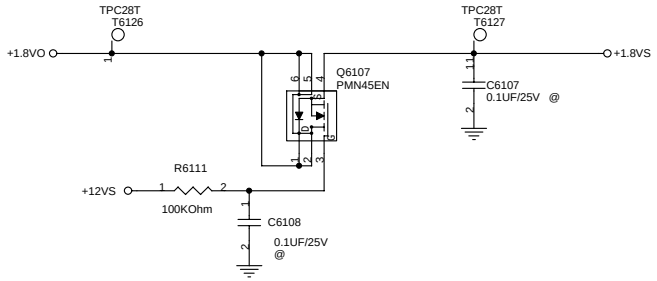




SUSB#_PWR POWER







ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
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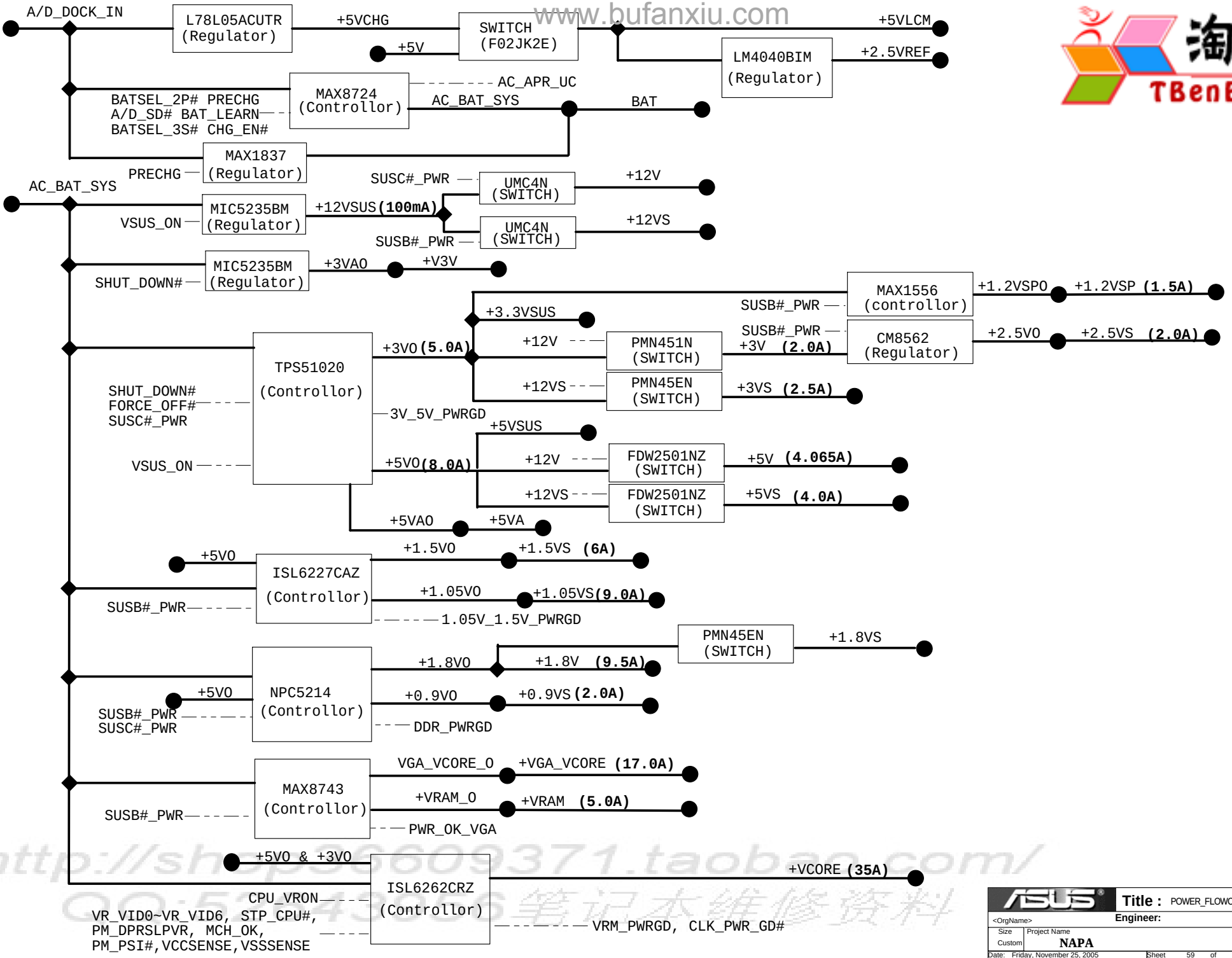

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
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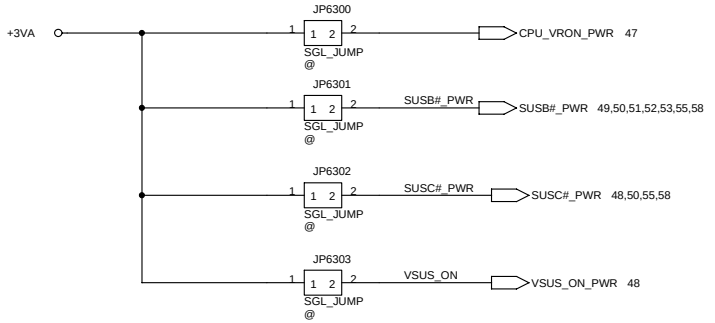
FOR POWER TEST

AC_BAT_SYS	AC_BAT_SYS	22,46,47,48,49,50,51,52,54,56
+3VA	+3VA	23,24,29,32,44,45,46,51
+5VA	+5VA	22,48,51,54
+5VO	+5VO	48,49,50,52,58
+3VO	+3VO	48,49,53,58
+3VSUS	+3VSUS	26,27,32,37,41,45,48
+5VSUS	+5VSUS	27,44,48
+3V	+3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+3VS	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,36,37,39,40,41,42,44,45,46,47,49,57,58
+12VSUS	+12VSUS	48,58
+12V	+12V	34,42,58
+12VS	+12VS	23,44,58
+5V	+5V	14,29,33,41,44,46,56,58
+5VS	+5VS	20,27,28,32,34,36,39,43,44,45,46,47,58
+2.5VO	+2.5VO	51
+2.5VS	+2.5VS	10,20,21,46,51
+1.8VO	+1.8VO	50,58
+1.8V	+1.8V	8,11,14,15,46,50
+1.8VS	+1.8VS	20,46,58
+0.9VS	+0.9VS	16,50
BAT	BAT	54
+5VCHG	+5VCHG	54,56
+5VLCM	+5VLCM	44,45,54,55,56,57
+2.5VREF	+2.5VREF	51,54,56,57
+VCORE	+VCORE	5,6,46,47
+VGA_VCORE	+VGA_VCORE	17,46,52
+VRAM	+VRAM	18,19,46,52
+1.2VSP	+1.2VSP	17,18,46,53
BAT_CON	BAT_CON	46,54



Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
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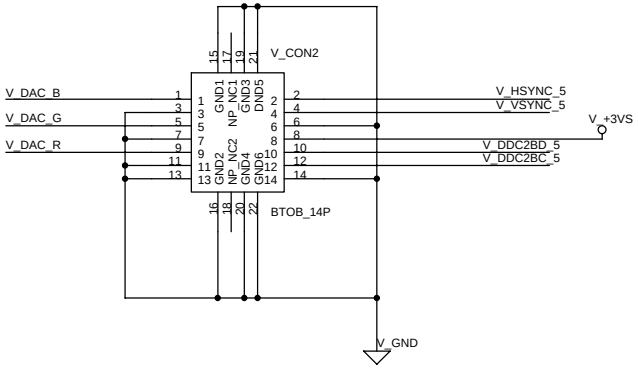
Revision History

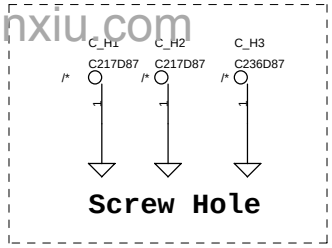
V1.0 to V1.1

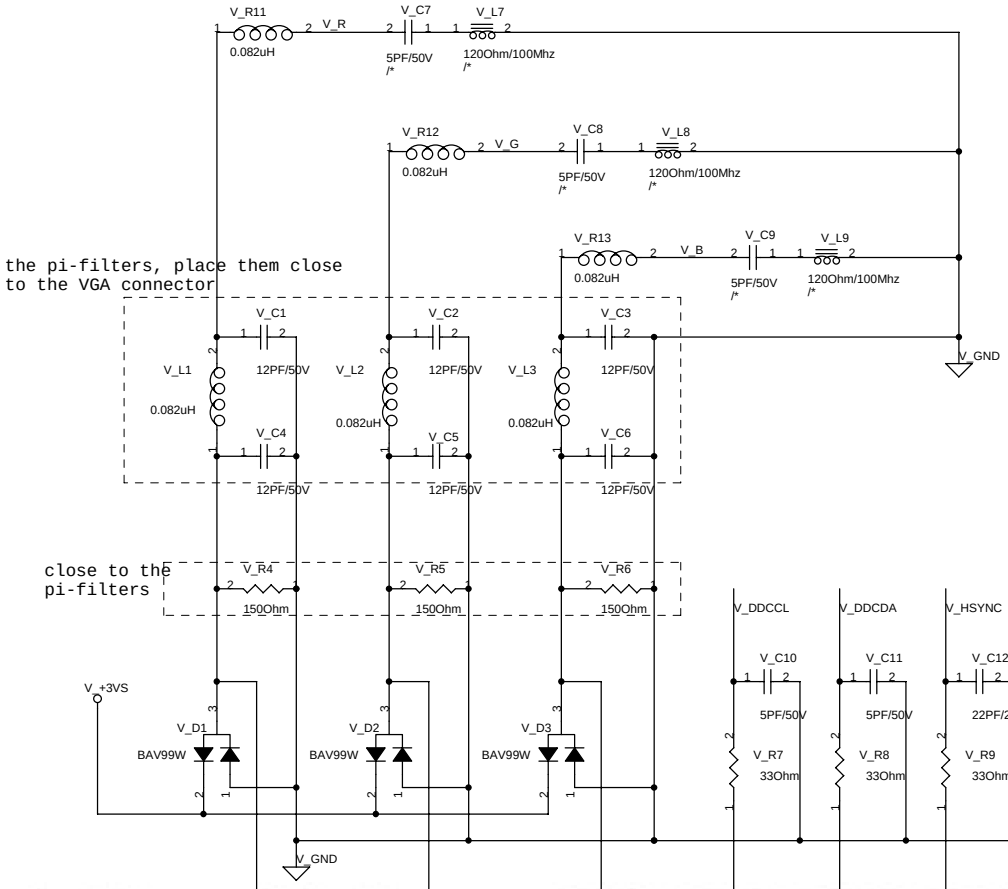
1. D58 change from DAP202 to 1ss355
2. Panel detection chagne from PID to EDID method.
3. Reserve panel dectection by PID method.
4. Tuning power sequence by power circuitry.
5. TP_MA_RCVEN* net can't connect with TP_MB_RCVEN*, so cut it.
6. CPU address A14 and A15 is swap for booting.
7. Populate R6347 = R6348 =120 Ohm by nVDIDA recommend.
8. Change VGA chip from G72M-V to G72M, so change device ID strapping.
9. CHG_FULL_OC net has doubled pull-up to +3vs and +3vsus, so remove +3vsus pull-up for leakage.
10. CLK_EN# pull-up to +3vs will has leakage current from cpu vcore controller. so remove it.
11. Lan chip reset signal has leakage current output to system reset signal, so add D6006 to solve it.
12. +1.5VS power trace is too small from source to calistoga IC, so increase trace width.
13. Remove R639 because system has no shutdown signal from POWER.
14. R638 change to 200k and C698 change to 1uF for power on button feeling.
15. CFG18, 16, 15 has wrong connection, correct it.
16. C138=C139=22pF for tunning 14.318MHz crystal freauency.
17. RN15 pin 2 pull-up power change from +3V to +3VS for solving leakage current at S3 state.
18. Change audio circuitry for solving pop noise.
19. Change pci-express decoupling caps from 0.1uF/Y5V to 0.1uF/X5R.
20. Microphone pull-up power source change to OP AMP generate.
21. R287=0 Ohm and R290 remove for G72M need +3VS level input about 27MHz spread spectrum input pin.
22. MAX6649 be used on G72M has wrong connection, so correct it.
23. Populate R574=0 Ohm for XD card work fine.
24. Remove R6360, R6361, R6358, R6359 for JTAG pin pull-up/down on G72M.
25. Populate C563, C566 for improve microphone quality.
26. Add D6008 for PM_RSMRST# discharge quickly.
27. Tunning C141~C146, R128, C490 value base on EVT report about clk signal quality issue.
28. Add ODD disable function support.

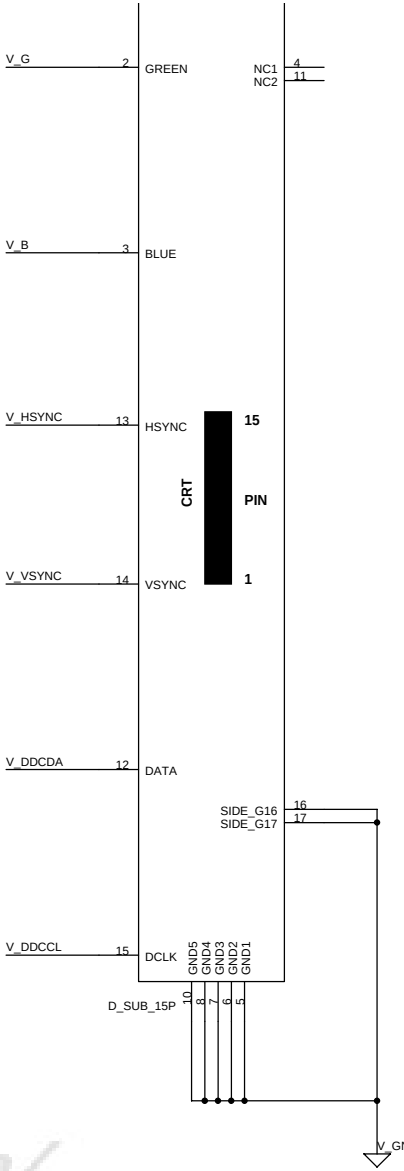
V1.1 to V2.0

1. Calistoga CRT disable guide change, so IREF pin connect to power directly.
2. Add circuitry for newcard disable support.
3. R381 change to 1K Ohm for ODD disable support.
4. Reserve newcard type debug card support circuitry.
5. Add mini card type debug card support circuitry.
6. MAX6649 be used on G72M change to MAX6657.
7. Add TPM connector debug card support.
8. The reset signal of lan chip pull-down 10K Ohm.
9. RTCRST# delay time control add diode for quick discharge.
10. Populate R6351, C? for solving led will flash once when system power on.
11. Add usb spring and beas on agnd and dgnd for EMI request.
12. Disable audio jack sense feature.
13. Add Q6130 for 1HZ flash









ASUS

Title : CRT OUT

<OrgName>

Engineer: Feng Lin

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Custom	V6J	2.0

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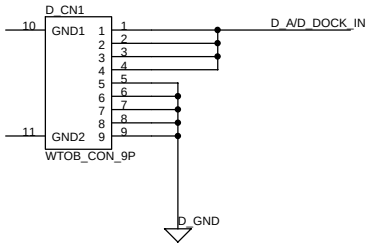

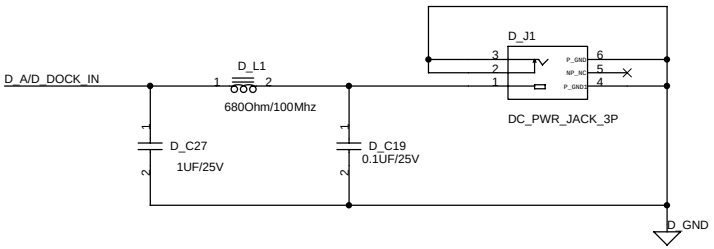

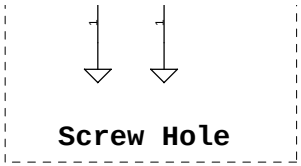

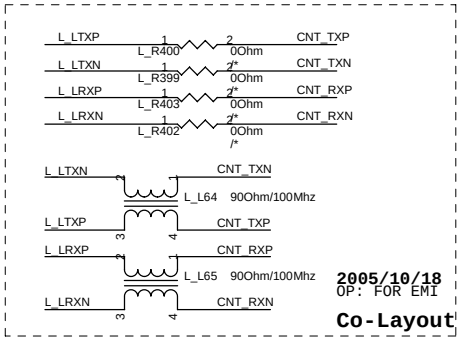

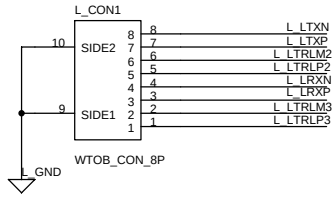

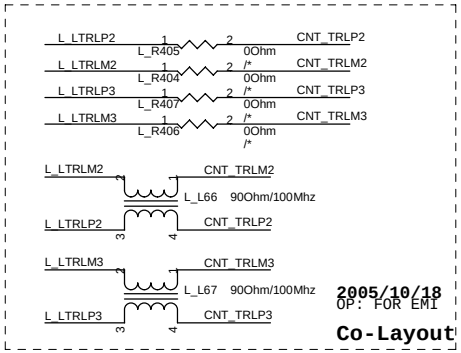

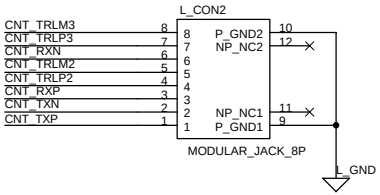

PROJECT: **V6J**	REVISION **2.0**	DATE: **Friday, November 25, 2005** SHEET **63** OF **63**	DESCRIPTION: ***DC IN***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER : ***Feng Lin***