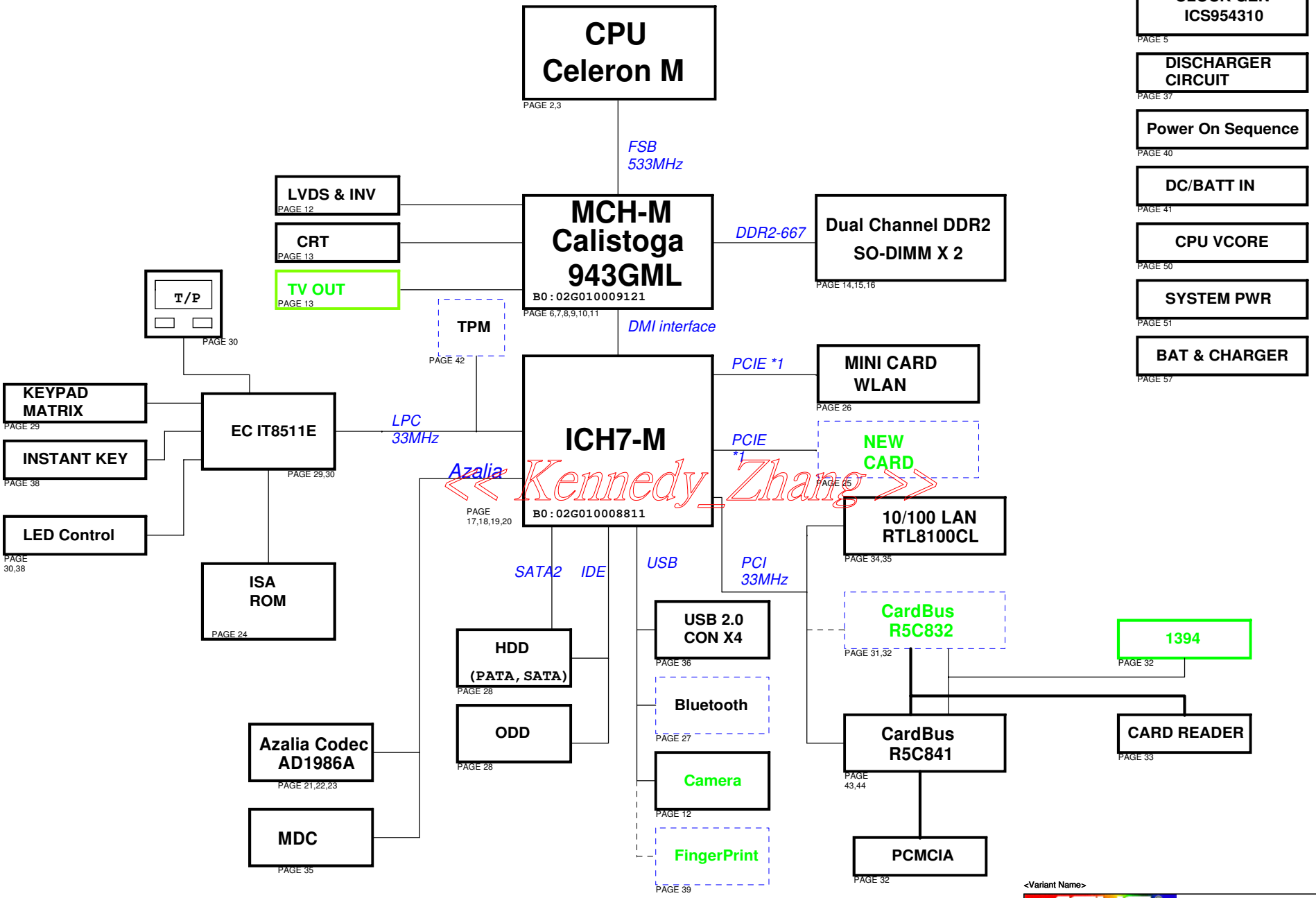
DC/BATT IN

T12F Block Diagram



<Variant Name>

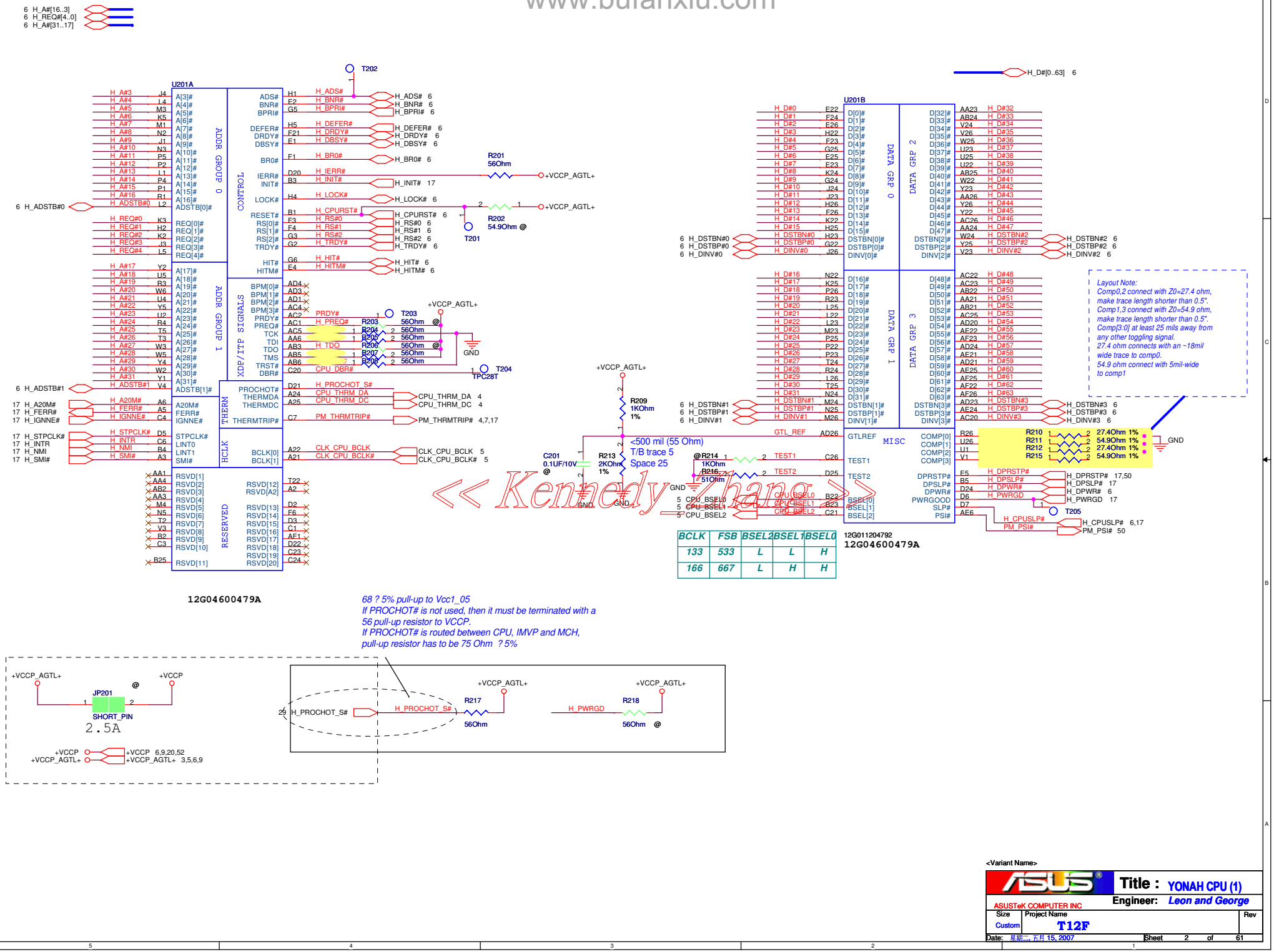
Title : BLOCK DIAGRAM

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12H	2.2

Date: 星期五, 五月 25, 2007 Sheet 1 of 61



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

12G04600479A

68 ? 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ? 5%

<Variant Name>

Title : YONAH CPU (1)		
ASUSTeK COMPUTER INC	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 2 of 61	

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP_AGTL+ → +VCCP_AGTL+ 2,5,6,9

+VCORE → +VCORE 50

+1.5VS → +1.5VS 9,10,20,25,26,37,52

+VCORE

U201C

VCC[1] VCC[2] VCC[3] VCC[4] VCC[5] VCC[6] VCC[7] VCC[8] VCC[9] VCC[10] VCC[11] VCC[12] VCC[13] VCC[14] VCC[15] VCC[16] VCC[17] VCC[18] VCC[19] VCC[20] VCC[21] VCC[22] VCC[23] VCC[24] VCC[25] VCC[26] VCC[27] VCC[28] VCC[29] VCC[30] VCC[31] VCC[32] VCC[33] VCC[34] VCC[35] VCC[36] VCC[37] VCC[38] VCC[39] VCC[40] VCC[41] VCC[42] VCC[43] VCC[44] VCC[45] VCC[46] VCC[47] VCC[48] VCC[49] VCC[50] VCC[51] VCC[52] VCC[53] VCC[54] VCC[55] VCC[56] VCC[57] VCC[58] VCC[59] VCC[60] VCC[61] VCC[62] VCC[63] VCC[64] VCC[65] VCC[66] VCC[67]

VCC[68] VCC[69] VCC[70] VCC[71] VCC[72] VCC[73] VCC[74] VCC[75] VCC[76] VCC[77] VCC[78] VCC[79] VCC[80] VCC[81] VCC[82] VCC[83] VCC[84] VCC[85] VCC[86] VCC[87] VCC[88] VCC[89] VCC[90] VCC[91] VCC[92] VCC[93] VCC[94] VCC[95] VCC[96] VCC[97] VCC[98] VCC[99] VCC[100]

VCCP[1] VCCP[2] VCCP[3] VCCP[4] VCCP[5] VCCP[6] VCCP[7] VCCP[8] VCCP[9] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]

VCCA

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]

VCCSENSE VSSSENSE

AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AE10 AE12 AE14 AE15 AE17 AE18 AF20

V6 G21 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21

B26

AF7 AE7

12G04600479A

+VCCA → JP301 (1 2) → +1.5VO

1MM_OPEN_5MIL

@

+VCCP_AGTL+ → RN303D (7 — 0Ohm — 8)

+VCCA

120mA / 20mil

Close to Pin B26

C301 10UF/10V

C318 0.01UF/25V

GND

checklist suggests 10uF POSCAP

AD6	H_VID0	1	0Ohm	2	RN302A	VR_VID0 50
AF5	H_VID1	3	0Ohm	4	RN302B	VR_VID1 50
AE5	H_VID2	5	0Ohm	6	RN302C	VR_VID2 50
AF4	H_VID3	7	0Ohm	8	RN302D	VR_VID3 50
AE3	H_VID4	1	0Ohm	2	RN303A	VR_VID4 50
AF2	H_VID5	3	0Ohm	4	RN303B	VR_VID5 50
AE2	H_VID6	5	0Ohm	6	RN303C	VR_VID6 50

R301 100Ohm

R302 100Ohm

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

U201D

VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71] VSS[72] VSS[73] VSS[74] VSS[75] VSS[76] VSS[77] VSS[78] VSS[79] VSS[80] VSS[81]

VSS[82] VSS[83] VSS[84] VSS[85] VSS[86] VSS[87] VSS[88] VSS[89] VSS[90] VSS[91] VSS[92] VSS[93] VSS[94] VSS[95] VSS[96] VSS[97] VSS[98] VSS[99] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162]

P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 AF3 AF6 AF8 AF11 AF13 AF16 AF19 AF21 AF24

GND GND

12G04600479A

+VCORE

CE301 220UF/4V @

1215---PWR comp

Place the cap on North of Secondary side

Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

Place these upper side inside socket cavity on L1

C302 C303 C304 C305 C306 C307 — 22UF/6.3V — GND

Place these lower side inside socket cavity on L1

C308 C309 C310 C311 C312 C313 — 22UF/6.3V — GND

R2 . 2

Reduce ESD

Place these upper side inside socket cavity on L6

C314 C315 C316 C317 — 22UF/6.3V — GND

C316 N/A C317 N/A

Place these lower side inside socket cavity on L6

C319 C320 C321 C322 — 22UF/6.3V — GND

R2 . 2

+VCCP_AGTL+

+1.05V Decoupling Capacitor
Place near CPU

C323 C324 C325 C326 C327 C328 — c0402 — 0.1UF/10V — GND

CE302 100UF/2.5V

<Variant Name>

Title : Yonah CPU (2)

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
A3	T12F	

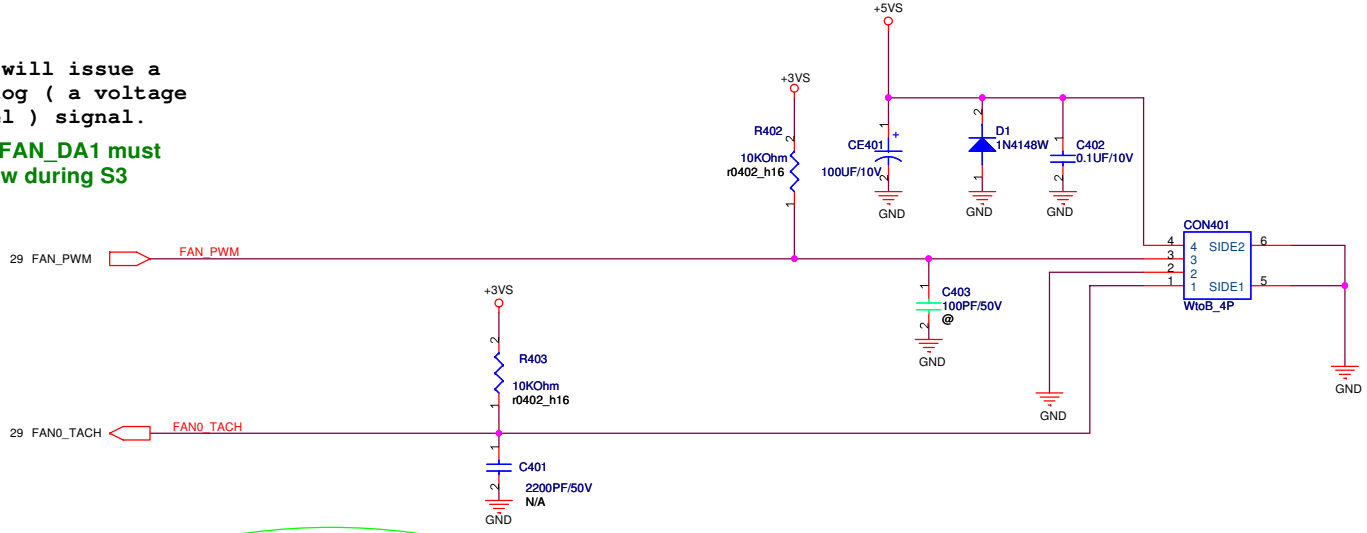
Date: 星期三, 五月 18, 2007 Sheet 3 of 61

Fan Speed Control

+5VS +5VS 13,19,20,21,22,28,29,30,37,38,50,61
+3VS +3VS 5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61
+3VA +3VA 12,20,22,29,37,38,40,54,59,63

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

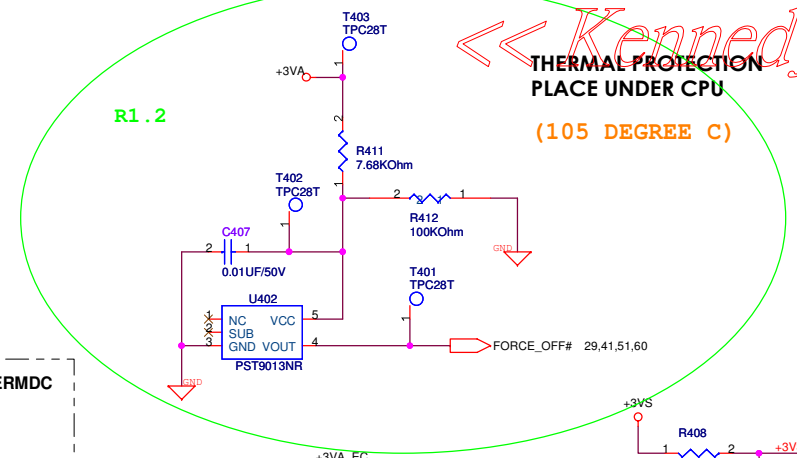


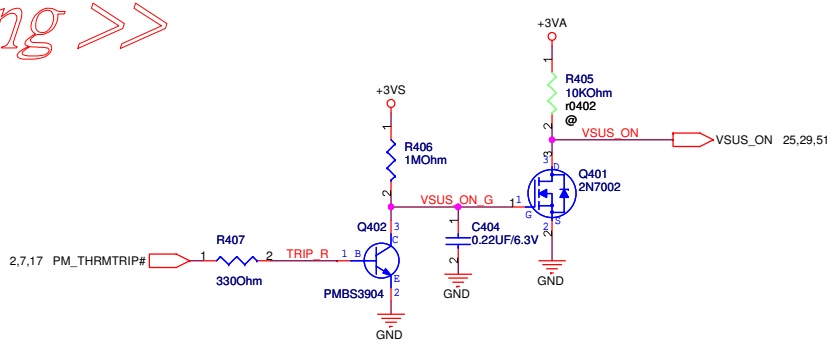
<<Kennedy_Zhang >>

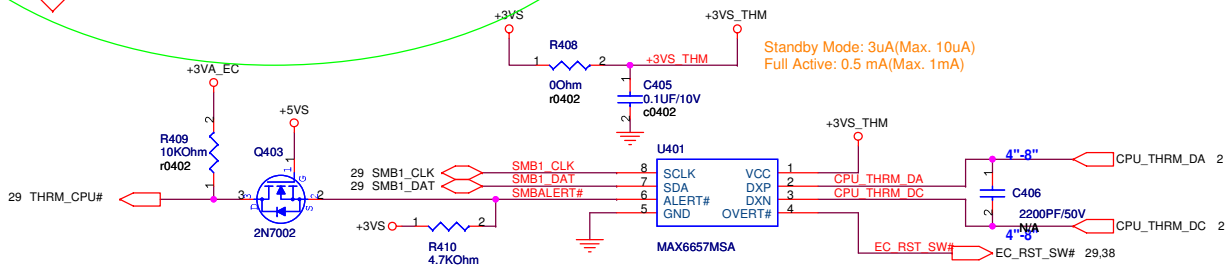
THERMAL PROTECTION
PLACE UNDER CPU

(105 DEGREE C)

R1.2







Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

<Variant Name>

Title : THER-SENSOR,FAN
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size: A3
Project Name: T12F
Rev:
Date: 星期二, 五月 15, 2007
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Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

R2.0

R1.1

U501

ICS954310CGLFT

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or
27M/27M_SS

Realtek:Mount R519,Remove R550 R534

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

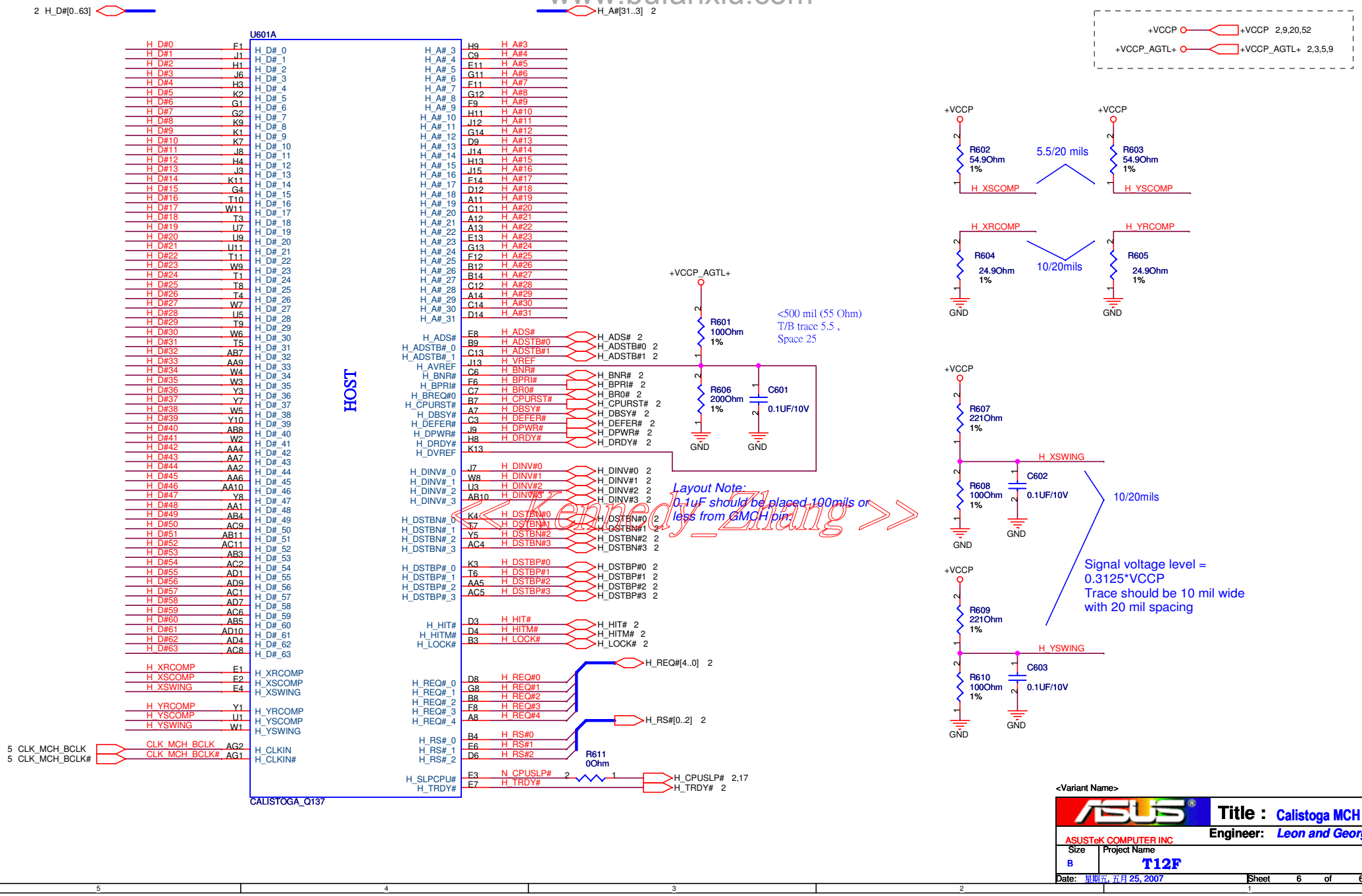
PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Internal Pull-Up Resistor

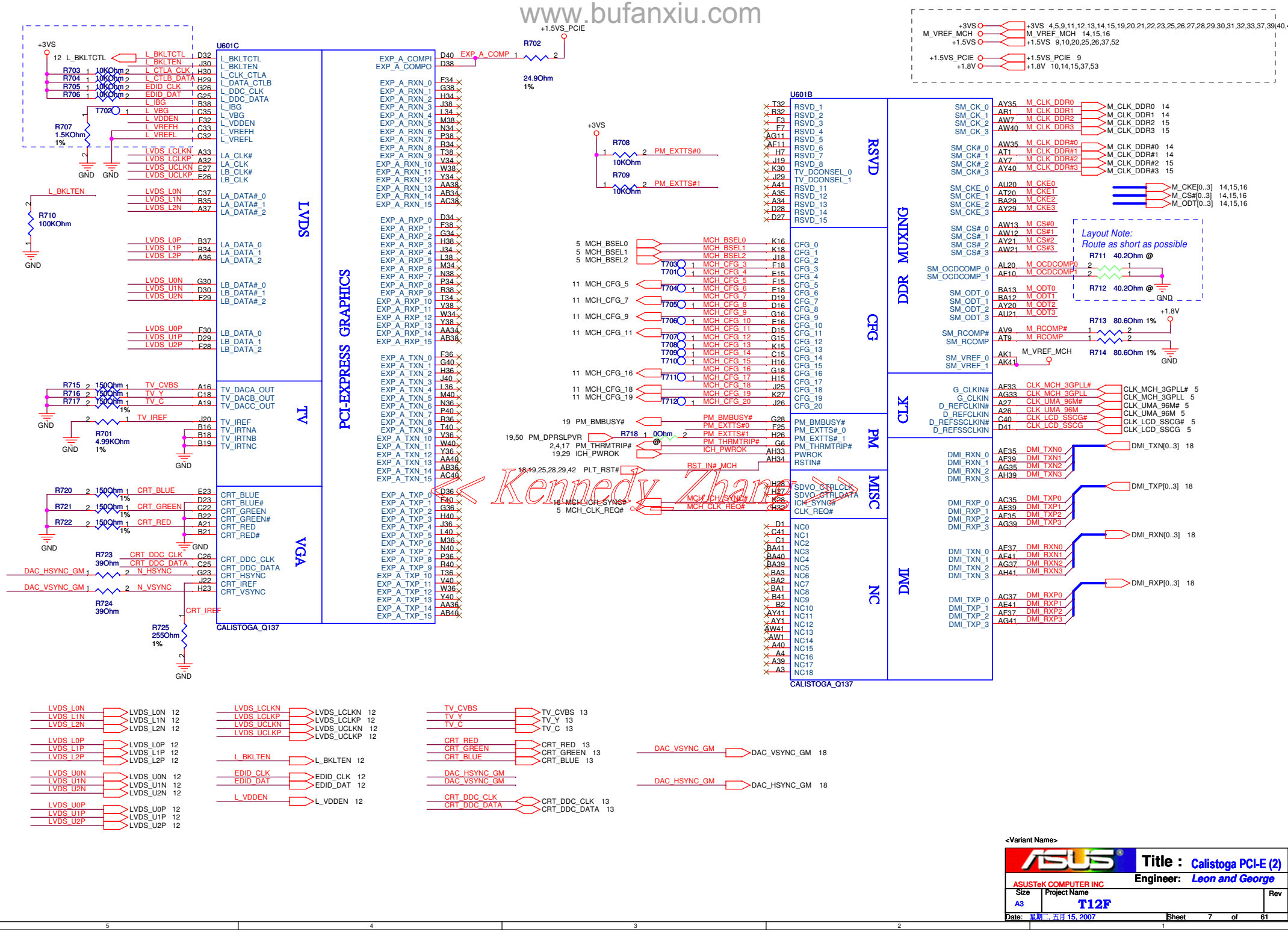
<Variant Name>

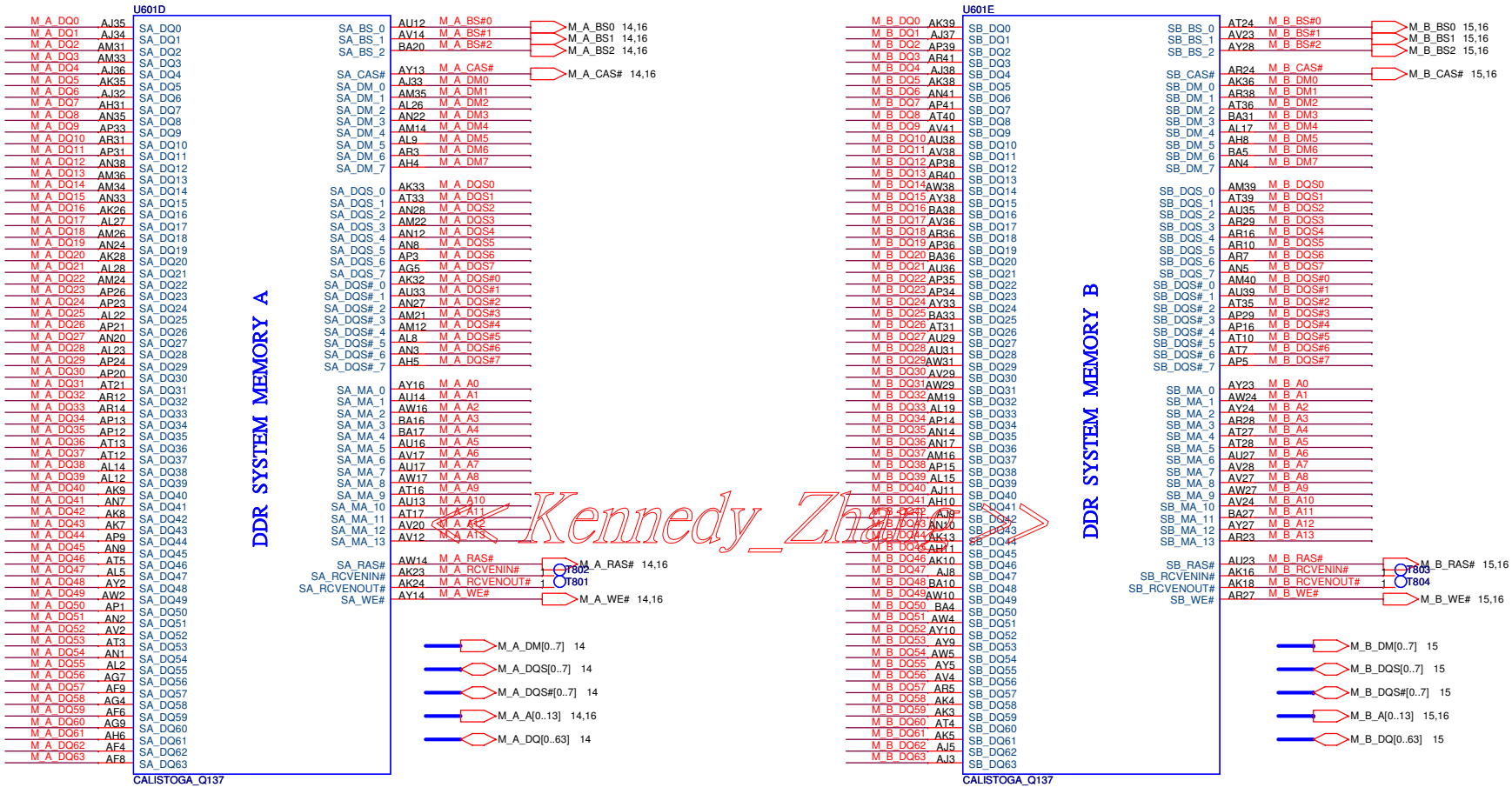
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Leon and George
Size: Custom | Project Name: T12F | Rev
Date: 星期二, 五月 15, 2007 | Sheet 5 of 61



<Variant Name>

Title : Calistoga MCH (1)		
ASUSTeK COMPUTER INC	Engineer: Leon and George	
Size: B	Project Name: T12F	Rev
Date: 星期五, 五月 25, 2007	Sheet 6 of 61	





<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga DDR2 (3)

Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

Date: 星期二, 五月 15, 2007 Sheet 8 of 61

Layout Note:
Place filter components close to GMCH

Layout Note:
Caps should be on Top layer

VCC3G
1500 mA
VCCA_3GPLL
VCCAUX 1900 mA
VCCA_DPLLA 50 mA
VCCA_DPLLB 50 mA
VCCA_HPLL 45 mA
VCCA_MPLL 45 mA

GMCH VCORE

+1.05VS 3500 mA
JP902 SHORT_PIN @
JP901 SHORT_PIN @

VCCD_LVDS 20 mA
Pin A28 B28 C28

24 mA

Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
0.1uF caps in 1.5VS_xPLL need to be located as edge caps within 200 mils.

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

VCCA_LVDS Pin A38 10 mA
VCCA_3GBG Pin G41 2 mA
VCCTX_LVDS 60 mA Pin A30 B30 C30

70 mA

VCC_HV 40 mA Pin A23 B23 B25

Layout Note:
These Caps should be within 250 mils of edge of GMCH

POWER

U601H
CALISTOGA_Q137

Layout Note:
These Caps used in +3VS_TVDACx should be within 250 mils of edge of GMCH

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS
+2.5VS should be placed within 200 mils of edge.

Layout Note:
Place on the edge

800 mA

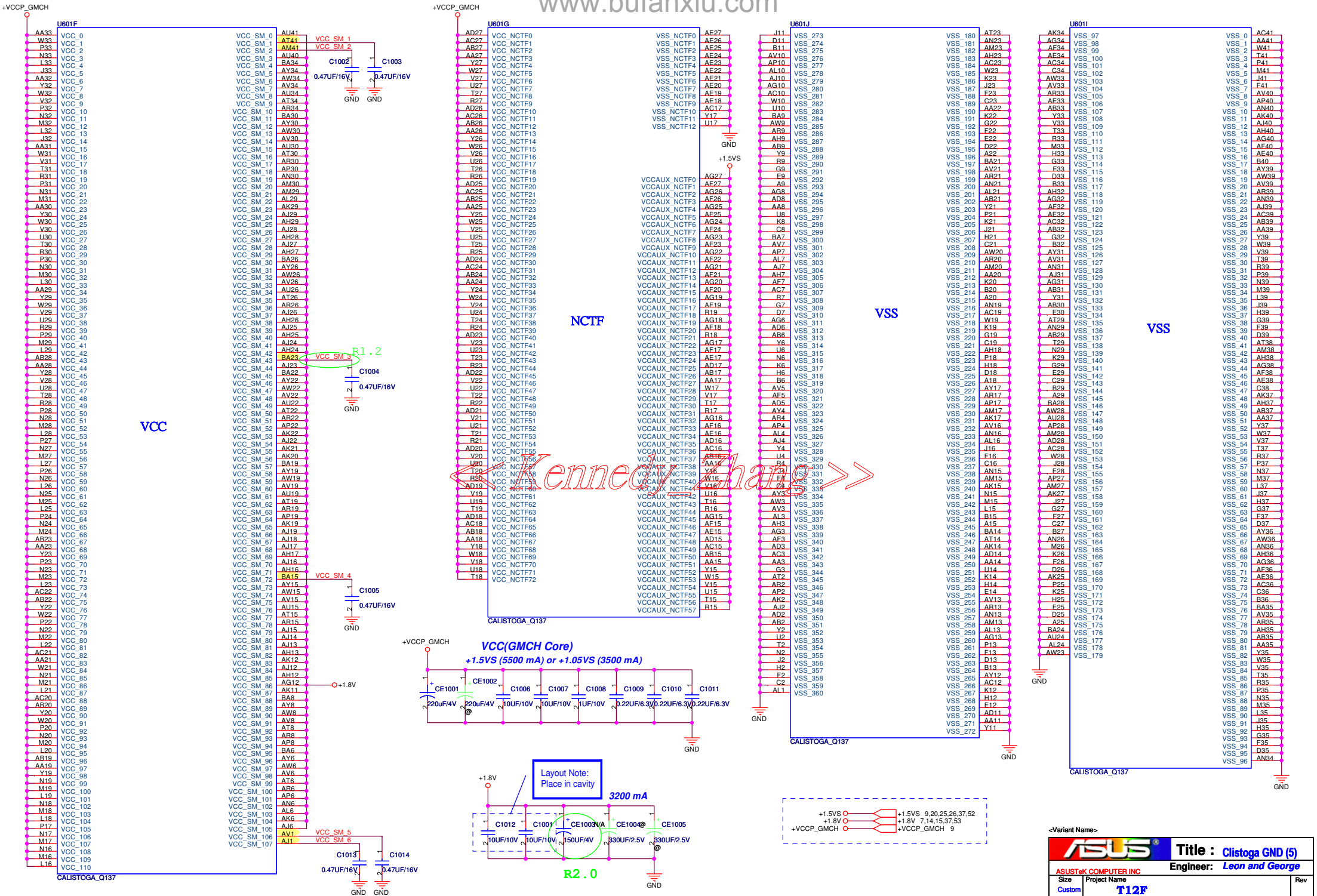
Layout Note:
Place in cavity

Total Power Consumption 120 mA

VCCA_TVBG Pin H20
VCCA_TVDACA Pin E19 F19
VCCA_TVDACB Pin C20 D20
VCCA_TVDACC Pin E20 F20

<Variant Name>

Title : Calistoga Power (4)		
Engineer: Leon and George		
ASUSTeK COMPUTER INC		
Size: A3	Project Name: T12F	Rev
Date: 星期五, 五月 18, 2007	Sheet 9 of 61	



<Variant Name>

ASUSTeK COMPUTER INC

Title : Clistoga GND (5)

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

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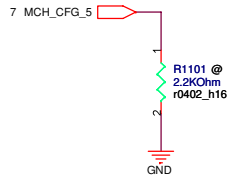
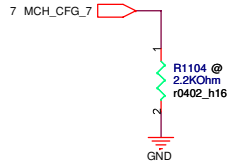
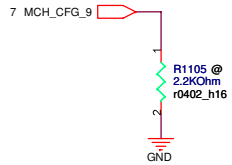


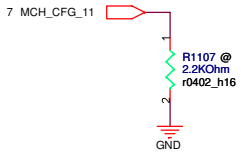
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



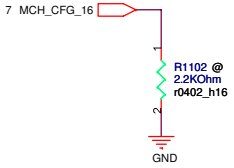
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



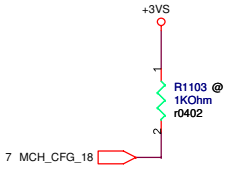
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



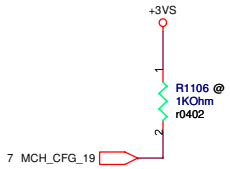
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane	0 = Reverse Lanes 1 = Normal (Default)
11:10	Reversal	
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga Strapping
Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

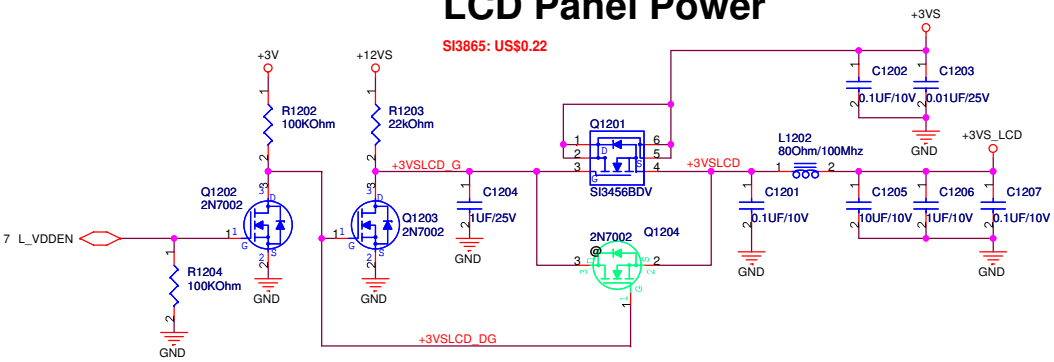
Date: 星期二, 五月 15, 2007 Sheet 11 of 61

3~3.6V
Full Active: 410 mA(Max. 500 mA)

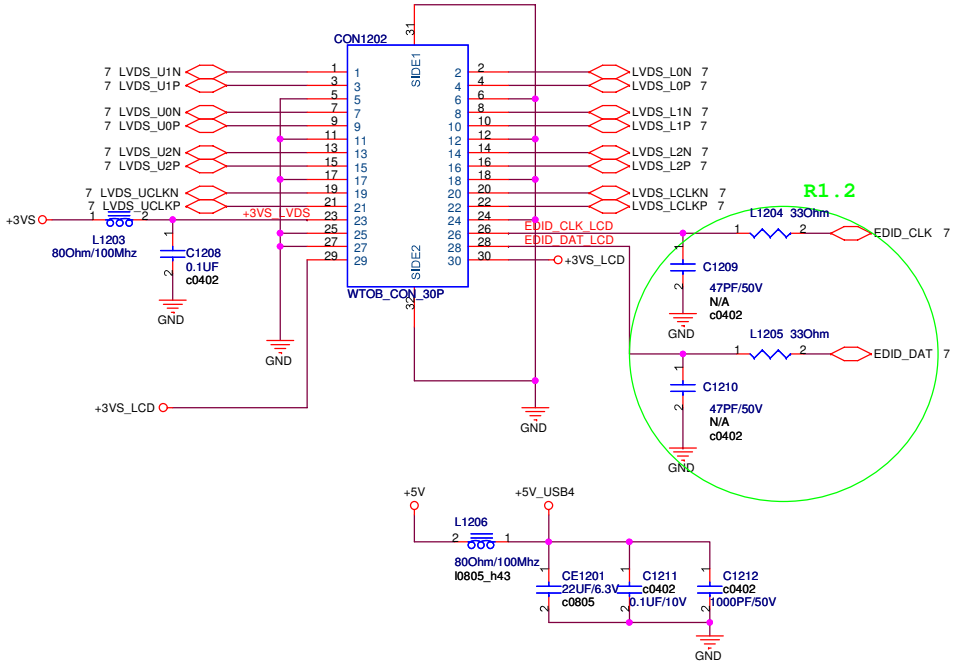
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

LCD Panel Power

SI3865: US$0.22



LCD LVDS Interface



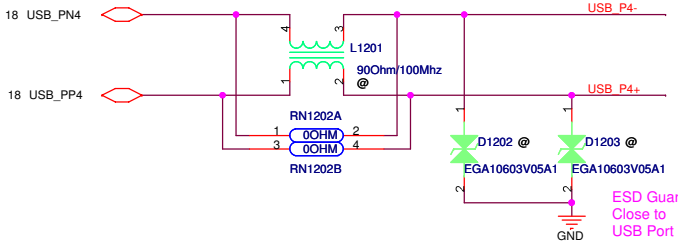
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

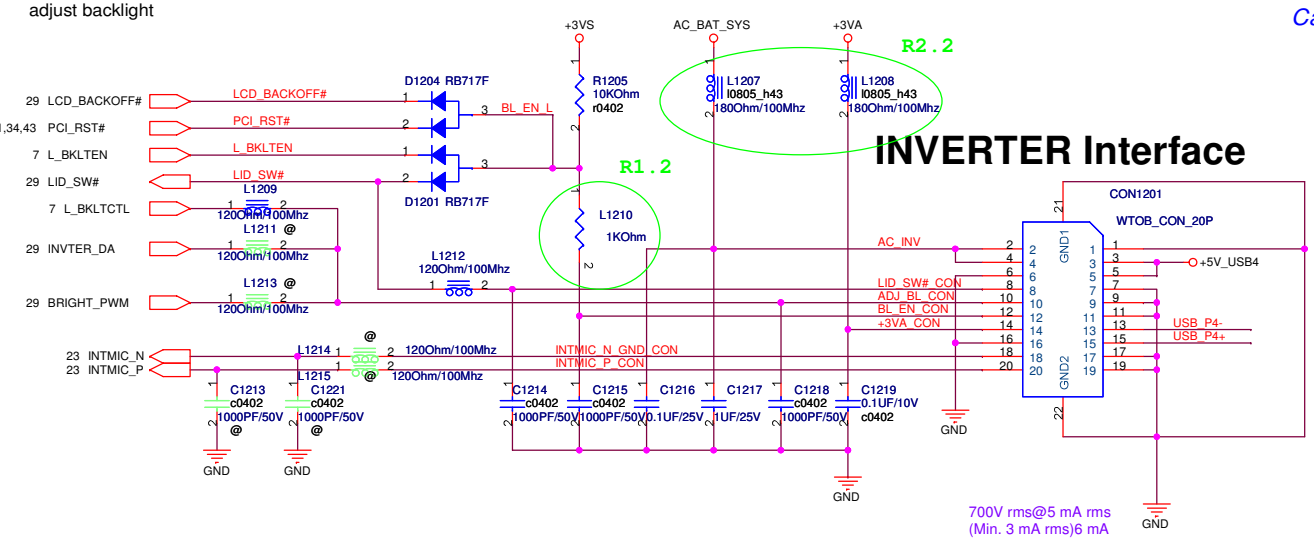
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 14 1W LCD Panel

USB4 For CMOS Camera



INVERTER Interface

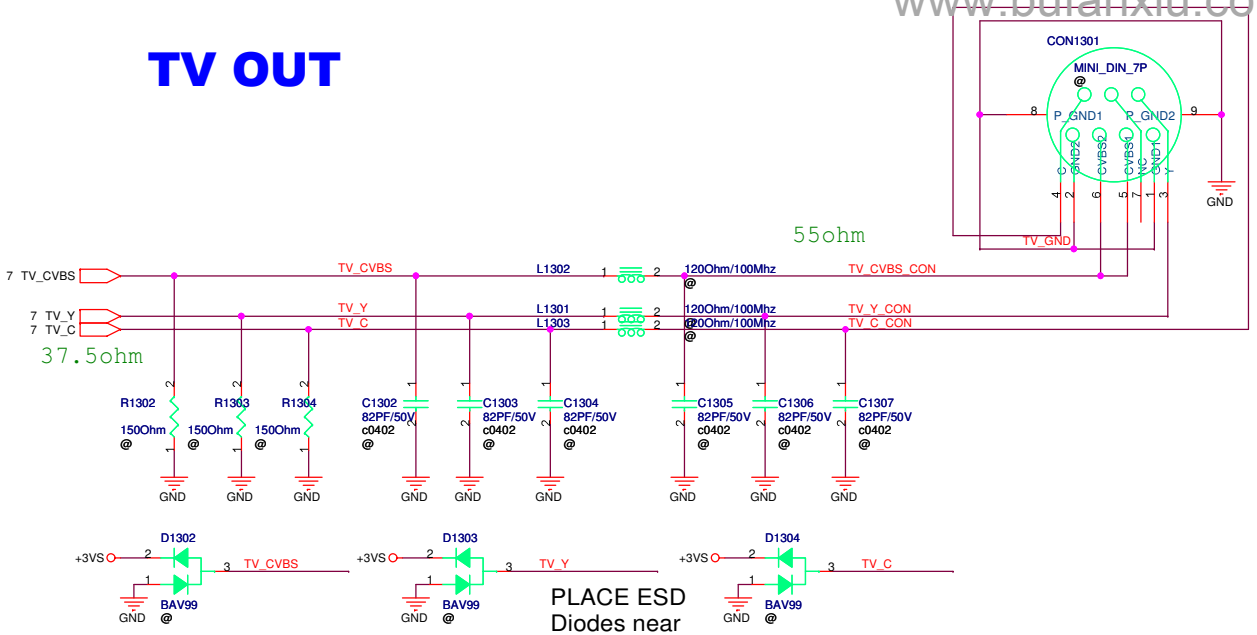


700V rms@5 mA rms (Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

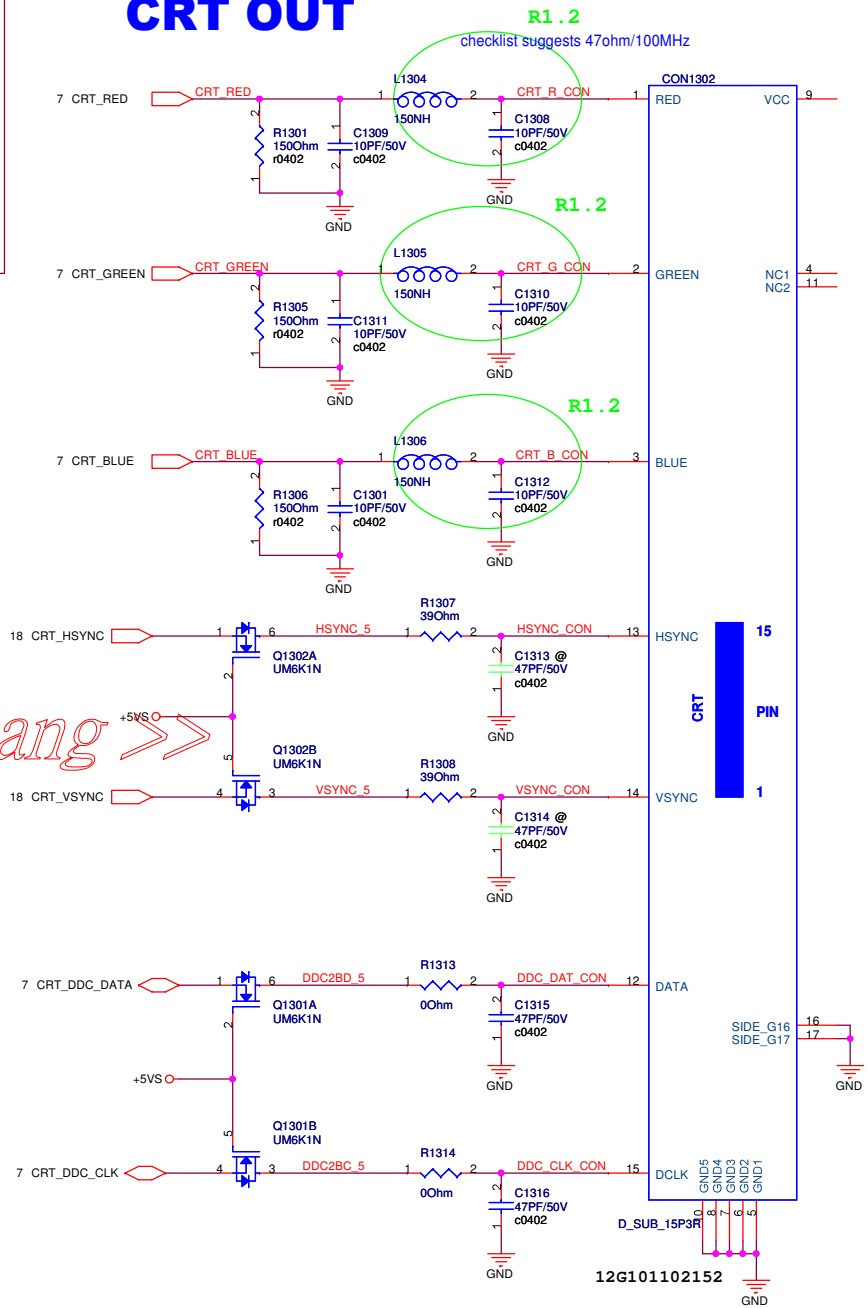
<Variant Name>

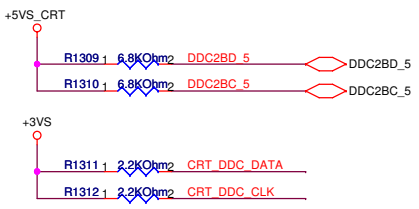
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Leon and George	
Size: A3	Project Name: T12F	Rev
Date: 星期一, 五月 21, 2007	Sheet 12 of 61	

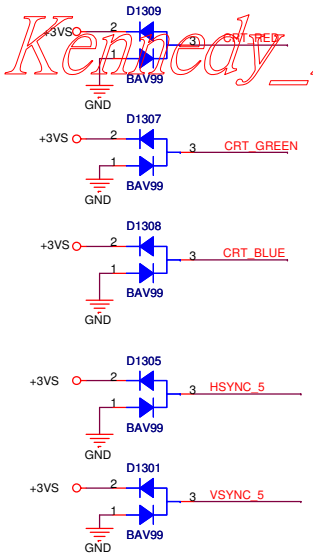
TV OUT



CRT OUT







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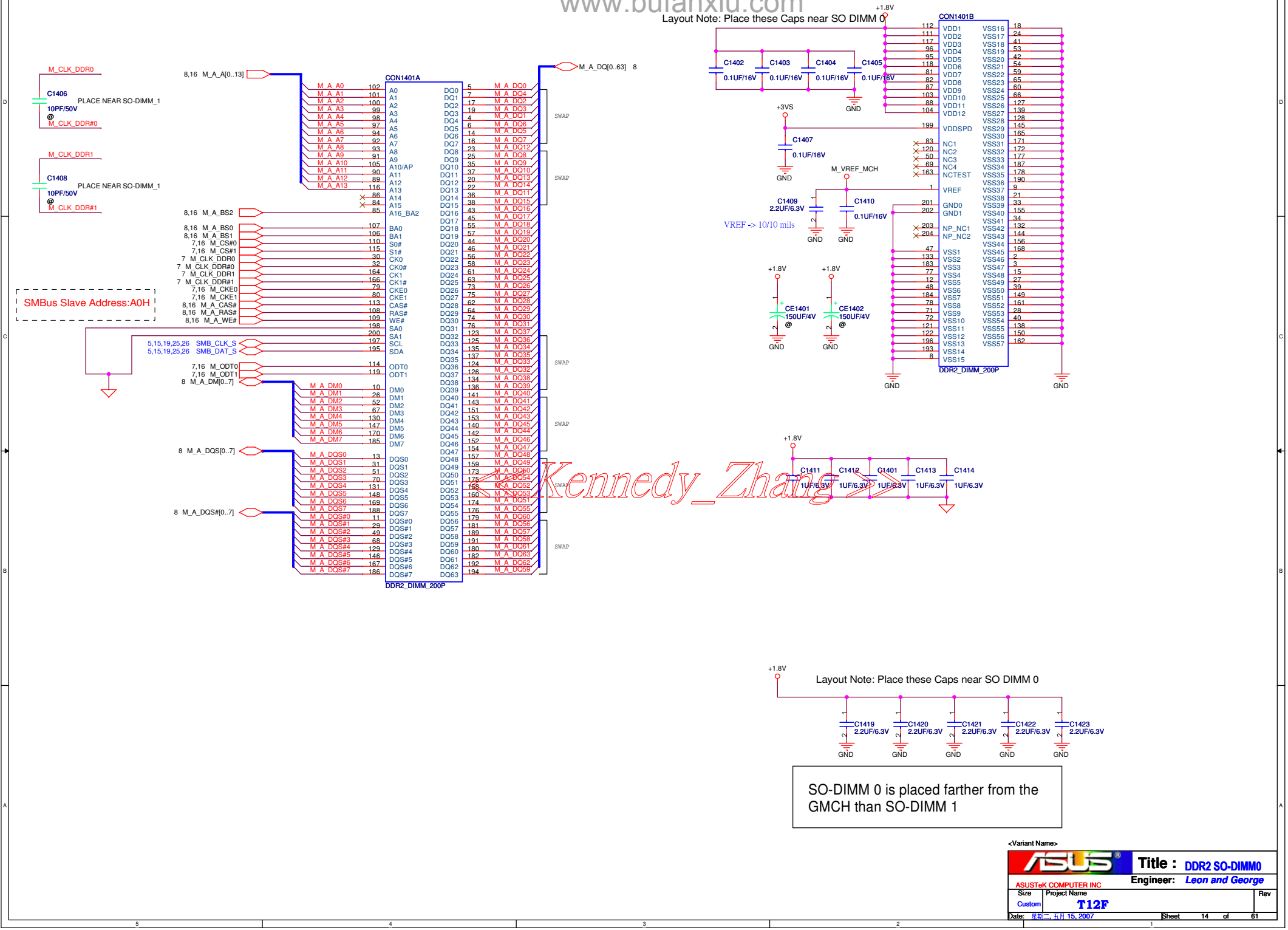
ASUSTeK COMPUTER INC	Title : CRT & TV OUT	
	Engineer: Leon and George	
Size: A3	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 13 of 61	



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM0

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: 星期二, 五月 15, 2007 Sheet 14 of 61

SMBus Slave Address:A4H

Address reference +1.8V, add four 0.1uF decoupling CAP.

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these High-Freq decoupling Caps near the GMCH

Layout Note: Place these CAPs near the GMCH

<Variant Name>

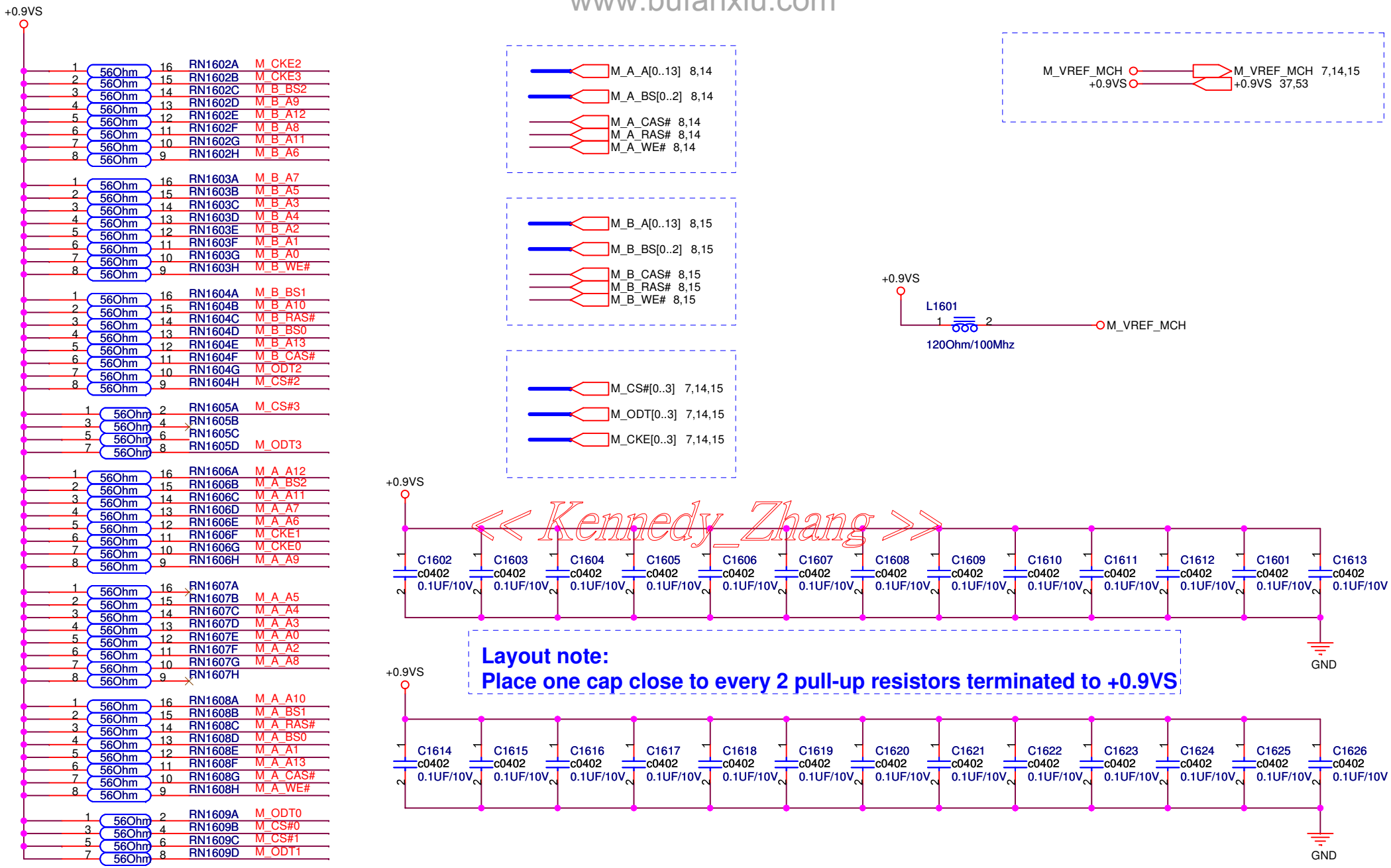
Title : DDR2 SO-DIMM1

ASUSTeK COMPUTER INC

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: 星期二, 五月 15, 2007 Sheet 15 of 61



<Variant Name>

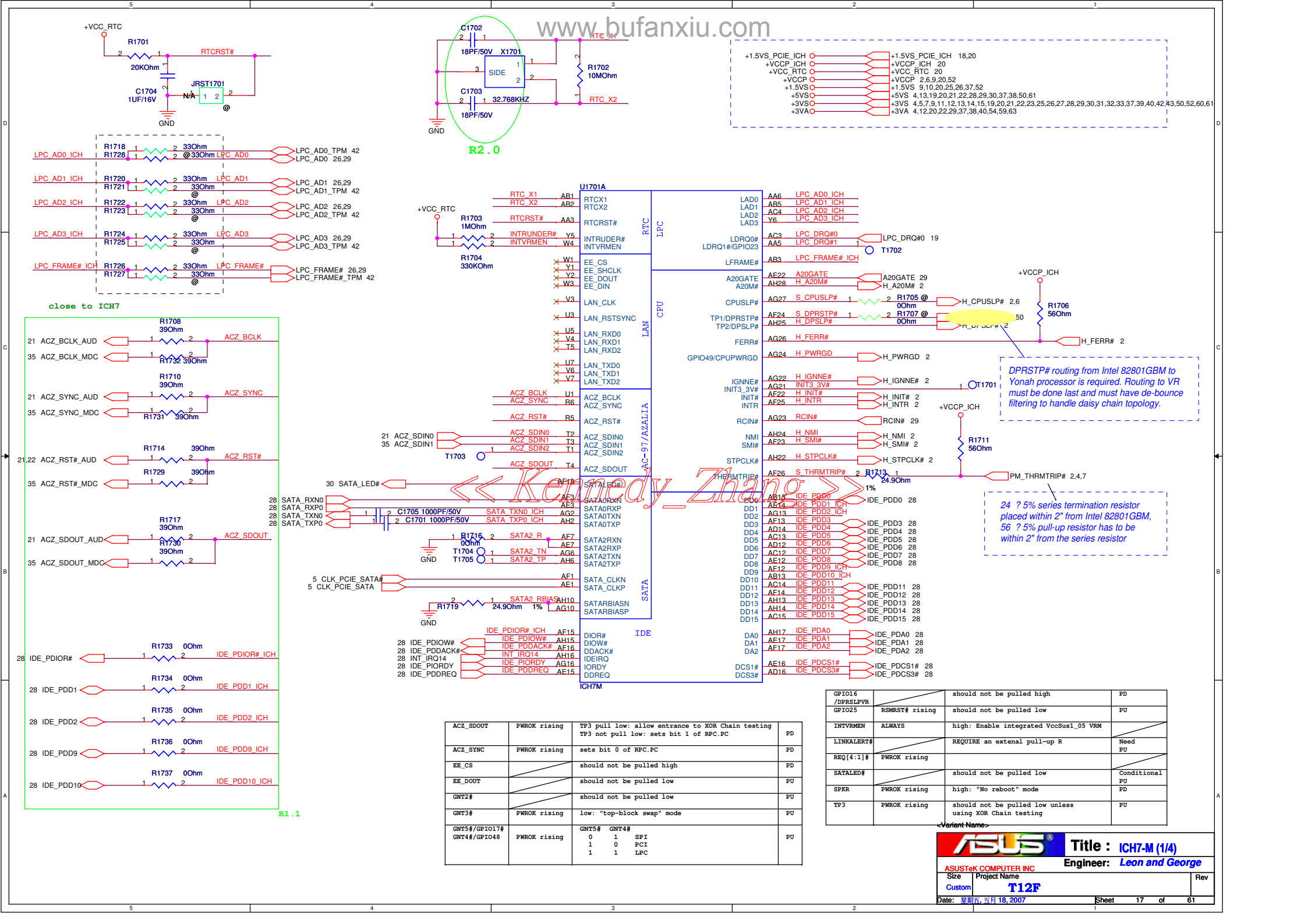
ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: 星期二, 五月 15, 2007 Sheet 16 of 61



ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (1/4)

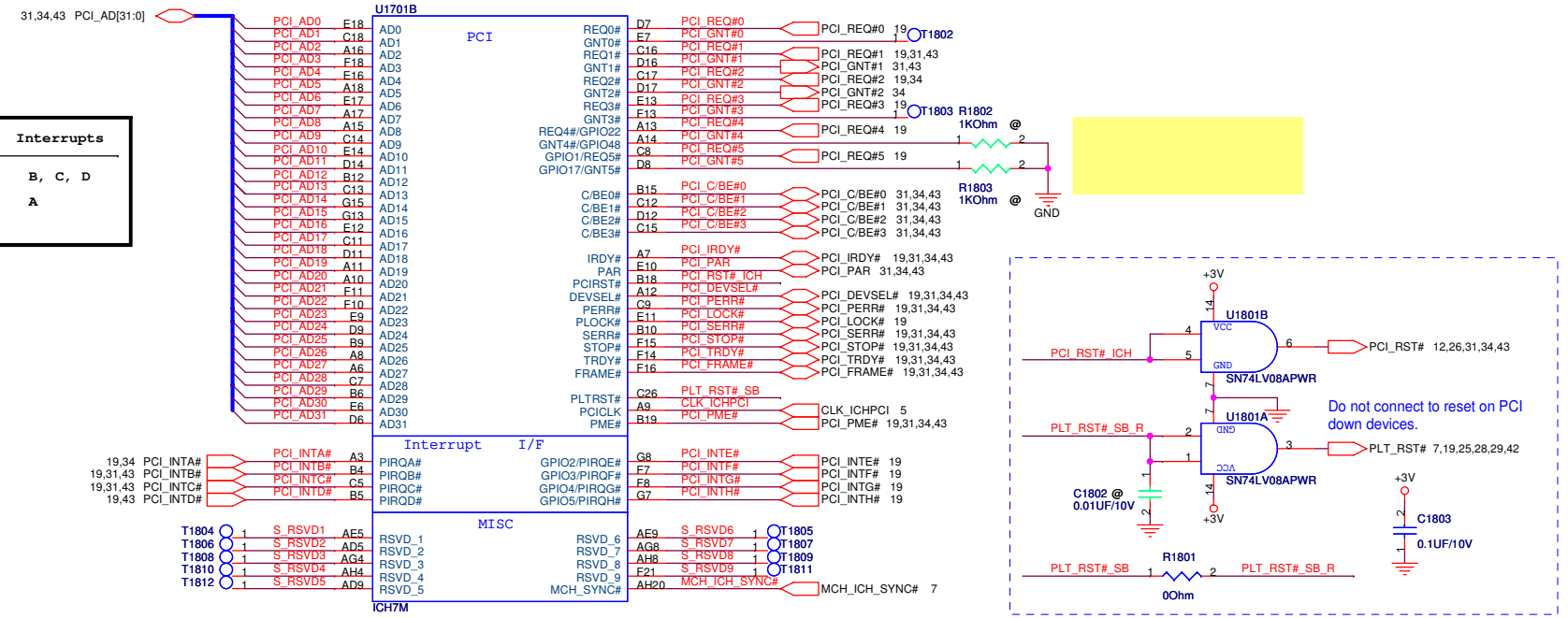
Engineer: Leon and George

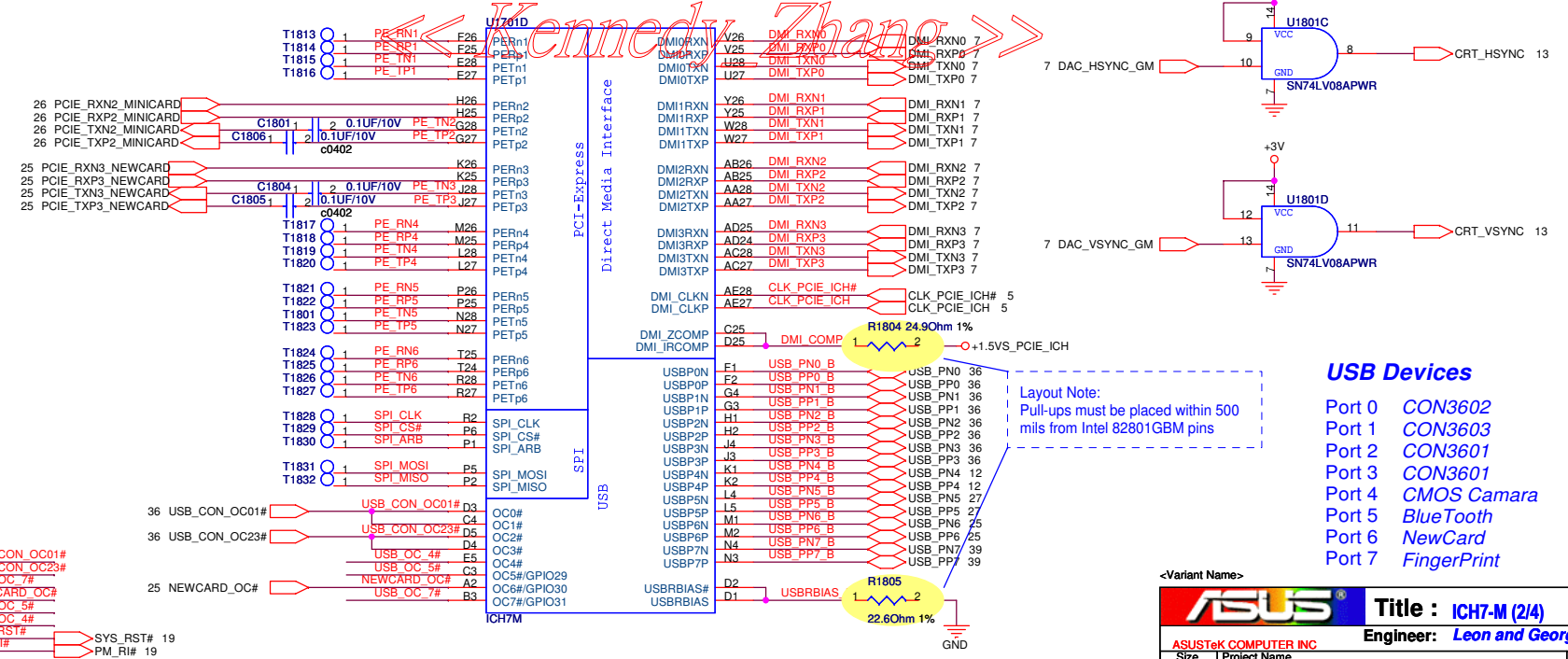
Size	Project Name	Rev
Custom	T12F	

Date: 星期五, 五月 18, 2007 Sheet 17 of 61

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A





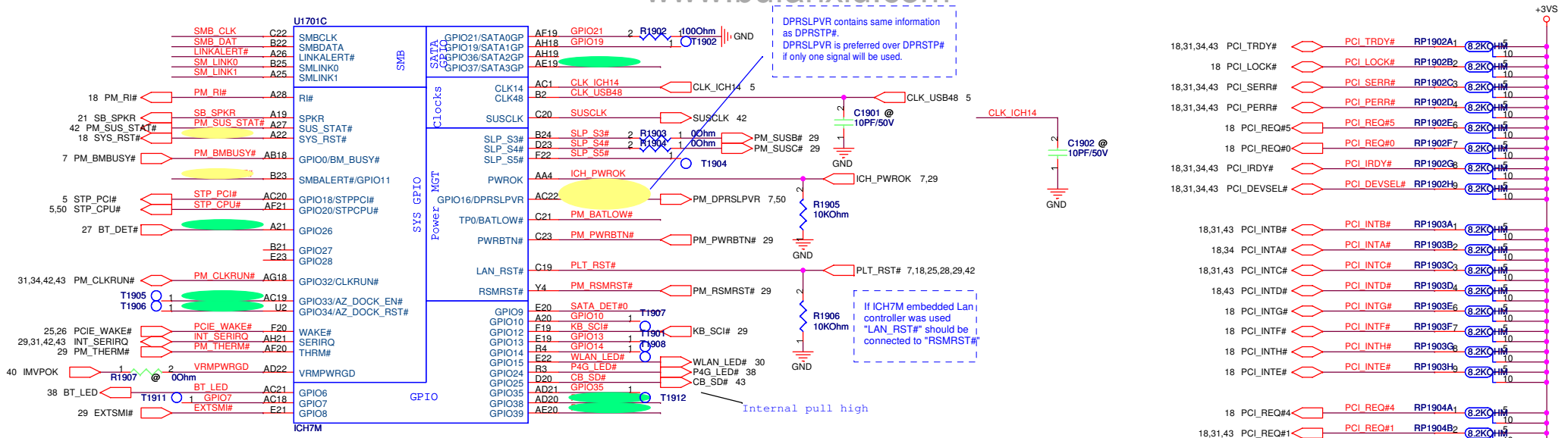
Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

USB Devices

Port 0	CON3602
Port 1	CON3603
Port 2	CON3601
Port 3	CON3601
Port 4	CMOS Camara
Port 5	BlueTooth
Port 6	NewCard
Port 7	FingerPrint

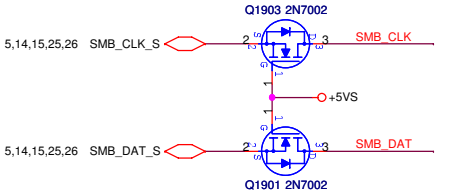
<Variant Name>

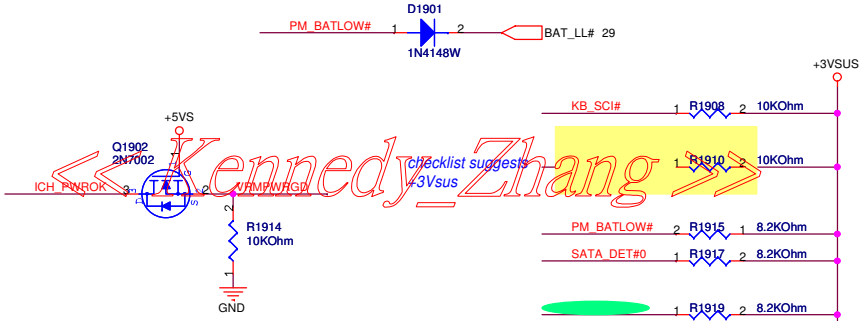
Title : ICH7-M (2/4)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12F | Rev
Date: 星期二, 五月 15, 2007 | Sheet 18 of 61

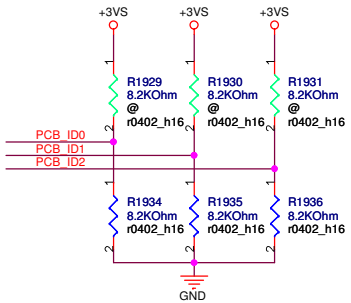


GPIO Power Plane

CPU Vcore	GPIO[49]
5V Core	GPIO[5:1]
3.3V Core	GPIO[0][7:6][23:16][39:32][48]
3.3V Resume	GPIO[15:8][31:24]

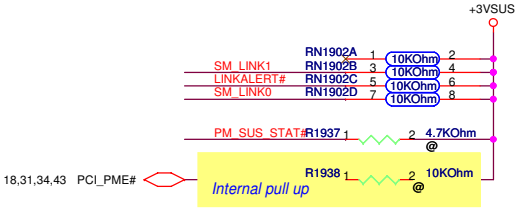


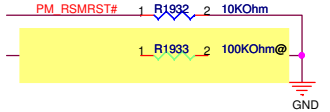




PCB_VID3 : PROJECT CODE

PCB_VID	0	1	2
MB V1.0	0	0	0





<Variant Name>

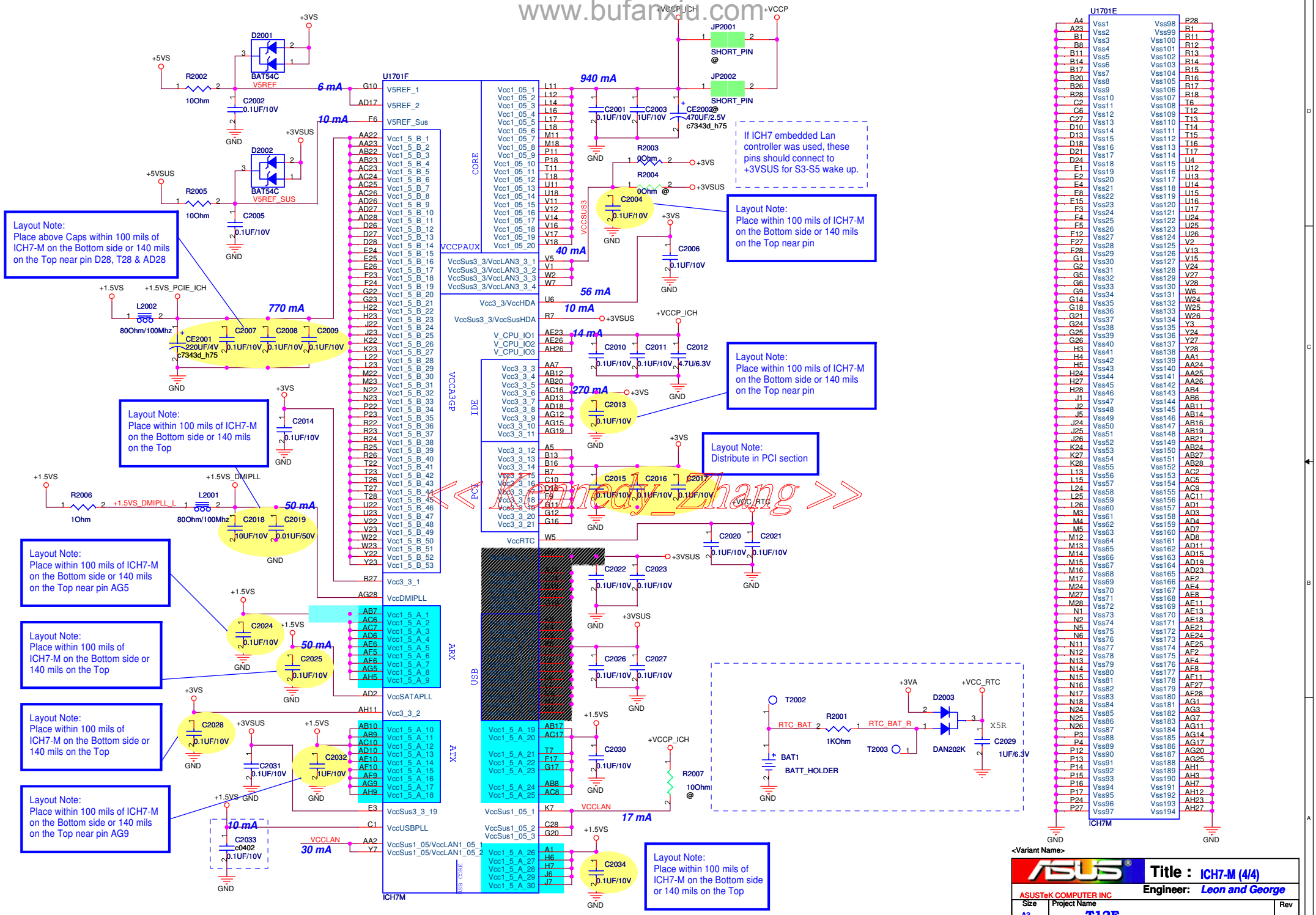
Title : ICH7-M (3/4)

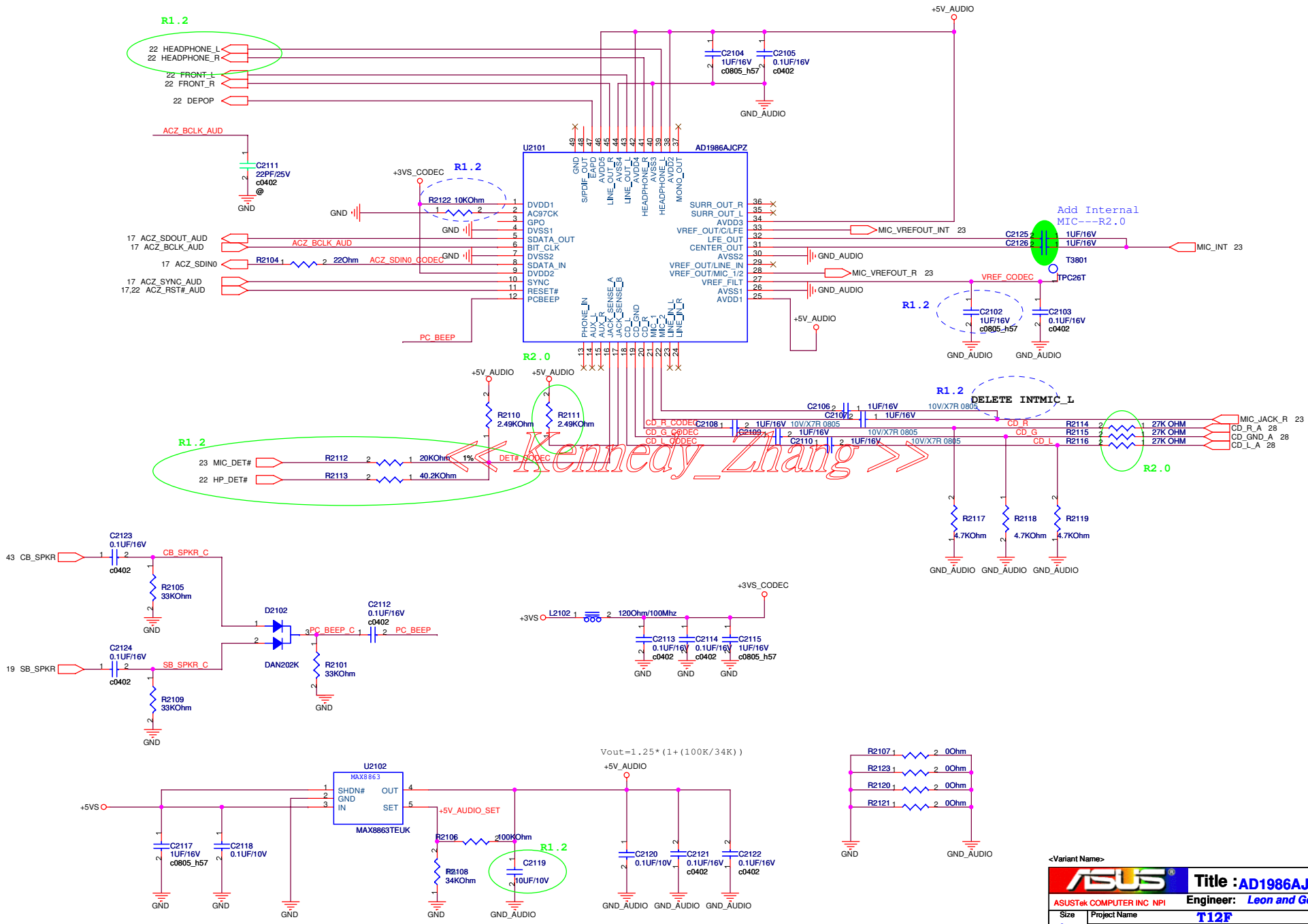
Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
A3	T12F	

Date: 星期五, 五月 18, 2007 Sheet 19 of 61





<Variant Name>

ASUSTek COMPUTER INC NPI

Title : AD1986AJCPZ

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	
	P/N <OrgAddr2>	

Date: 星期五, 五月 18, 2007 Sheet 21 of 61

Woofer (Optional)

The sub-woofer dimension could be less than 20mm. fo will be >400Hz.

BPF first, then Power Amp

Woofer frequency response setting: FL = 153Hz, FH = 2.26KHz

FL = TBD
FH = TBD

(Headphone Mode) FL = TBD
(Headphone Mode) FH = TBD

AV= 0dB

AV= 6dB

<<Kennedy_Zhang>>

HP JACK

100PF/50V use 11G233010104311---change

Change for Layout

To Internal Speaker Connector

<Variant Name>

Title : AUDIO AMP

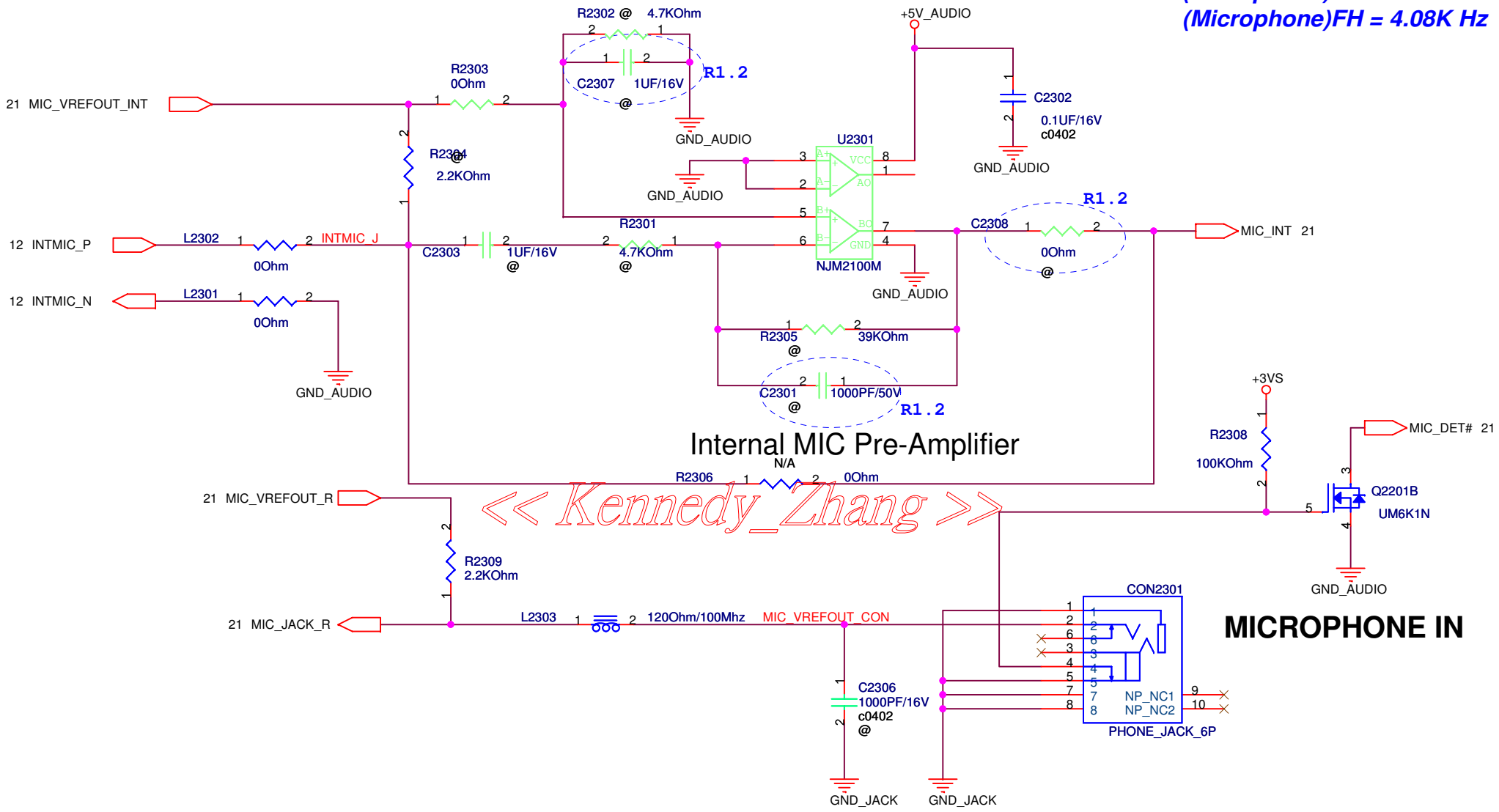
Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	

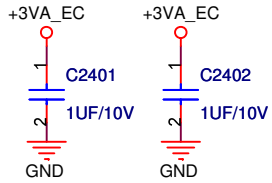
Date: 星期五, 五月 18, 2007 Sheet 22 of 61

(Microphone)FL = 33.86 Hz
(Microphone)FH = 4.08K Hz

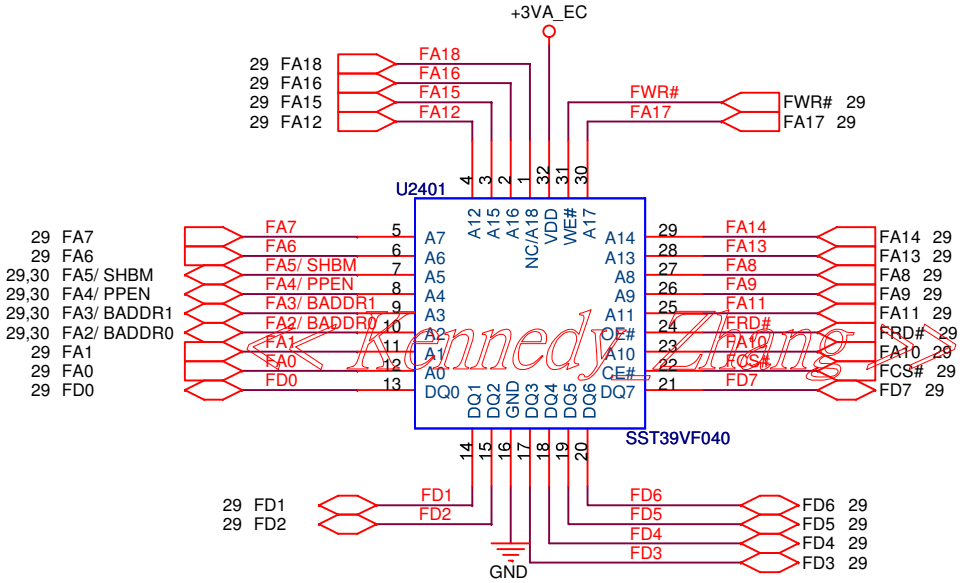


<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC Pre-AMP	
	Engineer: Leon and George	
Size: A4	Project Name: T12F	Rev
Date: 星期一, 五月 21, 2007	Sheet 23 of 61	



ISA ROM



<Variant Name>

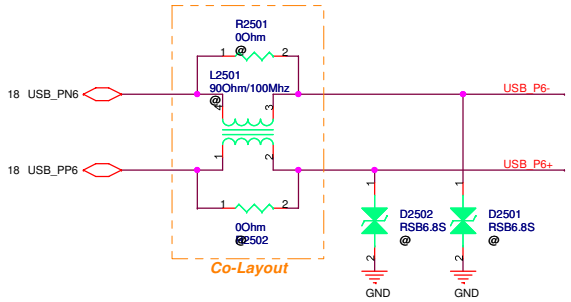
ASUSTeK COMPUTER INC

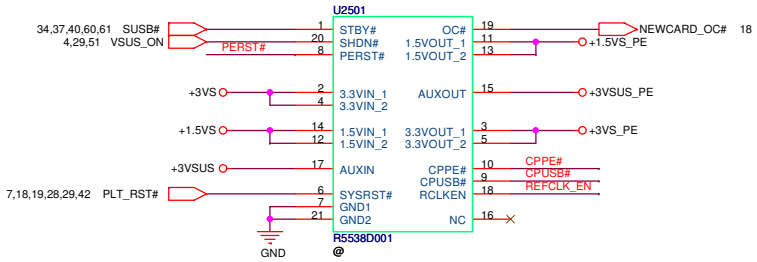
Title : ISA ROM

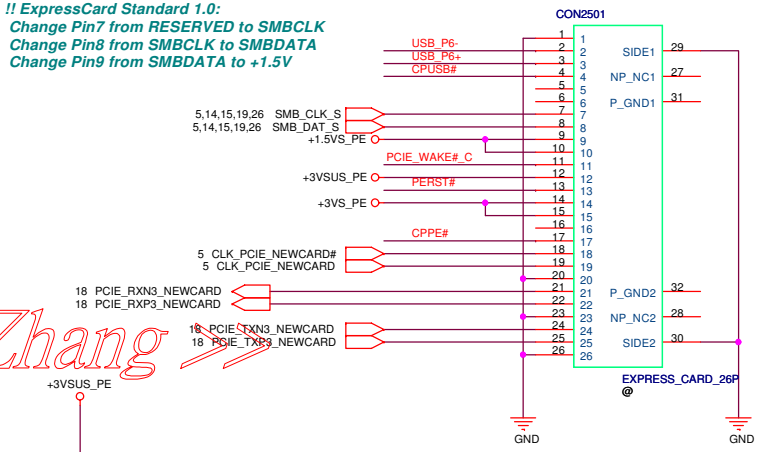
Engineer: Leon and George

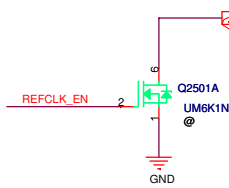
Size	Project Name	Rev
A4	T12F	

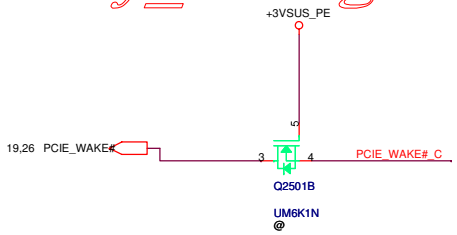
Date: 星期二, 五月 15, 2007 Sheet 24 of 61

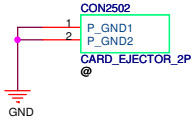


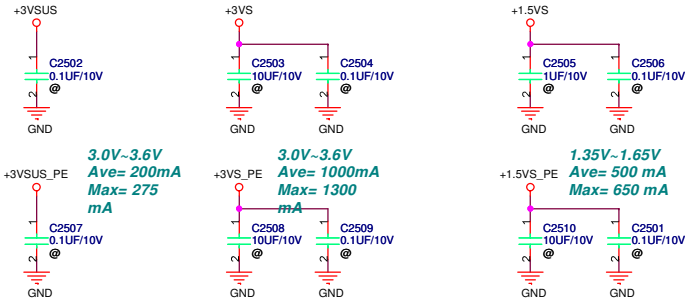








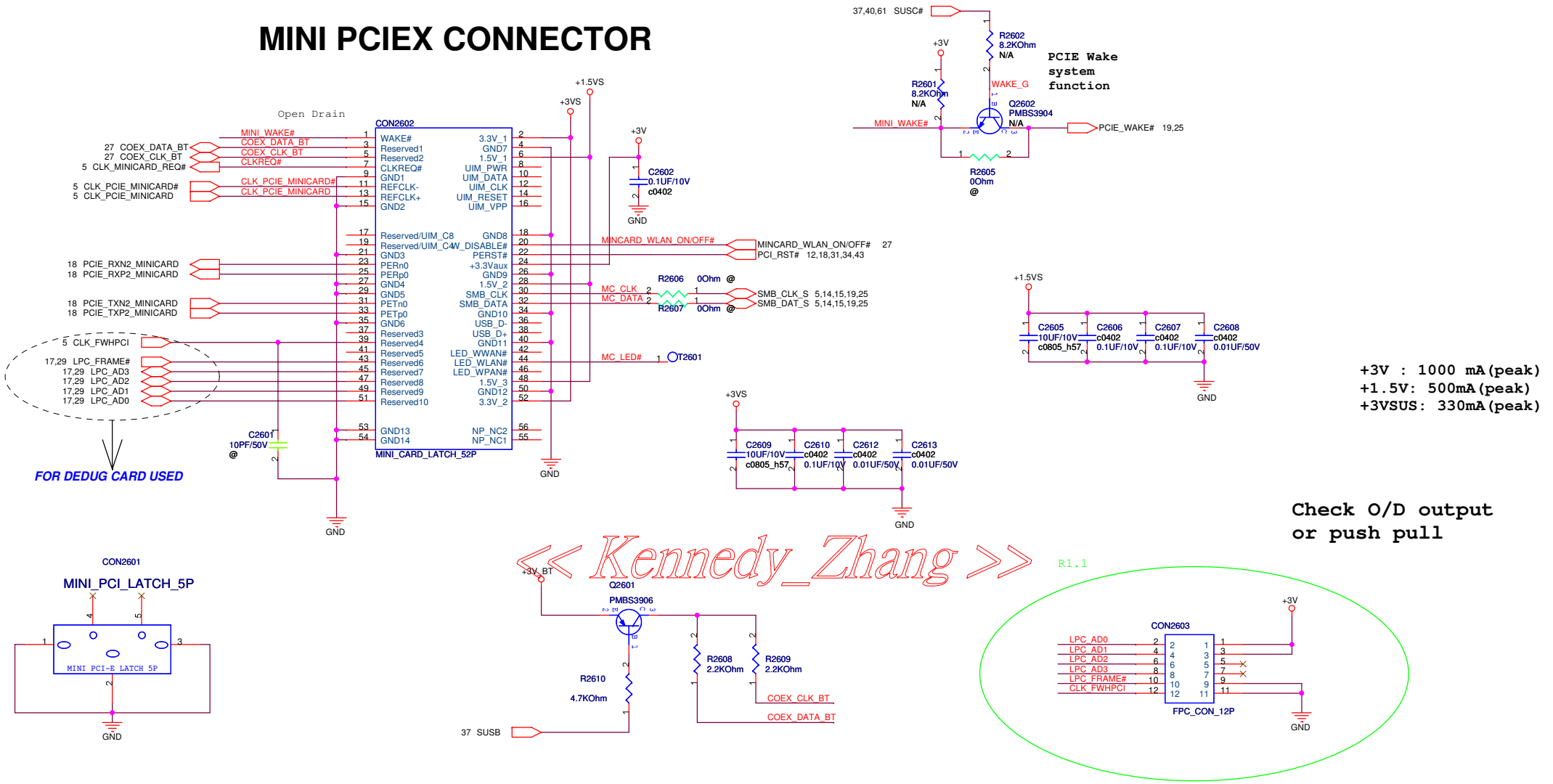




<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 25 of 61	

MINI PCIEX CONNECTOR



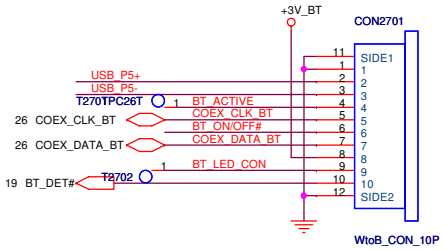
+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

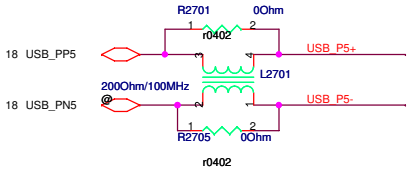
Check O/D output
or push pull

<Variant Name>

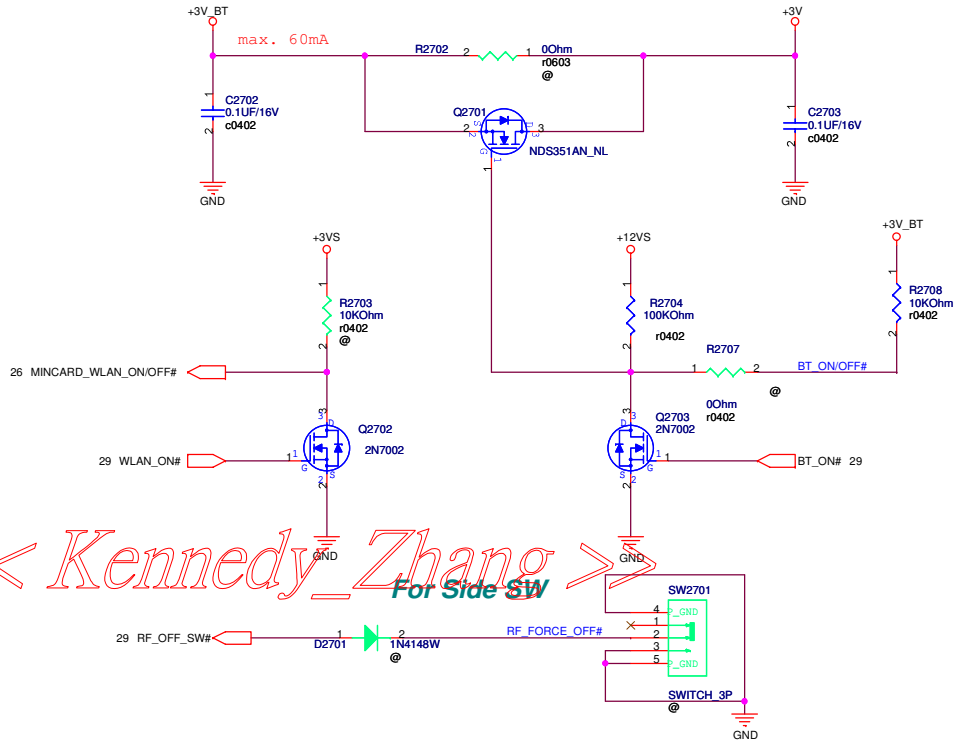
ASUSTeK COMPUTER INC	Title : MINI PCIEX	
	Engineer: Leon and George	
Size: A3	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 26 of 61	

For Bluetooth



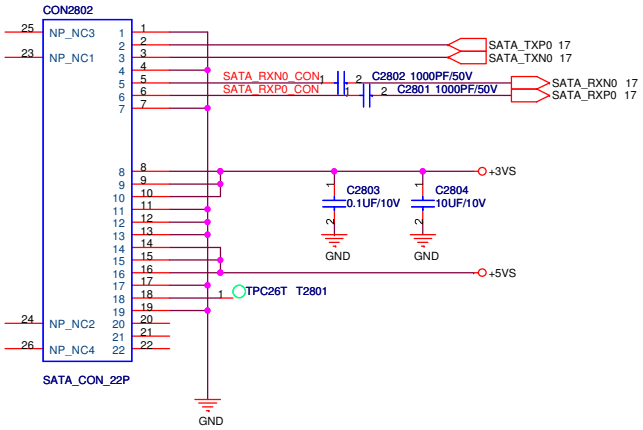


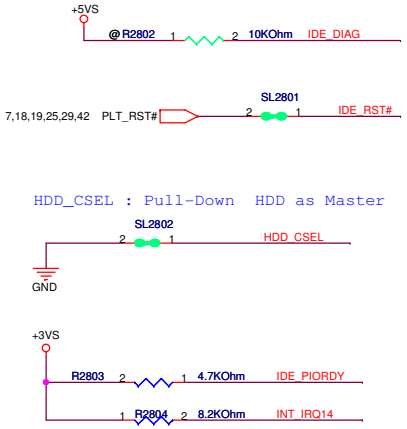
WLAN/BT ON/OFF Control

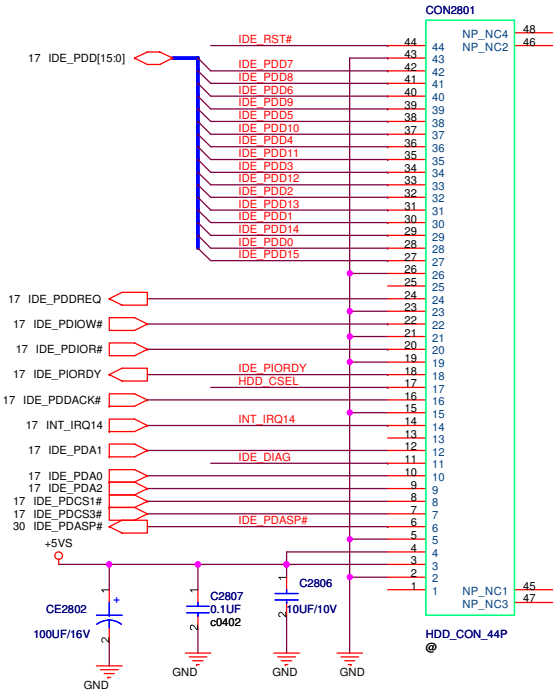


<Variant Name>

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期四, 五月 24, 2007	Sheet 27 of 61	



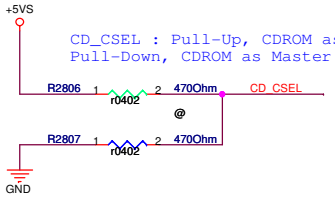


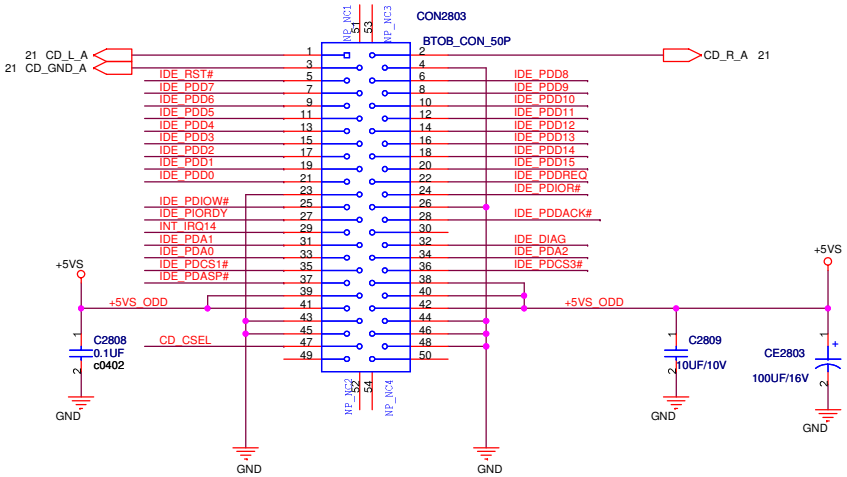


SATA HDD

PATA HDD

CD-ROM





<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : PATA-SATA & ODD	
	Engineer:	
Size: Custom	Project Name: T12F	Rev
Date: 星期一, 五月 21, 2007	Sheet 28 of 61	

TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

Follow Z94 Keyboard

U2901 IT8511TE

LPC: LAD0 LAD1 LAD2 LAD3 LPCCLK LFRAME# LPCRST#/WUI4/GPD2 SERIRQ ECSMI#/GPM0 ECSCI#/GPD3 GA20/GPB5 KBRST#/GPB6 WRST# PWUREQ#/GPM1

FLASH ROM: FRD# FWR# FCS# FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7 FA0 FA1 FA2/BADDR0 FA3/BADDR1 FA4/PPEN FA5/SHBM FA6 FA7 FA8 FA9 FA10 FA11 FA12 FA13 FA14 FA15 FA16/GPG0 FA17/GPG1 FA18/GPG2 FA19/GPG3

KBMX: KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

PS2: CK32K CK32KE PS2CLK0/GPF0 PS2DAT0/GPF1 PS2CLK1/GPF2 PS2DAT1/GPF3

SMBus: SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2

ADC: ADC0/GPK0 ADC1/GPK1 ADC2/GPK2 ADC3/GPK3 ADC8/GPK4 ADC9/GPK5

DAC: DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3

GPIO: PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/GPA6 PWM7/GPA7 RXD/GPB0 TXD/GPB1 GPB2 RING#/PWRFAIL#/LPCRST#/GPB7 CLKOUT/GPC0 GPC3 TMRI0/WUI2/GPC4 GPC5 TMRI1/WUI3/GPC6 CK32KOUT/GPC7 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1 GPD4 GINT/GPD5 TACH0/GPD6 TACH1/GPD7 ADC4/GPE0 ADC5/GPE1 ADC6/GPE2 ADC7/GPE3 PWRSW/GPE4 WUI5/GPE5 LPCPD#/WUI6/GPE6 CLKRUN#/WUI7/GPE7 PS2CLK2/GPF4 PS2DAT2/GPF5 PS2CLK3/GPF6 PS2DAT3/GPF7 FA20/GPG4 FA21/GPG5 LPC80HL/GPG6 LPC80LL/GPG7 GPH0 GPH1 GPH2 GPH3 GPH4 GPH5 GPH6 GPH7 GPI0 GPI1 GPI2 GPI3 GPI4 GPI5 GPI6

TBD

R2.0
close to EC
X2901 32.768KHz C2911 15PF/50V C2915 15PF/50V R2919 @ 10MOhm R2920 0Ohm CLK32 EC_XIN EC_XOUT
Cload=12.5PF

R2922 0Ohm ECSCI# KB_SCI# KB_SCI# 19
R2921 0Ohm EC_AGND

RF_LED CRX 30 RF_LED 30,38 RF_OFF_SW# 27 BT_ON# 27 WLAN_ON# 27

Layout Note: Close to Switch

THRO_CPU Q2902 2N7002 H_PROCHOT_S# 2

R2.2
4,38 EC_RST_SW# R2918 0Ohm N/A C2910 0.1UF/50V U2902 RN5VD27CA C2912 0.1UF/10V

4,41,51,60 FORCE_OFF#

Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms

<Variant Name>

Title : EC IT8510TE
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size A3 | Project Name T12F | Rev
Date: 星期五, 五月 18, 2007 | Sheet 29 of 61

EC Hardware Strap

Strap value sampled after VSTBY power up reset

+3VA_EC

PNPCFG base address set by SWCBAHR/SWCBALR

R3002 @ 10KOhm r0402

FA2/ BADDR0 — FA2/ BADDR0 24,29

R3006 10KOhm r0402

GND

+3VA_EC

R3003 10KOhm r0402

FA3/ BADDR1 — FA3/ BADDR1 24,29

R3007 @ 10KOhm r0402

GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

EC ADC

Battery

BAT — **16.8V**

R3004 @ 18KOhm r0402_h16

BAT0_R_AD

R3008 @ 3.92KOhm

GND

+3VACC

D3002 @ 1N4148W

R3005 @ 1KOhm

D3003 @ 1N4148W

C3002 @ 0.1UF/10V c0402

BAT0_AD 29

Adaptor

A/D_DOCK_IN — **19V**

R3009 @ 20KOhm

AC_R_AD

R3012 @ 3.74KOhm

GND

+3VACC

D3001 @ 1N4148W

R3011 @ 1KOhm

D3004 @ 1N4148W

C3003 @ 0.1UF/10V c0402

AC_AD 29

3V — **2.99V**

Share Memory

+3VA_EC

R3010 10KOhm r0402

FA5/ SHBM — FA5/ SHBM 24,29

R3013 @ 10KOhm r0402

GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

+3VA_EC

R3001 @ 10KOhm r0402

FA4/ PPEN — FA4/ PPEN 24,29

R3014 10KOhm r0402

GND

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

+5VS — +5VS_TP — +5VSUS — +5V

C3004 0.01UF/25V

C3005 0.1UF/10V

GND

L3001 80Ohm/100Mhz

C3001 0.1UF/10V

GND

29 CRX

29 TPAD_DAT

29 TPAD_CLK

HDD_LED#

802_LED#_R

CHG_LED#_R

PWR_LED#_R

FPC_CON_15P — CON3001 — SIDE2 — SIDE1

Touchpad I/F

Touchpad

+3VS — +5VS

R3019 10KOhm

R3020 10KOhm

17 SATA_LED#

28 IDE_PDASP#

D3005

DAP202K

R3018 @ 0Ohm

HDD_LED#

HDD LED

CHARGE LED

+5VSUS

R3015 10KOhm

T3001

Q3001B UM6K1N

Q3001A UM6K1N

29 CHG_LED_UP#

CHG_LED#_R

GND

POWER LED

+5V

R3017 10KOhm

Q3002A UM6K1N

Q3002B UM6K1N

29 PWR_LED_UP#

PWR_LED#_R — PWR_LED#_R 38

GND

WLAN LED

19 WLAN_LED#

29,38 RF_LED

R3021 0Ohm

R3022 @ 0Ohm N/A

+5VS

R3016 10KOhm

Q3004A UM6K1N

Q3004B UM6K1N

802_LED#_R

GND

R1.2

<Variant Name>

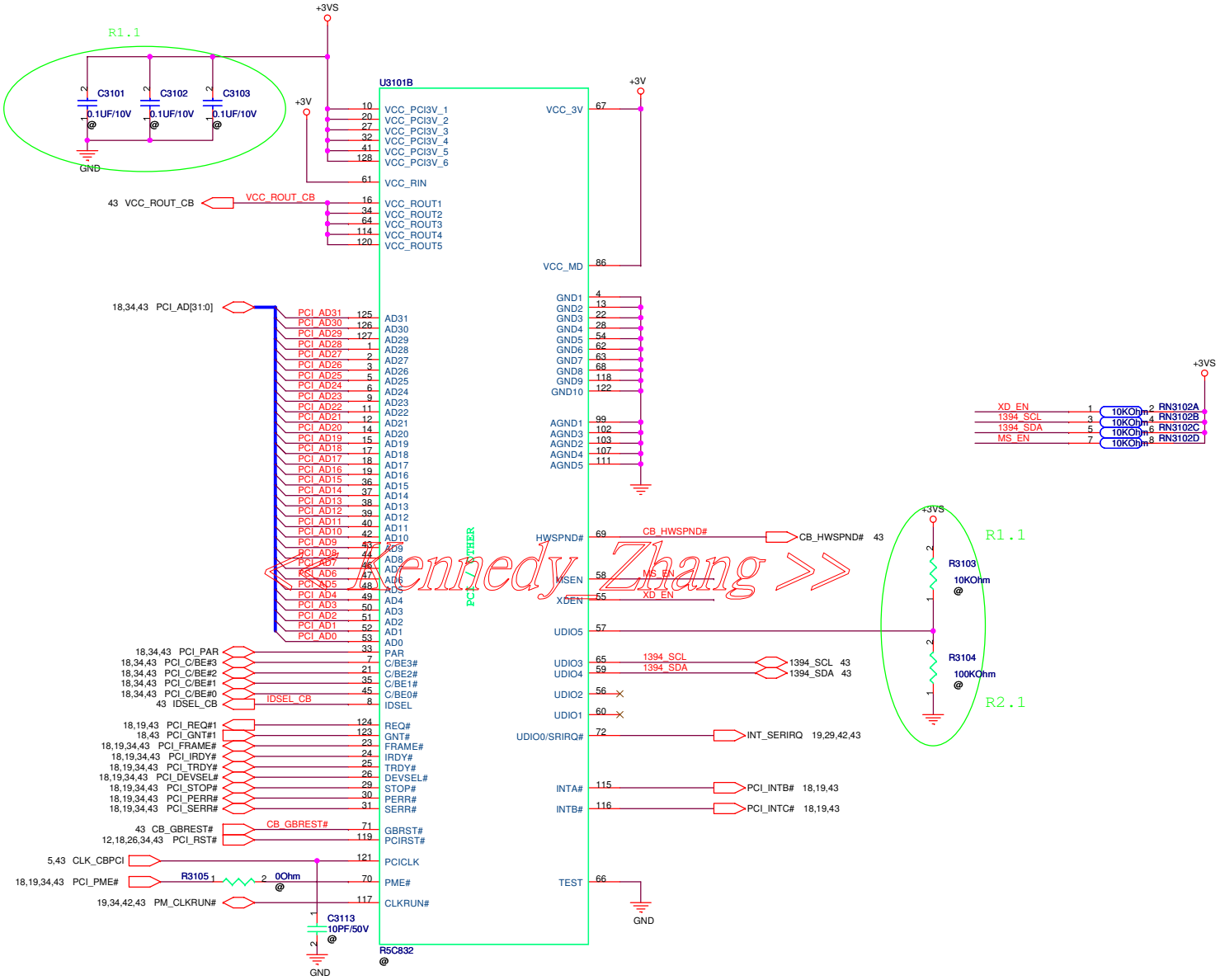
ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: Leon and George

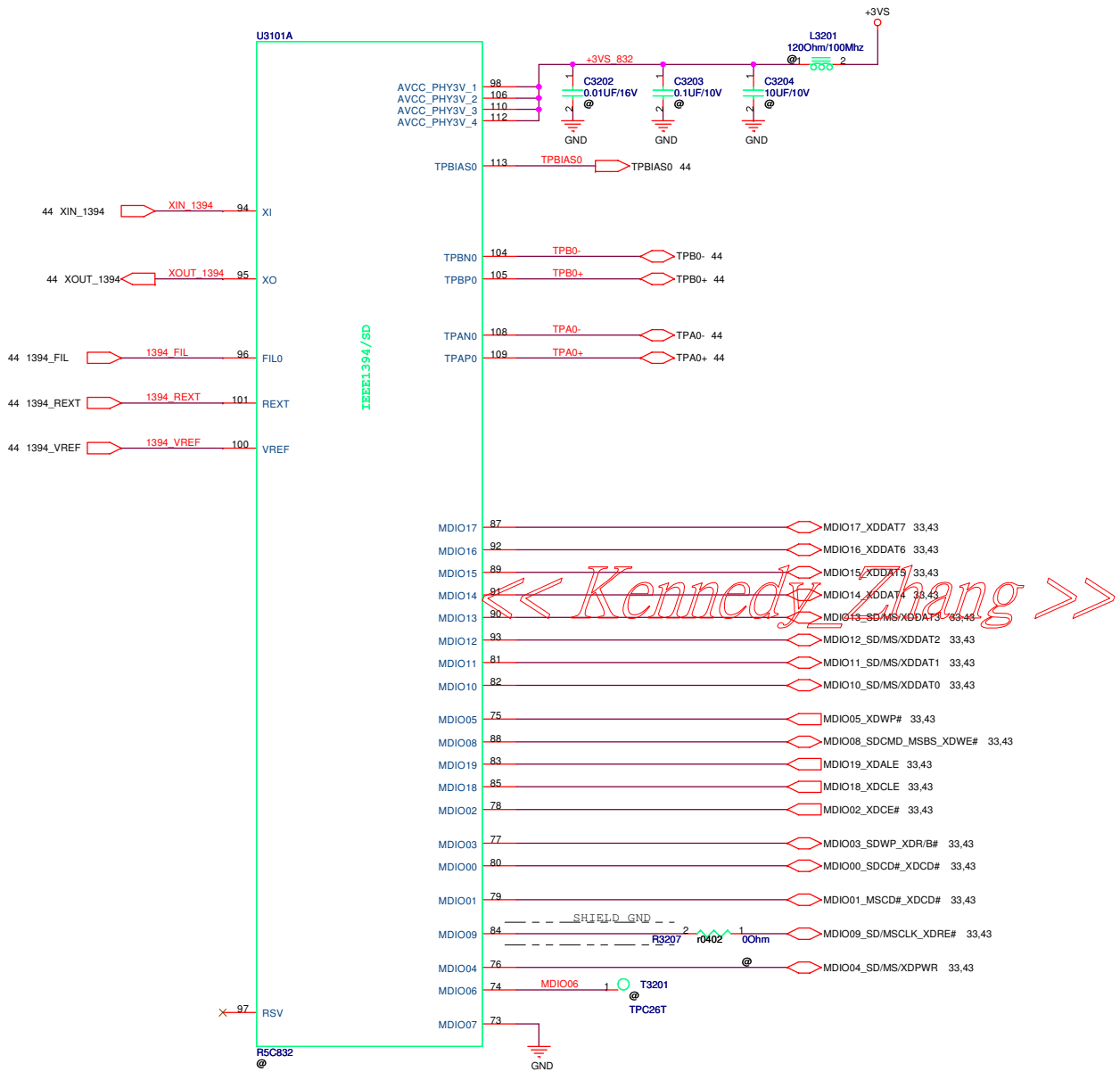
Size	Project Name	Rev
A3	T12F	

Date: 星期五, 五月 18, 2007 — Sheet 30 of 61



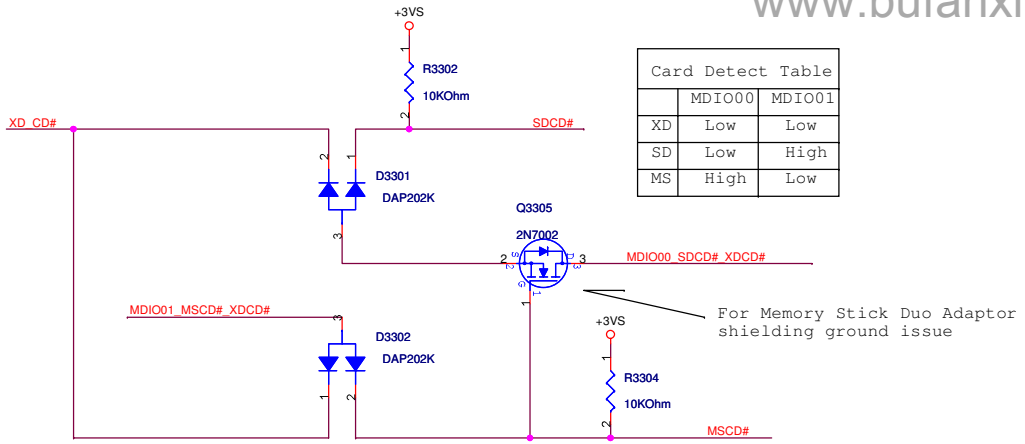
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(1)	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期五, 五月 18, 2007	Sheet 31 of 61	



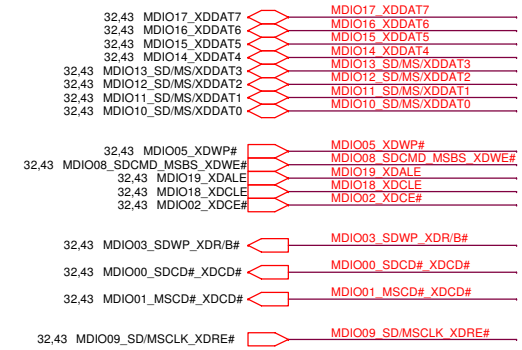
<Variant Name>

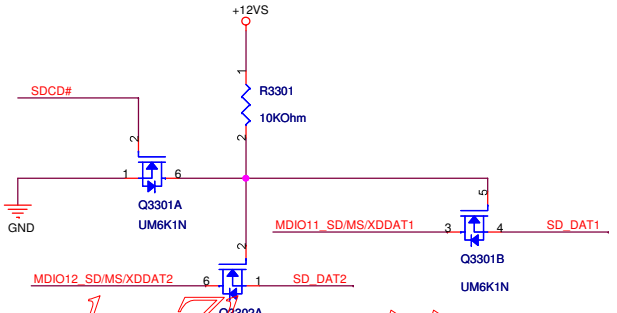
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 32 of 61	



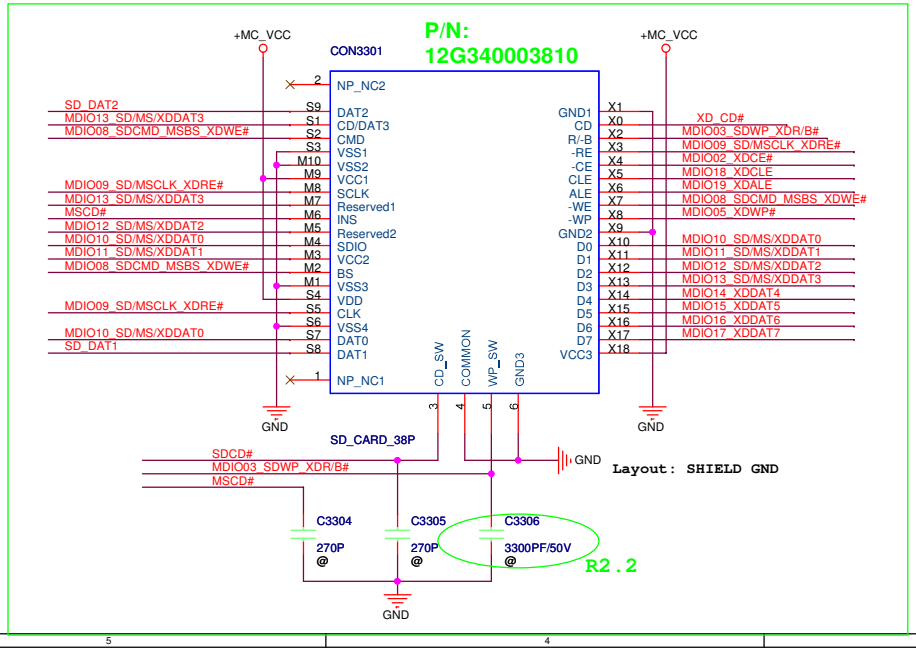
Card Detect Table		
	MDIO000	MDIO001
XD	Low	Low
SD	Low	High
MS	High	Low

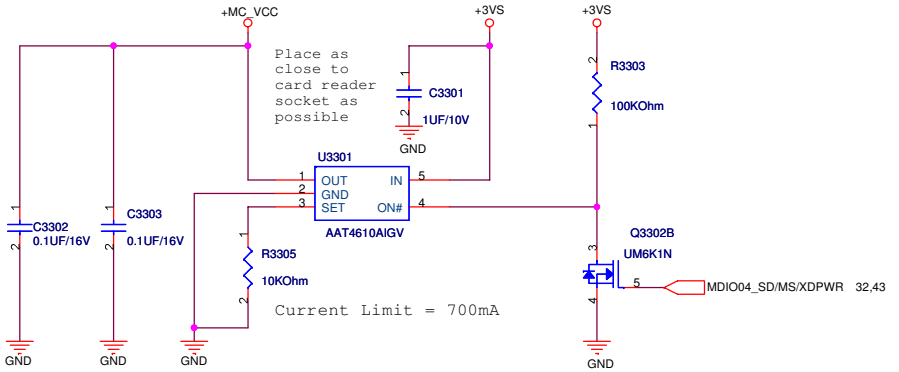
Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU





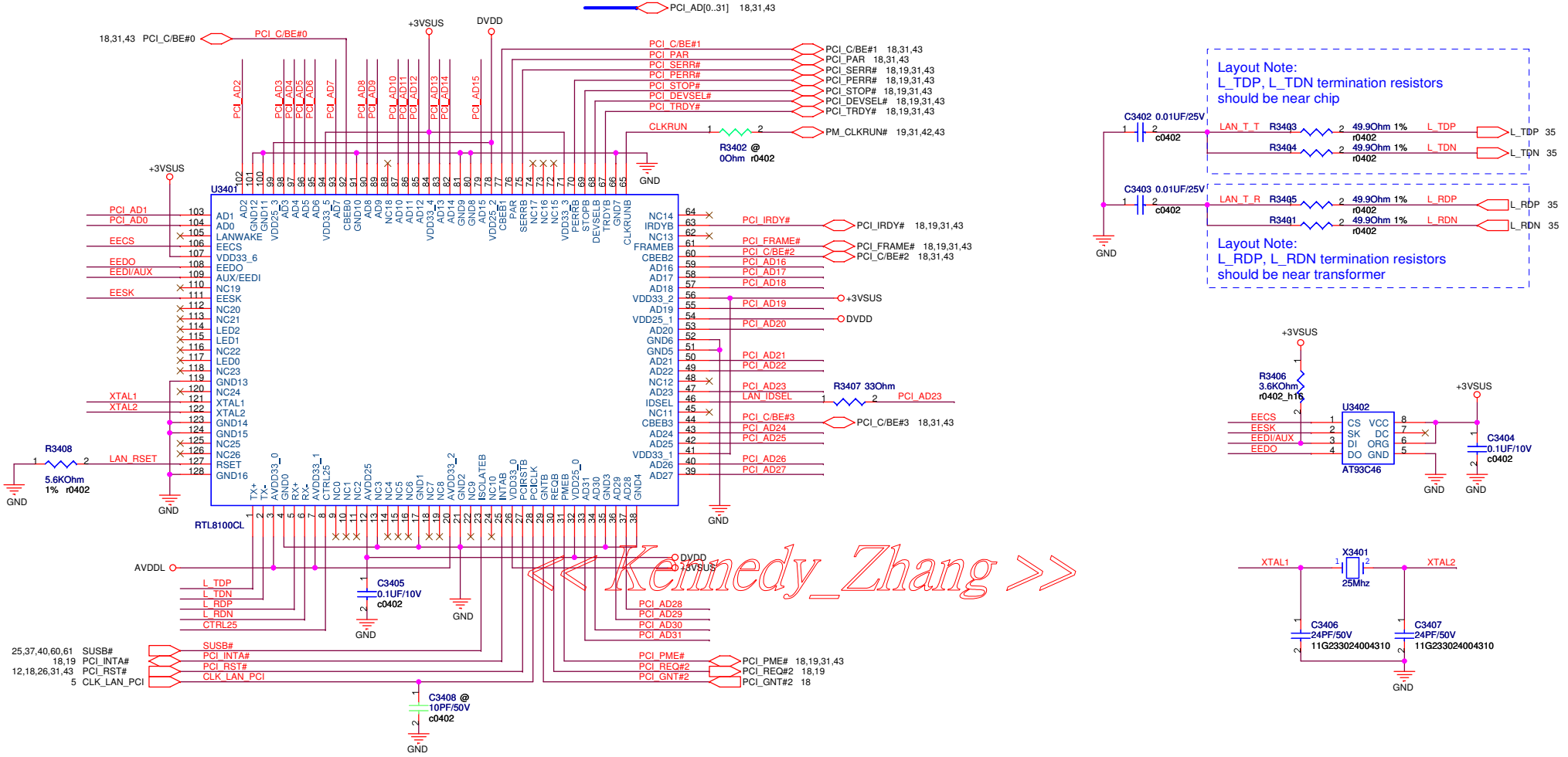
R2.3





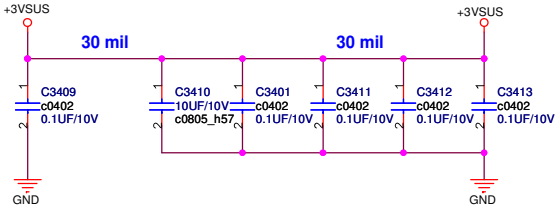
<Variant Name>

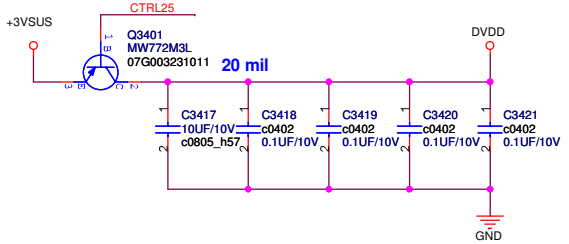
Title	4 in 1 CARD READER		
ASUSTeK COMPUTER INC	Engineer:	Leon and George	
Size: A3	Project Name: T12F		Rev
Date: 星期五, 五月 25, 2007	Sheet 33 of 61		

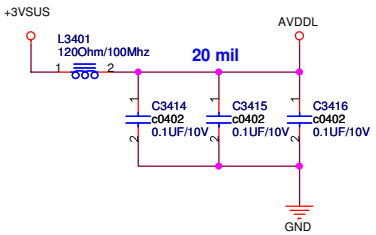


Layout Note:
L_TDP, L_TDN termination resistors
should be near chip

Layout Note:
L_RDP, L_RDN termination resistors
should be near transformer



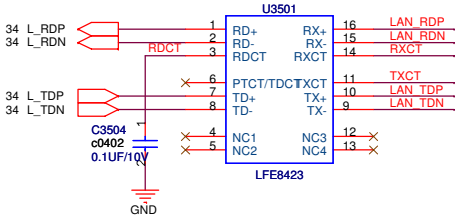


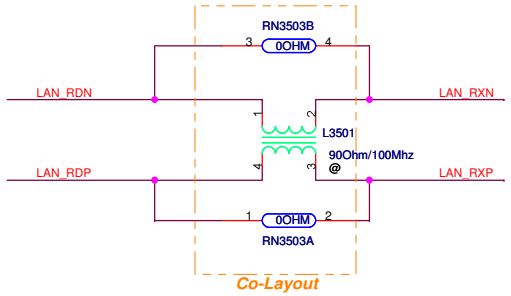


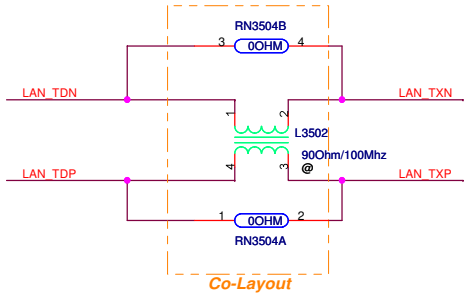
<Variant Name>

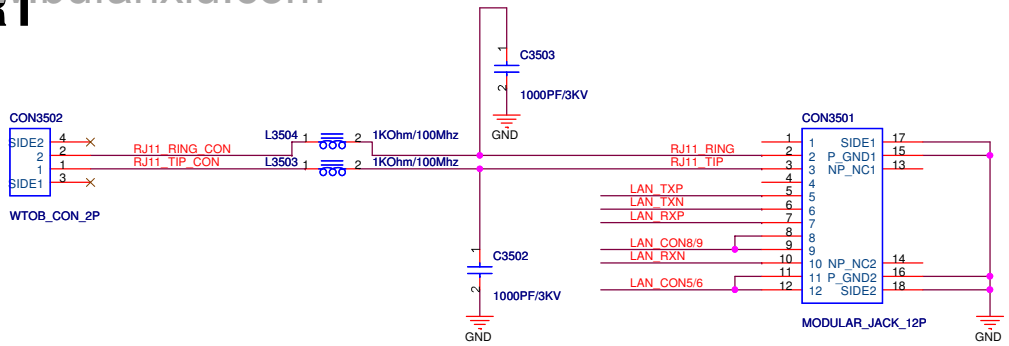
ASUSTeK COMPUTER INC	Title : LAN_RTL8100CL	
	Engineer: Leon and George	
Size: A3	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 34 of 61	

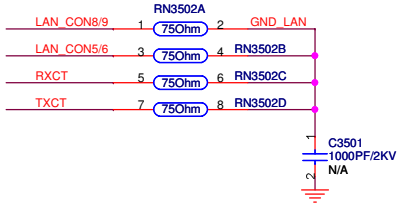
LAN PORT





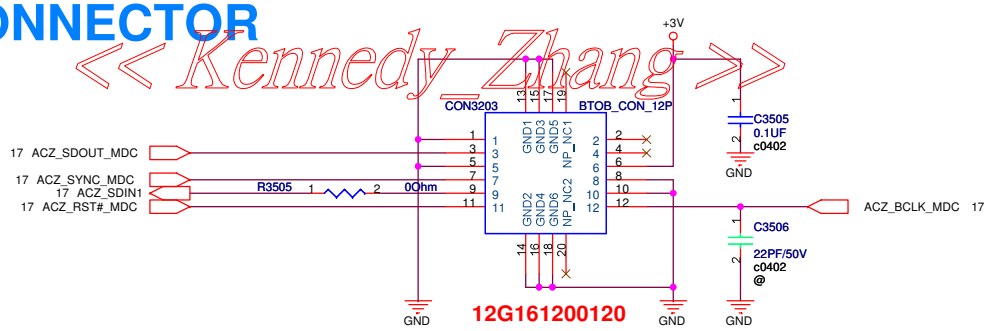


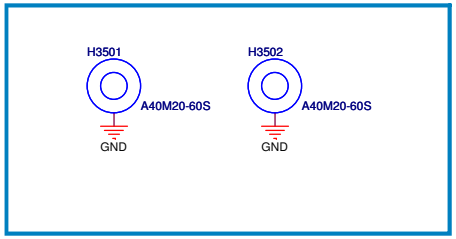




R1.2

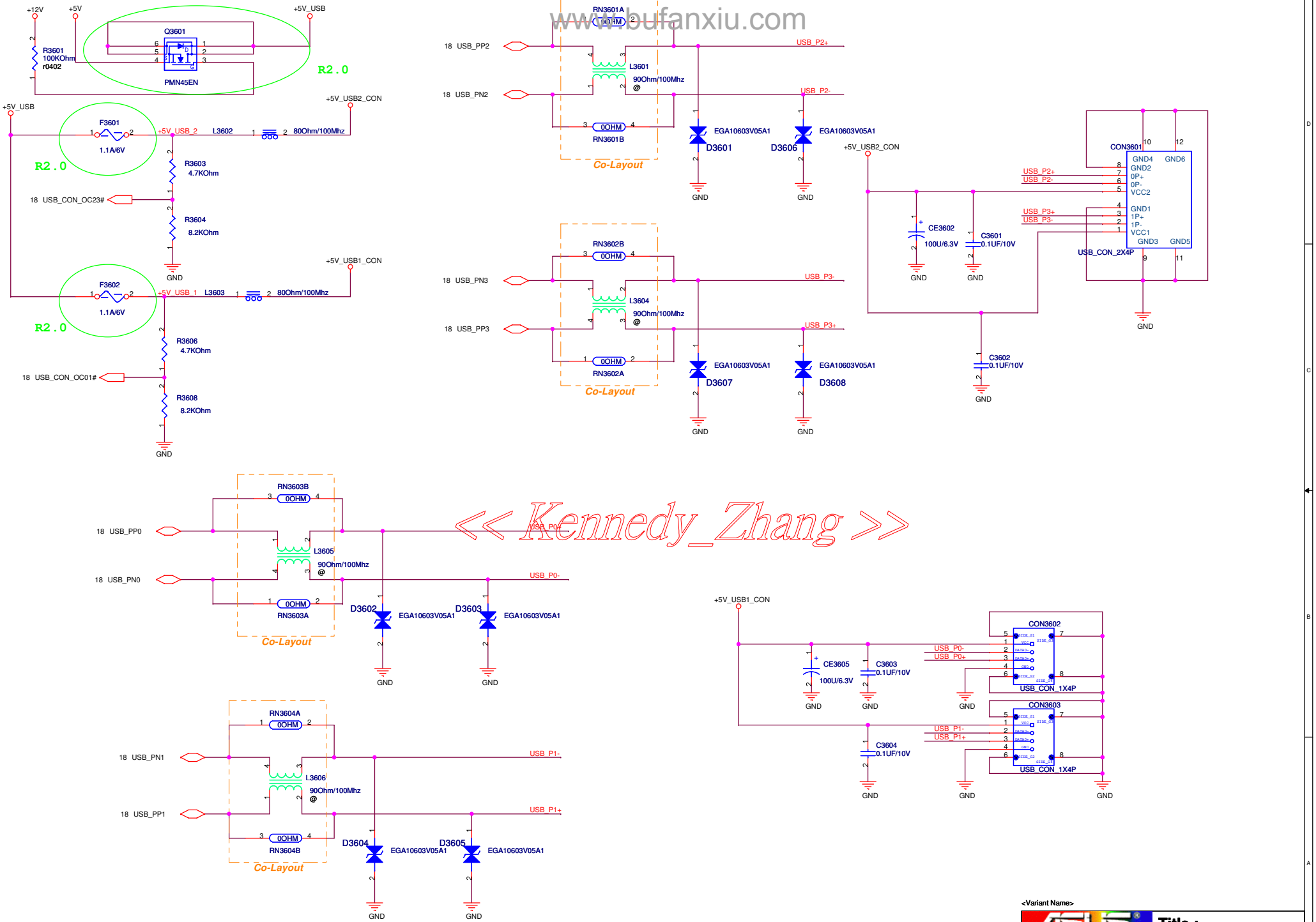
MDC CONNECTOR





<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: Leon and George	
Size: Custom	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 35 of 61	



<Variant Name>

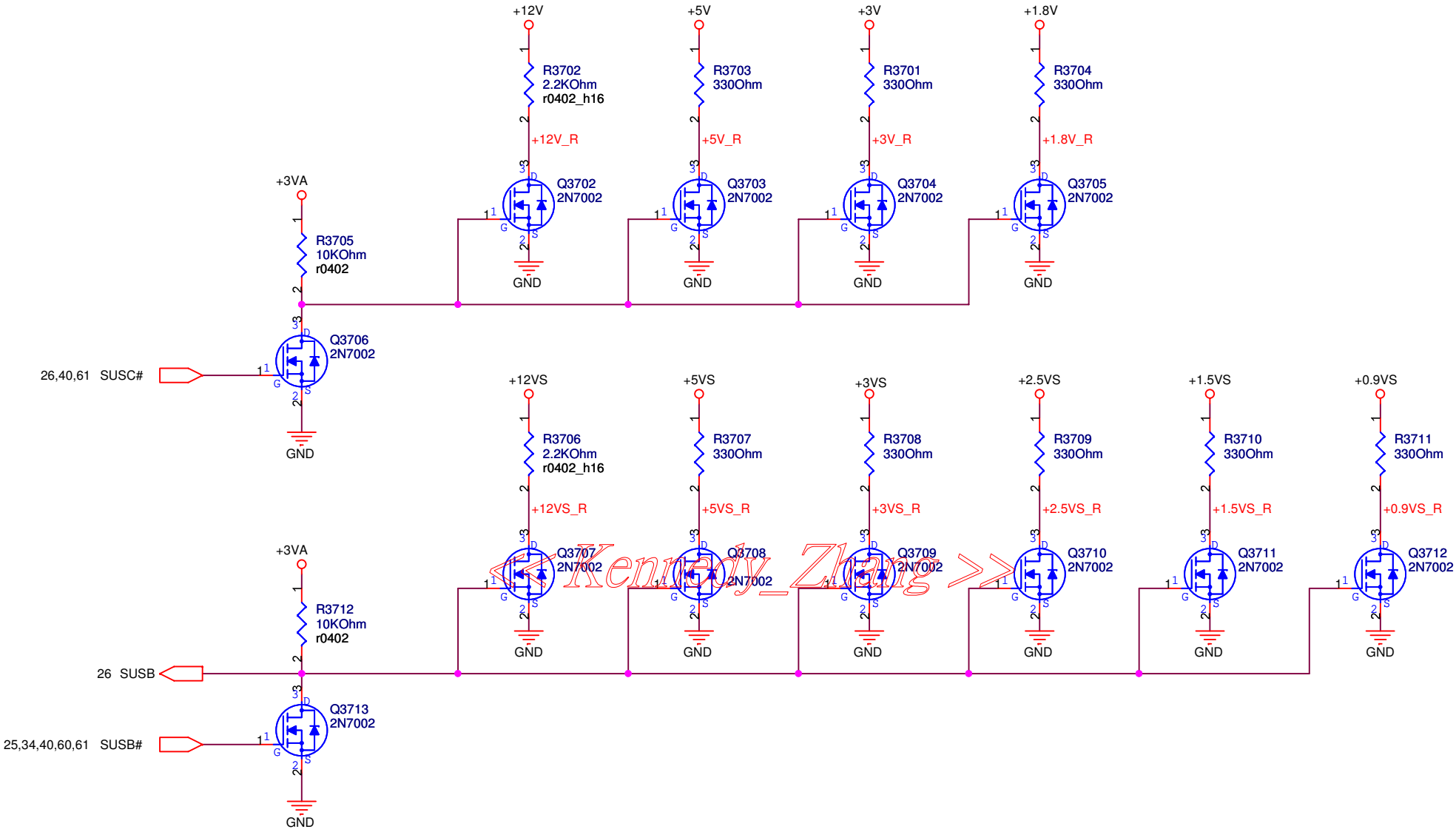
Title : USB CONN x4

ASUSTeK COMPUTER INC. NB1

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

Date: 星期二, 五月 15, 2007 Sheet 36 of 61



<Variant Name>

ASUSTeK COMPUTER INC

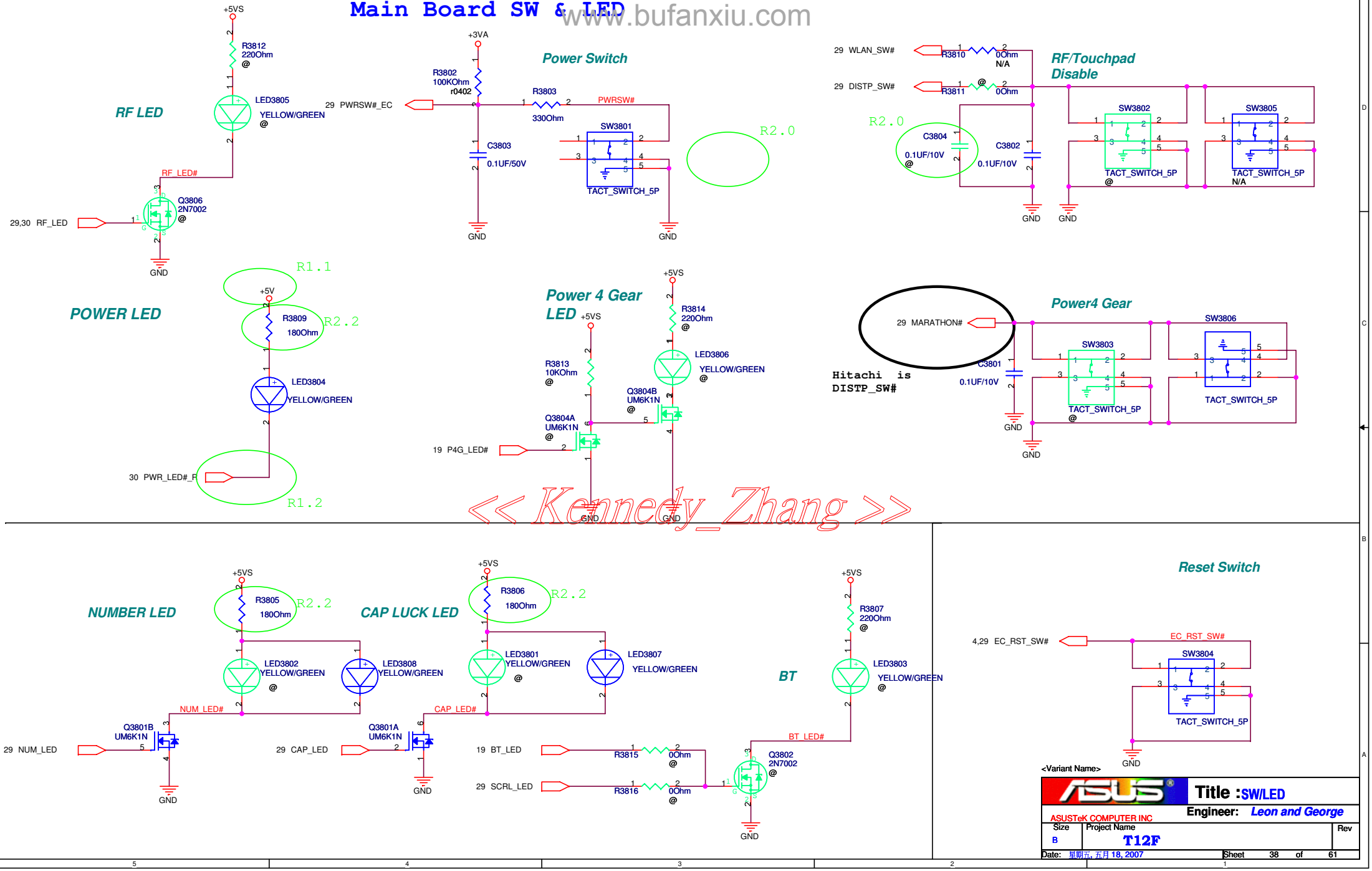
Title : Discharge Circuit

Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: 星期二, 五月 15, 2007 Sheet 37 of 61

Main Board SW & LED



<Variant Name>

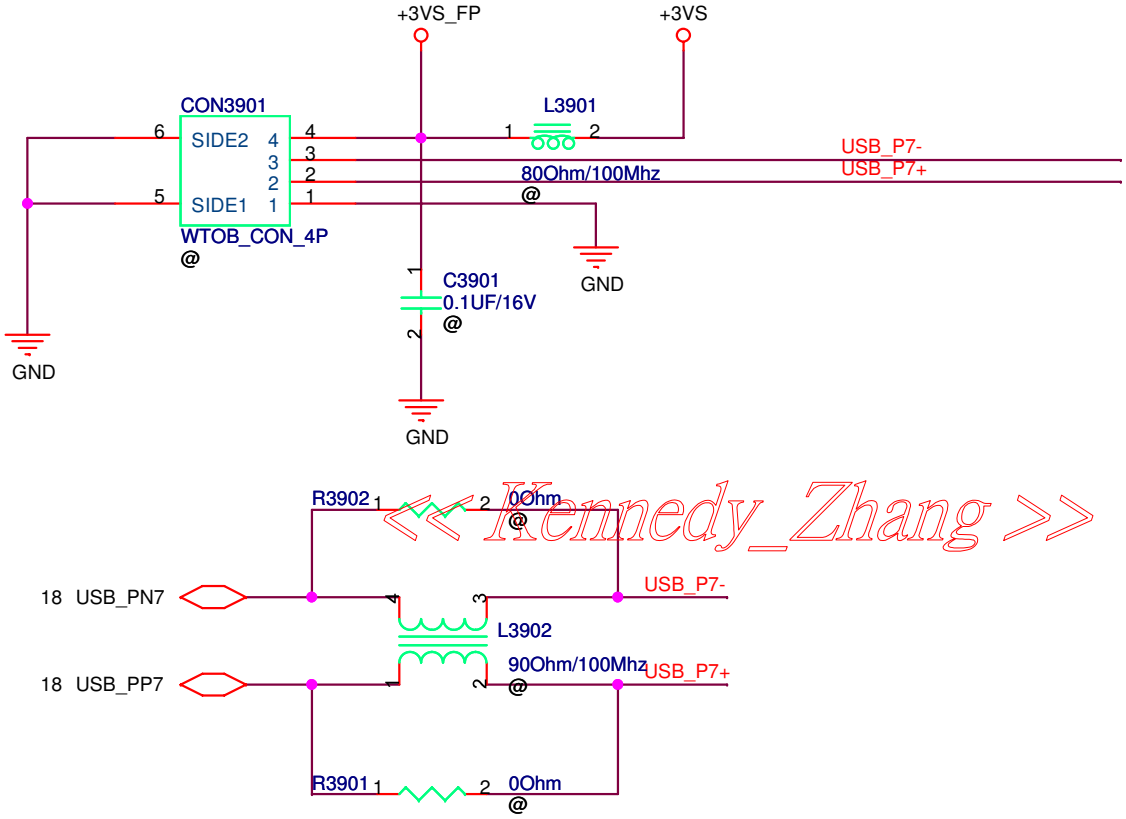
ASUSTeK COMPUTER INC

Title : SW/LED

Engineer: Leon and George

Size	Project Name	Rev
B	T12F	

Date: 星期五, 五月 18, 2007 Sheet 38 of 61



<Variant Name>

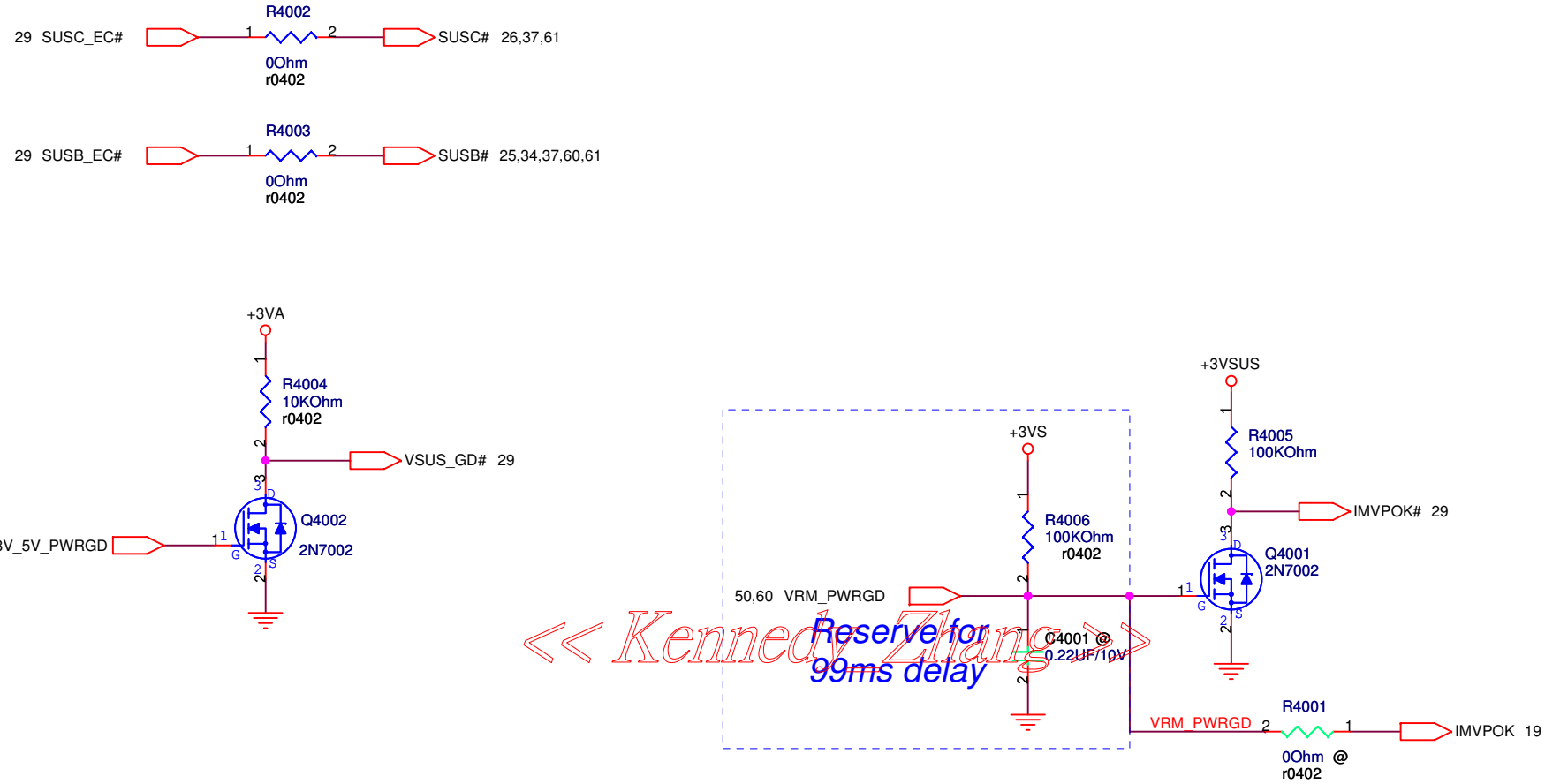
ASUSTeK COMPUTER INC

Title : FINGER PRINT

Engineer: Leon and George

Size	Project Name	Rev
A	T12F	

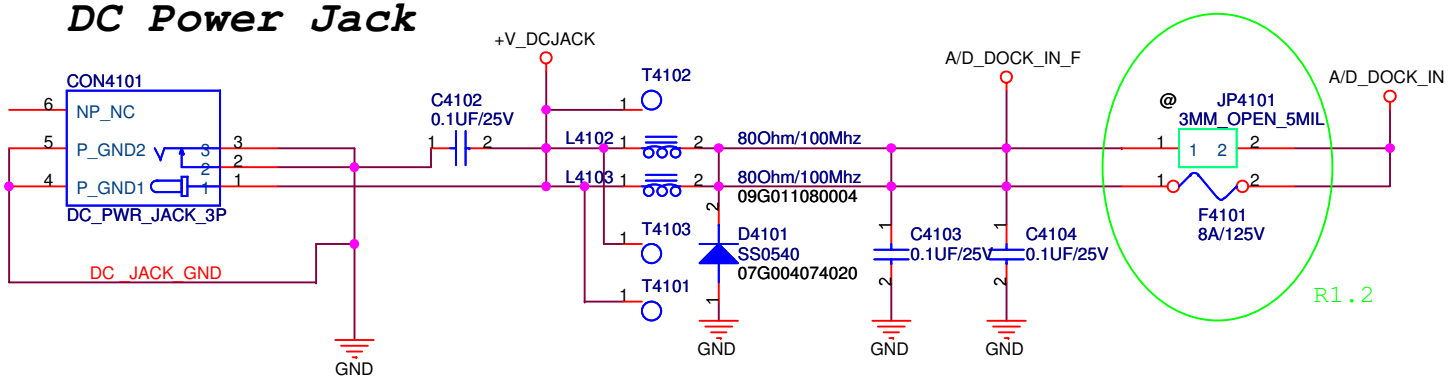
Date: 星期二, 五月 15, 2007 Sheet 39 of 61



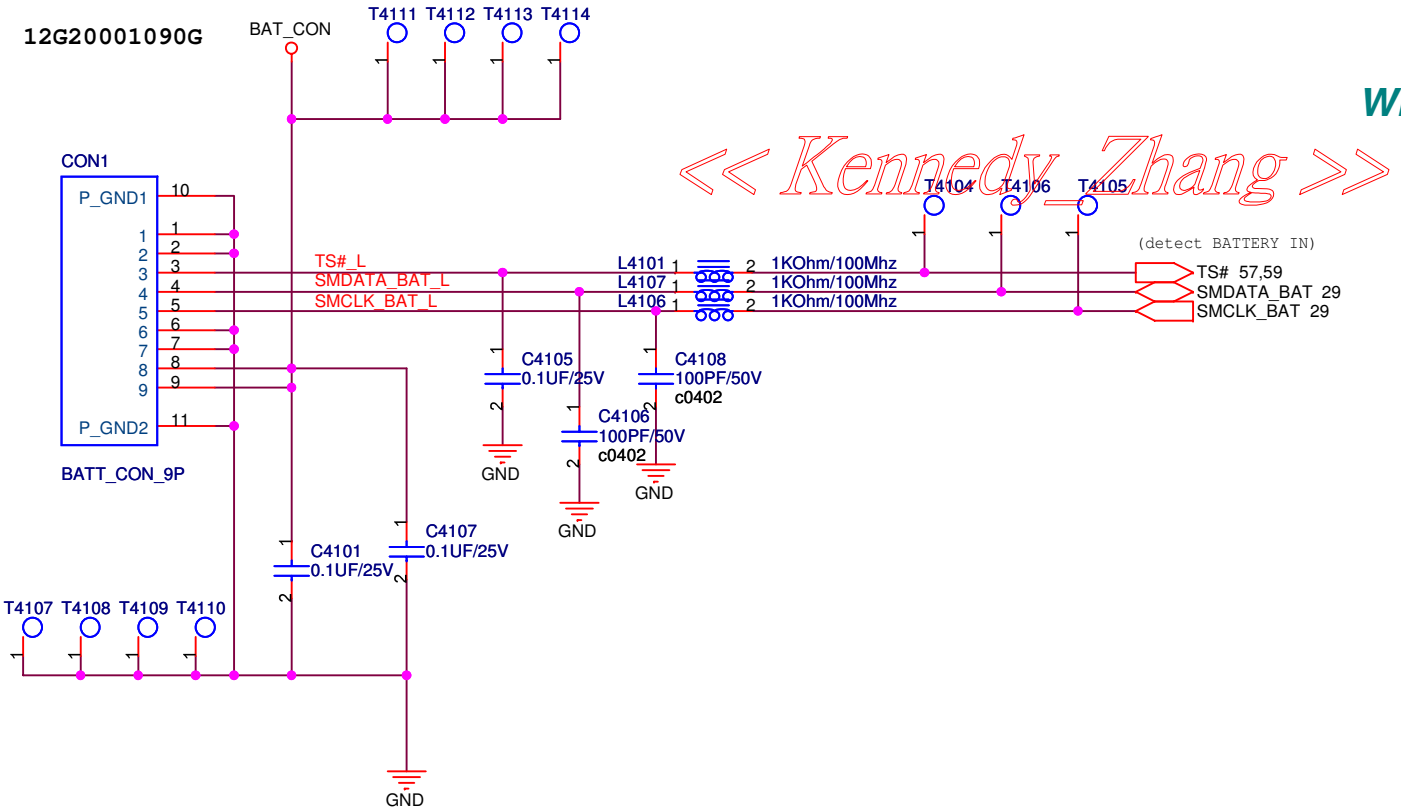
<Variant Name>

ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: Leon and George	
Size: A4	Project Name: T12F	Rev
Date: 星期二, 五月 15, 2007	Sheet 40 of 61	

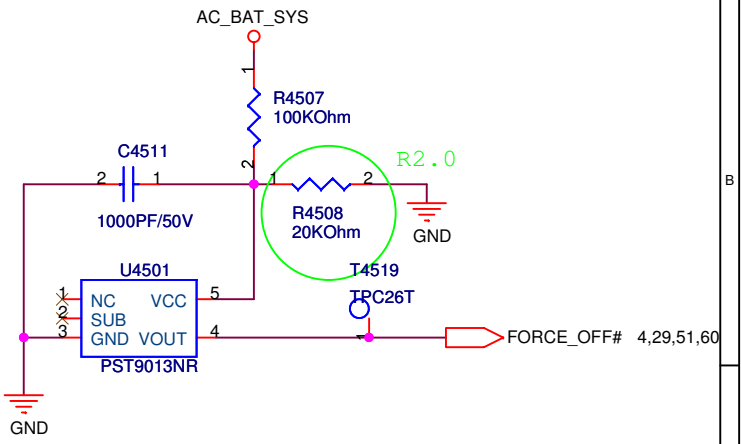
DC Power Jack



12G20001090G



Without Battery & Pull out Adapter



<Variant Name>

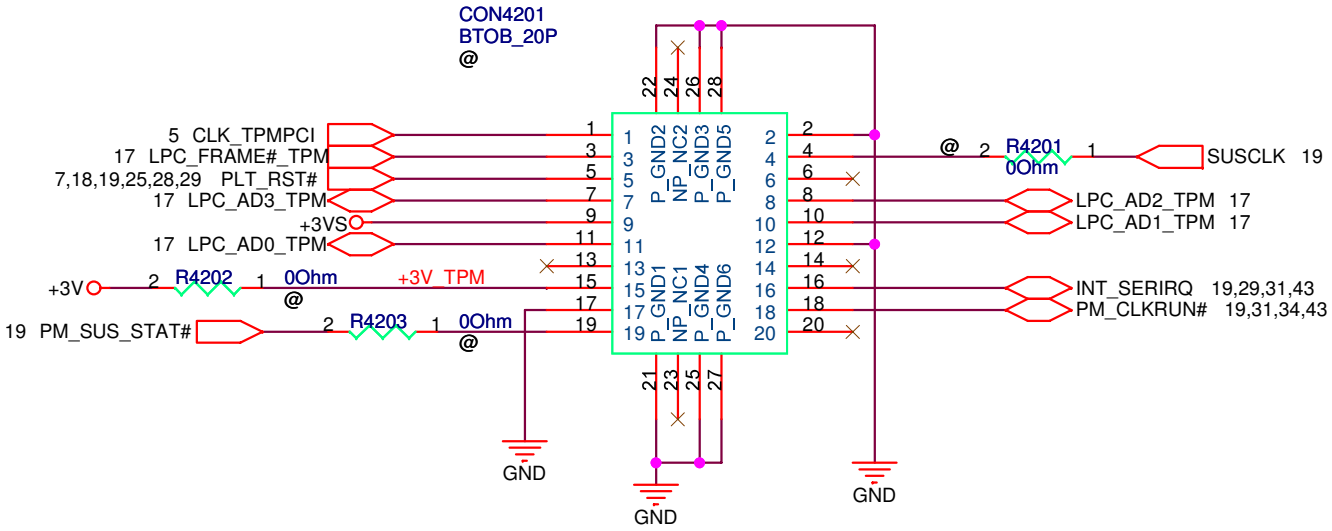
ASUSTeK COMPUTER INC

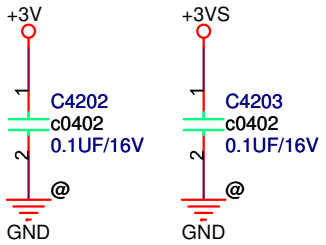
Title : DC/ BATT IN

Engineer: Leon and George

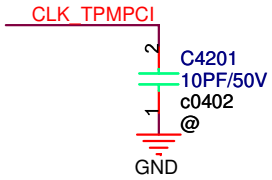
Size	Project Name	Rev
A4	T12F	

Date: 星期二, 五月 15, 2007 Sheet 41 of 61





TPM Module CON



<Variant Name>

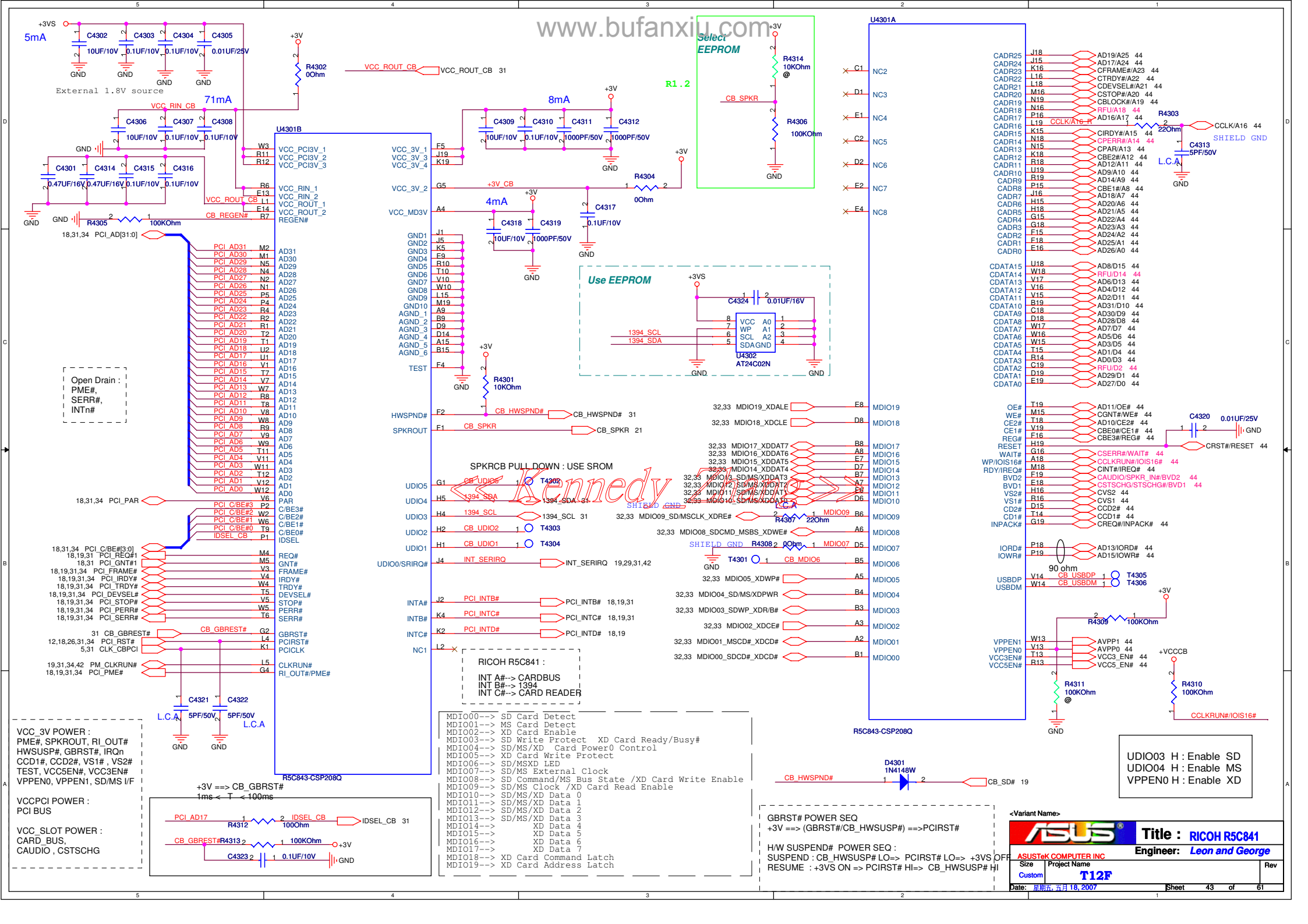
ASUSTeK COMPUTER INC

Title : TPM

Engineer: ~

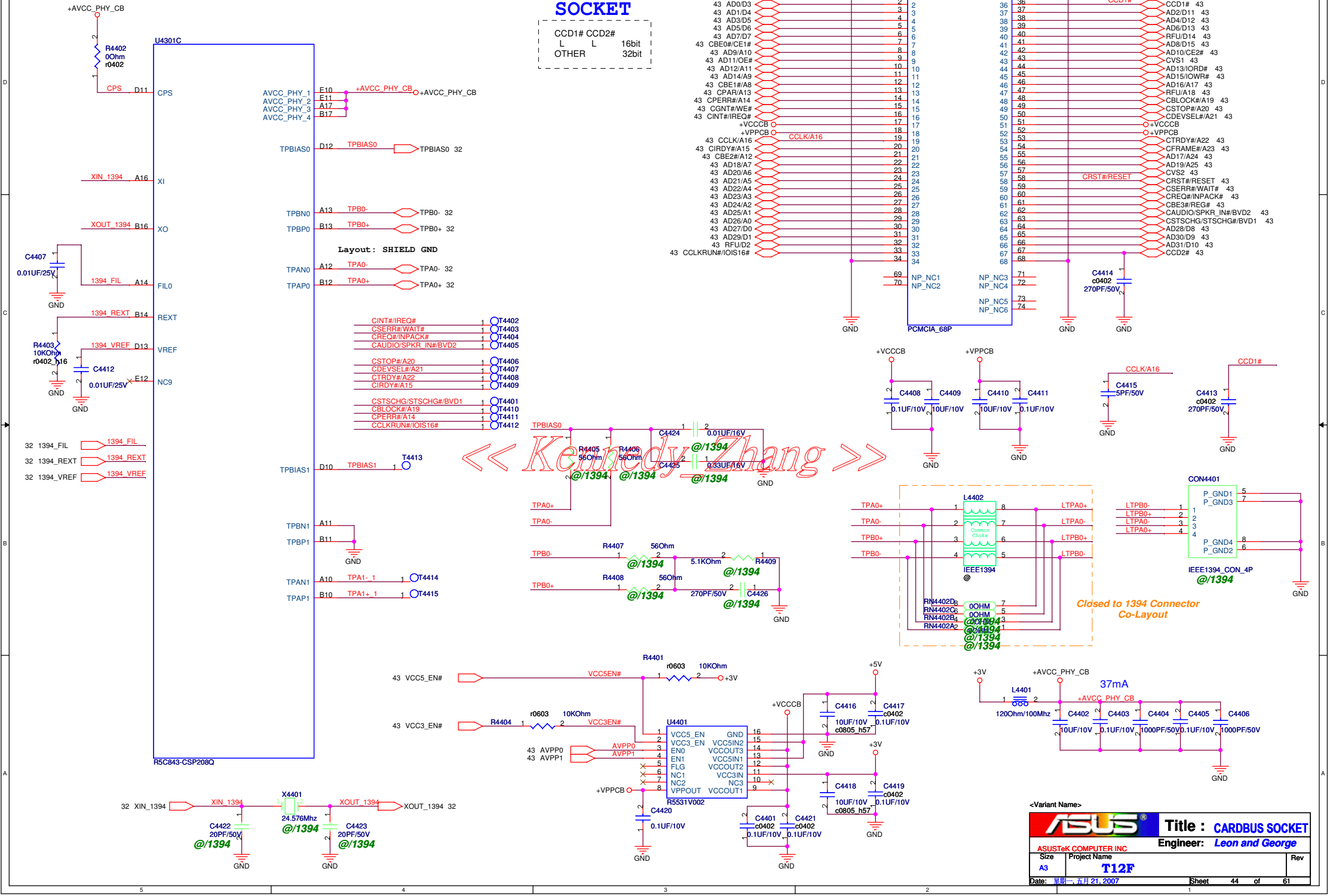
Size	Project Name	Rev
A	T12F	

Date: 星期二, 五月 15, 2007 Sheet 42 of 61



PCMCIA SOCKET

CCD1# CCD2#
L L 16bit
OTHER 32bit



ASUSTeK COMPUTER INC
Engineer: Leon and George

Title : CARDBUS SOCKET

Size	Project Name	Rev
A3	T12F	

Date: 星期一, 五月 21, 2007 Sheet 44 of 61

<Variant Name>

ABCDH

H4501 R335X335D91N
H4502 R335X335D91N
H4503 R335X335D91N
H4504 R335X335D91N
H4505 R335X335D91N
H4506 R335X335D91N
H4507 R335X335D91N
H4508 R335X335D91N
H4509 RT492X335SB335D91N
H4510 R335X335D91N
H4511 R335X335D91N
GND
GND

E

H4512 OT276X354RB315D91N
H4513 OT276X354RB315D91N
GND

F

H4514 CT271B177D138
H4515 CT271B177D138
H4516 CT271B177D138
H4517 CT271B177D138
GND

固定孔

H4518 C83D83N
H4519 O98X83DO98X83N N/A

I

H4520 A40M20-60S N/A
GND

G

H4521 T12F
H4522 E40M20-251630AS
GND

<Variant Name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: Leon and George

Size	Project Name	Rev
A4	T12F	

Date: 星期五, 五月 18, 2007 Sheet 45 of 61

R1.1

Page	Action	Reason
5	Add R566,R567,R568,R569 to divide voltage.	Clock GEN output voltage is too high.
17	Add R1733~R1737 (Reserve)	For EMI request
17	Add R1729~R1732	Add MDC feature
22	Change C2222 from 0.1uF to 0.47uF	Delay the HP turn-on timing to avoid noise at the system power on.
22	Add R2233 and L2202 to link the different GND	For EMI request
26	Add CON2603	Only use for debug, it will be deleted before MP
31	Add C3101~C3103	Reduce power rippler of R5C832
31	Add R3103	UDIO5 pull high to disable external EEPROM
35	Add CON3203 and MDC relative circuit	Add MDC feature
38	Change power LED power from +5VS to +5V	Slove LED can't flash in S3

R1.2

Page	Action	Reason
4	Add U402 and relative circuit.	Add hardware thermal protection circuit
12	Change L1204,L1205,C1209,1210	For EMI request
12	Change L1210 to 1k ohm	Reduce leakage current.
13	Change L1304~L1306 to 150nH and C1308 C1310 C1312 change to 10pF	Improve CRT signal
21	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
22	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
23	All R1.2 modification in this page	Improve microphone quality
30	Add R3022	Reserve RF_LED feature
38	Del Q3005 and link PWR_LED#_R to LED directly	Cost down
41	Add F4101 and JP4101	Reserve, normal use JP4101
43	Add R4314	Reserve, normal no use

R2.0

Page	Action	Reason
5	Change C516,C517 value	Tune up accuracy of 14.318MHz.
17	Change C1702,C1703 value	Tune up accuracy of 32.768KHz.
21	Add R2111 to pull high	Avoid input pin NC.
29	Change C2911,C2915 value	Tune up accuracy of 32.768KHz.
36	Modify Q3601 circuit	Solve system will auto turn-on when remove USB HDD with external power.
38	Add C3804	For ESD request
41	Change R4508 from 16.9K to 20K ohm	Solve shutdown issue when plug-in AC jack in low battery mode.
10	Add CE1003	Reduce power rippler of +1.8V

R2.2

Page	Action	Reason
29	Add R2918 and change C2910 to 0.1uF	Solve CMOS clear issue.
33	Add C3306	Solve Type-H XD can't work normally.
38	Change R3805,R3806,R3809 to 180ohm(1/10W)	Improve Derating

R2.3

Page	Action	Reason
33	Change CON3301 to ALPS	Prevent card from being shaved by connector

<Variant Name>

ASUSTeK COMPUTER INC

Title : HISTORY

Engineer: Leon and George

Size	Project Name	Rev
A3	T12F	

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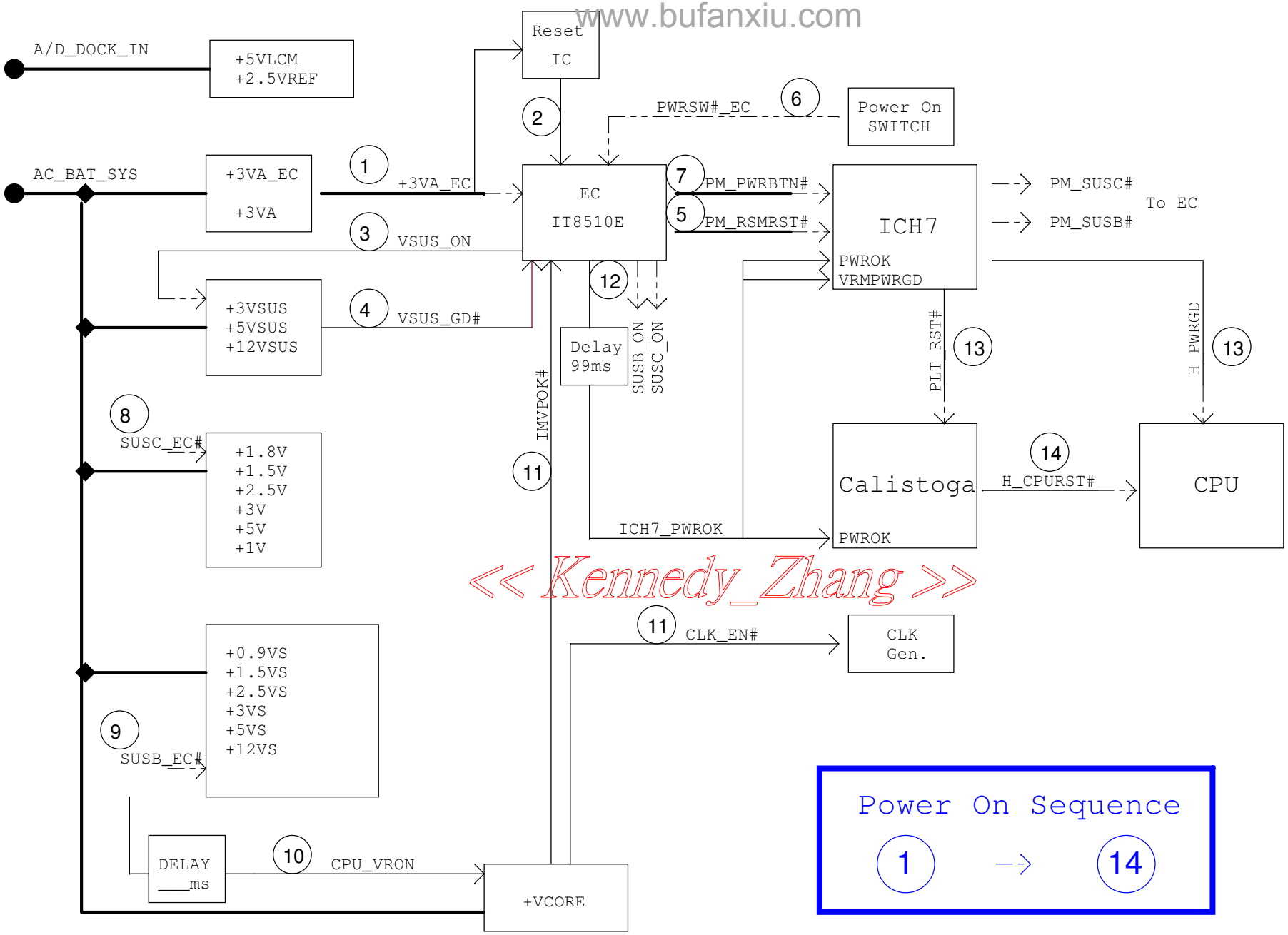

<Variant Name>

Title : FLOWCHART

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	

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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM		48	GPH0	VSUS_ON	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/		55	GPH2	IMVPOK#	I
37	PWM3/GPA3	/		69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#		76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH7_PWROK	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCH_DOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RC_IN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O				
				8	GPL0	WLAN_ON#	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	11	GPL1	BT_ON#	O
170	SMDAT1/GPC2	SMB1_DAT	I/0	12	GPL2	RF_OFF_SW#	I
171	GPC3	/		20	GPL3	RF_LED	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	92	CRX	CRX	I/0
175	GPC5	OP_SD#	O				
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RI1#/WUI0/GPD0	PM_SUSB#	I				
29	RI2#/WUI1/GPD1	PM_SUSC#	I				
30	LPCRST#/WUI4//GPD2	PLT_RST#	I				
31	ECSCI#/GPD3	EXT_SCI#	O				
41	GPD4		I				
42	GINT/GPD5	/					
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#	I				
88	ADC5/GPE1	/	I				
89	ADC6/GPE2	MARATHON#	I				
90	ADC7/GPE3	DISTP_SW#	I				
2	PWRSW/GPE4	PWRSW#_EC	I				
44	WUI5/GPE5	/					
24	LPCPD#/WUI6/GPE6	LID_EC#	I				
25	CLKRUN#/WUI7/GPE7		O				
110	PS2CLK0/GPF0	/					
111	PS2DAT0/GPF1	/					
114	PS2CLK1/GPF2	/	I/0				
115	PS2DAT1/GPF3	/	I/0				
116	PS2CLK2/GPF4	TP_CLK					
117	PS2DAT2/GPF5	TP_DAT					
118	PS2CLK3/GPF6	PWRLMT#					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	O
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

Title : GPIO Setting

ASUSTeK COMPUTER INC

Engineer: Leon and George

Size	Project Name	Rev
Custom	T12F	

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<Variant Name>

Title : N/A

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12F	

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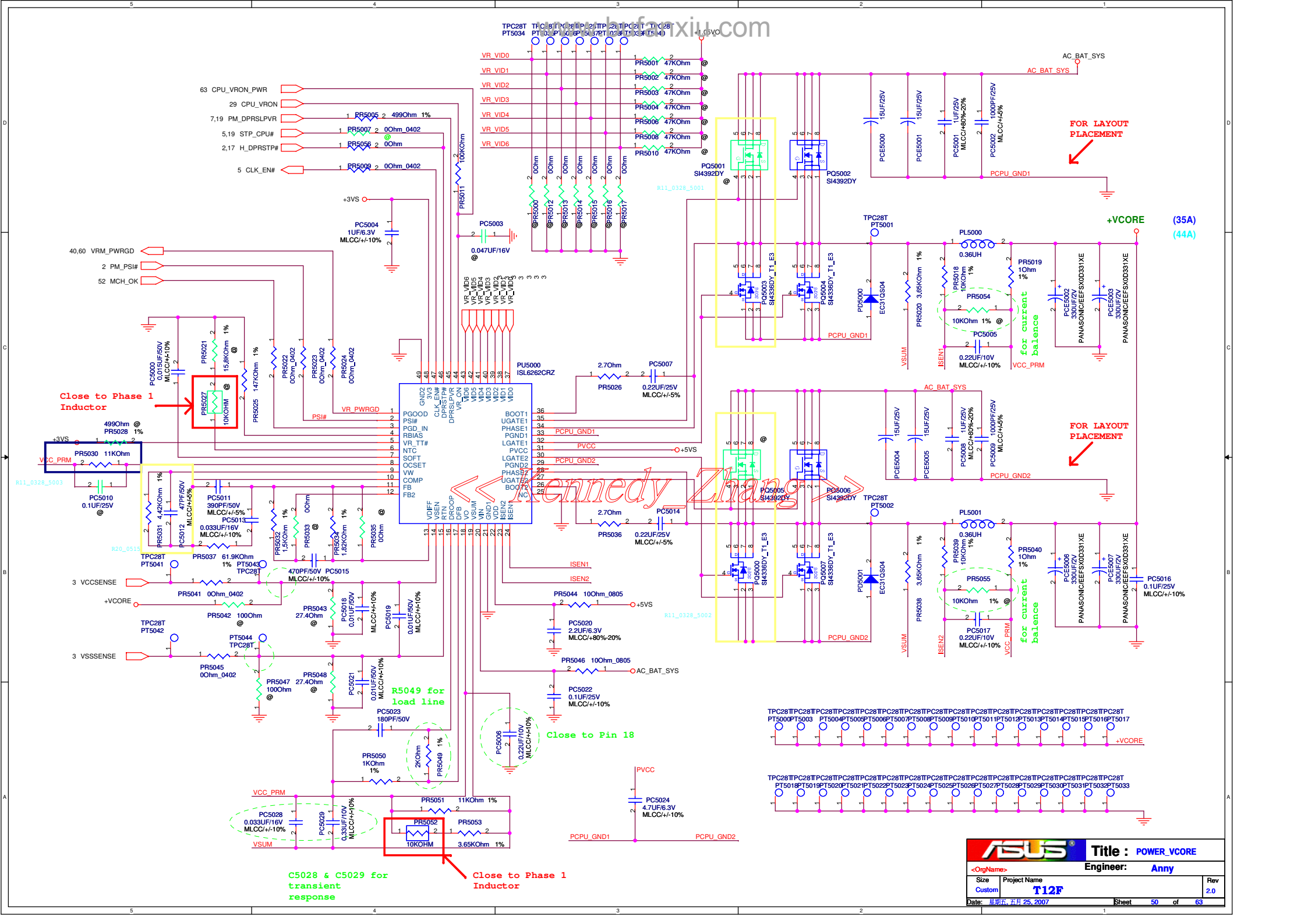
www.bufanxiu.com
<Kennedy Zhang>
+VCORE (35A) (44A)
Close to Phase 1 Inductor
Close to Phase 1 Inductor
Close to Pin 18
C5028 & C5029 for transient response
R5049 for load line
FOR LAYOUT PLACEMENT
FOR LAYOUT PLACEMENT
for current balence
for current balence
PU5000 ISL6262CRZ
Title : POWER_VCORE
Engineer: Anny
Project Name T12F
Size Custom
Rev 2.0
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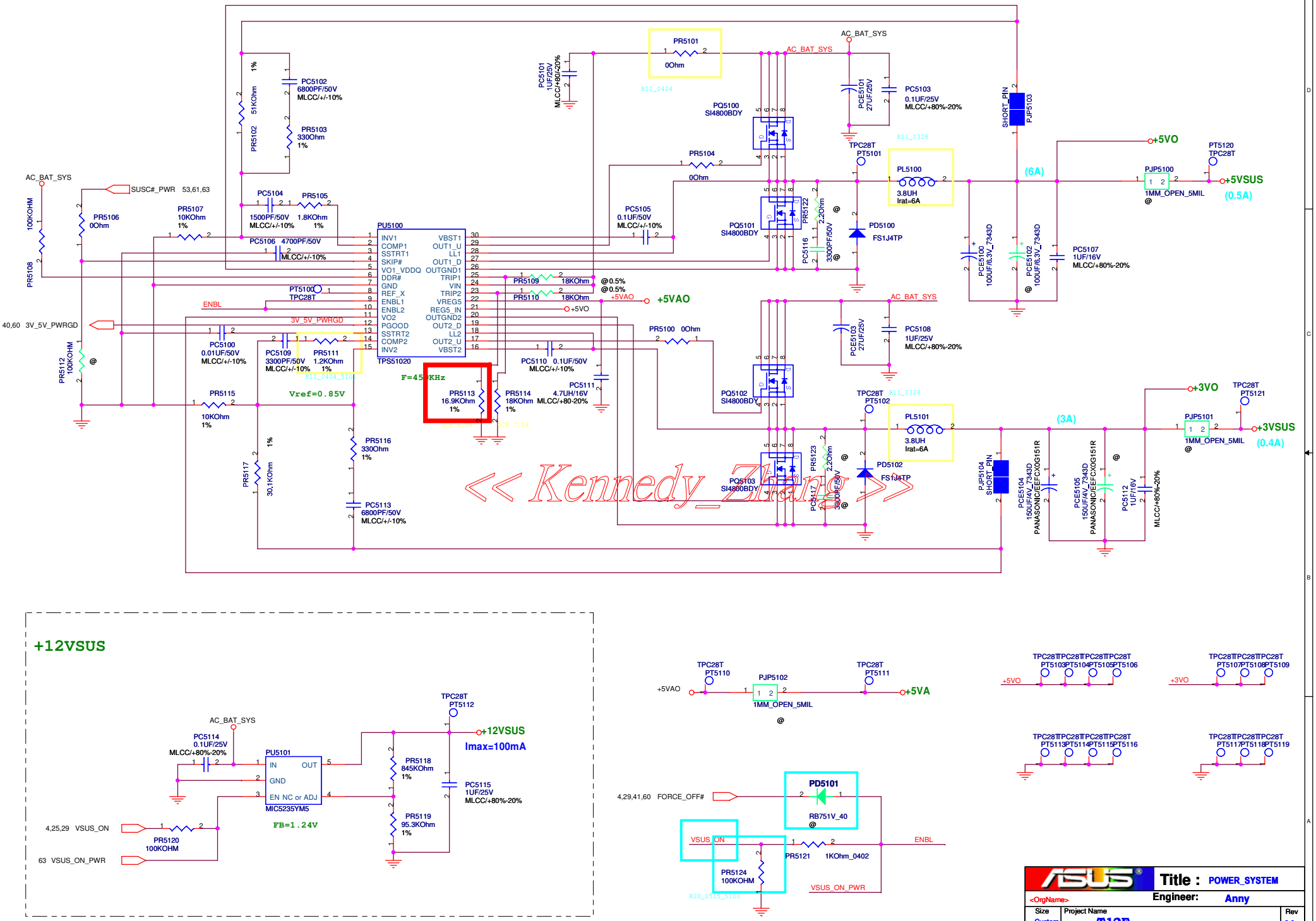

ASUS

Title : POWER_SYSTEM

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12F	2.0

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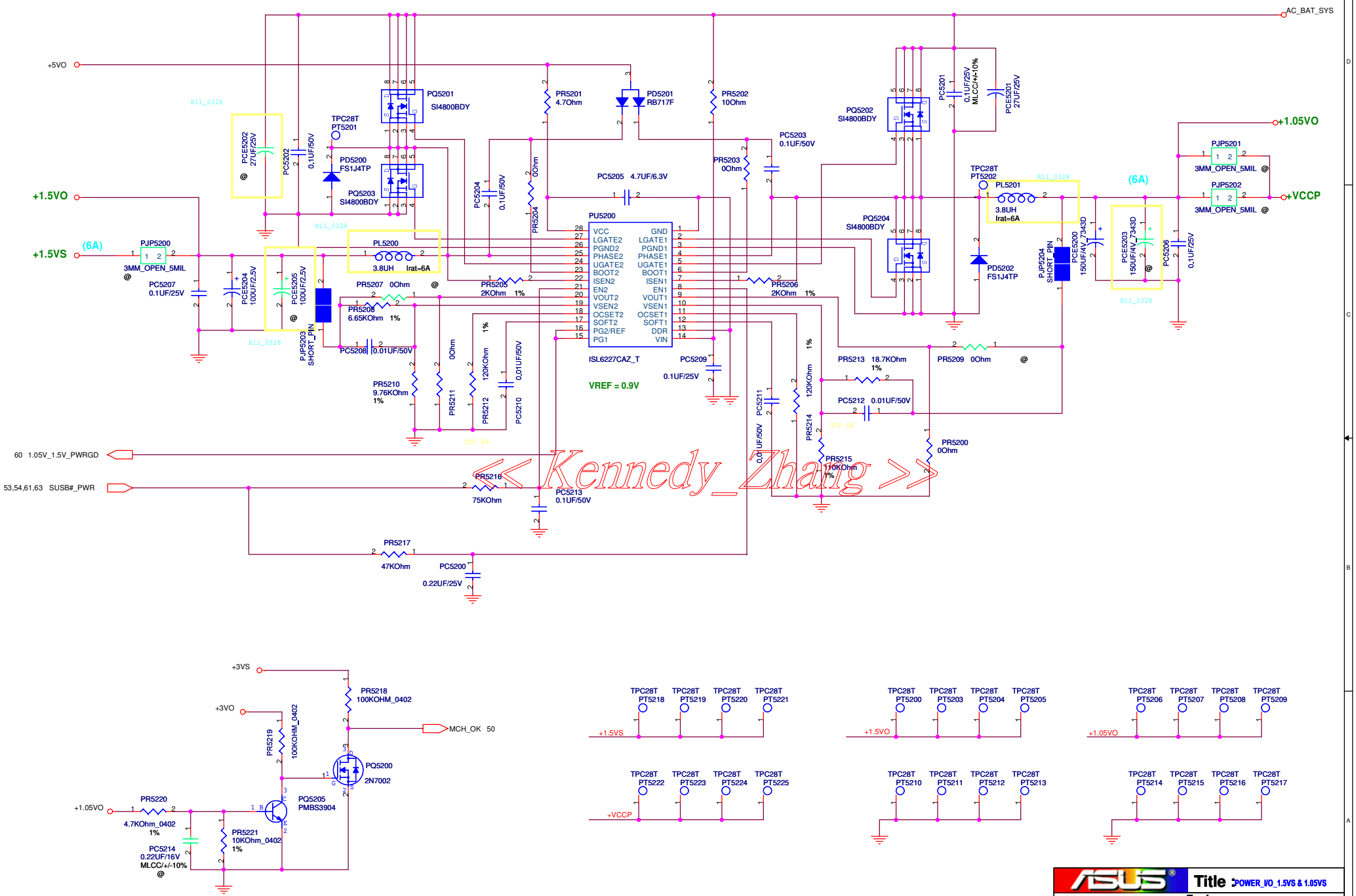

ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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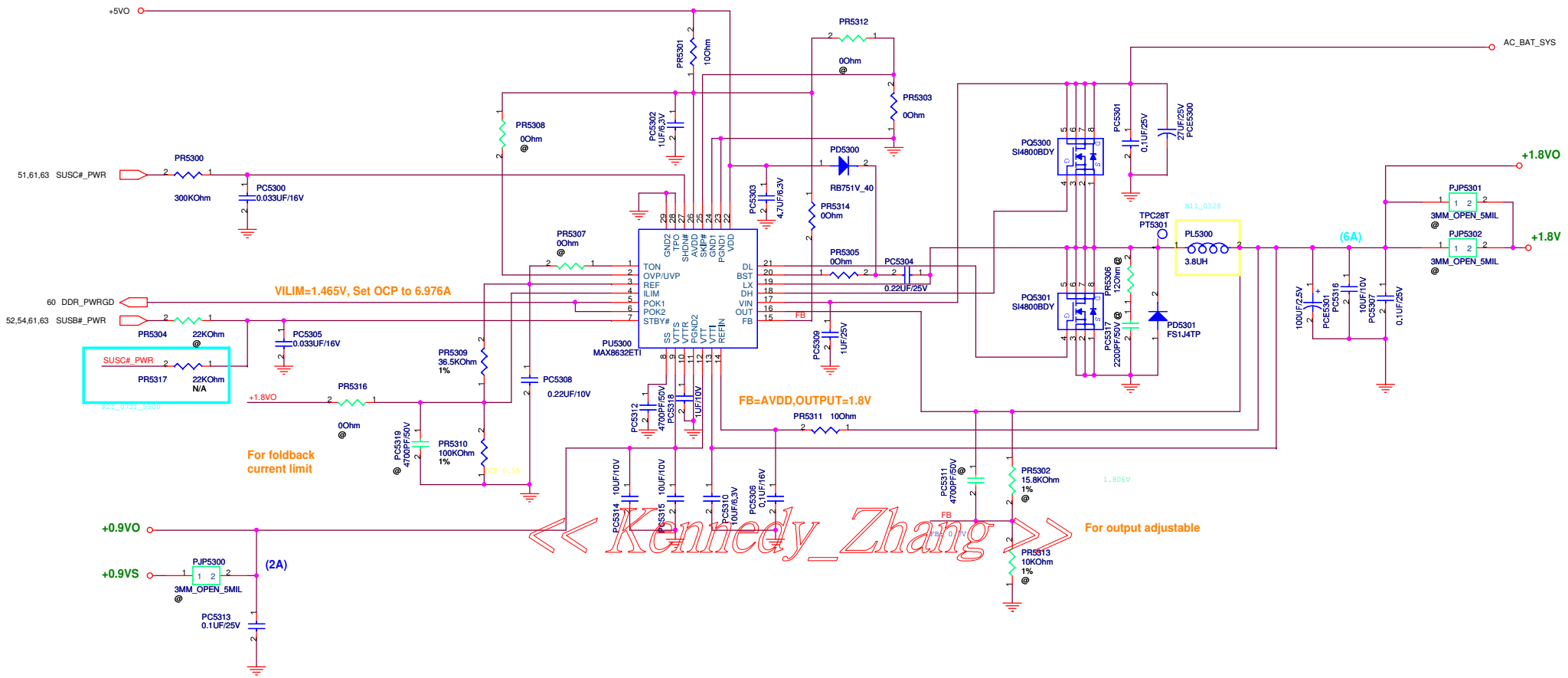

Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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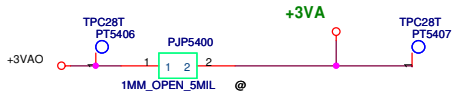
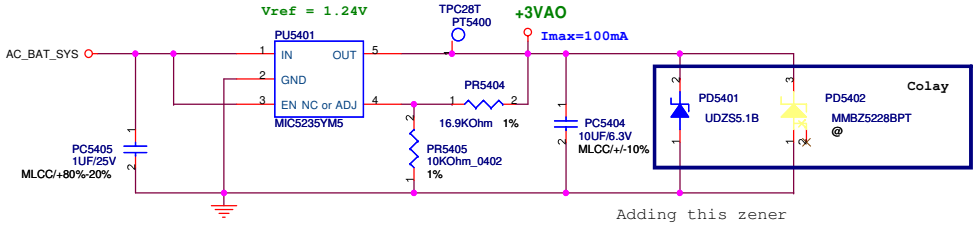
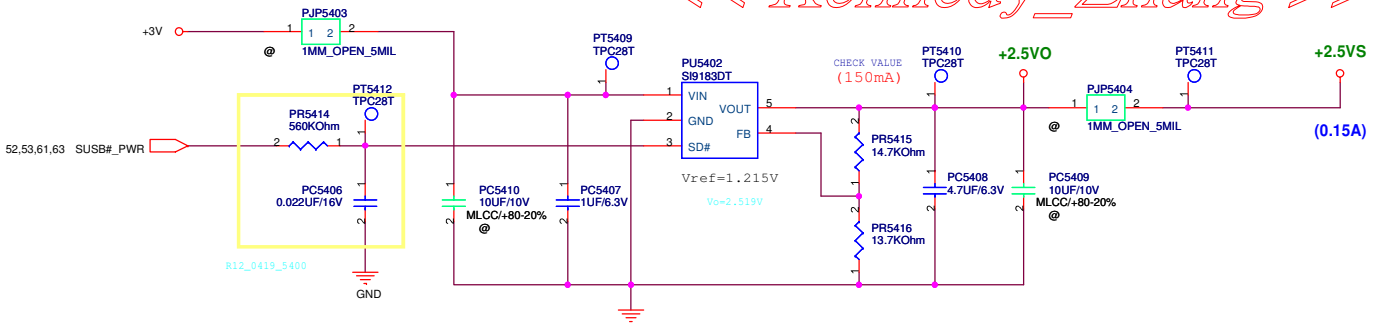
+3VAO





Adding this zener diode to make sure that EC doesn't release smoke when PU5401.1 is short to PU5401.5

+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.1
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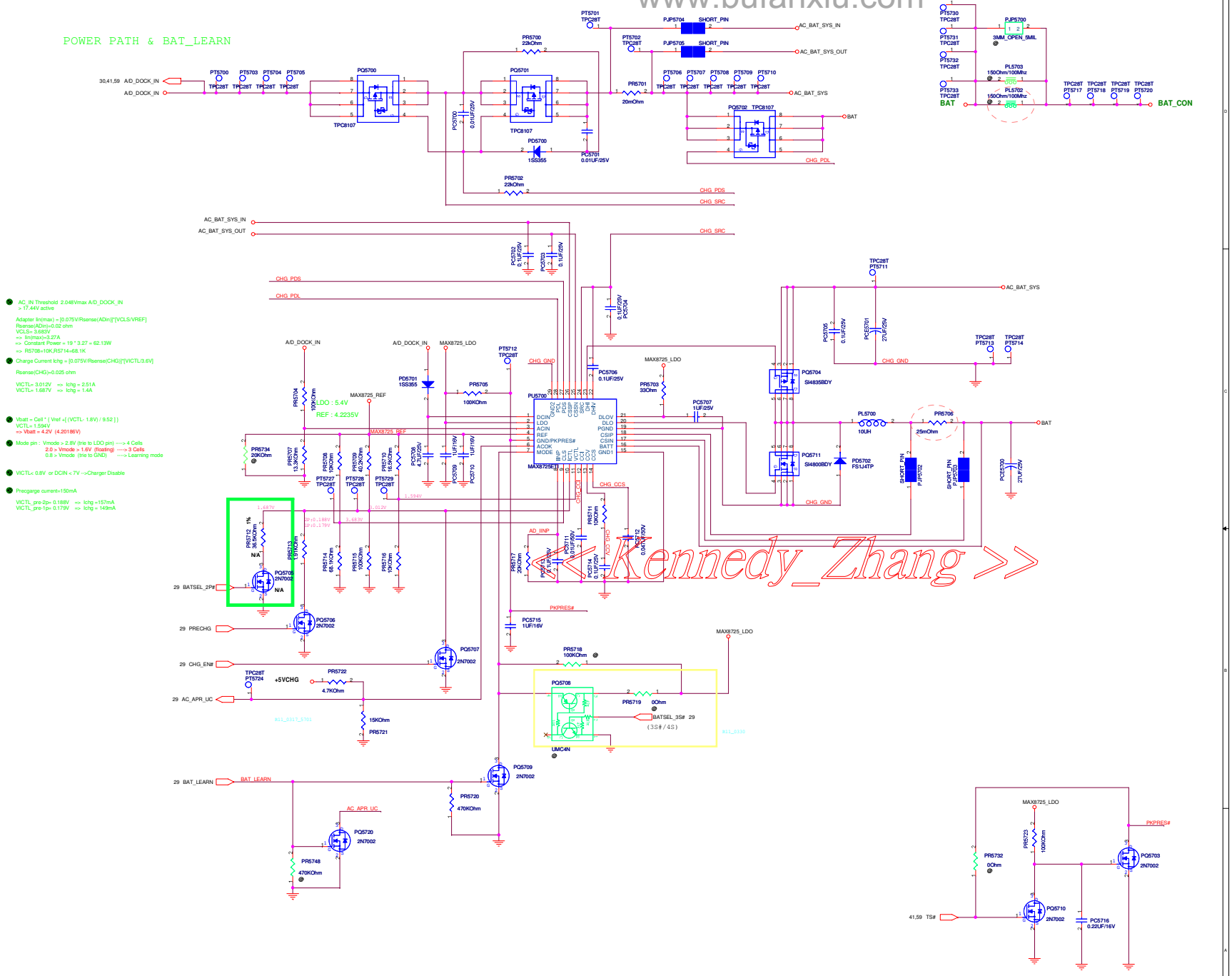
POWER PATH & BAT_LEARN



Title : POWER_CHARGER			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12F		Rev: 2.0
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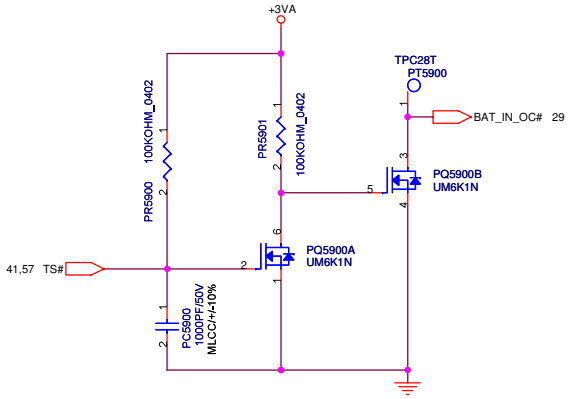
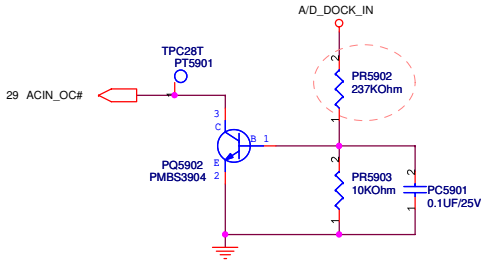
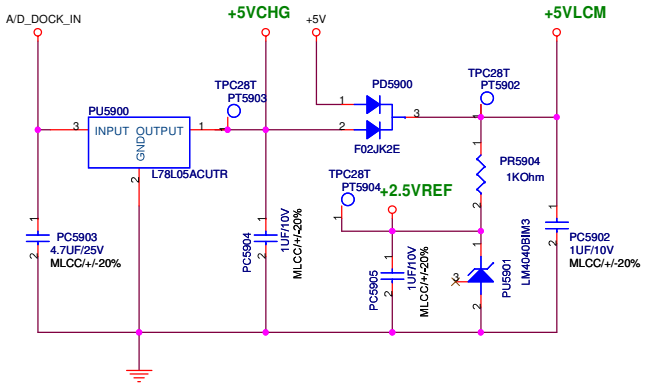
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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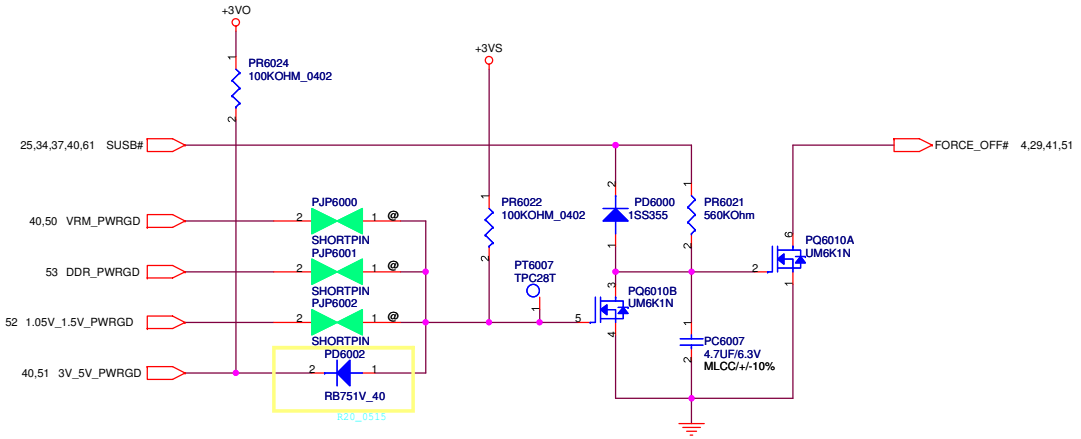
POWER GOOD DETECTER



TPC28T PT6003 — VRM_PWRGD
TPC28T PT6004 — DDR_PWRGD
TPC28T PT6005 — 3V_5V_PWRGD
TPC28T PT6006 — 1.05V_1.5V_PWRGD

ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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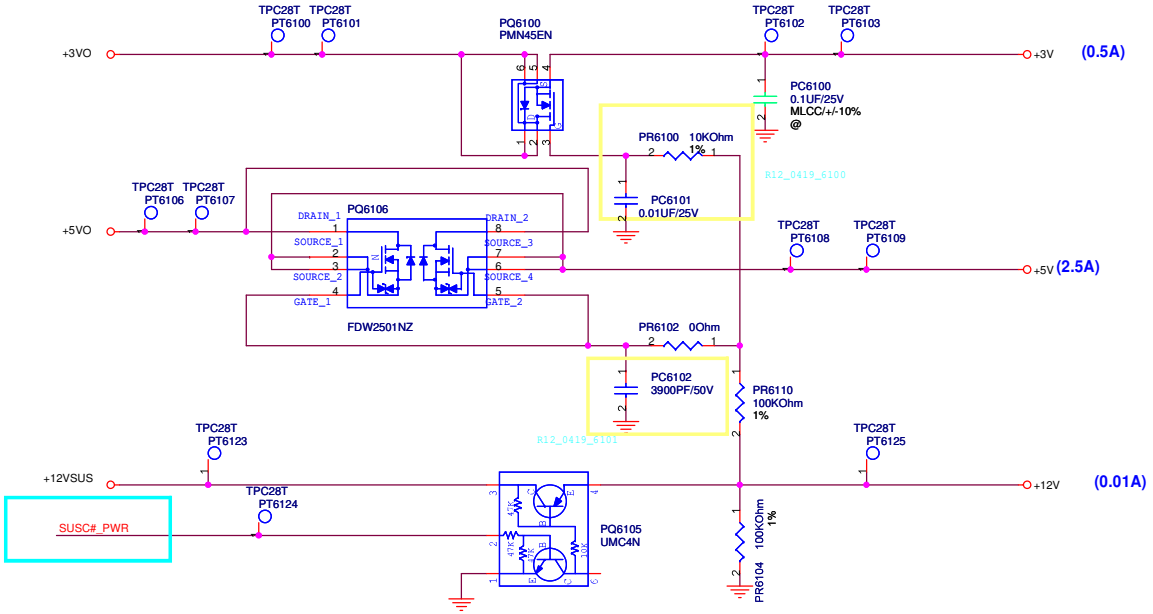
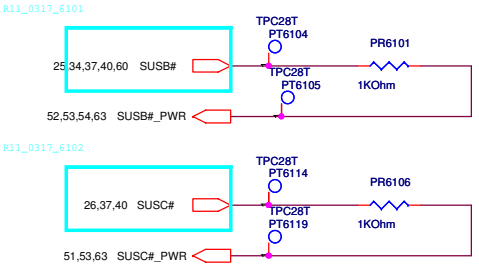
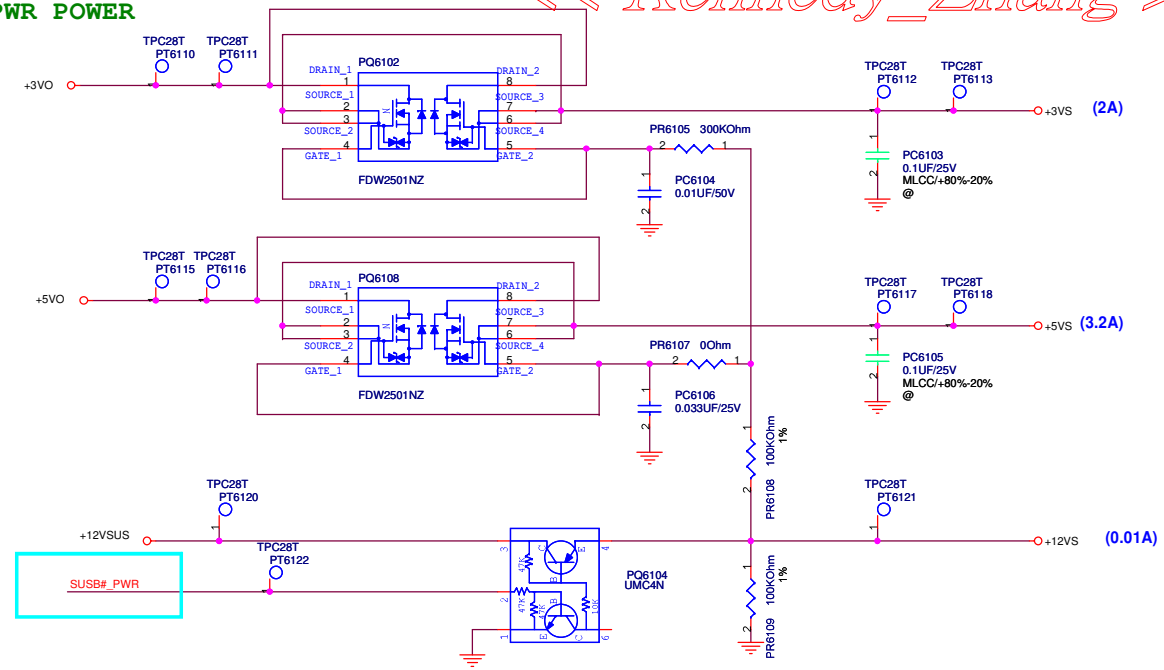
SUSC#_PWR POWER





SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA → +3VA 4,12,20,22,29,37,38,40,54,59

+5VA → +5VA 51

+5VO → +5VO 51,52,53,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 18,19,20,25,29,34,40,51

+5VSUS → +5VSUS 20,30,51

+3V → +3V 12,18,26,27,31,35,37,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 36,37,61

+12VS → +12VS 12,22,27,33,37,61

+5V → +5V 9,12,30,36,37,38,44,59,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,37,38,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,37,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,37,53

+VCCP → +VCCP 2,6,9,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH → +VCCP_GMCH 9,10

+VCCP_ICH → +VCCP_ICH 17,20

+0.9VS → +0.9VS 16,37,53

BAT → BAT 30,57

+5VCHG → +5VCHG 57,59

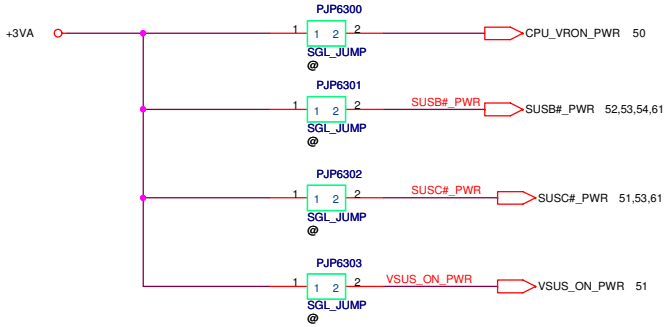
+5VLCM → +5VLCM 59

+2.5VREF → +2.5VREF 59

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST



<< Kennedy_Zhang >>

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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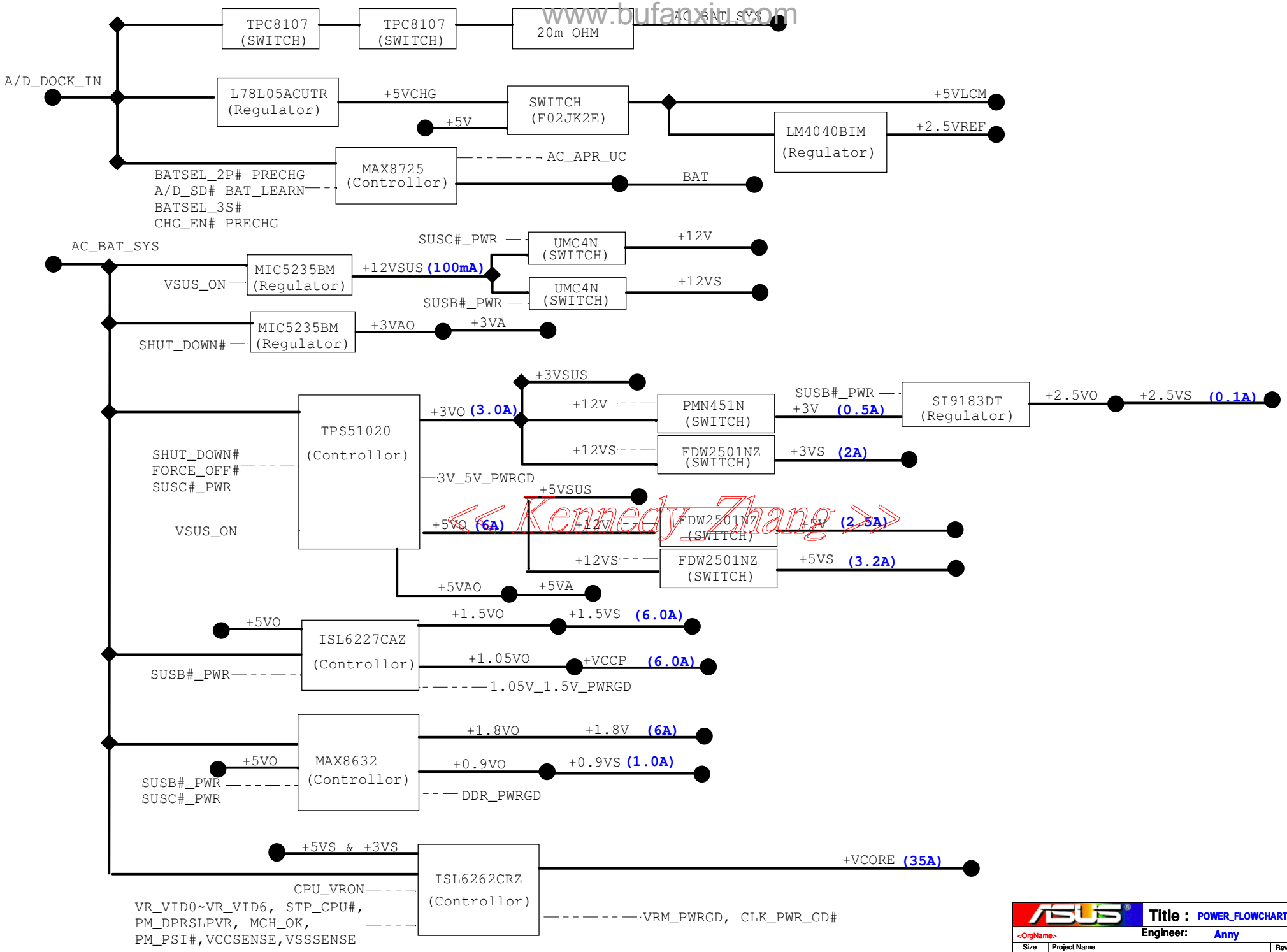

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12F	Rev: 2.0
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