


# A8Jp/Jv/Je/Jn/Fm SCHEMATIC

PAGE	Content	PAGE	Content
	<b>SYSTEM PAGE REF.</b>		<b>POWER PAGE REF.</b>
4	Merom CPU (1)	50	POWER_VCORE
5	Merom CPU (2)	51	POWER_SYSTEM
6	CPU CAP/THERMAL SENSOR	52	POWER_I/O_1.8V & 1.05VS
7	CLOCK GEN.	53	POWER_I/O_+1.5VS
8	Calistoga--CPU	54	POWER_I/O_VTT & +2.5VS
9	Calistoga--PCIE	55	POWER_VGA_CORE (Empty)
10	Calistoga--DDR2	56	POWER_VGA_RAM (Empty)
11	Calistoga--POWER	57	POWER_CHARGER
12	Calistoga--GND	58	POWER_PIC
13	Calistoga--Strap	59	POWER_SELECTOR
14	DDR2 SO-DIMM_0	60	POWER_PROTECT
15	DDR2 SO-DIMM_1	61	POWER_LOAD SWITCH
16	DDR2 ADDRESS TERMINATION	62	POWER_FLOWCHART
17	VGA CONN	63	POWER_SIGNAL
18	LVDS & INVERTER CONN		
19	CRT & TV_OUT		
20	ICH7M--CPU, IDE, AUDIO		
21	ICH7M--PCI, PCI-E, USB		
22	ICH7M--GPIO		
23	ICH7M--VCC, GND		
24	HDD & CD-ROM CONN		
25	USB PORTS		
26	SUPER I/O LPC47N217		
27	BIOS & FIR		
28	KBC 38857		
29	SM BUS & POWER PORT		
30	PCI-E--GIGA_LAN RTL8111B		
31	PCI-E--MINI CARD		
32	PCI-E--NEW CARD		
33	PCI--1394, CardReader R5C832		
34	PCI--4 IN1 CON		
35	PCI--Empty		
36	AUDIO CODEC AD1986A		
37	AUDIO AMP G1420		
38	MDC, B/T, TPM & DISCHG, HOLE		
39	DVI CONN		
40	ACIN, BAT, FAN, I/O PORT		
41	SW & LED & TP		
42	POWER-ON SEQUENCE		
43	HISTORY		
44	I/O PORT		

**ASUSTek COMPUTER INC.** 

File: **PAGE REF.**

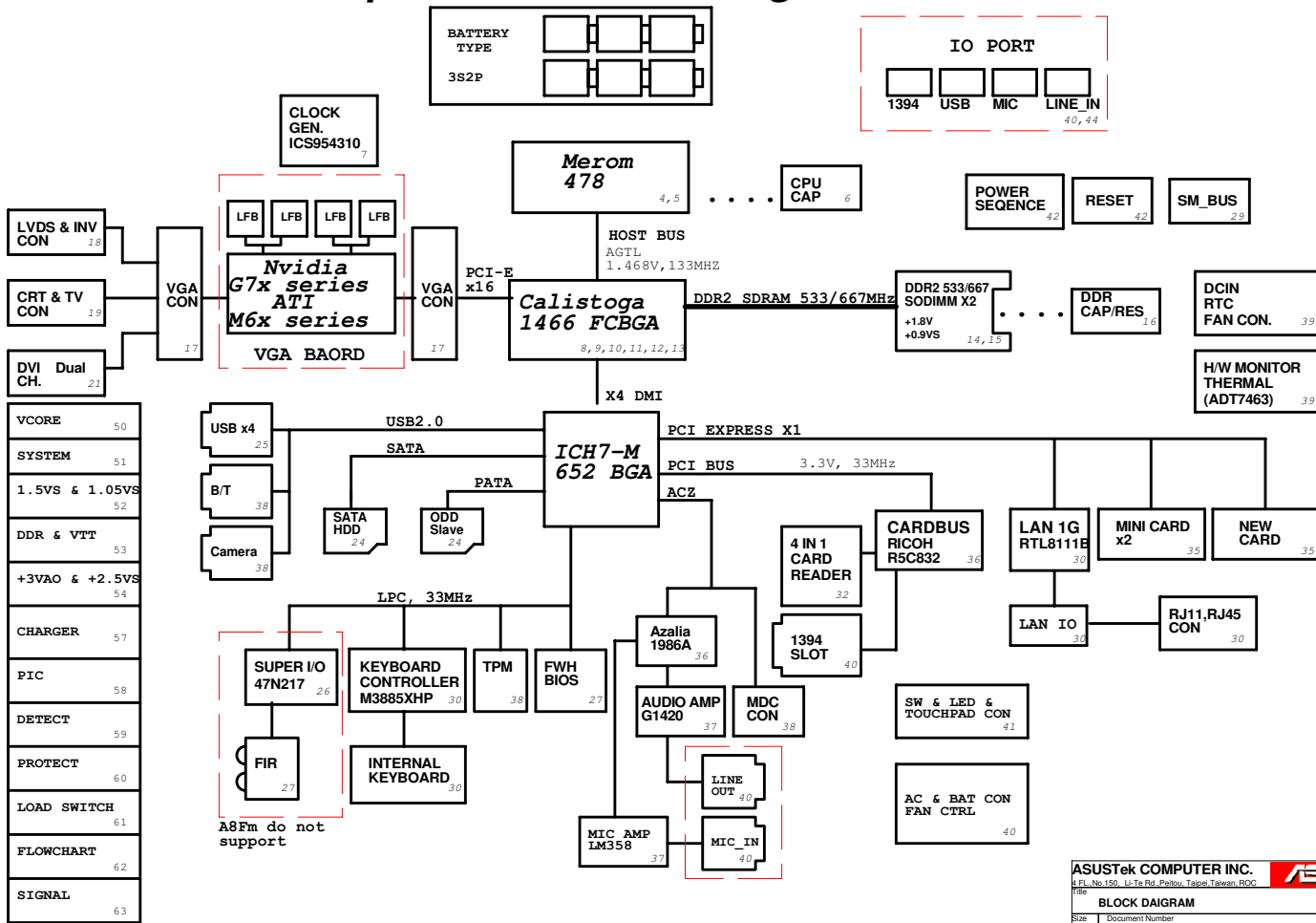
Size: Document Number


Customer: **A8J/F** Rev: 2.0

Date: 5/15/07 Sheet 1 of 63

<< Kennedy\_Zhang >>

# A8Jp/Fm Merom/Calistoga BLOCK DIAGRAM



ASUSTek COMPUTER INC.   
 4 FL., No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC  
 Title: BLOCK DAIGRAM  
 Size: Custom Document Number: A8J/F Rev: 2.0  
 Date: 5/25/2007 Sheet: 2 of 63

<< Kennedy\_Zhang >>


PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Integrated LAN	AD24(NO USE)			
1394	AD16	0	A	
4 IN 1		0	B	

SM\_BUS ADDRESS : Thermal MAX6657 = 1001100x ( 98h )  
 CLK GEN. = 1101001x ( D2h )  
 DDR\_SODIMMO = 1010000x ( A0h )  
 DDR\_SODIMM1 = 1010010x ( A4h )  
 VGA Thermal IC = 1001100x ( 9Ah )

ICH7M GPIO	Use As	Signal Name	Power	
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BACK_OFF#	+3VS
GPIO 07	i	GPI	RF_SW_OFF#	+3VS
GPIO 08	i	GPI	EXTSMI#_3A	+3VSUS
GPIO 09	i	GPI	PD_DeDock#(PWRLMT#)	+3VSUS
GPIO 10	i	GPI	CHG_FULL_OC	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KB_SCI#	+3VSUS
GPIO 13	i	GPI	SIO_SMI#	+3VSUS
GPIO 14	i	GPI	PD_UnDock#(PWRLMT#)	+3VSUS
GPIO 15	i	GPO	802_LED_EN#	+3VSUS
GPIO 16	o	GPO	PM_DPRSPLVR	+3VS
GPIO 17	o	GPO	PCI_EN#5	+3VS
GPIO 18	o	GPO	STP_PCI#	+3VS
GPIO 19	i	GPI	PD_RDY#	+3VS
GPIO 20	o	GPO	STP_CPU#	+3VS
GPIO 21	i	GPO	PD_SIO_RST#	+3VS
GPIO 22	i	Native	PCI_REQ#4	+3VS
GPIO 23	i	Native	LPC_DRQ#1	+3VS
GPIO 24	o	GPO	PD_EN#	+3VSUS
GPIO 25	o	GPO	CB_SD#	+3VSUS
GPIO 26	o	GPO	OP_SD#	+3VSUS
GPIO 27	o	GPO	WLAN_ON#	+3VSUS
GPIO 28	o	GPO	1Hz	+3VSUS
GPIO 29	i	Native	USB_OC#5	+3VSUS
GPIO 30	i	Native	USB_OC#6	+3VSUS
GPIO 31	i	Native	USB_OC#7	+3VSUS
GPIO 32	o	GPO	PM_CLKRUN#	+3VS
GPIO 33	o	GPO	BT_ON/OFF#	+3VS
GPIO 34	o	GPO	FWH_WP#	+3VS
GPIO 35	o	GPO	SATACLKREQ#	+3VS
GPIO 36	i	GPO	BT_LED_EN#	+3VS
GPIO 37	i	GPI	PCB_ID0	+3VS
GPIO 38	i	GPI	PCB_ID1	+3VS
GPIO 39	i	GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS	
GPIO 49	Native	H_PWRGD	+VCORE	

M38857 GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPI	SMD_BAT	+3V
P77	GPI	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI	NONE	+3VS
GPIO11	GPO	NONE	+3VS
GPIO12	GPO	NONE	+3VS
GPIO13	GPI	NONE	+3VS
GPIO14	GPI	NONE	+3VS
GPIO23	GPO	ATI_RST#	+3VS
GPIO40	GPI		+3VS
GPIO41	GPI		+3VS
GPIO40	GPI		+3VS
GPIO43	GPI		+3VS
GPIO44	GPI		+3VS
GPIO45	GPI		+3VS
GPIO46	GPI	VGA_DETEC#	+3VS
GPIO47	GPI		+3VS

ASUSTek COMPUTER INC. 

File: SCHEMATICS REF.

Size: A8J/F

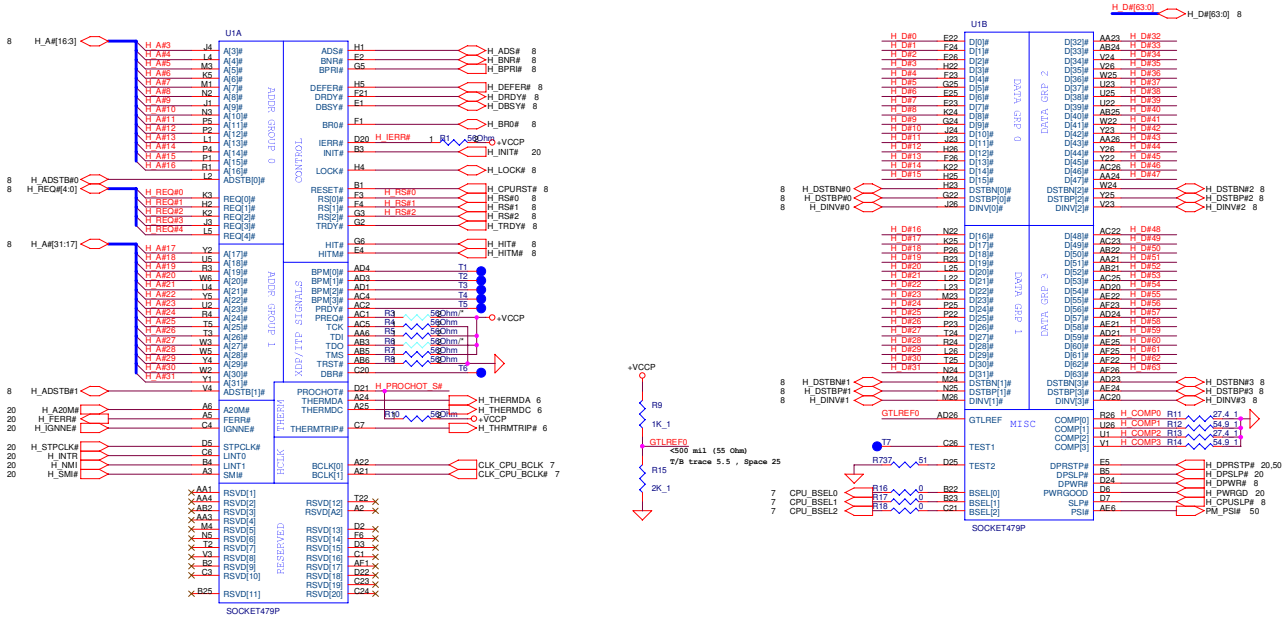
Customer: A8J/F

Date: 2007.09.03

Sheet: 3 of 63

Rev: 2.0

<< Kennedy\_Zhang >>



**ASUSTek COMPUTER INC.**

ASUS

File: YONAH\_CPU1

Size: Document Number

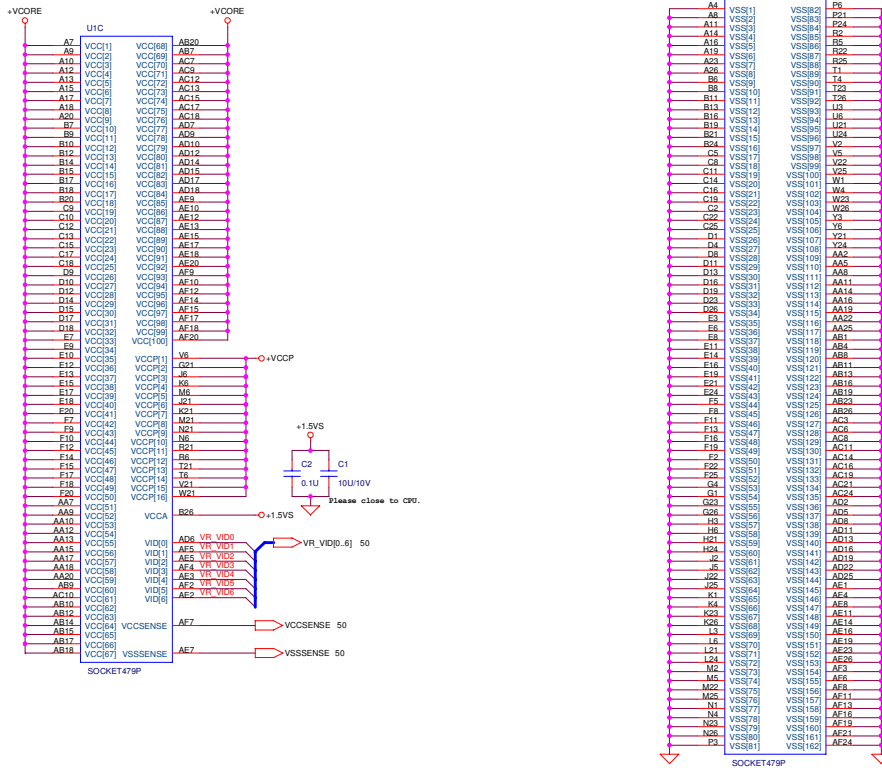
Customer: A&J/F


Date: 5/5/2007

Sheet: 4 of 63

Rev: 2.0

<< Kennedy\_Zhang >>



**ASUSTek COMPUTER INC.** 

4 FL, No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC

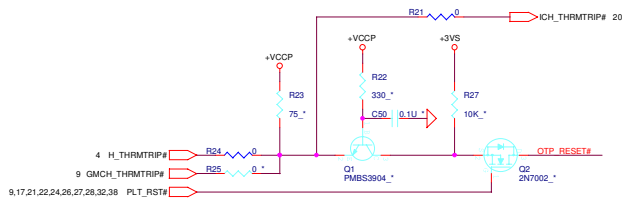
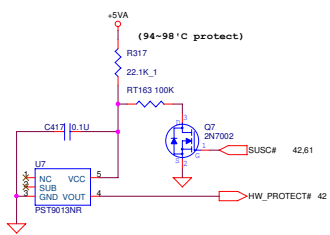
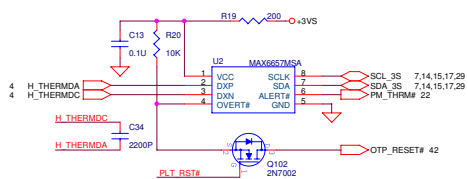
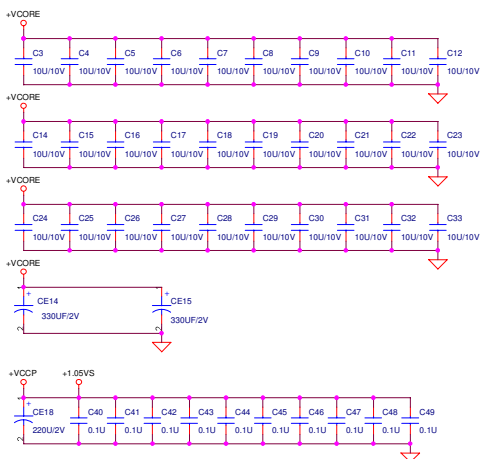
File: **YONAH CPU2**

Size: Document Number

Customer: **A8J/F**

Date: 5/5/2007 Sheet 5 of 63

<< Kennedy\_Zhang >>



+VCCP	4,5,8,11,12,20,23,52
+VCORE	5,50
+3VS	7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+5VA	51,54

**ASUSTek COMPUTER INC.**

PL: No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC

**CPU CAP.THERMAL SENSOR**

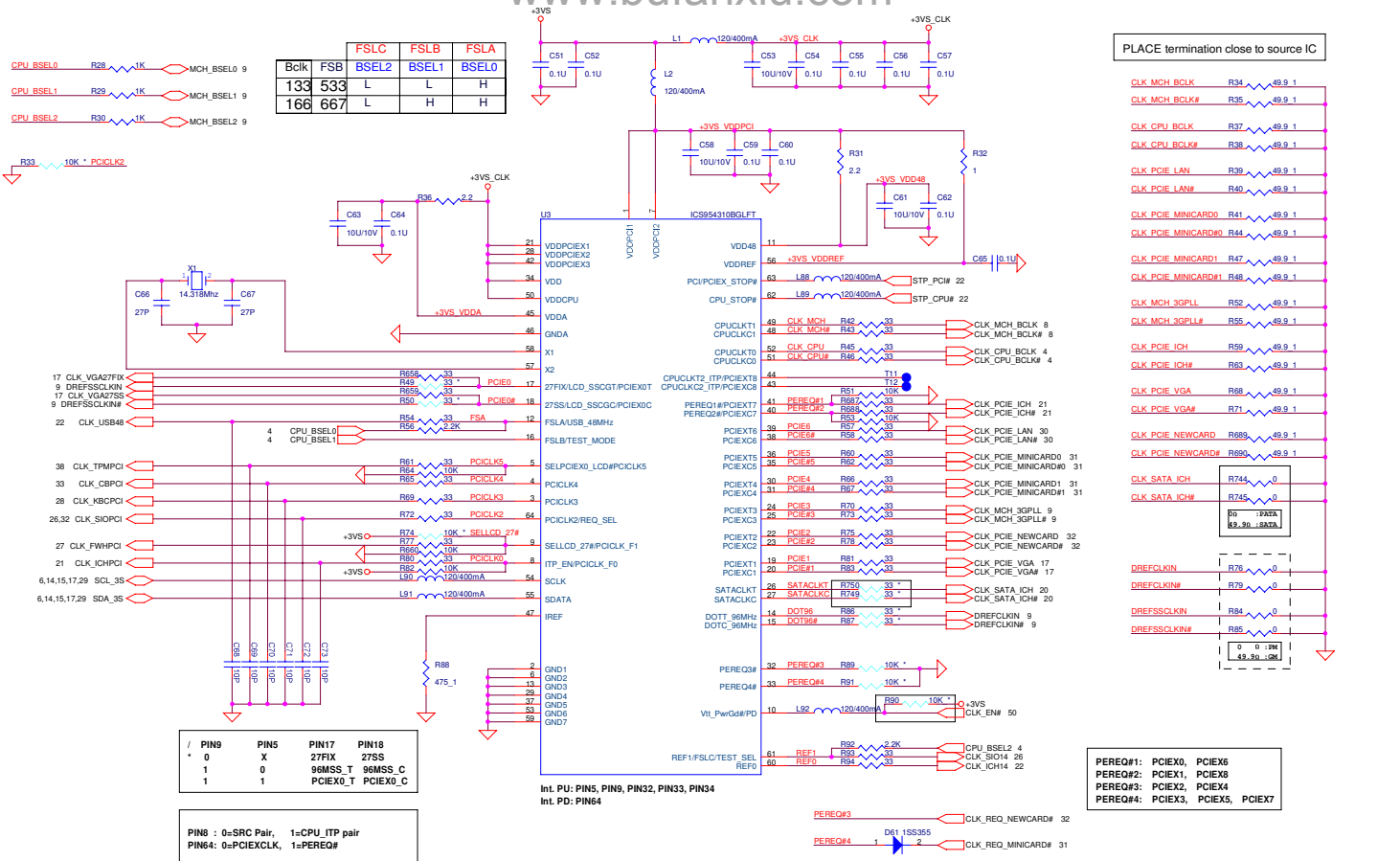
Doc: A8J/F

Date: 03/03/2007


Rev: 2.0

Sheet: 6 of 63

<< Kennedy\_Zhang >>



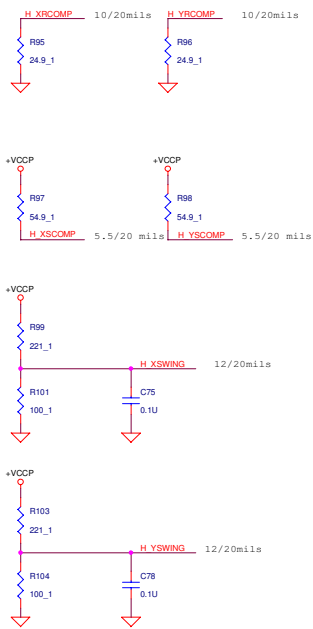
PLACE termination close to source IC

ASUSTek COMPUTER INC. 

File: CLK ICS954310AGLF

Sub	Document Number	Rev
Customer	A6JF	2.0
Date:	日期: 03/2007	Sheet 7 of 63

<< Kennedy\_Zhang >>



4 H\_DM0[0..63] H\_DM0[63]

H_DM0	F1	H_DM_0
H_DM1	H1	H_DM_1
H_DM2	J8	H_DM_2
H_DM3	H3	H_DM_3
H_DM4	H3	H_DM_4
H_DM5	K2	H_DM_5
H_DM6	G1	H_DM_6
H_DM7	G2	H_DM_7
H_DM8	H7	H_DM_8
H_DM9	K1	H_DM_9
H_DM10	K7	H_DM_10
H_DM11	A6	H_DM_11
H_DM12	H4	H_DM_12
H_DM13	K11	H_DM_13
H_DM14	G4	H_DM_14
H_DM15	T10	H_DM_15
H_DM16	T11	H_DM_16
H_DM17	T3	H_DM_17
H_DM18	J7	H_DM_18
H_DM19	L9	H_DM_19
H_DM20	L11	H_DM_20
H_DM21	L9	H_DM_21
H_DM22	L11	H_DM_22
H_DM23	W9	H_DM_23
H_DM24	T1	H_DM_24
H_DM25	T8	H_DM_25
H_DM26	T4	H_DM_26
H_DM27	W7	H_DM_27
H_DM28	L6	H_DM_28
H_DM29	T9	H_DM_29
H_DM30	W8	H_DM_30
H_DM31	T5	H_DM_31
H_DM32	A67	H_DM_32
H_DM33	AA9	H_DM_33
H_DM34	Y4	H_DM_34
H_DM35	W3	H_DM_35
H_DM36	Y4	H_DM_36
H_DM37	Y4	H_DM_37
H_DM38	W5	H_DM_38
H_DM39	Y10	H_DM_39
H_DM40	AB8	H_DM_40
H_DM41	W2	H_DM_41
H_DM42	AA4	H_DM_42
H_DM43	AA7	H_DM_43
H_DM44	AA7	H_DM_44
H_DM45	AA6	H_DM_45
H_DM46	AA0	H_DM_46
H_DM47	Y8	H_DM_47
H_DM48	AA1	H_DM_48
H_DM49	AB4	H_DM_49
H_DM50	AC9	H_DM_50
H_DM51	AB11	H_DM_51
H_DM52	AC11	H_DM_52
H_DM53	AB3	H_DM_53
H_DM54	AC2	H_DM_54
H_DM55	AD1	H_DM_55
H_DM56	AD9	H_DM_56
H_DM57	AD7	H_DM_57
H_DM58	AC7	H_DM_58
H_DM59	AC6	H_DM_59
H_DM60	AB5	H_DM_60
H_DM61	AD10	H_DM_61
H_DM62	AD4	H_DM_62
H_DM63	AC8	H_DM_63

H\_XRCOMP E1 H\_XRCOMP  
H\_XSCOMP E2 H\_XSCOMP  
H\_XSWING E4 H\_XSWING  
H\_YRCOMP Y1 H\_YRCOMP  
H\_YSCOMP U1 H\_YSCOMP  
H\_YSWING W1 H\_YSWING

7 CLK\_MCH\_BCLK AG2 CLK\_MCH\_BCLK# AG1  
7 CLK\_MCH\_BCLK# AG1 CLK\_MCH\_BCLK#

H\_A#3[31] H\_A#3[31] 4

H_A#_3	H_A#3
H_A#_4	H_A#4
H_A#_5	H_A#5
H_A#_6	H_A#6
H_A#_7	H_A#7
H_A#_8	H_A#8
H_A#_9	H_A#9
H_A#_10	H_A#10
H_A#_11	H_A#11
H_A#_12	H_A#12
H_A#_13	H_A#13
H_A#_14	H_A#14
H_A#_15	H_A#15
H_A#_16	H_A#16
H_A#_17	H_A#17
H_A#_18	H_A#18
H_A#_19	H_A#19
H_A#_20	H_A#20
H_A#_21	H_A#21
H_A#_22	H_A#22
H_A#_23	H_A#23
H_A#_24	H_A#24
H_A#_25	H_A#25
H_A#_26	H_A#26
H_A#_27	H_A#27
H_A#_28	H_A#28
H_A#_29	H_A#29
H_A#_30	H_A#30
H_A#_31	H_A#31

H\_ADS#\_0 H\_ADS#\_0  
H\_ADS#\_1 H\_ADS#\_1  
H\_ADS#\_2 H\_ADS#\_2  
H\_ADS#\_3 H\_ADS#\_3  
H\_ADS#\_4 H\_ADS#\_4  
H\_ADS#\_5 H\_ADS#\_5  
H\_ADS#\_6 H\_ADS#\_6  
H\_ADS#\_7 H\_ADS#\_7  
H\_ADS#\_8 H\_ADS#\_8  
H\_ADS#\_9 H\_ADS#\_9  
H\_ADS#\_10 H\_ADS#\_10  
H\_ADS#\_11 H\_ADS#\_11  
H\_ADS#\_12 H\_ADS#\_12  
H\_ADS#\_13 H\_ADS#\_13  
H\_ADS#\_14 H\_ADS#\_14  
H\_ADS#\_15 H\_ADS#\_15  
H\_ADS#\_16 H\_ADS#\_16  
H\_ADS#\_17 H\_ADS#\_17  
H\_ADS#\_18 H\_ADS#\_18  
H\_ADS#\_19 H\_ADS#\_19  
H\_ADS#\_20 H\_ADS#\_20  
H\_ADS#\_21 H\_ADS#\_21  
H\_ADS#\_22 H\_ADS#\_22  
H\_ADS#\_23 H\_ADS#\_23  
H\_ADS#\_24 H\_ADS#\_24  
H\_ADS#\_25 H\_ADS#\_25  
H\_ADS#\_26 H\_ADS#\_26  
H\_ADS#\_27 H\_ADS#\_27  
H\_ADS#\_28 H\_ADS#\_28  
H\_ADS#\_29 H\_ADS#\_29  
H\_ADS#\_30 H\_ADS#\_30  
H\_ADS#\_31 H\_ADS#\_31

H\_DIN#\_0 H\_DIN#\_0  
H\_DIN#\_1 H\_DIN#\_1  
H\_DIN#\_2 H\_DIN#\_2  
H\_DIN#\_3 H\_DIN#\_3  
H\_DIN#\_4 H\_DIN#\_4  
H\_DIN#\_5 H\_DIN#\_5  
H\_DIN#\_6 H\_DIN#\_6  
H\_DIN#\_7 H\_DIN#\_7  
H\_DIN#\_8 H\_DIN#\_8  
H\_DIN#\_9 H\_DIN#\_9  
H\_DIN#\_10 H\_DIN#\_10  
H\_DIN#\_11 H\_DIN#\_11  
H\_DIN#\_12 H\_DIN#\_12  
H\_DIN#\_13 H\_DIN#\_13  
H\_DIN#\_14 H\_DIN#\_14  
H\_DIN#\_15 H\_DIN#\_15  
H\_DIN#\_16 H\_DIN#\_16  
H\_DIN#\_17 H\_DIN#\_17  
H\_DIN#\_18 H\_DIN#\_18  
H\_DIN#\_19 H\_DIN#\_19  
H\_DIN#\_20 H\_DIN#\_20  
H\_DIN#\_21 H\_DIN#\_21  
H\_DIN#\_22 H\_DIN#\_22  
H\_DIN#\_23 H\_DIN#\_23  
H\_DIN#\_24 H\_DIN#\_24  
H\_DIN#\_25 H\_DIN#\_25  
H\_DIN#\_26 H\_DIN#\_26  
H\_DIN#\_27 H\_DIN#\_27  
H\_DIN#\_28 H\_DIN#\_28  
H\_DIN#\_29 H\_DIN#\_29  
H\_DIN#\_30 H\_DIN#\_30  
H\_DIN#\_31 H\_DIN#\_31

H\_DSTBN#\_0 H\_DSTBN#\_0  
H\_DSTBN#\_1 H\_DSTBN#\_1  
H\_DSTBN#\_2 H\_DSTBN#\_2  
H\_DSTBN#\_3 H\_DSTBN#\_3  
H\_DSTBN#\_4 H\_DSTBN#\_4  
H\_DSTBN#\_5 H\_DSTBN#\_5  
H\_DSTBN#\_6 H\_DSTBN#\_6  
H\_DSTBN#\_7 H\_DSTBN#\_7  
H\_DSTBN#\_8 H\_DSTBN#\_8  
H\_DSTBN#\_9 H\_DSTBN#\_9  
H\_DSTBN#\_10 H\_DSTBN#\_10  
H\_DSTBN#\_11 H\_DSTBN#\_11  
H\_DSTBN#\_12 H\_DSTBN#\_12  
H\_DSTBN#\_13 H\_DSTBN#\_13  
H\_DSTBN#\_14 H\_DSTBN#\_14  
H\_DSTBN#\_15 H\_DSTBN#\_15  
H\_DSTBN#\_16 H\_DSTBN#\_16  
H\_DSTBN#\_17 H\_DSTBN#\_17  
H\_DSTBN#\_18 H\_DSTBN#\_18  
H\_DSTBN#\_19 H\_DSTBN#\_19  
H\_DSTBN#\_20 H\_DSTBN#\_20  
H\_DSTBN#\_21 H\_DSTBN#\_21  
H\_DSTBN#\_22 H\_DSTBN#\_22  
H\_DSTBN#\_23 H\_DSTBN#\_23  
H\_DSTBN#\_24 H\_DSTBN#\_24  
H\_DSTBN#\_25 H\_DSTBN#\_25  
H\_DSTBN#\_26 H\_DSTBN#\_26  
H\_DSTBN#\_27 H\_DSTBN#\_27  
H\_DSTBN#\_28 H\_DSTBN#\_28  
H\_DSTBN#\_29 H\_DSTBN#\_29  
H\_DSTBN#\_30 H\_DSTBN#\_30  
H\_DSTBN#\_31 H\_DSTBN#\_31

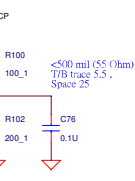
H\_HIT#\_0 H\_HIT#\_0  
H\_HIT#\_1 H\_HIT#\_1  
H\_HIT#\_2 H\_HIT#\_2  
H\_HIT#\_3 H\_HIT#\_3

H\_REQ#\_0 H\_REQ#\_0  
H\_REQ#\_1 H\_REQ#\_1  
H\_REQ#\_2 H\_REQ#\_2  
H\_REQ#\_3 H\_REQ#\_3  
H\_REQ#\_4 H\_REQ#\_4

H\_RS#\_0 H\_RS#\_0  
H\_RS#\_1 H\_RS#\_1  
H\_RS#\_2 H\_RS#\_2  
H\_RS#\_3 H\_RS#\_3

H\_SLP#\_0 H\_SLP#\_0  
H\_SLP#\_1 H\_SLP#\_1  
H\_SLP#\_2 H\_SLP#\_2  
H\_SLP#\_3 H\_SLP#\_3

+VCCP 4,5,6,11,12,20,23,52



**ASUSTek COMPUTER INC.**

File: Galistoga-CPU

Size	Document Number	Rev
Customer	A&J/F	2.0

Date: 5/5/2007 Sheet 8 of 63

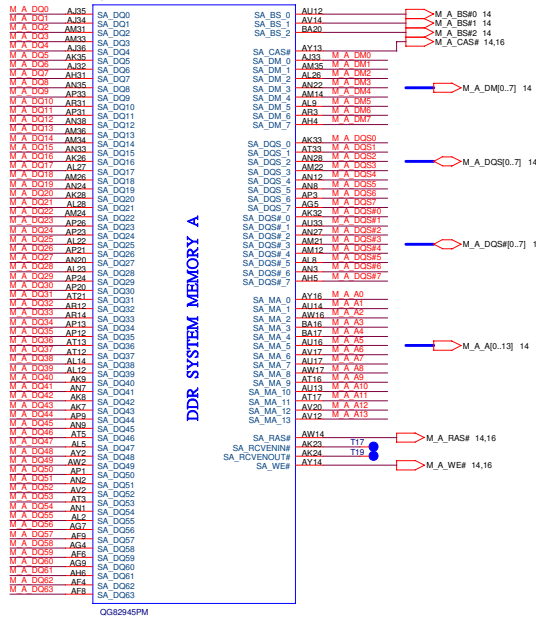
<< Kennedy\_Zhang >>





14 M\_A\_DQ[0..63]

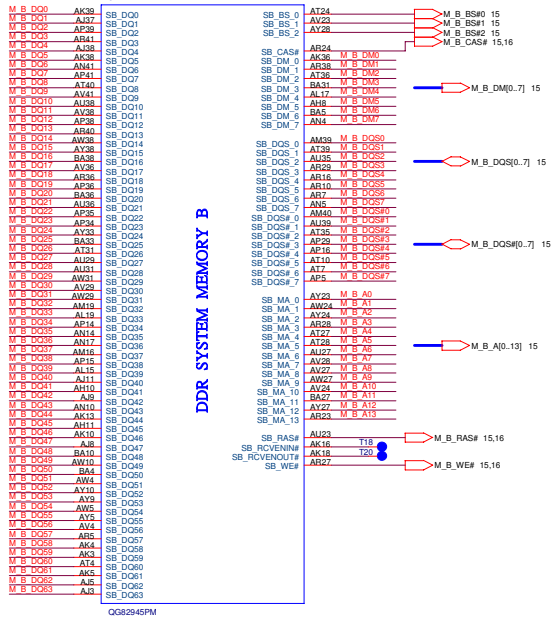
U4D



QG82945PM

15 M\_B\_DQ[0..63]

U4E



QG82945PM

ASUSTek COMPUTER INC.

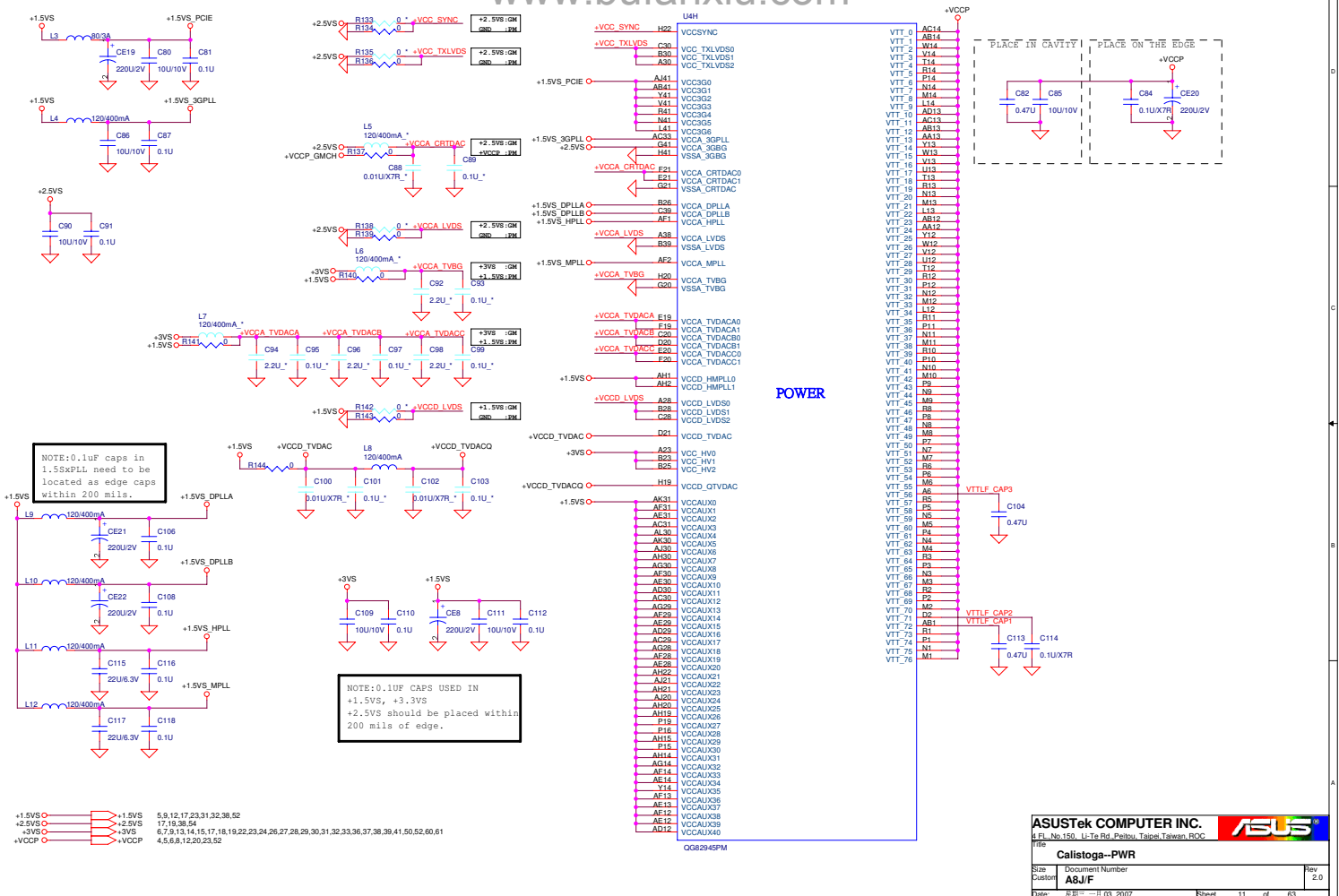
File: No.150\_Li-Te Rd., Peitou, Taipei, Taiwan, ROC

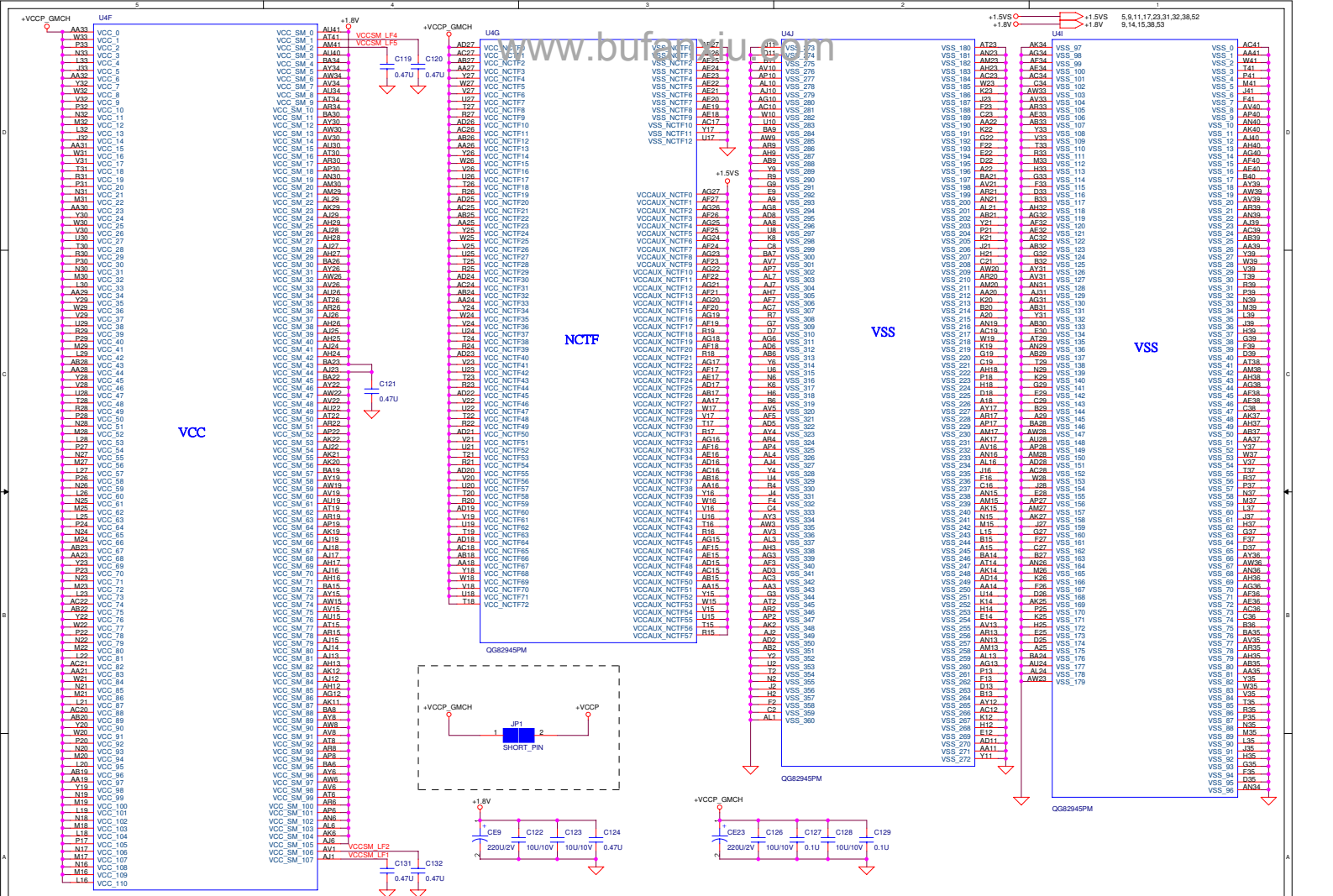
Model: Calistoga-DDR2

Size	Document Number	Rev
Customer	A8J/F	2.0

Date: 5/15/2007 Sheet 10 of 63

<< Kennedy\_Zhang >>





ASUSTek COMPUTER INC.   
 File: Calistoga-GND  
 Date: 08/03/2007 Sheet: 02 of 03

« Kennedy\_Zhang »

Pin	Document Number	Rev
Customer	AGJ/F	2.0



**CFG5 : DMI STRAP**  
 LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**



**CFG[13:12] : GMCH TEST MODE SELECT**  
 00 = Partial CLK gating disable  
 01 = XOR Mode Enable  
 10 = ALL Z Mode Enable  
**11 = NORMAL OPERATION (Default)**



**CFG7 : CPU STRAP**  
 LOW = RESERVED  
**HIGH = Mobile Yonah CPU (Default)**



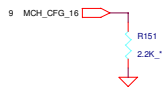
**CFG9 : PCIE GRAPHIC LANE**  
 LOW = REVERSE LANE  
**HIGH = NORMAL OPERATION (Default)**



**CFG15 : ICH RESET Disable**  
 LOW = ICH RESET Disabled  
**HIGH = Normal Operation (Default)**



**CFG10 : HOST PLL VCO SELECT**  
 LOW = RESERVED  
**HIGH = MOBILITY (Default)**



**CFG16 : FSB Dynamic ODT**  
 LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**



**CFG11 : PSB 4x CLK ENABLE**  
 LOW = 4X ENABLED  
**HIGH = 8X ENABLED (Default)**



**CFG18 : GMCH Core Voltage Level**  
**LOW = 1.05V (Default)**  
 HIGH = 1.5V

CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.

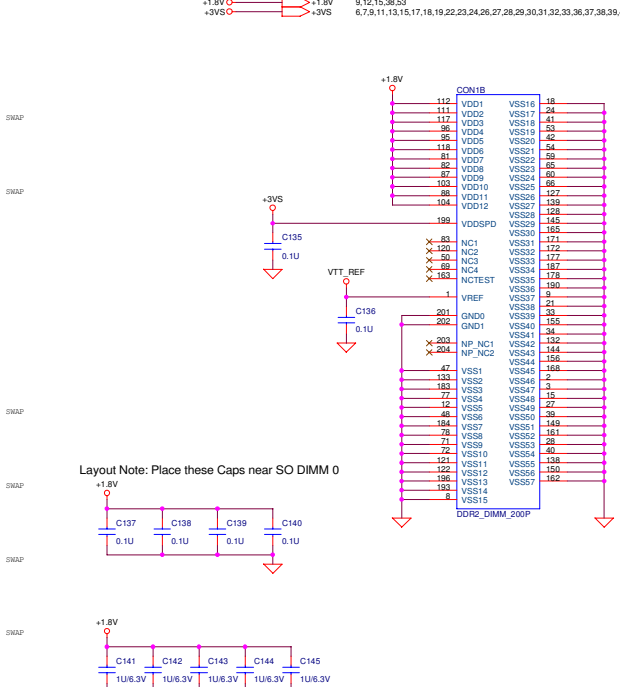
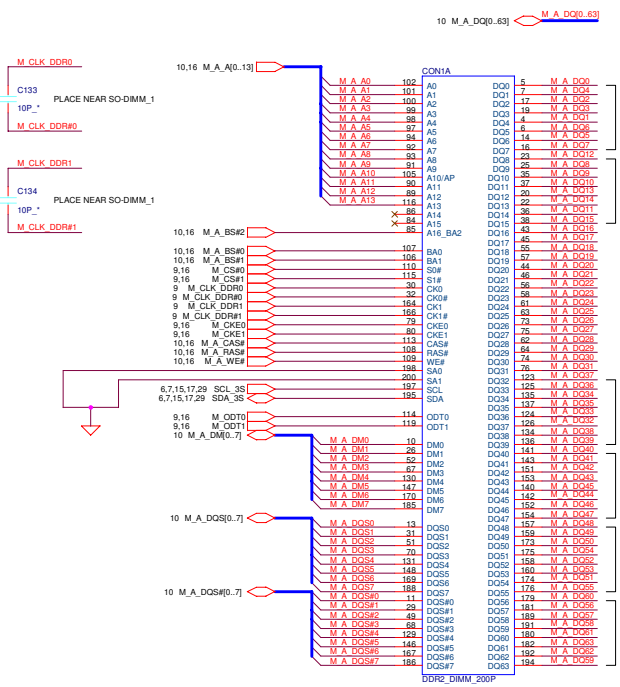


**CFG19 : DMI LANE REVERSAL**  
**LOW = NORMAL (Default)**  
 HIGH = LANES REVERSED

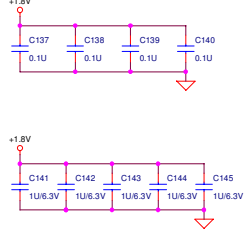
ASUSTek COMPUTER INC.		
File No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC		
Title: Galistoga-straps		
Size	Document Number	Rev
Custom	A&J/F	2.0
Date: 5/15/2007	Sheet 13 of 63	


<< Kennedy\_Zhang >>

+1.8V  
+3VS  
9.12,15,38,53  
6.7,9,11,13,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61



Layout Note: Place these Caps near SO DIMM 0



**ASUSTek COMPUTER INC.** 

File: **DDR2 SO-DIMM0**

Size: **A8/JF**

Date: 6/6/2007

Sheet 14 of 63

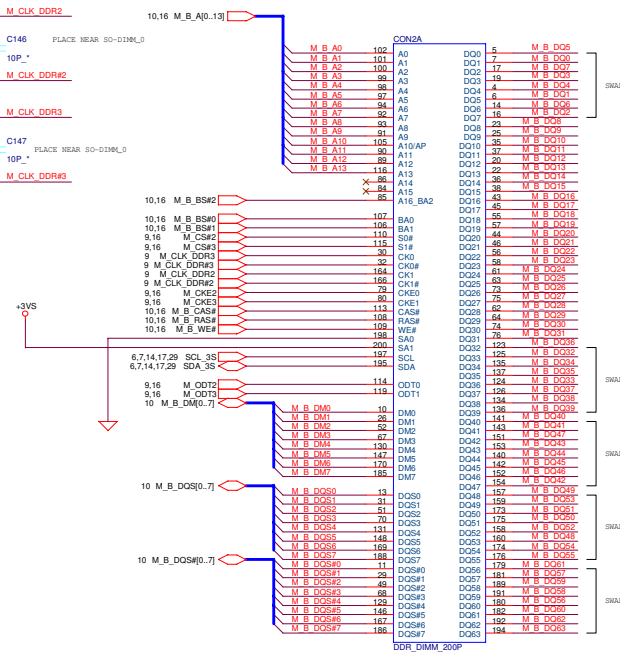
Rev 2.0

<< Kennedy\_Zhang >>

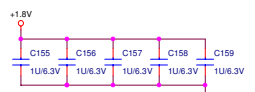
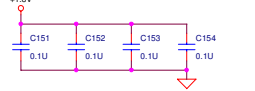
+1.8V  
+3VS  
+5V

9.12,14,38,53  
6.7,8,11,13,14,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61  
17,19,25,28,32,36,38,40,41,59,61

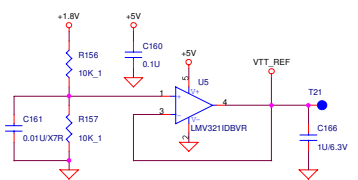
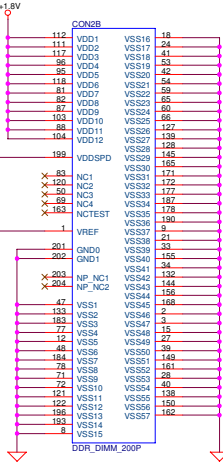
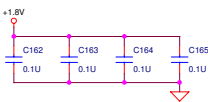
10 M\_B\_DQ0\_63 M\_B\_DQ0\_63



Layout Note: Place these Caps near SO DIMM 0

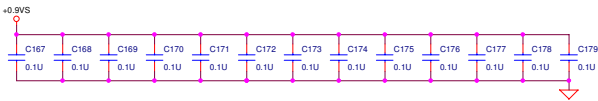


Layout Note: Place these High-Freq decoupling Caps near the GMCH

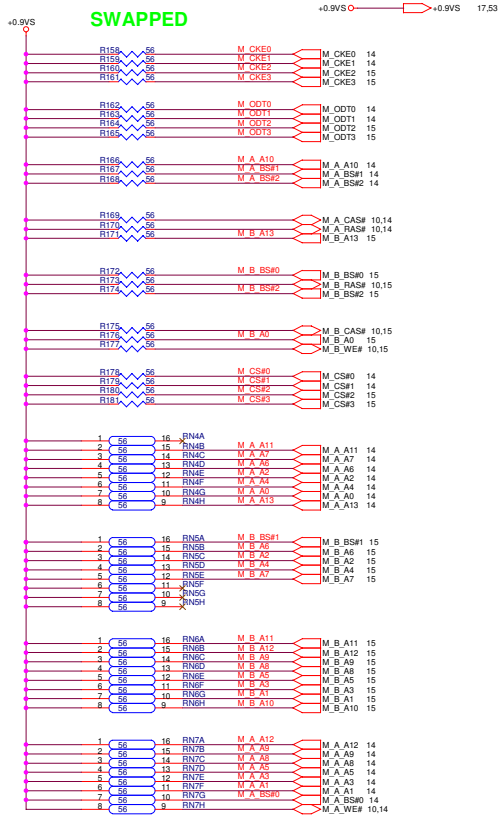
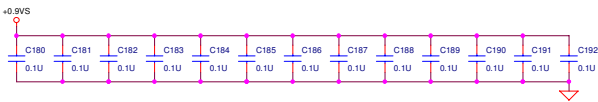



ASUSTek COMPUTER INC. ASUS  
File No. 150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC  
File: DDR2 SO-DIMM1  
Size: Document Number: A&J/F Rev: 2.0  
Date: 8/8/2007 Sheet: 15 of 63

<< Kennedy\_Zhang >>



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



**ASUSTek COMPUTER INC.** 

File: **DDR2 ADDRESS TERMINATION**

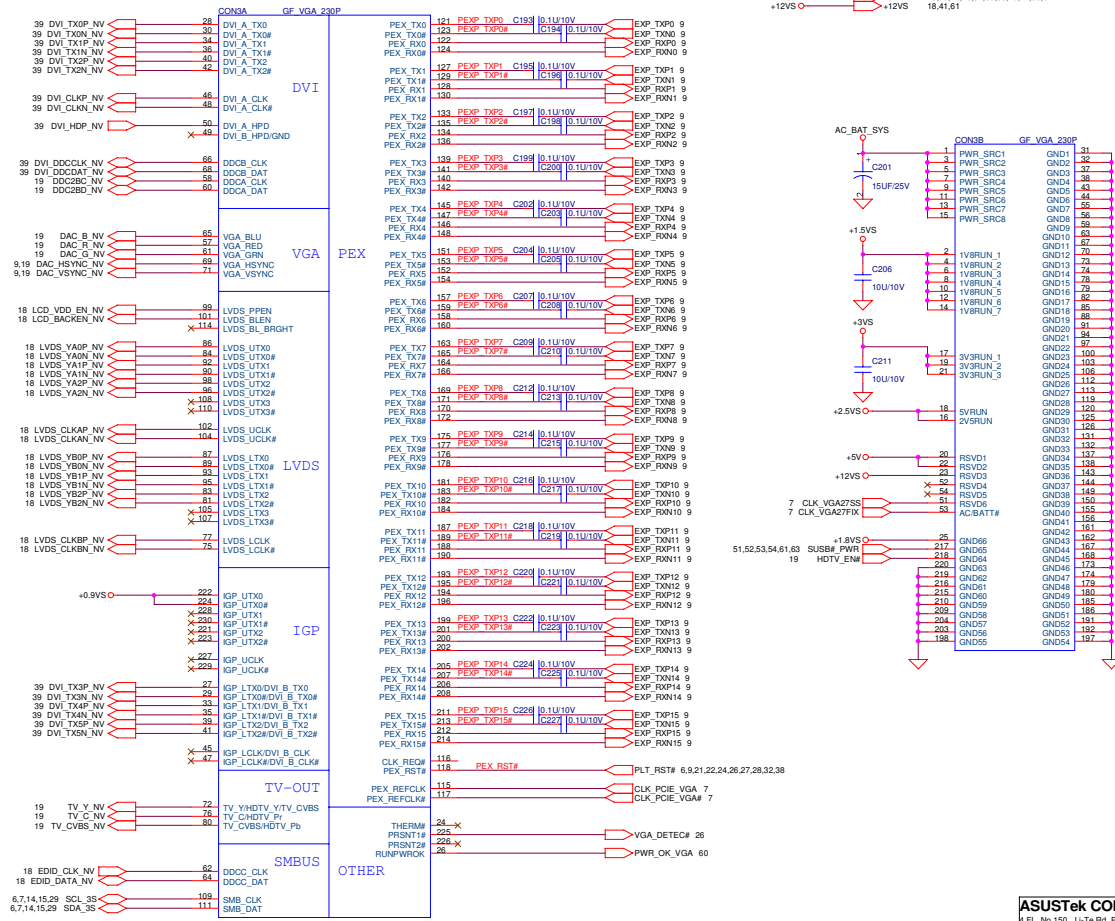
Size: **A8J/F**

Date: 8/8/2007

Sheet 16 of 63

<< Kennedy\_Zhang >>





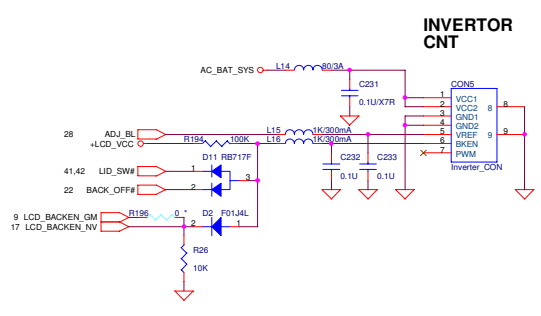
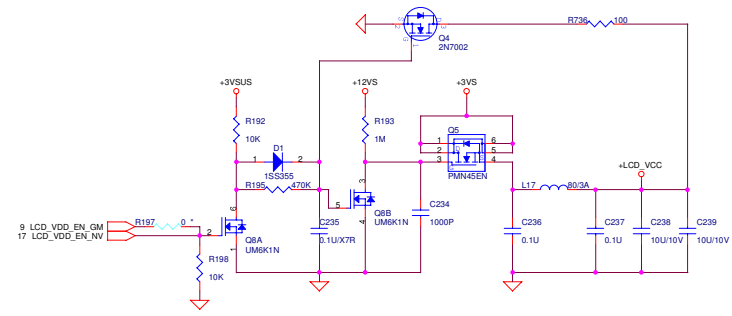
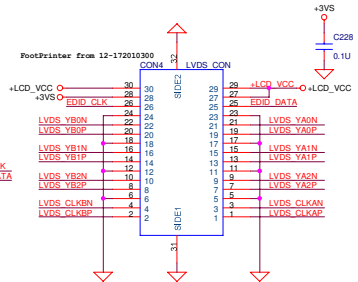
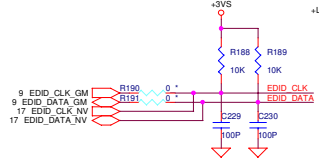
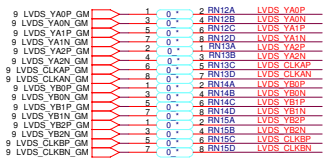
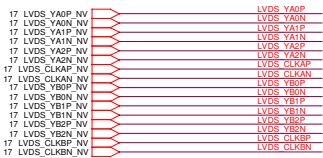
**ASUSTek COMPUTER INC.**

File: **VGA CONN**

Sub Customer:	Document Number:	Rev:
AS/JF		Z.0

Date: 2007.03.03 Sheet 17 of 63

<< Kennedy\_Zhang >>



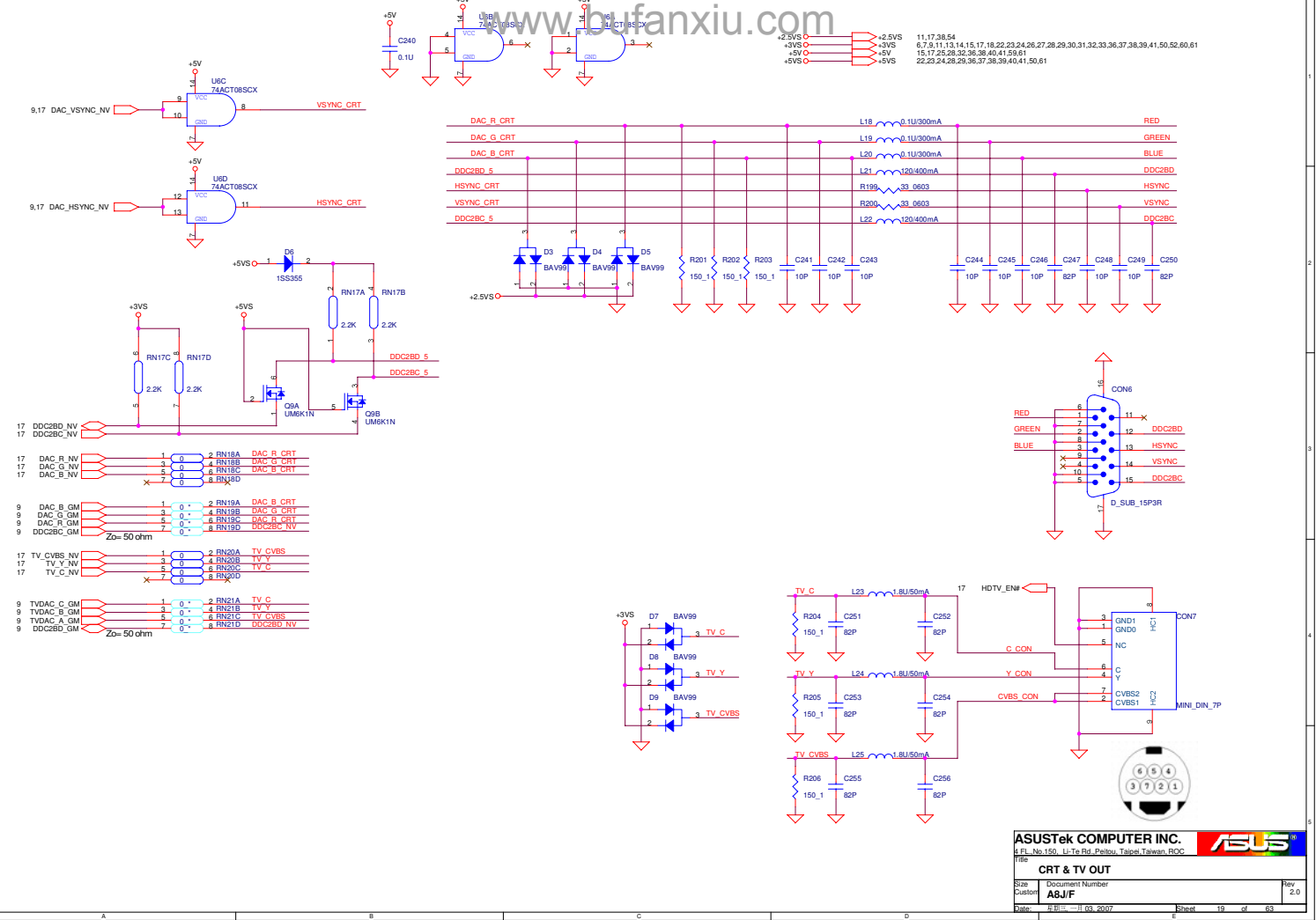
ASUSTek COMPUTER INC.

File: LVDS\_INVERTER\_CONN

Rev: 2.0

Date: 2007.03.03

<< Kennedy\_Zhang >>



**ASUSTek COMPUTER INC.**

File: **CRT & TV OUT**

Size: **A8J/F**

Customer: **A8J/F**

Date: 8/18/2007

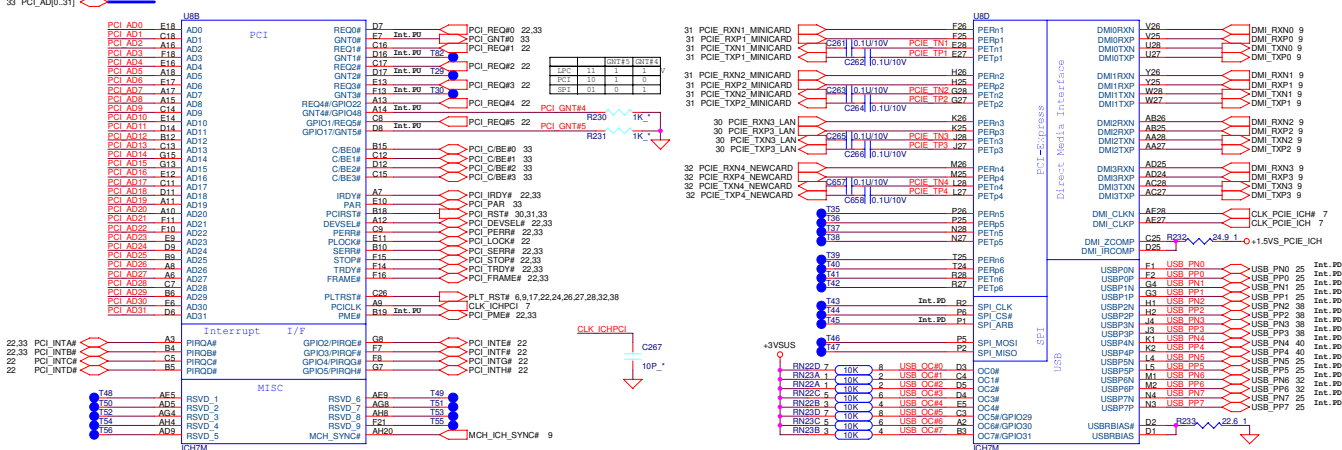
Sheet: 19 of 63

Rev: 2.0

<< Kennedy\_Zhang >>



33 PCI\_AD0..31



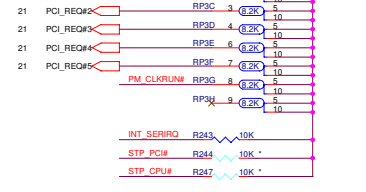
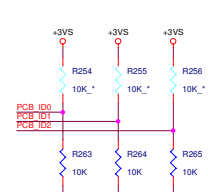
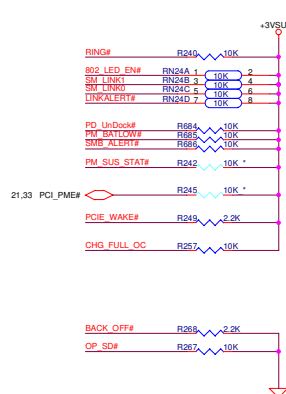
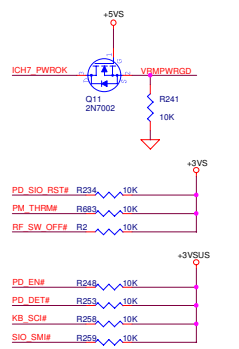
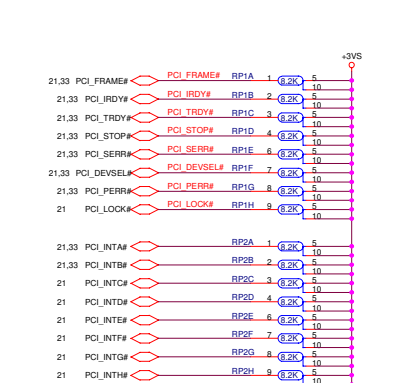
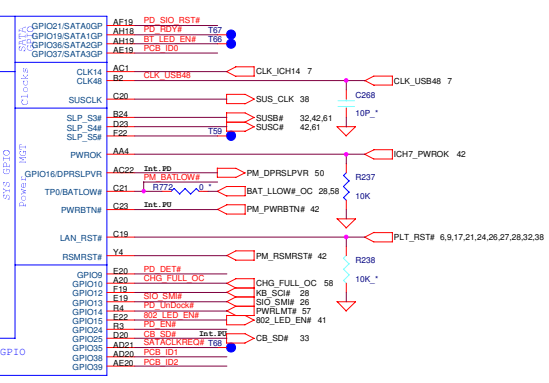
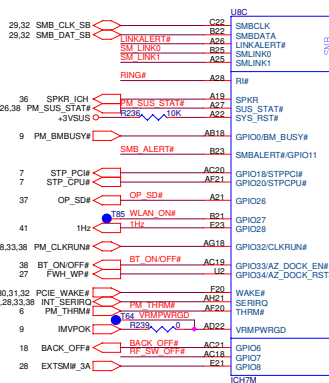
**ASUSTek COMPUTER INC.**

File: **ICH7M-PCI,PCI-E,USB**

Sub: **Customer** Document Number: **A8J/F** Rev: **2.0**

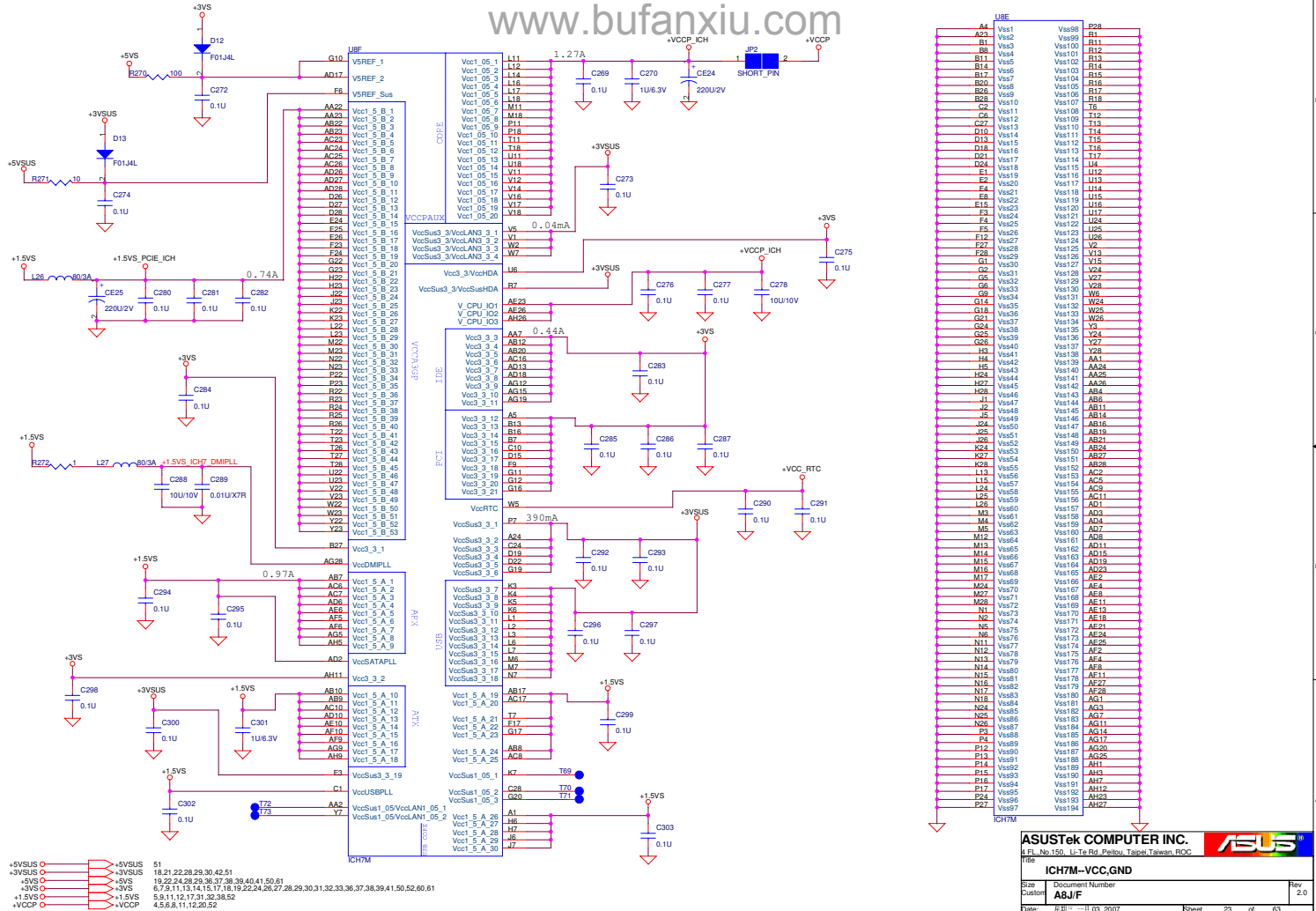
Date: **2007.03.03** Sheet: **21** of **63**

<< Kennedy\_Zhang >>

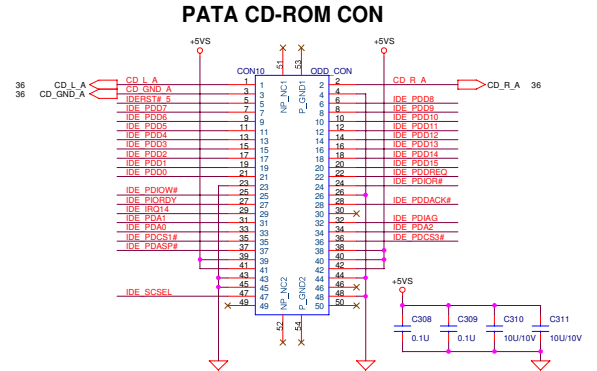
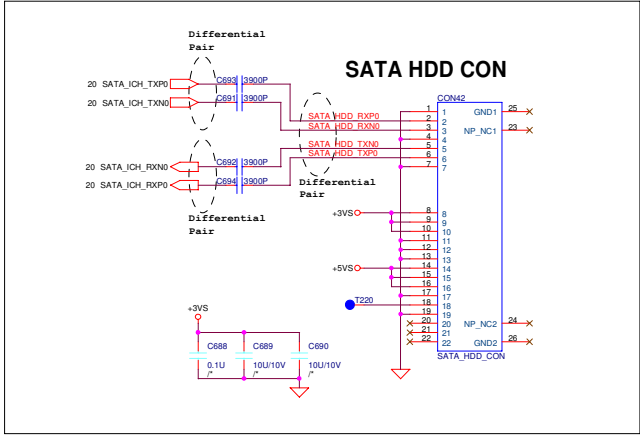
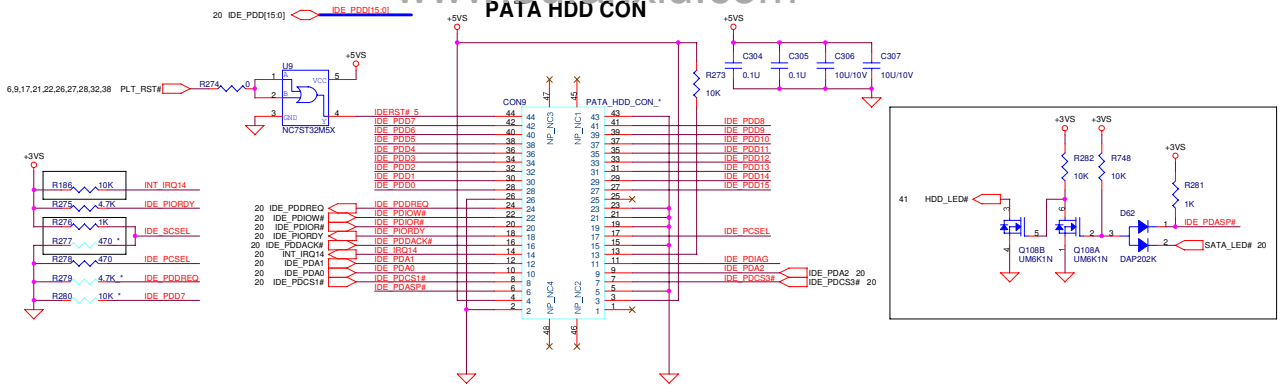


ASUSTek COMPUTER INC. ASUS  
File: ICH7M-GPIO  
Size: 2.0  
Customer: A&J/F  
Date: 03/09/2007 Sheet 22 of 63

<< Kennedy\_Zhang >>



Pin	Label	Label
A4	Vsb99	P28
A22	Vsb99	R1
B1	Vsb99	R10
B8	Vsb99	R12
B11	Vsb99	R14
B14	Vsb99	R16
B17	Vsb99	R18
B20	Vsb99	R20
B23	Vsb99	R22
B26	Vsb99	R24
B29	Vsb99	R26
B32	Vsb99	R28
B35	Vsb99	R30
B38	Vsb99	R32
B41	Vsb99	R34
B44	Vsb99	R36
B47	Vsb99	R38
B50	Vsb99	R40
B53	Vsb99	R42
B56	Vsb99	R44
B59	Vsb99	R46
B62	Vsb99	R48
B65	Vsb99	R50
B68	Vsb99	R52
B71	Vsb99	R54
B74	Vsb99	R56
B77	Vsb99	R58
B80	Vsb99	R60
B83	Vsb99	R62
B86	Vsb99	R64
B89	Vsb99	R66
B92	Vsb99	R68
B95	Vsb99	R70
B98	Vsb99	R72
B101	Vsb99	R74
B104	Vsb99	R76
B107	Vsb99	R78
B110	Vsb99	R80
B113	Vsb99	R82
B116	Vsb99	R84
B119	Vsb99	R86
B122	Vsb99	R88
B125	Vsb99	R90
B128	Vsb99	R92
B131	Vsb99	R94
B134	Vsb99	R96
B137	Vsb99	R98
B140	Vsb99	R100
B143	Vsb99	R102
B146	Vsb99	R104
B149	Vsb99	R106
B152	Vsb99	R108
B155	Vsb99	R110
B158	Vsb99	R112
B161	Vsb99	R114
B164	Vsb99	R116
B167	Vsb99	R118
B170	Vsb99	R120
B173	Vsb99	R122
B176	Vsb99	R124
B179	Vsb99	R126
B182	Vsb99	R128
B185	Vsb99	R130
B188	Vsb99	R132
B191	Vsb99	R134
B194	Vsb99	R136
B197	Vsb99	R138
B200	Vsb99	R140
B203	Vsb99	R142
B206	Vsb99	R144
B209	Vsb99	R146
B212	Vsb99	R148
B215	Vsb99	R150
B218	Vsb99	R152
B221	Vsb99	R154
B224	Vsb99	R156
B227	Vsb99	R158
B230	Vsb99	R160
B233	Vsb99	R162
B236	Vsb99	R164
B239	Vsb99	R166
B242	Vsb99	R168
B245	Vsb99	R170
B248	Vsb99	R172
B251	Vsb99	R174
B254	Vsb99	R176
B257	Vsb99	R178
B260	Vsb99	R180
B263	Vsb99	R182
B266	Vsb99	R184
B269	Vsb99	R186
B272	Vsb99	R188
B275	Vsb99	R190
B278	Vsb99	R192
B281	Vsb99	R194
B284	Vsb99	R196
B287	Vsb99	R198
B290	Vsb99	R200
B293	Vsb99	R202
B296	Vsb99	R204
B299	Vsb99	R206
B302	Vsb99	R208
B305	Vsb99	R210
B308	Vsb99	R212
B311	Vsb99	R214
B314	Vsb99	R216
B317	Vsb99	R218
B320	Vsb99	R220
B323	Vsb99	R222
B326	Vsb99	R224
B329	Vsb99	R226
B332	Vsb99	R228
B335	Vsb99	R230
B338	Vsb99	R232
B341	Vsb99	R234
B344	Vsb99	R236
B347	Vsb99	R238
B350	Vsb99	R240
B353	Vsb99	R242
B356	Vsb99	R244
B359	Vsb99	R246
B362	Vsb99	R248
B365	Vsb99	R250
B368	Vsb99	R252
B371	Vsb99	R254
B374	Vsb99	R256
B377	Vsb99	R258
B380	Vsb99	R260
B383	Vsb99	R262
B386	Vsb99	R264
B389	Vsb99	R266
B392	Vsb99	R268
B395	Vsb99	R270
B398	Vsb99	R272
B401	Vsb99	R274
B404	Vsb99	R276
B407	Vsb99	R278
B410	Vsb99	R280
B413	Vsb99	R282
B416	Vsb99	R284
B419	Vsb99	R286
B422	Vsb99	R288
B425	Vsb99	R290
B428	Vsb99	R292
B431	Vsb99	R294
B434	Vsb99	R296
B437	Vsb99	R298
B440	Vsb99	R300
B443	Vsb99	R302
B446	Vsb99	R304
B449	Vsb99	R306
B452	Vsb99	R308
B455	Vsb99	R310
B458	Vsb99	R312
B461	Vsb99	R314
B464	Vsb99	R316
B467	Vsb99	R318
B470	Vsb99	R320
B473	Vsb99	R322
B476	Vsb99	R324
B479	Vsb99	R326
B482	Vsb99	R328
B485	Vsb99	R330
B488	Vsb99	R332
B491	Vsb99	R334
B494	Vsb99	R336
B497	Vsb99	R338
B500	Vsb99	R340
B503	Vsb99	R342
B506	Vsb99	R344
B509	Vsb99	R346
B512	Vsb99	R348
B515	Vsb99	R350
B518	Vsb99	R352
B521	Vsb99	R354
B524	Vsb99	R356
B527	Vsb99	R358
B530	Vsb99	R360
B533	Vsb99	R362
B536	Vsb99	R364
B539	Vsb99	R366
B542	Vsb99	R368
B545	Vsb99	R370
B548	Vsb99	R372
B551	Vsb99	R374
B554	Vsb99	R376
B557	Vsb99	R378
B560	Vsb99	R380
B563	Vsb99	R382
B566	Vsb99	R384
B569	Vsb99	R386
B572	Vsb99	R388
B575	Vsb99	R390
B578	Vsb99	R392
B581	Vsb99	R394
B584	Vsb99	R396
B587	Vsb99	R398
B590	Vsb99	R400
B593	Vsb99	R402
B596	Vsb99	R404
B599	Vsb99	R406
B602	Vsb99	R408
B605	Vsb99	R410
B608	Vsb99	R412
B611	Vsb99	R414
B614	Vsb99	R416
B617	Vsb99	R418
B620	Vsb99	R420
B623	Vsb99	R422
B626	Vsb99	R424
B629	Vsb99	R426
B632	Vsb99	R428
B635	Vsb99	R430
B638	Vsb99	R432
B641	Vsb99	R434
B644	Vsb99	R436
B647	Vsb99	R438
B650	Vsb99	R440
B653	Vsb99	R442
B656	Vsb99	R444
B659	Vsb99	R446
B662	Vsb99	R448
B665	Vsb99	R450
B668	Vsb99	R452
B671	Vsb99	R454
B674	Vsb99	R456
B677	Vsb99	R458
B680	Vsb99	R460
B683	Vsb99	R462
B686	Vsb99	R464
B689	Vsb99	R466
B692	Vsb99	R468
B695	Vsb99	R470
B698	Vsb99	R472
B701	Vsb99	R474
B704	Vsb99	R476
B707	Vsb99	R478
B710	Vsb99	R480
B713	Vsb99	R482
B716	Vsb99	R484
B719	Vsb99	R486
B722	Vsb99	R488
B725	Vsb99	R490
B728	Vsb99	R492
B731	Vsb99	R494
B734	Vsb99	R496
B737	Vsb99	R498
B740	Vsb99	R500
B743	Vsb99	R502
B746	Vsb99	R504
B749	Vsb99	R506
B752	Vsb99	R508
B755	Vsb99	R510
B758	Vsb99	R512
B761	Vsb99	R514
B764	Vsb99	R516
B767	Vsb99	R518
B770	Vsb99	R520
B773	Vsb99	R522
B776	Vsb99	R524
B779	Vsb99	R526
B782	Vsb99	R528
B785	Vsb99	R530
B788	Vsb99	R532
B791	Vsb99	R534
B794	Vsb99	R536
B797	Vsb99	R538
B800	Vsb99	R540
B803	Vsb99	R542
B806	Vsb99	R544
B809	Vsb99	R546
B812	Vsb99	R548
B815	Vsb99	R550
B818	Vsb99	R552
B821	Vsb99	R554
B824	Vsb99	R556
B827	Vsb99	R558
B830	Vsb99	R560
B833	Vsb99	R562
B836	Vsb99	R564
B839	Vsb99	R566
B842	Vsb99	R568
B845	Vsb99	R570
B848	Vsb99	R572
B851	Vsb99	R574
B854	Vsb99	R576
B857	Vsb99	R578
B860	Vsb99	R580
B863	Vsb99	R582
B866	Vsb99	R584
B869	Vsb99	R586
B872	Vsb99	R588
B875	Vsb99	R590
B878	Vsb99	R592
B881	Vsb99	R594
B884	Vsb99	R596
B887	Vsb99	R598
B890	Vsb99	R600
B893	Vsb99	R602
B896	Vsb99	R604
B899	Vsb99	R606
B902	Vsb99	R608
B905	Vsb99	R610
B908	Vsb99	R612
B911	Vsb99	R614
B914	Vsb99	R616
B917	Vsb99	R618
B920	Vsb99	R620
B923	Vsb99	R622
B926	Vsb99	R624
B929	Vsb99	R626
B932	Vsb99	R628
B935	Vsb99	R630
B938	Vsb99	R632
B941	Vsb99	R634
B944	Vsb99	R636
B947	Vsb99	R638
B950	Vsb99	R640
B953	Vsb99	R642
B956	Vsb99	R644
B959	Vsb99	R646
B962	Vsb99	R648
B965	Vsb99	R650
B968	Vsb99	R652
B971	Vsb99	R654
B974	Vsb99	R656
B977	Vsb99	R658
B980	Vsb99	R660
B983	Vsb99	R662
B986	Vsb99	R664
B989	Vsb99	R666
B992	Vsb99	R668
B995	Vsb99	R670
B998	Vsb99	R672
B1001	Vsb99	R674
B1004	Vsb99	R676
B1007	Vsb99	R678
B1010	Vsb99	R680
B1013	Vsb99	R682
B1016	Vsb99	R684
B1019	Vsb99	R686
B1022	Vsb99	R688
B1025	Vsb99	R690
B1028	Vsb99	R692
B1031	Vsb99	R694
B1034	Vsb99	R696
B1037	Vsb99	R698
B1040	Vsb99	R700
B1043	Vsb99	R702
B1046	Vsb99	R704
B1049	Vsb99	R706
B1052	Vsb99	R708
B1055	Vsb99	R710
B1058	Vsb99	R712
B1061	Vsb99	R714
B1064	Vsb99	R716
B1067	Vsb99	R718
B1070	Vsb99	R720
B1073	Vsb99	R722
B1076	Vsb99	R724
B1079	Vsb99	R726
B1082	Vsb99	R728
B1085	Vsb99	R730
B1088	Vsb99	R732
B1091	Vsb99	R734
B1094	Vsb99	R736
B1097	Vsb99	R738
B1100	Vsb99	R740
B1103	Vsb99	R742
B1106	Vsb99	R744
B1109	Vsb99	R746
B1112	Vsb99	R748
B1115	Vsb99	R750
B1118	Vsb99	R752
B1121	Vsb99	R754
B1124	Vsb99	R756
B1127	Vsb99	R758
B1130	Vsb99	R760
B1133	Vsb99	R762
B1136	Vsb99	R764
B1139	Vsb99	R766
B1142	Vsb99	R768
B1145	Vsb99	R770
B1148	Vsb99	R772
B1151	Vsb99	R774
B1154	Vsb99	R776
B1157	Vsb99	R778
B1160	Vsb99	R780
B1163	Vsb99	R782
B1166	Vsb99	R784
B1169	Vsb99	R786
B1172	Vsb99	R788
B1175	Vsb99	R790
B1178	Vsb99	R792
B1181	Vsb99	R794
B1184	Vsb99	R796
B1187	Vsb99	R798
B1190	Vsb99	R800
B1193	Vsb99	R802
B1196	Vsb99	R804
B1199	Vsb99	R806
B1202	Vsb99	R808
B1205	Vsb99	R810
B1208	Vsb99	R812
B1211	Vsb99	R814
B1214	Vsb99	R816
B1217	Vsb99	R818
B		



+3VS → +3VS  
 +5VS → +5VS  
 +5V → +5V  
 6,9,11,13,14,15,17,18,19,22,23,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61  
 19,22,23,28,29,36,37,38,39,40,41,50,61  
 15,17,19,29,32,36,38,40,41,59,61

ASUSTek COMPUTER INC.

File: **HDD & CD-ROM CONN**

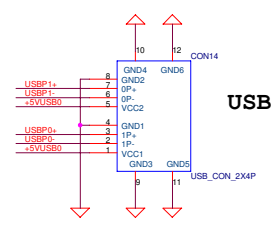
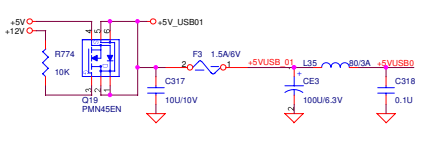
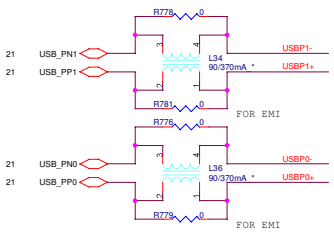
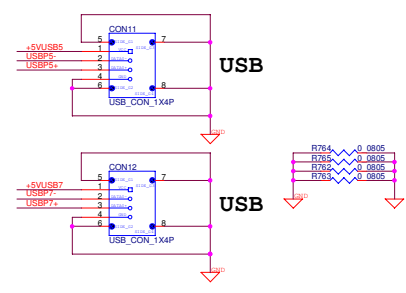
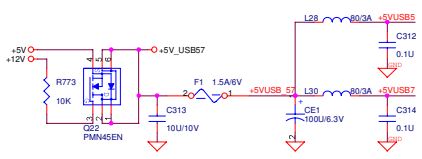
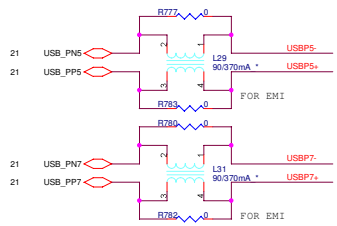
Sub Customer: **A8J/F**

Date: 2007.03.03

Sheet 24 of 63

<< Kennedy\_Zhang >>





+5V  $\rightarrow$  +5V 15,17,19,28,32,36,38,40,41,59,61

**ASUSTek COMPUTER INC.**  
 # FL. No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC

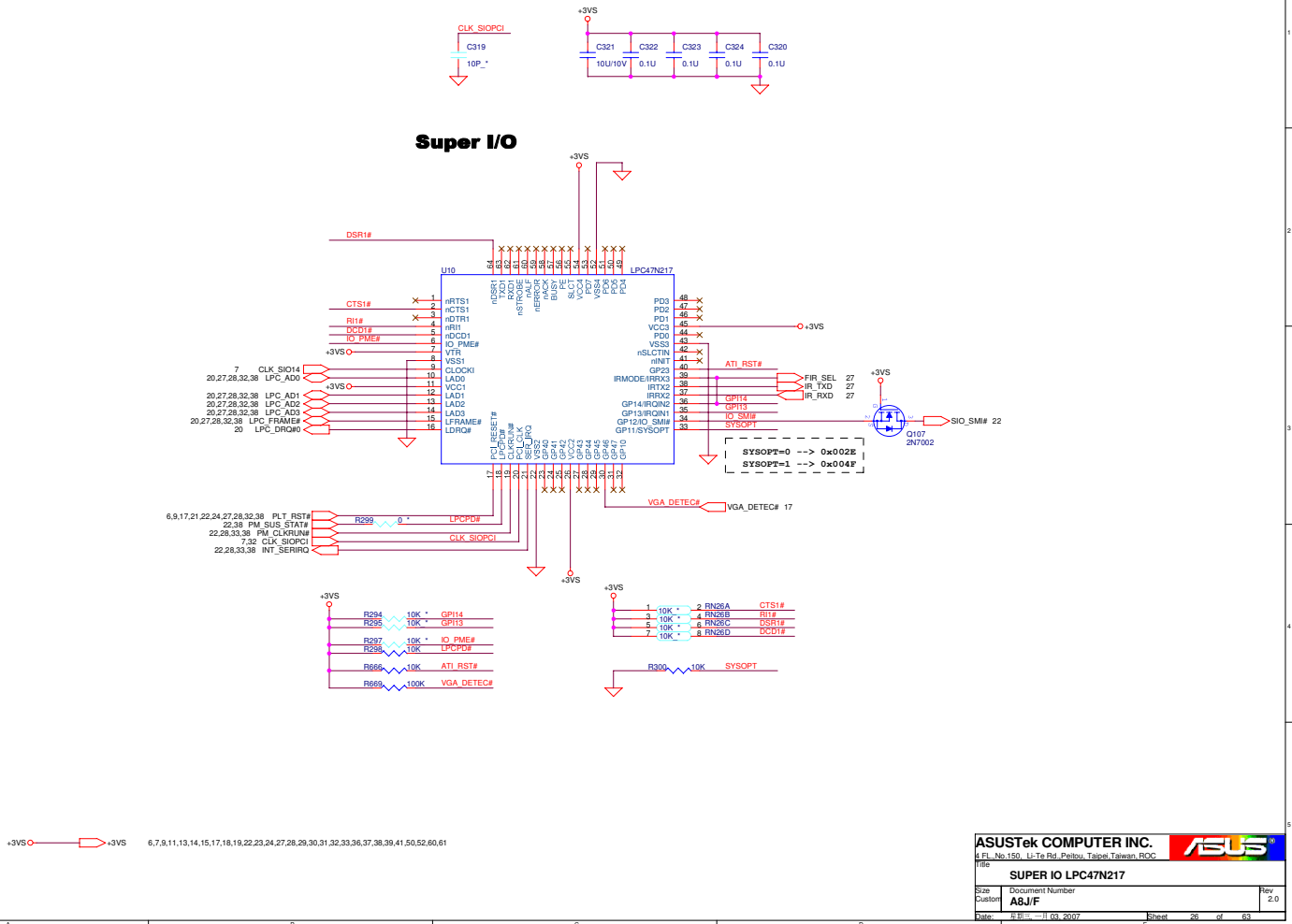
**ASUS**

**USB PORTS**

Size	Document Number	Rev
Custom	<b>A&amp;J/F</b>	2.0

Date: 5/5/2007 Sheet 25 of 63

<< Kennedy\_Zhang >>



**ASUSTek COMPUTER INC.**  
 # FL: No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC

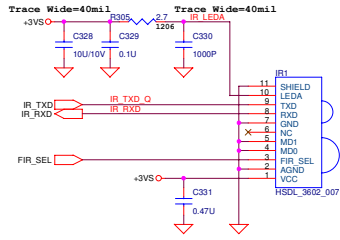
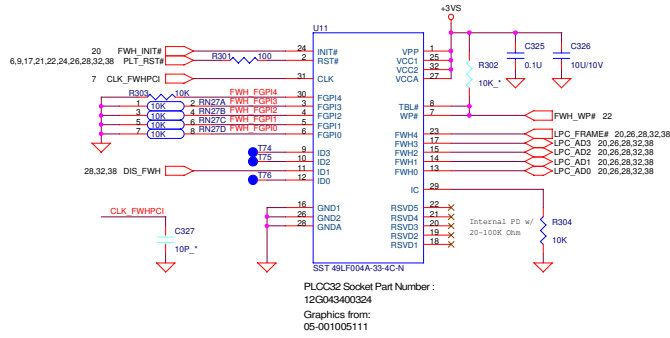
**ASUS**

File: **SUPER IO LPC47N217**

Size	Document Number	Rev
Custom	<b>A&amp;J/F</b>	2.0

Date: 5/5/2007 Sheet 28 of 63

<< Kennedy\_Zhang >>



+3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61

**ASUSTek COMPUTER INC.**

ASUS

File: BIOS\_IR

Size	Document Number	Rev
Custom	A&J/F	2.0

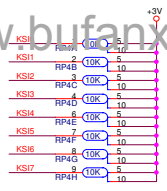
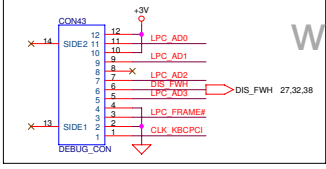
Date: 8/8/2007 Sheet 27 of 63

<< Kennedy\_Zhang >>

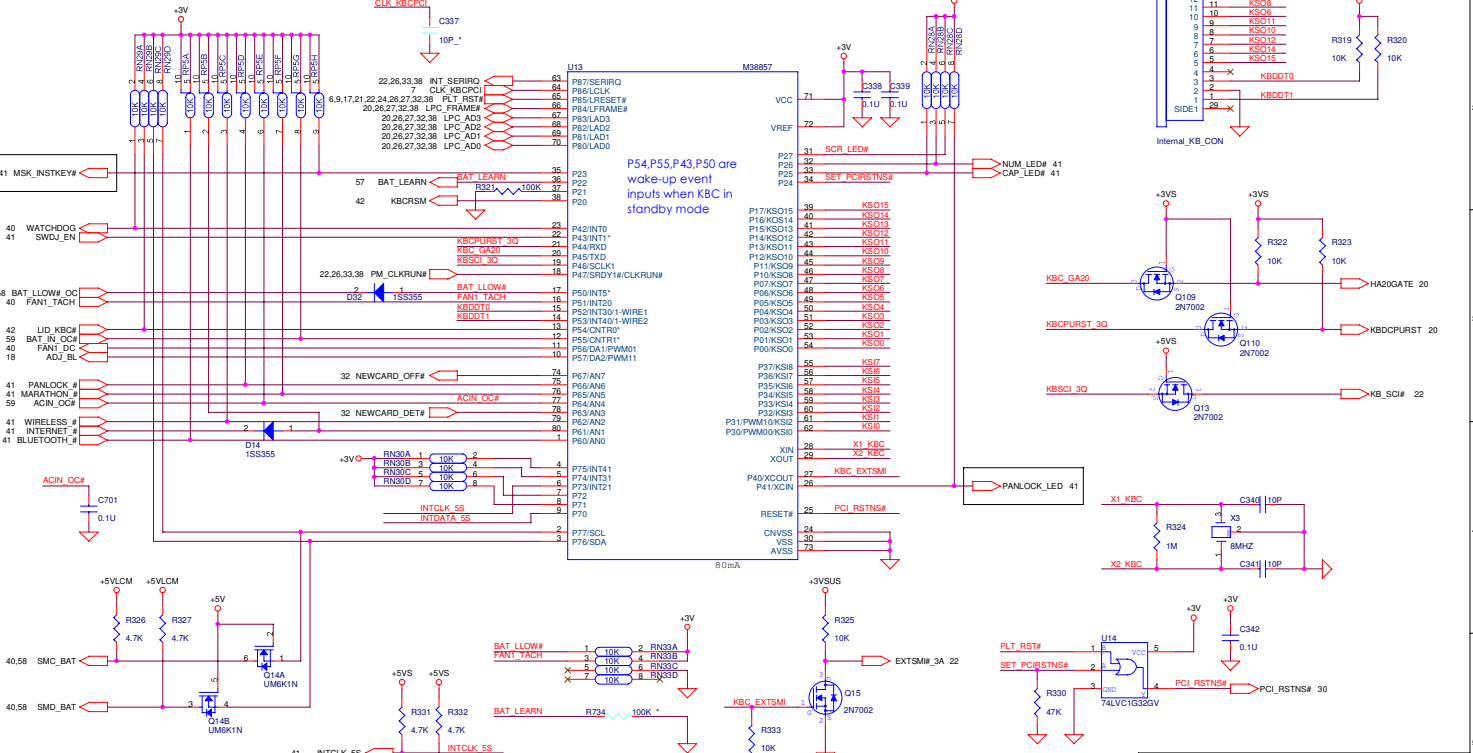
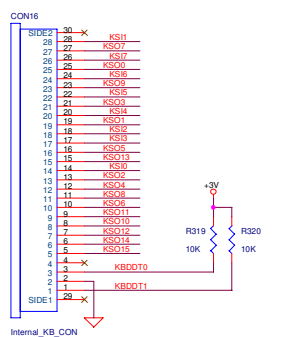
P2.1 Low : Power Button Override disable  
Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event  
inputs when KBC in standby mode

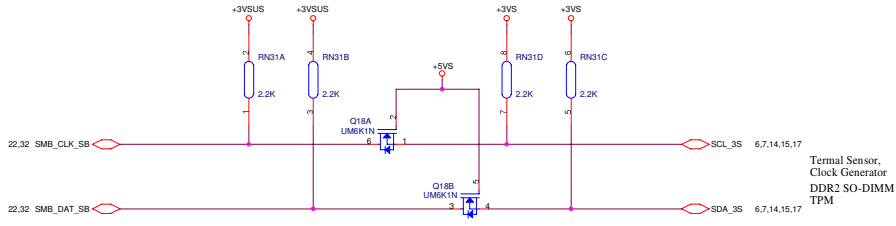
EC should set  
OP\_SD low in S3,  
keep from  
leakage



KBDOT1	KBDOT0	MatLxLx
1	1	US
1	0	UK
0	1	JP




ICH7-M



Terminal Sensor,  
Clock Generator  
DDR2 SO-DIMM  
TPM

+3VA	20,38,41,42,54,59,63
+5VA	6,51,54
+3VSUS	18,21,22,23,28,30,42,51
+5VSUS	23,51
+0.9VS	15,17,53
+VCCP	4,5,6,8,11,12,20,23,52
+1.5VS	5,9,11,12,17,23,31,32,38,52
+2.5VCC	11,17,19,28,54
+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,30,31,32,33,36,37,38,39,41,50,52,60,61
+5VS	19,22,23,24,26,36,37,38,39,40,41,50,61
+12VS	17,18,41,61
+1.8V	9,12,14,15,38,53
+3V	28,30,31,32,34,37,38,42,54,61
+5V	15,17,19,25,29,32,35,38,40,41,59,61
+12V	25,34,37,40,61
+VCCORE	5,6,50
+5VLCM	28,57,58,59,60

**ASUSTek COMPUTER INC.** 

File: No.150\_Li-Te Rd., Peitou, Taipei, Taiwan, ROC

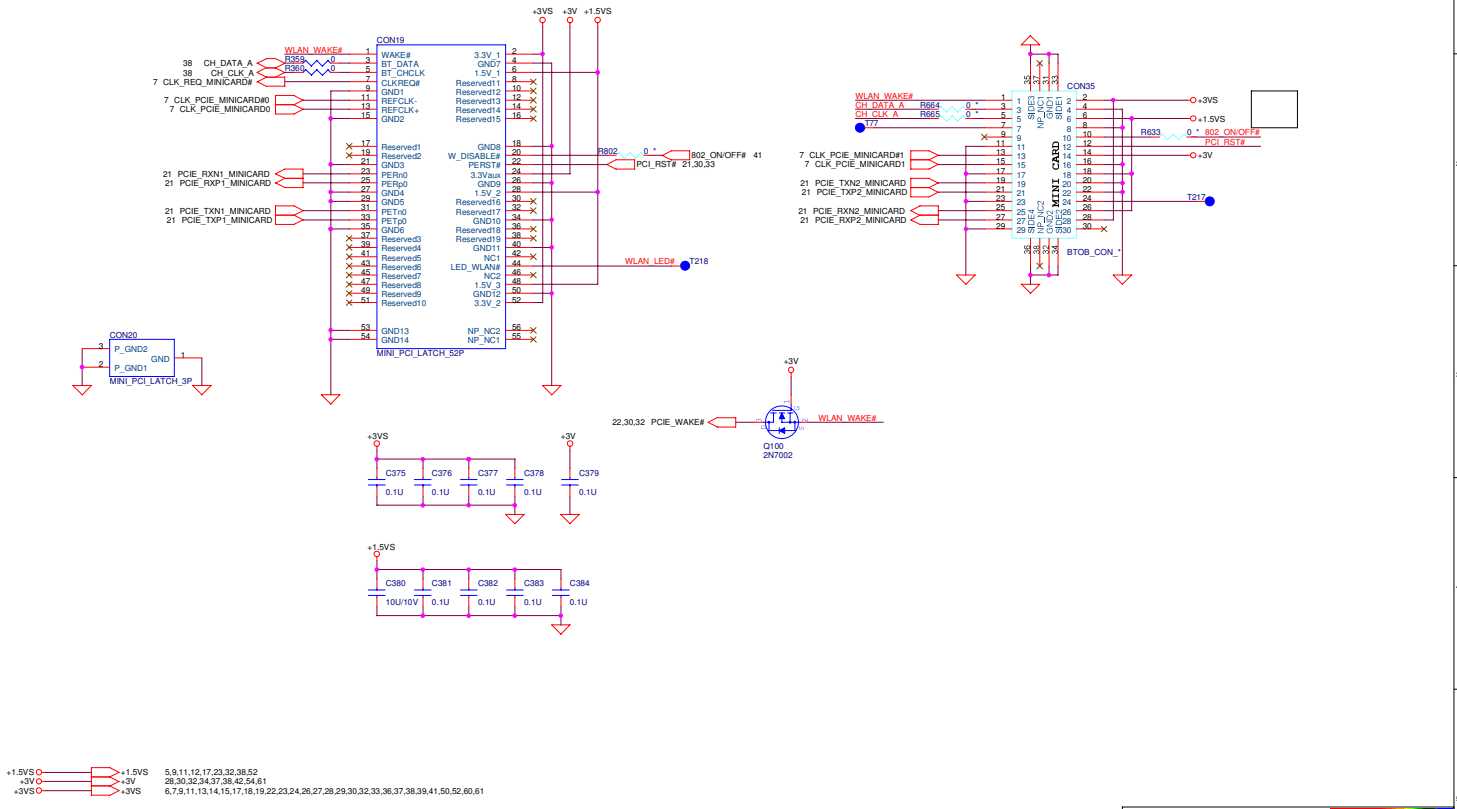
**SM BUS & POWER PORT**

Size	Document Number	Rev
Custom	<b>A&amp;J/F</b>	2.0

Date: 5/15/2007 Sheet 28 of 63

<< Kennedy\_Zhang >>



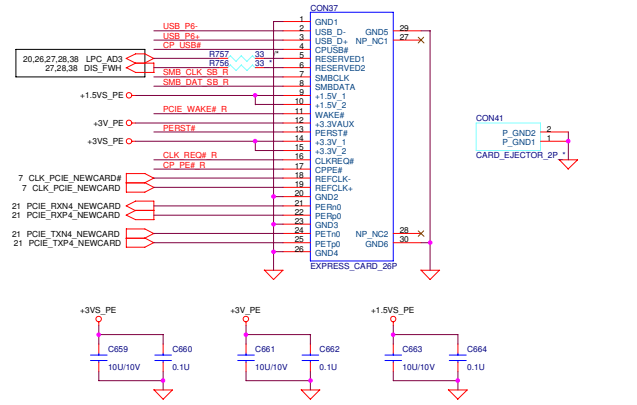
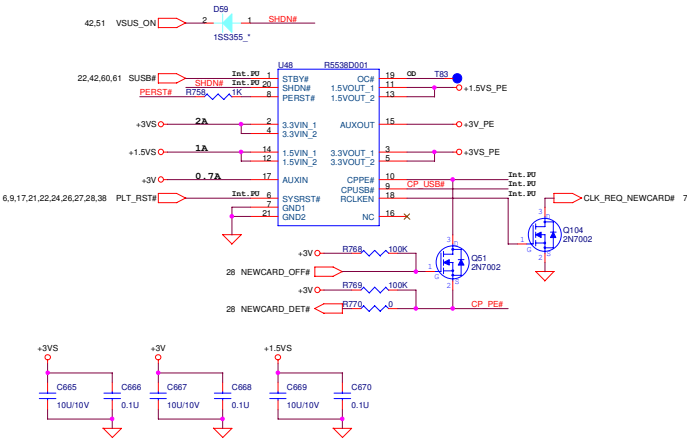
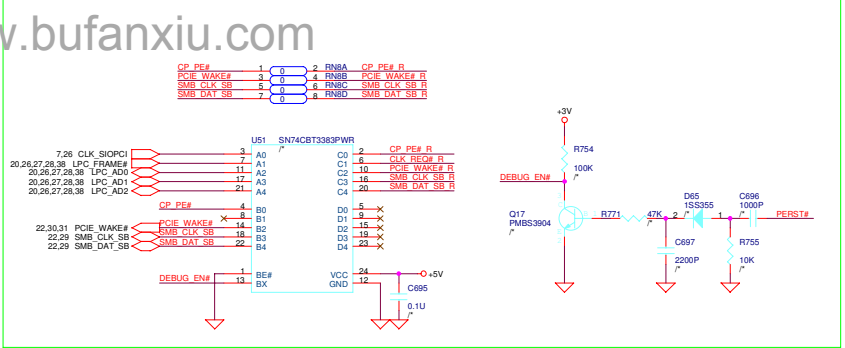
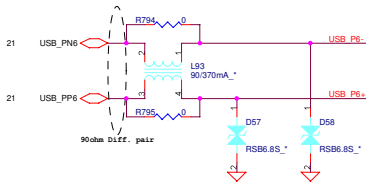


**ASUSTek COMPUTER INC.**  
 4 FL, No.150, Li-To Rd., Peitou, Taipei, Taiwan, ROC

**MINI CARD**

Rev	2.0
Doc No.	A6J/F
Date	03/03/2007
Sheet	31 of 63

<< Kennedy\_Zhang >>



+1.5V C	+1.5V	5,9,11,12,17,23,31,38,52
+3V C	+3V	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,33,36,37,38,39,41,50,52,60,61
+3V C	+3V	23,30,31,34,37,38,42,54,61

**ASUSTek COMPUTER INC.**

File: **NEW CARD**

Sub: **Document Number**

Customer: **A6J/F**

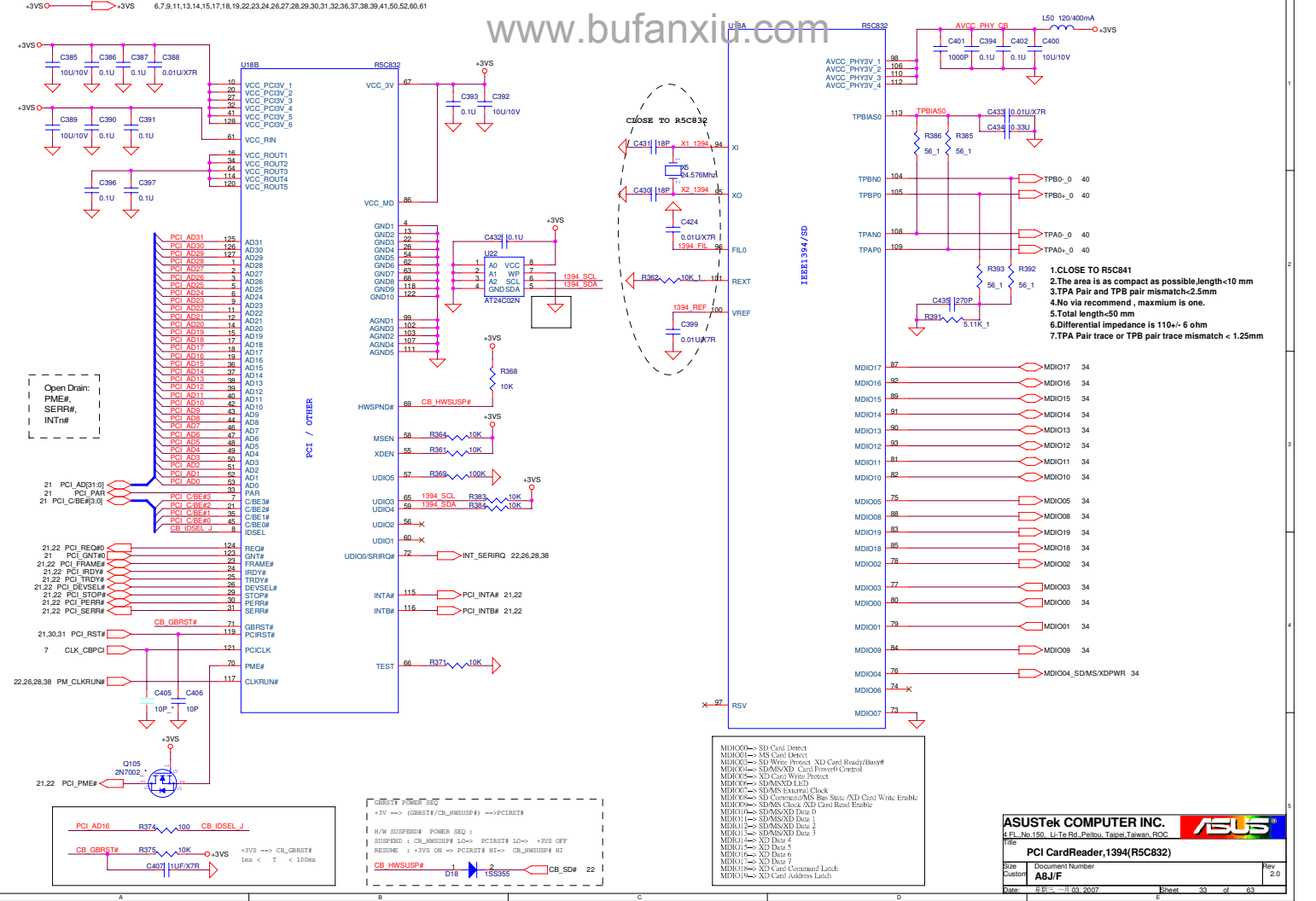
Date: 2007.03.03

Sheet: 32 of 63

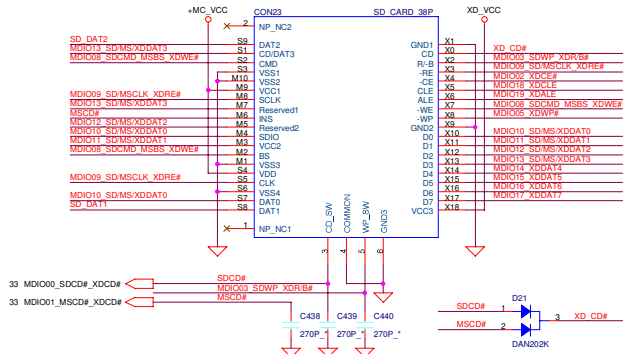
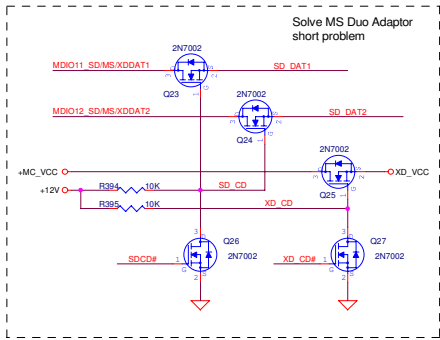
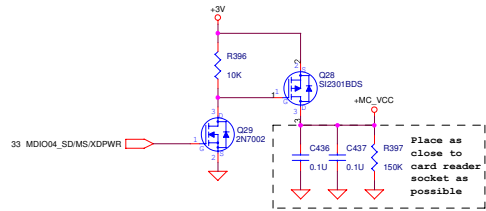
Rev: 2.0

<< Kennedy\_Zhang >>





<< Kennedy\_Zhang >>



**ASUSTek COMPUTER INC.**  
 # FL. No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC


**ASUS**

File: **4 IN 1 CONN**

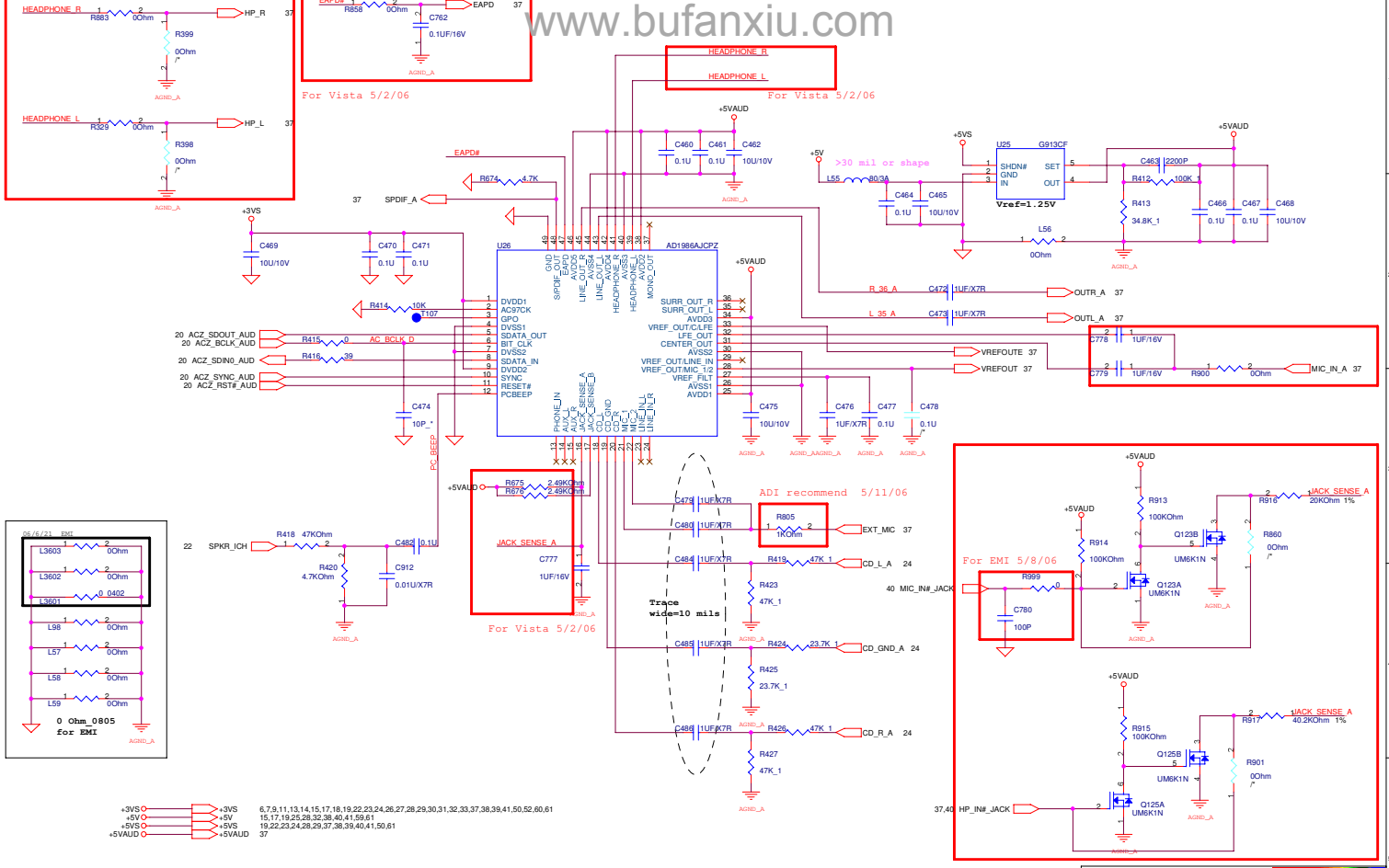
Size	Document Number	Rev
Customer	<b>A8JF</b>	2.0


Date: 8/8/2007 Sheet 34 of 63

<< Kennedy\_Zhang >>

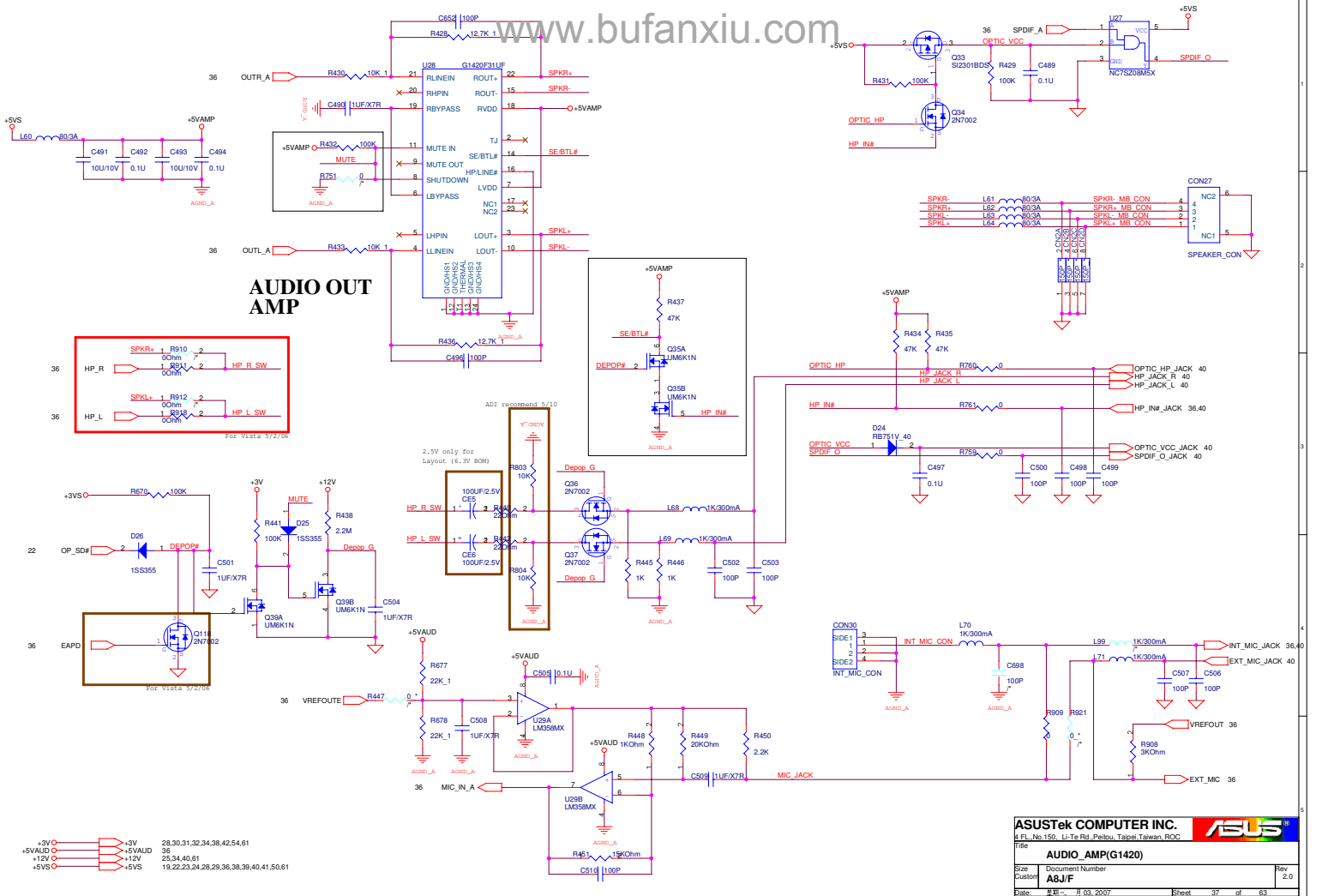
<b>ASUSTek COMPUTER INC.</b>		
4 FL, No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC		
Title		
Empty		
Size	Document Number	Rev
Custom	A&J/F	2.0
Date	8/8/07	Sheet 35 of 63

<< Kennedy\_Zhang >>

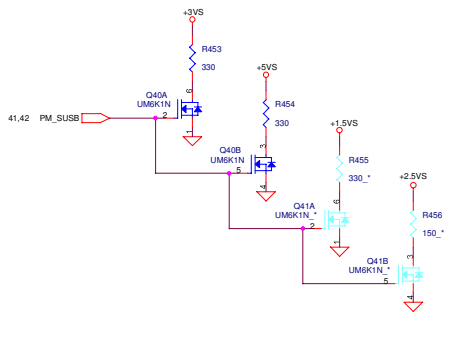
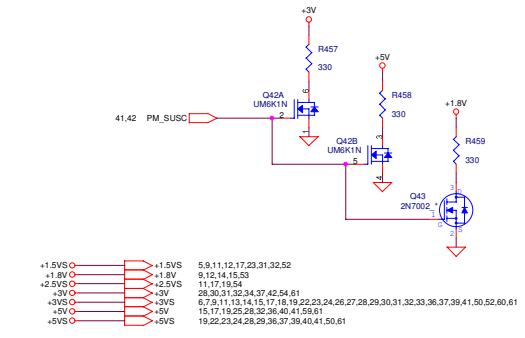
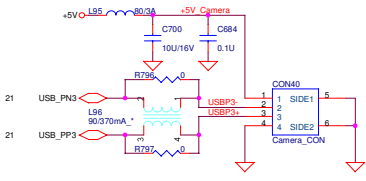
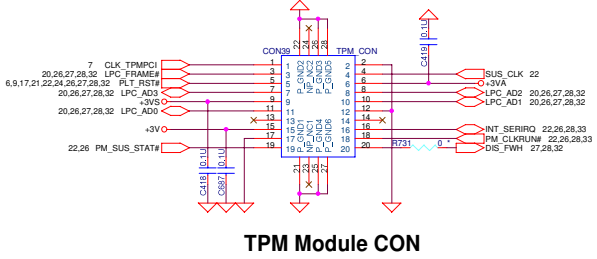
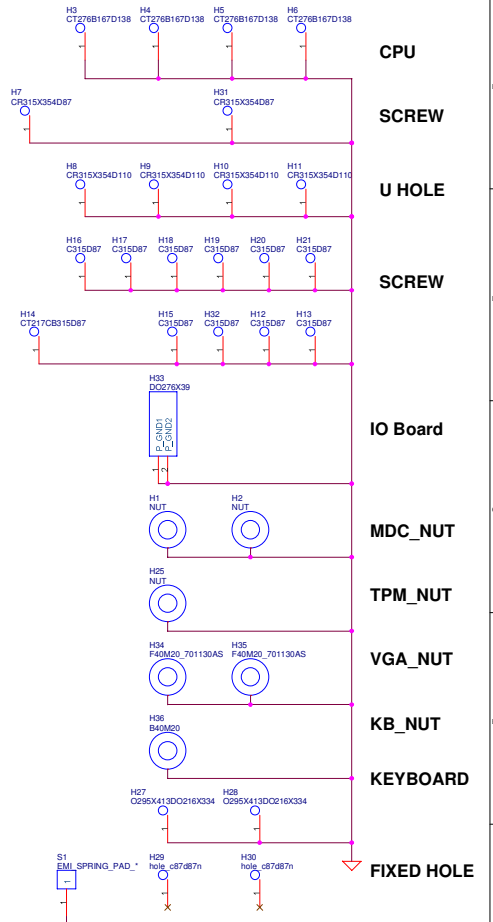
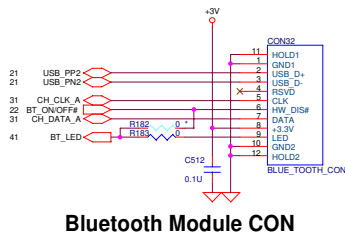
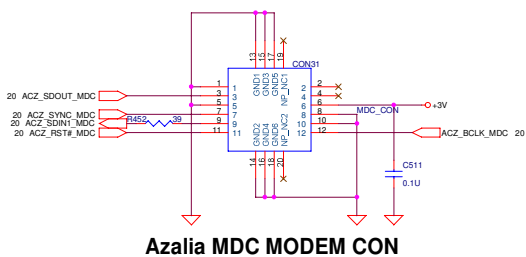


ASUSTek COMPUTER INC. 	
EPL No.150, Li-To Rd., Peitou, Taipei, Taiwan, ROC	
File: ADI1986A	
Sub: Document Number	Rev: 2.0
Customer: A6JF	
Date: 03.03.2007	Sheet: 36 of 63

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>



+1.5VS	→ +1.5VS	5,9,11,12,17,23,31,32,52
+1.8V	→ +1.8V	9,12,14,15,53
+2.5VS	→ +2.5VS	11,17,19,54
+3V	→ +3V	28,30,31,33,34,37,42,54,61
+3VS	→ +3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,39,41,50,52,60,61
+5V	→ +5V	15,17,19,25,28,32,36,40,41,56,61
+5VS	→ +5VS	19,22,23,24,28,29,36,37,39,40,41,50,61

**ASUSTek COMPUTER INC.**

File: MDC,B/T,TPM,Camera & DISCHG.HOLE

Size: A8/J/F

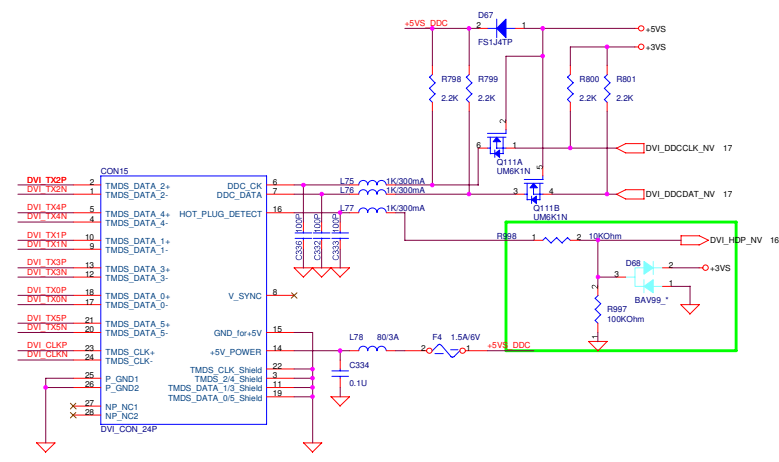
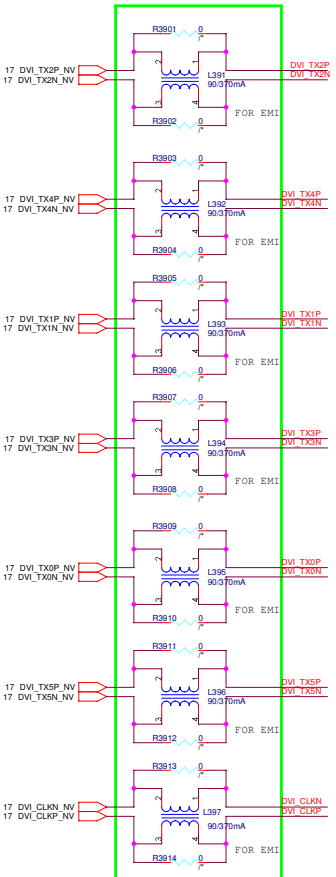
Rev: 2.0

Date: 8/8/2007


Sheet: 38 of 63

<< Kennedy\_Zhang >>

Add DVI Choke 09G092145000  
for EMI issue 2006.08.04



+5VS  $\rightarrow$  +5VS 19,22,23,24,29,29,36,37,38,40,41,50,61

**ASUSTek COMPUTER INC.** 

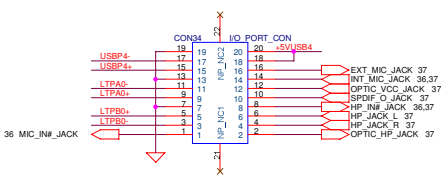
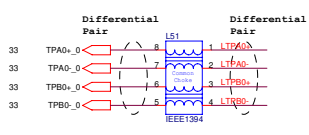
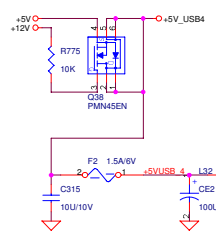
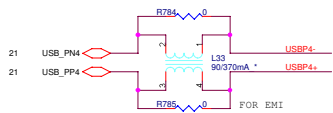
File: **DVI CONN**

Size: **A8J/F**

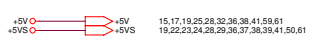
Customer: **A8J/F**

Date: 05/05/2007 Sheet 39 of 63

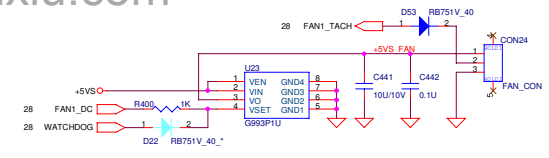
<< Kennedy\_Zhang >>



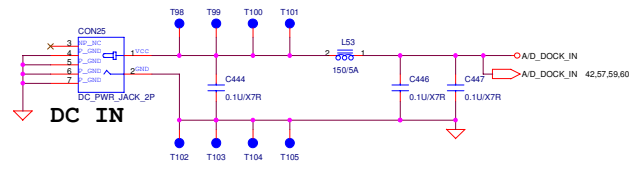
I/O PORT



15,17,19,25,28,32,36,38,41,59,61  
19,22,23,24,28,29,36,37,38,59,41,50,61

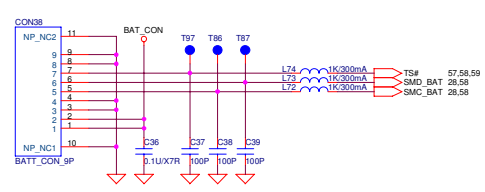


FAN CONTROL



DC IN

ACIN\_CONN



BAT\_CONN

ASUSTek COMPUTER INC.

File: FAN\_CTRL & ACIN & BAT & I/O PORT

Sub: Document Number

Customer: A&J/F

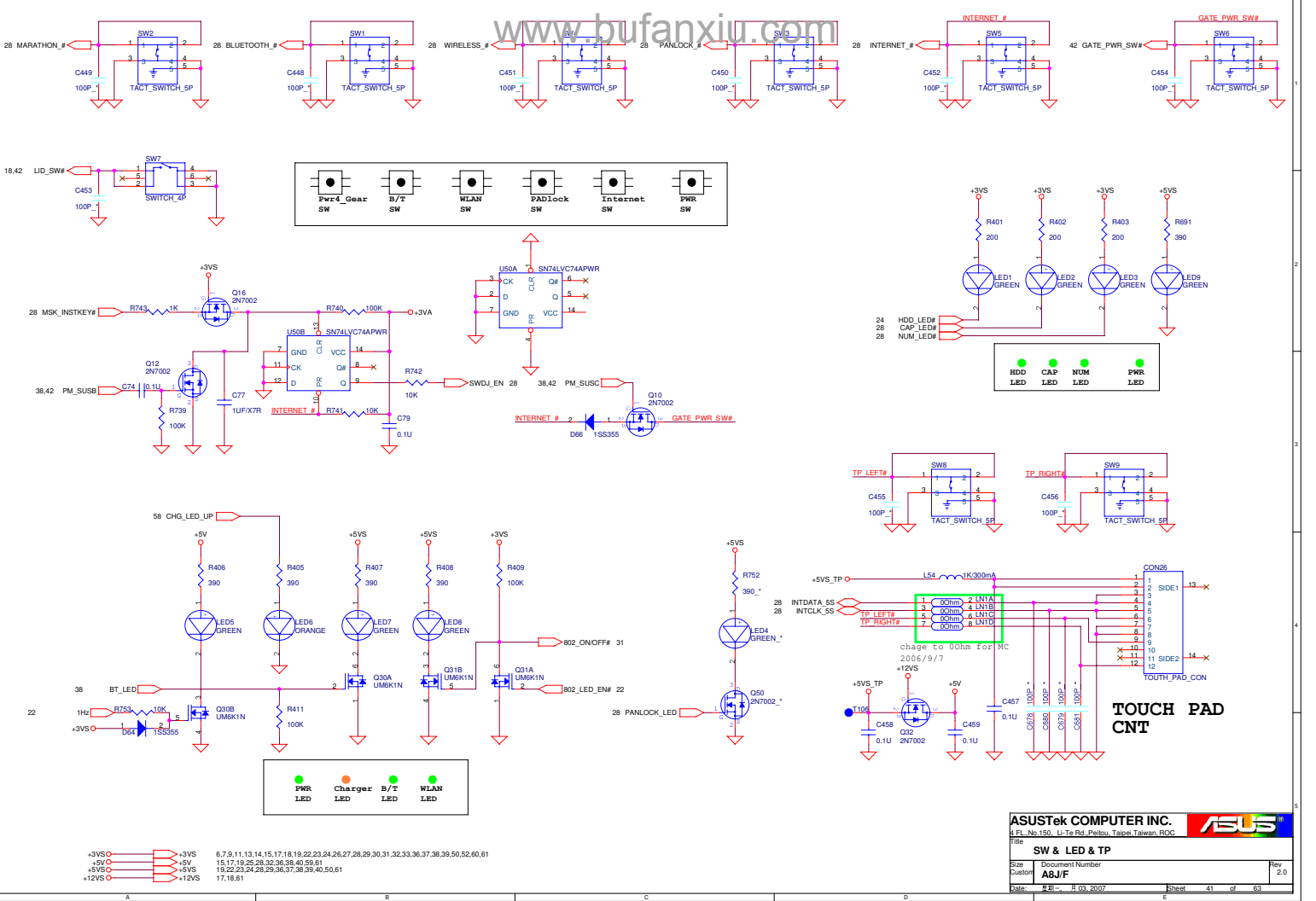
Date: 2007.03.03

Sheet: 40 of 63

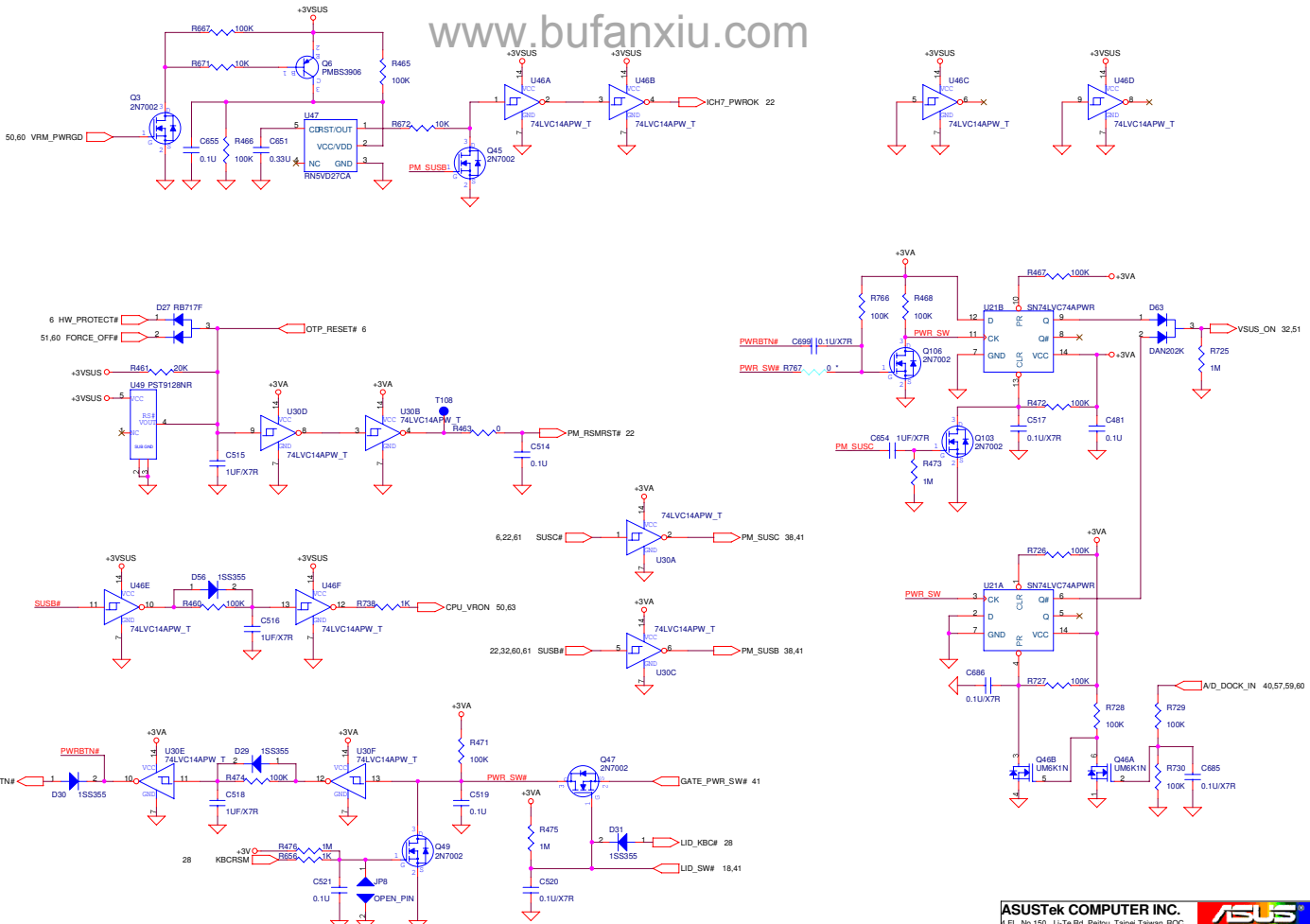
Rev: 2.0

<< Kennedy\_Zhang >>






<< Kennedy\_Zhang >>



+3V	28,30,31,32,34,37,38,54,61
+3VA	20,38,41,54,59,63
+3VSUS	18,21,22,23,28,29,30,51

**ASUSTek COMPUTER INC.** 

ASUS Logo

PL. No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC

**POWER-ON SEQUENCE**

Doc No.	Document Number	Rev
A6J/F	A6J/F	2.0


Date: 2007.03.03 Sheet 42 of 63

<< Kennedy\_Zhang >>

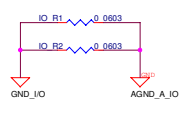
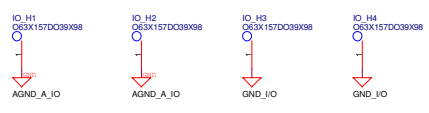
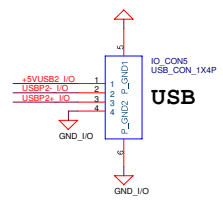
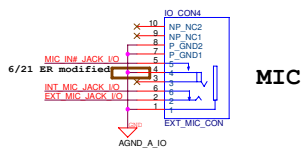
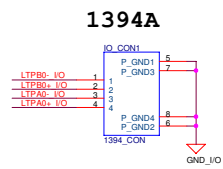
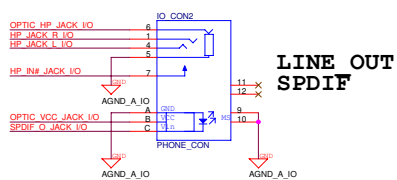
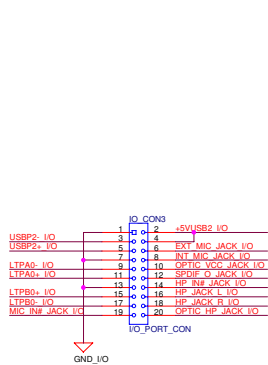
Revision History

Power:

System:

<b>ASUSTek COMPUTER INC.</b>		
4 FL, No.150, Li-Ta Rd., Peitou, Taipei, Taiwan, ROC		
Title: <b>HISTORY</b>		
Size	Document Number	Rev
Custom	<b>A&amp;J/F</b>	2.0
Date:	8/8/2007	Sheet 43 of 63

<< Kennedy\_Zhang >>



ASUSTek COMPUTER INC.

File: I/O PORT

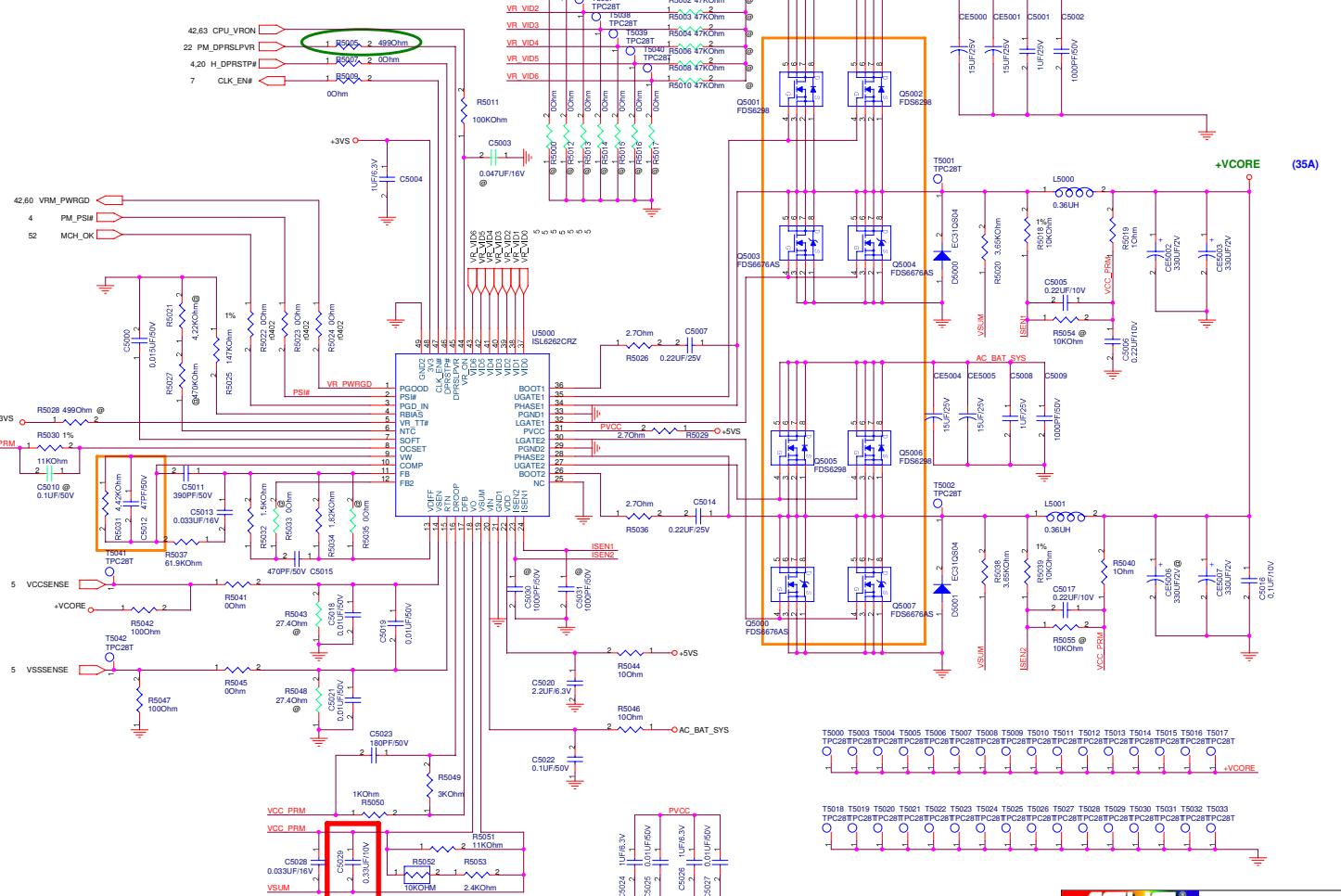
Sub: Document Number

Customer: A&J/F

Date: 2007.03.03 Sheet 44 of 63

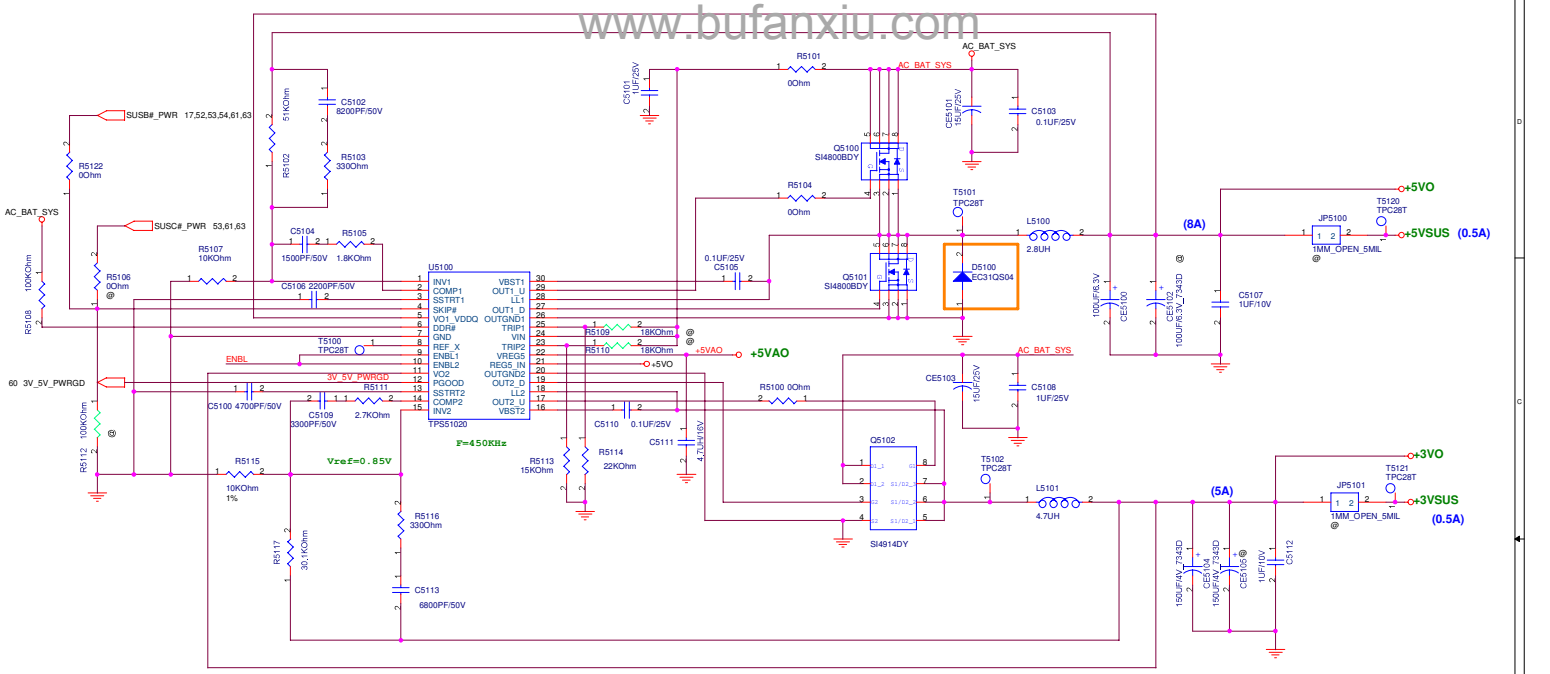
Rev: 2.0

<< Kennedy\_Zhang >>

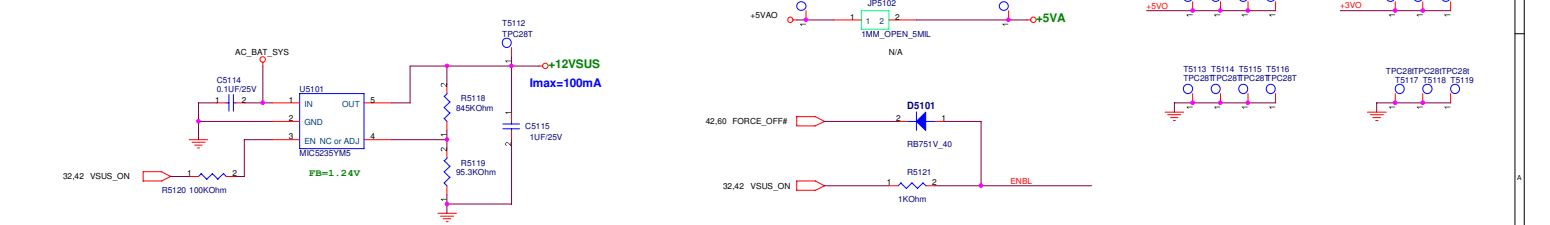


<b>ASUS</b>		<b>Title : POWER_VCORE</b>	
-<OrigName>		Engineer: Mia / Charlse	
Size	Project Name	Rev	
Custom	<b>A8J</b>	2.0	
Date: 2007-03-03	Sheet: 50	of	83

<< Kennedy\_Zhang >>

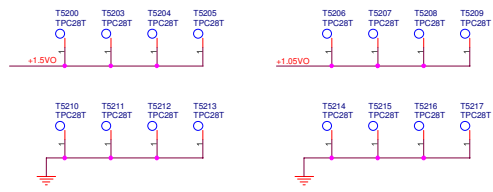
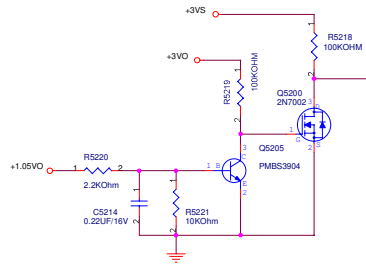
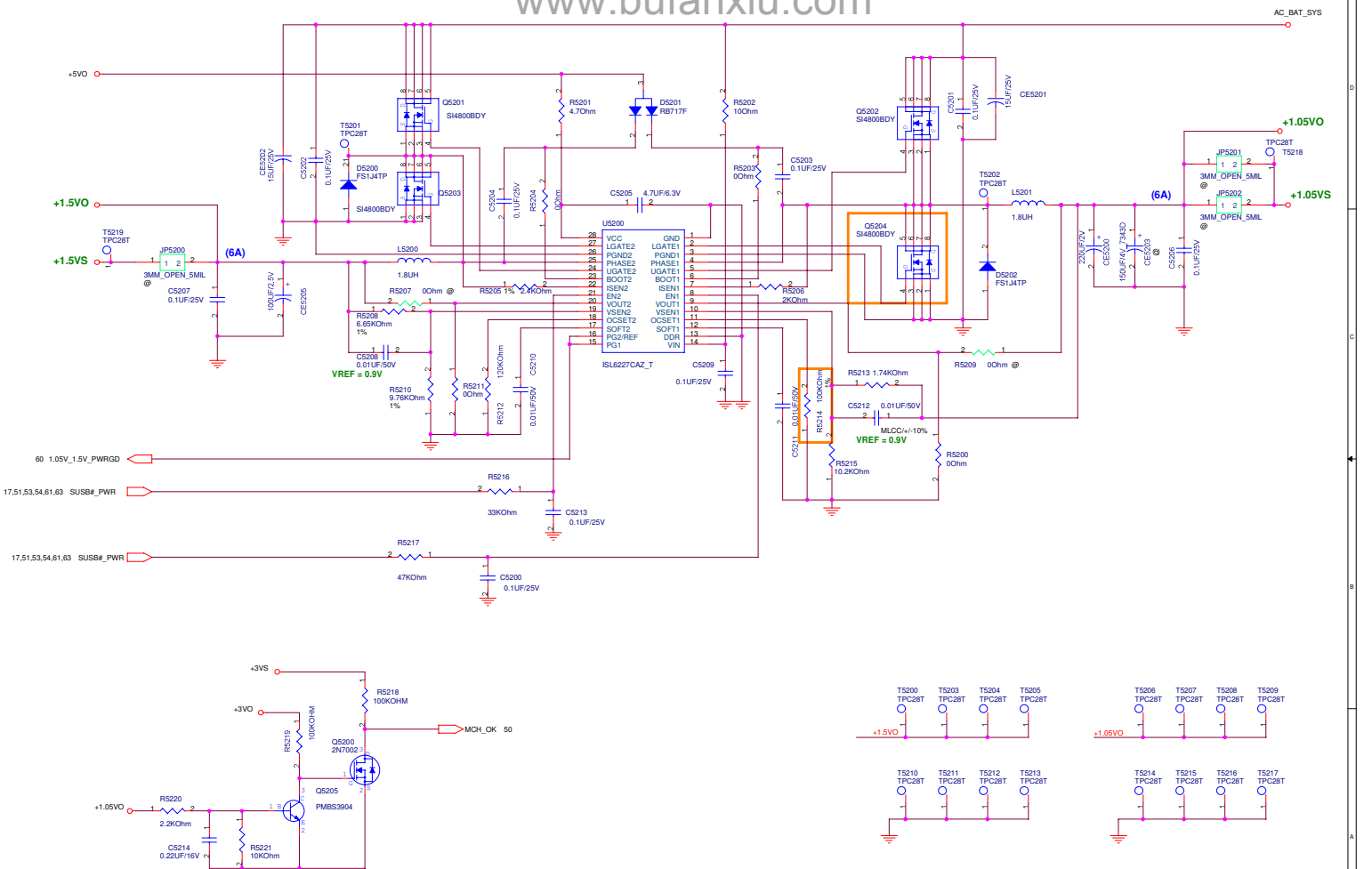


+12VSUS



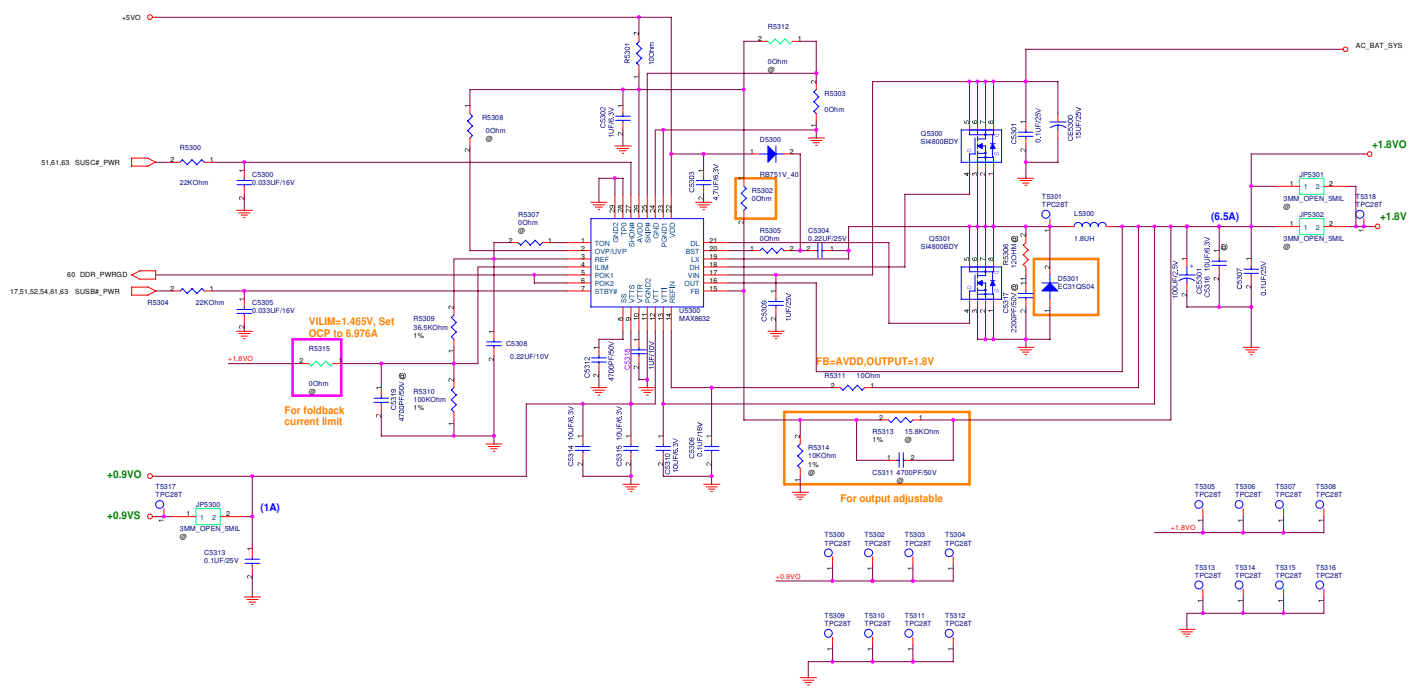
<b>ASUS</b>		<b>Title : POWER_SYSTEM</b>	
<OrigName>	Project Name	Engineer: Mia / Charlse	Rev
Custom	<b>A8J</b>		2.0
Date: 11/03/2007	Sheet 51	of 83	

<< Kennedy\_Zhang >>



<b>ASUS</b>		<b>Title</b> POWER_IO_1.5VS & 1.05VS	
-<OrigName>		Engineer: Mia / Charise	
Size	Project Name	Custom	Rev
	<b>A8J</b>		2.0
Date: 03/03/2007	Sheet	68	of 83

<< Kennedy\_Zhang >>

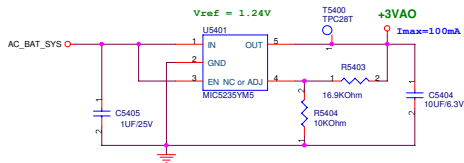
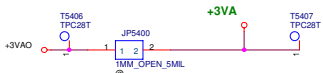


<b>ASUS</b>		<b>Title :</b> POWER IC_DDR & VTT
-OrigName		<b>Engineer:</b> Mia / Charise
Size	Project Name	Rev
Custom	A8J	2.0
Date: 8/11/2007	File: 83	of 83

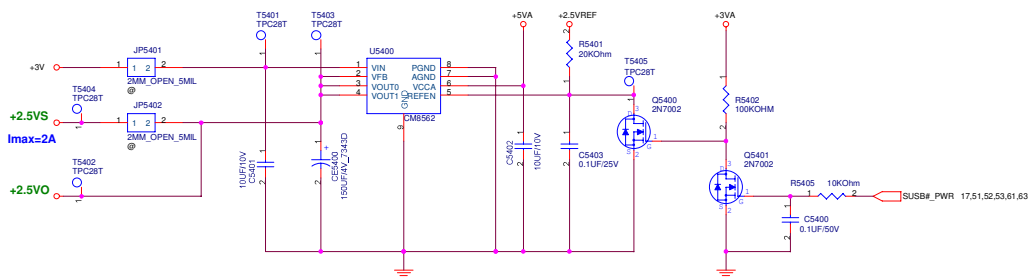
<< Kennedy\_Zhang >>



+3VAO

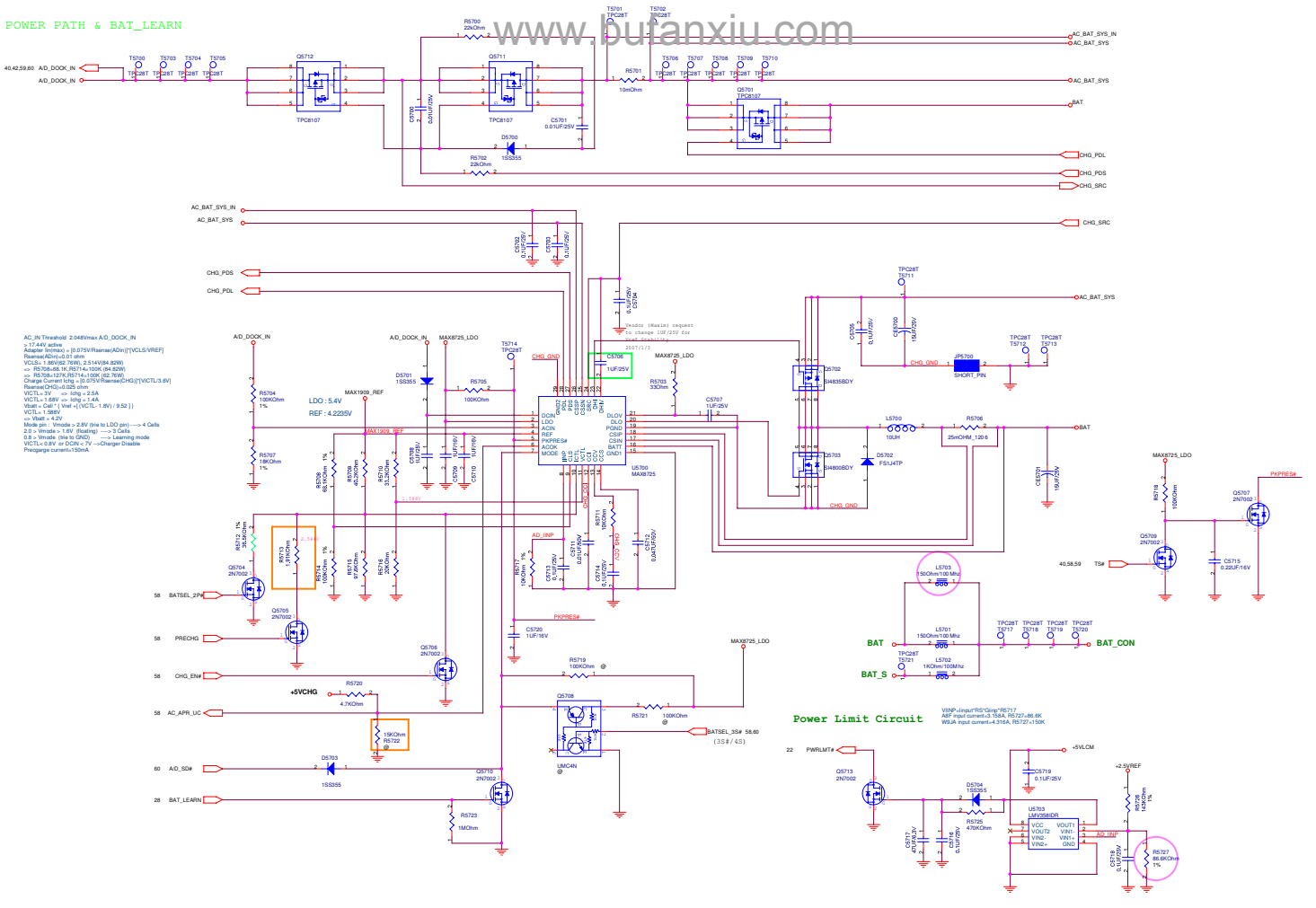


+2.5VS



<b>ASUS</b>		<b>Title : POWER_IO_+3VA &amp; +2.5V</b>	
-<OrigName>		Engineer: Mia / Charise	
Size	Project Name	Rev	
Custom	<b>A8J</b>	2.0	
Date: 11/03/2007		Sheet: 54	of 83

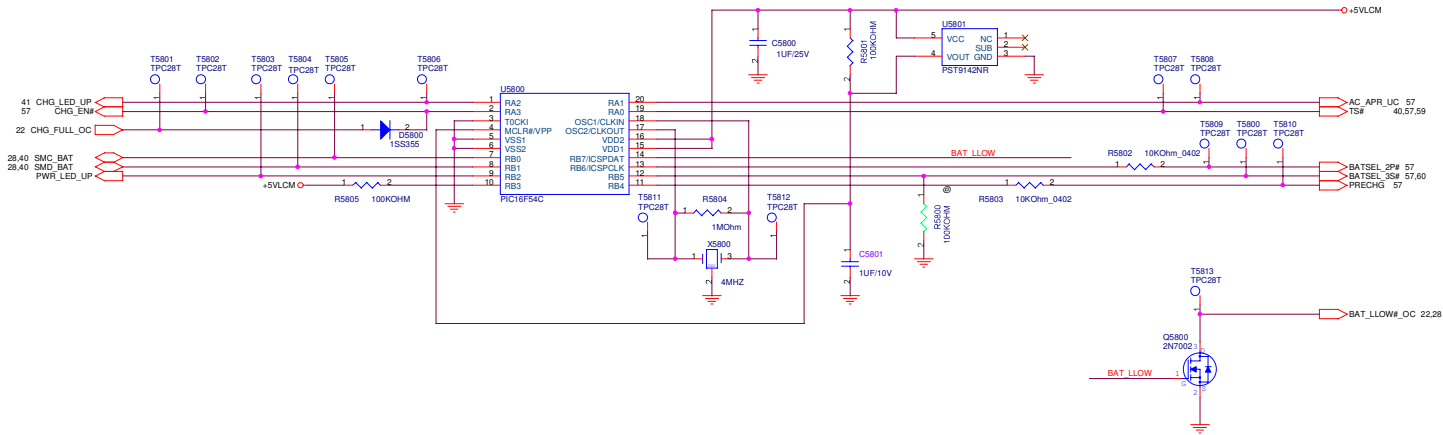
<< Kennedy\_Zhang >>



<b>ASUS</b> Title : POWER VGA RAM	
Engineer: Mia / Charbe	
Sheet : 1	Project Name : Custom
Date : 08/24/2007	Rev : 2.0
Page : 67	of : 67

<< Kennedy\_Zhang >>

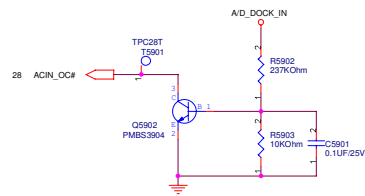
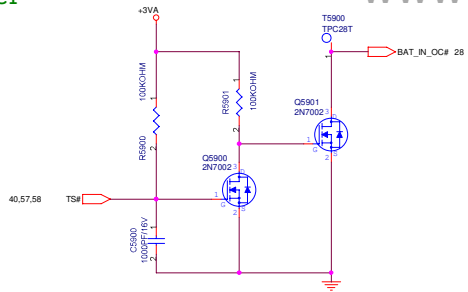
PIC16F54C



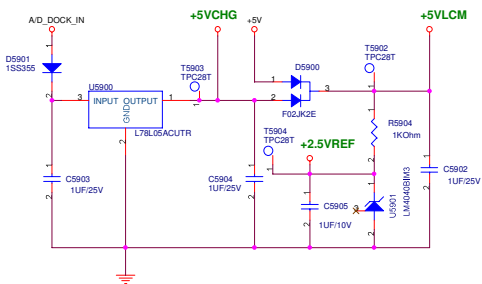
<b>ASUS</b>		<b>Title : POWER_PIC</b>	
-<OrigName>		Engineer: Mia / Charise	
Size	Project Name		Rev
Custom	ABJ		2.0
Date: 2007-03-03		Sheet 58	of 83

<< Kennedy\_Zhang >>

BATTERY IN DETECT

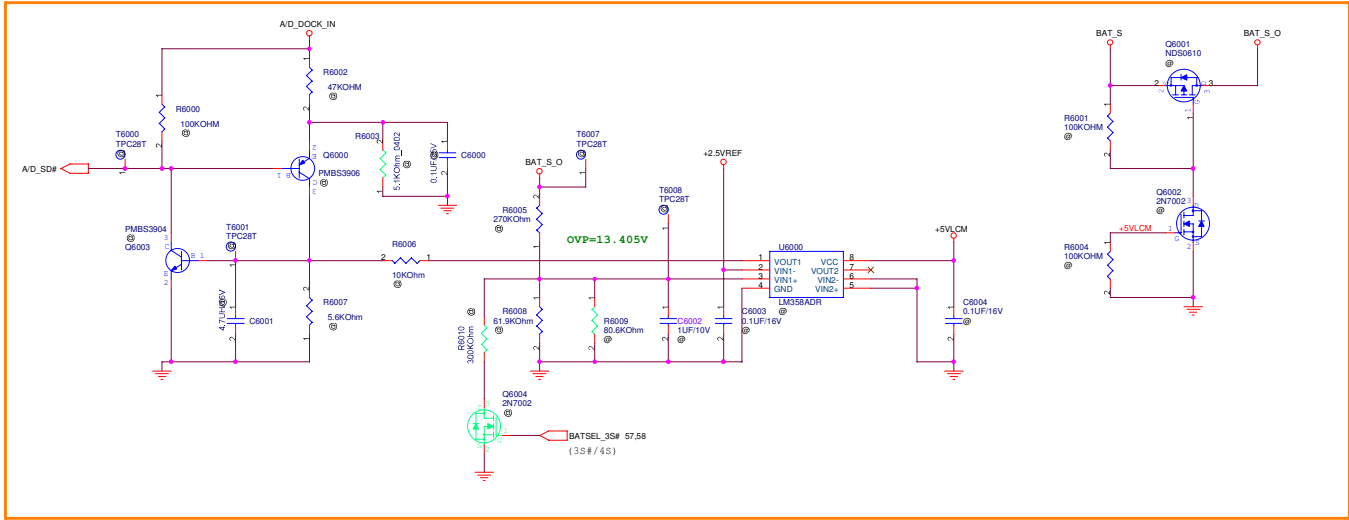


+5VLCM, +5VCHG & +2.5VREF

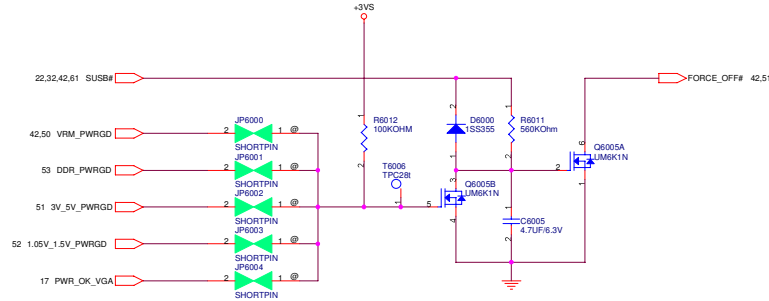


<b>ASUS</b>		<b>Title : POWER_DETECT</b>	
<OrigName>	Project Name	Engineer: Mia / Charise	Rev
Custom	ABJ		2.0
Date: 11/03/2007		Sheet 69	of 83

<< Kennedy\_Zhang >>



POWER GOOD DETECTOR

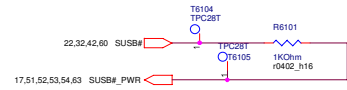
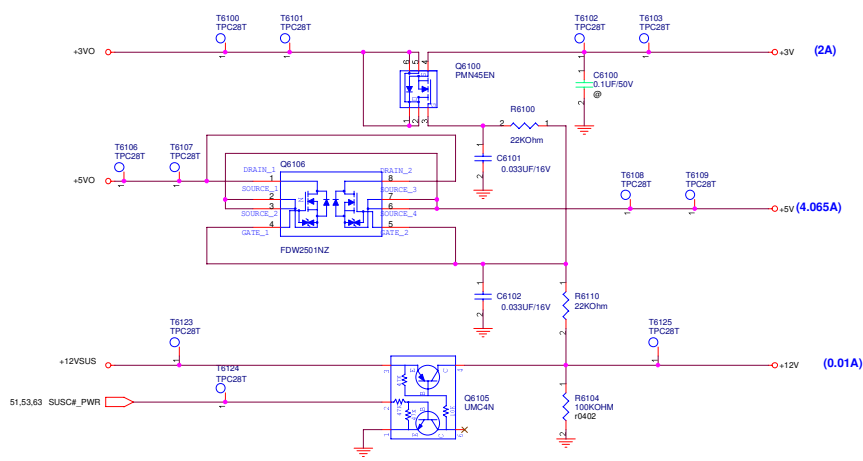


- TPC28T T6002 1 VRM\_PWRGD
- TPC28T T6003 1 DDR\_PWRGD
- TPC28T T6004 1 3V\_5V\_PWRGD
- TPC28T T6005 1 1.05V\_1.5V\_PWRGD

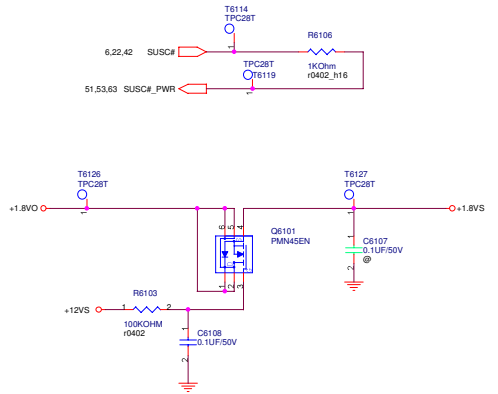
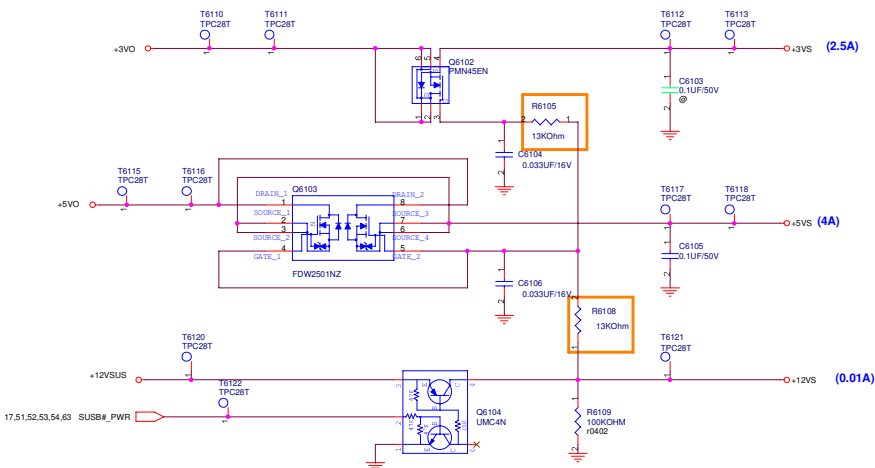
<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
Size	Project Name	Engineer: Mia / Charlse	Rev
Custom	<b>A8J</b>		2.0
Date: 11/03/2007		Sheet: 60	of 83

<< Kennedy\_Zhang >>

SUSC#\_PWR POWER

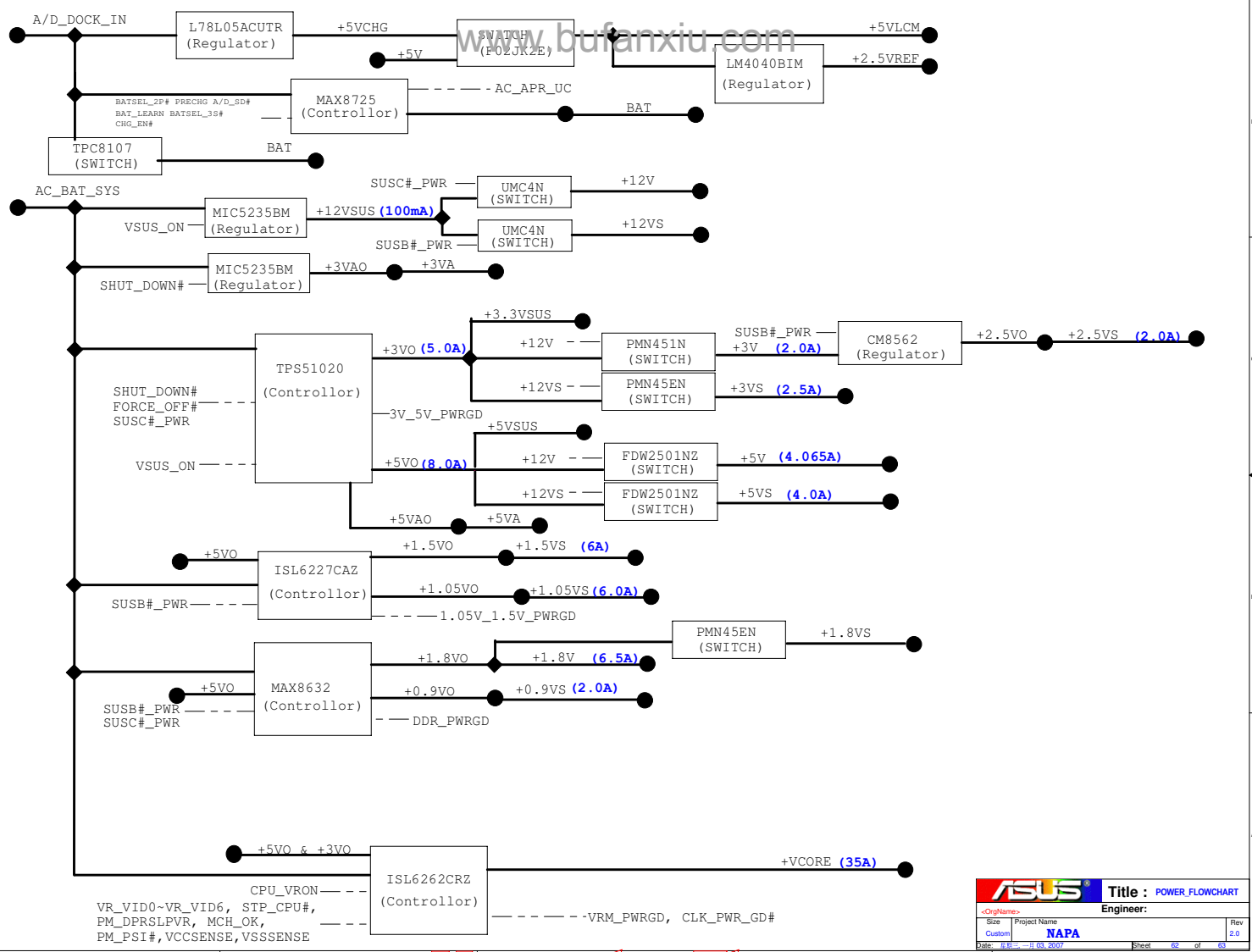


SUSB#\_PWR POWER



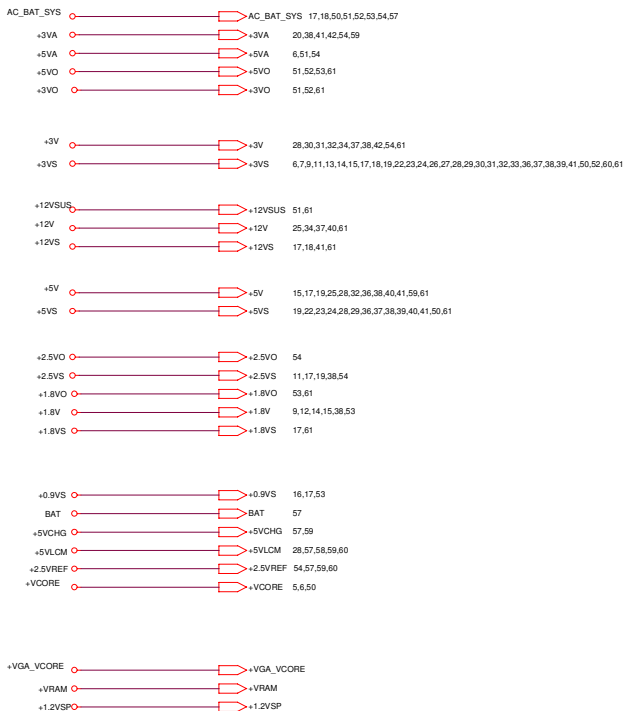
<b>ASUS</b>		<b>Title : POWER_LOAD_SWITCH</b>	
<OrigName>	Project Name	Engineer:	Mia / Charise
Size	Custom	ABJ	Rev 2.0
Date: 03/03/2007	Sheet 61	of 83	

<< Kennedy\_Zhang >>

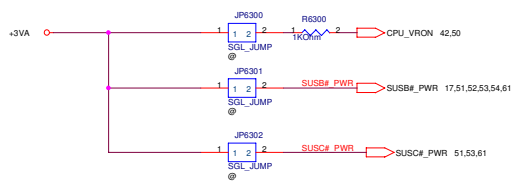


<b>ASUS</b>		<b>Title : POWER_FLOWCHART</b>	
.<OrigName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.0	
Date: 2007-03-03		Sheet: 66	of 83

<< Kennedy\_Zhang >>



FOR POWER TEST



<b>ASUS</b>		<b>Title : POWER_SIGNAL</b>	
-<OrigName>		Engineer:	
Size	Project Name		Rev
Custom	<b>NAPA</b>		2.0
Date: 03/03/2007		Sheet: 63	of 63

<< Kennedy\_Zhang >>