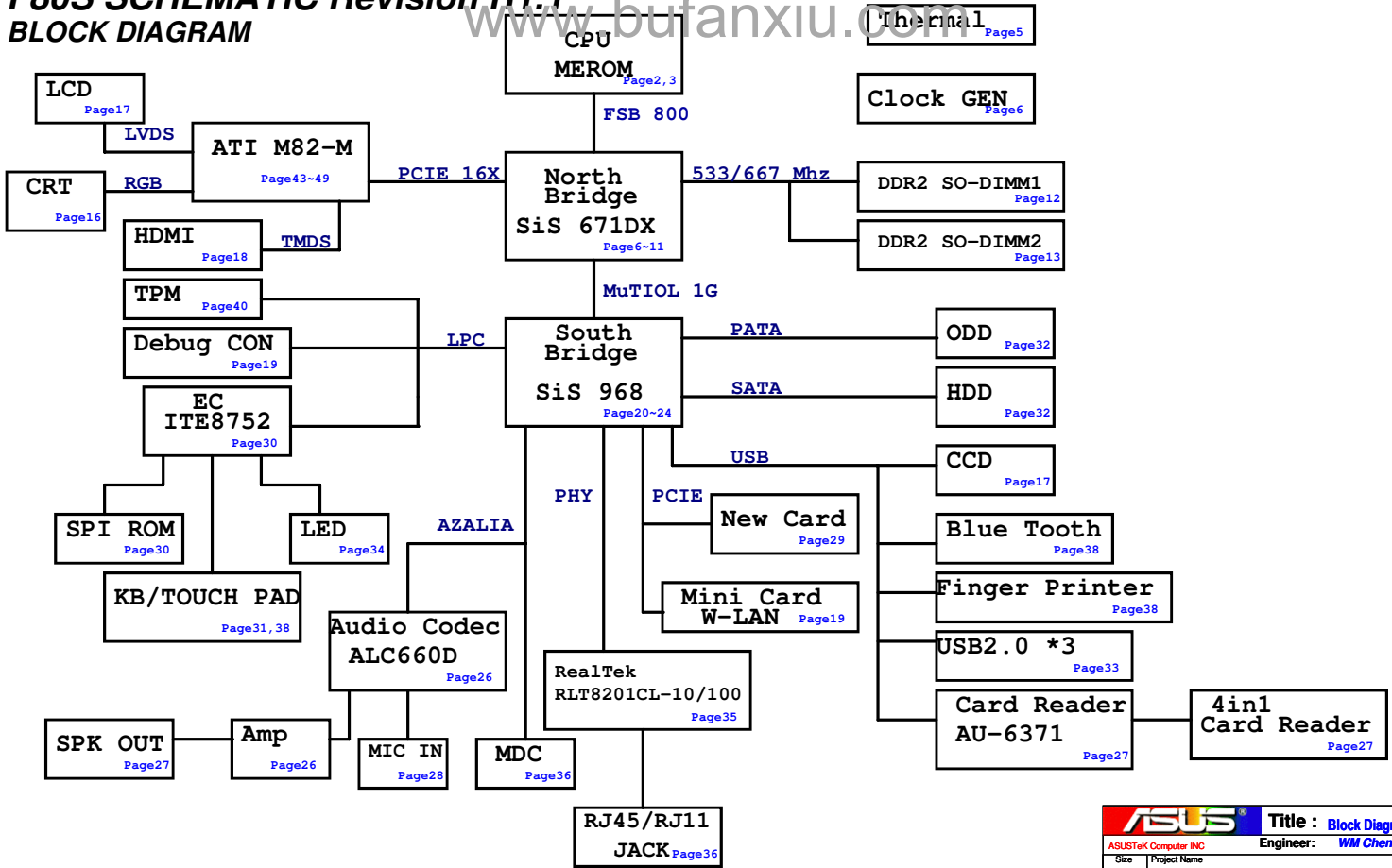


F80S SCHEMATIC Revision R1.1

BLOCK DIAGRAM

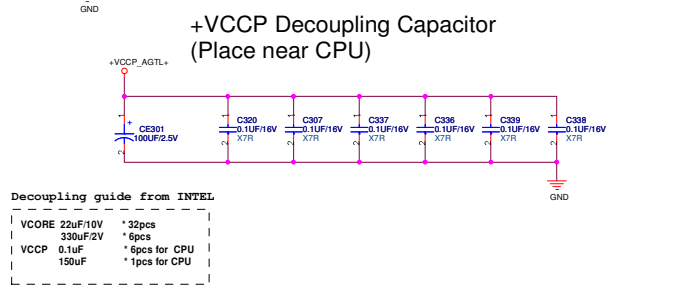
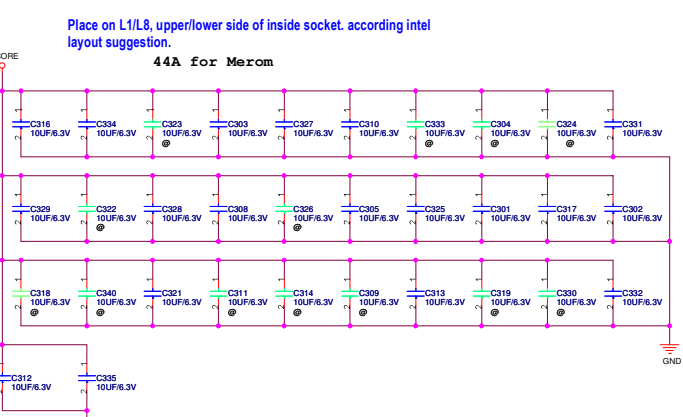
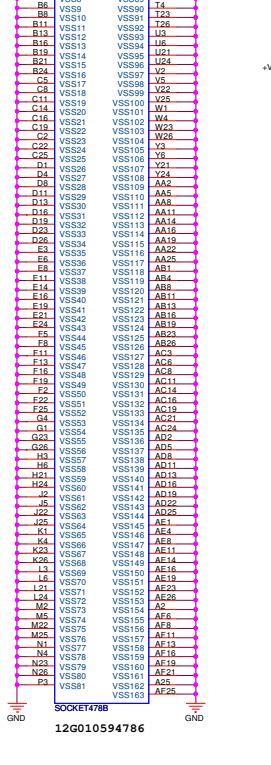
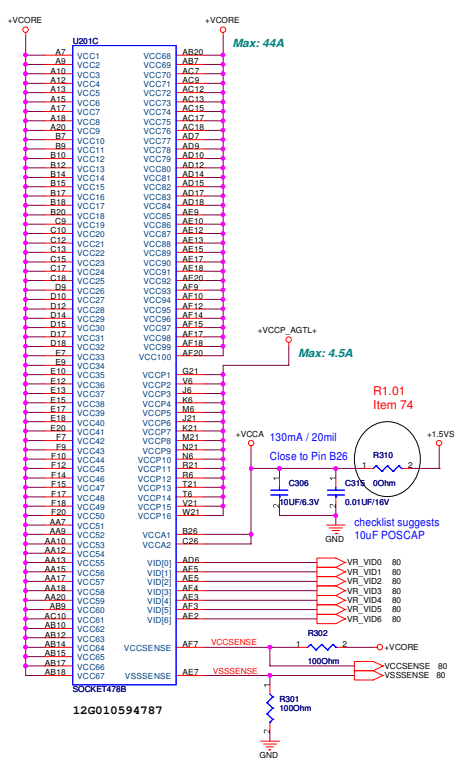
www.bufanxiu.com



ASUS		Title : Block Diagram	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name	Rev	
B	F80S	1.1	
Date: Friday, February 15, 2008		Sheet	1 of 94

<< MaryL_Liu >>

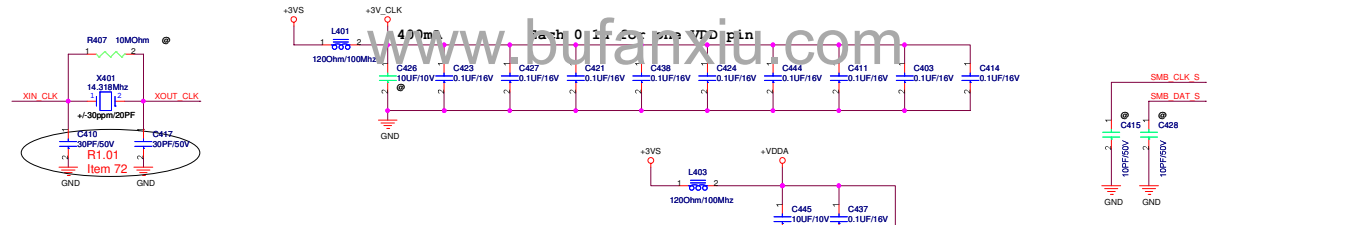
MEROM FSB 800			
V _{CC}	Min	Typ	Max
V _{CC}	1.20V	0.93V	1.310V
ICCP	Min	Typ	Max
ICCP			2.5A



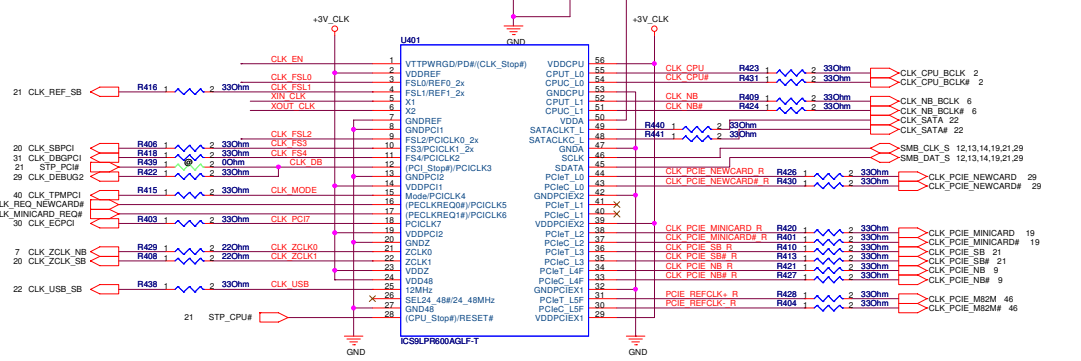
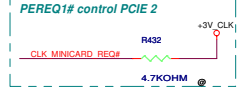
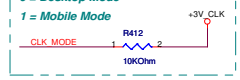
Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27-4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

ASUS		Title : MEROM CPU (2)
ASUSTeK COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
A3	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	3 of 84

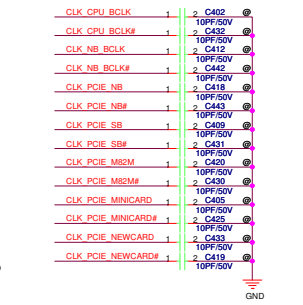
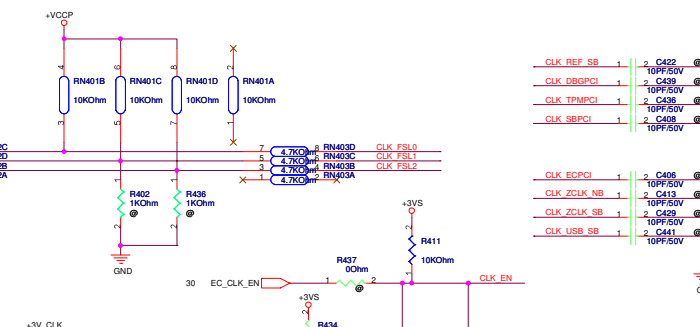
<< MaryL_Liu >>



CLK_MODE



FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100

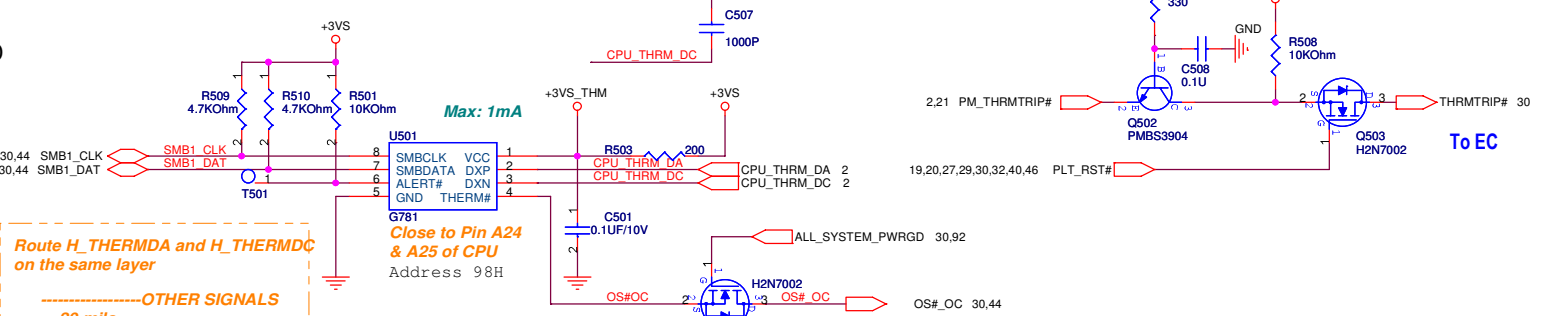


ASUS		Title : Clock GEN	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name	Date	Rev
A3	F80S	Wednesday, February 13, 2008	1.1
Date: Wednesday, February 13, 2008		Sheet 4 of 94	

<< MaryL_Liu >>

CPU Thermal Sensor

www.bufanxiu.com



Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
20 mils

=====GND
10 mils

=====H_THERMDA(10 mils)
10 mils

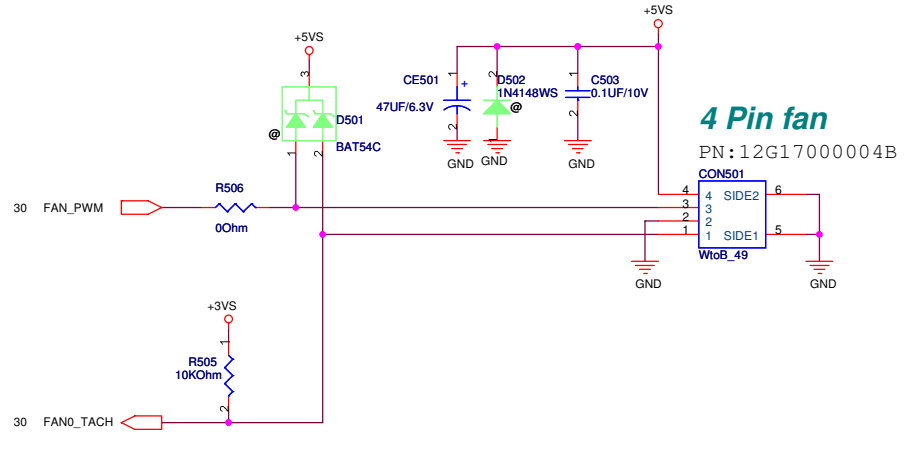
=====H_THERMDC(10 mils)
10 mils

=====GND
20 mils

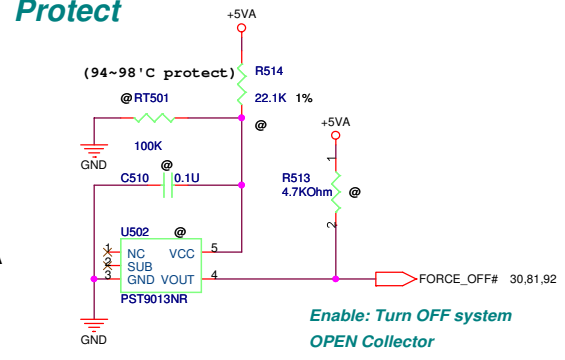
-----OTHER SIGNALS

Avoid FSB,Power

DC FAN Control

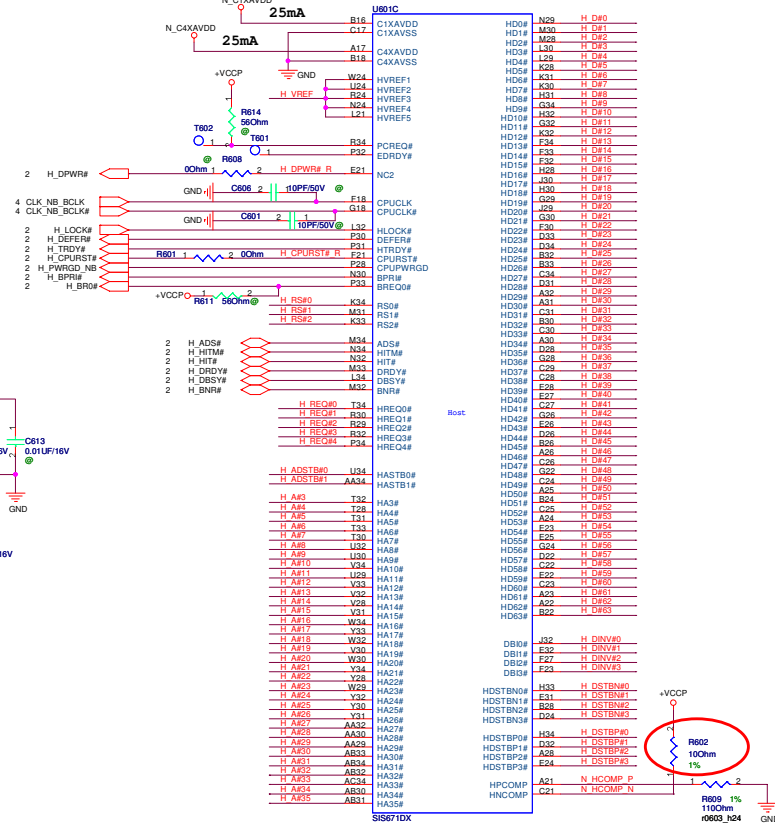
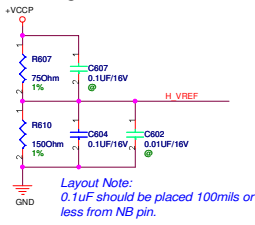


H/W Thermal Protect

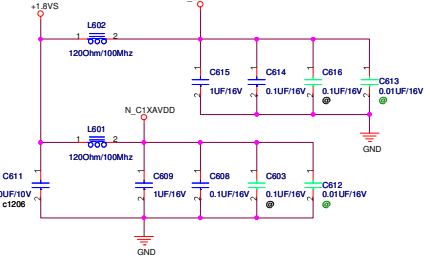


ASUS		Title : Thermal Sensor	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S	Date: Wednesday, February 13, 2008	Sheet 5 of 94
			Rev 1.1

<< MaryL_Liu >>



- H_A#35[3:0] 2
- H_REQ#4[0] 2
- H_DRDY#3[0] 2
- H_RS#2[0] 2
- H_ADSTB#1[0] 2
- H_DIN#V[3:0] 2
- H_DSTB#3[0] 2
- H_DSTB#N[3:0] 2

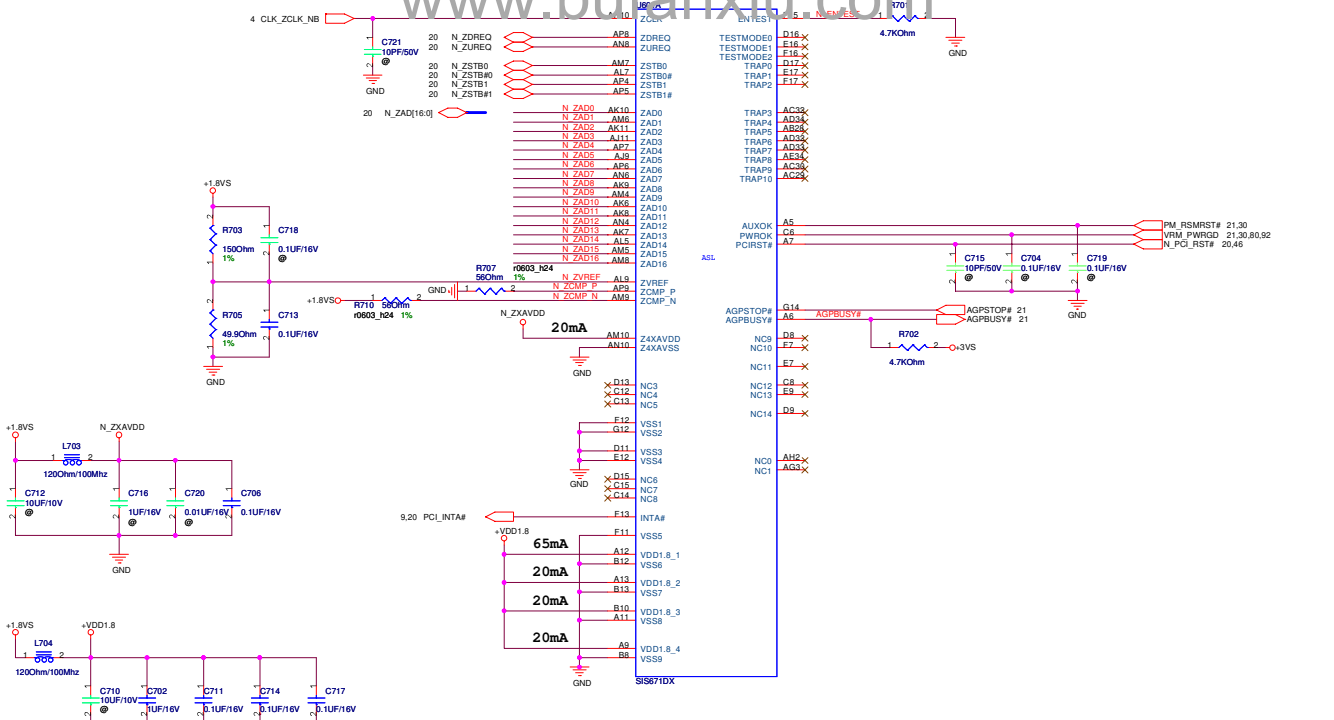


Trace should be 10 mil wide with 20 mil spacing

0829 S1S recommend

ASUS		Title : M671DX (HOST)	
ASUSTek Computer INC		Engineer: WM Chen	
Size: A3	Project Name: F80S	Rev: 1.1	
Date: Wednesday, February 13, 2008		Sheet: 8	of: 94

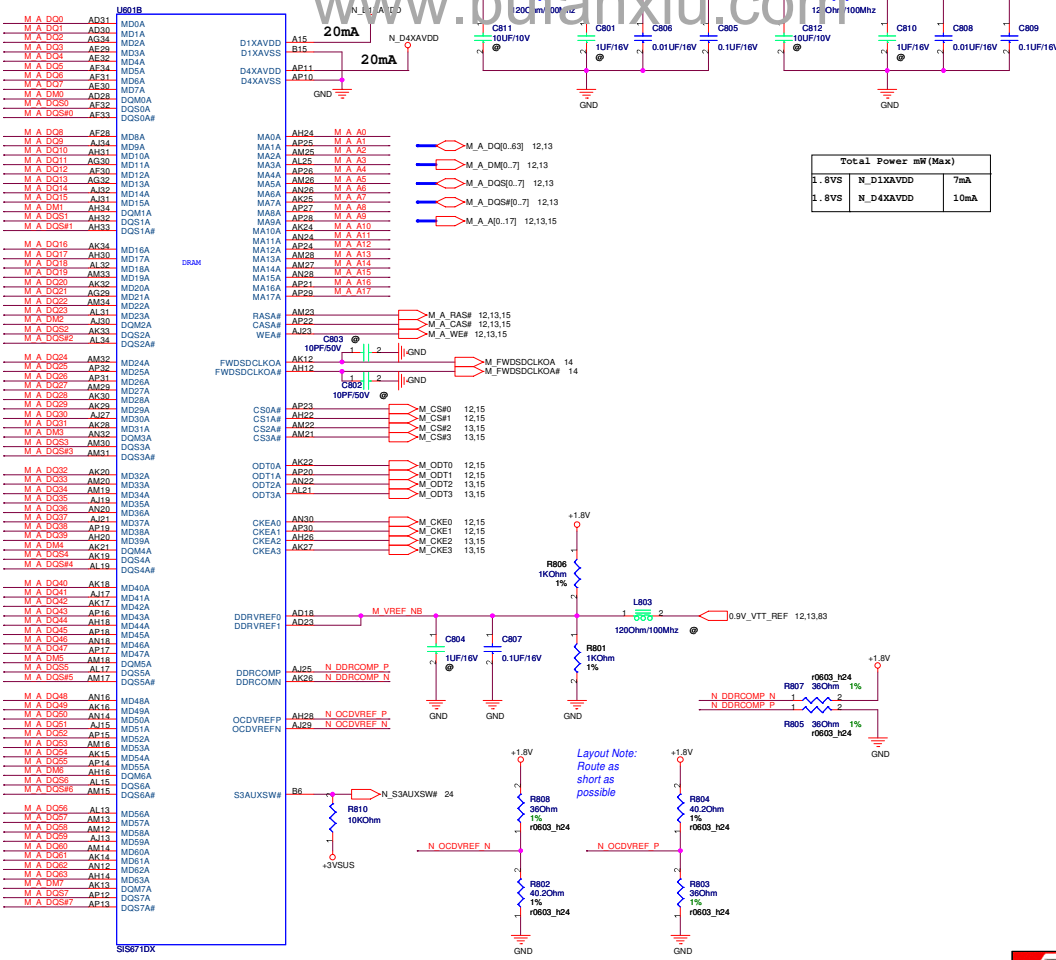
<< MaryL_Liu >>



Layout Trace width

ASUS		Title M671DX(MuTIO&VGA)	
ASUSTek Computer INC		Engineer: WM Chen	
Size: A3	Project Name: F80S	Rev: 1.1	
Date: Wednesday, February 13, 2008		Sheet: 7	of 94

<< MaryL_Liu >>



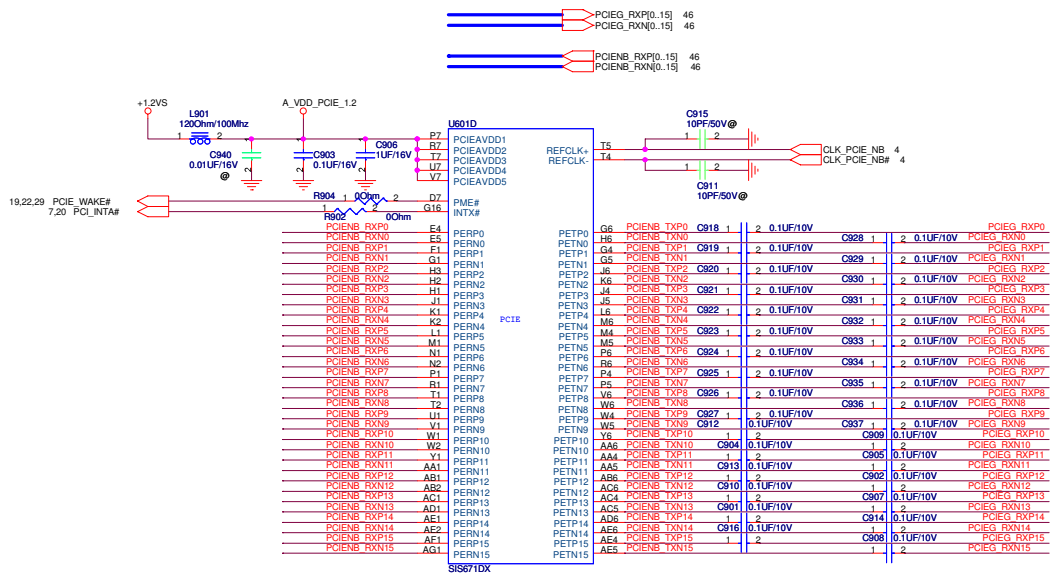
ASUS Title: M671DX (DDR2)

ASUSTek Computer INC Engineer: WM Chen

Size	Project Name	Rev
A3	F80S	1.1

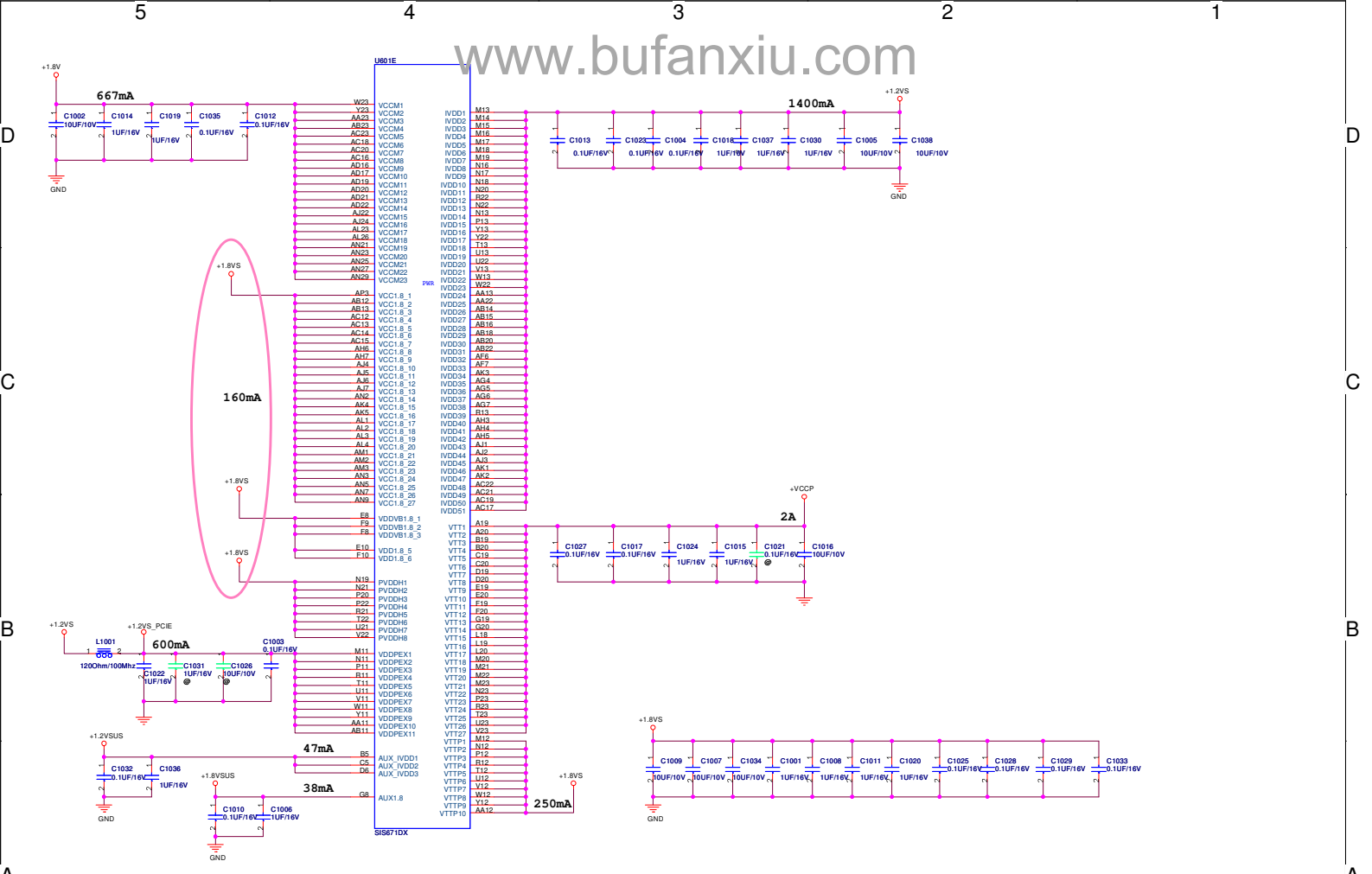
Date: Wednesday, February 13, 2008 Sheet 8 of 94

<< MaryL_Liu >>



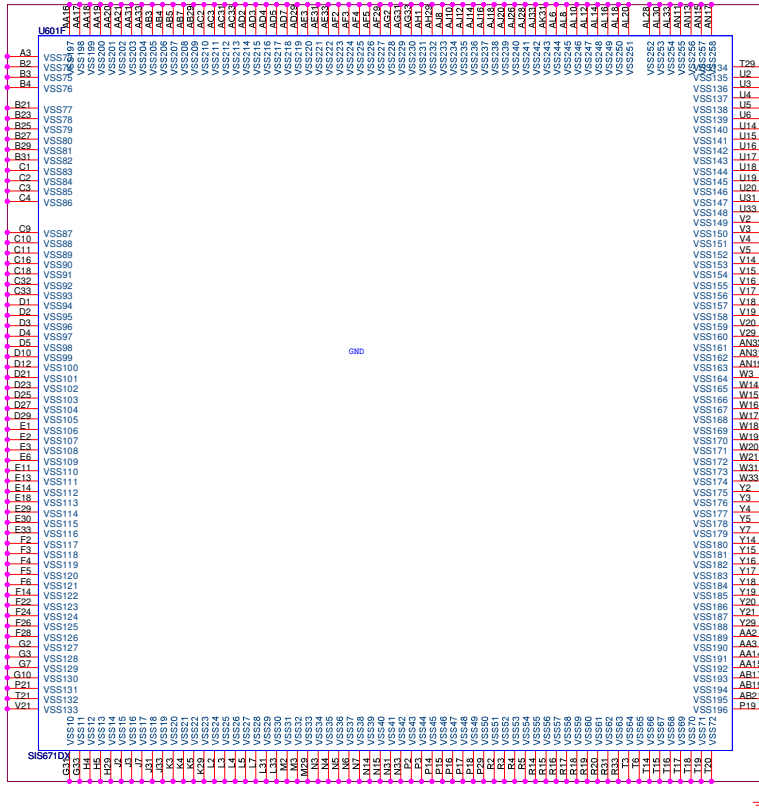
ASUS		Title : M6710X (PCI-E)	
ASUSTeK Computer INC		Engineer: WM Chen	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	9 of 94

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ASUS		Title : M671DX (PWR)	
ASUSTek Computer INC		Engineer: WM Chen	
Site	Project Name	Rev	
Customer	F80S	L1	
Date: Wednesday, January 23, 2008	Sheet 10	of 94	

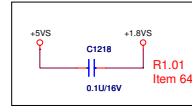
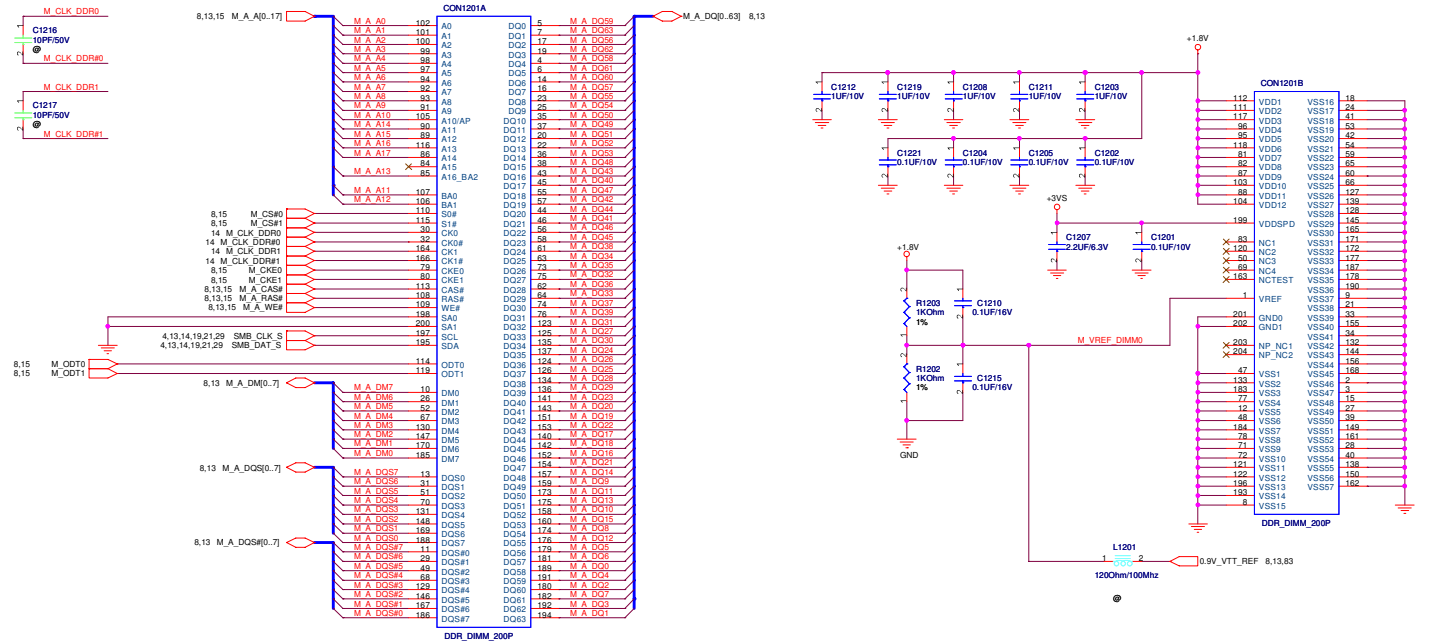
« MaryL_Liu »



ASUS		Title : M671DX (GND)	
ASUSTeK Computer INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, January 30, 2008		Sheet	11 of 94

<< MaryL_Liu >>

R0.4
Item 30
P/N : 12G025122006 H:5.2mm

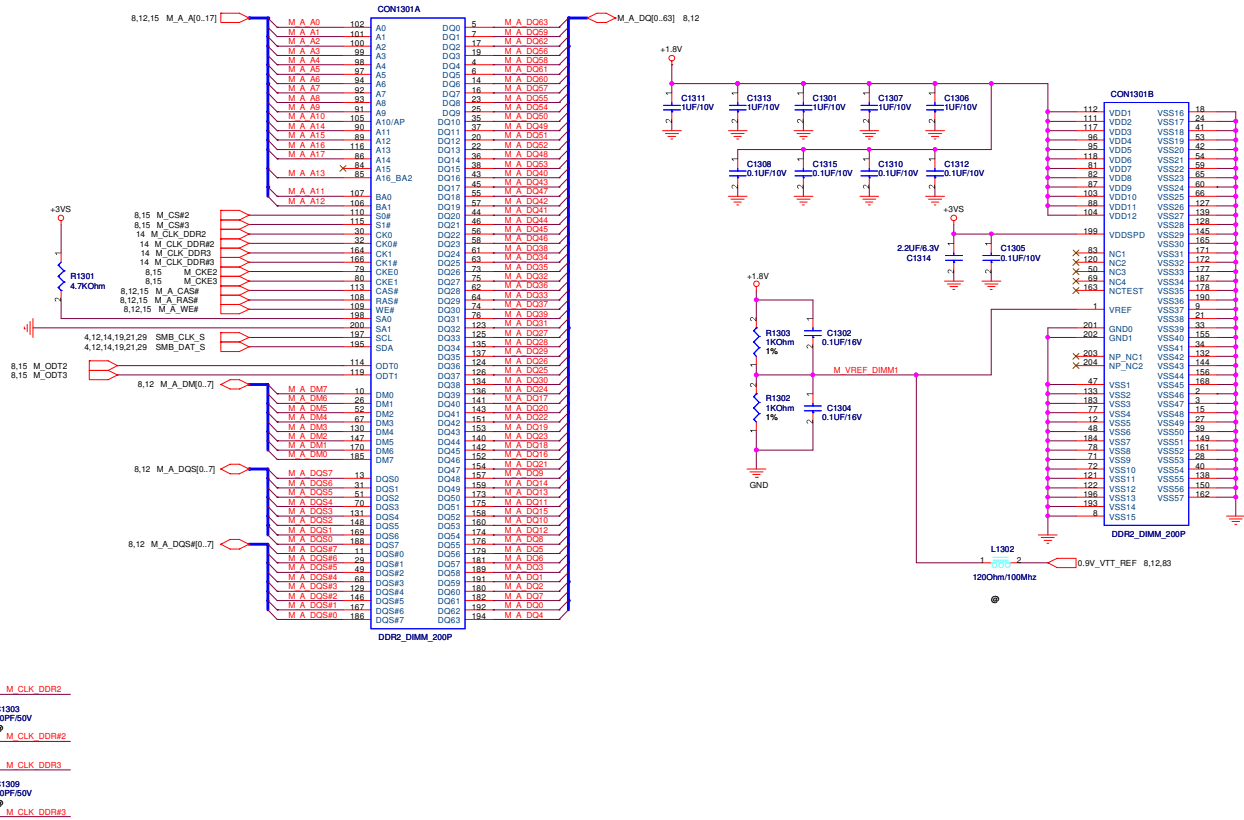


ASUS Title : DDR2 SO-DIMM
 ASUSTek Computer INC Engineer: **WM Chen**
 Size Project Name Rev
 A3 F80S 1.1
 Date: Wednesday, February 13, 2008 Sheet 12 of 94

<< MaryL_Liu >>

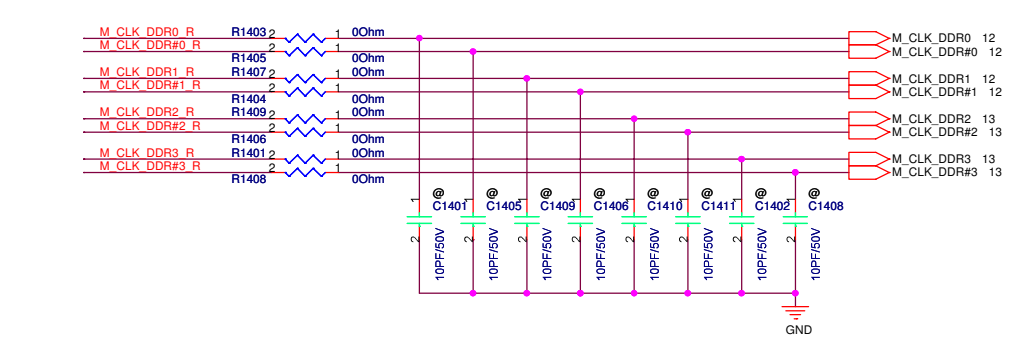
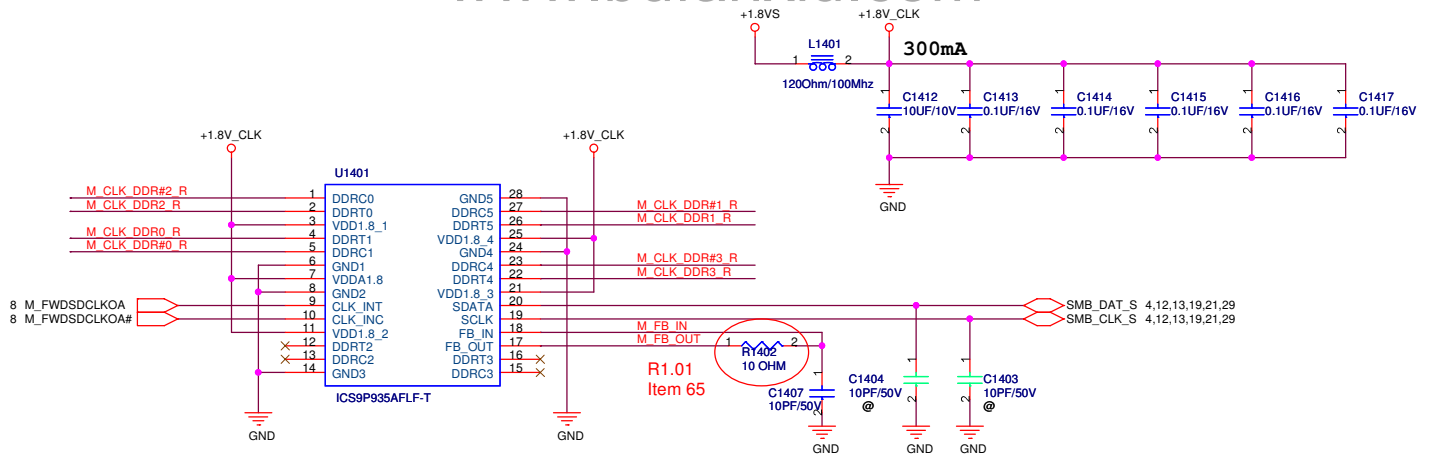
R0.4
Item 30

P/N : 12G025C22002 H:9.2mm



ASUS		Title : DDR2 SO-DIMM2	
ASUSTek Computer Inc		Engineer: WM Chen	
Size: A3	Project Name: F80S	Date: Wednesday, February 13, 2008	Sheet: 13 of 34
		Rev: 1.1	

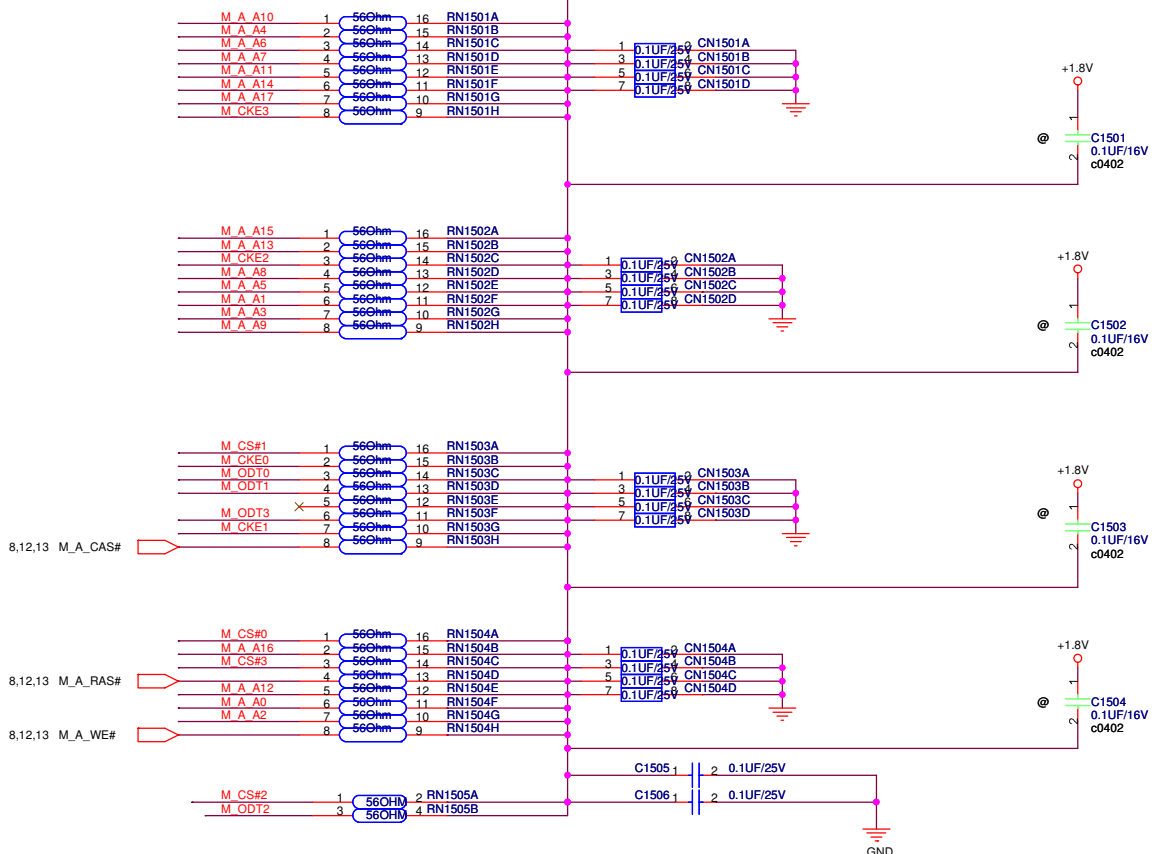
<< MaryL_Liu >>



ASUS		Title : DDR2 BUFFER	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet	14 of 94

<< MaryL_Liu >>

8,12,13 M_A_A[17:0]
8,12,13 M_CKE[0:3]
8,12,13 M_CS#[0:3]
8,12,13 M_ODT[0:3]

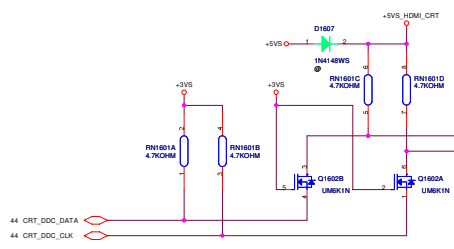
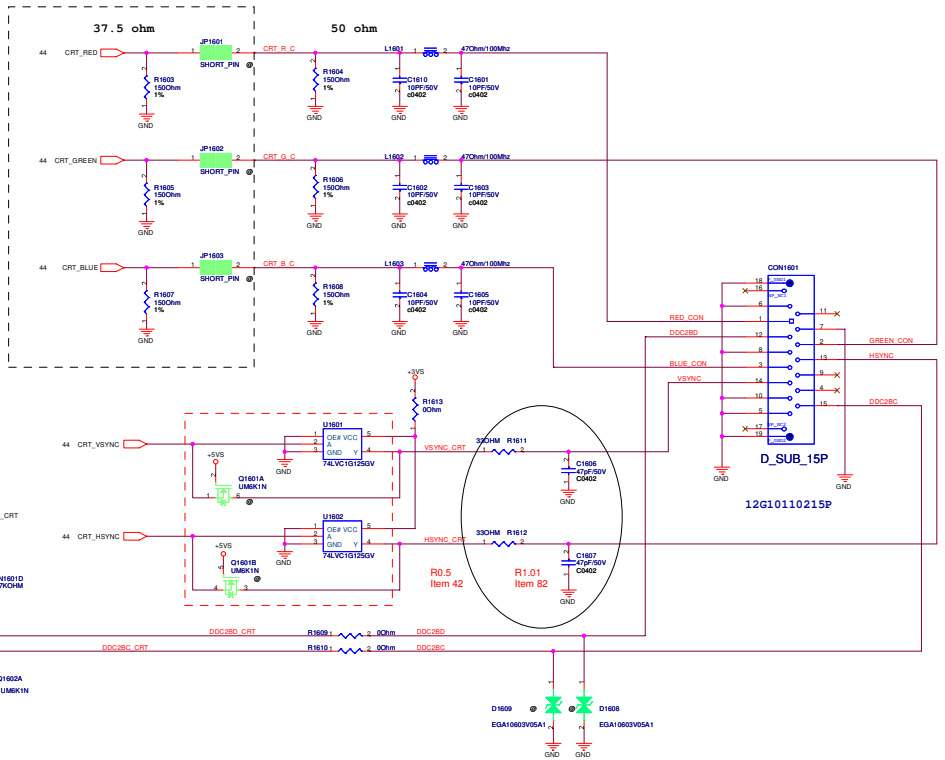
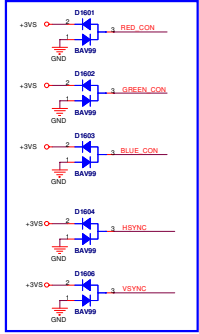


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

ASUS		Title : DDR2 TERMINATION	
ASUSTeK Computer INC		Engineer: WM Chen	
Size A4	Project Name F80S		Rev 1.1
Date: Wednesday, February 13, 2008		Sheet 15 of 94	

<< MaryL_Liu >>

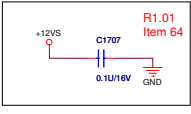
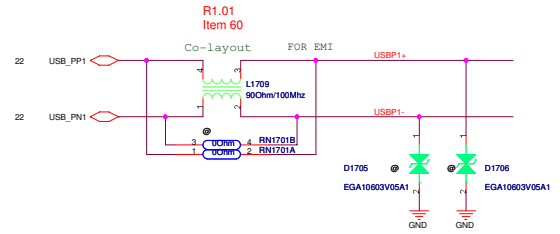
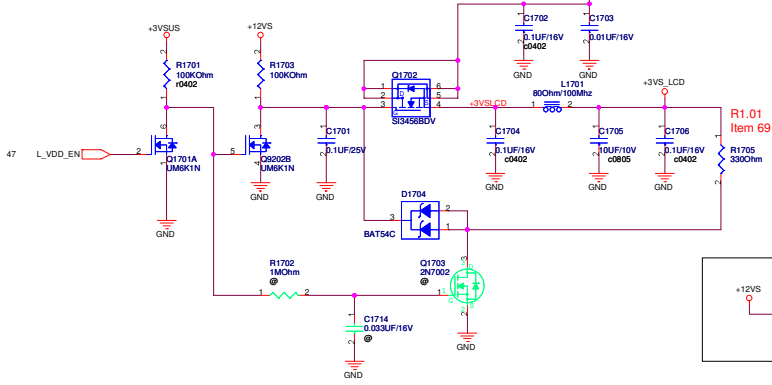
PLACE ESD Diodes near connector



ASUS		Title : CRT
ASUSTEK COMPUTER INC.		Engineer: WM Chen
Size	Project Name	Rev
C	F80S	1.1
Date: Wednesday, February 18, 2009		Sheet: 15 of 24

<< MaryL_Liu >>

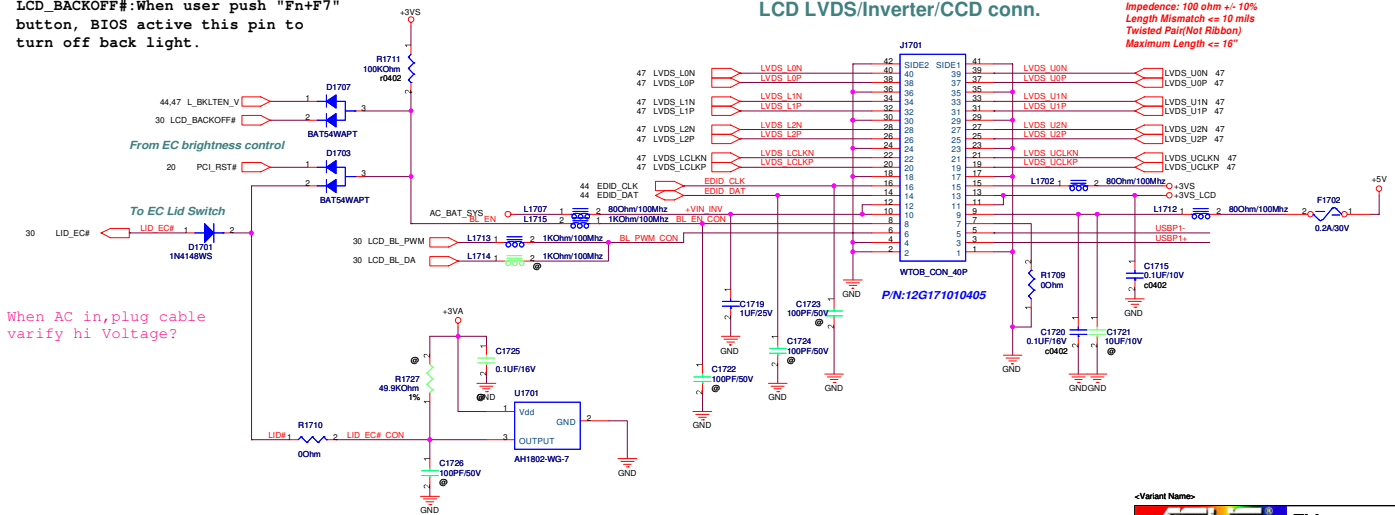
LCD Power



BIOS
LCD_BACKOFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

LCD LVDS/Inverter/CCD conn.

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

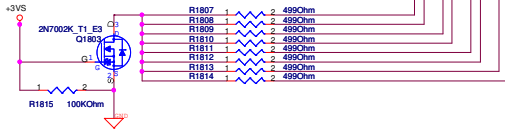
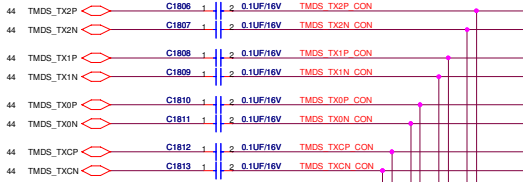


When AC in, plug cable
varify hi Voltage?

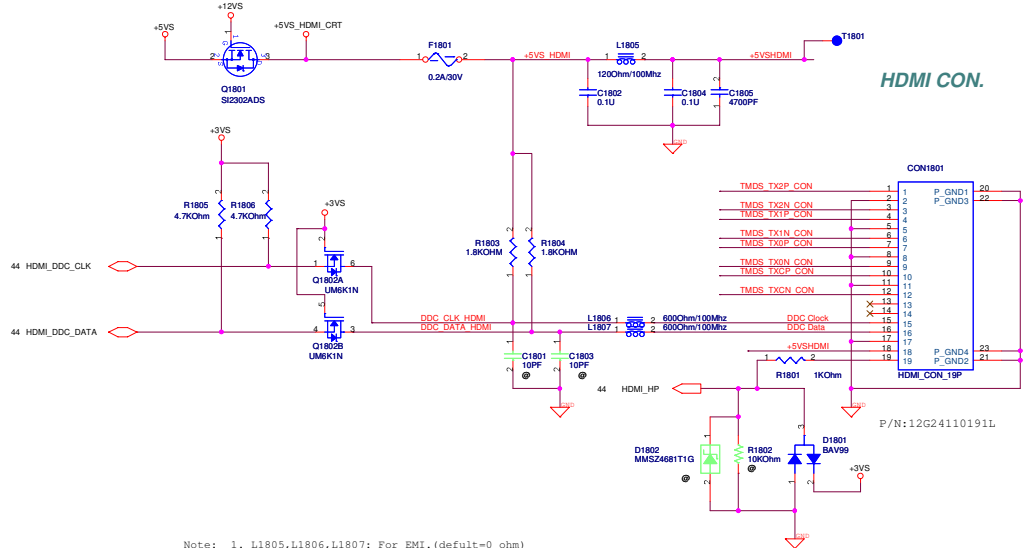
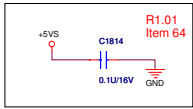
ASUS Logo
Title : LVDS & INVERTER
 ASUSTEK COMPUTER INC Engineer: WM Chen
 Size Project Name: Custom F80S Rev: 1.1
 Date: Wednesday, February 13, 2008 Sheet: 17 of 34

<< MaryL_Liu >>

near the HDMI connector



Reference should be +5VS, but Avl answer that +3VS is fine. As long as it can turn the MOSFET on.



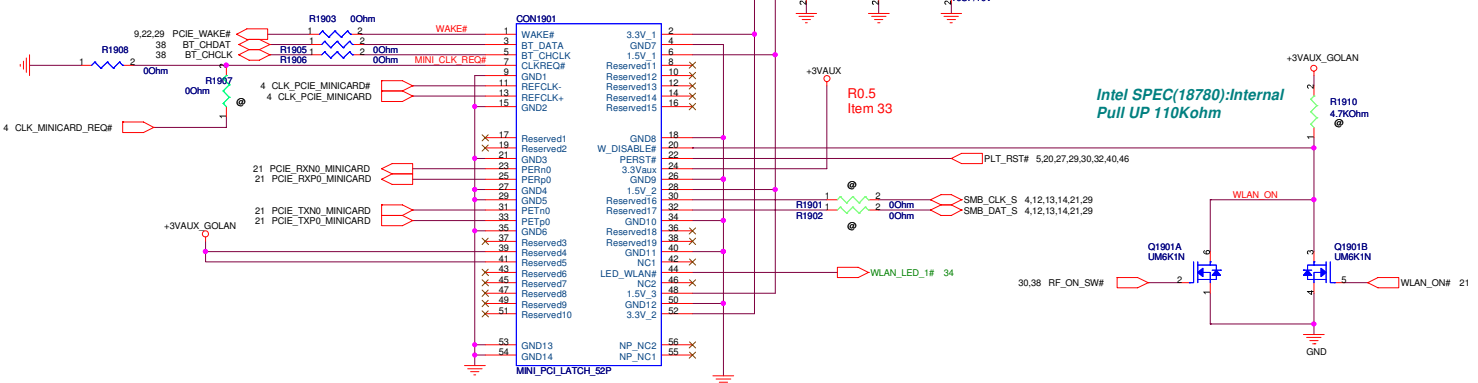
Note: 1. L1805,L1806,L1807: For EMI. (default=0 ohm)
 2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

ASUS		Title : TV & HDMI	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet: 18	of	34

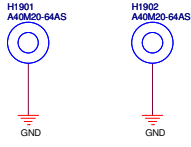
<< MaryL_Liu >>

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

Reserved R to +3VSUS for Wake on WLAN function!

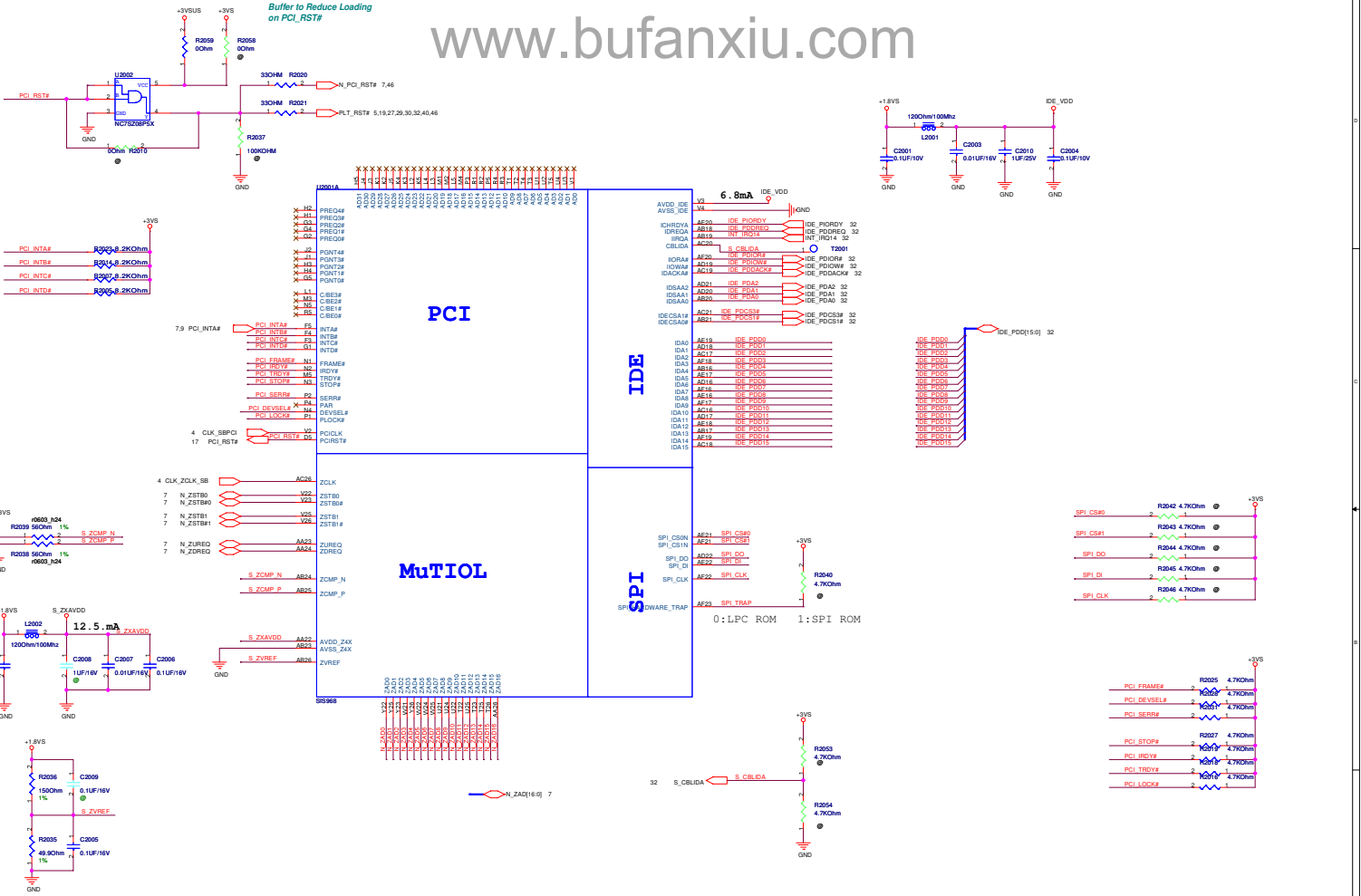


PN: 12G03000052B

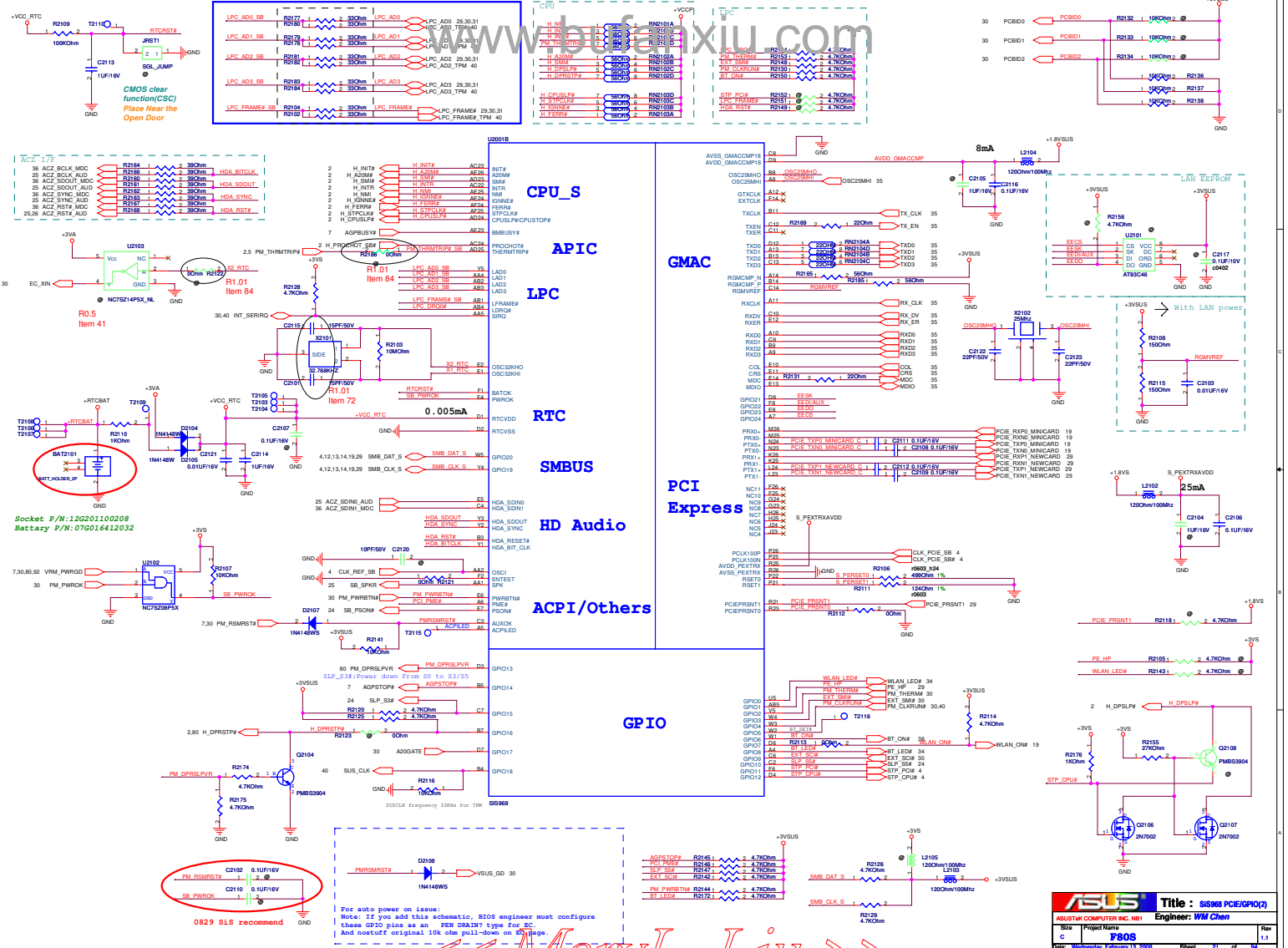


ASUS		Title : Mini card	
ASUSTek Computer INC		Engineer: WM Chen	
Size	Project Name	Rev	
B	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	19 of 94

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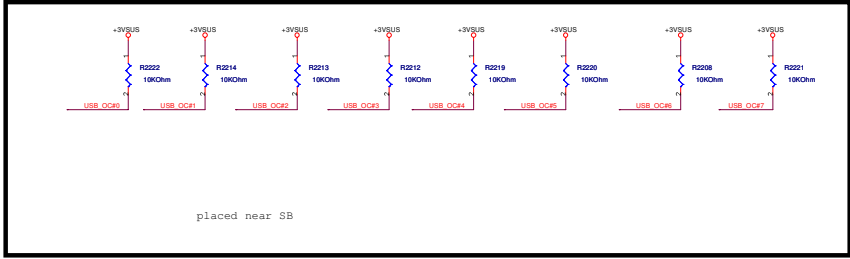
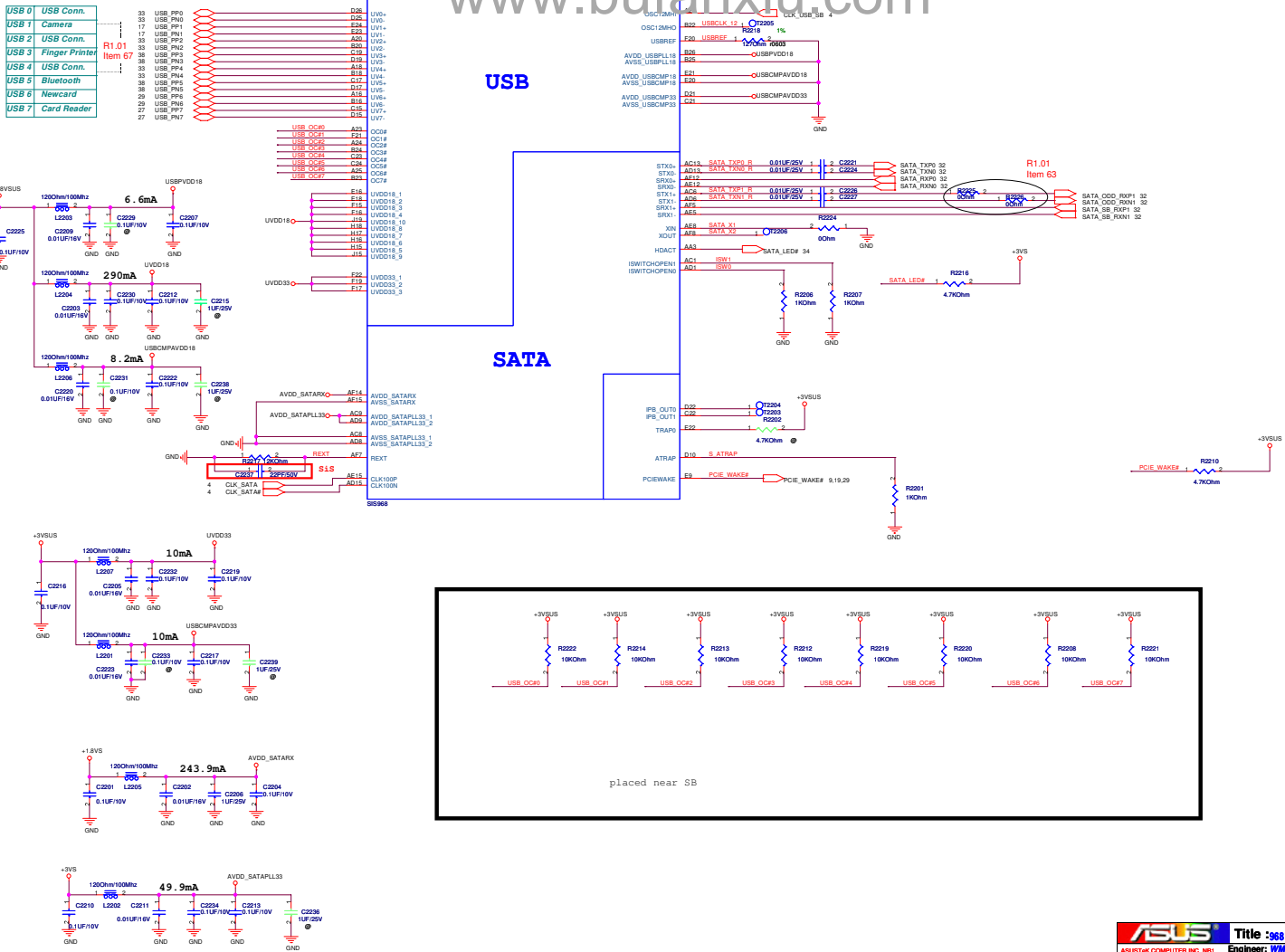


<< MaryL_Liu >>

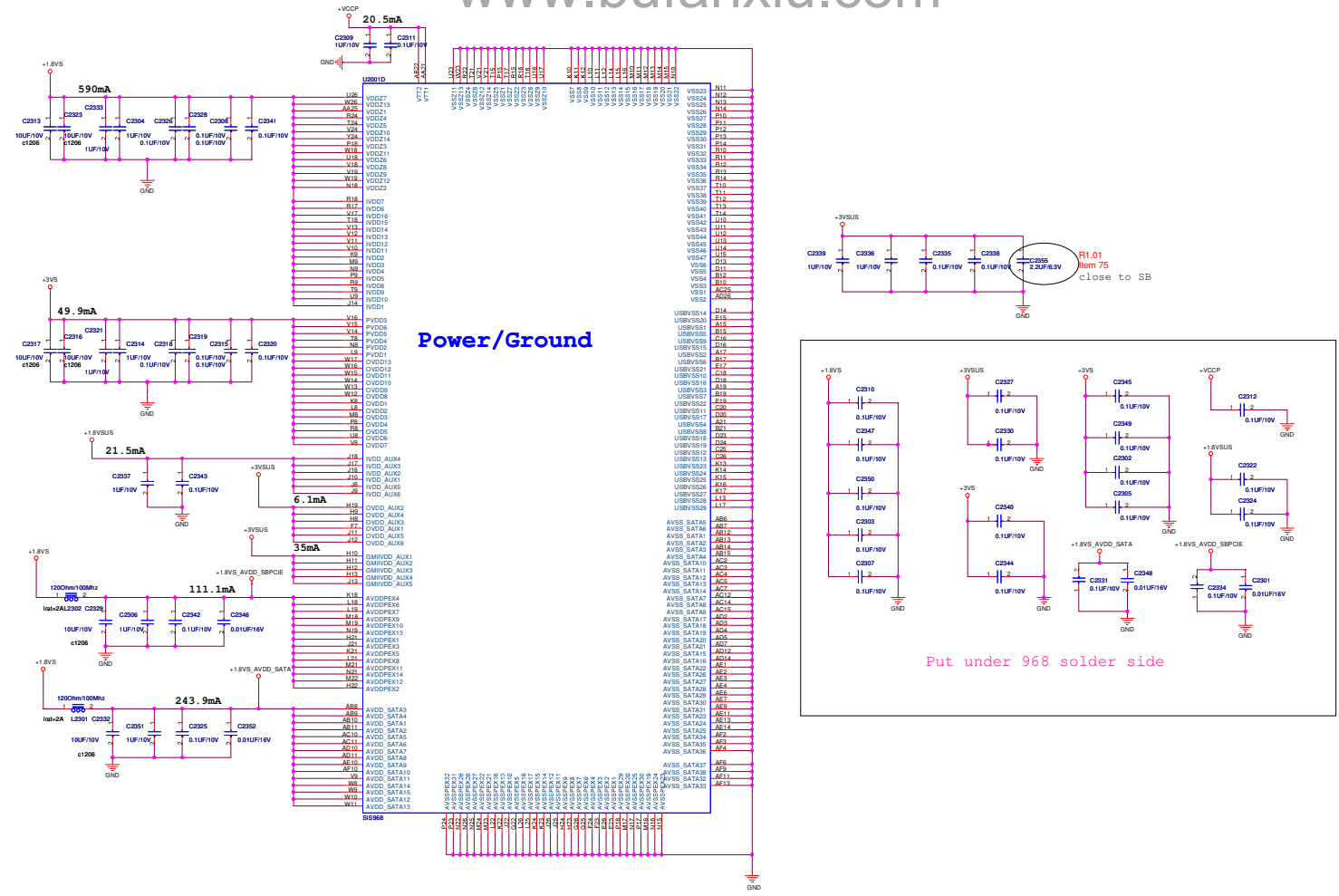


«MarryL_Liu»

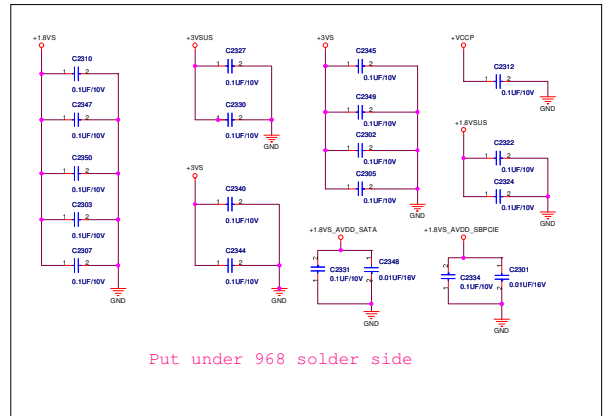
ASUS Title: S89S PCIe/GPI/Q2
 ASUSTEK COMPUTER INC. NBI
 Engineer: WM Chen
 Rev
 C Project Name
 Date: Wednesday, February 18, 2009 Ethen 21 of 24



<< MaryL_Liu >>



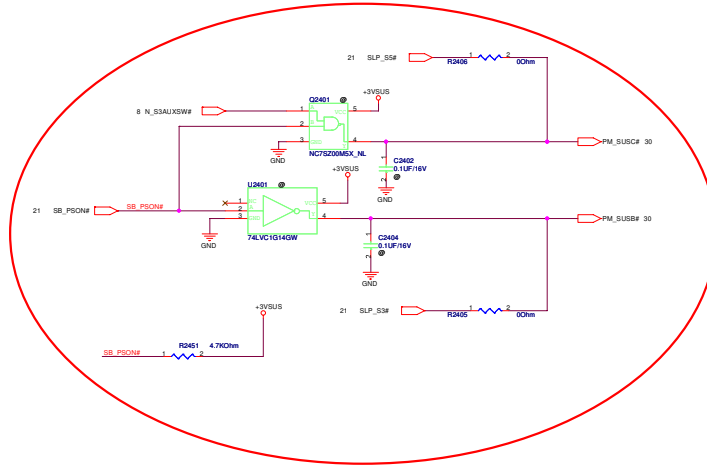
Power/Ground



ASUS		Title: 968 Power(4)	
ASUSTeK COMPUTER INC. (NFI)		Engineer: WM Chen	
S	Project Name		Rev
C	F80S		1.1
Date:	Wednesday, January 29, 2009	Sheet	25 of 24

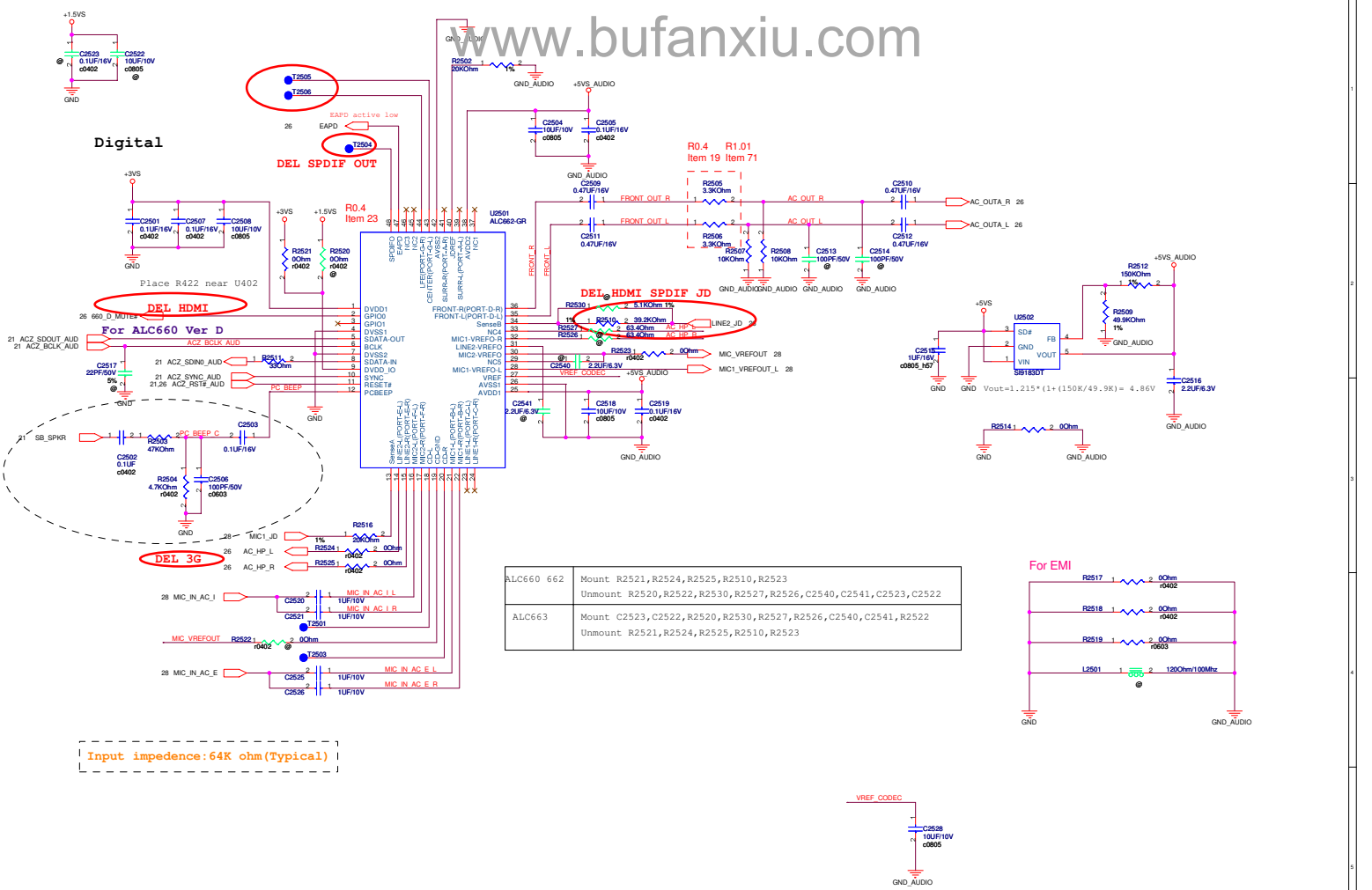
<< MaryL_Liu >>

0829 SIS recommend

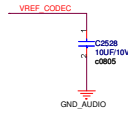
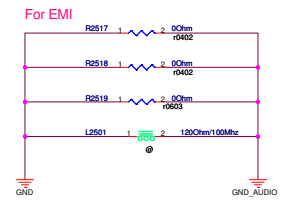


ASUS		Title : 988 Step(5)	
ASUSTEK COMPUTER INC. NEI		Engineer: WW Chen	
Size	Project Name	Rev	
c	P80S	1.1	
Date: Wednesday, February 11, 2009	Sheet	24	of 24

<< MaryL_Liu >>



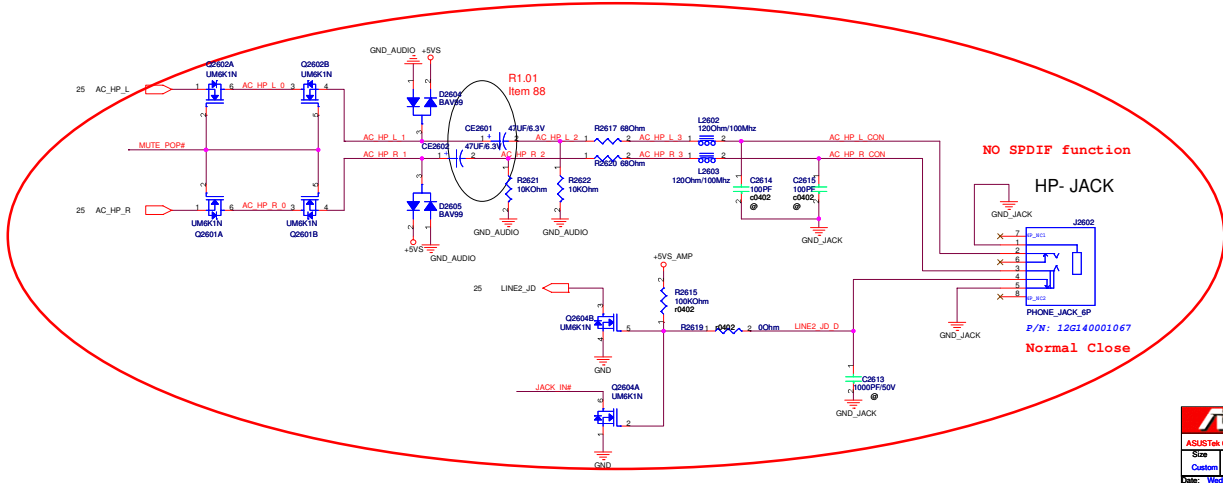
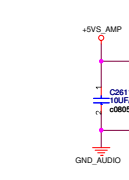
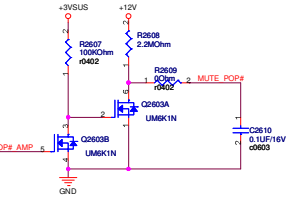
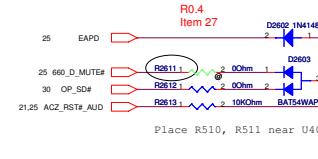
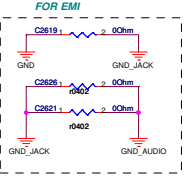
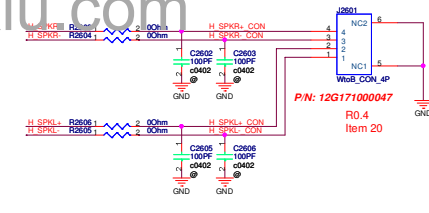
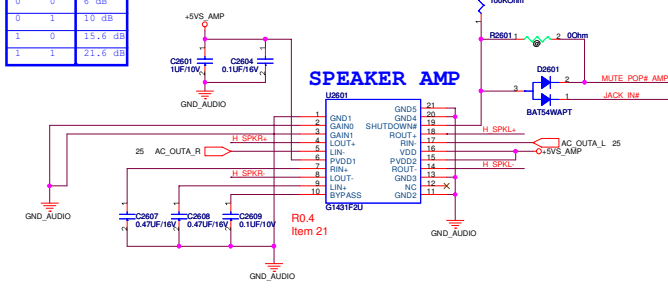
Input impedance: 64K ohm (Typical)



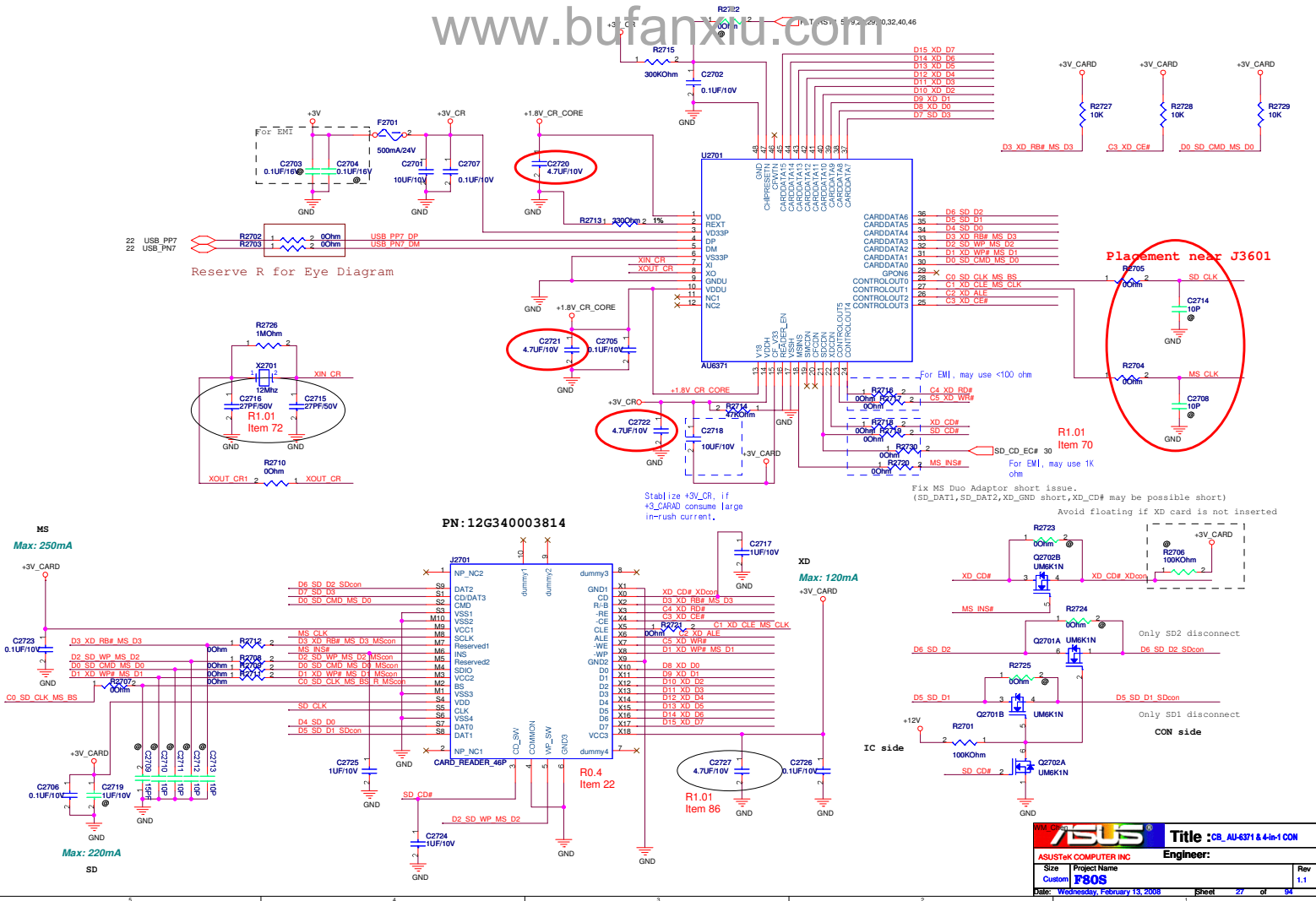
ASUS		Title: ALC660-GR
ASUSTek COMPUTER INC	Engineer: WM Chen	
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	25 of 24

<< MaryL_Liu >>

GA1NO	GA2NI	Av(±mV)
0	0	5 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



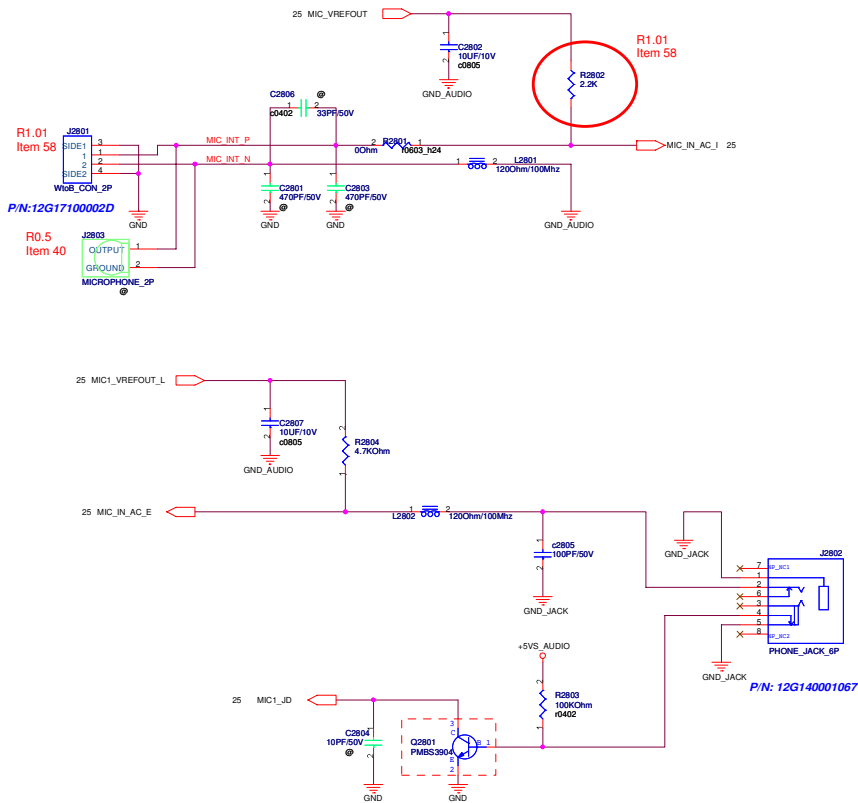
<< MaryL_Liu >>



ASUS		Title : CB_AU-6371 & 4-in-1 COM	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Customer	Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008 Sheet 27 of 84			

<< MaryL_Liu >>

Internal MIC Pre-Amplifier



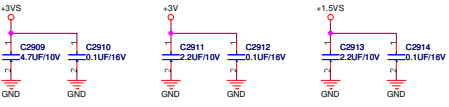
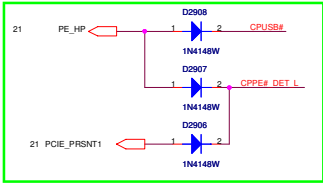
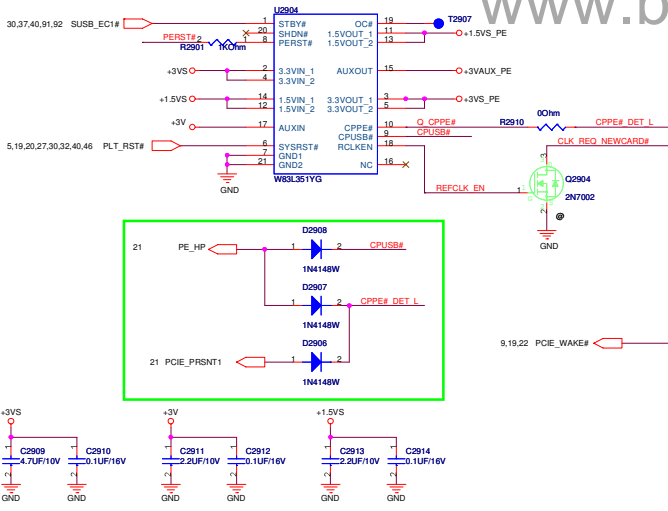
<Variant Name>

ASUS		Title : MICROPHONE
ASUSTEK COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	28 of 34

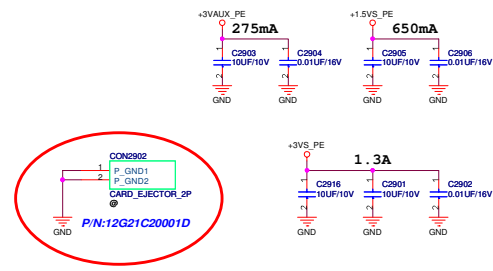
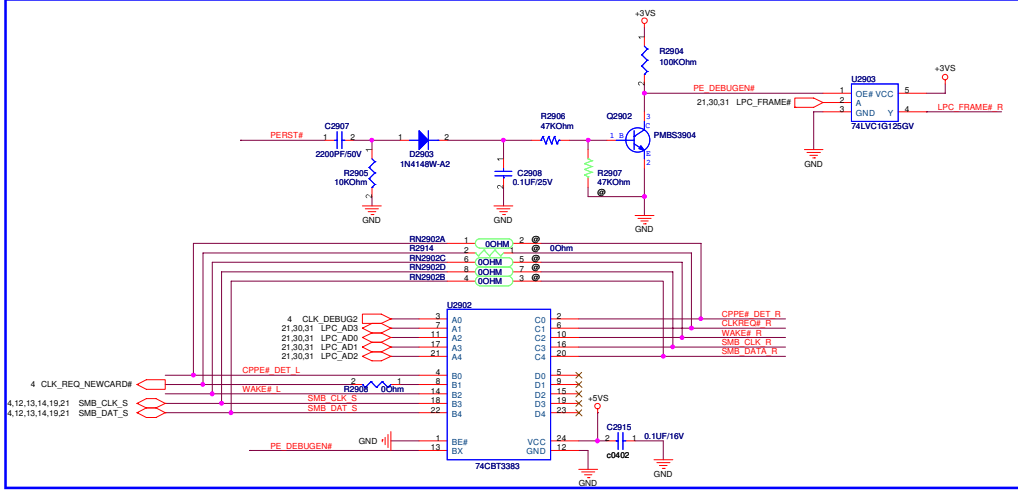
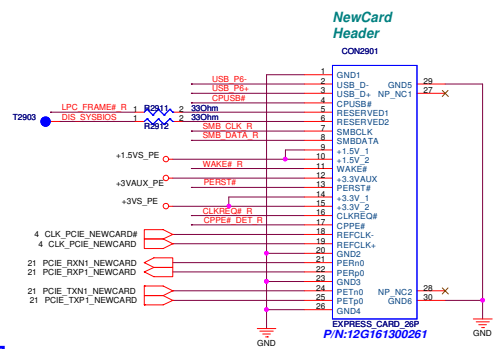
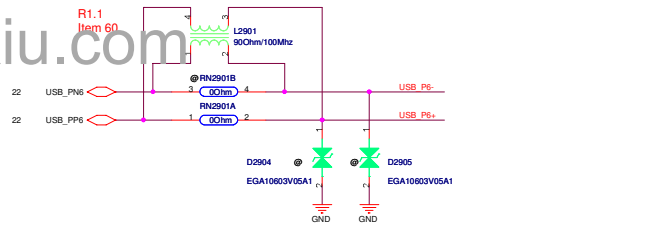
<< MaryL_Liu >>

New EC pin to avoid the re-recognize when resume from S3/S4.

CHANGE TO WINBOND



R1.1 Item 60

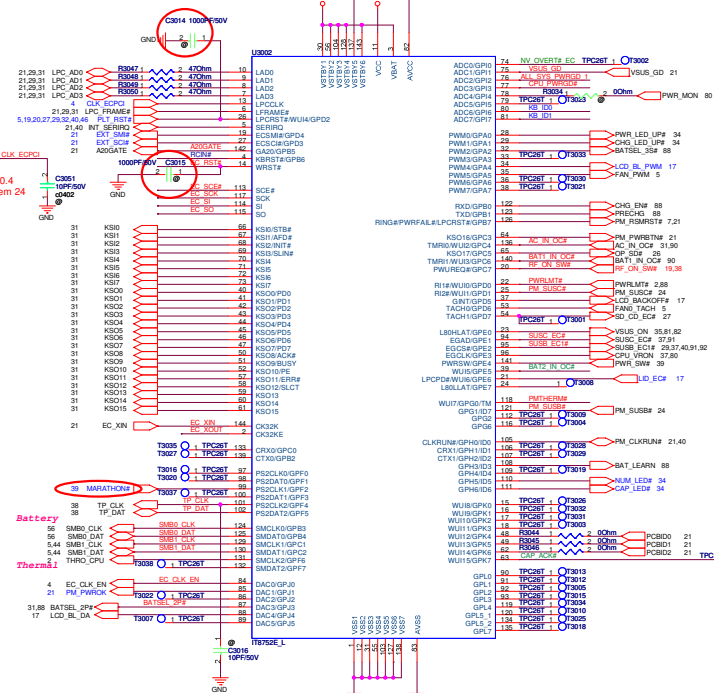


ASUSTek COMPUTER INC. Li-Te Rd., Peitou, Taipei, Taiwan, ROC. NEW CARD. Document Number: F80S. Date: Wednesday, February 13, 2008. Sheet 29 of 94.

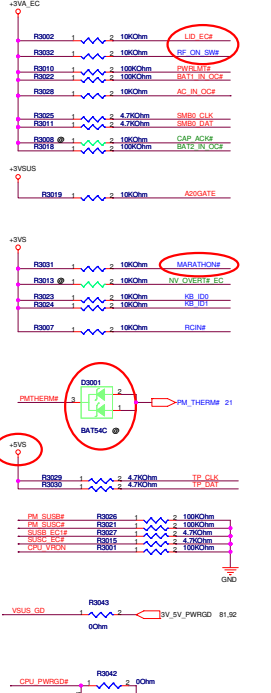
<< MaryL_Liu >>

IT8752 Core Chip

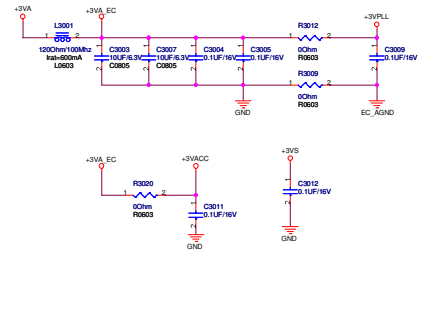
Standby (Sleep) Power Consumption:
0.1mA @ 3.3V = 0.33mW



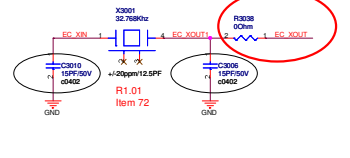
EC Pull Up/Down



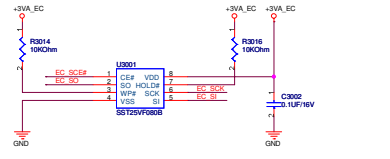
EC Power



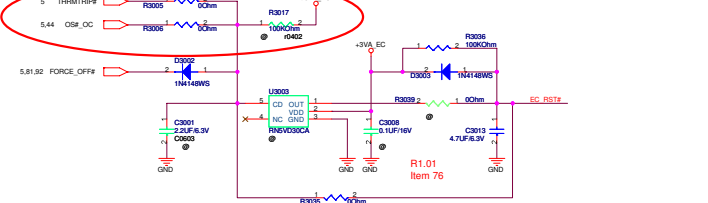
EC XTAL



SPI ROM



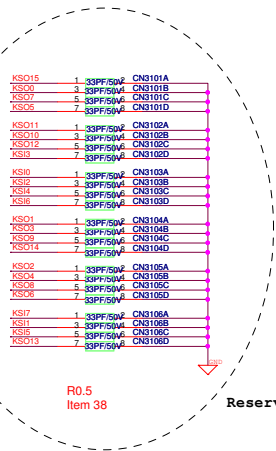
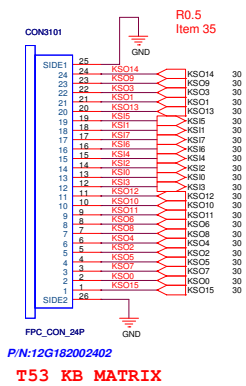
EC Reset



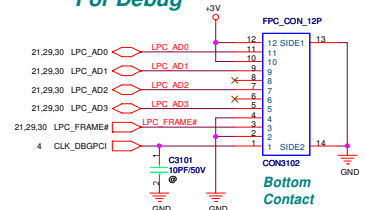
ASUS
ASUSTeK COMPUTER INC
Title: EC-IT8752
Engineer:
Size: Project Name: P808
Date: 2008/04/15 13:08
Rev: 1.1
Page: 30 of 35

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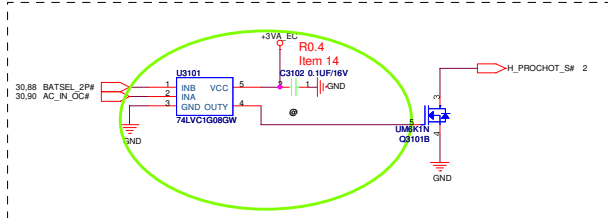
For Keyboard



For Debug



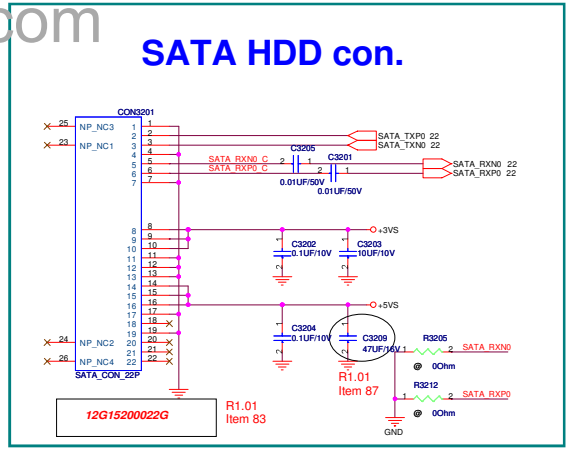
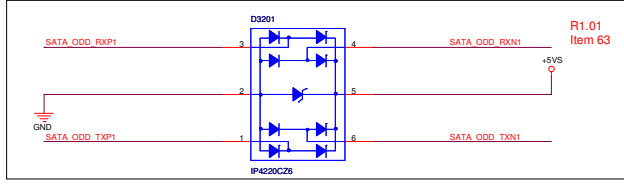
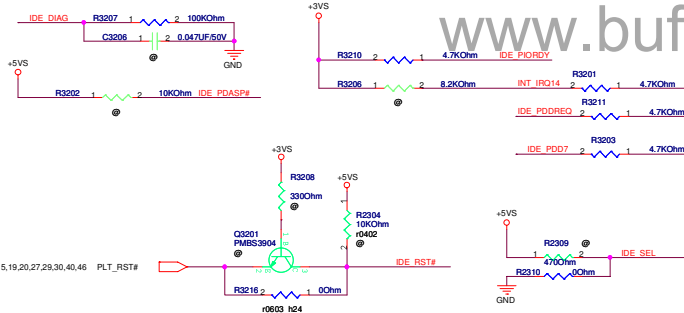
PWRLMT Circuit: For 65W adaptor.



<Variant Name>

ASUS		Title : KB conn	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008	Sheet	31	of 34

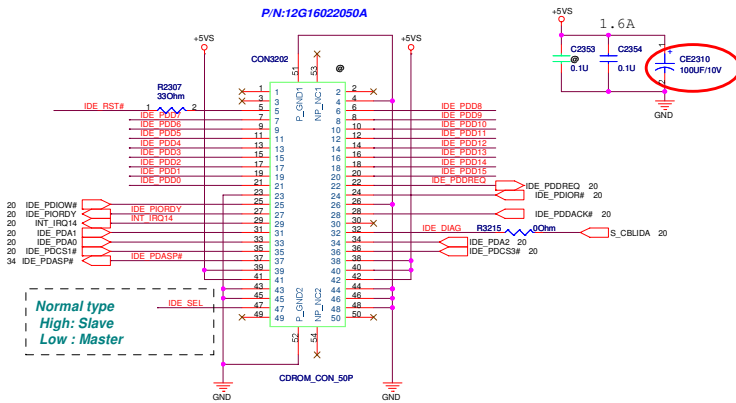
« MaryL_Liu »



CD-ROM

PATA CD-ROM CON

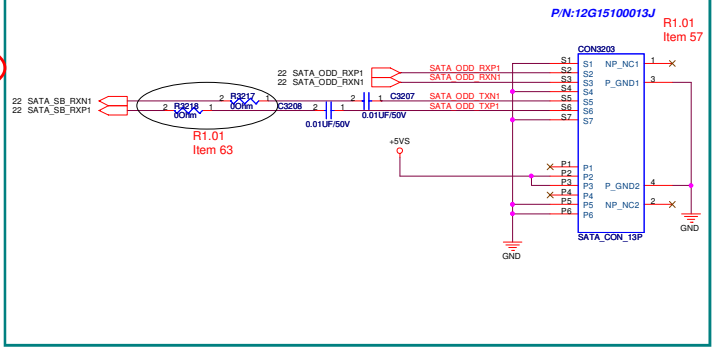
P/N: 12G16022050A



Normal type
High: Slave
Low: Master

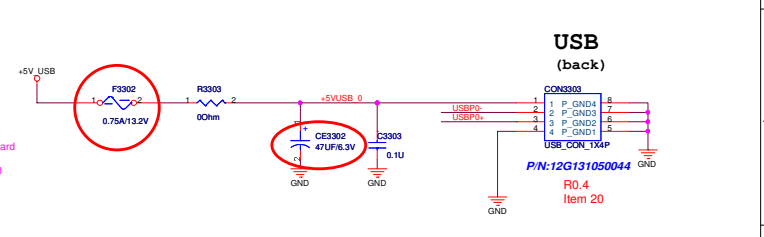
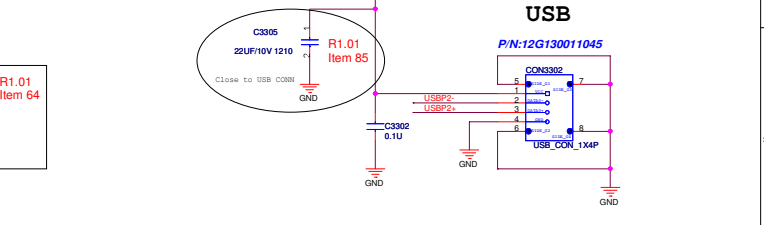
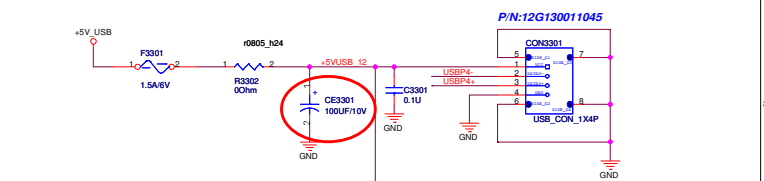
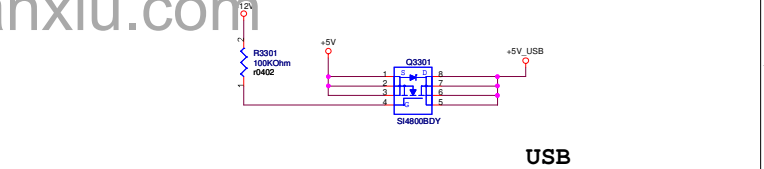
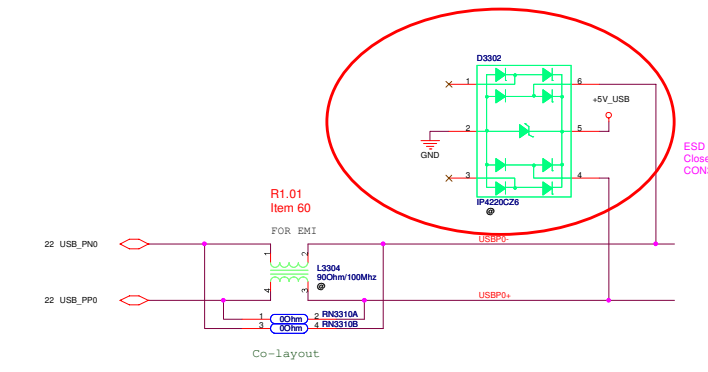
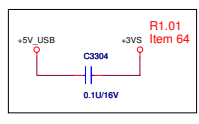
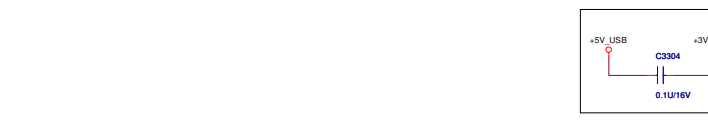
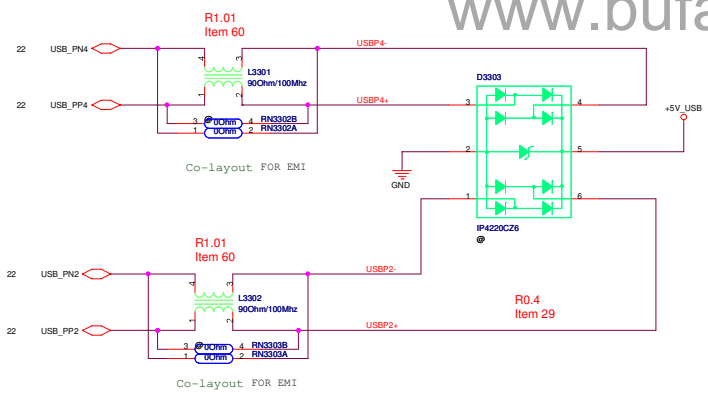
SATA CD-ROM con.

P/N: 12G15100013J



ASUS		Title : HDD & CD-ROM	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Custom	F80S
Date	Wednesday, February 13, 2008	Sheet	32 of 34

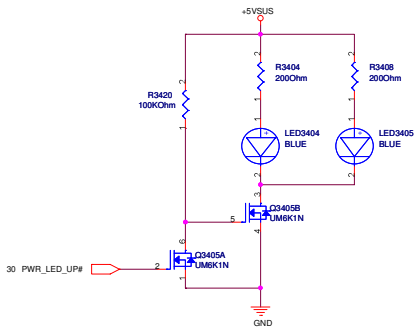
« MaryL_Liu »



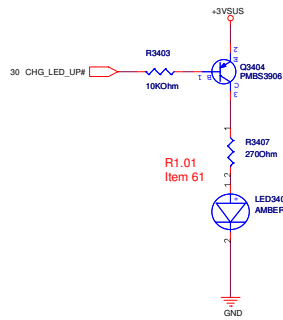
ASUS		Title : USB PORTS	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	FBOS	1.1	
Date: Wednesday, February 13, 2008		Sheet 33 of 34	

<< MaryL_Liu >>

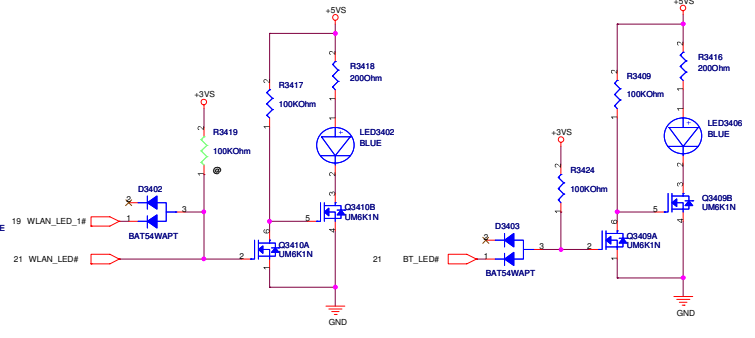
PWR LED



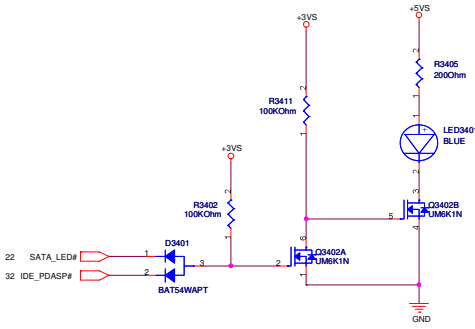
For BATTERY LED



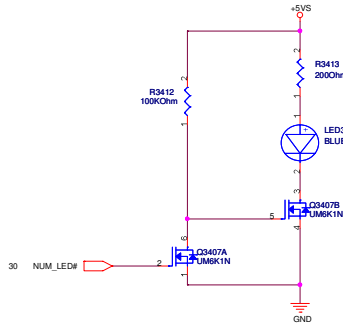
BT LED



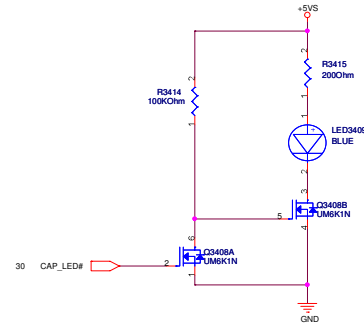
SATA/IDE LED



Num Lock

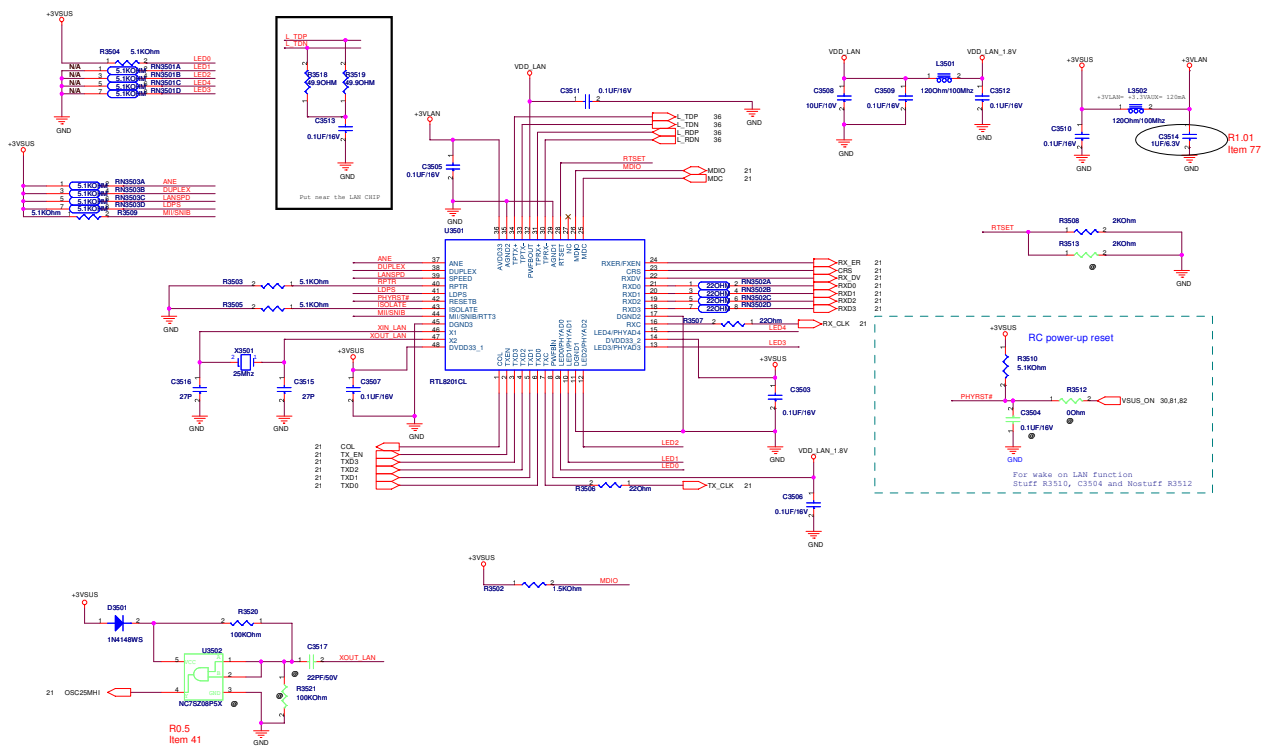


Cap. Lock



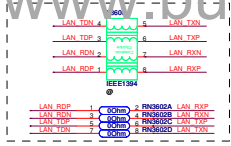
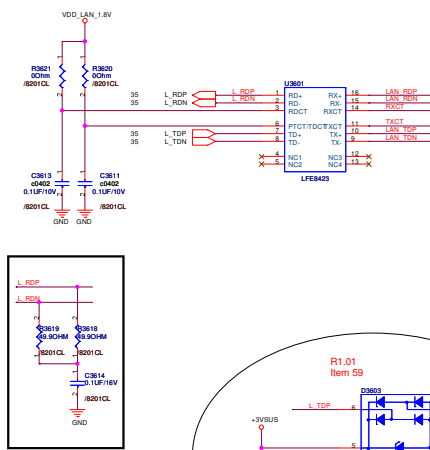
-Variant Name-		Title : LED	
ASUS		Project Name: F80S	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site:	Project Name:	Rev:	1.1
Custom:	F80S	Date:	Wednesday, February 13, 2008
		Sheet:	34 of 34

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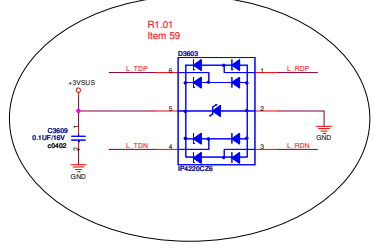
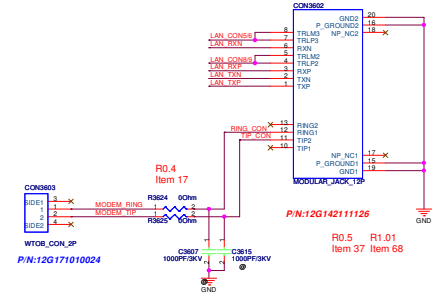


ASUS		Title : LAN 10/100 PHY
ASUSTEK COMPUTER INC. NBI		Engineer: WM Chen
Size	Project Name	Rev
C	F80S	1.1
Date: Wednesday, February 18, 2009		Sheet: 35 of 34

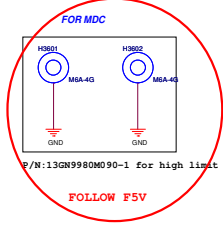
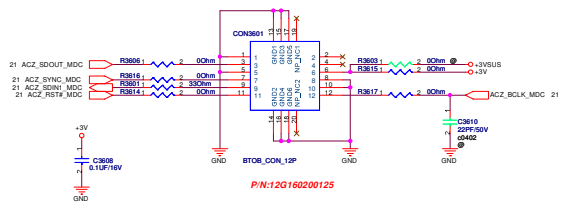
<< MaryL_Liu >>



LAN / MODEM PORT



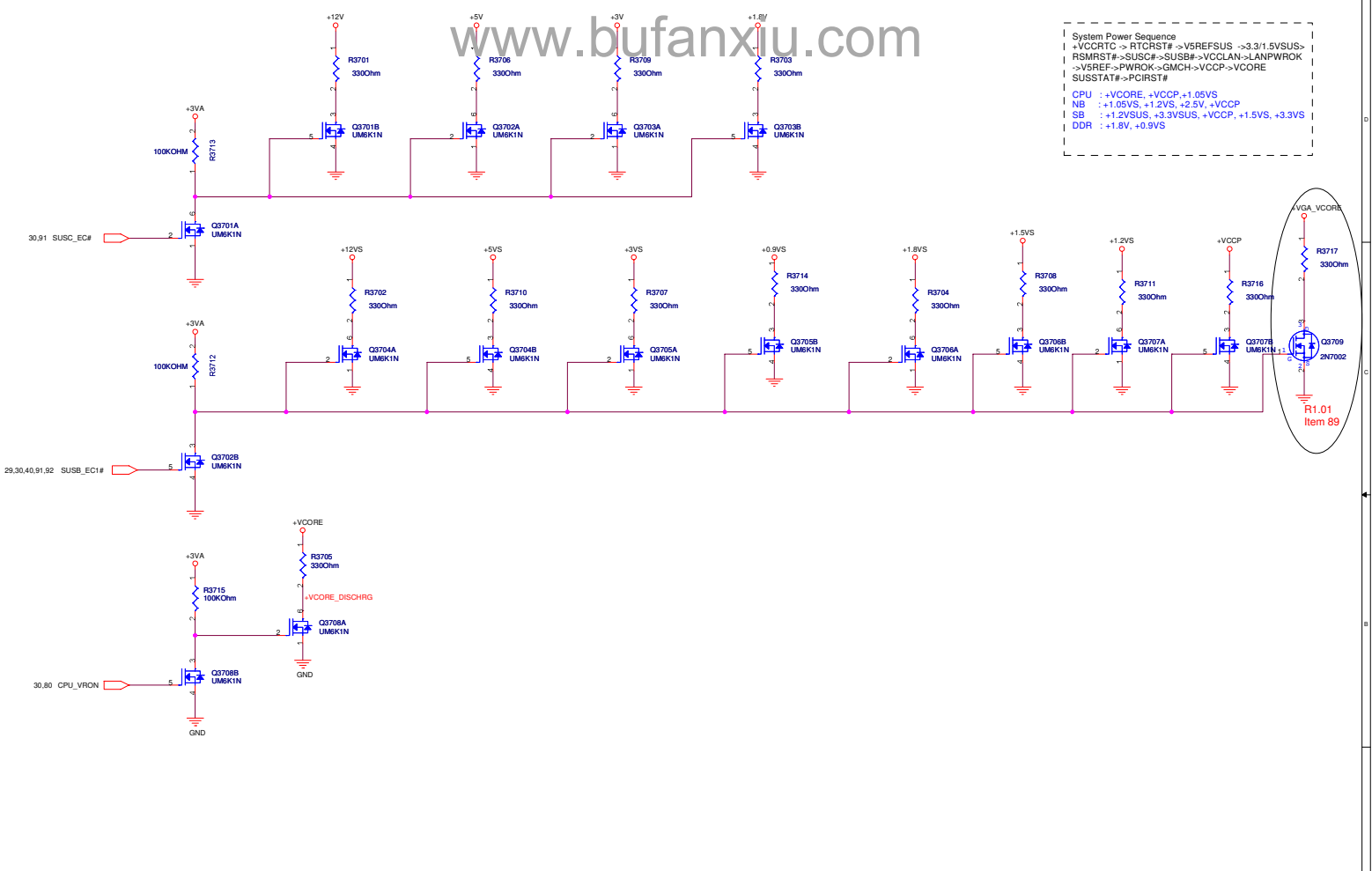
MDC



ASUS		Title : RJ11+M3 & MDC	
ASUSTEK COMPUTER INC.		Engineer: WM Chen	
Doc	Project Name	Rev	1.1
P80S			
Date: Wednesday, February 18, 2009	Sheet	35	of 34

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System Power Sequence
 +VCCRSTC -> RTCRST# -> V5REFSUS -> 3.3/1.5VSUS->
 RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK->
 V5REF->PWROK->GMCH->VCCP->VCORE
 SUSSTAT#->PCRST#
 CPU : +VCORE, +VCCP, +1.05VS
 NB : +1.05VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS

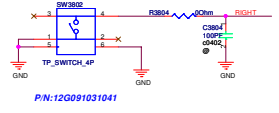
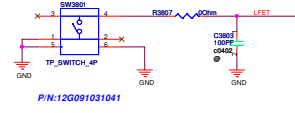
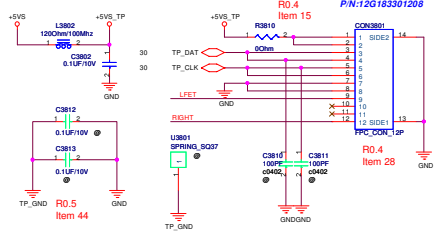


<Variant Name>

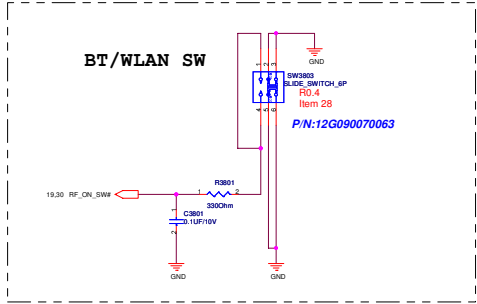
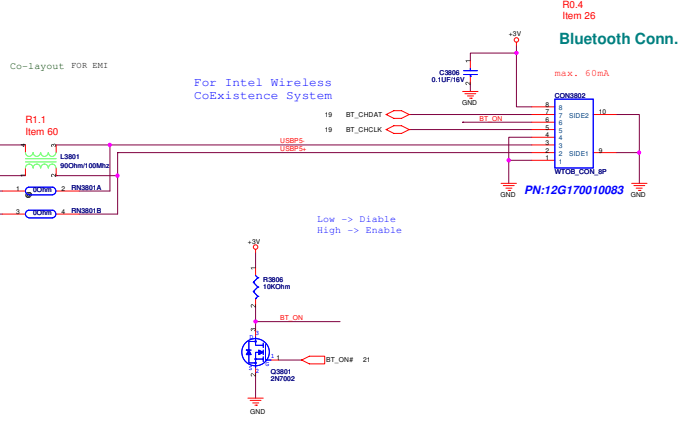
ASUS		Title : DISCHARGE CKT	
ASUSTEK COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet	37 of 34

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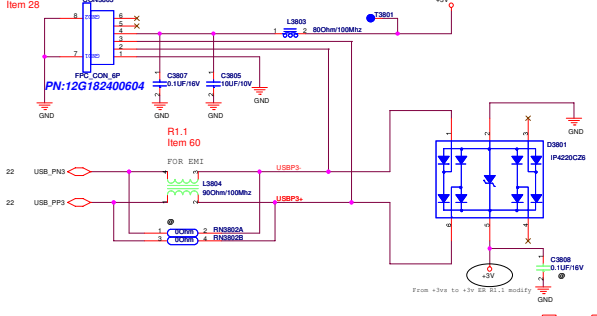
Touch-Pad



For Bluetooth



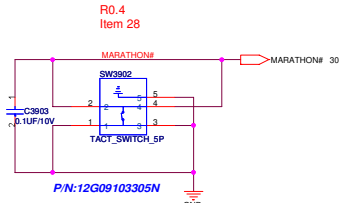
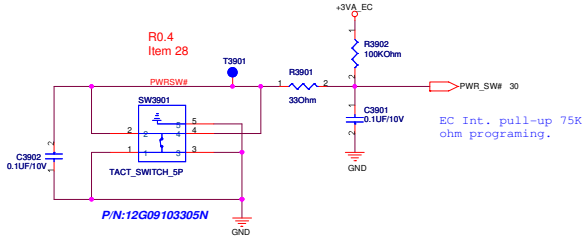
Finger Printer Conn.



ASUS		Title : BT&TP&FP	
ASUSTEK COMPUTER INC. NBI		Engineer: WM Chen	
Size	Project Name	Rev	
C	F80S	1.1	
Date: Wednesday, February 18, 2009	Sheet: 35	of	34

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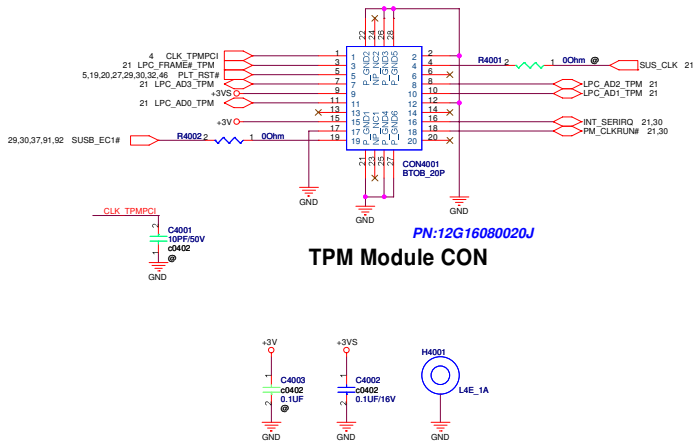
Power Button



<Variant Name>

		Title : SWITCH	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	39 of 34

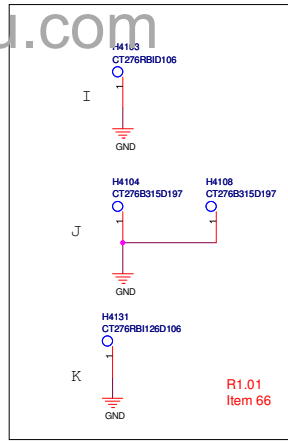
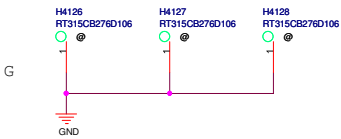
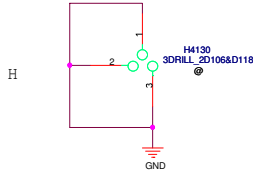
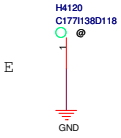
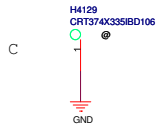
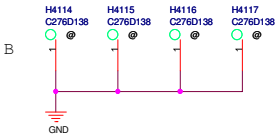
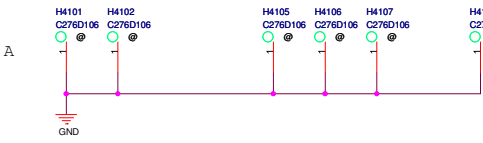
<< MaryL_Liu >>



<Variant Name>			
ASUS		Title : TPM	
ASUSTek COMPUTER INC. NBI		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	40 of 84

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R0.5
Item 36



		Title : Screw hole	
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name		Rev
B	F80S		1.1
Date: Wednesday, January 30, 2008		Sheet	41 of 94

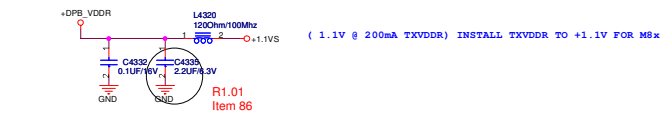
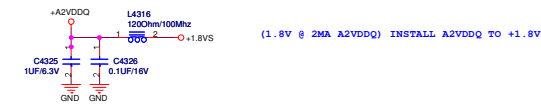
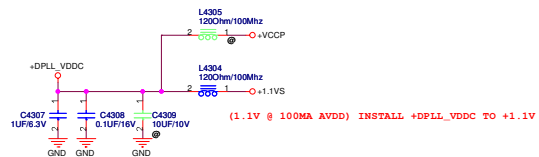
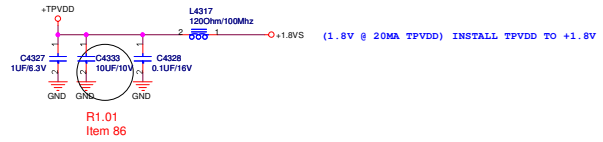
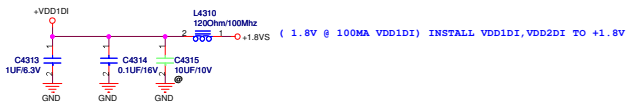
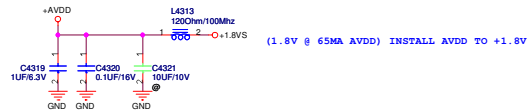
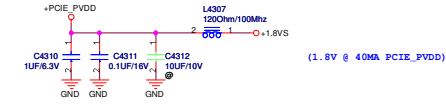
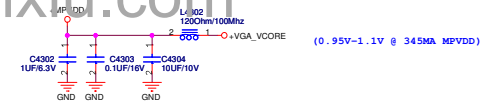
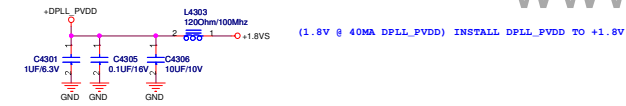
<< MaryL_Liu >>

		Title :BLANK
ASUSTek COMPUTER INC		Engineer: WM Chen
Size	Project Name	Rev
Custom	F80S	1-1
Date: Wednesday, February 13, 2008	Sheet	42 of 84

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M8x Power

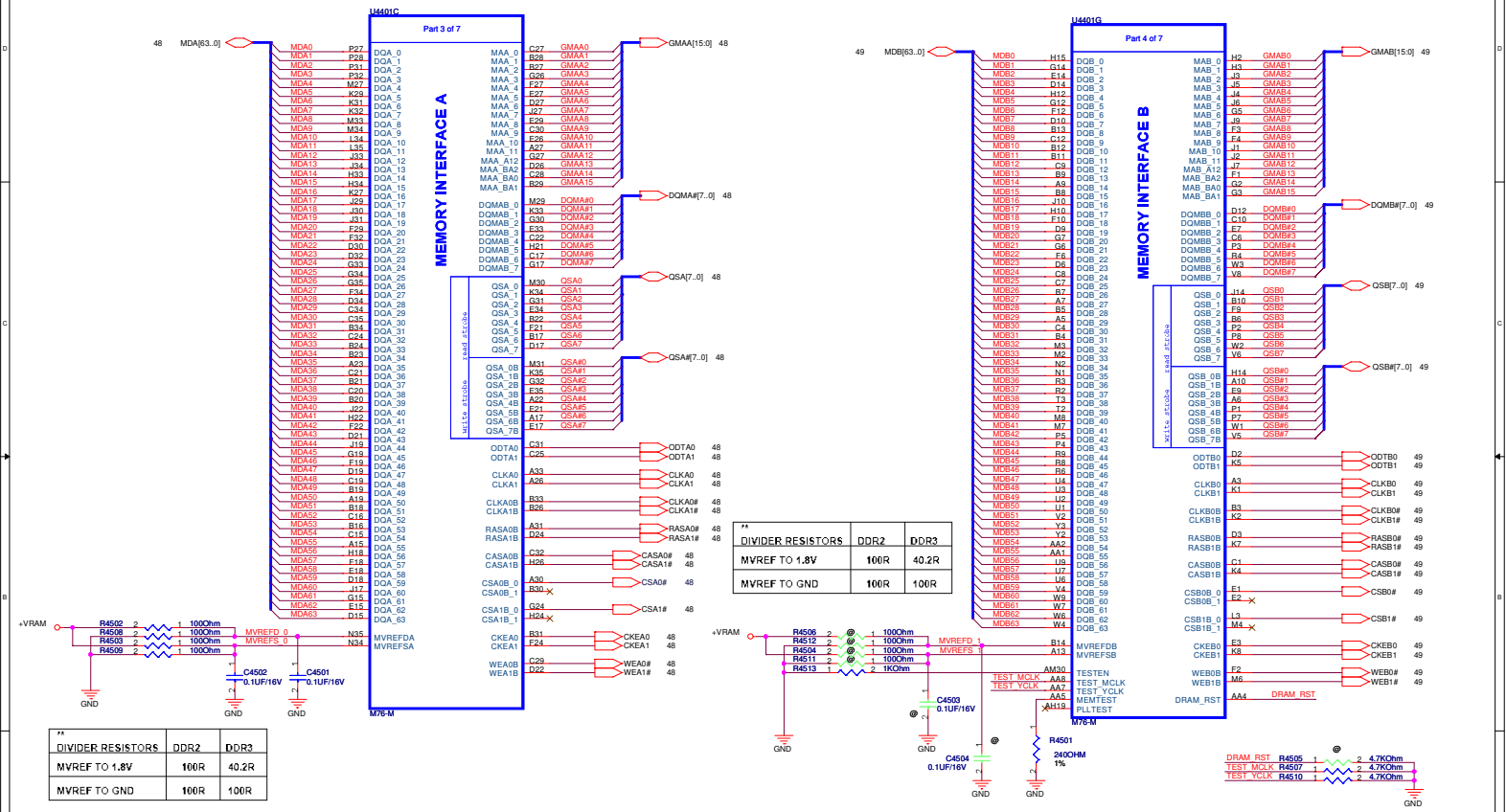
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



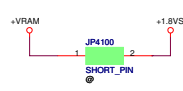
<Variant Name>

ASUS		Title : VGA M8x-M POWER	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Date	Rev
Custom	F80S	Wednesday, January 30, 2008	1.1
		Sheet	43 of 84

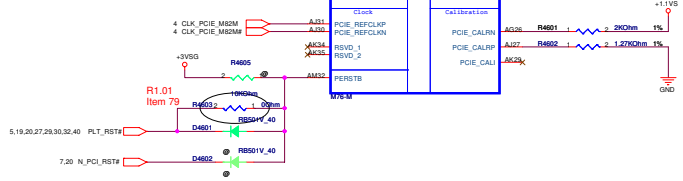
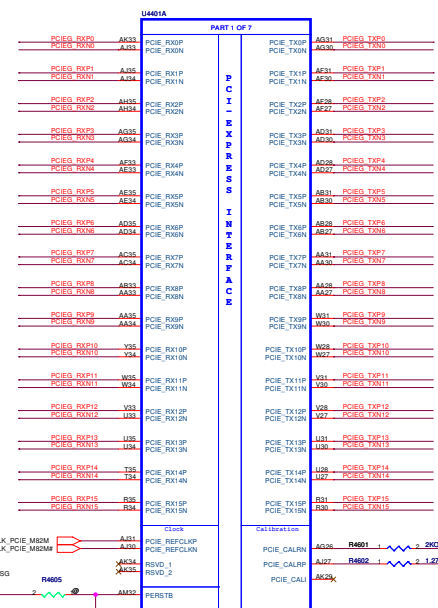
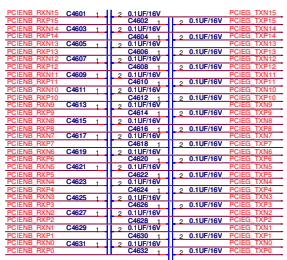
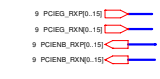
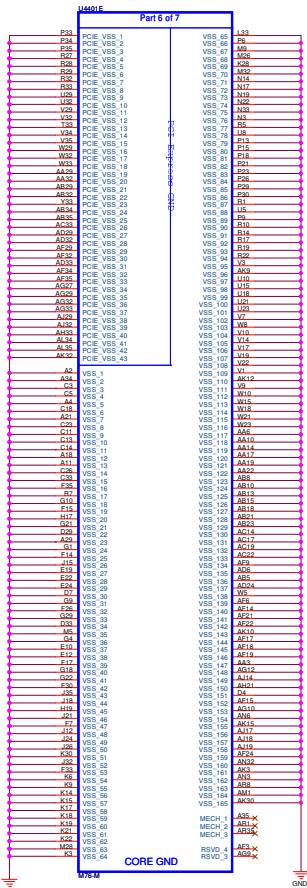
<< MaryL_Liu >>



MVREF TO 1.8V	DDR2	DDR3
100R	100R	40.2R
MVREF TO GND	100R	100R

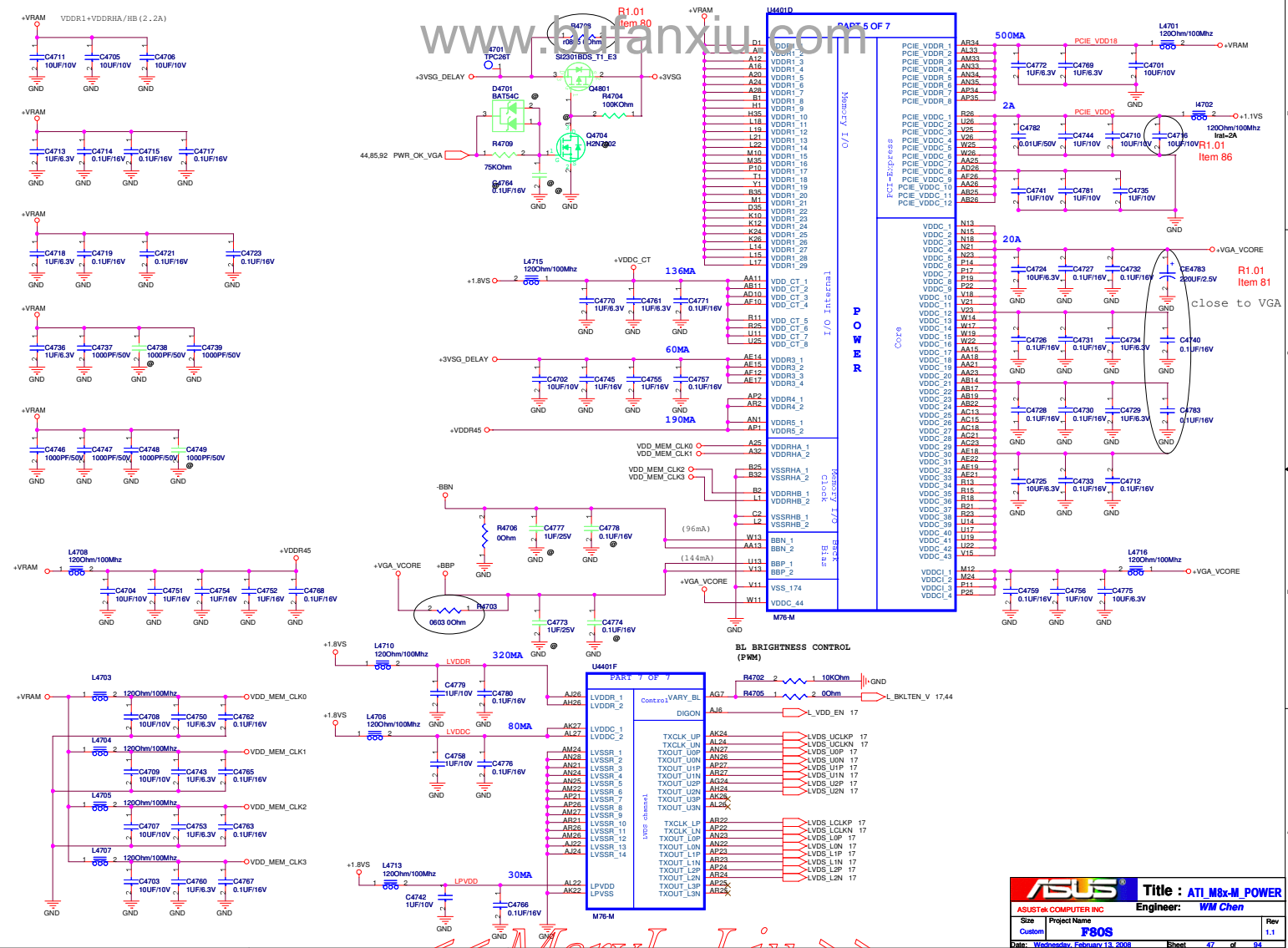


<< MaryL_Liu >>



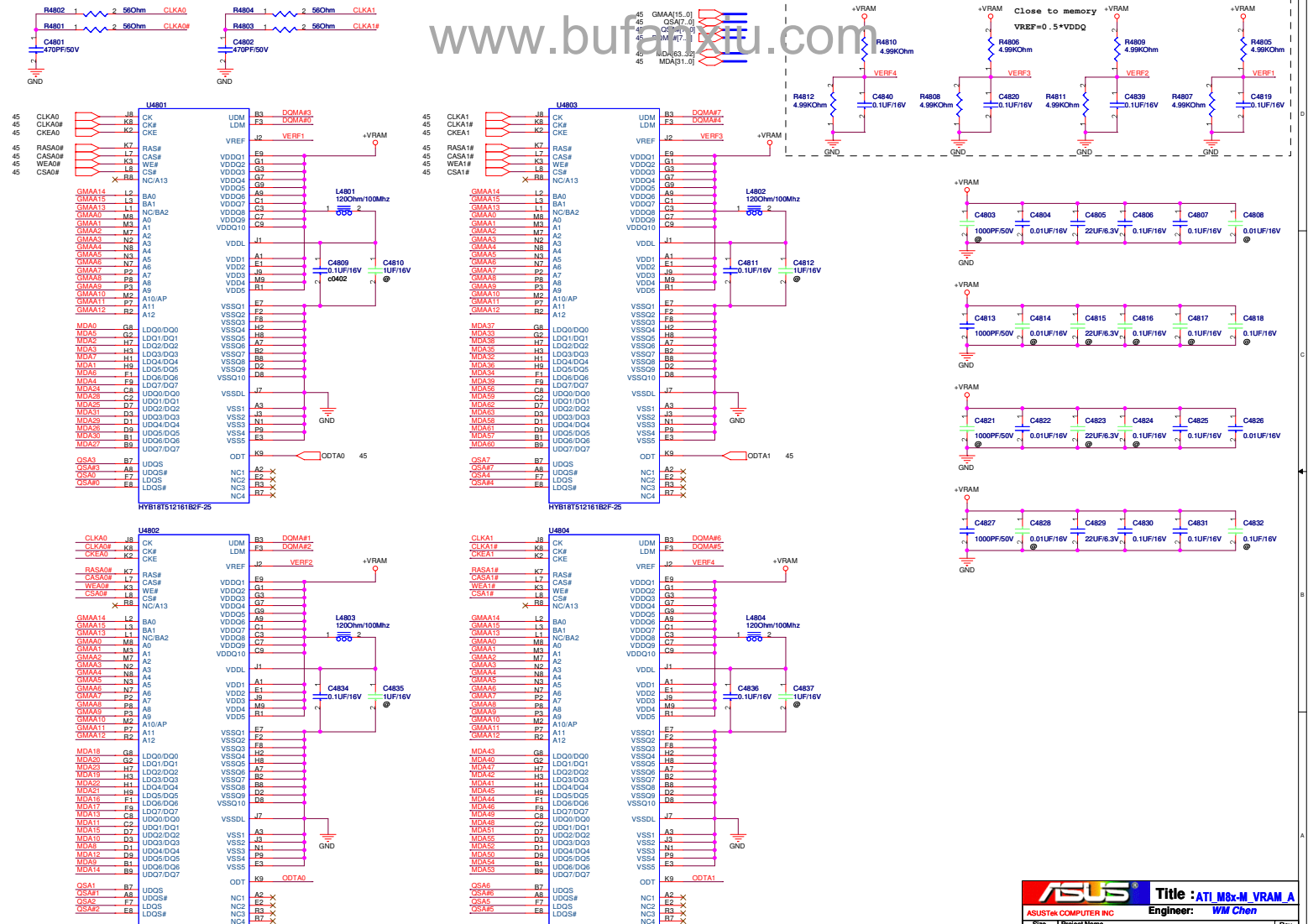
ASUS Title: **ATI M8-M PCI-E**
 ASUSTek COMPUTER INC. Engineer: **WM Chen**
 Size: **F80S** Project Name: **F80S** Rev: **1.1**
 Date: **Wednesday, February 15, 2006** Sheet: **48** of **54**

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ASUS		Title : ATU Mx-M POWER	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet	47	of 54

« MaryL Liu »

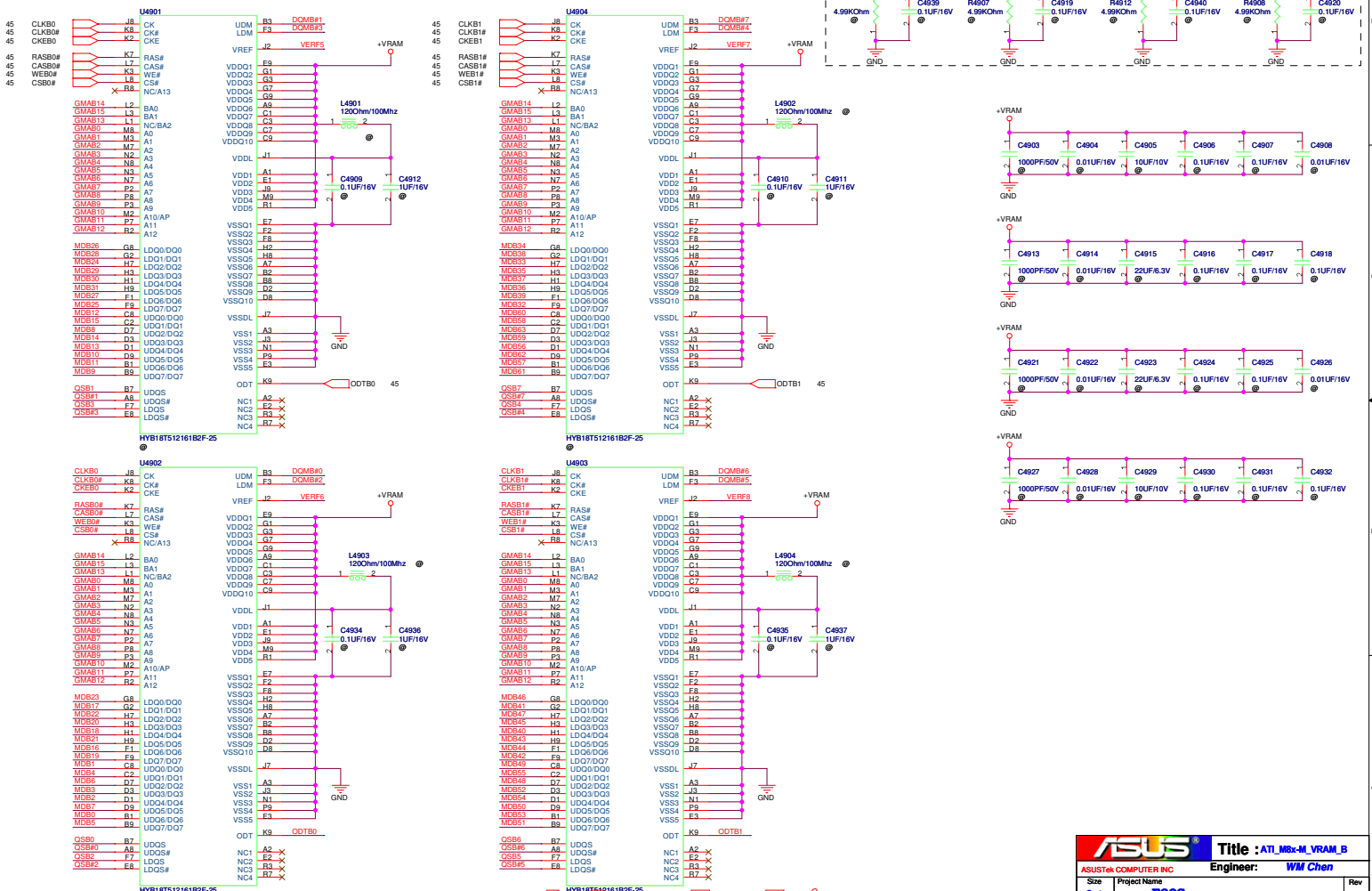


ASUS		Title : ATI M8x-M VRAM_A	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name	File	Rev
Custom	F80S	File: Wchsdslv_F80s13_2008	1.1
		Sheet	48 of 84

« MaryL_Liu »

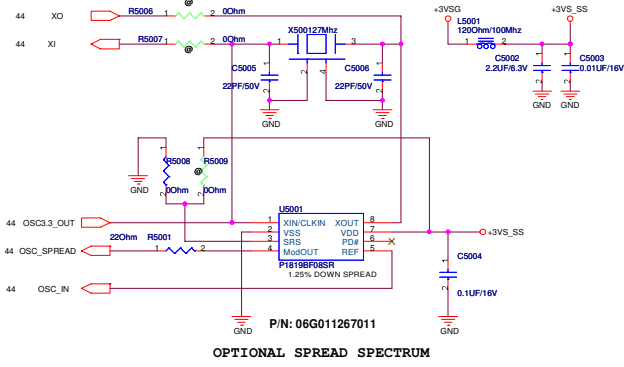
DO NOT INSTALL CHANNEL B WITH M82M

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ASUS		Title : AT1_M8x-M_VRAM_B	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet: 49 of 54	

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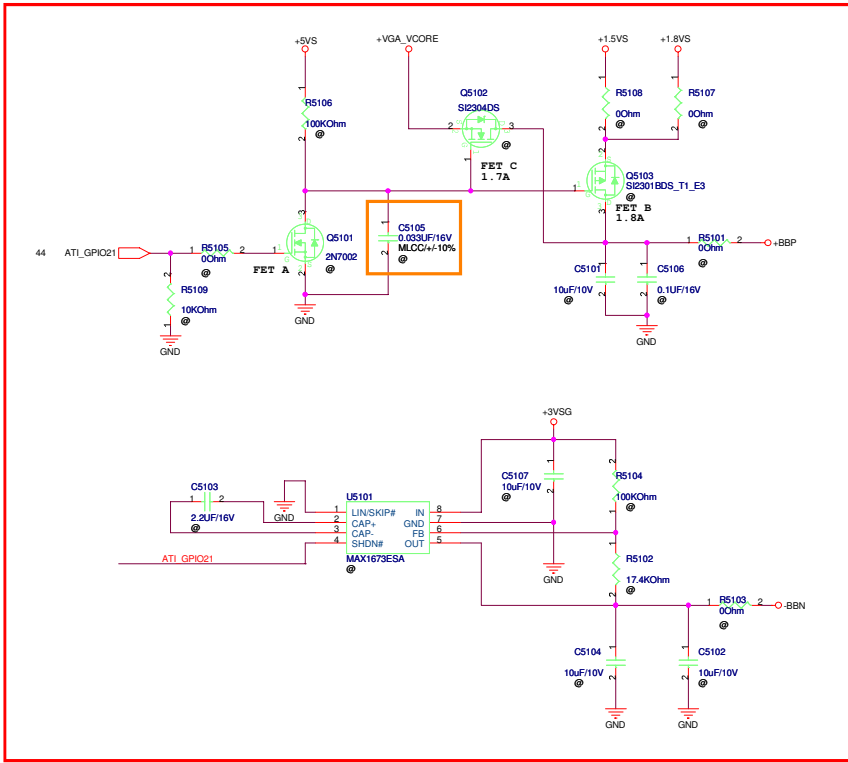
ASUS		Title : Blank Page	
ASUSTek COMPUTER INC		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	50 of 54

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COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = +VGA_CORE

R0.4
Item 30



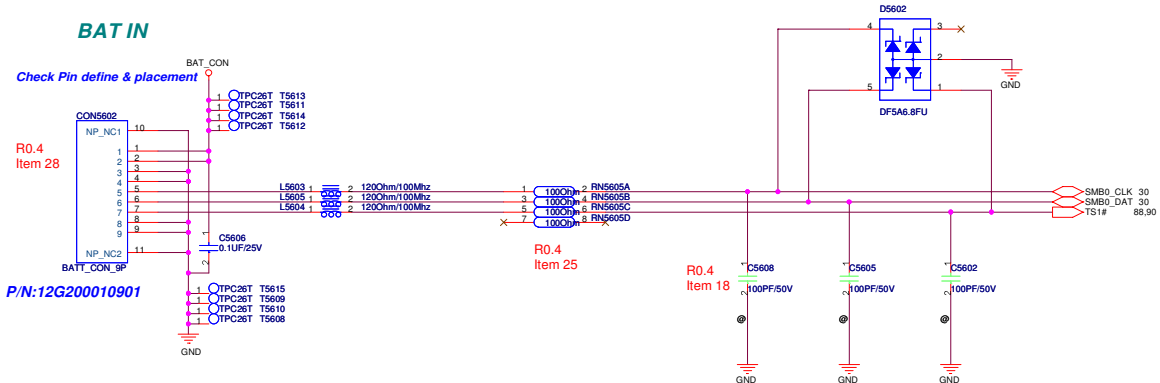
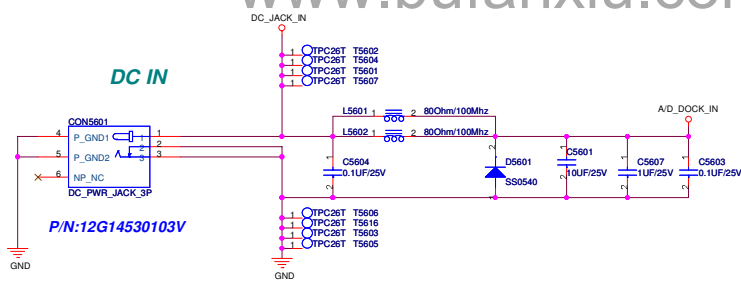
BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.5V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.5V

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V

GPIO_21_BB_EN	-BBN
0	GND
1	-0.5V

ASUS		Title : BACK BIAS
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
B	F80S	1.1
Date: Wednesday, February 13, 2008		Sheet 51 of 94

<< MaryL_Liu >>



ASUS		Title : AC/BAT JACK	
ASUSTek COMPUTER INC. NB1		Engineer: WM Chen	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008	Sheet 56	of 94	

<< MaryL_Liu >>

R0.4
Item 31

D

D

C


C

B

B

A

A

		Title : Empty
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 57 of 94

<< MaryL_Liu >>

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : BLANK
ASUSTeK COMPUTER INC. NB1		Engineer: WM Chen
Size	Project Name	Rev
A	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 58 of 94

<< MaryL_Liu >>

5

4

3

2

1

R0.4 revision history:

1. Delete R511,R515,D503,C503,C509,Q505,R506 from 100K change to 0ohm for better signal quality .
2. Change D3302,D3303,D2107 from 1SS355 to 1N4148WS-L for cost down.
3. Change D3401,D3402,D2601,D2603 to BAT54WAPT for cost down and common part
4. Change D2106 to BAT54C for cost down.
5. Change U1701 to AH180-WG-7 for cost down.
6. Delete RN301,RN302 for not use on board CPU cost down.
7. Add R3047-R3050 for newcard debug card.
8. Change CAP_ACK# from pin24 to pin63 for EC(page30) pin assignment R0.06.
9. Add R3028 for net:AC_IN_OC# pull hi.
10. Change C3002 from 1uF to 0.1uF for cost down.
11. Change Q4203 from 2N7002 to PMBS3904 for cost down and MIC jack.
12. Unmount R1727 for pull hi in p34.Change L1716 to R1710 for U1701 on MB.
13. Change USB connector J2401- J2403.
14. Unmount C3102 for cost down.
15. Reserve R3810 for prevent power short cause large current.
16. Change R3404,R3403,R3412,R3414 from 4.7K to 10K for power saving.
17. Change L3601,L3605 to R3622,R3623 for EMI fine tune cost down.
18. Unmount C5608,C5605,C5602 for EMI fine tune cost down.
19. Change R2505,R2506 from 680ohm to 2.7Kohm for 1W speaker.
20. Change CON3303,J2601 part number for ME request.
21. Change U2601 from TI to GMT,C2609 to 0.1uF for cost down.
22. Change card reader connector J2701 part number for connector in bottom side.
23. Change U2501 from 660 to 662 for the logo request codec need 2-ADC after 2008/6.
24. Reserve C3051 for fine tune CLK_ECPCI.
25. Add RN5605 for protect EC to prevent voltage damage.
26. Change CON3802 pin assignment for use W7 BT cable.
27. Unmount R2611 for ALC662 not need.
28. Change SW3901,SW3902,SW3801,SW3802,SW3803,J2801,CON5602,BAT2101,CON3801,CON3803 part number for ME request.
29. Delete D3301 for cost down.
30. Add VGA Back Bias on page51 for power play function
31. +1.2VSUS from page57 change to page82 for power circuit
32. Delete H_PWRGD_EC (Q202,R233) because it's not necessary.

R0.5 revision history:

33. Reserve CON1901 pin24 to +3VAUX for Azurewave's Wireless-Lan Card.
34. Modify p25,p26 for colay ALC662 and ALC663 for sales reccommand.
35. Change KB connector CON3101 part number for ME request.
36. Change Screw hole for ME request .
37. Change CON3602 part number for ME request.
38. Cap. Array CN3101-CN3106 from 0805 change to 1206 size.
39. Add H4401,H4402 VGA NUT
40. Reserve internal mic J2803 for experiment.
41. Reserve U3502,U2103 circuit for experiment.
42. Add U1601,U1602 for NB output 3.3V level cost down.
43. Change page34 LED schematic for use Blue LED.
44. Reserve C3812,C3813 for EMI request TP_GND.
45. Modify Page 22,32 for sales require SATA ODD.
46. Change SW3801,SW3802 part number for ME request.
47. Change U3001 part number for cost down.
48. Reserve R208,C202 for H_CPURST#.
49. Add U3801 for EMI request.
50. Add RN1801-RN1804 for EMI request.
51. Delete VRAM termination
52. Add Q4405,R4411,C4466 for +3VSG
53. Change Hall-sensor U1701 part number for ME request.

R1.01 revision history:

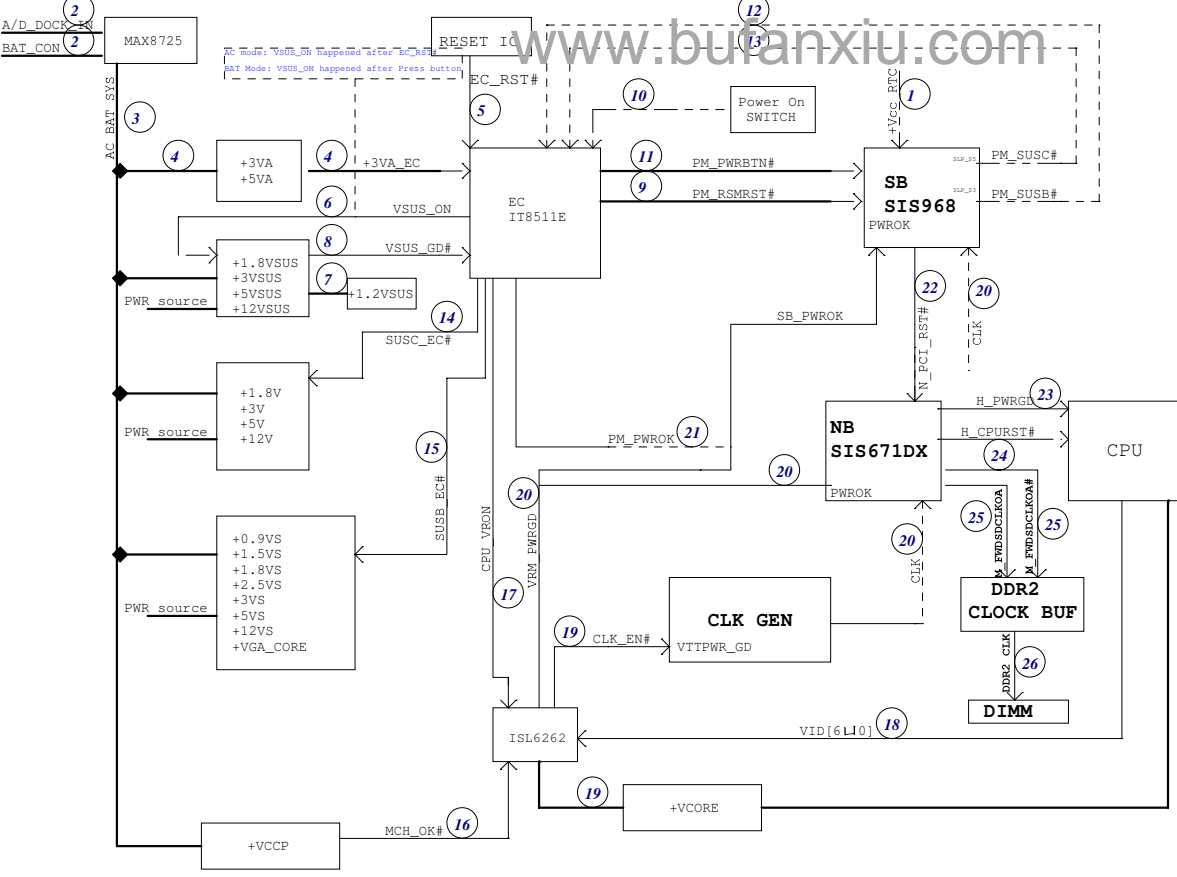
54. Unmount R4428 for leakage current issue.
55. Change R4435 from 7.5 to 50 for SIS request.
56. Mount Q440, Q441, R4413 37.4 ohm for VGA issue.
57. Change SATA ODD Connector CON3203 part number for ME request.
58. Change J2801 connector for Wire-MIC,change R2802 from 4.7K to 2.2K after test internal mic performance.
59. ADD D3603,C3609 for LAN ESD solution.
60. Change L1709,L3801,L3804,L3301,L3302,L3304,L2901 part number for colay footprint.
61. Change R3407,LED3403 value for meet factory LED spec.
62. Change VGA NUT H4401,H4402 to 13G021036001 for Thermal request.
63. Add D3201 IP4220C26 and R2225, R2226, R3217, R3218 0 ohm for EMI request.
64. Add C1218, C1707, C1814, C3304 0.1uF for EMI request.
65. Change R1402 from 22 to 10 for DDR Feedback quality.
66. Change Screw hole H4103, H4104, H4108 and Add H4131 for ME request.
67. Change USB external ports for controller.
68. Change CON3602 RJ11+45 part number for ME request.
69. Change R1705 from 100ohm to 330ohm for meet panel spec.
70. Add R2730 for factory recovery AU6371 driver CD.
71. Change R2505,R2506 from 2.7K to 3.3K for HDD-Speaker resonance issue.
72. Change C410,C417,C2101,C2115,C2715,C2716,C3006,C3010 value for TXC report suggest.
73. Del R1816,R1817 for SMT colay request.
74. Add R310 for +VCCA_CPU voltage ripple.
75. Add C2355 2.2uf for SB issue.
76. Unmount R3017,C3001,U3003,C3008,mount R3036,D3003,C3013,R3035,Add R3039 for cost down.
77. Add C3514 for Lan issue.
78. Mount R4459 and unmount Q4405, R4411,C4466 for cost down.
79. Add R4603 and unmount D4601 for cost down.
80. Mount R4708 and unmount Q4801,Q4704,R4709,R4704 for cost down.
81. ADD CE4783 220UF,C4740,C4783 0.1uF for VGA issue.
82. Mount R1611,R1612 from 0 ohm to 33 ohm and mount C1606,C1607 for meet spec.
83. Change CON3201 part number for ME request.
84. Add R2122,R2186 for SB issue.
85. Add C3305 22UF for meet spec.
86. Add C1905,C2727,C4333,C4334,C4335,C4716,Del C4331 for meet spec.
87. Del CE3202 100UF and Add C3209 47UF for ME request.
88. Change CE2601,CE2602 from 27uF to 47uF for better Low frequency response.
89. Add D4401,R3717,Q3709 for meet VGA spec.

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		Title :	
ASUSTek COMPUTER INC. NB1		Engineer: WM Chen	
Site	Project Name		Rev
Custom	F80S		1.1
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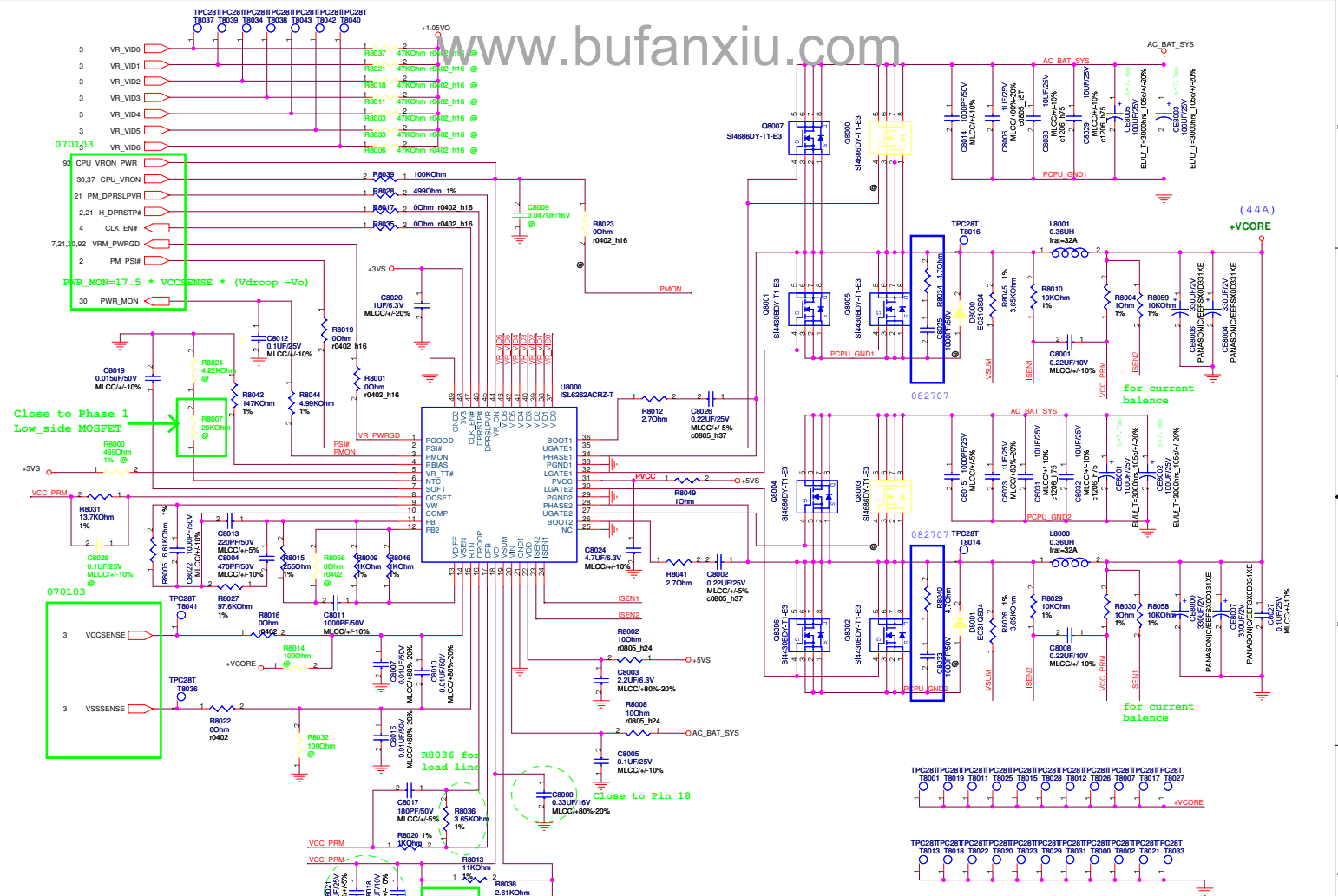
		Title : BLANK
ASUSTeK COMPUTER INC. NBI		Engineer: WM Chen
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 60 of 84

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Power On Sequence
 1 -----> 26

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Close to Phase 1
Low_side MOSFET

Close to Pin 18

Close to Phase 1
Inductor

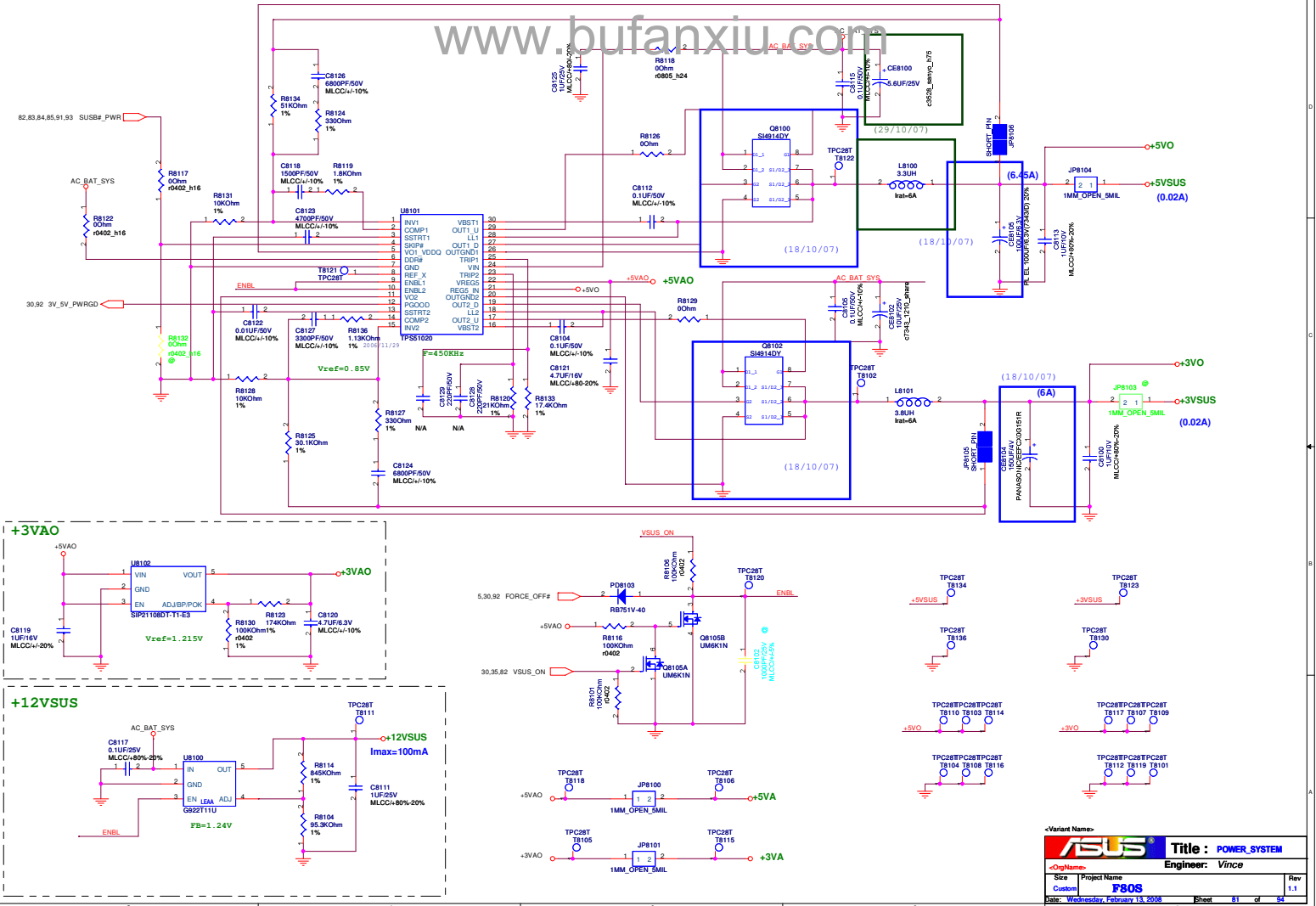
C8021 & C8018 for transient
response

R8036 for
load line

VCC_PRIM

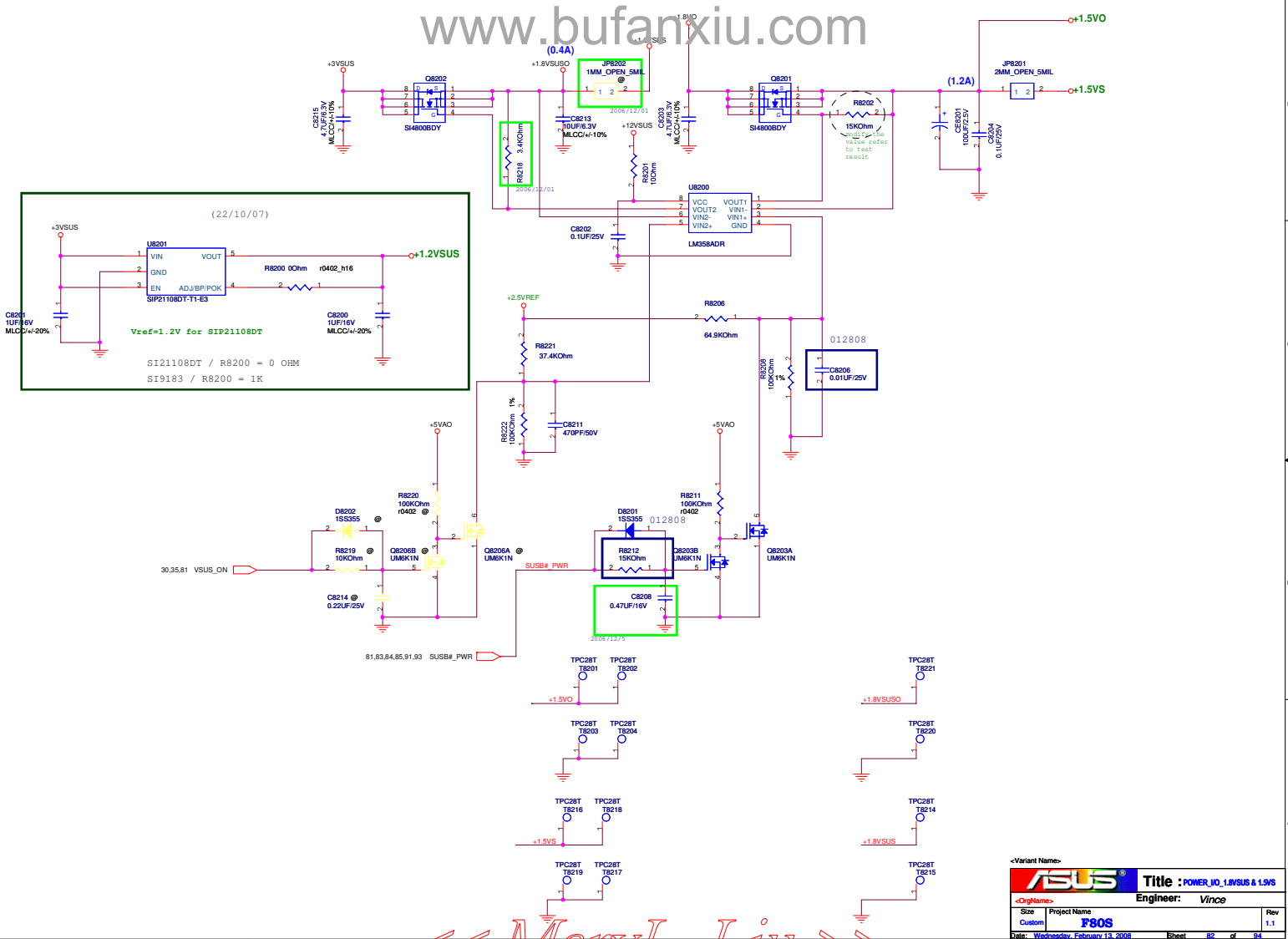
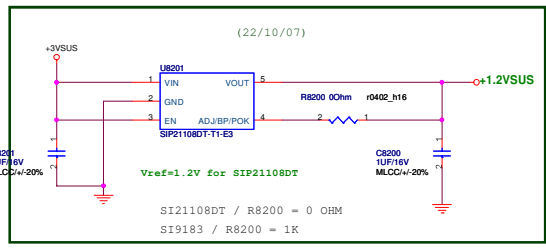
ASUS		Title : POWER_VCORE	
ASUSTEK COMPUTER INC. NB		Engineer: Vince	
Size	Project Name	Rev	
Custom	F80S	1.1	
Date: Wednesday, February 13, 2008		Sheet 80 of 84	

<< MaryL Liu >>



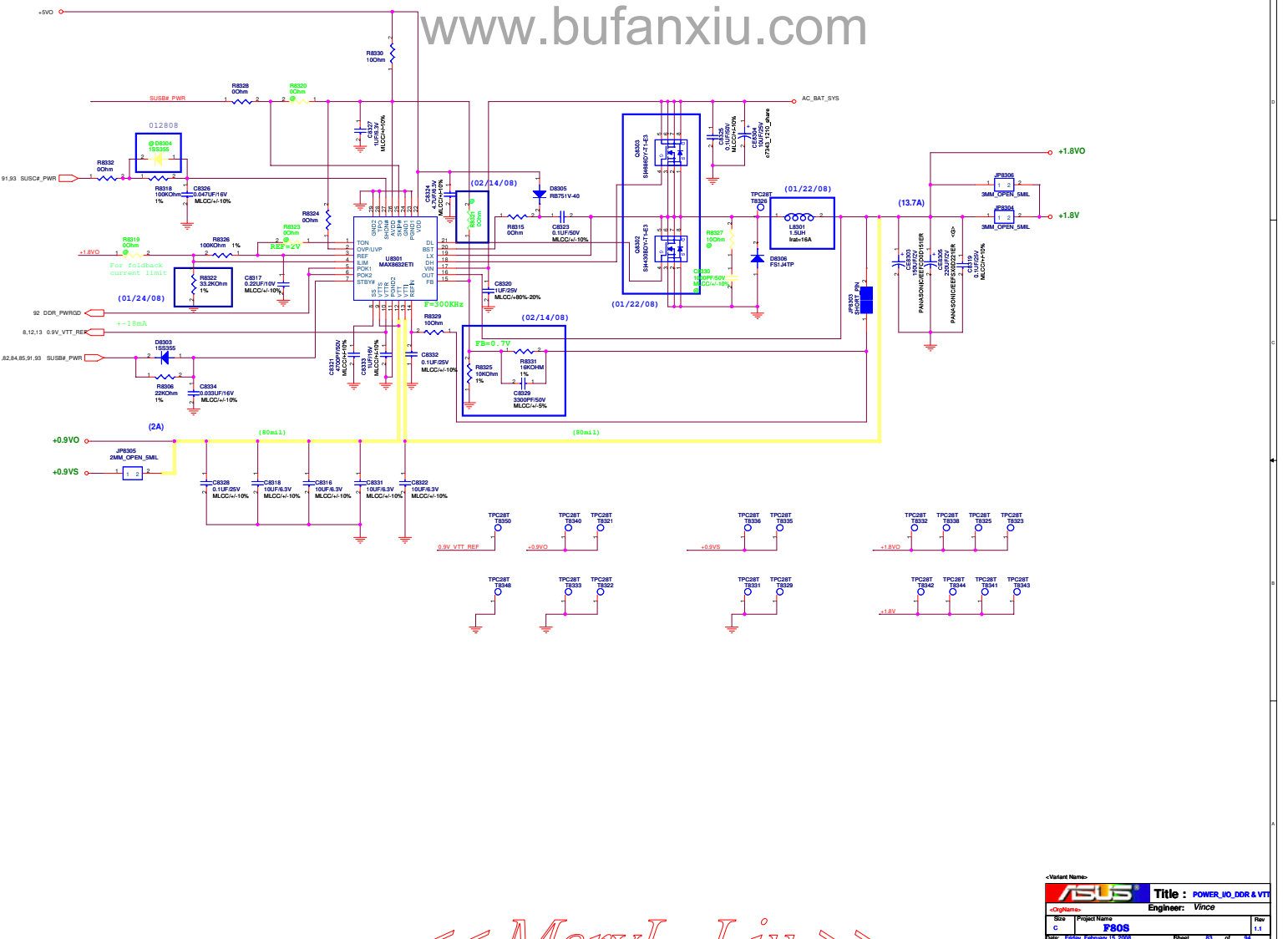
ASUS		Title: POWER_SYSTEM
DocName:	Project Name:	Engineer: Vince
Size:	Project Name:	Rev: 1.1
Custom:	F80S	
Date: Wednesday, February 13, 2008	Sheet: 81	of 84

<< MaryL_Liu >>



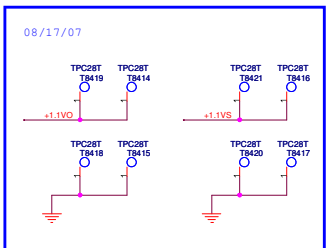
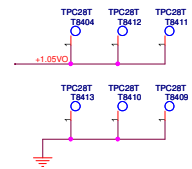
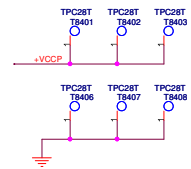
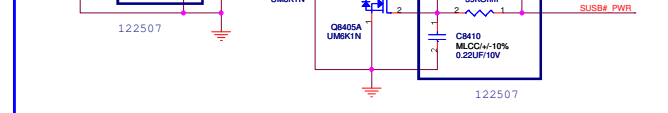
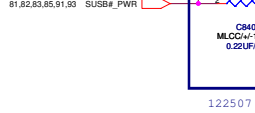
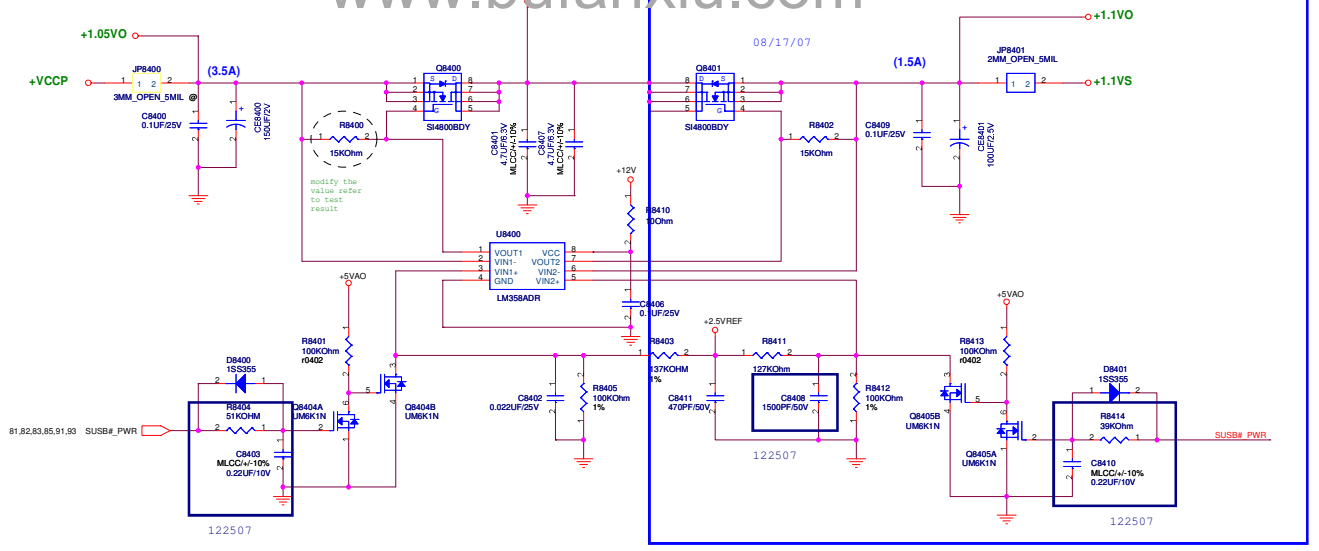
-Variant Name-		ASUS Title : POWER_IO_1.8VSUS & 1.5VS	
<OrigName>	Project Name	Engineer:	Vince
Size	Custom	Rev	1.1
Date:	Wednesday, February 13, 2008	Sheet	82 of 84

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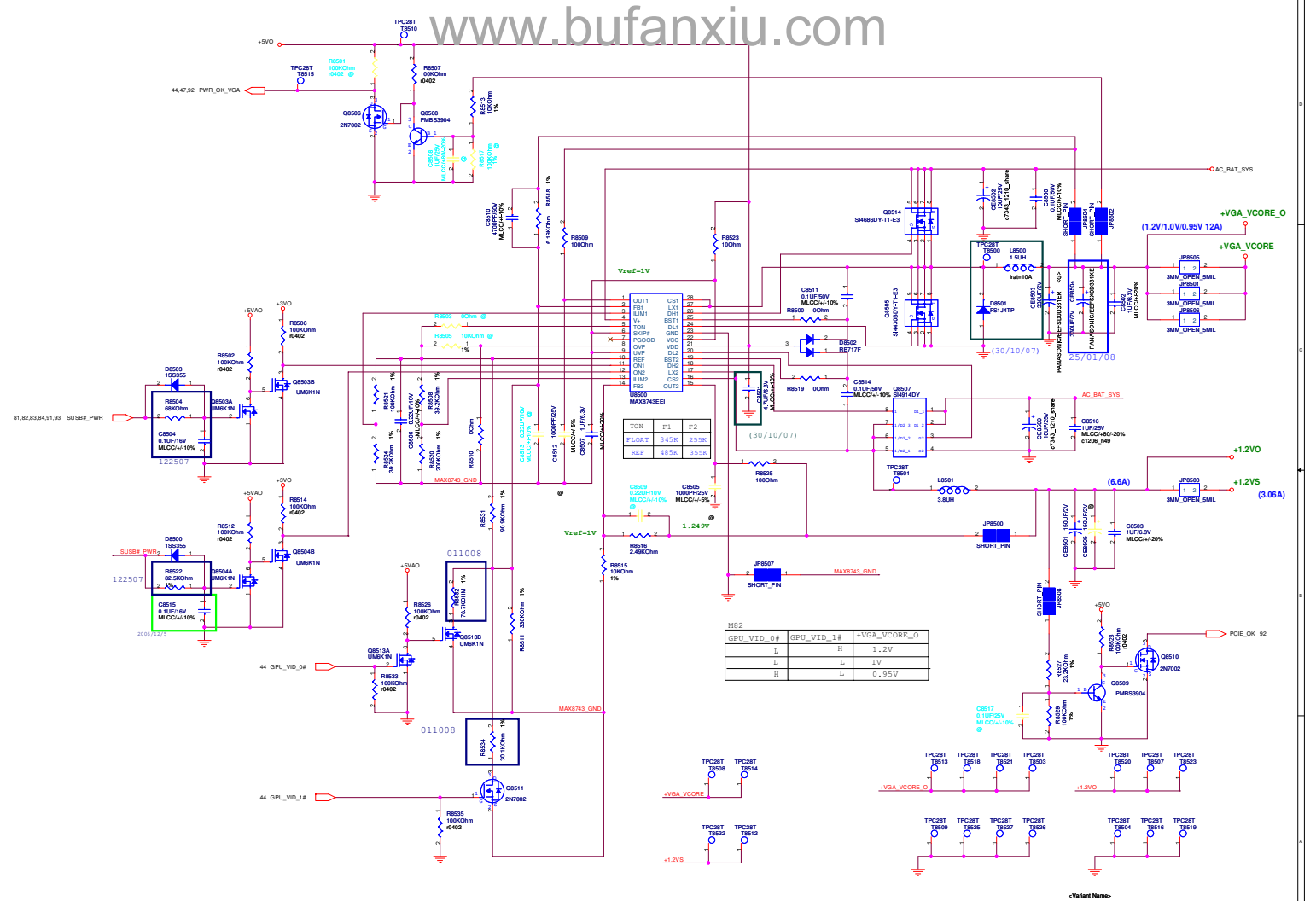
ASUS		Title : POWER_M0_D0R & VTT	
ASUS		Engineer: Vince	
Ver	Project Name	Rev	
C	F80S	1.1	
Date: Friday, February 15, 2008		Sheet	83 of 84



<-Variant Name>


ASUS		Title : POWER_IQ_VCCP & 1.1VS	
<OrigName>		Engineer: vince	
Site	Project Name		Rev
Custom	F80S		1.1
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ASUS Title: POWER_VGA_CORE & RM
 Engineer: Vince
 Project Name: F80S
 Date: Wednesday, February 18, 2009

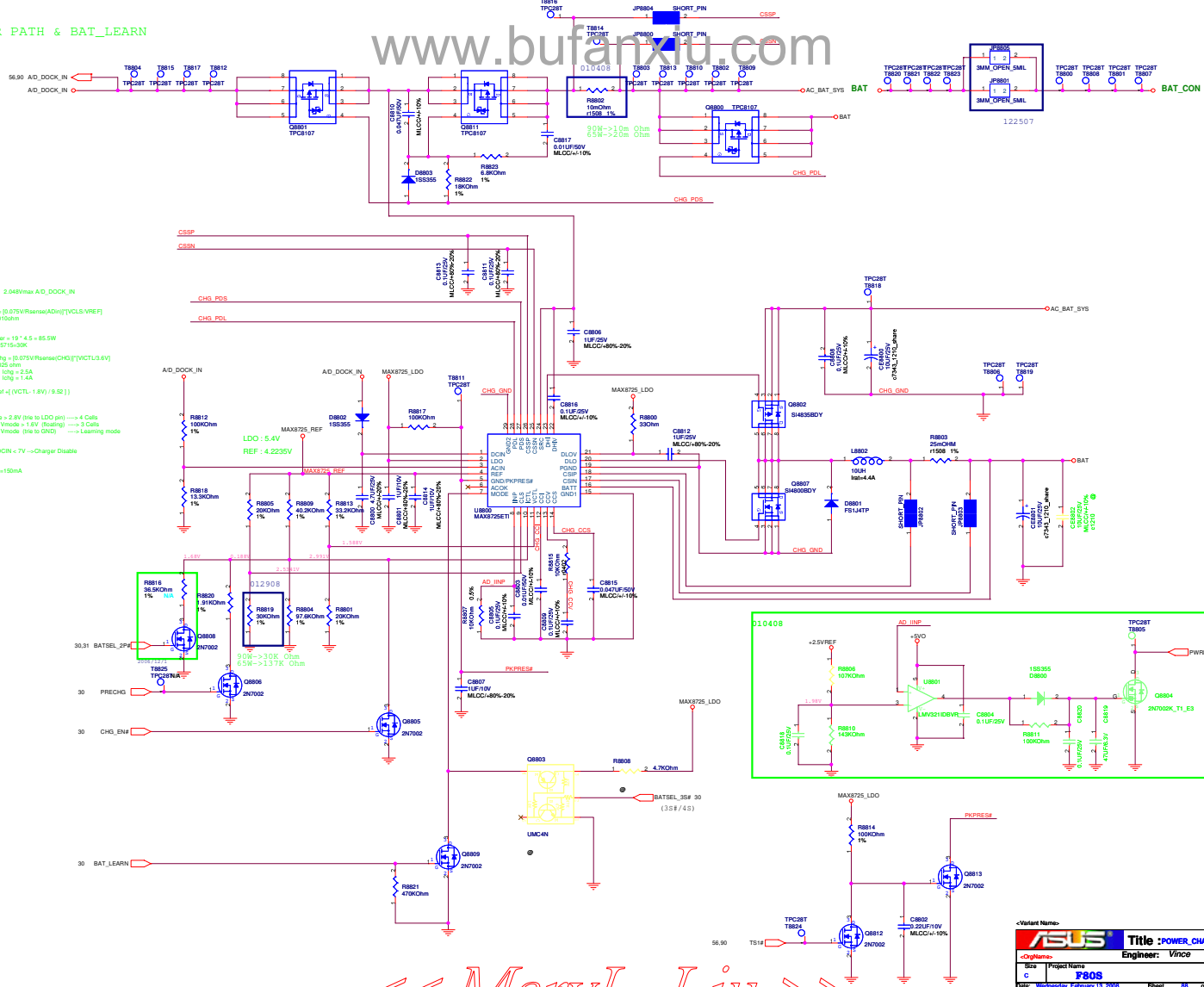
<< MaryL_Liu >>

<Variant Name>		
		Title :N/A
<OrgName>		Engineer: Vince
Size B	Project Name F80S	Rev 1.1
Date: Wednesday, January 30, 2008		Sheet 86 of 94

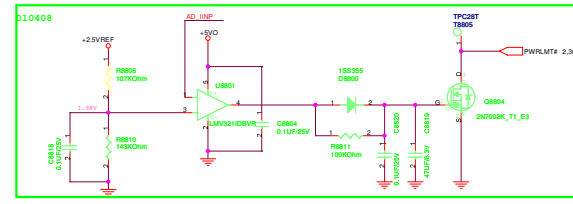
<< MaryL_Liu >>

<Variant Name>		
		Title : N/A
<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 87 of 84

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VC_IN Threshold > 0.049Vmax AD_DOCK_IN
 > 17.44V active
 Adapter In(max) = (0.075V/Rsense/Adm)[VCL5 VREF]
 Resense/Adm=0.000m
 VCL5=2.534V
 => In(max)=4.5A
 => Constant Power = 13.145 + 85.5W
 => RST to 200mA/500mA/1500mA
 Charge Current Ichg = (0.075V/Rsense/CHG)[VCTL3.6V]
 Resense/CHG=0.002m
 VCTL=3V => Ichg = 2.5A
 VCTL=1.588V => Ichg = 1.4A
 Vbat = Gd1 + (Vbat - (VCTL - 1.5V) / 9.52)
 VCTL = 1.588V
 => Vbat = 4.2V
 Mode pin: Vinode > 2.8V (96 to LDO pin) => 4 Cells
 2.0 ~ Vinode > 1.8V (Booting) => 3 Cells
 G.A ~ Vinode (96 to GND) => Learning mode
 VICT < 0.8V or DCIN = 7V => Charger Disable
 Precharge current=150mA



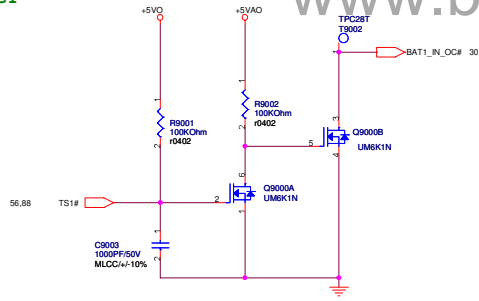
ASUS		Title: POWER CHARGER
Project Name	Engineer: Vince	
Rev	Rev	
C	F80S	1.1
Date: Wednesday, February 18, 2009	Sheet: 85	of 84

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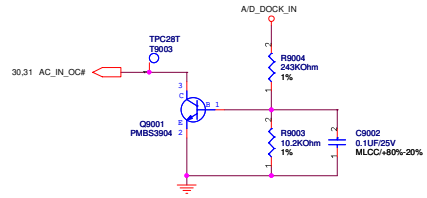
<Variant Name>		
		Title : N/A
<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, January 30, 2008		Sheet 89 of 94

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BATTERY IN DETECT



ADAPTER IN DETECT



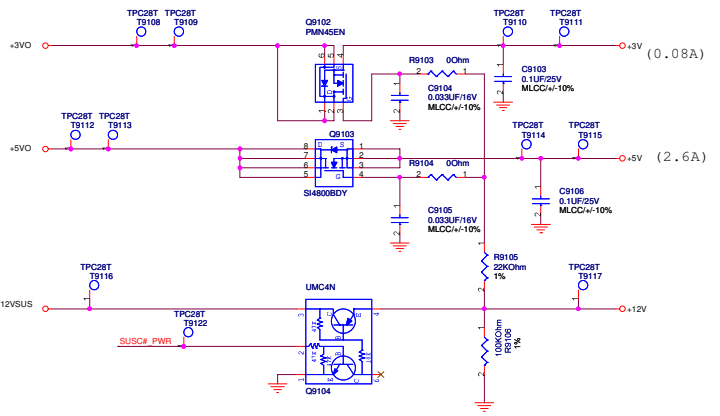
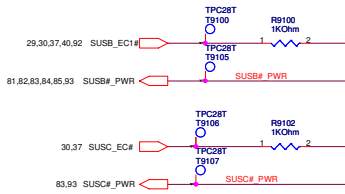
+2.5VREF



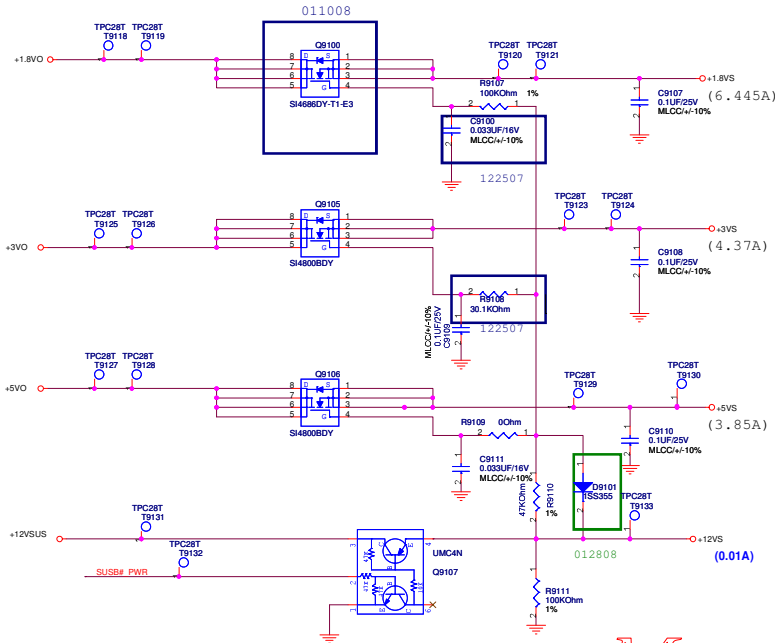
<Variant Name>

		Title : POWER_DETECT	
<OrigName>		Engineer: Vince	
Size	Project Name		Rev
Custom	F80S		1.1
Date: Wednesday, February 13, 2008		Sheet	90 of 94

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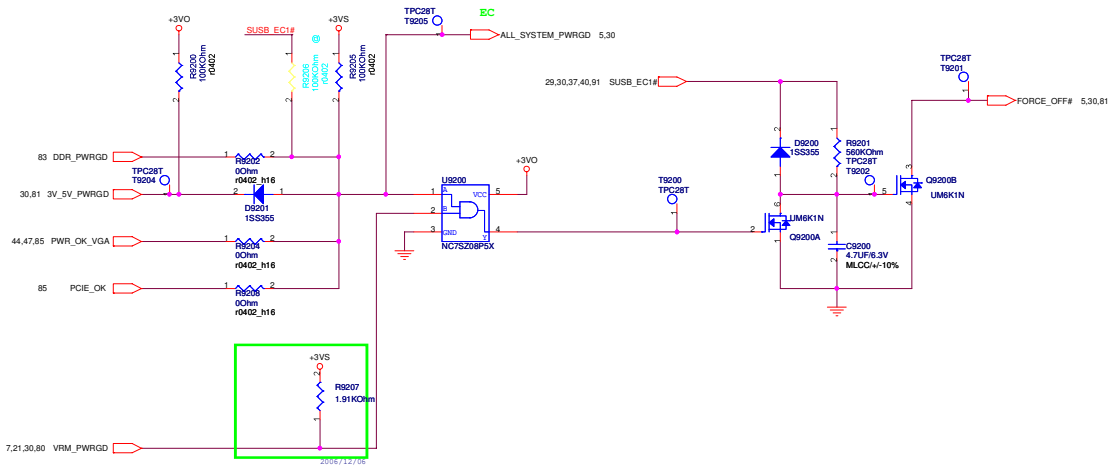
SUSB#_PWR POWER



ASUS		Title : POWER_LOAD SWITCH	
Engineer: Vince		Rev	
Size	Project Name	Custom	F80S
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POWER GOOD DETECTOR

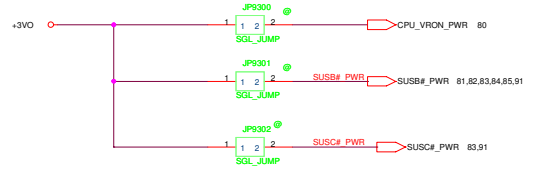


<Variant Name>		
ASUS		Title : POWER_PROTECT
<OrigName>		Engineer: Vince
Site	Project Name	Rev
Custom	F80S	1.1
Date: Wednesday, February 13, 2008	Sheet	82 of 84

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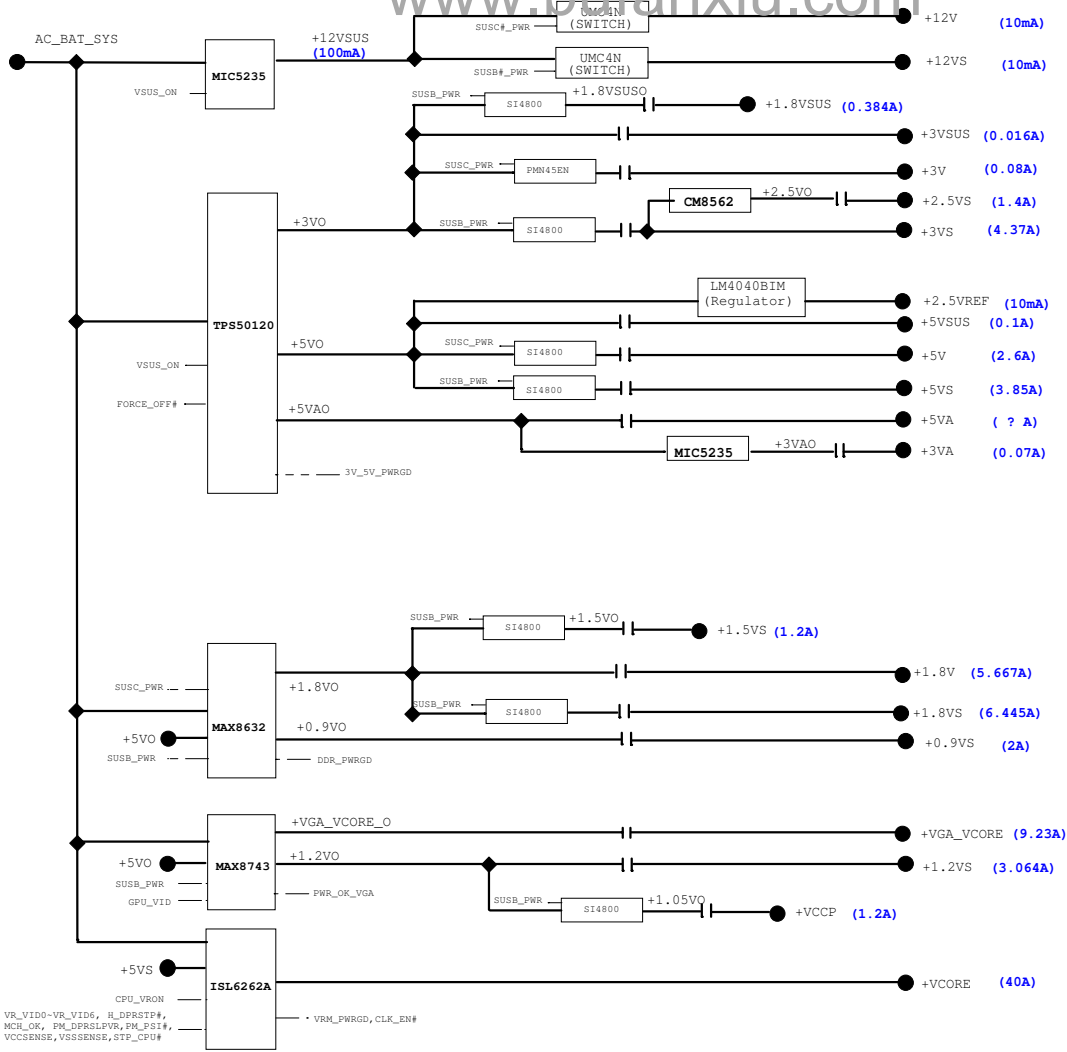
AC_BAT_SYS	AC_BAT_SYS	17,80,81,83,85,88
+3VA	+3VA	17,21,30,37,81
+5VA	+5VA	5,81
+5VD	+5VD	81,83,85,88,90,91
+3VD	+3VD	81,85,91,92
+3VSUS	+3VSUS	8,17,19,20,21,22,23,24,26,30,34,35,36,81,82
+5VSUS	+5VSUS	34,81
+3V	+3V	19,27,29,31,36,37,38,40,91
+3VS	+3VS	2,4,5,7,12,13,16,17,18,19,20,21,22,23,25,29,30,32,33,34,37,40,44,80,91,92
+12VSUS	+12VSUS	81,82,91
+12V	+12V	26,27,33,37,84,91
+12VS	+12VS	17,18,37,44,91
+5V	+5V	17,33,37,91
+5VS	+5VS	5,12,16,18,25,26,29,30,32,34,37,38,51,80,91
+1.8VD	+1.8VD	82,83,91
+1.8VSUS	+1.8VSUS	10,21,22,23,82
+1.8V	+1.8V	8,10,12,13,15,37,83
+1.8VS	+1.8VS	6,7,8,10,12,14,20,21,22,23,37,43,44,45,47,51,91
+1.5V	+1.5V	3,19,25,29,37,51,82
+VCCP	+VCCP	2,4,5,6,10,21,23,37,43,84
+0.9VS	+0.9VS	15,37,83
BAT	BAT	88
+2.5VREF	+2.5VREF	62,84,88,90
+VCORE	+VCORE	3,37,80
+VGA_VCORE	+VGA_VCORE	37,43,47,51,85
+1.2VD	+1.2VD	84,85
+1.2VS	+1.2VS	9,10,37,85
BAT_CON	BAT_CON	56,88

FOR POWER TEST



-Variant Name-		Title : POWER_SIGNAL	
ASUS		Engineer: Vince	
-CmpName-	Size	Project Name	Rev
	Custom	F80S	1.1
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