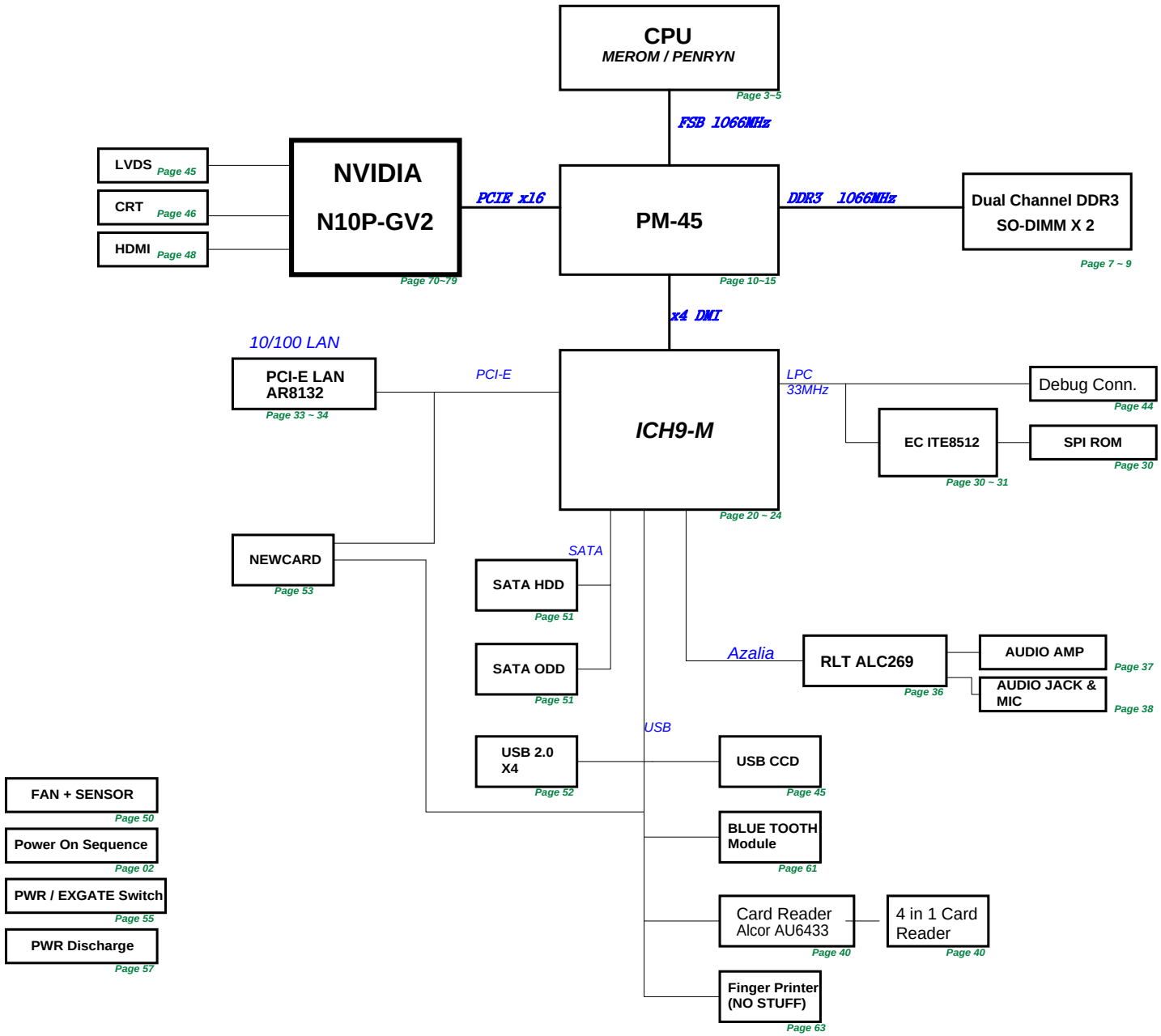
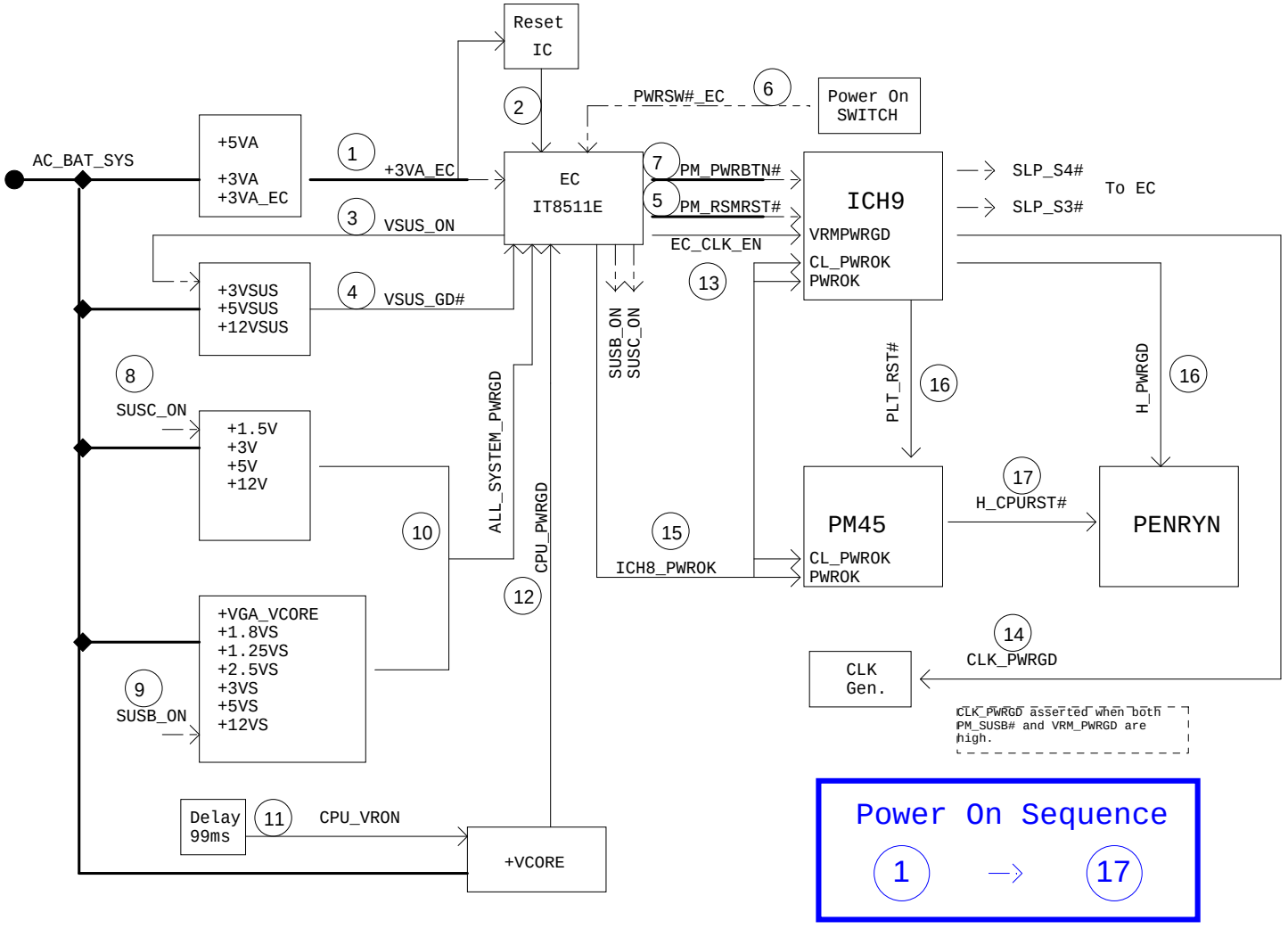
F83Vf MonteVina BLOCK DIAGRAM

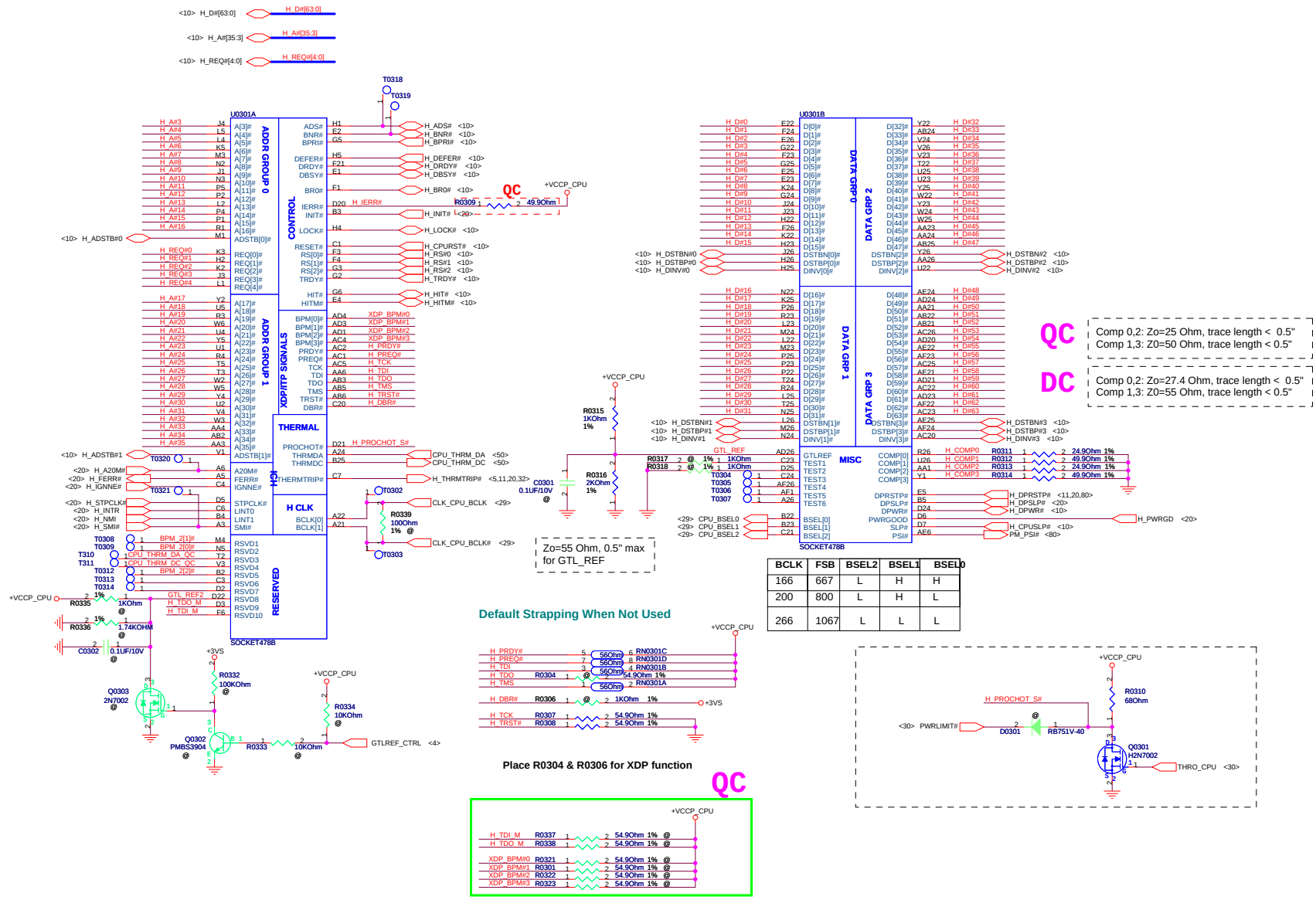


Power

PEGATRON	Title :	Block Diagram
PEGATRON COMPUTER INC	Engineer:	Zack Kuo
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 1 of 100	

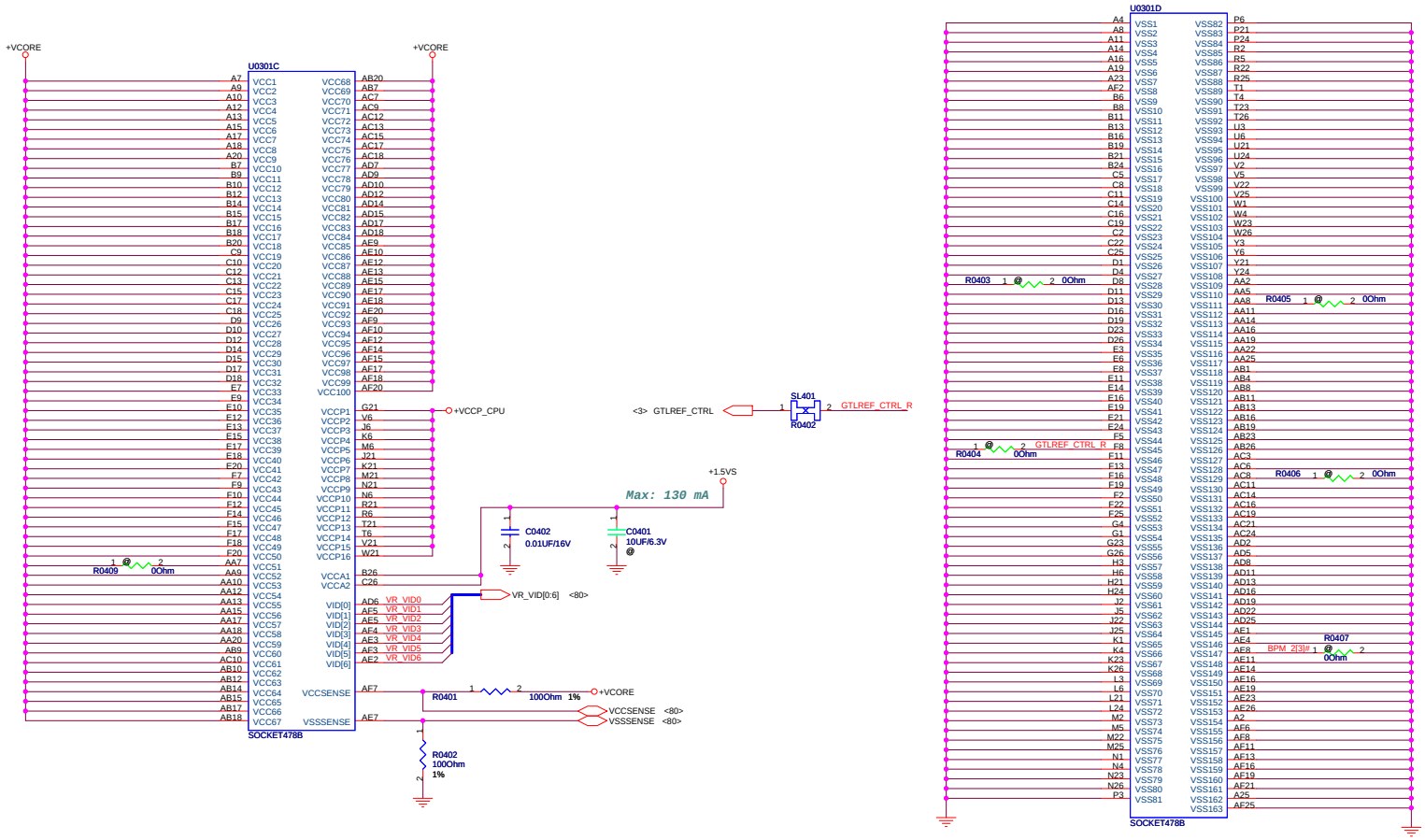


PEGATRON	Title : Power Sequence		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 2 of 100		

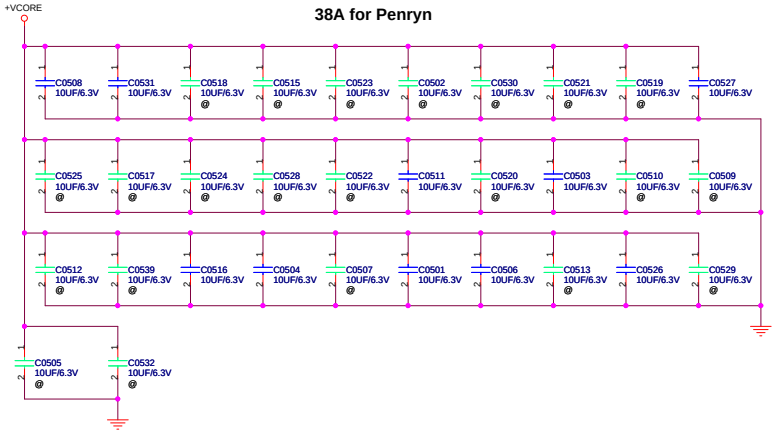


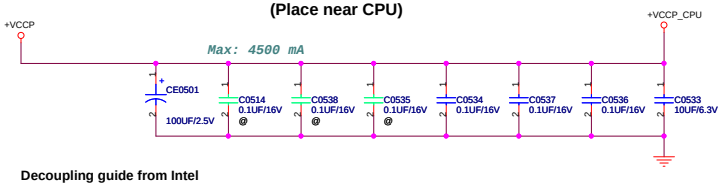
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

PEGATRON	Title :	Penryn(1)
PEGATRON COMPUTER INC	Engineer:	Zack Kuo
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 3 of 100	



PEGATRON	Title :	Penryn(2)	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 4 of 100		

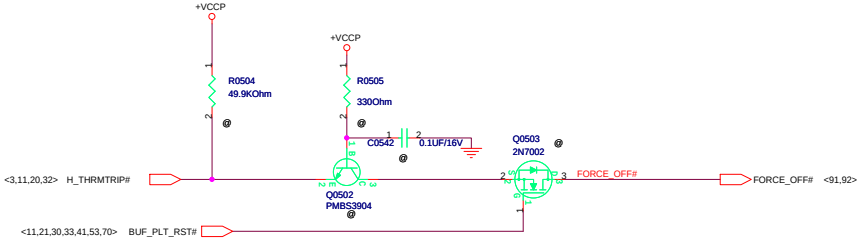




Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

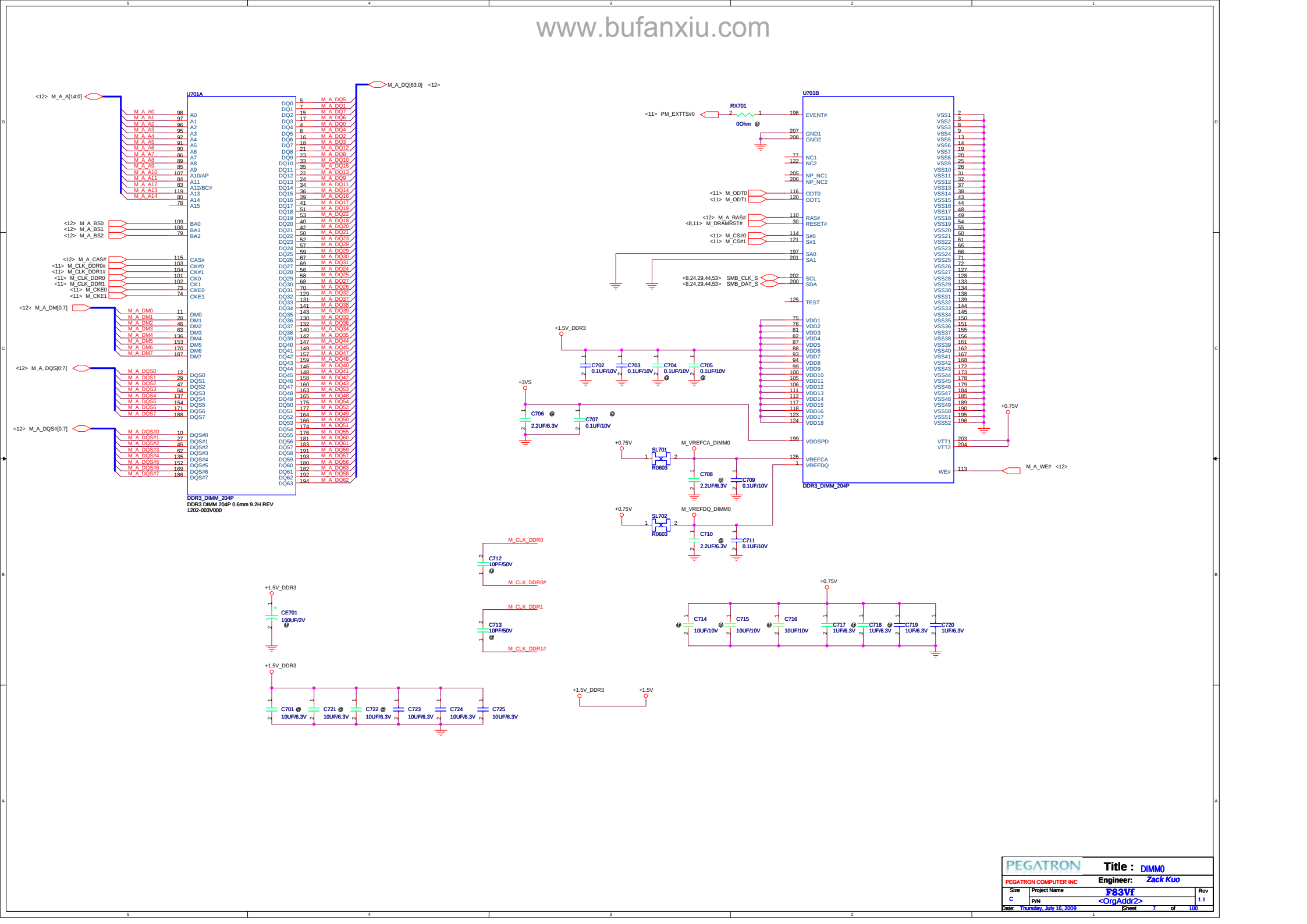
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F83Vf: 10UF*12*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *3*
V1V: ?



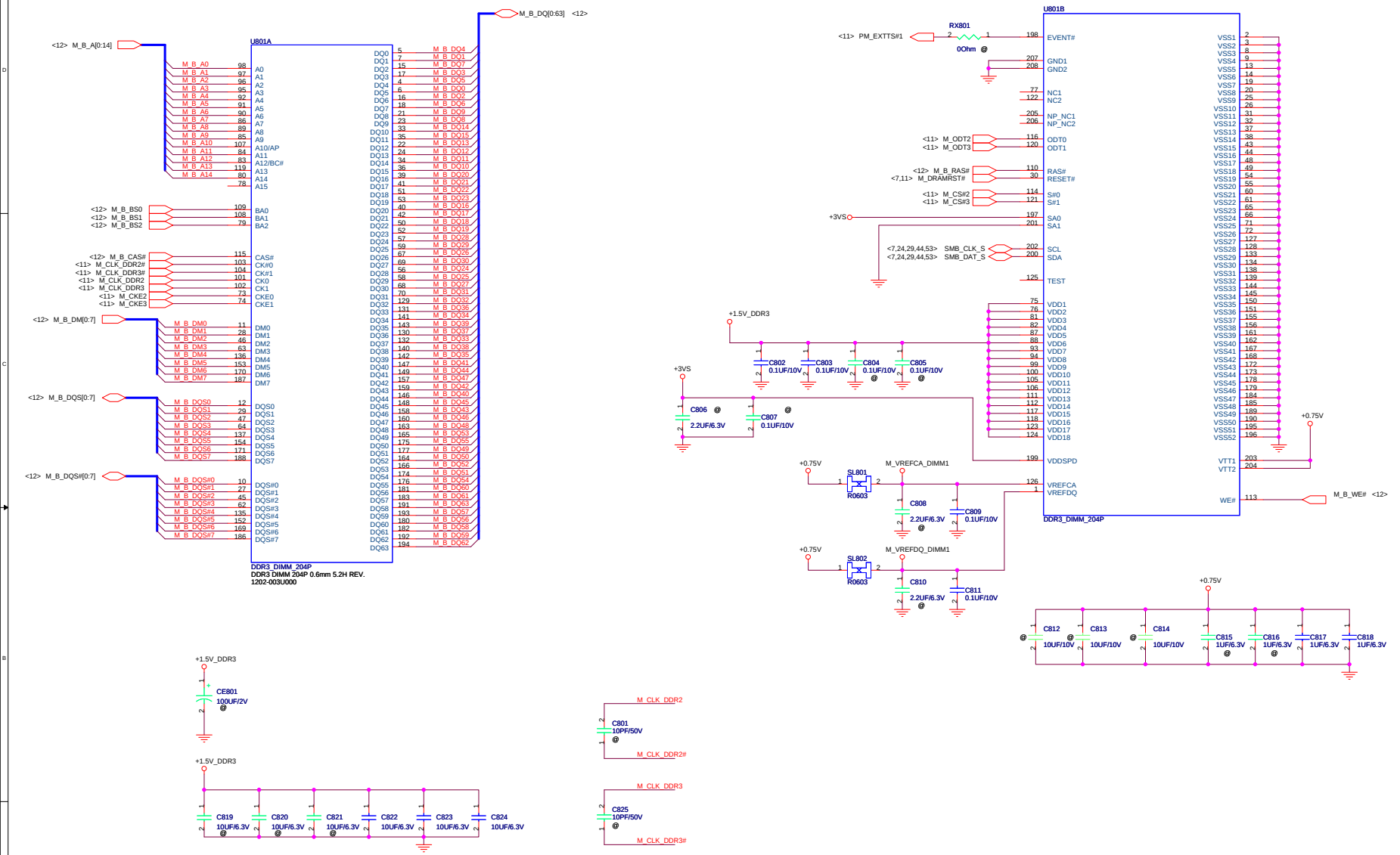
Thermal Trip signal (From CPU to ICH-9M and sequence)

PEGATRON	Title :	CPU Decouple	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 5 of 100		

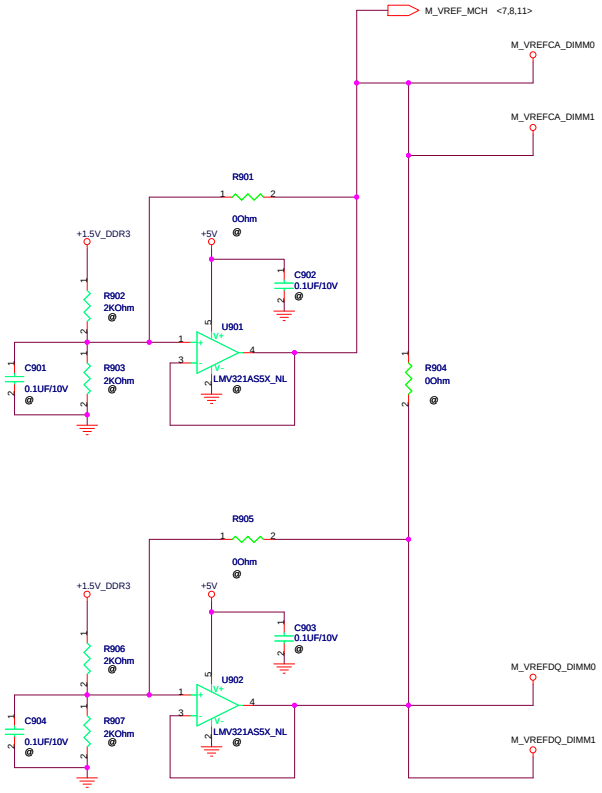
PEGATRON	Title : CPU ***		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 6 of 100		



Title :	DIMM0
Engineer:	Zack Kuo
PEGATRON COMPUTER INC	
Size: C	Project Name: F83Vf
P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 7 of 100



PEGATRON	Title : DIMM1		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 8 of 100		



PEGATRON

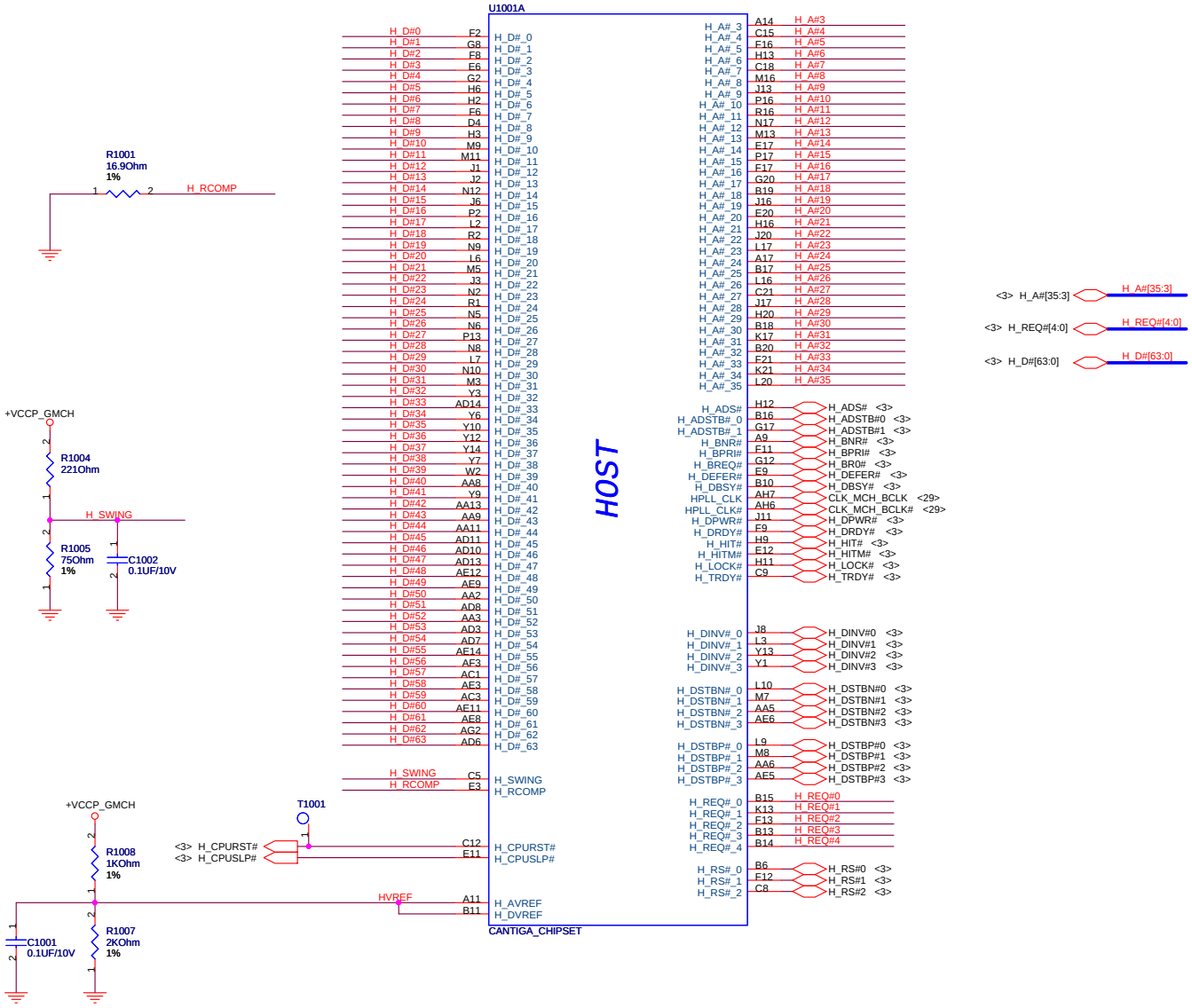
PEGATRON COMPUTER INC

Title : DIMM_TERM

Engineer: Zack Kuo

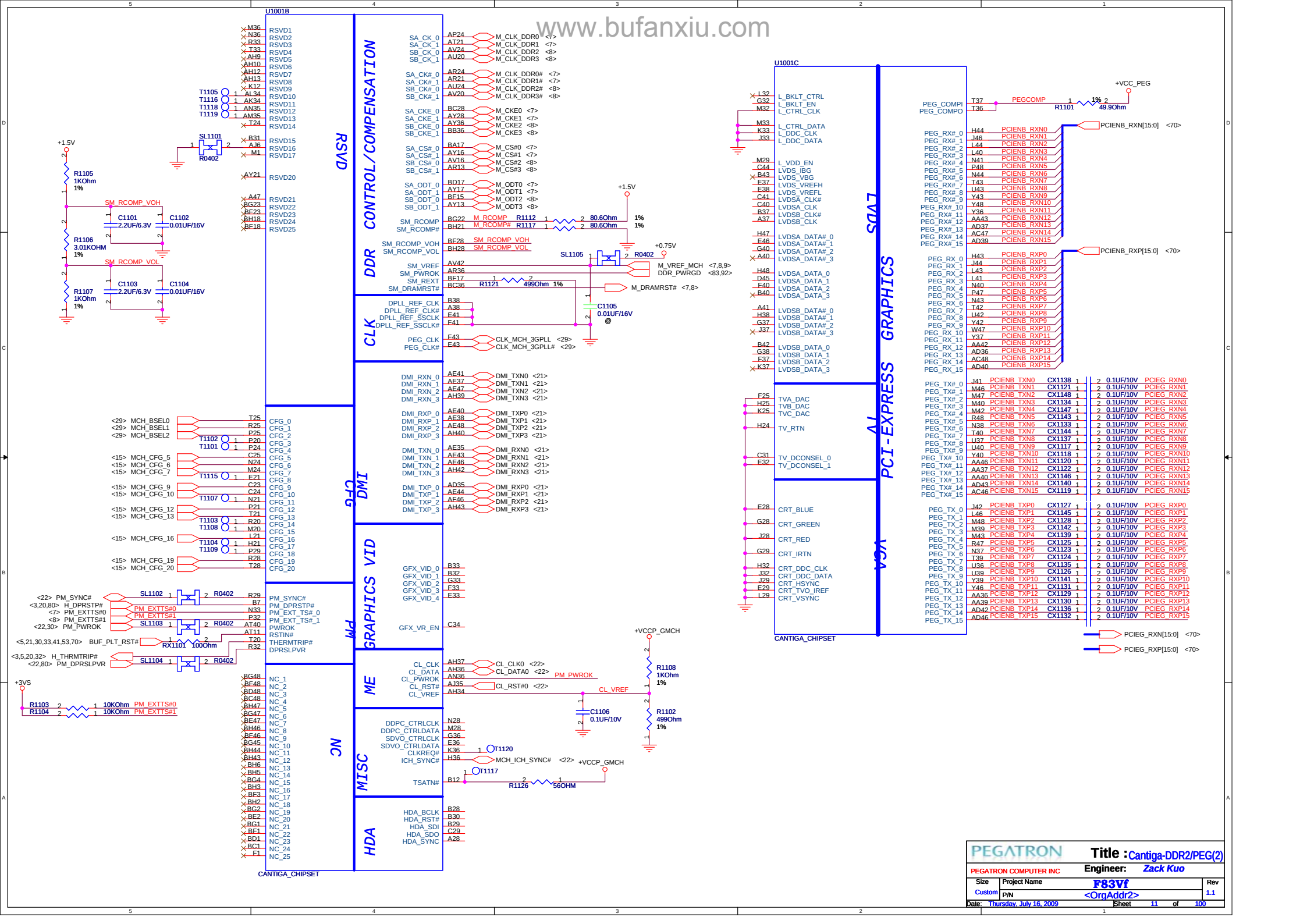
Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

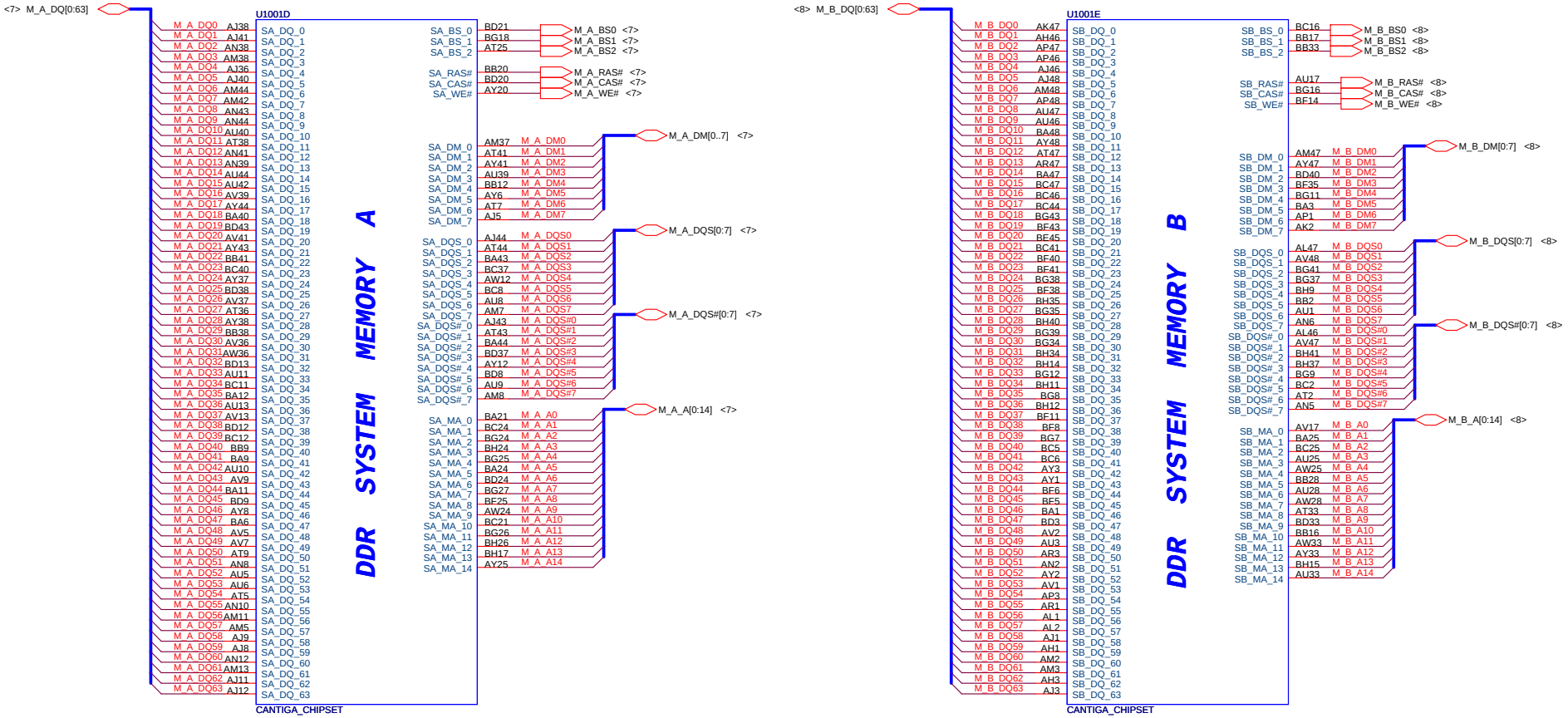
Date: Thursday, July 16, 2009 Sheet 9 of 100



Cap 0.1uF within 100 mils from GMCH

PEGATRON	Title : Cantiga -- CPU (1)		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: Custom	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 10 of 100		





PEGATRON

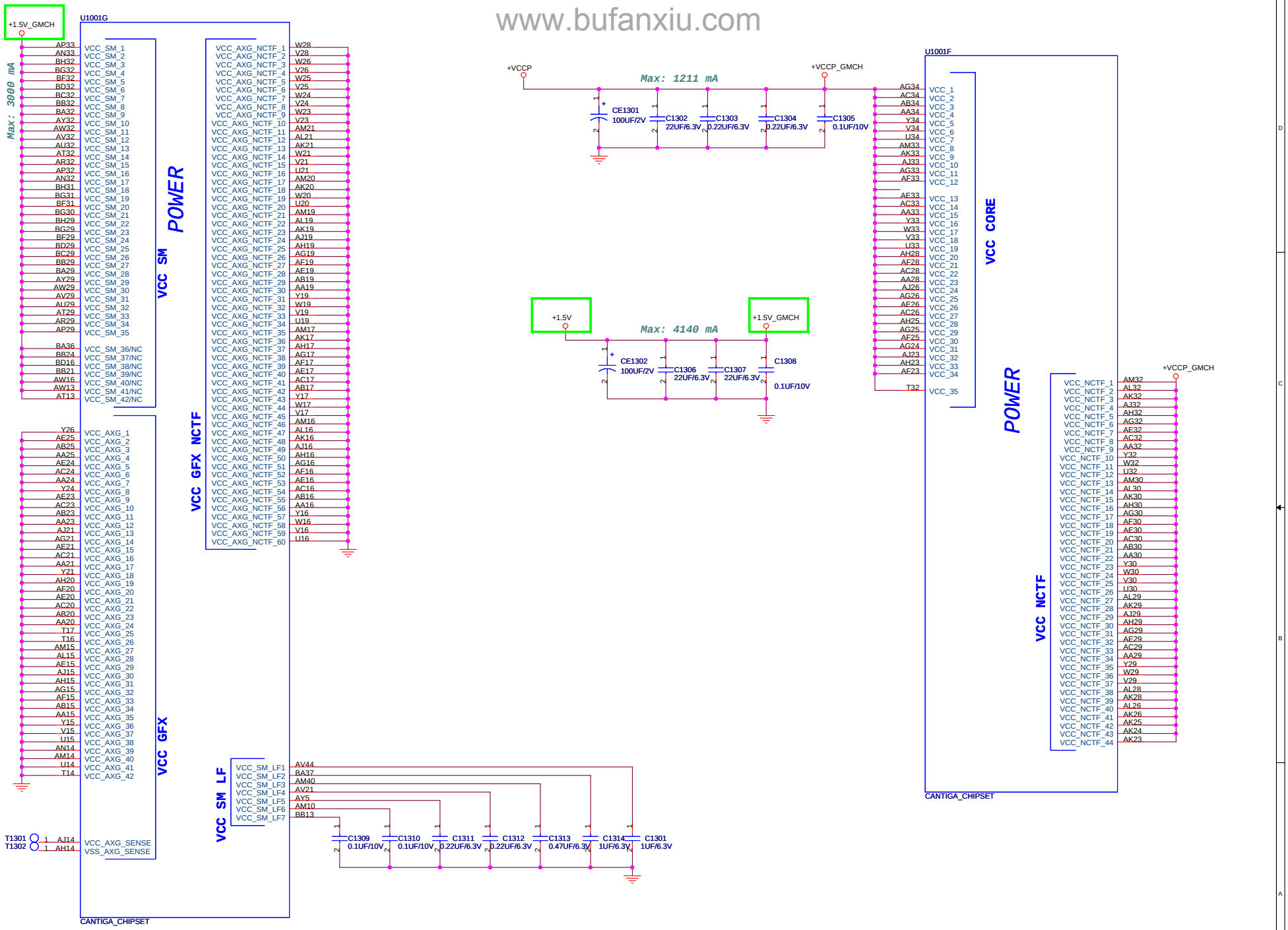
Title : Cantiga--DDR2 bus (3)

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 12 of 100



PEGATRON

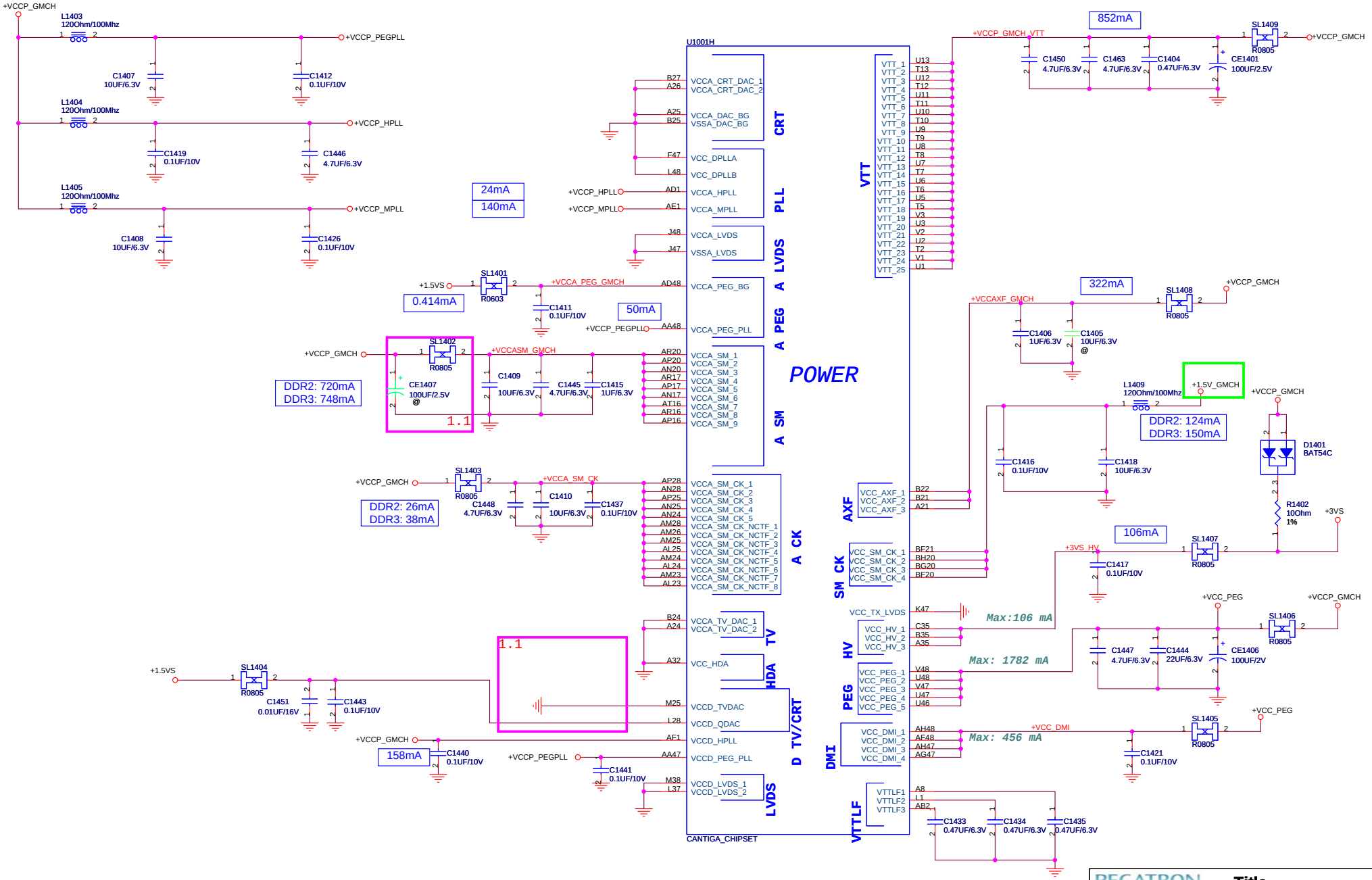
Title : Cantiga--POWER (4)

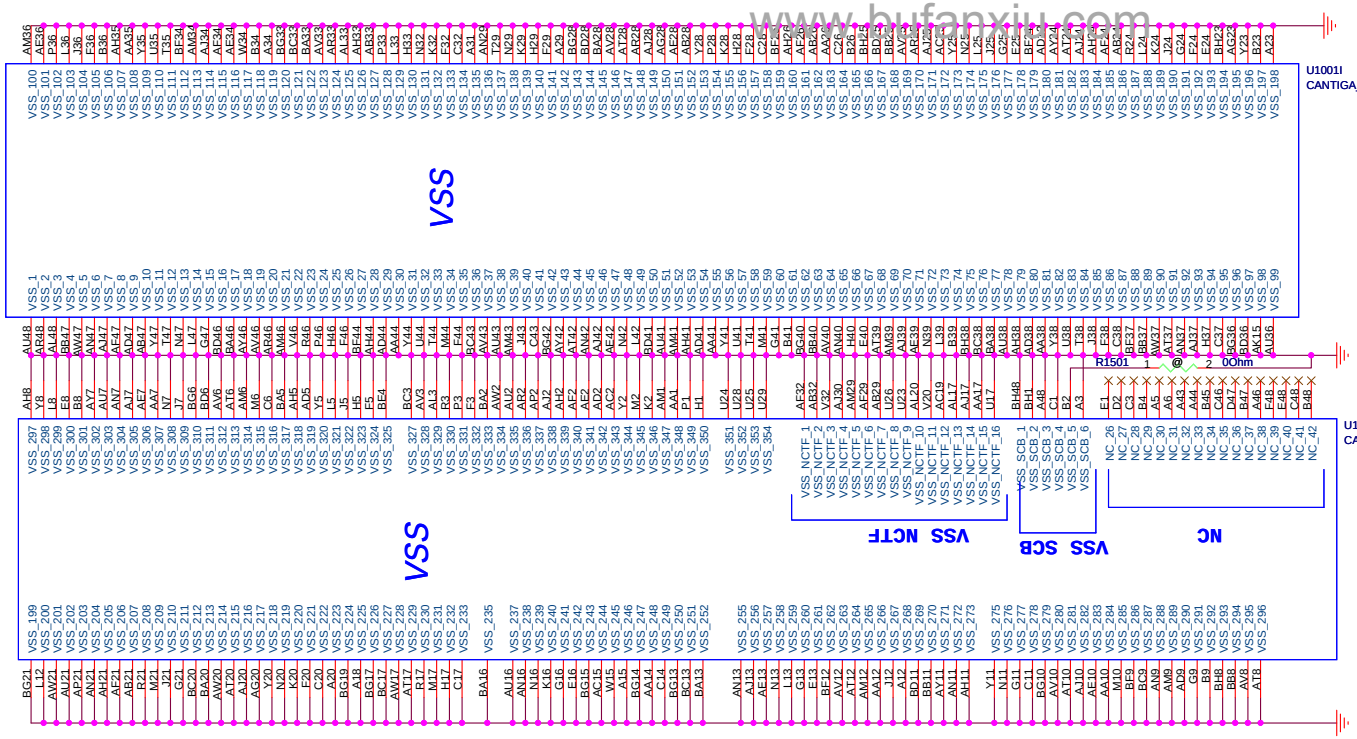
PEGATRON COMPUTER INC

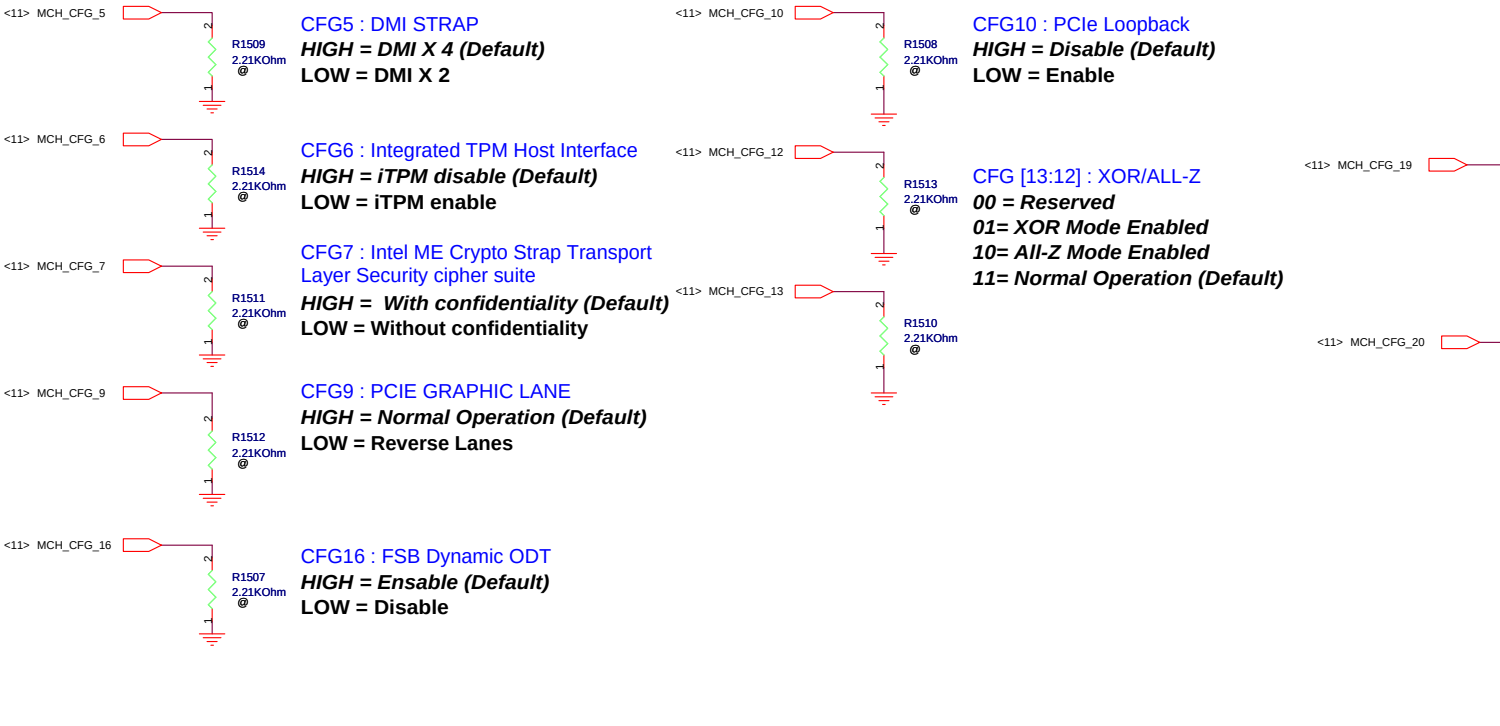
Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 13 of 100







PEGATRON	Title : Cantiga-GND	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: Custom	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 15 of 100	

PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: Custom	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 16 of 100		

Main Board

PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: Custom	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 17 of 100		

Main Board

PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: Custom	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 18 of 100		

PEGATRON	Title :		
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 19 of 100		

1.1

Place Near the Open Door

VccLAN1_05 & VccCL1_05 Internal VR	VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
High = Enable (Default)	High = Enable (Default)
Low = Disable	Low = Disable

U2001A

ICH9M

SATA	HDD
SATA1	HDD 1
SATA2	ODD
SATA4	HDD 2
SATA5	ESATA

[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

00 = Reserved

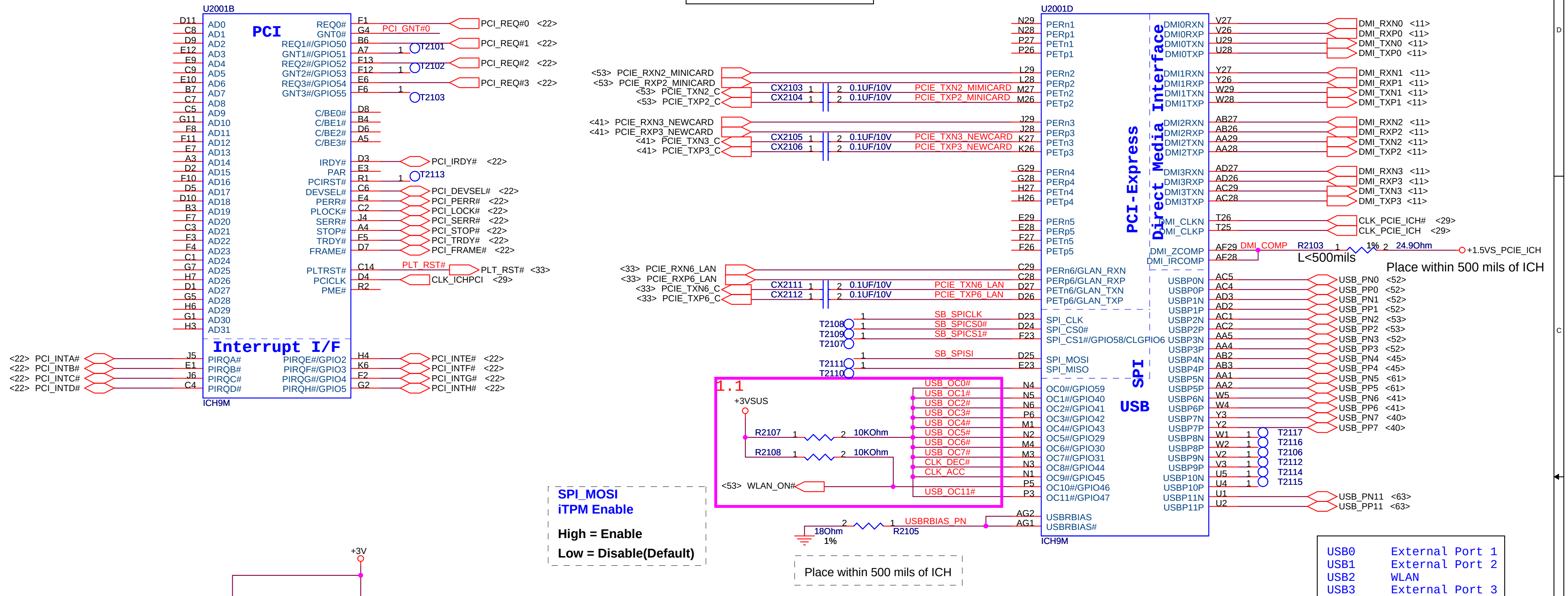
01= Enter XOR Chain

10= Normal Operation (Default)

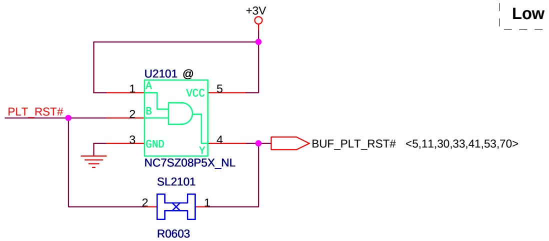
11= Set PCIe Port Config Bit 1

PEGATRON	Title : SB-ICH9M(1)		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: Custom	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 20 of 100		

PCIE1	NC
PCIE2	MiniCard
PCIE3	NewCard
PCIE4	NC
PCIE5	NC
PCIE6	LAN



U2001B
PCI
AD0 … AD31
REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
C/BE0# C/BE1# C/BE2# C/BE3#
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PLTRST# PCICLK PME#
PCI_GNT#0
PCI_REQ#0 <22>
PCI_REQ#1 <22>
PCI_REQ#2 <22>
PCI_REQ#3 <22>
T2101 T2102 T2103 T2113
PCI_IRDY# <22>
PCI_DEVSEL# <22>
PCI_PERR# <22>
PCI_LOCK# <22>
PCI_SERR# <22>
PCI_STOP# <22>
PCI_TRDY# <22>
PCI_FRAME# <22>
PLT_RST#
PLT_RST# <33>
CLK_ICHPCI <29>
Interrupt I/F
PIRQA# PIRQB# PIRQC# PIRQD# PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
<22> PCI_INTA#
<22> PCI_INTB#
<22> PCI_INTC#
<22> PCI_INTD#
PCI_INTE# <22>
PCI_INTF# <22>
PCI_INTG# <22>
PCI_INTH# <22>
ICH9M
<53> PCIE_RXN2_MINICARD
<53> PCIE_RXP2_MINICARD
<53> PCIE_TXN2_C
<53> PCIE_TXP2_C
CX2103 0.1UF/10V PCIE_TXN2_MIMICARD
CX2104 0.1UF/10V PCIE_TXP2_MINICARD
<41> PCIE_RXN3_NEWCARD
<41> PCIE_RXP3_NEWCARD
<41> PCIE_TXN3_C
<41> PCIE_TXP3_C
CX2105 0.1UF/10V PCIE_TXN3_NEWCARD
CX2106 0.1UF/10V PCIE_TXP3_NEWCARD
<33> PCIE_RXN6_LAN
<33> PCIE_RXP6_LAN
<33> PCIE_TXN6_C
<33> PCIE_TXP6_C
CX2111 0.1UF/10V PCIE_TXN6_LAN
CX2112 0.1UF/10V PCIE_TXP6_LAN
U2001D
PERn1 PERp1 PETn1 PETp1 … PERn5 PERp5 PETn5 PETp5
PERn6/GLAN_RXN PERp6/GLAN_RXP PETn6/GLAN_TXN PETp6/GLAN_TXP
PCI-Express
Direct Media Interface
DMI0RXN DMI0RXP DMI0TXN DMI0TXP … DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP DMI_ZCOMP DMI_IRCOMP
DMI_RXN0 <11> DMI_RXP0 <11> DMI_TXN0 <11> DMI_TXP0 <11>
DMI_RXN1 <11> DMI_RXP1 <11> DMI_TXN1 <11> DMI_TXP1 <11>
DMI_RXN2 <11> DMI_RXP2 <11> DMI_TXN2 <11> DMI_TXP2 <11>
DMI_RXN3 <11> DMI_RXP3 <11> DMI_TXN3 <11> DMI_TXP3 <11>
CLK_PCIE_ICH# <29>
CLK_PCIE_ICH <29>
DMI_COMP R2103 1% 24.9Ohm +1.5VS_PCIE_ICH
L<500mils
Place within 500 mils of ICH
SPI
SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO
SB_SPICLK SB_SPICS0# SB_SPICS1# SB_SPISI
T2108 T2109 T2107 T2111 T2110
USB
USBP0N USBP0P … USBP11N USBP11P
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47
USBRBIAS USBRBIAS#
1.1
+3VSUS
R2107 10KOhm
R2108 10KOhm
USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7# CLK_DEC# CLK_ACC USB_OC11#
<53> WLAN_ON#
USBRBIAS_PN 18Ohm 1% R2105
USB_PN0 <52> USB_PP0 <52> USB_PN1 <52> USB_PP1 <52>
USB_PN2 <53> USB_PP2 <53> USB_PN3 <52> USB_PP3 <52>
USB_PN4 <45> USB_PP4 <45> USB_PN5 <61> USB_PP5 <61>
USB_PN6 <41> USB_PP6 <41> USB_PN7 <40> USB_PP7 <40>
T2117 T2116 T2106 T2112 T2114 T2115
USB_PN11 <63> USB_PP11 <63>
ICH9M
SPI_MOSI
iTPM Enable
High = Enable
Low = Disable(Default)
Place within 500 mils of ICH

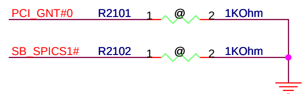


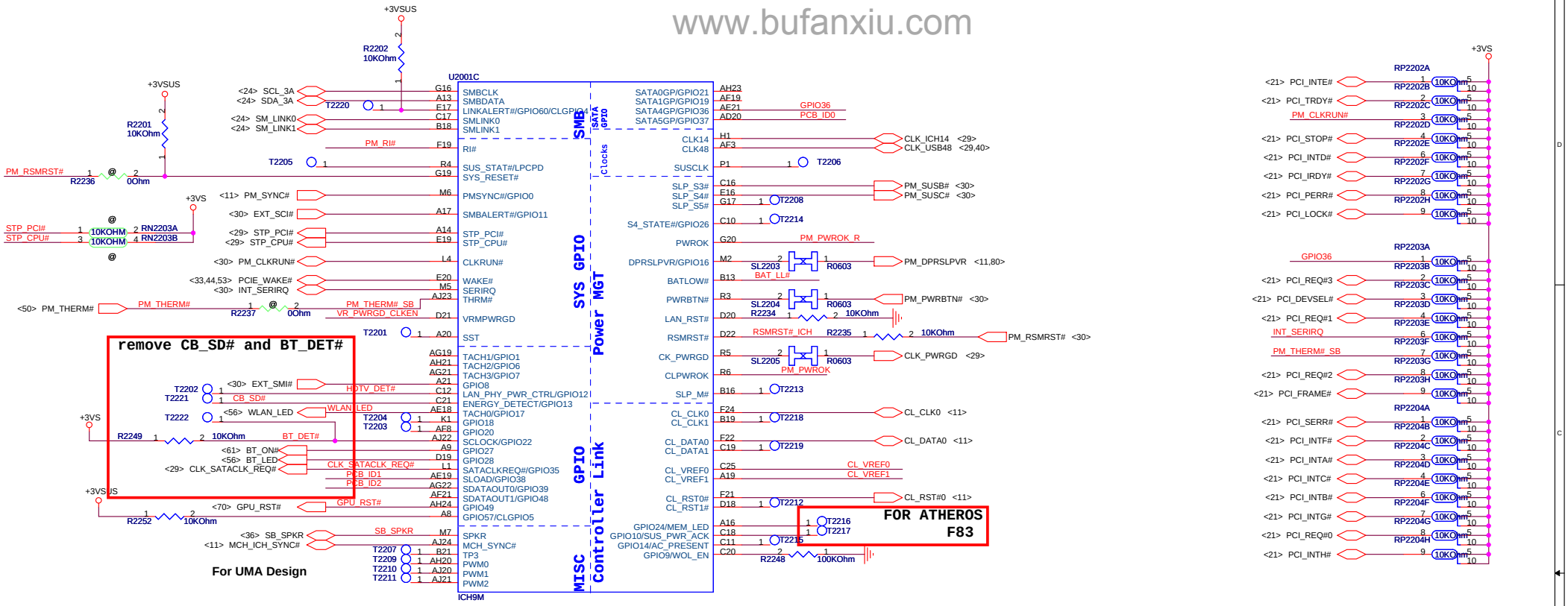
USB0	External Port 1
USB1	External Port 2
USB2	WLAN
USB3	External Port 3
USB4	CMOS Camera
USB5	BT
USB6	NEWCARD
USB7	CardReader
USB8	FREE
USB9	FREE
USB10	FREE
USB11	FingerPrinter

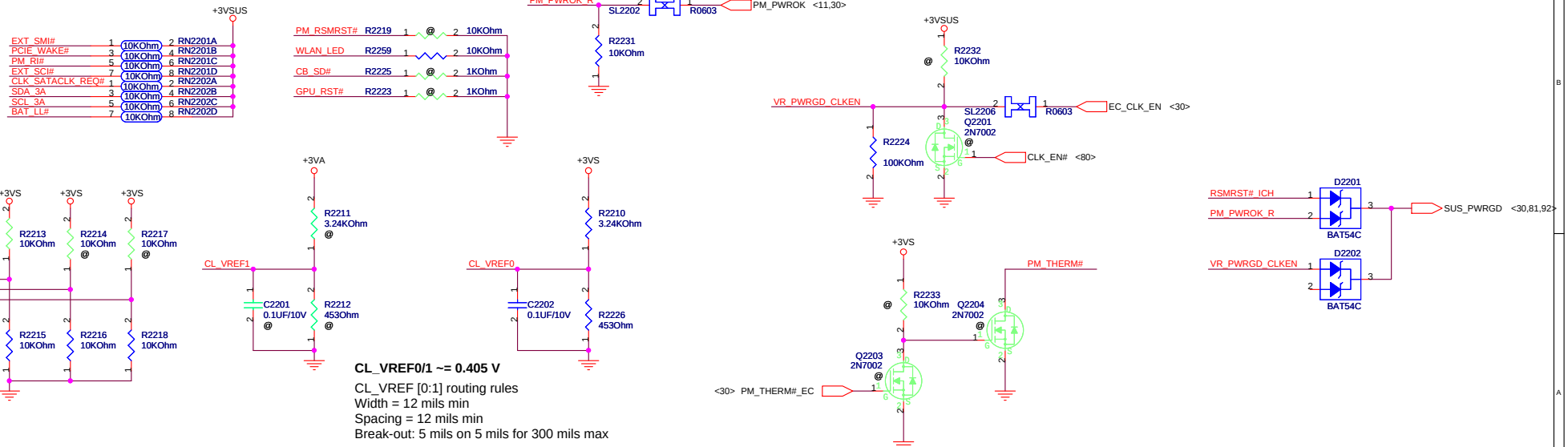
ICH9 Boot BIOS select

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)



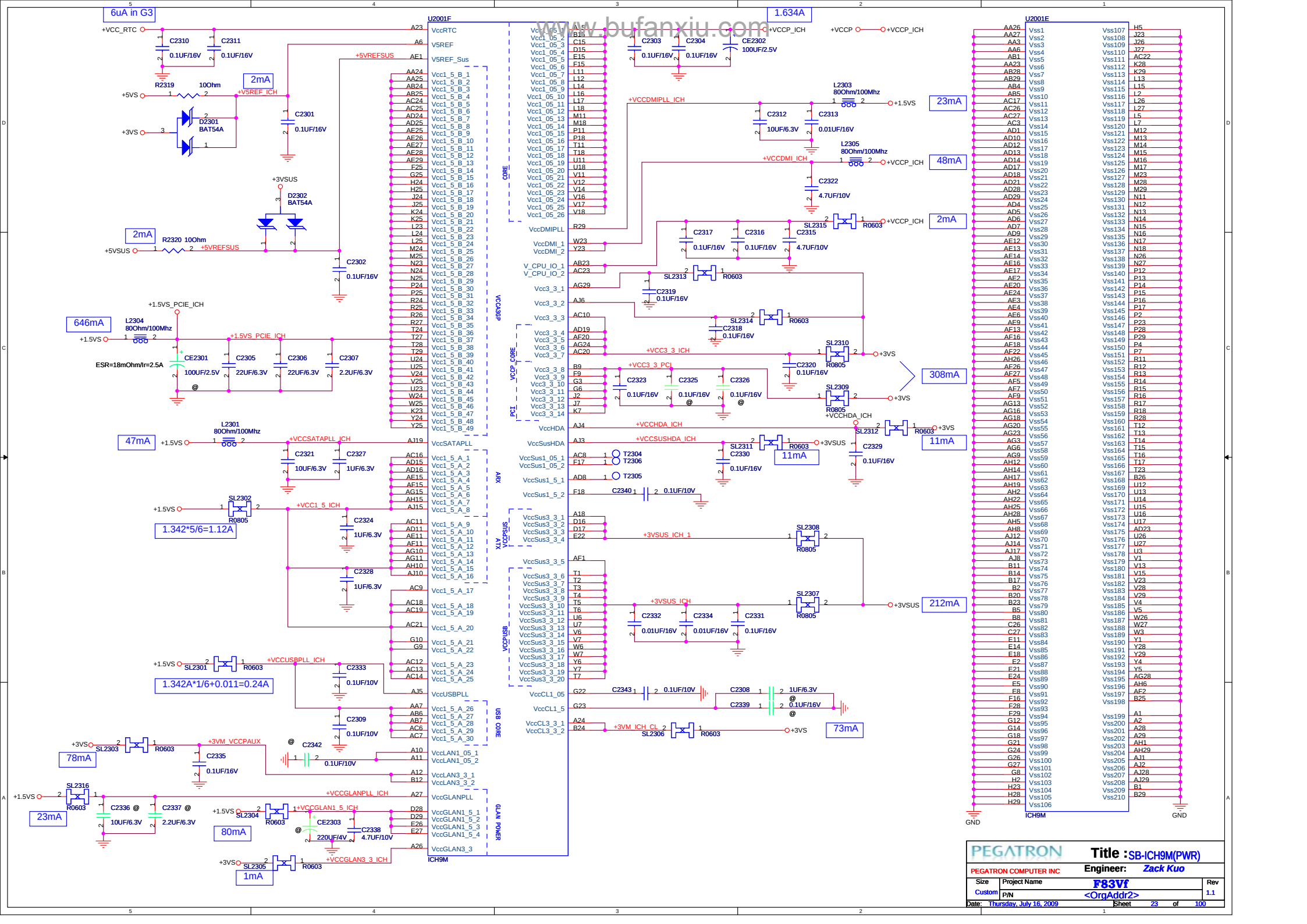




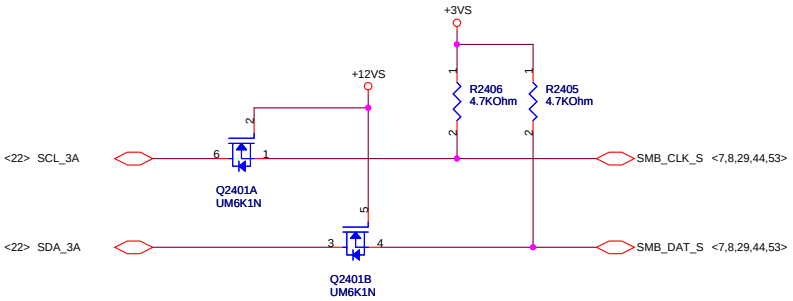
CL_VREF0/1 ~= 0.405 V

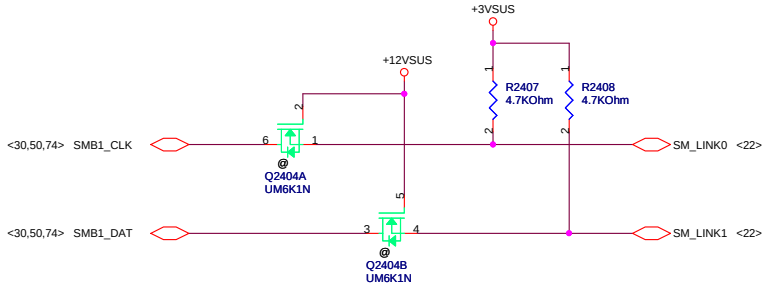
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max

PEGATRON	Title : SB-ICH9M(3)		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: Custom	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 22 of 100		



ICH9-M





PEGATRON COMPUTER INC

Title : ICH9M-Other

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 24 of 100

Main Board

PEGATRON

PEGATRON COMPUTER INC

Title : SB_****

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 25 of 100

Main Board

PEGATRON

PEGATRON COMPUTER INC

Title : SB_****

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 26 of 100

Main Board

PEGATRON

Title : SB_****

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 27 of 100

Main Board

PEGATRON

PEGATRON COMPUTER INC

Title : SB_****

Engineer: Zack Kuo

Size	Project Name	Rev
Custom	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 28 of 100

Main Board

U2901

ICS9LPR362AGLF-T
0610-000C000

Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0
33PCI3 R2907 10KOhm

0 : Pin 43/44 = SRC CLK
1 : Pin 43/44 = CPU_ITP CLK
33PCIF4 R2908 10KOhm

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0
33PCIF5 R2910 10KOhm

0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#
33PCI0 R2911 10KOhm
R2928 10KOhm

PEREQ1#:
PEREQ1# R2922 10KOhm

PEREQ2#:
PEREQ2# R2923 10KOhm

PEREQ3# : PCIEX2/4
PEREQ4# : PCIEX3/5/7

For 364 Over-clocking

33PCI1 R2932 10KOhm, R2929 @ 10KOhm
REF0 R2931 10KOhm, R2930 @ 10KOhm

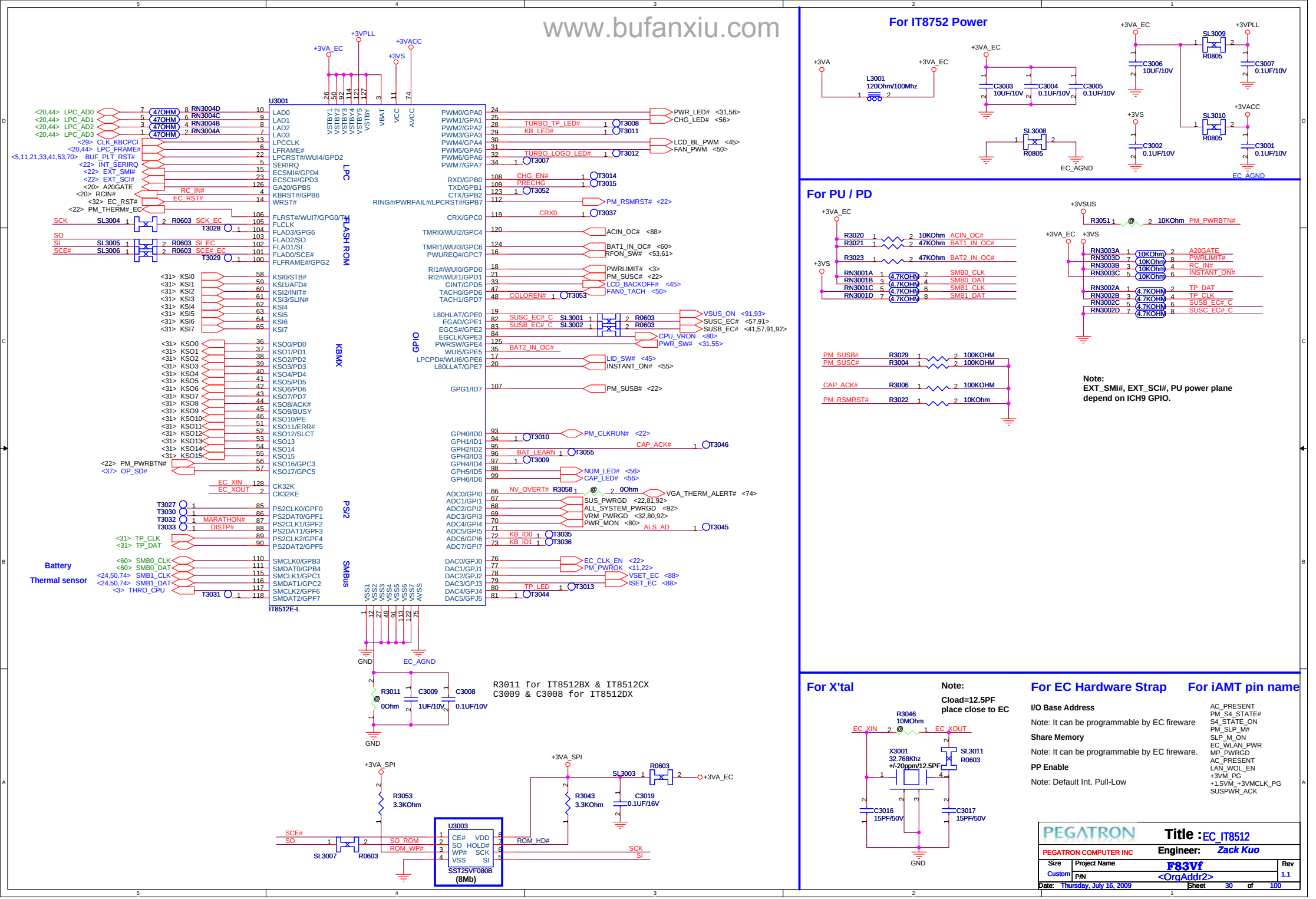
Reserved for R1.0 Debug

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

F83

	R2903	R2904	R2925
363:VREF	1K	330	@
364:TURBO	@	10K	0
364:NO TURBO	@	@	@

PEGATRON COMPUTER INC
Title : CLK_ICS9LPR363
Engineer: Zack Kuo
Size: Custom | Project Name: F83Vf | Rev: 1.1
P/N: <OrgAddr2>
Date: Thursday, July 16, 2009 | Sheet 29 of 100



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal

Note:
Cload=12.5PF place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

PP Enable

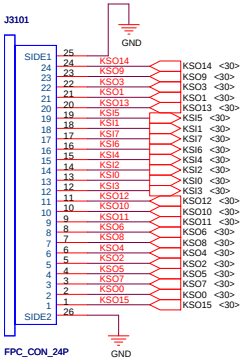
Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM, +3VMCLK_PG
SUSPWR_ACK

PEGATRON	Title : EC_IT8512	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: Custom	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 30 of 100	

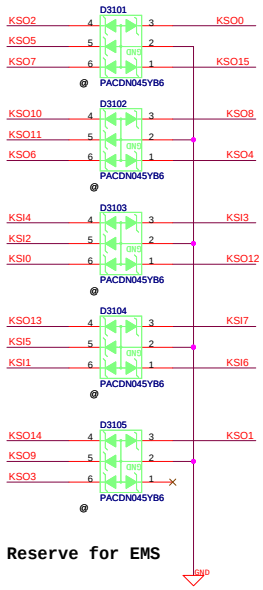
For Keyboard



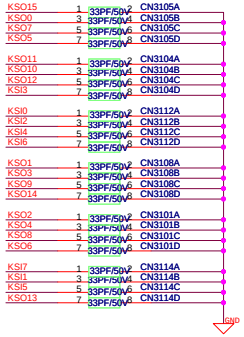
P/N:12G182002408

T53 KB MATRIX

Close to keyboard connect

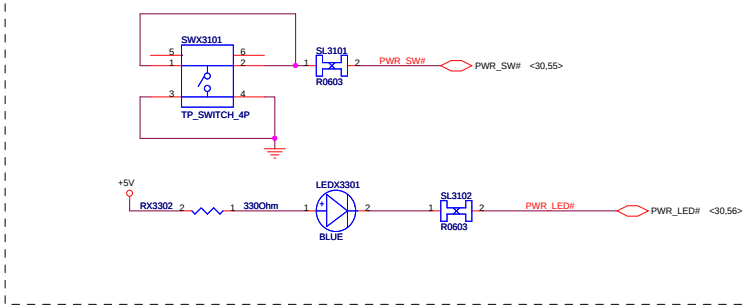


Reserve for EMS



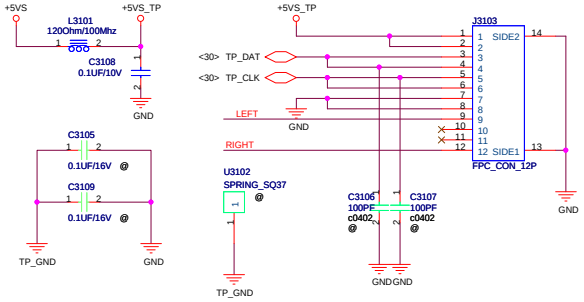
Reserve for EMI

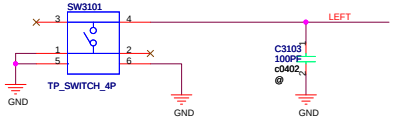
TEST



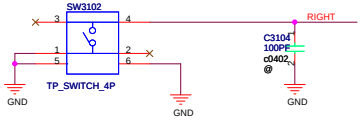
Touch-Pad

P/N:12G183301208



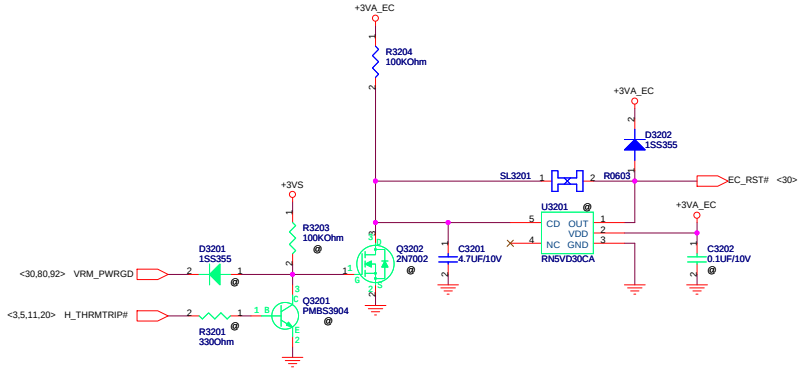


P/N:12G091031041



P/N:12G091031041

PEGATRON	Title :	EC_IT8512 (2/2)	
PEGATRON COMPUTER INC	Engineer:	Zack Kuo	
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 31 of 100		



PEGATRON

Title : EC_RESET

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 32 of 100

+3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>

+3VSUS <20,21,22,23,24,30,37,45,53,56,91,92>

GND <3,4,5,7,8,9,10,11,13,14,15,20,21,22,23,29,30,31,32,34,36,37,38,40,41,44,45,46,48,50,51,52,53,55,56,57,60,61,63,68,70,72,73,74,75,76,77,80,81,82,83,84,85,88,91,92>

LAN_GND <34>

LAN_GND

ground pad要打散熱孔

PCIE Tx,Rx方向是以南橋爲觀點
Chip pin Tx,Rx是以chip爲觀點

AR8121: Remove R3313
AR8131: Remove R3314

Close to U3301

For AR8131 : Remove R3309

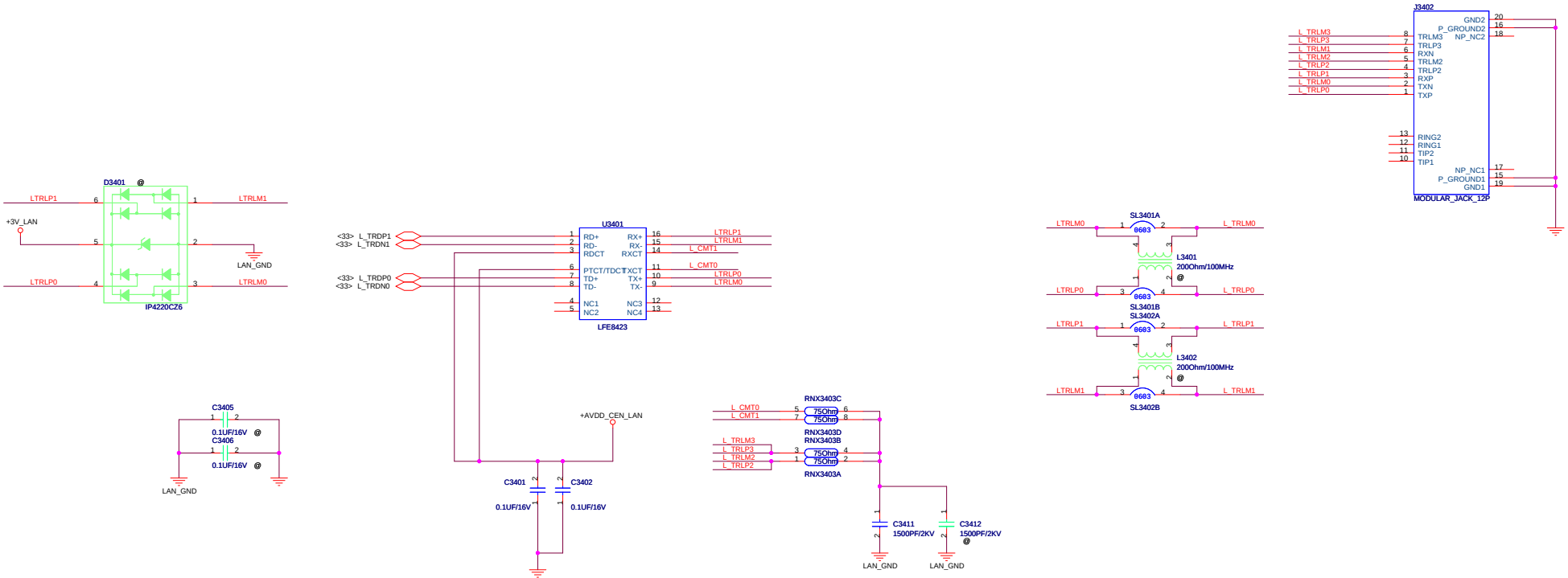
AR8121:Remove C3328
AR8131/25MHz: Remove C3328

With overclock:Remove SL3304, Add R3325
Not overclock:Add SL3304, Remove R3325

C3301 C3302 C3303 C3304 close to pin2

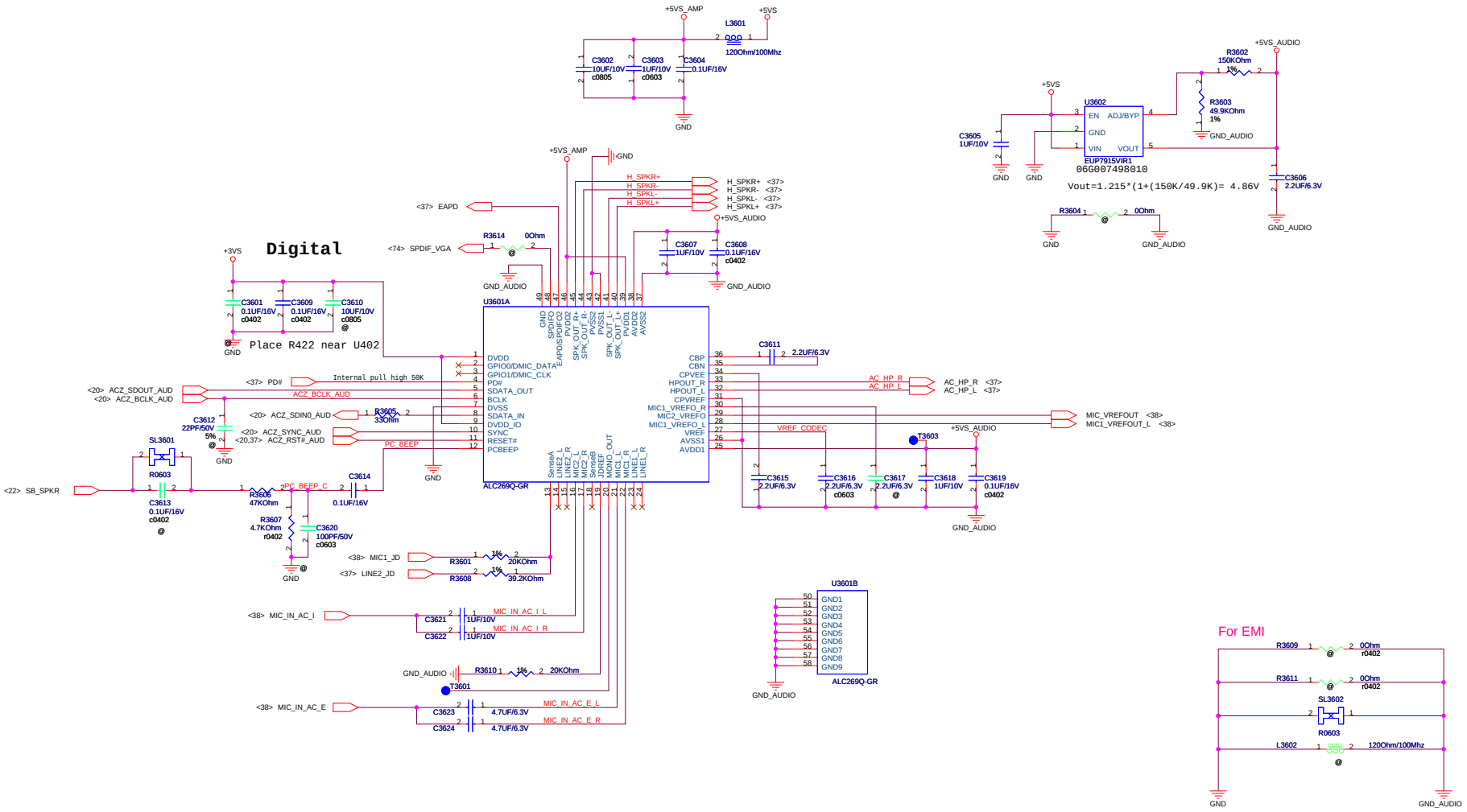
PEGATRON	Title : Atheros 8132		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 33 of 100		

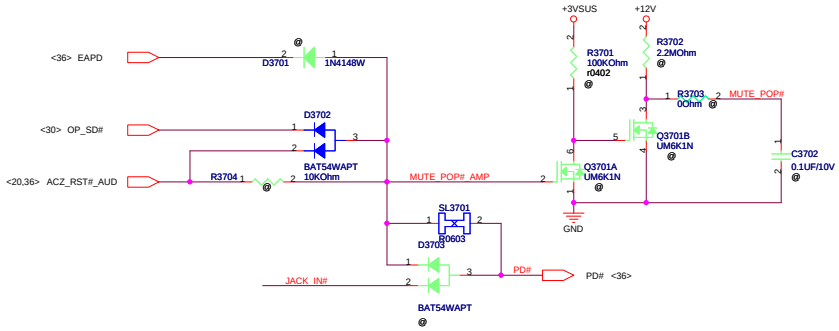
LAN / MODEM PORT

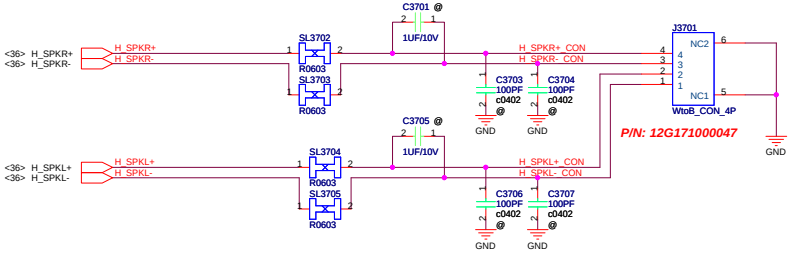


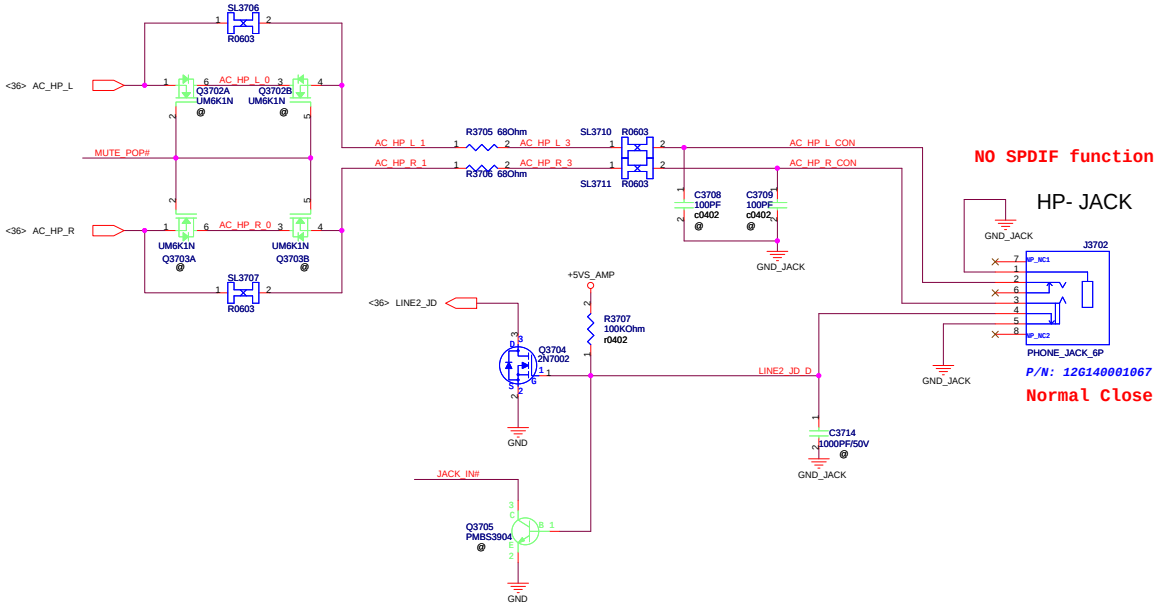
PEGATRON	Title : RJ45		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 34 of 100		

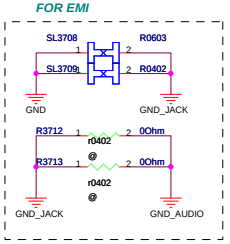
PEGATRON	Title : <Title>		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 35 of 100		





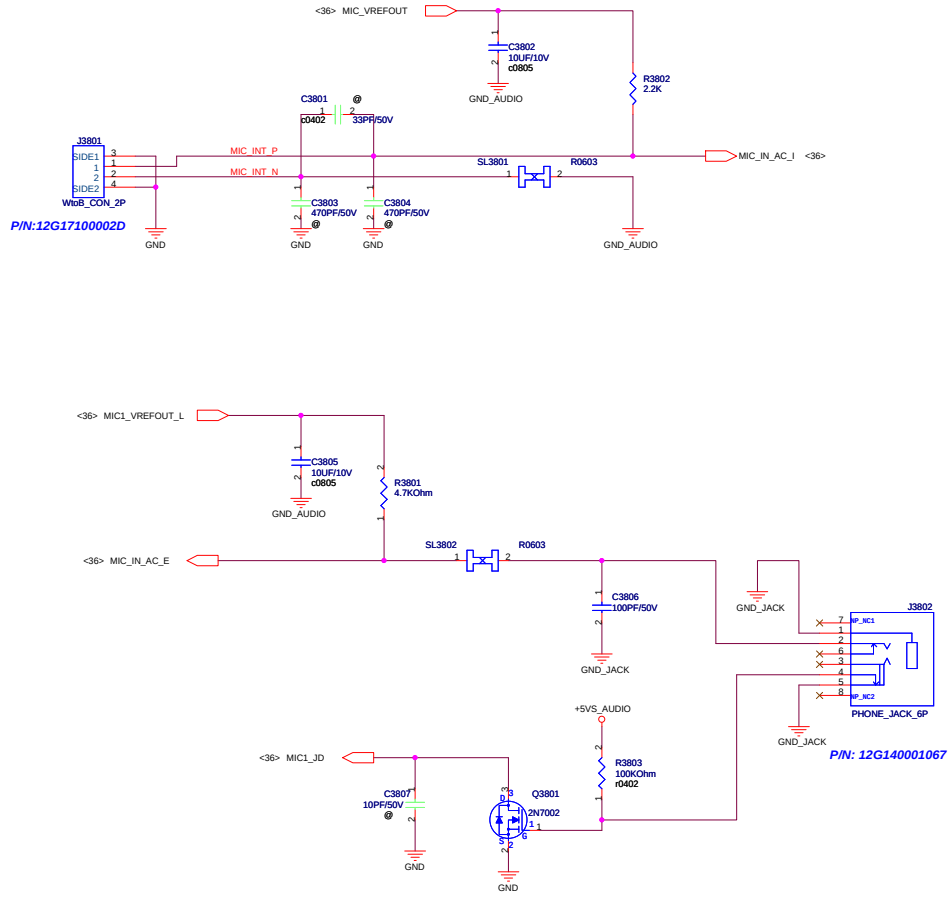






PEGATRON	Title : AUDIO		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 37 of 100		

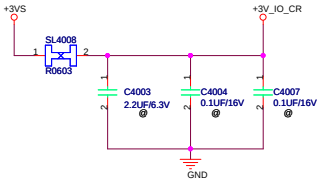
Internal MIC Pre-Amplifier



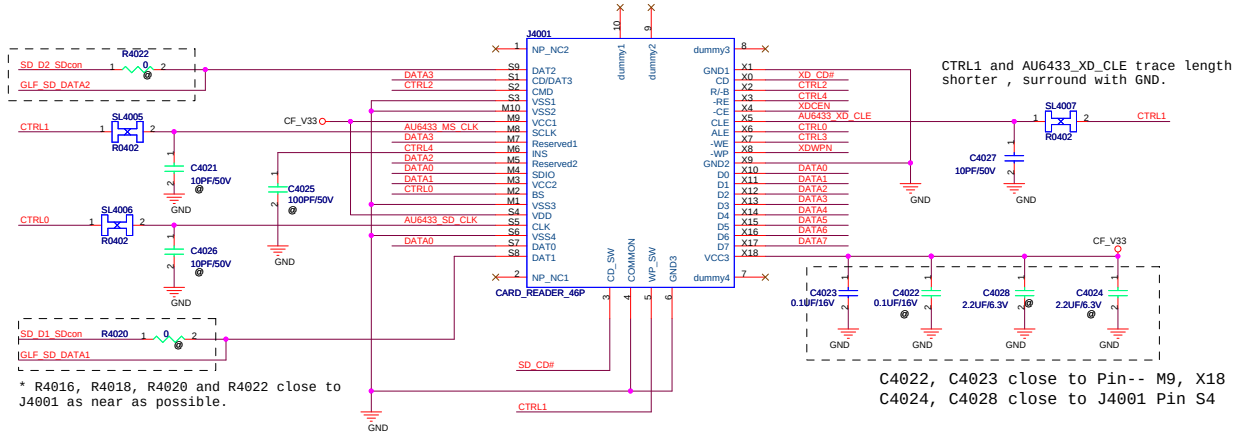
PEGATRON	Title : AUDIO		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf	P/N: <OrgAddr2>	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 38 of 100		

PEGATRON	Title : <Title>		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 39 of 100		

0304 for card reader chip via



CARD READER CONNECTOR

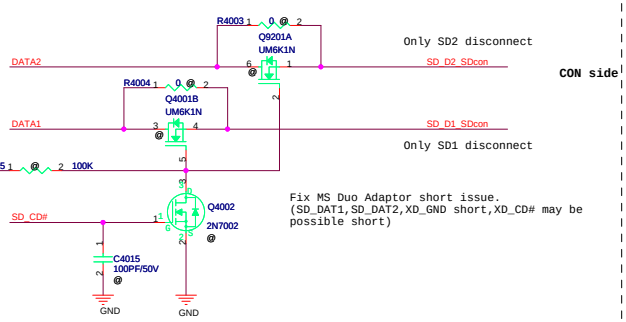


CTRL1 and AU6433_XD_CLE trace length shorter , surround with GND.

* R4016, R4018, R4020 and R4022 close to J4001 as near as possible.

C4022, C4023 close to Pin-- M9, X18
C4024, C4028 close to J4001 Pin S4

For AU6433-GEF

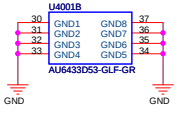


Only SD2 disconnect

Only SD1 disconnect

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

0304 for card reader chip via



48MHZ can provide by Clock GEN.
logic 1 or open on pad1->oscillator output

CHIPRESETN should keep low(< 0.8V) for 2ms ~ 10ms after:

1. 3.3V stable
2. Clock stable

Use AU6433-GEF
1:For check(Default)
0:For no check

AU6433-GLF :020K-000B000
AU6433-GEF :020K-0005000

CTRL0->SDCLK/XDALE/MSBS
CTRL1->SDWP/XDCLE/MSCLK
CTRL2->SDCMD/XDRBN
CTRL3->SDCDN/XDWRN
CTRL4->XDRDN/MSINS

XDCDN->XDCDN
XDCEN->XDCEN
SDDATA2->SDDATA2/xD CIS check is disable
XDWPN->XDWPN

ADDATA1->SDDATA1

DATA0->SDDATA0/XDDATA0/MSDATA0
DATA1->XDDATA1/MSDATA1
DATA2->XDDATA2/MSDATA2
DATA3->SDDATA3/XDDATA3/MSDATA3
DATA4->SDDATA4/XDDATA4/MSDATA4
DATA5->SDDATA5/XDDATA5/MSDATA5
DATA6->SDDATA6/XDDATA6/MSDATA6
DATA7->SDDATA7/XDDATA7/MSDATA7

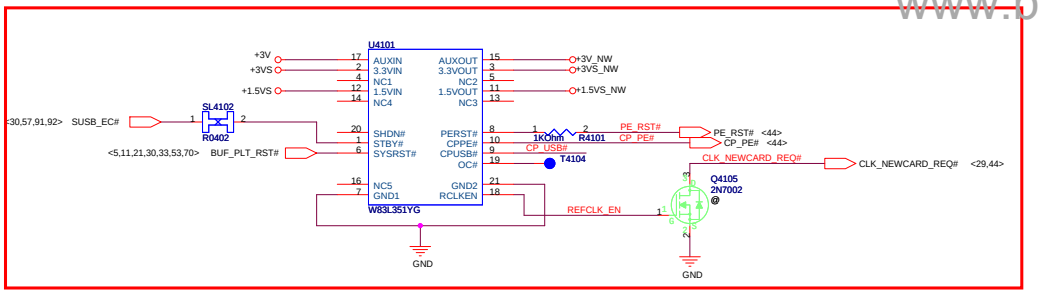
AU6433 GEF /GLF colay.

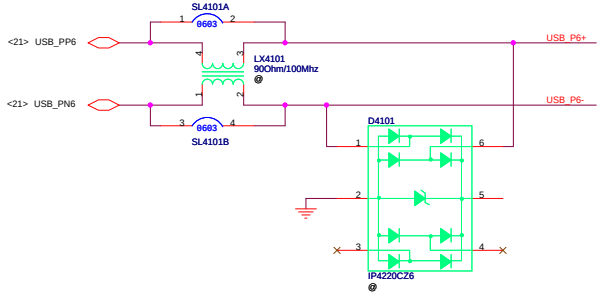
Option 1:AU6433-GEF
If use GEF package need:

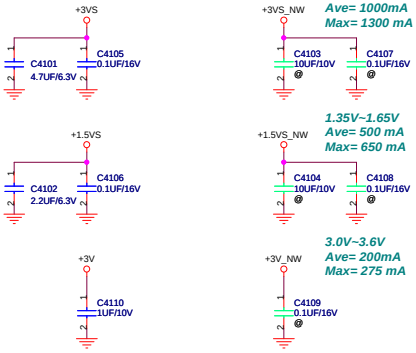
unmount-> R4016,R4018
mount->R4017,R4020,R4022,R4025,Q4001,Q4002.

Option 2:AU6433-GLF
If use GLF package need:
unmount->
R4017,R4020,R4022,R4025,Q4001,Q4002.
mount->R4016,R4018

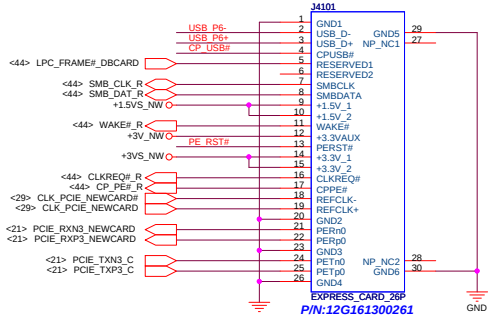
PEGATRON	Title : Card Reader AU8433	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 40 of 100	



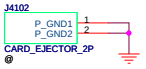




NewCard Header



NewCard Ejecter

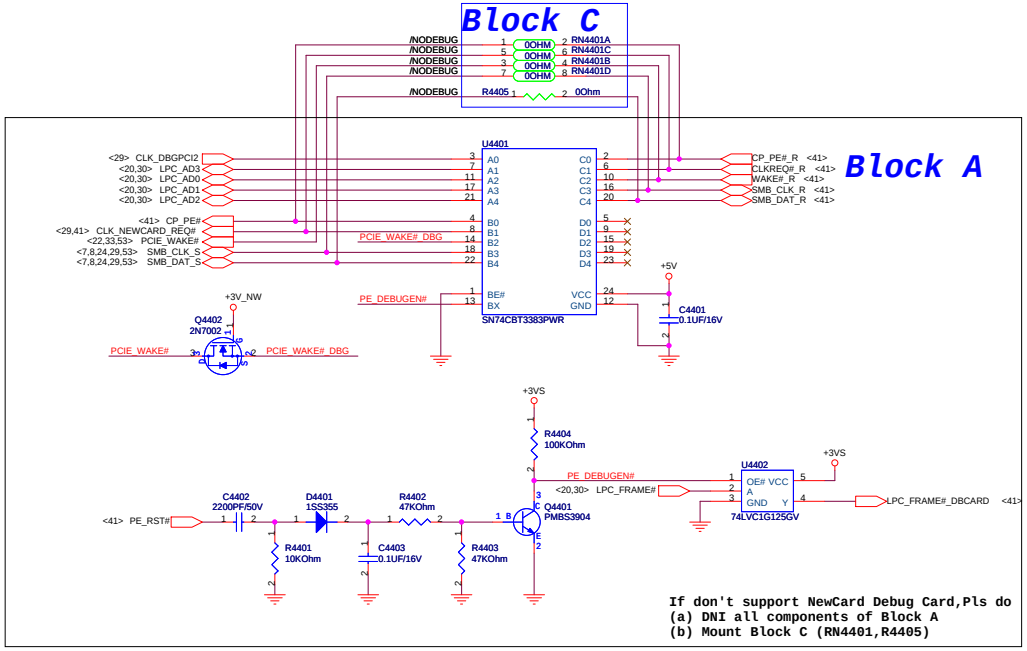


PEGATRON	Title :	CB_NEWCARD
PEGATRON COMPUTER INC	Engineer:	Zack Kuo
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 41 of 100	

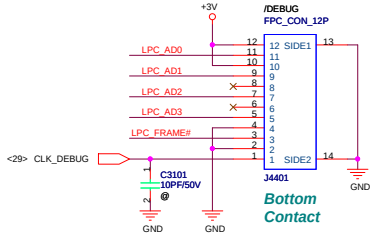
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 42 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 43 of 100		

For NewCard Debug Card

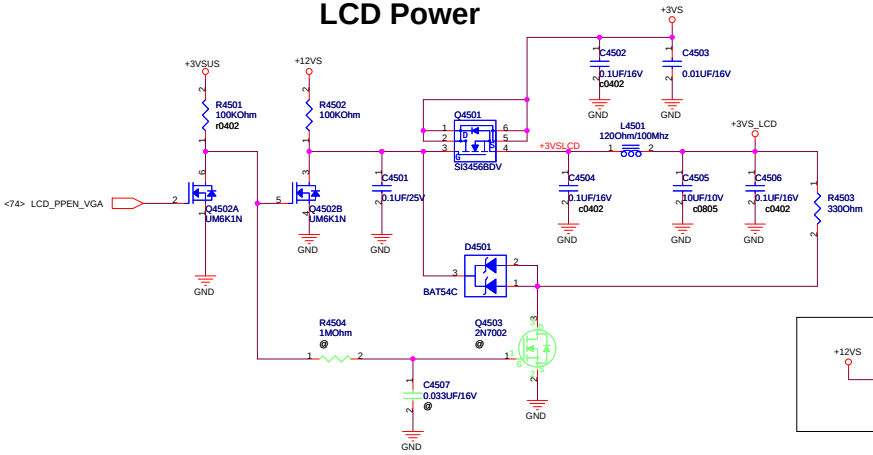


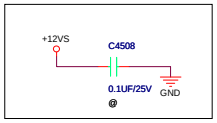
LPC Debug Port

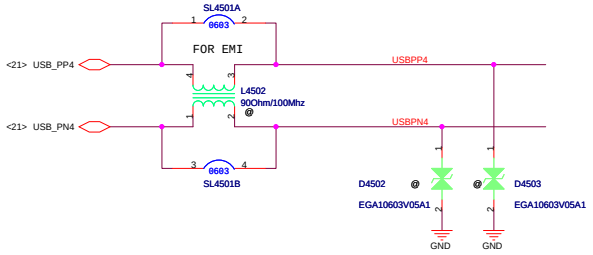


PEGATRON	Title : DEBUG		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 44 of 100		

LCD Power



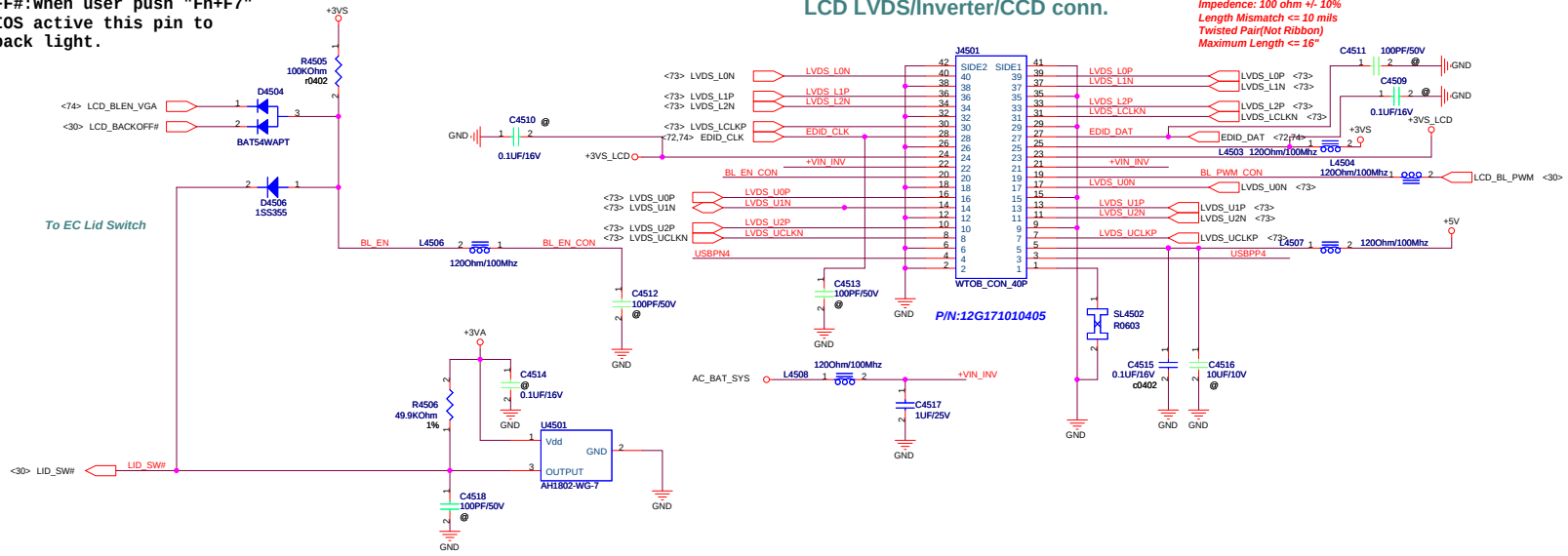




BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

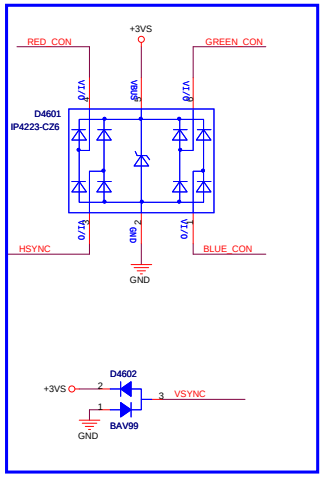
LCD LVDS/Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

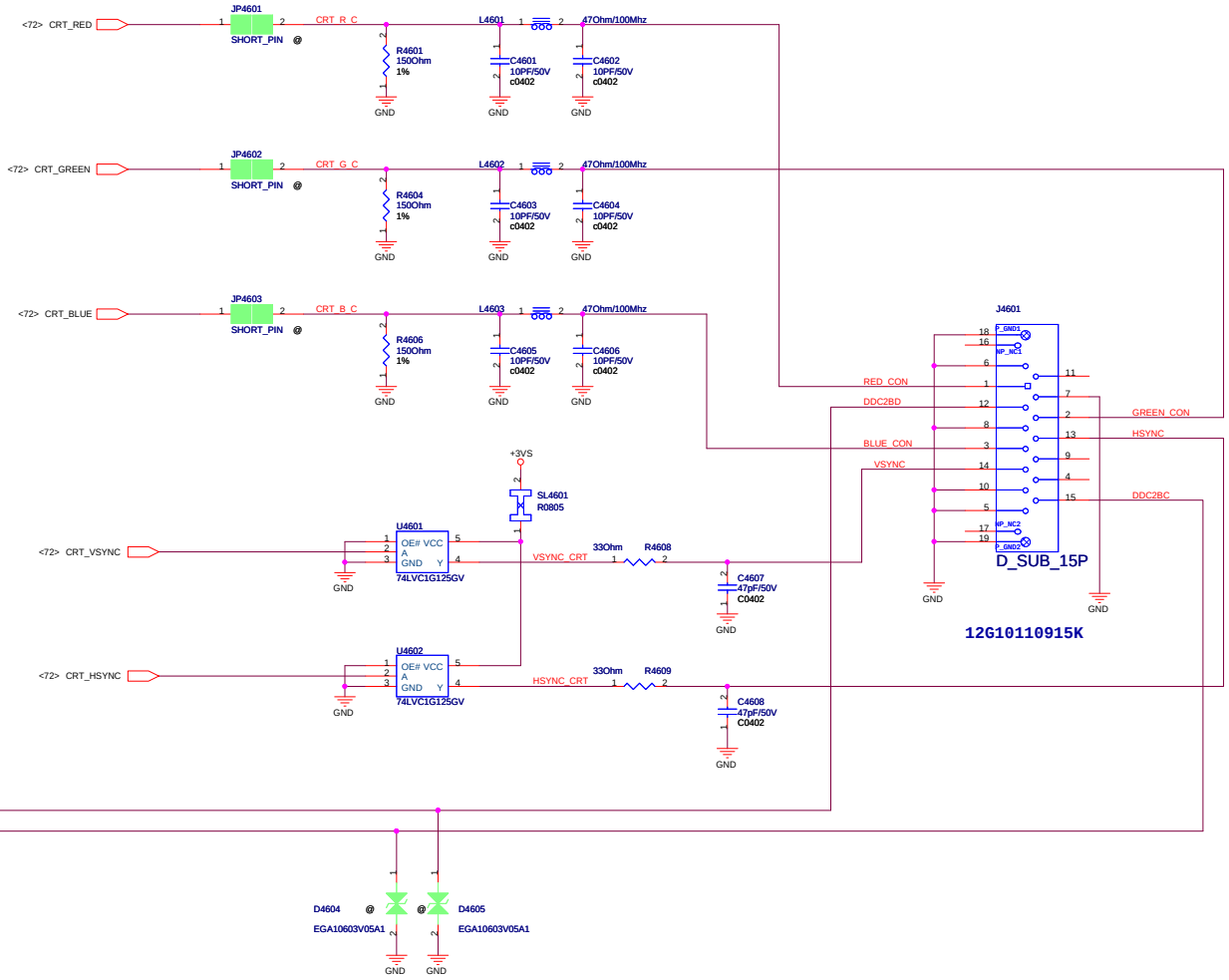


PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 45 of 100		

PLACE ESD Diodes near connector



37.5 ohm **50 ohm**

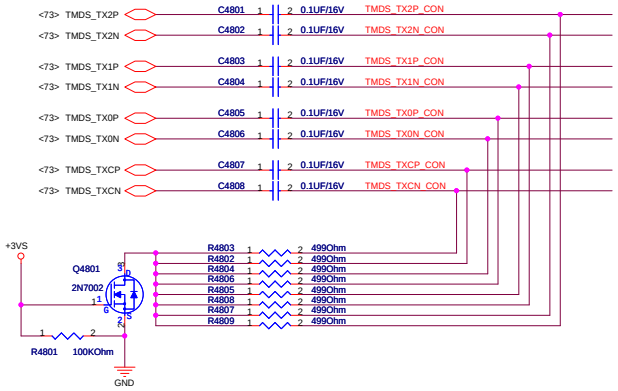


PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 46 of 100		

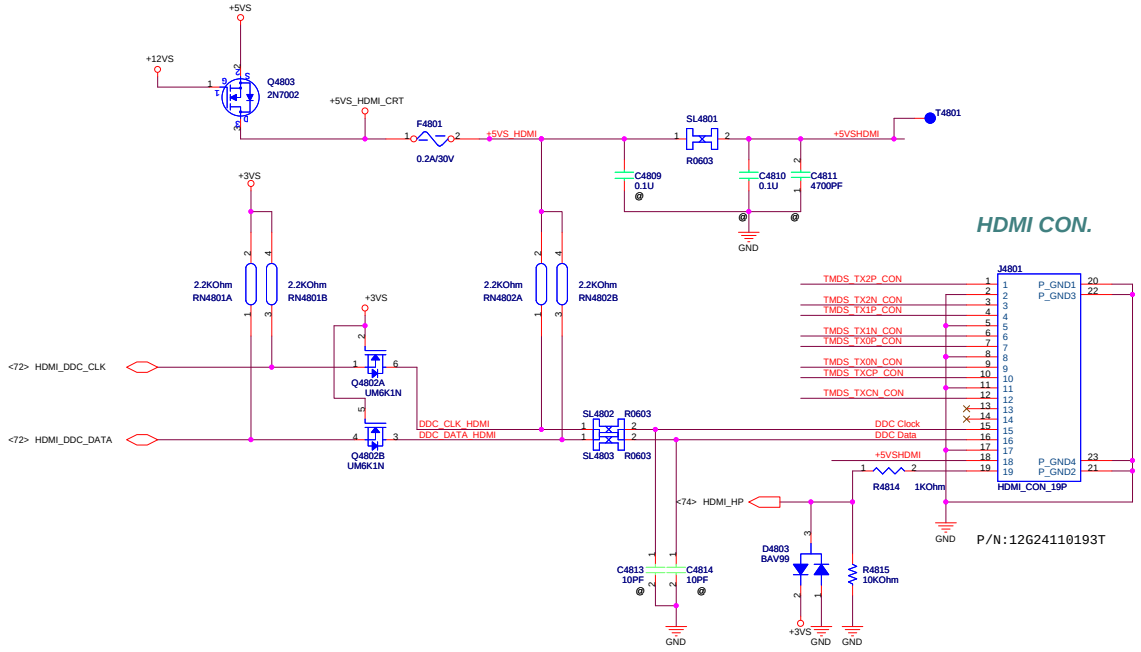
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 47 of 100		

HDMI

near the HDMI connector



Reference should be +5VS, but A71 answer that +3VS is fine. As long as it can turn the MOSFET on.



HDMI CON.

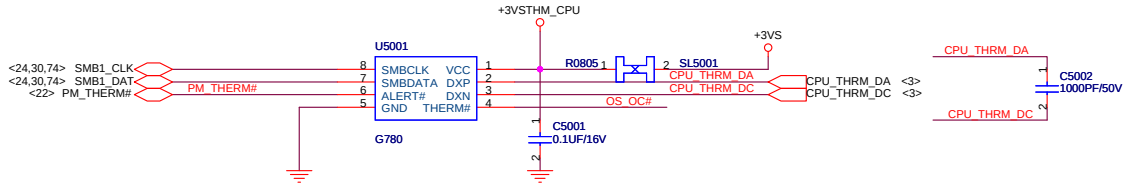
P/N:12G24110193T

Note: 1. L1805,L1806,L1807: For EMI.(defult=0 ohm)
2. DDC_CLK_HDMI,DDC_DATA_HDMI: +5V tolerant

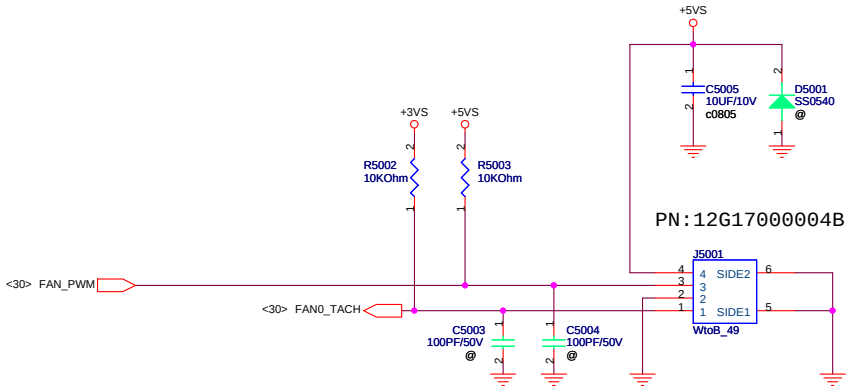
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 48 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 49 of 100		

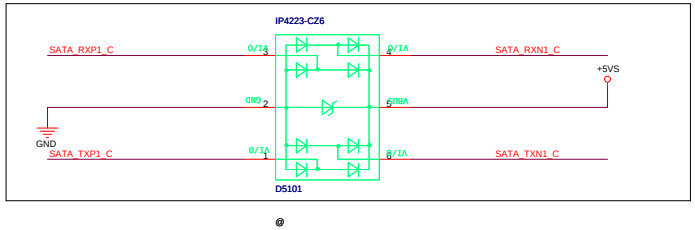
CPU Thermal Sensor



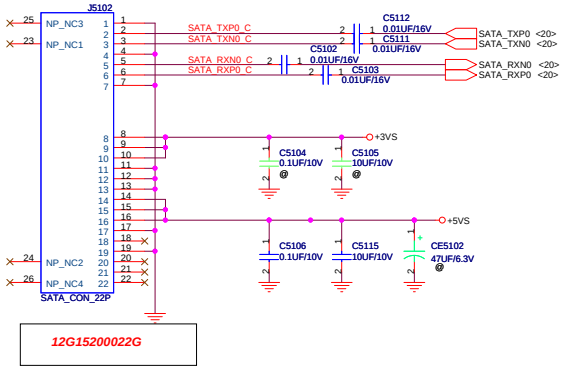
PWM Fan



ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Zack Kuo	
Size: Custom	Project Name: F83Vf	Rev: 1.1
Date: Thursday, July 16, 2009	Sheet 50 of 100	

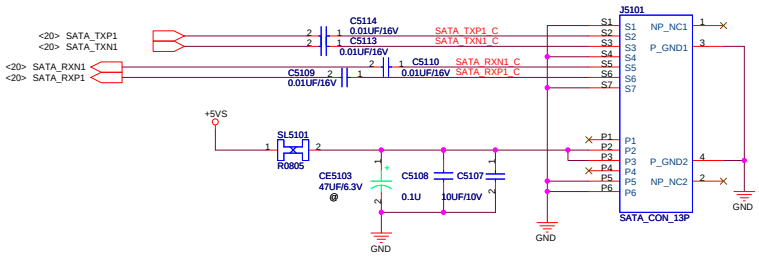


SATA HDD con.

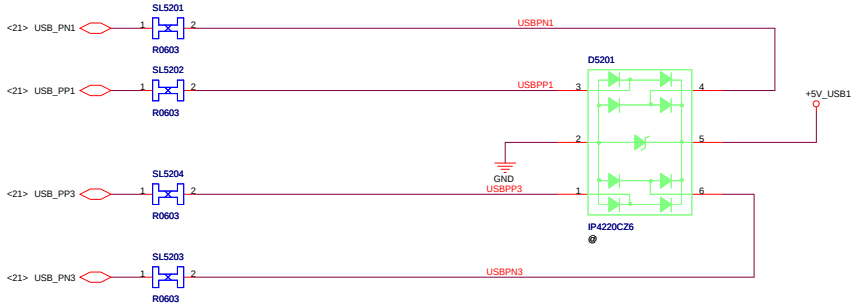


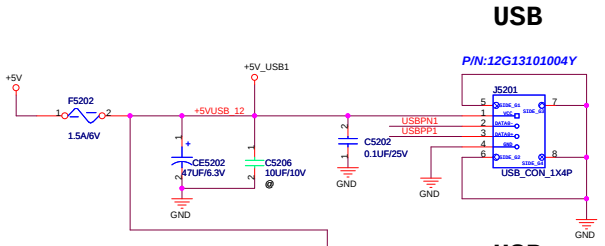
SATA CD-ROM con.

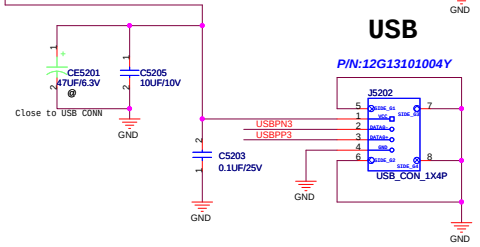
P/N:12G15100013J

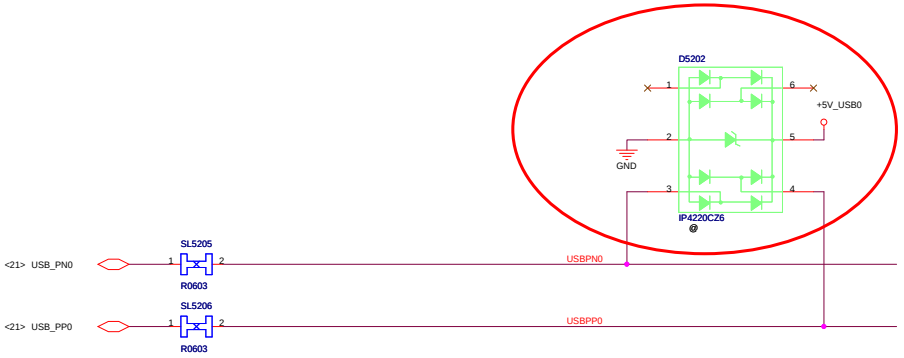


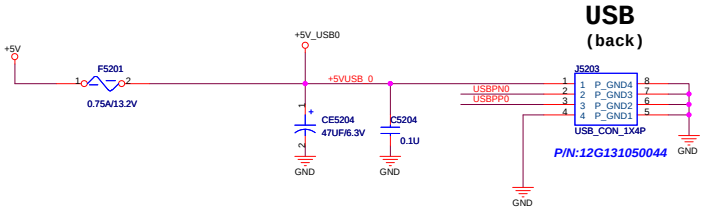
PEGATRON	Title : HDD/ODD CON		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 51 of 100		











PEGATRON

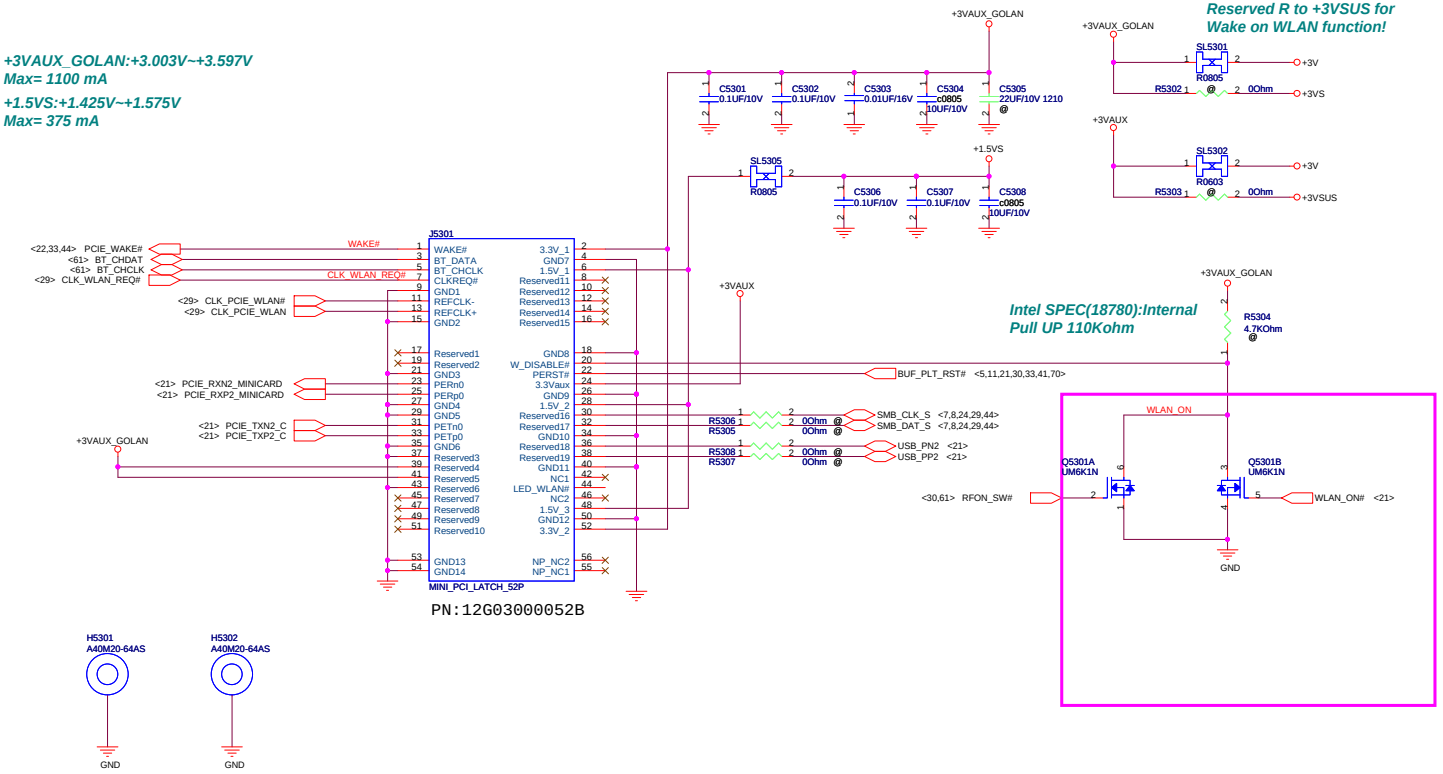
Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

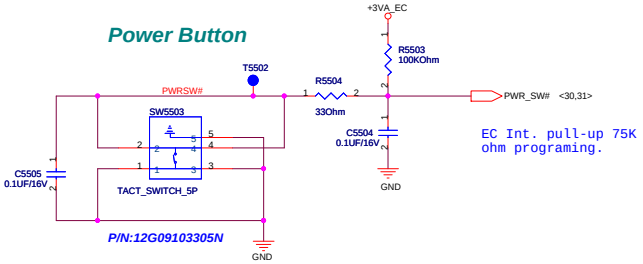
Date: Thursday, July 16, 2009 Sheet 52 of 100



PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 53 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 54 of 100		

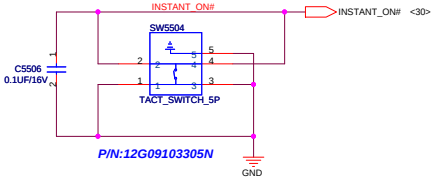
Power Button



EC Int. pull-up 75K ohm programing.

P/N:12G09103305N

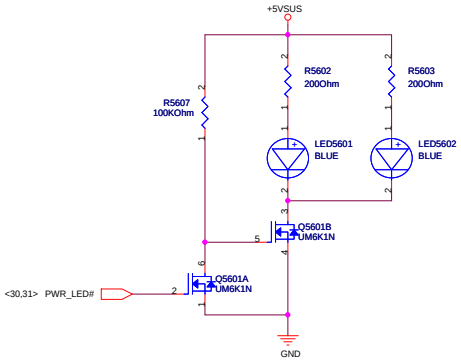
EXPRESS GATE



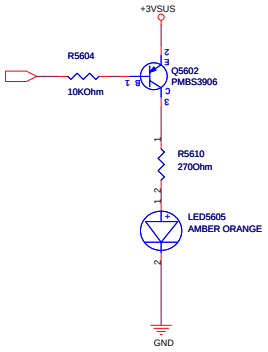
P/N:12G09103305N

PEGATRON	Title : SWITCH	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 55 of 100	

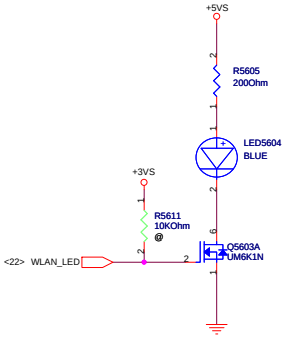
PWR LED



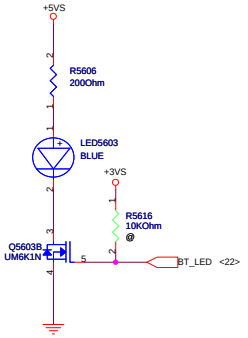
For BATTERY LED



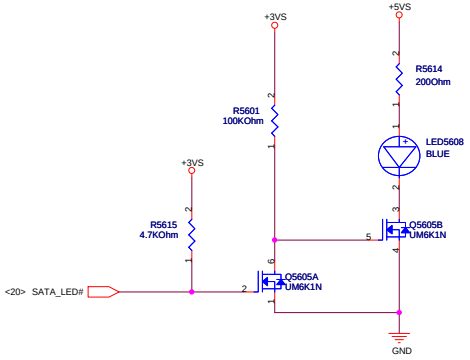
WireLess LED



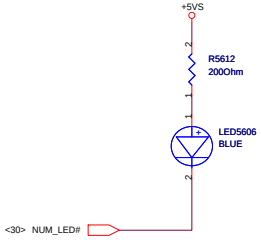
BT LED



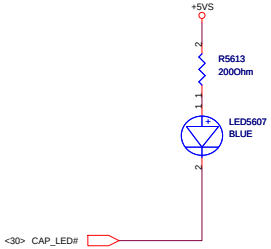
SATA LED



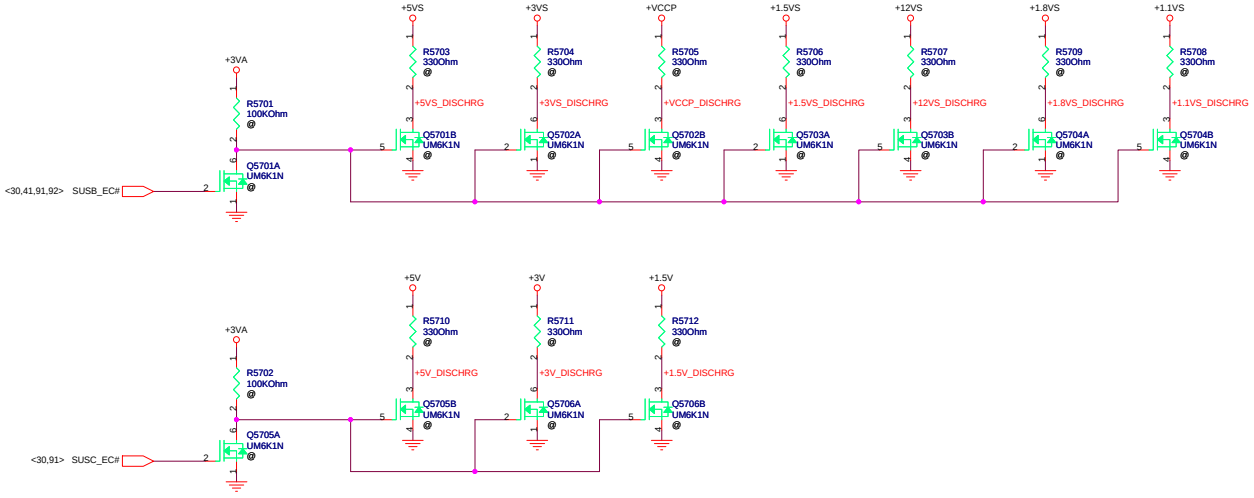
Num Lock



Cap. Lock



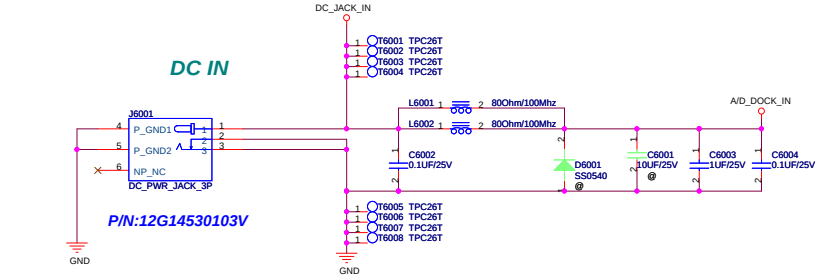
PEGATRON	Title :	Connector, LED
PEGATRON COMPUTER INC	Engineer:	Zack Kuo
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 56 of 100	

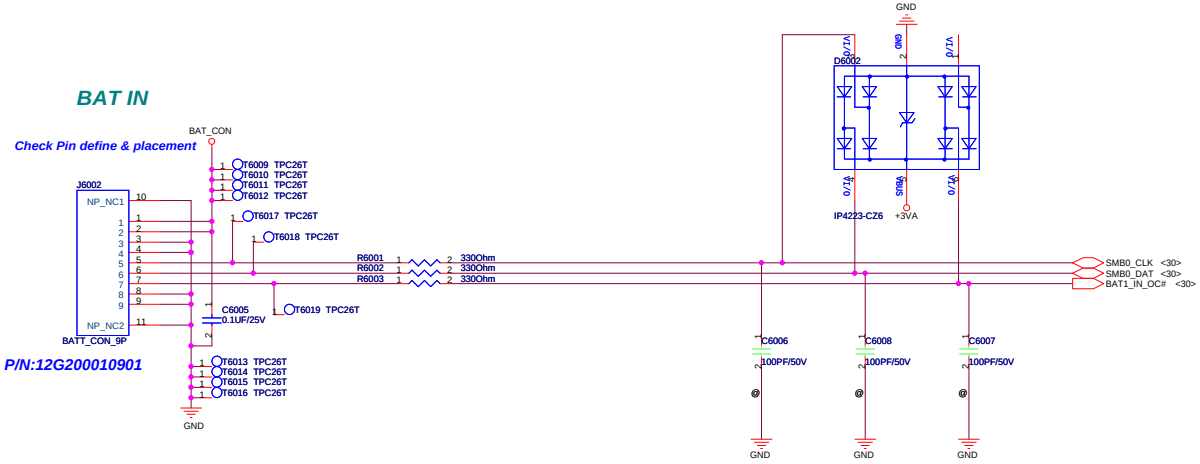


PEGATRON	Title : DISCHARGE	
PEGATRON COMPUTER INC	Engineer: Zack Kuo	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 57 of 100	

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 58 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 59 of 100		



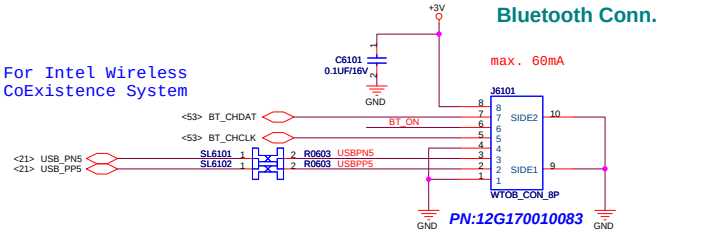


PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 60 of 100		

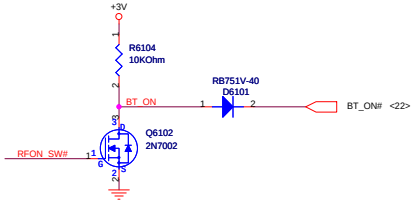
Bluetooth Conn.

For Intel Wireless
CoExistence System

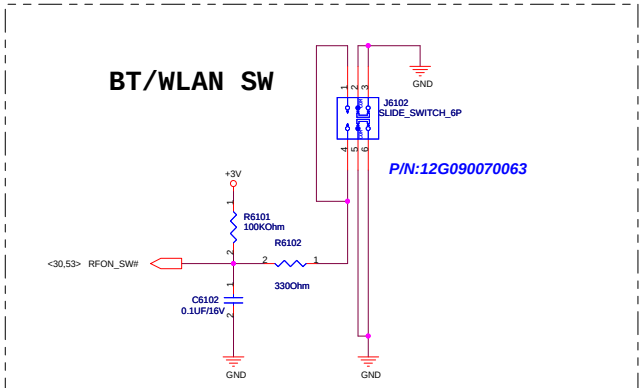
max. 60mA



P/N:12G170010083



BT/WLAN SW

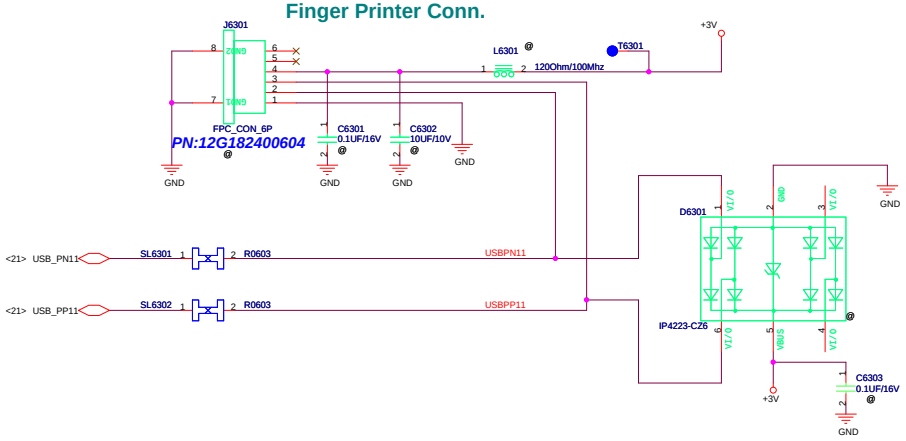


P/N:12G090070063

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 61 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 62 of 100		

Finger Printer Conn.



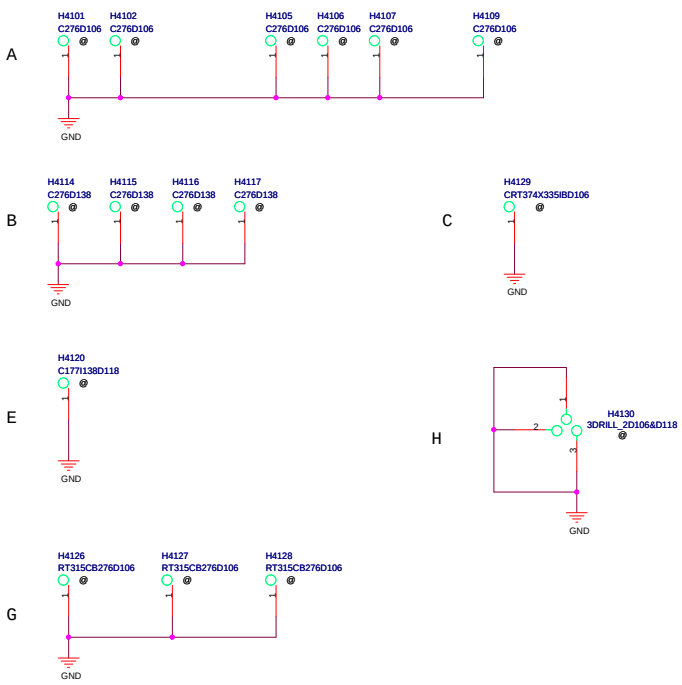
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 63 of 100		

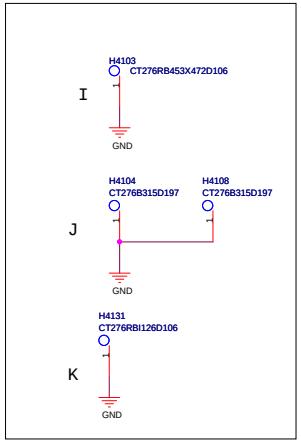
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 64 of 100		

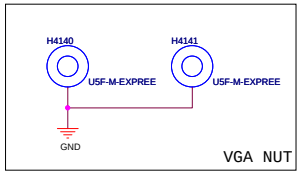
PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 65 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 66 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 67 of 100		







PEGATRON	Title : ScrewHole		
PEGATRON COMPUTER INC	Engineer: Zack Kuo		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 68 of 100		

R1.1

2009/06/30

1. Set DDR3 VREF to 0.75V LDO output.
2. Change Card Reader to AU6433D53-GLF.
3. Change LAN to Atheros AR6132.
4. Change Transformer to 10/100 TAIMAG HA003
5. Change ClockGen to ICS9LPR363.
6. Remove ClockGen 3362 circuits.
7. Unstuff Finger Printer Connector.
8.

PEGATRON

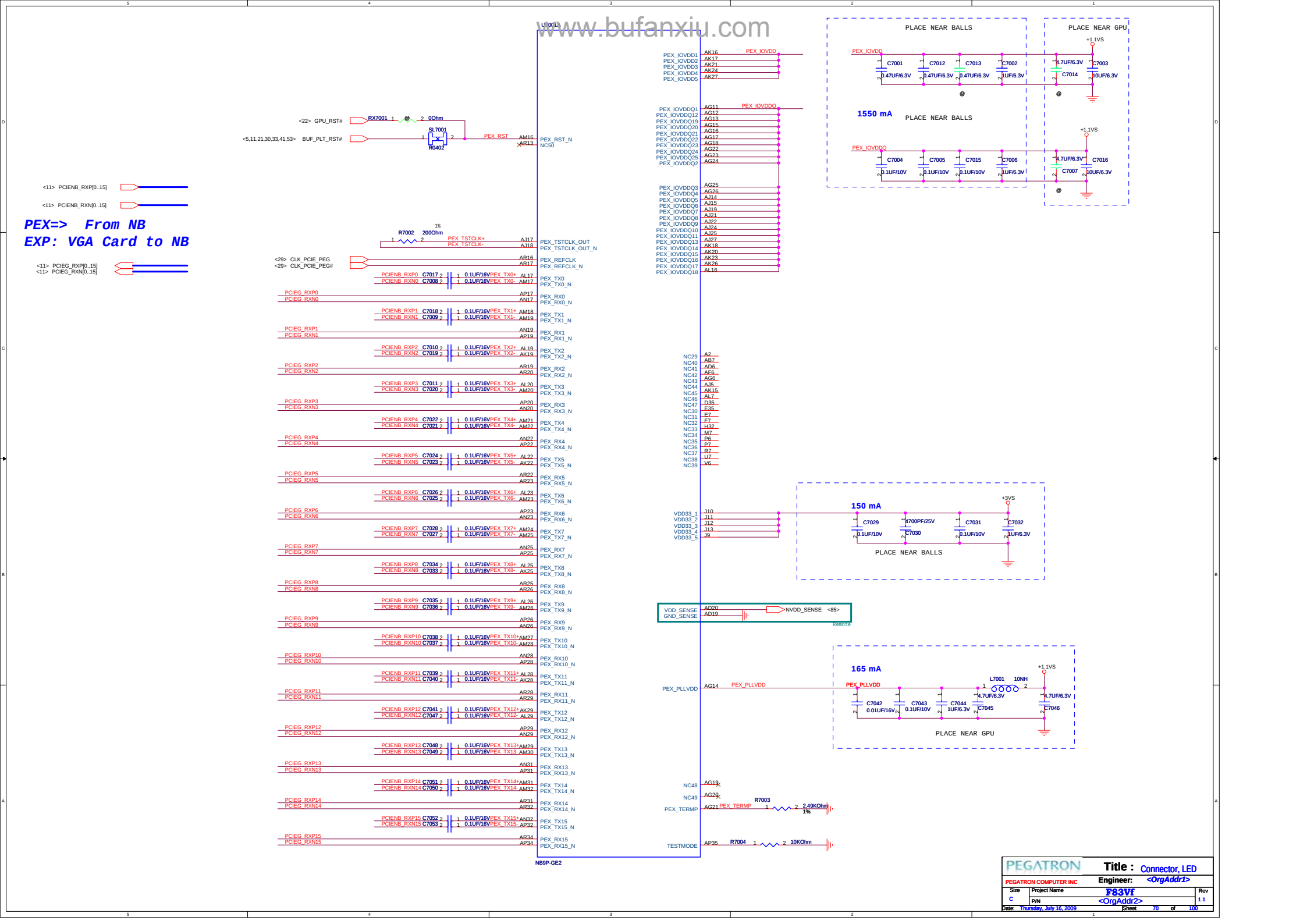
Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: Zack Kuo

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 69 of 100



PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 70 of 100

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: <OrgAddr1>		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 71 of 100		

change 4.7uF to 1uF
C5001,C5005,C5015

CRT

+3VS

RN7205A 2.2KOhm
RN7205B 2.2KOhm

L7201 220Ohm/100Mhz
130 mA
I0603
Irat=600mA
C7201 4.7UF/6.3V
C7202 4700PF/25V
c0603
C7203 0.01UF/25V
R7201 1240Ohm 1%

DACA_VDD
DACA_VREF
DACA_RSET

U7001F
AJ12 DACA_VDD
AK12 DACA_VREF
AK13 DACA_RSET
I2CA_SCL
I2CA_SDA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
NB9P-GE2

G1 I2CA_CLK
G4 I2CA_DAT
33OHM RN7201B
33OHM RN7201A
CRT_DDC_CLK <46>
CRT_DDC_DAT <46>

AM13 CRT_HSYNC <46>
AL13 CRT_VSYNC <46>
AM15 DAC_VR CRT_RED <46>
AM14 DAC_VG CRT_GREEN <46>
AL14 DAC_VB CRT_BLUE <46>

JP7201
JP7202
JP7203

R7202 150Ohm
R7203 150Ohm
R7204 150Ohm

near GPU

(180 mA)

DACB_VDD
RN7219A 10KOHM
U7001H
AC6 DACB_VDD
AC5 DACB_VREF
AB6 DACB_RSET
DACB_CSYNC
DACB_RED
DACB_GREEN
DACB_BLUE
NB9P-GE2
AB5
AA4
AB4
Y4
Composite

(130 mA)

DACC_VDD
RN7219B 10KOHM
U7001G
AG7 DACC_VDD
AK6 DACC_VREF
AH7 DACC_RSET
I2CB_SCL
I2CB_SDA
DACC_HSYNC
DACC_VSYNC
DACC_RED
DACC_GREEN
DACC_BLUE
NB9P-GE2
AM1
AM2
AK4
AL4
AJ4

G3 I2CB_CLK
G2 I2CB_DAT
33OHM RN7220B
33OHM RN7220A
HDMI_DDC_CLK <48>
HDMI_DDC_DATA <48>

XTAL_IN , XTAL_OUT
3.3V tolerance

correspondent BGA balls must be
12mils and 16 mil wide
near GPU

65 +25 +50 mA

+1.1VS
L7202 220Ohm/100Mhz
I0603
C7205 4.7UF/6.3V
C7204 1UF/6.3V
C7206 0.1UF/16V
C7207 0.1UF/16V
PLL_VDD

U7001E
AE9 PLLVDD
AD9 VID_PLLVDD
AF9 SP_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
NB9P-GE2
D2
B1
D1
B2

<29> CLK_GFX_SSC
<29> CLK_GFX_NOSSC
R7216 @ 0Ohm
R7217 @ 0Ohm
XTALSSIN
XTALIN
XTALOUT
XTAL_OUTB

R7209 10KOhm
R7218 @ 10KOhm
X7201 27Mhz
C7208 18PF/50V
C7209 18PF/50V
10/10/5 PPM

near GPU
R7207 @ 22Ohm
R7208 10KOhm
NOT SSC NEED PD 10K

SS_CLKIN

+3VS
R7210 @ 4.7Ohm
+3VS_SSC
C7210 @ 1UF/6.3V
C7211 @ 0.1UF/16V
C7212 @ 470PF/50V

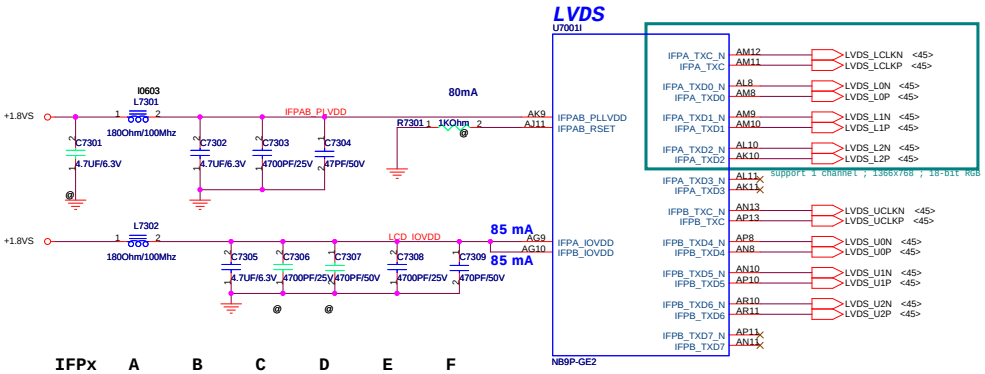
RN7202A 10KOHM @
RN7202B 10KOHM @

U7201 @ ICS91730AMLF
CLKIN
VDD
GND
CLKOUT/FS_IN0
PD#
SCLK
SDATA
REF_OUT/FS_IN1
SS_PD#
SS_REFOUT
EDID_CLK <45,74>
EDID_DAT <45,74>

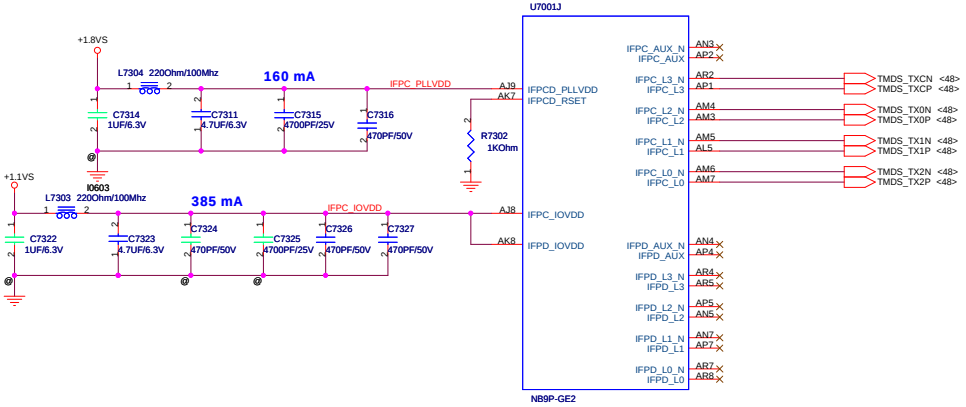
R7211 @ 22Ohm
SS_CLKOUT
near ICS

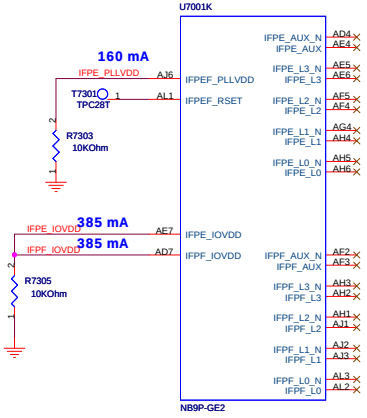
EXTERNAL SPREAD SPECTRUM
Address: 0xD4H

PEGATRON	Title : Connector, LED	
PEGATRON COMPUTER INC	Engineer: <OrgAddr1>	
Size: C	Project Name: F83Vf	Rev: 1.1
	P/N: <OrgAddr2>	
Date: Thursday, July 16, 2009	Sheet 72 of 100	



IFPx	A	B	C	D	E	F
	LVDS	LVDS				
			HDMI DVI	HDMI DVI(S/D)	HDMI DVI(S/D)	



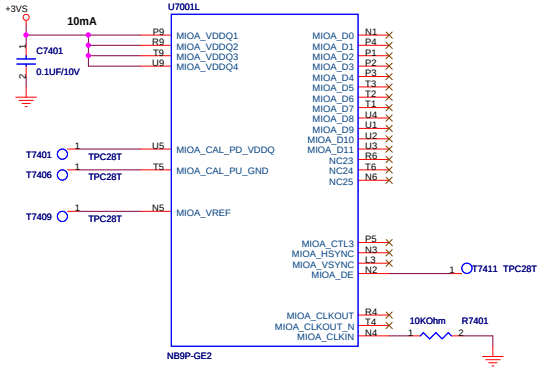


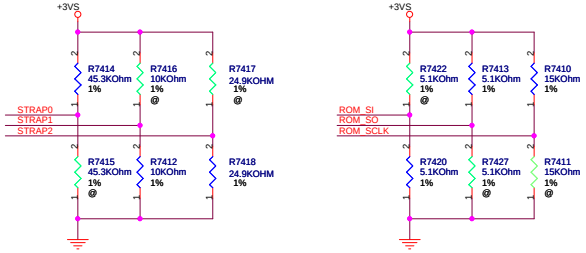
PEGATRON
PEGATRON COMPUTER INC

Title : Connector, LED
Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

Date: Thursday, July 16, 2009 Sheet 73 of 100





STRAP0

USER

3	2	1	0	PANEL	VS/HS
0	0	0	0	XGA	-/-
0	0	0	1	XGA	+/+
0	0	1	0	SXGA	+/+
0	0	1	1	SXGA+	-/-
0	1	0	0	UXGA	+/+
1	1	1	1	EDID	N/A

STRAP1

3GIO PADCFG

3	2	1	0	PANEL
0	0	0	0	DESKTOP
0	0	0	1	NOTEBOOK
0	0	1	0	RESERVED
.				
.				
1	1	1	1	RESERVED

STRAP2

LOGICAL BIT

0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

N10P-GE1 : 0x0652
N10P-GV2 : 0x0654
~10100
= PCI_DEVICE[4][3][2][1][0]

ROM_SI_RAMCONFIG

MONO RANK

Hynix 64Mx16 -> ram_cfg = 0x0
Samsung 64Mx16 -> ram_cfg = 0x1
Samsung 32Mx16 -> ram_cfg = 0x5
Hynix 32Mx16 -> ram_cfg = 0x7

5K PU 1000	PD 0000
10K PU 1001	PD 0001
15K PU 1010	PD 0010
20K PU 1011	PD 0011
25K PU 1100	PD 0100
30K PU 1101	PD 0101
35K PU 1110	PD 0110
45K PU 1111	PD 0111

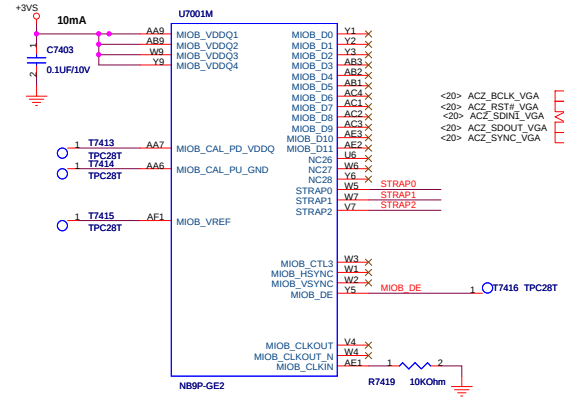
ROM_SO

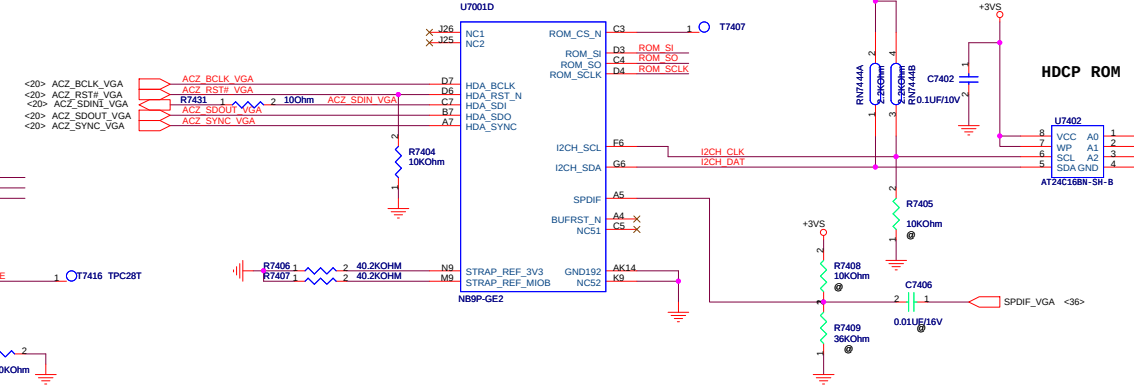
XCLK_277	TVMODE[2]..TVMODE[0]
XCLK_277	0 RESERVED
	1 27MHZ
TVMODE	000 NTSC M
	001 NTSC J
	010 PAL M
	011 PAL N
	100 PAL CN
	101 PAL_BDGHI
	110 RESERVED
	111 RESERVED

ROM_SCLK

LOGICAL BIT

3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM



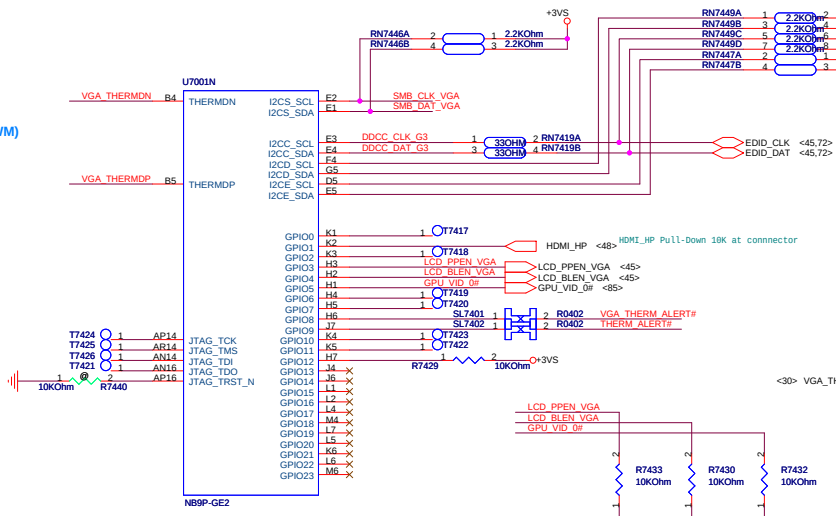


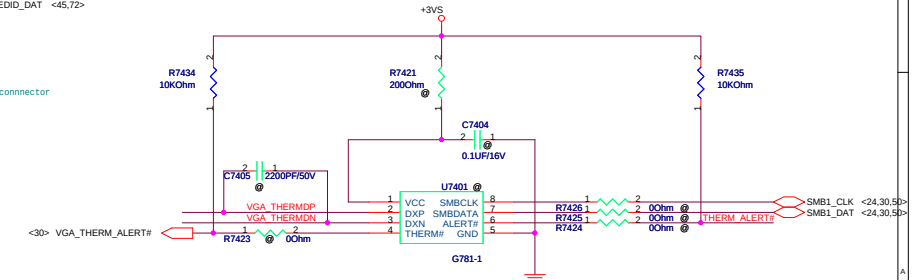
Default GPIO Assignment

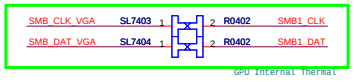
==========

GPIO0 -- AVAILABLE
GPIO1 -- IFPC (HDMI) Hot Plug Detect
GPIO2 -- Panel backlight brightness (PWM) (platform use EC PWM)
GPIO3 -- Panel power enable
GPIO4 -- Panel backlight ON/OFF
GPIO5 -- GPU VID0
GPIO6 -- GPU VID1
GPIO7 -- GPU VID2 / FBVDD VID0
GPIO8 -- OverTemp/GPU shutdown
GPIO9 -- ThermAlert/Fan PWM
GPIO10 -- FBVref Select
GPIO11 -- SLI SYNC0
GPIO12 -- AC power detect in
GPIO13 -- PS_CONTROL0
GPIO14 -- PS_CONTROL1
GPIO15 -- IFPE Hotplug detect
GPIO16 -- Dongle IFPC DVI mode
GPIO17 -- Dongle IFPC HDMI mode
GPIO18 -- Dongle IFPD DVI mode
GPIO19 -- Dongle IFPD HDMI mode
GPIO20 -- IFPD Hotplug detect
GPIO21 -- NVGEM/ (IFPF Hotplug detect)
GPIO22 -- SWAP Ready (SLI)
GPIO23 -- AVAILABLE

GPU_VID0	VID0	+VGA_VCORE
Low	0	0.9V
High	1	1.10V







PEGATRON

Title : Connector, LED

PEGATRON COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

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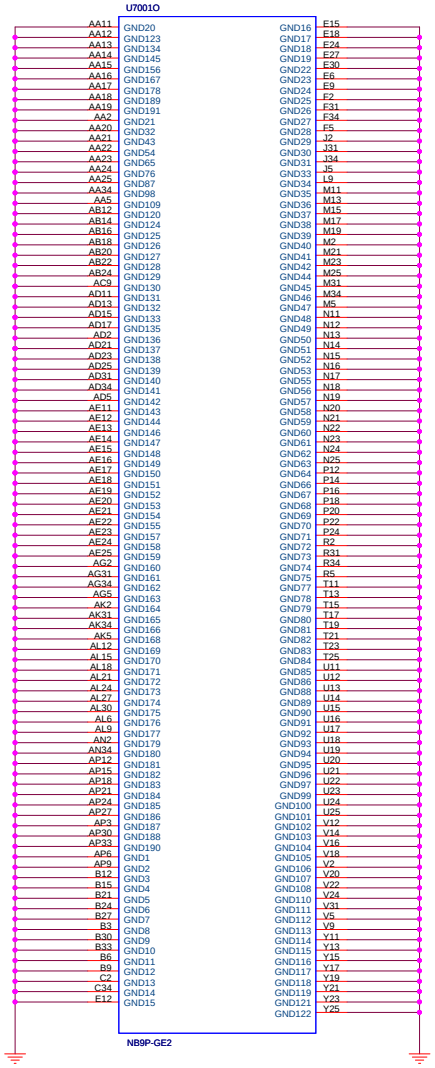

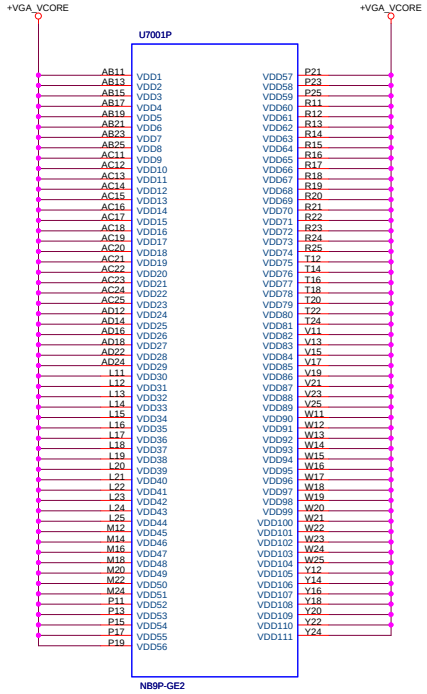

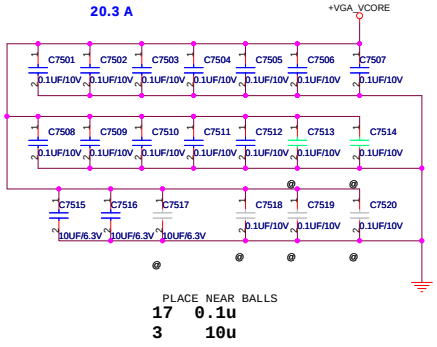

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: <OrgAddr1>		
Size: C	Project Name: F83Vf		Rev: 1.1
	P/N: <OrgAddr2>		
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BOT SIDE

U7001B

1720 mA

+1.8VS

Place Near Balls

C7608 C7611 C7606 C7618 C7612 C7613 C7610
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 4.7UF/6.3V 4.7UF/6.3V

C7601 C7605 C7604 C7602 C7603 C7609 C7607
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 1UF/6.3V 1UF/6.3V

PLACE BELOW GPU

FBVDDQ18 FBVDDQ19 FBVDDQ20 FBVDDQ1 FBVDDQ12 FBVDDQ23 FBVDDQ33 FBVDDQ34 FBVDDQ35 FBVDDQ36 FBVDDQ37 FBVDDQ38 FBVDDQ2 FBVDDQ3 FBVDDQ4 FBVDDQ5 FBVDDQ6 FBVDDQ7 FBVDDQ8 FBVDDQ9 FBVDDQ10 FBVDDQ11 FBVDDQ13 FBVDDQ14 FBVDDQ15 FBVDDQ16 FBVDDQ17

FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63

FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7

FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7

FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7

NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12

FB_VREF

FB_VREF1

N89P-GE2

FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28

FBA_A3 FBA_A0 FBA_A2 FBA_A1 FBB_A3 FBB_A4 FBB_A5 FBA_CS1# FBA_CS0# FBA_WE# FBA_BA0 FBA_CKE FBA_RST FBB_A2 FBA_A12 FBA_RAS# FBA_A11 FBA_A10 FBA_BA1 FBA_A8 FBA_A9 FBA_A6 FBA_A5 FBA_A7 FBA_A4 FBA_CAS# FBA_A13 FBA_BA2 FBA_CMD28

T7604 TPC28t

T7603 TPC28t

FBA_CKE

R7607 10KOhm

GND

FBA_RST FBA_ODT

R7612 10KOhm

GND

FBA_CLK0 FBA_CLK0_N FBA_CLK1 FBA_CLK1_N

FBA_CLK0 FBA_CLK0# FBA_CLK1 FBA_CLK1#

R7601 475Ohm

R7602 475Ohm

Near VRAM

FBA_DEBUG

R7606 60.4Ohm 1%

+1.8VS

T0401 TPC28t

25+25 mA

FB_DLLAVDD0 FB_PLLAVDD0

FB_PLLAVDD0

L7601 180Ohm/100Mhz

+1.1VS

C7644 C7614 C7619 C7615
0.01UF/16V 0.1UF/16V 0.1UF/16V 1UF/6.3V

+1.8VS

R7604 1% 1KOhm @ C7617 0.01UF/25V @

FB_VREF1

R7605 1% 1KOhm @ C7616 0.01UF/25V @

DDR2: VREF = 0.5 * FBVDDQ
DDR3: VREF = 0.7 * FBVDDQ
GPU Internal VREF R7604,R7605,C7617,C7616 no-stuff

+1.8VS +1.8VS

R7609 1KOhm 1% FBAVREF0 R7608 C0441 1KOhm 1% 0.047UF/16V

R7611 1KOhm 1% FBAVREF1 R7610 C0420 1KOhm 1% 0.047UF/16V

GND GND

LOWER SUB-PARTITION BOT SIDE

U7601

FBA_CLK0 FBA_CLK0# FBA_CKE FBA_RAS# FBA_CAS# FBA_WE# FBA_CS0# FBA_A13 FBA_BA0 FBA_BA1 FBA_BA2 FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12

mini-bus

FBADQM3 FBADQM2 FBAVREF0 +1.8VS

FBAD18 FBAD17 FBAD23 FBAD19 FBAD16 FBAD20 FBAD21 FBAD22 FBAD31 FBAD26 FBAD29 FBAD28 FBAD25 FBAD30 FBAD24 FBAD27

FBADQS_WP3 FBADQS_RN3 FBADQS_WP2 FBADQS_RN2

FBA_ODT

H5PS1G63EFR-S6

LOWER SUB-PARTITION TOP SIDE

U7602

FBA_CLK0 FBA_CLK0# FBA_CKE FBA_RAS# FBA_CAS# FBA_WE# FBA_CS0# FBA_A13 FBA_BA0 FBA_BA1 FBA_BA2 FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12

mini-bus

FBADQM1 FBADQM0 FBAVREF0 +1.8VS

FBAD1 FBAD7 FBAD2 FBAD6 FBAD5 FBAD4 FBAD0 FBAD8 FBAD15 FBAD10 FBAD12 FBAD14 FBAD11 FBAD13 FBAD9

FBADQS_WP1 FBADQS_RN1 FBADQS_WP0 FBADQS_RN0

FBA_ODT

H5PS1G63EFR-S6

orignal footprint:nb_bga_84p_31_512x394_share 0315-00BB000

UPPER SUB-PARTITION TOP SIDE

U7603

FBA_CLK1 FBA_CLK1# FBA_CKE FBA_RAS# FBA_CAS# FBA_WE# FBA_CS0# FBA_A13 FBA_BA0 FBA_BA1 FBA_BA2 FBB_A2 FBB_A3 FBB_A4 FBB_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12

mini-bus

FBADQM5 FBADQM6 FBAVREF1 +1.8VS

FBAD50 FBAD54 FBAD48 FBAD49 FBAD55 FBAD52 FBAD53 FBAD51 FBAD40 FBAD42 FBAD46 FBAD43 FBAD41 FBAD47 FBAD45 FBAD44

FBADQS_WP5 FBADQS_RN5 FBADQS_WP6 FBADQS_RN6

FBA_ODT

H5PS1G63EFR-S6

UPPER SUB-PARTITION BOT SIDE

U7604

FBA_CLK1 FBA_CLK1# FBA_CKE FBA_RAS# FBA_CAS# FBA_WE# FBA_CS0# FBA_A13 FBA_BA0 FBA_BA1 FBA_BA2 FBA_A0 FBA_A1 FBB_A2 FBB_A3 FBB_A4 FBB_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12

mini-bus

FBADQM7 FBADQM4 FBAVREF1 +1.8VS

FBAD39 FBAD33 FBAD38 FBAD32 FBAD36 FBAD35 FBAD34 FBAD37 FBAD58 FBAD56 FBAD60 FBAD63 FBAD61 FBAD59 FBAD62 FBAD57

FBADQS_WP7 FBADQS_RN7 FBADQS_WP4 FBADQS_RN4

FBA_ODT

H5PS1G63EFR-S6

+1.8VS

C7638 C7637 C7635 C7624 C7621 C7633 C7628 C7622 C7625 C7626
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V 4.7UF/6.3V 4.7UF/6.3V

C7640 C7639 C7634 C7630 C7629 C7636 C7631 C7632 C7627 C7623 C7643 C7642
1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V 1UF/6.3V

PEGATRON

Title : F/B A GPU

PEGATRON COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

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BOT SIDE

U7001C

1720 mA

+1.8VS

C7712 0.1UF/10V, C7723 0.1UF/10V, C7716 1UF/6.3V, C7718 4.7UF/6.3V

C7711 0.1UF/10V, C7721 0.1UF/10V, C7710 0.1UF/10V, C7707 0.1UF/10V

Main source :
Hynix DDR2 64M*16 500Hz/1.8V
H5PS1G63EFR-20L(0315-00AZ000)

Second source :
SAMSUNG DDR2 64M*16 500Hz/1.8V
K4N1G164QQ-HC20(0315-002E0AS)

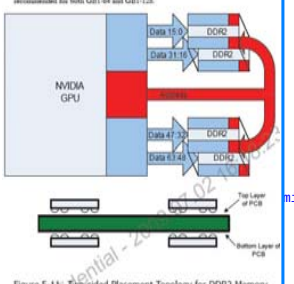

Figure 5-11. Two-sided Placement Topology for DDR2 Memory, Single Rank

Pins	Mapping Mode A	Pins	Mapping Mode A
FBx_CMD	CS0/CS1	FBx_CMD15	RAS
FBx_CMD0	A3[1] (low)	FBx_CMD16	A11
FBx_CMD1	A0	FBx_CMD17	A10
FBx_CMD2	A2 (low)	FBx_CMD18	BA1
FBx_CMD3	A1	FBx_CMD19	A8
FBx_CMD4	A3 (high)	FBx_CMD20	A9
FBx_CMD5	A4 (high)	FBx_CMD21	A6
FBx_CMD6	A5 (high)	FBx_CMD22	A5 (low)
FBx_CMD7	CS1/BA2	FBx_CMD23	A7
FBx_CMD8	CS0	FBx_CMD24	A4 (low)
FBx_CMD9	WE	FBx_CMD25	CAS
FBx_CMD10	BA0	FBx_CMD26	A13
FBx_CMD11	CKE	FBx_CMD27	BA2
FBx_CMD12	RST/ODT	FBx_CMD28	RFU0
FBx_CMD13	A2 (high)	FBx_CMD29	RFU1
FBx_CMD14	A12	FBx_CMD30	RFU2

T7704, T7703

R7713 10KOhm, R7710 10KOhm

R7704 475Ohm, R7705 475Ohm — Near VRAM

R7709 60.4Ohm 1% +1.8VS

T7701 TPC28t

25+25 mA

L7701 180Ohm/100Mhz +1.1VS

C7750 0.01UF/16V, C7701 0.1UF/16V, C7702 0.1UF/16V, C7703 1UF/6.3V

R7714 30.1Ohm 1%, R7708 36.5Ohm 1%, R7717 40.2Ohm 1% +1.8VS

NB9P-GE2

	FBVDDQ	FBCAL_PD_GND	FBCAL_PU_GND	FBCAL_thrm_GND
DDRII	1.8V	30.1 ohm	36.5 ohm	40.2 ohm

LOWER SUB-PARTITION TOP SIDE

U7701

mini-bus

+1.8VS

H5PS1G63EFR-S6

LOWER SUB-PARTITION BOT SIDE

orignal footprint:nb_bga_84p_31_512x394_share

U7702

mini-bus

+1.8VS

H5PS1G63EFR-S6

UPPER SUB-PARTITION BOT SIDE

U7703

mini-bus

+1.8VS

H5PS1G63EFR-S6

UPPER SUB-PARTITION TOP SIDE

U7704

mini-bus

+1.8VS

H5PS1G63EFR-S6

R7707 1KOhm 1% FBCVREF0, R7706 1KOhm 1% C7725 0.047UF/16V

R7712 1KOhm 1% FBCVREF1, R7711 1KOhm 1% C7724 0.047UF/16V

+1.8VS

C7728 0.1UF/10V, C7731 0.1UF/10V, C7704 0.1UF/10V, C7706 0.1UF/10V, C7739 4.7UF/6.3V, C7708 4.7UF/6.3V

C7732 1UF/6.3V, C7734 1UF/6.3V, C7719 1UF/6.3V, C7715 1UF/6.3V, C7714 1UF/6.3V, C7717 1UF/6.3V, C7736 1UF/6.3V, C7705 1UF/6.3V

PEGATRON COMPUTER INC

Title : F/B C GPU

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83Vf	1.1
	P/N <OrgAddr2>	

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IMON=Gm(IMON) * [(Vcsp1-Vcsn1) + (Vcsp2-Vcsn2)]

RIMON = 0.9V / [IMAX * Rsense(MIN) * Gm(IMON_MIN)]

Gm(IMON) = 2.4mS , Gm(IMON_MIN) = 2.36mS

AC_BAT_SYS

Close to Phase 1 Low_side MOSFET

RIMON

RFB

Tsw = 16.3pF * (RTON +6.5K)

OCP>54.45A
Ipp=9.185A
Fsw=300KHZ

(50A) +VCORE

DCR = 1m OHM

Close to Phase 1 Inductor

Close to Phase 2 Inductor

2009/06/22

2009/07/02

2009/07/03

09/02/13

RFB = Rdroop / (Rsense * Gm)

Gm = 600uS , R8022 for load lin

Variant Name	
Title	POWER_VCORE
OrgName	Engineer: Anysc
Size	Custom
Project Name	F83
Rev	1.0
Date	Thursday, July 16, 2009
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SKIP:
GND : DEM operation;
REF : Ultrasonic Mode operation;
VCC : PWM operation.

TON:(5V/3.3V)
VCC:(200kHz/250kHz)
REF:(300kHz/375kHz)
GND:(400kHz/500kHz)

VENLDO:
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

AC_BAT_SYS

<82,83,85,91,93> SUS#_PWR
09/04/17
R8123 0Ohm r0402_h16
SKIP#
R8105 0Ohm r0402_h16 @

2009/06/22
R8128 10Ohm
+5VAO
R8139 0Ohm @
C8115 1UF/6.3V MLCC/+/-10% @
R8126 100KOhm 5%
R8114 0Ohm
R8141 0Ohm @
C8113 1UF/6.3V MLCC/+/-10%
GND_17020
R8122 @ 0Ohm
R8117 0Ohm
C8112 MLCC/+/-10% 0.1UF/25V
R8146 @ 150KOhm
C8109 4.7UF/6.3V MLCC/+/-10%
C8109 0.22UF/10V
R8142 0Ohm
C8102 0.1UF/25V
C8117 10UF/25V_1206
Q8102 SI4134DY-T1-GE3

Iin=2.99A
C8118 10UF/25V_1206
C8105 0.1UF/25V MLCC/+/-10%
Q8100 SI4134DY-T1-GE3
Iin=2.78A

OCP>8.7A
4.966V~~~5.217V
Ipp=3.72A LIR=0.62
Fsw=300KHZ

OCP>7.9A
3.285V~~~3.375V
Ipp=2.2A LIR=0.37
Fsw=375KHZ

+5VO
(Max:5.68A)
+5VSUS
(0.31A)
JP8100 @
1MM_OPEN_5MIL
(5.99A)
DCR:Typ=28mOhm;Max=30mOhm
L8100 3.3UH Irat=6A
40mil
10mil
Separate
R8125 330KOHM
SUS_PWRGD
ENBL
U8100A
BYP VOUT1 FB1 ILIM1 PGOOD1 EN1 UGATE1 PHASE1
GND2 FB2 ILIM2 VOUT2 SKIP# PGOOD2 EN2 UGATE2 PHASE2
NC2 LDO NC3 NC1 ENLDO TON REF
BOOT1 UGATE1 LGATE1 SECFB GND1 PGND LGATE2 BOOT2
+3VO_FB
R8124 330KOHM
SKIP#
R8113 0Ohm
+5VAO
GND_17020
OCP Set
C8110 0.1UF/25V MLCC/+/-10%
RT8206AGQW
R8120 0Ohm
R8119 0Ohm
C8111 MLCC/+/-10% 0.1UF/25V
DL1
(5V:300kHz)
(3.3V:375kHz)
Q8101 SI4134DY-T1-GE3
Q8103 SI4134DY-T1-GE3
R8115 2.2Ohm 5% r1206
C8125 1500PF/50V MLCC/+/-10%
R8116 2.2Ohm 5% r1206 @
C8126 1500PF/50V MLCC/+/-10% @
JP8104 SHORT_PIN

2009/06/18
2009/06/22
2009/06/18
2009/06/18
2009/06/22
C8103 150UF/16V ESR=30mOHM/1400mA
C8100 1UF/10V
C8104 1UF/10V
CE8101 100UF/6.3V ESR=30mOHM/1400mA
JP8105 SHORT_PIN
JP8109 SHORT_PIN

(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)
(Typ: Rdson = 14.5m OHM)
(Max: Rdson = 17.5m OHM)
FB1=2V(T=1.25%)

L8101 3.3UH Irat=6A
(6.432A)
+3VO
(MAX:5.712A)
JP8101 @
1MM_OPEN_5MIL
+3VA
(0.22A)

JP8108 @
1MM_OPEN_5MIL
+5VAO
+5VA
C8134 39PF/50V @
C8136 0.1UF/25V @
R8108 30.9KOhm 1%
R8109 20KOhm 1%
C8114 1UF/6.3V MLCC/+/-10%
C8137 39PF/50V @
SECFB
R8127 200KOhm
+15VO
*SECFB:2V(T=4%)
R8132 39KOHM
JP8110
SHORT_PIN
<22,30,92> SUS_PWRGD
<91> 5VO_ENBL
U8100B GND3 GND4 GND5 GND6 RT8206AGQW
R8112 13.3KOhm 1%
C8135 39PF/50V
C8138 0.1UF/25V @
R8111 20KOhm 1% @
09/05/18

2009/07/02

+12VSUS
+5VO
D8104 BAT54S
C8121 0.1UF/25V MLCC/+/-10%
2009/06/22
20mil
DL1
C8120 0.1UF/25V MLCC/+/-10%
2009/06/22
C8122 1UF/25V MLCC/+/-10% @
+10VO
C8123 1UF/25V MLCC/+/-10%
(Max:0.02A)
D8103 BAT54S
+15VO
JP8106 @
1MM_OPEN_5MIL
+12VSUS
C8124 1UF/25V MLCC/+/-10%
VOUT:Typ.=12.256V;Max.=12.962V;Min.=11.571V;T=5.76%

TPC26TPC26TPC26TPC26TPC26
+5VO TB110 TB103 TB114 TB120
+5VSUS TB134 TB132 TB135 TB121
+3VO TB117 TB107 TB109 TB122
TB104 TB108 TB116 TB126
TB112 TB119 TB101 TB130

TOTAL COUNT : 38 PCS

<Variant Name>
Title : POWER_SYSTEM
<OrgName>
Engineer: Anysc
Size Custom
Project Name F83
Rev 1.0
Date: Thursday, July 16, 2009
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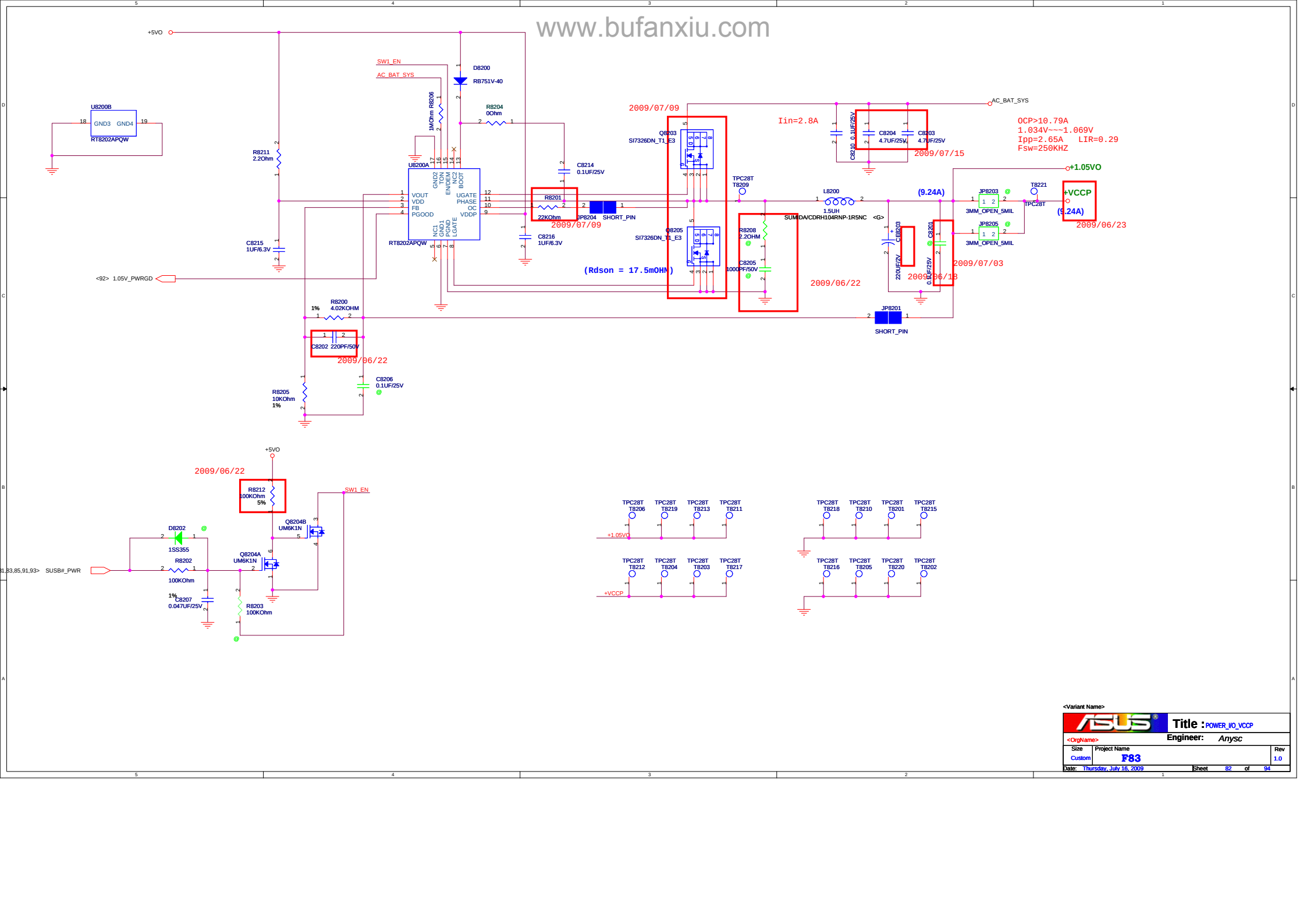

<Variant Name>

Title : POWER_I/O_VCCP

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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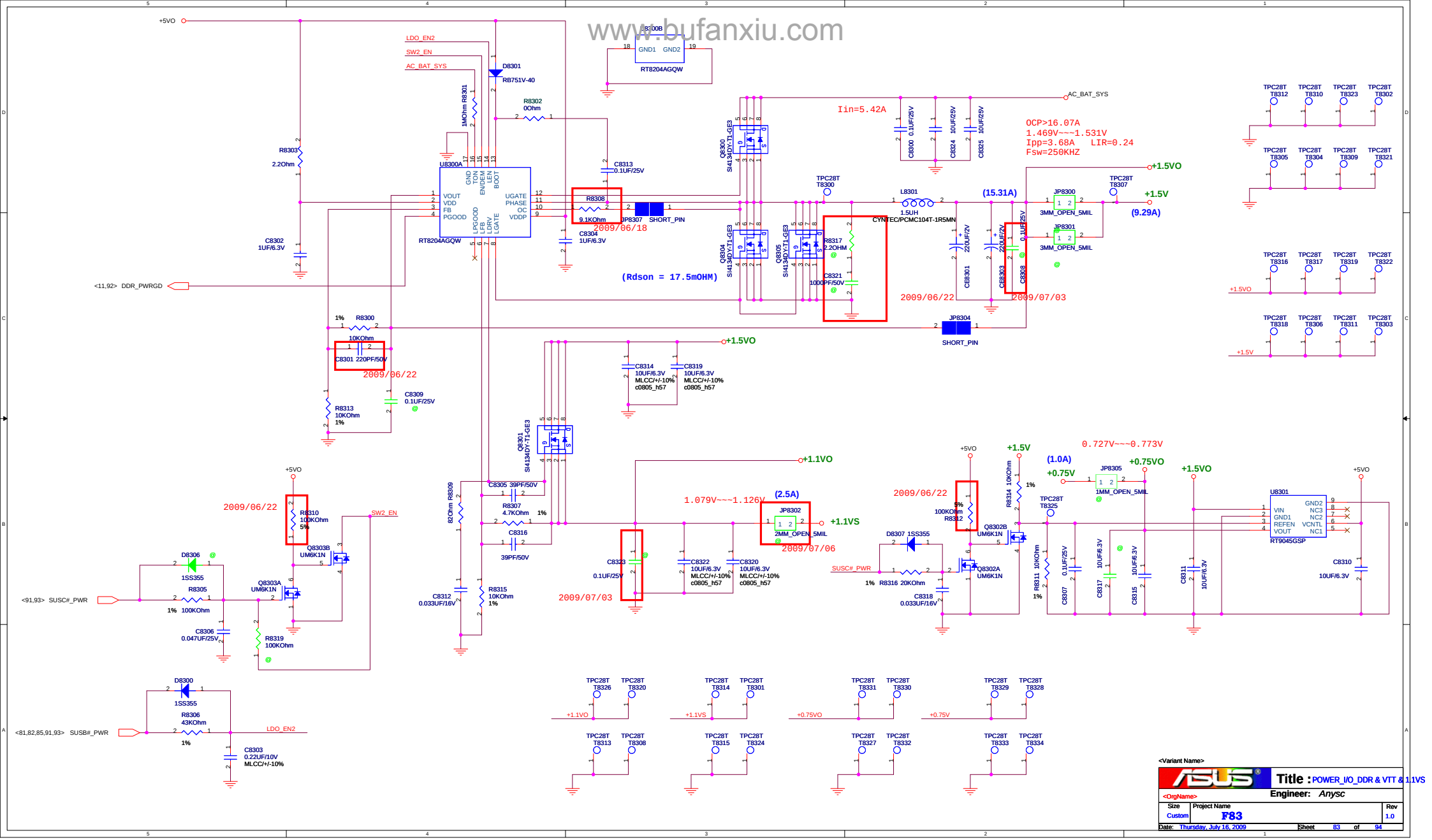
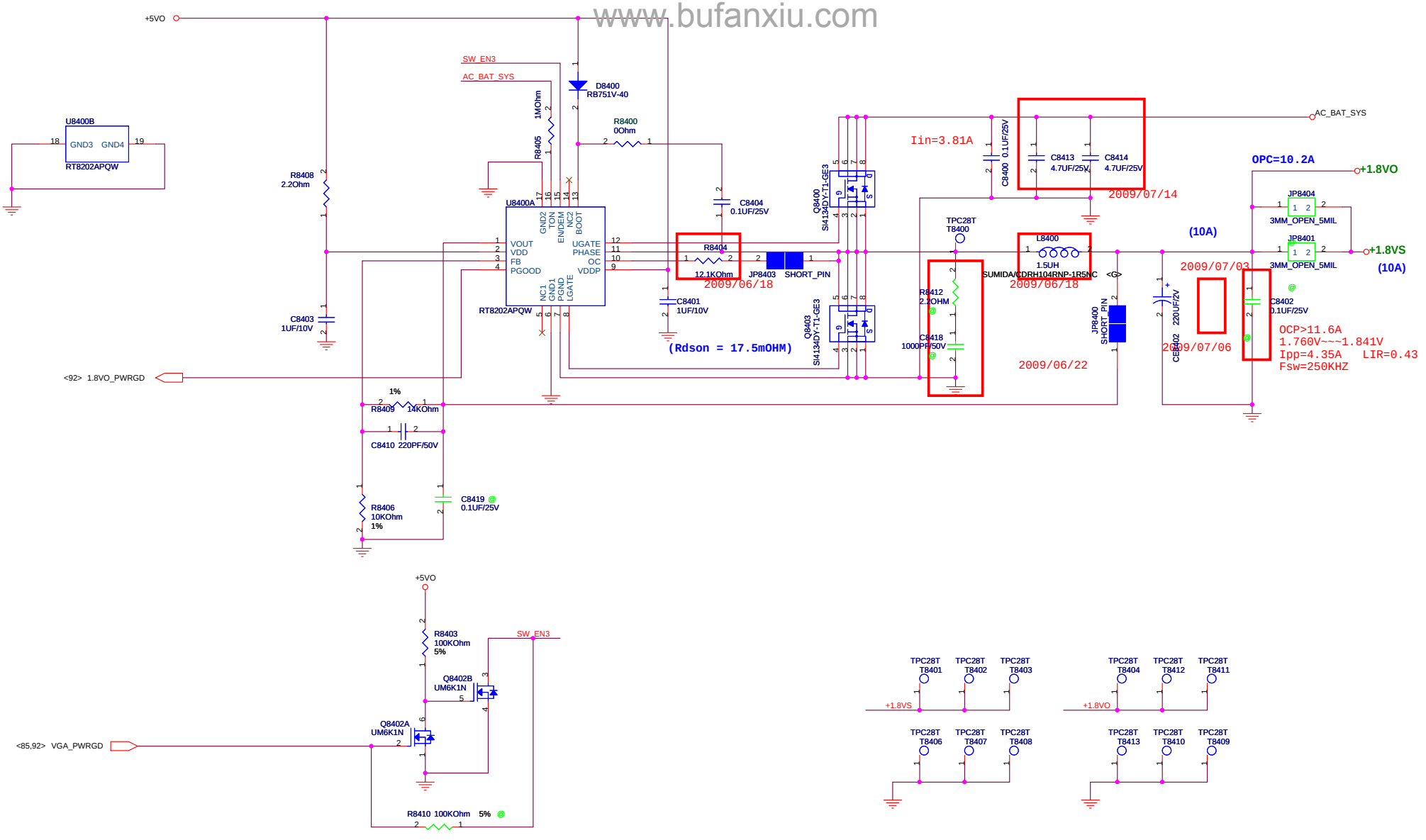
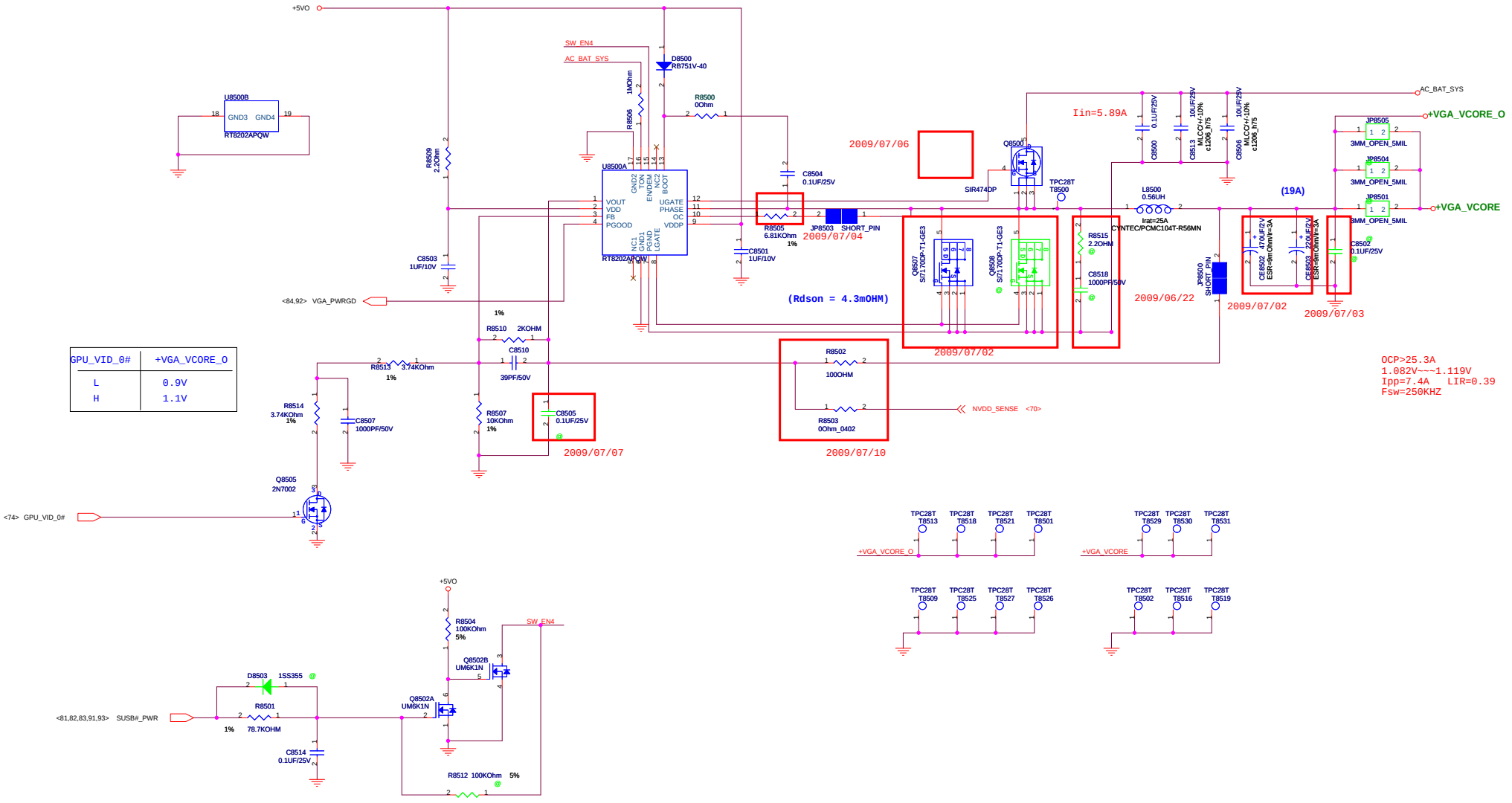




<Variant Name>

ASUS	Title : POWER_I/O_1.8VS	
<OrgName>	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
Date: Thursday, July 16, 2009	Sheet 84 of 94	



GPU_VID_0#	+VGA_VCORE_O
L	0.9V
H	1.1V

<Variant Name>

Title : POWER_VGA_VCORE

<OrgName> Engineer: Anysc

Size	Project Name	Rev
C	F83	1.0

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<Variant Name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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<Variant Name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
C	F83	1.0

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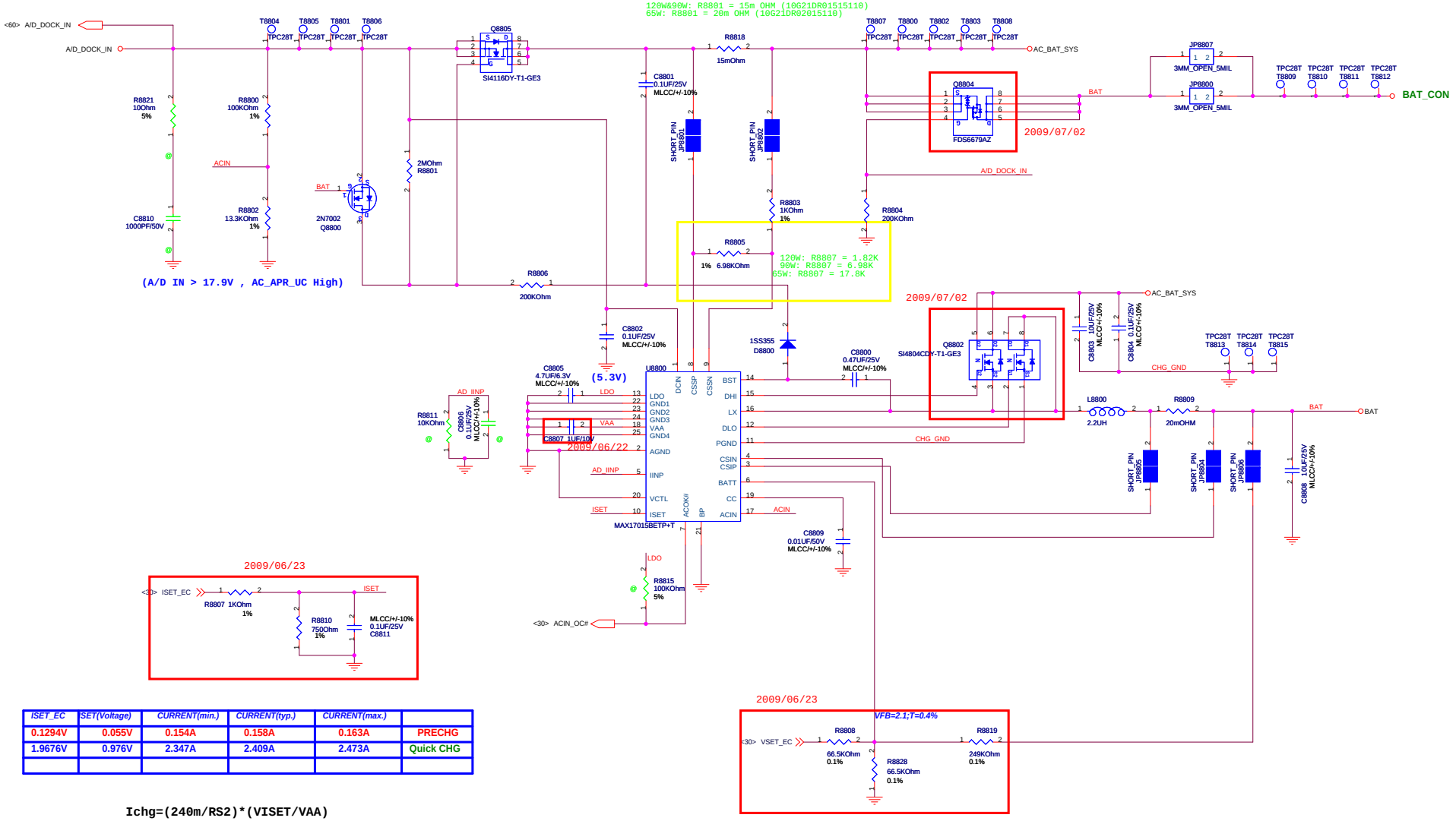

ISET_EC	ISET(Voltage)	CURRENT(min.)	CURRENT(typ.)	CURRENT(max.)	
0.1294V	0.055V	0.154A	0.158A	0.163A	PRECHG
1.9676V	0.976V	2.347A	2.409A	2.473A	Quick CHG

Ichg=(240m/RS2)*(VISET/VAA)
Ichg=(240m/20m)*(0.055/4.2)=0.157A
Ichg=(240m/20m)*(0.865/4.2)=2.4714A

VCTL connect to GND,VFB=2.1V
VBAT=2.1*(R8819+R8828)/R8828

VSET_EC	BAT(min.)	BAT(typ.)	BAT(max.)
1.3948V	12.511V	12.604V	12.696V

12.641V(min)<VBAT-12.515(Typ)<12.768V(Max)

<Variant Name>

Title : POWER_CHARGER
<OrgName> Engineer: Anysc
Size C | Project Name F83 | Rev 1.0
Date: Thursday, July 16, 2009 | Sheet 88 of 94

<Variant Name>

Title : N/A

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

Date: Thursday, July 16, 2009 Sheet 89 of 94

BATTERY IN DETECT

2009/07/08
delete batt detect

<Variant Name>

Title : POWER_DETECT

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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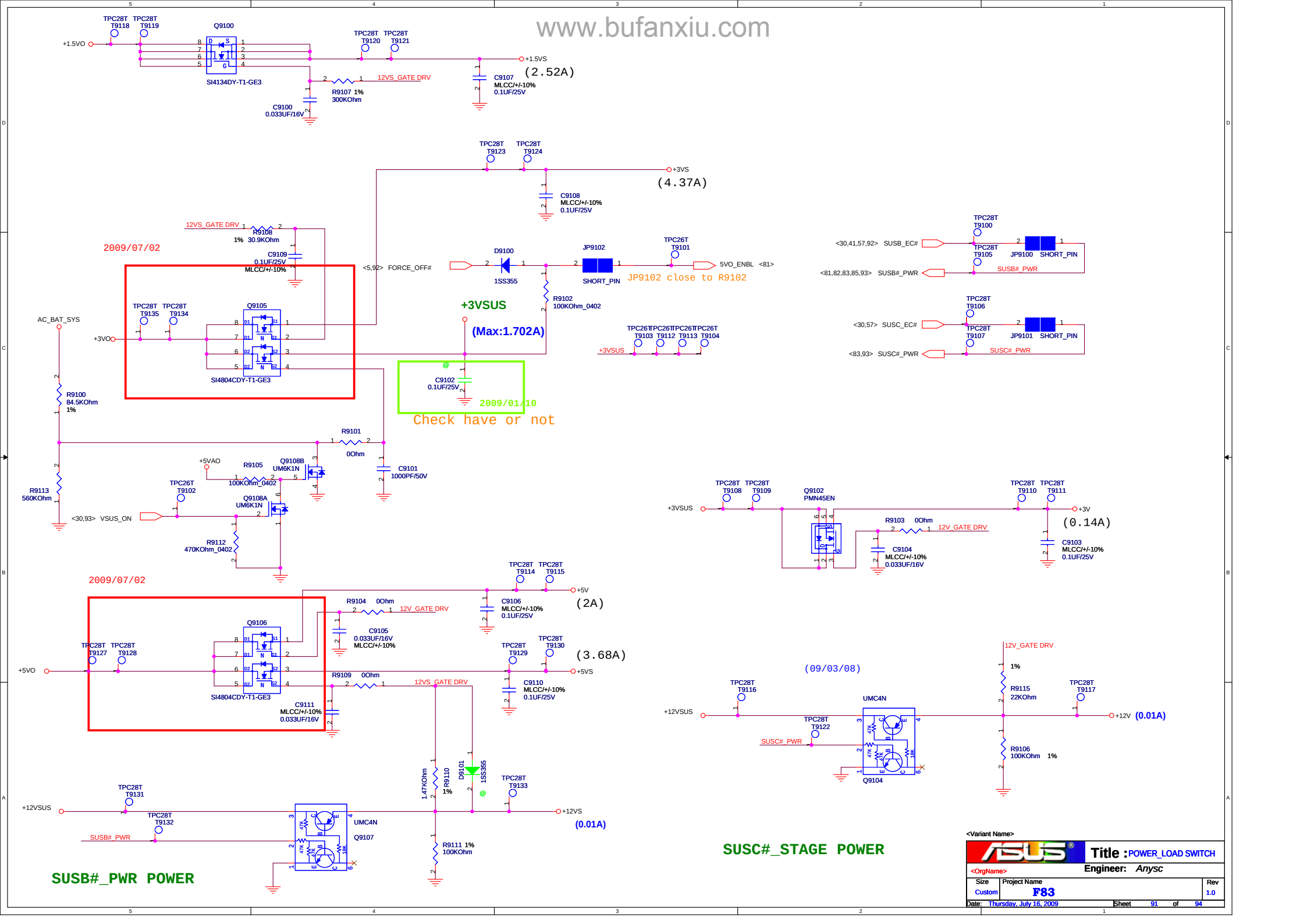

<Variant Name>

Title : POWER_LOAD SWITCH

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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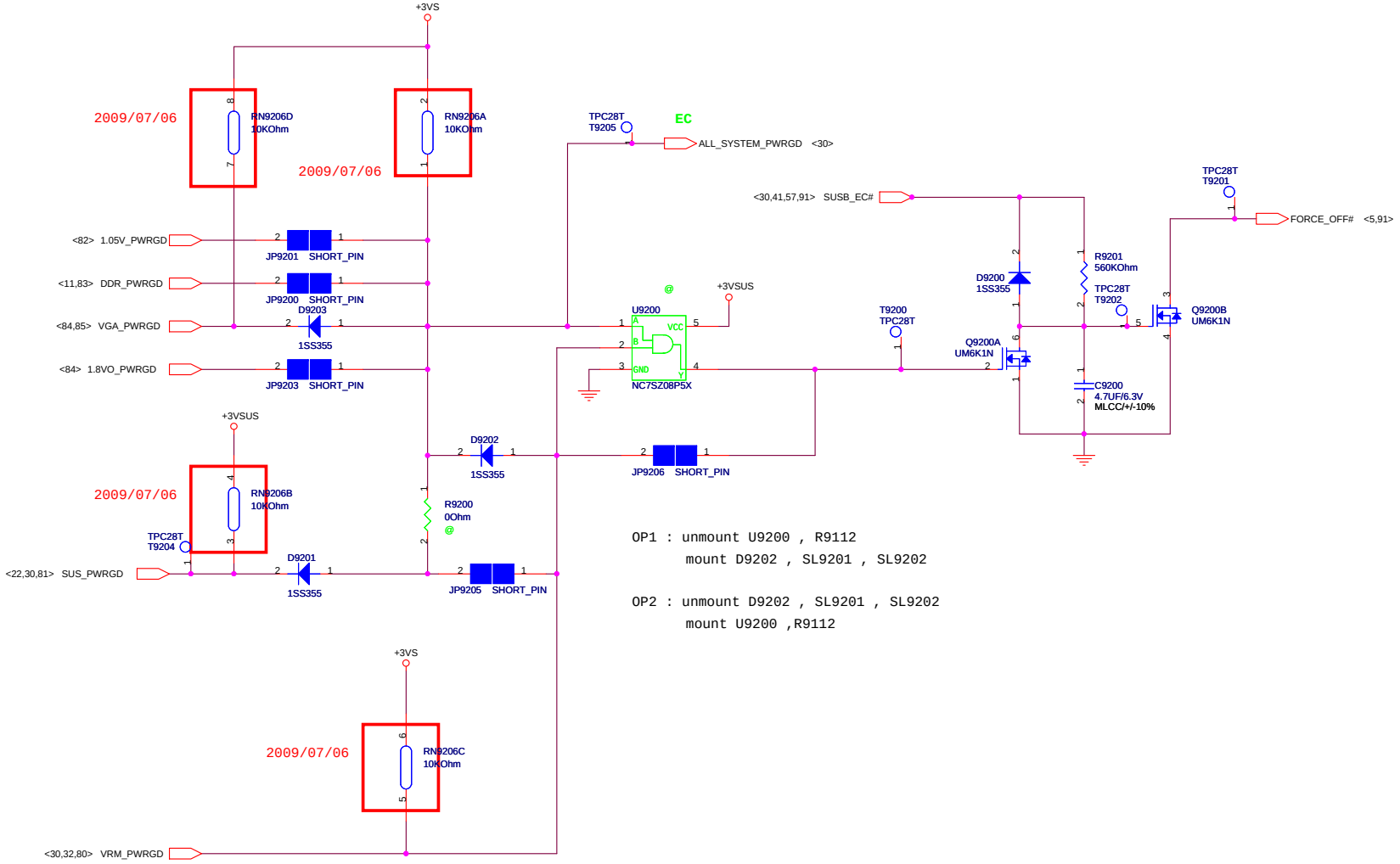
POWER GOOD DETECTER



OP1 : unmount U9200 , R9112
mount D9202 , SL9201 , SL9202

OP2 : unmount D9202 , SL9201 , SL9202
mount U9200 ,R9112

<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
Date: Thursday, July 16, 2009	Sheet 92 of 94	

FOR POWER TEST

+3VA → +3VA <20,22,30,45,57,60,81>

+3VSUS → +3VSUS <20,21,22,23,24,30,33,37,45,53,56,91,92>
+5VSUS → +5VSUS <23,56,81>
+12VSUS → +12VSUS <24,81,91>

+5VO → +5VO <81,82,83,84,85,91>
+3VO → +3VO <81,91>
+1.05VO → +1.05VO <82>
+1.5VO → +1.5VO <83,91>
+0.75VO → +0.75VO <83>
+1.8VO → +1.8VO <84>
+1.1VO → +1.1VO <83>
+VGA_VCORE_O → +VGA_VCORE_O <85>

+3V → +3V <21,33,41,44,53,57,61,63,91>
+5V → +5V <9,31,44,45,52,57,91>
+12V → +12V <37,91>
+1.5V → +1.5V <7,8,9,11,13,14,57,83>

+3VS → +3VS <3,7,8,11,14,15,22,23,24,29,30,32,36,40,41,44,45,46,48,50,51,53,56,57,70,72,74,80,91,92>
+12VS → +12VS <24,40,45,48,57,91>
+5VS → +5VS <23,31,36,46,48,50,51,56,57,80,91>
+1.8VS → +1.8VS <57,73,76,77,84>
+1.5VS → +1.5VS <4,14,23,41,53,57,91>
+VCCP → +VCCP <3,4,5,10,11,13,14,20,23,29,57,82>
+0.75V → +0.75V <7,8,11,83>
+1.1VS → +1.1VS <57,70,72,73,76,77,83>
+VGA_VCORE → +VGA_VCORE <75,85>
+VCORE → +VCORE <4,5,80>

AC_BAT_SYS → AC_BAT_SYS <45,80,81,82,83,84,85,88,91>
BAT → BAT <88>
BAT_CON → BAT_CON <60,88>

+3VO → JP9300 (@) 1 | 1 2 | 2 → CPU_VRON_PWR <80>
SGL_JUMP

+3VO → JP9301 (@) 1 | 1 2 | 2 → SUSB#_PWR → SUSB#_PWR <81,82,83,85,91>
SGL_JUMP

+3VO → JP9302 (@) 1 | 1 2 | 2 → SUSC#_PWR → SUSC#_PWR <83,91>
SGL_JUMP

+3VO → JP9303 (@) 1 | 1 2 | 2 → VSUS_ON <30,91>
SGL_JUMP

<Variant Name>

<OrgName>	Title : POWER_SIGNAL	
	Engineer: Anysc	
Size: Custom	Project Name: F83	Rev: 1.0
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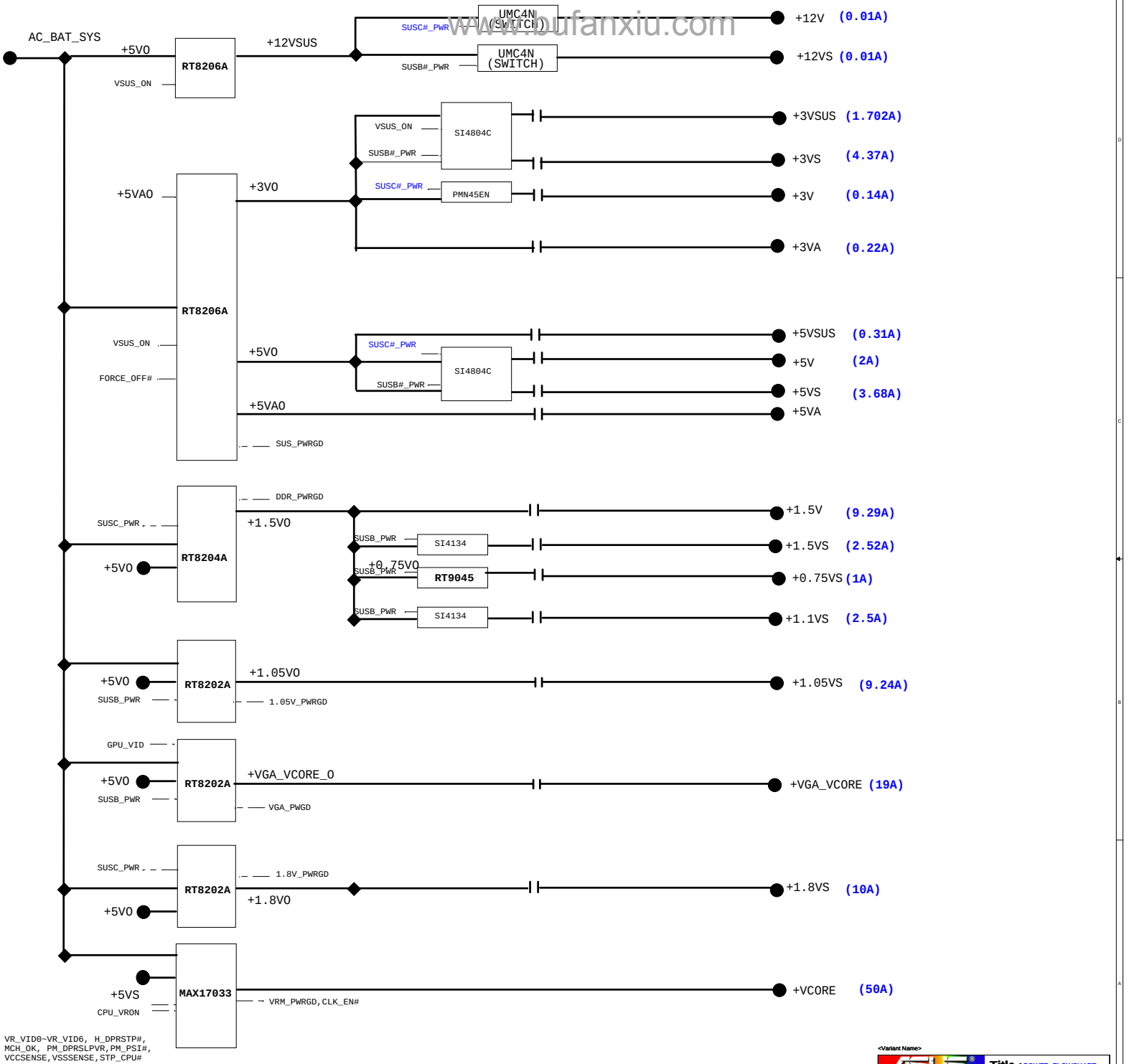

<Variant Name>

ASUS

Title : POWER_FLOWCHART

<OrgName>

Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0

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PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Colin Chang		
Size: C	Project Name: VX5		Rev: 1.0
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 98 of 100		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Colin Chang		
Size: C	Project Name: VX5		Rev: 1.0
	P/N: <OrgAddr2>		
Date: Thursday, July 16, 2009	Sheet 99 of 100		