RTC_BTY

BATT

PART for BOM only

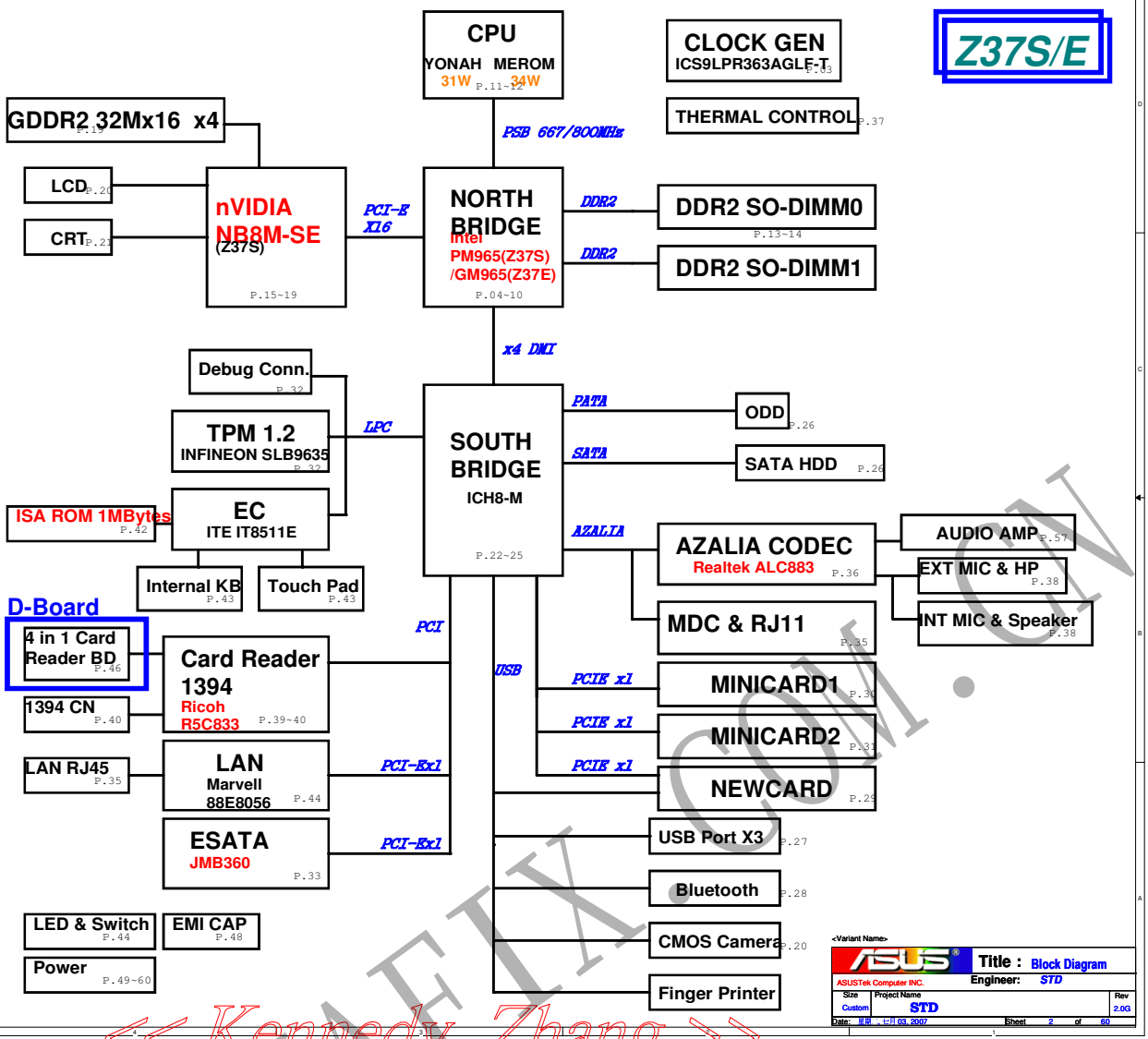
Function	ASUS Partnumber	LOCATION
RTC BTY	07G016412032	
GPU NB8M	02G190012900	

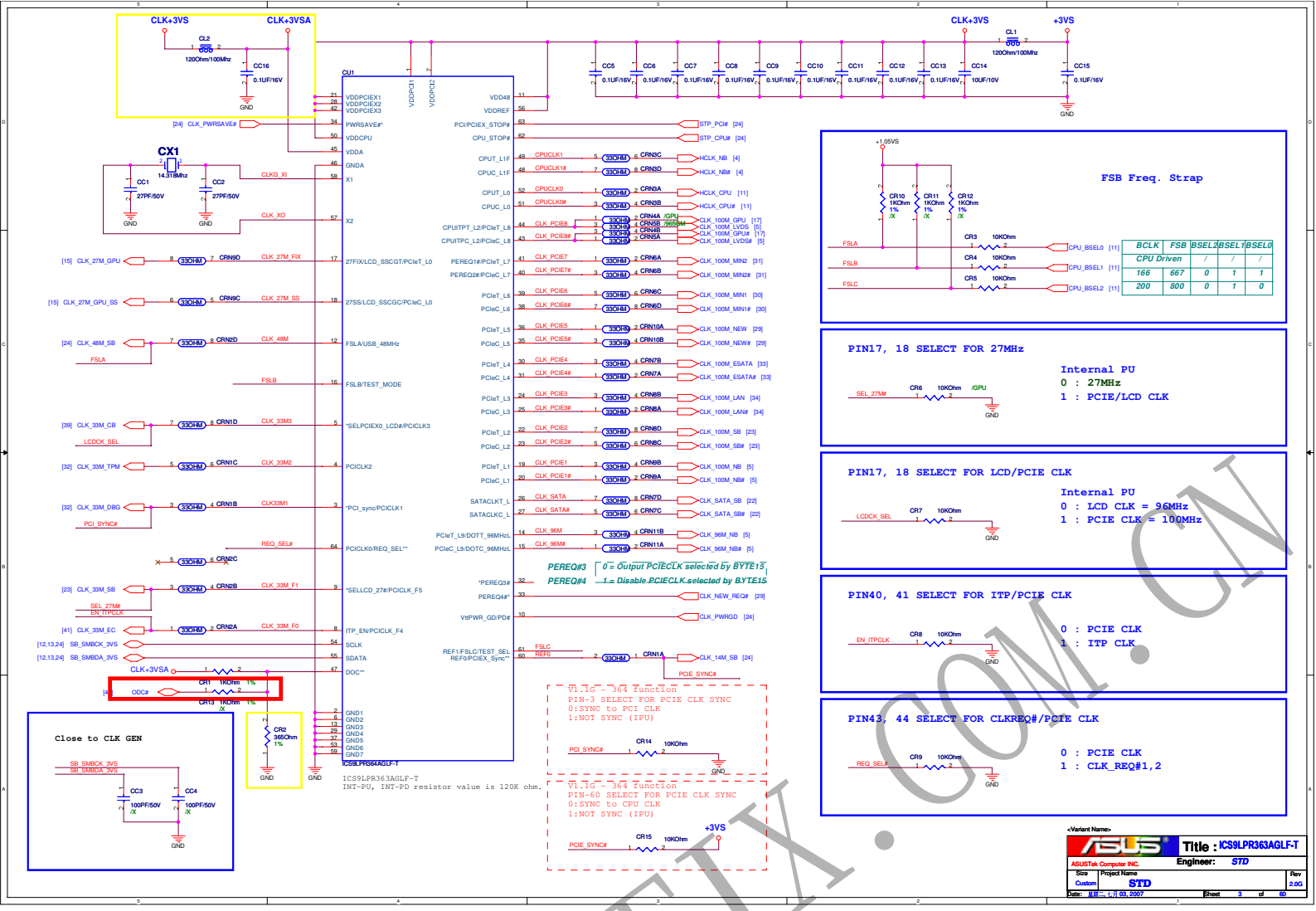
Temp Modify

1012: Delete EC23,31,32,34,39 already have in location
Delete EC35,36 No space to add
Delete GC114,115,120,121,122,123,116,117,118,119 No space to add

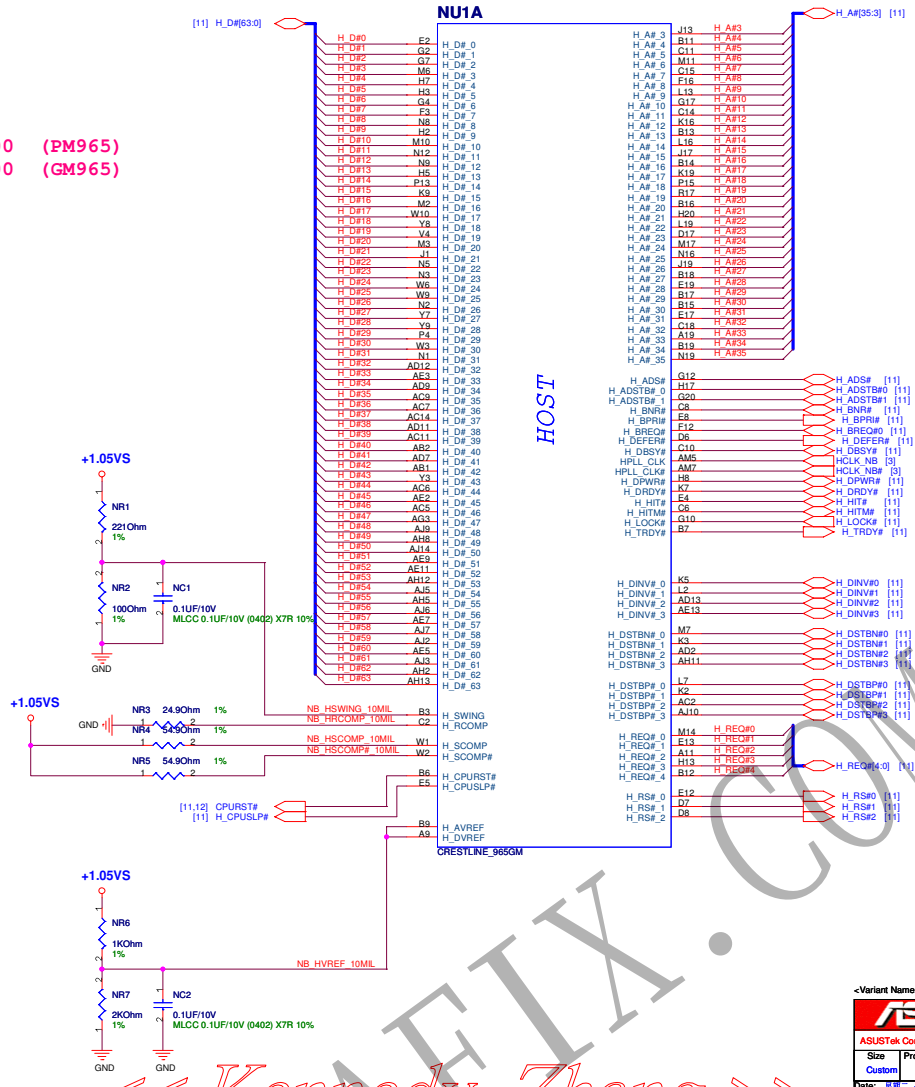
<Variant Name>

Title	Revision	
Size A3	Document Number STD	Rev 2.0G
Date: 星期二, 十月 03, 2007	Sheet 1 of 60	





Z37S:02G010017200 (PM965)
Z37E:02G010017300 (GM965)
V2.0G



<Variant Name>

ASUSTek Computer INC.

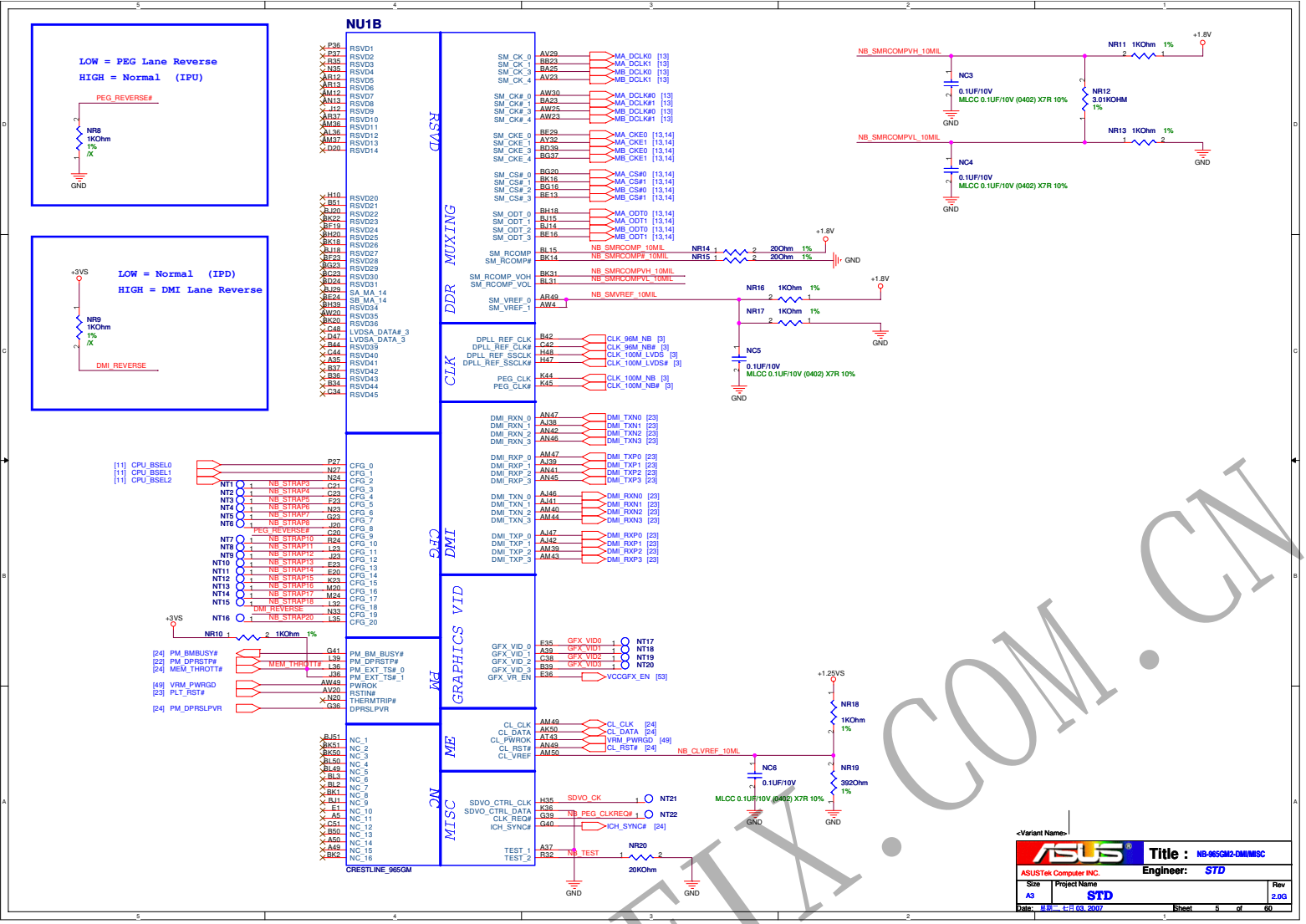
Title :NB-965GM1-FSB

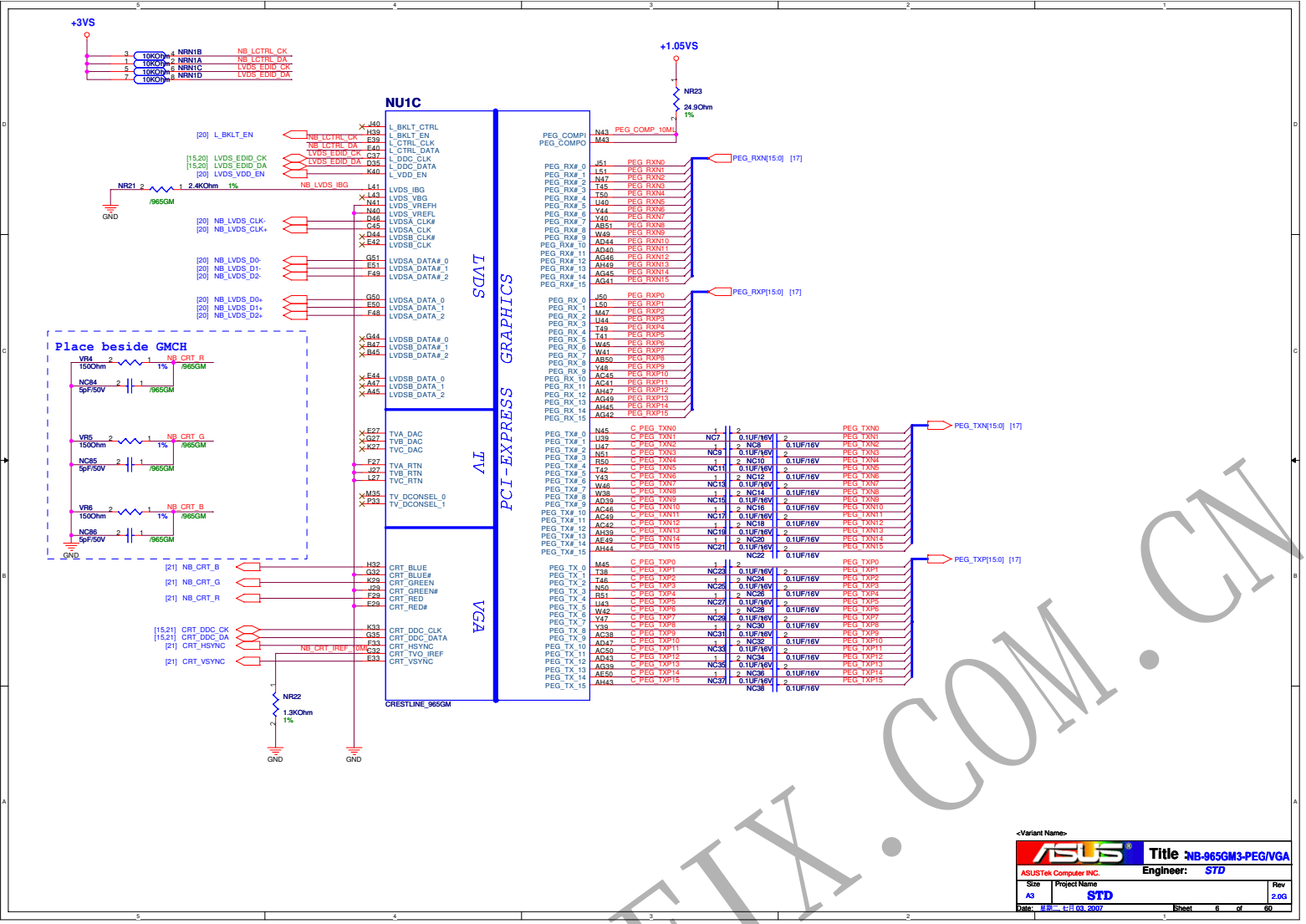
Engineer: STD

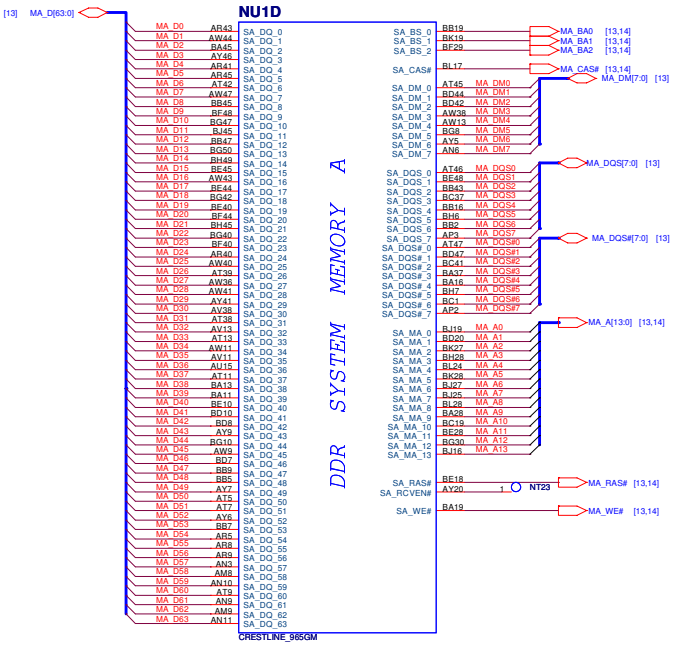
Size	Project Name	Rev
Custom	STD	2.0G

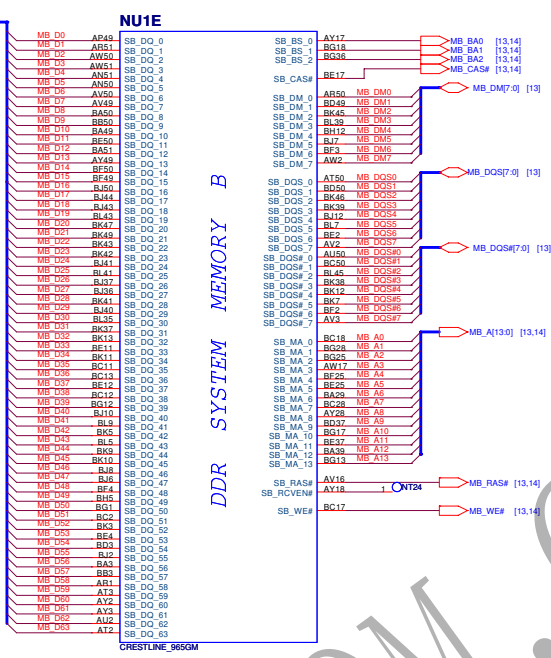
Date: 星期二, 七月 03, 2007 Sheet 4 of 60

<< Kennedy_Zhang >>









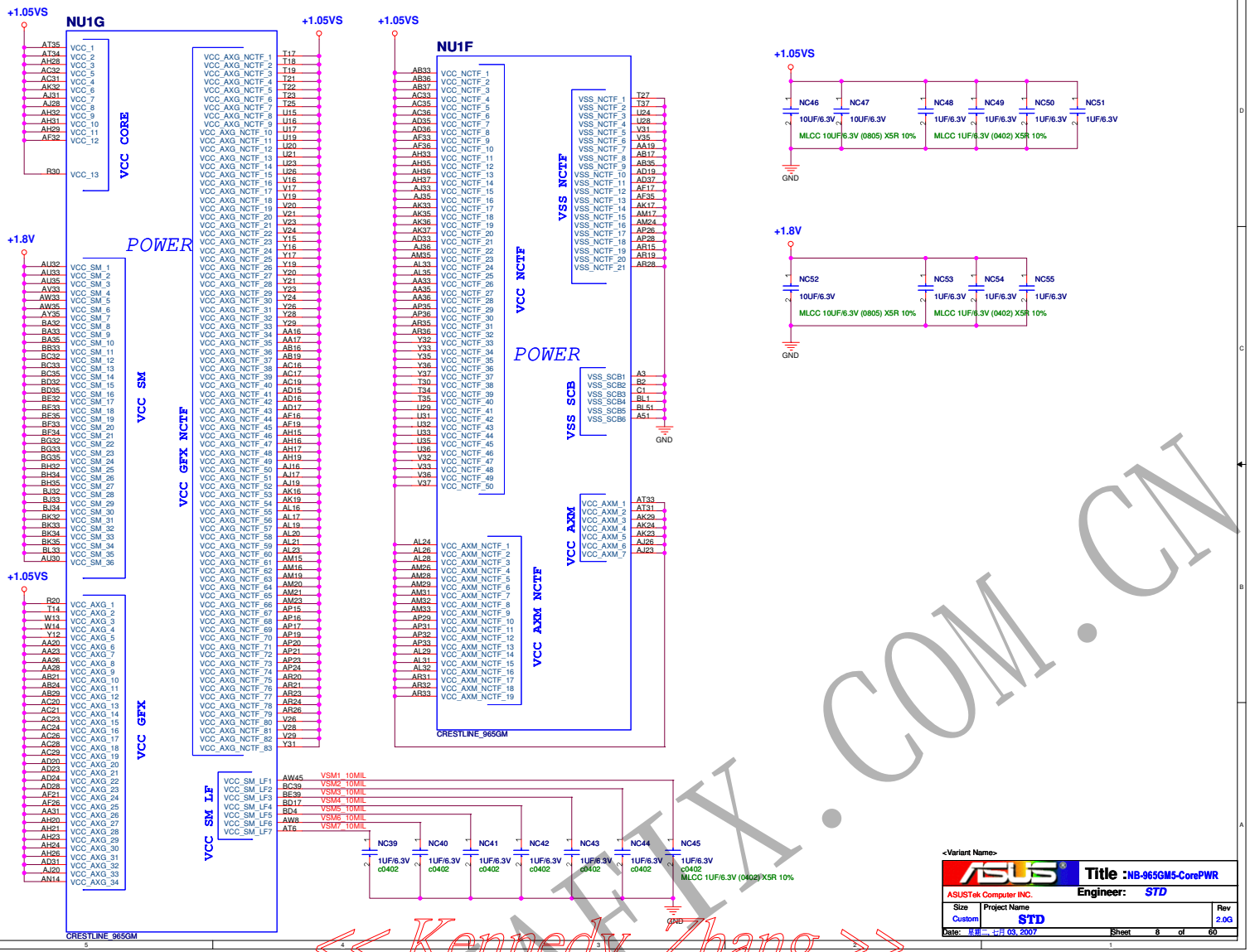
<Variant Name>

Title : NB-965GM4-DDR2

ASUSTek Computer INC. Engineer: STD

Size	Project Name	Rev
A3	STD	2.0G

Date: 星期一, 七月 03, 2007 Sheet 7 of 60



<Variant Name>

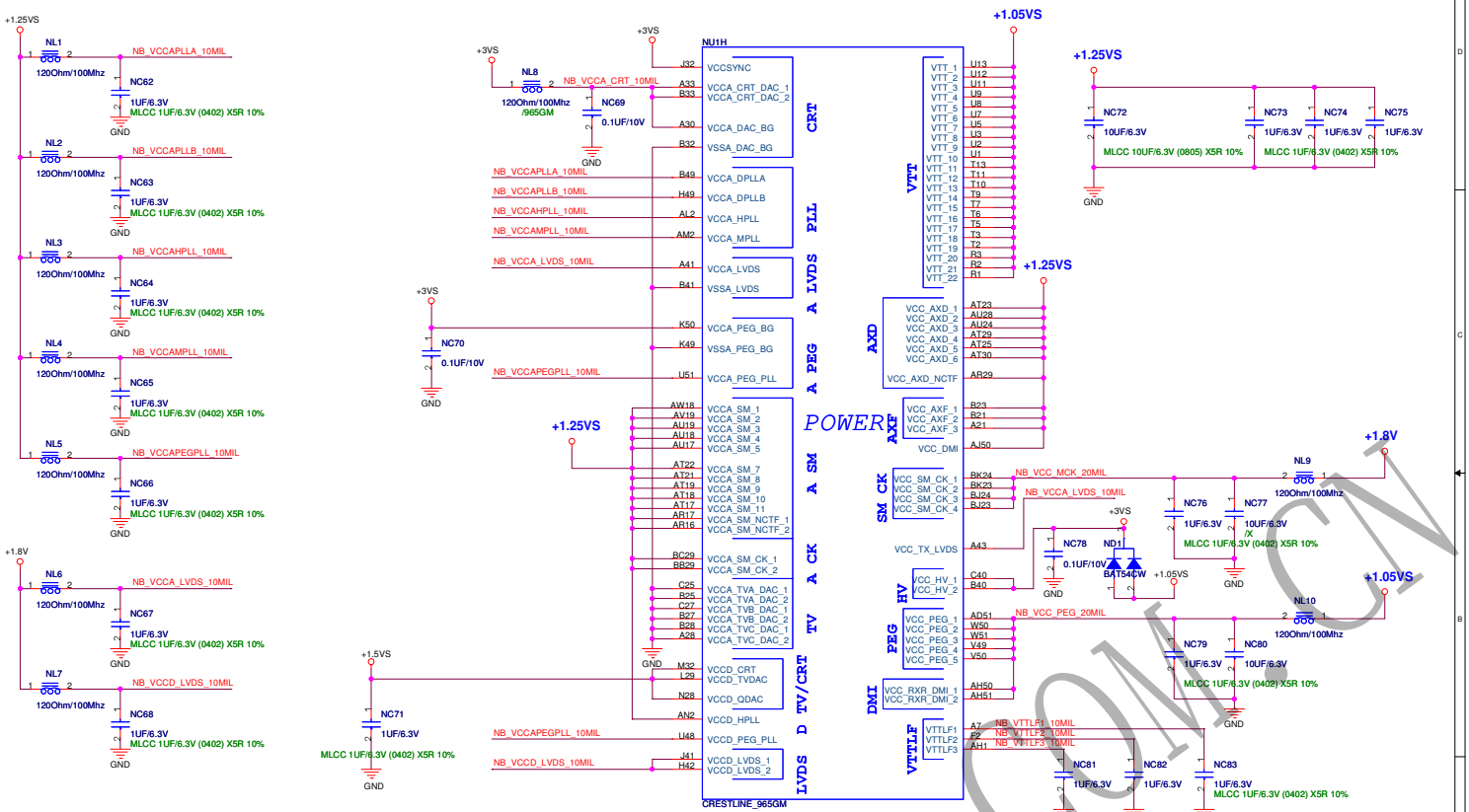
ASUSTek Computer INC.

Title : NB-965GM5-CorePWR

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 8 of 60



HIGH = CANES REVERSED

<Variant Name>

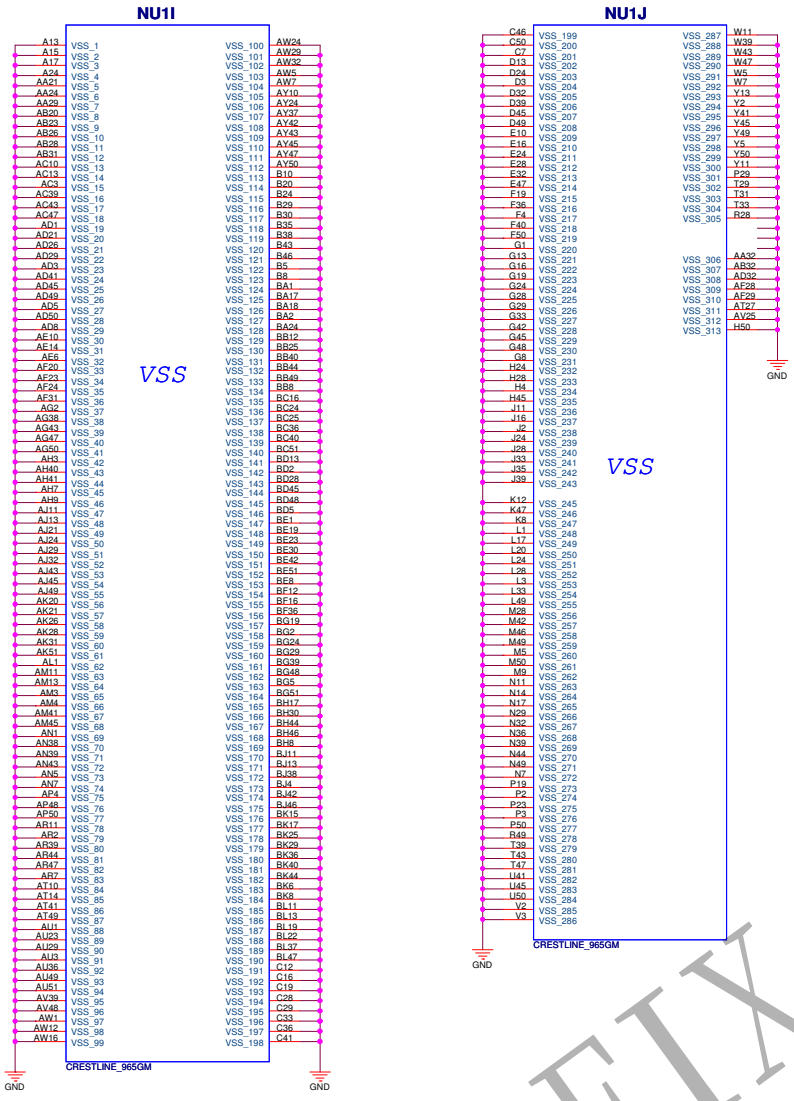
ASUSTek Computer INC.

Title : NB-965GM6-IOPWR

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 9 of 60



<Variant Name>

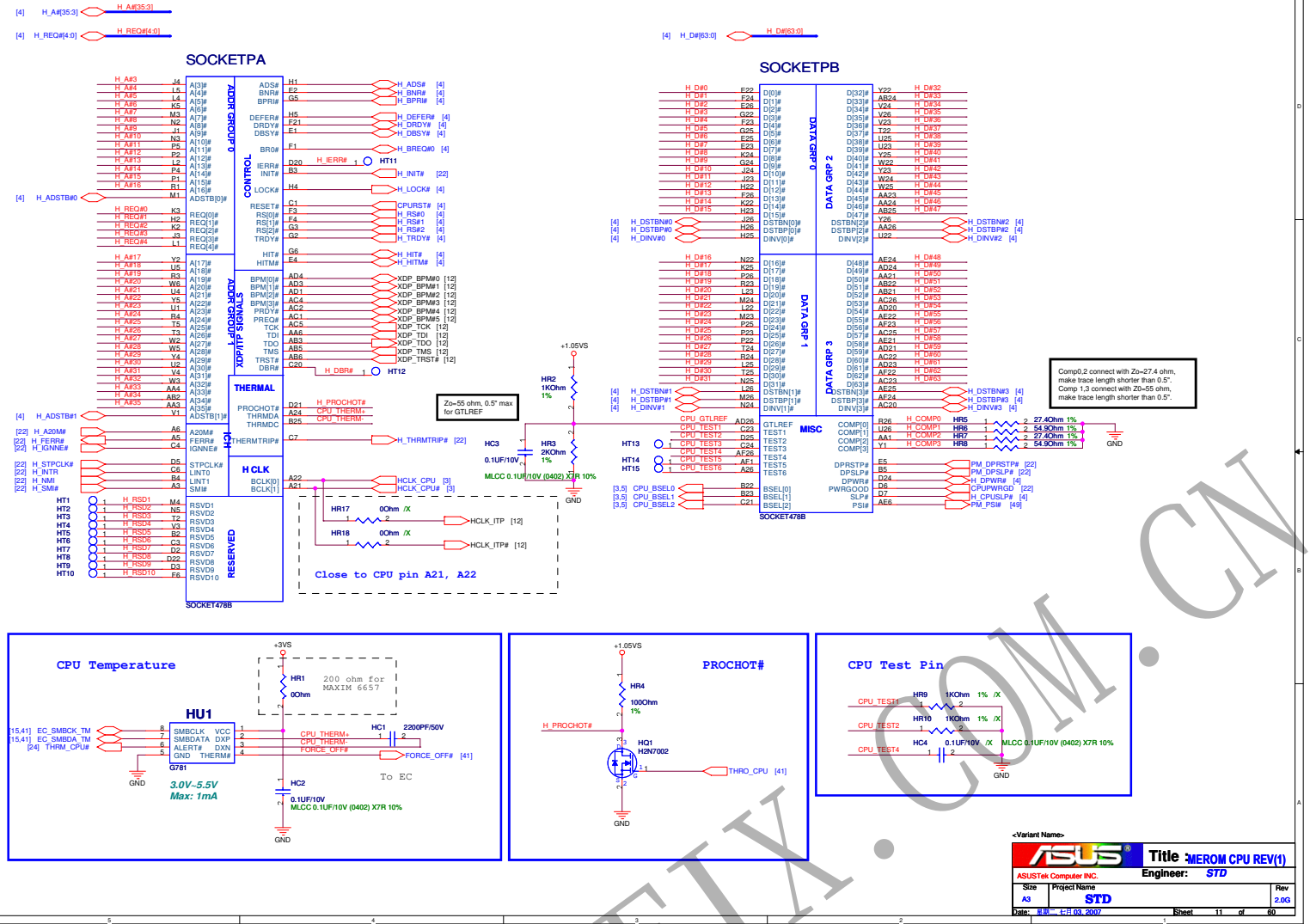
ASUSTek Computer INC.

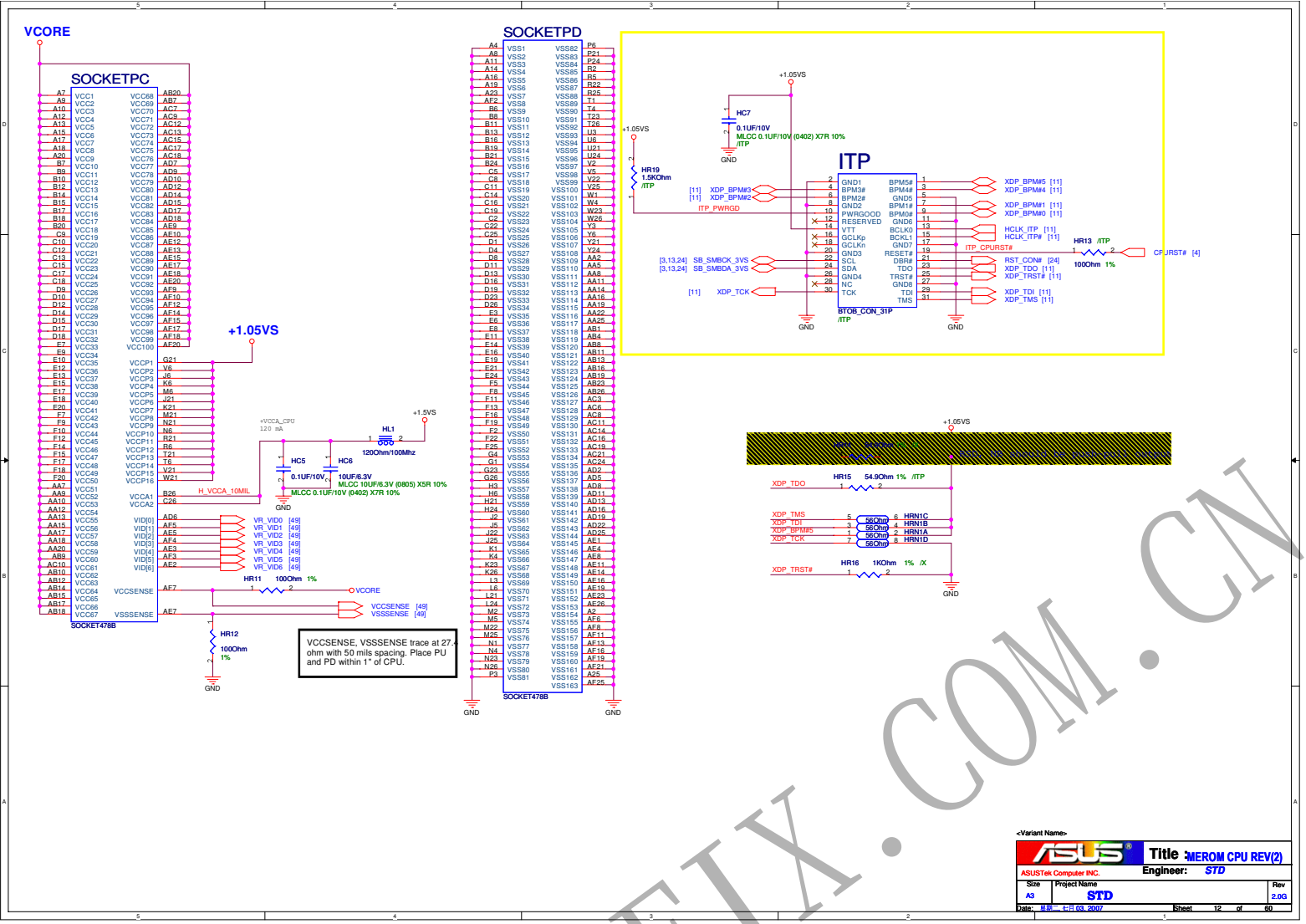
Title : NB-965GM7-GND

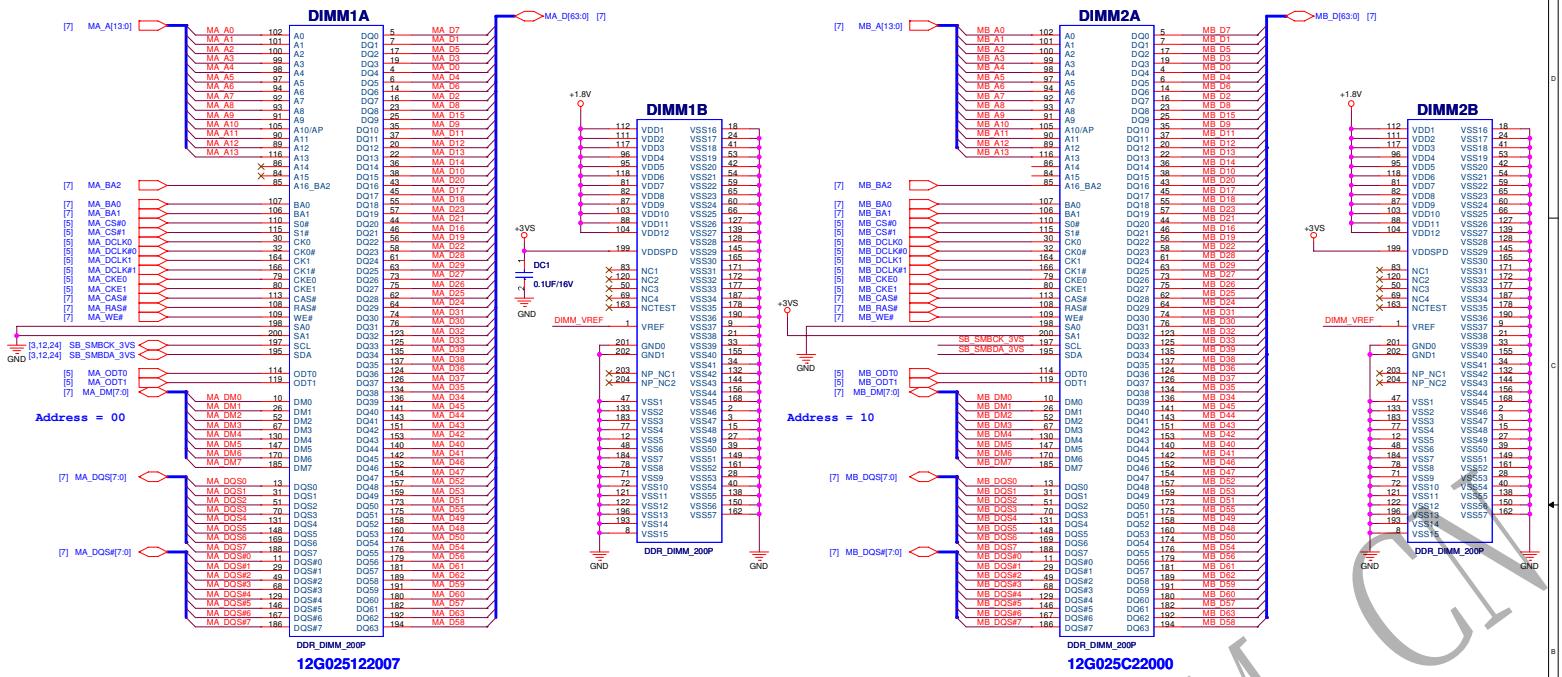
Engineer: STD

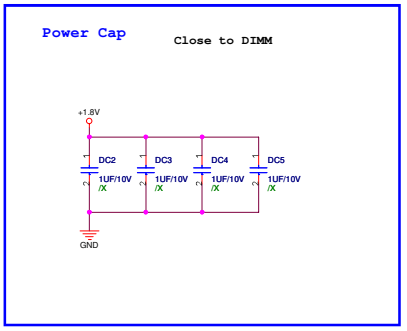
Size	Project Name	Rev
Custom	STD	2.0G

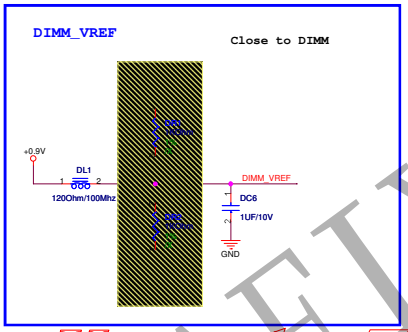
Date: 星期二, 七月 03, 2007 Sheet 10 of 60

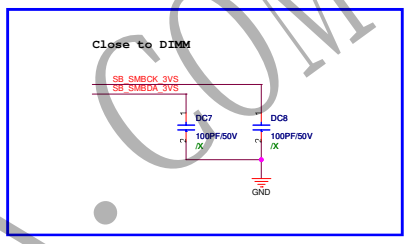


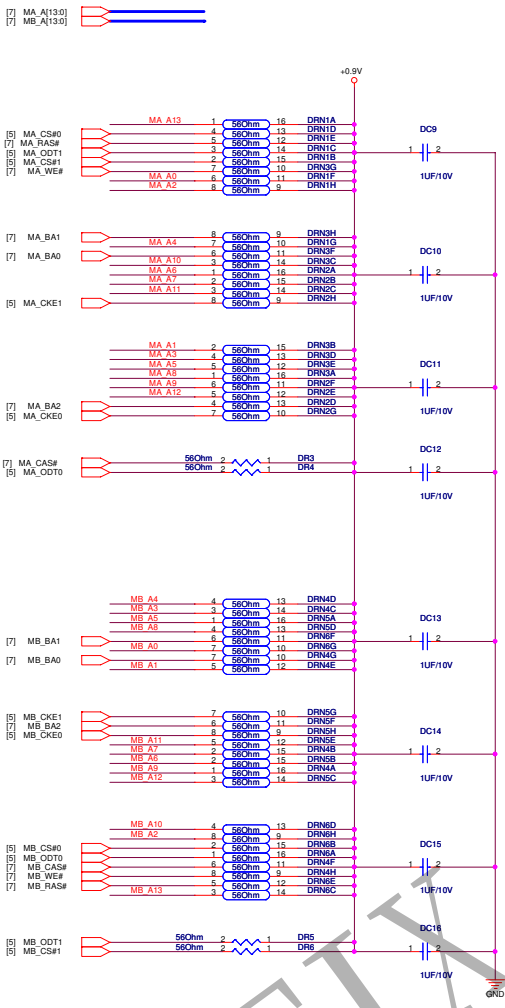












<Variant Name>

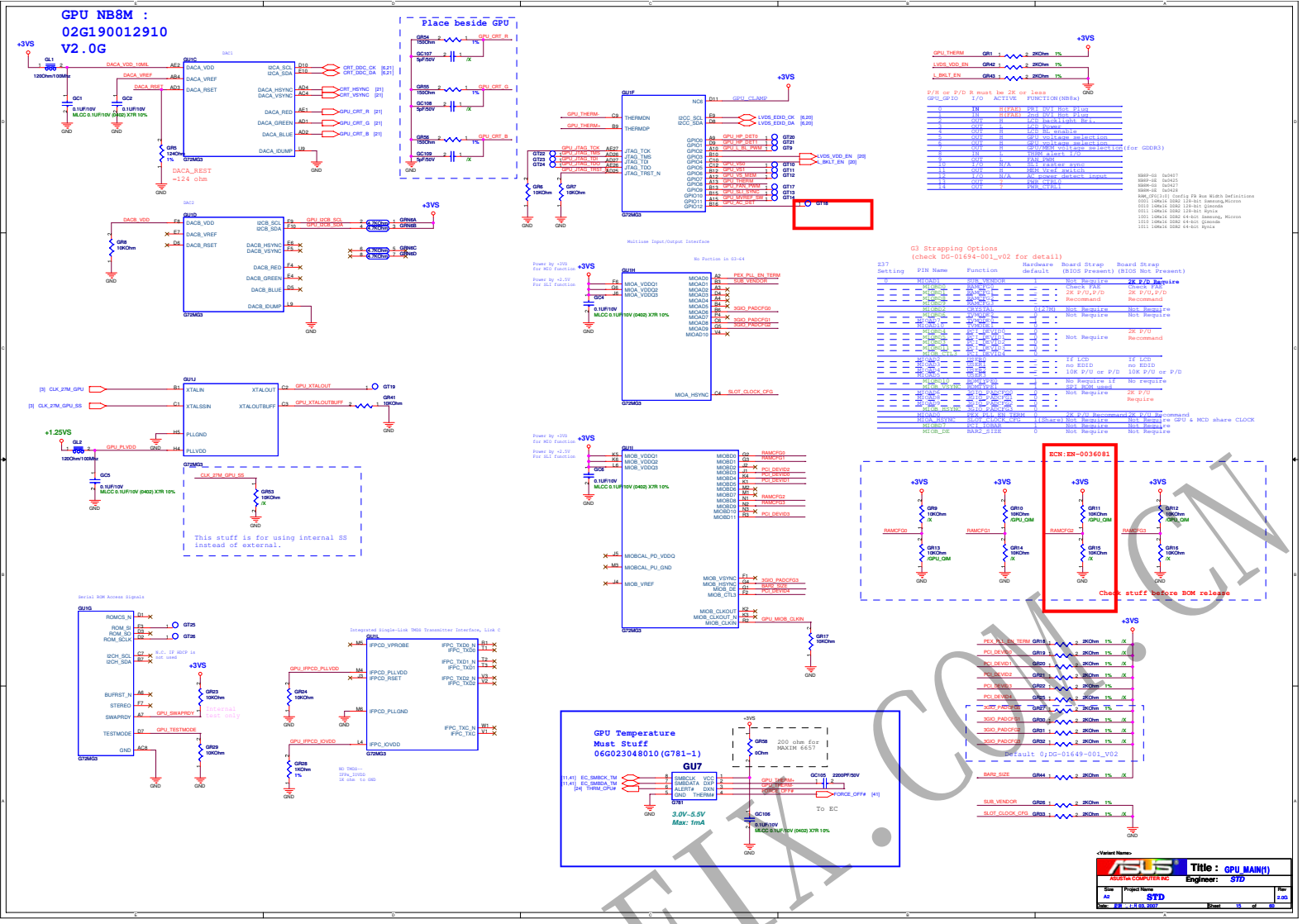
ASUSTek Computer INC.

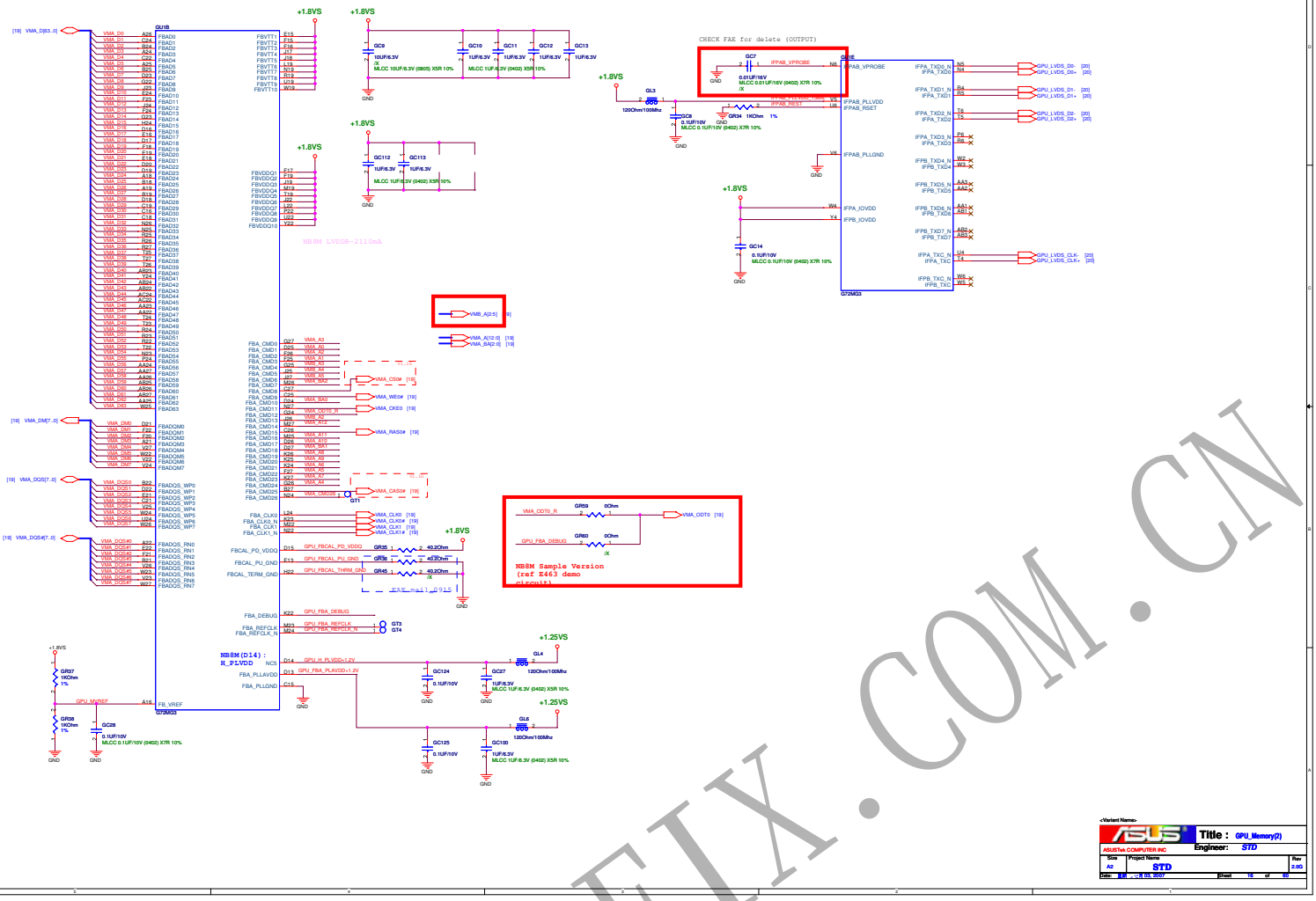
Title : DDR2 TERMINATION

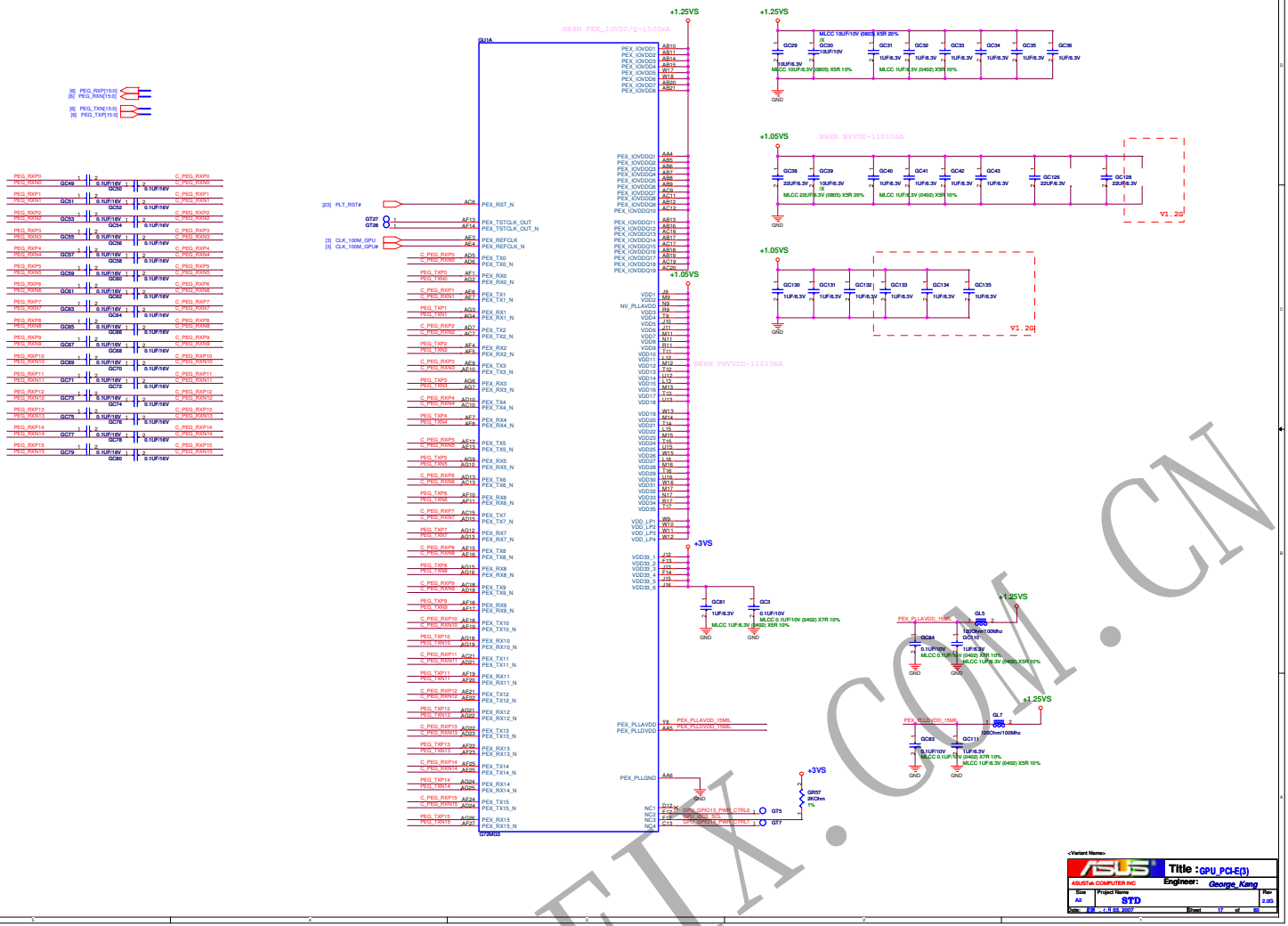
Engineer: STD

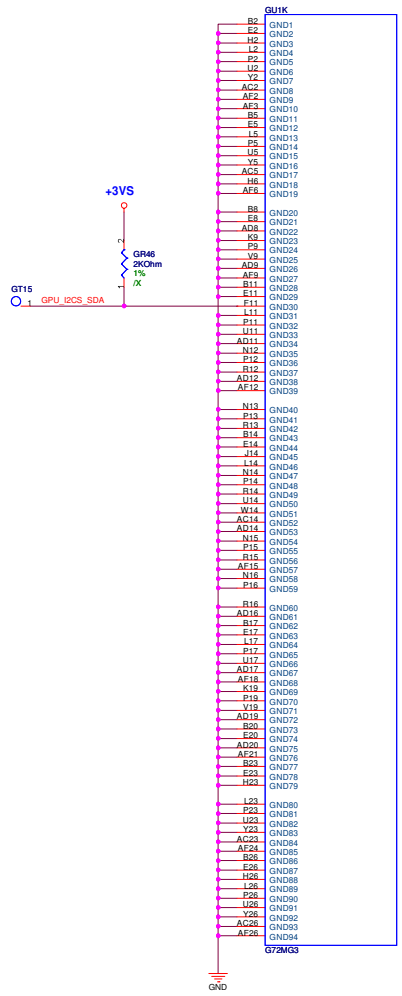
Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期 二, 七月 03, 2007 Sheet 14 of 60









<Variant Name>

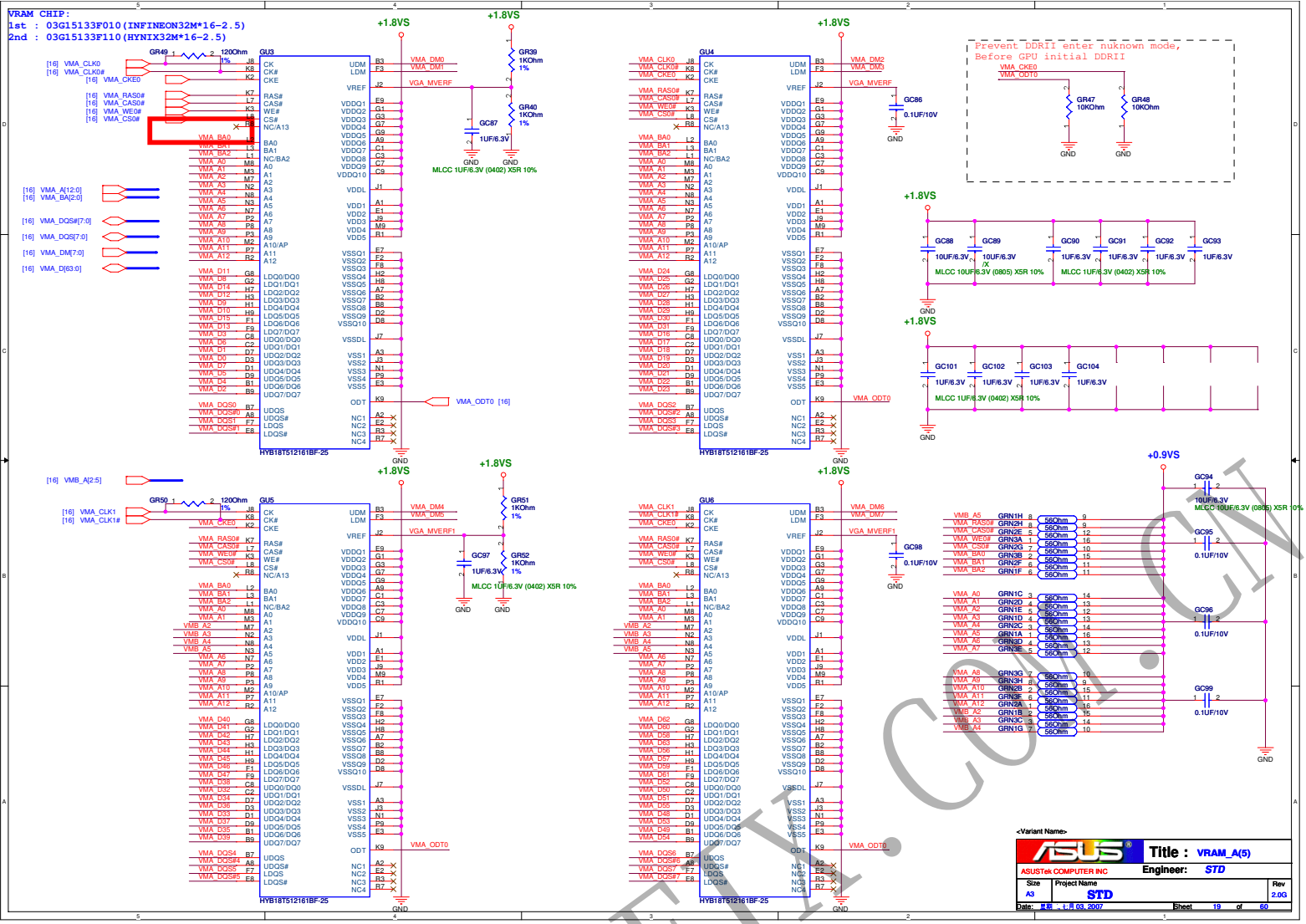
Title : GPU_POWER_GND(4)

ASUSTek COMPUTER INC

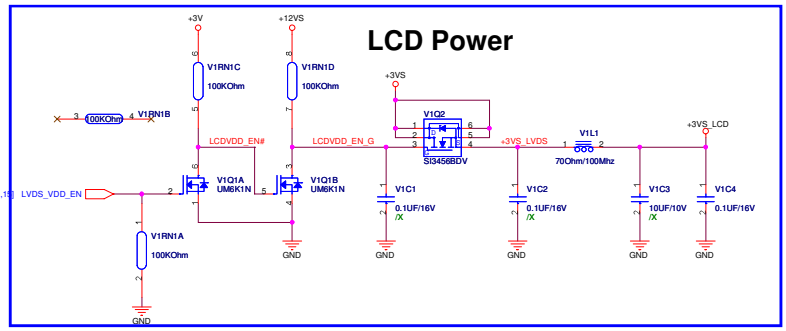
Engineer: STD

Size	Project Name	Rev
A3	STD	2.0G

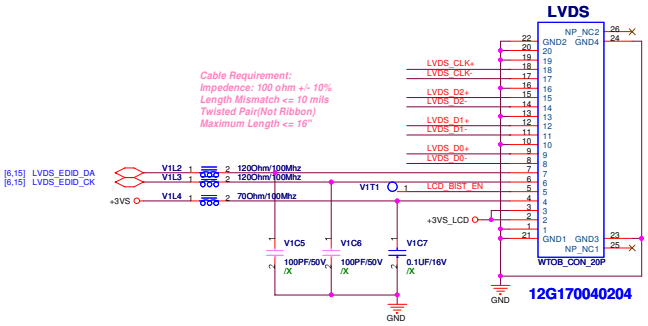
Date: 星期二, 七月 03, 2007 Sheet 18 of 60



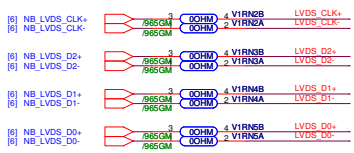
LCD Power



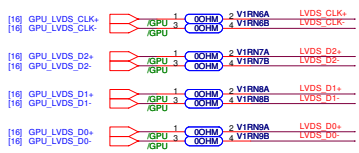
LCD LVDS Connector



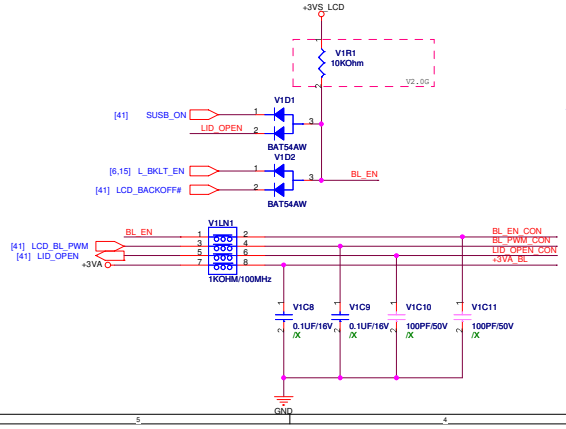
LVDS from 965GM

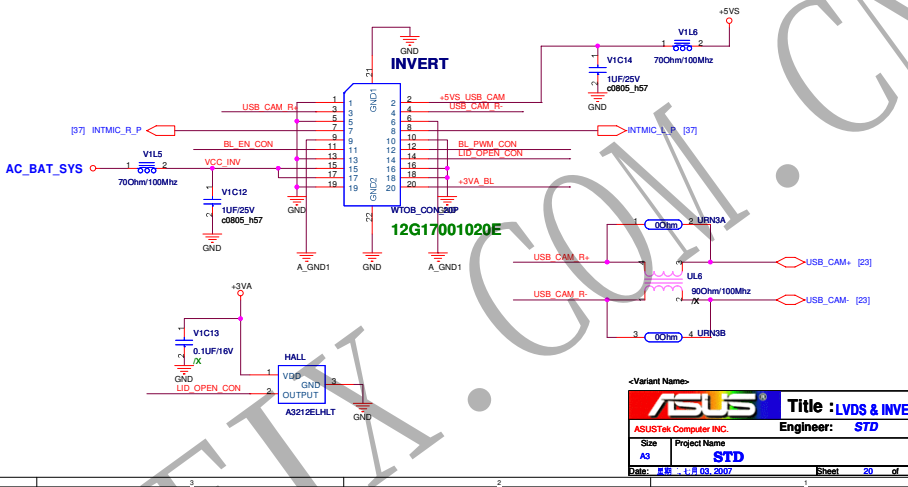


LVDS from GPU-NB8M



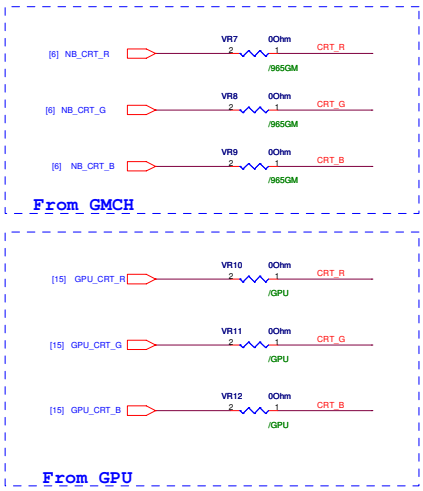
LCD Inverter Connector

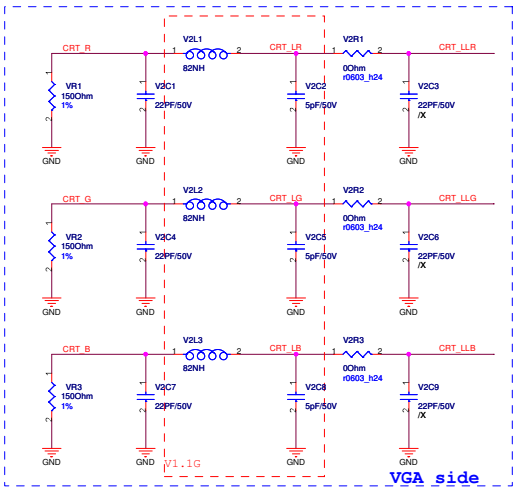


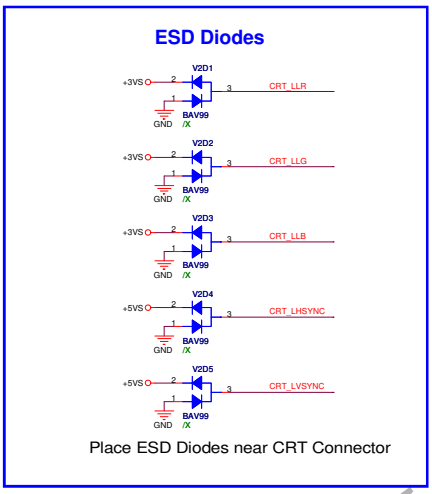


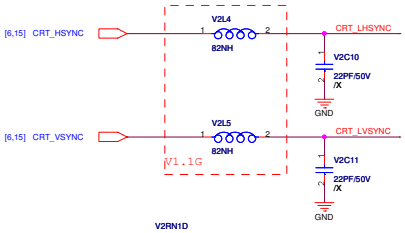
<Variant Name>

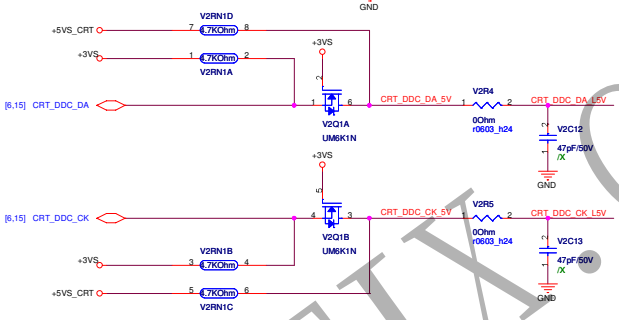
ASUSTek Computer INC.	Title : LVDS & INVERTER	
	Engineer: STD	
Size: A3	Project Name: STD	Rev: 2.0G
Date: 星期 一, 十月 03, 2007	Sheet 20 of 60	

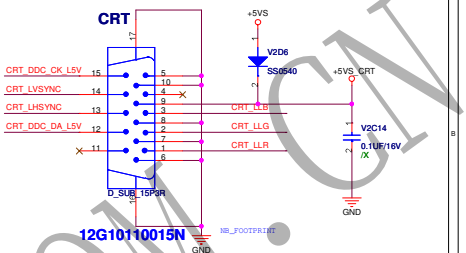


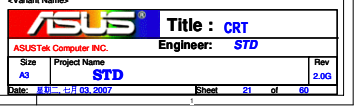


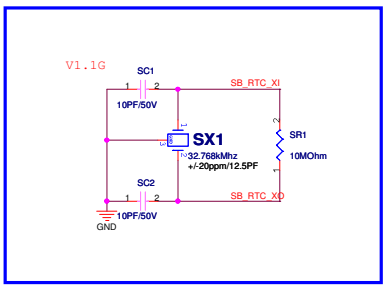


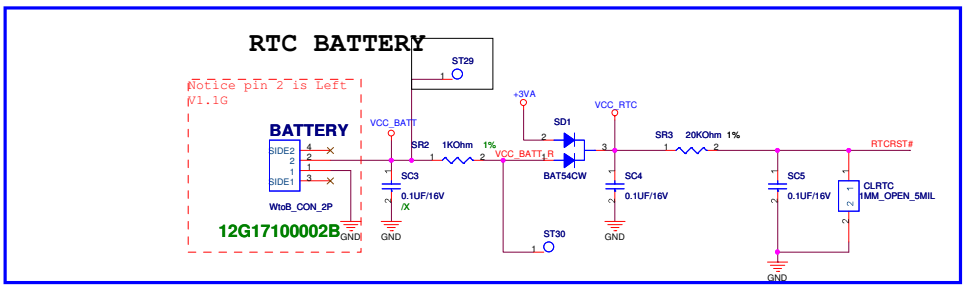




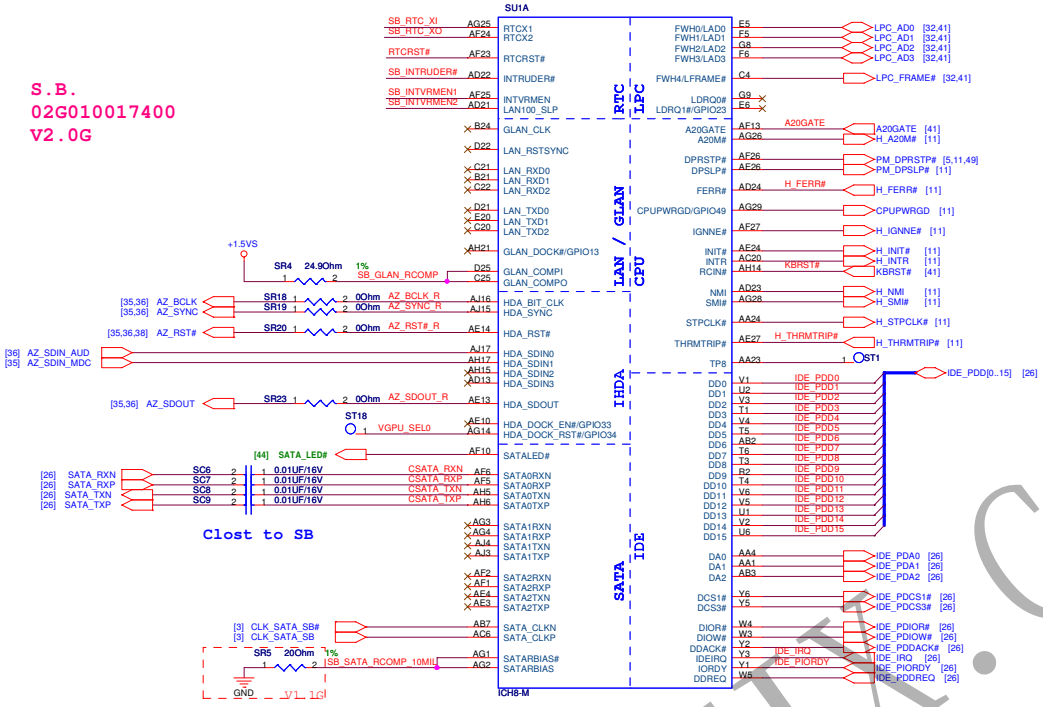


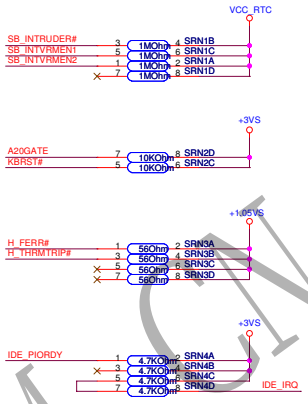






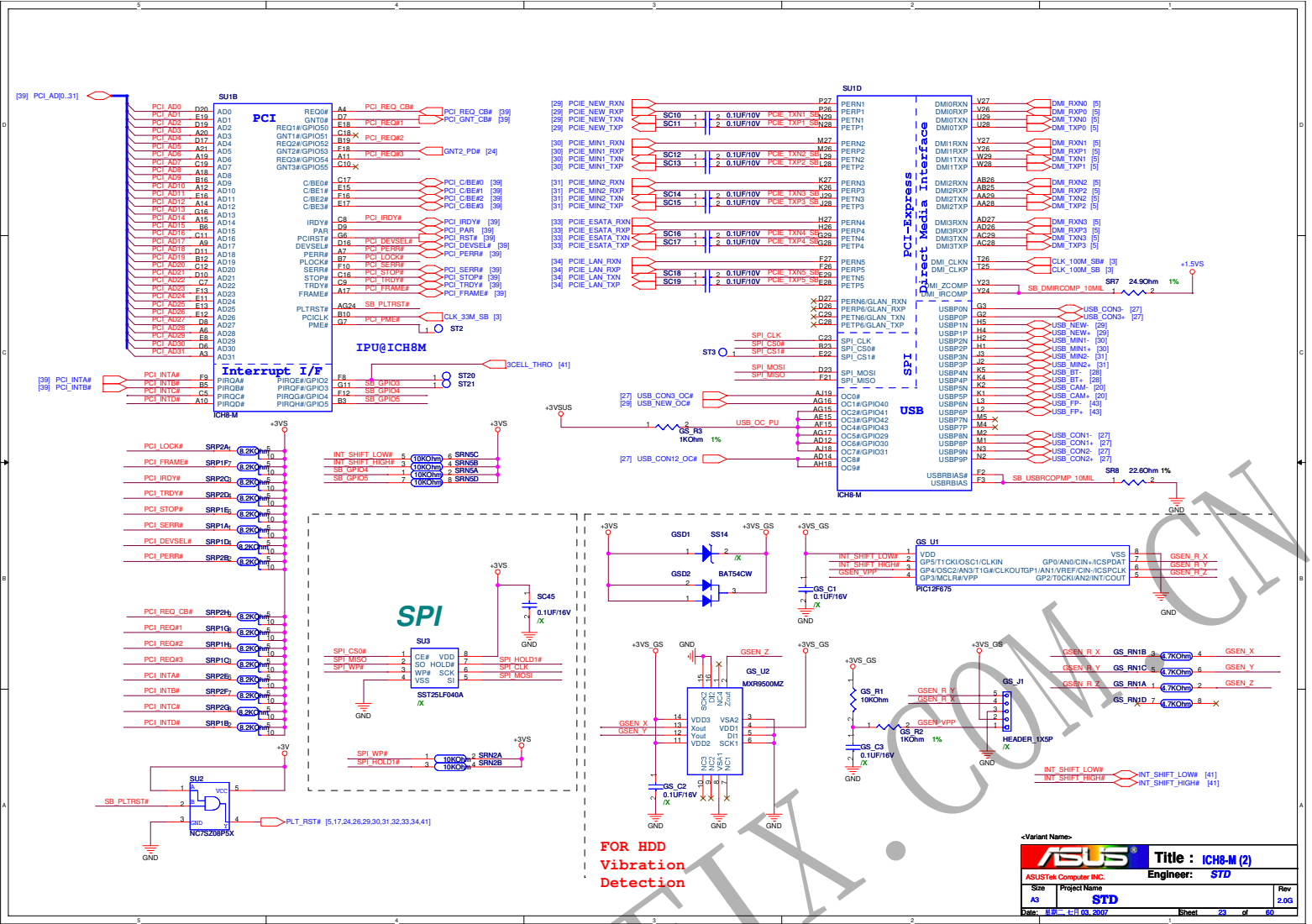
S.B.
02G010017400
V2.0G

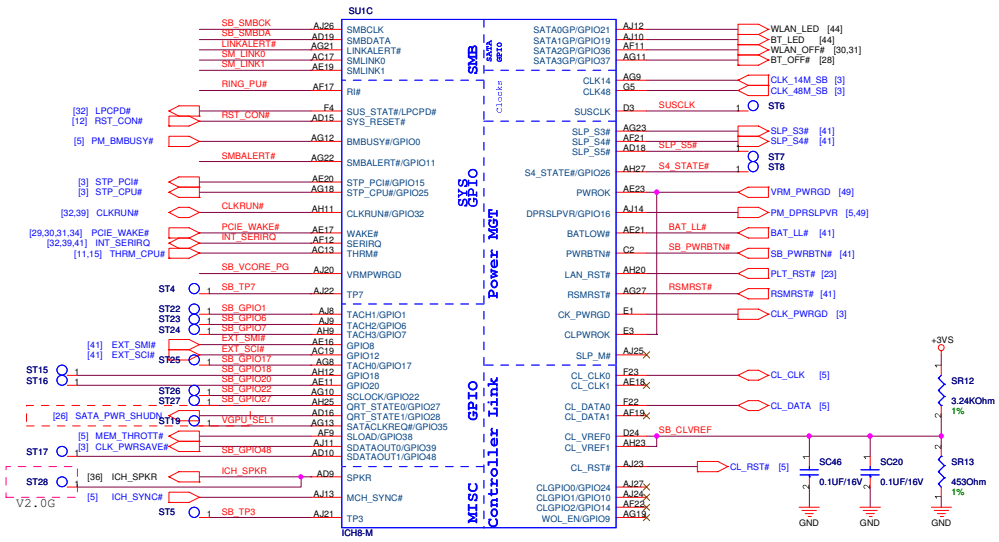


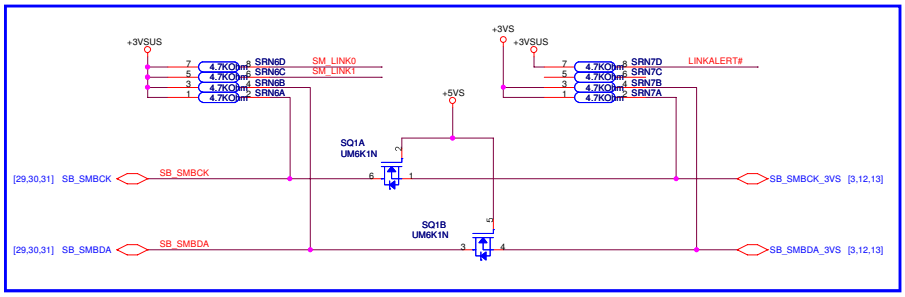


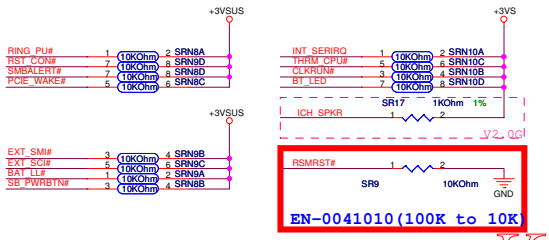
<Variant Name>

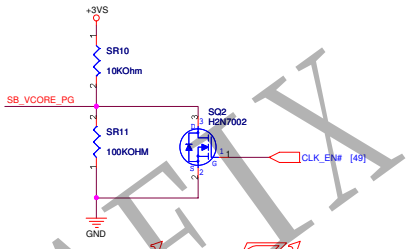
ASUSTeK Computer INC.	Title : ICH8-M (1)	
	Engineer: STD	
Size: Custom	Project Name: STD	Rev: 2.2G
Date: 星期二 七月 03, 2007	Sheet 22 of 60	











(ICH_TP3)
1 = PCIE Strap (*) default internal PU
0 = XOR chan test mode

(HDA_SDOUT, HDA_SYNC)
(11) = LANE1~4 as a PCIEx4 port
(00) = LANE1~4 as 4 PCIEx1 ports (*) default internal PD
others = reserved

(GNT2#)
1 = LANE5~6 reserved (internal PU)
0 = LANE5~6 as 2 PCIEx1 ports (*)

(SB_GPIO20)
1 = reserved
0 = Intel recommend (* internal PD)

(GNT1#)
1 = Destop/Mobile (* internal PU)
0 = Server

(GNT3#)
1 = Normal (* internal PU)
0 = Top-block swap for FWH

(SPI_CS1# : GNT0#) = 11 (* internal PU)

	GNT0#	SPI_CS1#
SPI	0	1
PCI	1	0
LPC	1	1

(INTVRMEN, LAN100_SLP)
1 = Enabled internal VRMs for VccSus1_05, 1_5 and VccCL1_5, 1_05 and VccLAN1_05 (*)
0 = Disabled internal VRMs

(ICH_SATALED#)
1 = LANE1~4 normal (* internal PU)
0 = LANE1~4 reverse

(SPKR)
1 = Disabled TCO Reboot
0 = Enabled TCO Reboot (* internal PD)

(TP_GPIO33) : Not used for ICH8M
1 = Enabled Descriptor Security (* internal PU)
0 = Dnabled Descriptor Security

<Variant Name>

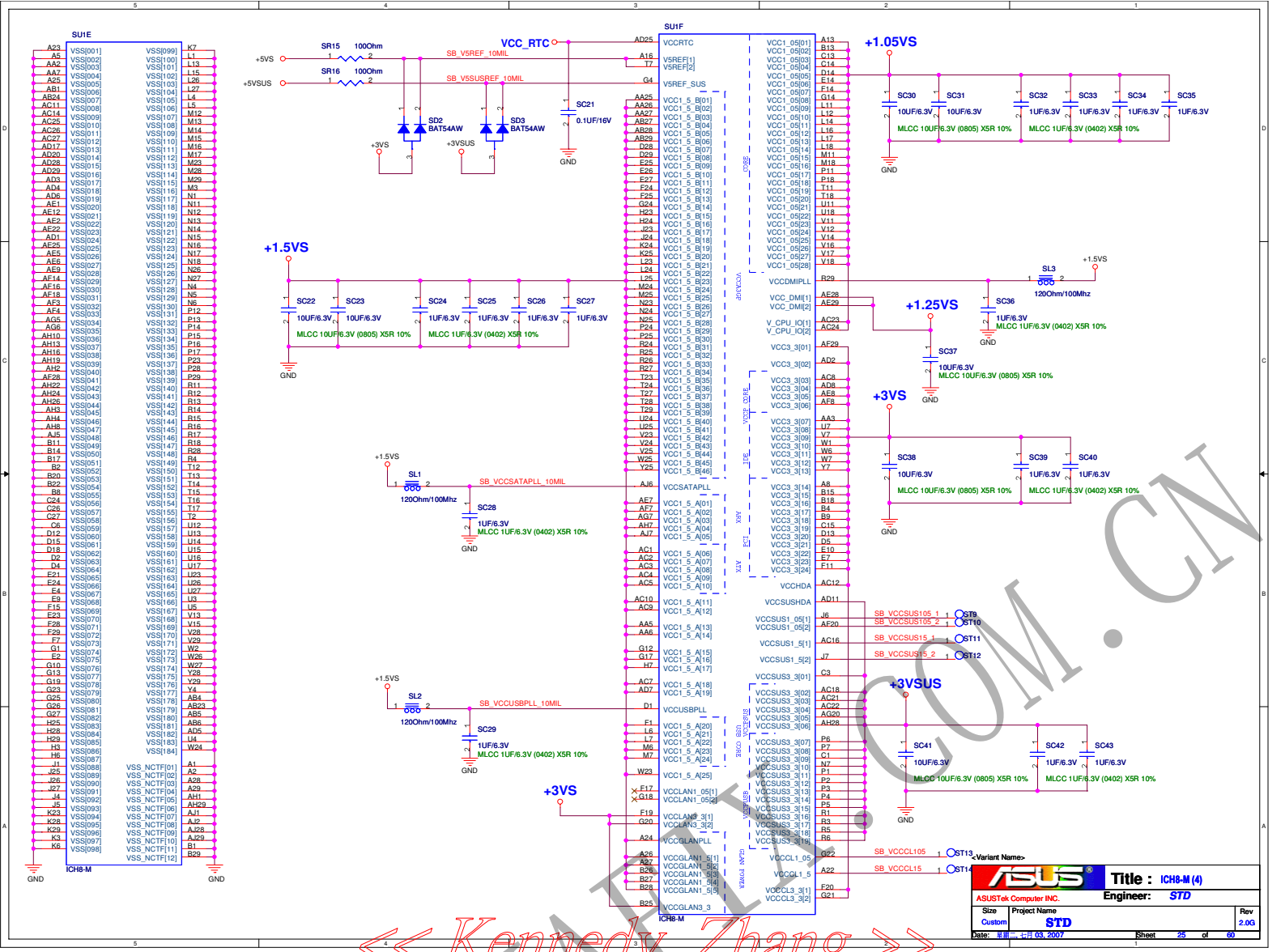
ASUSTek Computer INC.

Title : ICH8-M (3)

Engineer: STD

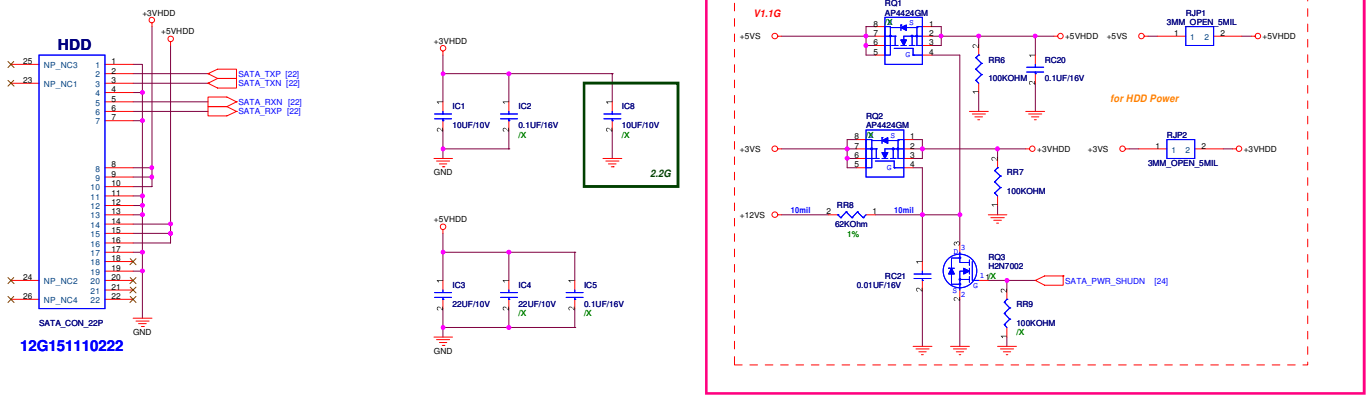
Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 24 of 60



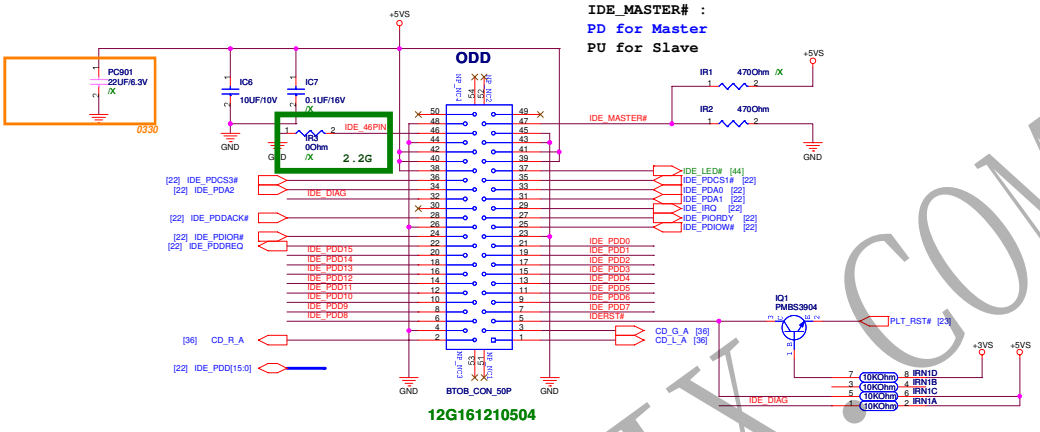
Title :	ICH8-M (4)
ASUSTek Computer INC.	Engineer: STD
Size: Custom	Project Name: STD
Rev: 2.0G	
Date: 星期二, 七月 03, 2007	Sheet 25 of 60

SATA HDD



12G151110222

ODD

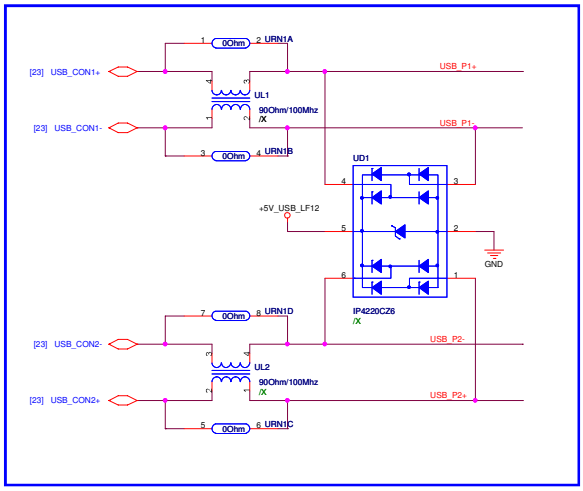


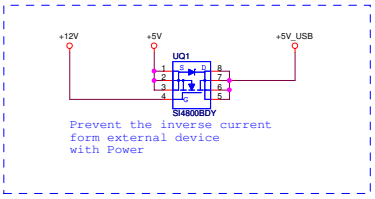
12G161210504

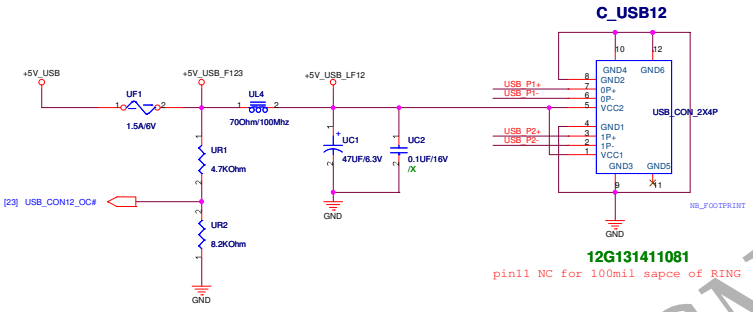
<Variant Name>

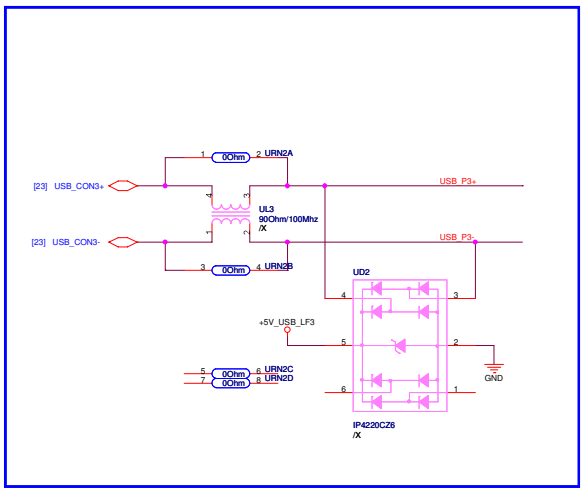
ASUSTek Computer INC.	Title : SATA-HDD & ODD	
	Engineer: STD	
Size: Custom	Project Name: STD	Rev: 2.2G
Date: 星期 二 七月 03, 2007	Sheet 26 of 60	

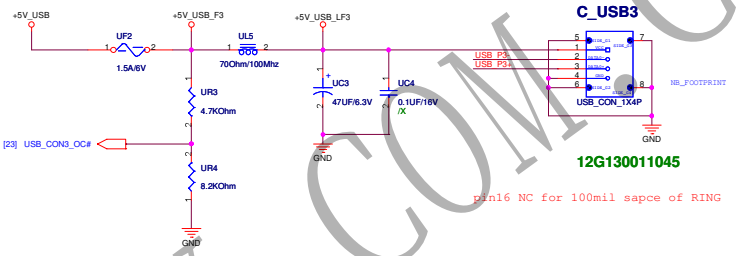
All close to USB connectors











<Variant Name>

ASUSTek Computer INC.

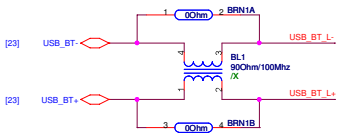
Title : USB CONN

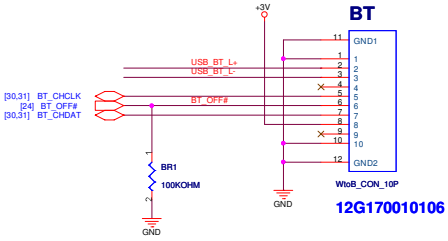
Engineer: STD

Size	Project Name	Rev
A3	STD	2.0G

Date: 星期 , 十月 03, 2007 Sheet 27 of 60

Bluetooth Connector





BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

<Variant Name>

ASUSTek Computer INC.

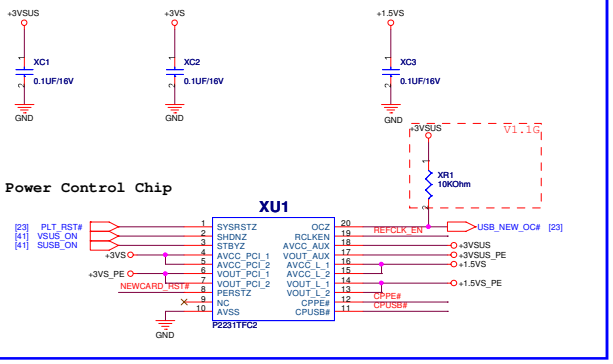
Title : Blue Tooth

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

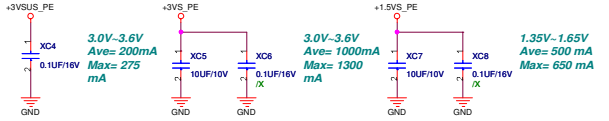
Date: 星期 二, 七月 03, 2007 Sheet 28 of 60

Decouple Cap. (Near XU1)



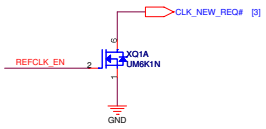
Power Control Chip

Decouple Cap. (Near Express connector)

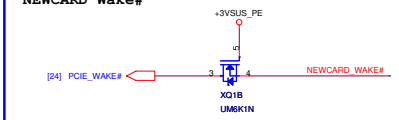


12G161300261

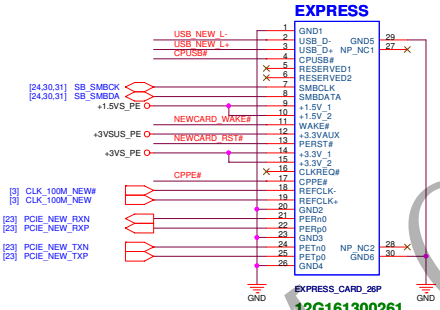
NEWCARD CLK Request



NEWCARD Wake#



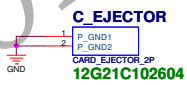
EXPRESS



12G161300261

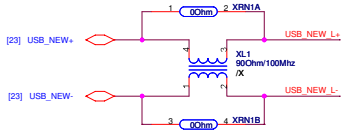
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector



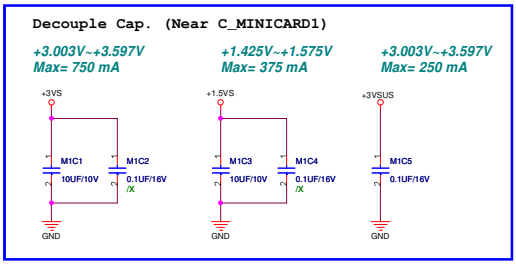
12G21C102604

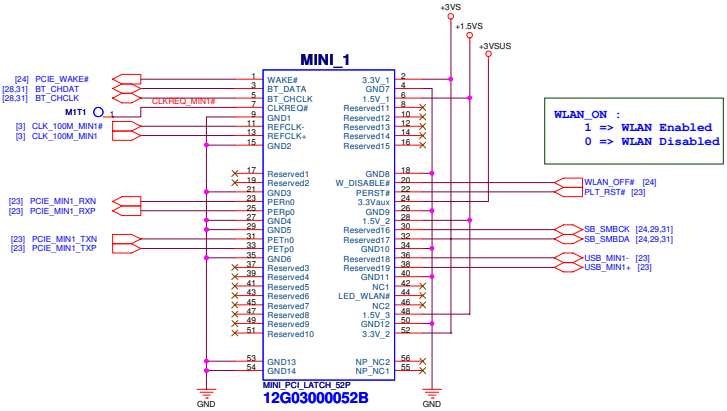
USB CHOKE FOR EMI



<Variant Name>

ASUSTek Computer INC.	Title : NEWCARD	
	Engineer: STD	
Size: Custom	Project Name: STD	Rev: 2.0G
Date: 星期 二, 七月 03, 2007	Sheet 29 of 60	





<Variant Name>

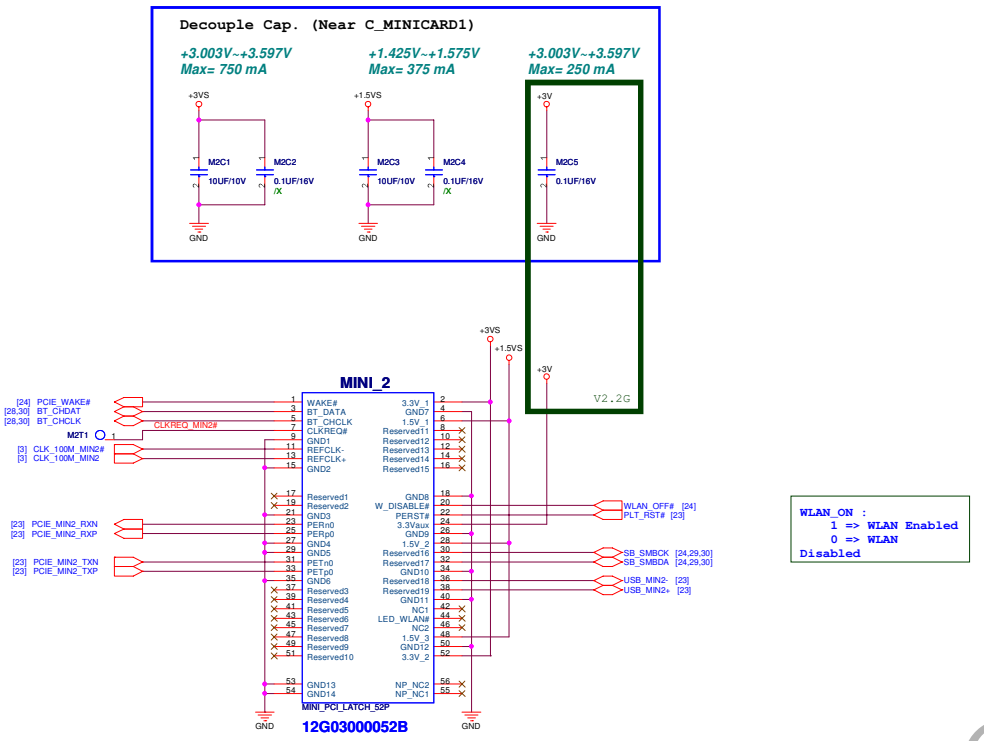
ASUSTek Computer INC.

Title : MINI CARD

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 30 of 60




```
WLAN_ON :
    1 => WLAN Enabled
    0 => WLAN
Disabled
```

<Variant Name>

ASUSTek Computer INC.

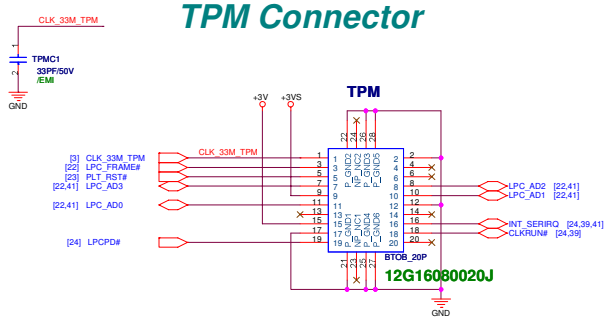
Title : MINI CARD

Engineer: STD

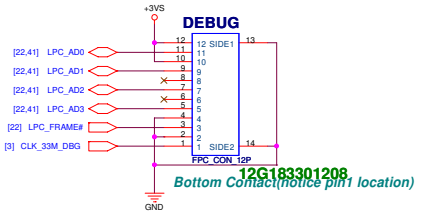
Size	Project Name	Rev
Custom	STD	2.2G

Date: 星期二, 七月 03, 2007 Sheet 31 of 60

TPM Connector

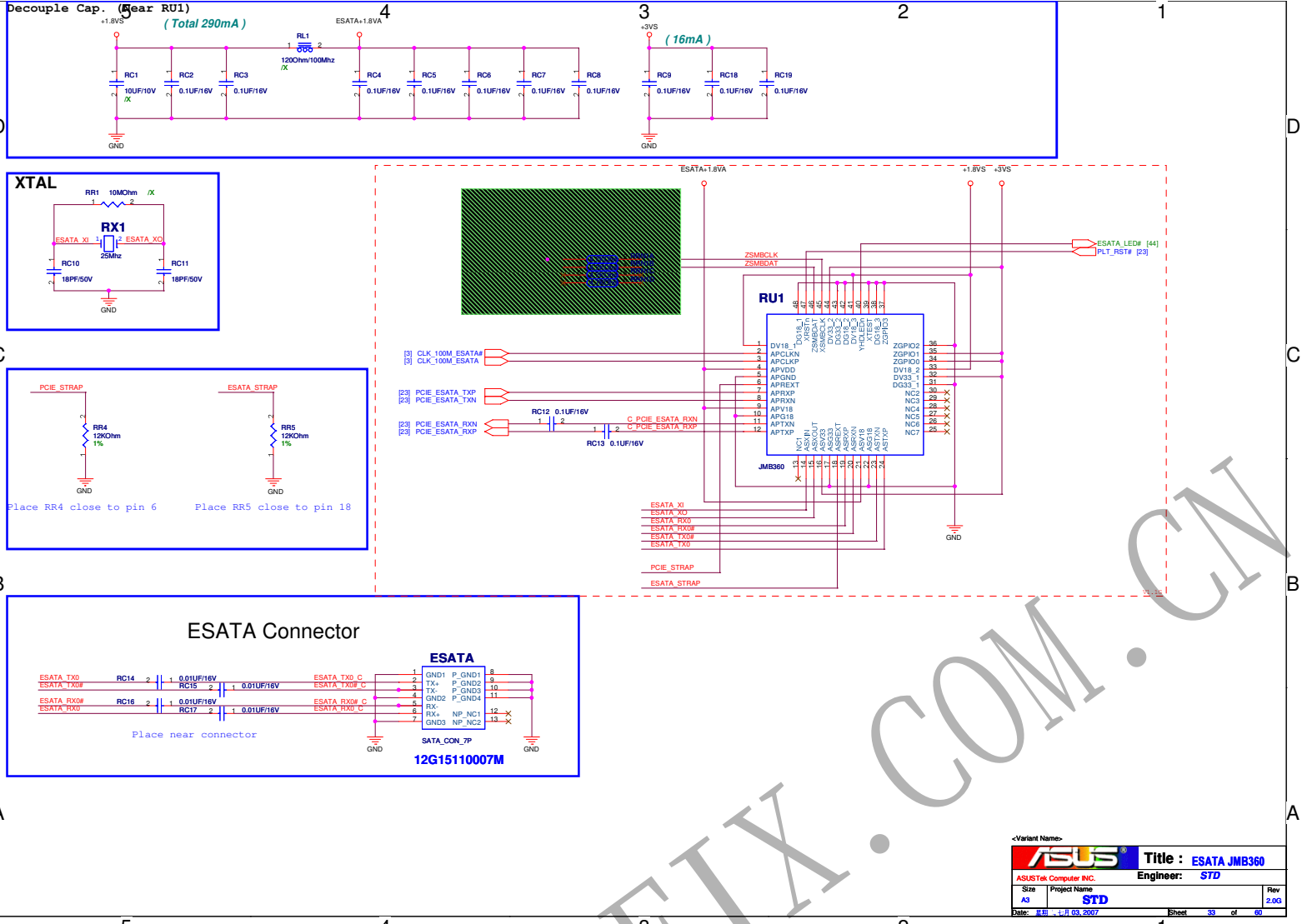


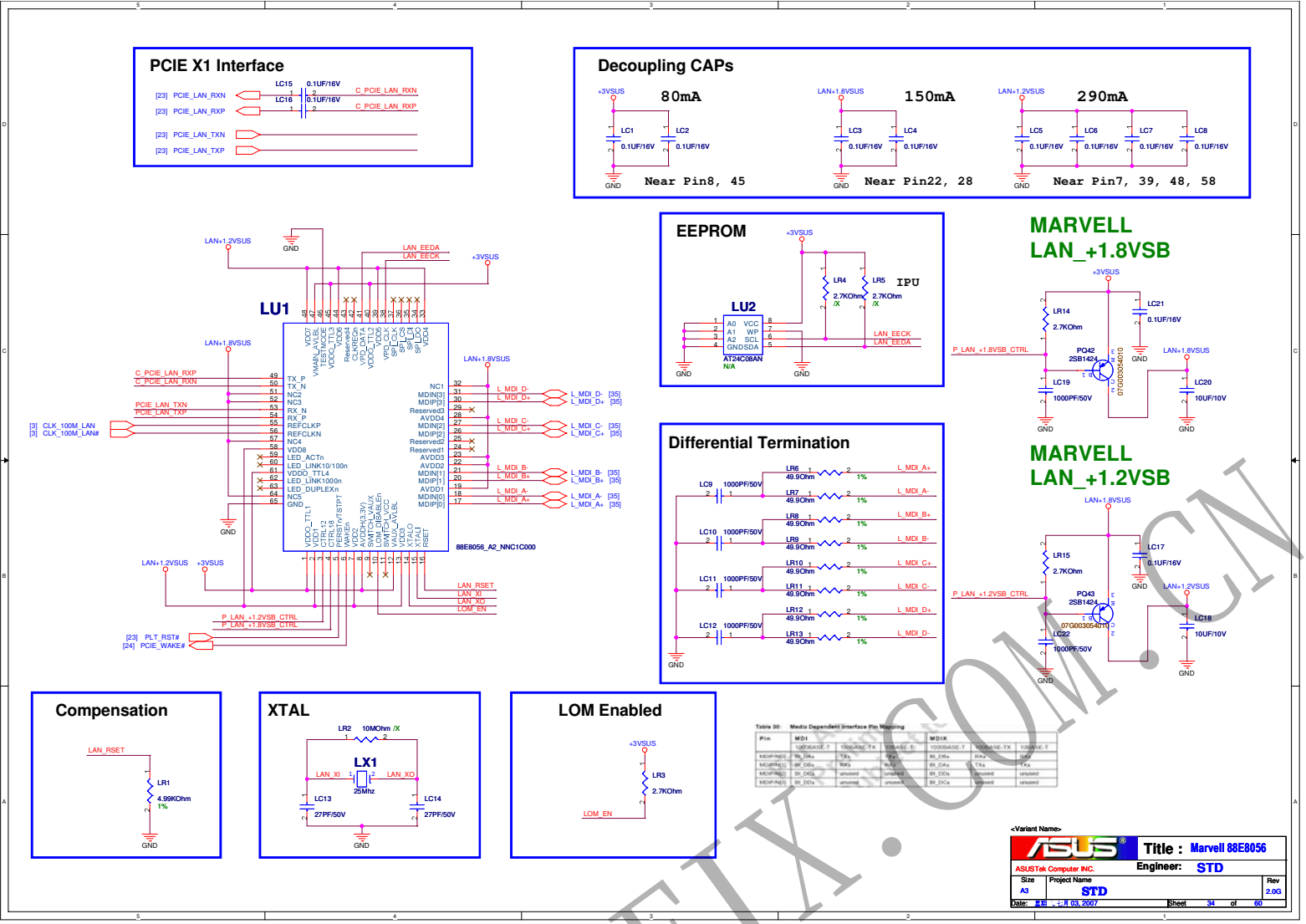
Debug Connector

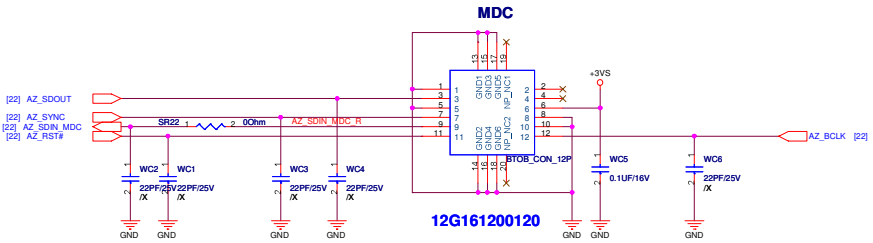


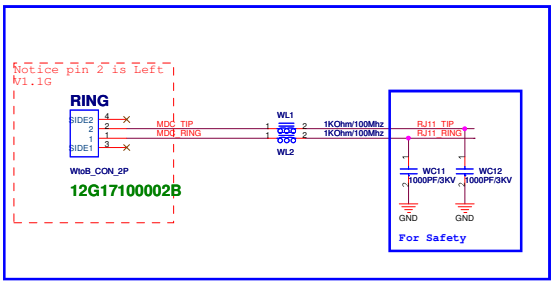
<Variant Name>

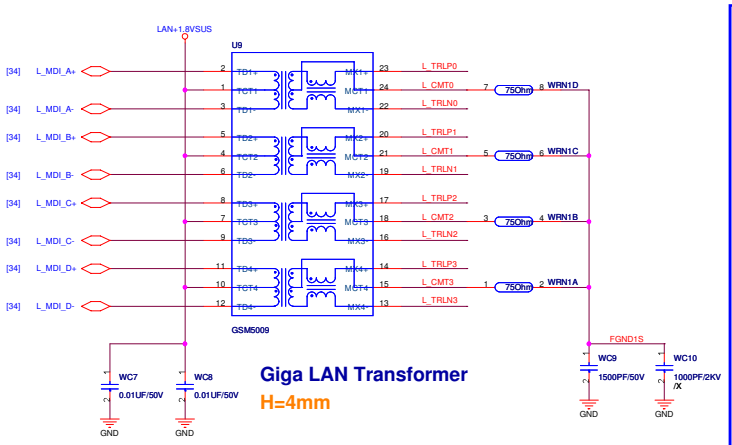
ASUSTek Computer INC.	Title : TPM	
	Engineer: STD	
Size: Custom	Project Name: STD	Rev: 2.0G
Date: 星期 二 七月 03, 2007	Sheet 32 of 60	

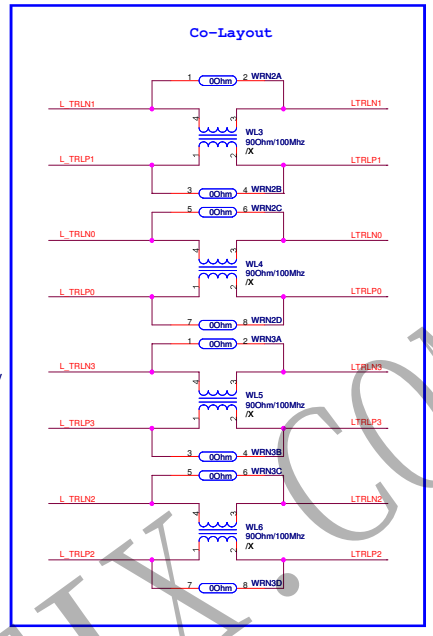


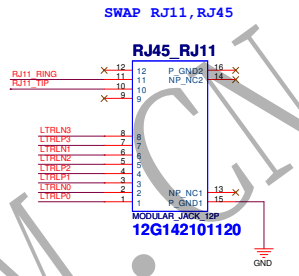


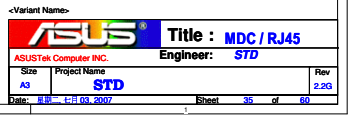


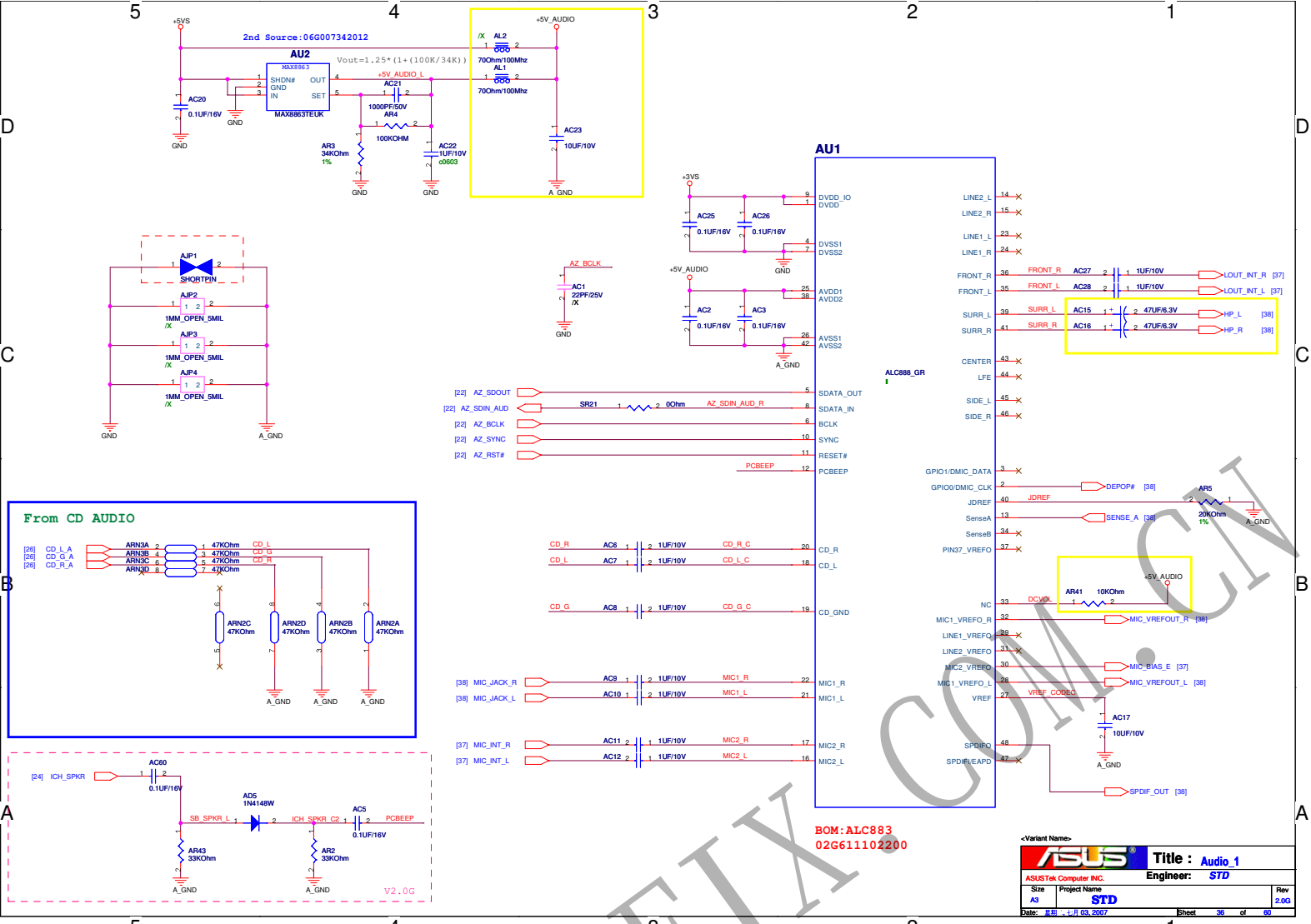




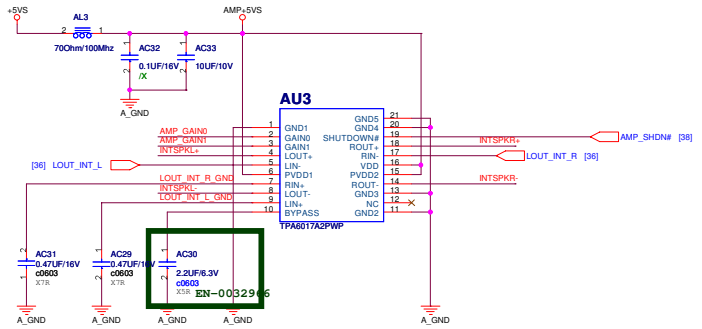






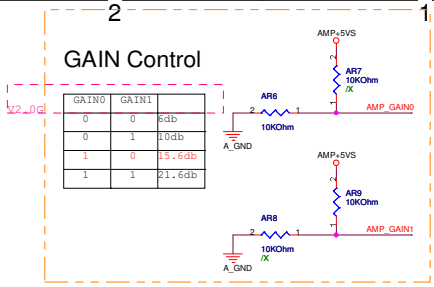


Audio Amp.

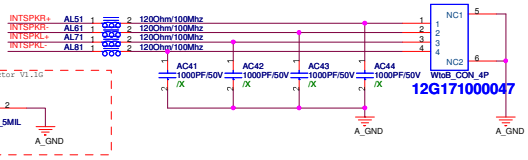


GAIN Control

GAIN0	GAIN1	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



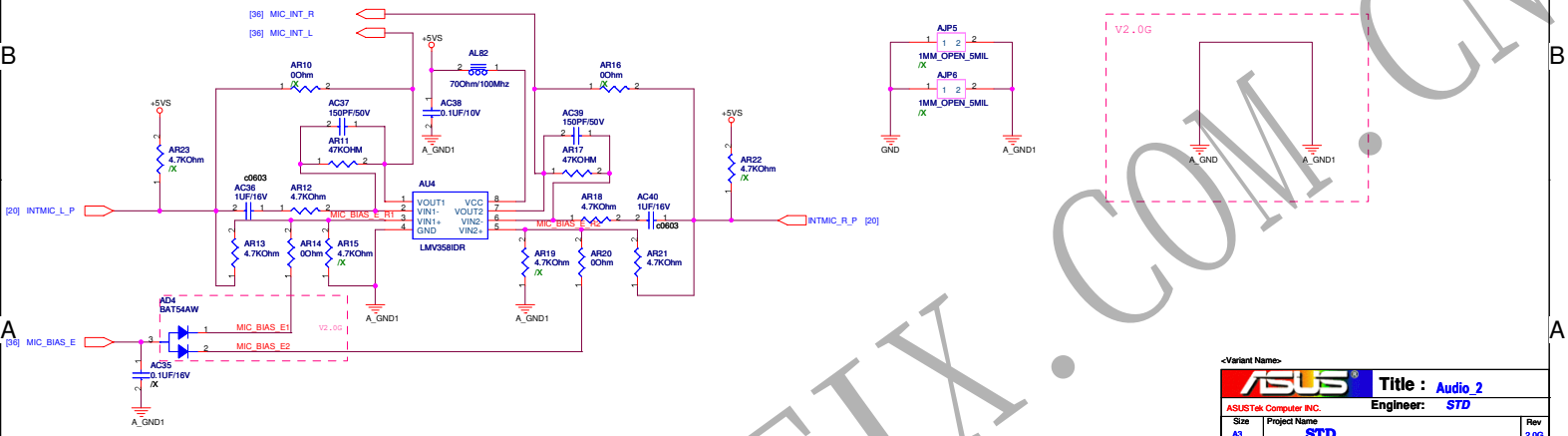
SPEAKER



Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz

Place Near INTMIC Connector



<Variant Name>

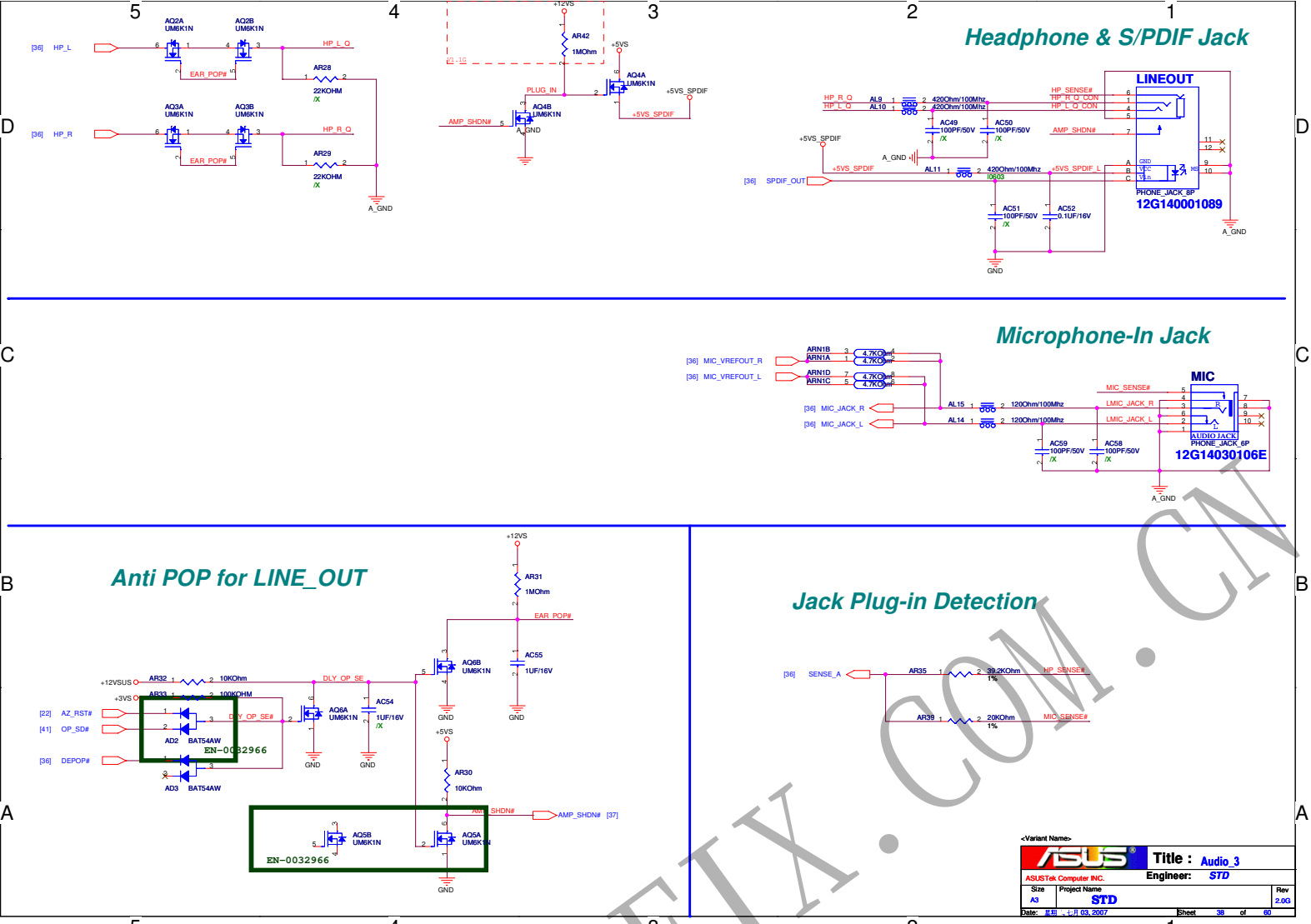
ASUSTek Computer INC.

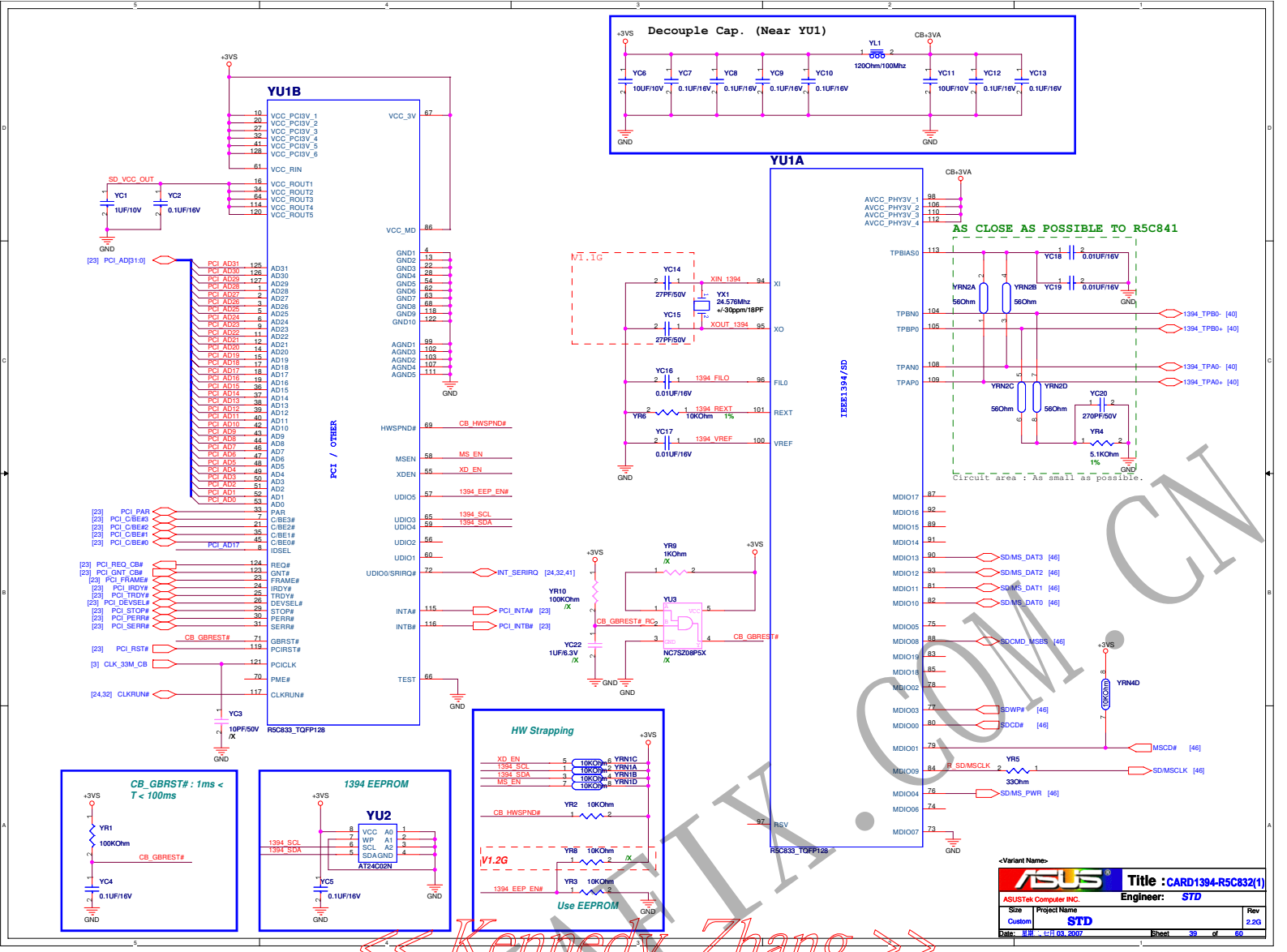
Title : Audio_2

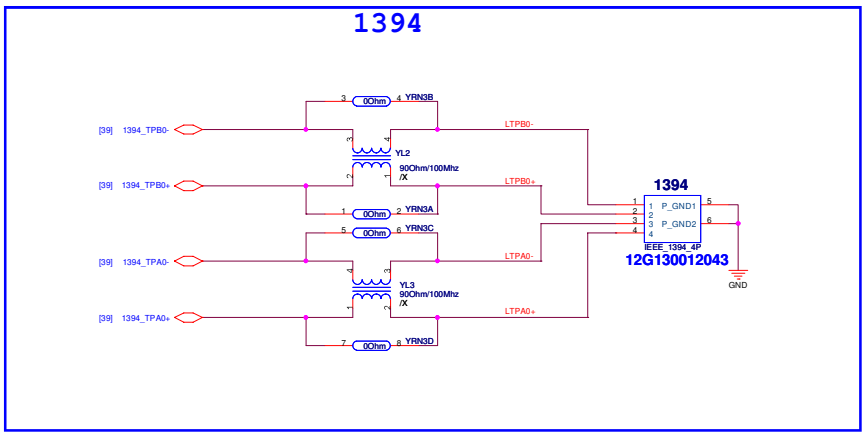
Engineer: STD

Size	Project Name	Rev
A3	STD	2.0G

Date: 星期 二, 七月 03, 2007 Sheet 37 of 60

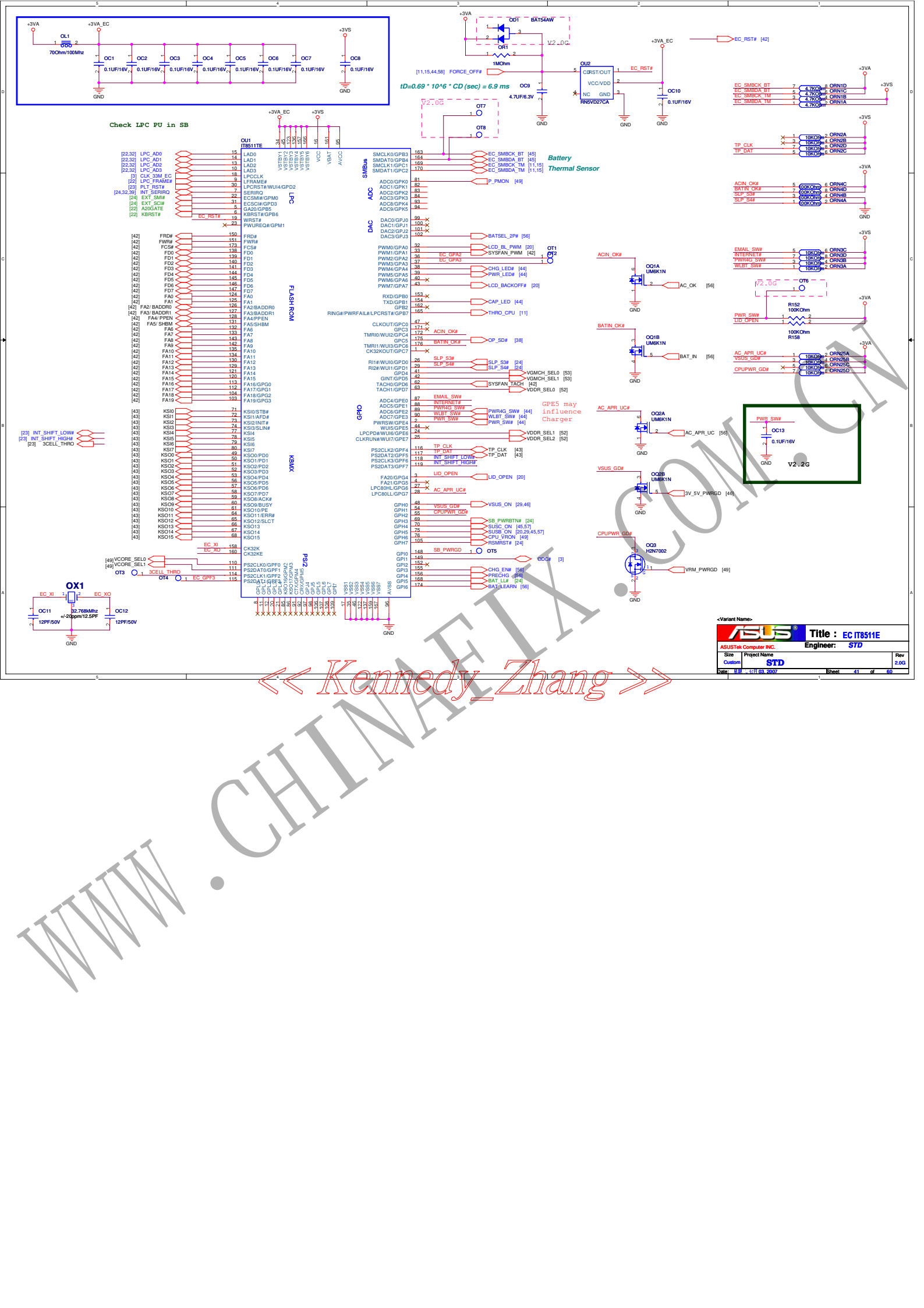






<Variant Name>

ASUSTek Computer INC.	Title: 1394 CON	
	Engineer: STD	
Size: A3	Project Name: STD	Rev: 2.0G
Date: 星期一 十月 03, 2007	Sheet 40 of 60	



ISA ROM

EC Hardware Strapping

[FA3/ BADDR1 : FA2/ BADDR0]

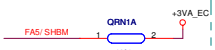
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
01: PNPCNG Access Register Pair Are 004Eh and 004Fh
10: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved

FA4/ PPEN

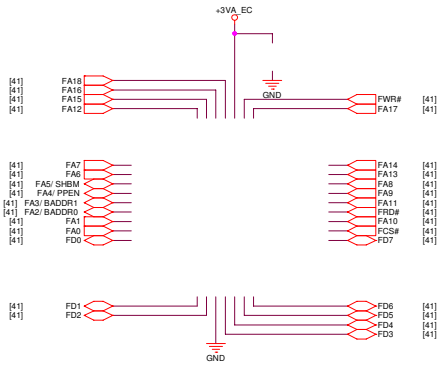
0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

FA5/ SHBM

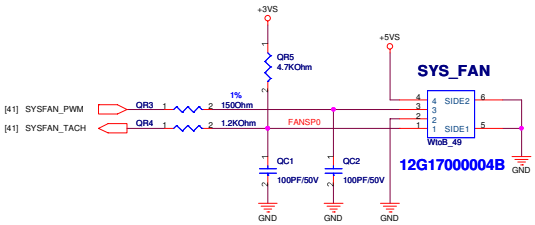
0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

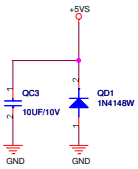


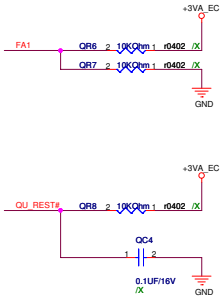
Note: Sampled at VSTBY Power Up Reset

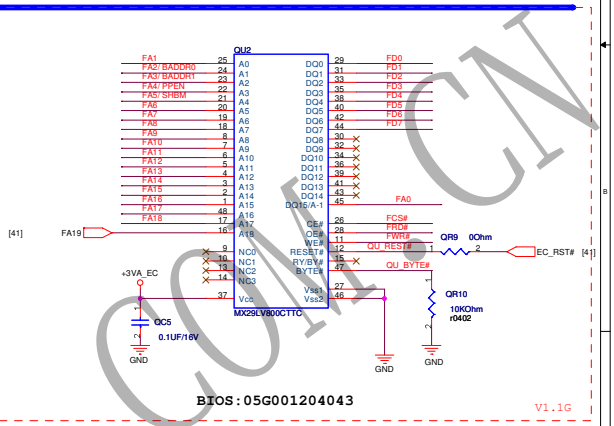


System Fan Connector





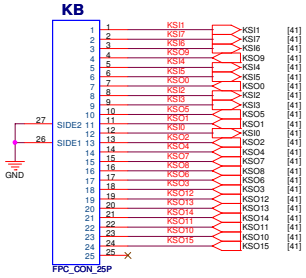




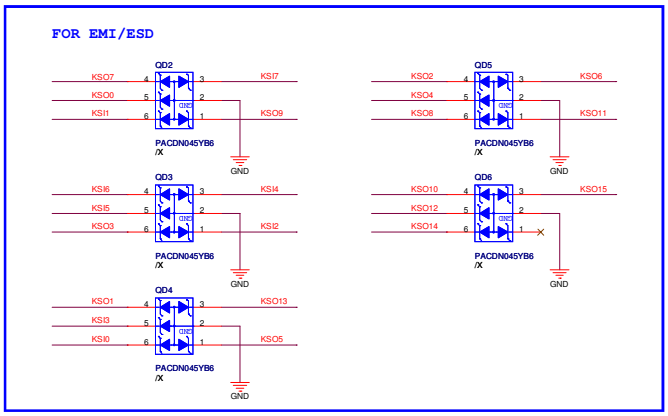
<variant_name>

ASUSTek Computer INC.	Title : ISA FLASH ROM	
	Engineer: STD	
Size: Custom	Project Name: STD	Rev: 2.0G
Date: 星期 二, 七月 03, 2007	Sheet 42 of 60	

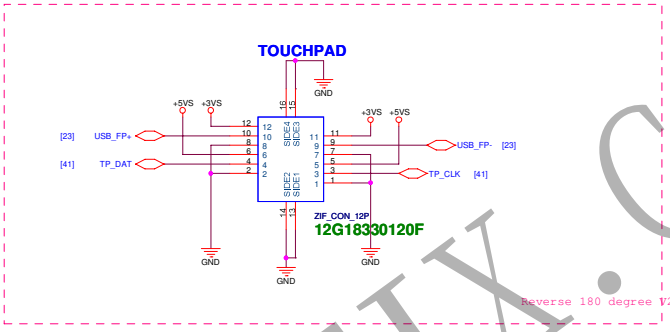
Keyboard Connector



12G182002501

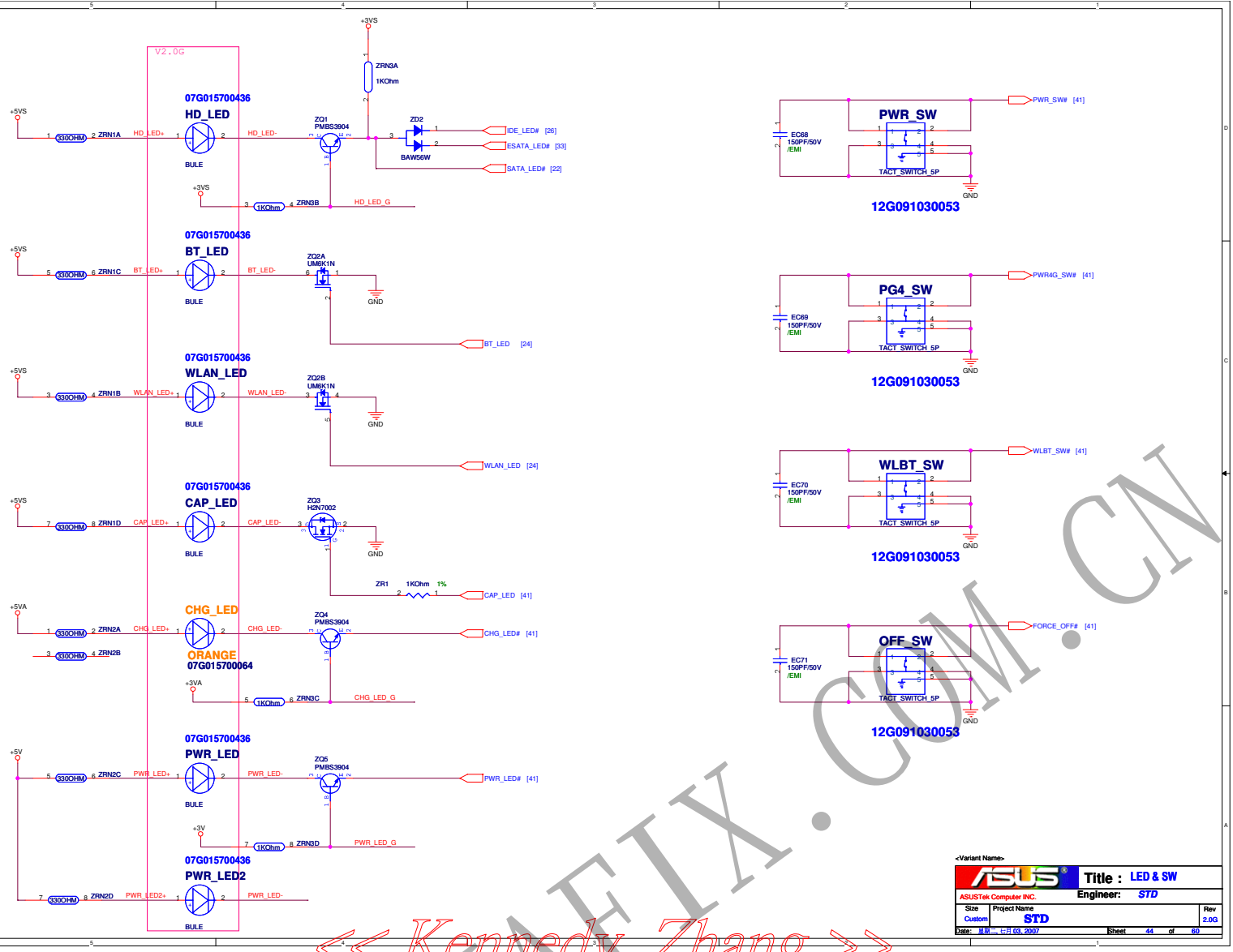


Fingerprint & TouchPad Connector



<Variant Name>

Title :	Touch Pad & KB
ASUSTek Computer INC.	Engineer: STD
Size: Custom	Project Name: STD
Rev: 2.0G	
Date: 星期二, 七月 03, 2007	Sheet 43 of 60



<Variant Name>

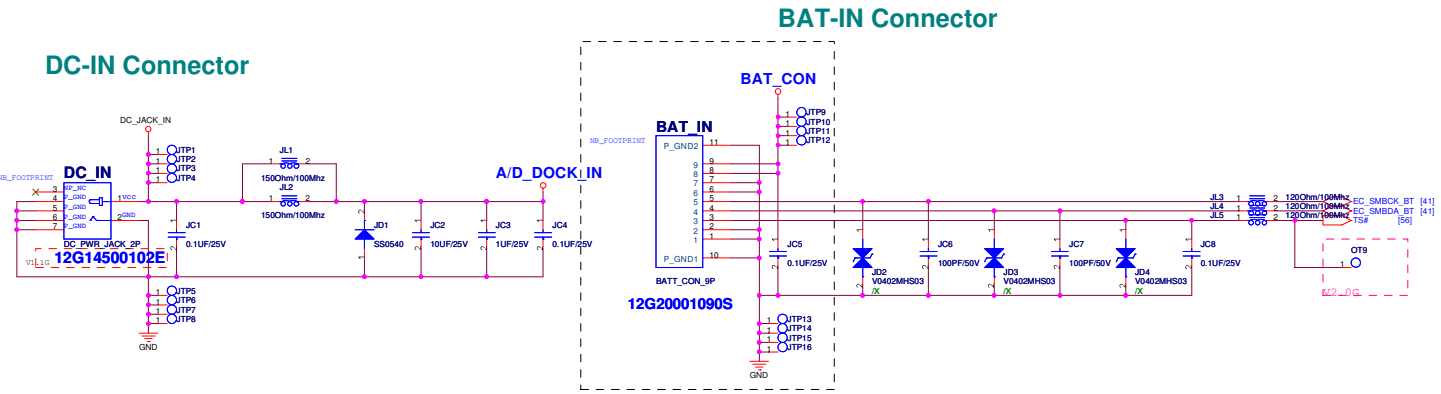
ASUSTek Computer INC.

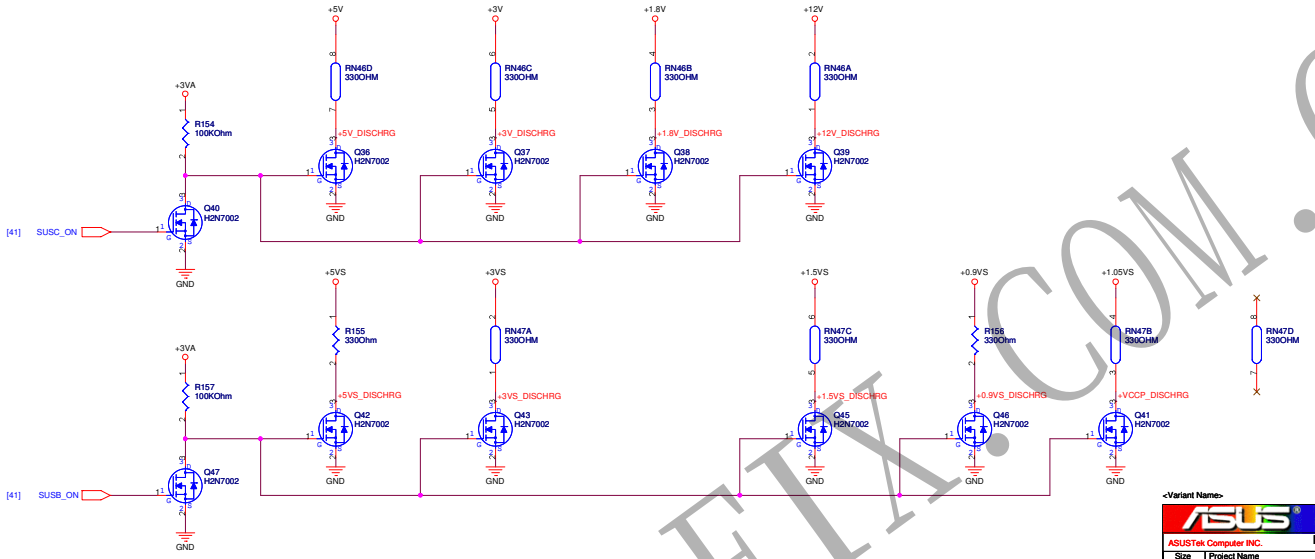
Title : LED & SW

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 44 of 60





<variant_name>

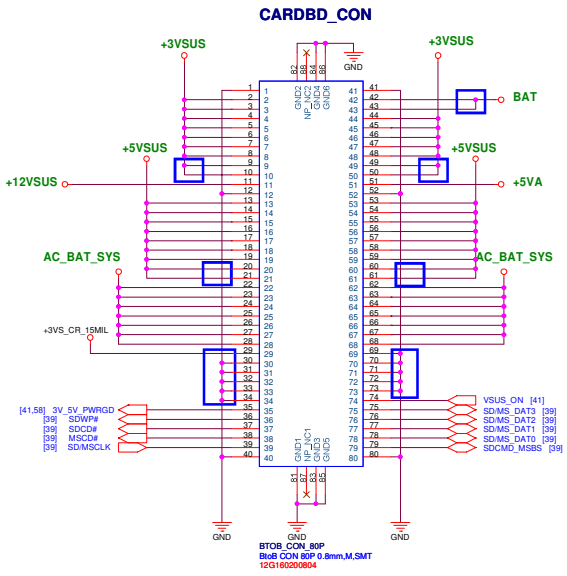
Title : DC IN & BAT IN

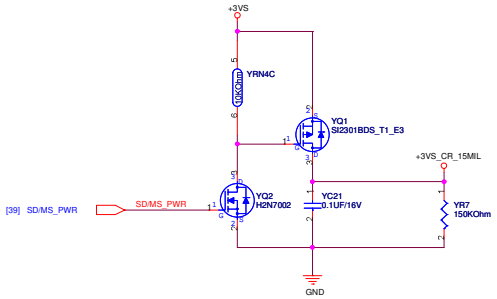
ASUSTek Computer INC.

Engineer: STD

Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期 二, 七月 03, 2007 Sheet 45 of 60





BOM : 12G160200805 --8mmHigh

<Variant Name>

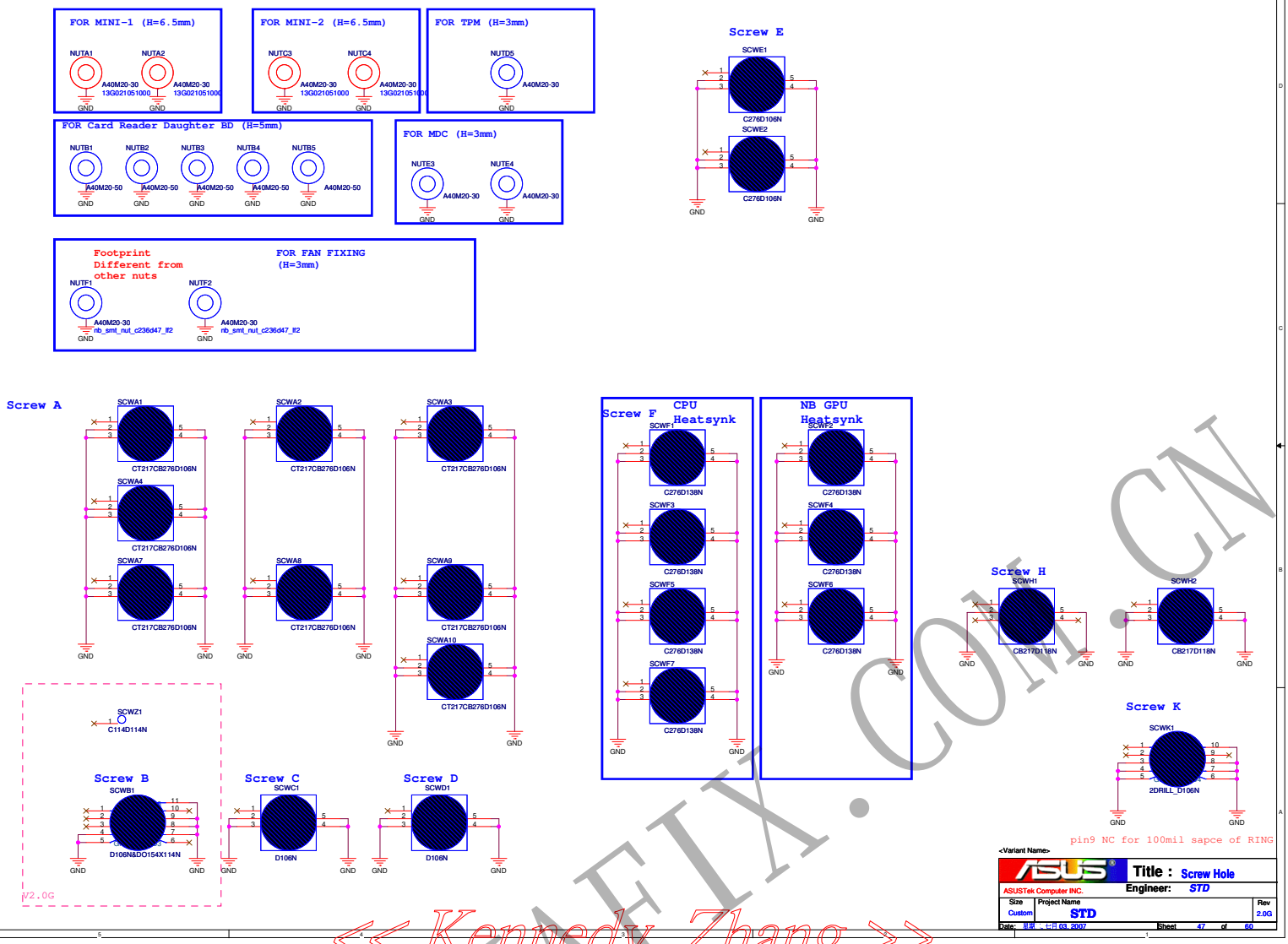
ASUSTek Computer INC.

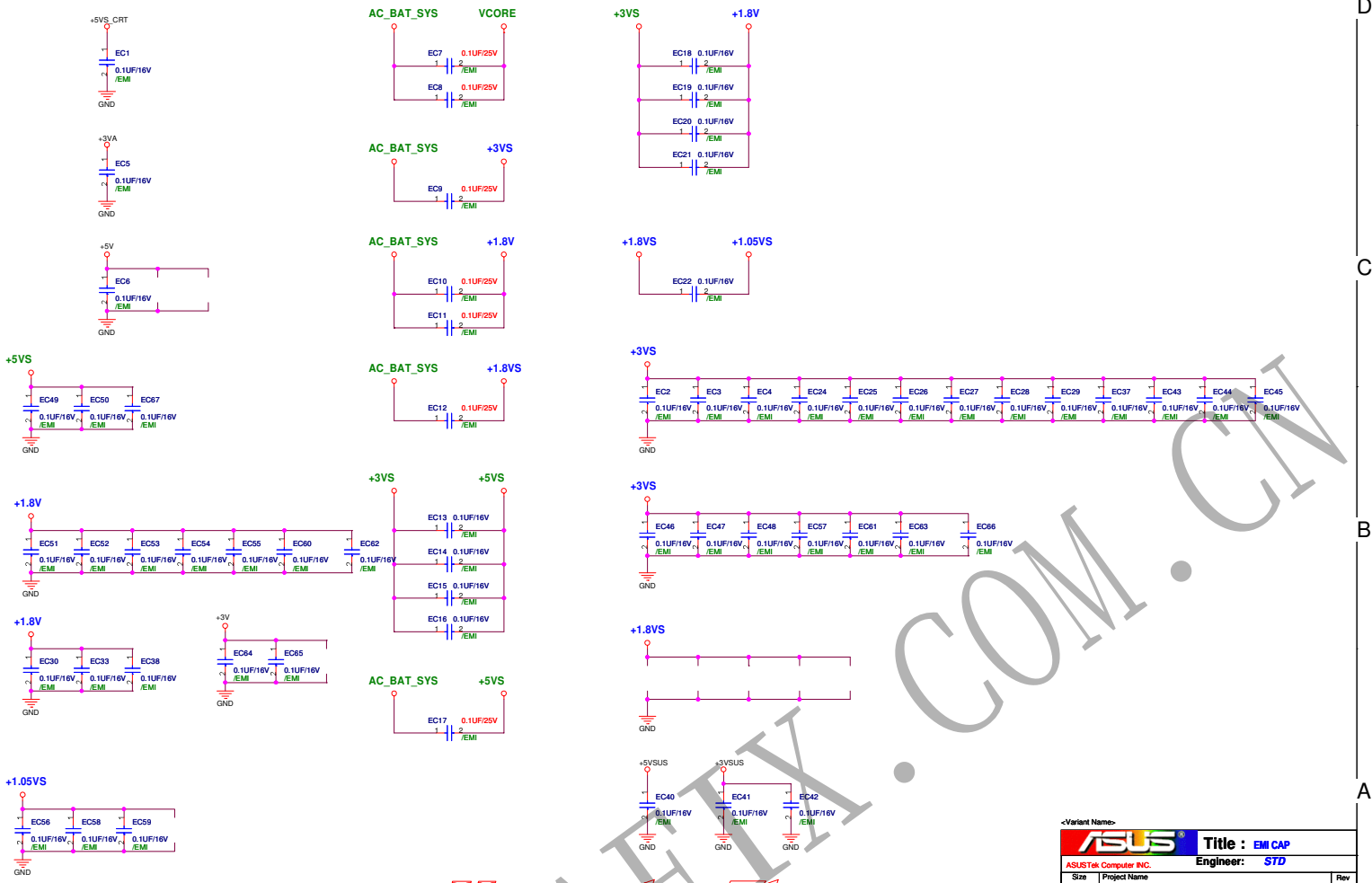
Title : 4 in 1 CARD READER

Engineer: STD

Size	Project Name	Rev
A3	STD	2.0G

Date: 星期一 十月 03, 2007 Sheet 46 of 60





<Variant Name>

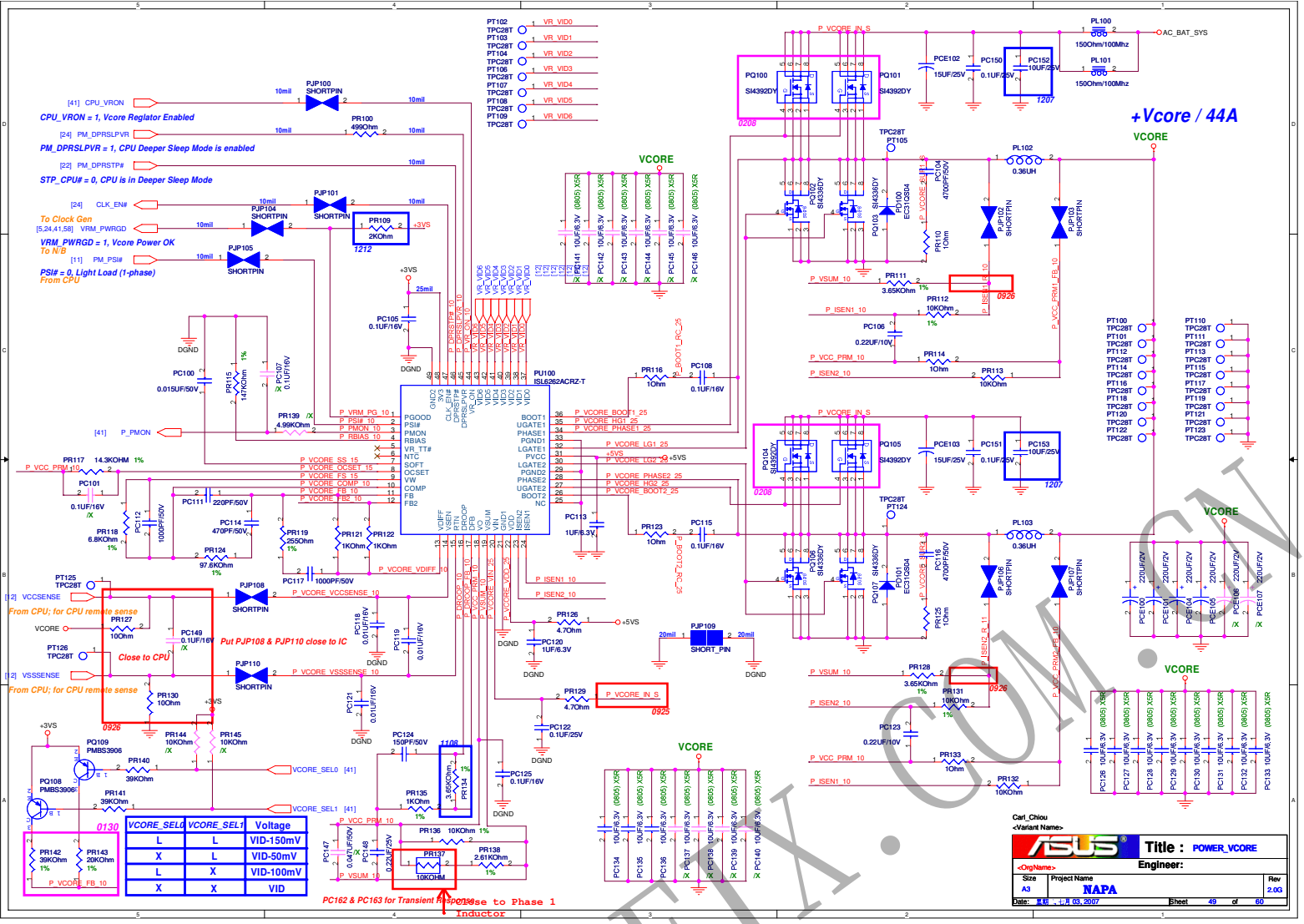
ASUSTek Computer INC.

Title : EMI CAP

Engineer: STD

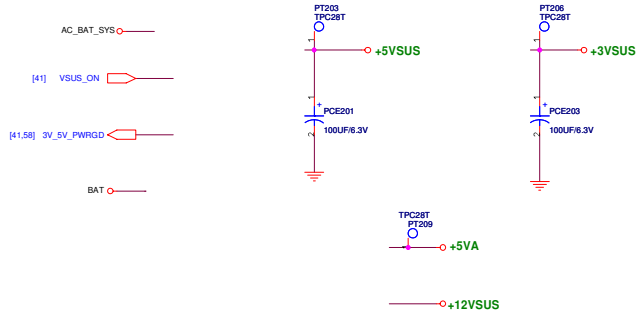
Size	Project Name	Rev
Custom	STD	2.0G

Date: 星期二, 七月 03, 2007 Sheet 48 of 60



VCORE_SEL0	VCORE_SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

Put these elements close to daughter board !!



<Variant Name>

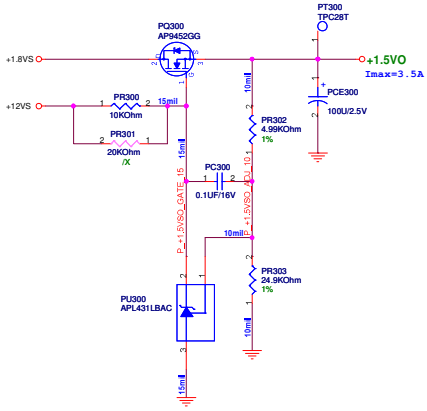
Title : POWER_SYSTEM

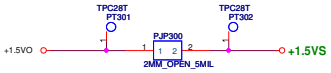
<OrgName> Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

Date: 星期 一, 十月 03, 2007 Sheet 50 of 60

+1.5VS / 3.5A





for CPU(VCCA), NB, SB, Other Devices Power

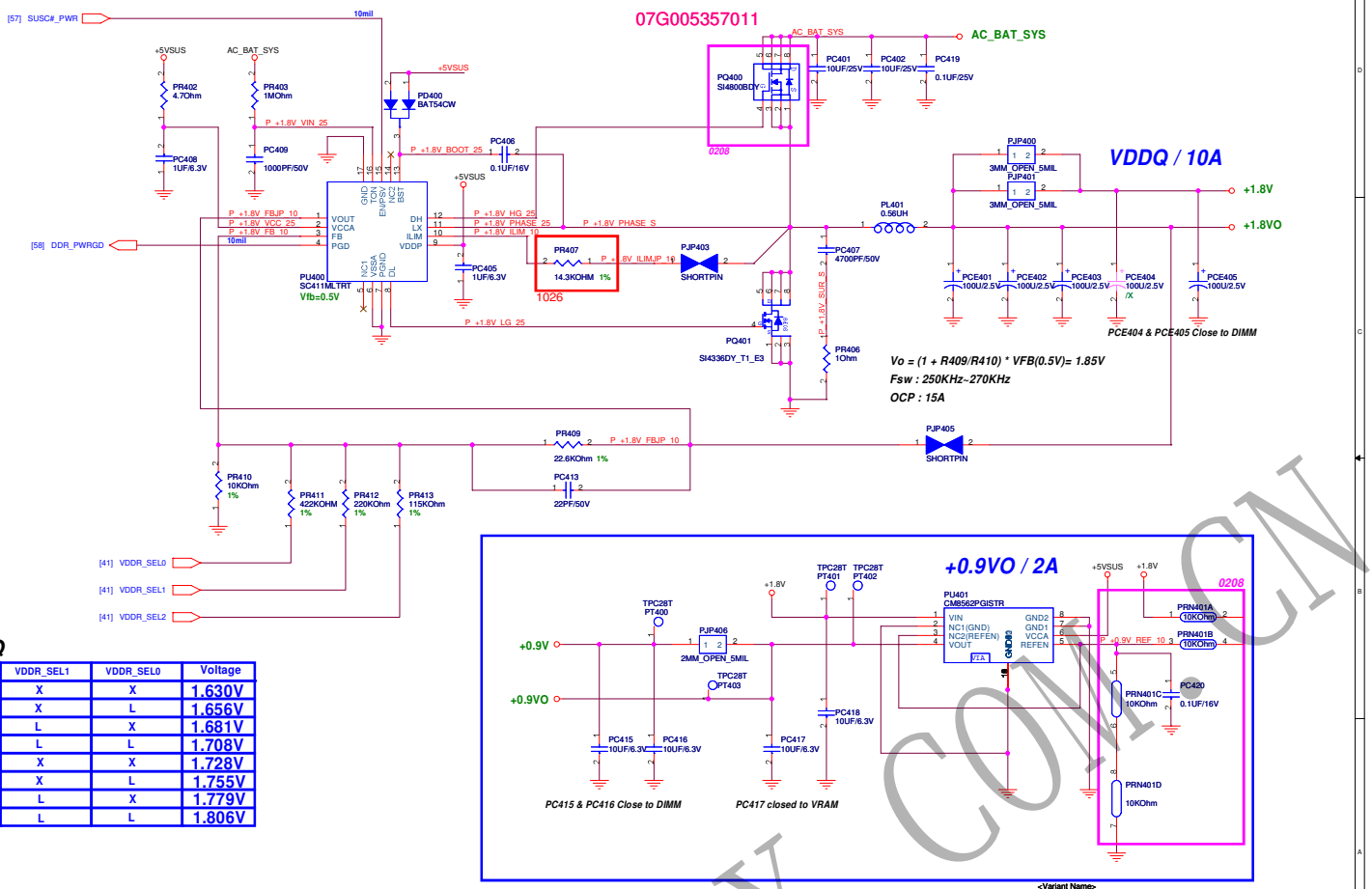
<Variant Name>

ASUS Title :POWER_I/O_1.5VS & 1.05VS

<OrgName> Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

Date: 日期 十月 03, 2007 Sheet 51 of 60



+VDDQ

VDDR_SEL2	VDDR_SEL1	VDDR_SEL0	Voltage
X	X	X	1.630V
X	X	L	1.656V
X	L	X	1.681V
X	L	L	1.708V
L	X	X	1.728V
L	X	L	1.755V
L	L	X	1.779V
L	L	L	1.806V

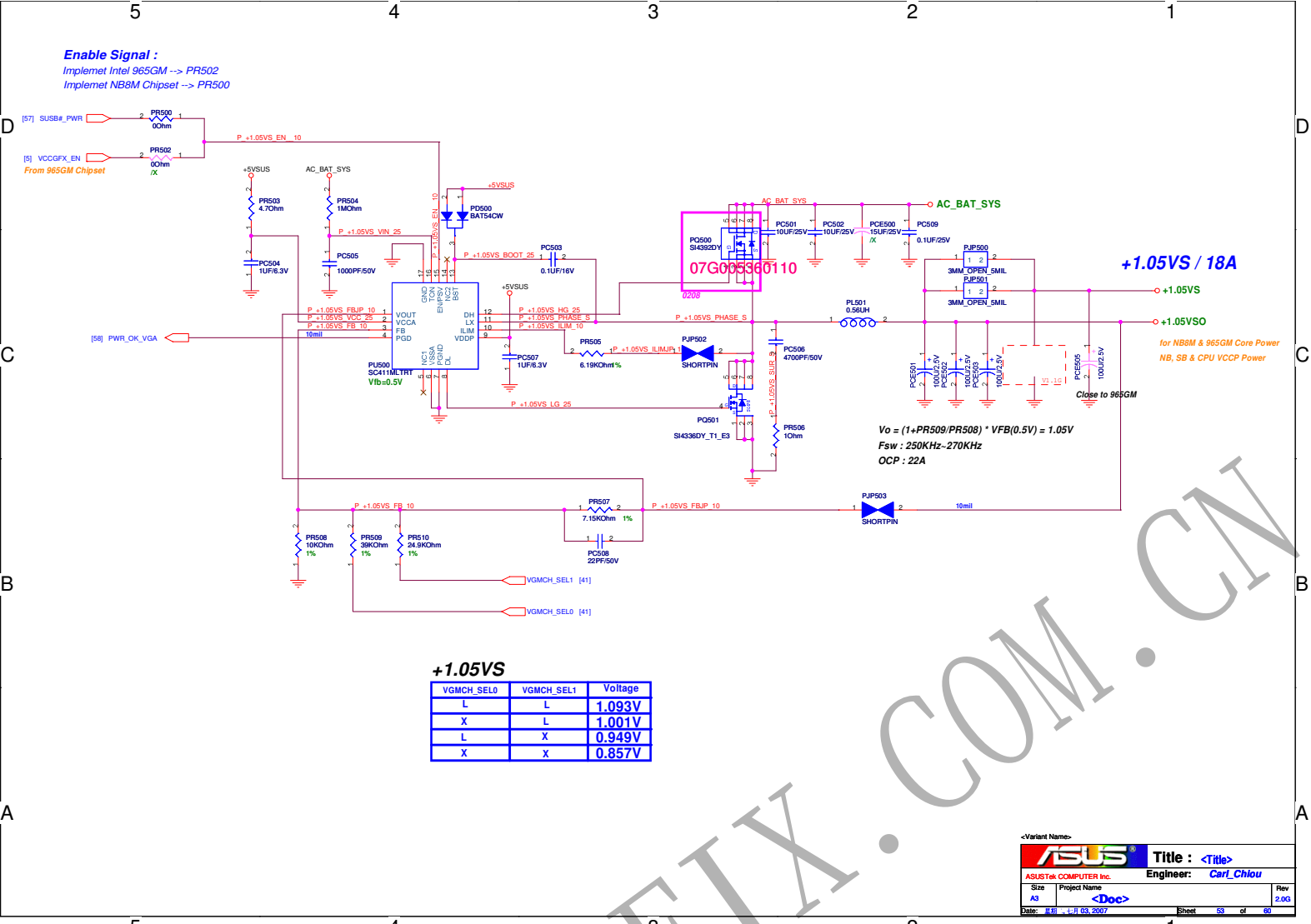
<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName> Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

Date: 星期 一, 十月 03, 2007 Sheet 52 of 60



+1.05VS

VGMCH_SEL0	VGMCH_SEL1	Voltage
L	L	1.093V
X	L	1.001V
L	X	0.949V
X	X	0.857V

<Variant Name>

ASUSTek COMPUTER Inc.

Title : <Title>

Engineer: Carl_Chiou

Size	Project Name	Rev
A3	<Doc>	2.0G

Date: 星期一, 七月 03, 2007 Sheet 53 of 60

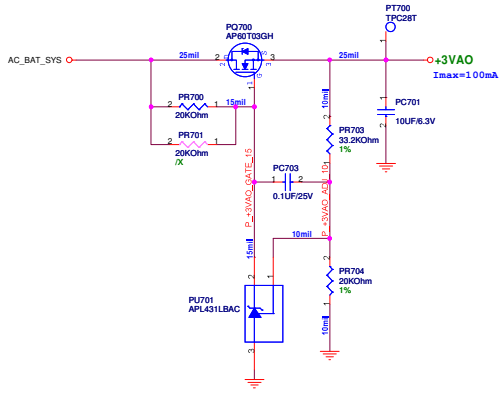
<Variant Name>

Title : POWER_VGA_CORE & RAM

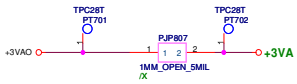
<OrgName> Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

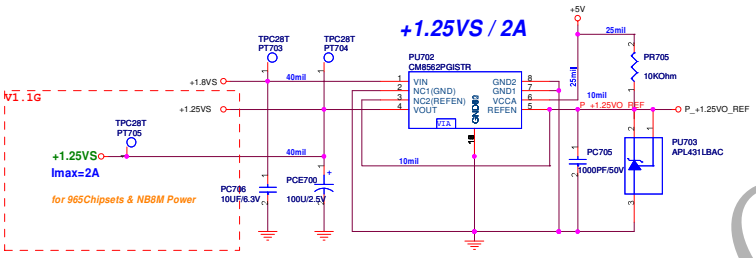
Date: 星期 一, 十月 03, 2007 Sheet 54 of 60



+3VAO / 100mA



+1.25VS / 2A



<Variant Name>

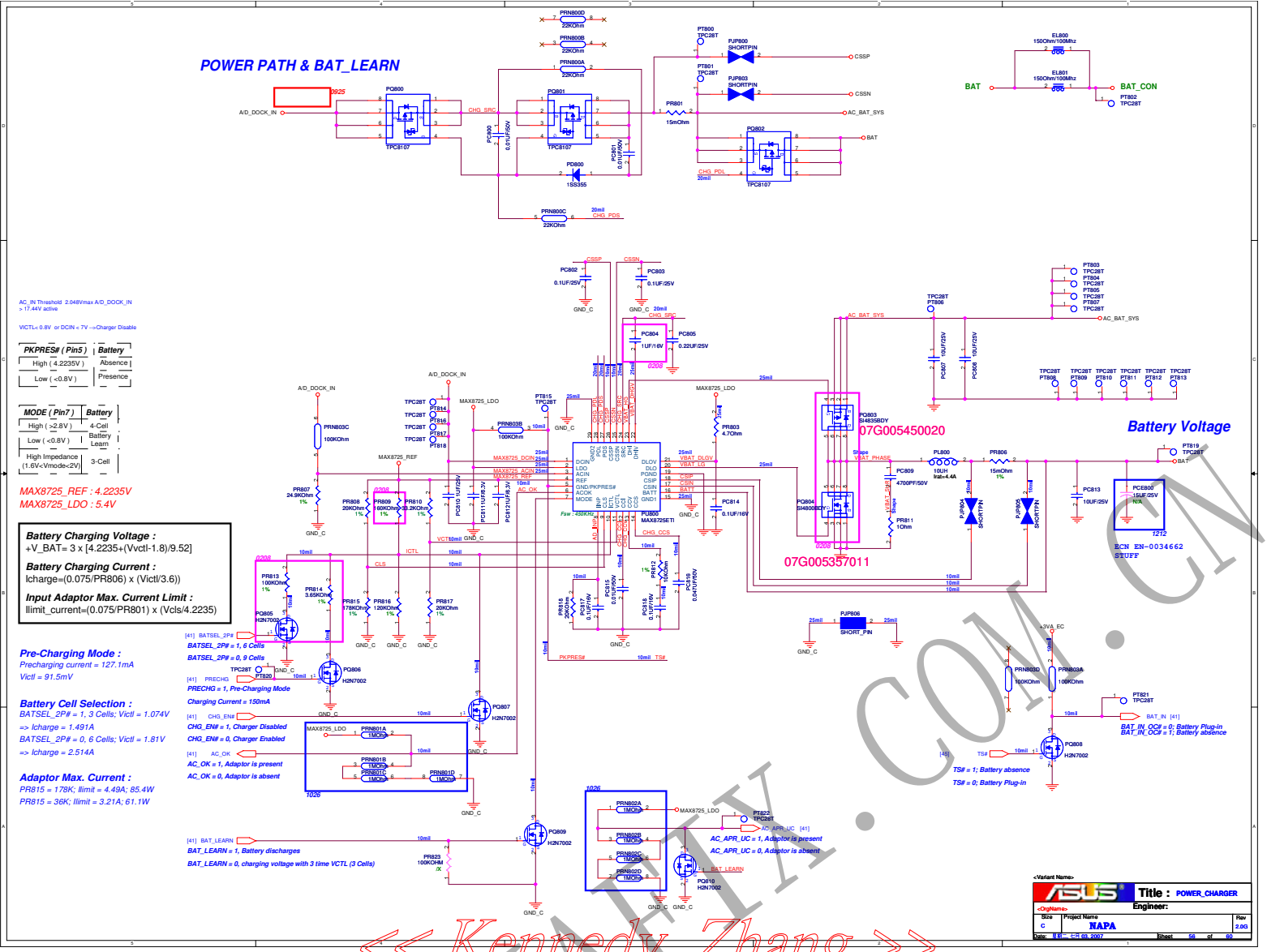
Title : POWER_I/O_+3VA & +2.5V

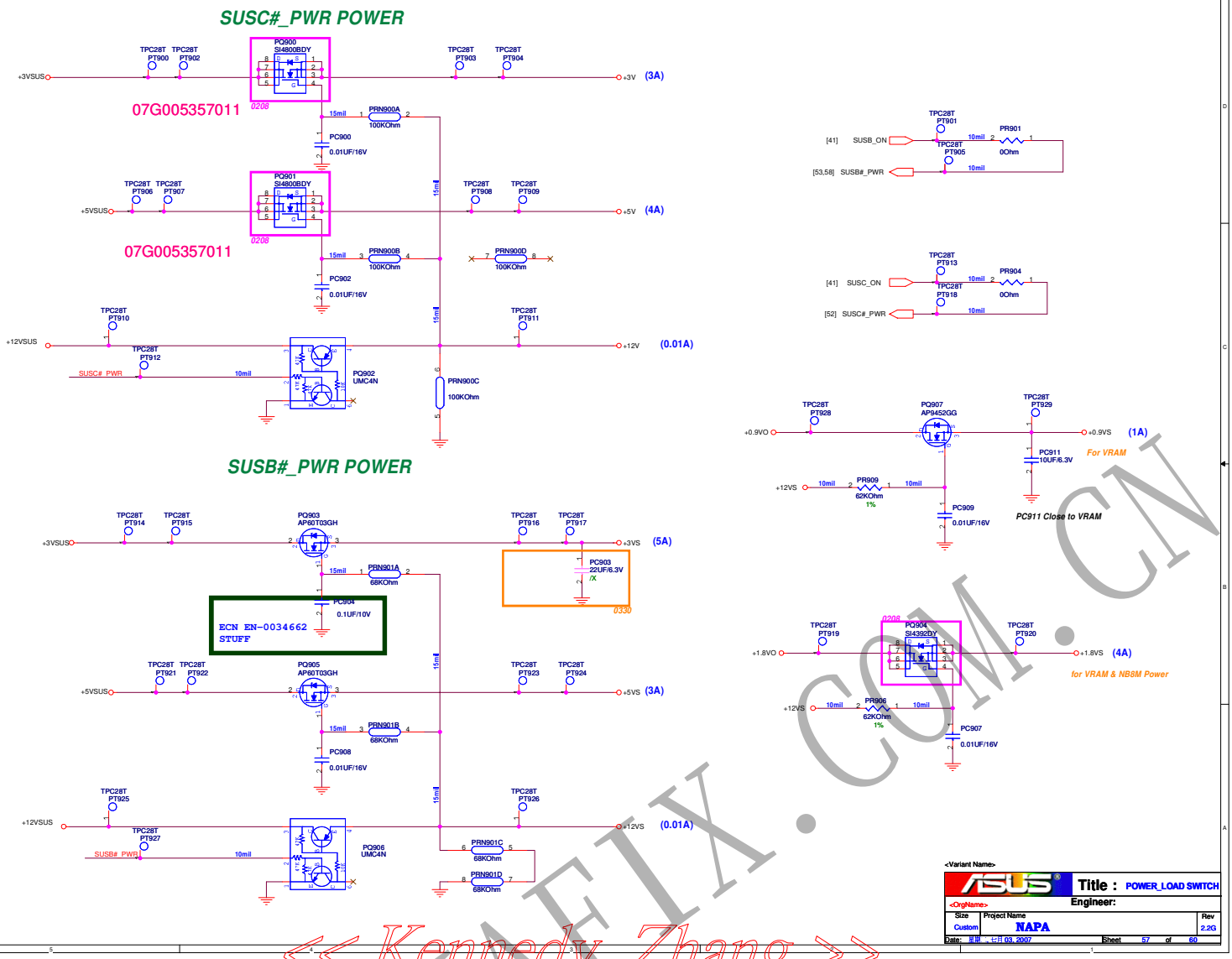
<OrgName>

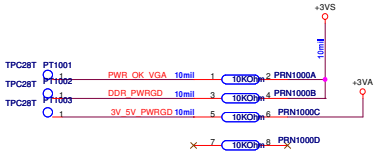
Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

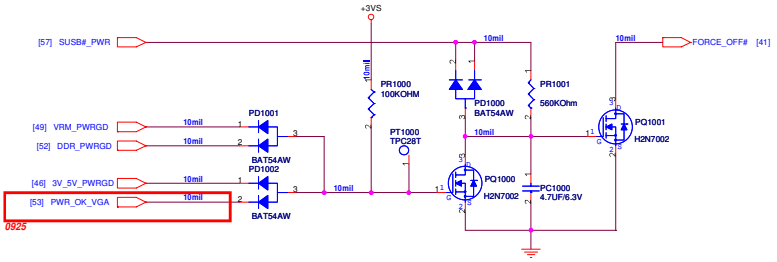
Date: 星期二, 七月 03, 2007 Sheet 55 of 60

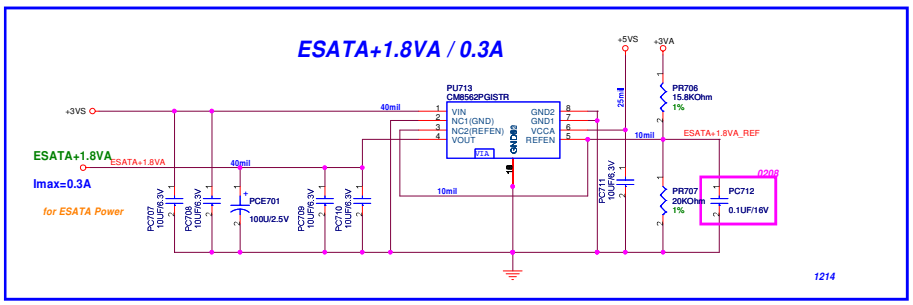






Power Good Detecter





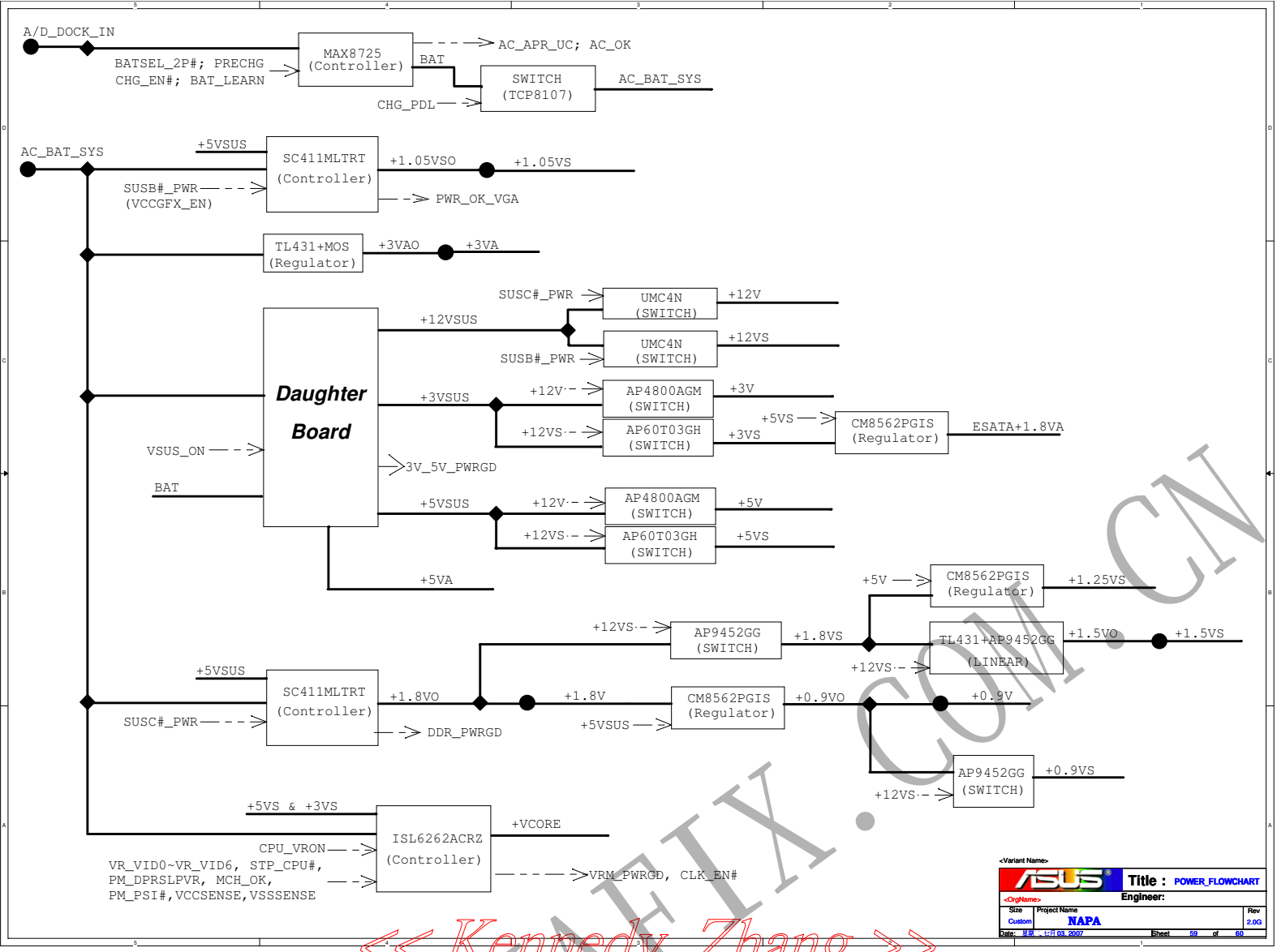
<Variant Name>

Title : POWER_DETECT

<OrgName> Engineer:

Size	Project Name	Rev
A3	NAPA	2.0G

Date: 星期 一, 十月 03, 2007 Sheet 58 of 60



<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer: Carl_Chiou

Size	Project Name	Rev
Custom	NAPA	2.0G

Date: 星期二, 七月 03, 2007 Sheet 60 of 60