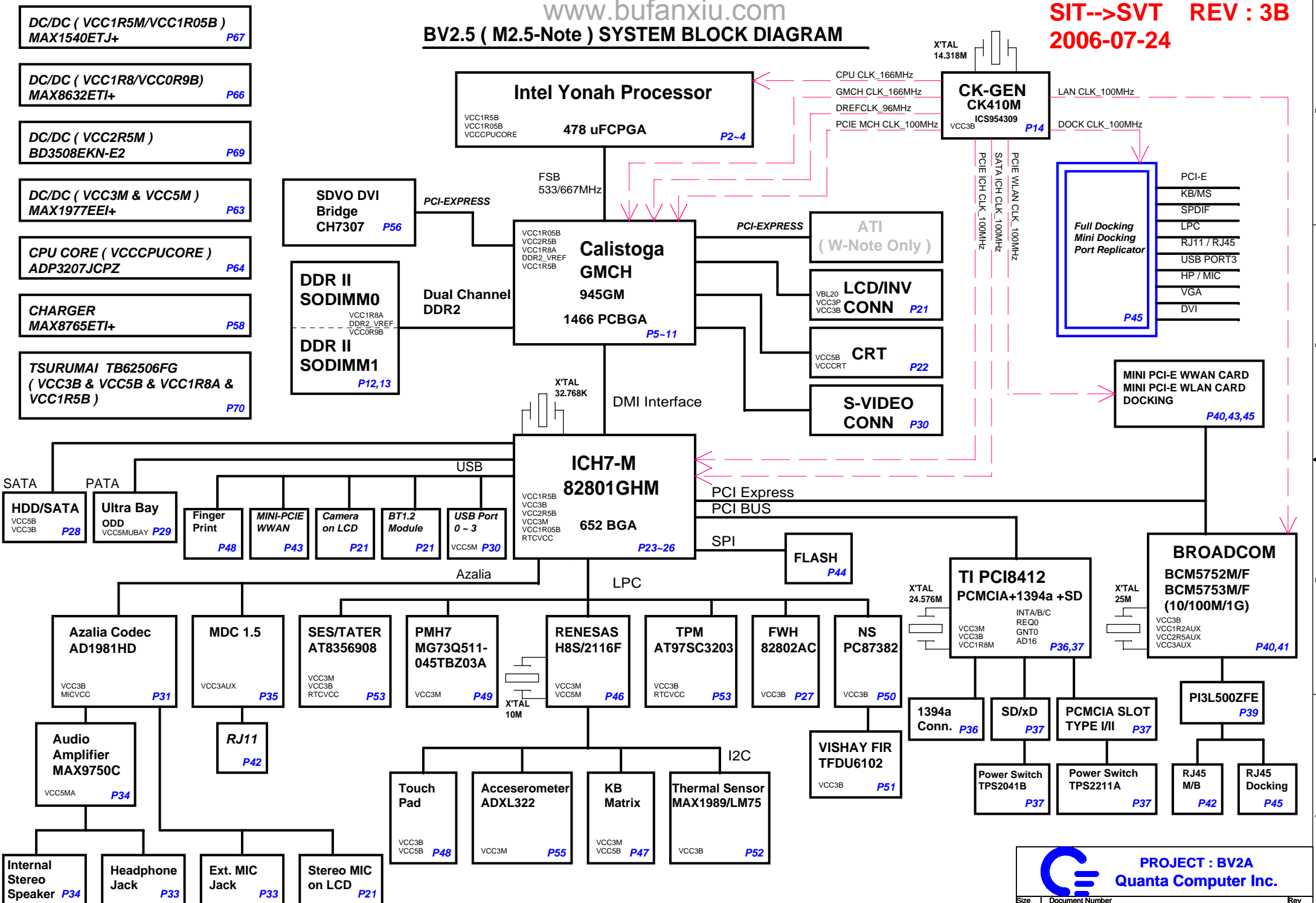
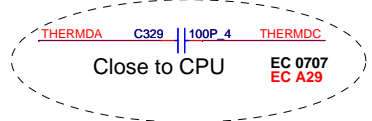
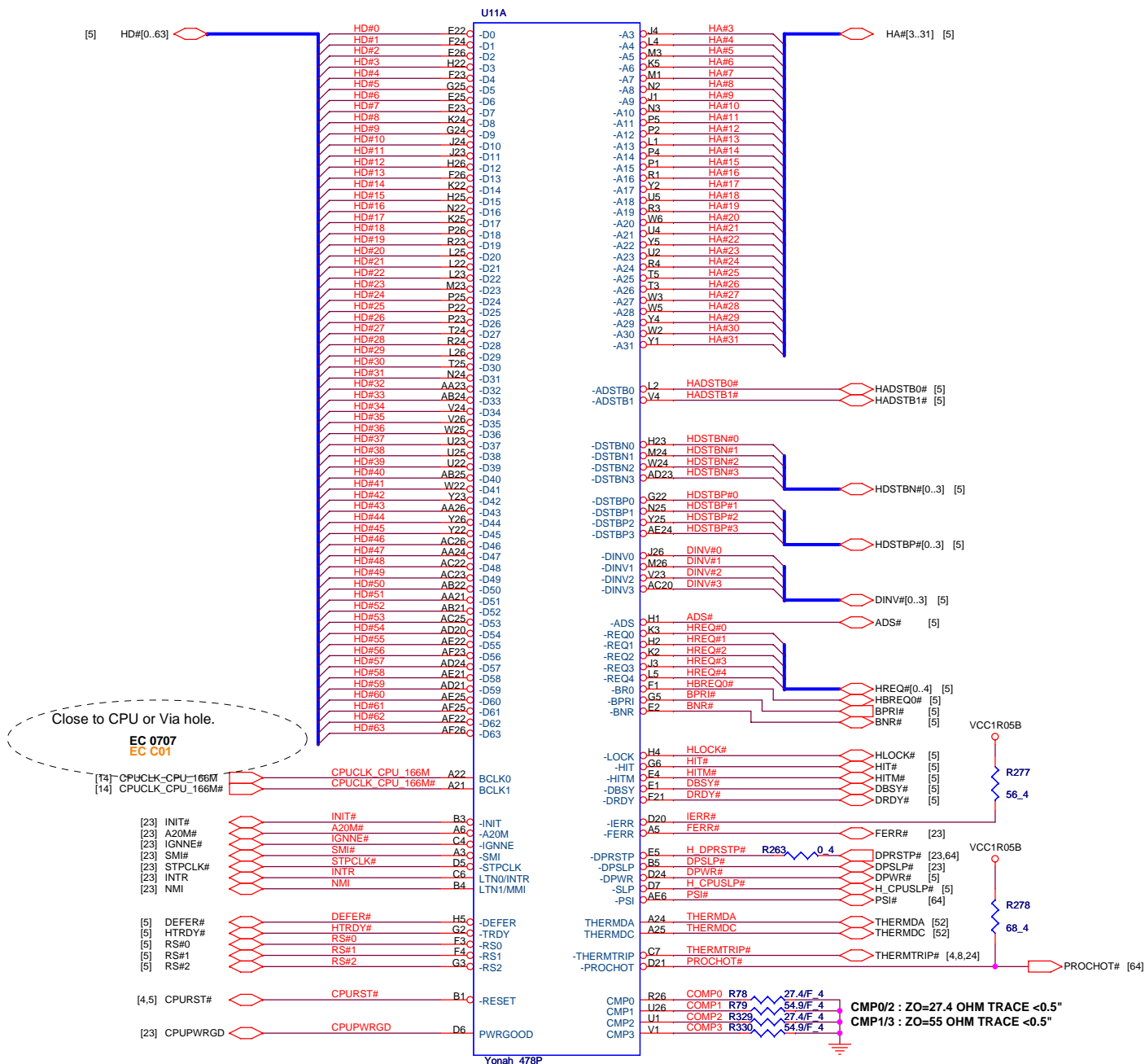


BV2.5 (M2.5-Note) SYSTEM BLOCK DIAGRAM

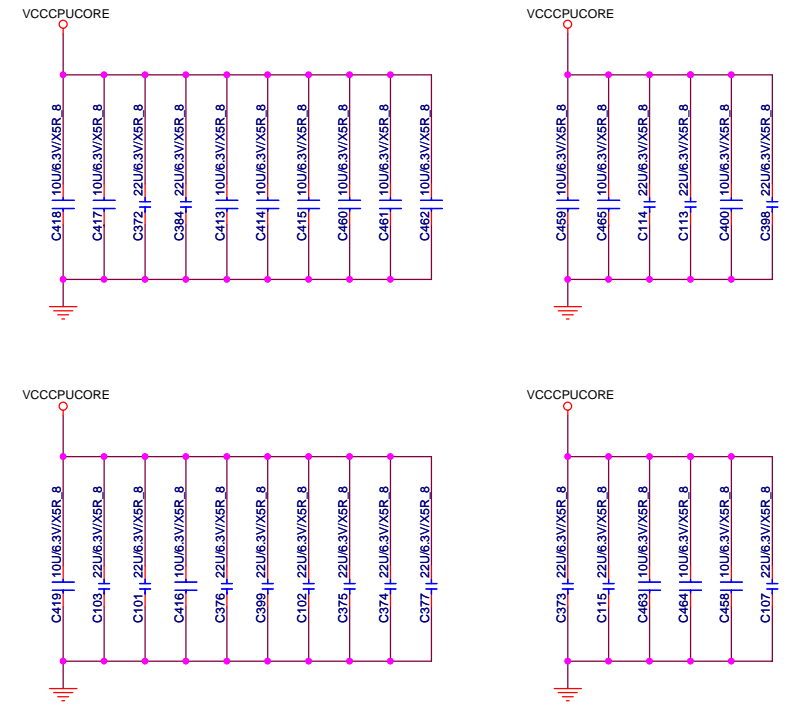
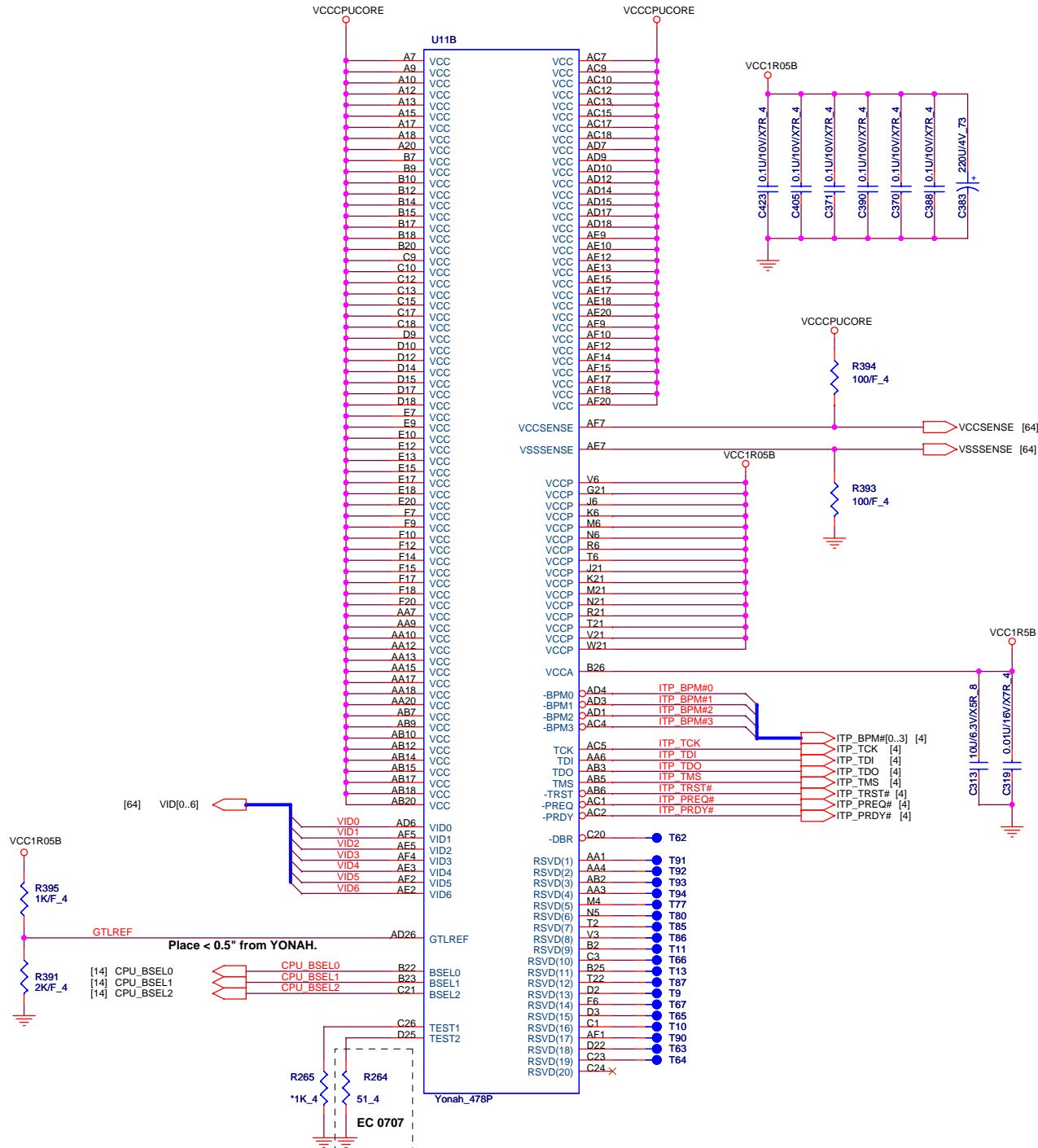
SIT-->SVT REV : 3B
2006-07-24



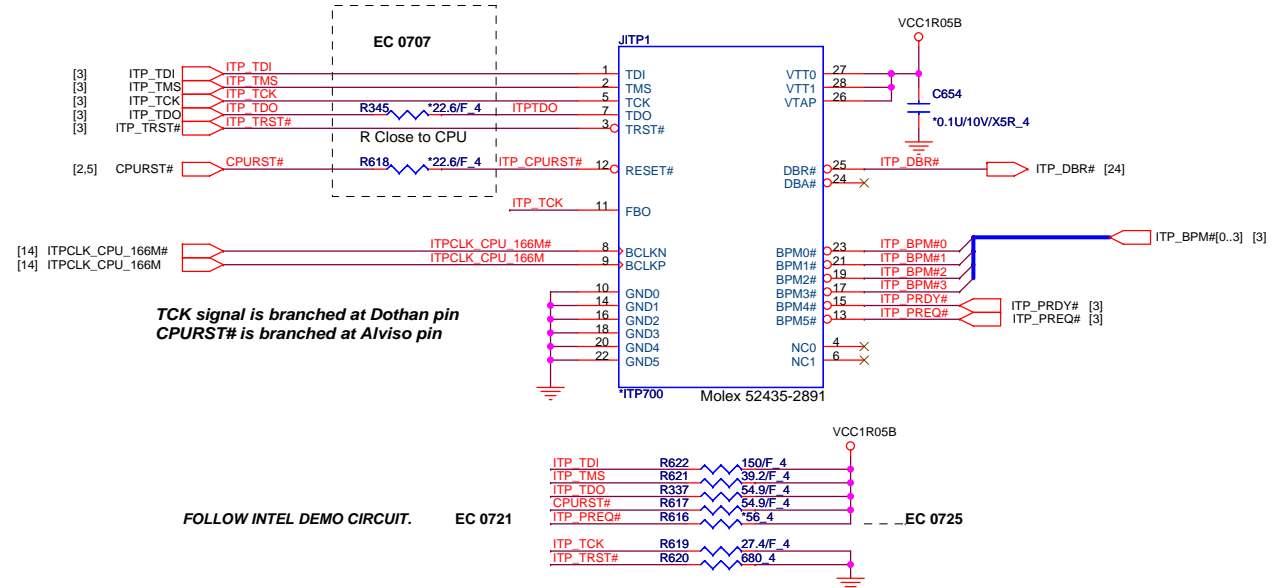
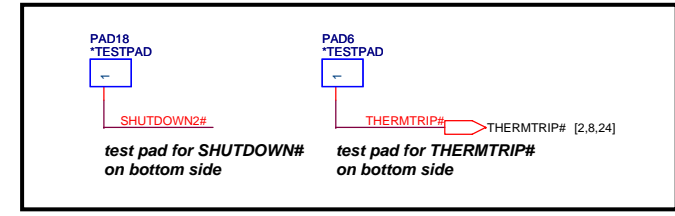
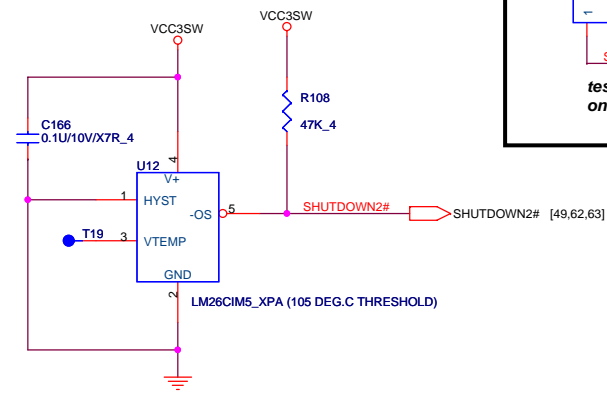
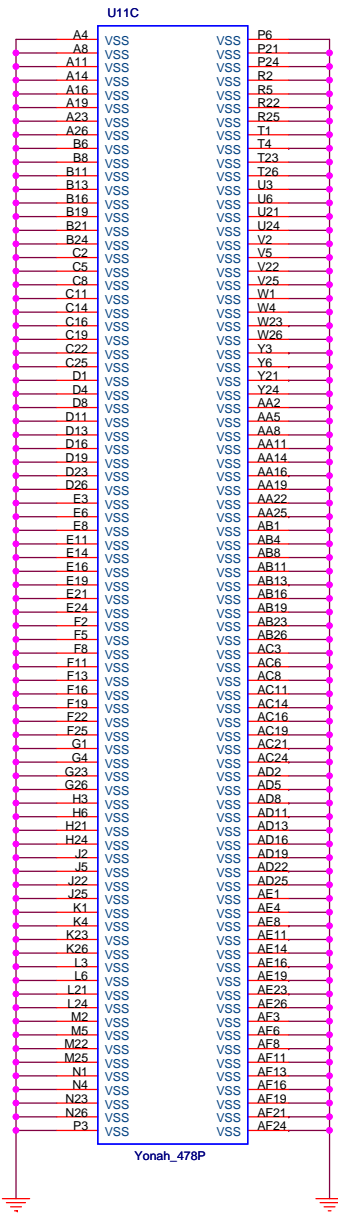


VCCCPUCORE DECOUPLING

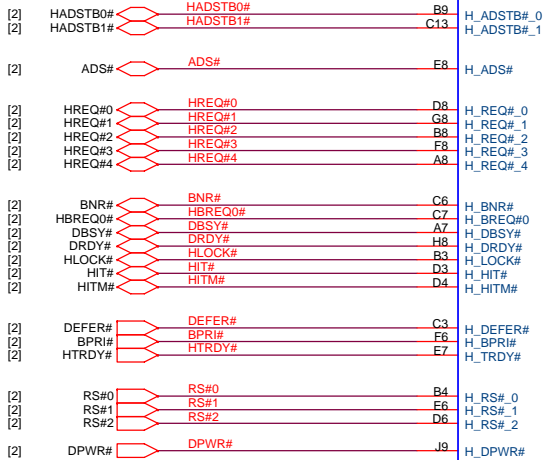
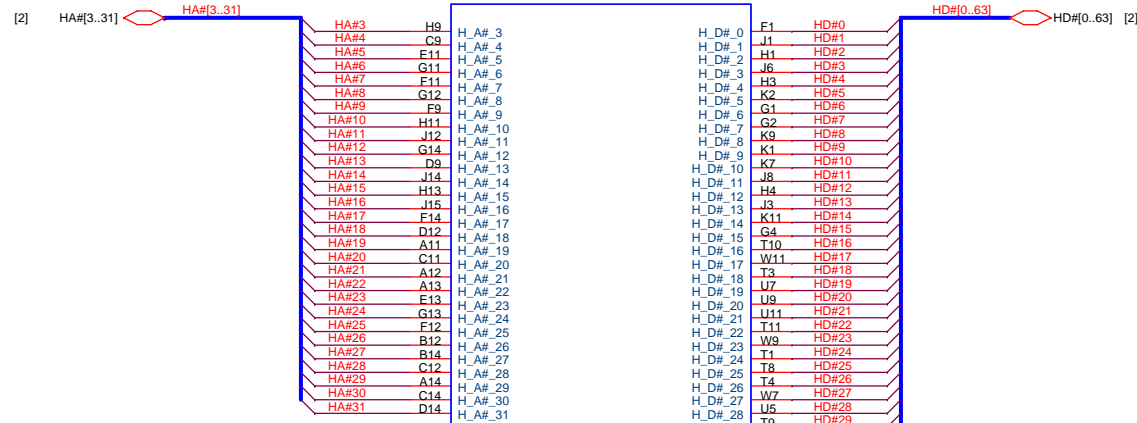
03



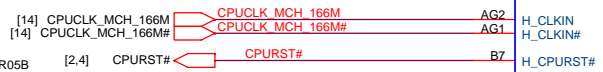
EC A-18 22UF 6.3V X5R 2125(0805) 1/16W X16 PCS
 10UF 6.3V X5R 2125(0805) X16 PCS



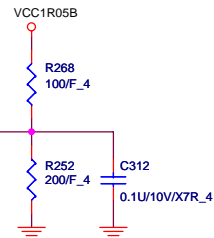
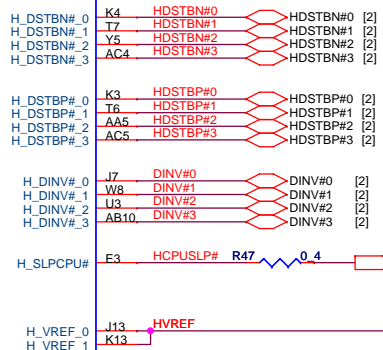
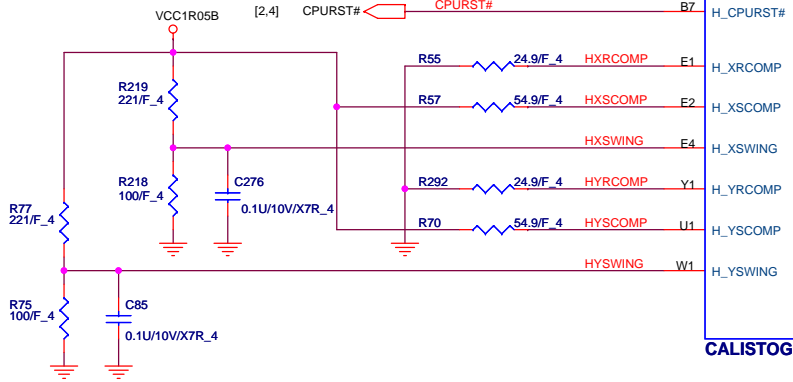
U9A

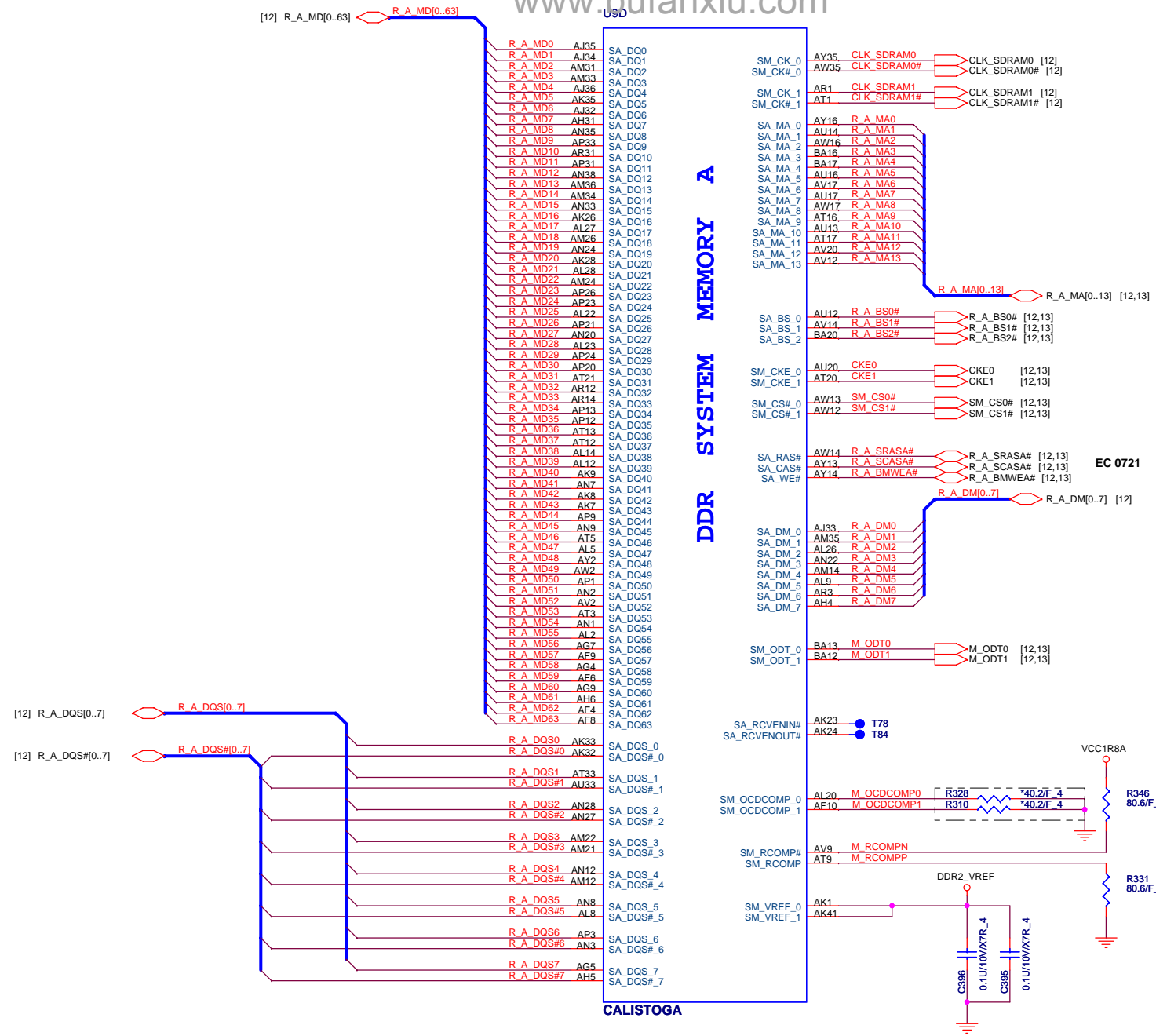


HOST



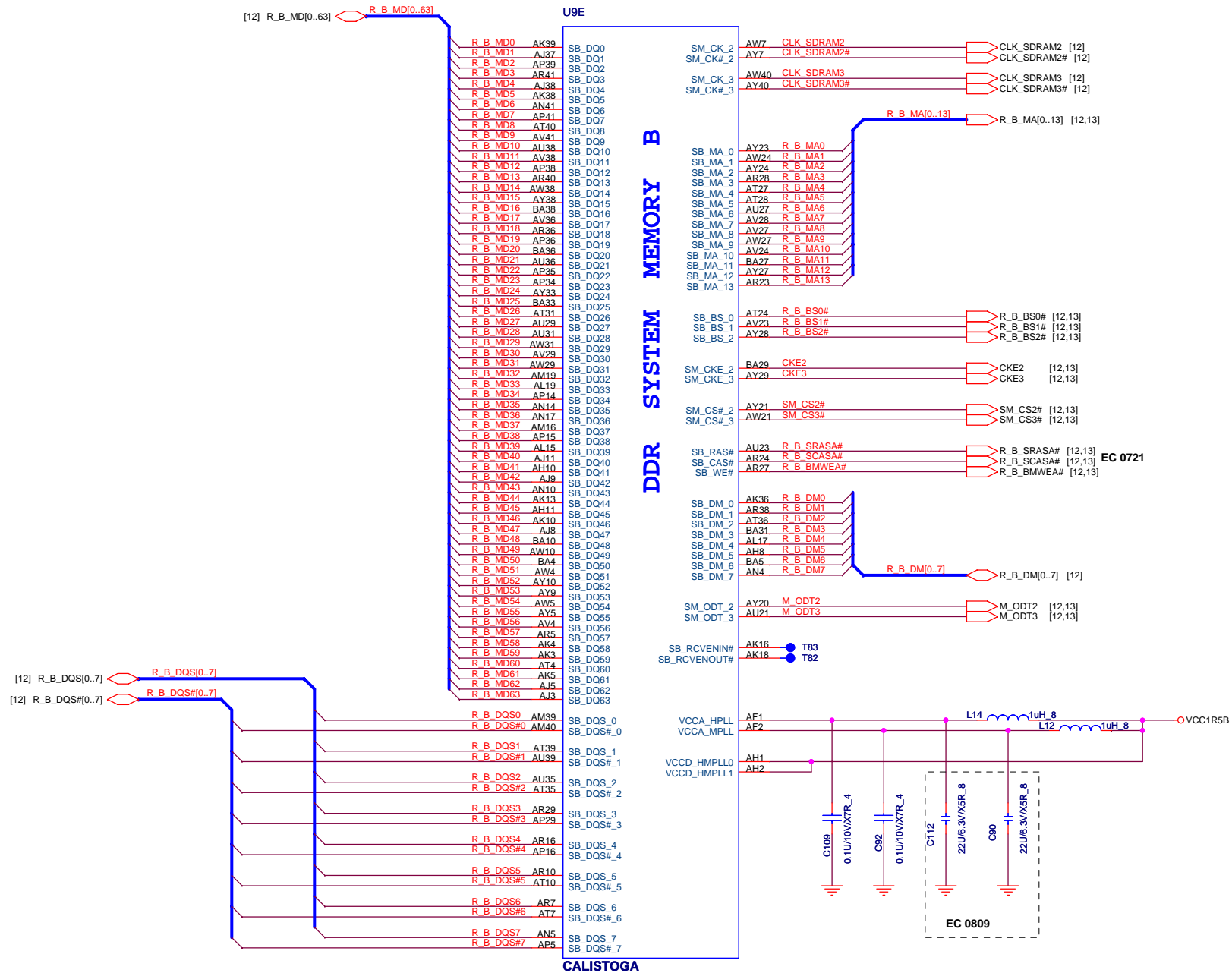
CALISTOGA

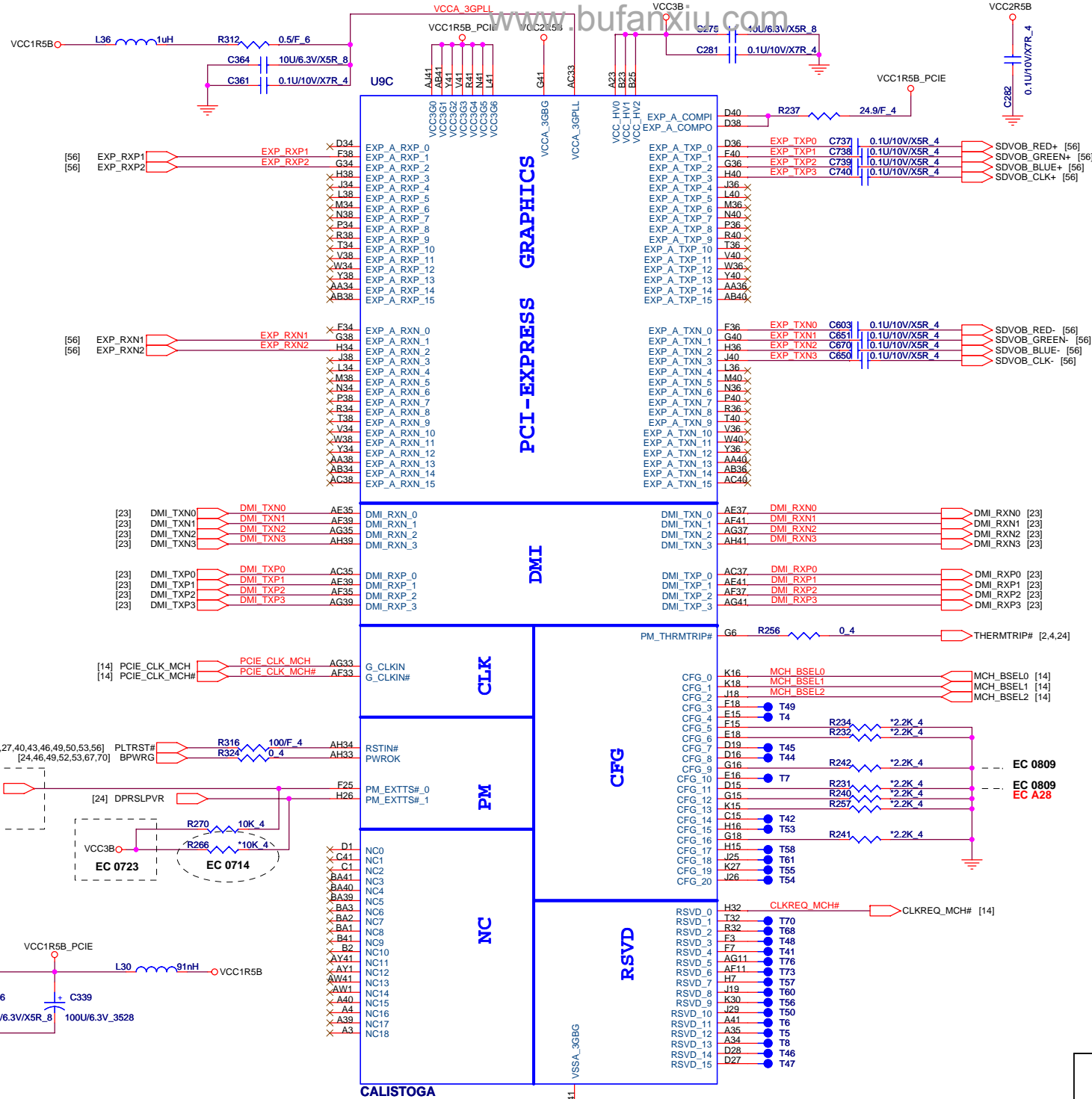




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Quanta Computer Inc.

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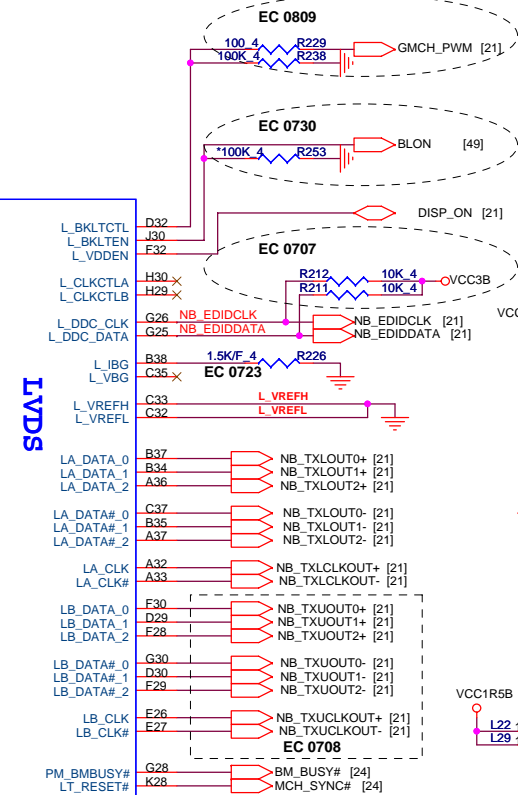
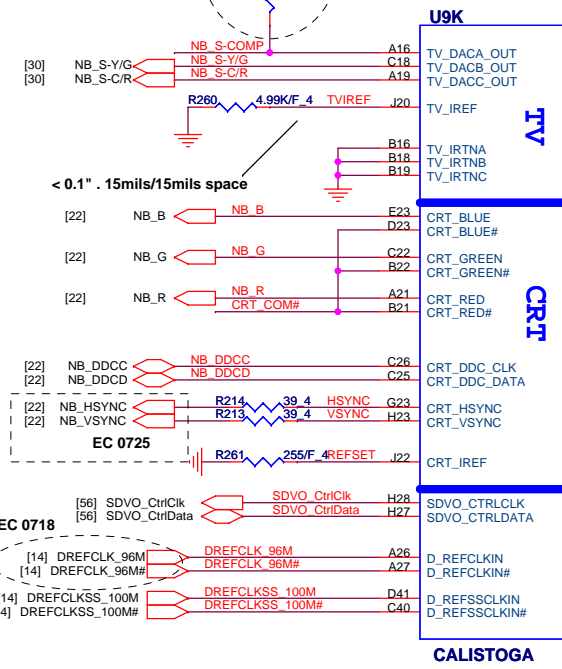
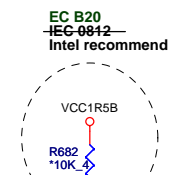
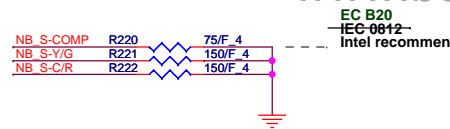
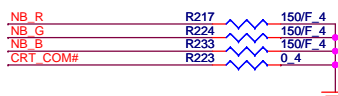




	Low	NO_ASM
CFG5	DMix2	DMix4
CFG6	MOBY DISK	CALISTOGA
CFG9	Reverse Lane	Normal Operation
CFG11	MOBY DISK	CALISTOGA
CFG12	00 : Reserved	
CFG13	01 : XOR Mode Enabled	
	10 : All Z Mode Enabled	
	11 : Normal Operation	
CFG16	FSB Dynamic ODT Disabled	FSB Dynamic ODT Enabled

CFG9 : PCI-E Graphics Lane
 Note : If in integrated GFX mode, need to use lane-reversal ADD2 add-in card since SDVO I/O does not support lane reversal.

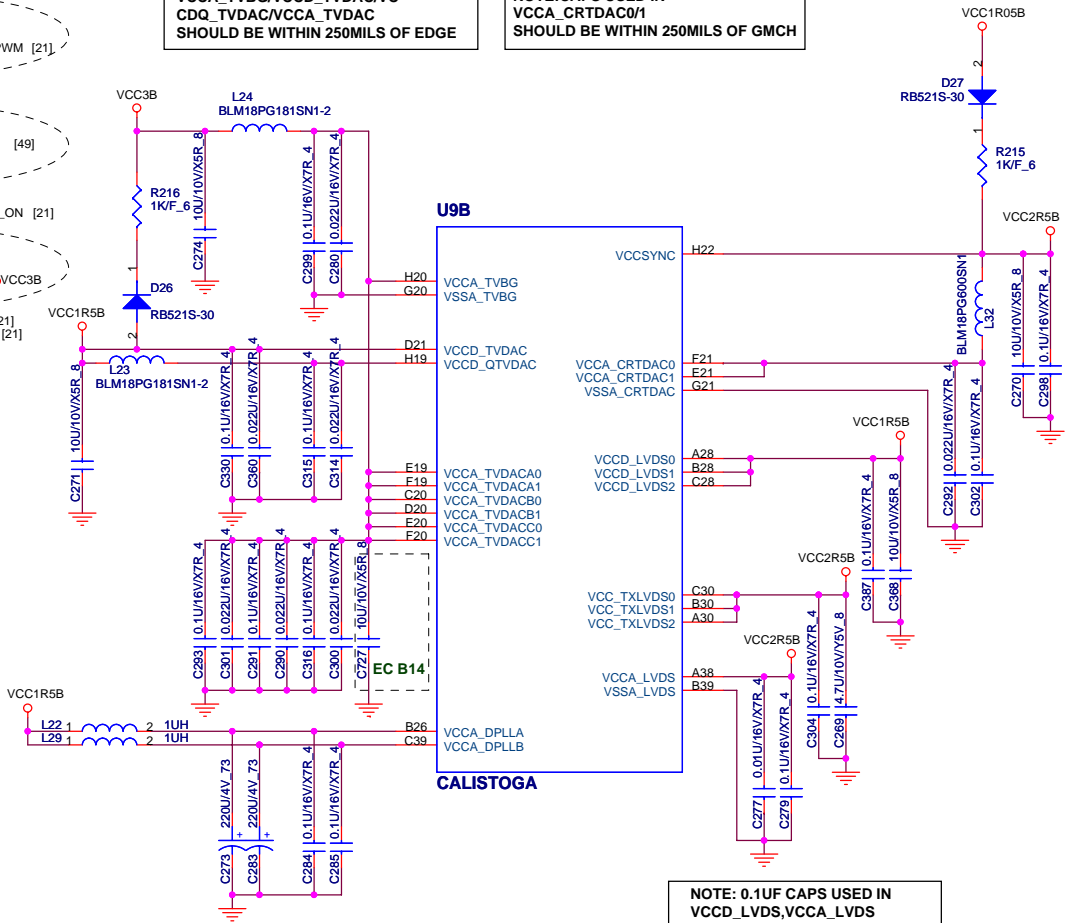
CFG[17:3] INTERNAL PULLUP
 CFG[20:18] INTERNAL PULLDOWN



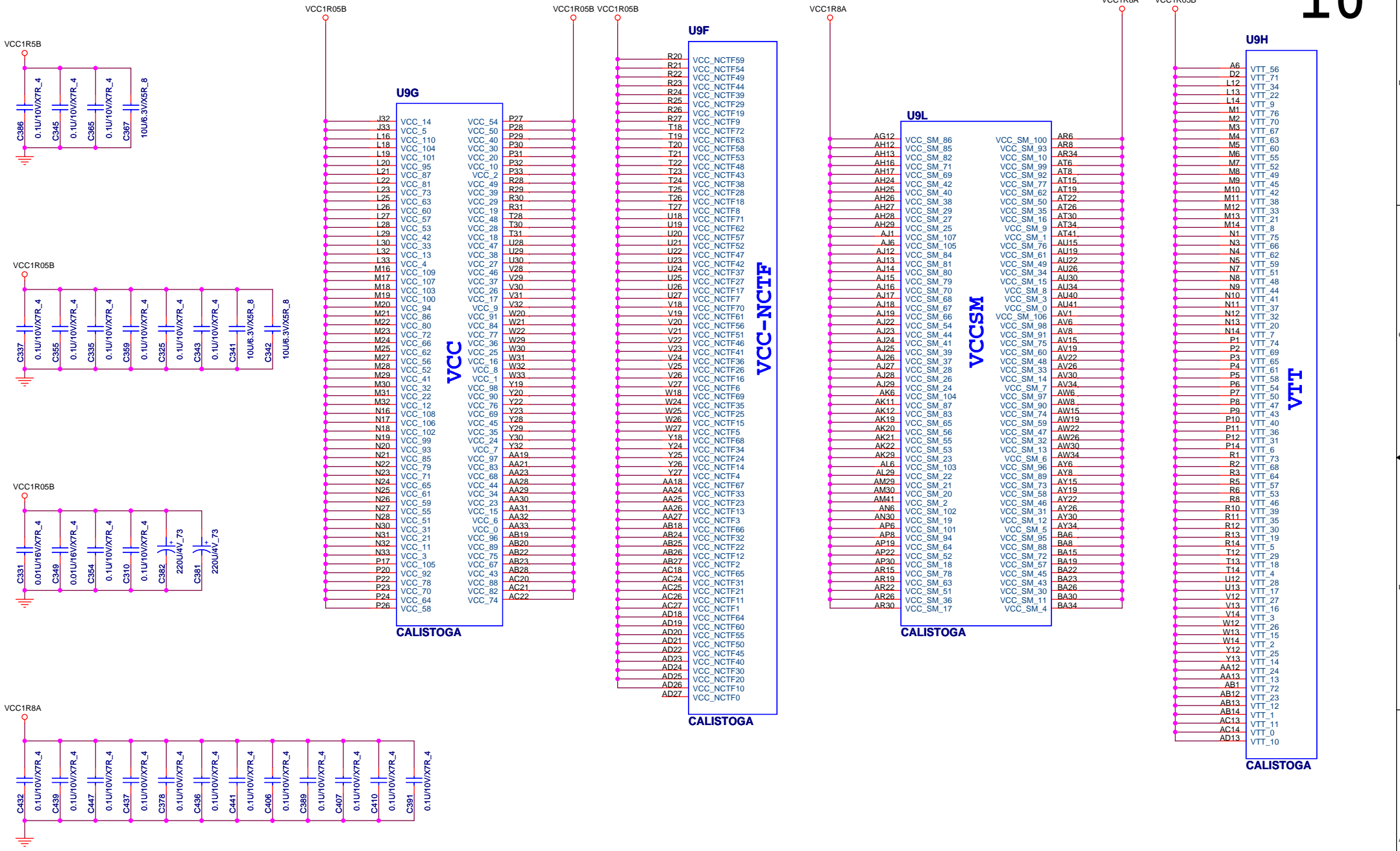
NOTE: 0.1UF CAPS NEED TO BE LOCATED AS EDGE CAPS WITHIN 200MILS

NOTE: CAPS USED IN VCCA_TVBG/VCCD_TV DAC/VCCD_TV DAC/VCCA_TV DAC SHOULD BE WITHIN 250MILS OF EDGE

NOTE: CAPS USED IN VCCA_CRTDAC0/1 SHOULD BE WITHIN 250MILS OF GMCH



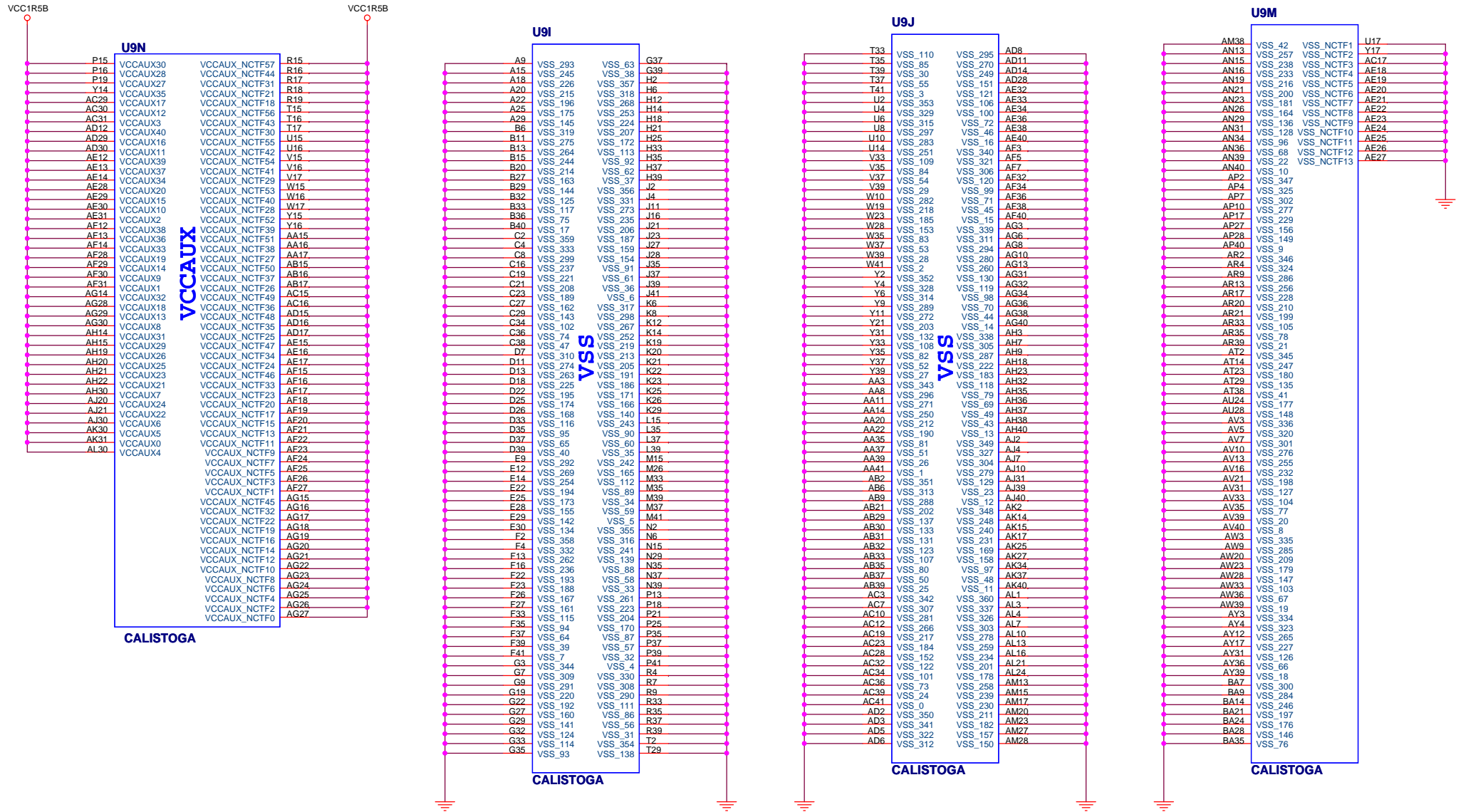
NOTE: 0.1UF CAPS USED IN VCCD_LVDS, VCCA_LVDS, VCC_TX LVDS SHOULD BE PLACED WITHIN 200MILS EDGE

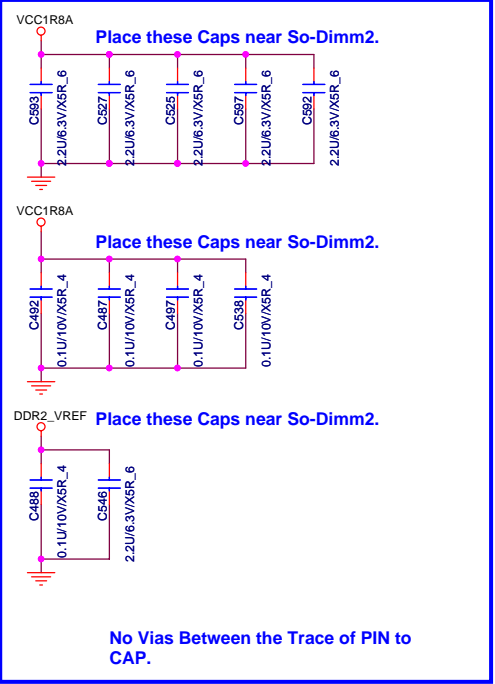
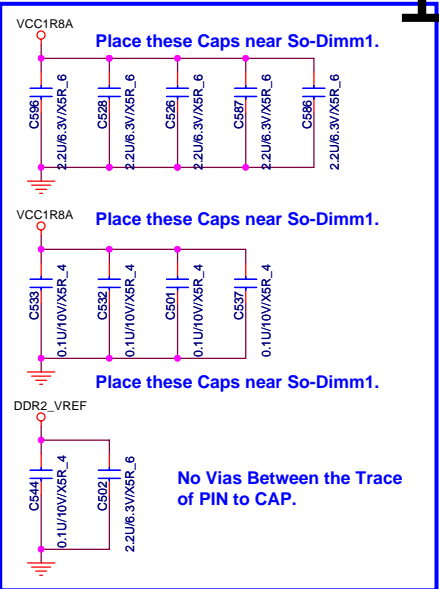
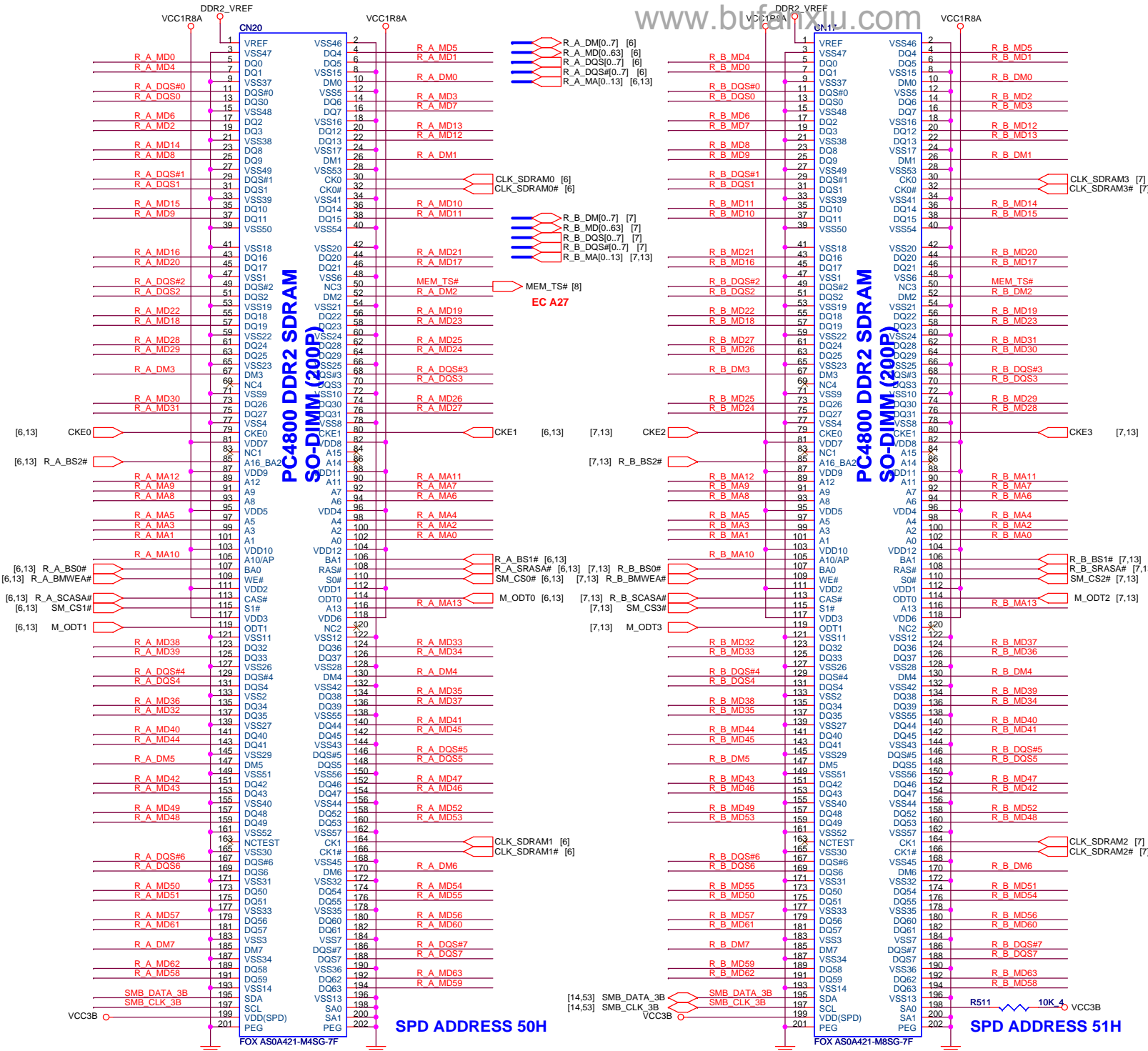


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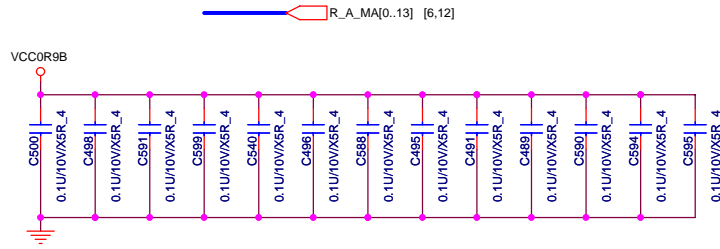
CLOCK 0,1
CKE 0,1

CLOCK 3,4
CKE 2,3

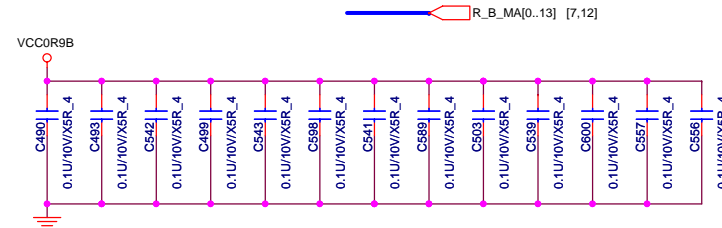
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DDRII DUAL CHANNEL A,B.

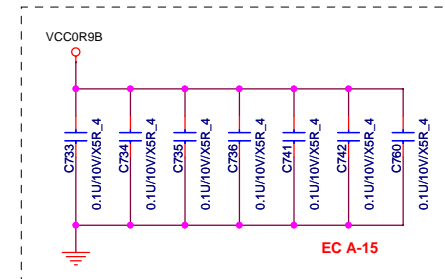
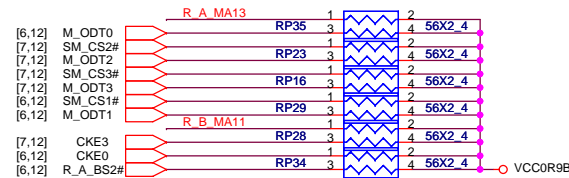
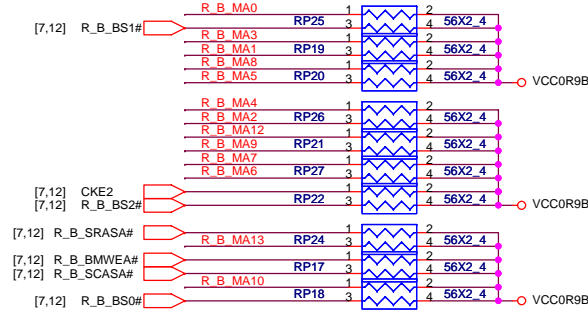
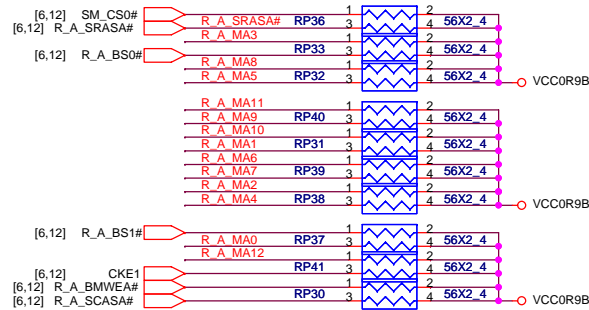
DDRII A CHANNEL

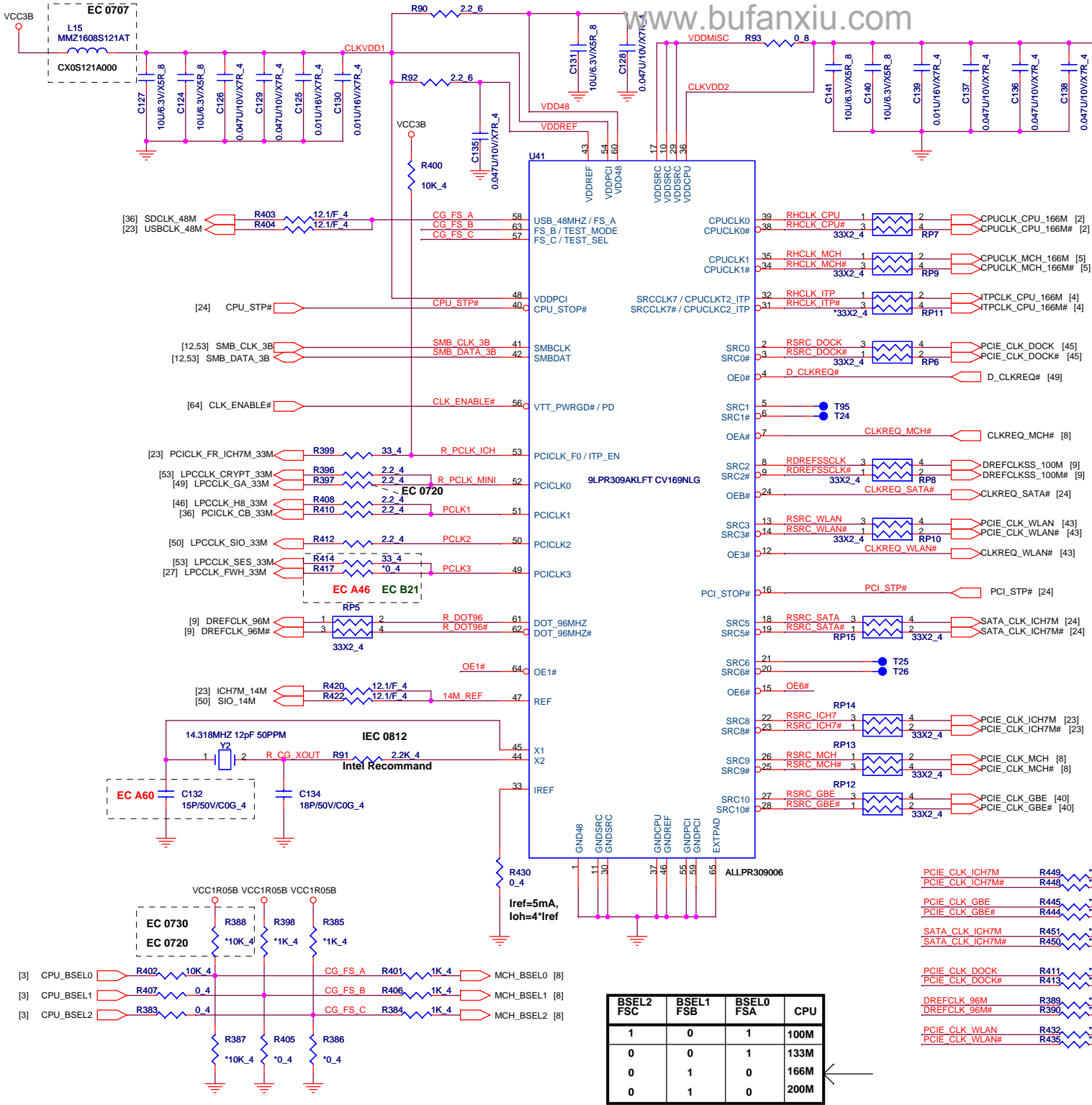


DDRII B CHANNEL

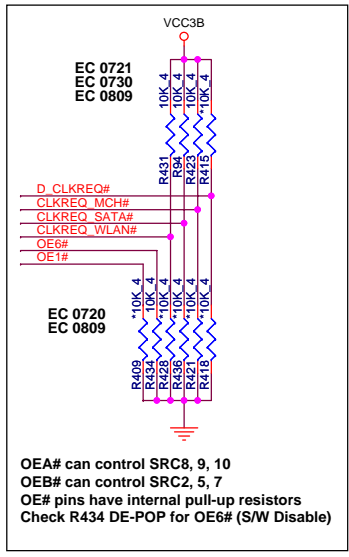


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





EC A26	Supplier	Part number	R389, R390, R411, R413, R424, R425, R426, R427, R429, R432, R433, R435, R444, R445, R446, R447, R448, R449, R450, R451	R430
ICS	IDT	954309B CV150	ASM	475 ohm
ICS	Cypress	9LPR309 CY28446 CV169NGLG	NO ASM	0 ohm




OEA# can control SRC8, 9, 10
 OEB# can control SRC2, 5, 7
 OE# pins have internal pull-up resistors
 Check R434 DE-POP for OE6# (S/W Disable)


- CPULCK CPU 166M R425 *49.9/F 4
- CPULCK CPU 166M# R426 *49.9/F 4
- CPULCK MCH 166M R429 *49.9/F 4
- CPULCK MCH 166M# R433 *49.9/F 4
- ITPCLK CPU 166M R442 *49.9/F 4
- ITPCLK CPU 166M# R443 *49.9/F 4
- PCIE CLK MCH R446 *49.9/F 4
- PCIE CLK MCH# R447 *49.9/F 4
- DREFCLKSS 100M R424 *49.9/F 4
- DREFCLKSS 100M# R427 *49.9/F 4
- PCIE CLK DOCK R411 *49.9/F 4
- PCIE CLK DOCK# R413 *49.9/F 4
- DREFCLK 96M R389 *49.9/F 4
- DREFCLK 96M# R390 *49.9/F 4
- PCIE CLK WLAN R432 *49.9/F 4
- PCIE CLK WLAN# R435 *49.9/F 4
- PCIE CLK ICH7M R449 *49.9/F 4
- PCIE CLK ICH7M# R448 *49.9/F 4
- PCIE CLK GBE R445 *49.9/F 4
- PCIE CLK GBE# R444 *49.9/F 4
- SATA CLK ICH7M R451 *49.9/F 4
- SATA CLK ICH7M# R450 *49.9/F 4

BSEL2 F5C	BSEL1 F5B	BSEL0 F5A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	166M
0	1	0	200M


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		Quanta Computer Inc.	
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BLANK

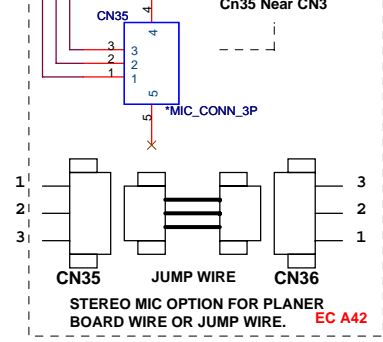
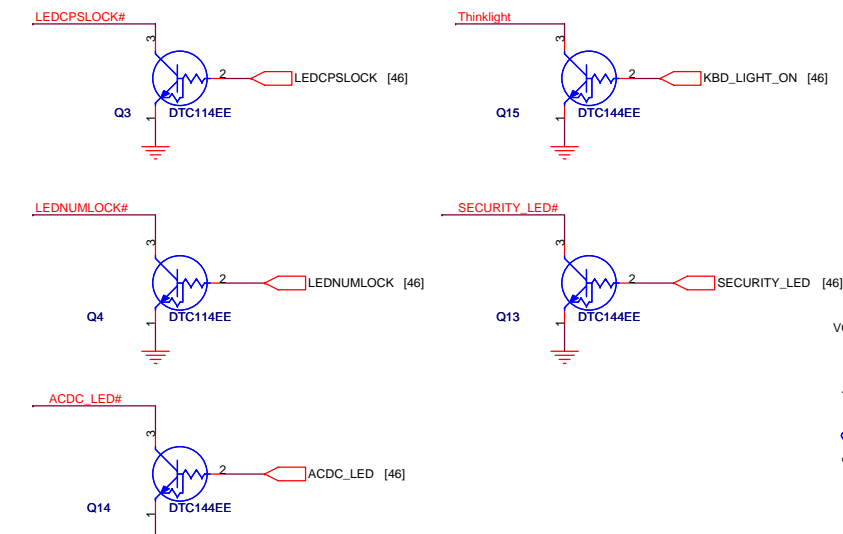
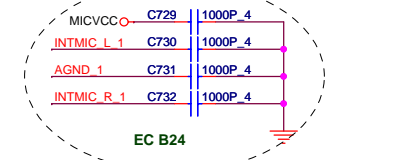
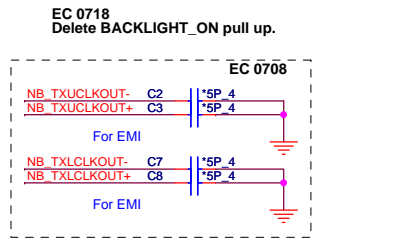
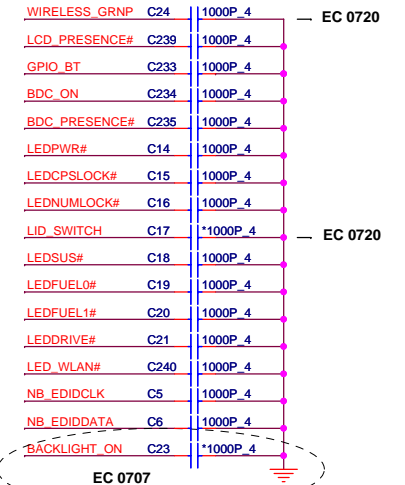
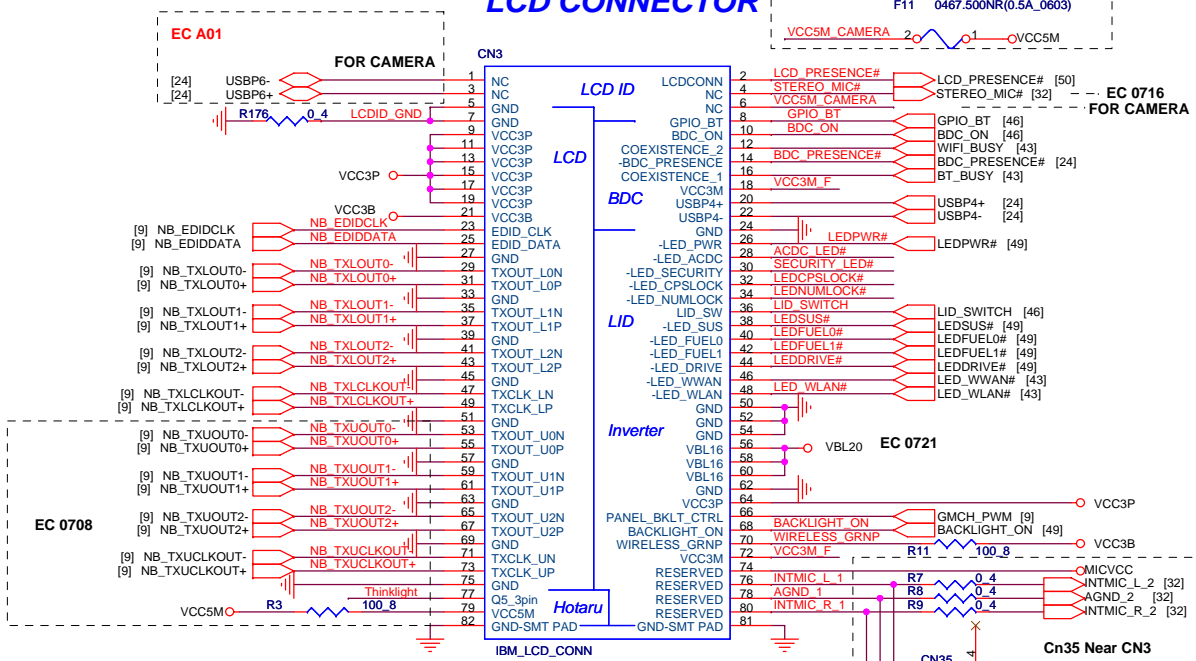
		PROJECT : BV2A Quanta Computer Inc.
Size Custom	Document Number BLANK	Rev 3B
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BLANK

		PROJECT : BV2A	
		Quanta Computer Inc.	
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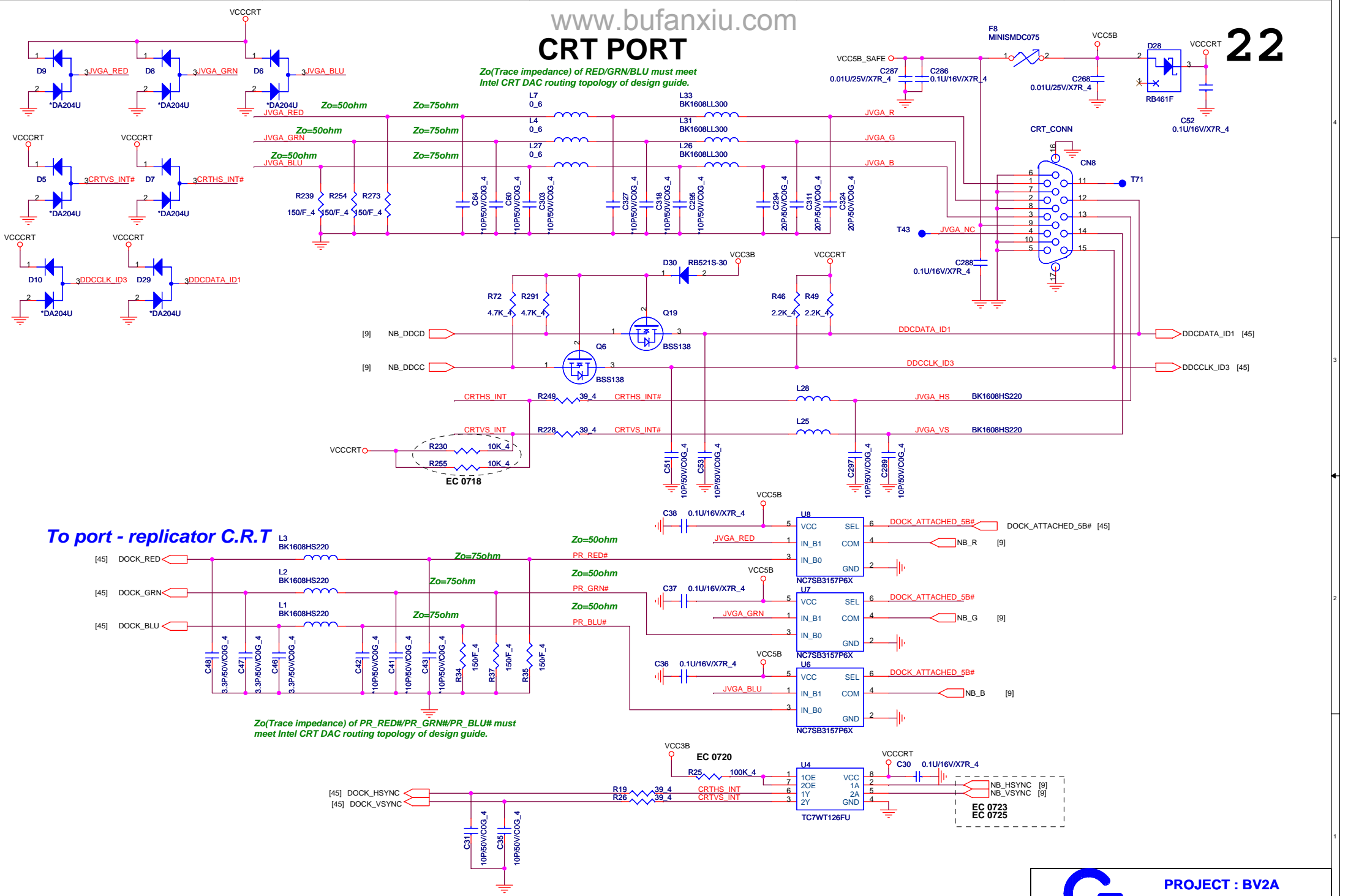
BLANK

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		Quanta Computer Inc.	
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CRT PORT

Zo(Trace impedance) of RED/GRN/BLU must meet Intel CRT DAC routing topology of design guide.



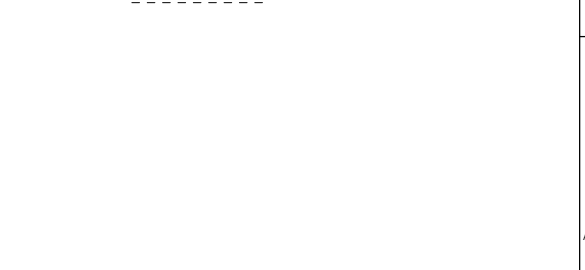
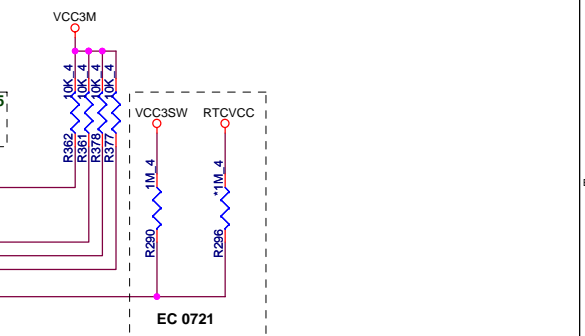
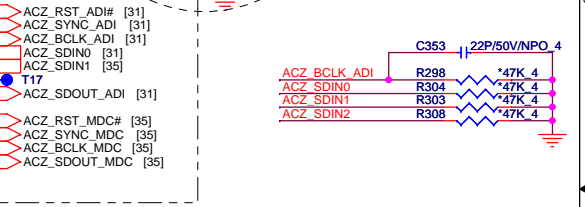
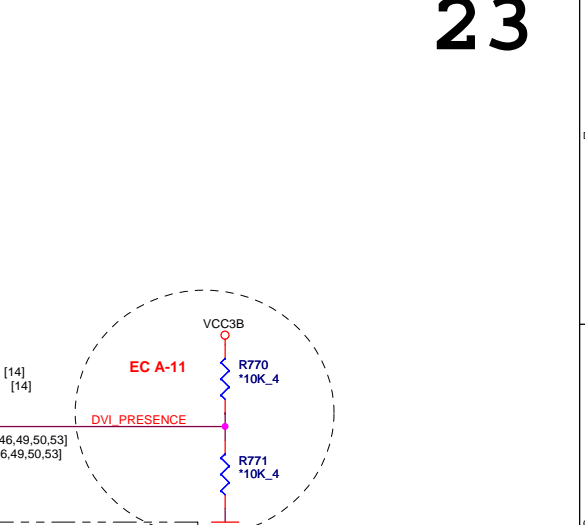
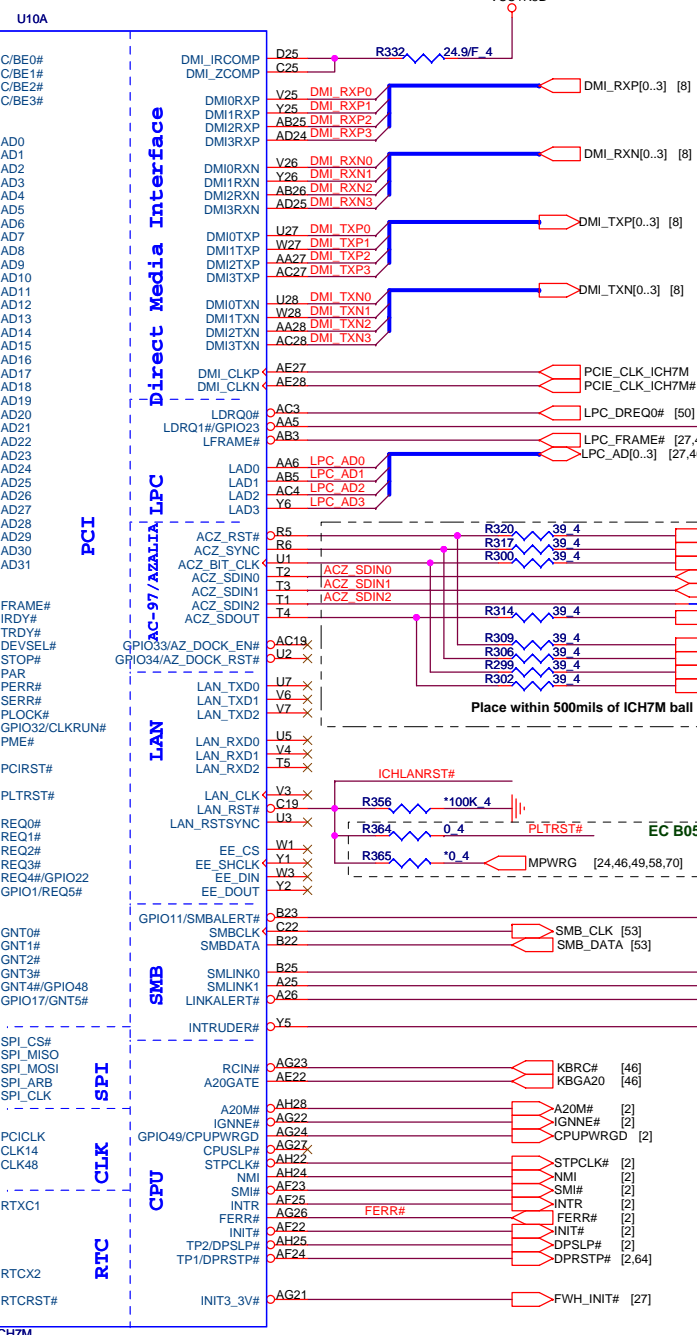
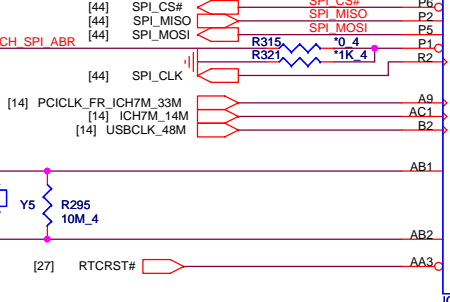
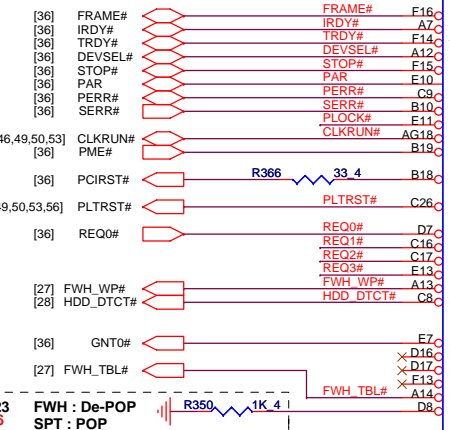
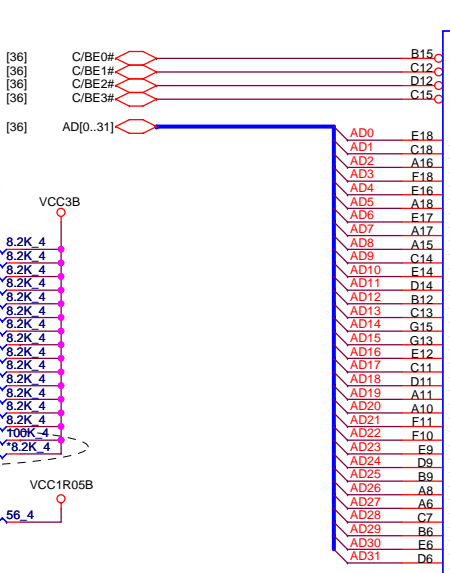
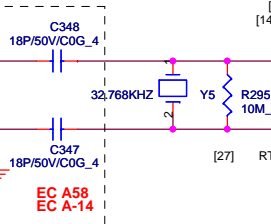
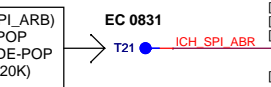
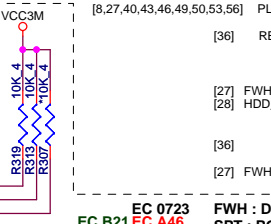
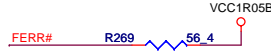
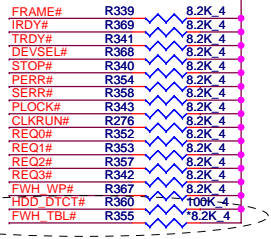
To port - replicator C.R.T

Zo(Trace impedance) of PR_RED#/PR_GRN#/PR_BLU# must meet Intel CRT DAC routing topology of design guide.

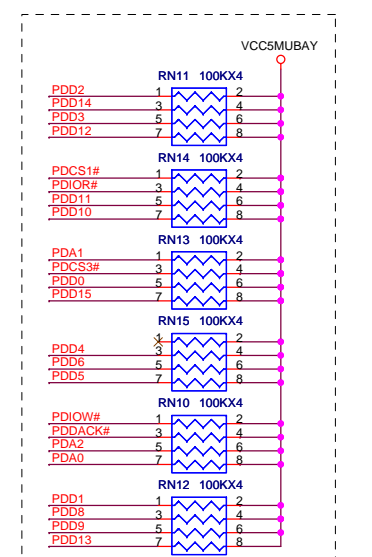
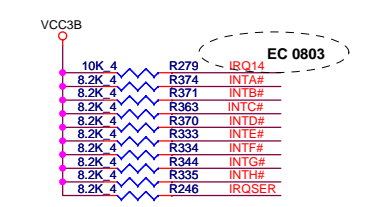
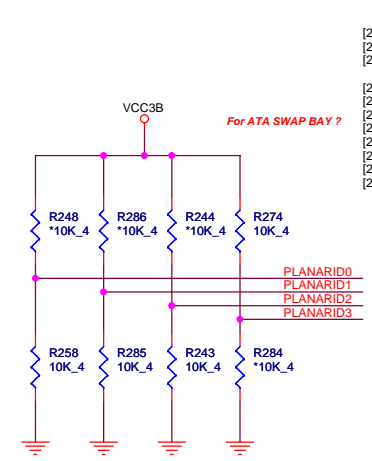
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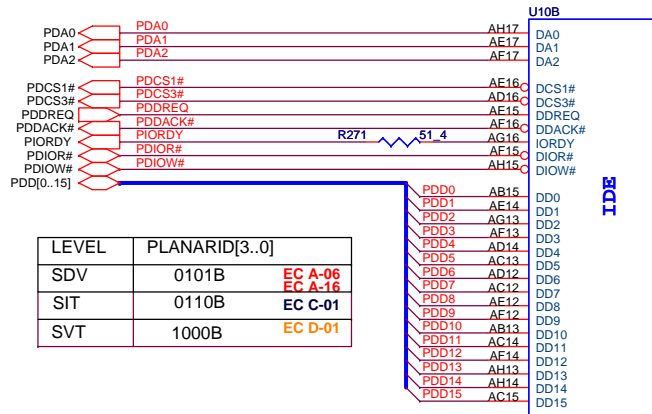
PCI Pullups



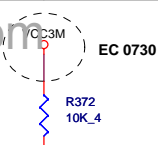
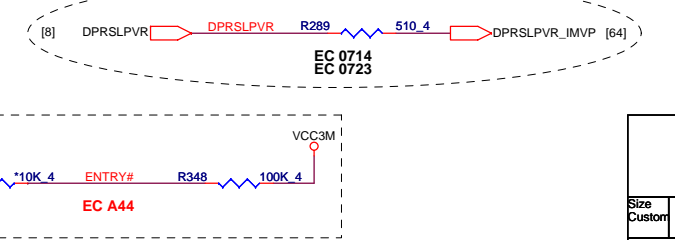
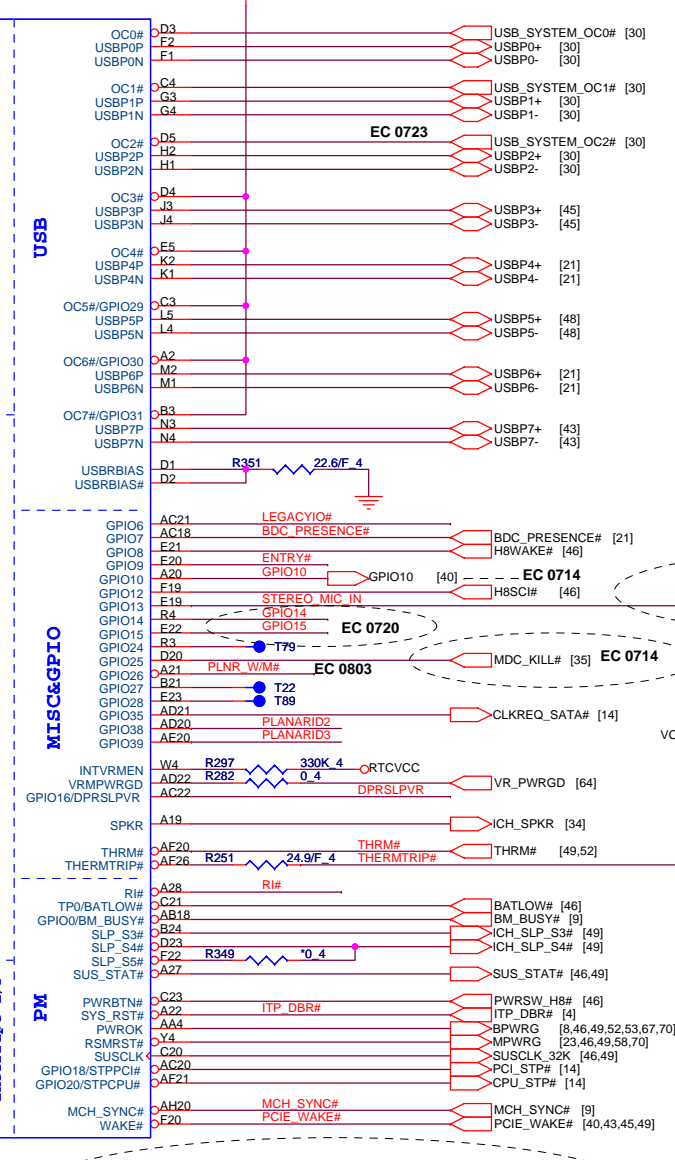
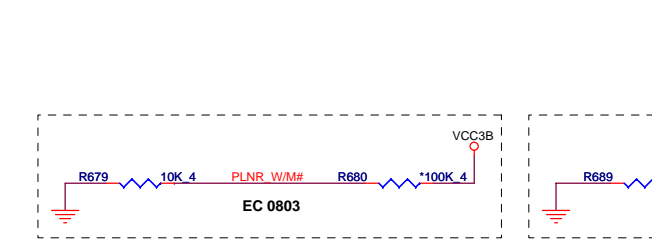
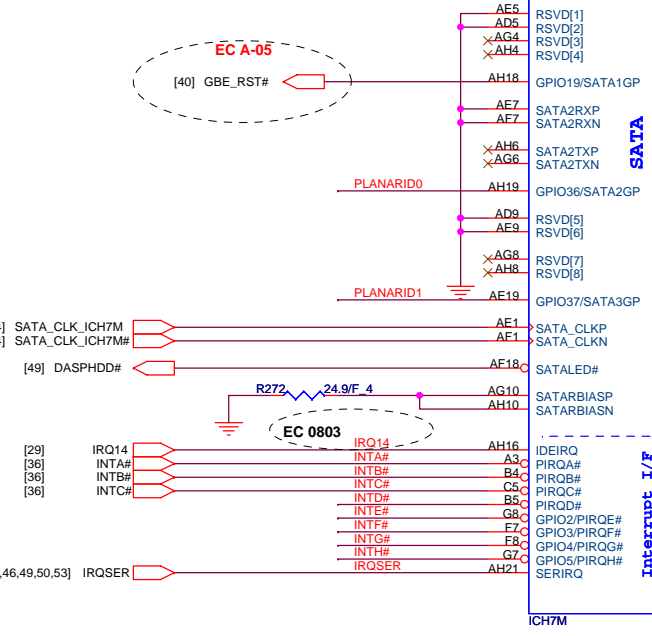
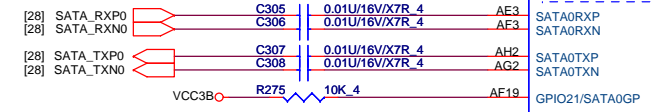
FOR THE STUFFING OPTION(ICH_SPL_ARB)
 AMT ENABLE : 0 OHM SHOULD BE POP
 AMT DISABLE : 0 OHM SHOULD BE DE-POP
 (ICH7M has internal pull down resistor 20K)



EC 0707 DEL PDD SIGNAL PULL UP
EC 0803 Add pull up for data
EC 0809 No stuff
EC A41 Stuff

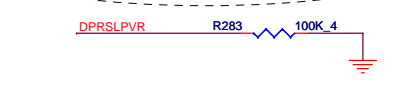
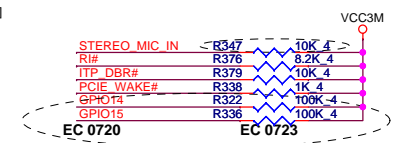
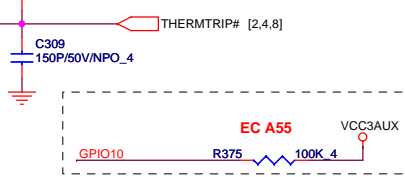
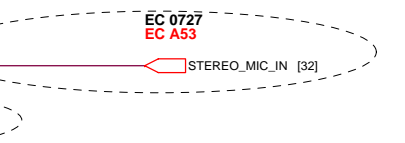
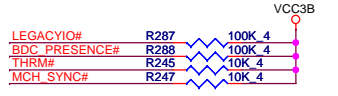


LEVEL	PLANARID[3..0]	
SDV	0101B	EC A-06 EC A-16
SIT	0110B	EC C-01
SVT	1000B	EC D-01



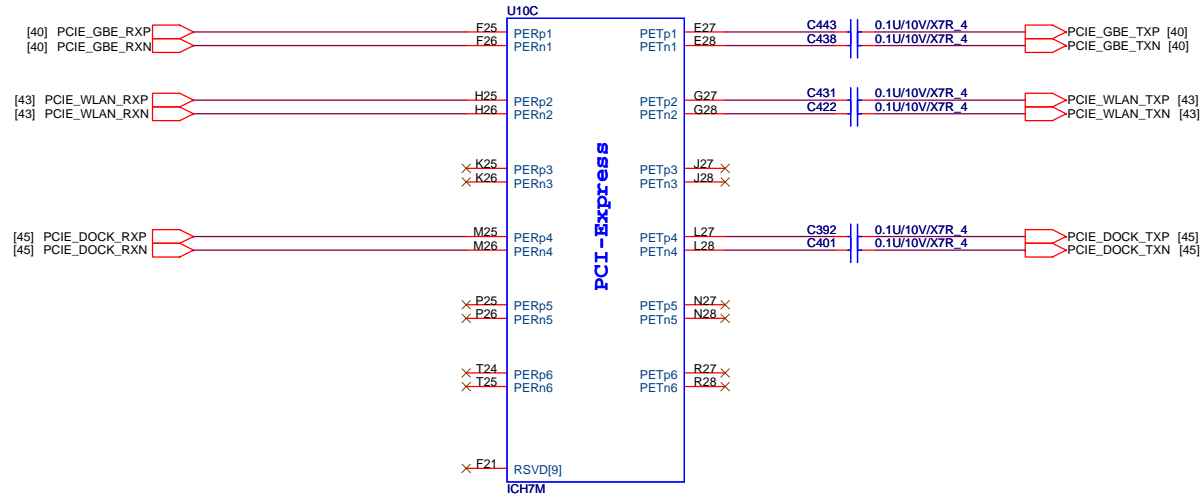
USB distribution

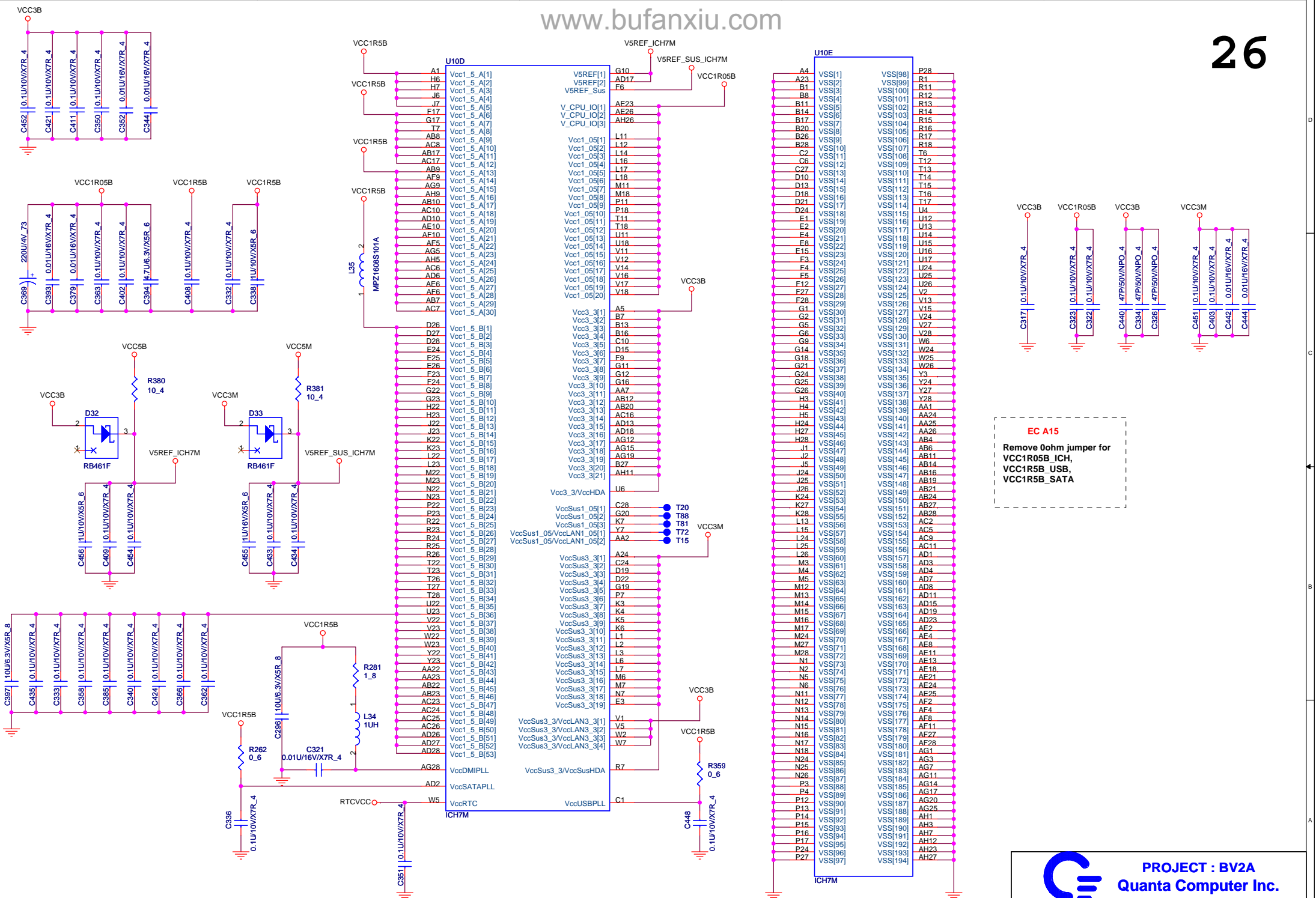
USB0	USB Port 1
USB1	USB Port 2
USB2	USB Port 3
USB3	Docking
USB4	Bluetooth
USB5	Finger print
USB6	Camera
USB7	MINI PCI-E CARD



PCIE distribution

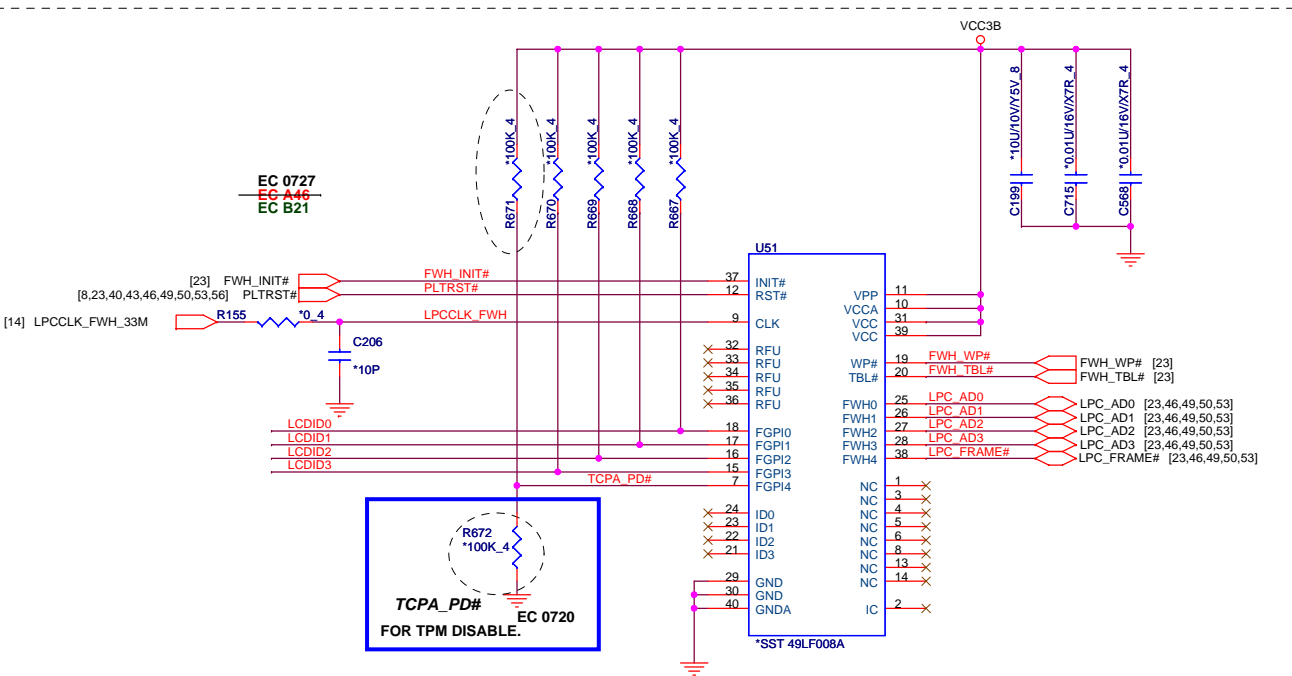
PCIE1	Enthernet Controller
PCIE2	PCIE WLAN
PCIE3	NC
PCIE4	Docking
PCIE5	NC
PCIE6	NC





EC A15

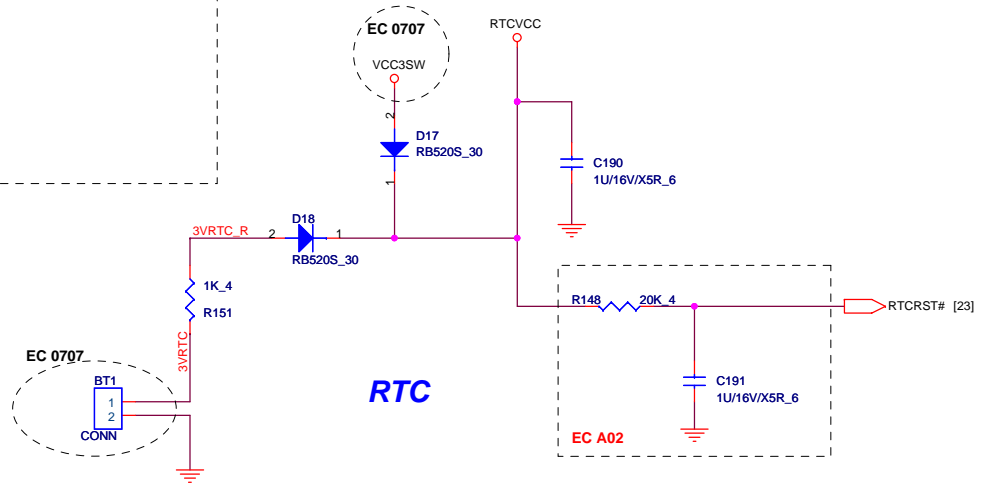
Remove 0ohm jumper for
VCC1R05B_ICH,
VCC1R5B_USB,
VCC1R5B_SATA



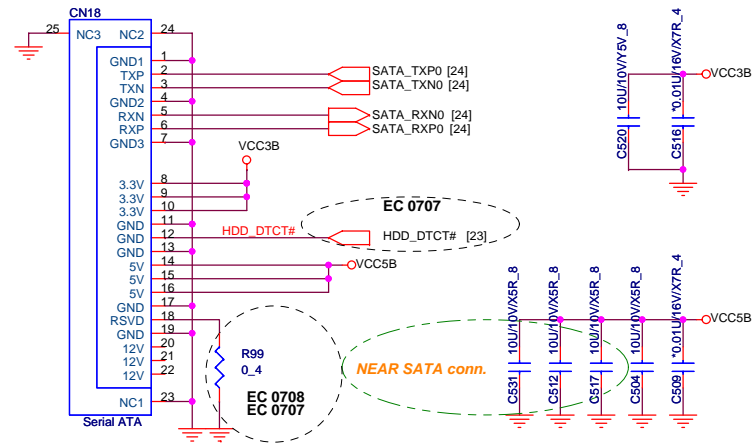
FWH change to co-layout TSSOP40 & PLCC32 type

EC 0720 JUST FOR DEBUG AND SMT 5PCS.
EC A43 Delete PLCC socket

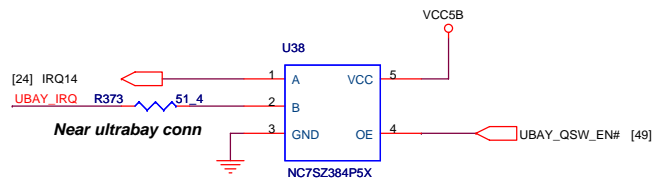
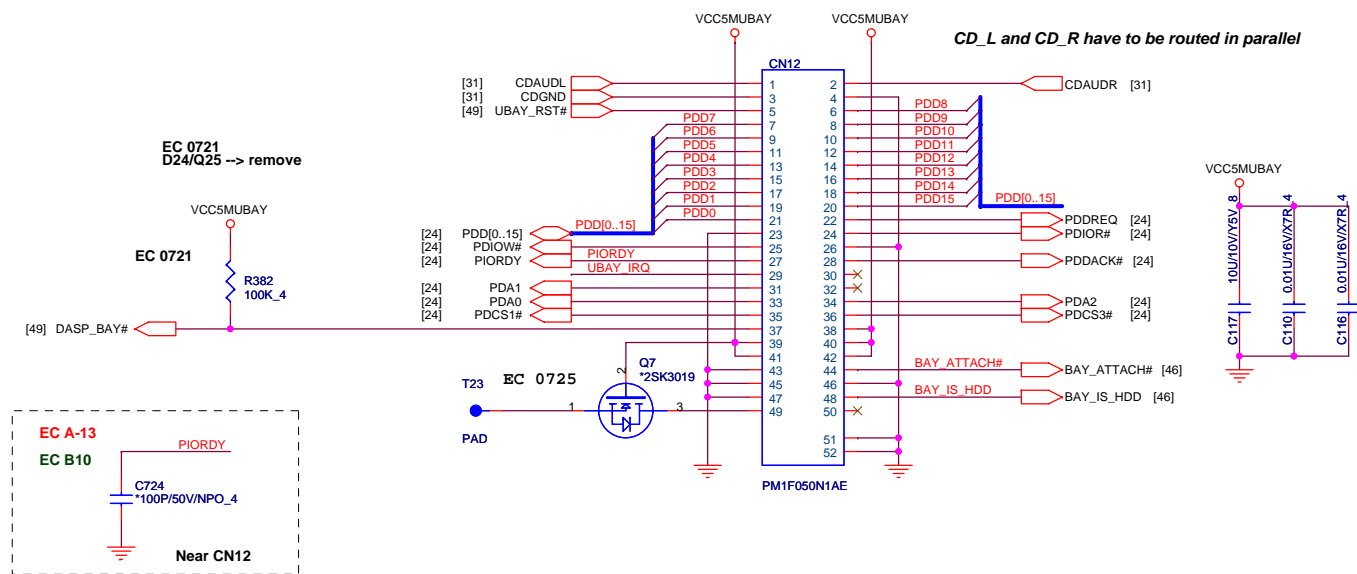
TCPA_PD#
EC 0720
FOR TPM DISABLE.



EC 0714 NO TEST PAD FOR SATA SIGNAL.



ODD CONNECTOR



	BAY_ATTACH#	BAY_IS_HDD
NO_DEVICE	H	Don't care
OPTICAL	L	L
HDD	L	H

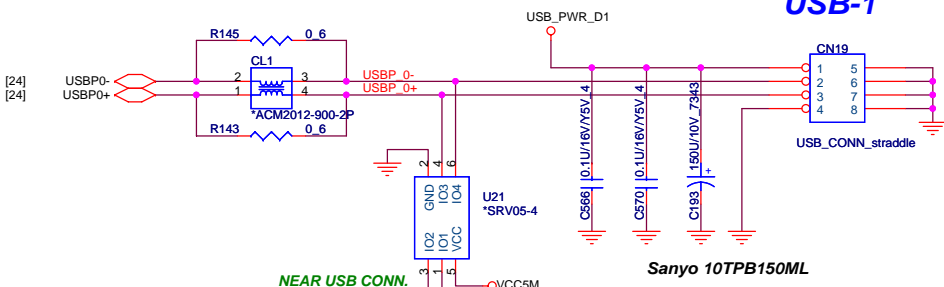
USB port(straddle type) *2

1. Common mode choke coil : TDK ACM2012-900 (reserved)

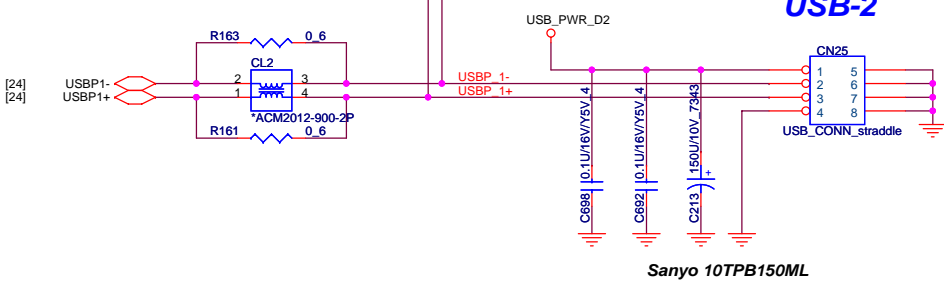
Place these resistors as the choke coil are also placed on the same pads of these two 0ohm resistors (0603size)

2. PGB0010603 ESD diode and 150U cap should close to USB conn

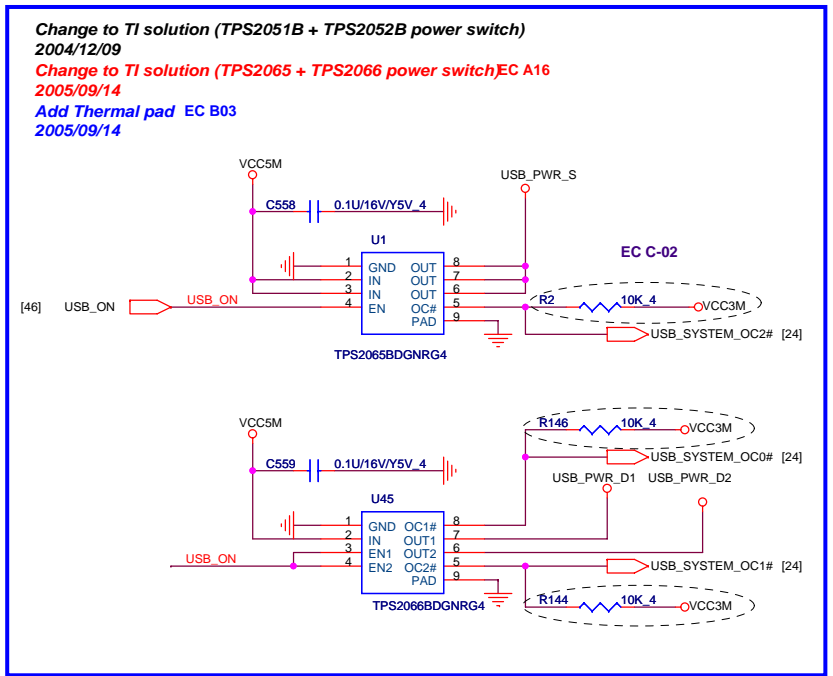
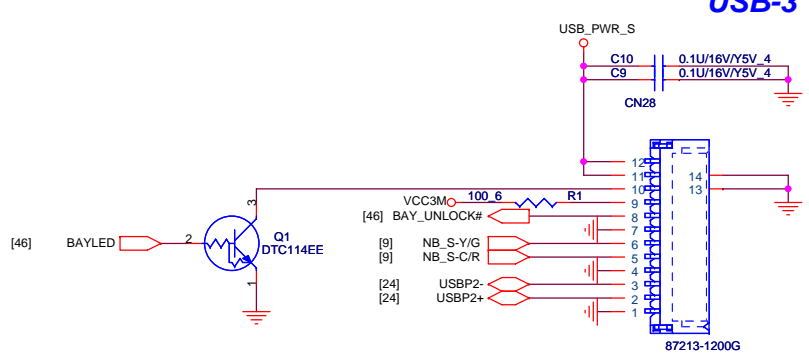
USB-1



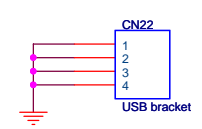
USB-2

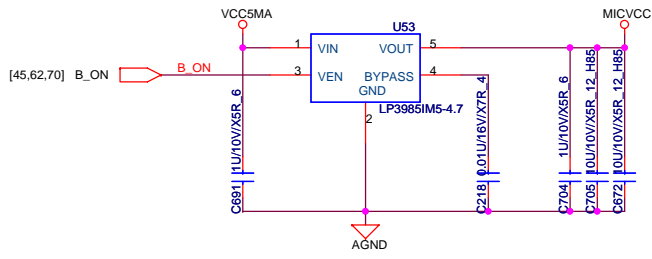


USB-3

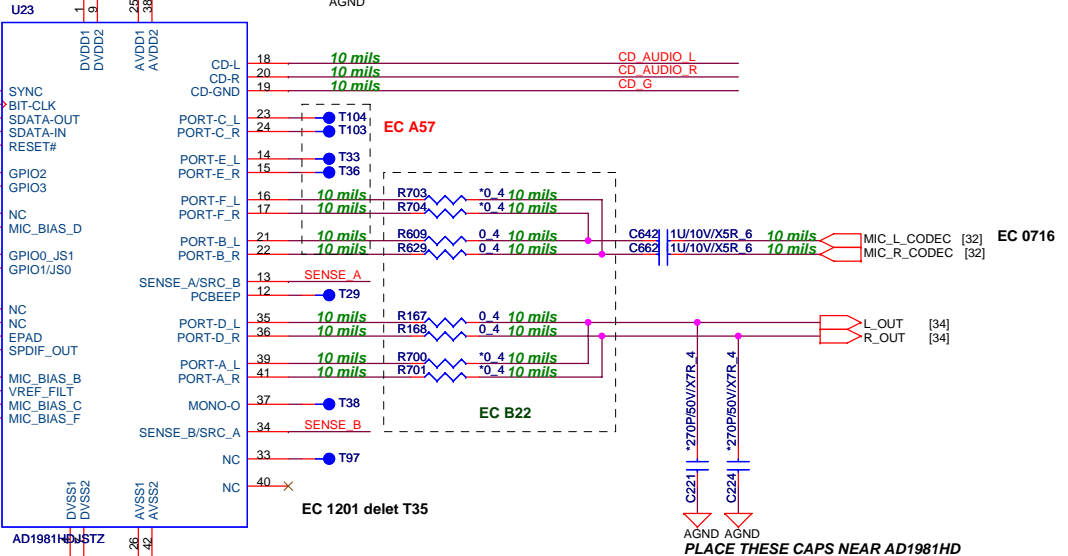
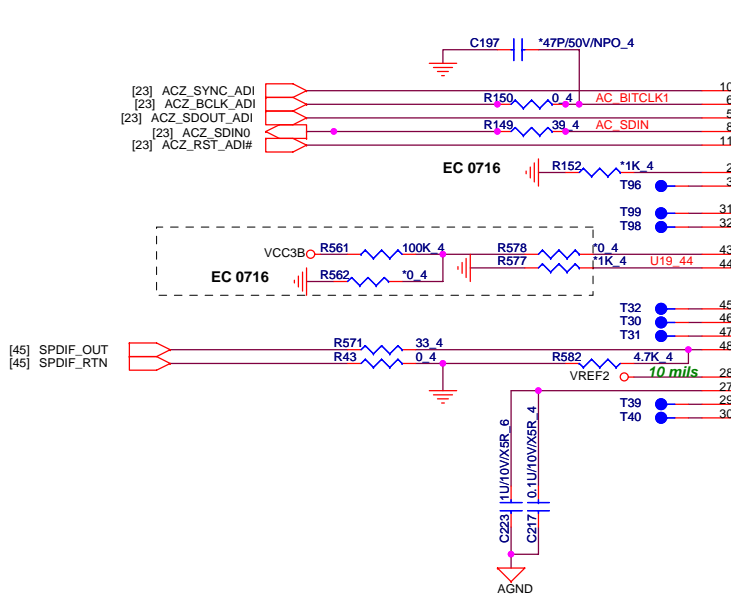
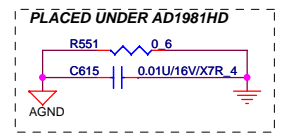
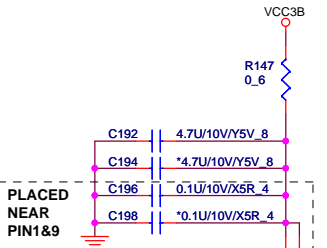
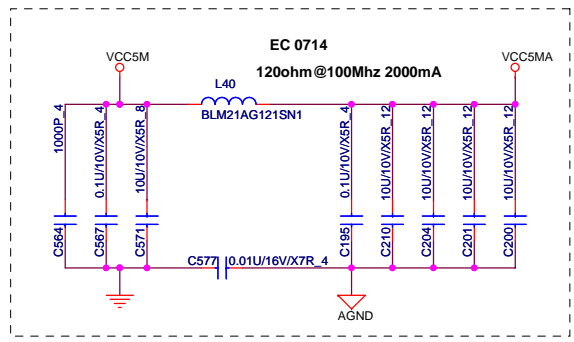
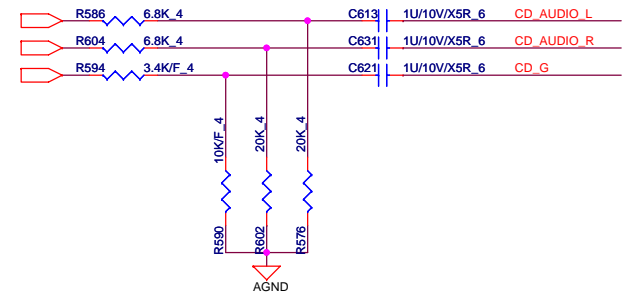


USB Bracket



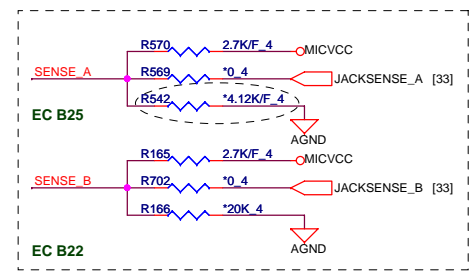


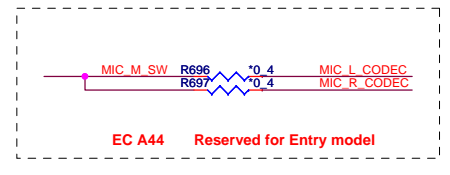
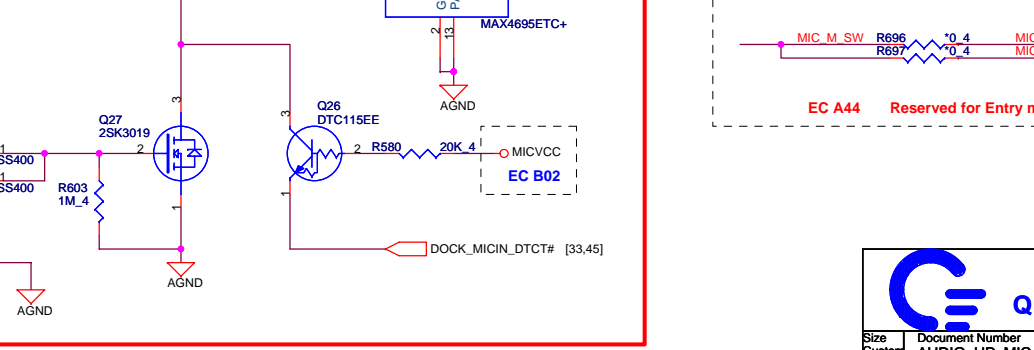
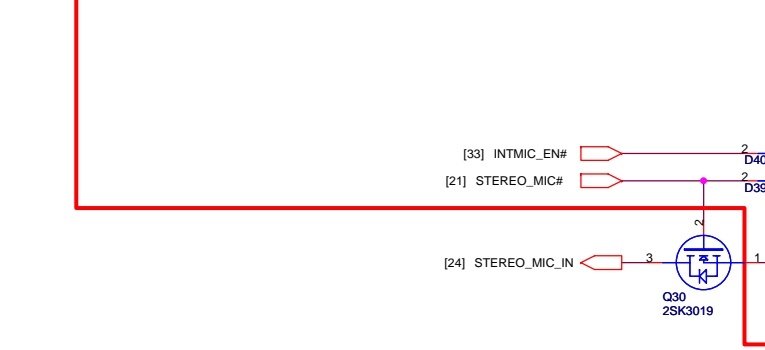
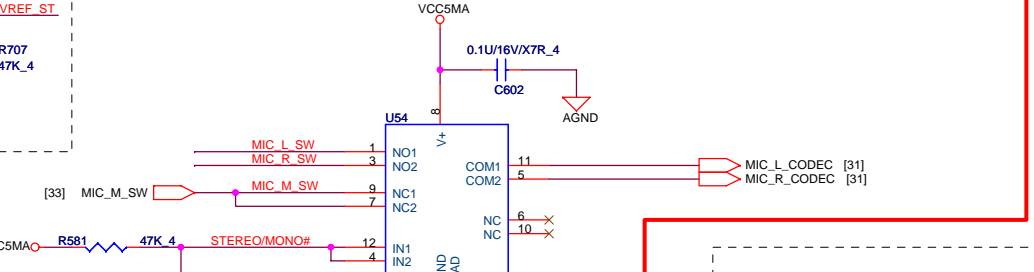
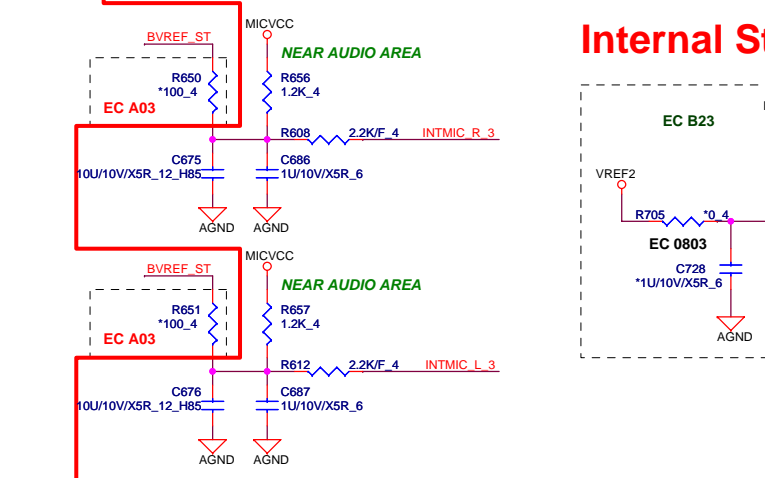
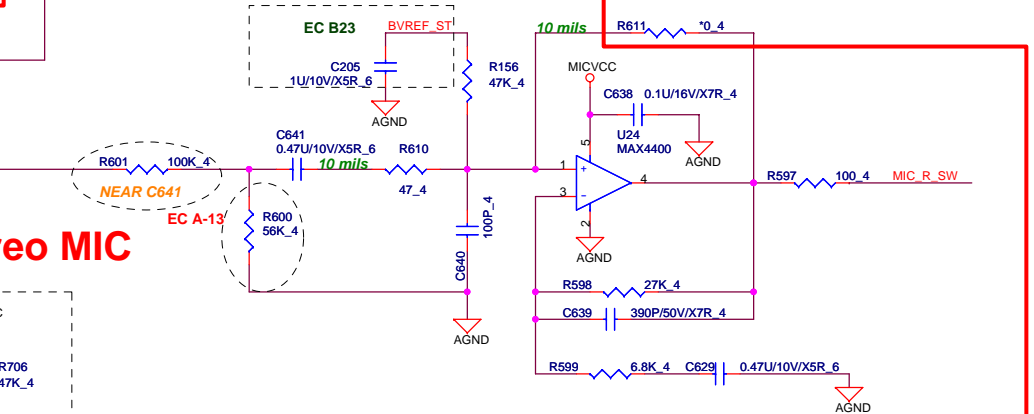
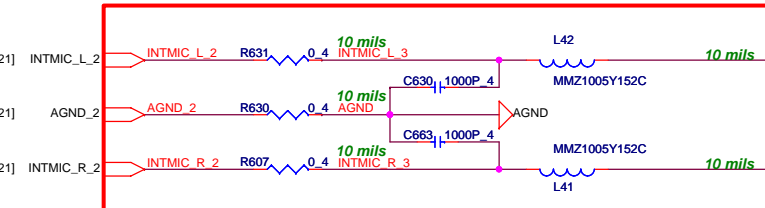
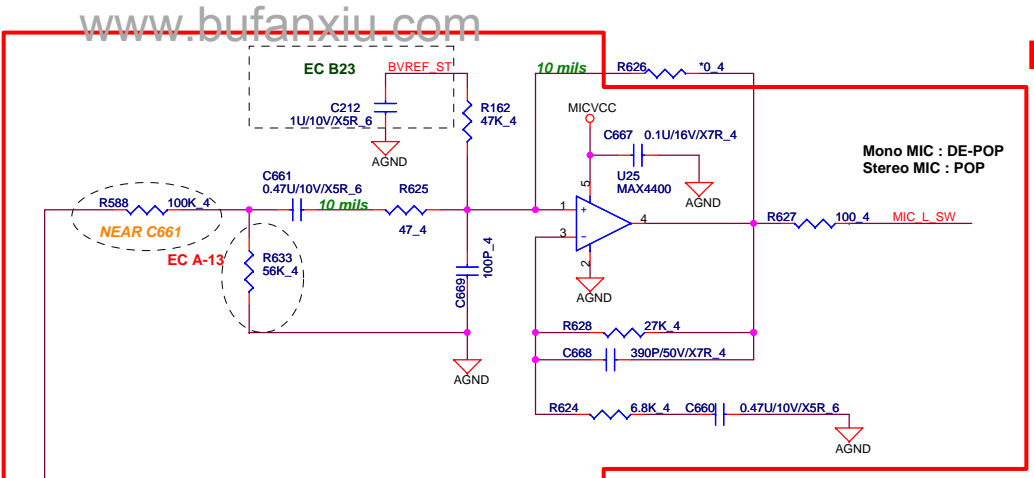
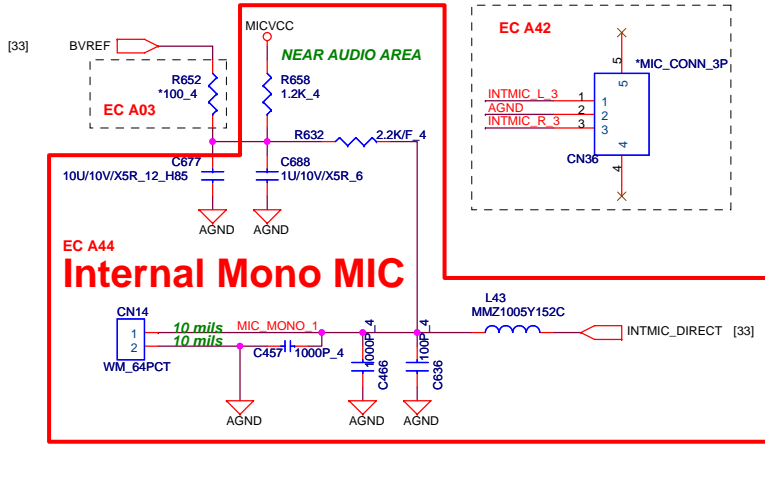
- [29] CDAUDL
- [29] CDAUDR
- [29] CDGND

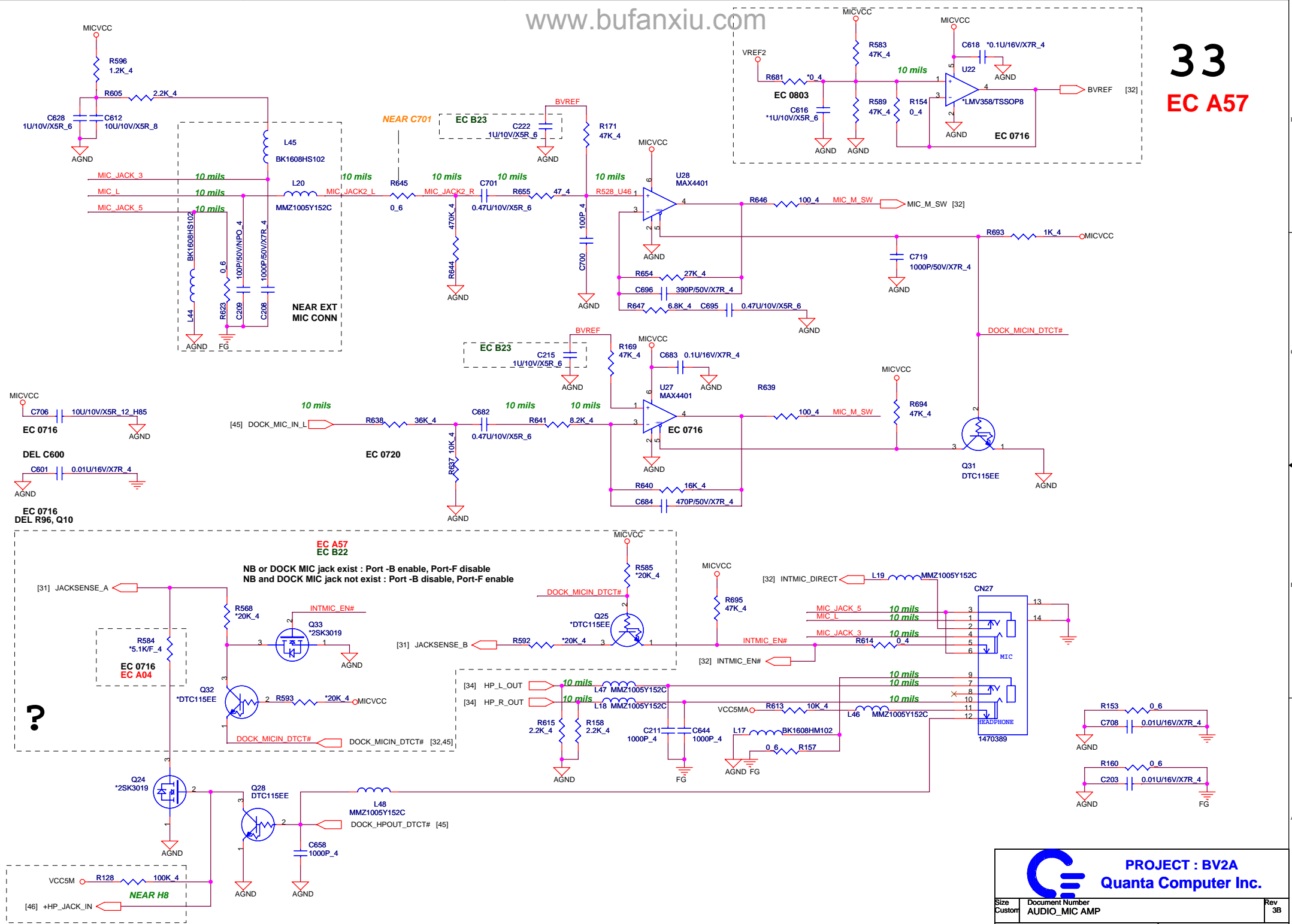


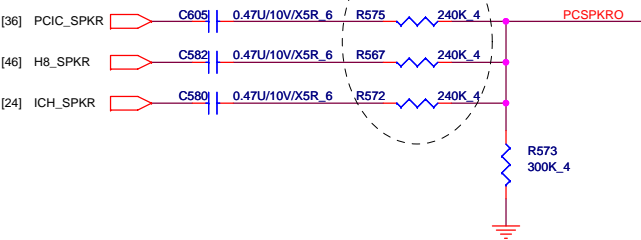
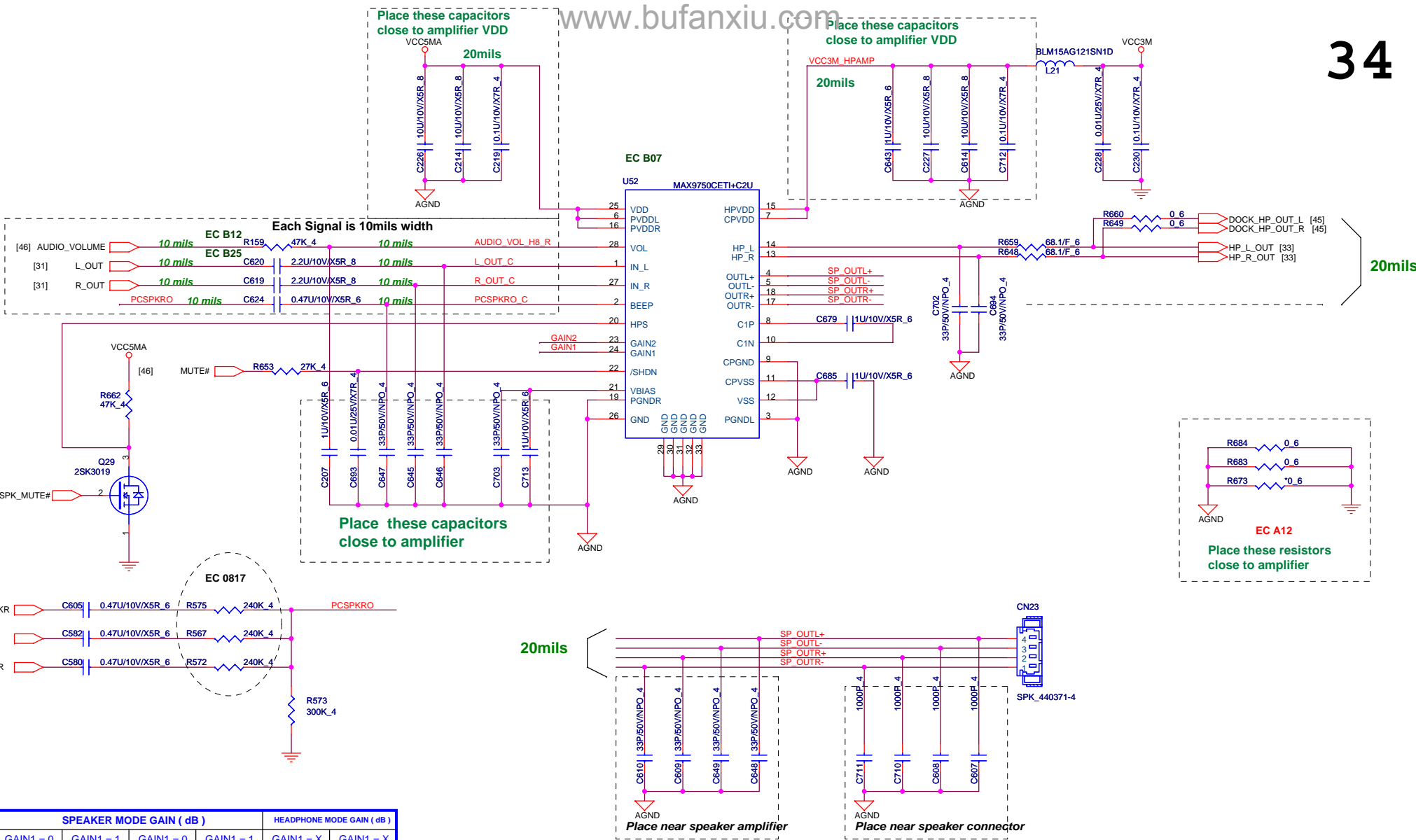
PLACE THESE CAPS NEAR AD1981HD

Resistor (1% tolerance)	SENSE_A		SENSE_B	
	Function	Port	Function	Port
R584	5.1K	Line out	D	N/A
	10.0K	Line in	C	N/A
R568	20.0K	Front MIC	B	Rear MIC
	39.2K	Headphone	A	Aux in

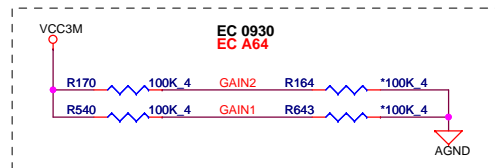


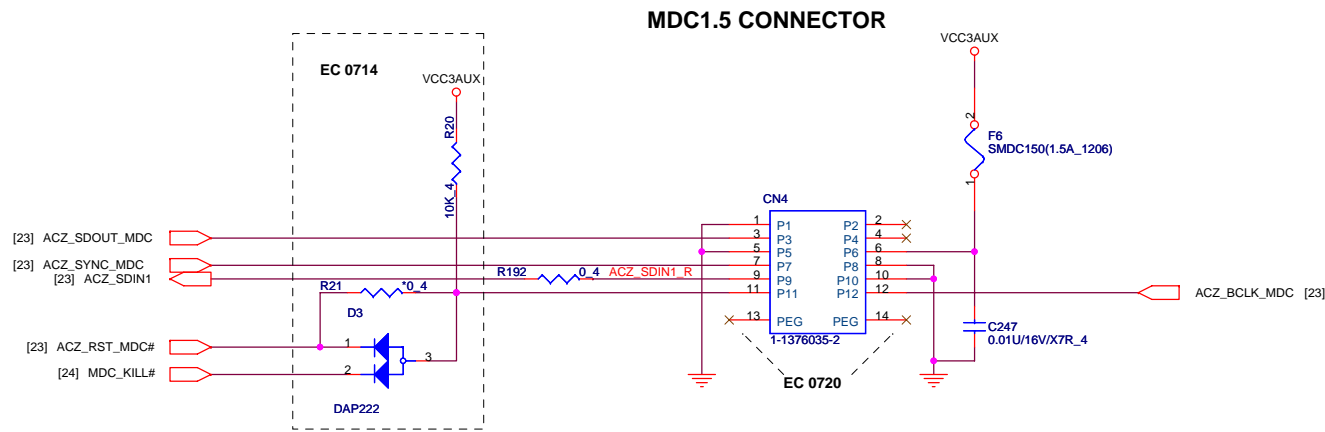


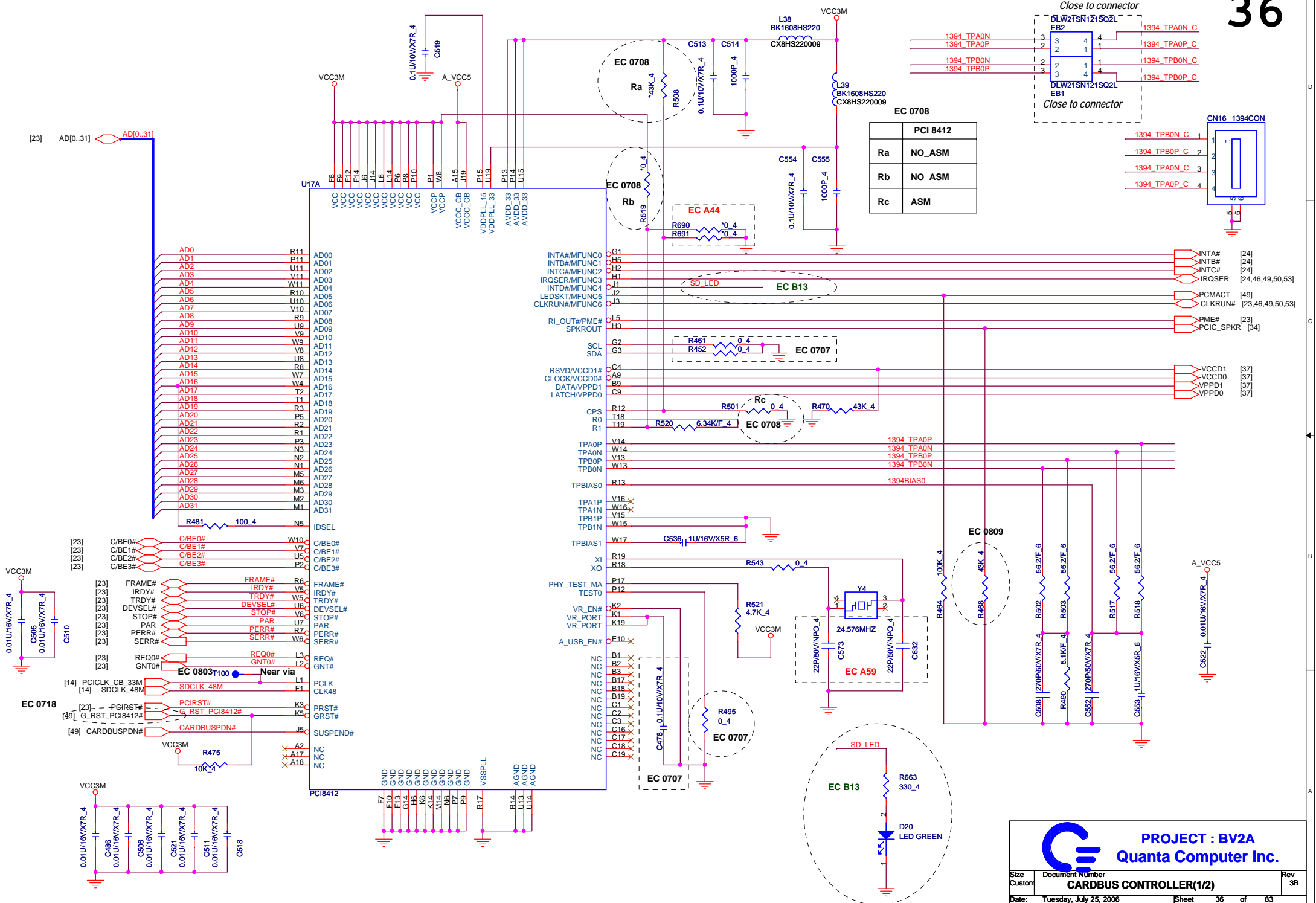




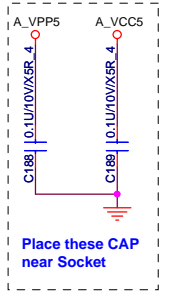
SPEAKER MODE GAIN (dB)				HEADPHONE MODE GAIN (dB)	
GAIN1 = 0	GAIN1 = 1	GAIN1 = 0	GAIN1 = 1	GAIN1 = X	GAIN1 = X
GAIN2 = 0	GAIN2 = 0	GAIN2 = 1	GAIN2 = 1	GAIN2 = 0	GAIN2 = 1
6	7.5	9	10.5	0	3
			V		V



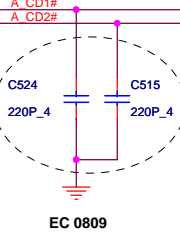
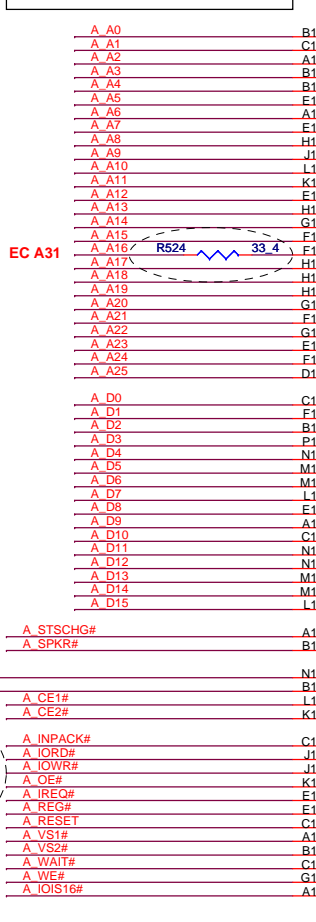




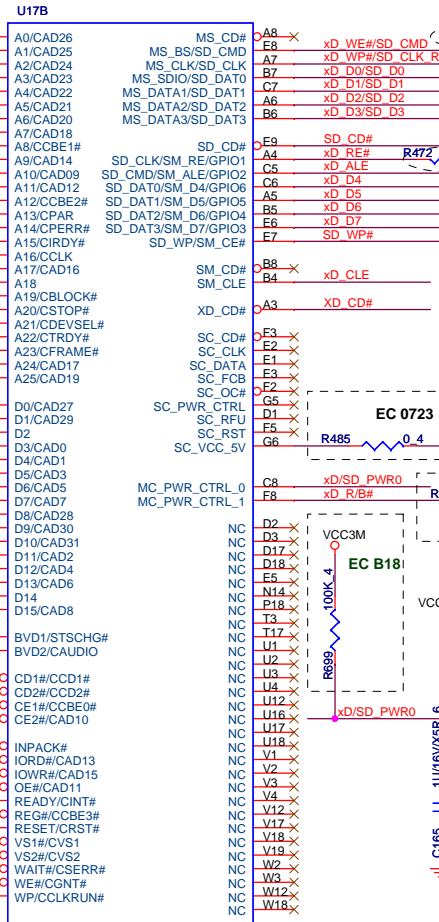
A_A16: CARDBUS CLK 33MHZ
A_IORD#, A_IOWR#: USB2.0



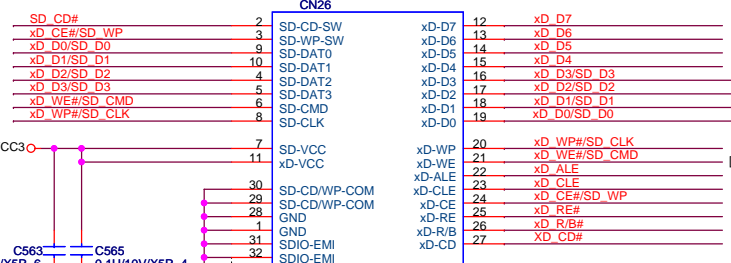
Place these CAP near Socket



EC 0809



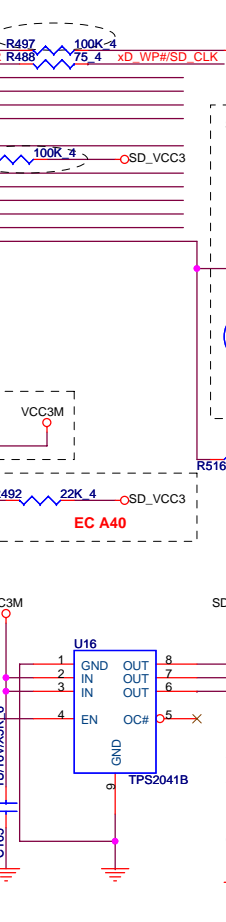
SD/xD SLOT



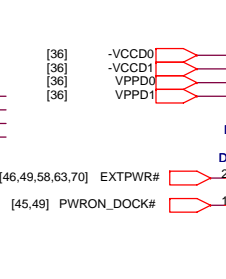
QEC 0809

CARDREADER
2IN1-R013-D10-NR-32P-V-BV2

DFHS32FR042

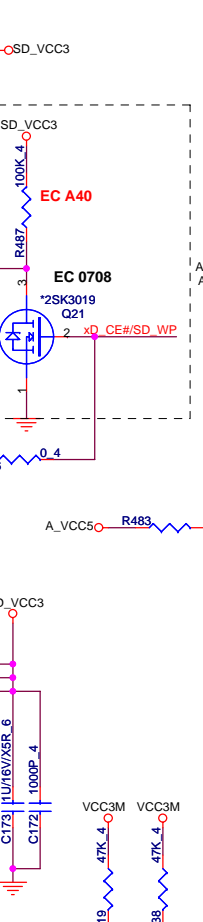


PCI8412

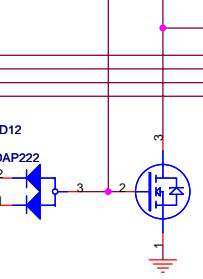


U16

TPS2041B

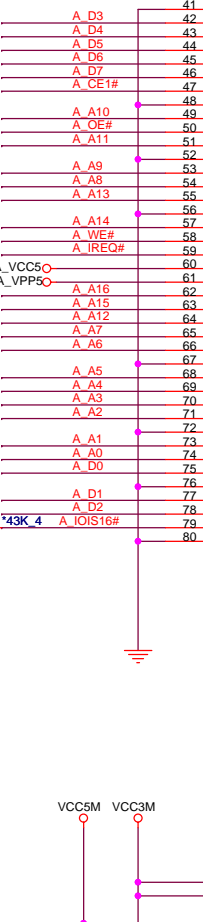


SD/xD SLOT

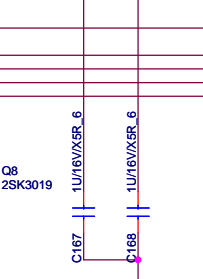


D12

DAP222

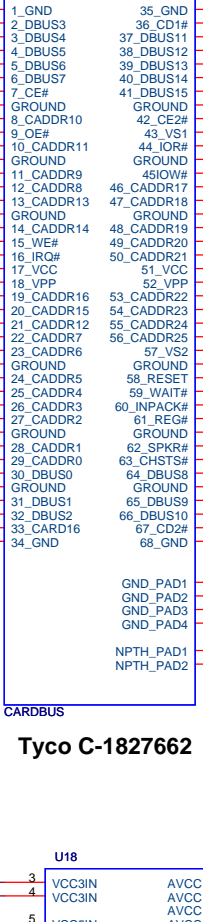


SD/xD SLOT

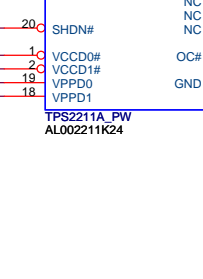


Q8

2SK3019

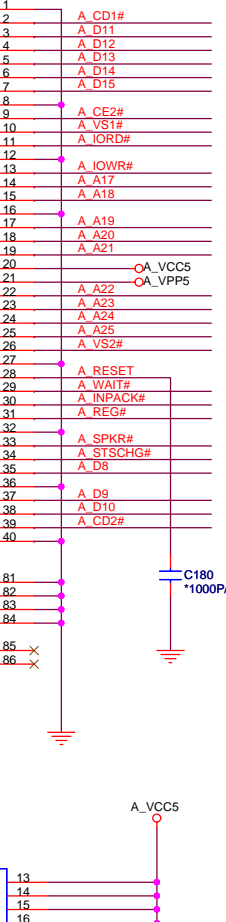


SD/xD SLOT

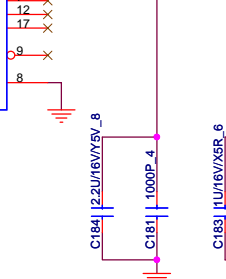


U18

TPS2211A_PW
AL002211K24



CARDBUS




C180

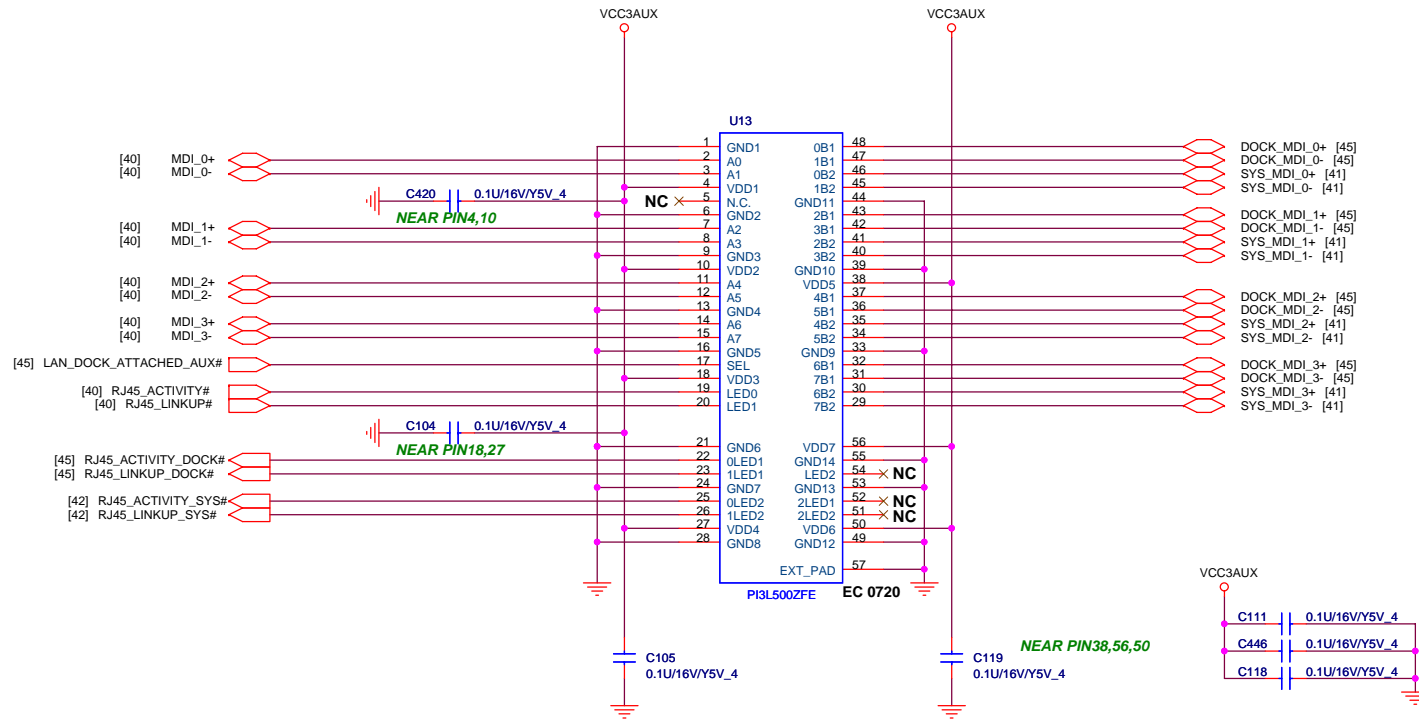
*1000P/50V/X7R_4

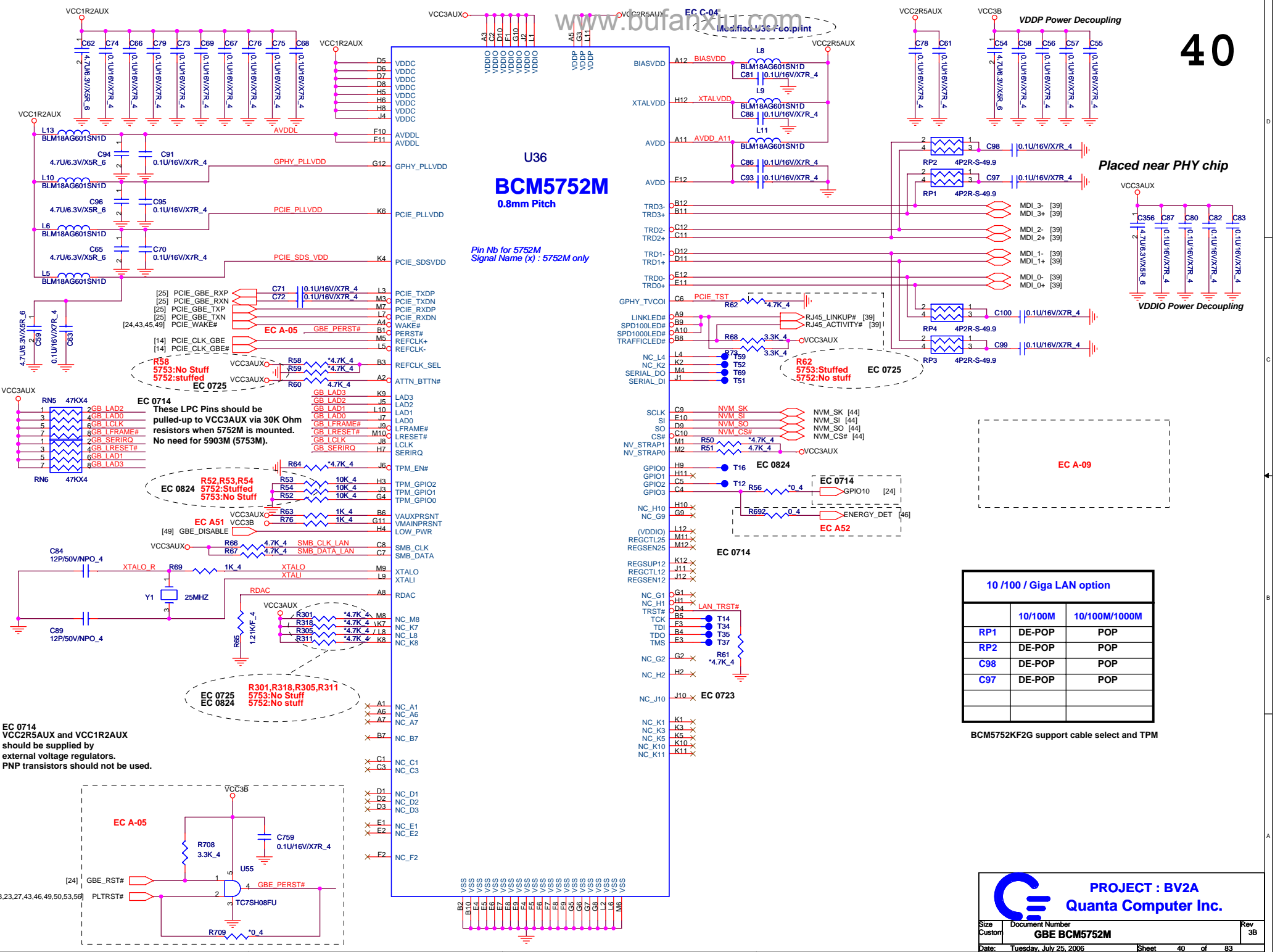
Tyco C-1827662

PROJECT : BV2A
Quanta Computer Inc.
Size Custom Document Number CARDBUS CONTROLLER(2/2) Rev 3B
Date: Tuesday, July 25, 2006 Sheet 37 of 83

BLANK PAGE

		PROJECT : BV2A	
		Quanta Computer Inc.	
Size Custom	Document Number BLANK	Rev 3B	
Date: Tuesday, July 25, 2006		Sheet	38 of 83





U36
BCM5752M
0.8mm Pitch

Pin Nb for 5752M
Signal Name (x) : 5752M only

EC 0714
These LPC Pins should be pulled-up to VCC3AUX via 30K Ohm resistors when 5752M is mounted. No need for 5903M (5753M).

EC 0824
R52, R53, R54
5752: Stuffed
5753: No Stuff

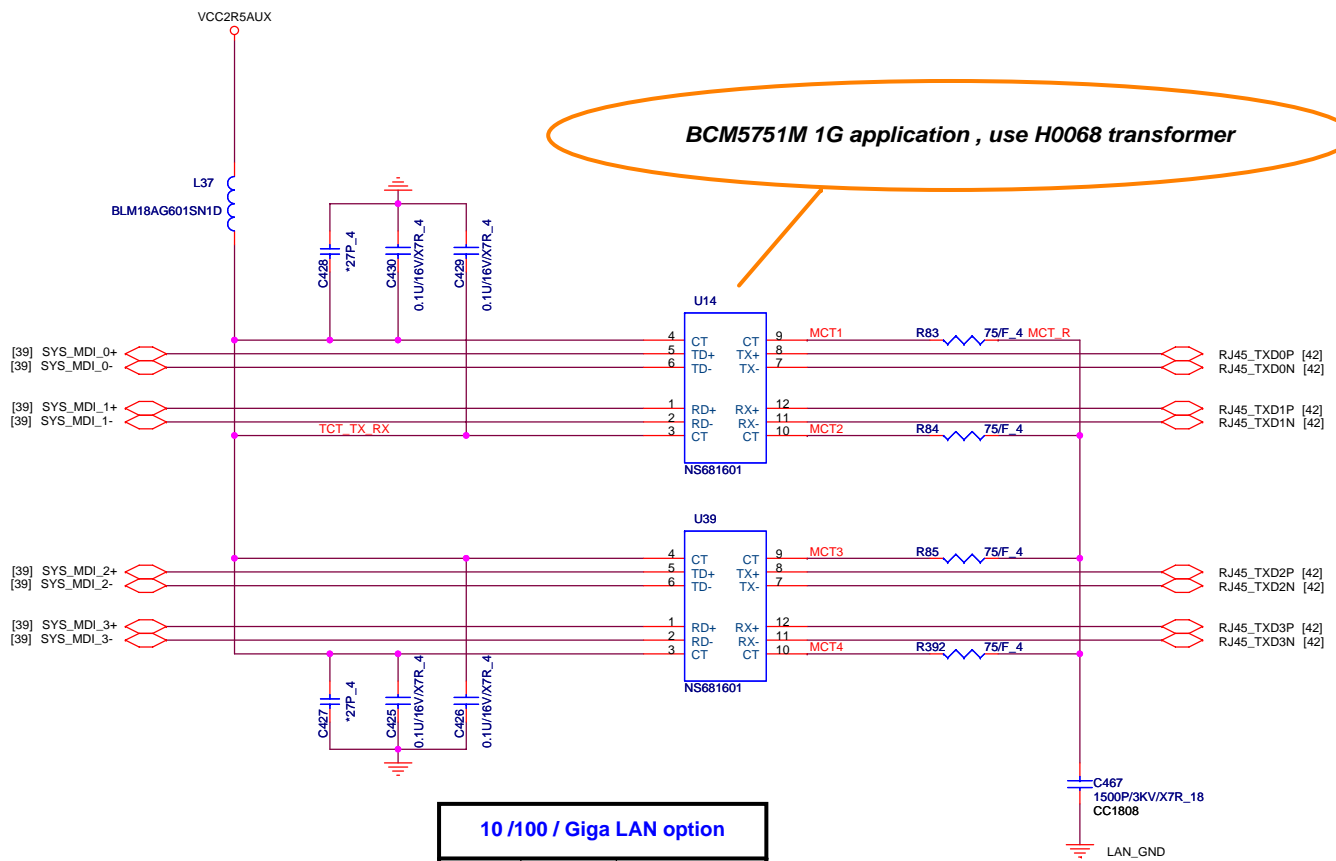
EC 0725
R301, R318, R305, R311
5753: No Stuff
5752: No stuff

EC 0725
R62
5753: Stuffed
5752: No stuff

EC 0714

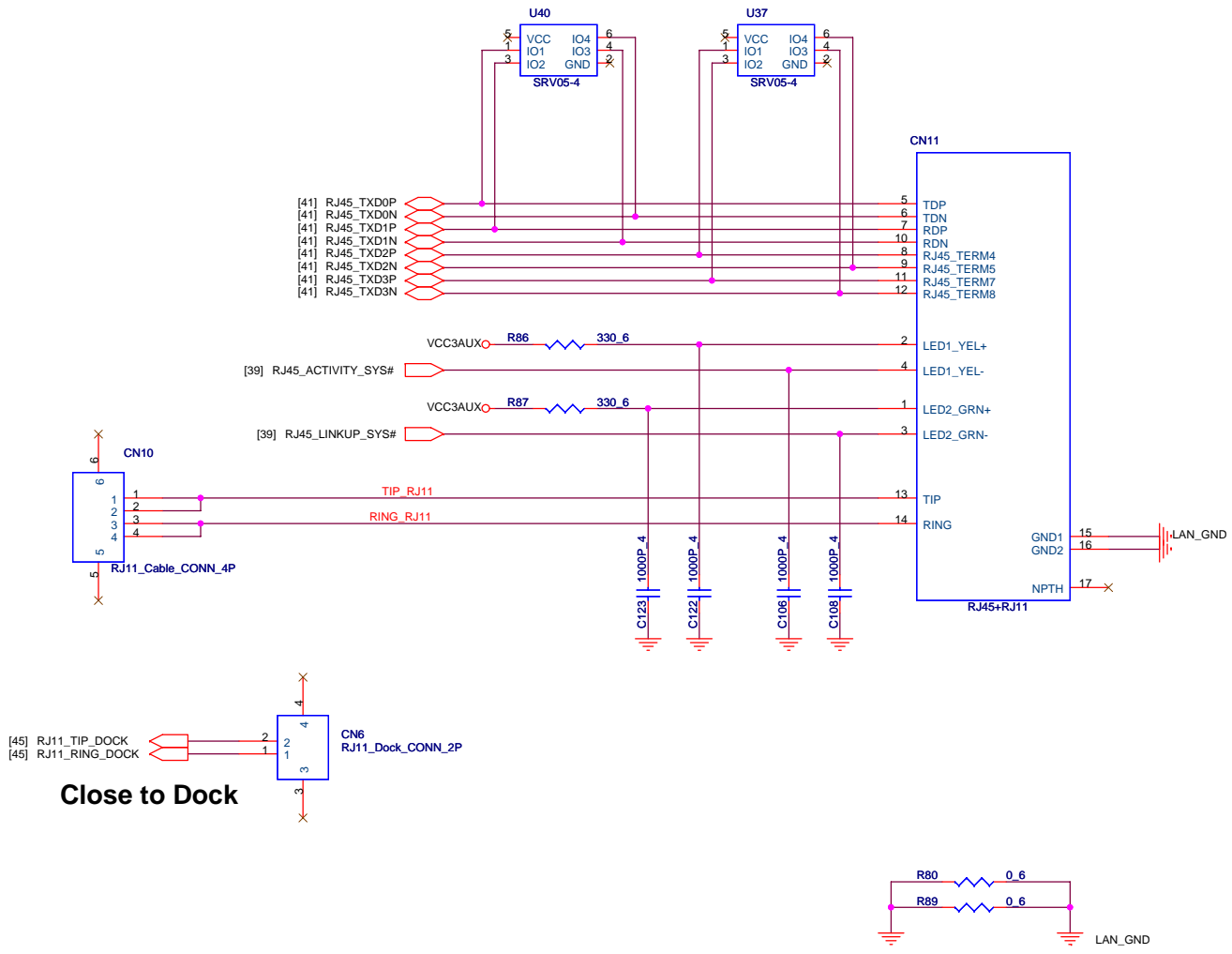
10 / 100 / Giga LAN option		
	10/100M	10/100M/1000M
RP1	DE-POP	POP
RP2	DE-POP	POP
C98	DE-POP	POP
C97	DE-POP	POP

BCM5752KF2G support cable select and TPM

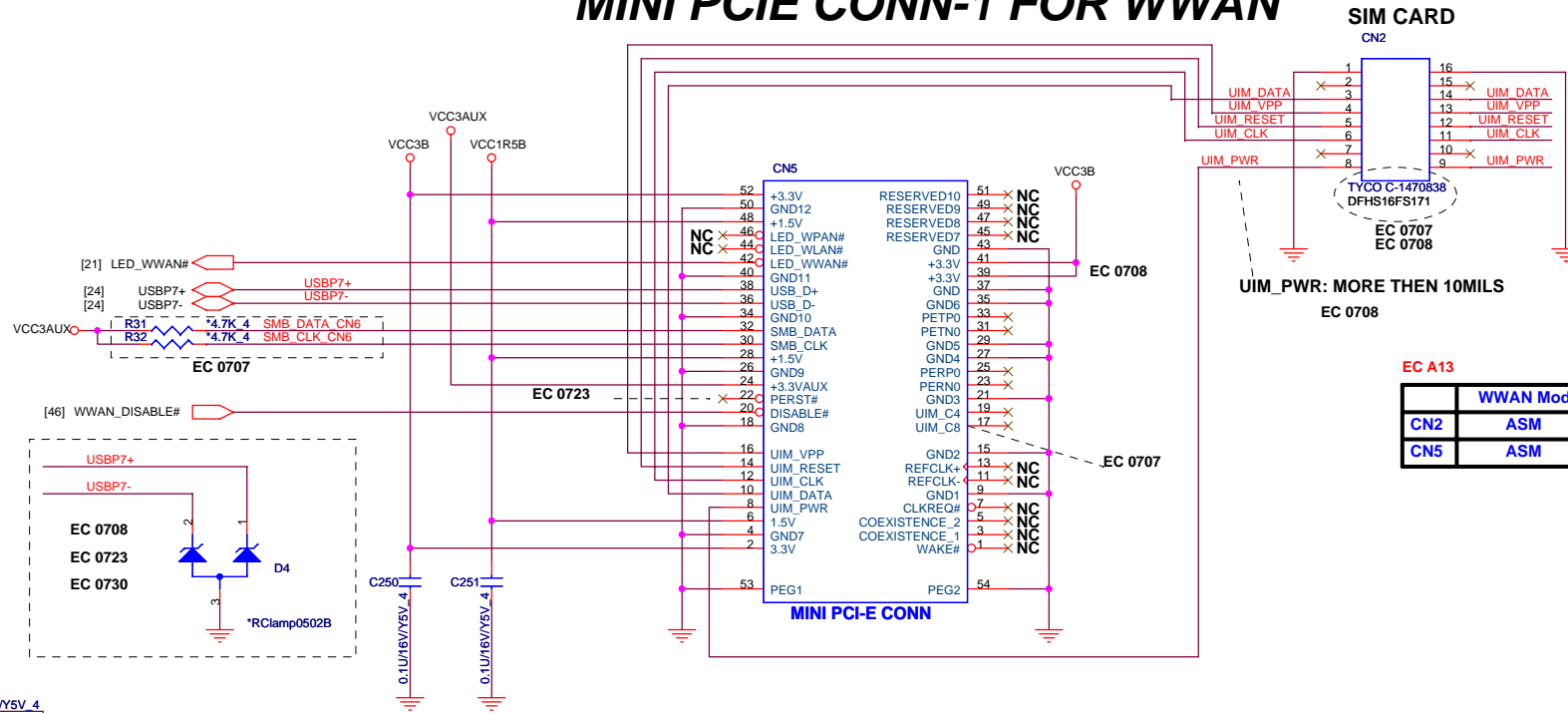


10 /100 / Giga LAN option

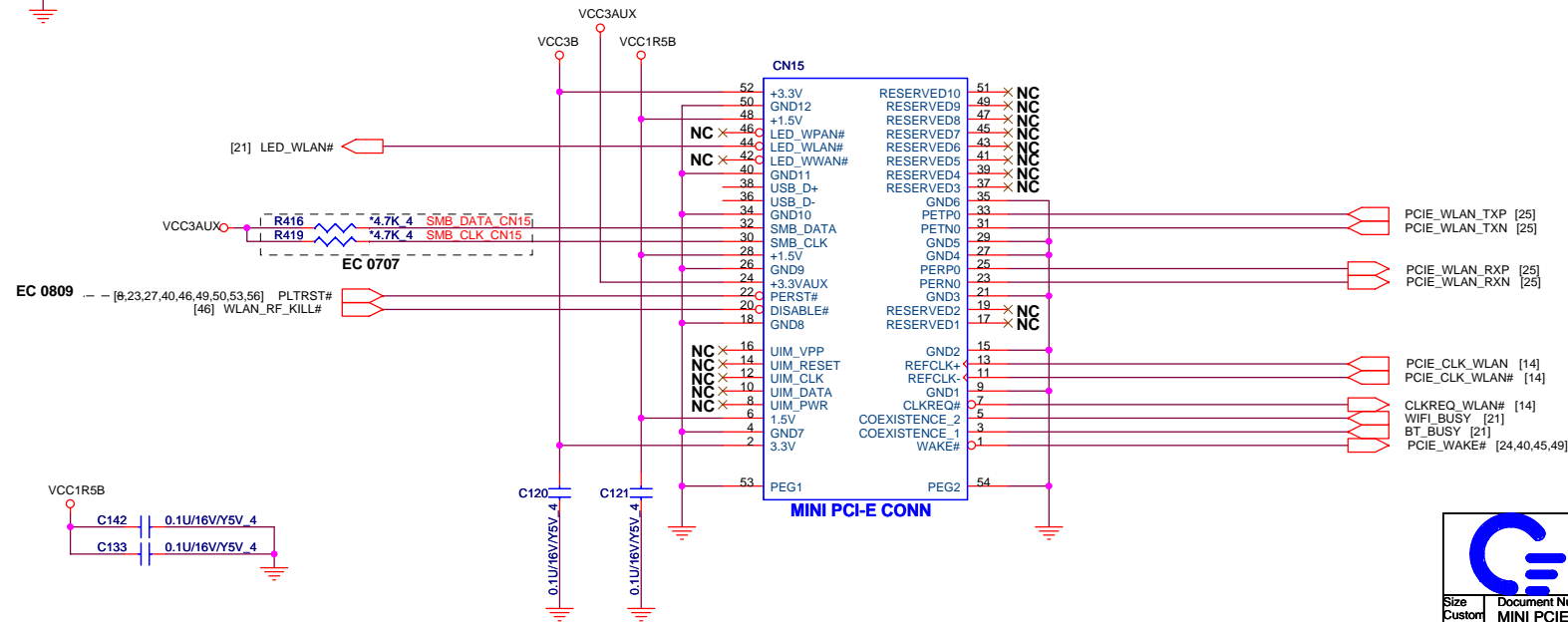
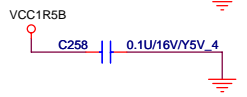
	10/100M	10/100M/1000M
U39	DE-POP	POP
C425	DE-POP	POP
C426	DE-POP	POP
R85	DE-POP	POP
R392	DE-POP	POP



MINI PCIE CONN-1 FOR WWAN

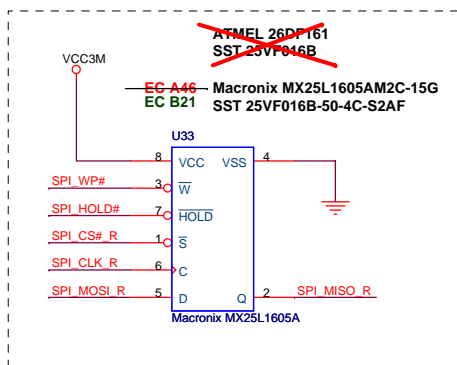


MINI PCIE CONN-2 FOR WLAN

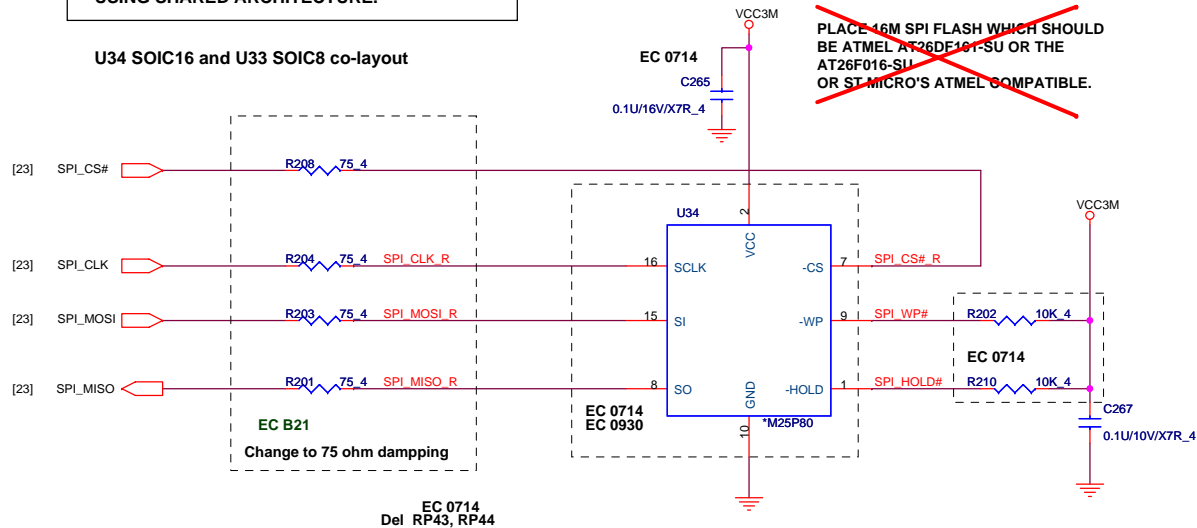


SYSTEM SPI FLASH (ICH7-M)

PLACE LESS THAN 2 INCH FROM THE ICH IF USING SHARED ARCHITECTURE.



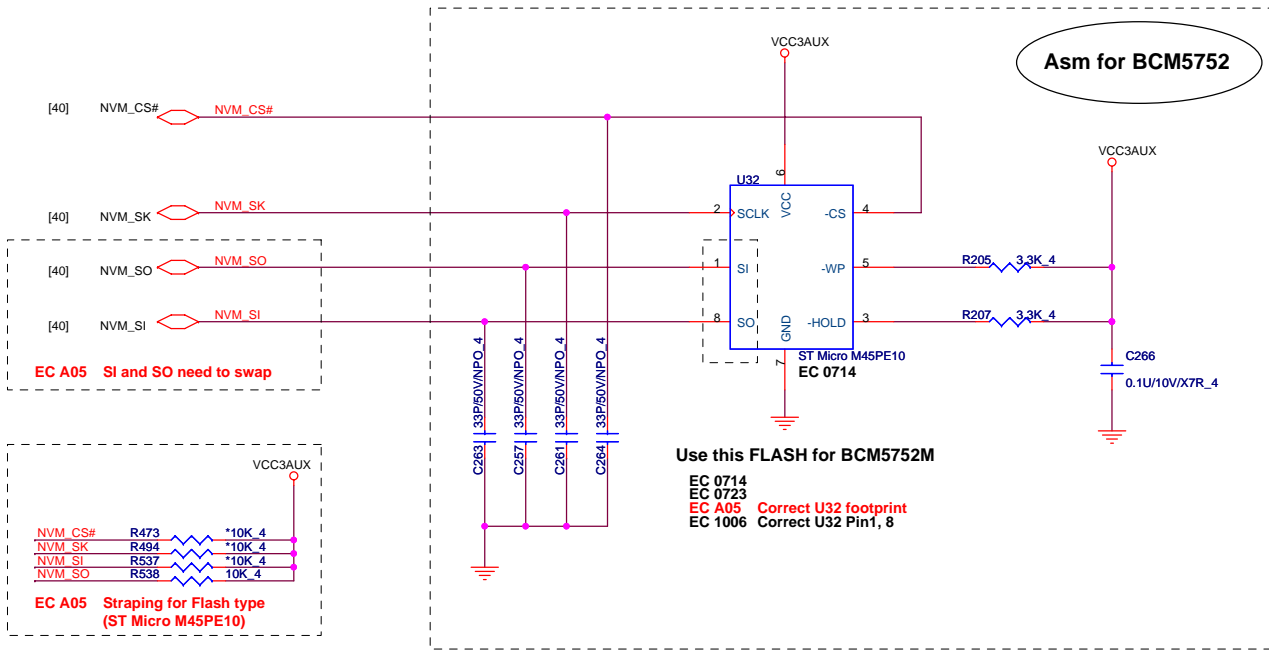
U34 SOIC16 and U33 SOIC8 co-layout

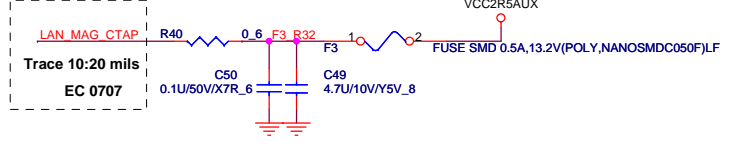
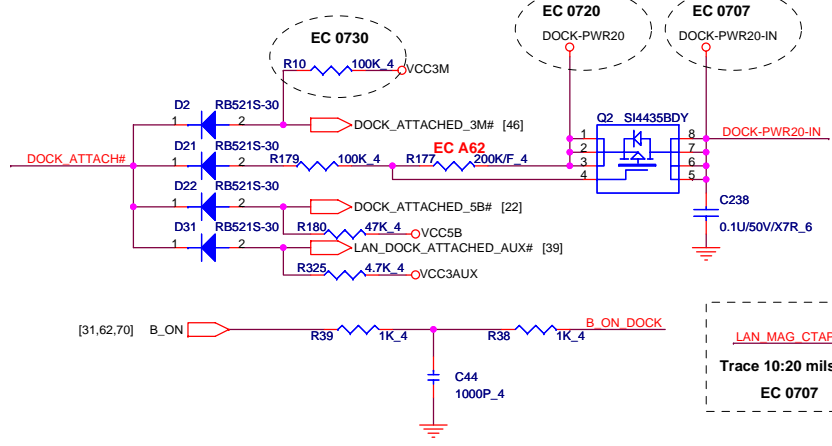
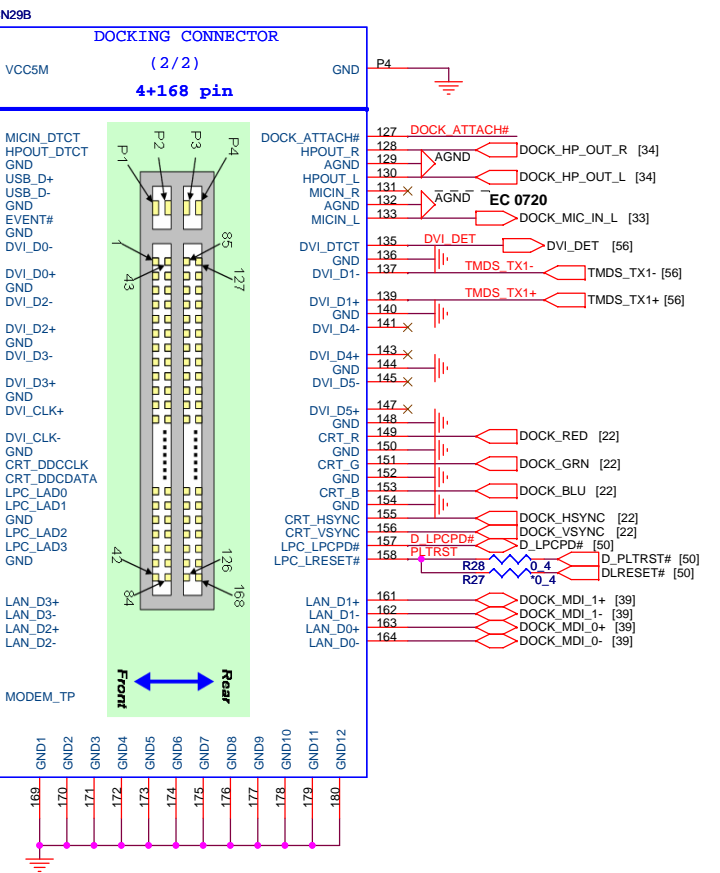
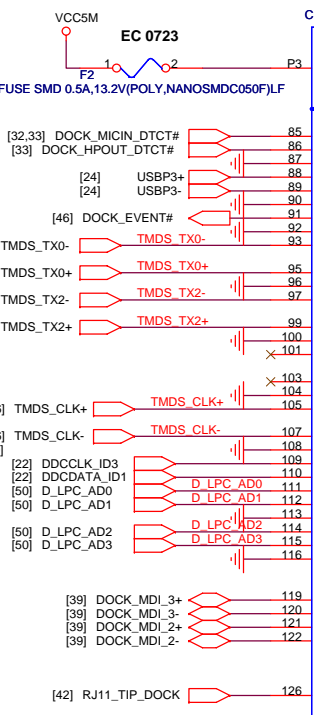
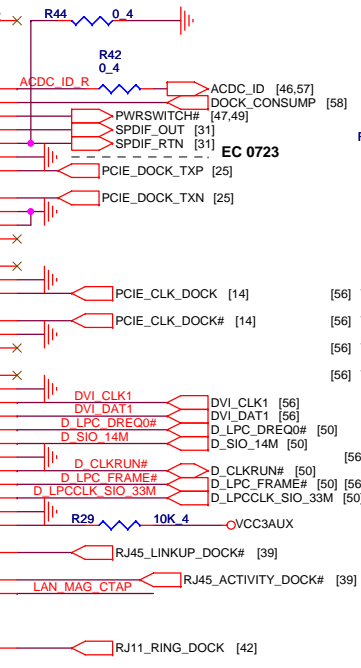
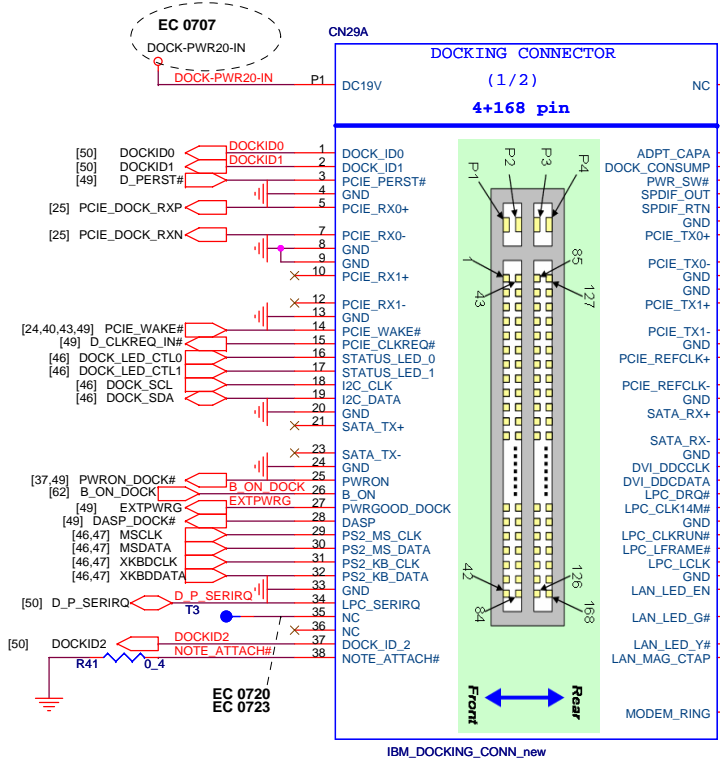
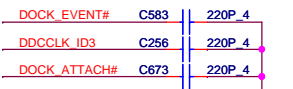
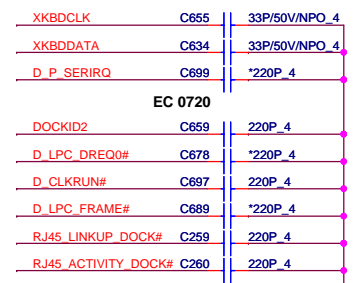
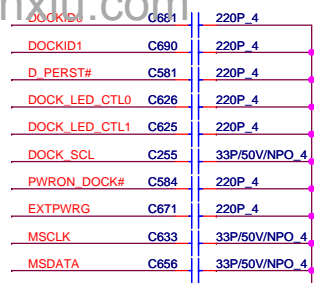
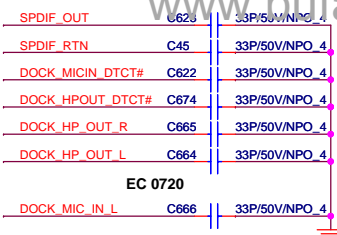
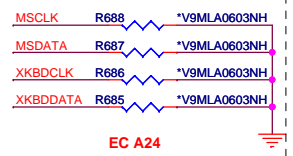


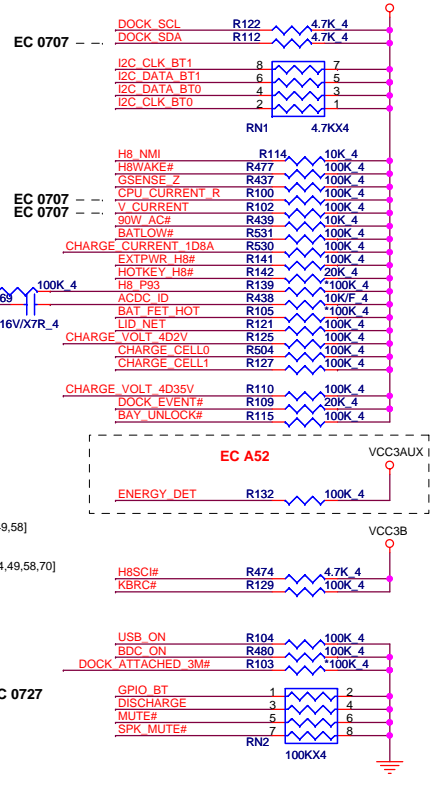
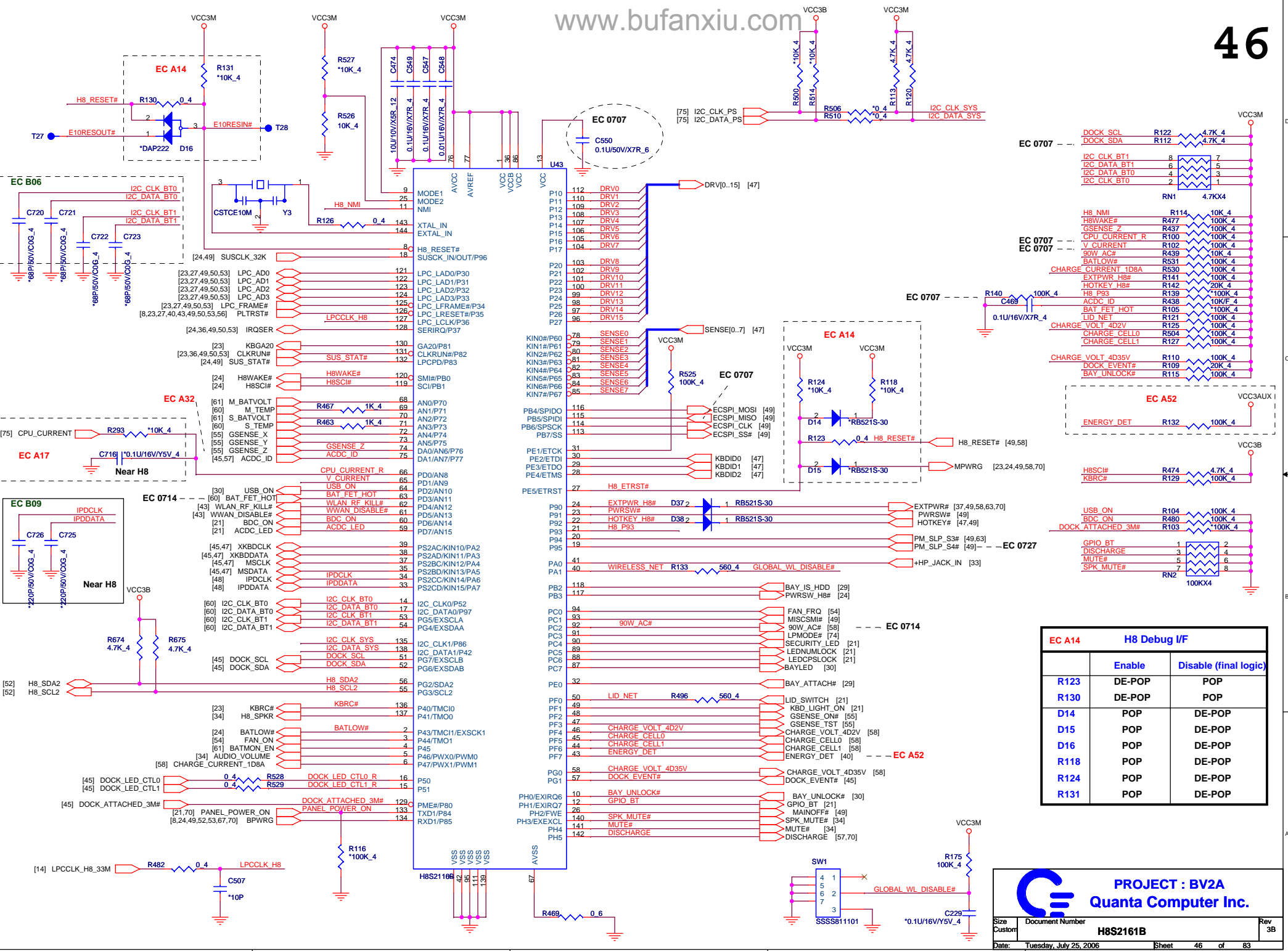
~~PLACE 16M SPI FLASH WHICH SHOULD BE ATMEL AT26DF161-SU OR THE AT26F016-SU OR ST MICRO'S ATMEL COMPATIBLE.~~

LAN SPI FLASH (BCM5752M/F)

BCM5752 / 5753 Stuff option		
	BCM5752M/F	BCM5753M/F
U32	POP	DE-POP
C266	POP	DE-POP
C263	POP	DE-POP
C257	POP	DE-POP
C261	POP	DE-POP
C264	POP	DE-POP
R205	POP	DE-POP
R207	POP	DE-POP
R473	DE-POP	DE-POP
R494	DE-POP	DE-POP
R537	DE-POP	DE-POP
R538	POP	DE-POP





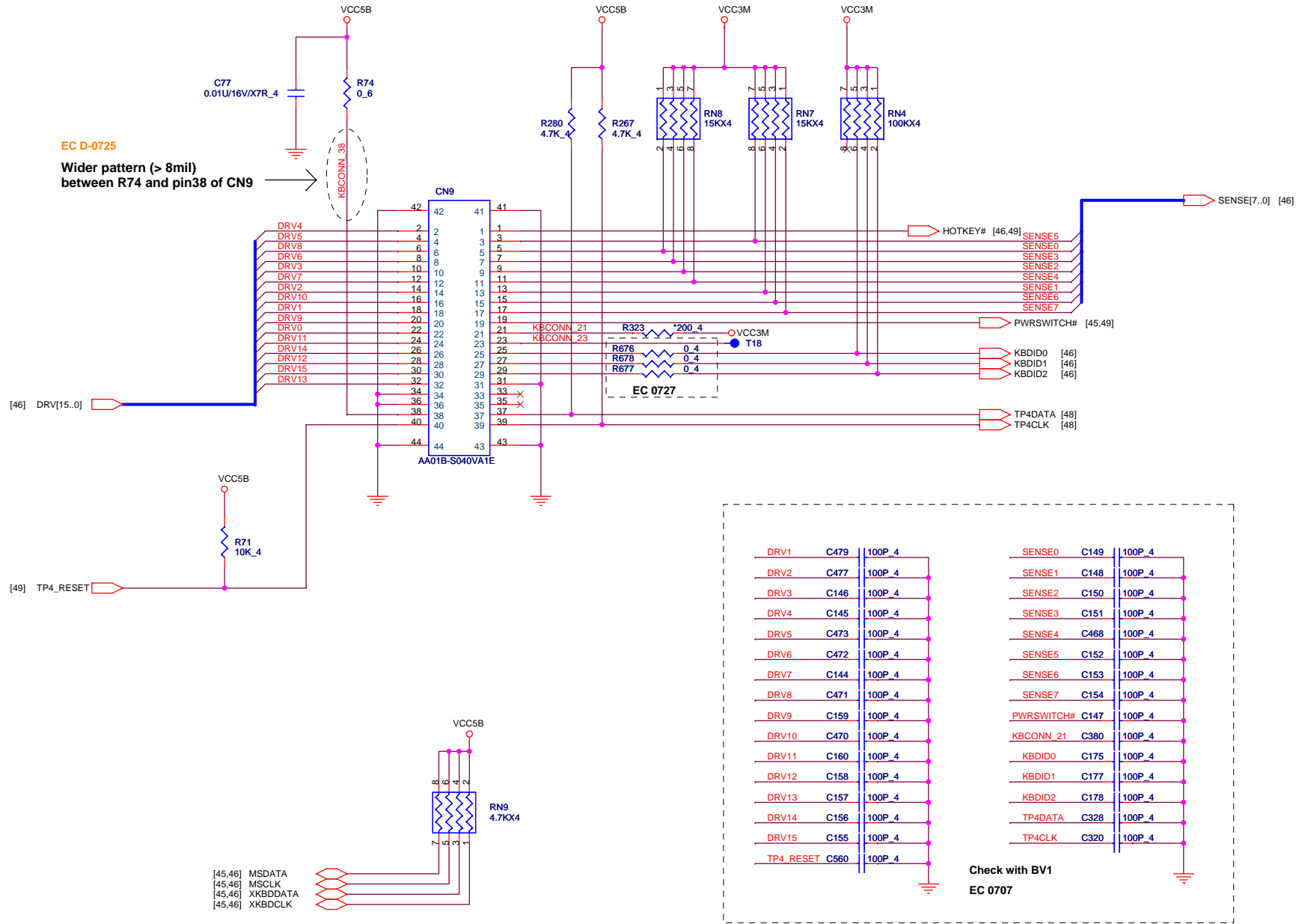


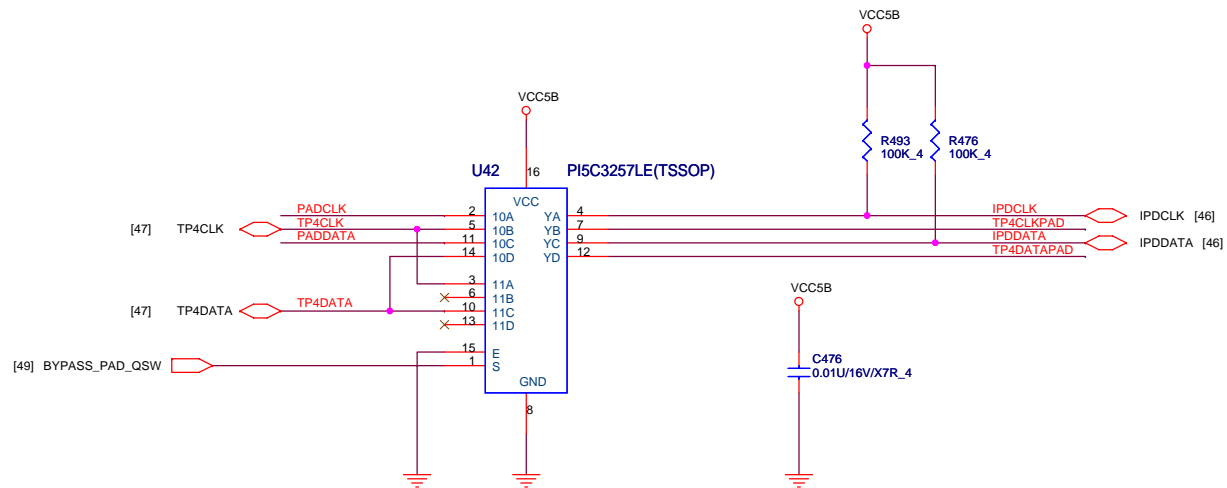
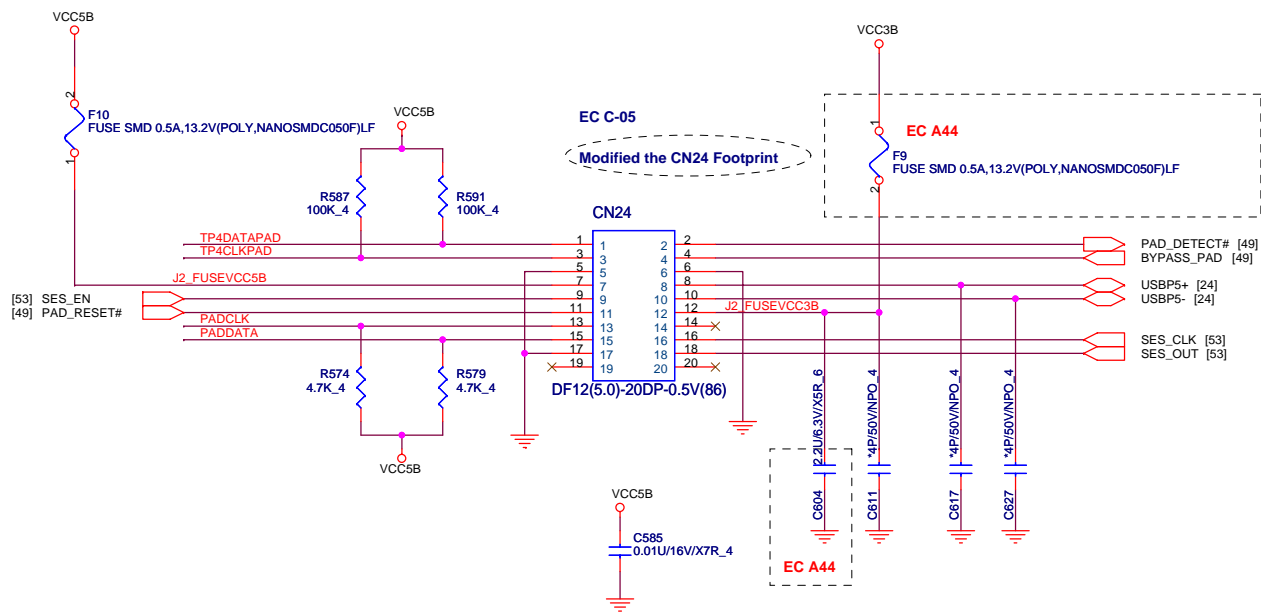
EC A14 H8 Debug I/F		
	Enable	Disable (final logic)
R123	DE-POP	POP
R130	DE-POP	POP
D14	POP	DE-POP
D15	POP	DE-POP
D16	POP	DE-POP
R118	POP	DE-POP
R124	POP	DE-POP
R131	POP	DE-POP

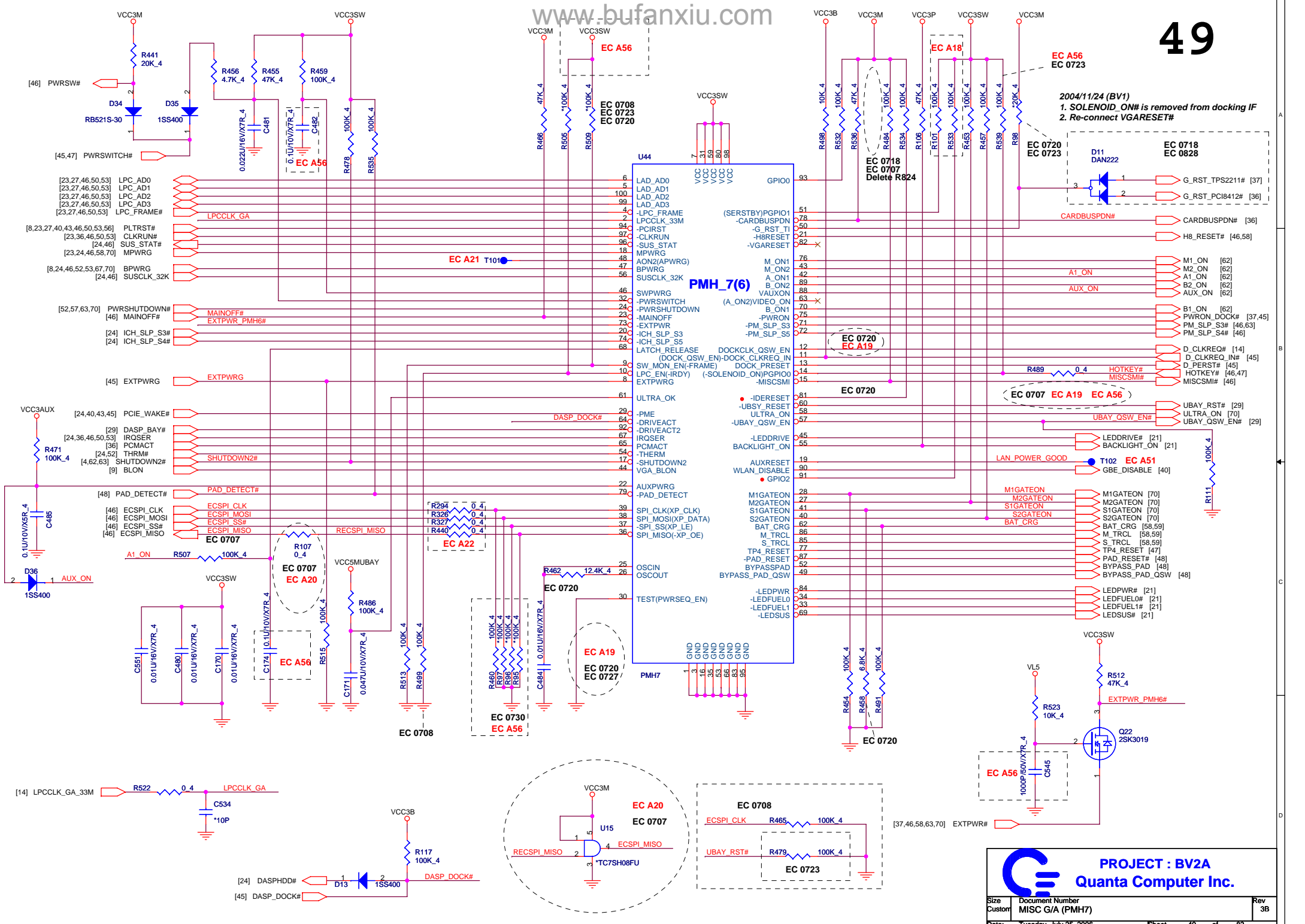
PROJECT : BV2A
Quanta Computer Inc.

Size: Custom Document Number: **H8S2161B** Rev: 3B

Date: Tuesday, July 25, 2006 Sheet: 46 of 83

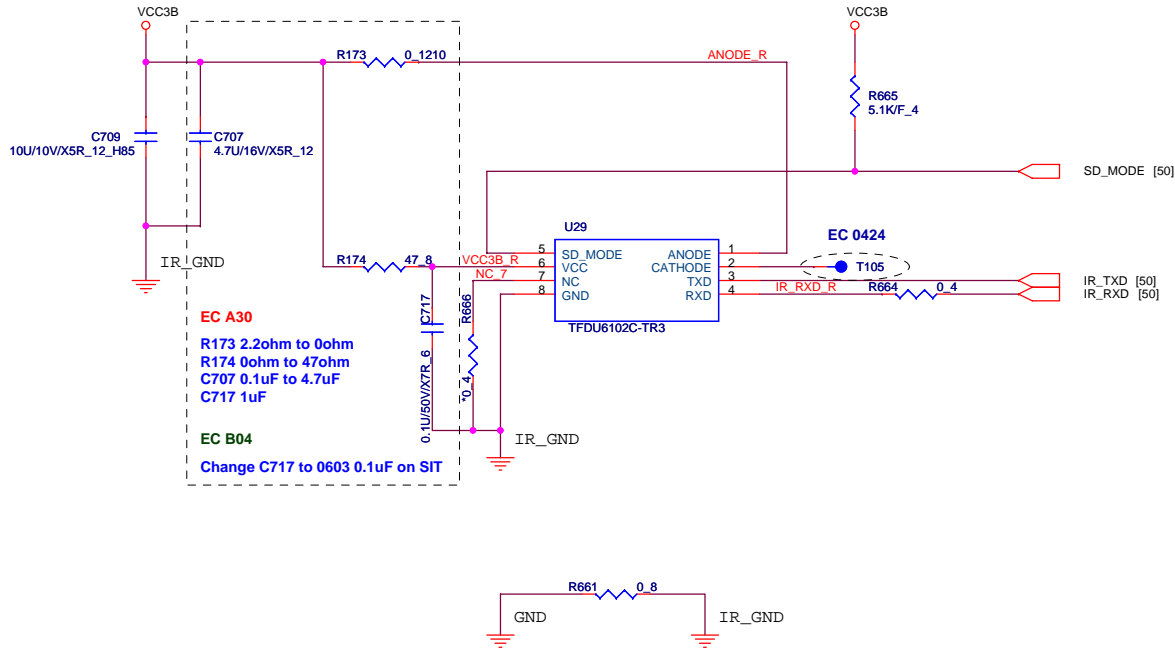


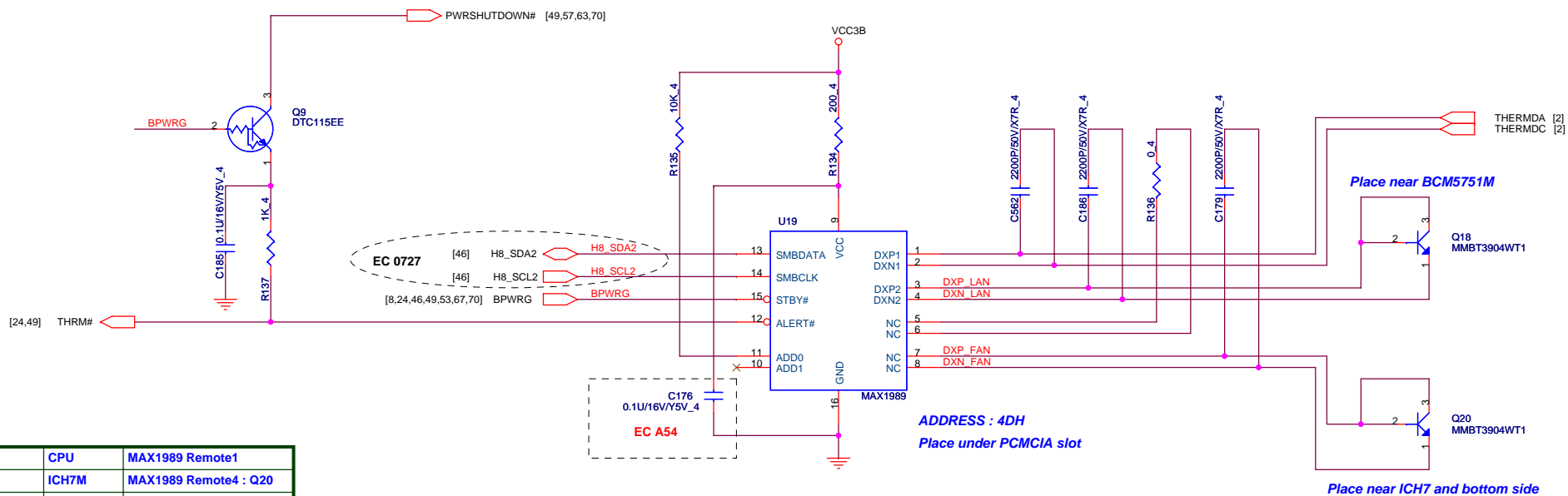




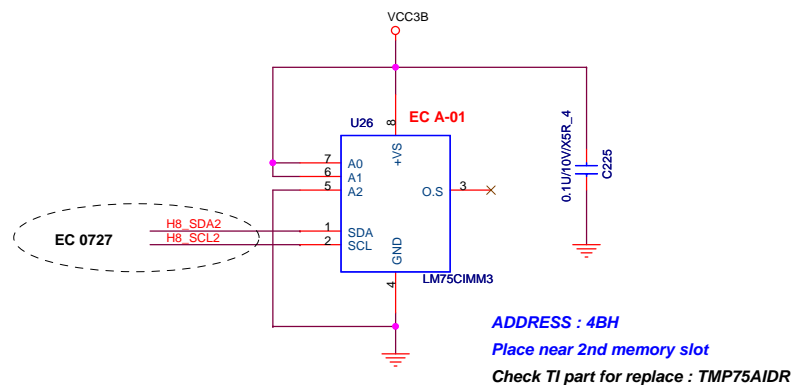
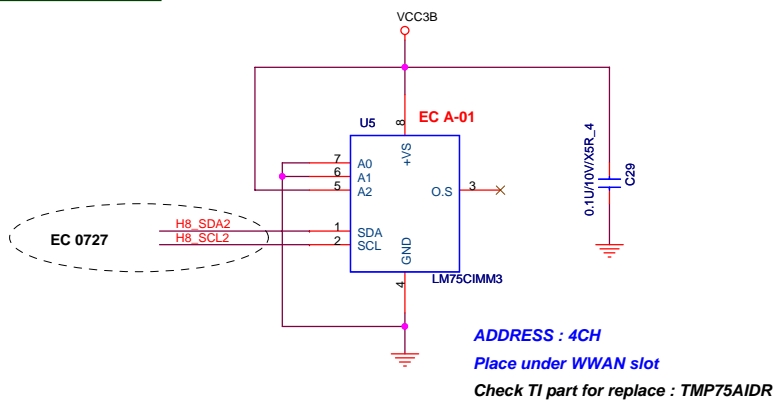
2004/11/24 (BV1)
 1. SOLENOID_ON# is removed from docking IF
 2. Re-connect VGARESET#

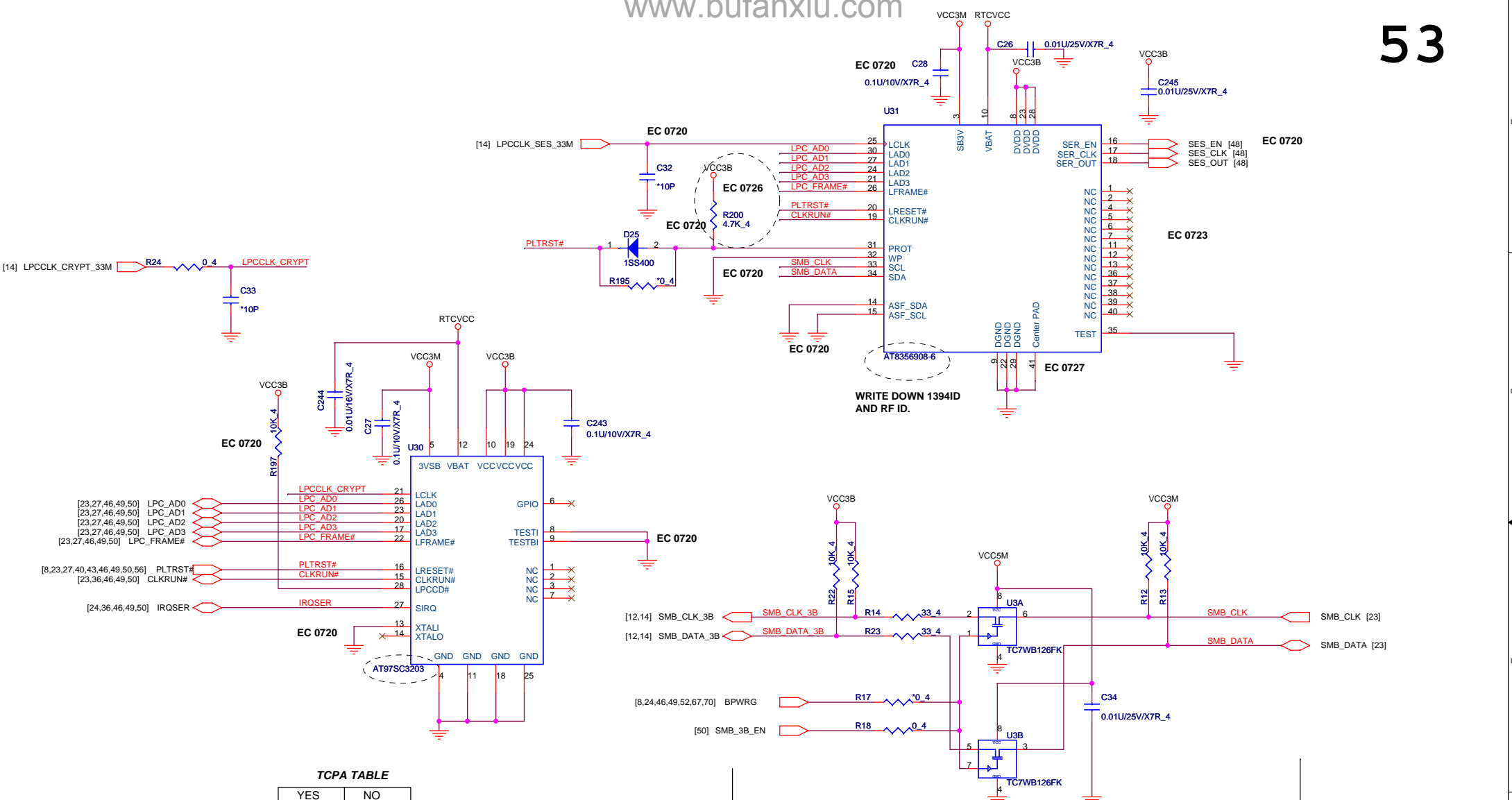
Entry Model	Normal Model
All DE-POP	All POP (Except R666)





S0	CPU	MAX1989 Remote1
S1	ICH7M	MAX1989 Remote4 : Q20
S2	WWAN	LM75 : U5
S3	---	---
S4-S7	---	Battery pack : FET, Cell
S8	DDR	LM75 : U26
S9	PCMCIA	MAX1989 Local : U19
S10	GBE	MAX1989 Remote2 : Q18





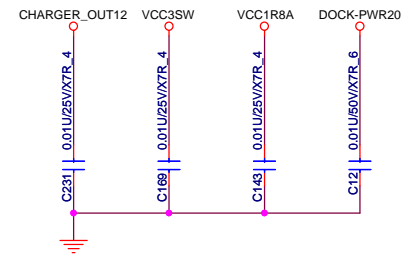
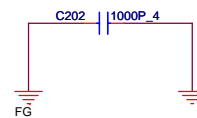
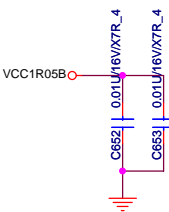
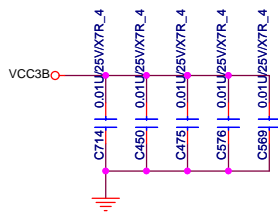
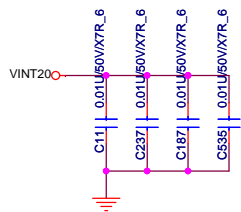
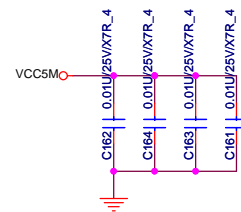
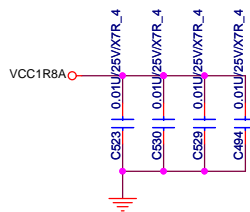
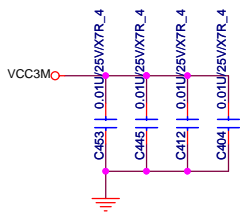
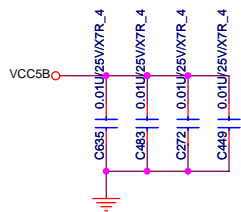
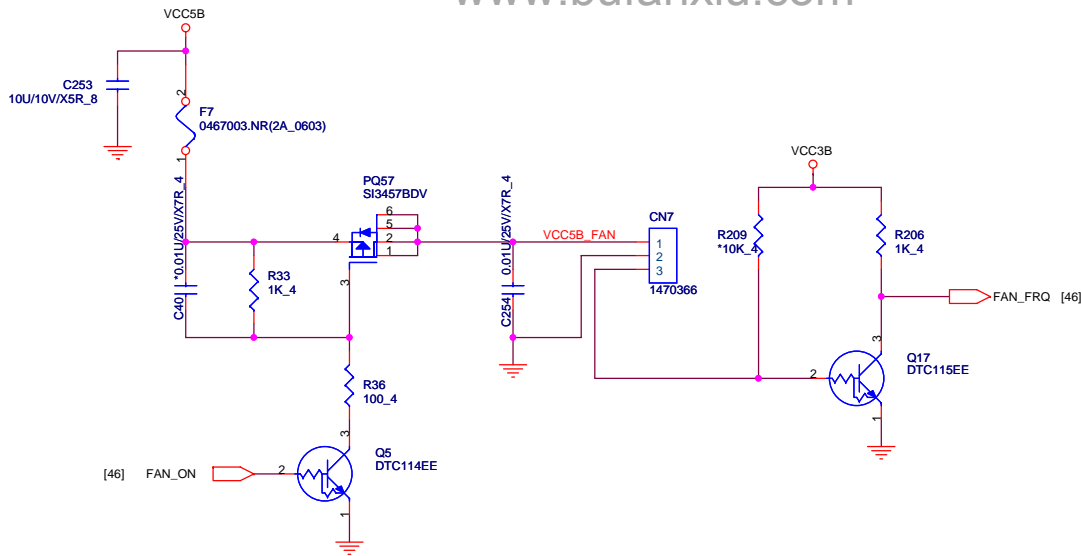
TCPA TABLE

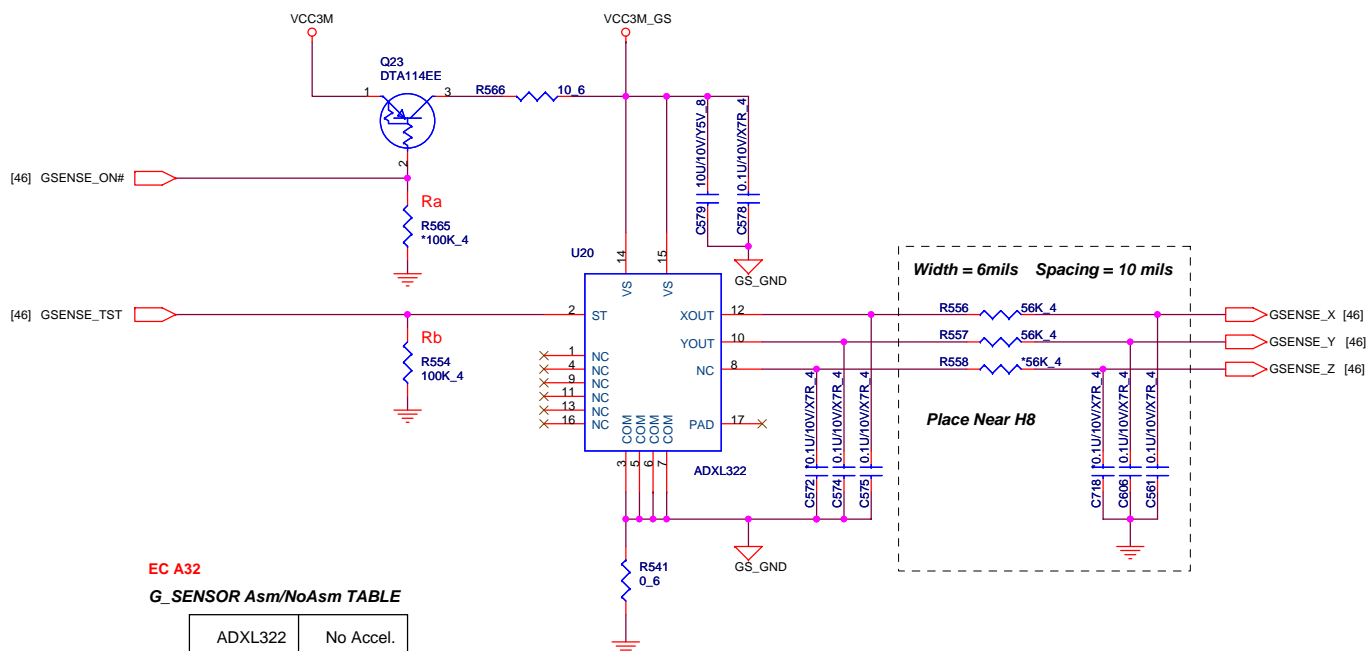
	YES	NO
U30	ASM	NO_ASM
C266	ASM	NO_ASM
C267	ASM	NO_ASM
R683	ASM	NO_ASM
R671	NO_ASM	ASM

← Check IBM R988

WRITE DOWN 1394ID AND RF ID.

Follow Intel RDDP SMBus 2.0 SPEC.

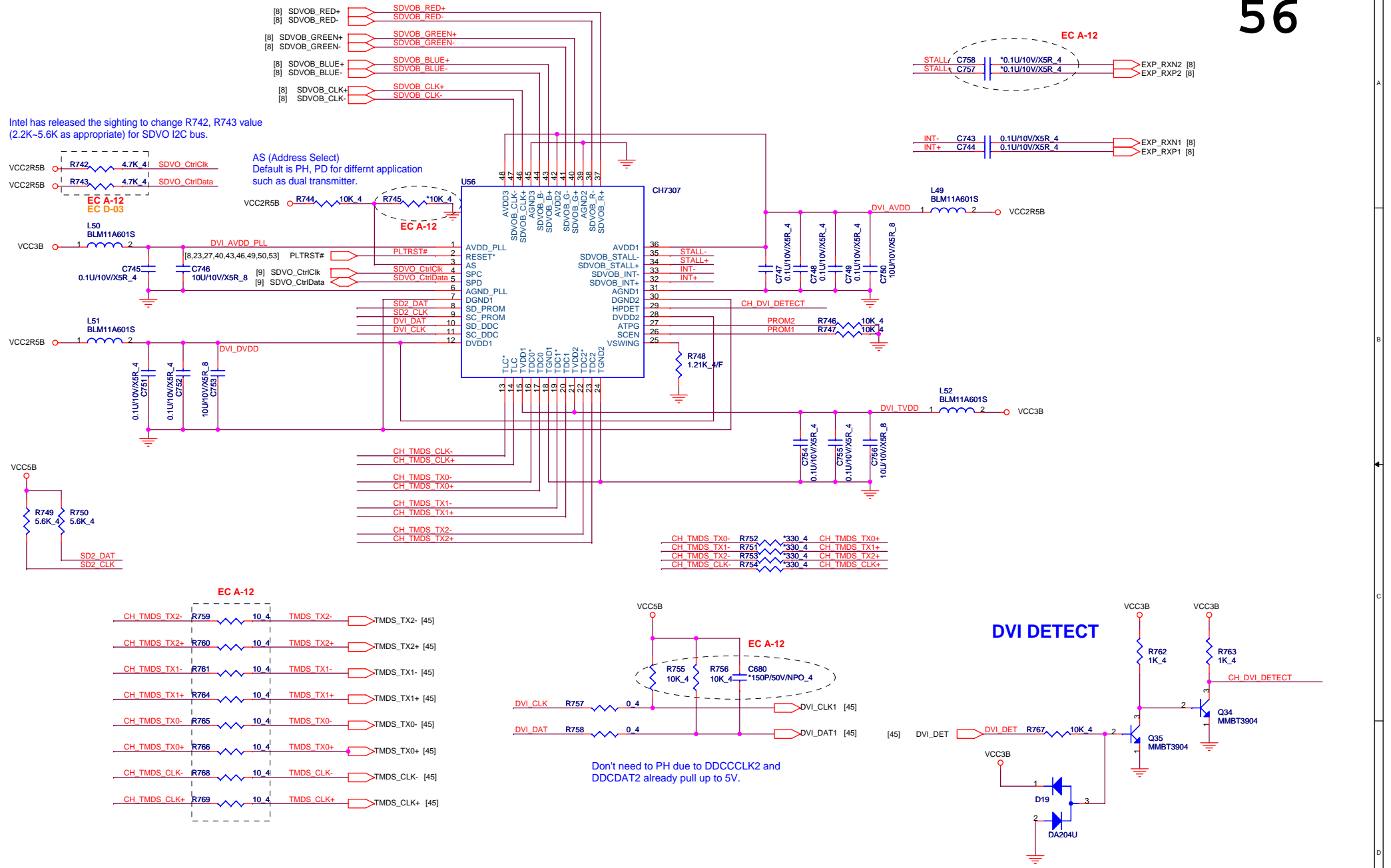




EC A32

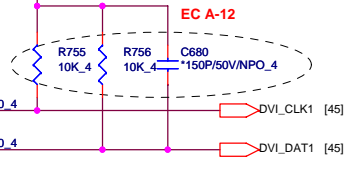
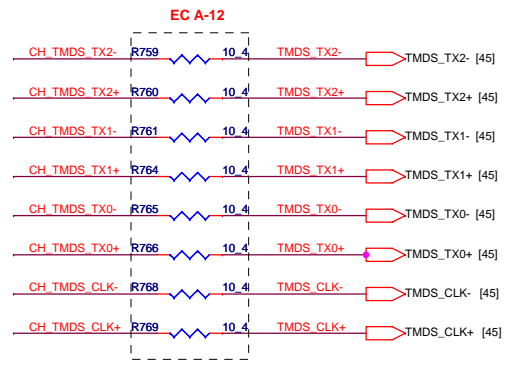
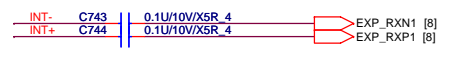
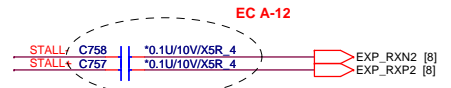
G_SENSOR Asm/NoAsm TABLE

	ADXL322	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

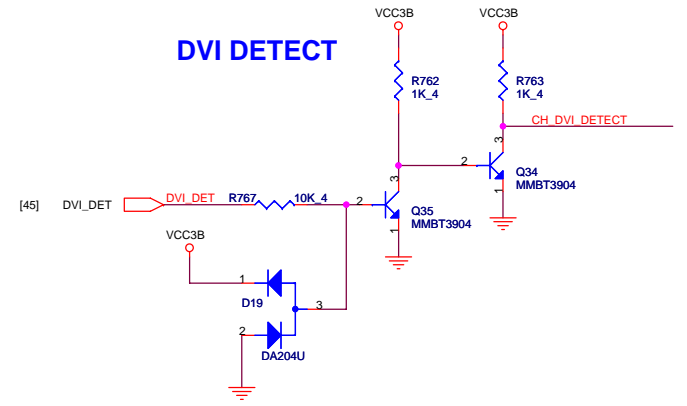


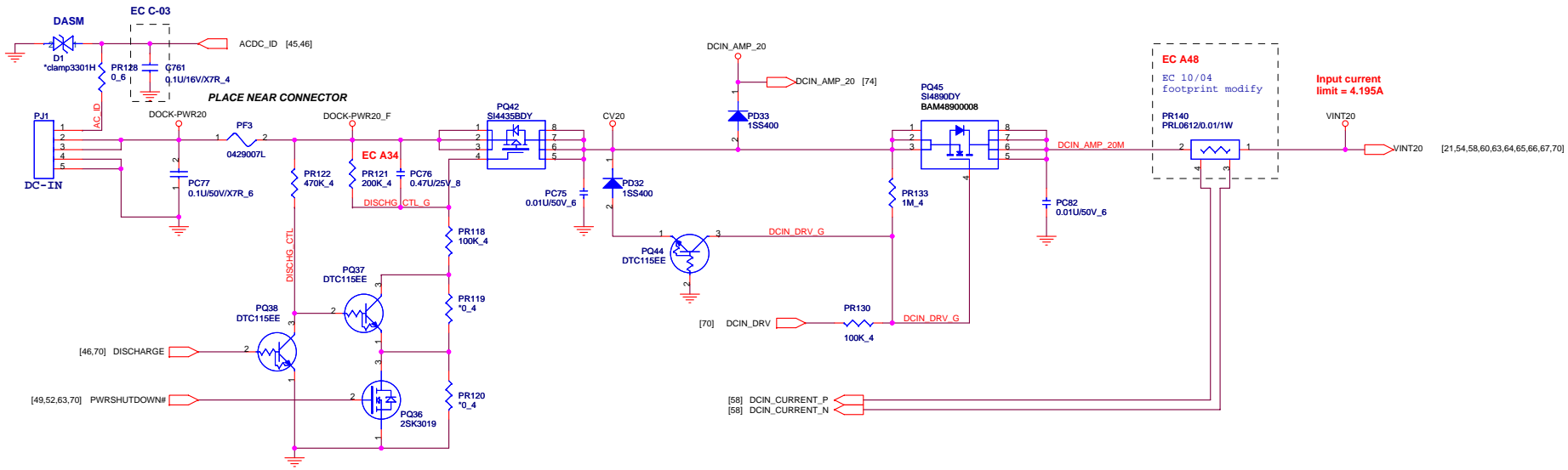
Intel has released the sighting to change R742, R743 value (2.2K-5.6K as appropriate) for SDVO I2C bus.

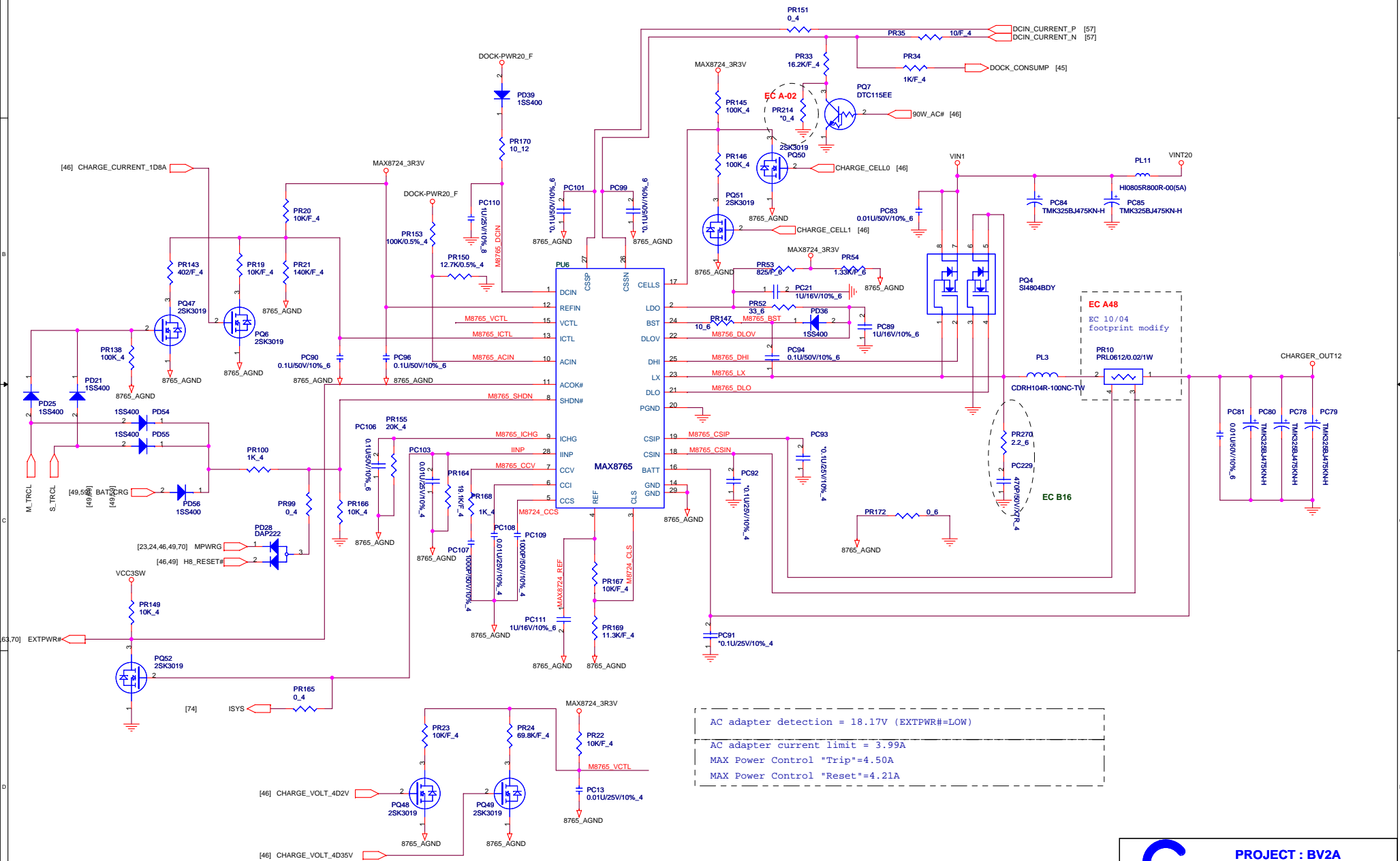
AS (Address Select)
Default is PH, PD for different application such as dual transmitter.



Don't need to PH due to DDCCCLK2 and DDCCDAT2 already pull up to 5V.



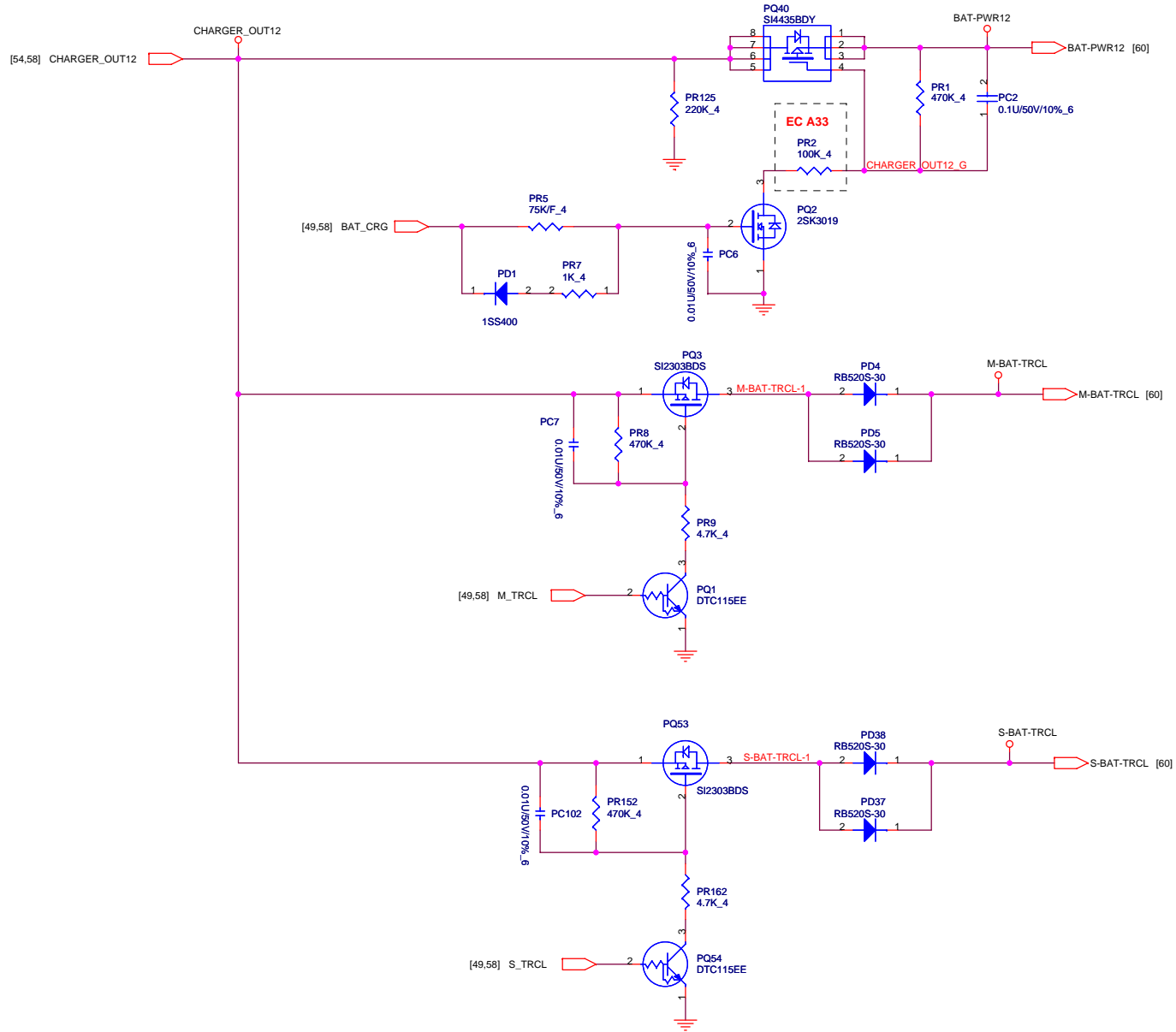


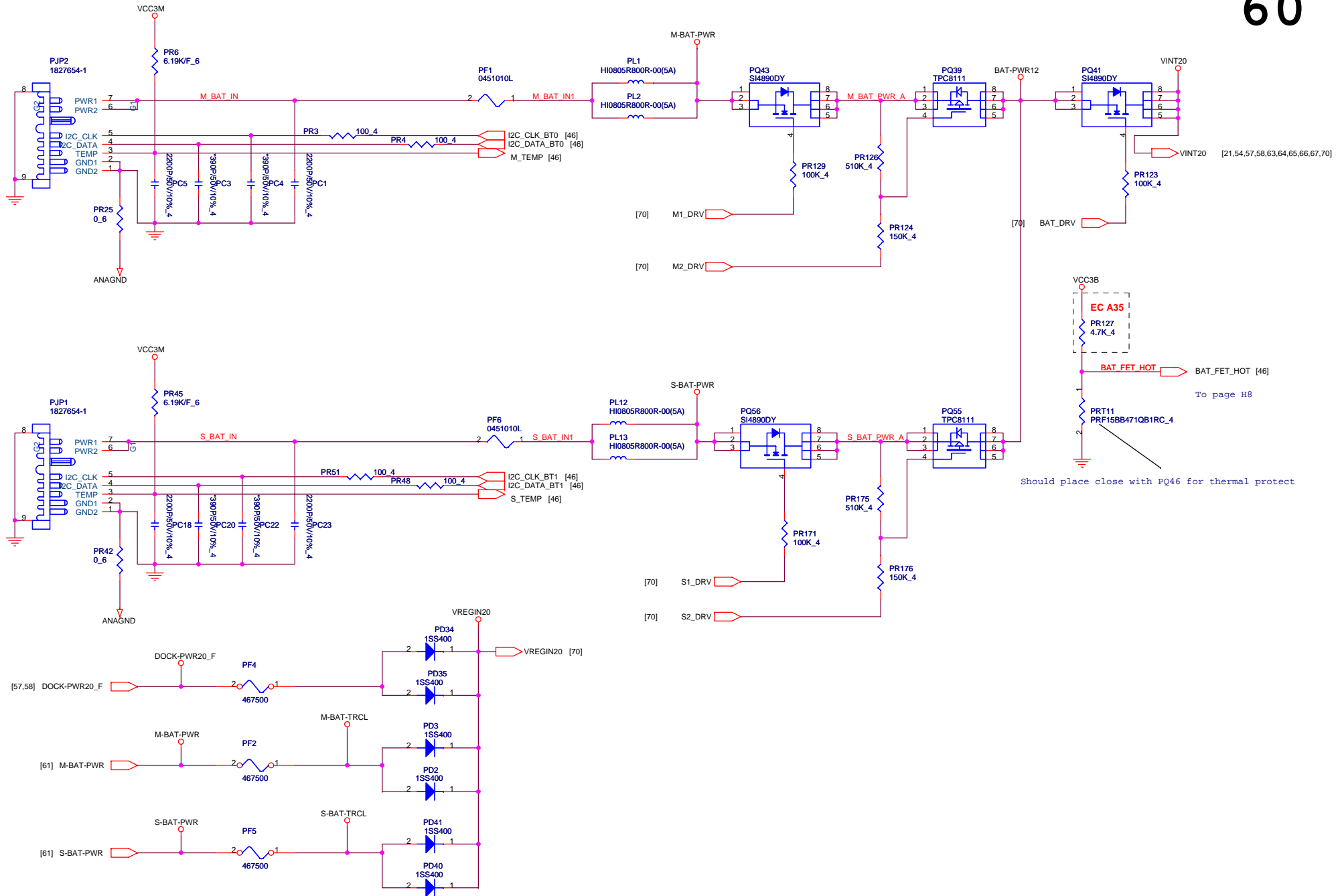


AC adapter detection = 18.17V (EXTPWR#=LOW)
 AC adapter current limit = 3.99A
 MAX Power Control "Trip"=4.50A
 MAX Power Control "Reset"=4.21A

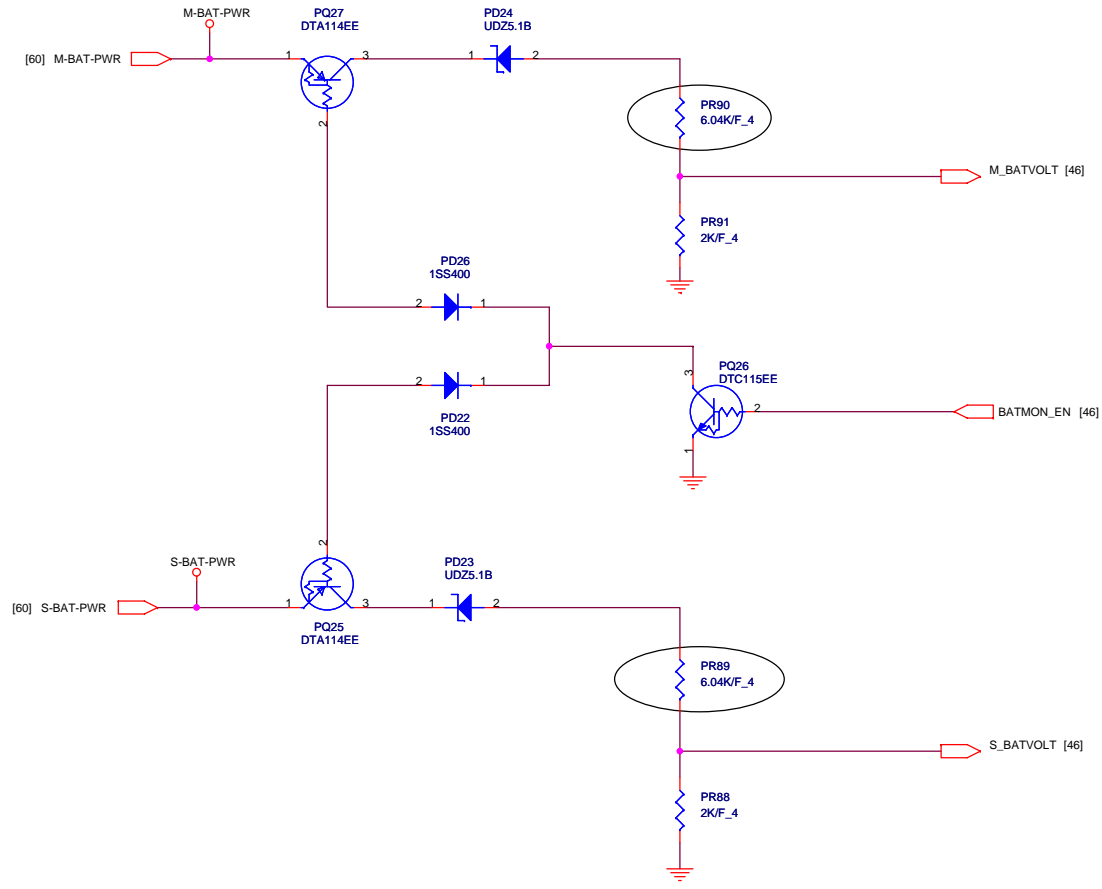
PROJECT : BV2A
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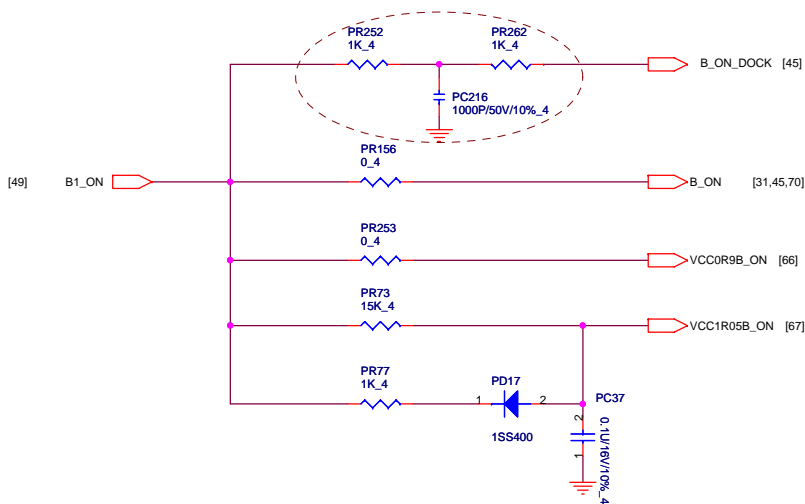
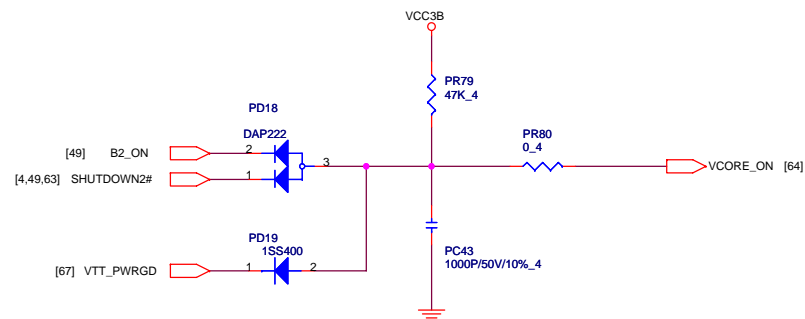
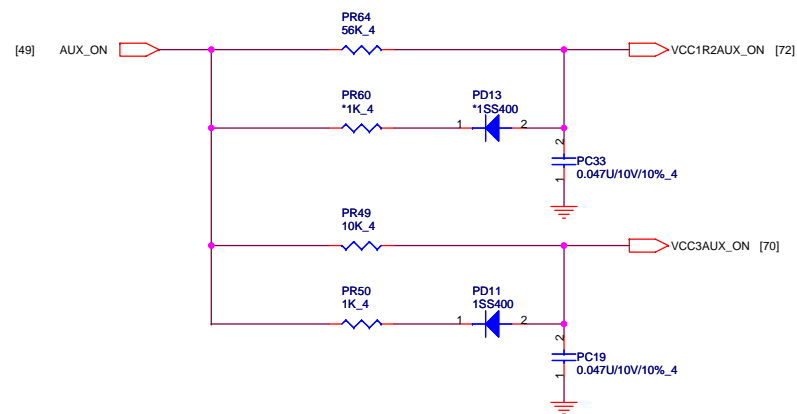
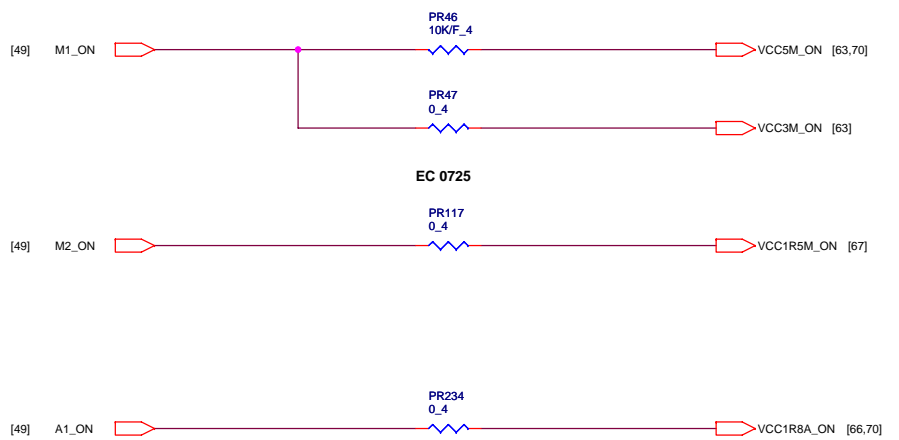
Size	Document Number	Rev
Custom	BATTERY CHARGER (MAX8765)	38
Date:	Tuesday, July 25, 2006	Sheet 58 of 83

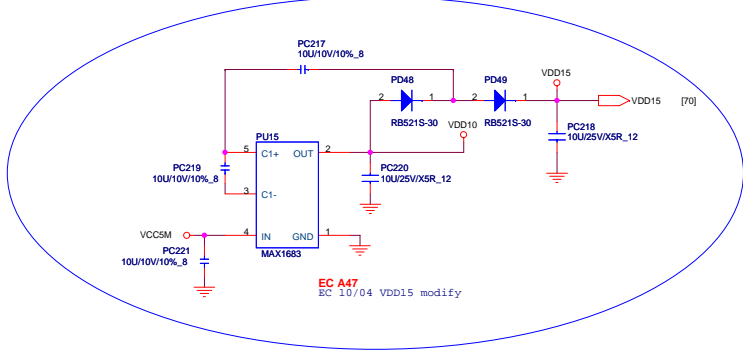
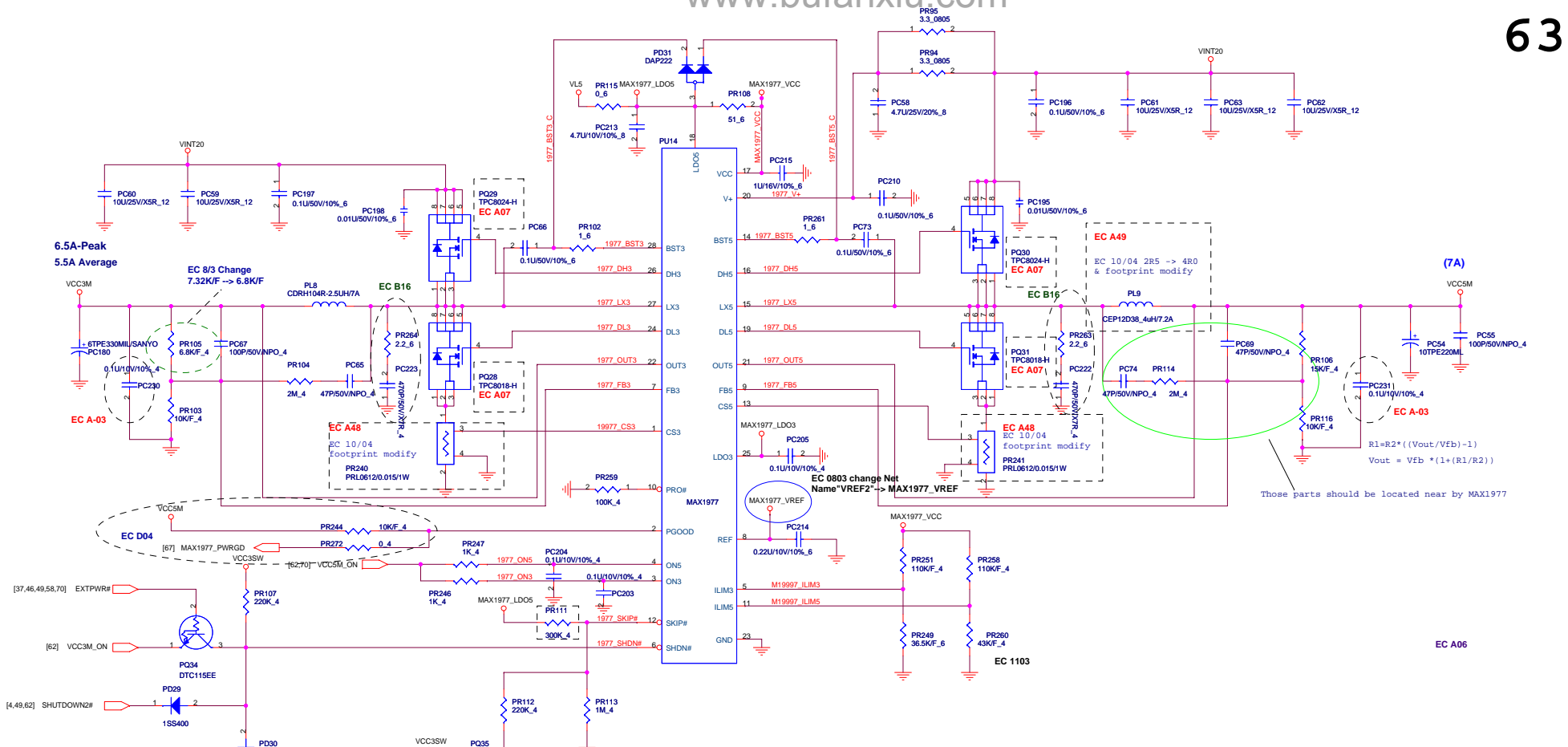


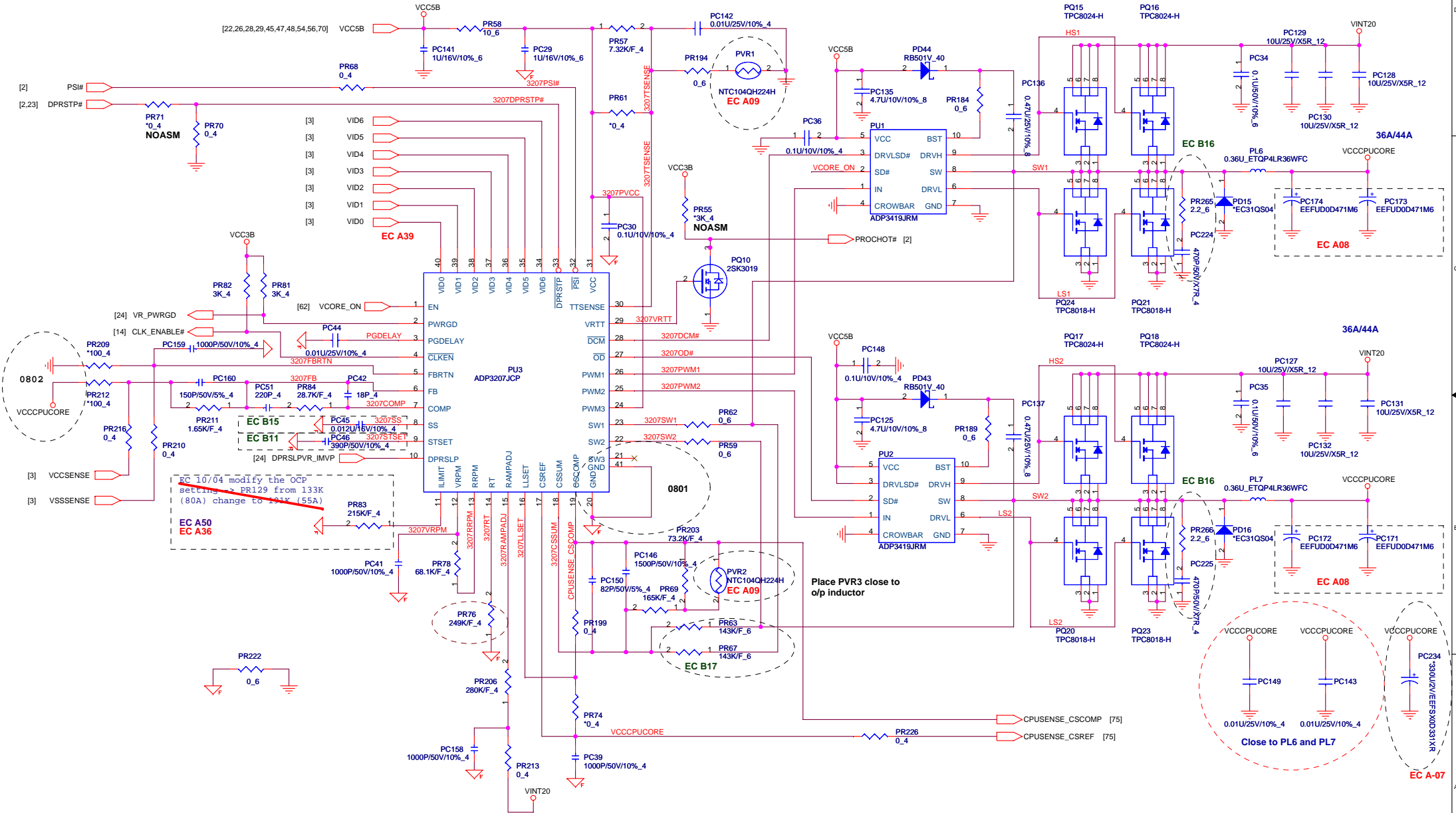


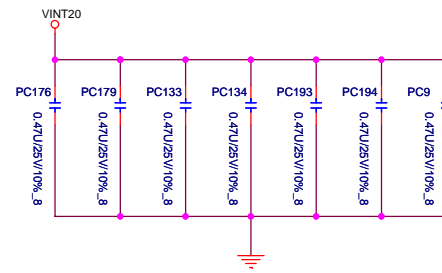
VCC3B
 EC A35
 PR127 4.7K_4
 BAT_FET_HOT [46]
 To page H8
 PR111 PRF15BB471QB1RC_4
 Should place close with PQ46 for thermal protect




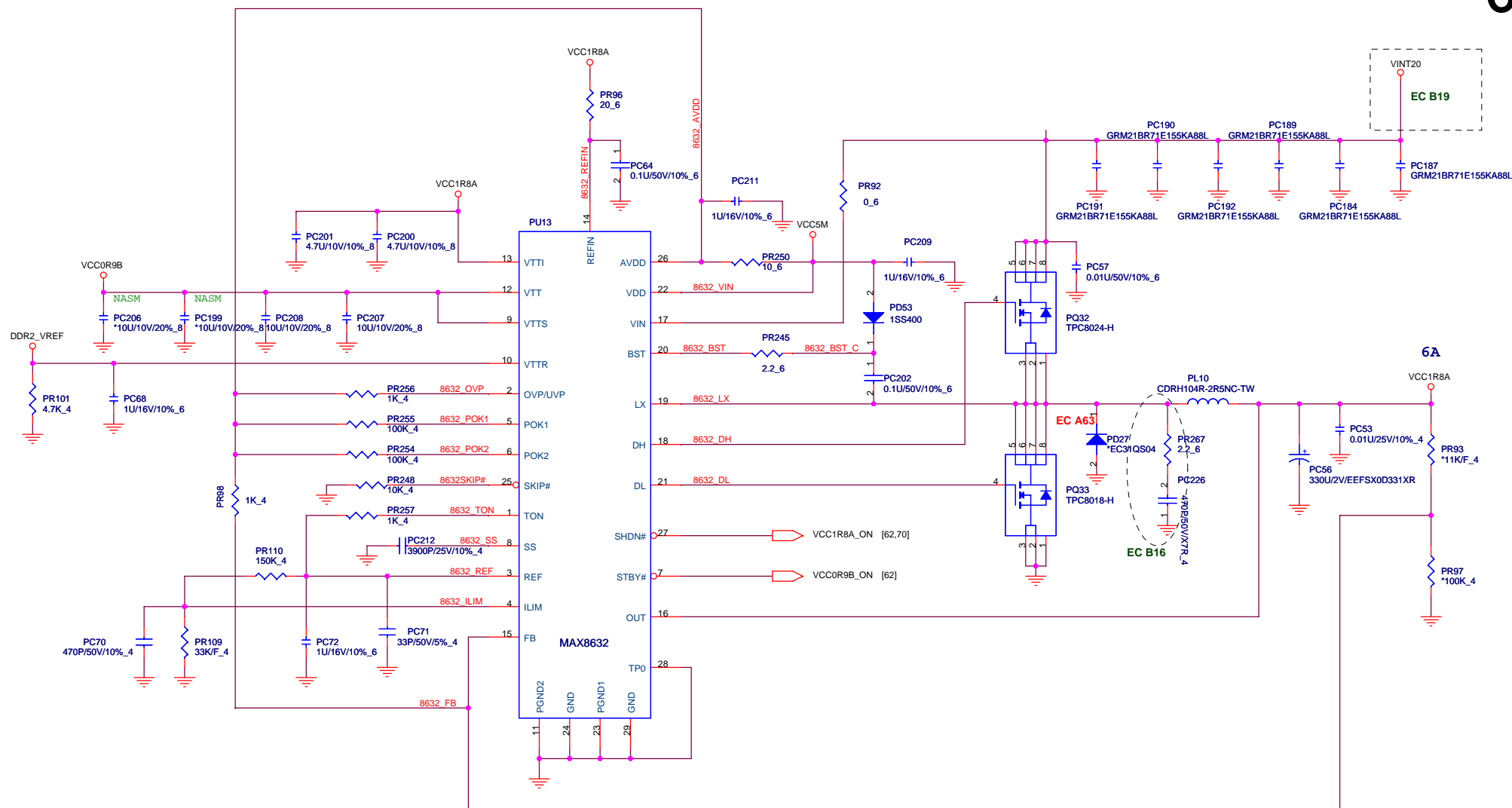


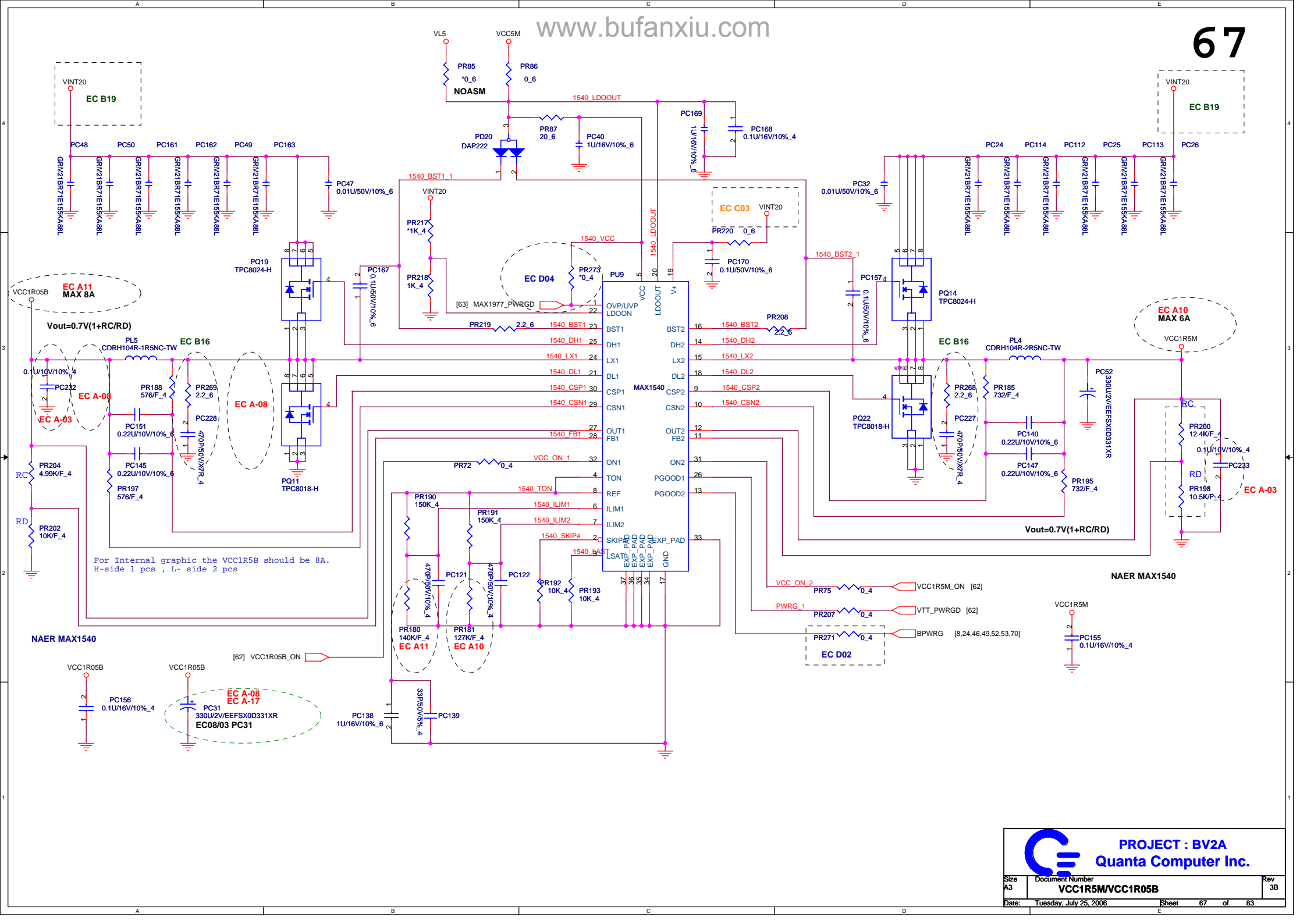







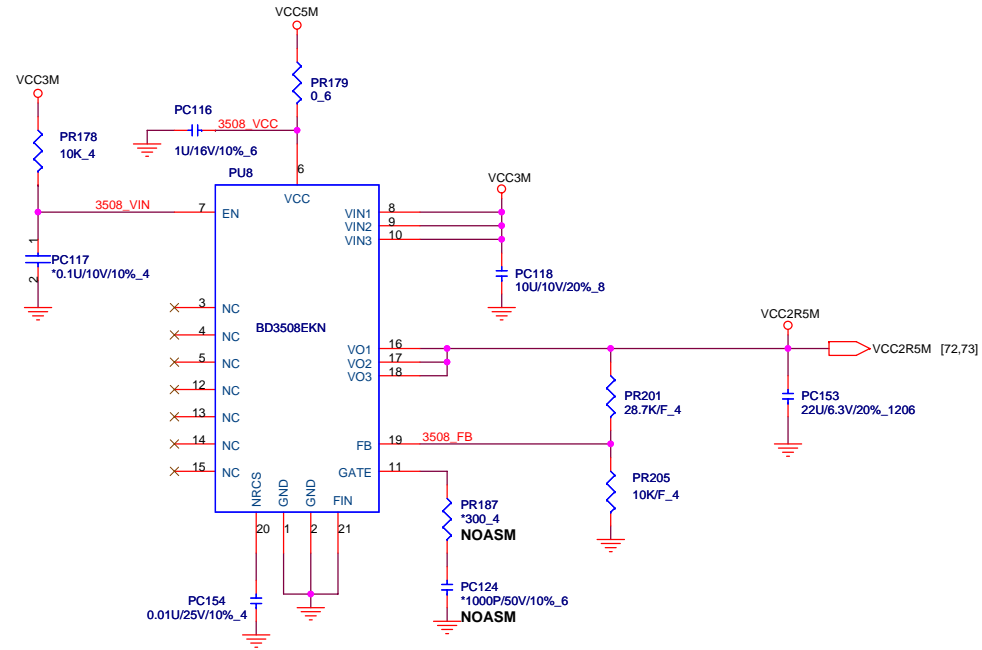
		PROJECT : BV2A Quanta Computer Inc.	
Size Custom	Document Number DC-DC VCORE INPUT CAP	Date Tuesday, July 25, 2006	Rev 3B
		Sheet 65 of 83	

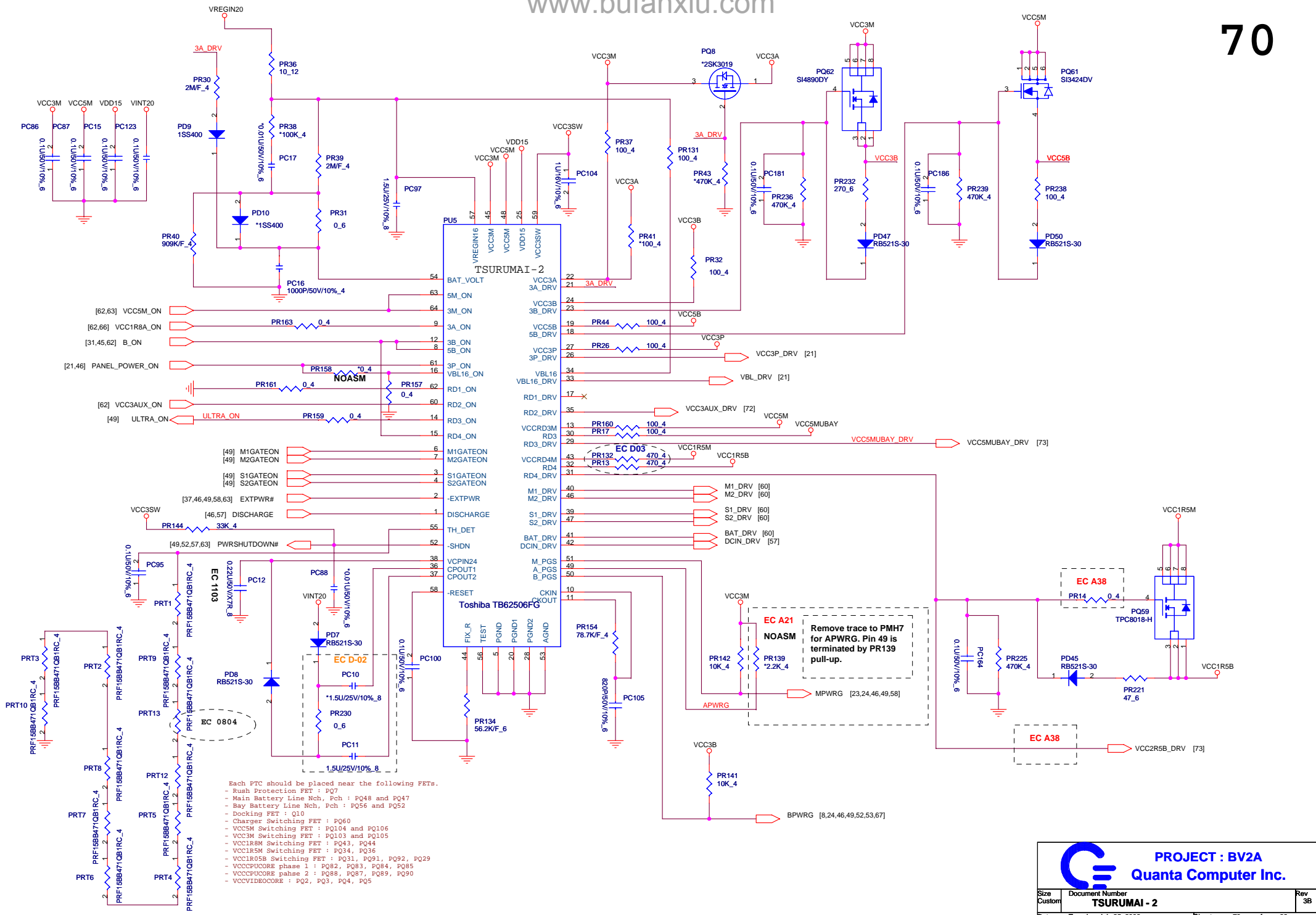




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		PROJECT : BV2A Quanta Computer Inc.
Size Custom	Document Number BLANK PAGE	Rev 3B
Date: Tuesday, July 25, 2006	Sheet 68	of 83






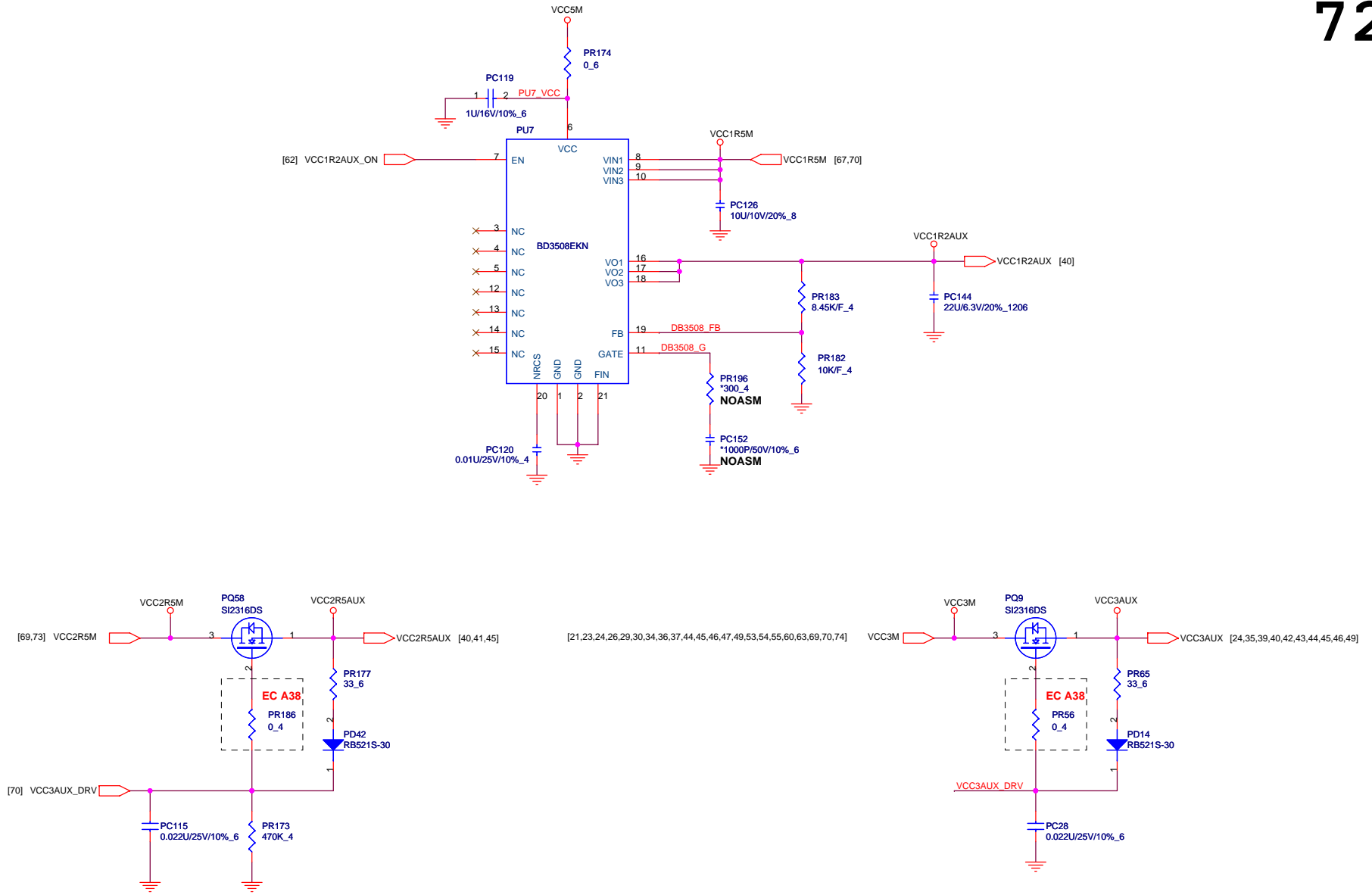
- Each PTC should be placed near the following FETs.
- Rush Protection FET : P07
 - Main Battery Line Nch, Pch : P048 and P047
 - Bay Battery Line Nch, Pch : P056 and P052
 - Docking FET : Q10
 - Charger Switching FET : P060
 - VCC5M Switching FET : P0104 and P0106
 - VCC3M Switching FET : P0103 and P0105
 - VCC1R5M Switching FET : P043, P044
 - VCC1R5M Switching FET : P034, P036
 - VCC1R05B Switching FET : P031, P031, P032, P029
 - VCCPCUCORE phase 1 : P082, P083, P084, P085
 - VCCPCUCORE phase 2 : P088, P087, P089, P090
 - VCCVIDECCORE : P02, P03, P04, P05

PROJECT : BV2A
Quanta Computer Inc.

Size	Document Number	Rev
Custort	TSURUMAI - 2	3B
Date:	Tuesday, July 25, 2006	Sheet 70 of 83

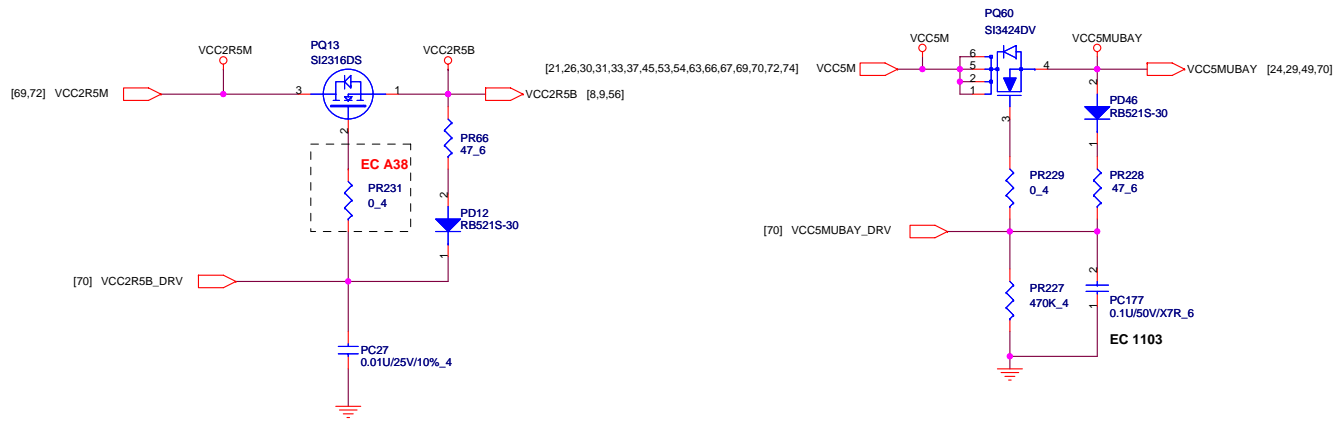
BLANK PAGE

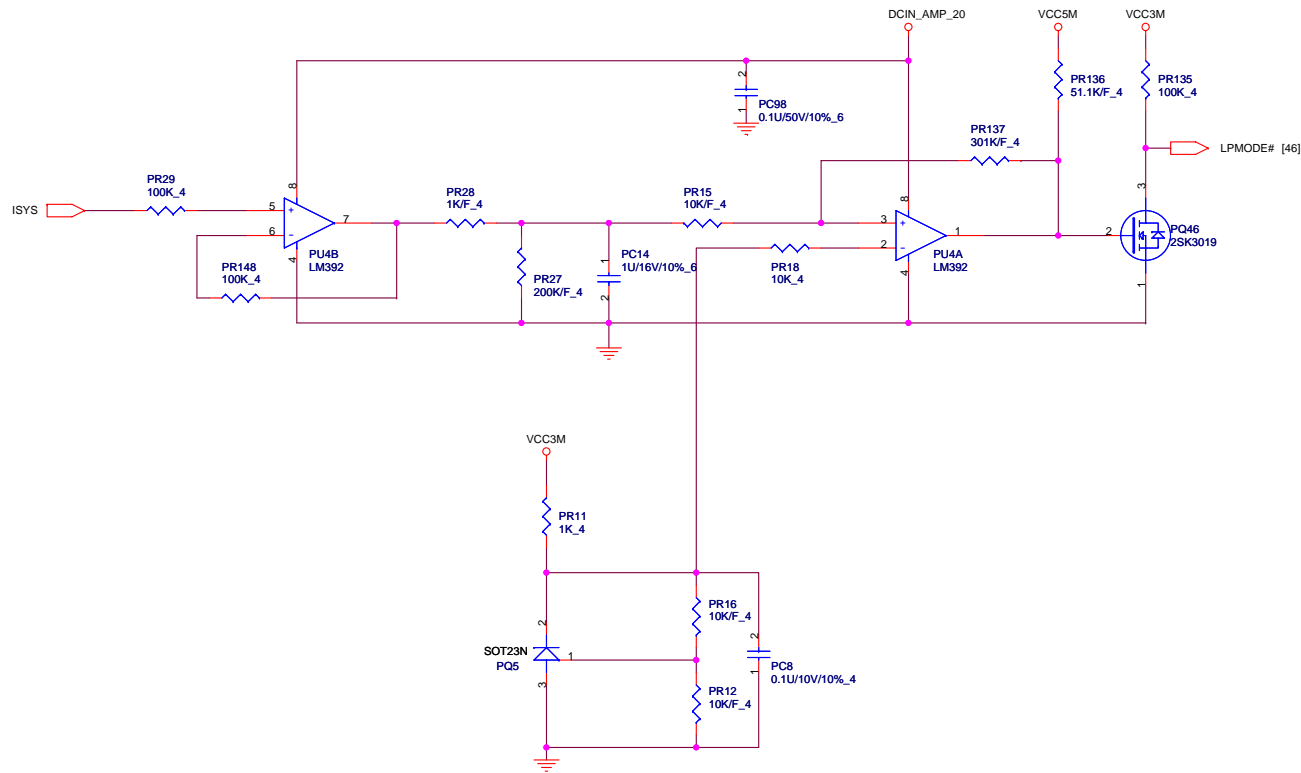
		PROJECT : BV2A Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	BLANK	3B	
Date:	Tuesday, July 25, 2006	Sheet	71 of 83

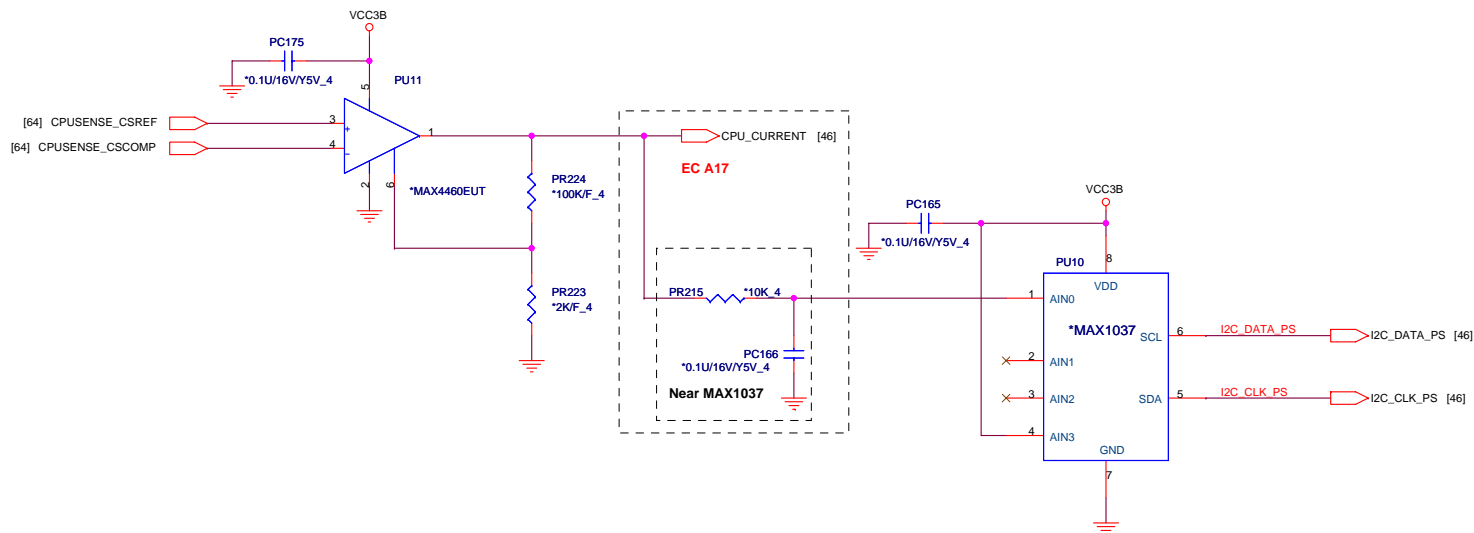


PROJECT : BV2A
Quanta Computer Inc.

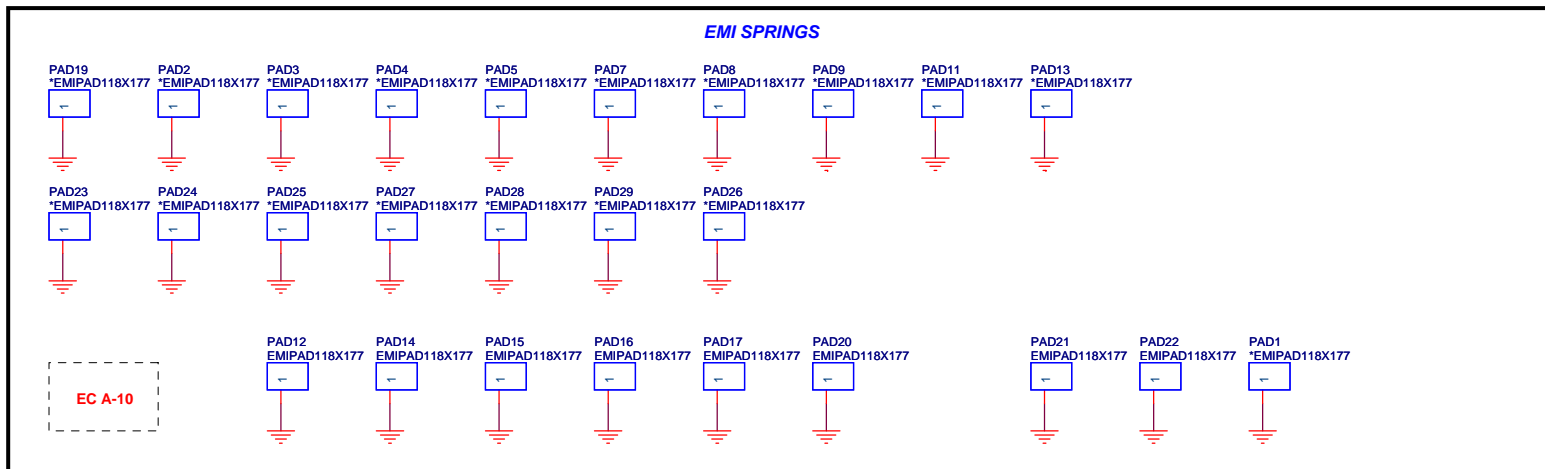
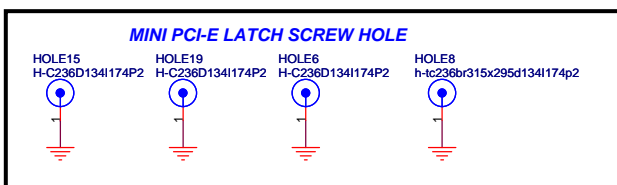
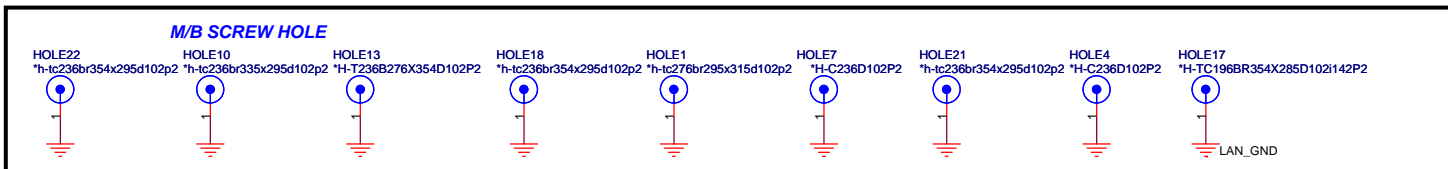
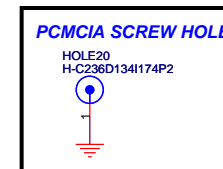
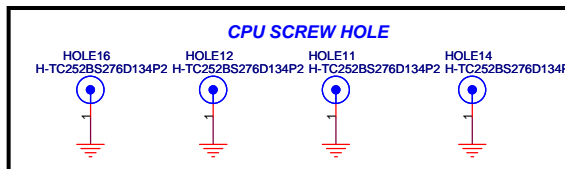
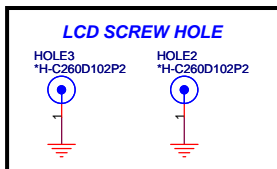
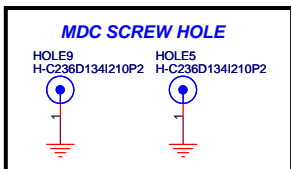
Size	Document Number	Rev
Custom	LOAD SW 2 (AUX)	3B
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SCREW HOLE



Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A	07/08 2005	DV	Initial release	08/04 2005	08/04 2005
2A	08/31 2005	SIV	Change list as Page79, 80	10/13 2005	10/12 2005
3A	11/28 2005	SIT	Change list as Page81	12/19 2005	12/05 2005
3A	01/26 2006	SIT2	Change list as Page81 (Planar ID only)	01/26 2006	01/26 2006
1A	02/22 2006	SDV	Change list as Page83 (M2.5)	02/22 2006	03/13 2006
3A	04/21 2006	SIT	Change list as Page83 (M2.5)	04/21 2006	


Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					NOASM	1K ohm 1% SMD 0402 package and NOASM
1K_6	5%		0603 (1608)				ASM	1K ohm 5% SMD 0603 package and ASM
1K_8	5%			0805 (2125)			ASM	1K ohm 5% SMD 0805 package and ASM
1K_12	5%				1206 (3216)		ASM	1K ohm 5% SMD 1206 package and ASM
1K_1210	5%					1210 (3225)	ASM	1K ohm 5% SMD 1210 package and ASM

CAPACITOR

Value	Voltage	Material	6			*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)			NOASM	0.1UF 10V X5R SMD 0402 package NOASM
1U/25V/X7R_6	25V	X7R	0603 (1608)			ASM	0.1UF 25V X7R SMD 0603 package ASM



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Size Custom	Document Number Revision	Rev 3B
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M2-NOTE SKU TABLE

When setup the BOM, please make sure every item are finalized or not !


Function	Standard	Entry	Page
GPIO9 (ICH7) R348 R689	pull-up ASM NoASM	pull-down NoASM ASM	24
WWAN (MIMI-PCIe) CN2 CN5 C250 C251 D4	Y ASM ASM ASM ASM NoASM	N NoASM NoASM NoASM NoASM NoASM	43
Camera F11	Y ASM	N NoASM	21
FingerPrint F9 C604	Y ASM ASM	N NoASM NoASM	48
TPM R396 R397 R671 R672 R24 U30 C27 C244 R197	Y ASM 2.2 ohm ASM NoASM ASM ASM ASM ASM ASM	N NoASM 33 ohm NoASM NoASM NoASM NoASM NoASM NoASM NoASM	14, 27, 53
1394 U17 EB1 EB2 CN16 C573 C632 R543 Y4 R502 R503 R517 R518 R490 C508 C552 C553 R690 R691 R501 R520	Y PCI8412ZHK ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM ASM NoASM NoASM NoASM ASM ASM ASM	N PCI8412ZHK NoASM	36
FIR R189 R190 U29 R173 R174 R664 R665 R666 R661 C707 C709 C717	Y ASM ASM ASM ASM ASM ASM NoASM ASM ASM ASM ASM	N NoASM NoASM NoASM NoASM NoASM NoASM NoASM NoASM NoASM NoASM NoASM	50, 51

TI recommend

Function	Standard	Entry	Page
MIC (Stereo/Mono) Stereo MIC Mono MIC R696 R697 R7 R8 R9	Stereo ASM ASM NoASM NoASM ASM ASM ASM	Mono NoASM ASM ASM ASM NoASM NoASM NoASM	32

EC A01/21/ USB +/- signal for camera should be swapped for FPC layout concern
 EC A02/27/ R148 value need to change to 20K_4 and C191 change 1U/16V/X5R_6 to follow Intel design guide
 EC A03/32/ R650, R651, R652 change to not ASM
 EC A04/33/ R584 change value to 5.1K_4/F
 EC A05/44/ Change FLASH for BCM5752, SI and SO need to swap (SIV-Lenovo-037)
~~EC A06/63/ Change PD48, PD49, PD51, PD52 from 1SS400 to RB521S_30 (power portion)~~
 EC A07/63/ Change PQ29,PQ30 from FDS6680AS to TPC8024-H, change PQ28,PQ31 from SI4892DY to TPC8018-H (power portion)
 EC A08/64/ Change PC171, PC172, PC173, PC174 from EEFSD0D331R to EEFUD0D471M6 (power portion)
 EC A09/64/ Change PVR1, PVR2 from TH05-3L104FR to NTC104QH224H, footprint 0603 (power portion)
 EC A10/67/ Change PR181 from 69.8K to 127K/F (power portion)
 EC A11/67/ Change PR180 from 48.7K/F to 140K/F (power portion)
 EC A12/34/ Add R673, R683, R684 to connect GND and AGND
 EC A13/43/ Non-WWAN model information (SIV-Lenovo-014)
 EC A14/46/ Disable H8 debug I/F (SIV-Lenovo-013) (SIV-Lenovo-031)
 EC A15/26/ Remove 0ohm jumper for Cost reduction (SIV-Lenovo-012)
 EC A16/30/ USB Power Distribution Switch TPS2051B->TPS2065, TPS2052B->TPS2066 (SIV-Lenovo-011)
 EC A17/46/74/ Power Monitor modify, CPU_CURRENT (SIV-Lenovo-010)
 EC A18/49/ R101, R533 change to pull-up by VCC3SW (SIV-Lenovo-009)
 EC A19/49/ Delete R440, R473, R494 for cost reduction (SIV-Lenovo-009)
 EC A20/49/ Depop U15, pop R107 for cost reduction (SIV-Lenovo-009)
 EC A21/49/70/ R460 is not needed. Remove trace between PMH7 and Tsurumai for APWRG (SIV-Lenovo-019)
 EC A22/49/ Add dumper resistors between H8 and PMH7 (SIV-Lenovo-004)
 EC A23/45/ Delete debug port
 EC A24/45/ Add R685, R686, R687, R688 but NoASM (SIV-Lenovo-007)
 EC A25/24/ Planar ID change to 0001B for SIV stage (SIV-Lenovo-001)
 EC A26/14/ CLKGen parts change to LOW Power parts (SIV-Lenovo-002)
 EC A27/08/12/ Add thermal sensor signals between Calistoga and DIMMs (SIV-Lenovo-003)
 EC A28/08/ Config 11 of Alviso (confirmation) (SIV-Lenovo-006)
 EC A29/02/ C329 ASM 100pF (SIV-Lenovo-016)
 EC A30/51/ IR capacitor add but not ASM (SIV-Lenovo-022) (SIV-Lenovo-033)
 EC A31/37/ Change R524 from 75ohm to 33ohm
 EC A32/46/55/ G-sensor Parts change and single source (SIV-Lenovo-020)
 EC A33/59/ PR2 change to 100K from 10K (SIV-Lenovo-023)
 EC A34/57/ ~~PR121 change to 100K from 220K~~ to 200K from 100K (SIV-Lenovo-024)
 EC A35/60/ PR127 change to 4.7K from 100K (SIV-Lenovo-025)
 EC A36/64/ PR83 change to 215K/F from 250K/F (SIV-Lenovo-026)
 EC A37/67/ PQ2 change to NOASM (SIV-Lenovo-027)
 EC A38/70/72/73/ EC for Load SW FETs (SIV-Lenovo-028)
~~EC A39/64/ Reserve 0ohm for VID selection~~
 EC A40/37/ R487, R497, R472 change to 10Kohm, R492 change to 22Kohm, TI SPEC
 EC A41/24/ PN10~RN15 ASM for PDD Pull-up
 EC A42/21/32/ Reserve Jump wire/cable for stereo MIC
 EC A43/27/ Delete PLCC Socket for FWH
 EC A44/24/36/78/ Entry model (SIV-Lenovo-015)
 EC A45/67/ PR200 change to 12.4K/F from 11.5K/F, PR198 change to 10.5K/F from 10K/F (SIV-Lenovo-034)
~~EC A46/44/23/27/44/ FWH change SPI FLASH (SIV-Lenovo-030)~~
 EC A47/63/ VDD15 modify (power portion)
 EC A48/57/58/63/ Change current sense resistor footprint (power portion)
 EC A49/63/ PL9 change from 2R5 to 4R0, and footprint modify (power portion)
~~EC A50/64/ PR83 change to 101K/F from 133K/F (power portion)~~

- EC A51/40/49/ BCM5752 VMAINPRSNT change to connect VCC3B (SIV-Lenovo-038)
- EC A52/40/46/ Energy detect EC, GPIO connect to H8 (SIV-Lenovo-038)
- EC A53/24/ GPIO13 change from STEREO_MIC# to STEREO_MIC_IN (SIV-Lenovo-036) (SIV-Lenovo-041)
- EC A54/52/ Thermal chip capacitor (SIV-Lenovo-039)
- EC A55/24/ GPIO10 change to pull up to VCC3AUX instead of VCC3B (SIV-Lenovo-035)
- EC A57/49/ PMH7 EC (SIV-Lenovo-042)
- EC A58/31/32/33/ Stereo MIC EC (SIV-Lenovo-040)
- EC A59/23/ C347 and C348 change to 15pF for RTC accuracy
- EC A60/36/ C573 and C632 change to 22pF (TXC recommend)
- EC A61/14/ C132 change to 15pF (KDS recommend)
- EC A62/21/ Reserve F11 for Camera
- EC A63/45/ PR177 change from 470K to 200K (SIV-Lenovo-043)
- EC A64/66/ DEPOP PD27 (Power portion)
- EC A65/34/ Audio AMP gain change from 9 to 10.5dB

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BV2 / M2-Note Schematic EC Tracking Record B (for SIV --> SIT) Nov. 29, 2005**EC #/Page/Description/Part Affected/CMVC #**

EC B01/21/ Add R698 47k pull-up to MICVCC for STEREO_MIC#
 EC B02/32/ Q26 base change to pull to MICVCC
 EC B03/30/ U1 and U45 add thermal pad (SIT-Lenovo-011)
 EC B04/51/ C717 footprint change from 0402 to 0603, 1u change 0.1u (SIT-Lenovo-001)
 EC B05/23/ R364 change to ASM, R365 change to NOASM (SIT-Lenovo-002)
 EC B06/46/ Reserve 68pF Cap for I2C_BT and NOASM (SIT-Lenovo-004)
 EC B07/34/ U52 MAX9750CETI should using +C2U Ver. (SIT-Lenovo-005)
 EC B08/24/ Planar ID change to 0010B for SIT stage (SIT-Lenovo-006)
 EC B09/46/ Reserve 220pF Cap for PS2/C and NOASM (SIT-Lenovo-008)
 EC B10/29/ Add 100pF capacitor on PIORDY signal near ODD connector (SIT-Lenovo-010)
 EC B11/64/ PC46 change to 390pF 10% from 690pF 10% (power portion) (SIT-Lenovo-012)
 EC B12/34/ R159 change from 4.7K to 47K (SIT-Lenovo-013)
 EC B13/36/ Card reader LED indicator should be high active (SIT-Lenovo-017)
 EC B14/09/ Add Cap to prevent S-video ripple
 EC B15/64/ PC45 change from 0.047u to 0.012u (power portion)
 EC B16/58/63/64/66/67/ Reserve snubber circuit for all switching power and ASM (power portion)
 EC B17/64/ PR63, PR67 change to 0603 footprint (power portion)
 EC B18/37/ Add R699 pull-up on xD/SD_PWR0
 EC B19/66/67/ Delete PL14, PL15, PL16 (power portion)
 EC B20/09/ R220 change to ASM 75ohm, R682 change to NoASM
 EC B21/14/23/27/44/ FWH change SPI FLASH
 EC B22/31/33/ Audio Jack sense circuit modify (SIT-Lenovo-032)
 EC A44/24/ GPIO9 for Entry model (SIT-Lenovo-029)
 EC B23/32/33/ Audio noise reduction (SIT-Lenovo-031)
 EC B24/21/ Add ESD cap for stereo MIC signals (SIT-Lenovo-037)
 EC B25/34/ C619, C620 change to 2.2U/X5R from 4.7U/Y5V (SIT-Lenovo-039)

BV2 / M2-Note Schematic EC Tracking Record C (for SIT --> SIT2) Jan. 26, 2006**EC #/Page/Description/Part Affected/CMVC #**

EC C01/02/ Change the test pad to bottom side
 EC C02/24/ Planar ID change to 0011B for SIT2 stage
 EC C03/67/ Connect VIN8 to VINT20 (SVT-Lenovo-003)

- EC D01/24/ Update plannar ID to 0100b for SVT (SVT-Lenovo-001)
- EC D02/67/ Connect BPWRG signal to PGOOD2 pin of MAX1540 thru 0ohm (SVT-Lenovo-007)
- EC D03/70/ PR13, PR132 change to 470ohm from 0ohm (SVT-Lenovo-008)
- EC D04/63/67/ connect MAX1977_PWRGD to MAX1540 (SVT-Lenovo-012)

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BV2A / M2.5-Note Schematic EC Tracking Record A (for SDV) Feb. 22, 2006**EC #/Page/Description/Part Affected/CMVC #**

EC A-01 /52/	LM75C1MM -- >> DS75U+T&R	(SDV-Lenovo-001)
EC A-02 /58/	Pull down pad (no asm) for 65W only support / Add PR214	(SDV-Lenovo-002)
EC A-03 /63/67/	Added PC230,PC231,PC232,PC233	(SDV-Lenovo-003)
EC A-04 /56/	DVI chip implementation	(SDV-Lenovo-005)
EC A-05 /24/40/	Add AND gate for PLTRST# for Gigabit ethernet	(SDV-Lenovo-006)
EC A-06 /24/	Planar ID set to "0101"	(SDV-Lenovo-007)
EC A-07 /64/	Added PC234,no ASM	(SDV-QCI Power)
EC A-08 /67/	Delete PC38,PQ12 and PC31 ASM	(SDV-QCI Power)
EC A-09 /40/	Delete I2C I/F EEPROM	(SDV-QCI EE)
EC A-10 /76/	Delete PAD10	(SDV-QCI EE)
EC A-11 /23/	detection for DVI function capability at ICH7 GPIO23	(SDV-Lenovo-008)
EC A-12 /56/	DVI parts change	(SDV-Lenovo-009)
EC A-14 /23/	C347,C348 change from 15p to 18P	(SDV-Lenovo-***)
EC A-15 /13/	Place capacitors on top size	(SDV-Lenovo-012)
EC A-13 /29/32/	C724 NoASM, Internal Stereo MIC parts change	(SDV-Lenovo-014)
EC A-16 /24/	correct Planar ID "0101b" <- Schematics indicates "1010b"	(SDV-Lenovo-018)
EC A-17 /67/	Delete description "NOASM" to avoid confusion	(SDV-Lenovo-019)
EC A-18 /03/	Change 16pcs of capacitors at CPU DC/DC : 22uF -> 10uF	(SDV-Lenovo-020)

BV2A / M2.5-Note Schematic EC Tracking Record C (for SDV-->SIT) Apr. 21, 2006**EC #/Page/Description/Part Affected/CMVC #**

EC C-01 /24/	Change planar ID to 0110B	(SIT-Lenovo-001)
EC C-02 /30/	USB OC signals, change pull-up Vcc from VCC5M to VCC3M and pull-up R from 47k to 10k	(SIT-Lenovo-002)
EC C-03 /57/	Added C761 for EMI	(SIT-QCI EE)
EC C-04 /40/	Modified the U36 (Broadcom5752M) footprint	(SIT-QCI EE)
EC C-05 /48/	Modified the CN24 (Touch PAD Connector) footprint	(SIT-QCI EE)

BV2A / M2.5-Note Schematic EC Tracking Record D (for SIT-->SVT) July. 03, 2006**EC #/Page/Description/Part Affected/CMVC #**

EC D-01 /24/	Change planar ID to 1000B	(SVT-Lenovo-001)
EC D-02 /70/	Del PD6, add R230 0 ohm and PC10 No-ASM	(SVT-Lenovo-002)
EC D-03 /56/	Change R742/R743 from 2.2K to 4.7K ohm for DVI device detect issue	(SVT-Lenovo-003)