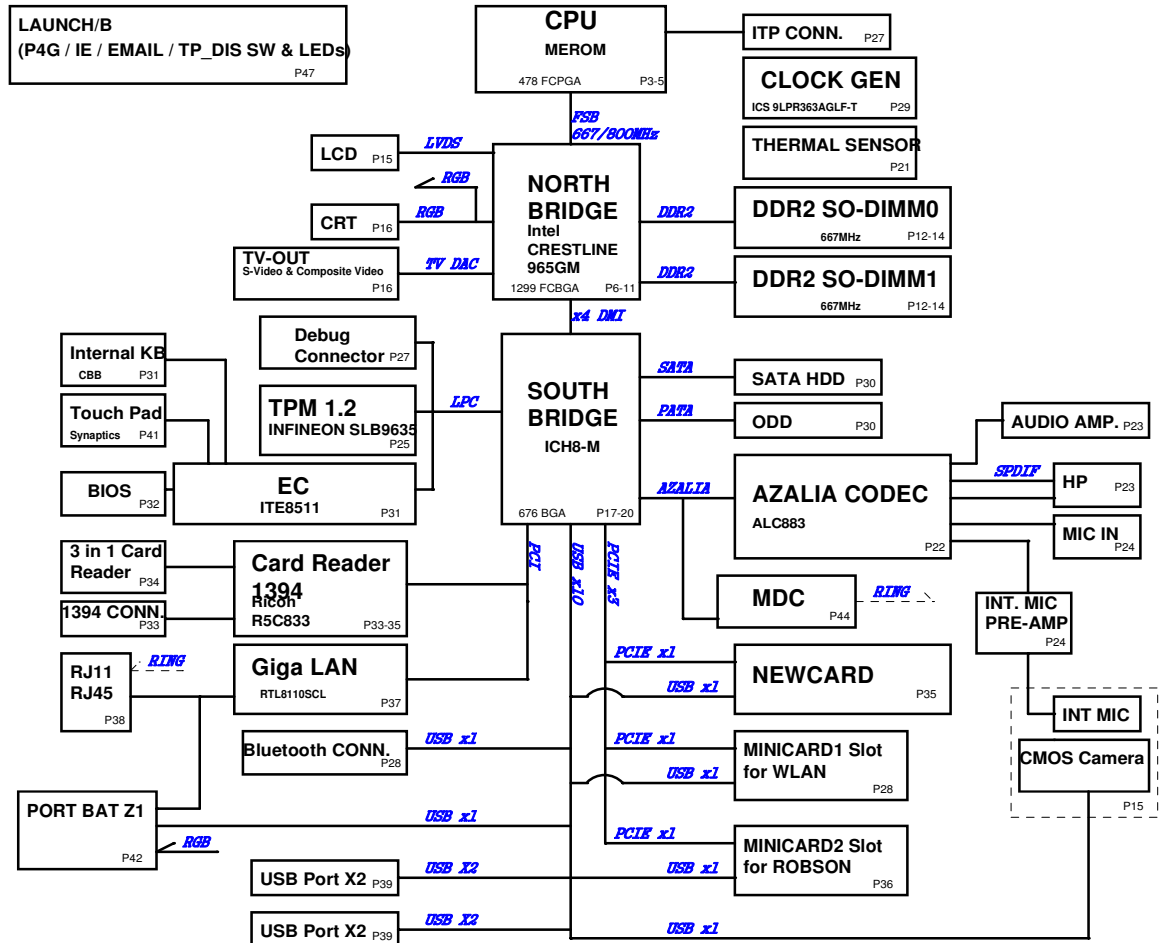


- 01_Block Diagram
- 02_System Setting
- 03_Merom CPU (1)
- 04_Merom CPU (2)
- 05_CPU CAPS.
- 06_965PM-CPU (1)
- 07_965PM-DDR2/PEG (2)
- 08_965PM-DDR2 BUS (3)
- 09_965PM-POWER (4)
- 10_965PM-POWER (5)
- 11_965PM-GND/STRAPPING (6)
- 12_DDR2 SO-DIMM0
- 13_DDR2 SO-DIMM1
- 14_DDR2 ADDRESS/TERMINATION
- 15_LVDS & INVERTER CONNECTOR
- 16_TV / CRT CONN
- 17_ICH8M(1)
- 18_ICH8M(2)
- 19_ICH8M(3)
- 20_ICH8M-PEW/GND (4)
- 21_THER SENSOR & FAN
- 22_AUDIO_CODEC_ALC883
- 23_AUDIO AMP & HP JACK
- 24_AUDIO MIC JACK & PRE-AMP
- 25_TPM / MDC CONNECTOR
- 26_BLANK
- 27_ITP & Debug CONN
- 28_MiniCard1 (WLAN) / BT CONN
- 29_CLOCK_GEN-IC9LPR363AGLF-T
- 30_SATA-HDD & ODD
- 31_EC-IT8511TE(1/2)
- 32_EC-IT8511TE(2/2) & ISA ROM
- 33_RICOH-R5C833_PCI
- 34_RICOH-R5C833_1394/SD
- 35_3 in 1 CARD READER
- 36_MiniCard2 (ROBSON)
- 37_LAN-RTL8110SCL
- 38_RJ45/RJ11
- 39_USB CONN
- 40_DISCHARGE
- 41_LED / SW / TOUCHPAD CONN
- 42_PORT BAR_Z1
- 43_NEWCARD
- 44_POWER-ON SEQUENCE
- 45_DCIN & BAT CONN
- 46_SREW HOLE
- 47_LAUNCH/B CONN
- 48_POWER_FLOWCHART
- 49_POWER_CHARGER
- 50_POWER_SYSTEM_+3VO & +5VO
- 51_POWER_VCORE
- 52_POWER_IO_DDR & VTT
- 53_POWER_VCCGFX
- 54_POWER_IO_+3VAO & +2.5VS
- 55_POWER_IO_1.5VS & 1.15VS
- 56_POWER_GOOD_DETECT
- 57_POWER_LOAD SWITCH
- 58_POWER_IO_Linear
- 59_History (1)



<< Kennedy_Zhang >>

ASUS		Title: BLOCK DIAGRAM
ASUSTek COMPUTER INC.		Engineer: Mike Lee
Site	Project Name	Rev
Custom	Z62E	2.0G
Date: 8/8 - 8/15, 2007	Sheet	1 of 59

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSERVE#	O
37	PWM3/GPA3	/	O
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRLL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDA10GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A2OGATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	O
47	CLKOUT/GPC0	/	O
169	SMB1/GPC1	SMB1_CLK	I/O
170	SMDA11/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	R11#WUI0/GPD0	SUSB#	I
29	R12#WUI1/GPD1	SUSC#	I
30	LPCRS1#WUI4/GPD2	PLT_RST#	I
31	ECSC#GPD3	EXT_SCI#	O
41	GPD4	/	O
42	GINT/GPD5	/	O
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	I
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	I
24	LPCPD#WUI6/GPE6	LID_EC#	I
25	CLKRUN#WUI7/GPE7	/	I
110	PS2CLK0/GPF0	/	I
111	PS2DAT0/GPF1	/	I
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	O
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	O
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin Pin Name Signal Name Type

48	GPH0	VSUS_ON	O
54	GPH1	VSUS_G#	O
55	GPH2	CP-OPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICHT_PWROK	O
149	GPI1	/	O
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICHT-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCL_REQ#5	I/O	Core(To:3.5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:3.5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:3.5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:3.5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:3.5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCL_GNT#5	I/O	Core(To:3.3V)	LAN
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	LAN
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCL_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(To:3.3V)	Native
AG21	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_I0#	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
1394	AD17	0	INTA
CARD READER	AD17	0	INTB
LAN	AD23	2	INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

<Variant Name>

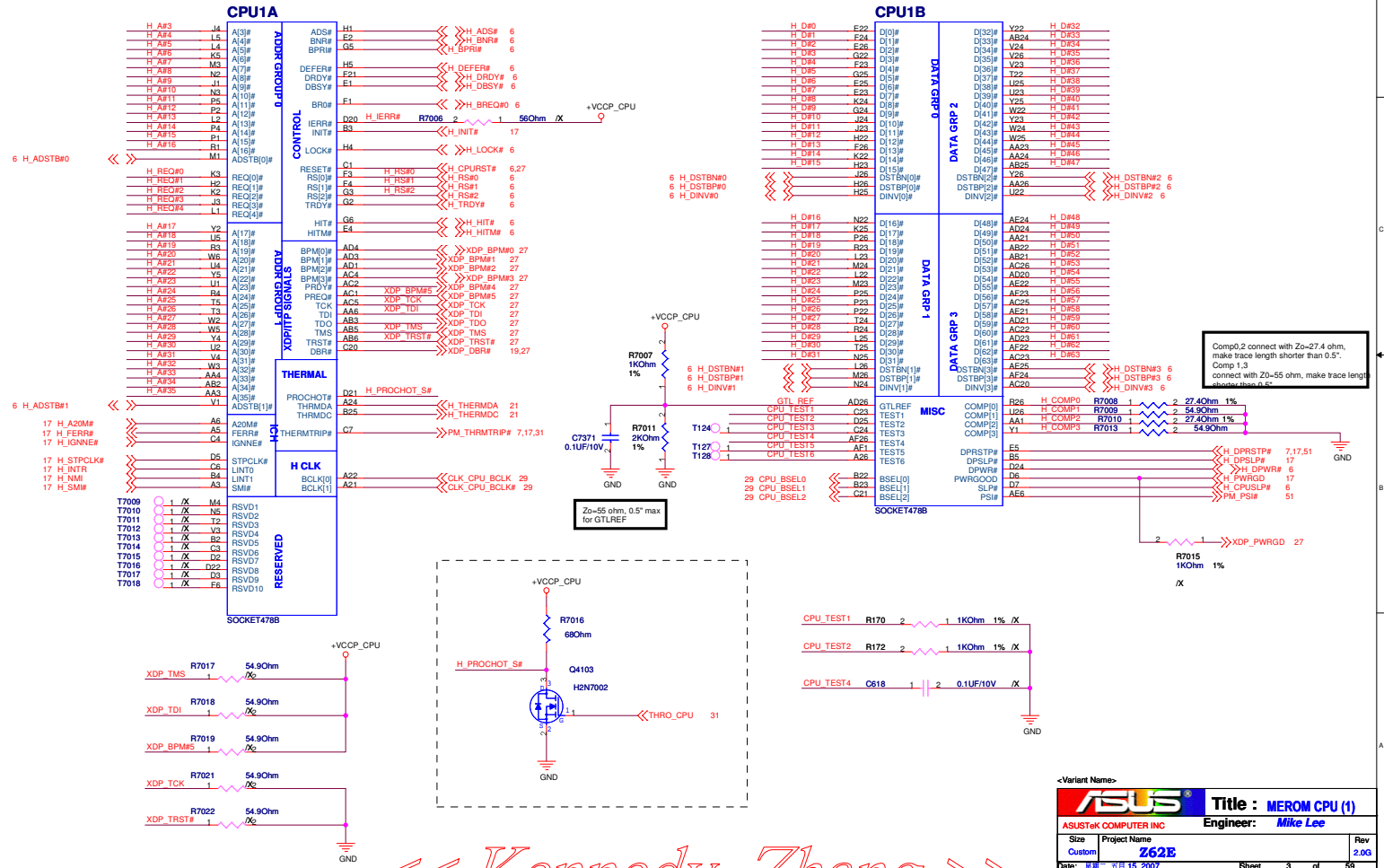


Title : System Setting
Engineer: Mike Lee

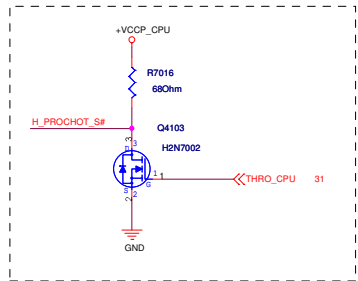
Site	Project Name	Rev
Custom	762E	2.00
Date: 05/15/2007	Sheet: 2	of 58

« Kennedy_Zhang »

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H_AR#(35:3) << H_AR#(35:3)
H_REQ#(4:0) << H_REQ#(4:0)

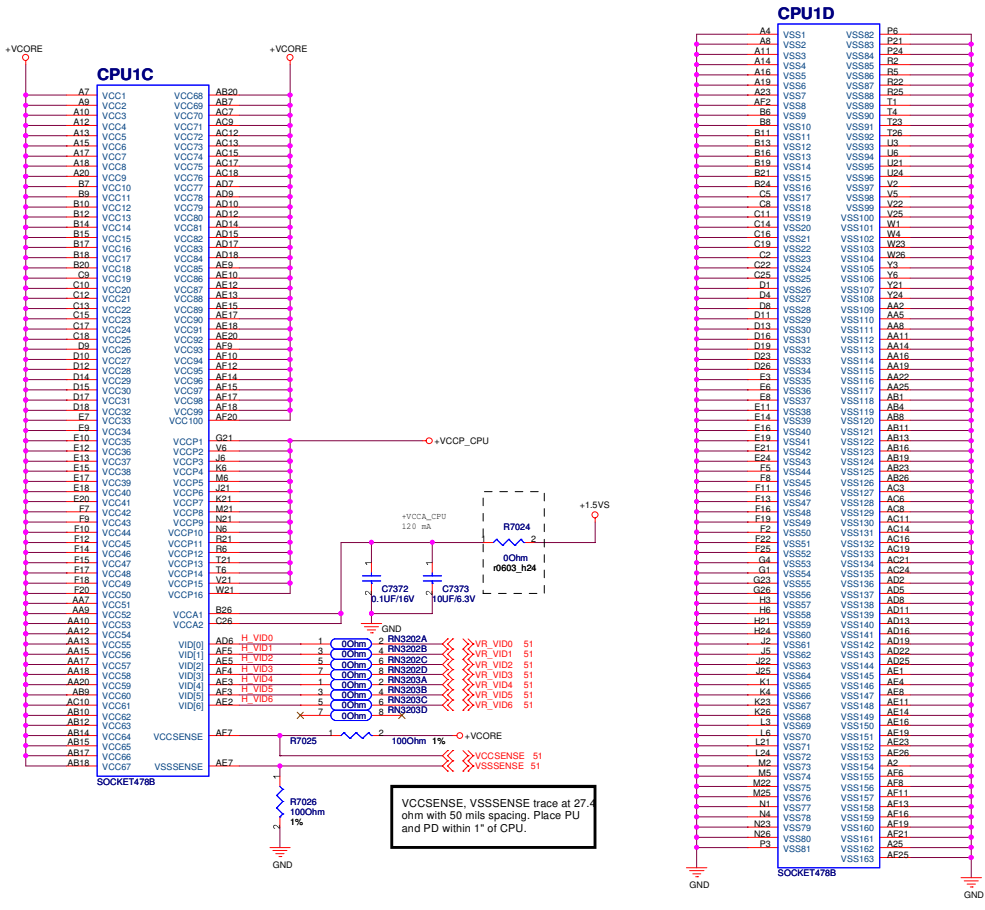


Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp 1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".



ASUS Title: MEROM CPU (1)
ASUSTek COMPUTER INC Engineer: Mike Lee
Size: Project Name: Z62E Rev: 2.00
Date: 08-11-15-2007 Sheet: 3 of 59

<< Kennedy_Zhang >>

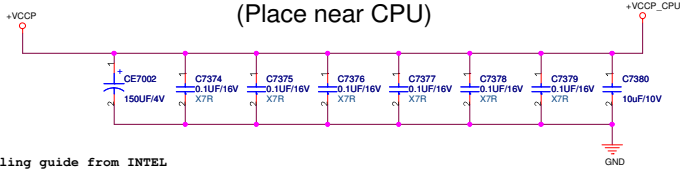


<-Variant Name->

ASUS		Title : MEROM CPU (2)
ASUSTek COMPUTER INC		Engineer: Mike Lee
Size	Project Name	Rev
Custom	Z62E	2.00
Date: 08-11-2007	Sheet 4 of 59	

<< Kennedy_Zhang >>

+VCCP Decoupling Capacitor (Place near CPU)



Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

« Kennedy_Zhang »

ASUS		Title :CPU CAP and HOLES	
ASUSTek COMPUTER INC. NB1		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	Z62E	2.00	
Date: 08-11-15-2007		Sheet 5	of 59

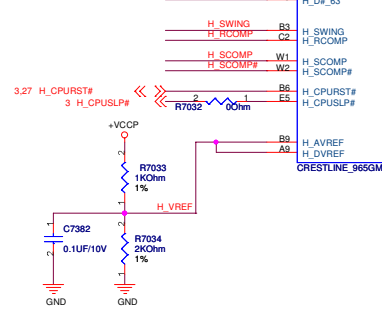
U4103A

H_D#0	E4	H_D# 0	H_A# 3	M13	H_A#3
H_D#1	G2	H_D# 1	H_A# 4	B11	H_A#4
H_D#2	G7	H_D# 2	H_A# 5	C11	H_A#5
H_D#3	M6	H_D# 3	H_A# 6	M11	H_A#6
H_D#4	H7	H_D# 4	H_A# 7	F18	H_A#7
H_D#5	G4	H_D# 5	H_A# 8	L13	H_A#8
H_D#6	H3	H_D# 6	H_A# 9	C12	H_A#9
H_D#7	F3	H_D# 7	H_A# 10	C14	H_A#10
H_D#8	N8	H_D# 8	H_A# 11	B16	H_A#11
H_D#9	N5	H_D# 9	H_A# 12	K18	H_A#12
H_D#10	M10	H_D# 10	H_A# 13	B13	H_A#13
H_D#11	N12	H_D# 11	H_A# 14	L16	H_A#14
H_D#12	N9	H_D# 12	H_A# 15	M17	H_A#15
H_D#13	H5	H_D# 13	H_A# 16	B14	H_A#16
H_D#14	E13	H_D# 14	H_A# 17	K19	H_A#17
H_D#15	K9	H_D# 15	H_A# 18	E15	H_A#18
H_D#16	M2	H_D# 16	H_A# 19	R17	H_A#19
H_D#17	Y8	H_D# 17	H_A# 20	B16	H_A#20
H_D#18	W10	H_D# 18	H_A# 21	S20	H_A#21
H_D#19	W4	H_D# 19	H_A# 22	L19	H_A#22
H_D#20	M4	H_D# 20	H_A# 23	D17	H_A#23
H_D#21	J1	H_D# 21	H_A# 24	M17	H_A#24
H_D#22	N4	H_D# 22	H_A# 25	M16	H_A#25
H_D#23	N3	H_D# 23	H_A# 26	B18	H_A#26
H_D#24	W5	H_D# 24	H_A# 27	E19	H_A#27
H_D#25	W8	H_D# 25	H_A# 28	B17	H_A#28
H_D#26	N2	H_D# 26	H_A# 29	B15	H_A#29
H_D#27	Y3	H_D# 27	H_A# 30	C18	H_A#30
H_D#28	Y9	H_D# 28	H_A# 31	E17	H_A#31
H_D#29	W4	H_D# 29	H_A# 32	A19	H_A#32
H_D#30	W3	H_D# 30	H_A# 33	B19	H_A#33
H_D#31	N4	H_D# 31	H_A# 34	M19	H_A#34
H_D#32	AD12	H_D# 32	H_A# 35		
H_D#33	AE3	H_D# 33			
H_D#34	AD9	H_D# 34			
H_D#35	AC9	H_D# 35			
H_D#36	AC7	H_D# 36			
H_D#37	AC14	H_D# 37			
H_D#38	AD11	H_D# 38			
H_D#39	AC11	H_D# 39			
H_D#40	AB2	H_D# 40			
H_D#41	AD7	H_D# 41			
H_D#42	AB1	H_D# 42			
H_D#43	Y3	H_D# 43			
H_D#44	AC9	H_D# 44			
H_D#45	AE2	H_D# 45			
H_D#46	ACS	H_D# 46			
H_D#47	AJ9	H_D# 47			
H_D#48	AJ4	H_D# 48			
H_D#49	AH9	H_D# 49			
H_D#50	AH4	H_D# 50			
H_D#51	AEB	H_D# 51			
H_D#52	AH12	H_D# 52			
H_D#53	AJ5	H_D# 53			
H_D#54	AJ5	H_D# 54			
H_D#55	AJ6	H_D# 55			
H_D#56	AJ6	H_D# 56			
H_D#57	AE7	H_D# 57			
H_D#58	AJ7	H_D# 58			
H_D#59	AJ2	H_D# 59			
H_D#60	AES	H_D# 60			
H_D#61	AJ9	H_D# 61			
H_D#62	AH2	H_D# 62			
H_D#63	AH13	H_D# 63			

HOST

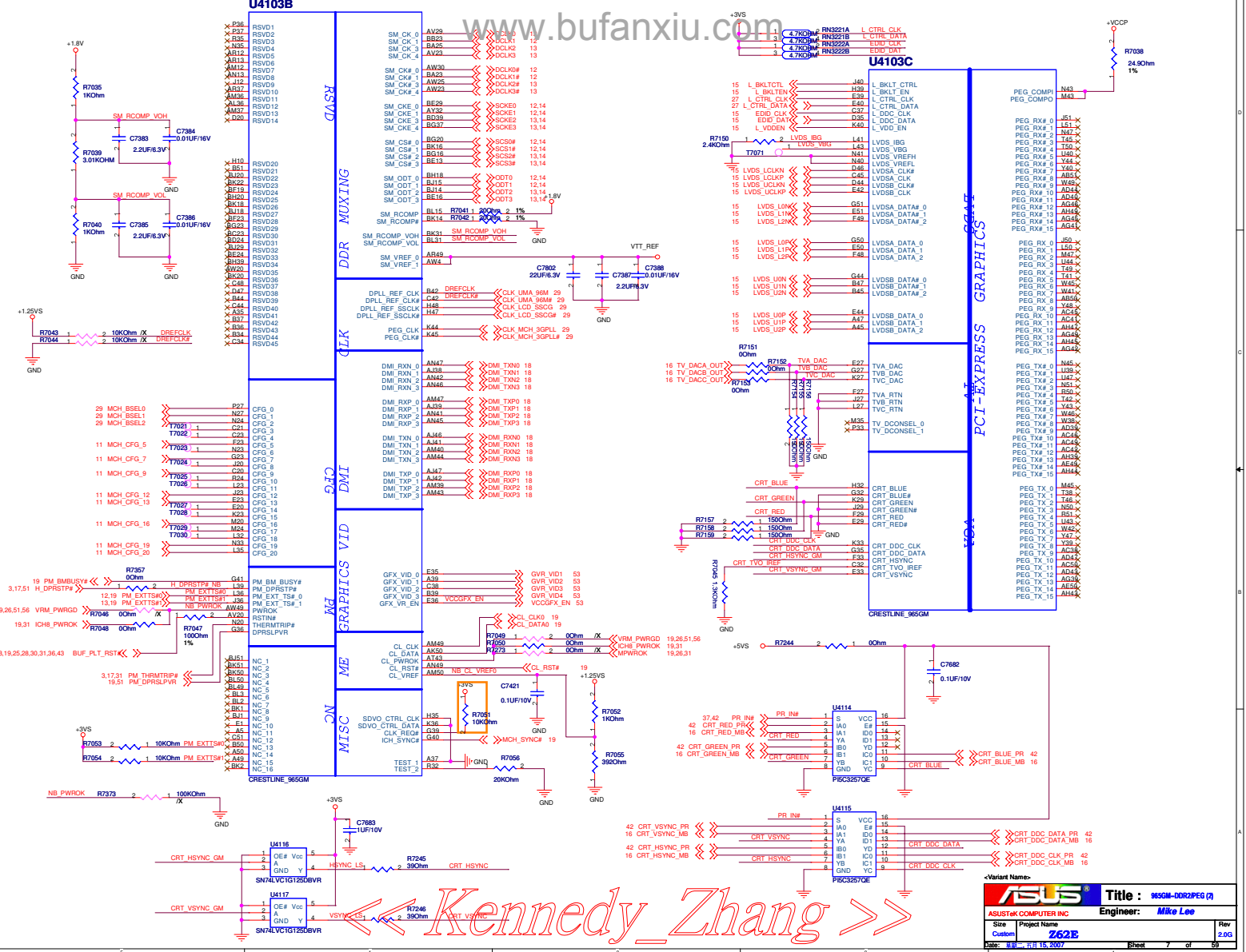
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H_DIN#_0 K5 <<> H_DIN#0 3
 H_DIN#_1 L2 <<> H_DIN#1 3
 H_DIN#_2 AD13 <<> H_DIN#2 3
 H_DIN#_3 AE13 <<> H_DIN#3 3
 H_DSTBN#_0 M7 <<> H_DSTBN#0 3
 H_DSTBN#_1 K3 <<> H_DSTBN#1 3
 H_DSTBN#_2 AC2 <<> H_DSTBN#2 3
 H_DSTBN#_3 AH11 <<> H_DSTBN#3 3
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 H_DSTBP#_1 K2 <<> H_DSTBP#1 3
 H_DSTBP#_2 AC2 <<> H_DSTBP#2 3
 H_DSTBP#_3 AJ10 <<> H_DSTBP#3 3
 H_REQ#_0 M14 H_REQ#0
 H_REQ#_1 A11 H_REQ#1
 H_REQ#_2 M13 H_REQ#2
 H_REQ#_3 B12 H_REQ#3
 H_RS#_0 E12 H_RS#0
 H_RS#_1 D7 H_RS#1
 H_RS#_2 D8 H_RS#2



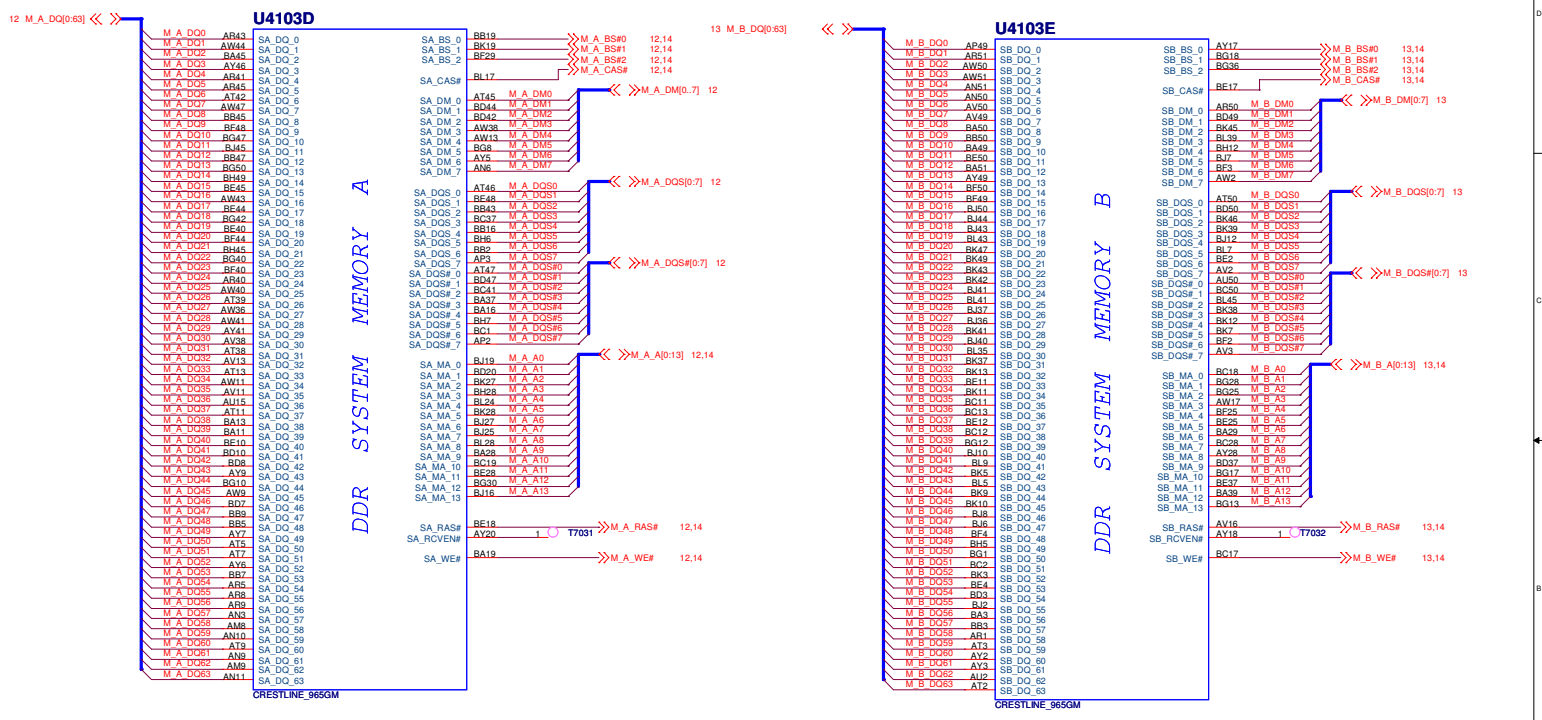
<-Variant Name-
ASUS Title : 965GM - CPU (1)
 ASUSTek COMPUTER INC Engineer: Mike Lee
 Size Project Name
 Custom Z62E
 Date: 08-11-15-2007 Sheet 6 of 59

<< Kennedy_Zhang >>



Kennedy_Zhang

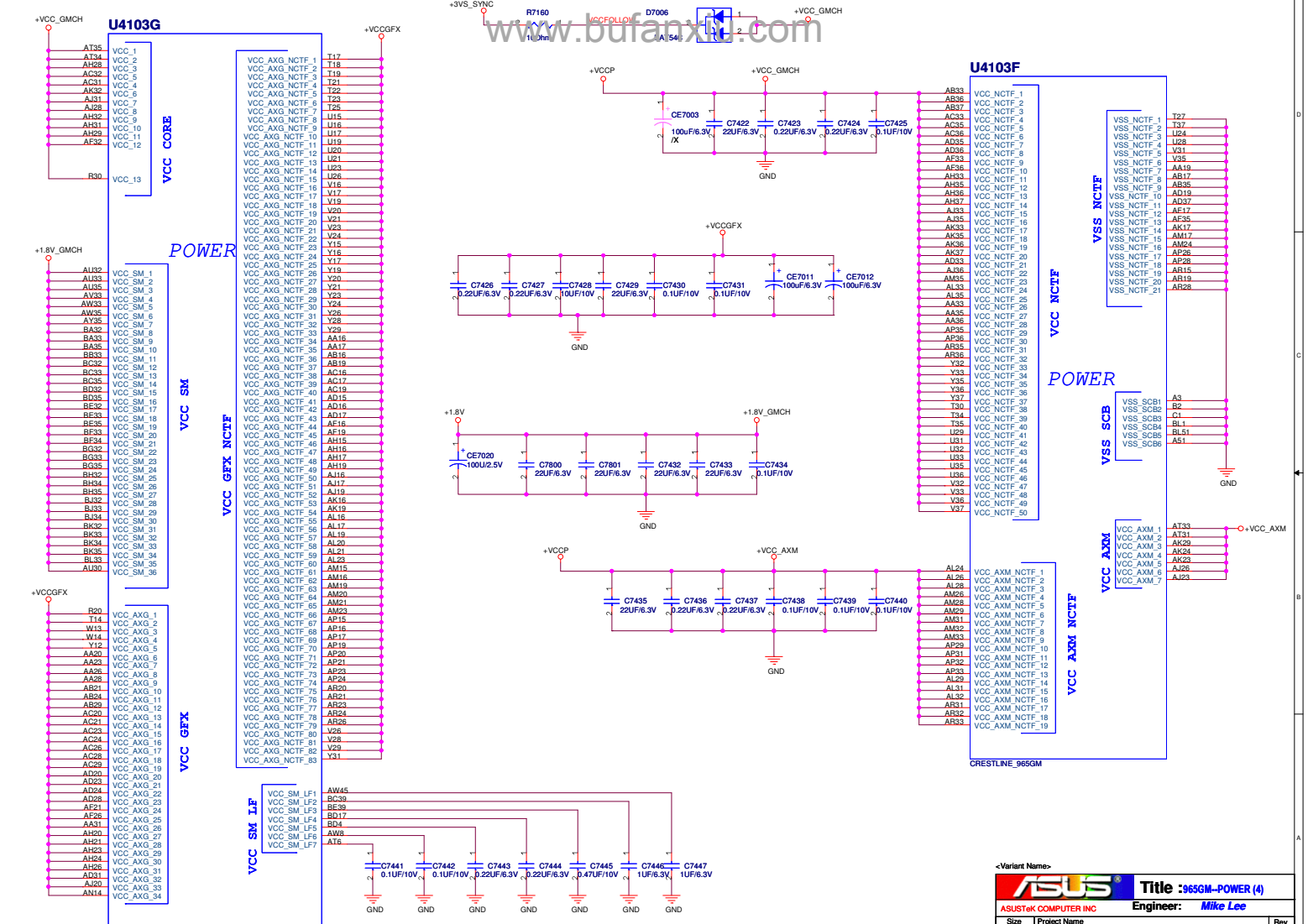
ASUS Title: 965GM-DR2PEG (R)
 ASUSTek COMPUTER INC Engineer: Mike Lee
 Size: Project Name
 Custom: 262E
 Date: 11/15/2007 Sheet: 7 of 98



-Variant Name-

ASUS		Title : 965GM-DDR2 bus (3)	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	
06/09	Z62E	2.00	
Date: 06-11-15, 2007	Sheet	8	of 59

<< Kennedy_Zhang >>

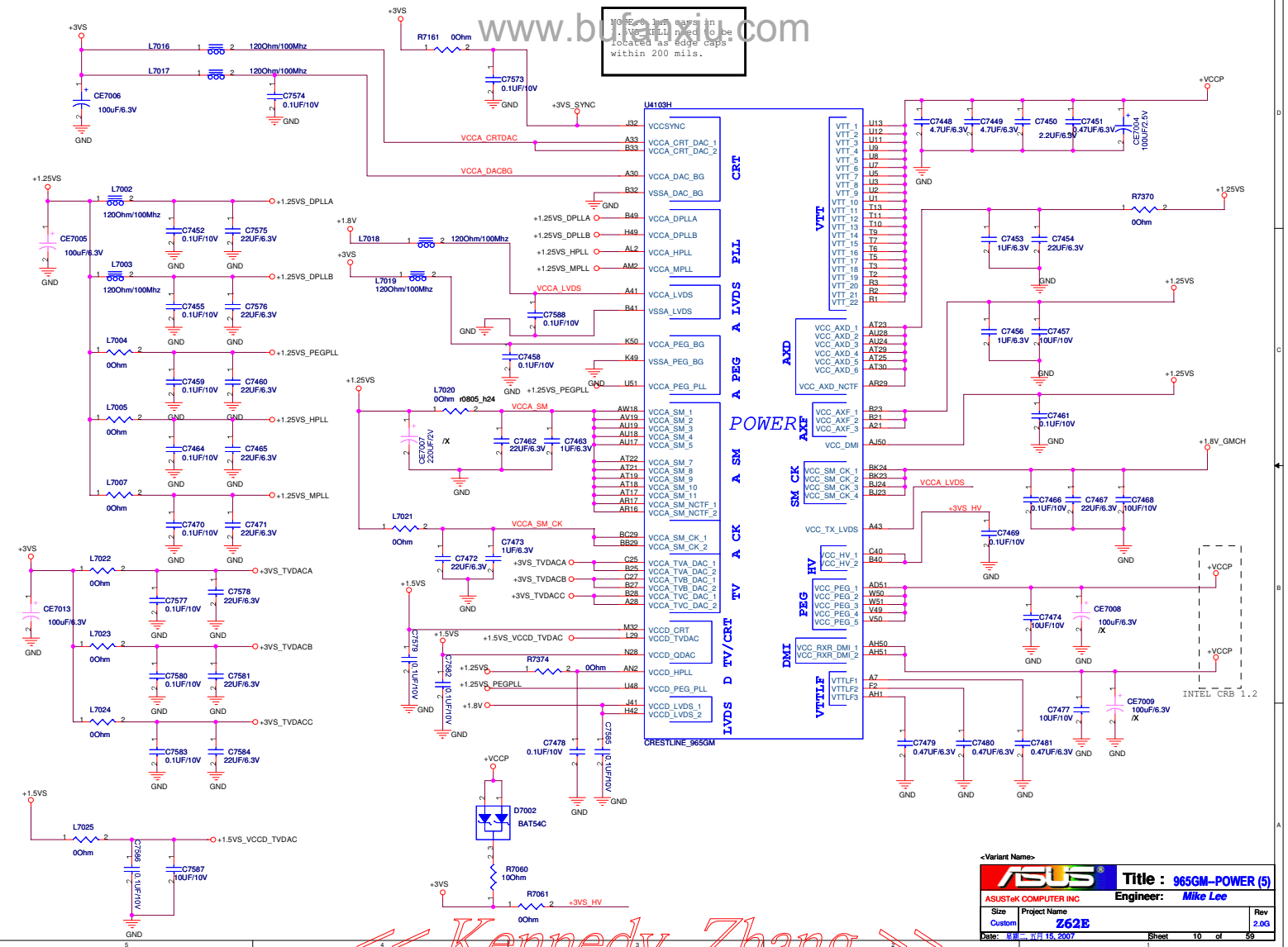


<Variant Name>

ASUS		Title : 965GM-POWER (4)	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name		Rev
Custom	Z62E		2.0G
Date: 2007.08.15	Sheet	9	of 59

<< Kennedy_Zhang >>

Note: All components should be located as edge caps within 200 mils.



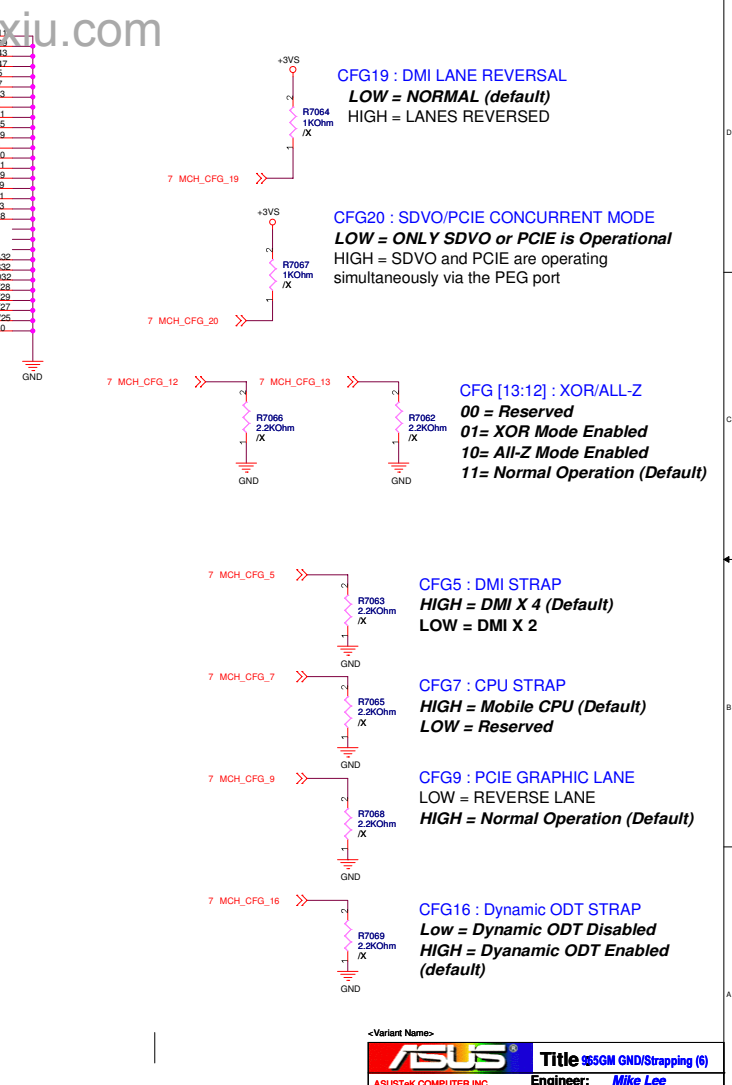
« Kennedy_Zhang »

HIGH LANES REVERSED

ASUS Title : 965GM-POWER (5)
 ASUSTek COMPUTER INC Engineer: Mike Lee
 Size Project Name
 Cus06M Z62E
 Date: 08-11-15-2007 Sheet 10 of 59

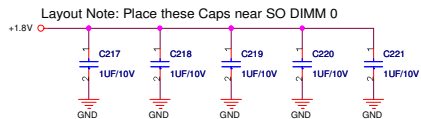
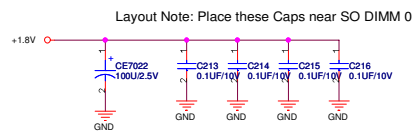
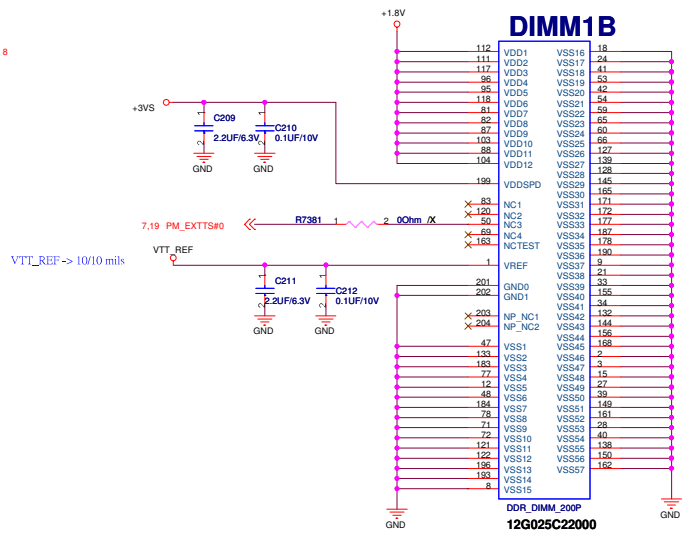
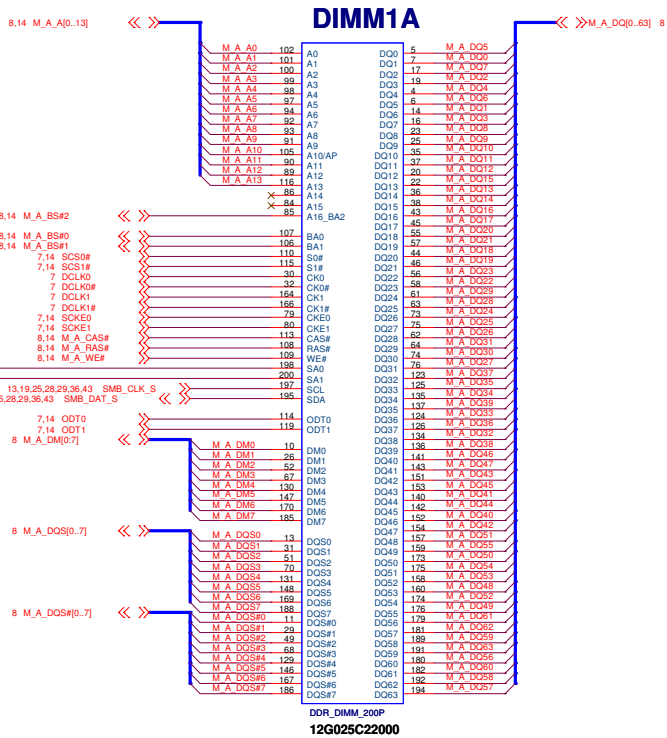
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A15	VSS_2	AW29
A17	VSS_3	AW32
AA21	VSS_4	AW5
AA24	VSS_5	AW7
AA29	VSS_6	AY10
AA30	VSS_7	AY24
AA32	VSS_8	AY27
AA33	VSS_9	AY42
AA38	VSS_10	AY46
AA31	VSS_11	AY47
AA310	VSS_12	AY50
AA313	VSS_13	B10
AA314	VSS_14	B20
AA315	VSS_15	B24
AA316	VSS_16	B29
AA317	VSS_17	B30
AA318	VSS_18	B32
AA319	VSS_19	B38
AA320	VSS_20	B41
AA321	VSS_21	B46
AA322	VSS_22	B5
AA323	VSS_23	B8
AA324	VSS_24	BA17
AA325	VSS_25	BA18
AA326	VSS_26	BA2
AA327	VSS_27	BA24
AA328	VSS_28	BA25
AA329	VSS_29	BA28
AA330	VSS_30	BB12
AA331	VSS_31	BB25
AA332	VSS_32	BB44
AA333	VSS_33	BB49
AA334	VSS_34	BC16
AA335	VSS_35	BC24
AA336	VSS_36	BC25
AA337	VSS_37	BC36
AA338	VSS_38	BC40
AA339	VSS_39	BC41
AA340	VSS_40	BC42
AA341	VSS_41	BD13
AA342	VSS_42	BD2
AA343	VSS_43	BD28
AA344	VSS_44	BD45
AA345	VSS_45	BD5
AA346	VSS_46	BD5
AA347	VSS_47	BE1
AA348	VSS_48	BE19
AA349	VSS_49	BE23
AA350	VSS_50	BE30
AA351	VSS_51	BE42
AA352	VSS_52	BE51
AA353	VSS_53	BE8
AA354	VSS_54	BE12
AA355	VSS_55	BE16
AA356	VSS_56	BE28
AA357	VSS_57	BG19
AA358	VSS_58	BG2
AA359	VSS_59	BG24
AA360	VSS_60	BG29
AA361	VSS_61	BG39
AA362	VSS_62	BG48
AA363	VSS_63	BG5
AA364	VSS_64	BH1
AA365	VSS_65	BH17
AA366	VSS_66	BH30
AA367	VSS_67	BH44
AA368	VSS_68	BH46
AA369	VSS_69	BH9
AA370	VSS_70	BJ11
AA371	VSS_71	BJ13
AA372	VSS_72	BK38
AA373	VSS_73	BK4
AA374	VSS_74	BK42
AA375	VSS_75	BK46
AA376	VSS_76	BK15
AA377	VSS_77	BK17
AA378	VSS_78	BK25
AA379	VSS_79	BK29
AA380	VSS_80	BK36
AA381	VSS_81	BK40
AA382	VSS_82	BK44
AA383	VSS_83	BK6
AA384	VSS_84	BK8
AA385	VSS_85	BL11
AA386	VSS_86	BL13
AA387	VSS_87	BL19
AA388	VSS_88	BL22
AA389	VSS_89	BL37
AA390	VSS_90	BL47
AA391	VSS_91	BL47
AA392	VSS_92	C16
AA393	VSS_93	C19
AA394	VSS_94	C28
AA395	VSS_95	C29
AA396	VSS_96	C33
AA397	VSS_97	C36
AA398	VSS_98	C38
AA399	VSS_99	C41

U4103J		
AA32	VSS_288	W29
AA33	VSS_289	W43
AA34	VSS_290	W47
AA35	VSS_291	W5
AA36	VSS_292	W7
AA37	VSS_293	Y13
AA38	VSS_294	Y2
AA39	VSS_295	Y41
AA40	VSS_296	Y45
AA41	VSS_297	Y49
AA42	VSS_298	Y5
AA43	VSS_299	Y50
AA44	VSS_300	Y11
AA45	VSS_301	Y29
AA46	VSS_302	Y31
AA47	VSS_303	Y33
AA48	VSS_304	Y38
AA49	VSS_305	Y42
AA50	VSS_306	AA32
AA51	VSS_307	AB32
AA52	VSS_308	AD32
AA53	VSS_309	AF28
AA54	VSS_310	AF29
AA55	VSS_311	AI21
AA56	VSS_312	AV25
AA57	VSS_313	H50
AA58	VSS_314	AA32
AA59	VSS_315	AA32
AA60	VSS_316	AA32
AA61	VSS_317	AA32
AA62	VSS_318	AA32
AA63	VSS_319	AA32
AA64	VSS_320	AA32
AA65	VSS_321	AA32
AA66	VSS_322	AA32
AA67	VSS_323	AA32
AA68	VSS_324	AA32
AA69	VSS_325	AA32
AA70	VSS_326	AA32
AA71	VSS_327	AA32
AA72	VSS_328	AA32
AA73	VSS_329	AA32
AA74	VSS_330	AA32
AA75	VSS_331	AA32
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AA77	VSS_333	AA32
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AA105	VSS_361	AA32
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AA107	VSS_363	AA32
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AA110	VSS_366	AA32
AA111	VSS_367	AA32
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AA126	VSS_382	AA32
AA127	VSS_383	AA32
AA128	VSS_384	AA32
AA129	VSS_385	AA32
AA130	VSS_386	AA32
AA131	VSS_387	AA32
AA132	VSS_388	AA32
AA133	VSS_389	AA32
AA134	VSS_390	AA32
AA135	VSS_391	AA32
AA136	VSS_392	AA32
AA137	VSS_393	AA32
AA138	VSS_394	AA32
AA139	VSS_395	AA32
AA140	VSS_396	AA32
AA141	VSS_397	AA32
AA142	VSS_398	AA32
AA143	VSS_399	AA32



ASUS		Title: 965GM GND/Strapping (6)	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name		Rev
Custom	Z62E		2.00
Date: 8/8/2007	11/15/2007	Sheet	11 of 59

« Kennedy_Zhang »



<-Variant Name->

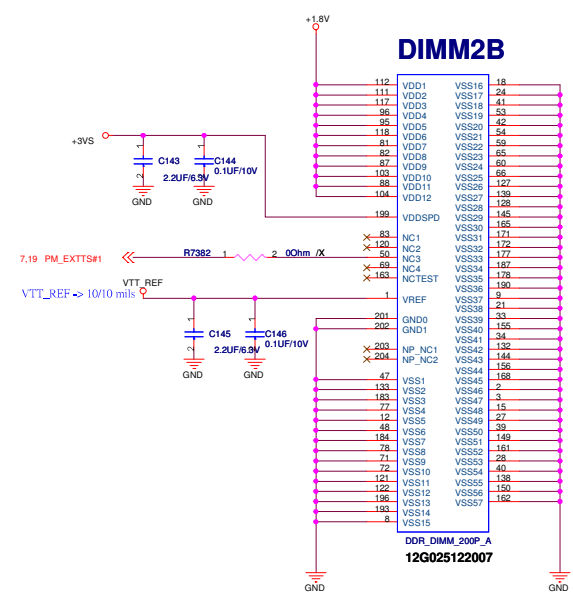
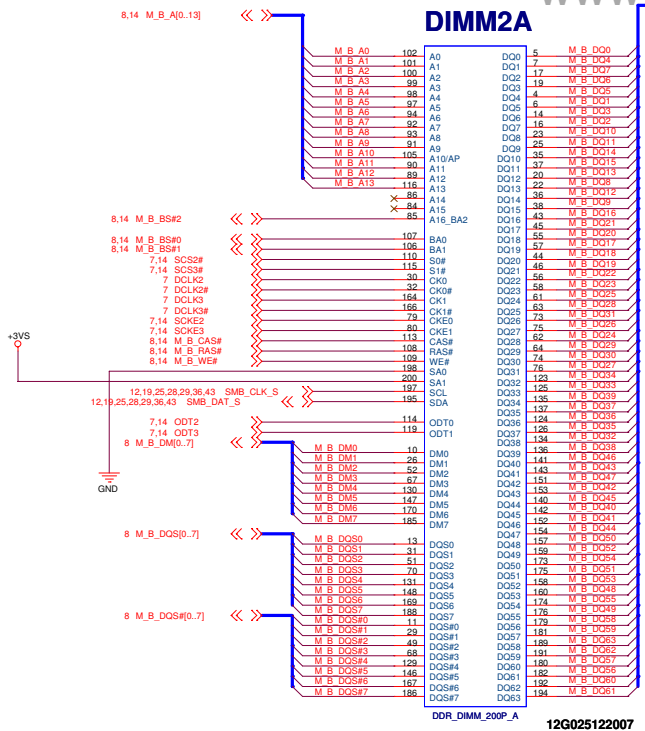
ASUS Title : DDR2 SO-DIMM(0)

ASUSTek COMPUTER INC Engineer: Mike Lee

Size Project Name
Custom Z62E

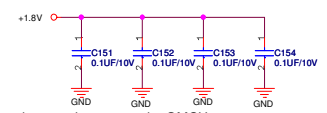
Date: 11/15/2007 Sheet 12 of 59

<< Kennedy_Zhang >>

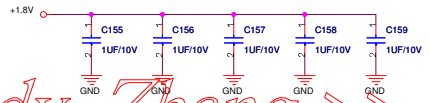


Layout Note: Place these Caps near SO DIMM 1

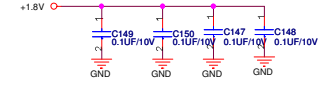
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these resistors near the GMCH



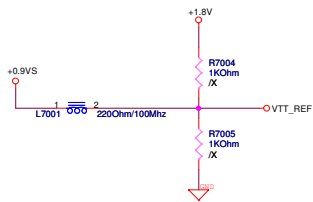
Layout Note: Place these Caps near SO DIMM 1



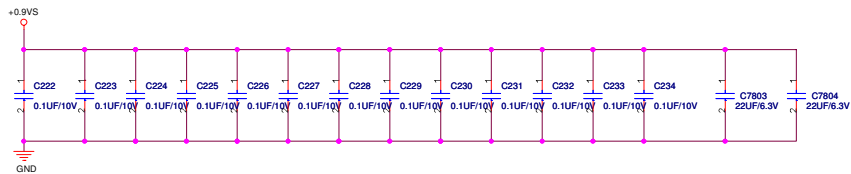
ASUS Title : **DDR2 SO-DIMM(1)**
 ASUSTek COMPUTER INC Engineer: **Mike Lee**

Size	Project Name	Rev
Customer	Z62E	2.00
Date: 8/8/2007	Sheet 13 of 59	

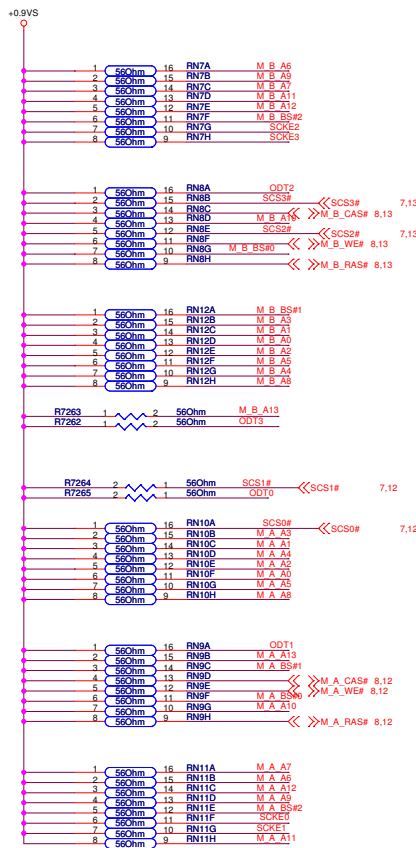
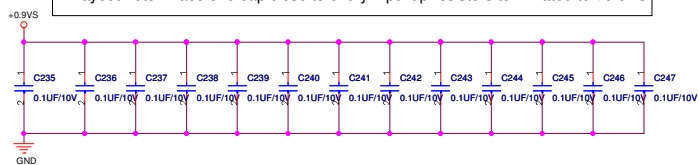
« Kennedy_Zhang »



- >> M_A_A[0..13] 8,12
- >> M_A_BS[0..2] 8,12
- >> M_B_A[0..13] 8,13
- >> M_B_BS[0..2] 8,13
- << SCKE[0:3] 7,12,13
- << ODT[0:3] 7,12,13



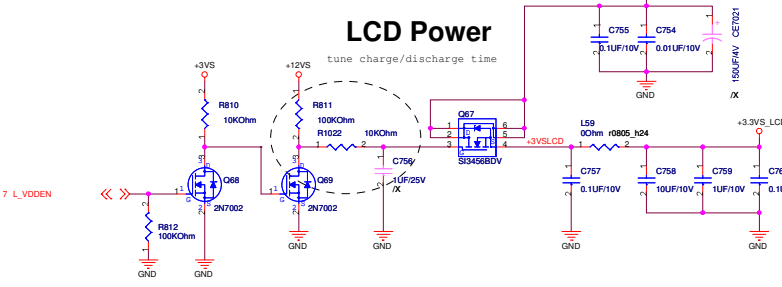
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



ASUS		Title : DDR2 TERM	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	
Customer	Z62E	2.00	
Date: 08-11-15-2007		Sheet	14 of 59

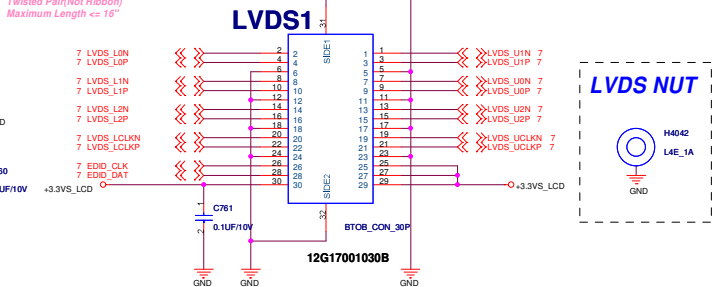
<< Kennedy_Zhang >>

LCD Backlight Control



Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

LCD LVDS Interface



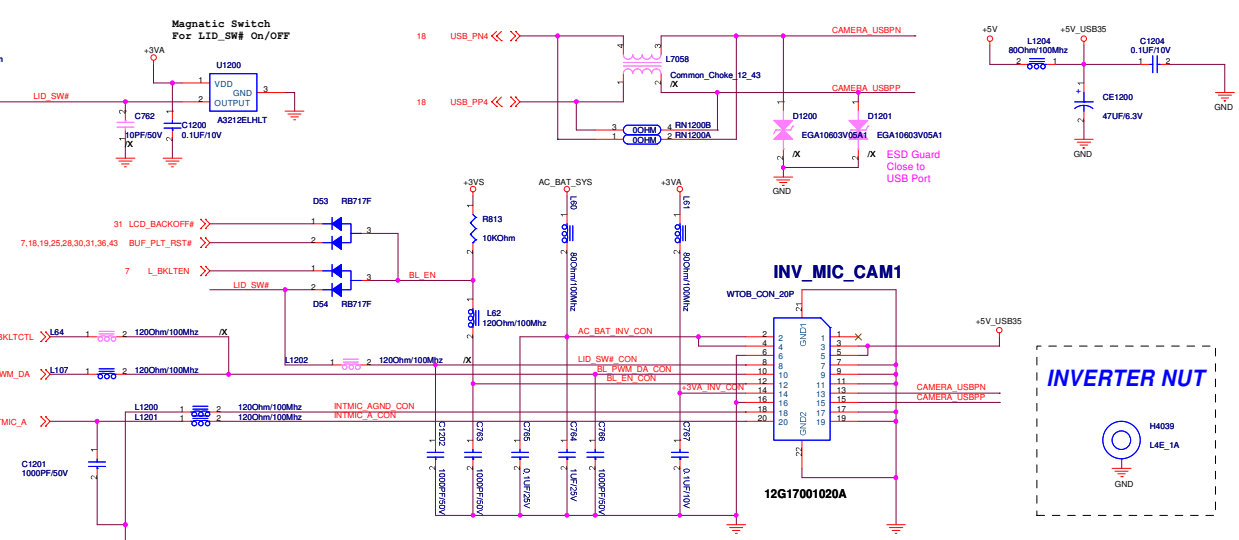
LVDS NUT



INVERTER Interface

BIOS
 LCD_BACKOFF#: When user push
 "Fn+F7" button, BIOS active this
 pin to turn off back light.

BIOS
 BACK_ADJ: KBC
 output PWM
 signal (adjust
 pulse width)
 to adjust Back
 light.



INVERTER NUT



Inverter Board built in 14.1W LCD Panel

(Min: 3 mA Arms) 6
 mA Arms (Max: 6.5
 mA Arms)

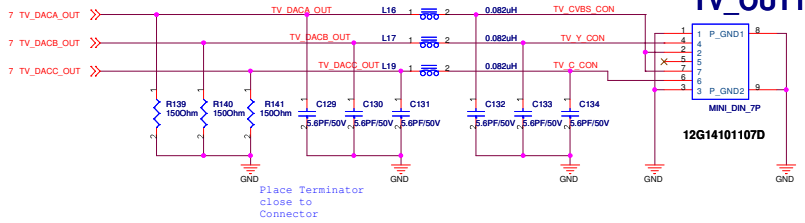
ASUS		Title : LVDS & INVERTER	
ASUSTEK COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	262E	2.00	
Date: 08. 05.15.2007	Sheet		15 of 58

<< Kennedy_Zhang >>

TV OUT

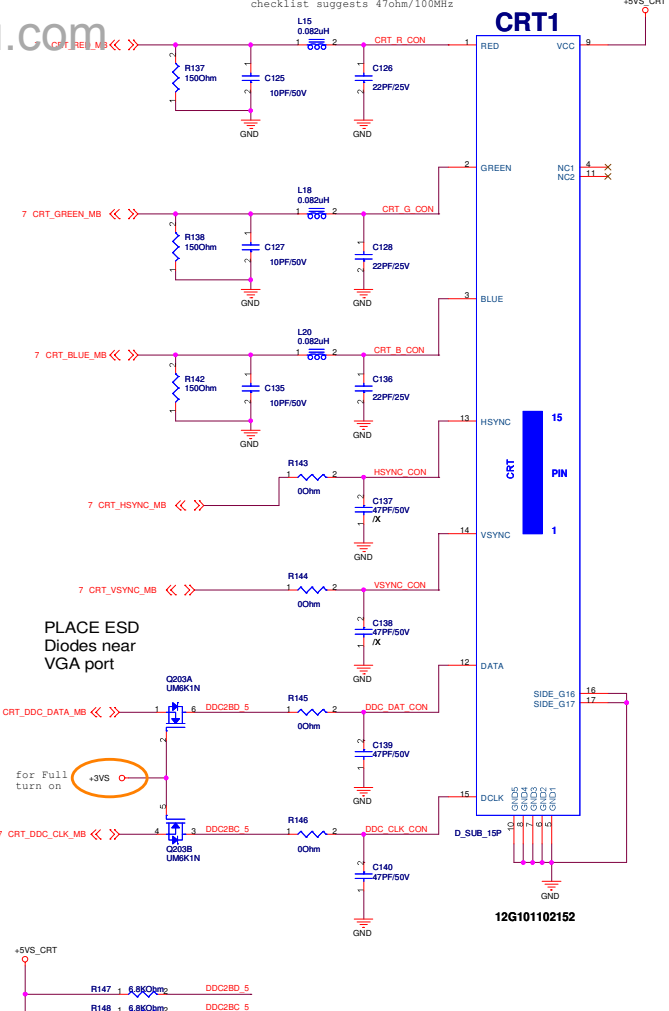
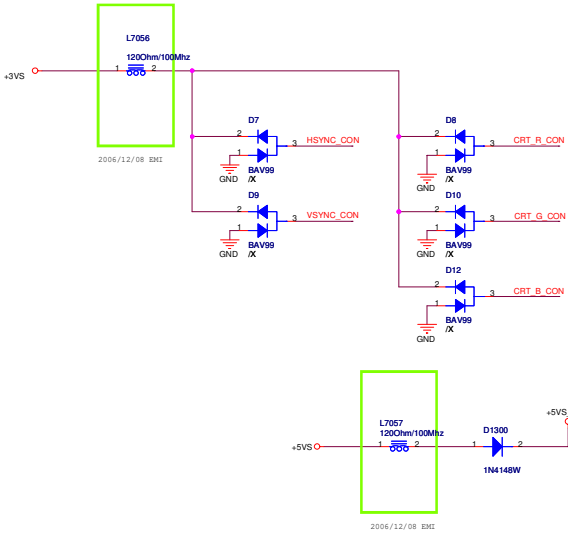
checklist suggests
150ohm/100MHz &
6pF

checklist suggests 47ohm/100MHz



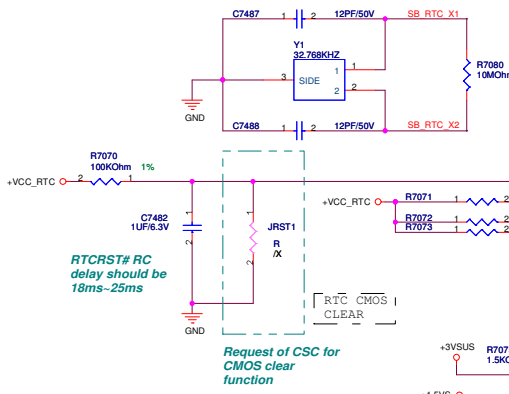
TV_OUT1

CRT OUT



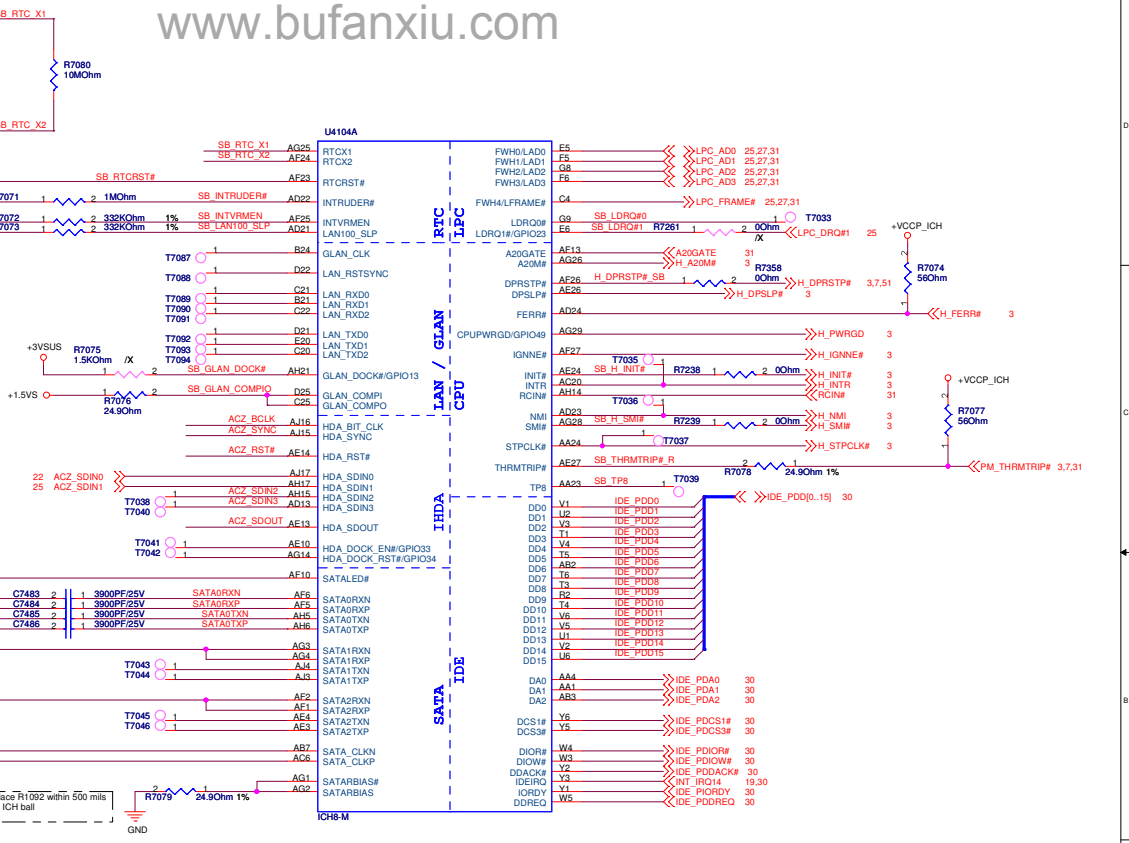
ASUS		Title : CRT & TV OUT	
ASUSTEK COMPUTER INC		Engineer: Mike Lee	
Site	Project Name	Rev	
Custom	262E	2.00	
Date: 08_15_2007	Sheet: 16	of	58

« Kennedy_Zhang »

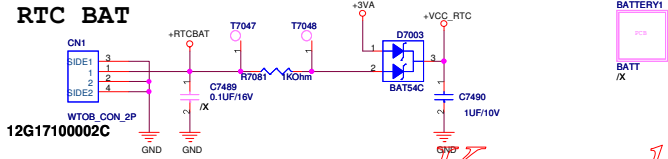


- 22 ACZ_BCLK_AUD <<> 1 330OHM 2 RN3225A ACZ_BCLK
- 25 ACZ_BCLK_MDC <<> 3 330OHM 4 RN3225B ACZ_BCLK
- 22 ACZ_SYNC_AUD <<> 1 330OHM 2 RN3225A ACZ_SYNC
- 25 ACZ_SYNC_MDC <<> 3 330OHM 4 RN3225B ACZ_SYNC
- 22.23 ACZ_RST#_AUD <<> 1 330OHM 2 RN3227A ACZ_RST#
- 25 ACZ_RST#_MDC <<> 3 330OHM 4 RN3227B ACZ_RST#
- 22 ACZ_SDOUT_AUD <<> 1 330OHM 2 RN3228A ACZ_SDOUT
- 25 ACZ_SDOUT_MDC <<> 3 330OHM 4 RN3228B ACZ_SDOUT

SATA:
Distance between the ICH7 and cap on the "P" signal should be identical
distance between the ICH7 and cap on the "N" signal for same pair.

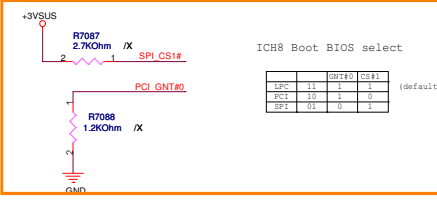
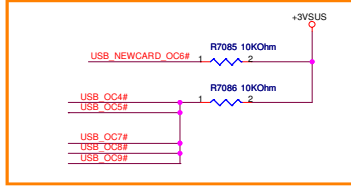
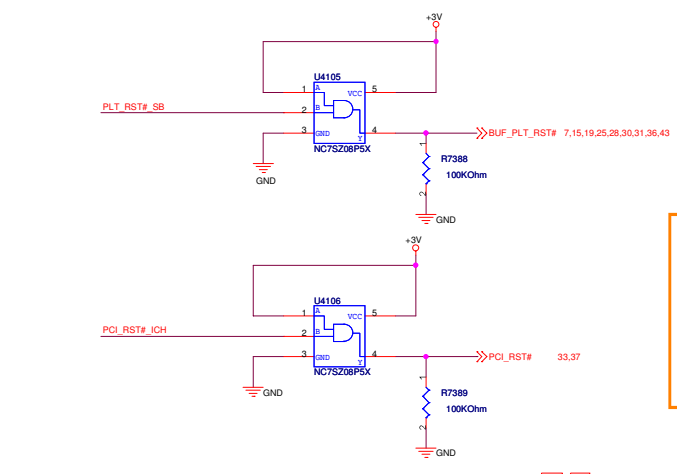
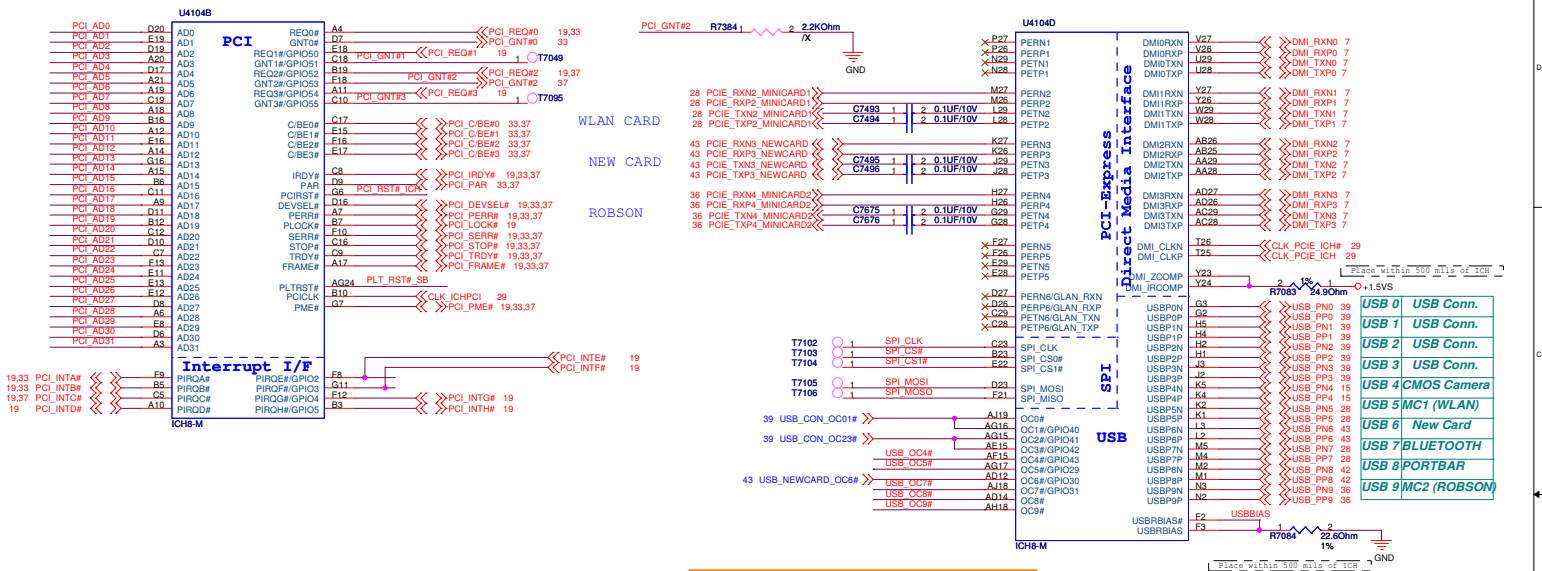


SATA if it non-used,
1)SATA[0:3]RXpN SATABIAS, SATABIAS# and SATA_CLKpN should be PD.
2)SATA[0:3]TXpN and SATALED# NO connect.



ASUS		Title : ICH8-M (1)	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	2.00
Custom	Z62E		
Date: 7/11/2007		Sheet	17 of 59

« Kennedy Zhang »



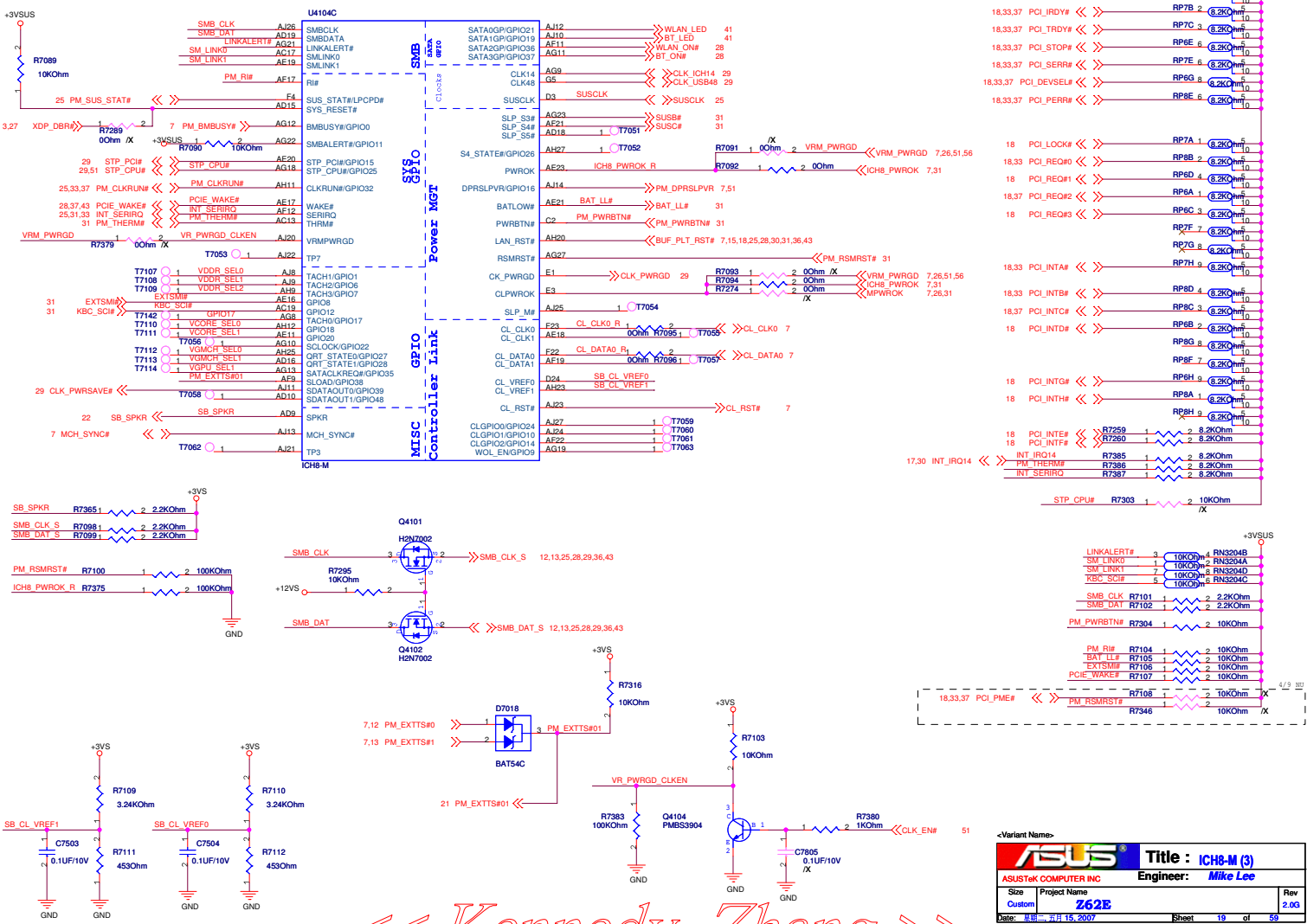
ASUS Title : ICH8-M (1)

ASUSTek COMPUTER INC Engineer: Mike Lee

Size Project Name: Z62E

Date: 8/15/2007 Sheet 18 of 59

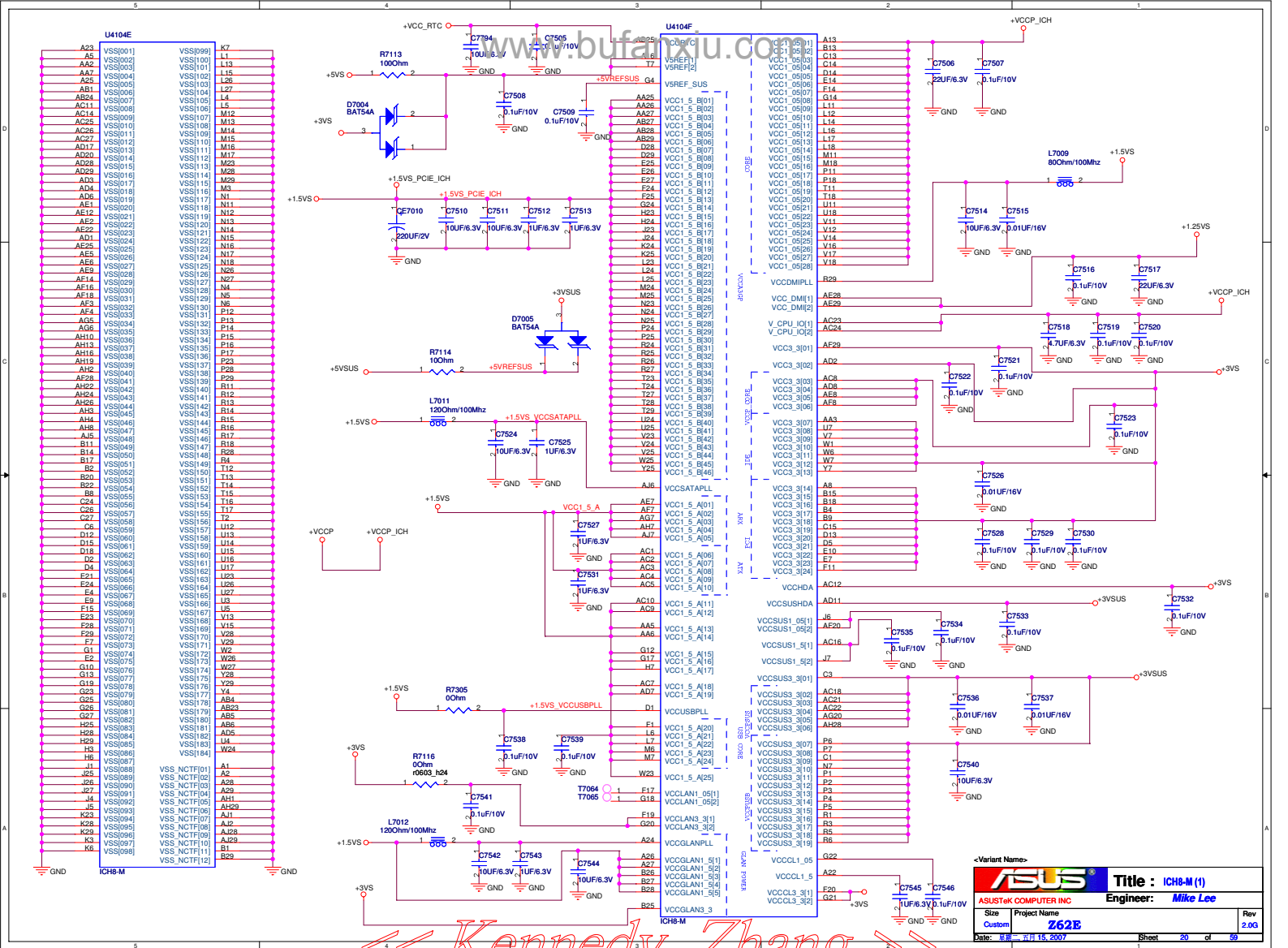
<< Kennedy_Zhang >>



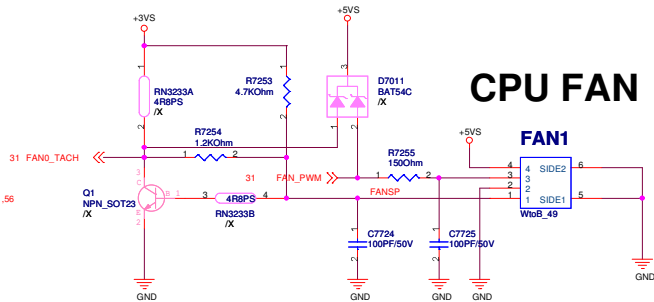
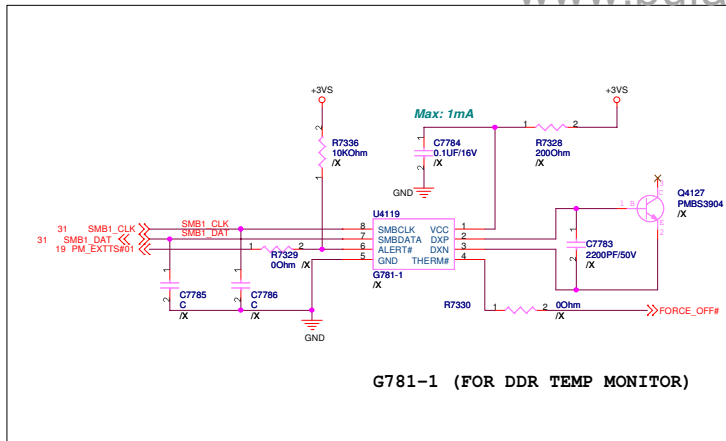
<Variant Name>

ASUS		Title : ICH8-M (3)
ASUSTeK COMPUTER INC		Engineer: Mike Lee
Size	Project Name	Rev
Custom	262E	2.00
Date: 2007.03.15		Sheet 19 of 59

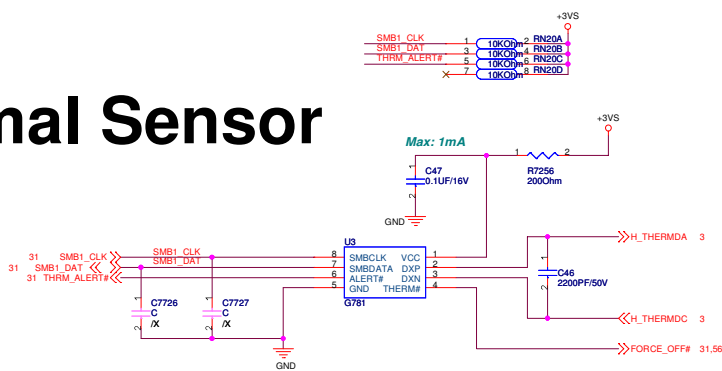
« Kennedy_Zhang »



« Kennedy_Zhang »



Thermal Sensor



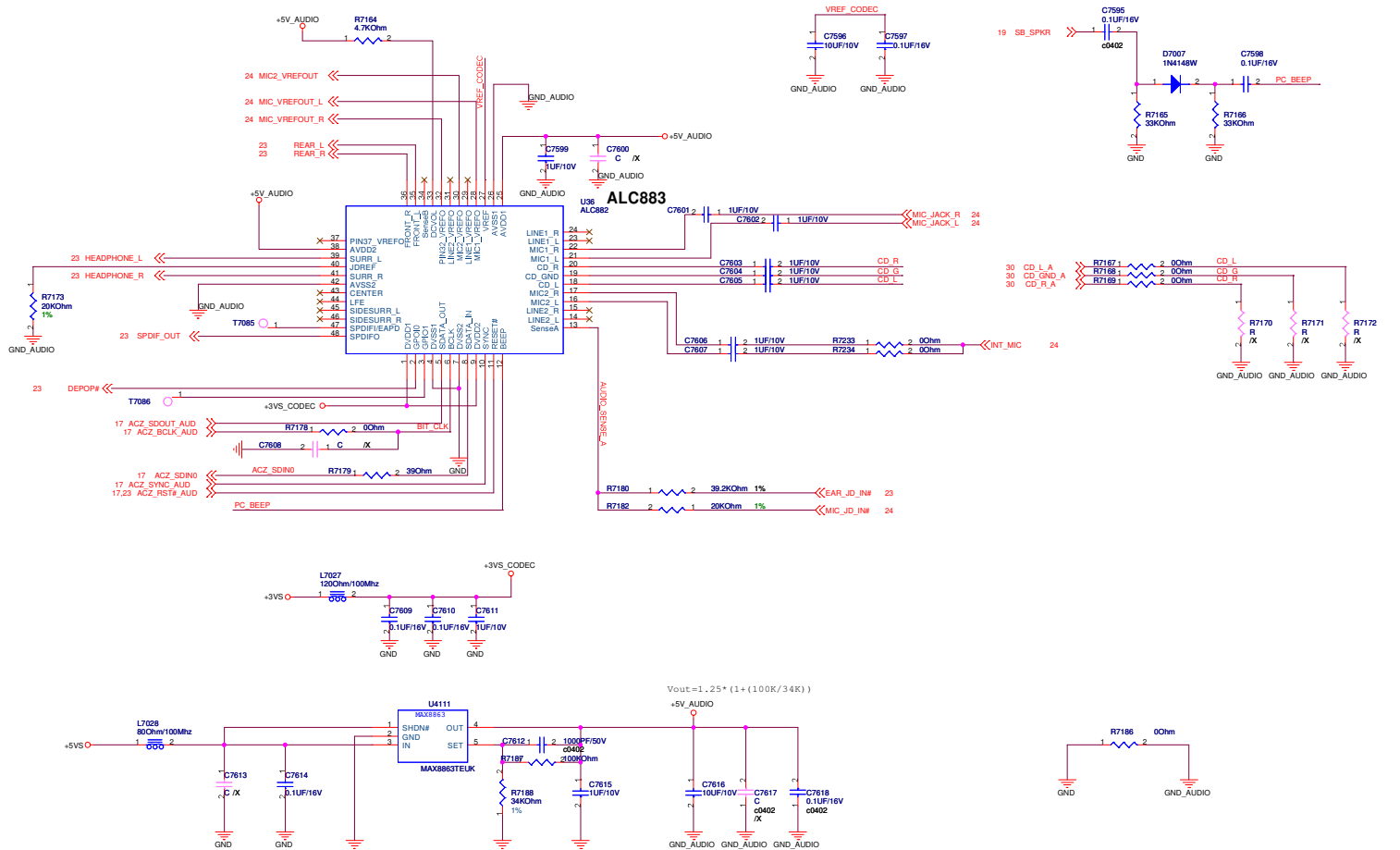
Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
 12 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 12 mils
 -----OTHER SIGNALS

Avoid BPSB,Power

ASUS		Title : THER-SENSOR,FAN	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	2.00
Custom	Z62E	Date	11/15/2007
Sheet 21		of 59	

« Kennedy_Zhang »

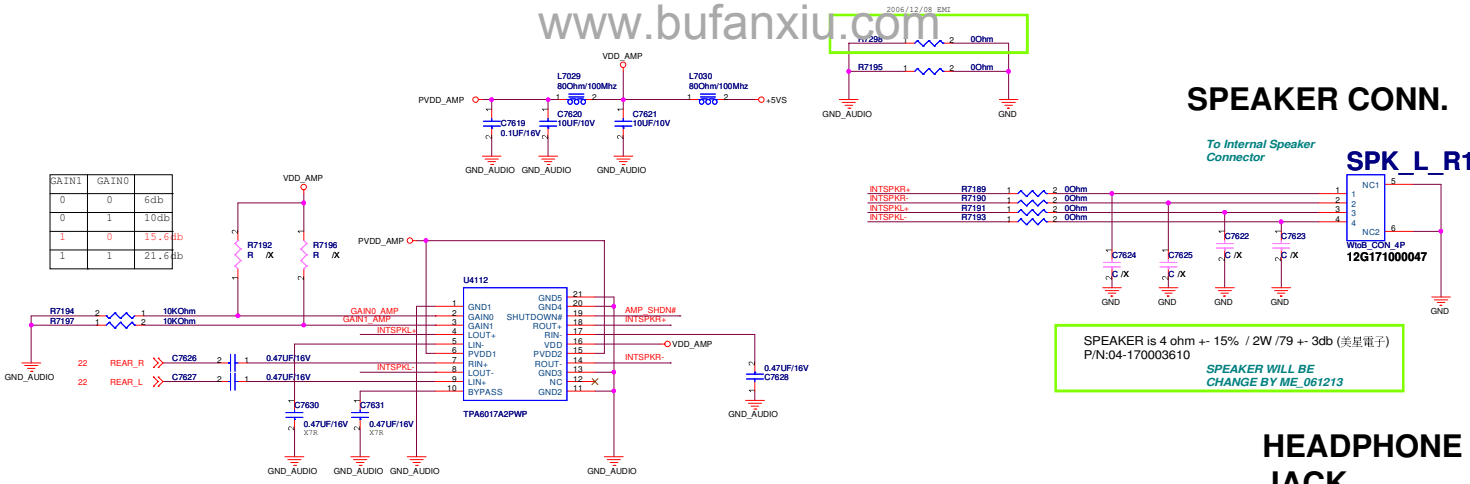


<Variant Name>

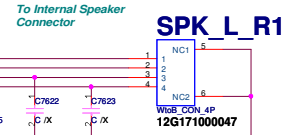
ASUS		Title : CODEC-ALC882	
Site	Project Name	Engineer:	Mike Lee
Custom	262E		
Date: 08_15_2007	Sheet: 22	of	58

« Kennedy_Zhang »

SAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	13.5db
1	1	21.5db



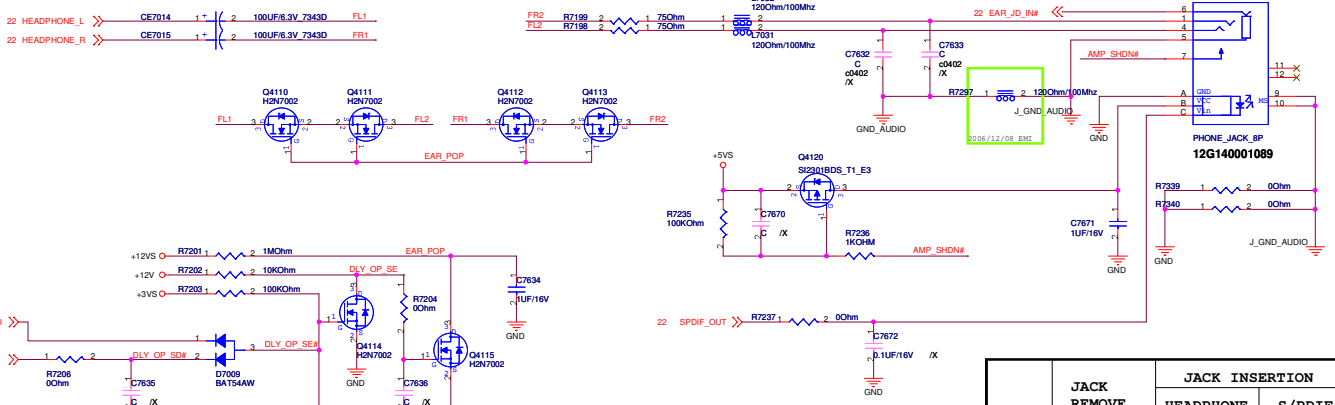
SPEAKER CONN.



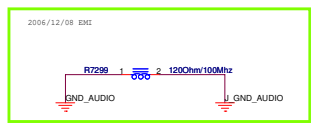
SPEAKER is 4 ohm +/- 15% / 2W / 79 + 3db (美星電子)
 P/N:04-170003610
 SPEAKER WILL BE CHANGE BY ME_061213

HEADPHONE JACK

HP_SPDIF1

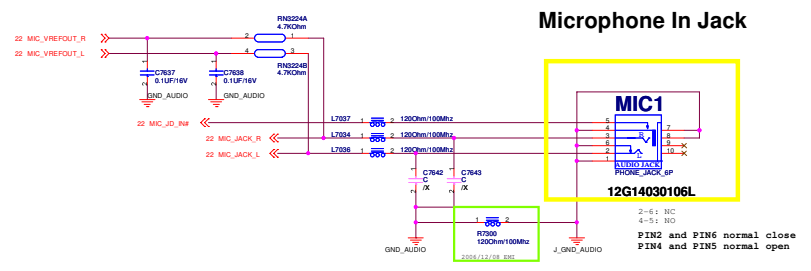
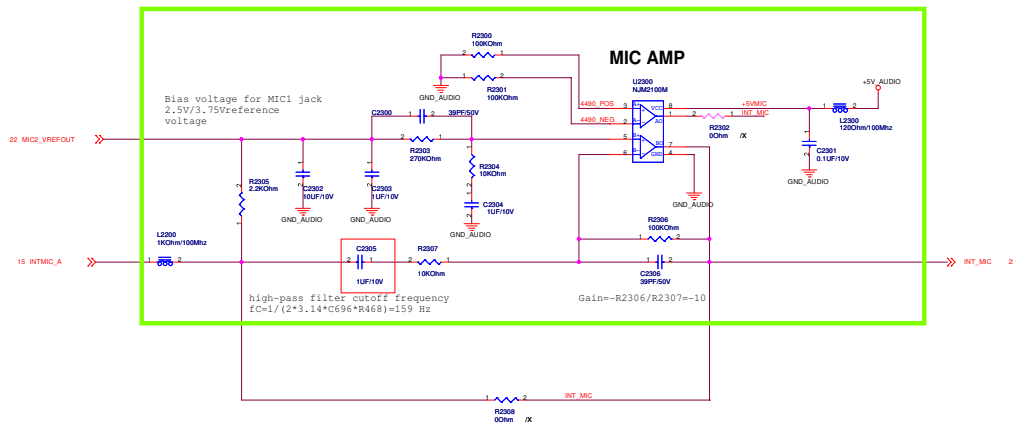


JACK REMOVE	JACK INSERTION	
	HEADPHONE	S/PDIF
PIN6	OPEN	LOW
PIN7	HIGH	LOW



ASUS
ASUSTeK COMPUTER INC. NBI Title : HP JACK & AMP
 Engineer: Mike Lee
 Project Name: 262E
 Date: 04_15_2007 Sheet: 28 of 58

« Kennedy_Zhang »



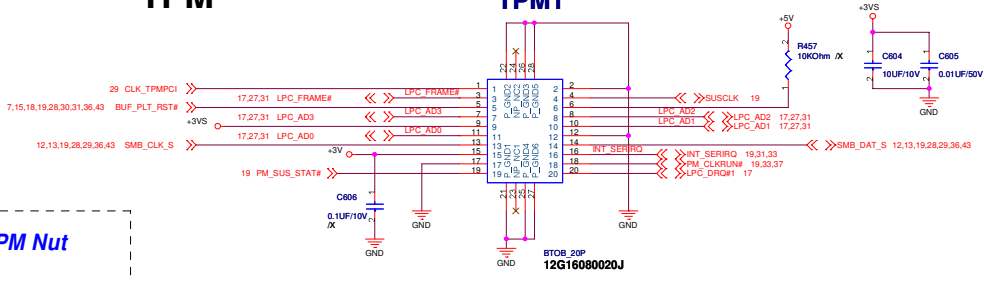
<Variant Name>

ASUS		Title : MIC JACK & Pre-AMP	
ASUSTeK COMPUTER INC. HSI		Engineer: Mike Lee	
Size	Project Name	Rev	
C	262B	2	2/93
Date: 98-10-15-2007	Sheet: 24	of	29

« Kennedy_Zhang »

TPM

TPM1

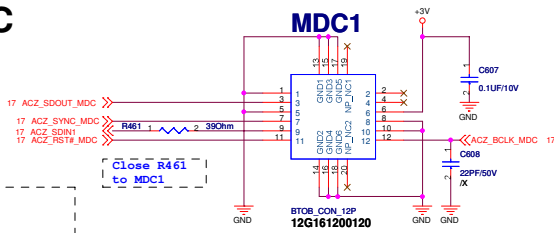


TPM Nut



MDC

MDC1

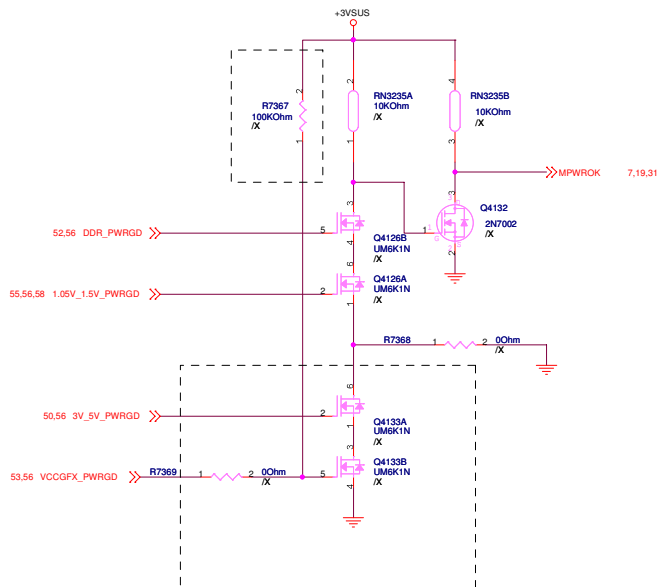
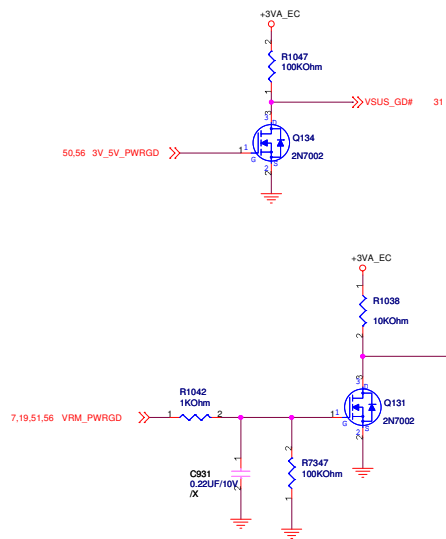


MDC Nut



ASUS		Title : MODULE-TPM / MDC	
ASUSTOR COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	762E	2.00	
Date: 08_15_2007		Sheet	26 of 59

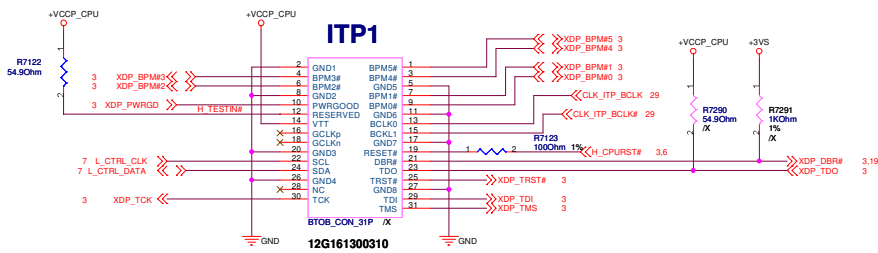
« Kennedy_Zhang »



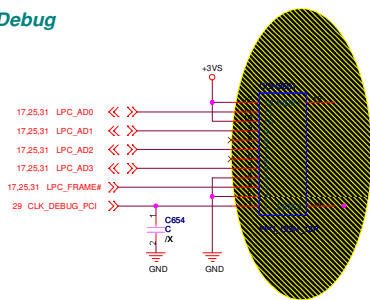
« Kennedy_Zhang »

<Variant Name>	
ASUS Title :POWER-ON SEQ.	
ASUSTek COMPUTER INC Engineer: Mike Lee	
Size	Project Name
Custom	Z62E
Date: 11/15/2007	Sheet 26 of 59

ITP



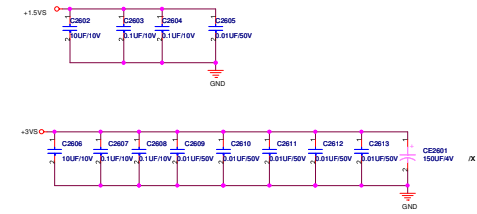
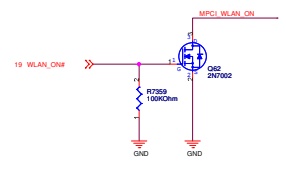
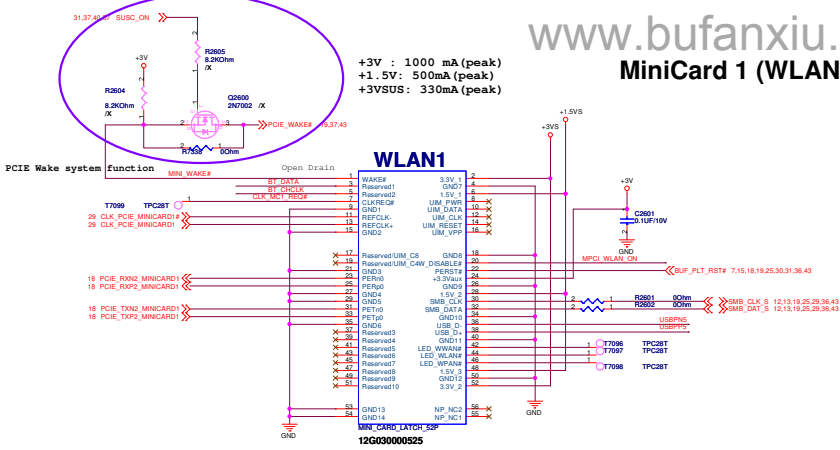
For Debug



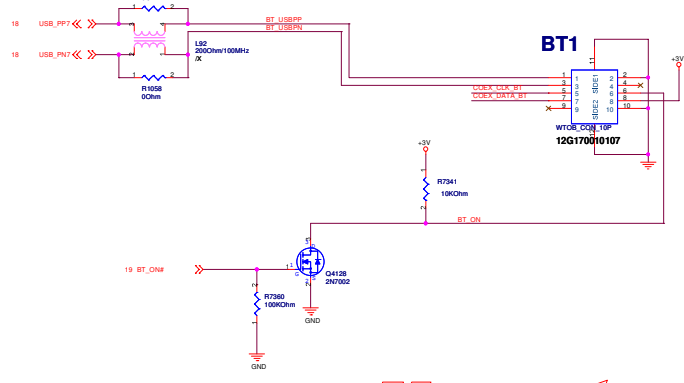
-Variant Name-

ASUS		Title : ITP/Debug connector	
ASUSTek Computer INC.		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	262E	2.03	
Date: 2007.11.15, 2007	Sheet 27	of	59

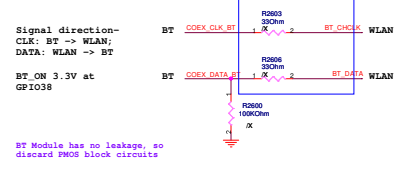
« Kennedy_Zhang »



BLUETOOTH CONNECTOR

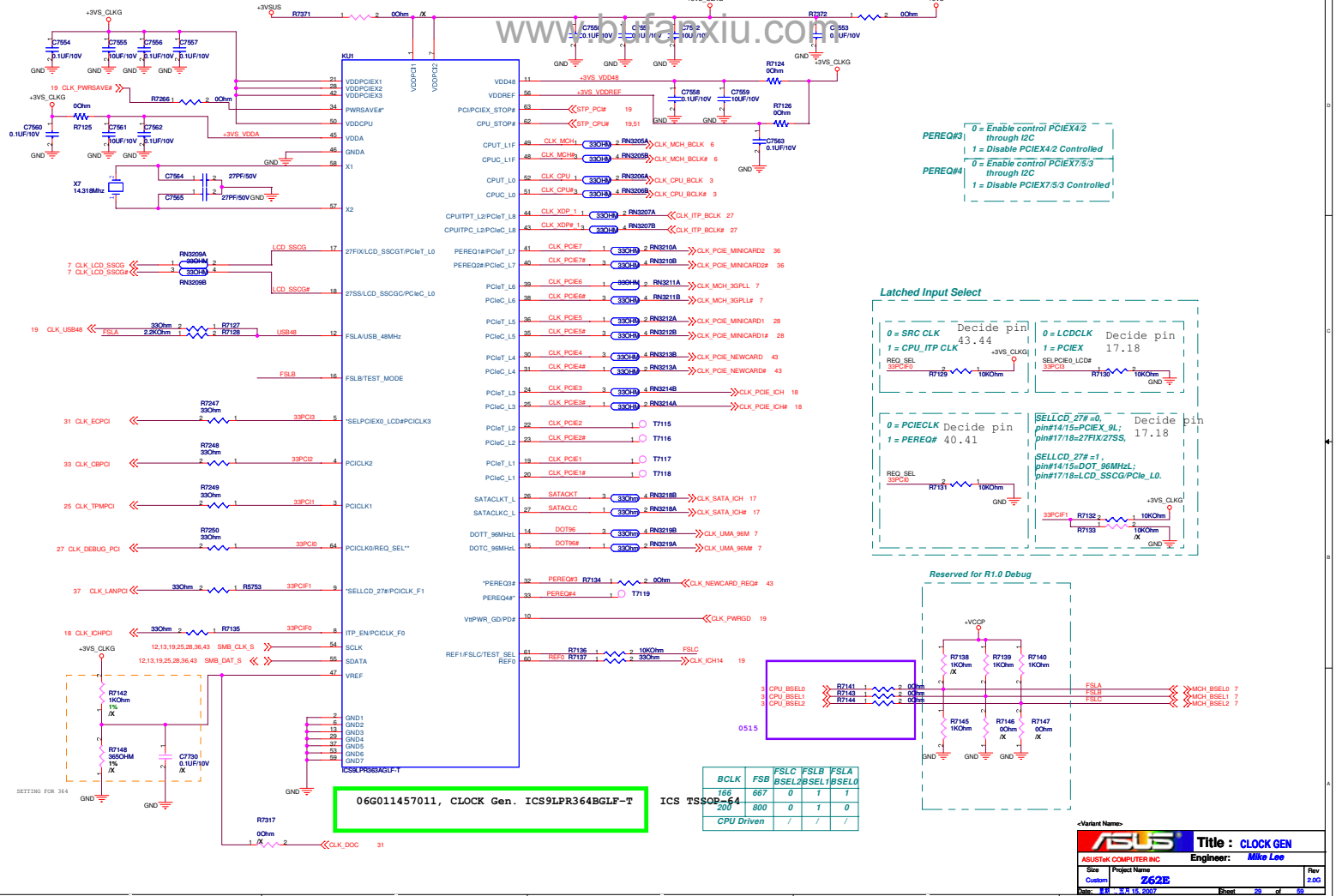


Check O/D output or push pull



ASUS		Title : MINI PCIe (TV) & BT Connector	
ASUSTEK COMPUTER INC.		Engineer: Mike Lee	
Size	Project Name	Rev	
C	262B	2/3	
Date: 11/15/2007	Sheet: 25	of	29

<< Kennedy_Zhang >>



PEREQ#3 = 0 = Enable control PCIeX4/2 through I2C
 = 1 = Disable PCIeX4/2 Controlled through I2C

PEREQ#4 = 0 = Enable control PCIeX7/5/3 through I2C
 = 1 = Disable PCIeX7/5/3 Controlled!

Latched Input Select

0 = SRC CLK Decide pin 43.44
 1 = CPU_I/P CLK

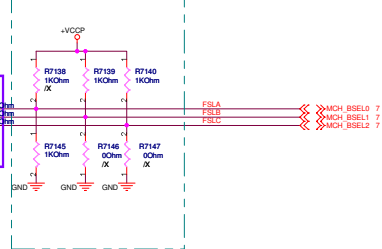
0 = LDCCLK Decide pin 17.18
 1 = PCIEX

0 = PCIECLK Decide pin 40.41
 1 = PEREQ#

0 = SELLCD_27# = 0 Decide pin 17.18
 pin#14:15=PCIEX_9L;
 pin#17:18=27FIX/27SS;

0 = SELLCD_27# = 1
 pin#14:15=DOT_96MHz;
 pin#17:18=LCD_SSCG/PCIE_L0;

Reserved for R1.0 Debug

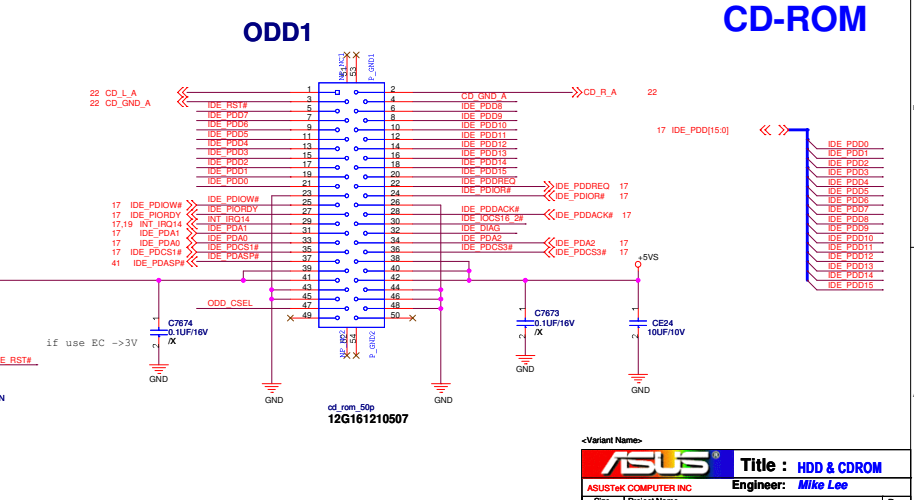
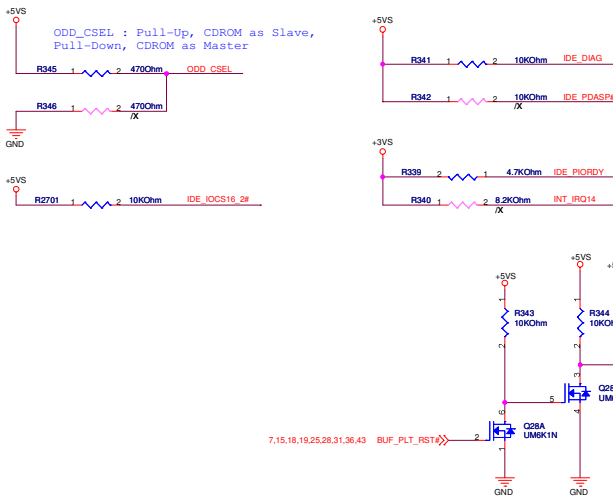
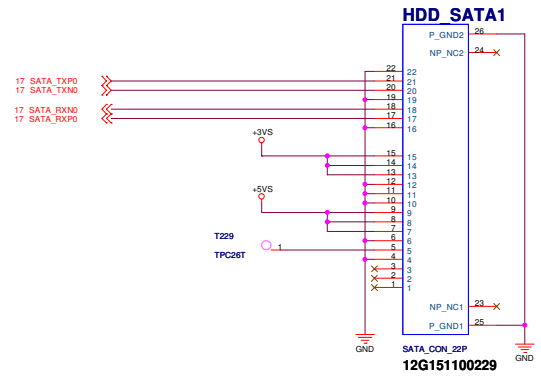
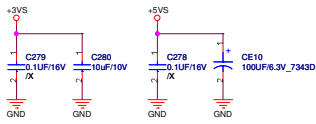


BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
CPU Driven	/	/	/	/

ASUSTeK COMPUTER INC. Title: CLOCK GEN
 Engineer: Mike Leo
 Size: Custom Project Name: Z62E Rev: 2.0G
 Date: 4.15.2007 Sheet: 25 of 29

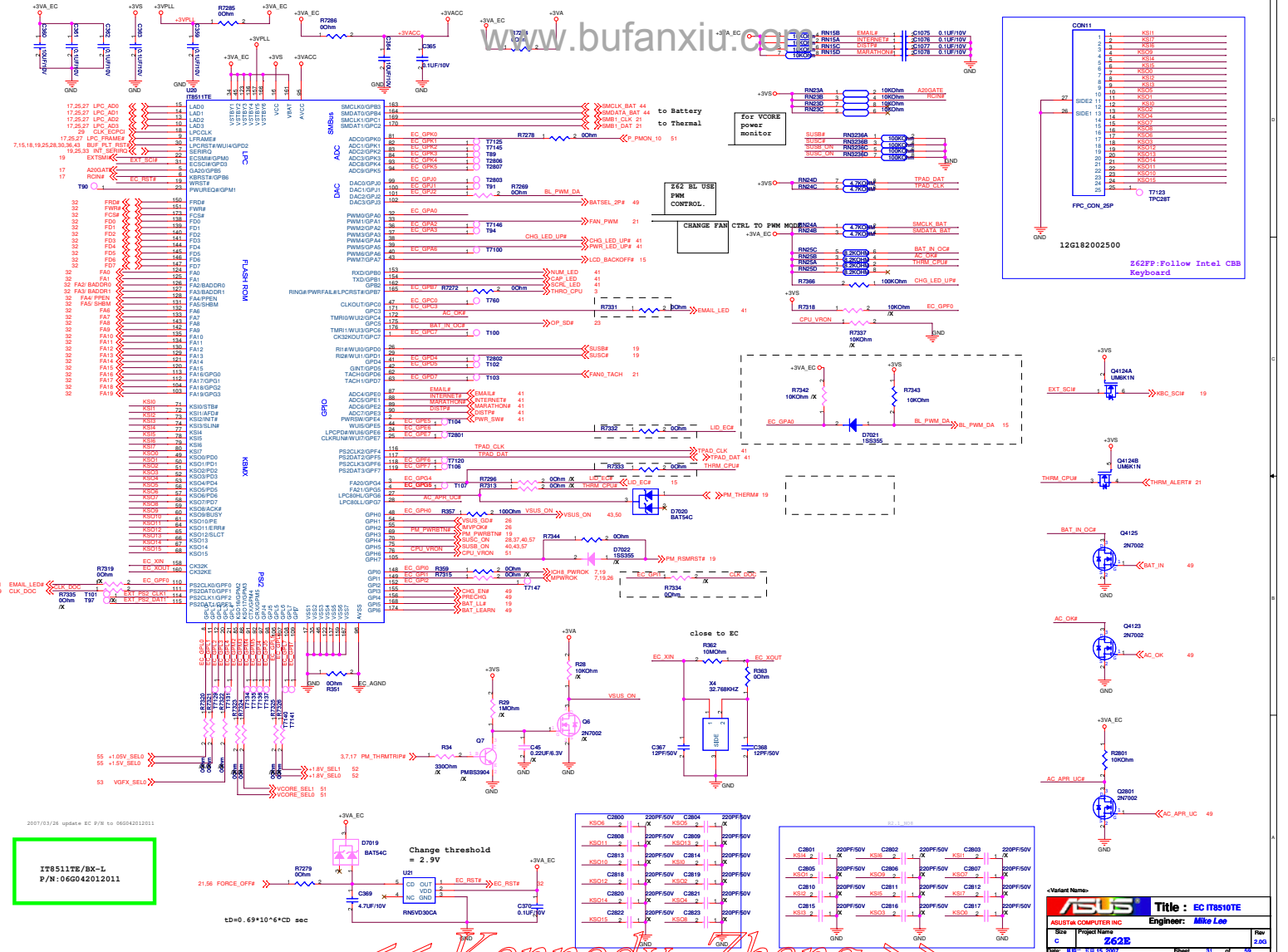
<< Kennedy_Zhang >>

SATA HDD Connector

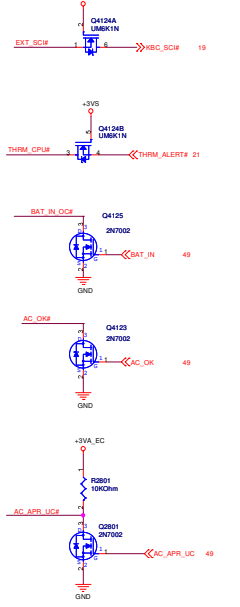
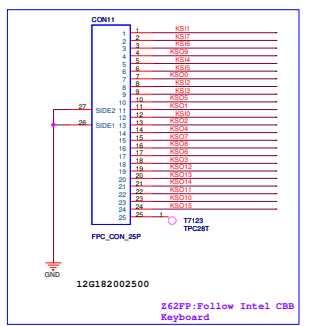
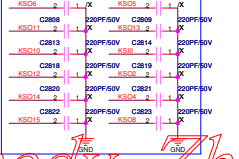
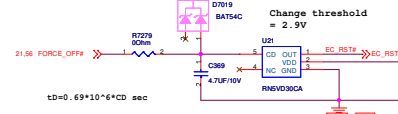


ASUS Title : HDD & CDROM
ASUSTEK COMPUTER INC Engineer: Mike Lee
Site: Custom Project Name: Z62E
Date: 08/15/2007 Rev: 2.00
Sheet: 30 of 58

« Kennedy_Zhang »

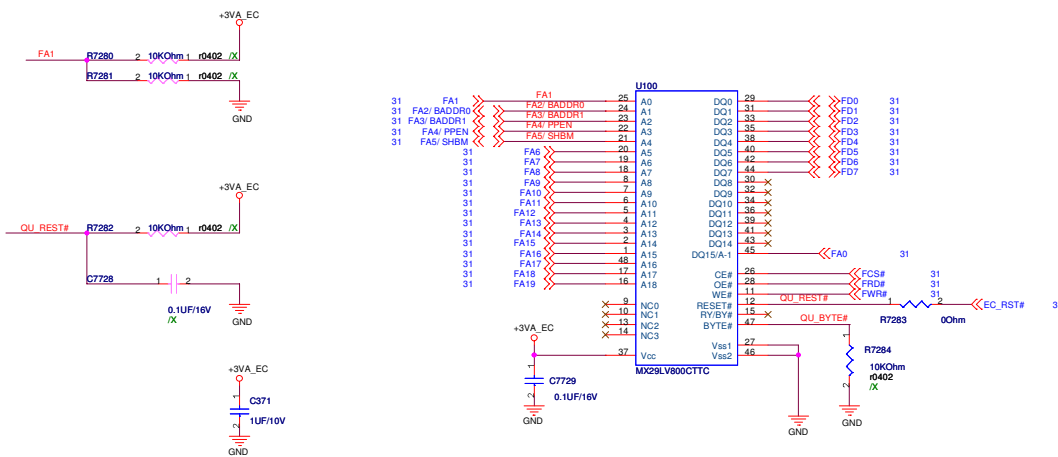


IT78511TE/BV-L
P/N:066042012011



ASUS		Title: EC18S10TE
ASUSTIA COMPUTER INC		Engineer: Mike Lee
Size: C	Project Name: Z62B	Rev: 2/93
Date: 10/15/2007	Sheet: 51	of: 59

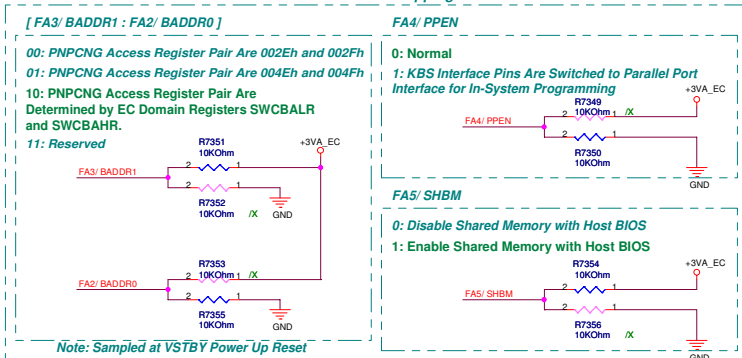
<< Kennedy_Zhang >>



BIOS: 05G001204043

ISA ROM

EC Hardware Strapping

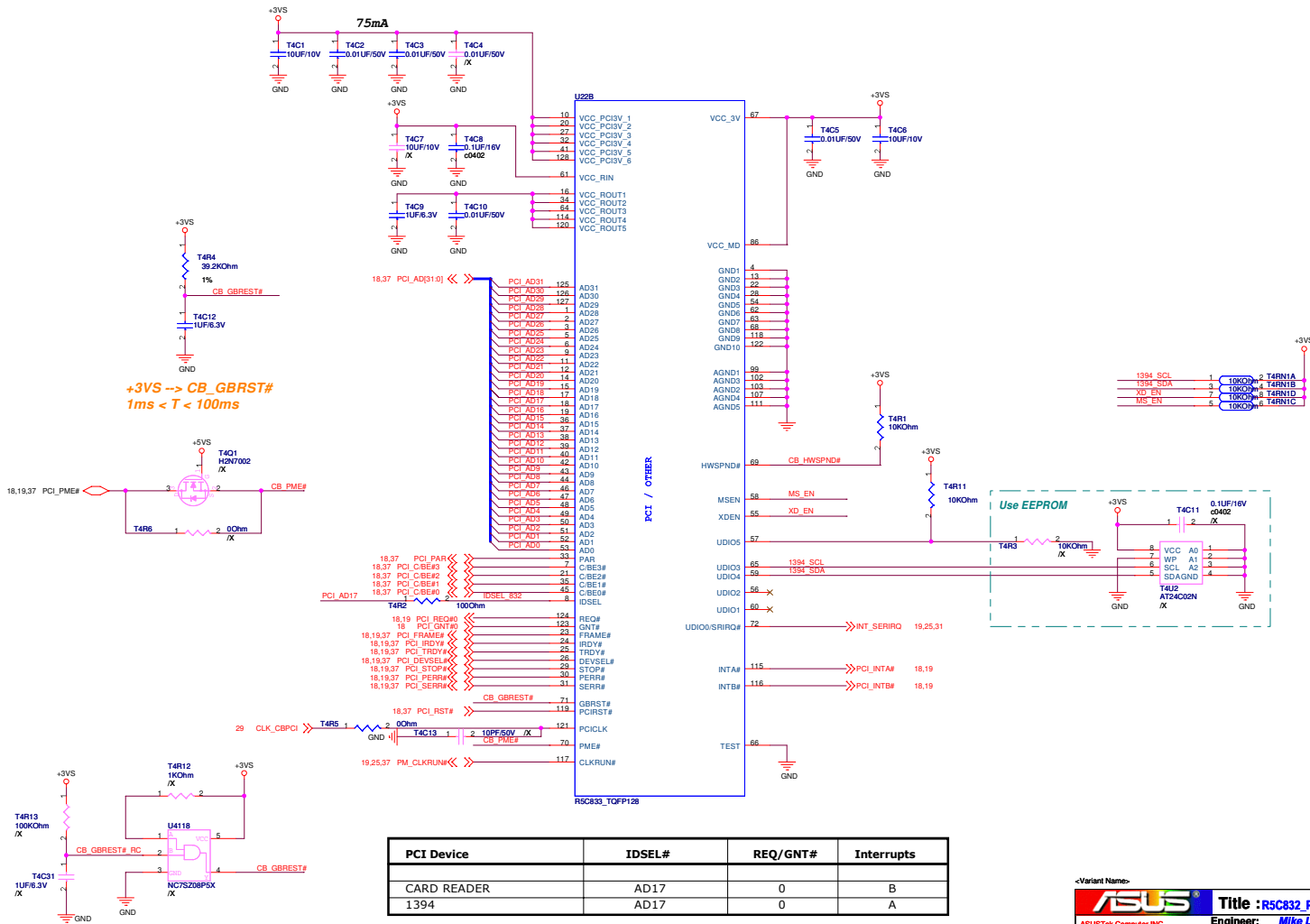


Note: Sampled at VSTBY Power Up Reset

<Variant Name>

ASUS		Title: EC:J78510TE(2/2) & ROM	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Date	Rev
Custom	Z62E	11/15/2007	2.00
Date: 11/15/2007		Sheet: 32	of 59

<< Kennedy_Zhang >>



PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A

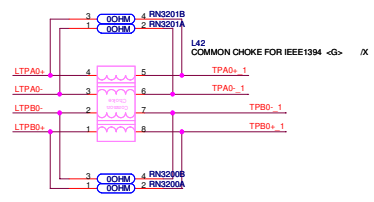
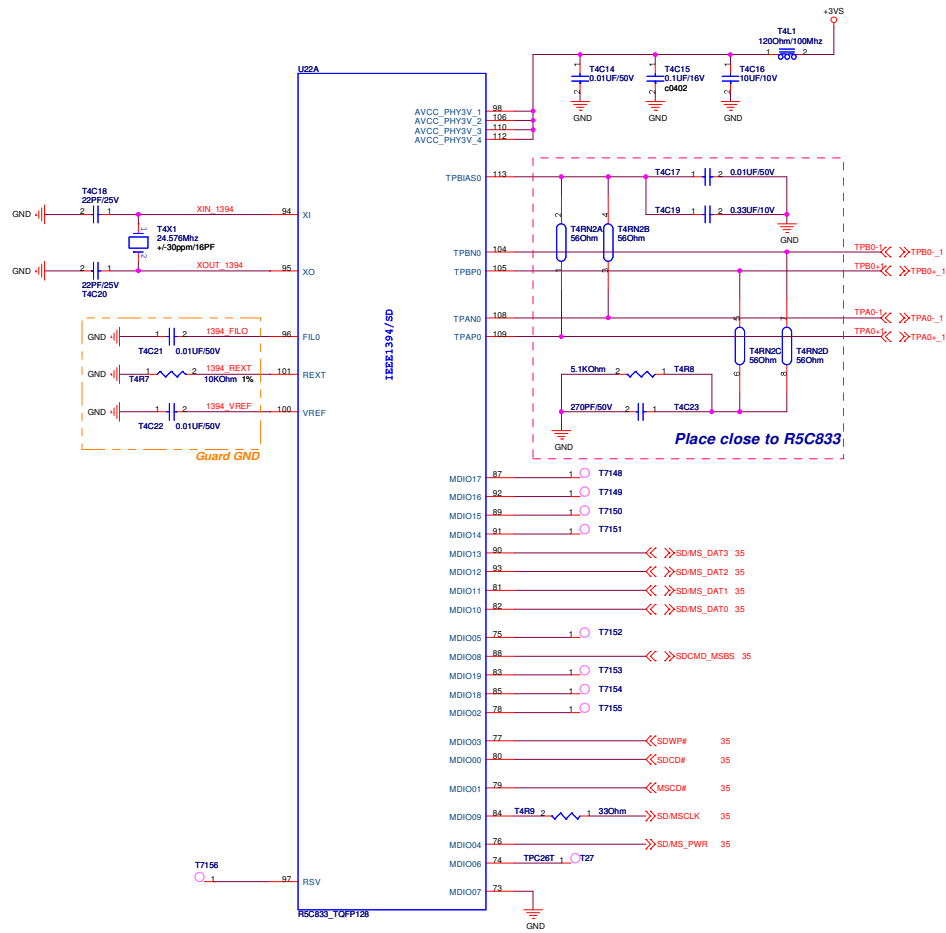
<Variant Name>

ASUS Title : R5C832_PCI

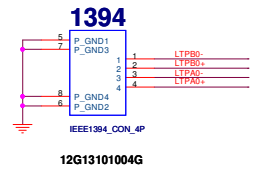
ASUSTek Computer INC. Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.00
Date: 05/15/2007	Sheet	33 of 50

<< Kennedy_Zhang >>



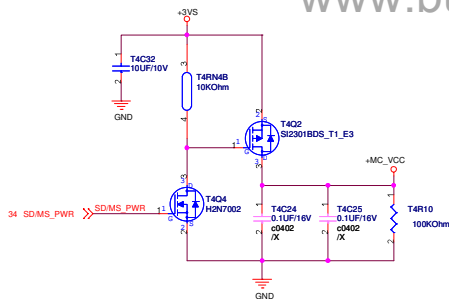
1. The area is as compact as possible, length < 10 mm
2. TPA Pair and TPB pair mismatch < 2.5mm
3. No via recommend, maximum is one.
4. Total length < 50 mm
5. Differential impedance is 110+/- 6 ohm
6. TPA Pair trace or TPB pair trace < 1.25mm



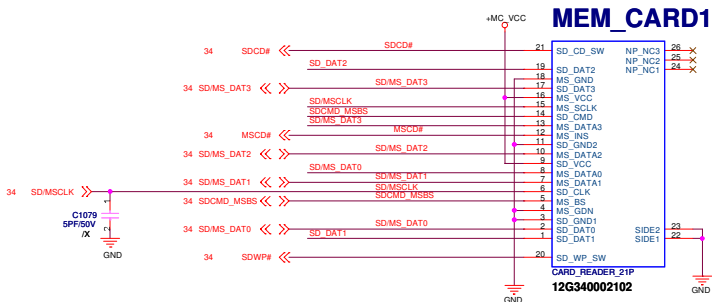
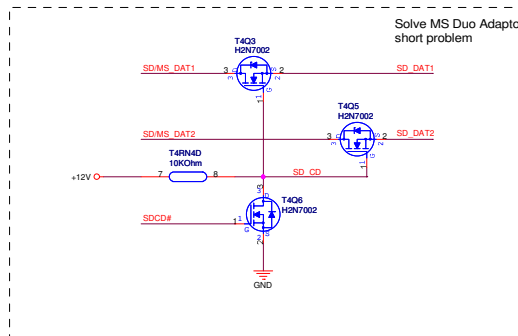
<Variant Name>

ASUS		Title : R5C32_1394/SD
ASUSTek Computer INC.		Engineer: Mike Lee
Size	Project Name	Rev
Custom	762E	2.00
Date: 08_05.15.2007	Sheet	34 of 58

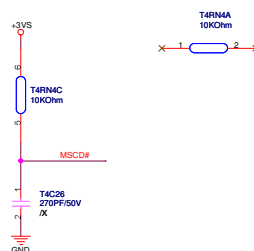
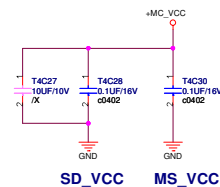
<< Kennedy_Zhang >>



Card Reader Power Switcher



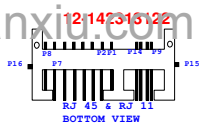
Layout: SHIELD GND



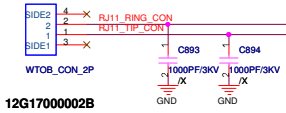
<Variant Name>

ASUS		Title 3 in 1 Card Reader	
ASUSTek Computer INC.		Engineer: Mika Lee	
Size	Project Name	Rev	
Custom	Z62E	2.0G	
Date: 08-15-2007	Sheet	35	of 59

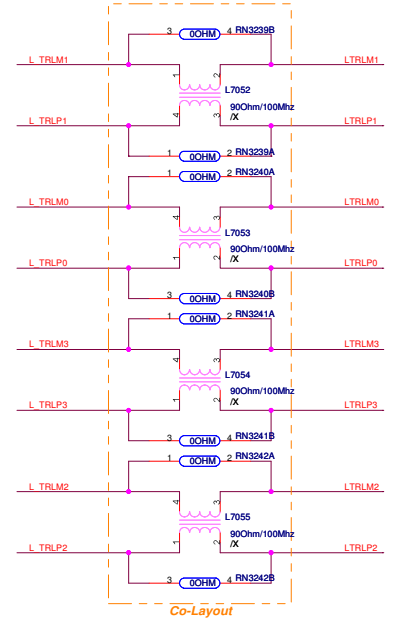
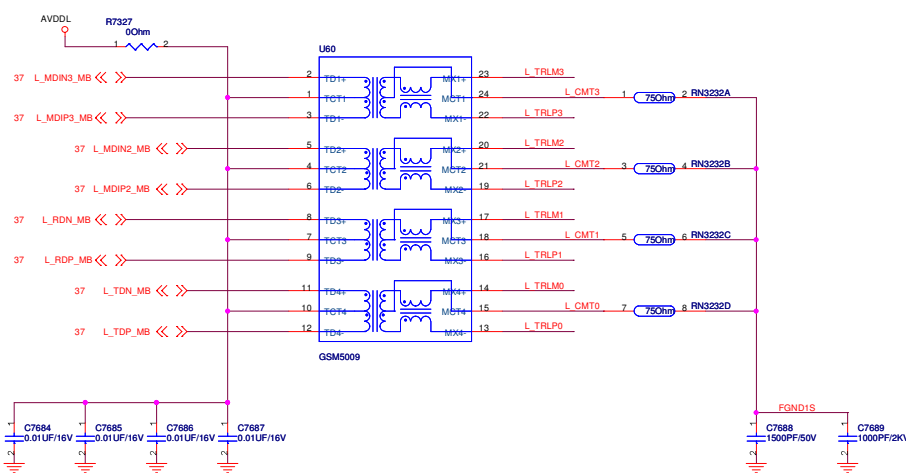
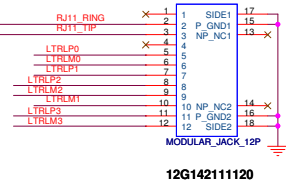
« Kennedy_Zhang »



RING1



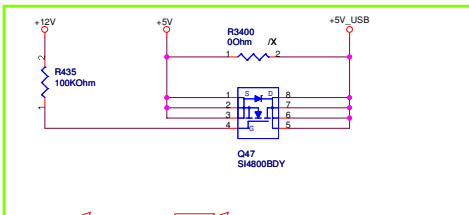
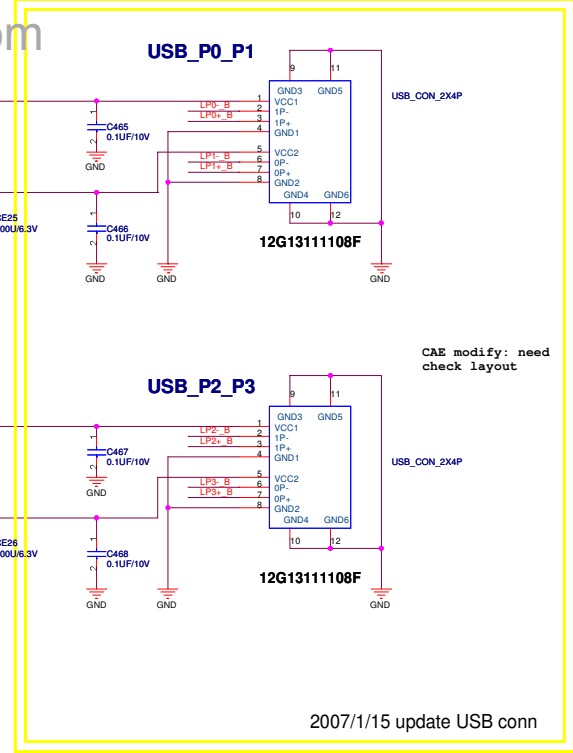
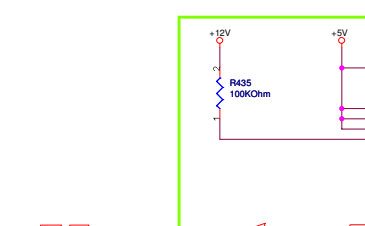
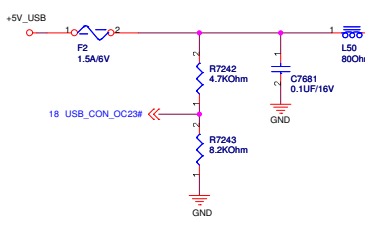
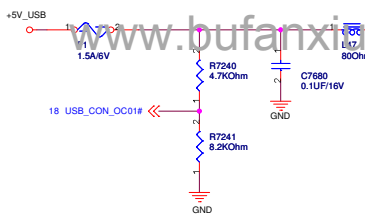
RJ45_RJ11



<Variant Name>

ASUS		Title : RJ11+45
ASUSTek COMPUTER INC		Engineer: Mike Lee
Size	Project Name	Rev
Custom	Z62E	2.00
Date: 11/15/2007	Sheet 38	of 59

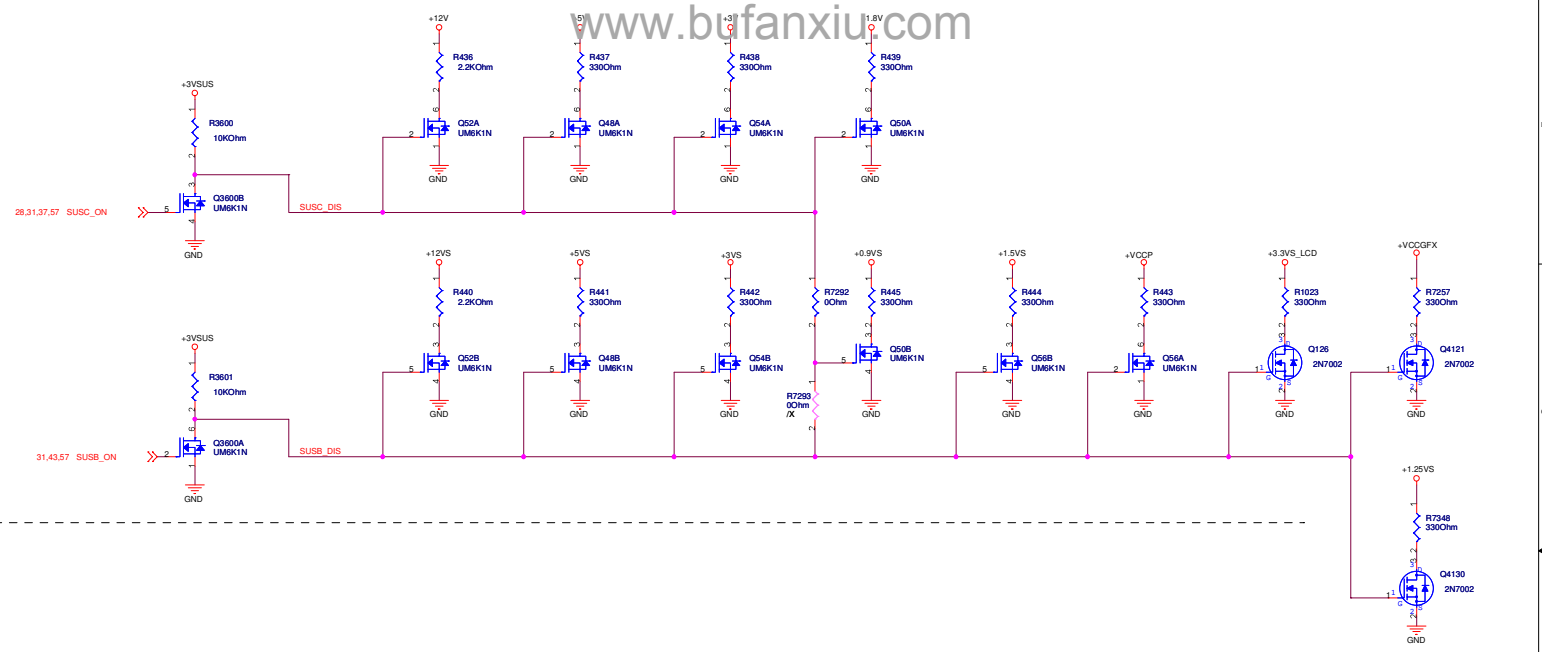
<< Kennedy_Zhang >>



<Variant Name>

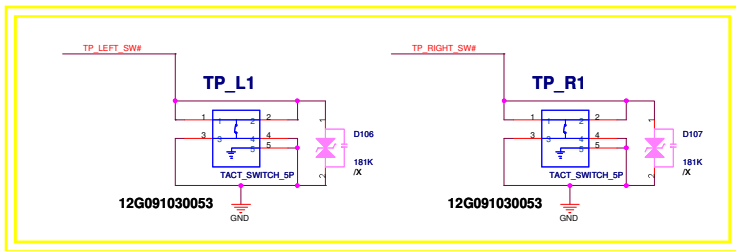
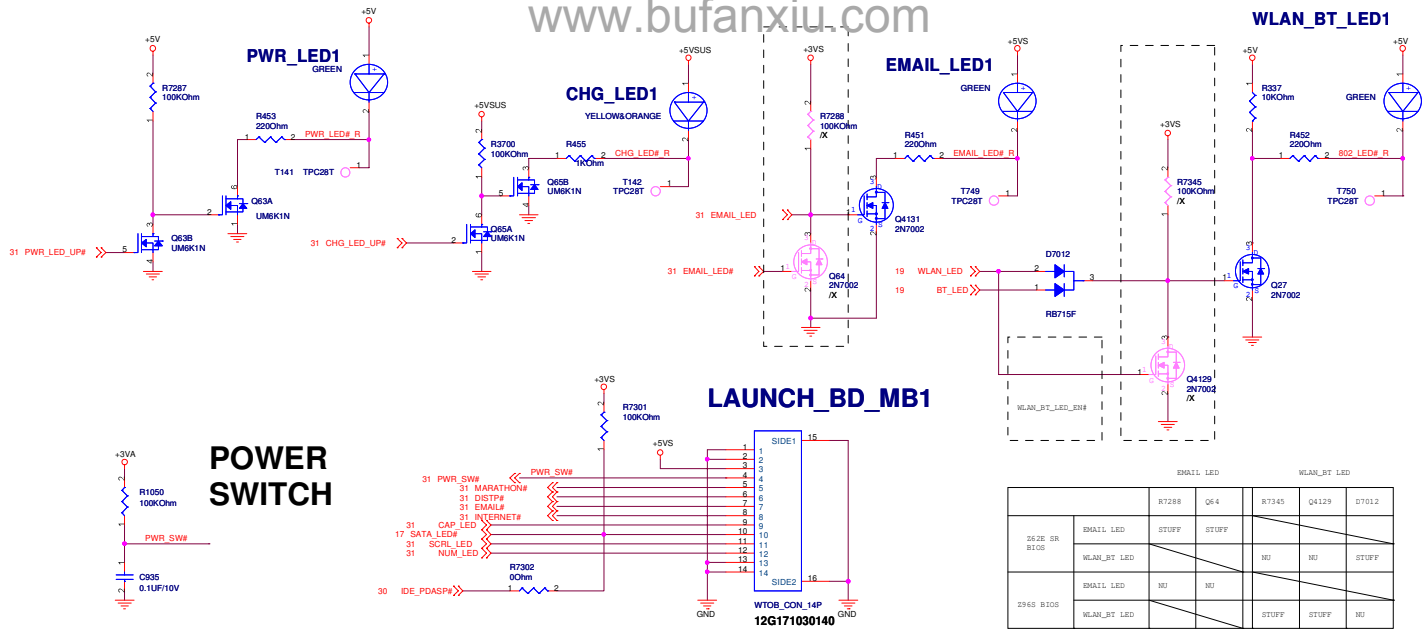
ASUS		Title : USB CONN X 5
ASUSTek COMPUTER INC		Engineer: Mike Lee
Size	Project Name	Rev
Customer	Z62E	2.00
Date: 08-11-15-2007	Sheet 39	of 59

<< Kennedy_Zhang >>



« Kennedy_Zhang »

ASUS		Title : Discharge Circuit	
ASUSTEK COMPUTER INC		Engineer: Mike Lee	
Size	Project Name		Rev
Custom	762E		2.00
Date: 8/15/2007		Sheet	40 of 58



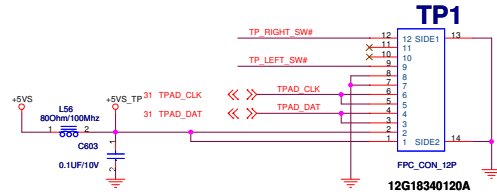
2007/1/15 change SW

TOUCH PAD SWITCH

Touch pad Definition

1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

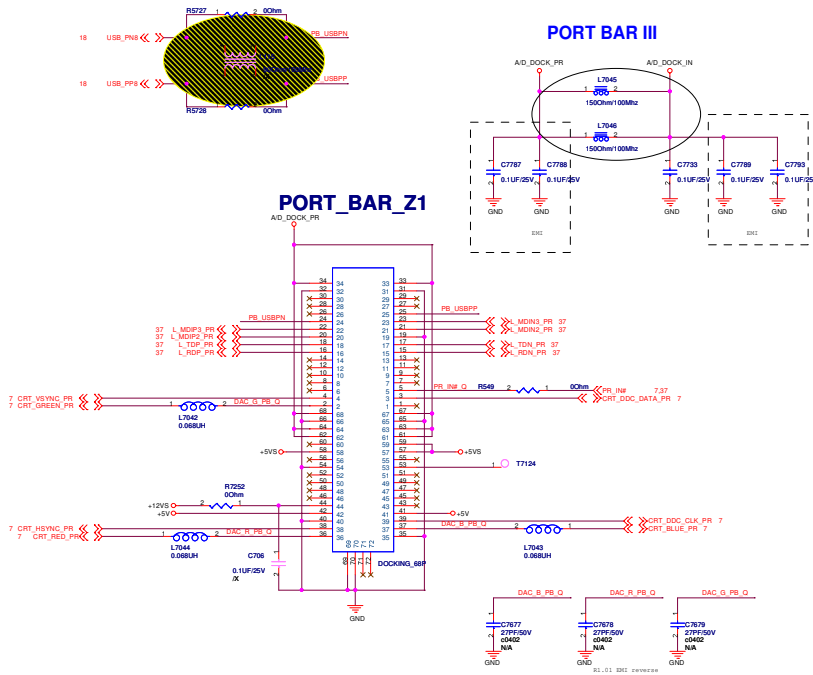
262F: pin1 reversal



<Variant Name>

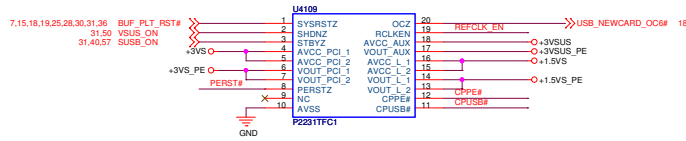
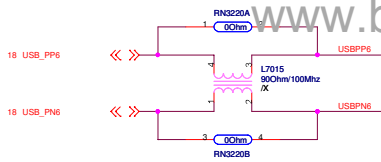
ASUS		Title : LED/SW/TouchPad	
ASUSTek COMPUTER INC		Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.00	
Date: 08/15/2007	Sheet: 41	of	58

« Kennedy_Zhang »

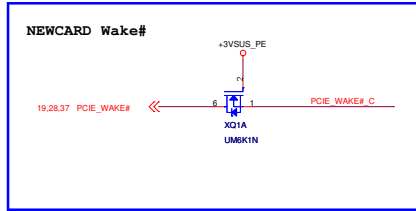
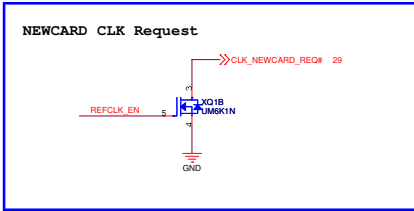
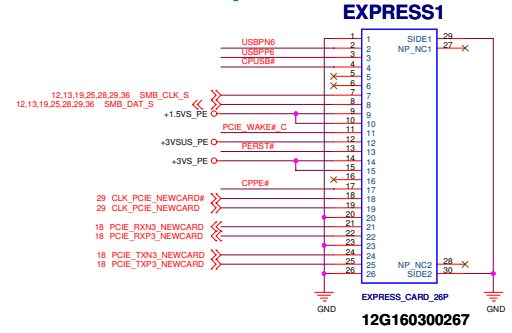


<< Kennedy_Zhang >>

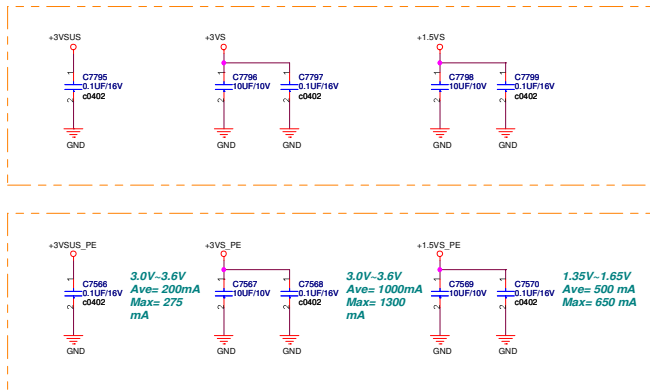
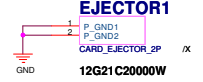
ASUS		Title : PORT BAR 3 Conn.	
ASUSTEK COMPUTER INC.		Engineer: Mike Lee	
Ver	Project Name	Rev	
C	262E	2	2/93
Date	10/15/2007	Sheet	45 of 59



ExpressCard Header

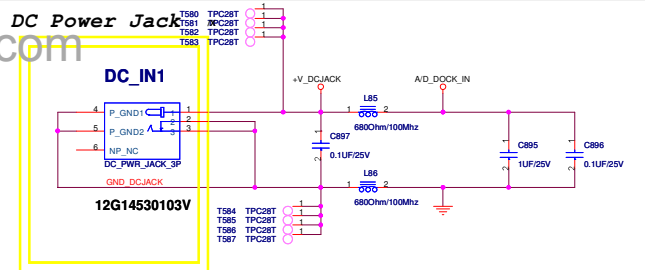
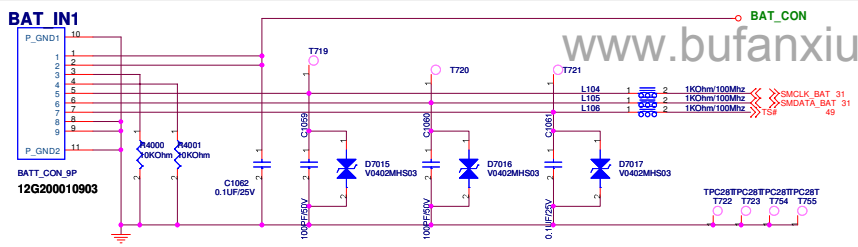


NewCard Ejector



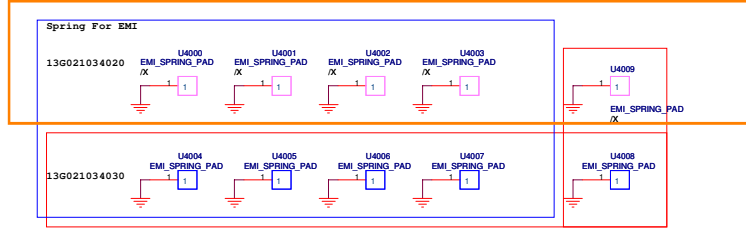
-Variant Name-		ASUS Title : ExpressCARD	
ASUSTek Computer INC.		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	762E	2.00	
Date: 07.15.2007	Sheet: 43	of	58

« Kennedy_Zhang »



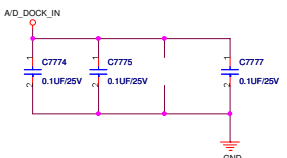
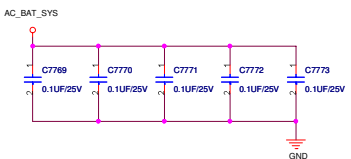
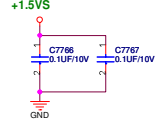
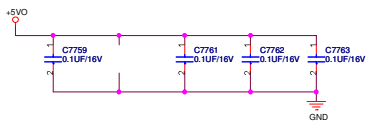
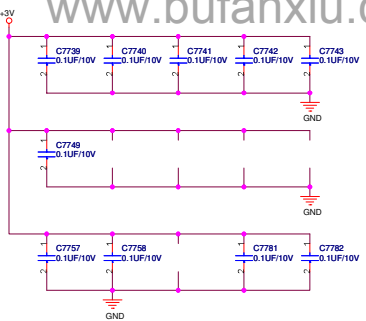
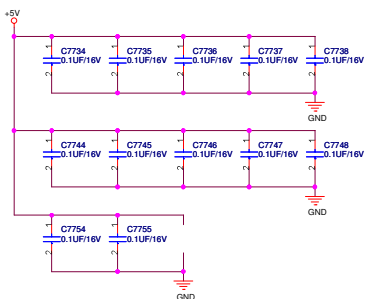
2007/1/15 change
DCIN jack

2007/04/01 13G021034020 SPRING --> NU



-Variant Name-		Title : DC/BATT IN	
ASUSTEK COMPUTER INC		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	762E	2.00	
Date: 05/15/2007		Sheet: 44	of 58

« Kennedy_Zhang »

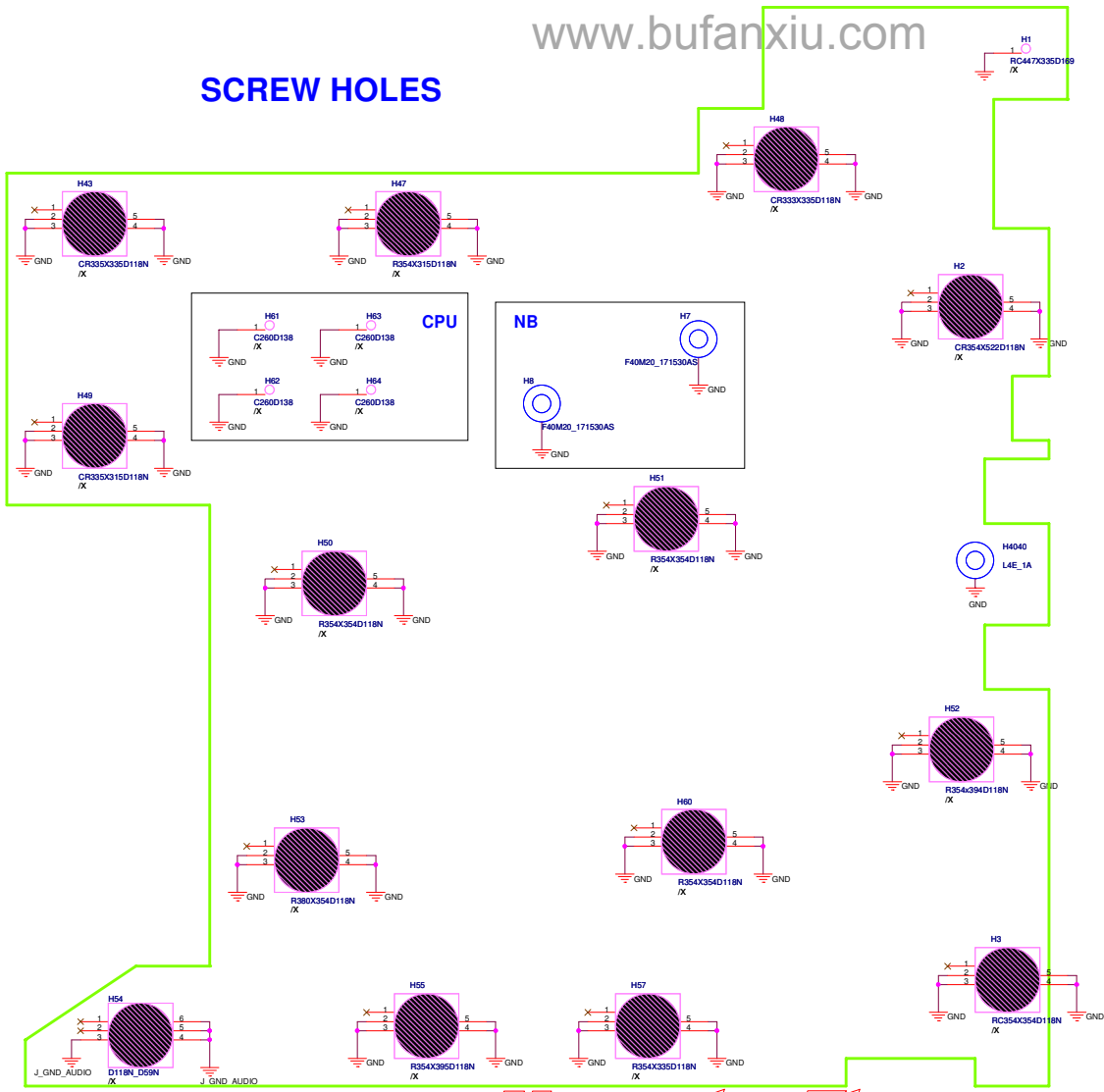


-Variant Name-

ASUS		Title : STITCHING CAP
ASUSTek Computer INC.		Engineer: Mike Lee
Size	Project Name	Rev
Custom	262E	2.03
Date: 2007.11.15	Sheet	45 of 58

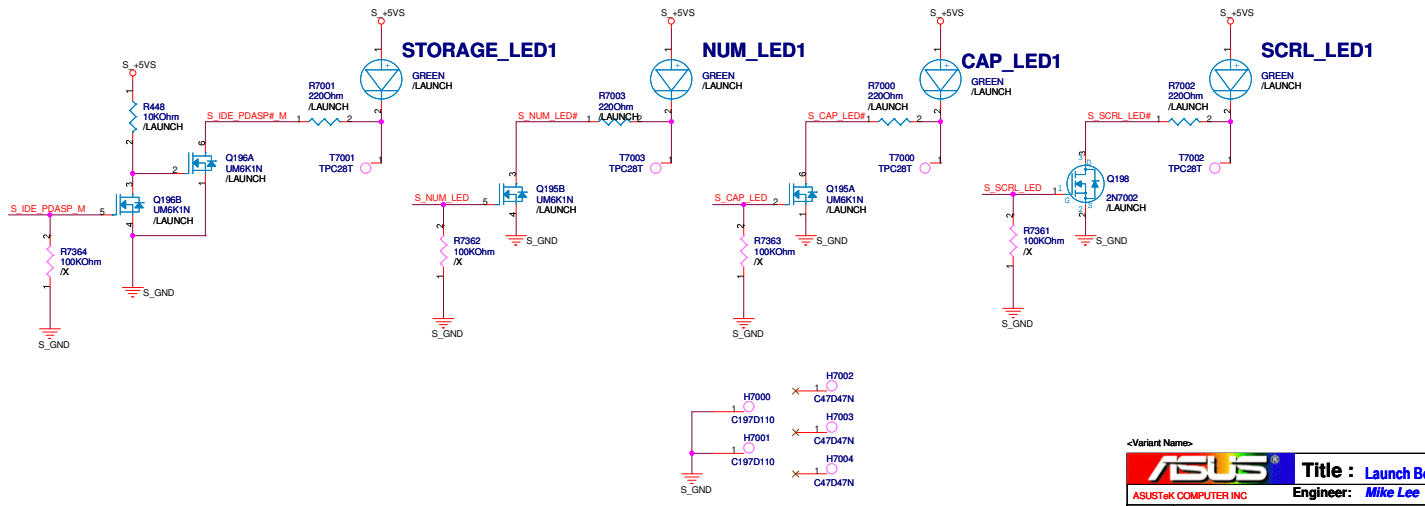
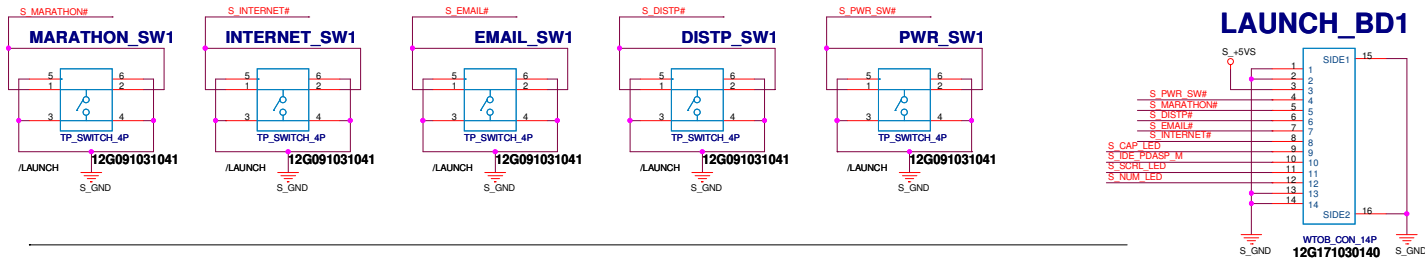
« Kennedy_Zhang »

SCREW HOLES



« Kennedy_Zhang »

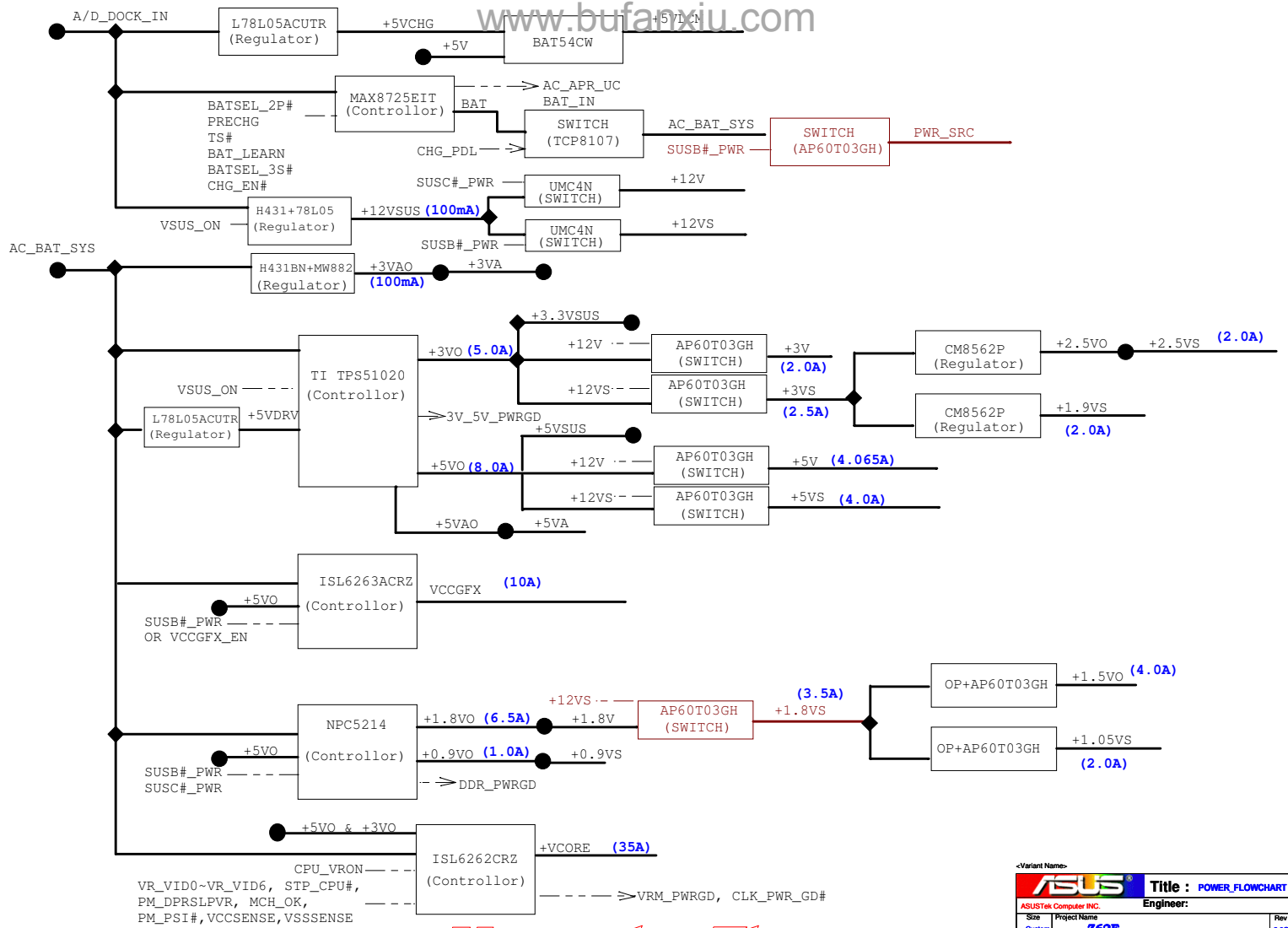
ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: Mike Lee	
Size	Project Name	Rev	
Custom	762E	2.00	
Date: 07.15.2007		Sheet: 46	of 59



<Variant Name>

ASUS		Title : Launch Board
ASUSTeK COMPUTER INC		Engineer: Mike Lee
Size	Project Name	Rev
B	262E	2.0G
Date: 2007.07.15	Sheet	47 of 59

<< Kennedy_Zhang >>



« Kennedy_Zhang »

ASUS		Title : POWER_FLOWCHART	
ASUSTek Computer Inc.		Engineer:	
Size	Project Name	Rev	
Custom	Z62E	2.00	
Date: 8/11/2007		Sheet 48	of 58

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(Adin)]*[VCLSV/VREF]

VCLSV = 2.855V

Adapter Max. Current

PR5708=20K PR5714 = 178K; Ilimit = 4.5A; 81W

PR5708=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * [Vref + (VCTL - 1.8V) / 9.52]]

VCTL = 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.5V]

Rsense(CHG) = 15m Ohm

Pre-Charging Mode

Precharging current = 148 - 152mA

Vctl = 0.107V - 0.109V

Battery Cell Selection

BATSEL_2PF = 1, 3 Cells; Vctl = 2.084V

=> Icharge = 1.6933A

BATSEL_2PF = 0, 6 or 9 Cells; Vctl = 2.111V

=> Icharge = 2.9329A

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (try to LDO pin) -> 4 Cells

2.0 > Vmode > 1.6V (floating) -> 3 Cells

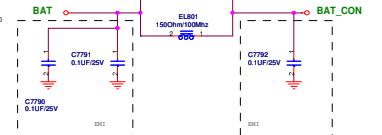
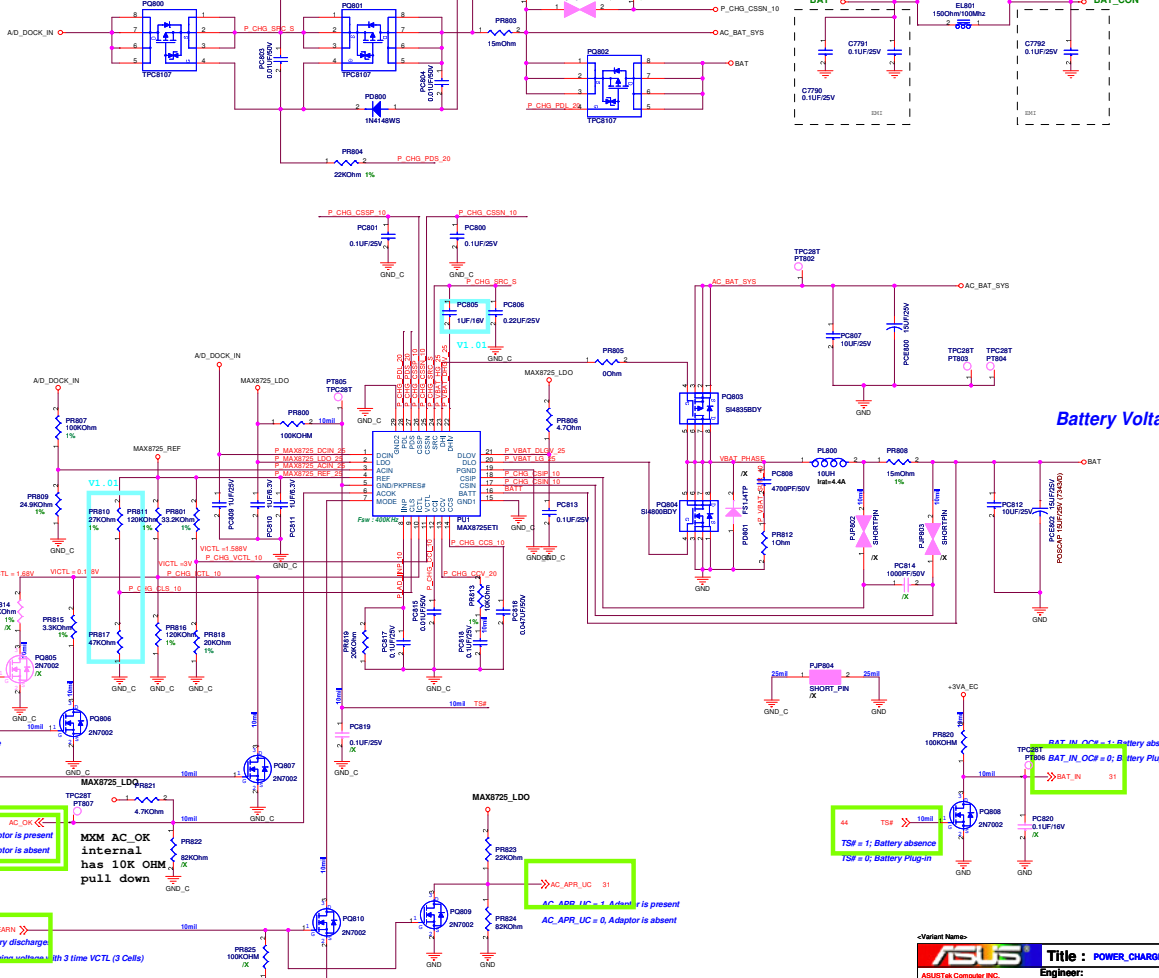
0.8 > Vmode (try to GND) -> Learning mode

VCTL < 0.8V or DCIN < 7V -> Charger Disable

MAX8725_LDO : 4.2235V

MAX8725_REF : 5.4V

POWER PATH & BAT_LEARN



Battery Voltage

- 31 BATSEL_2PF
- 31 PRECHG
- 31 CHG_ENF
- 31 AC_OK
- 31 BAT_LEARN

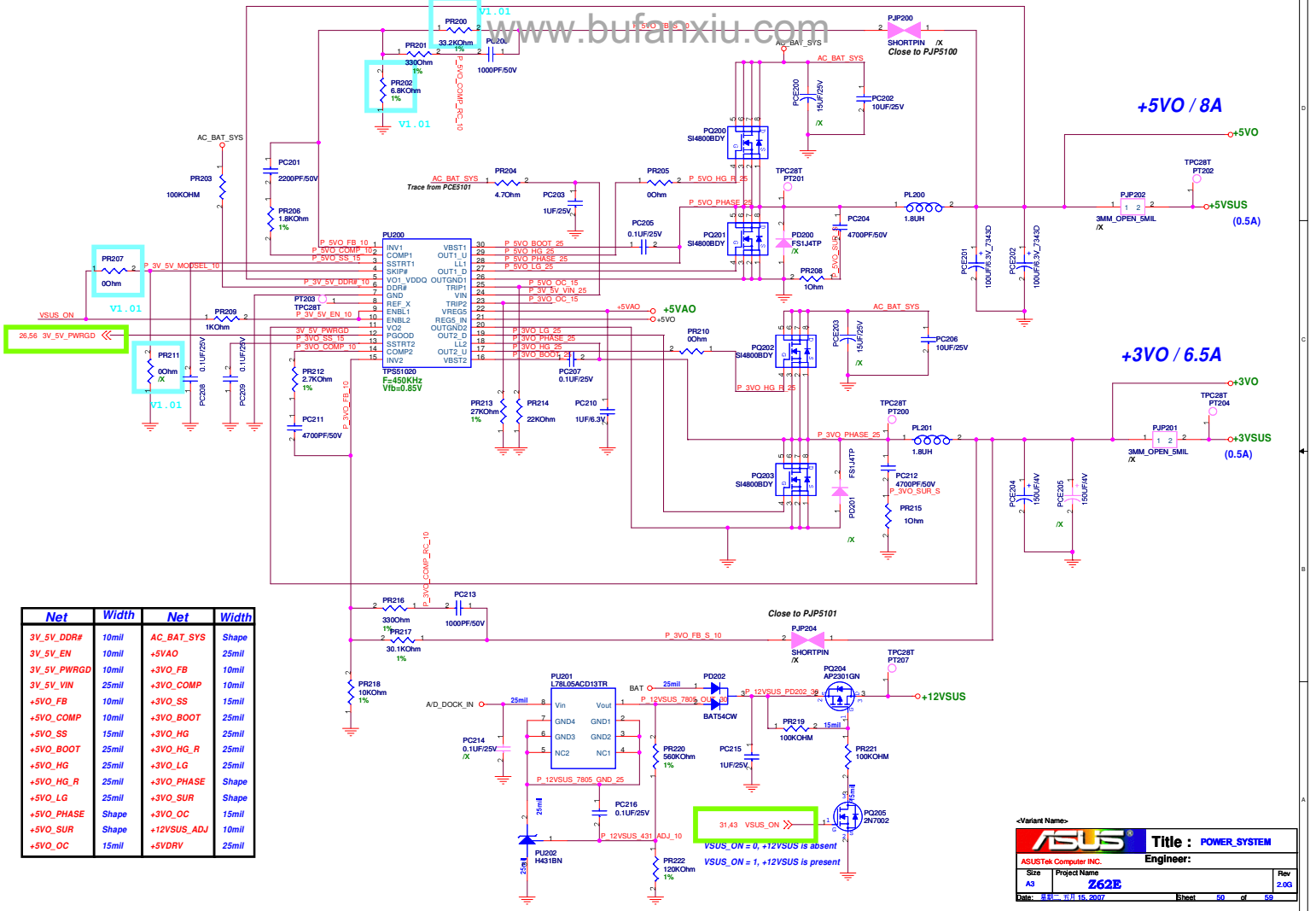
MAX8725_LDO internal has 10K OHM pull down

AC_APPR_UC = 1, Adaptor is present

TSE = 1; Battery absence

ASUS		Title : POWER_CHARGER	
ASUSTek Computer, Inc.			
Rev	Project Name	Engineer:	
C		284J	
Rev	Date	Sheet	of
	11.15.2017	49	59

<< Kennedy_Zhang >>



Net	Width	Net	Width
3V_SV_DDR#	10mil	AC_BAT_SYS	Shape
3V_SV_EN	10mil	+SVAO	25mil
3V_SV_PWRGD	10mil	+3VO_FB	10mil
3V_SV_VIN	25mil	+3VO_COMP	10mil
+SVO_FB	10mil	+3VO_SS	15mil
+SVO_COMP	10mil	+3VO_BOOT	25mil
+SVO_SS	15mil	+3VO_HG	25mil
+SVO_BOOT	25mil	+3VO_HG_R	25mil
+SVO_HG	25mil	+3VO_LG	25mil
+SVO_LG	25mil	+3VO_PHASE	Shape
+SVO_PHASE	25mil	+3VO_SUR	Shape
+SVO_SUR	Shape	+12VSUS_ADJ	15mil
+SVO_OC	15mil	+SVDRV	25mil

31.43 VSUS_ON >>
 VSUS_ON = 0, +12VSUS is absent
 VSUS_ON = 1, +12VSUS is present

<Variant Name>

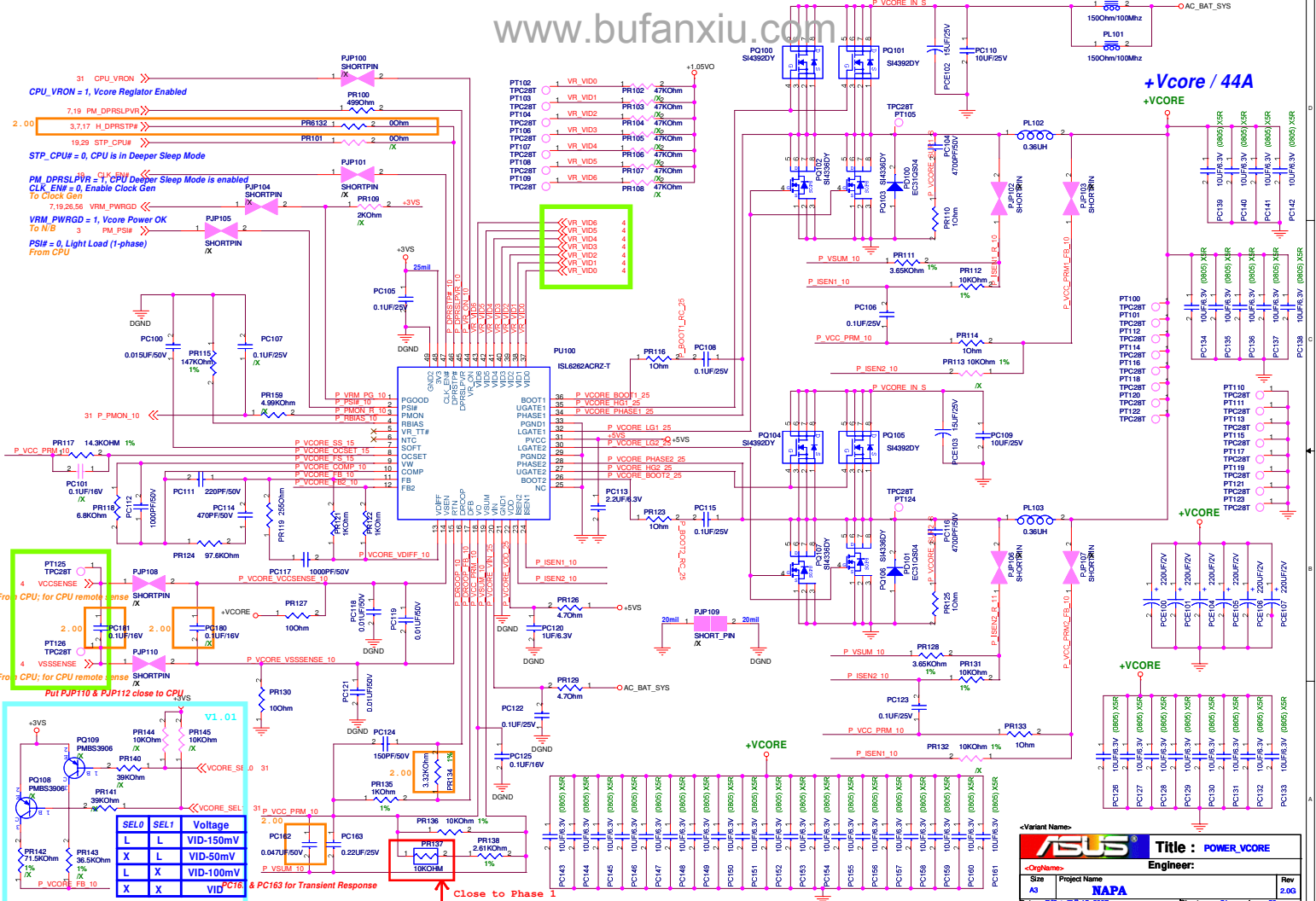
ASUS Title: POWER_SYSTEM

ASUSTek Computer INC. Engineer:

Site: Project Name: Rev: 2.00

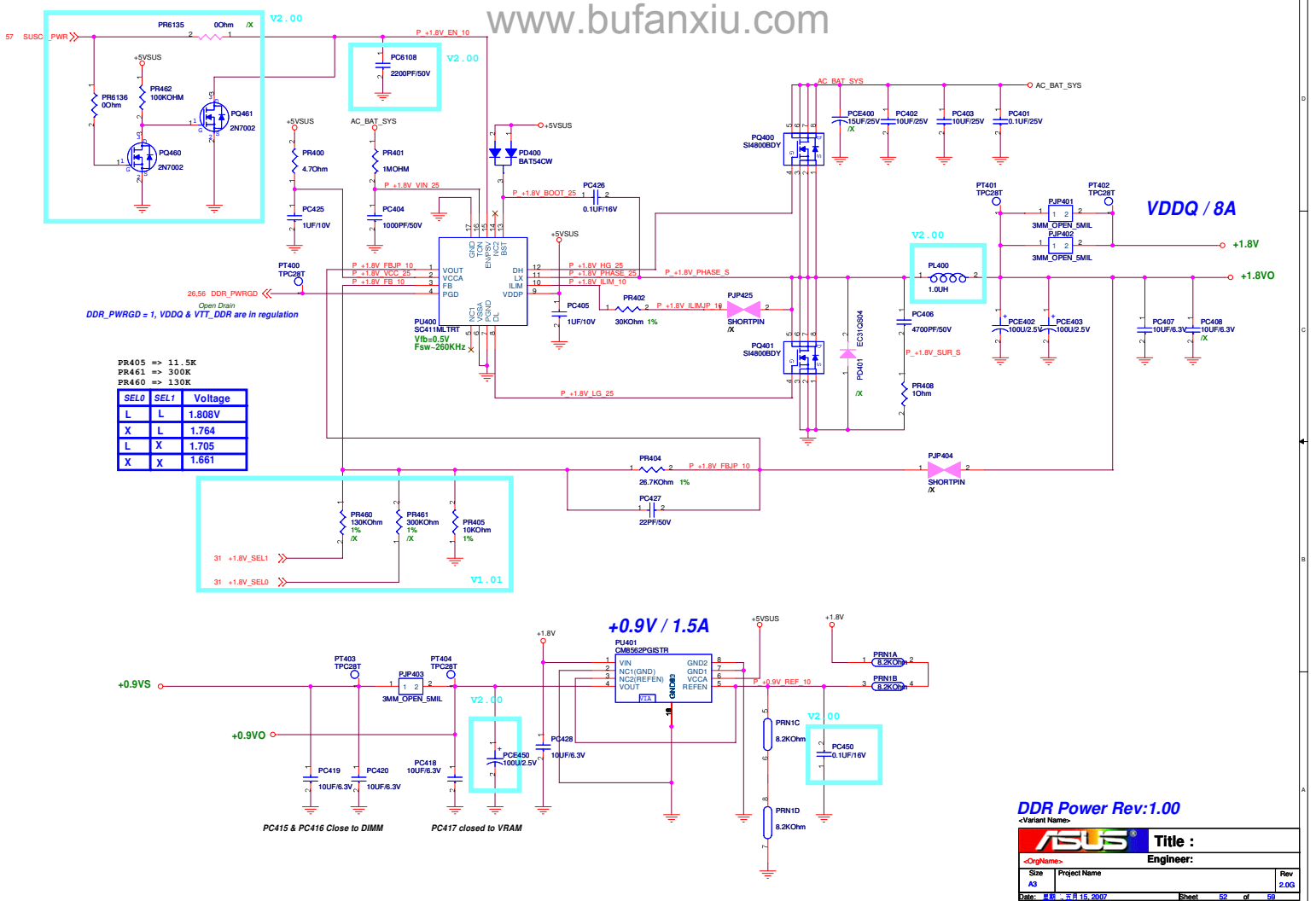
Date: 8/15/2007 Sheet 50 of 50


<< Kennedy_Zhang >>



ASUS Title: POWER_VCORE
 Project Name: NAPA
 Engineer: [Blank]
 Date: 11/15/2007
 Sheet 51 of 59

<< Kennedy_Zhang >>

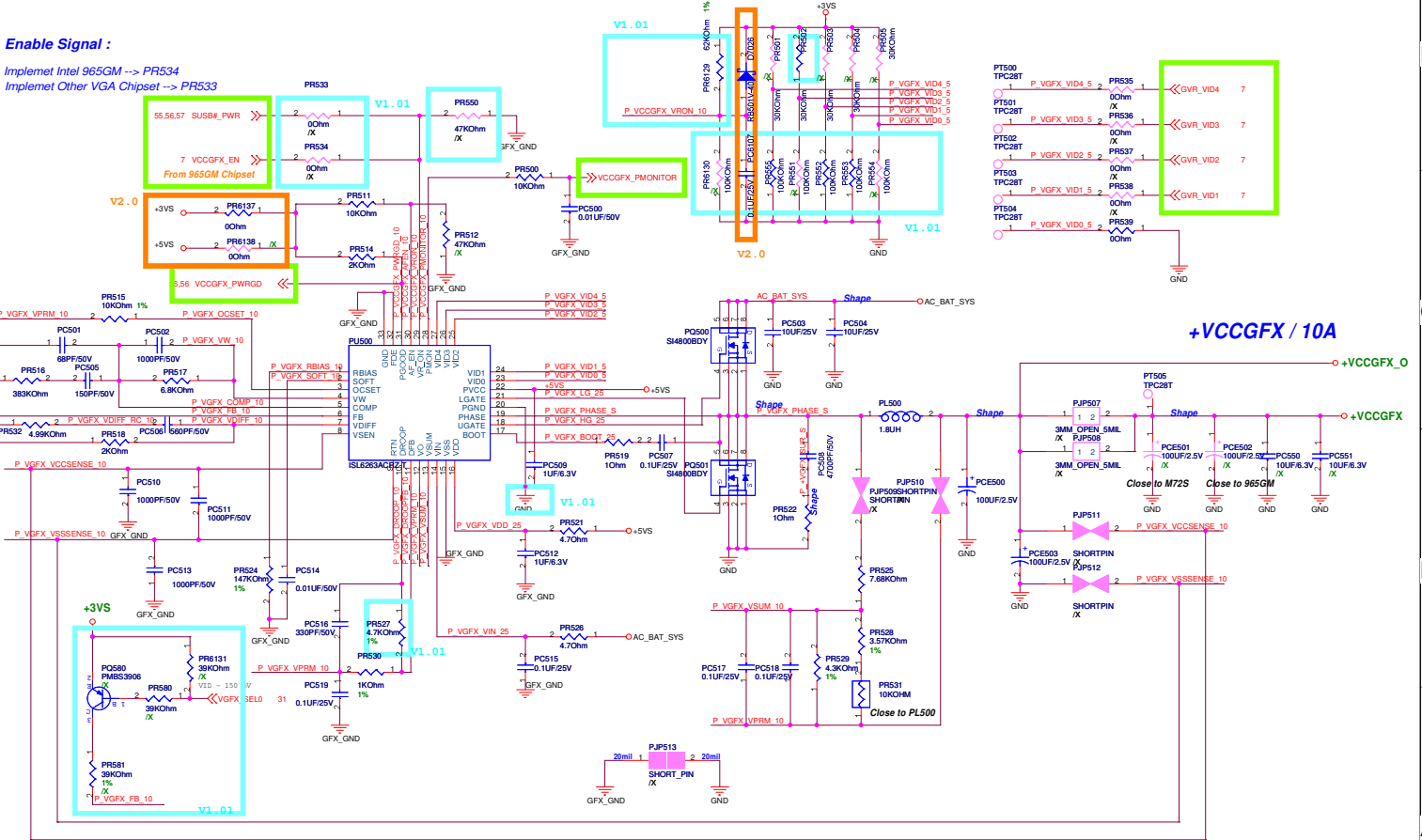


DDR Power Rev:1.00
 <Variant Name>
 **Title :**
Engineer:
 <OrigName>
 Size | Project Name | Rev
 A3 | | 2.00
 Date: 5/15/2007 | Sheet 62 of 69

<< Kennedy_Zhang >>

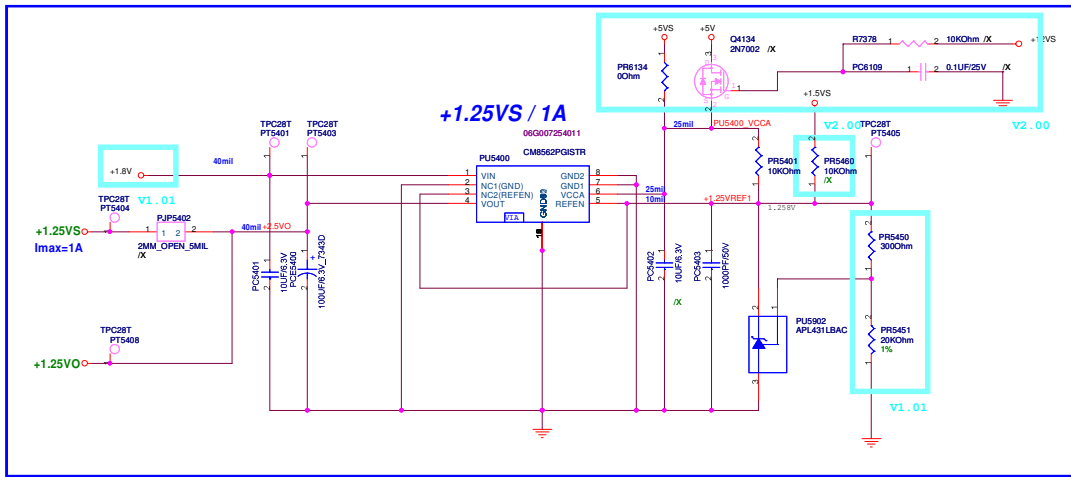
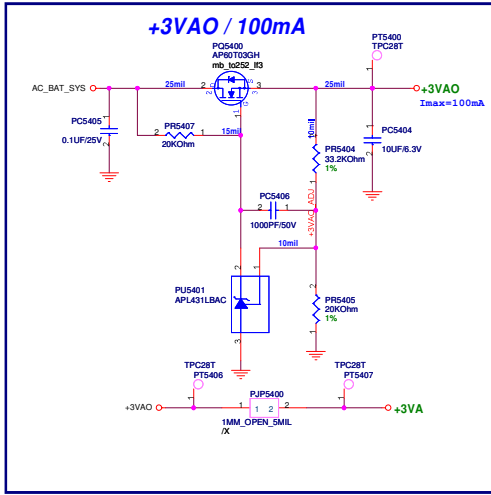
Enable Signal :

Implemet Intel 965GM -> PR534
Implemet Other VGA Chipset -> PR533



ASUS
ASUSTek COMPUTER Inc.
Title : <Title>
Engineer: Winnie Chen
Size Project Name
262E
Date: 8/16/2007 Sheet 83 of 89

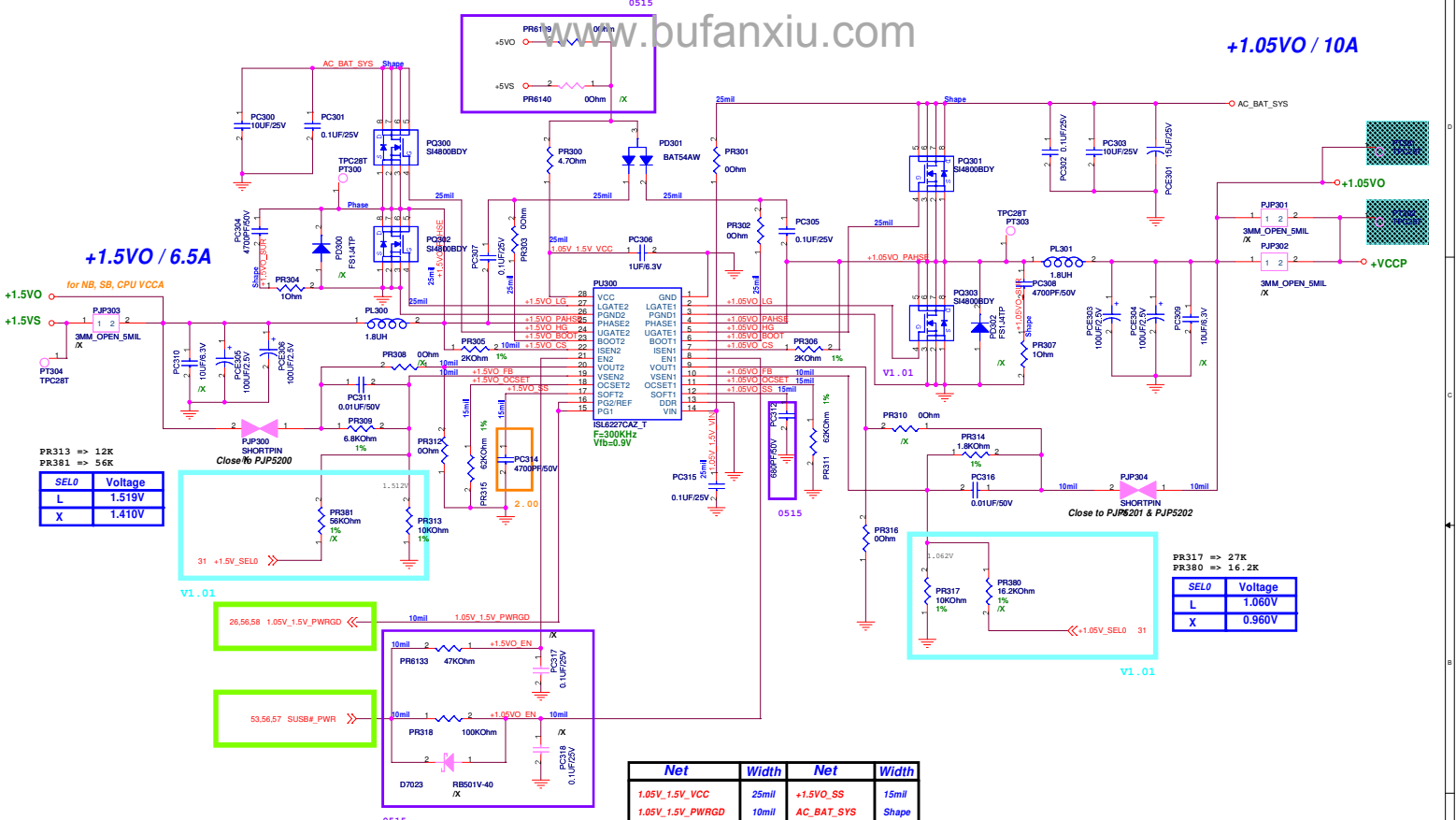
<< Kennedy_Zhang >>



<Variant Name>

ASUS		Title : POWER_IQ_+3VA & +2.5V	
ASUSTek Computer INC.		Engineer:	
Site	Project Name	Rev	
Custom	284J	2.00	
Date: 8/15/2007		Sheet	54 of 59

<< Kennedy_Zhang >>



SEL0	Voltage
L	1.519V
X	1.410V

SEL0	Voltage
L	1.519V
X	1.410V

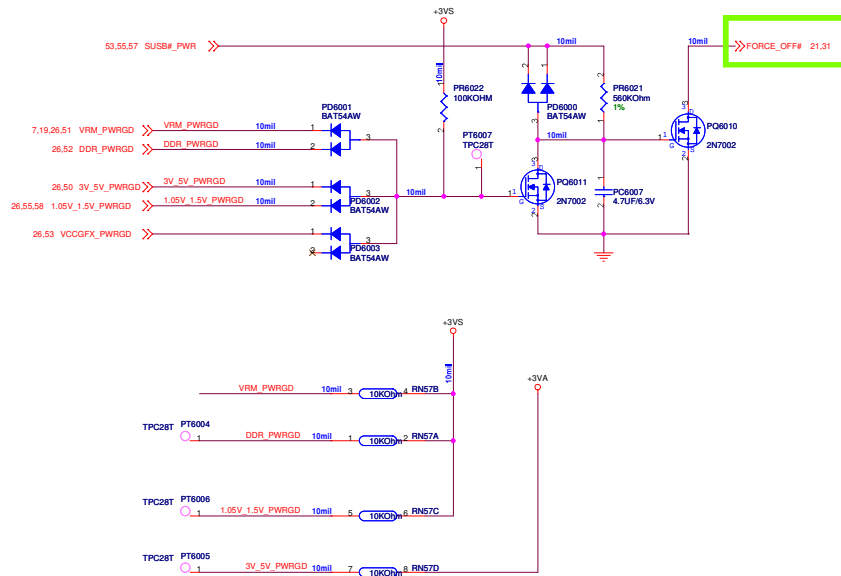
SEL0	Voltage
L	1.060V
X	0.960V

Net	Width	Net	Width
+1.05V_1.5V_VCC	25mil	+1.5V_SS	15mil
+1.05V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
+1.05V_1.5V_VIN	25mil	+1.05V_EN	10mil
+1.5V_EN	10mil	+1.05V_LG	25mil
+1.5V_LG	25mil	+1.05V_HG	25mil
+1.5V_HG	25mil	+1.05V_PHASE	Shape
+1.5V_PHASE	Shape	+1.05V_BOOT	25mil
+1.5V_BOOT	25mil	+1.05V_MODSEL	10mil
+1.5V_MODSEL	10mil	+1.05V_CS	10mil
+1.5V_CS	10mil	+1.05V_FB	10mil
+1.5V_FB	10mil	+1.05V_OCSET	25mil
+1.5V_OCSET	15mil	+1.05V_SS	15mil
+1.5V_SUR	Shape	+1.05V_SUR	Shape

ASUS
ASUSTeK COMPUTER INC
Title: POWER_ID_1.5V & 1.05V
Engineer:
Date: 2007.11.15
Sheet: 55 of 58

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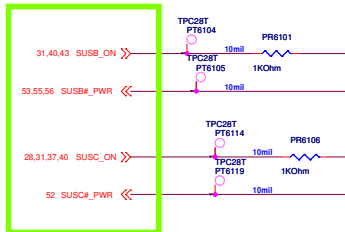
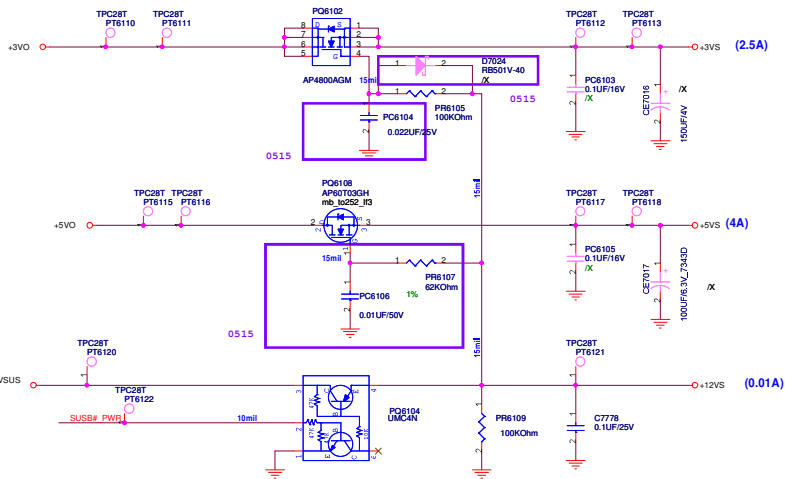
Power Good Detector



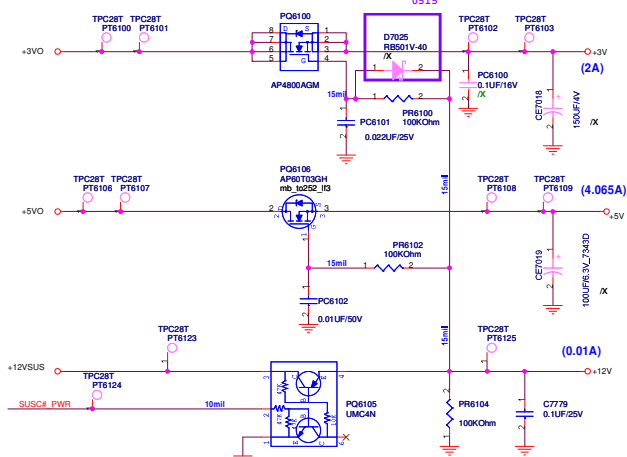
« Kennedy_Zhang »

<Variant Name>		ASUS		Title : POWER_PROTECT
ASUSTek Computer INC.		Engineer:		
Size	Project Name	Rev		
Custom	Z62E	2.0G		
Date: 8/11	11.15.2007	Sheet	56	of 58

SUSB#_PWR POWER



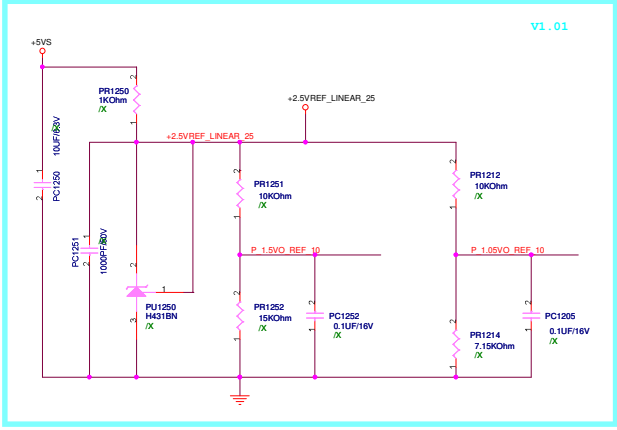
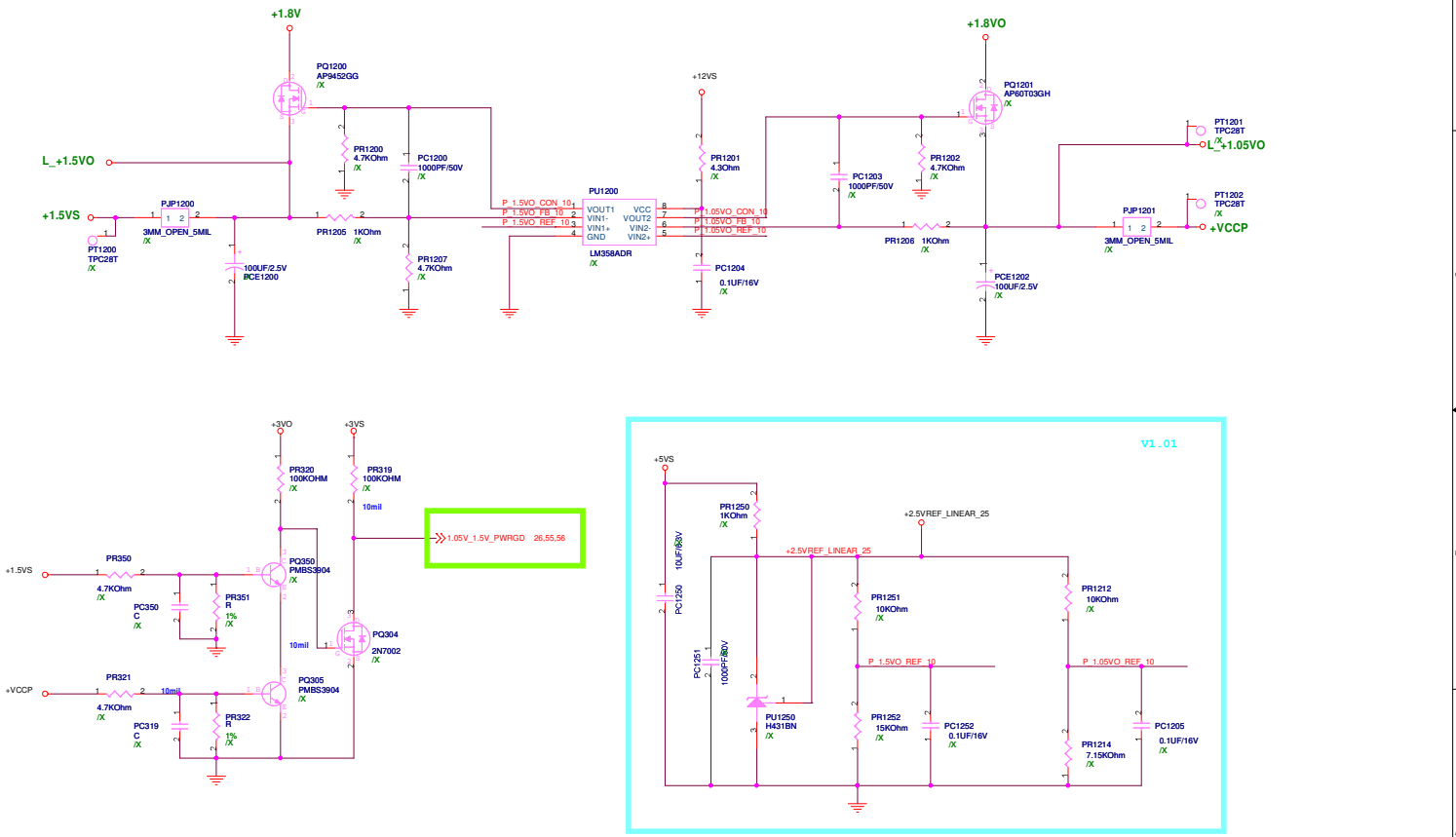
SUSC#_PWR POWER



<Variant Name>

ASUS		Title : POWER_LOAD SWITCH
ASUSTek Computer INC.		Engineer:
Size	Project Name	Rev
Custom	Z62E	2.00
Date: 8/11/15	2007	Sheet 57 of 58

« Kennedy_Zhang »



Title : POWER_I/O_DDR & VTT	
Engineer:	
Size	Project Name
Custom	298S
Date: 2007.11.15	Sheet 58 of 58

« Kennedy_Zhang »

<Variant Name>		
		Title : History(1)
ASUSTek COMPUTER INC		Engineer: Mike Lee
Site	Project Name	Rev
Custom	Z62E	2.00
Date: 05/15/2007	Sheet 59 of 59	

« Kennedy_Zhang »