Z94Rp

Rev.1.2

Yonah/RC410ME/IXP450 BLOCK DIAGRAM

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03	Yonah CPU(2)
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06	RC410ME A-LINK (2)
07	RC410ME DDR2 I/F (3)
08	RC410ME VIDEO I/F (4)
09	RC410ME POWER (5)
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15	DDR2 DIMMs
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31	USB/LED/TP
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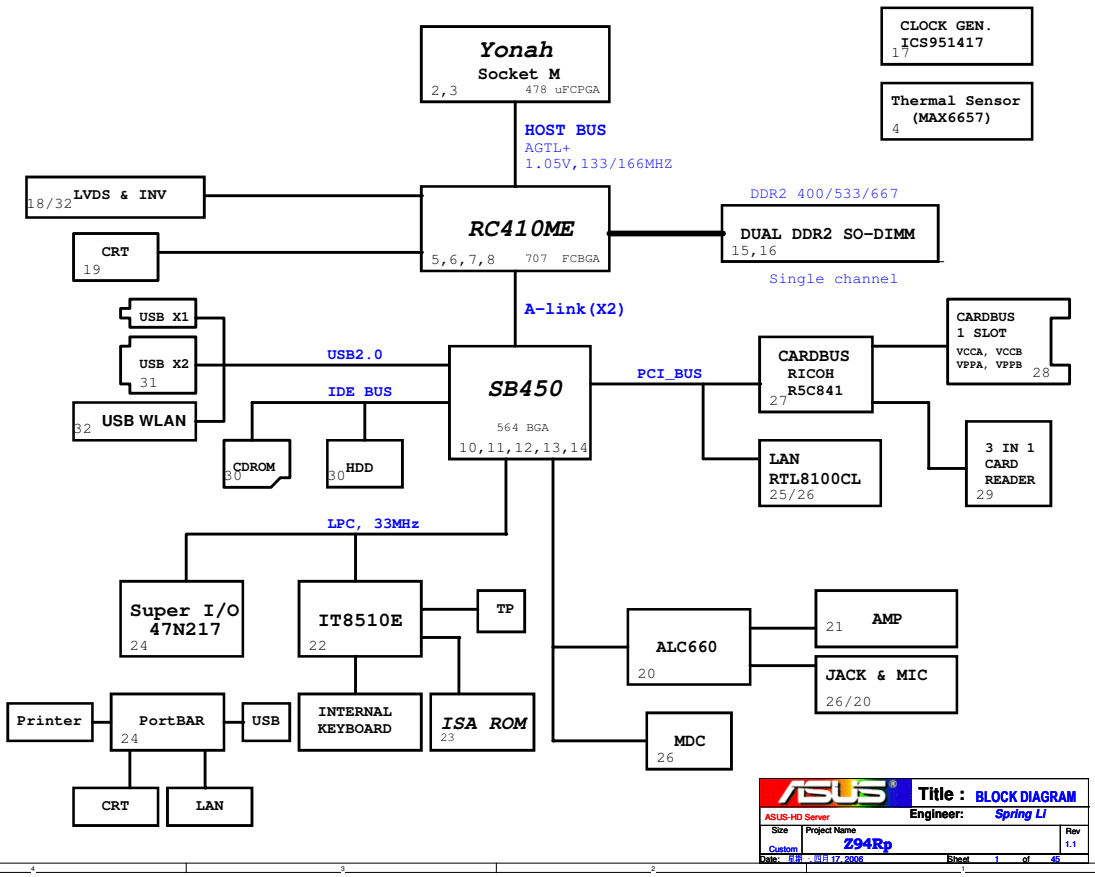
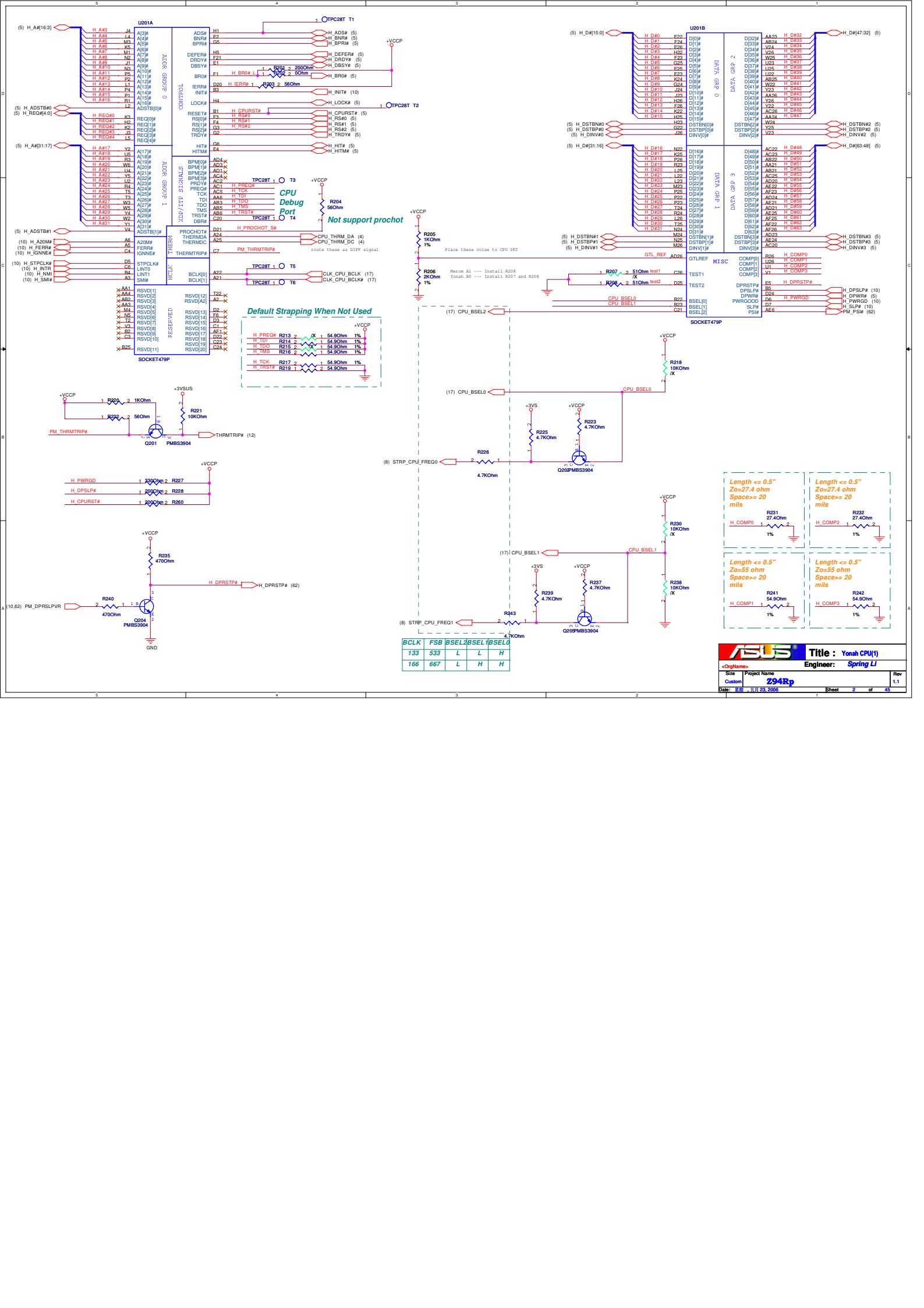
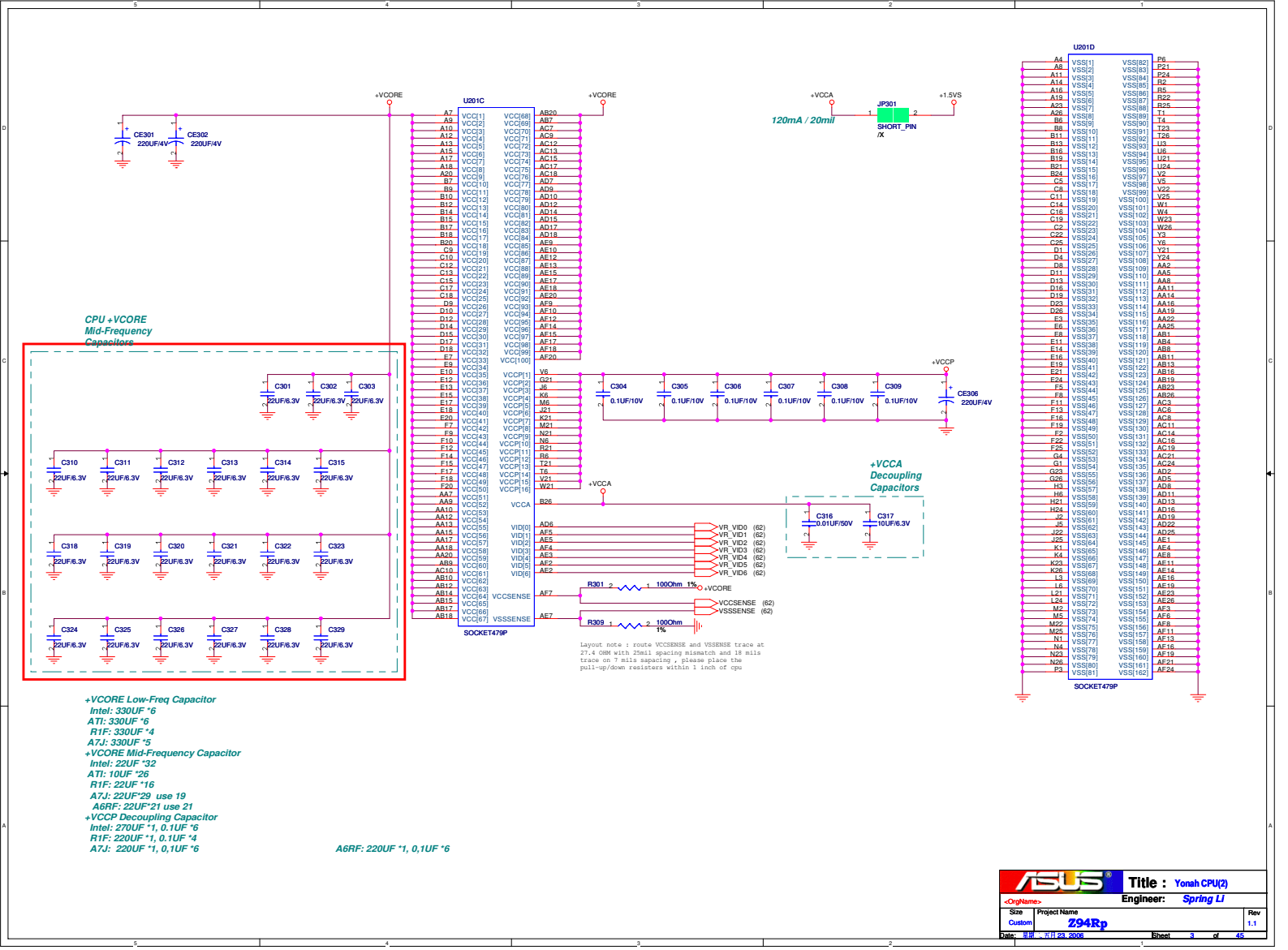
35	System Resource
61	Power-SEQUENCE
62	Power-VCORE
63	Power-3VSUS/5VSUS
64	Power-1.8VSUS/1.2VS
65	Power-VCCP/1.5VS/0.9VS
66	Power-BAT
67	Power-CHARGE
68	Power-POWER LIMIT/AC-BAT DETECT
69	Power-LOAD SWITCH
70	Power Block Diagram
**	
**	



ASUS-HD Server		Title :	BLOCK DIAGRAM
		Engineer:	Spring LI
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期一 四月 17, 2006		Sheet 1 of 45	


U201A
U201B
SOCKET479P
CPU Debug Port
Not support prochot
Default Strapping When Not Used
Q201 PMBS3904
Q202 PMBS3904
Q204 PMBS3904
Q205 PMBS3904
Length <= 0.5" Zo=27.4 ohm Space>= 20 mils
Length <= 0.5" Zo=55 ohm Space>= 20 mils
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : Yonah CPU(1)
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 2 of 45



+VCORE Low-Freq Capacitor
Intel: 330UF *6
ATI: 330UF *6
R1F: 330UF *4
A7J: 330UF *5
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
ATI: 10UF *26
R1F: 22UF *16
A7J: 22UF*29 use 19
A6RF: 22UF*21 use 21
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4
A7J: 220UF *1, 0,1UF *6

A6RF: 220UF *1, 0,1UF *6

ASUS	Title : Yonah CPU(2)		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 六月 23, 2006	Sheet 3 of 45		

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

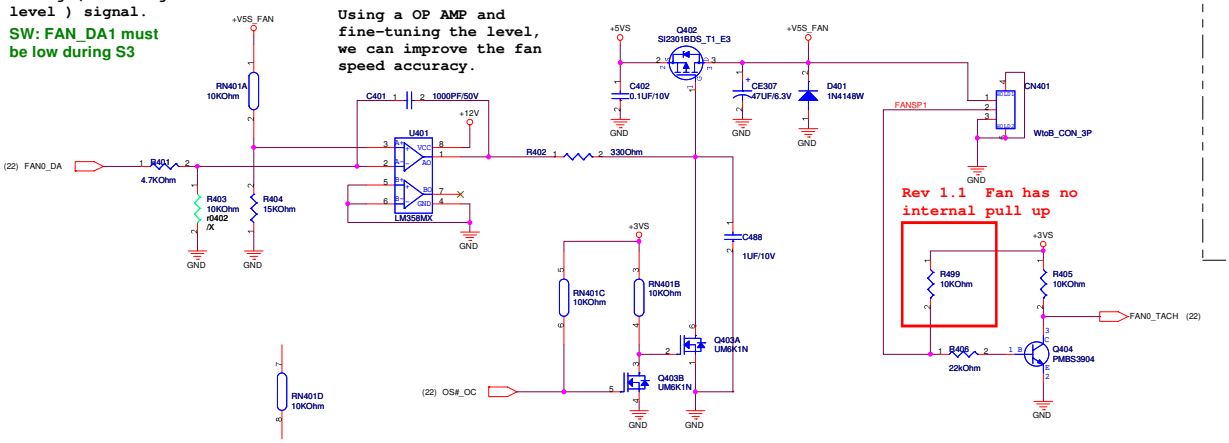
SW: FAN_DA1 must be low during S3

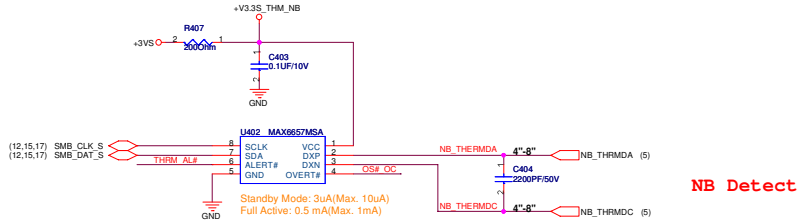
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

Route H_THERMDA and H_THERMDC on the same layer

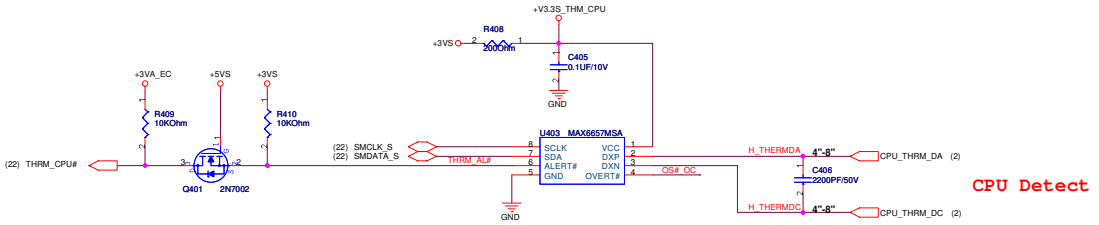
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power





NB Detect



CPU Detect

ASUS

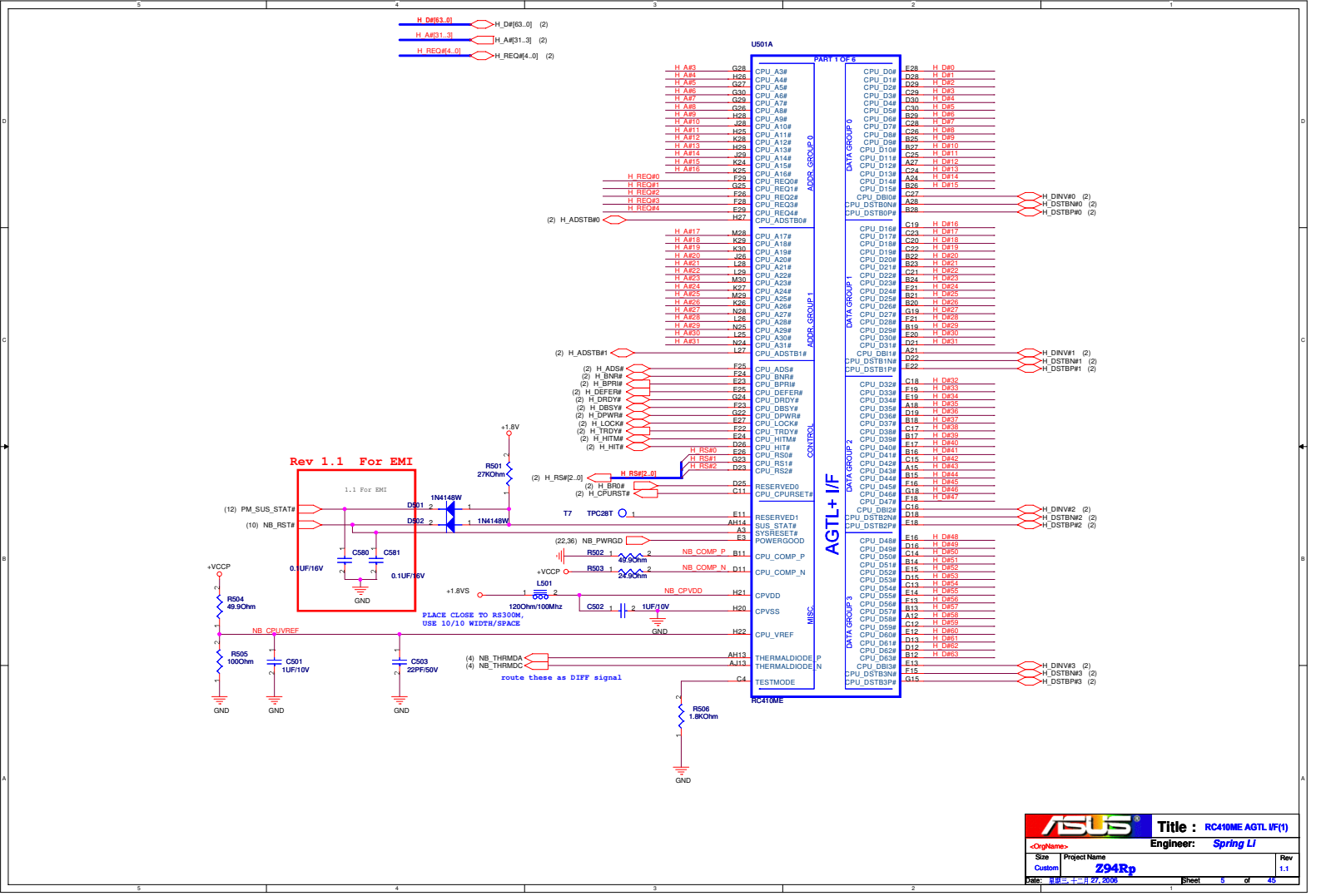
Title : THERMAL SERSOR,FAN

<OrgName>

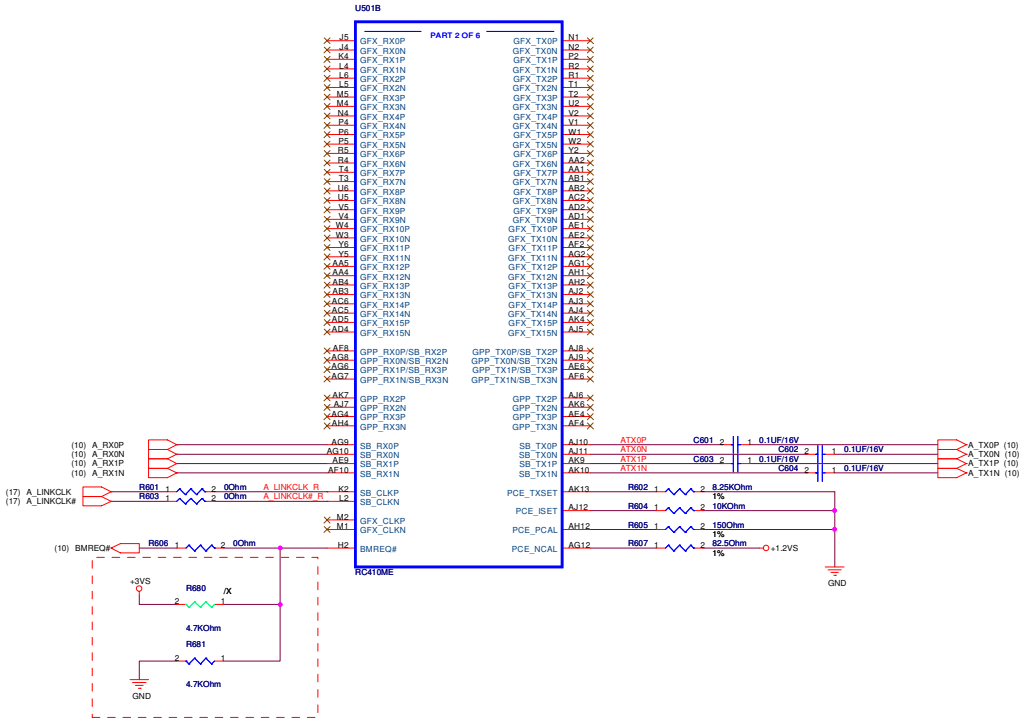
Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

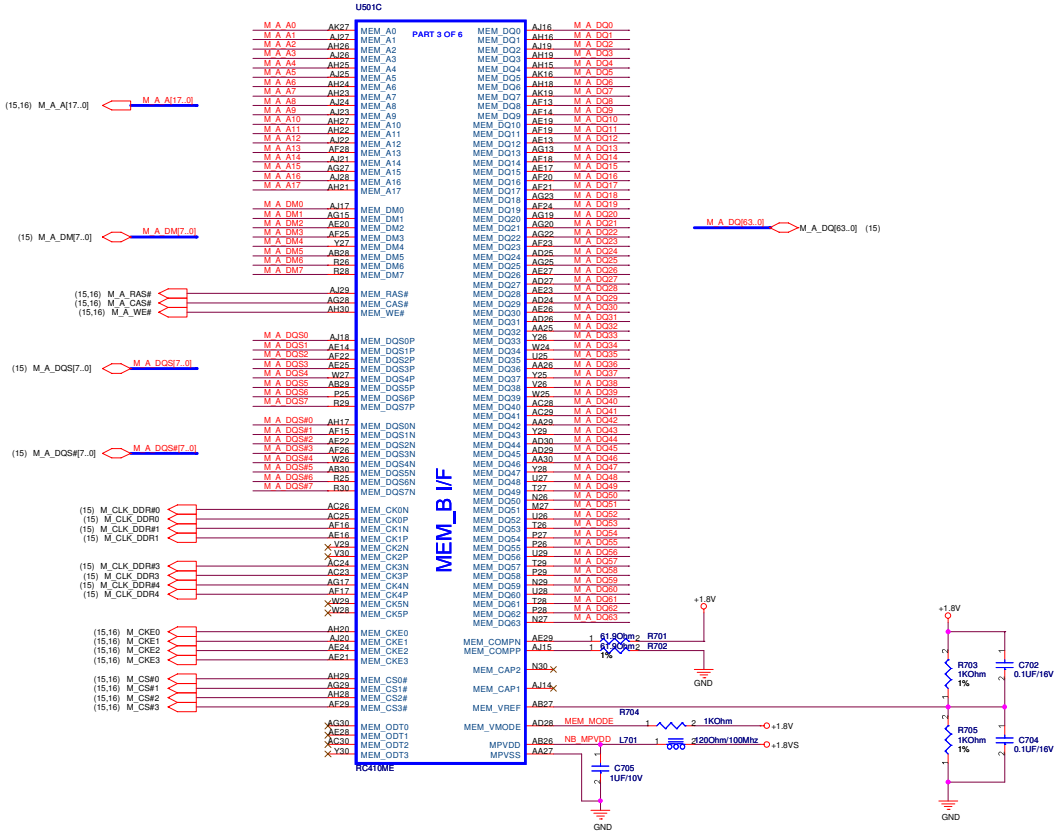
Date: 星期二, 五月 23, 2006 Sheet 4 of 45



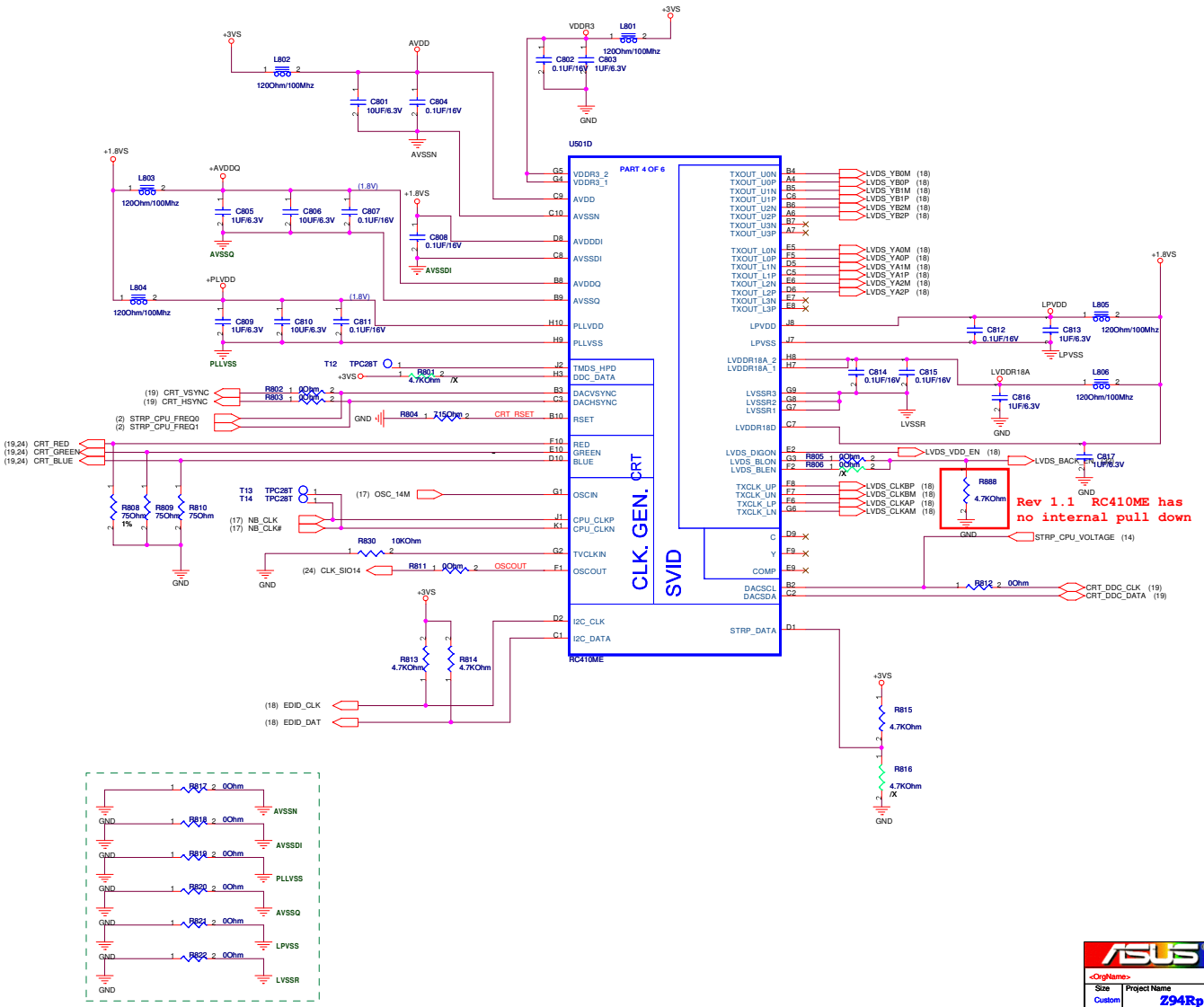
Title : RC410ME AGTL I/F(1)			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期三, 十一月 27, 2006	Sheet 5	of 45	



<OrgName>	Title : RC410ME PCIE & A-Link(2)		
	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期一, 十一月 27, 2006	Sheet 6 of 45		



<OrgName>	Title : RC410ME DDR2 I/F (3)		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期二, 十一月 27, 2006	Sheet 7 of 45		


U501D
PART 4 OF 6
CLK. GEN. CRT
SVID
RC410ME
Rev 1.1 RC410ME has no internal pull down
Title : RC410ME VIDEO I/F (4)
Engineer: Spring Li
Z94Rp
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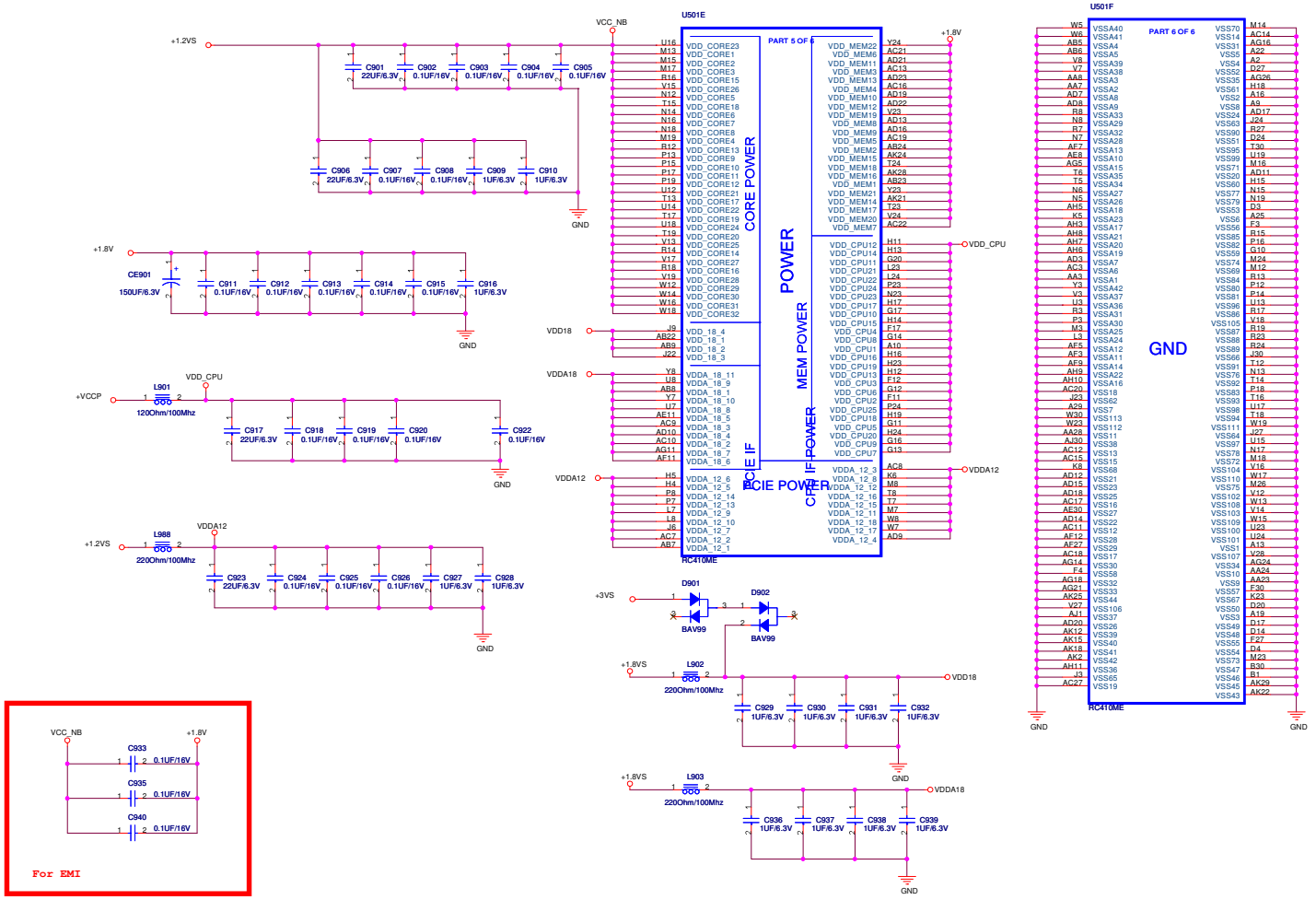
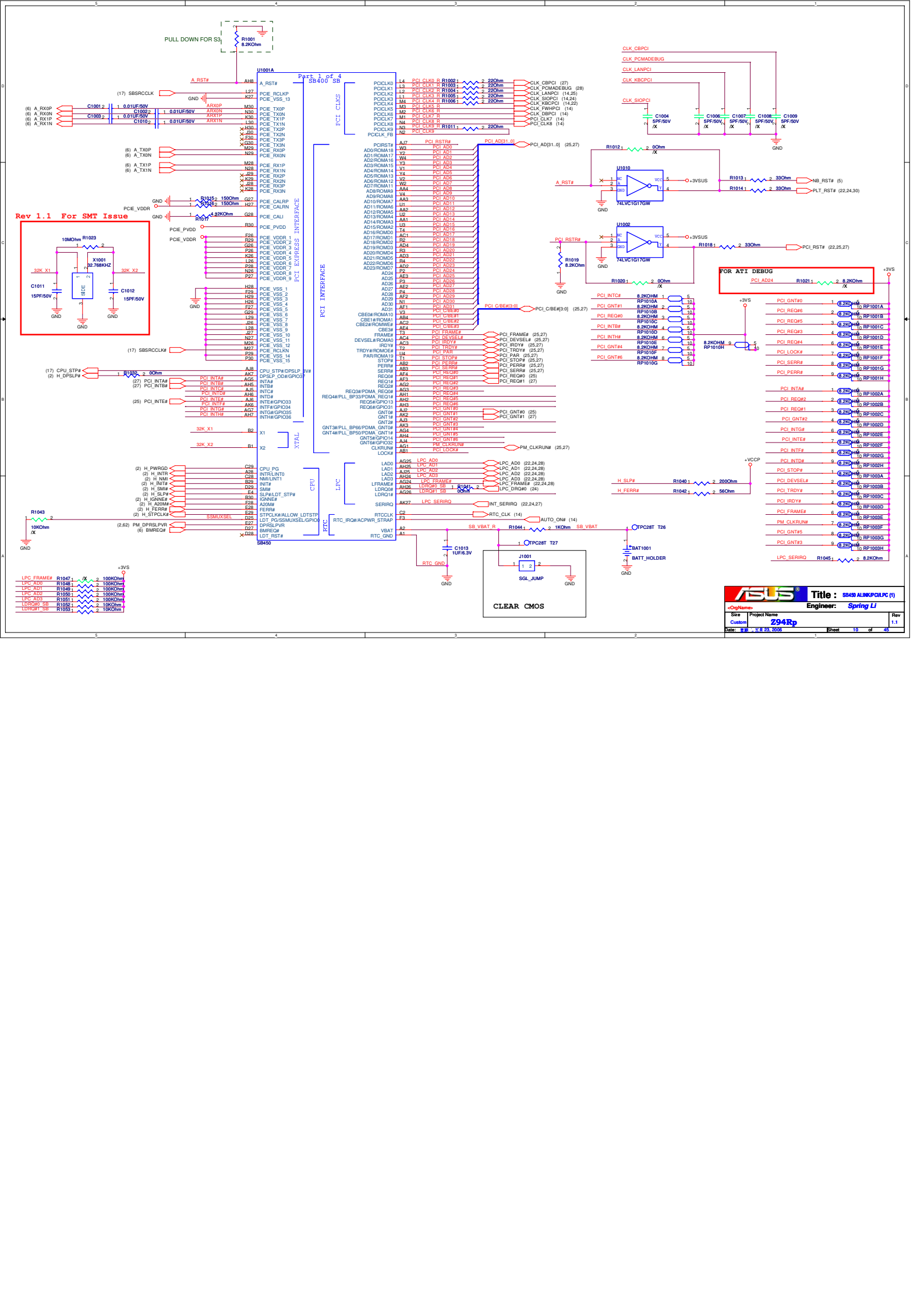
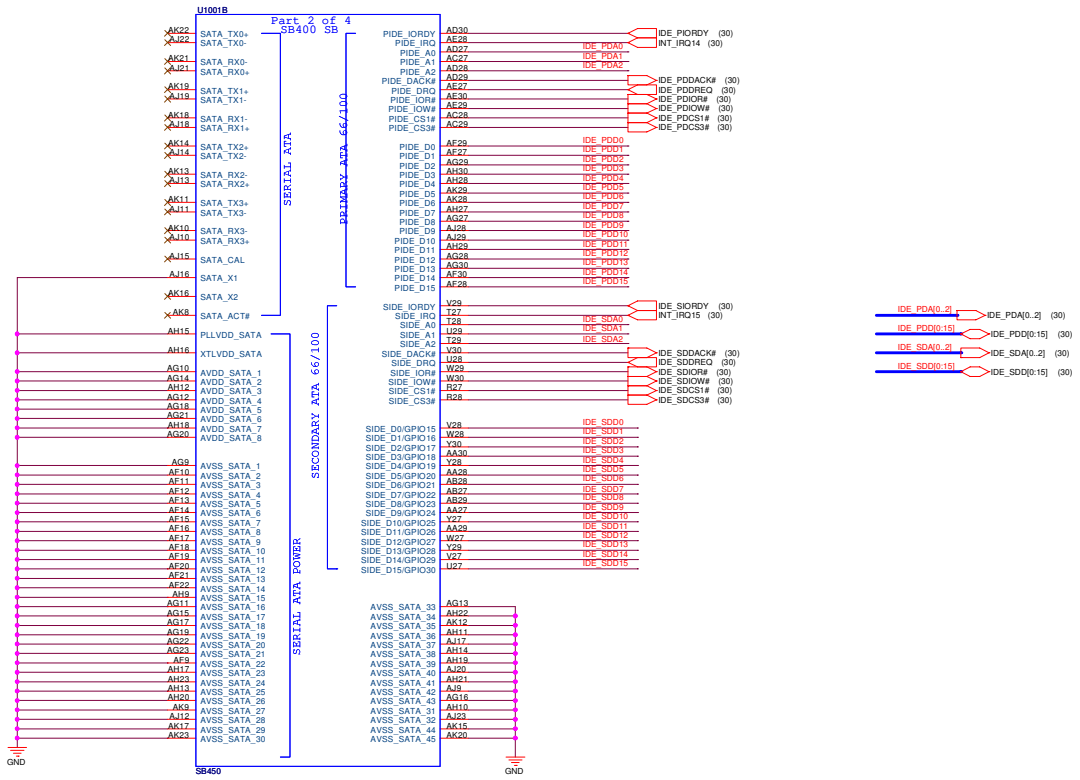
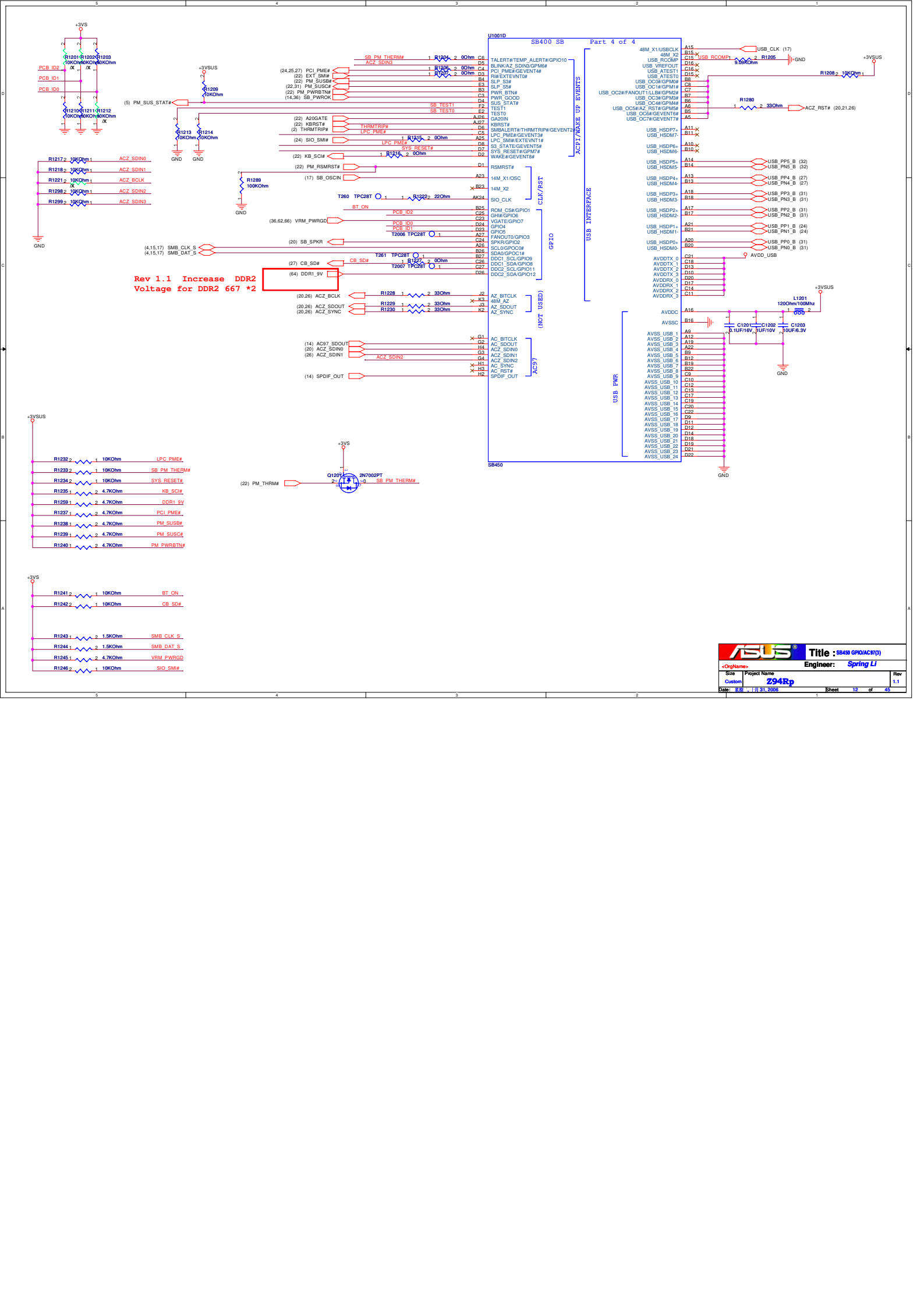


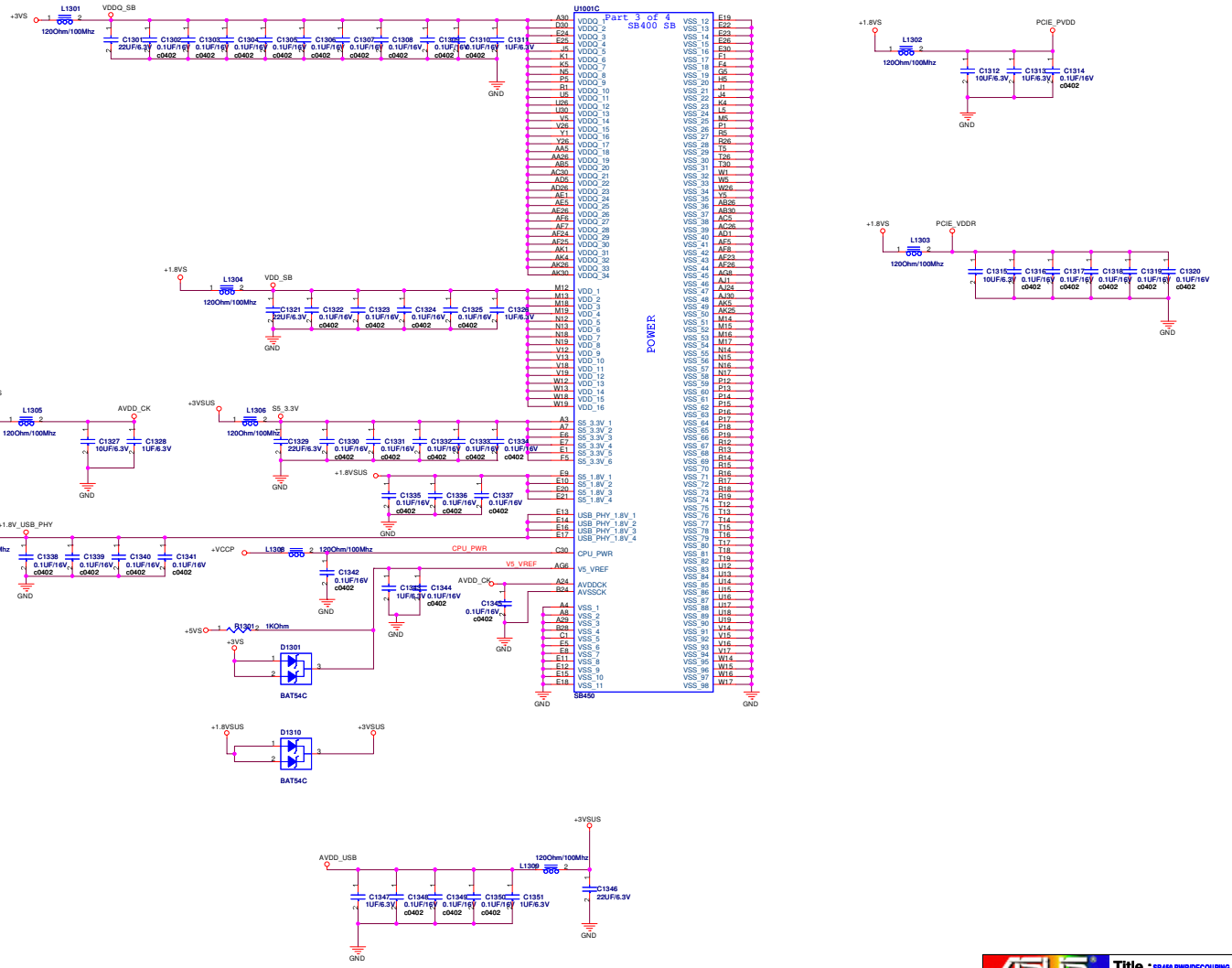
Title :	RC410ME POWER (5)		
<OrgName>		Engineer:	Spring LI
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期一, 十一月 27, 2006		Sheet 9 of 45	


PULL DOWN FOR S3
R1001 8.2KOhm
U1001A
Part 1 of 4
SB400 SB
A_RST#
PCI CLKS
PCI INTERFACE
PCI EXPRESS INTERFACE
XTAL
CPU
LPC
RTC
SB450
Rev 1.1 For SMT Issue
10MOhm R1023
X1001 32.768KHZ
32K_X1
32K_X2
C1011 15PF/50V
C1012 15PF/50V
SIDE
CLK_CBPCI
CLK_PCMADEBUG
CLK_LANPCI
CLK_KBCPCI
CLK_SIOPCI
C1004 5PF/50V /X
C1006 5PF/50V /X
C1007 5PF/50V /X
C1008 5PF/50V /X
C1009 5PF/50V /X
U1010
U1002
74LVC1G17GW
+3VSUS
NB_RST# (5)
PLT_RST# (22,24,30)
PCI_RST# (22,25,27)
FOR ATI DEBUG
PCI_AD24
+3VS
+VCCP
PCI_AD[31..0] (25,27)
PCI_C/BE#[3:0] (25,27)
PCI_FRAME# (25,27)
PCI_DEVSEL# (25,27)
PCI_IRDY# (25,27)
PCI_TRDY# (25,27)
PCI_PAR (25,27)
PCI_STOP# (25,27)
PCI_PERR# (25,27)
PCI_SERR# (25,27)
PCI_REQ#0 (25)
PCI_REQ#1 (27)
PCI_GNT#0 (25)
PCI_GNT#1 (27)
PM_CLKRUN# (25,27)
LPC_AD0 (22,24,28)
LPC_AD1 (22,24,28)
LPC_AD2 (22,24,28)
LPC_AD3 (22,24,28)
LPC_FRAME# (22,24,28)
LPC_DRQ#0 (24)
INT_SERIRQ (22,24,27)
RTC_CLK (14)
AUTO_ON# (14)
SB_VBAT
TPC28T T26
TPC28T T27
BAT1001
BATT_HOLDER
J1001
SGL_JUMP
CLEAR CMOS
GND
Title : SB450 ALINK/PCI/LPC (1)
Engineer: Spring Li
Project Name 294Rp
Size Custom
Rev 1.1
Sheet 10 of 45



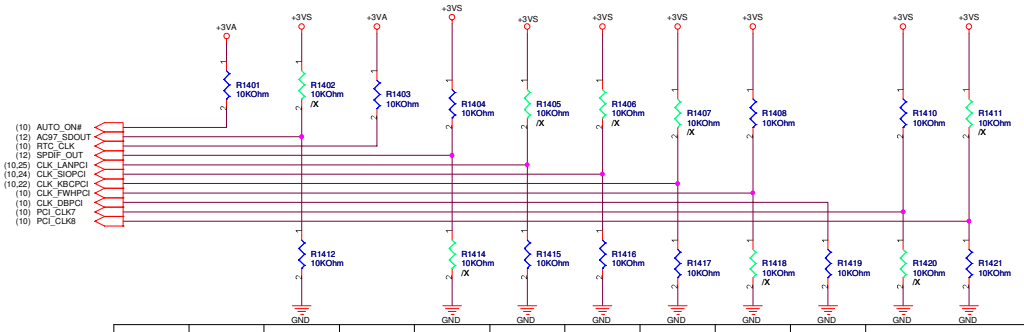
ASUS	Title : SB450 IDE (2)		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期一 十月 23, 2006	Sheet 11 of 45		


U1001D
SB400 SB
Part 4 of 4
SB450
ACPI/WAKE UP EVENTS
USB INTERFACE
CLK/RST
GPIO
(NOT USED)
AC97
USB PWR
Rev 1.1 Increase DDR2
Voltage for DDR2 667 *2
Title : SB450 GPIO/AC97(3)
Engineer: Spring Li
Project Name
Z94Rp
Rev
1.1
Sheet 12 of 45



Title :	SB450 PWR/DECOUPING
<OrgName>	Engineer: Spring Li
Size: Custom	Project Name: 294Rp
Rev: 1.1	
Date: 星期一, 六月 22, 2009	Sheet 13 of 45

REQUIRED STRAPS



	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4		

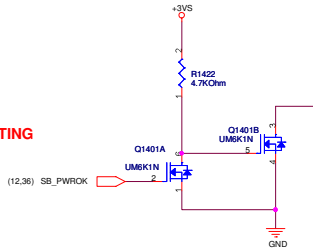
NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH



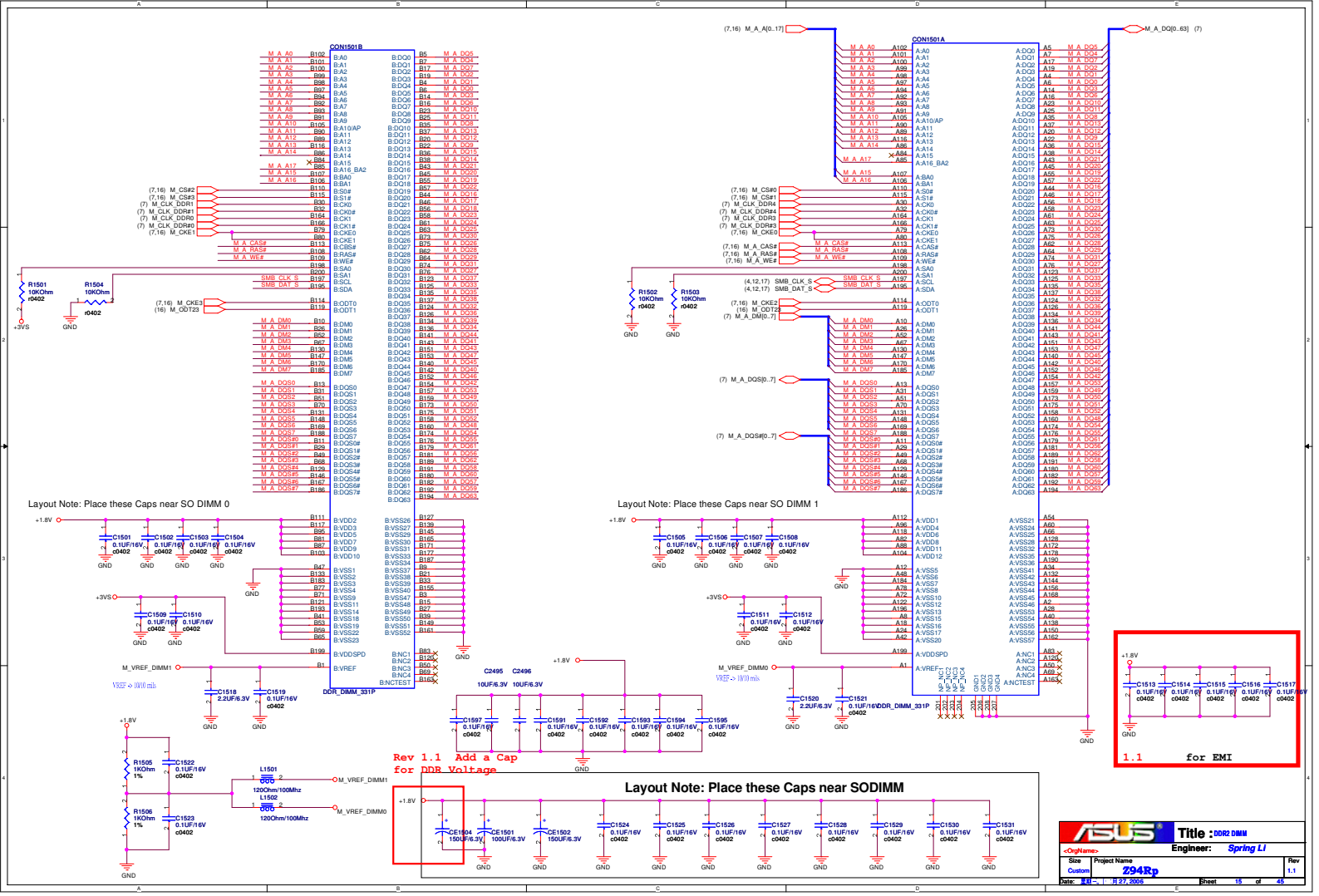
STRP_CPU_VOLTAGE: CPU VCC

0: MOBILE CPU
1: DESKTOP CPU

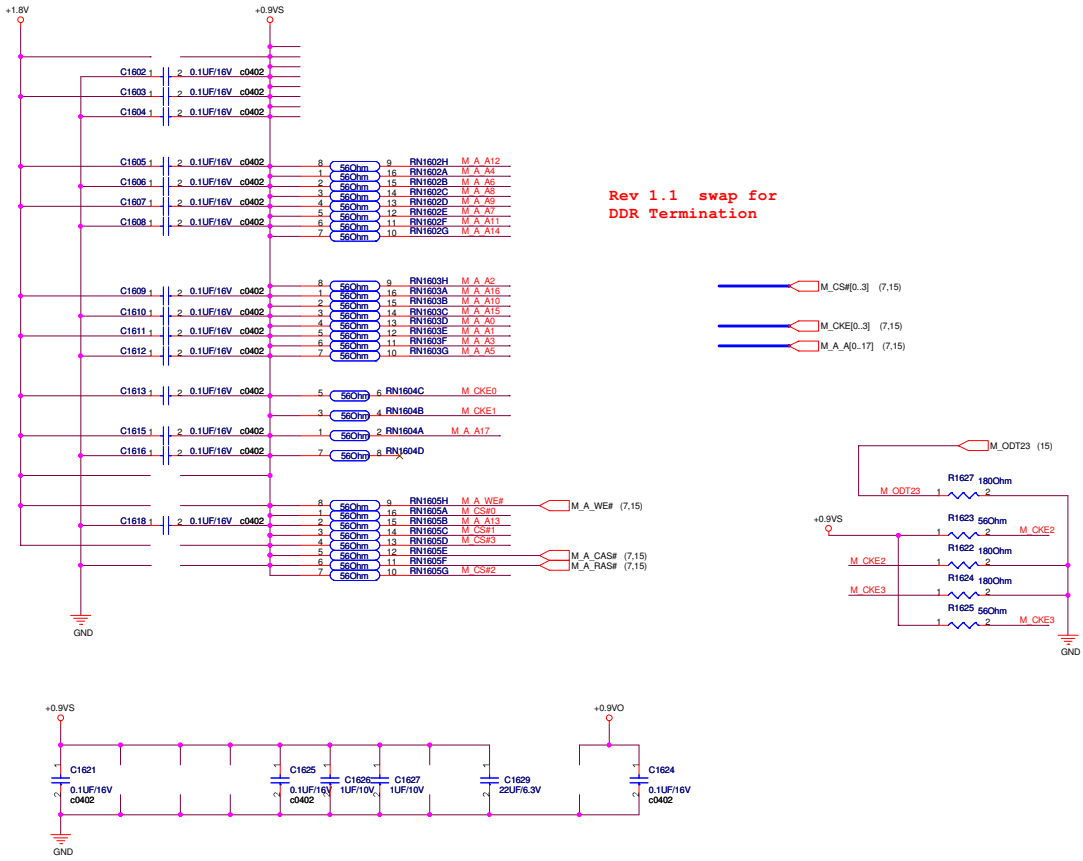
DEFAULT:0

STRP_CPU_VOLTAGE (8)

ASUS	Title : SB450 STRAPS(5)	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期一 十月 23, 2006	Sheet 14 of 45	



Title	DDR2 DIMM
Engineer	Spring Li
Size	Custom
Project Name	294Rp
Rev	1.1
Date	5 27, 2006
Sheet	15 of 45



Rev 1.1 swap for
DDR Termination

M_CS#[0..3] (7,15)
M_CKE[0..3] (7,15)
M_A_A[0..17] (7,15)

ASUS

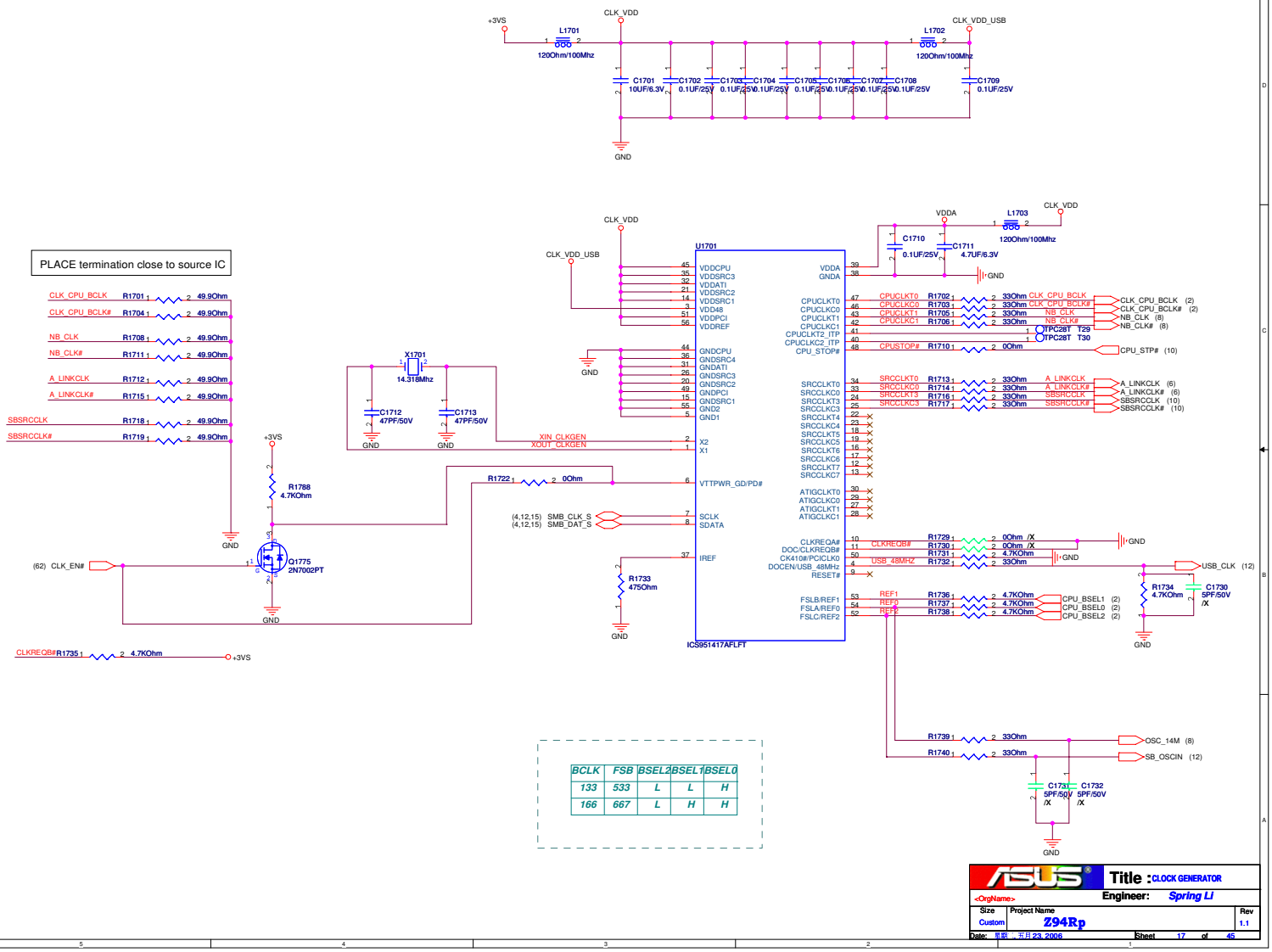
Title : DDR2 Termination

<OrgName>

Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

Date: 星期三, 十二月 27, 2006 Sheet 16 of 45



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Title : CLOCK GENERATOR

<OrgName> Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

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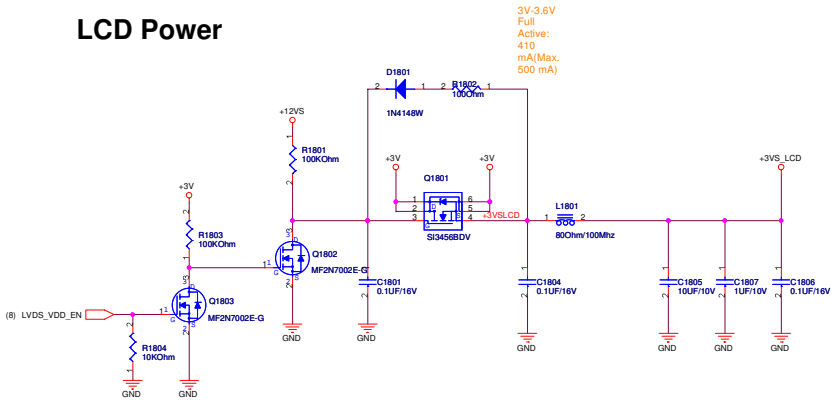
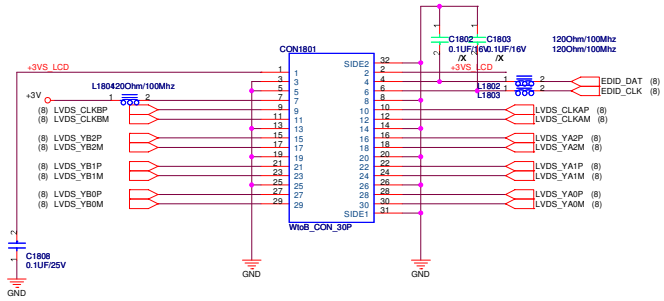
LCD Power

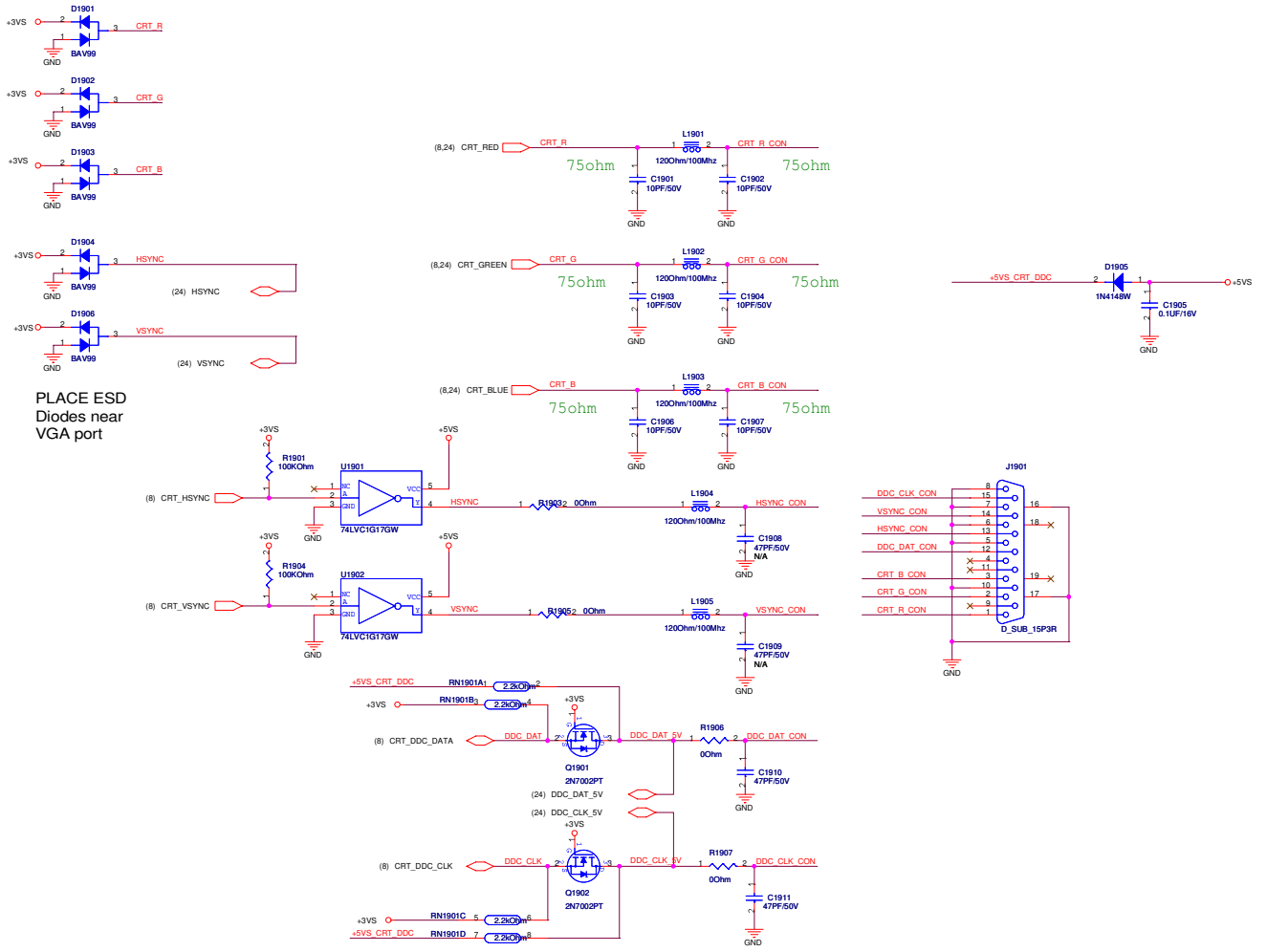




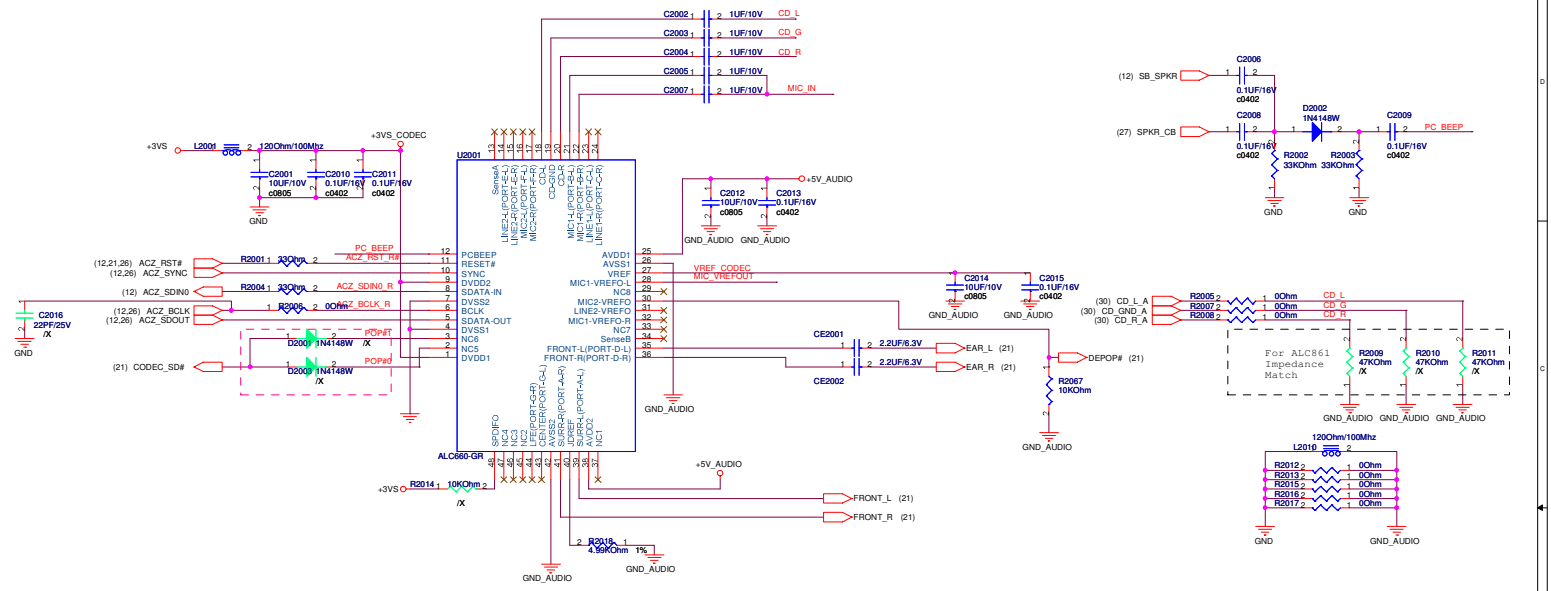
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

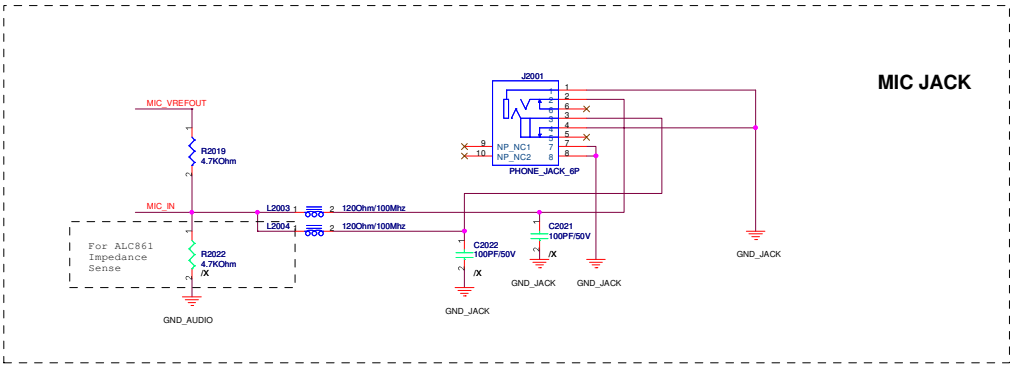
LCD LVDS Interface

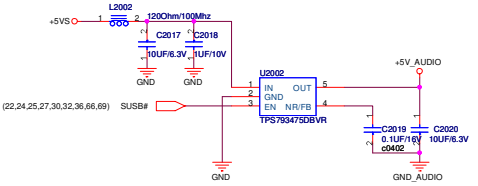
<OrgName>		Title :	LVDS & INVERTER (CAMERA)
		Engineer:	Spring LI
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 六月 23, 2009		Sheet 18 of 45	



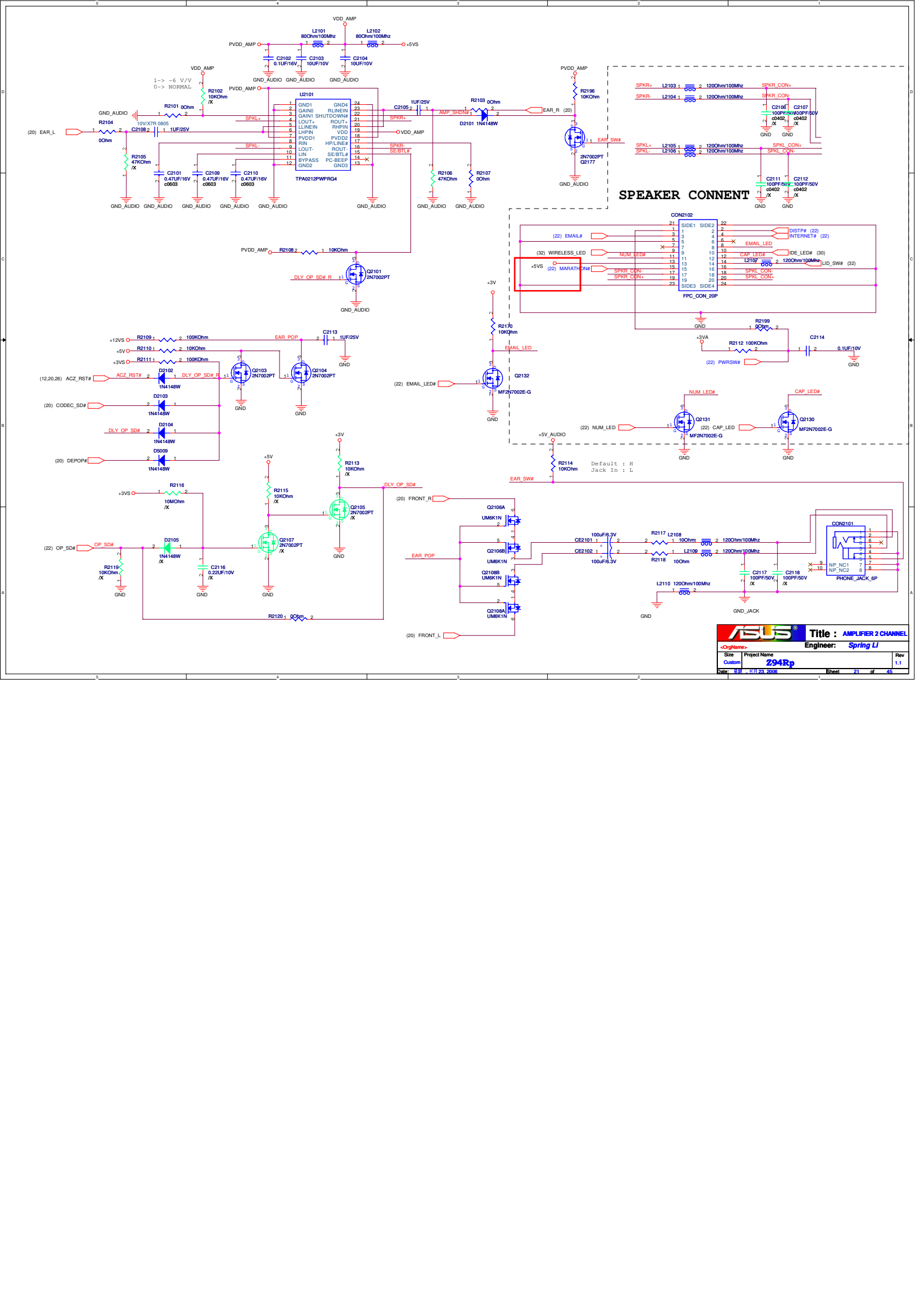
ASUS	Title : CRT CONNECTOR	
<OrgName>	Engineer: Spring LI	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期 二 六月 23, 2006	Sheet 19 of 45	







ASUS	Title : AZALIA		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 六月 23, 2009	Sheet 20 of 45		


SPEAKER CONNENT
U2101
TPA0212PWPRG4
CON2102
FPC_CON_20P
CON2101
PHONE_JACK_6P
Q2101 2N7002PT
Q2103 2N7002PT
Q2104 2N7002PT
Q2105 2N7002PT
Q2107 2N7002PT
Q2132 MF2N7002E-G
Q2131 MF2N7002E-G
Q2130 MF2N7002E-G
Q2106A UM6K1N
Q2106B UM6K1N
Q2108B UM6K1N
Q2108A UM6K1N
Q2101 1N4148W
D2102 1N4148W
D2103 1N4148W
D2104 1N4148W
D5009 1N4148W
D2105 1N4148W
Title : AMPLIFIER 2 CHANNEL
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
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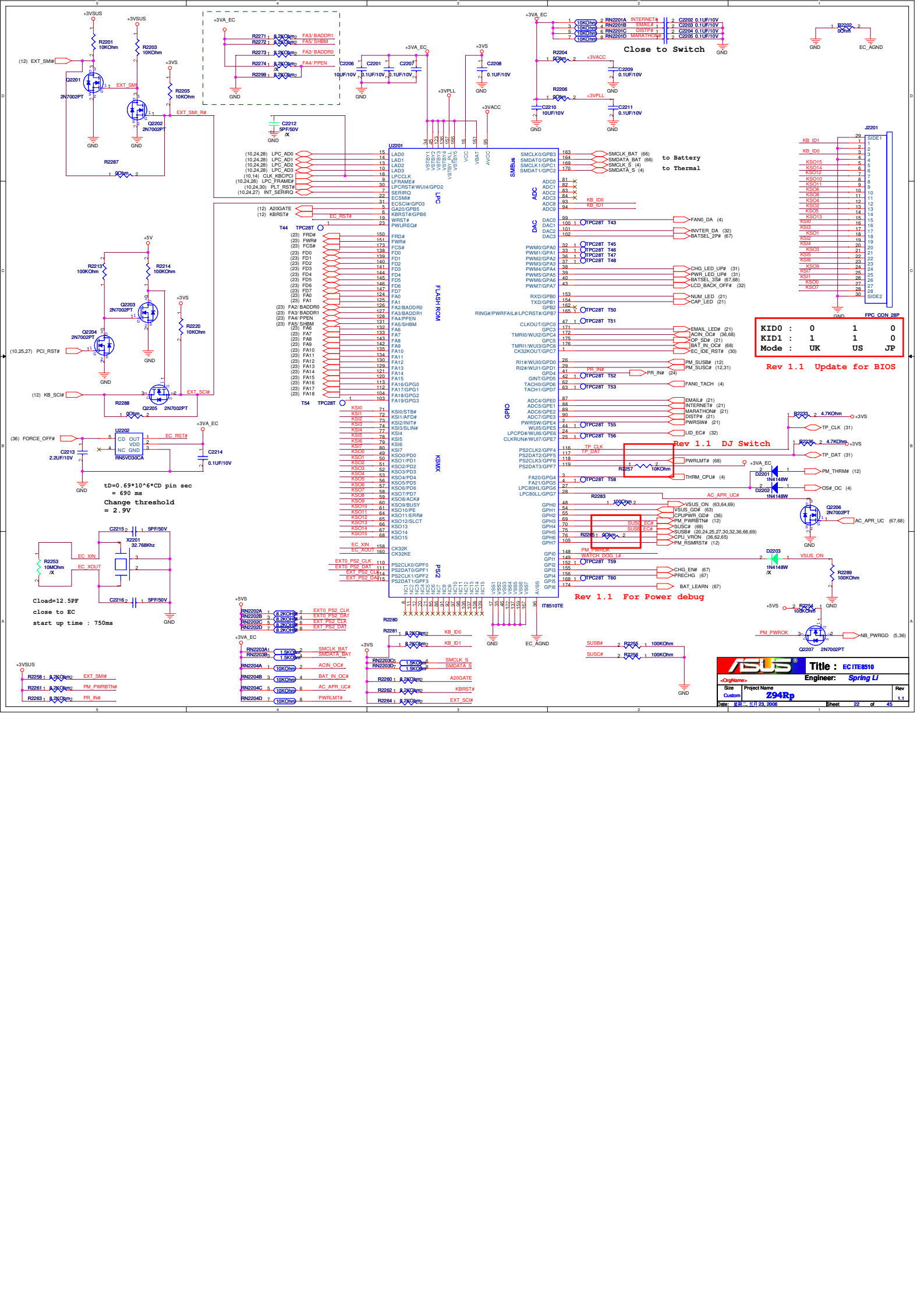
Close to Switch
Rev 1.1 Update for BIOS
KID0 : 0 1 0
KID1 : 1 1 0
Mode : UK US JP
Rev 1.1 DJ Switch
Rev 1.1 For Power debug
to Battery
to Thermal
tD=0.69*10^6*CD pin sec
= 690 ms
Change threshold
= 2.9V
Cload=12.5PF
close to EC
start up time : 750ms
Title : EC ITE8510
Engineer: Spring LI
Project Name Z94Rp
Rev 1.1
Date: 星期二, 五月 23, 2006
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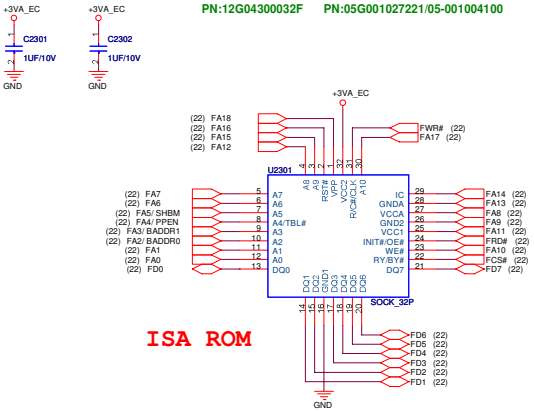
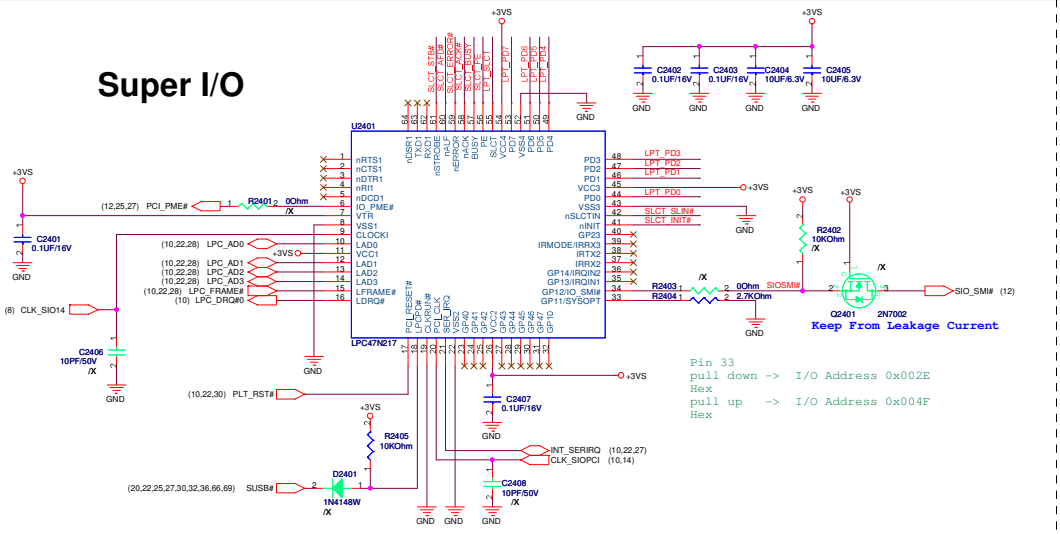
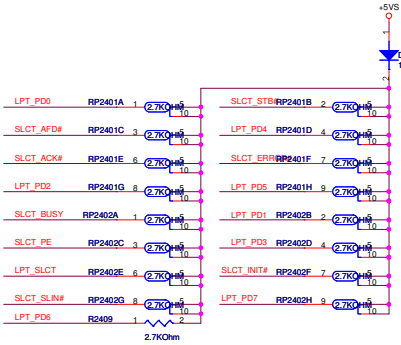
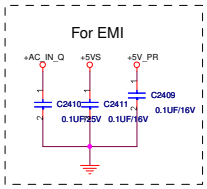


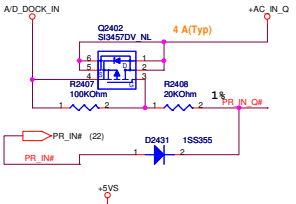
Title : ISA ROM & SPI ROM		
<OrgName>	Engineer: Spring LI	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期 二, 十月 23, 2007	Sheet 23 of 45	

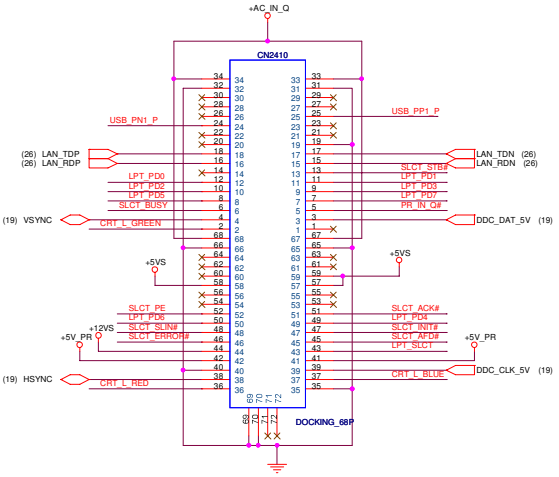
Super I/O

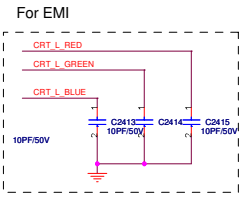


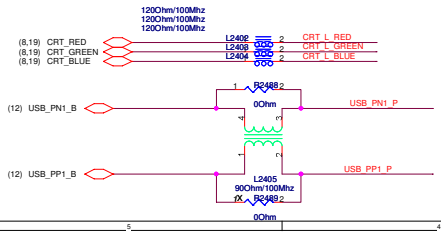




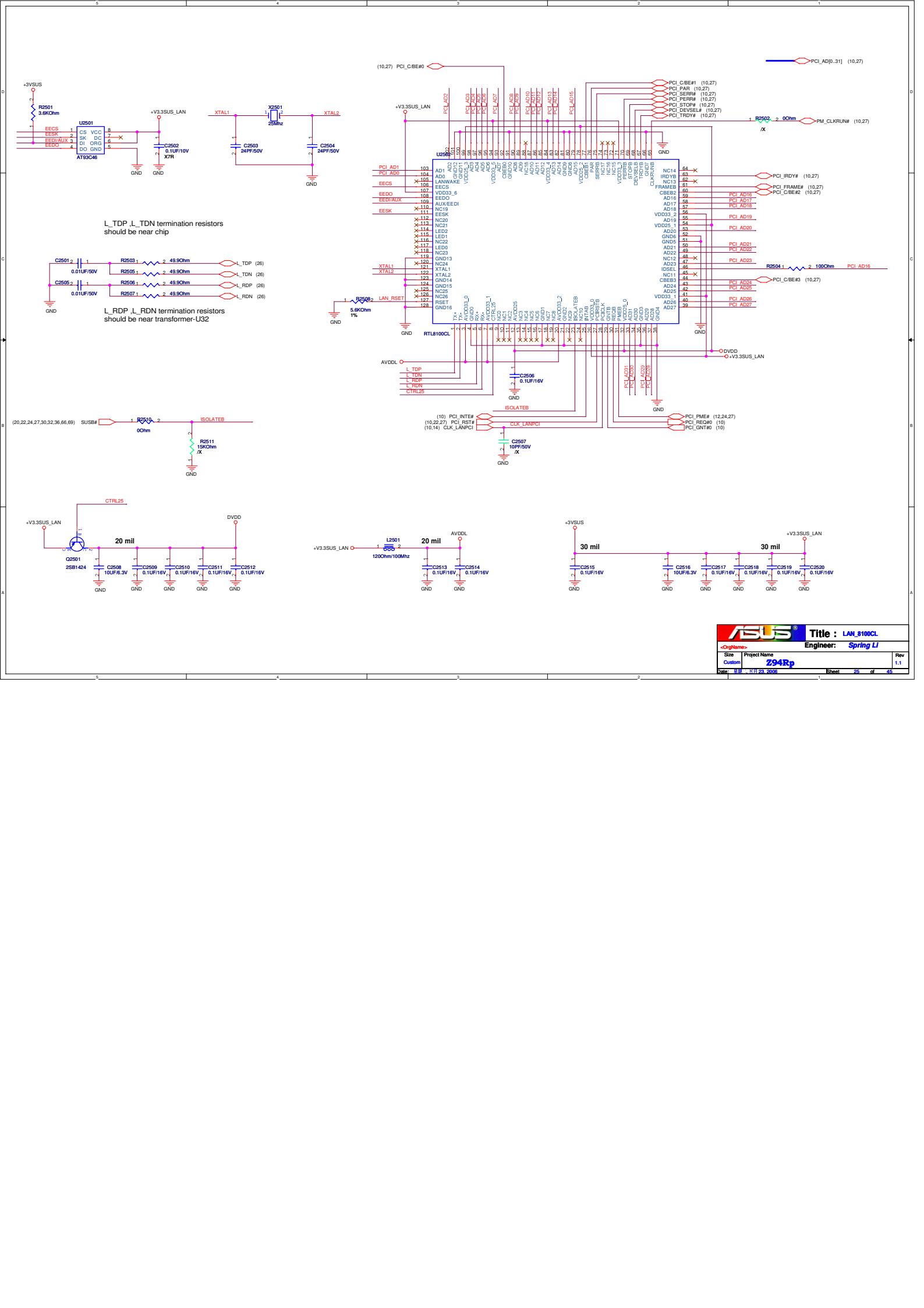






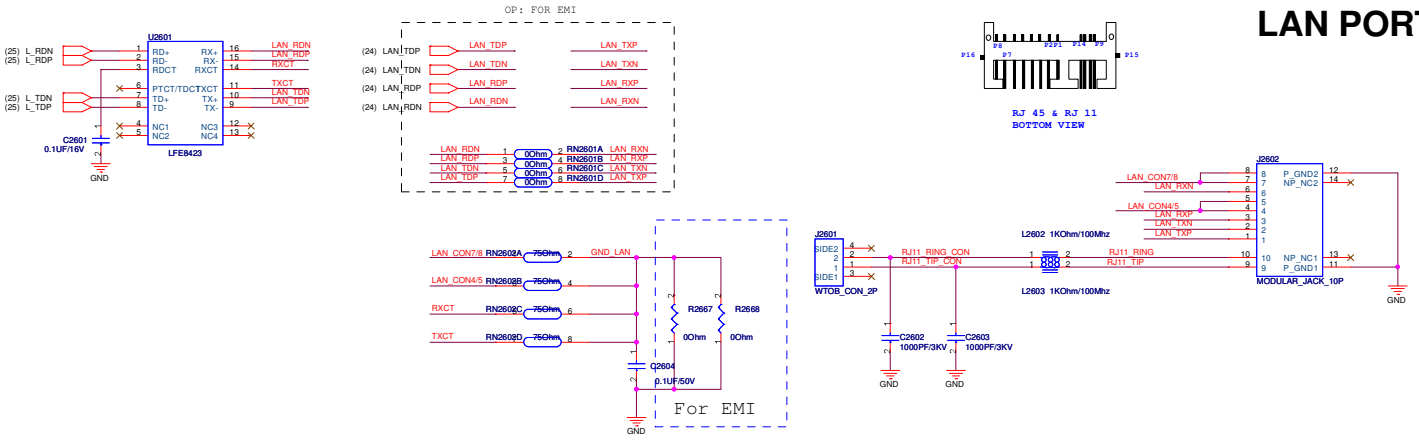


Title : Blank			
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 十月 23, 2006	Sheet 24 of 45		

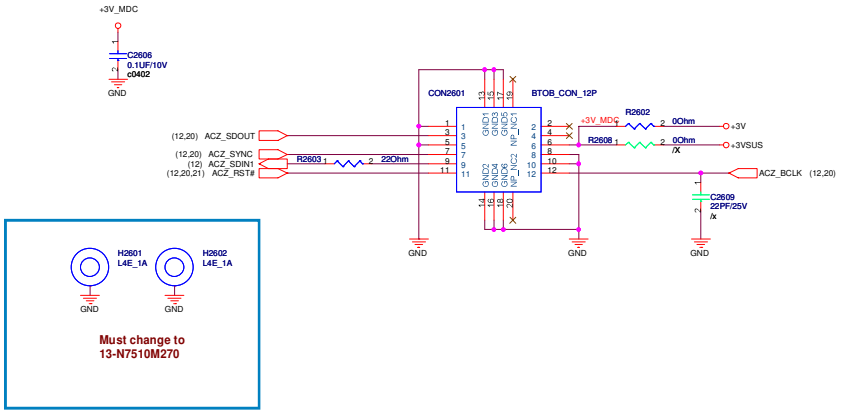


Title : LAN_8100CL		
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期 二, 十月 23, 2006	Sheet 25 of 45	

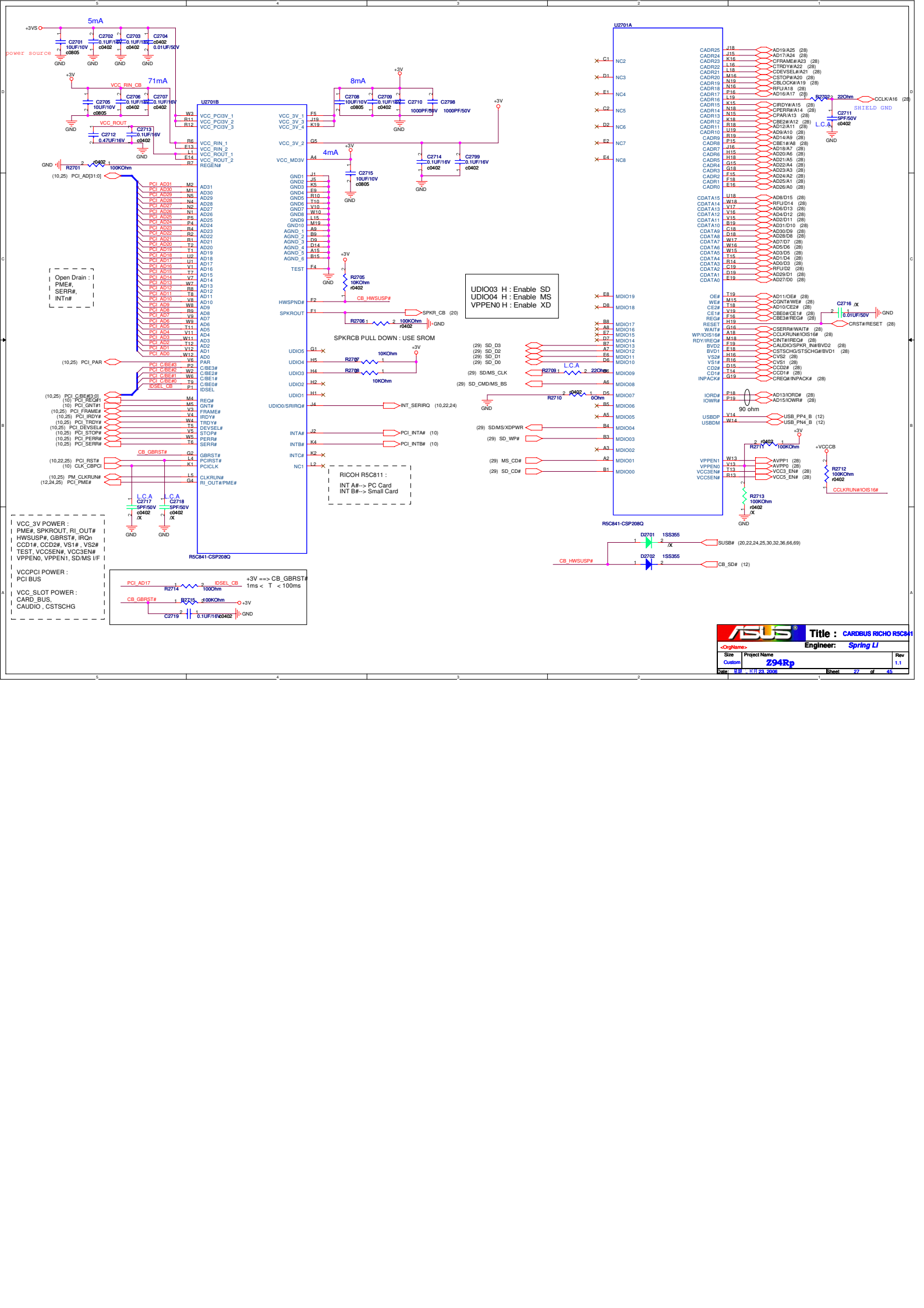
LAN PORT

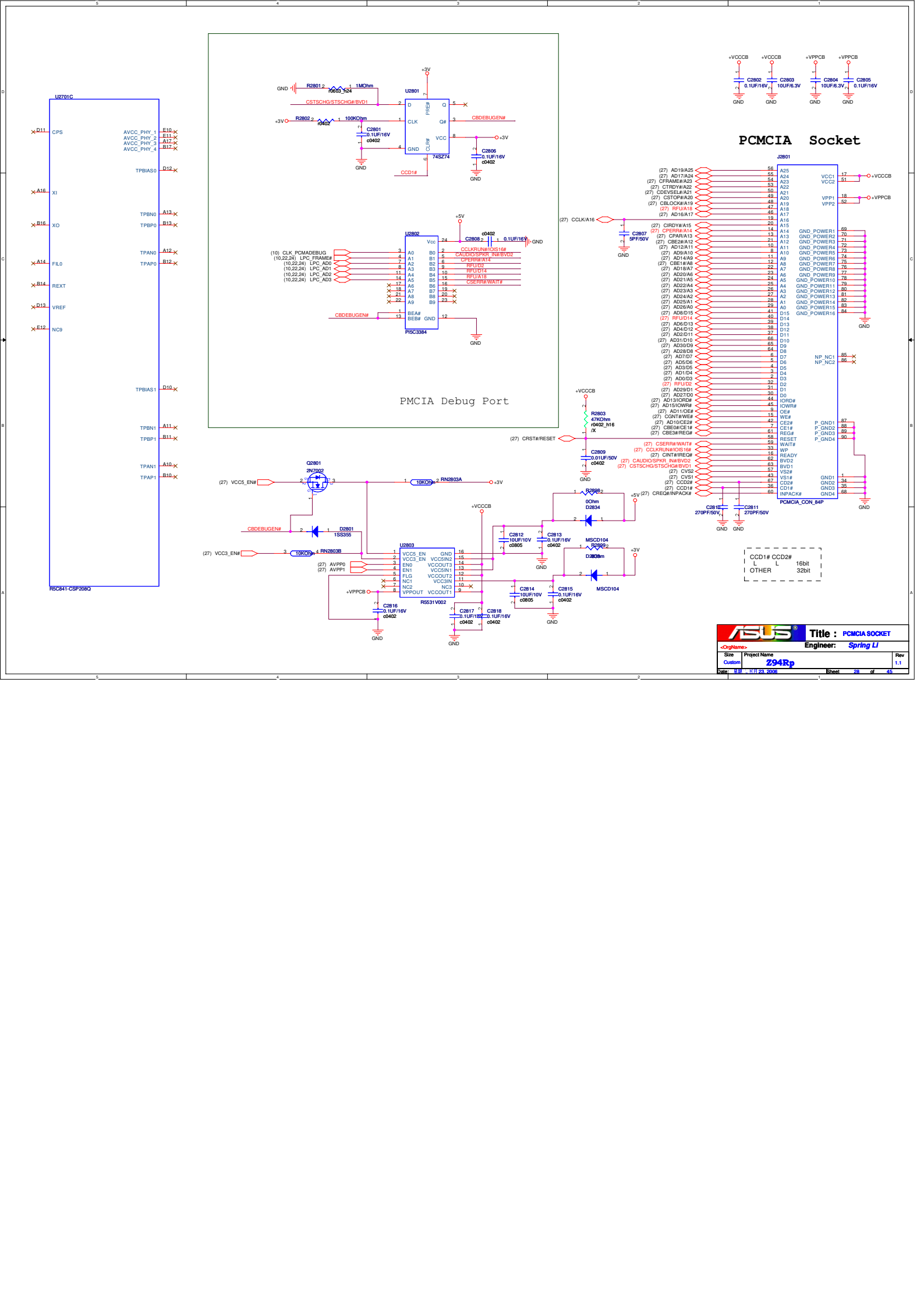


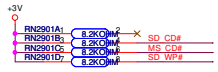
MDC



Title : RJ11+45 & MDC			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 六月 23, 2006	Sheet 26 of 45		


5mA
power source
71mA
8mA
4mA
U2701B
R5C841-CSP208Q
U2701A
R5C841-CSP208Q
Open Drain : PME#, SERR#, INTn#
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
SPKRCB PULL DOWN : USE SROM
RICOH R5C811 :
INT A#--> PC Card
INT B#--> Small Card
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
Title : CARDBUS RICHO R5C841
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 27 of 45

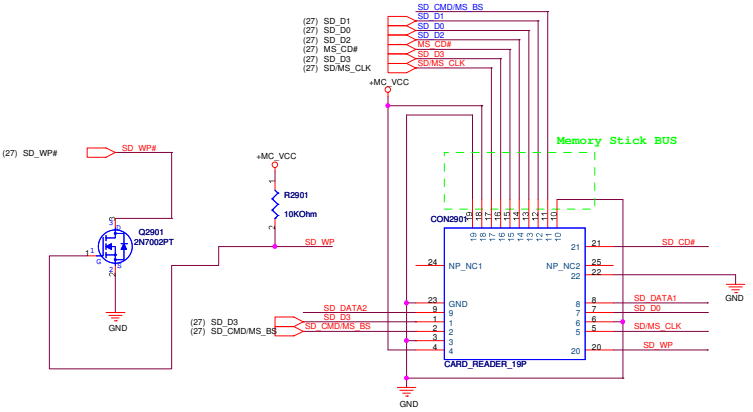

U2701C
R5C841-CSP208Q
CPS
XI
XO
FIL0
REXT
VREF
NC9
AVCC_PHY_1
AVCC_PHY_2
AVCC_PHY_3
AVCC_PHY_4
TPBIAS0
TPBN0
TPBP0
TPAN0
TPAP0
TPBIAS1
TPBN1
TPBP1
TPAN1
TPAP1
PMCIA Debug Port
R2801 1MOhm r0603_h24
CSTSCHG/STSCHG#/BVD1
R2802 100KOhm r0402
C2801 0.1UF/16V c0402
U2801
74SZ74
CBDEBUGEN#
C2806 0.1UF/16V c0402
CCD1#
U2802
PI5C3384
C2808 0.1UF/16V c0402
CCLKRUN#/IOIS16#
CAUDIO/SPKR_IN#/BVD2
CPERR#/A14
RFU/D2
RFU/D14
RFU/A18
CSERR#/WAIT#
(10) CLK_PCMADEBUG
(10,22,24) LPC_FRAME#
(10,22,24) LPC_AD0
(10,22,24) LPC_AD1
(10,22,24) LPC_AD2
(10,22,24) LPC_AD3
Q2801 2N7002
D2801 1SS355
(27) VCC5_EN#
(27) VCC3_EN#
10KOhm RN2803A
10KOhm RN2803B
U2803
R5531V002
(27) AVPP0
(27) AVPP1
C2812 10UF/10V c0805
C2813 0.1UF/16V c0402
C2814 10UF/10V c0805
C2815 0.1UF/16V c0402
C2816 0.1UF/16V c0402
C2817 0.1UF/16V c0402
C2818 0.1UF/16V c0402
MSCD104
R2808 0Ohm D2834
R2809 0Ohm D2838
C2807 5PF/50V
C2809 0.01UF/50V c0402
R2803 47KOhm r0402_h16 /X
(27) CRST#/RESET
C2810 270PF/50V
C2811 270PF/50V
C2802 0.1UF/16V
C2803 10UF/6.3V
C2804 10UF/6.3V
C2805 0.1UF/16V
PCMCIA Socket
J2801
PCMCIA_CON_84P
(27) CCLK/A16
(27) AD19/A25
(27) AD17/A24
(27) CFRAME#/A23
(27) CTRDY#/A22
(27) CDEVSEL#/A21
(27) CSTOP#/A20
(27) CBLOCK#/A19
(27) RFU/A18
(27) AD16/A17
(27) CIRDY#/A15
(27) CPERR#/A14
(27) CPAR/A13
(27) CBE2#/A12
(27) AD12/A11
(27) AD9/A10
(27) AD14/A9
(27) CBE1#/A8
(27) AD18/A7
(27) AD20/A6
(27) AD21/A5
(27) AD22/A4
(27) AD23/A3
(27) AD24/A2
(27) AD25/A1
(27) AD26/A0
(27) AD8/D15
(27) RFU/D14
(27) AD6/D13
(27) AD4/D12
(27) AD2/D11
(27) AD31/D10
(27) AD30/D9
(27) AD28/D8
(27) AD7/D7
(27) AD5/D6
(27) AD3/D5
(27) AD1/D4
(27) AD0/D3
(27) RFU/D2
(27) AD29/D1
(27) AD27/D0
(27) AD13/IORD#
(27) AD15/IOWR#
(27) AD11/OE#
(27) CGNT#/WE#
(27) AD10/CE2#
(27) CBE0#/CE1#
(27) CBE3#/REG#
(27) CSERR#/WAIT#
(27) CCLKRUN#/IOIS16#
(27) CINT#/IREQ#
(27) CAUDIO/SPKR_IN#/BVD2
(27) CSTSCHG/STSCHG#/BVD1
(27) CVS2
(27) CVS1
(27) CCD2#
(27) CCD1#
(27) CREQ#/INPACK#
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : PCMCIA SOCKET
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 28 of 45

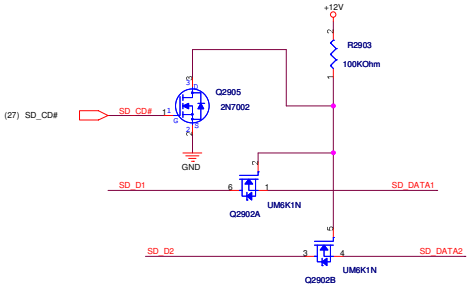


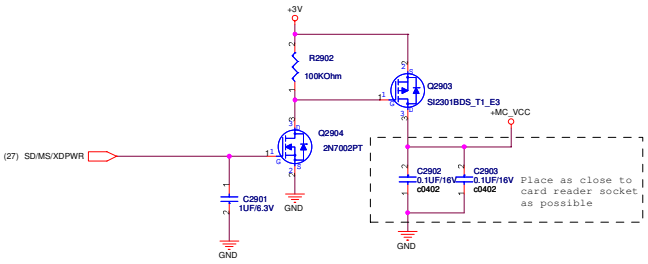
Memory Card Detect

MS_CD#	SD_CD#	
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

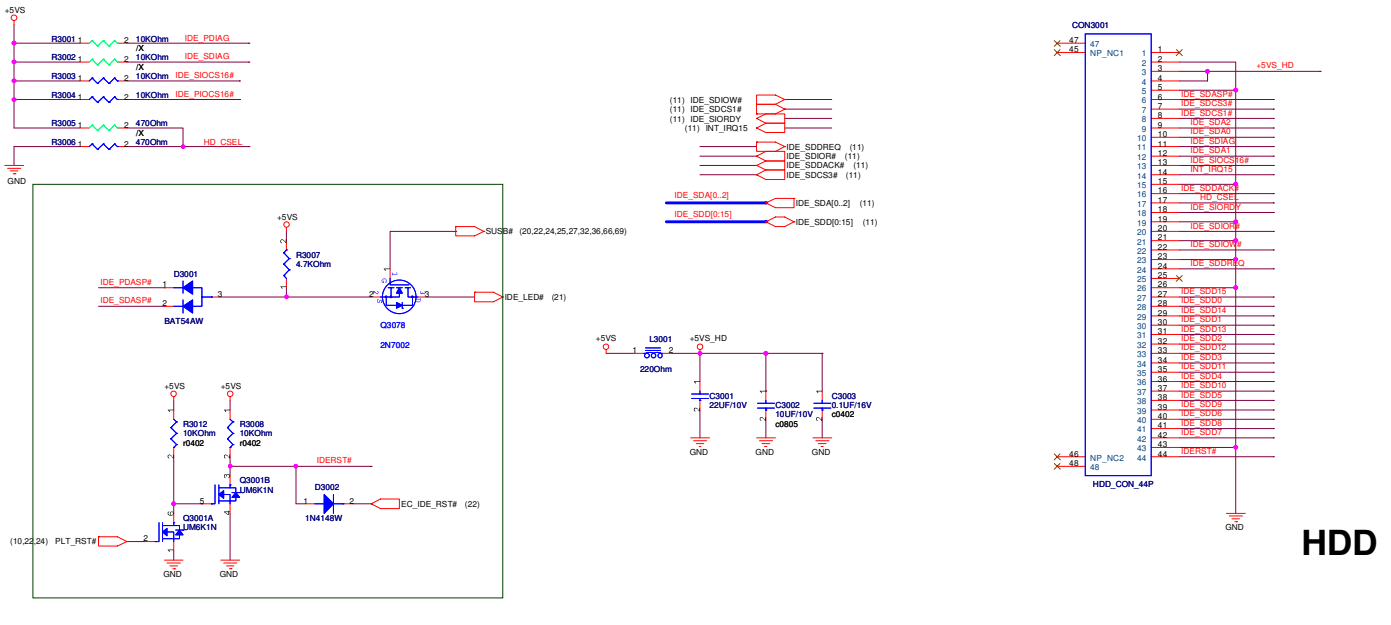
MC_CD# : Memory Card Detect



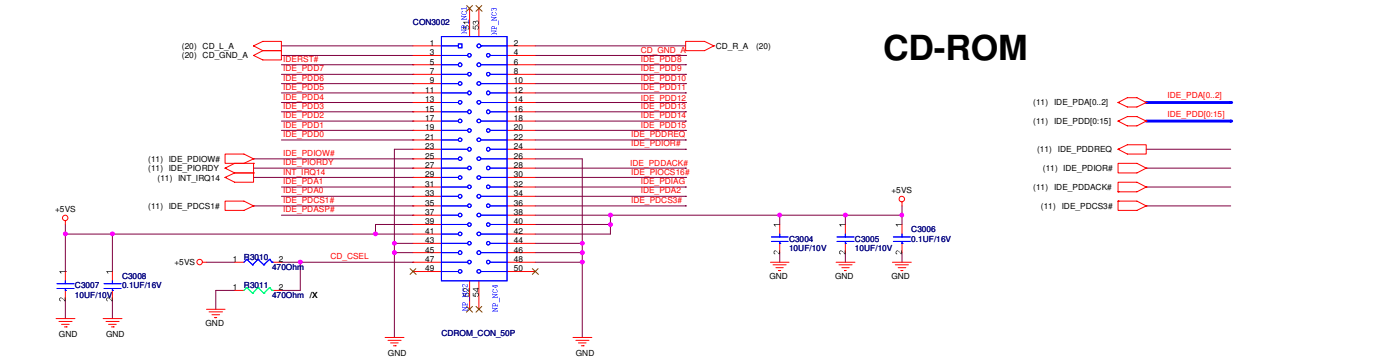




ASUS	Title : 4 IN 1 CON		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 八月 26, 2008	Sheet 29 of 45		



HDD

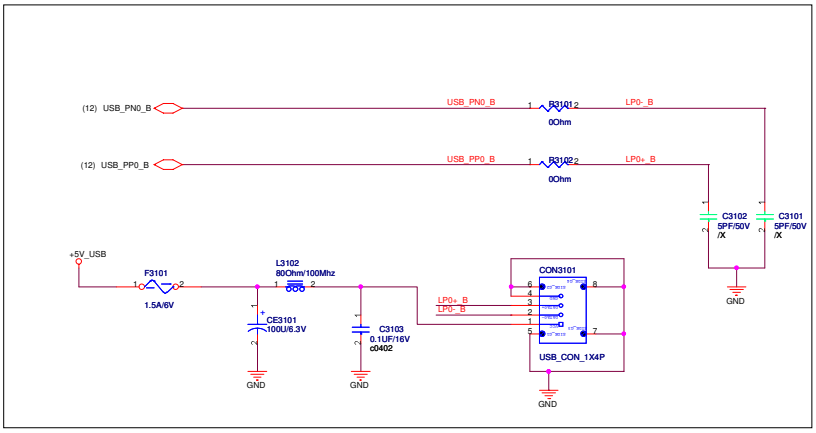


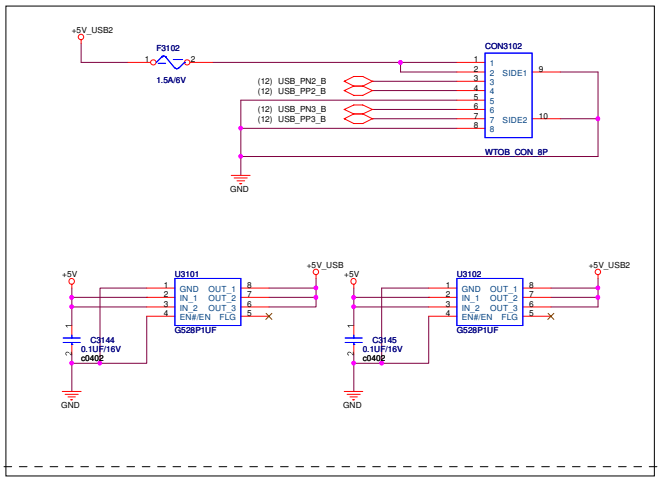
CD-ROM

ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master

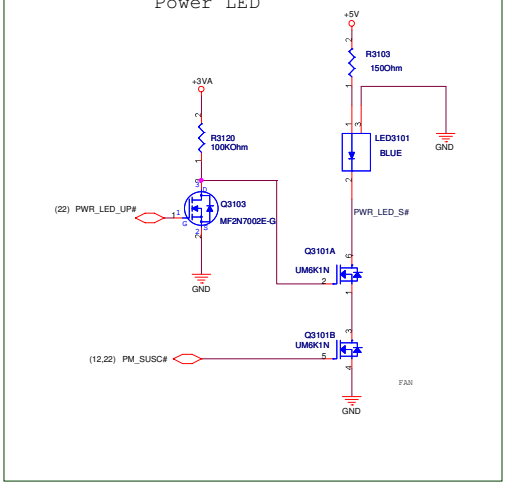
ASUS	Title : HDD & CD-ROM		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 十月 23, 2006	Sheet 30 of 45		

USB

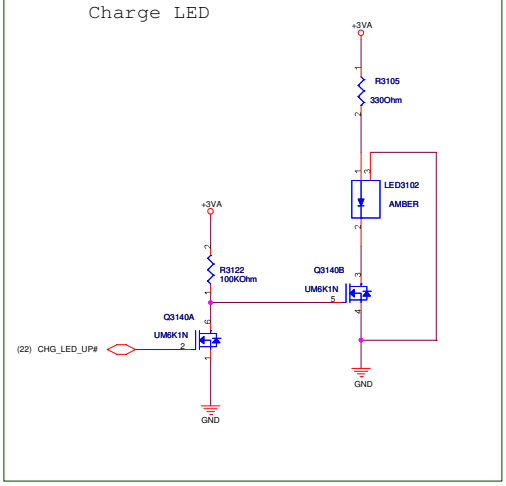




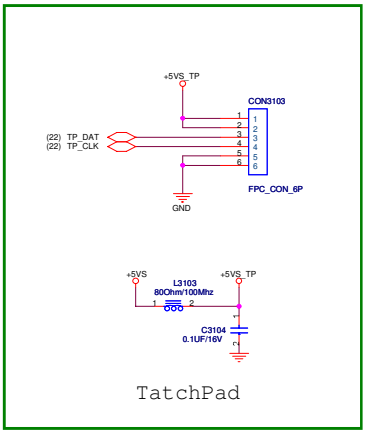
Power LED



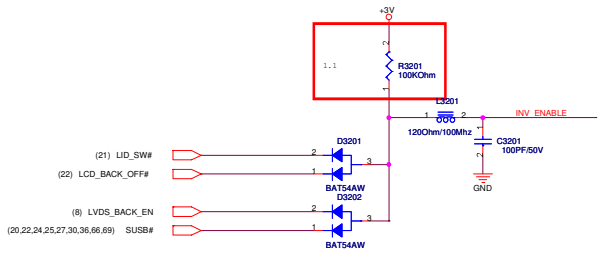
Charge LED



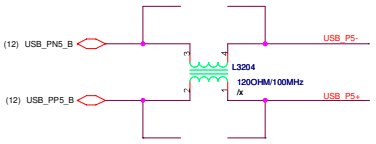
TatchPad

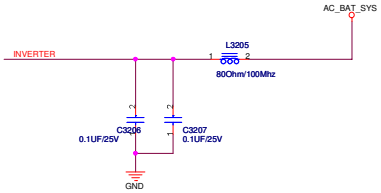


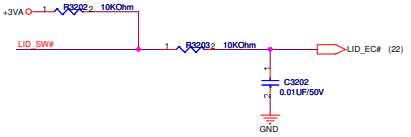
ASUS	Title : USB / LED / TP		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 六月 23, 2009	Sheet 31 of 45		



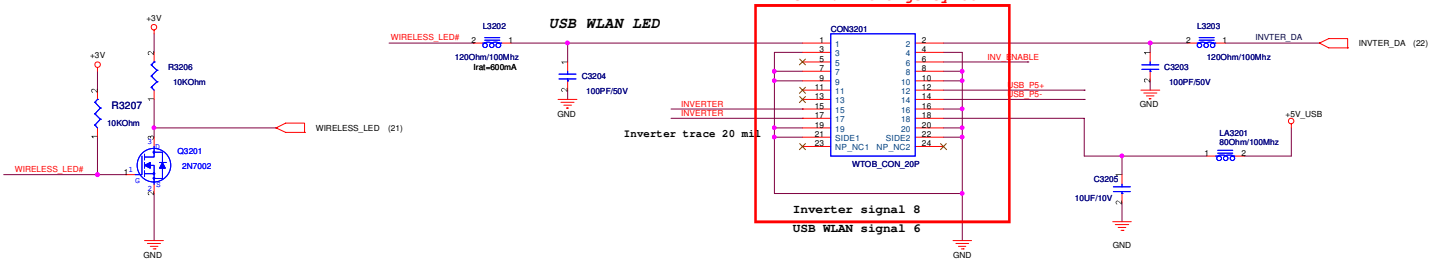
USB WIRESSLEE LAN



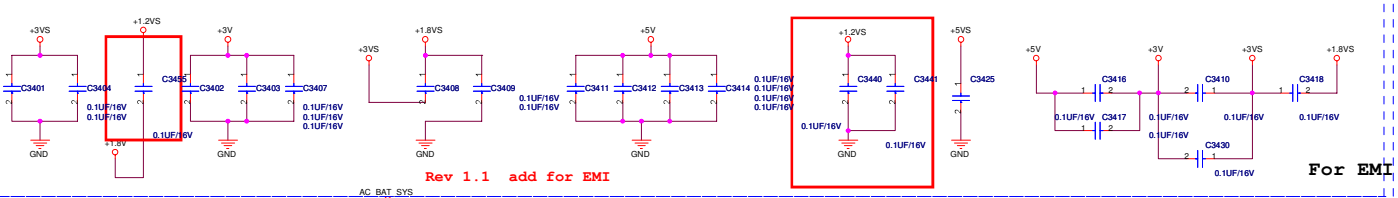


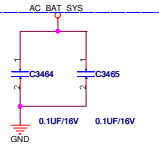


Rev 1.1 Change symbol

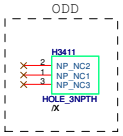


ASUS	Title : FUNCTION KEY & BT		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 六月 23, 2009	Sheet 32 of 45		

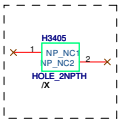




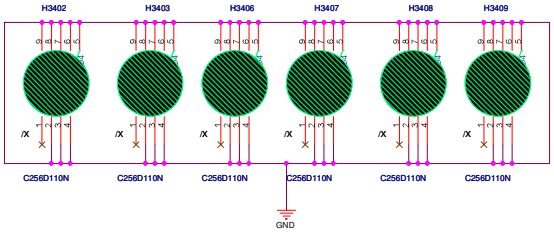
ODD



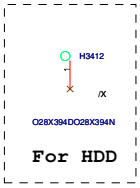
PAD Hole (2hole)--- E



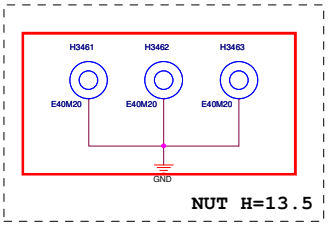
Hole no GND --- A



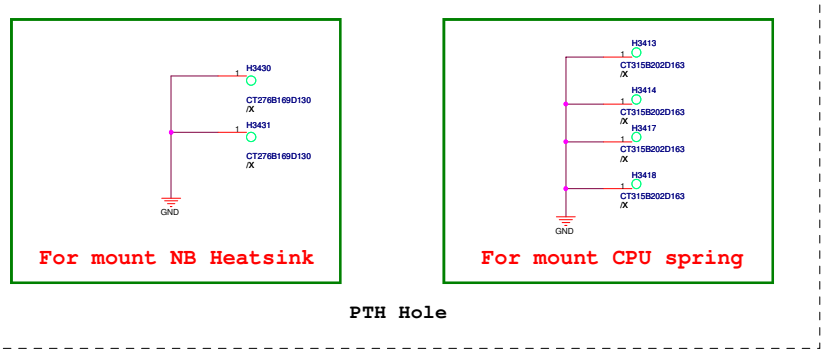
Oblong drill hole



For HDD



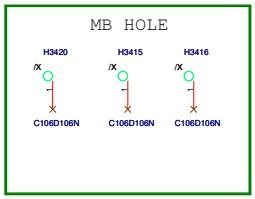
NUT H=13.5

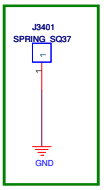


For mount NB Heatsink

For mount CPU spring

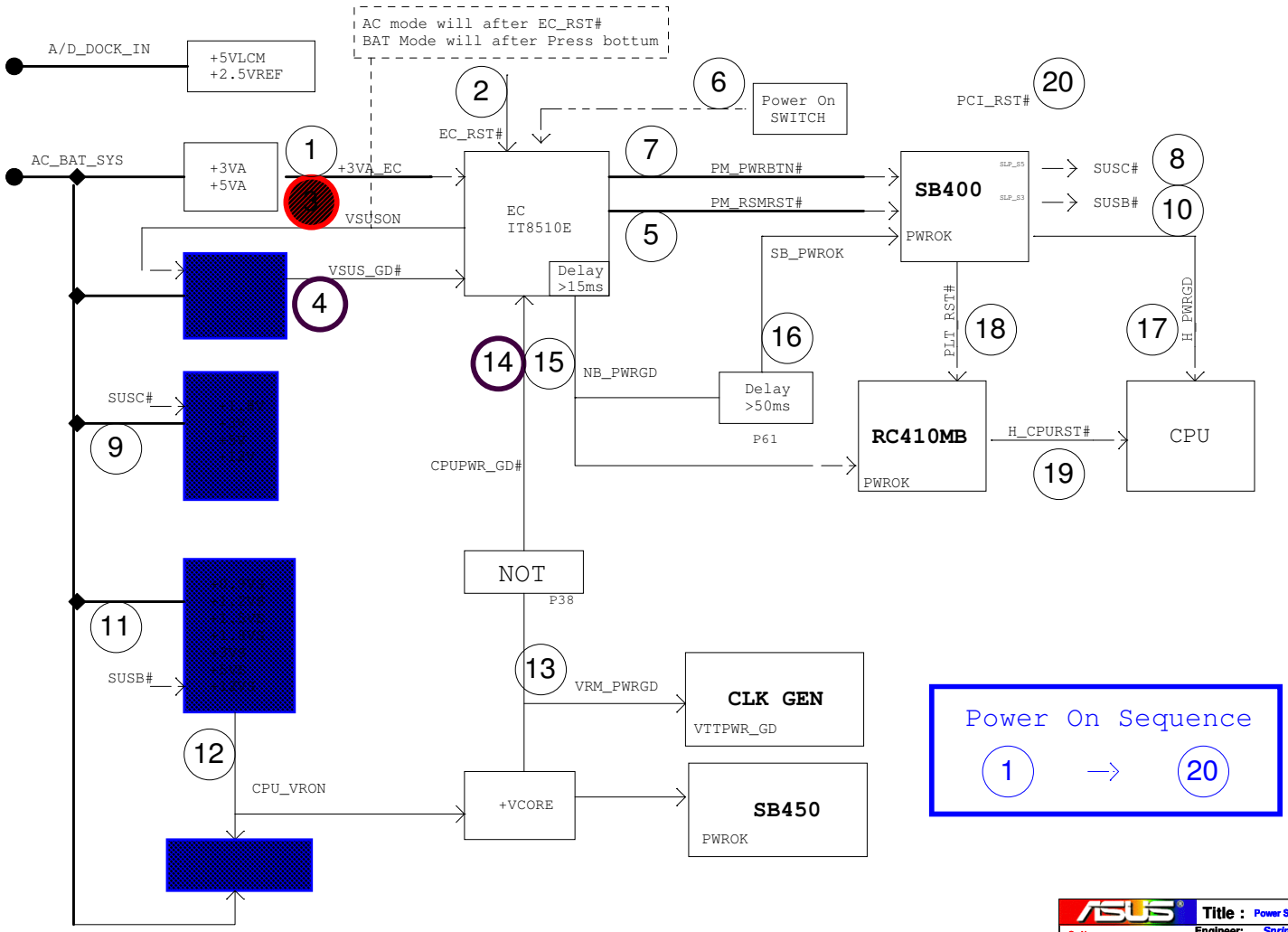
PTH Hole





For EMI

Title : Hole		
<OrgName>	Engineer: Spring LI	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 목요일, 9월 14, 2006	Sheet 33 of 45	



Title : Power Sequence			
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 四月 04, 2006	Sheet 34 of 45		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0->6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

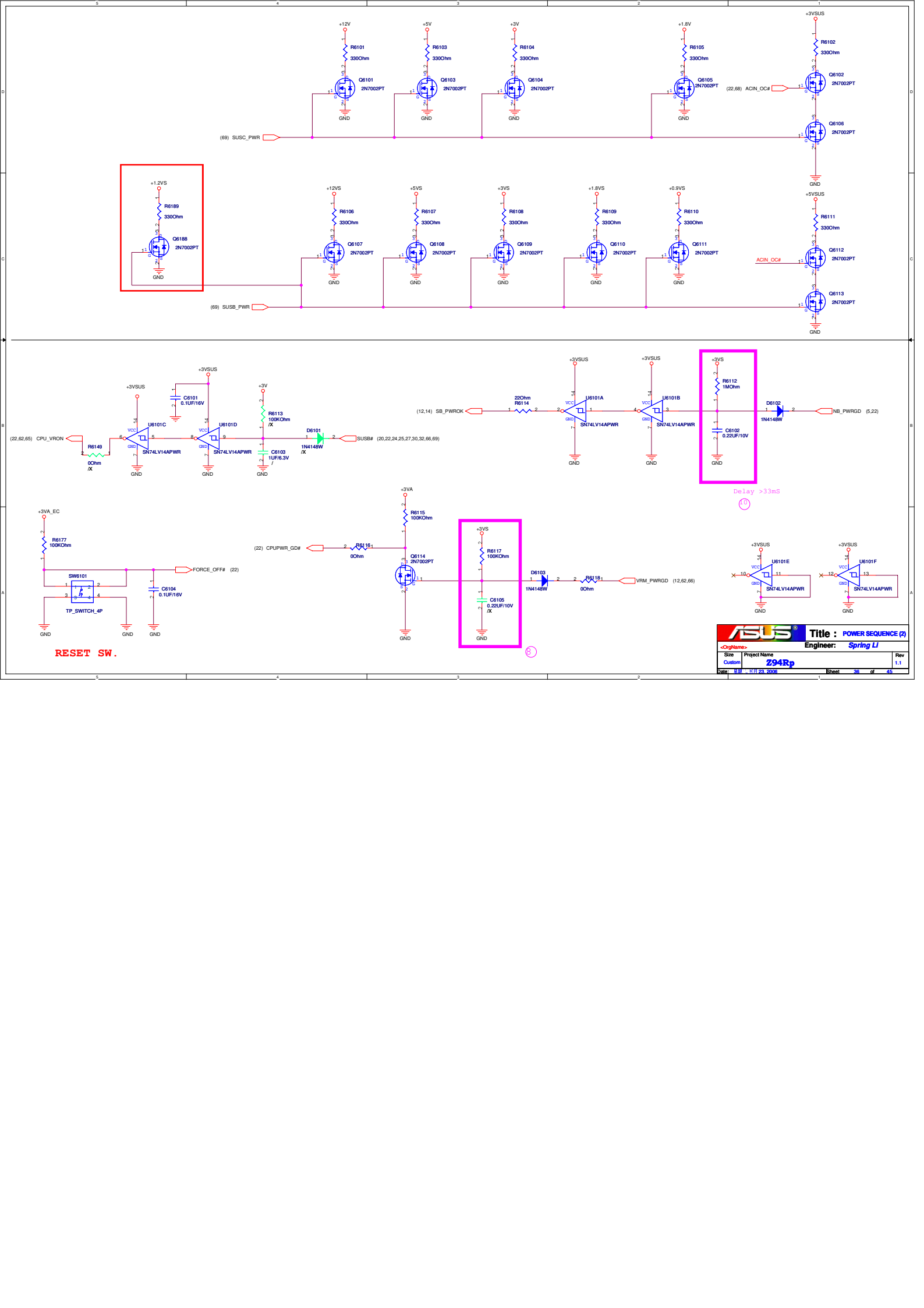
ASUS

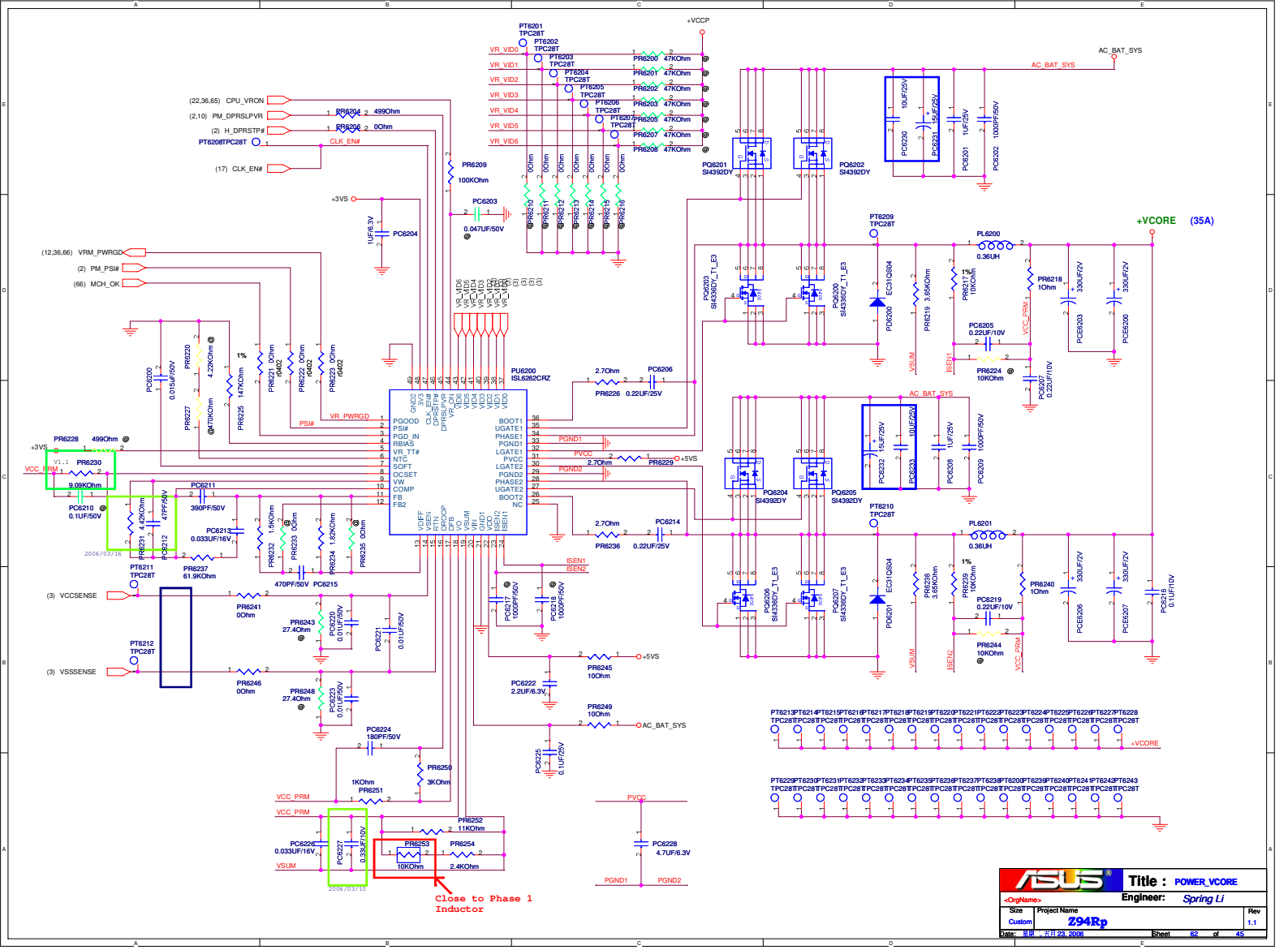
Title : SYSTEM RESOURCE

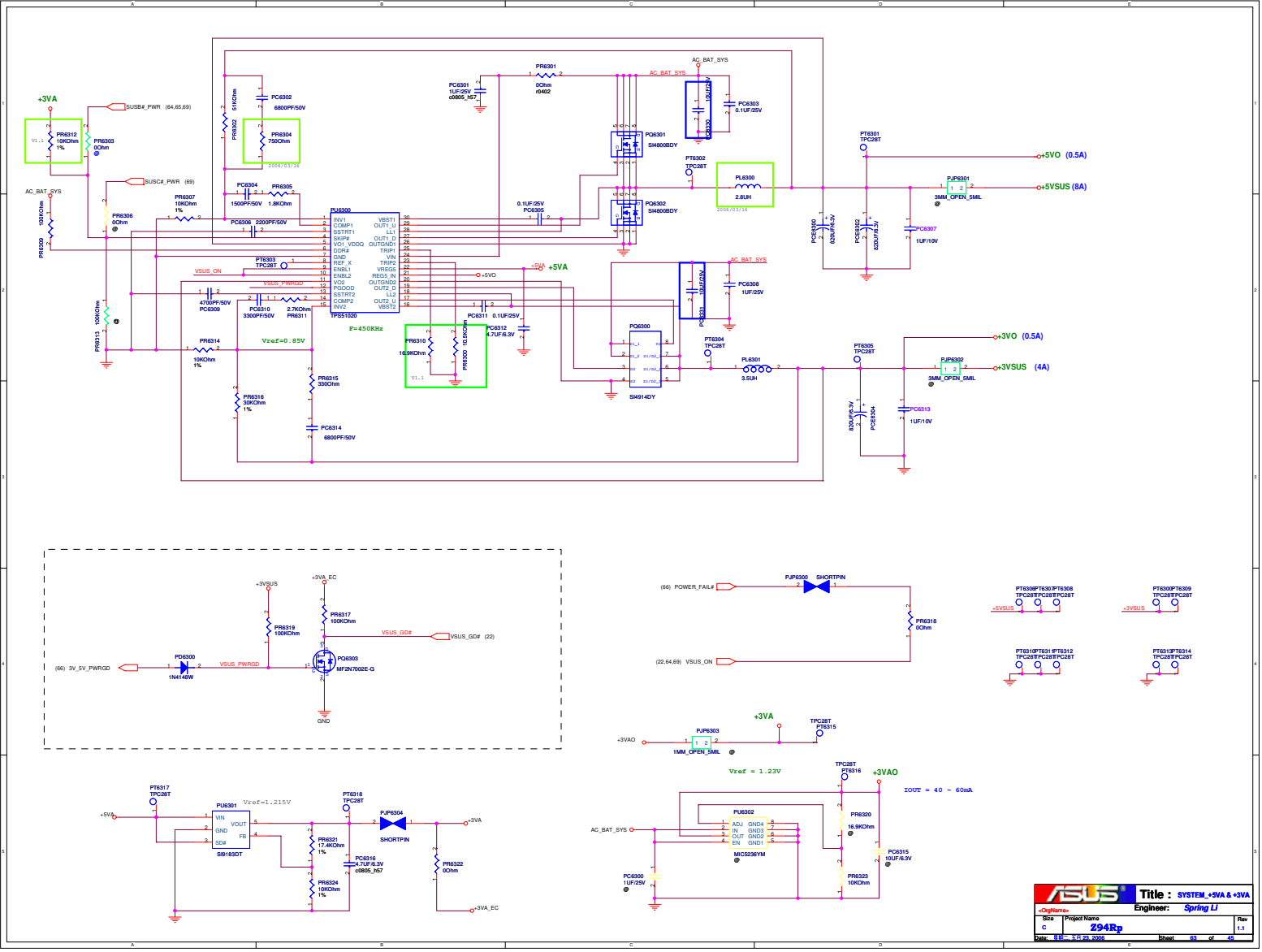
<OrgName> Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

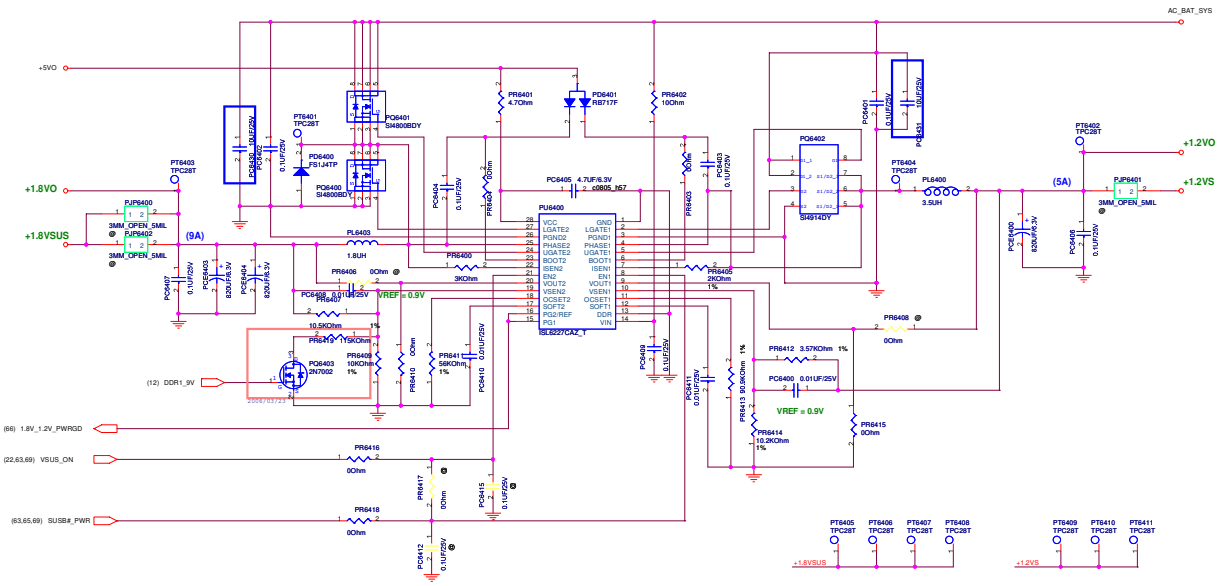
Date: 星期 二, 四月 04, 2006 Sheet 35 of 45


+12V
R6101
330Ohm
Q6101
2N7002PT
+5V
R6103
330Ohm
Q6103
2N7002PT
+3V
R6104
330Ohm
Q6104
2N7002PT
+1.8V
R6105
330Ohm
Q6105
2N7002PT
+3VSUS
R6102
330Ohm
Q6102
2N7002PT
Q6106
2N7002PT
(22,68) ACIN_OC#
(69) SUSC_PWR
GND
+1.2VS
R6189
330Ohm
Q6188
2N7002PT
+12VS
R6106
330Ohm
Q6107
2N7002PT
+5VS
R6107
330Ohm
Q6108
2N7002PT
+3VS
R6108
330Ohm
Q6109
2N7002PT
+1.8VS
R6109
330Ohm
Q6110
2N7002PT
+0.9VS
R6110
330Ohm
Q6111
2N7002PT
+5VSUS
R6111
330Ohm
Q6112
2N7002PT
Q6113
2N7002PT
ACIN_OC#
(69) SUSB_PWR
+3VSUS
C6101
0.1UF/16V
+3V
R6113
100KOhm
/X
U6101C
U6101D
SN74LV14APWR
(22,62,65) CPU_VRON
R6149
0Ohm
/X
D6101
1N4148W
/X
SUSB# (20,22,24,25,27,30,32,66,69)
C6103
1UF/6.3V
/
22Ohm
R6114
U6101A
U6101B
(12,14) SB_PWROK
R6112
1MOhm
D6102
1N4148W
NB_PWRGD (5,22)
C6102
0.22UF/10V
Delay >33mS
+3VA_EC
R6177
100KOhm
SW6101
TP_SWITCH_4P
FORCE_OFF# (22)
C6104
0.1UF/16V
RESET SW.
+3VA
R6115
100KOhm
(22) CPUPWR_GD#
R6116
0Ohm
Q6114
2N7002PT
R6117
100KOhm
C6105
0.22UF/10V
/X
D6103
1N4148W
R6118
0Ohm
VRM_PWRGD (12,62,66)
U6101E
U6101F
Title : POWER SEQUENCE (2)
<OrgName>
Engineer: Spring LI
Size
Custom
Project Name
Z94Rp
Rev
1.1
Date: 星期 二, 六月 23, 2009
Sheet 36 of 45

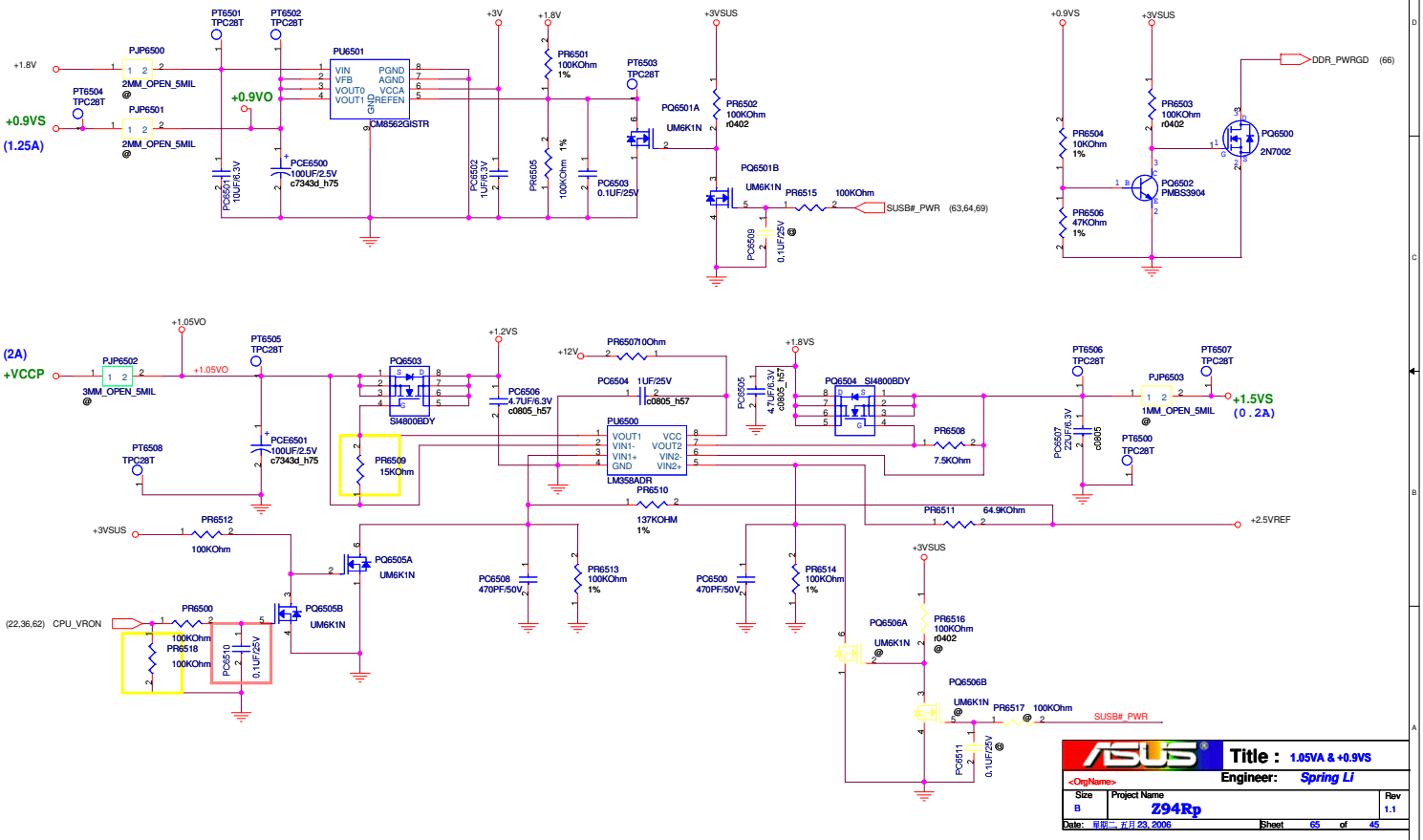

+VCCP
AC_BAT_SYS
+VCORE (35A)
PU6200 ISL6262CRZ
VR_PWRGD
PSI#
VCC_PRM
VSUM
ISEN1
ISEN2
PGND1
PGND2
PVCC
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 62 of 45



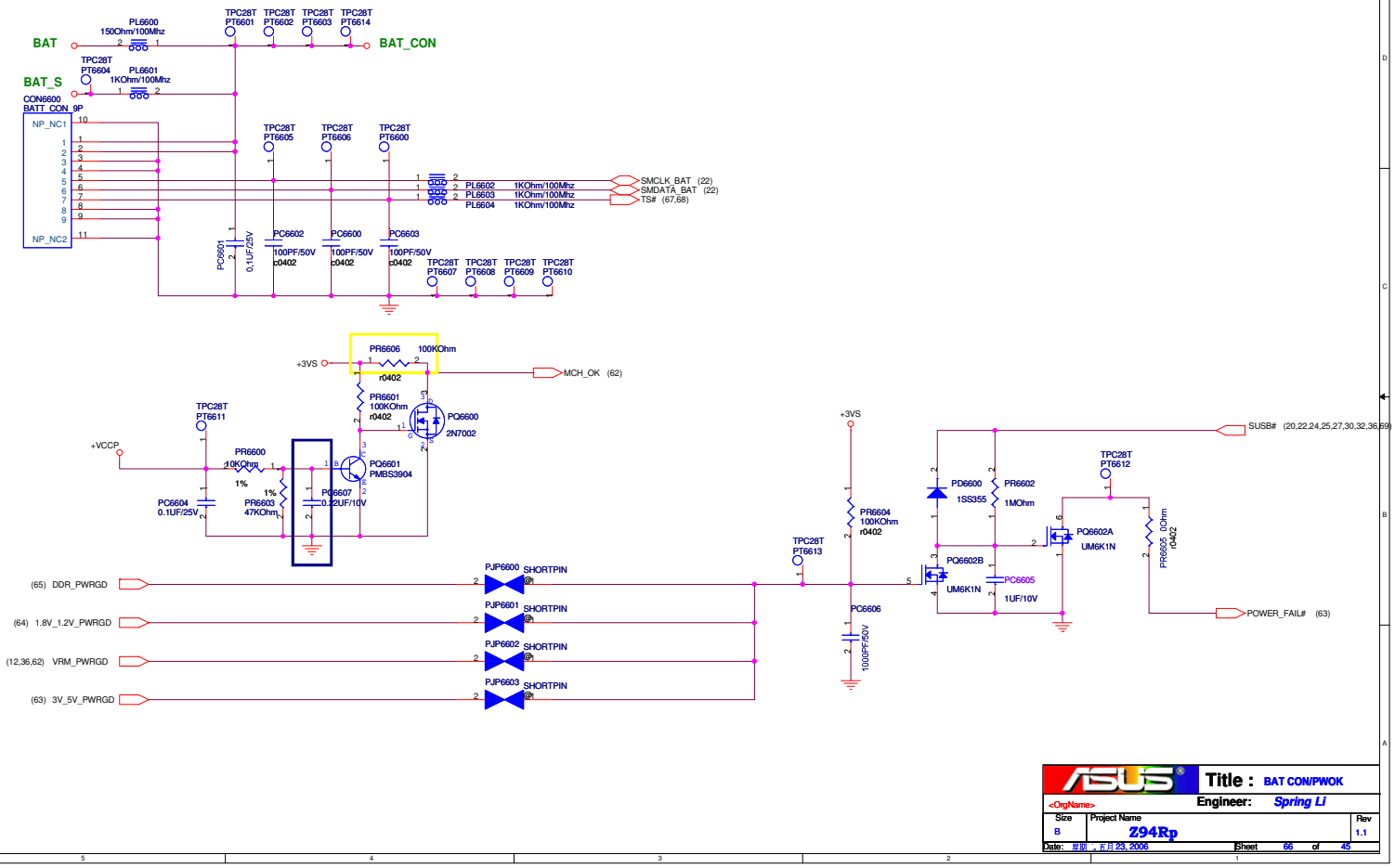
ASUS	Title : SYSTEM_+5VA & +3VA		
<OrgName>	Engineer: Spring Li		
Size: C	Project Name: Z94Rp		Rev: 1.1
Date: 三 8, 23, 2006	Sheet 63 of 45		



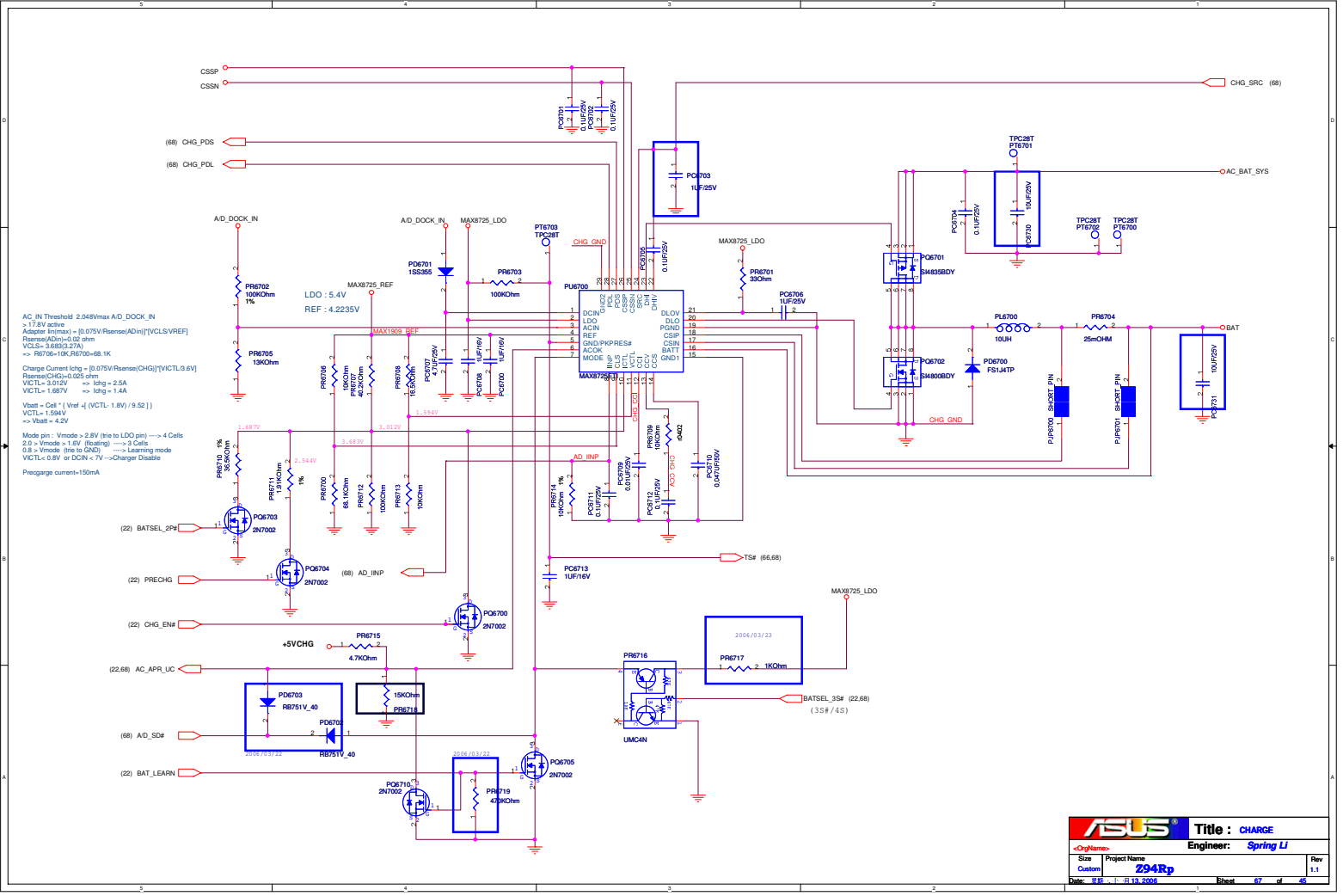
ASUS	Title : 1.8V&1.2VS		
<OrgName>	Engineer: Spring Li		
Size: C	Project Name: Z94Rp		Rev: 1.1
Date: 三 8, 月 23, 2006	Sheet 44 of 45		

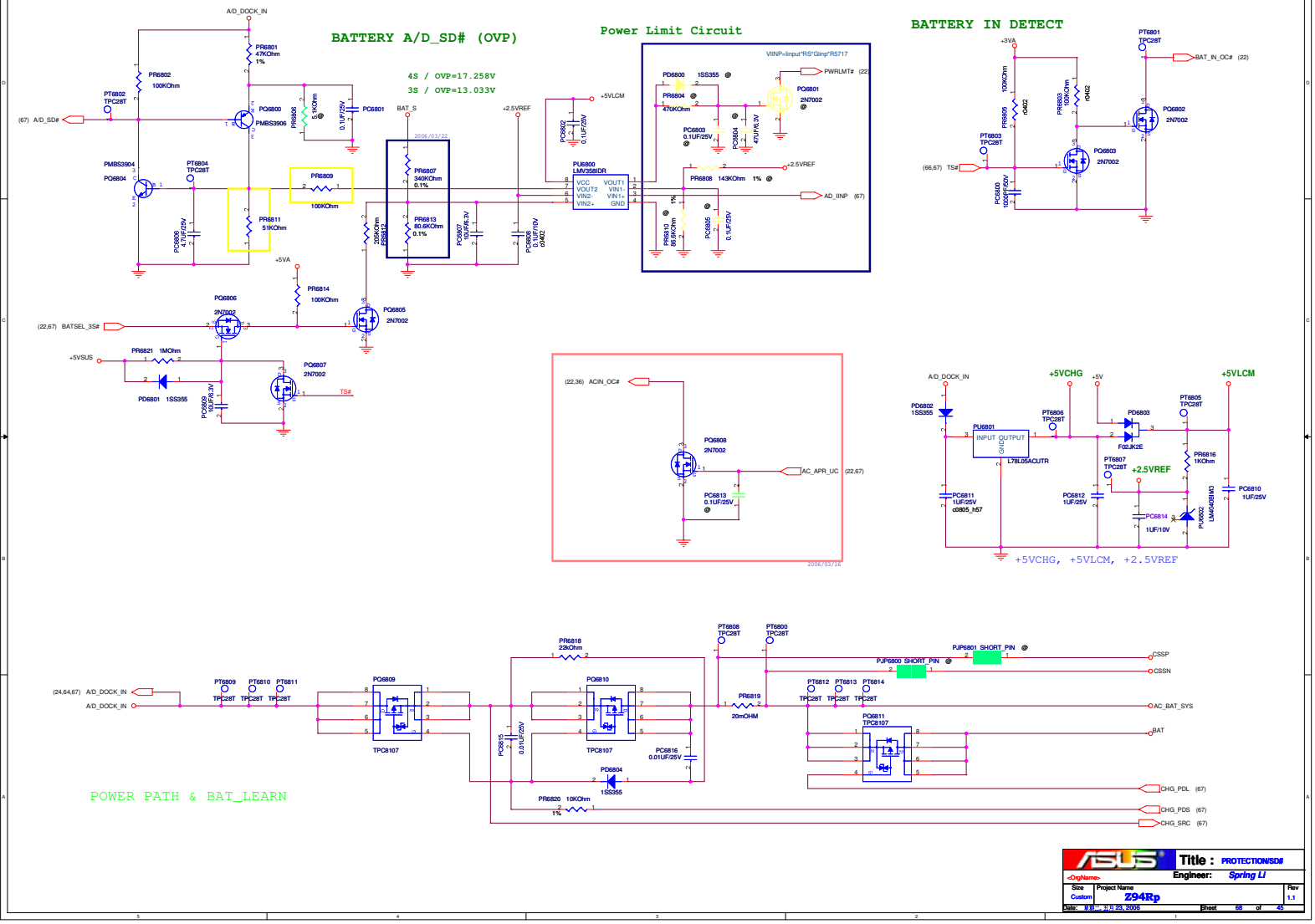


ASUS	Title : 1.05VA & +0.9VS	
<OrgName>	Engineer: Spring Li	
Size: B	Project Name: Z94Rp	Rev: 1.1
Date: 星期二, 五月 23, 2006	Sheet 65 of 45	

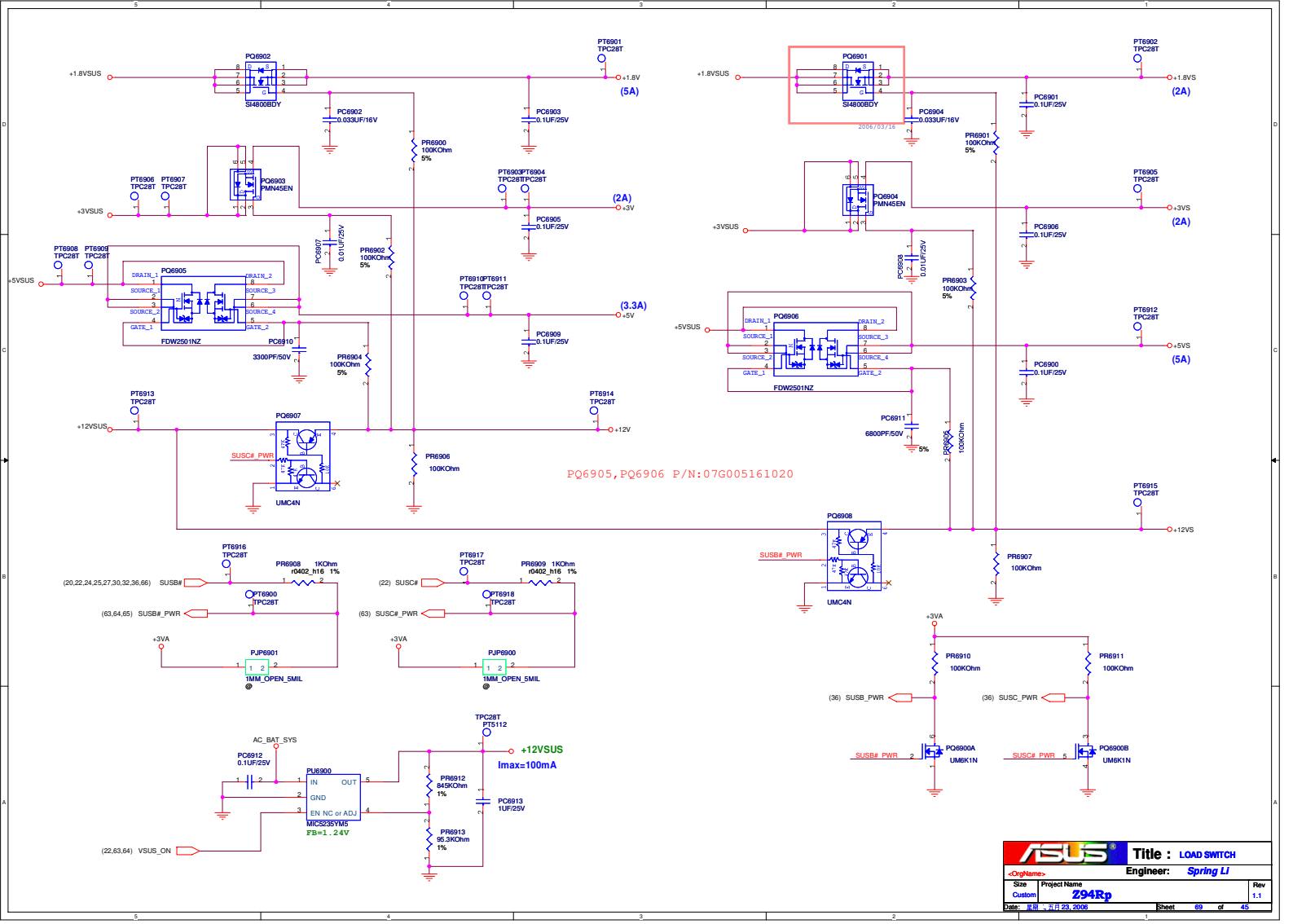


Title : BAT CON/PWOK		
<OrgName>	Engineer: Spring Li	
Size: B	Project Name: Z94Rp	Rev: 1.1
Date: 星期 一 五月 23, 2006	Sheet 66 of 45	

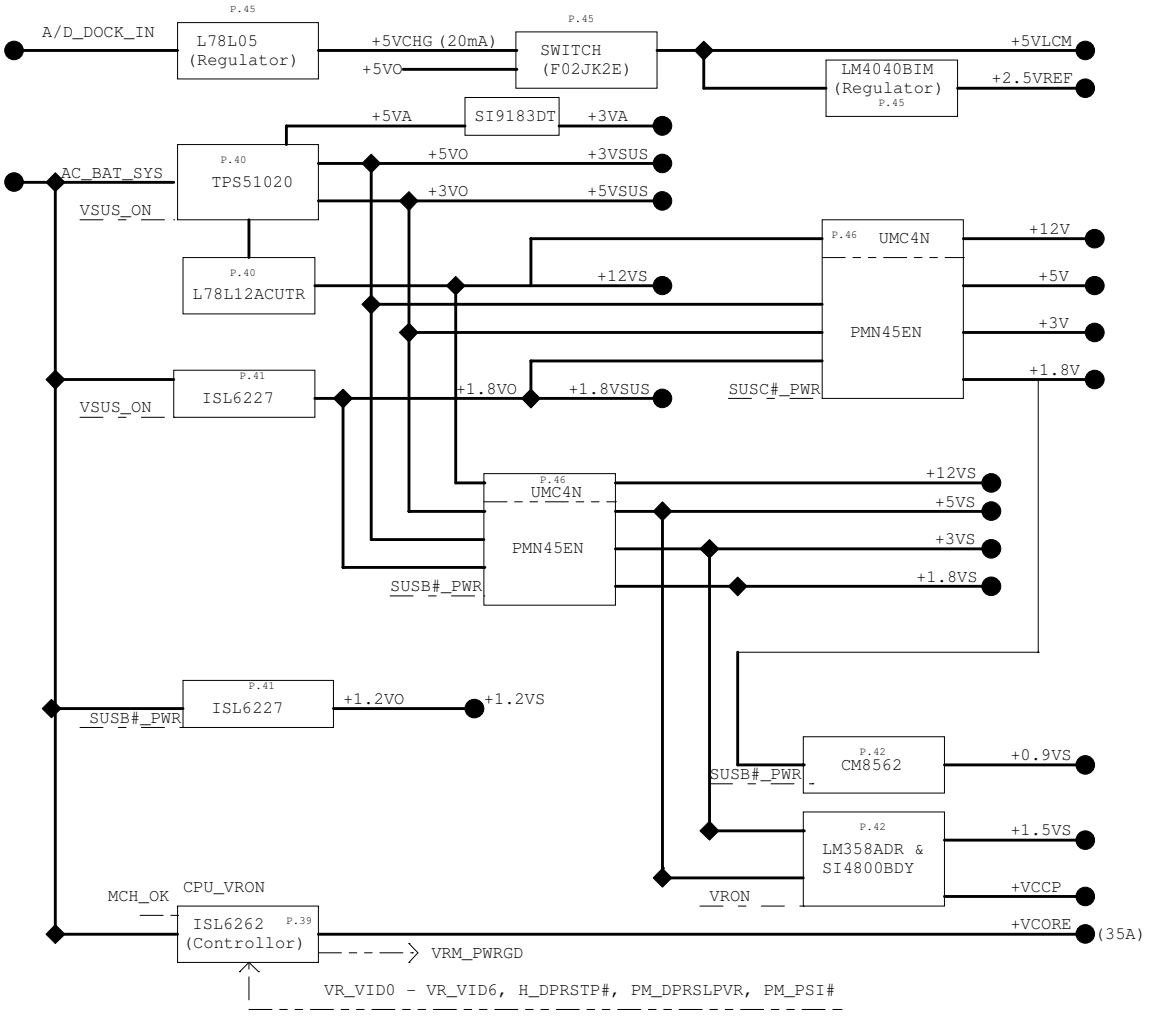

CSSP
CSSN
(68) CHG_PDS
(68) CHG_PDL
CHG_SRC (68)
AC_BAT_SYS
BAT
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
MAX1909_REF
CHG_GND
AD_IINP
TS# (66,68)
BATSEL_2P#
PRECHG
CHG_EN#
+5VCHG
AC_APR_UC
A/D_SD#
BAT_LEARN
BATSEL_3S# (22,68)
(3S#/4S)
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.8V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683(3.27A)
=> R6706=10K,R6700=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.012V => Ichg = 2.5A
VICTL= 1.687V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
Title : CHARGE
Engineer: Spring Li
Project Name 294Rp
Rev 1.1
Sheet 67 of 45



ASUS	Title : PROTECTION/SD#		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期一, 五月 29, 2006	Sheet 68 of 45		



Title : LOAD SWITCH			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 五月 23, 2006		Sheet 69 of 45	



<OrgName>	Title : POWER BLOCK DIAGRAM		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 四月 04, 2006	Sheet 70 of 45		