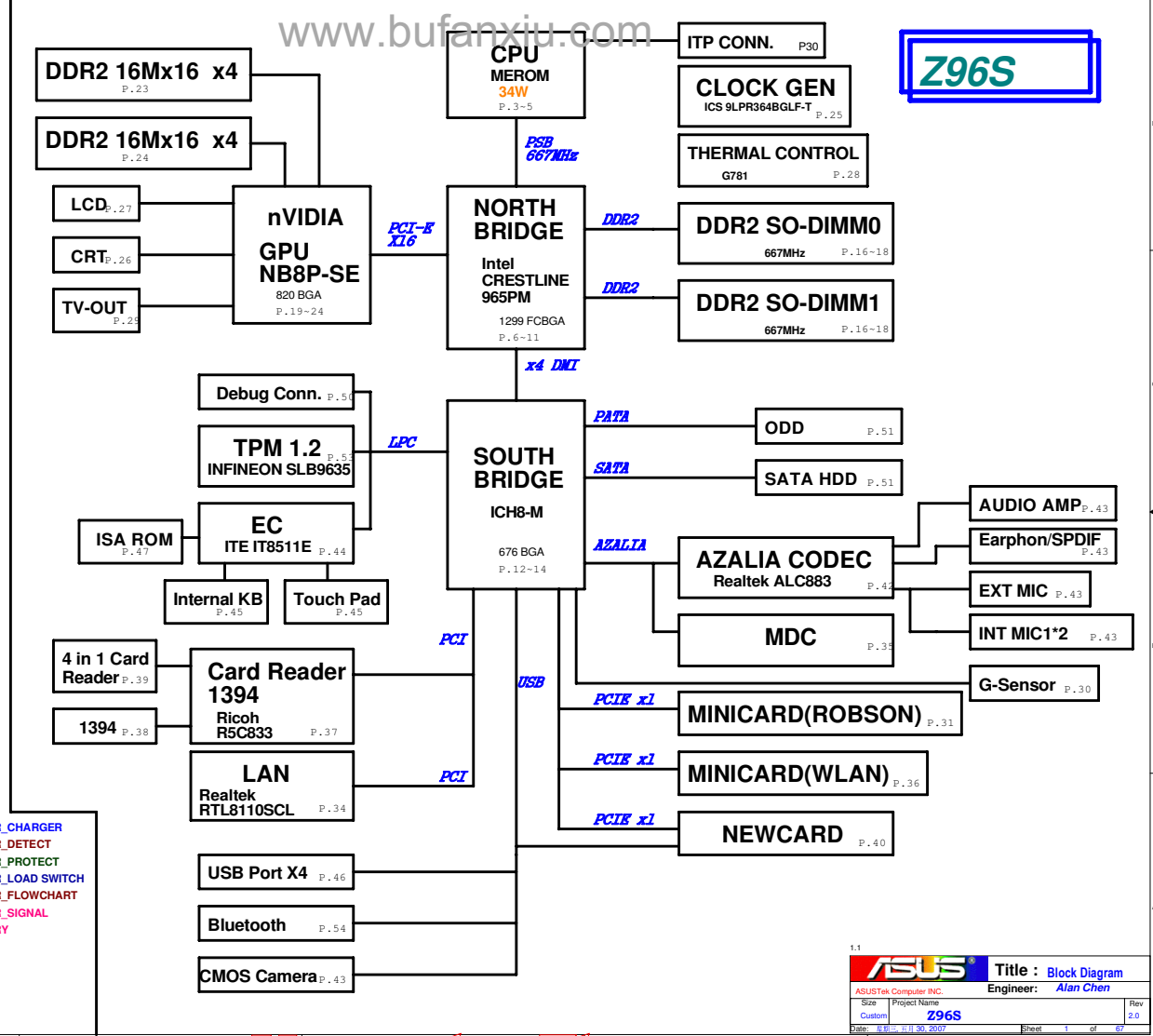




- 01\_Block Diagram
- 02\_System Setting
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- 04\_Merom CPU (2)
- 05\_CPU CAPS.
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- 07\_965PM-DDR2/PEG (2)
- 08\_965PM-DDR2 BUS (3)
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- 32\_SWITCH
- 33\_DISCHARGE
- 34\_GIGALAN-RTL8110SCL
- 35\_MDC&RJ45&RJ11
- 36\_MINI CARD -- WLAN
- 37\_RICOH-R5C833\_PCI
- 38\_RICOH-R5C833\_1394SD
- 39\_4 in 1 CARD READER
- 40\_NEWCARD
- 41\_Port Bar
- 42\_AUDIO-CODEC-ALC882
- 43\_AUDIO AMP & JACK
- 44\_EC-IT8511E
- 45\_Touch Pad/ KB
- 46\_USB CONN
- 47\_ISA ROM
- 48\_LED
- 49\_DCIN & BAT CONN
- 50\_Debug CONN.
- 51\_SATA-HDD & ODD
- 52\_SREW HOLE
- 53\_TPM CONNECTOR
- 54\_BT CONNECTOR
- 55\_POWER\_VCORE
- 56\_POWER\_SYSTEM\_+3VO & +5VO
- 57\_POWER\_1.5VS&1.05VS
- 58\_POWER\_IO\_DDR & VTT
- 59\_POWER\_+3VAO
- 60\_POWER\_VGA\_CORE
- 61\_POWER\_CHARGER
- 62\_POWER\_DETECT
- 63\_POWER\_PROTECT
- 64\_POWER\_LOAD SWITCH
- 65\_POWER\_FLOWCHART
- 66\_POWER\_SIGNAL
- 67\_HISTORY



ASUS		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007-11-30		Sheet	1 of 87

<< Kennedy\_Zhang >>

**EC GPIO SETTING**

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSERVE#	O
37	PWM3/GPA3	NA	O
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	NA	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	IO
164	SMDAT0/GPB4	SMB0_DAT	IO
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	NA	O
169	SMCLK1/GPC1	SMB1_CLK	IO
170	SMDAT1/GPC2	SMB1_DAT	IO
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	NA	O
26	RH#/WUI0/GPD0	SUSB#	I
29	RH#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PLT_RST#	I
31	ECSC#/#GPD3	EXT_SC#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	NA	O
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	NA	O
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	EXPLORE_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	NA	O
24	LPCPD#/WUI6/GPE6	NA	O
25	CLKRUN#/WUI7/GPE7	NA	O
101	GRJ2/DAC2	BL_DA	O
102	GRJ3/DAC3	BATSEL_2P#	O
81	GPK0/ADC0	P_PMON	I
22	ECSM#/#GPM0	EXT_SM#	O
116	PS2CLK2/GPF4	TP_CLK	IO
117	PS2DAT2/GPF5	TP_DAT	IO
118	PS2CLK3/GPF6	NA	O
119	PS2DAT3/GPF7	NA	O
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	NA	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	PMTHERM#	O
27	LPC80HL/GPG6	THRM_CPU#	I
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUP_WR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GP10	SB_PWRGD	O
149	GP11	NA	O
152	GP12	MCHOK	I
155	GP13	CHG_EN#	O
156	GP14	PRECHG	O
168	GP15	BAT_LL#	O
174	GP16	BAT_LEARN	O

**ICH8-M GPIO SETTING**

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AG12	GPIO0/BMBUSY#	PM_BMBUSY#	IO	Core(To:3.3V)	GPI
AJ8	GPIO1/TACH1	VDDR_SELO	IO	Core(To:3.3V)	GPI
F8	GPIO2/PIRQE#	INT_SHIFT_LOW#	I(OD)	Core(To:3.3V)	GPI
G11	GPIO3/PIRQF#	INT_SHIFT_HIGH#	I(OD)	Core(To:3.3V)	GPI
F12	GPIO4/PIRQG#	PCL_INTG#	I(OD)	Core(To:3.3V)	GPI
B3	GPIO5/PIROH#	PCL_INTH#	I(OD)	Core(To:3.3V)	GPI
AJ9	GPIO6/TACH2	VDDR_SEL1	IO	Core(To:3.3V)	GPI
AH9	GPIO7/TACH3	VDDR_SEL2	IO	Core(To:3.3V)	GPI
AE16	GPIO8	EXT_SM#	IO	SUS(To:3.3V)	GPI
AG19	GPIO9/WOL_EN	TP	IO	SUS(To:3.3V)	GPI
AJ24	GPIO10/CLGPI01	TP	IO	SUS(To:3.3V)	GPI
AG22	SMBALERT#/GPIO11	NC	IO	SUS(To:3.3V)	Native
AC19	GPIO12	EXT_SC#	IO	SUS(To:3.3V)	GPI
AH21	GPIO13/GLAN_DOCL#	NC	IO	SUS(To:3.3V)	Native
AF22	GPIO14/CLGPI02	TP	IO	SUS(To:3.3V)	GPI
AE20	GPIO15/STP_PCH#	STP_PCH#	IO	SUS(To:3.3V)	Native
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	IO	Core(To:3.3V)	Native
AG8	GPIO17/TACH0	PM_EXTTS#0	IO	Core(To:3.3V)	GPI
AH12	GPIO18	VCORE_SELO	IO	Core(To:3.3V)	GPO
AJ10	GPIO19/SATA1GP	CB_SD#	IO	Core(To:3.3V)	GPI
AE11	GPIO20	VCORE_SEL1	IO	Core(To:3.3V)	GPO
AJ12	GPIO21/SATA0GP	WLAN_BT_LED_EN#	IO	Core(To:3.3V)	GPI
AG10	GPIO22/SCLOCK	TP	IO	Core(To:3.3V)	GPI
E6	GPIO23/LDRQ1#	TP	IO	Core(To:3.3V)	Native
AJ27	GPIO24/CLGPI00	TP	IO	SUS(To:3.3V)	GPO
AG18	GPIO25/STP_CPU#	STP_CPU#	IO	SUS(To:3.3V)	Native
AH27	GPIO26/S4_STATE#	TP	IO	SUS(To:3.3V)	Native
AH25	GPIO27/ORT_STATE0	VGMCH_SELO	IO	SUS(To:3.3V)	GPO
AD16	GPIO28/ORT_STATE1	VGMCH_SEL1	IO	SUS(To:3.3V)	GPO
AG17	GPIO29/OC#5	USB_OC#5	IO	SUS(To:3.3V)	Native
AD12	GPIO30/OC#6	NEWCARD_OC#	IO	SUS(To:3.3V)	Native
AJ18	GPIO31/OC#7	USB_OC#7	IO	SUS(To:3.3V)	Native
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	IO	Core(To:3.3V)	Native
AE10	GPIO33/HDA_DOCK_EN#	TP	IO	Core(To:3.3V)	GPO
AG14	GPIO34/HDA_DOCK_RST#	TP	IO	Core(To:3.3V)	GPO
AG13	GPIO35/SATACLKREQ#	VGPU_SEL1	IO	Core(To:3.3V)	GPO
AF11	GPIO36/SATA2GP	WLAN_ON#	IO	Core(To:3.3V)	GPI
AG11	GPIO37/SATA3GP	BT_ON#	IO	Core(To:3.3V)	GPI
AF9	GPIO38/SLOAD	PM_EXTTS#1	IO	Core(To:3.3V)	GPI
AJ11	GPIO39/SDATAOUT0	CLK_PWRSERVE#	IO	Core(To:3.3V)	GPI
AG16	GPIO40/OC1#	USB_CON_OC01#	IO	SUS(To:3.3V)	Native
AG15	GPIO41/OC2#	USB_CON_OC23#	IO	SUS(To:3.3V)	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	REQ#0/GNT#0	INTB-->INTB
1394	AD17	REQ#0/GNT#0	INTA-->INTA
LAN	AD23	REQ#2/GNT#2	INTA-->INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor	0101110x ( 5C )

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AD16	GPIO42/OC3#	USB_CON_OC23#	IO	SUS(To:3.3V)	Native
AG17	GPIO43/OC4#	USB_CON_OC4#	IO	SUS(To:3.3V)	Native
NA	GPIO44	NA	IO	NA	NA
NA	GPIO45	NA	IO	NA	NA
NA	GPIO46	NA	IO	NA	NA
NA	GPIO47	NA	IO	NA	NA
AD10	GPIO48/SDATAOUT1	TP	IO	Core(To:3.3V)	GPI
AG29	GPIO49/CPUPWRGD	H_PWRGD	IO	V_CPU_IO	Native
E18	GPIO50/REQ1#	PCL_REQ#1	IO	Core(To:3.5V)	Native
C18	GPIO51/GNT1#	TP	IO	Core(To:3.3V)	Native
B19	GPIO52/REQ2#	PCL_REQ#2	IO	Core(To:3.5V)	Native
F18	GPIO53/GNT2#	PCL_GNT#2	IO	Core(To:3.3V)	Native
A11	GPIO54/REQ3#	PCL_REQ#3	IO	Core(To:3.5V)	Native
C10	GPIO55/GNT3#	NC	IO	Core(To:3.3V)	Native

ASUS Logo

**Title : System Setting**

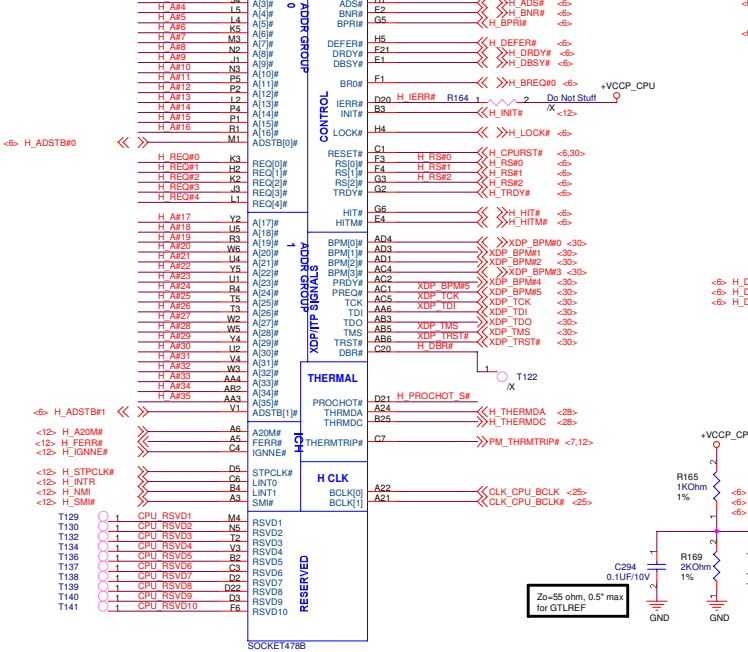
ASUSTek Computer INC. Engineer: Alan Chen

Size: Custom Project Name: Z96S Rev: 2.0

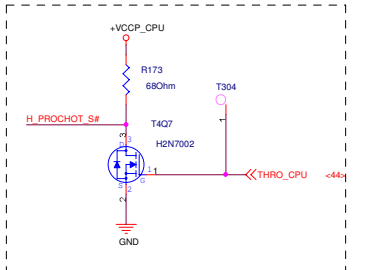
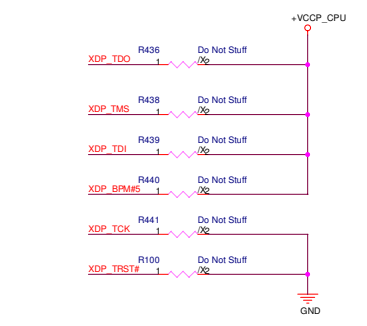
Date: 11/11/2007 Sheet: 2 of 67

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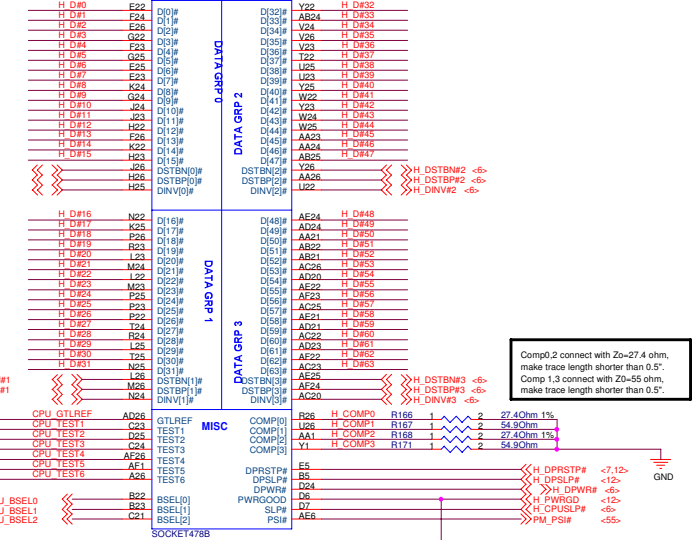
CPU1A



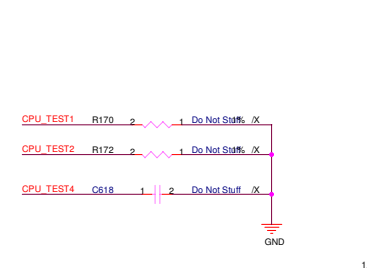
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CPU1B



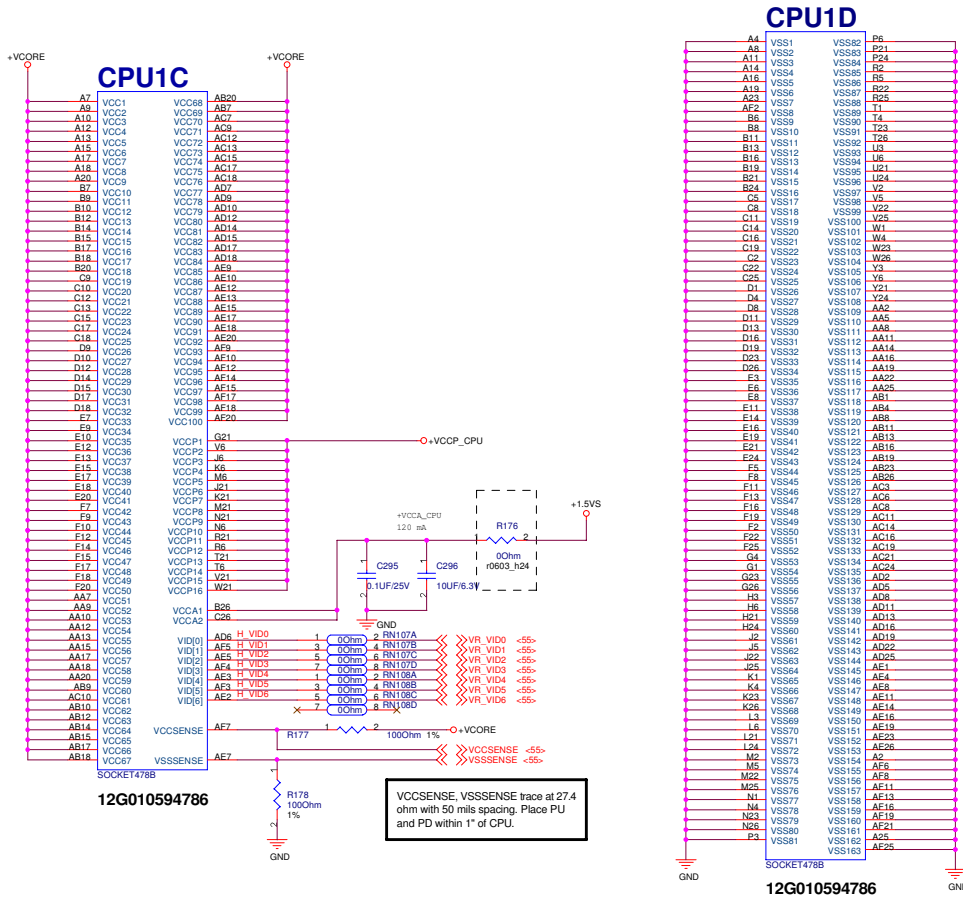
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Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp 1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".

**ASUS** Title : MEROM CPU (1)  
 ASUSTeK COMPUTER INC. Engineer: Alan Chen  
 Size Custom Project Name Z96S Rev 2.0  
 Date: 01/10/2007 Sheet 3 of 87

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1.1

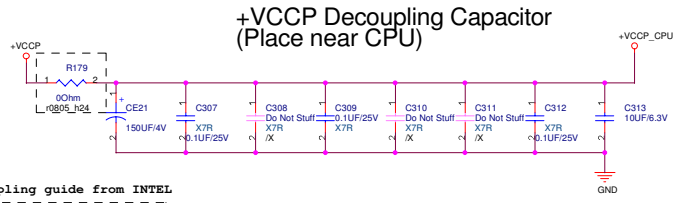
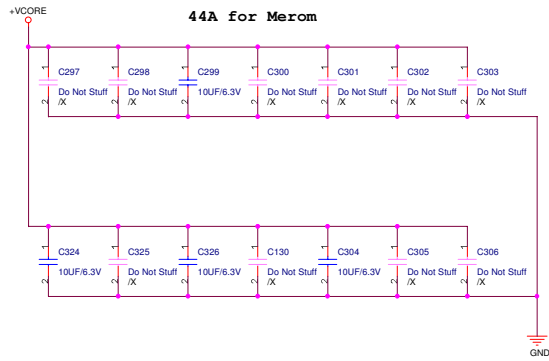
**ASUS** Title : MEROM CPU (2)

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

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**Decoupling guide from INTEL**

VCCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

1.1

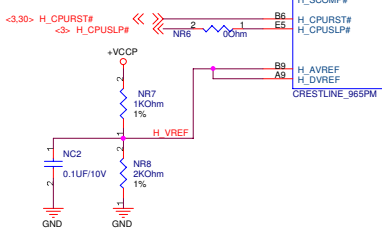
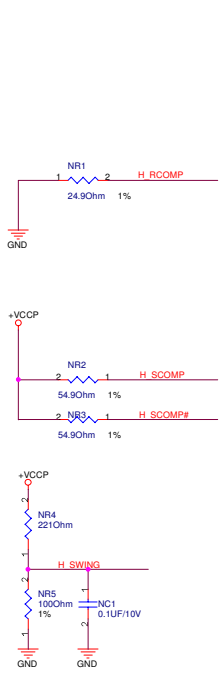
**ASUS** Title :CPU CAP and HOLES

ASUSTeK COMPUTER INC. NBI Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

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H_D#0	E2	H_D#0
H_D#1	G2	H_D#1
H_D#2	G7	H_D#2
H_D#3	M6	H_D#3
H_D#4	H7	H_D#4
H_D#5	H5	H_D#5
H_D#6	G4	H_D#6
H_D#7	F3	H_D#7
H_D#8	N8	H_D#8
H_D#9	H2	H_D#9
H_D#10	M10	H_D#10
H_D#11	N12	H_D#11
H_D#12	N9	H_D#12
H_D#13	H5	H_D#13
H_D#14	P13	H_D#14
H_D#15	K9	H_D#15
H_D#16	M2	H_D#16
H_D#17	W10	H_D#17
H_D#18	Y8	H_D#18
H_D#19	V4	H_D#19
H_D#20	M3	H_D#20
H_D#21	J1	H_D#21
H_D#22	N5	H_D#22
H_D#23	W6	H_D#23
H_D#24	W9	H_D#24
H_D#25	W9	H_D#25
H_D#26	Y7	H_D#26
H_D#27	M2	H_D#27
H_D#28	Y9	H_D#28
H_D#29	W3	H_D#29
H_D#30	N1	H_D#30
H_D#31	AD12	H_D#31
H_D#32	AE3	H_D#32
H_D#33	AD9	H_D#33
H_D#34	AG8	H_D#34
H_D#35	AC7	H_D#35
H_D#36	AD11	H_D#36
H_D#37	AD11	H_D#37
H_D#38	AD14	H_D#38
H_D#39	AD7	H_D#39
H_D#40	AB1	H_D#40
H_D#41	Y4	H_D#41
H_D#42	AC6	H_D#42
H_D#43	AE2	H_D#43
H_D#44	AC5	H_D#44
H_D#45	AC5	H_D#45
H_D#46	AG3	H_D#46
H_D#47	AG9	H_D#47
H_D#48	AH8	H_D#48
H_D#49	AJ14	H_D#49
H_D#50	AE9	H_D#50
H_D#51	AE11	H_D#51
H_D#52	AH12	H_D#52
H_D#53	AJ5	H_D#53
H_D#54	AH5	H_D#54
H_D#55	AH5	H_D#55
H_D#56	AE7	H_D#56
H_D#57	AJ7	H_D#57
H_D#58	AJ2	H_D#58
H_D#59	AE5	H_D#59
H_D#60	AJ3	H_D#60
H_D#61	AH2	H_D#61
H_D#62	AH13	H_D#62
H_D#63		H_D#63

HOST

H_A#_3	J13	H_A#3
H_A#_4	M11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L18	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	B16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L18	H_A#14
H_A#_15	L17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	R16	H_A#20
H_A#_21	L19	H_A#21
H_A#_22	G17	H_A#22
H_A#_23	M17	H_A#23
H_A#_24	M16	H_A#24
H_A#_25	J19	H_A#25
H_A#_26	B18	H_A#26
H_A#_27	E19	H_A#27
H_A#_28	B17	H_A#28
H_A#_29	B15	H_A#29
H_A#_30	E17	H_A#30
H_A#_31	C18	H_A#31
H_A#_32	A19	H_A#32
H_A#_33	B19	H_A#33
H_A#_34	N19	H_A#34
H_A#_35		H_A#35

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<< H\_REQ#[4:0] >> H\_REQ#[4:0]

<< H\_D#[63:0] >> H\_D#[63:0]

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H_ADSTB#_1	A20	H_ADSTB#1
H_ADSTB#_2	C8	H_ADSTB#2
H_ADSTB#_3	E8	H_ADSTB#3
H_BPN#	F12	H_BPN#
H_BREQ#	D6	H_BREQ#
H_DEFER#	G10	H_DEFER#
H_DBSY#	AMS	H_DBSY#
HPLL_CLK#	JAM	HPLL_CLK#
H_DPWR#	R6	H_DPWR#
H_DRDY#_0	K7	H_DRDY#0
H_DRDY#_1	E4	H_DRDY#1
H_DRDY#_2	E4	H_DRDY#2
H_HIT#	G8	H_HIT#
H_HITM#	G8	H_HITM#
H_LOCK#	G10	H_LOCK#
H_TRDY#	R7	H_TRDY#

1.1

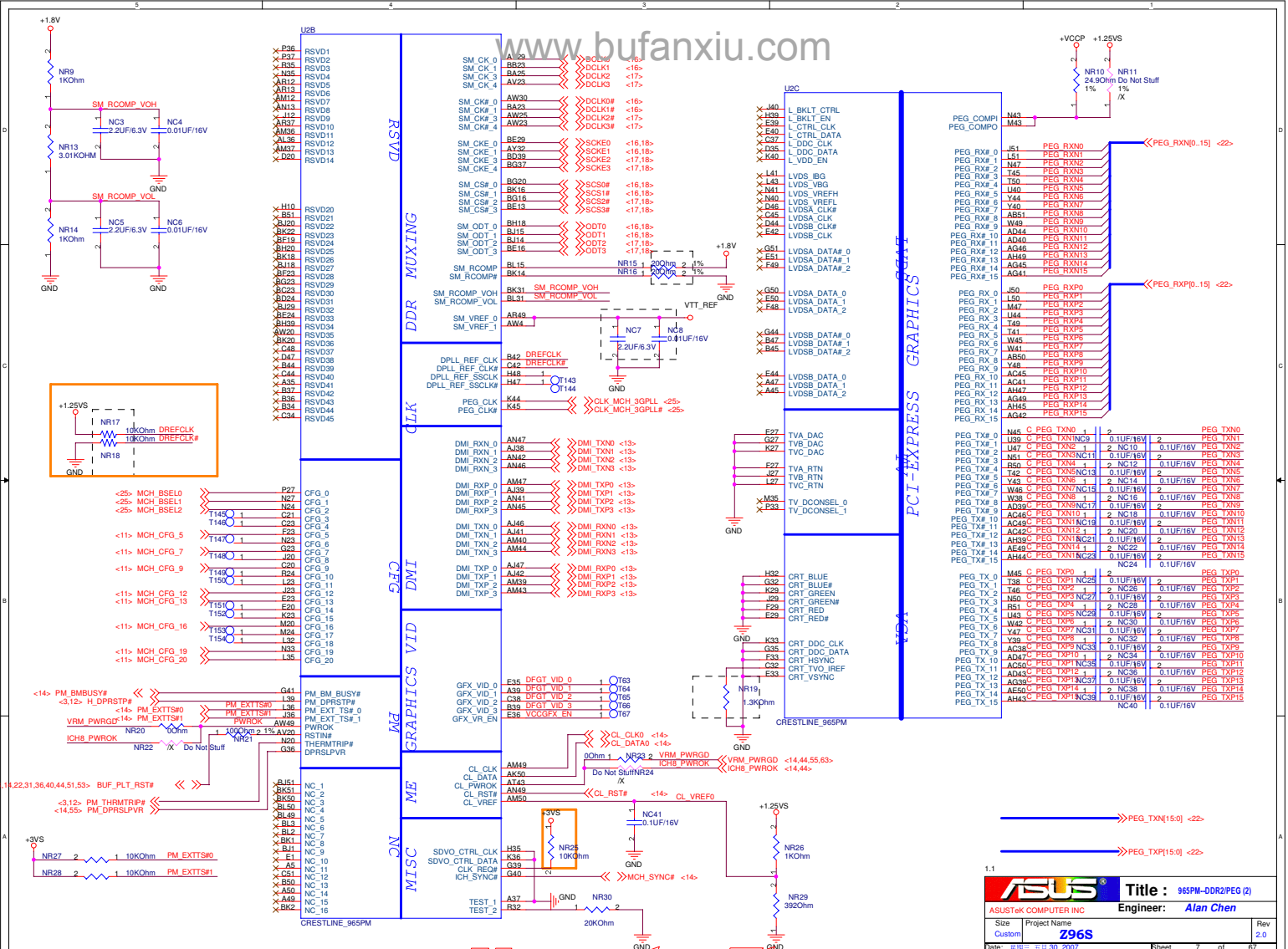
**ASUS** Title : 965PM - CPU (1)

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

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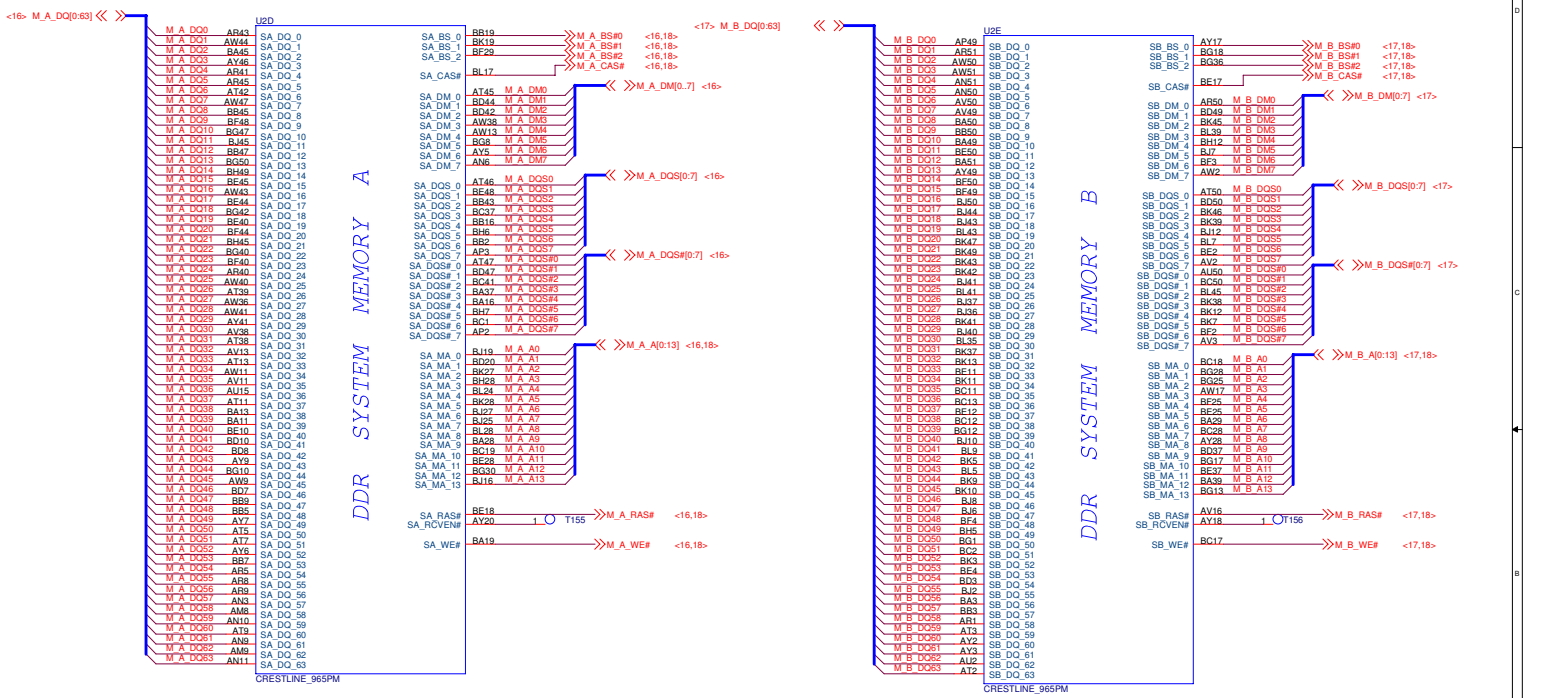
ASUS Title : 965PM-DDR2PEG (2)

ASUSTeK COMPUTER INC Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

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1.1

**ASUS** Title : 965PM-DDR2 bus (3)

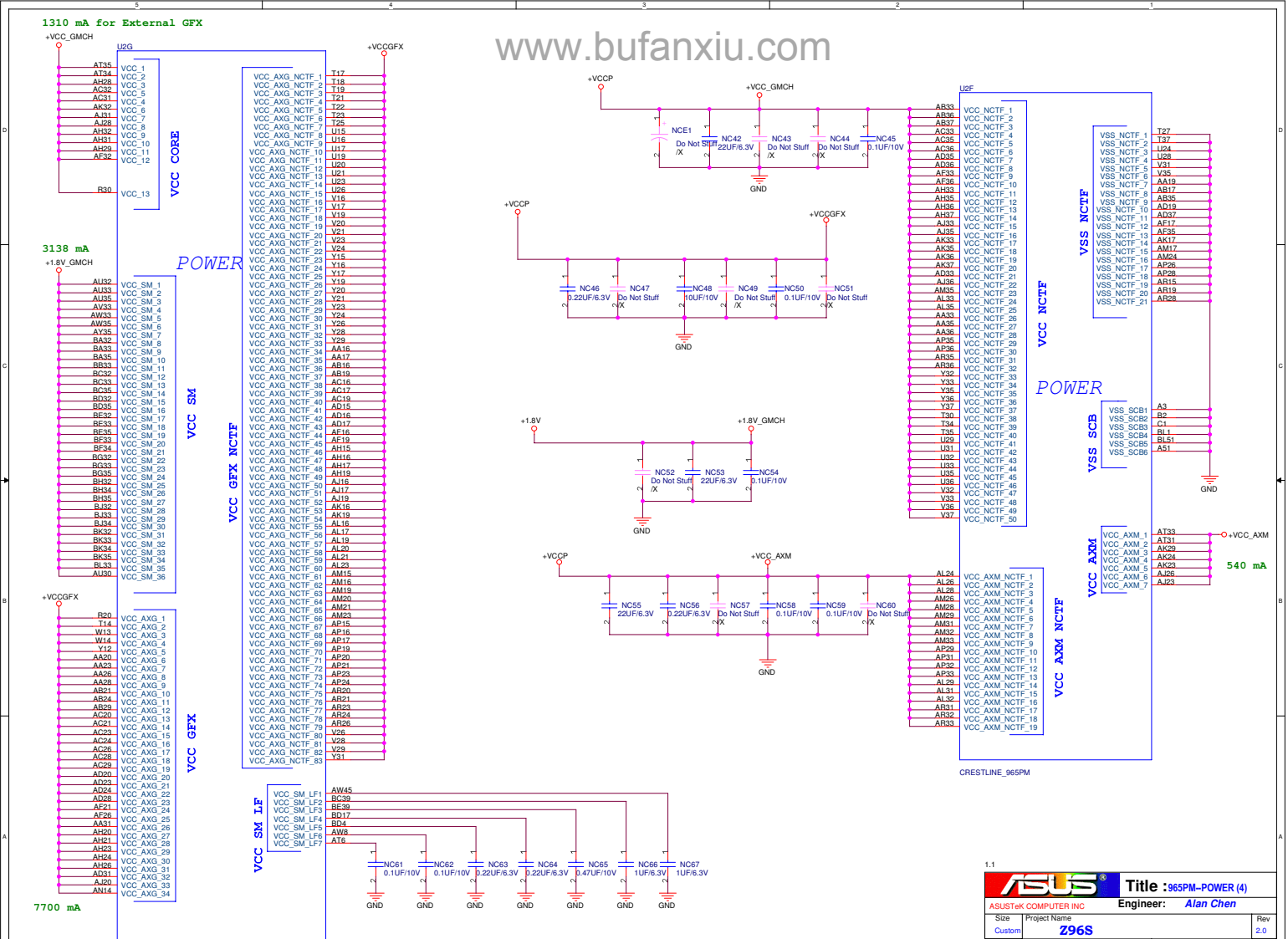
ASUSTeK COMPUTER INC Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

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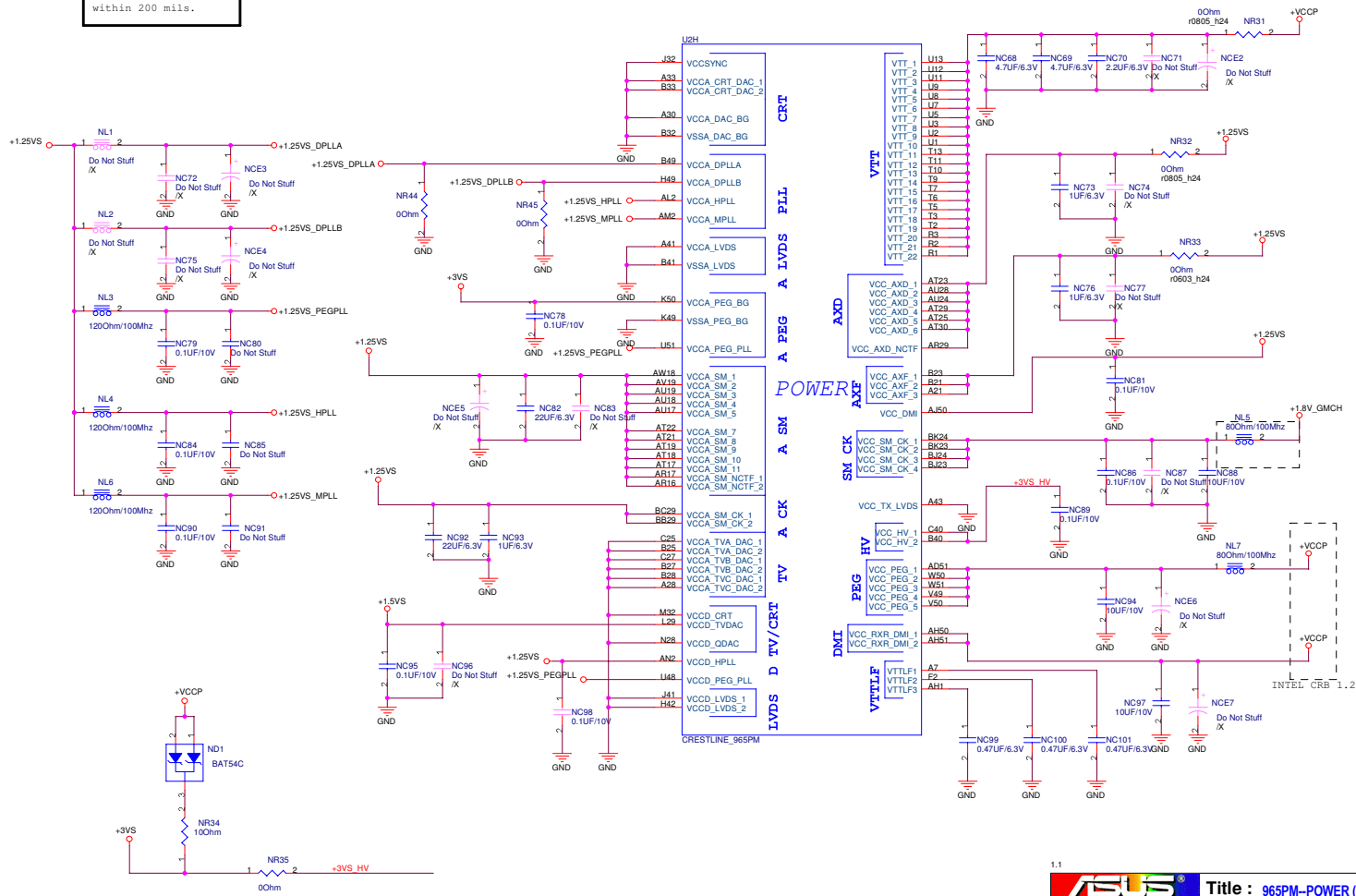




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1.1		<b>ASUS</b> Title :965PM-POWER (4)	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		
Custom	<b>Z96S</b>		Rev 2.0
Date: 2007.07.30		Sheet 9	of 67

NOTE:0.1uF caps in 1.5VS\_XPLL need to be located as edge caps within 200 mils.



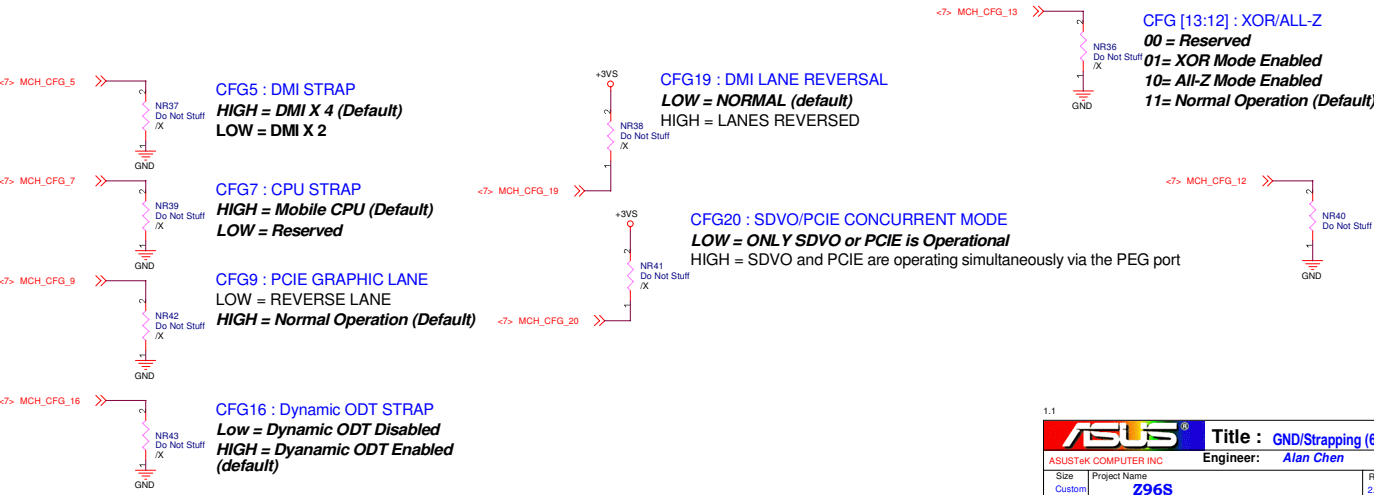
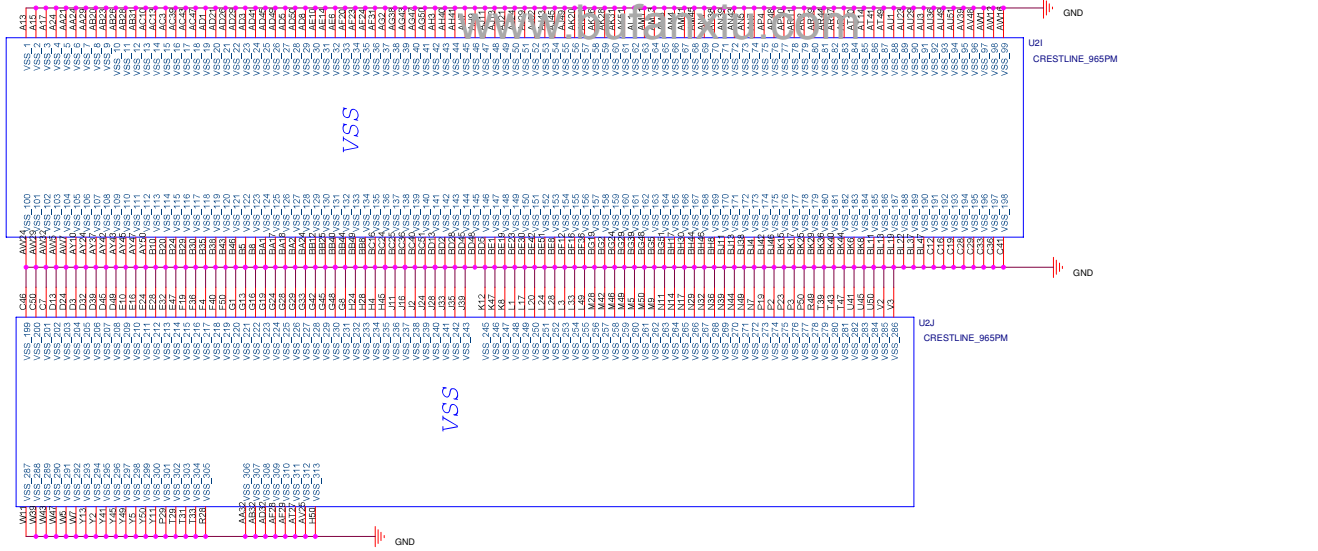
1.1

**ASUS** Title : 965PM-POWER (5)

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0
Date: 07-11-30-2007	Sheet	10 of 87

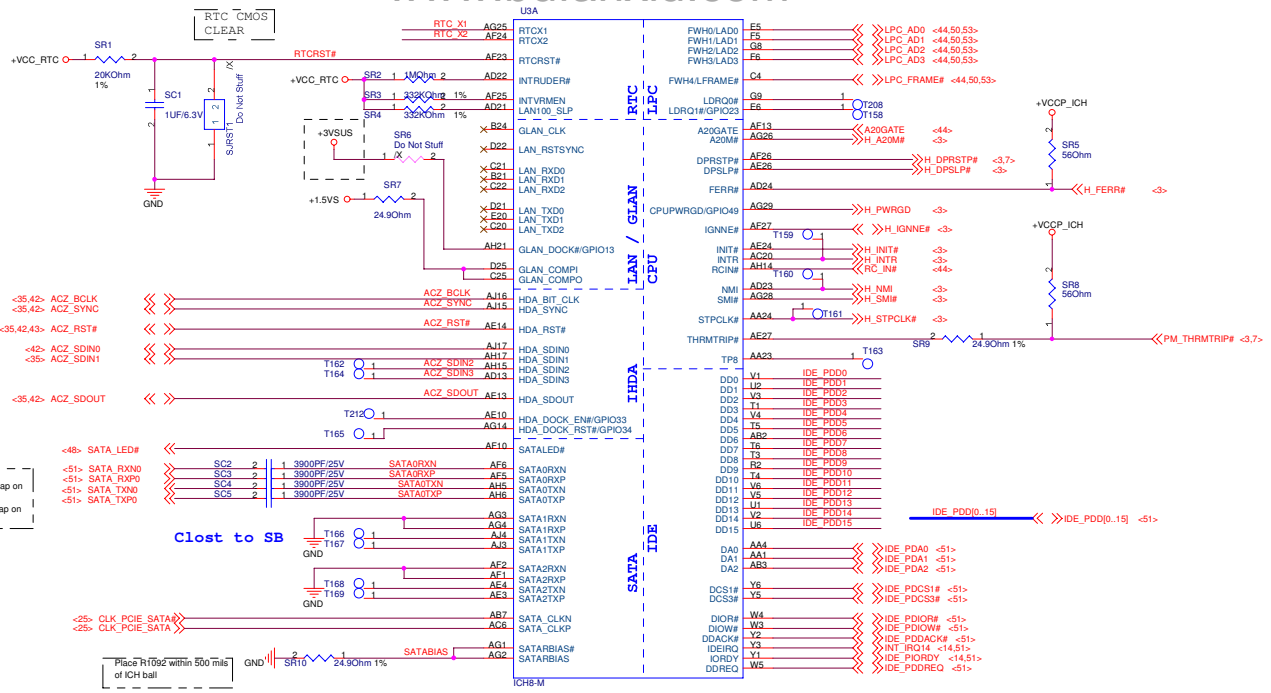
« Kennedy\_Zhang » HIGH-LANES REVERSED



1.1

<b>ASUS</b>		<b>Title : GND/Strapping (6)</b>	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007-11-30 2007		Sheet	11 of 87

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SATA:  
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

- <48> SATA\_LED#
- <51> SATA\_RXN0
- <51> SATA\_RXP0
- <51> SATA\_TXN0
- <51> SATA\_TXP0

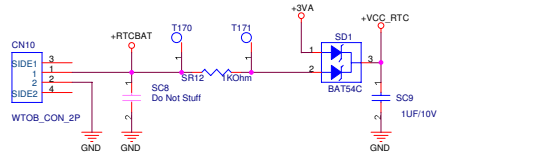
Close to SB

- <25> CLK\_PCIE\_SATA
- <25> CLK\_PCIE\_SATA

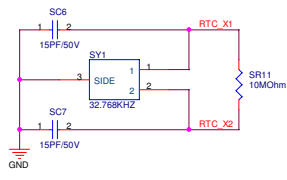
Place R1092 within 500 mils of ICH ball

SATA if it non-used,  
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA\_CLKpn should be PD.  
2)SATA[0:3]TXpn and SATALED# NO connect.

RTC BAT

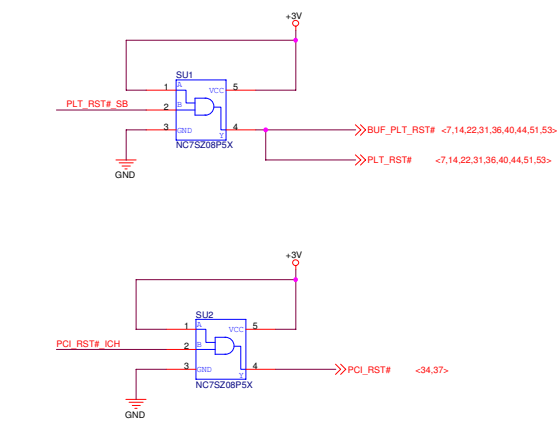
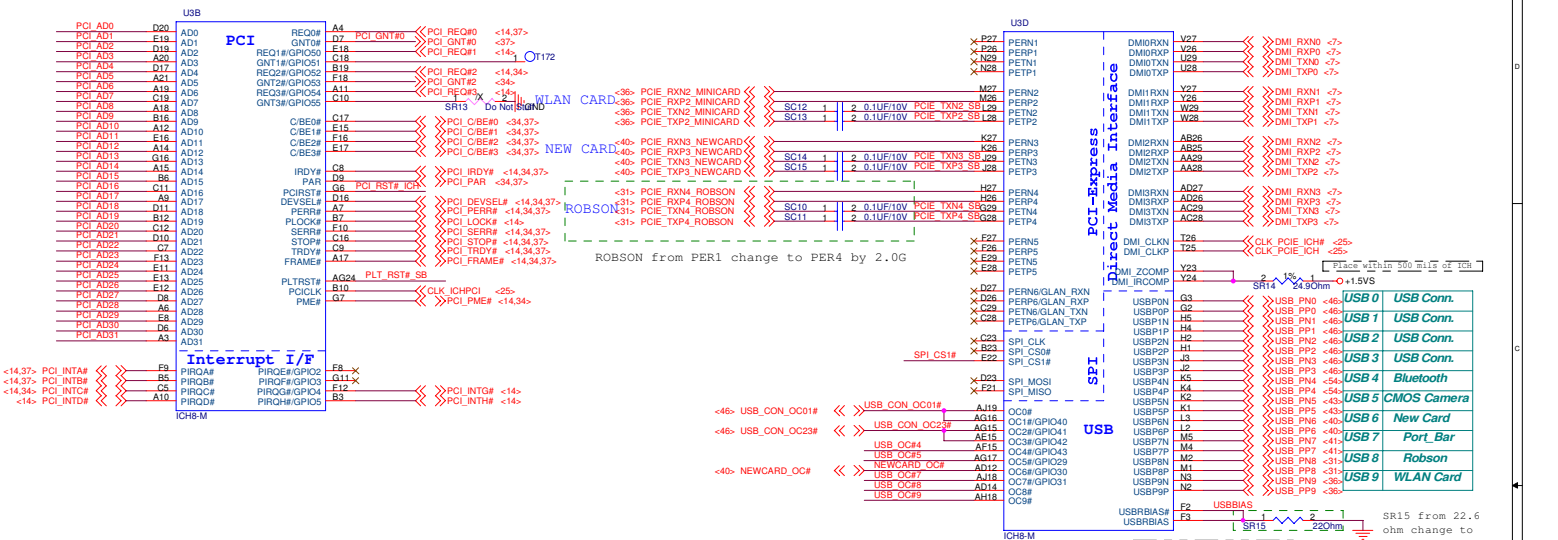


RTC Battery  
P/N=07-016322032



ASUS		Title : ICH8-M (1)	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 星期二, 7月30, 2007	Sheet	12	of 67

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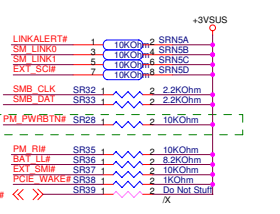
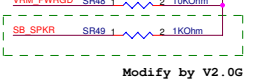
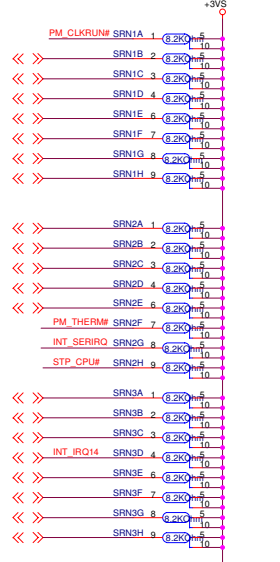
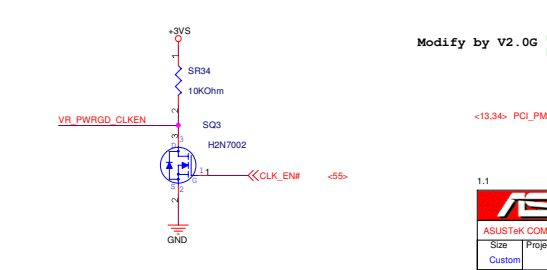
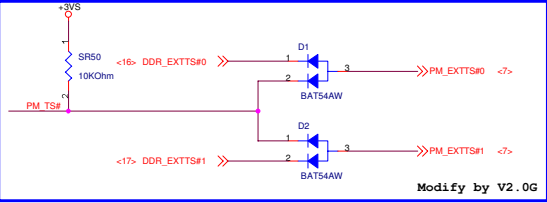
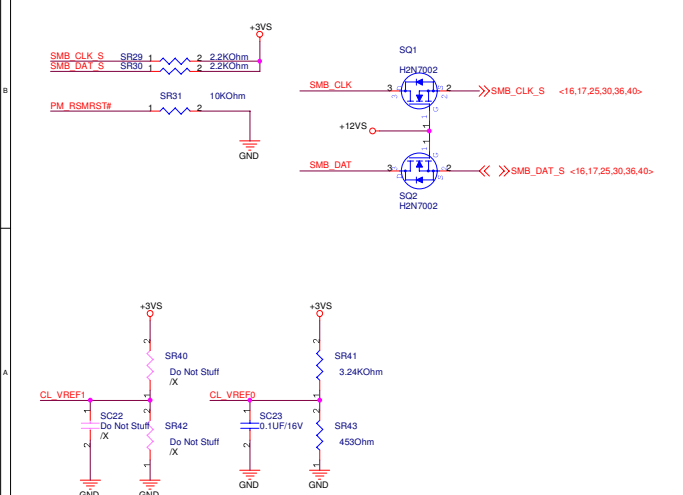
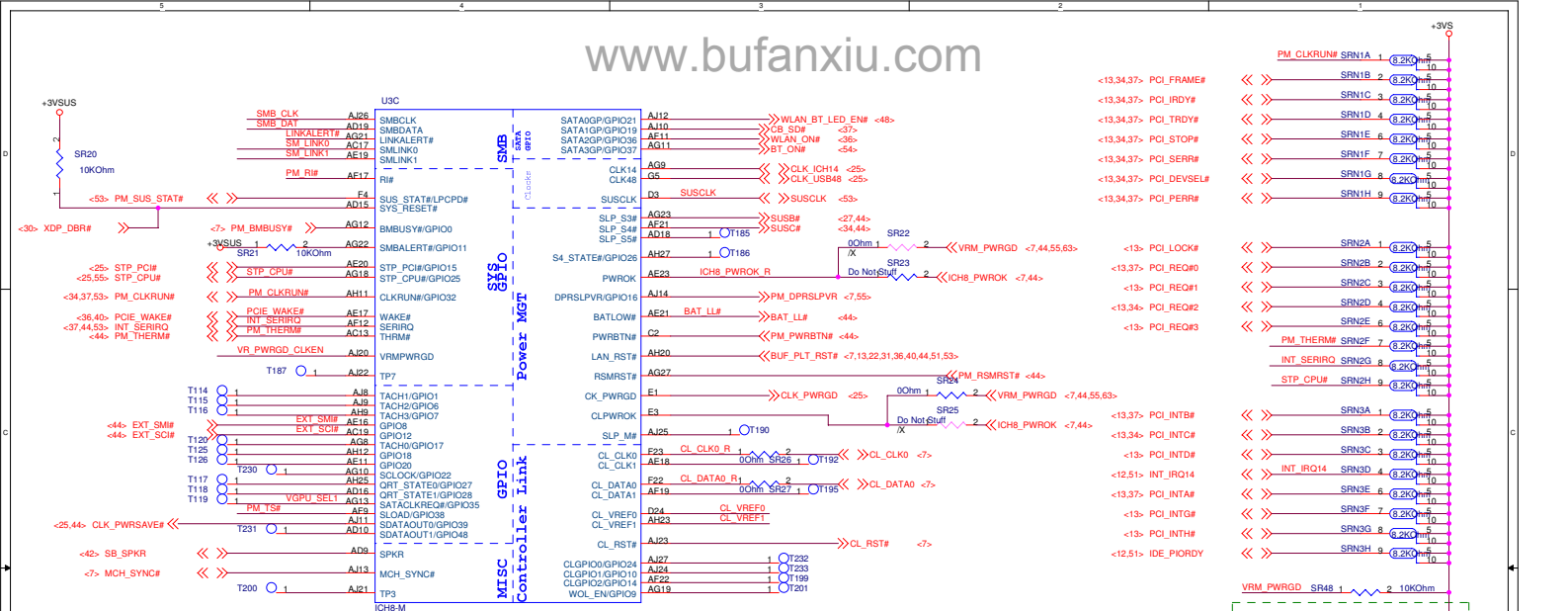
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	Bluetooth
USB 5	CMOS Camera
USB 6	New Card
USB 7	Port_Bar
USB 8	Robson
USB 9	WLAN Card

ICH8 Boot BIOS select

GPIO	CS#1#	(default)
GPIO 11	1	1
GPIO 10	1	0
GPIO 01	0	1

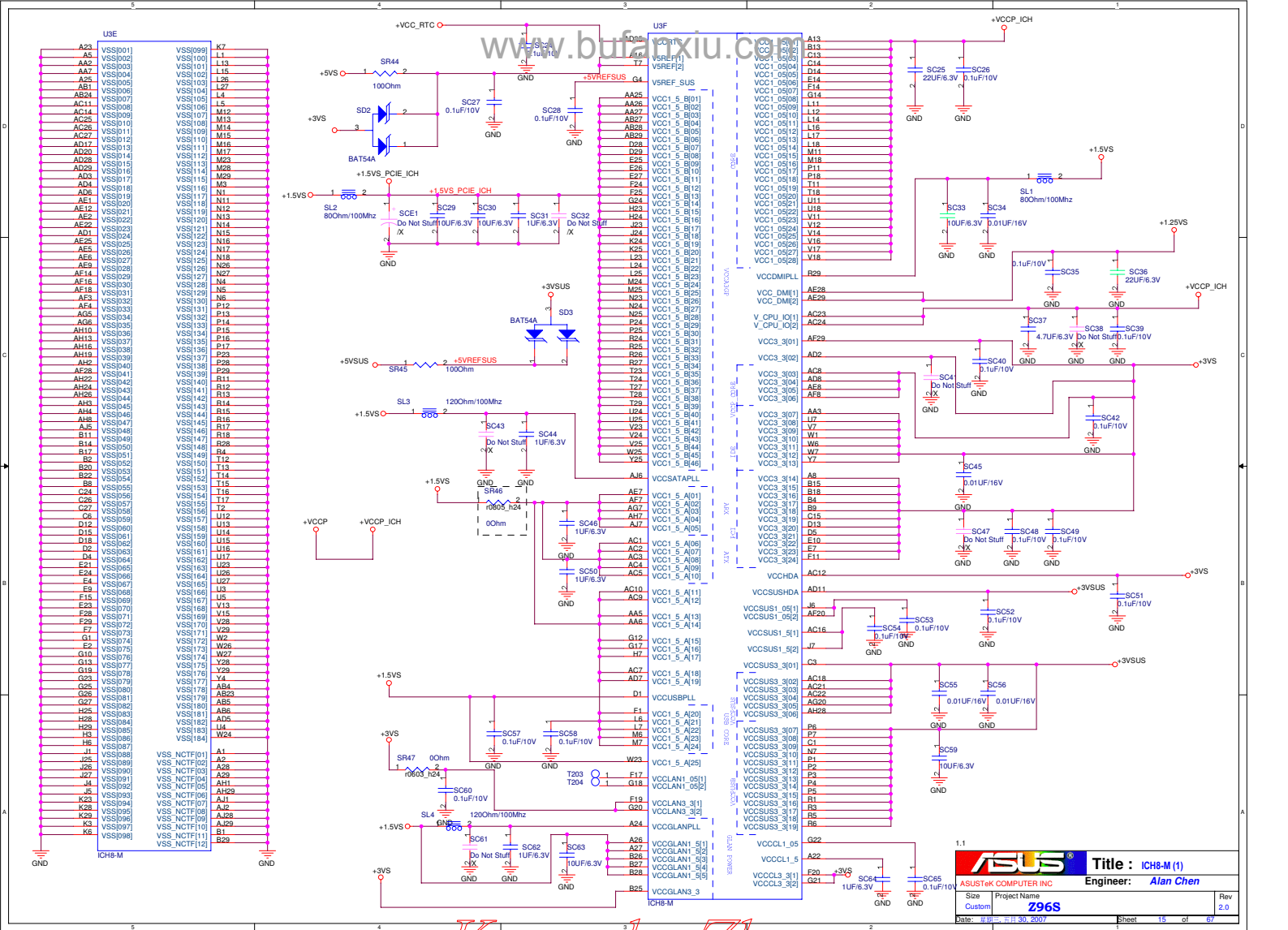
**ASUS** Title : ICH8-M (1)  
 ASUSTeK COMPUTER INC. Engineer: Alan Chen  
 Size Custom Project Name Z96S  
 Date: 01/11/30/2007 Sheet 13 of 87

<< Kennedy\_Zhang >>



<b>ASUS</b>		<b>Title : ICH8-M (3)</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Custom	Rev
296S	296S	2.0	2.0
Date: 2007.10.30	Sheet	14	of 67

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« Kennedy\_Zhang »

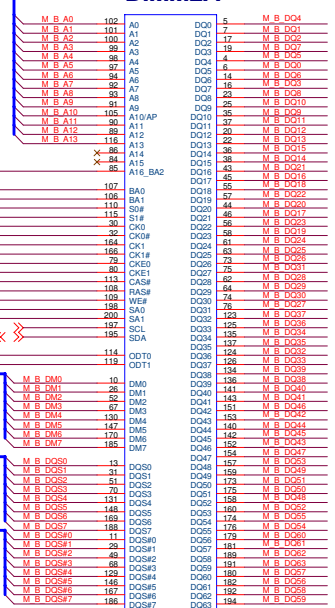




STD Type

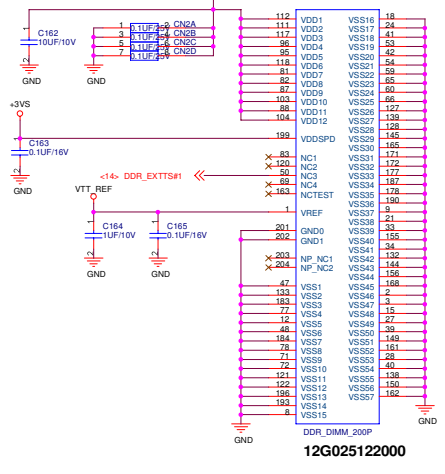


### DIMM2A



DDR\_DIMM\_200P  
12G025122000

### DIMM2B



DDR\_DIMM\_200P  
12G025122000

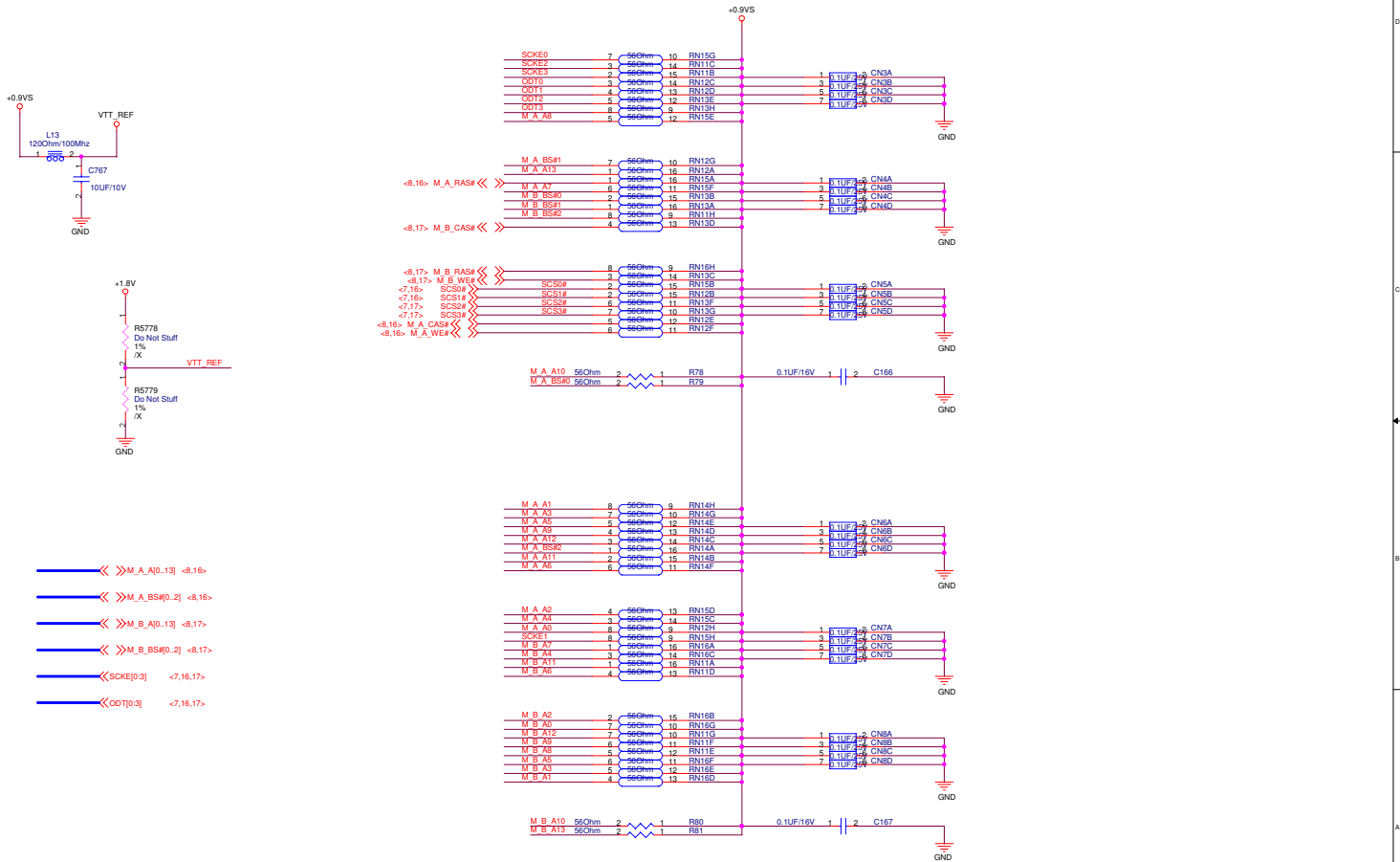
1.1

**ASUSTeK COMPUTER INC. NB1** **ASUS** **Title : DDR2 SO-DIMM1**  
 Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 01/10/2007 Sheet: 17 of 97

<< Kennedy\_Zhang >>



1.1

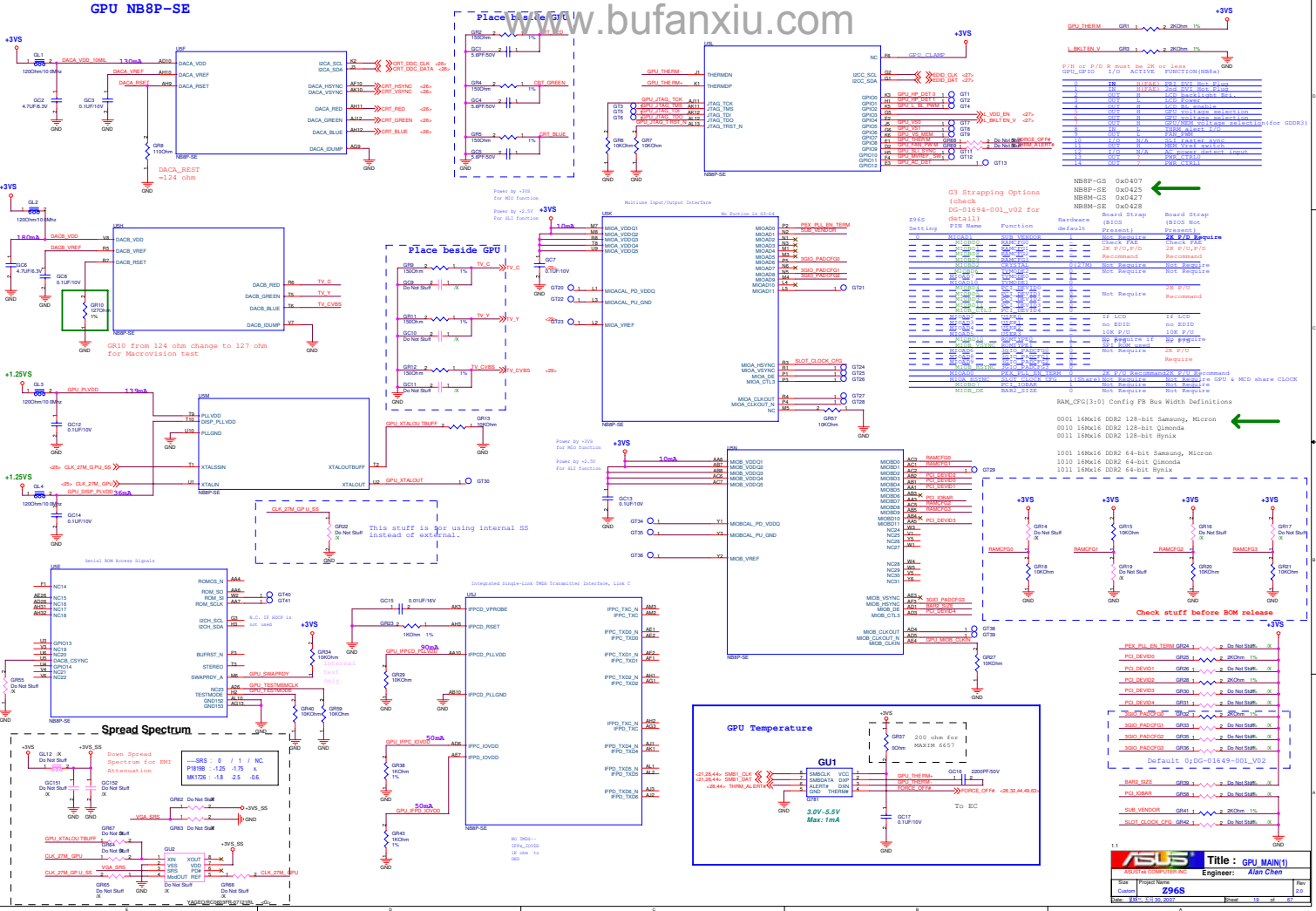
**ASUS** Title : DDR2 TERMINATION  
 ASUSTek COMPUTER INC. NB1 Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0
Date: 11/13/2007	Sheet 18 of 87	

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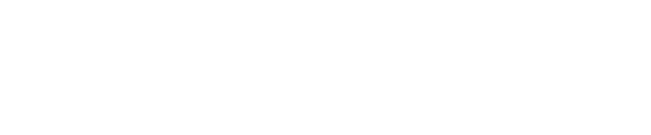
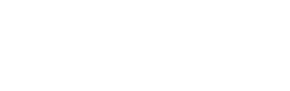
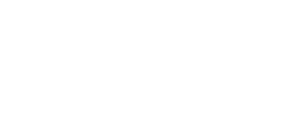
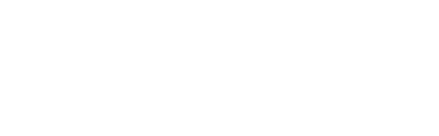
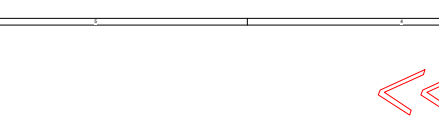
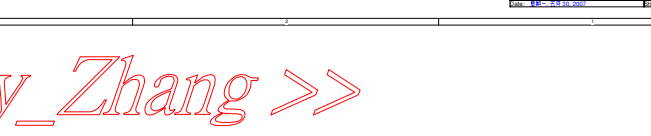
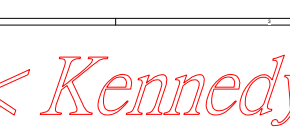
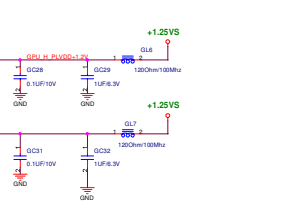
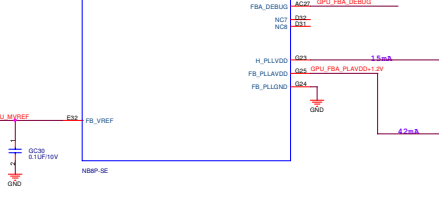
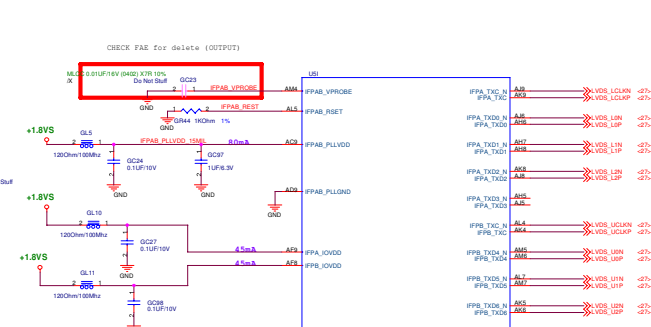
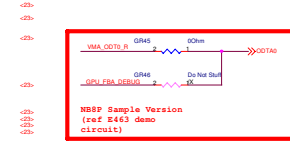
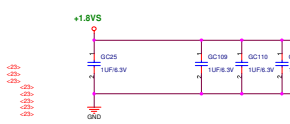
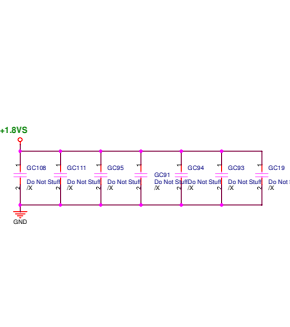
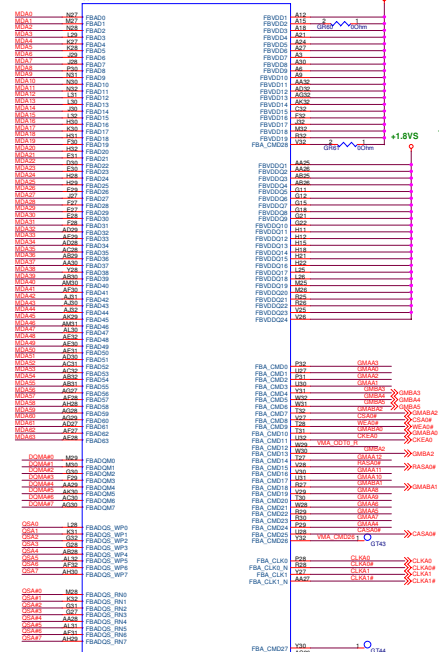
**GPU NB8P-SE**

www.bufanxiu.com

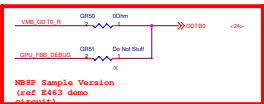
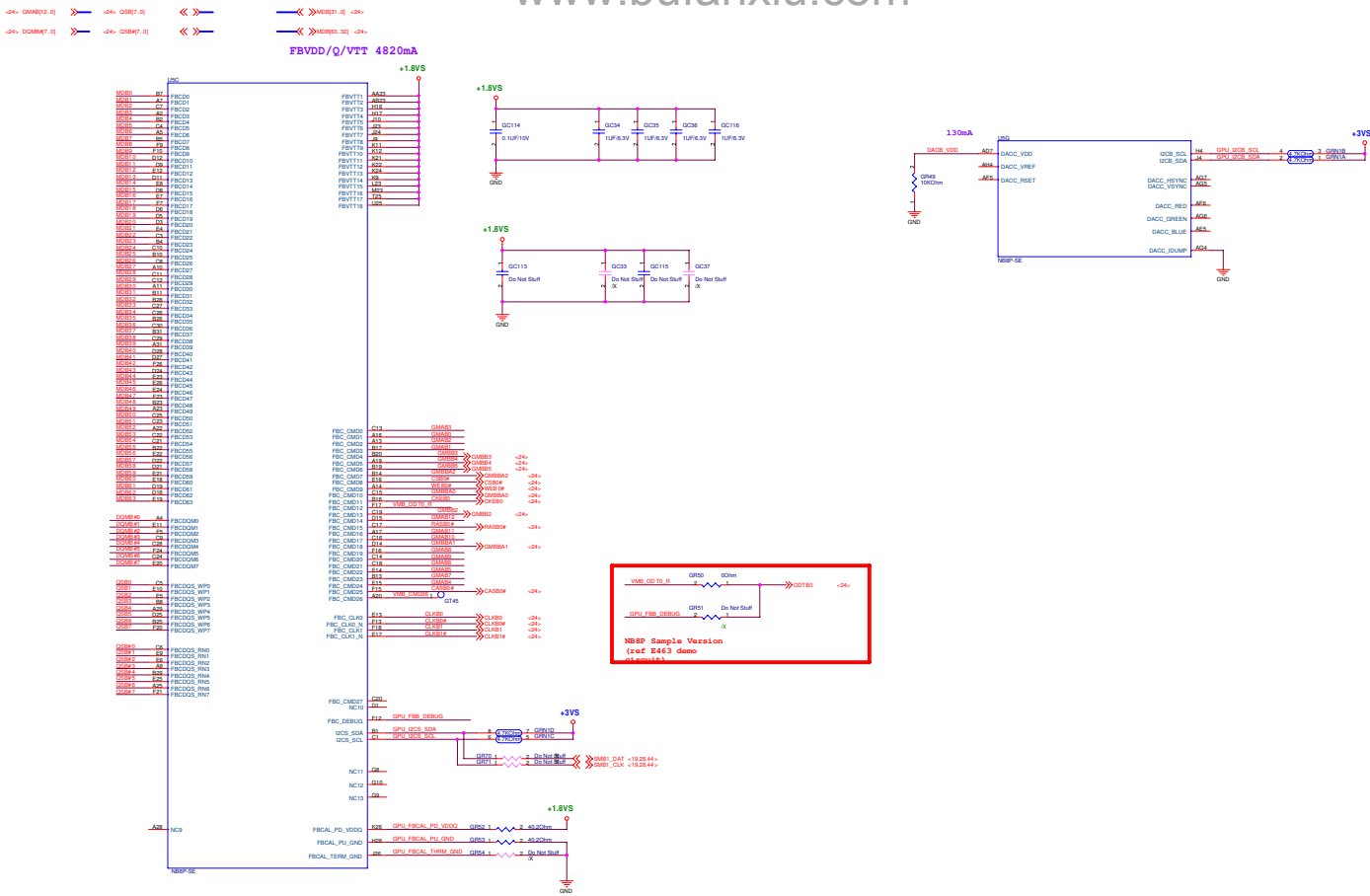


<< Kennedy\_Zhang >>

<< GMA12.0 >> << GMA7.0 >> << GMA3.2 >> << GMA2.0 >>

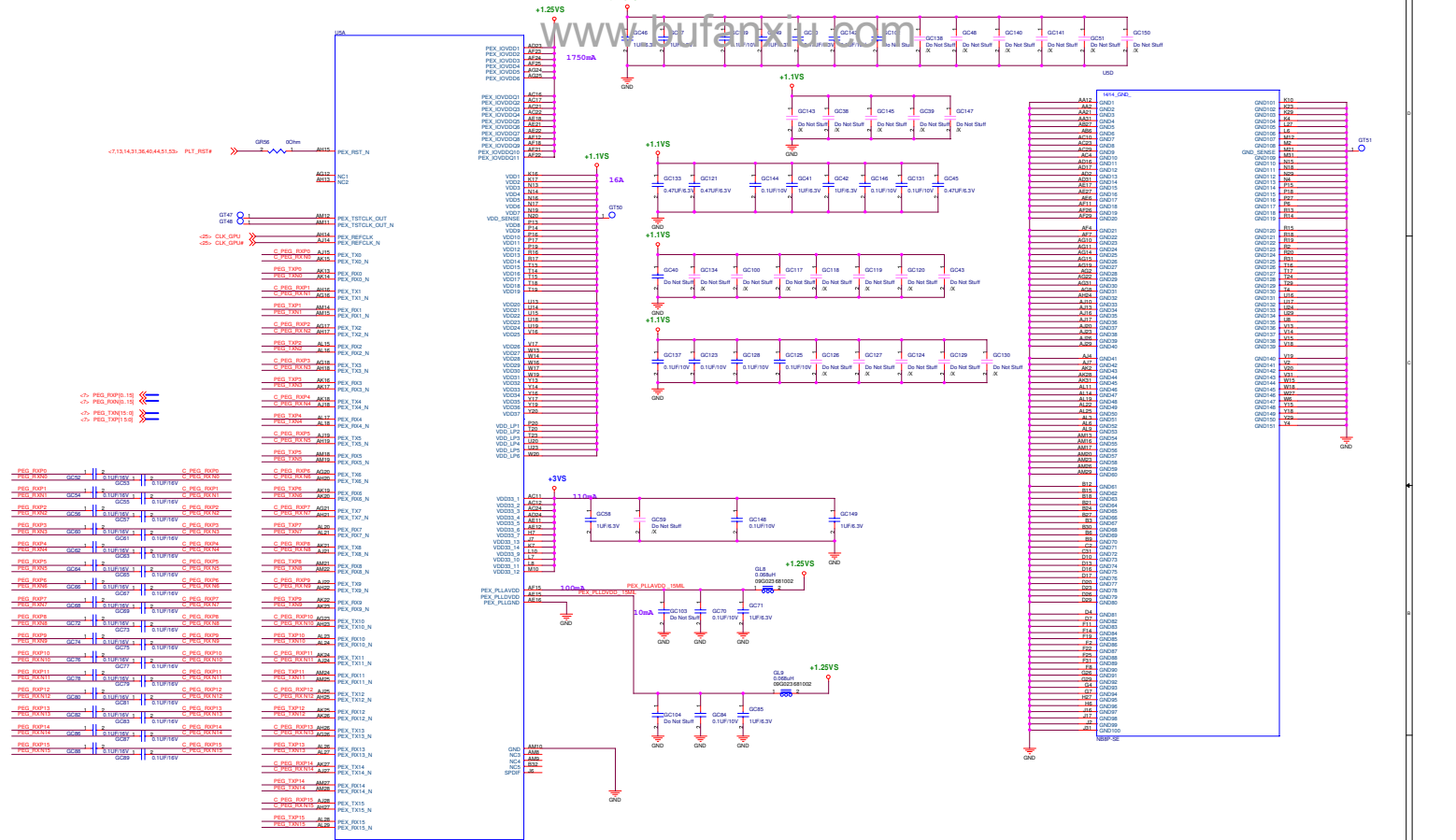


<< Kennedy\_Zhang >>



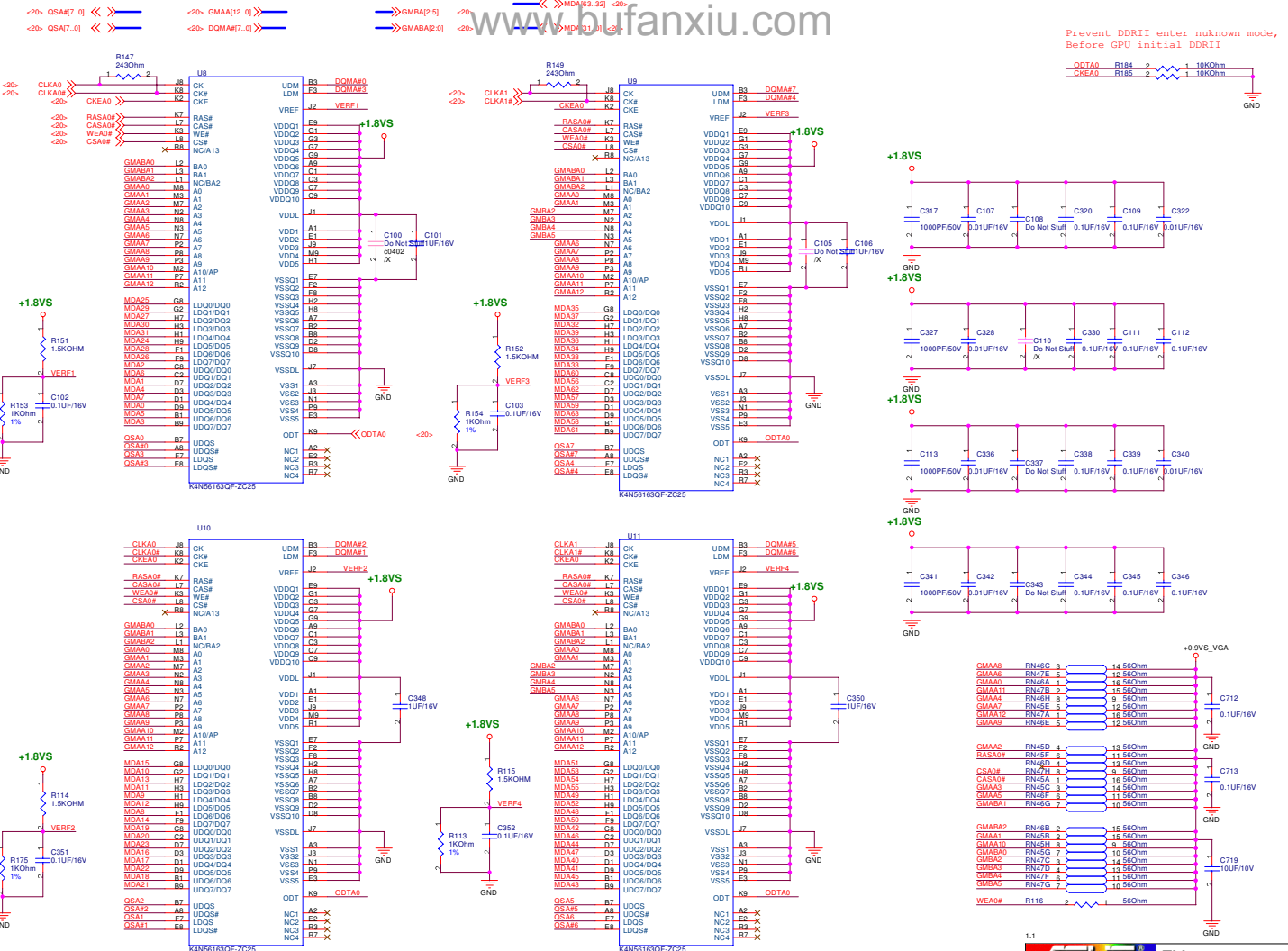
ASUS	Title: GPU PCI-E(3)
ASUSTAI COMPUTER INC.	Engineer: Alan Chen
Staff	Project Name:
Quantity	296S
Date: 10/23/2012	Page: 1/1

<< Kennedy\_Zhang >>



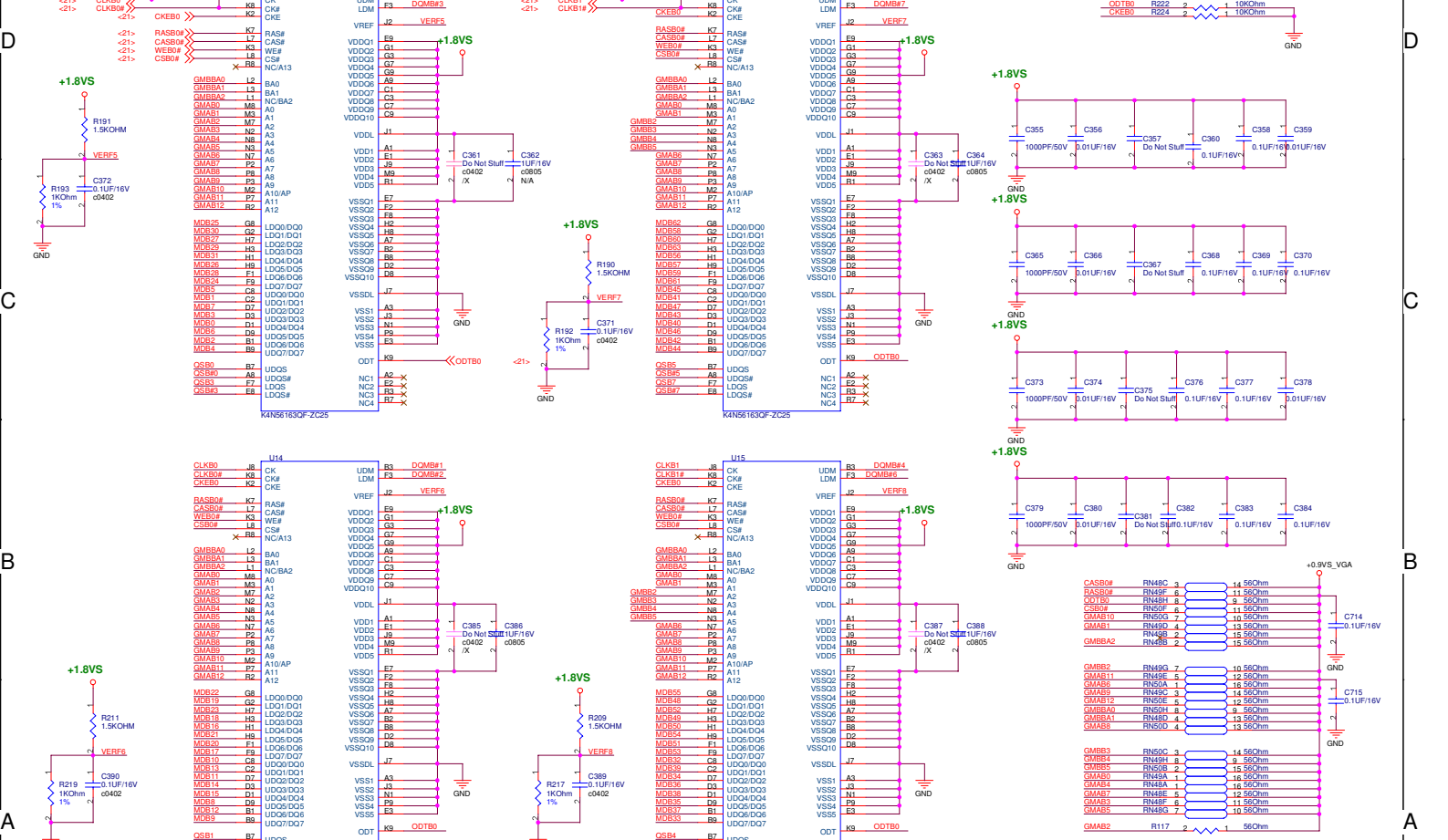
<< Kennedy\_Zhang >>

Prevent DDRII enter unknown mode, Before GPU initial DDRII



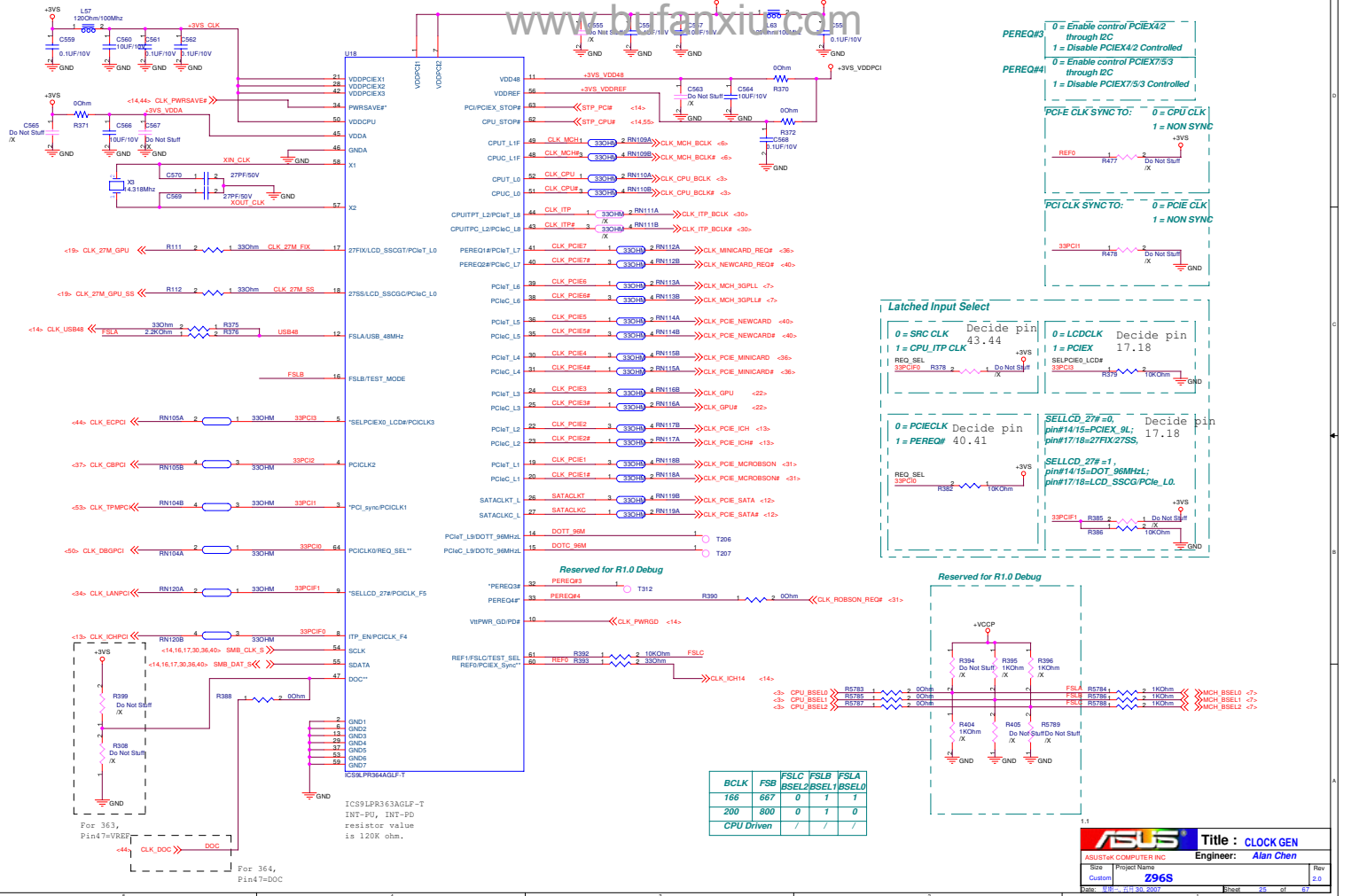
« Kennedy\_Zhang »

		<b>Title: VRAM_A(5)</b>	
		ASUSTek COMPUTER INC	Engineer: Alan Chen
Size	Project Name	296S	Rev 2.0
Custom			
Date: 2007-11-30	Sheet 23	of 67	



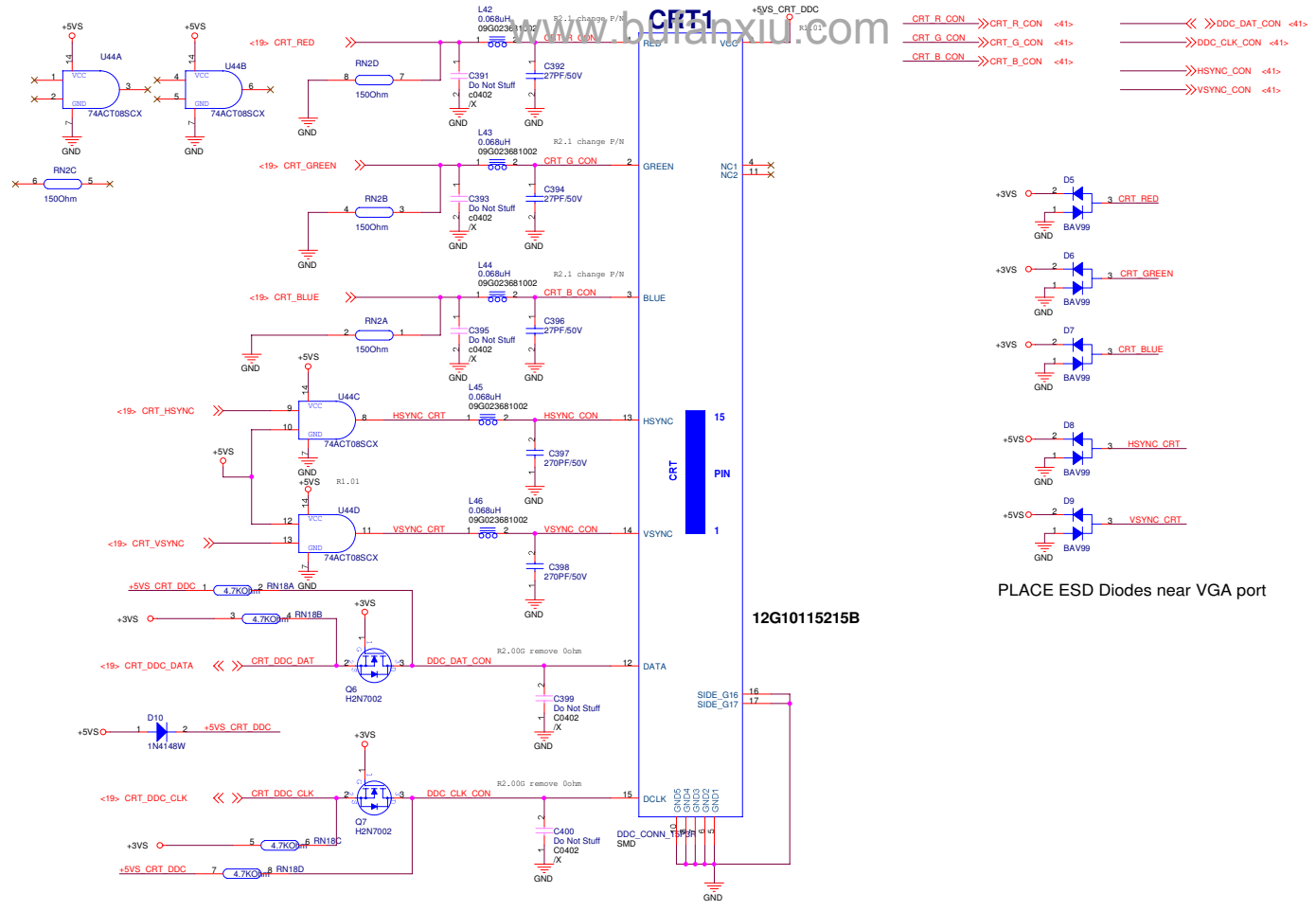
ASUS	Title : VRAM_A(6)
ASUSTek Computer INC.	Engineer: Alan Chen
Size : Project Name	Rev
Custom : Z96S	2.0
Date: 11/11/2011	Sheet 24 of 87



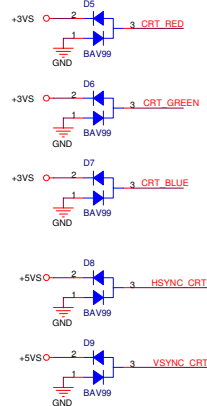


**ASUS** Title : CLOCK GEN  
 ASUSTeK COMPUTER INC. Engineer: Alan Chen  
 Project Name: Custom 296S  
 Rev: 2.0  
 Date: 11/13/2007

<< Kennedy\_Zhang >>



PLACE ESD Diodes near VGA port



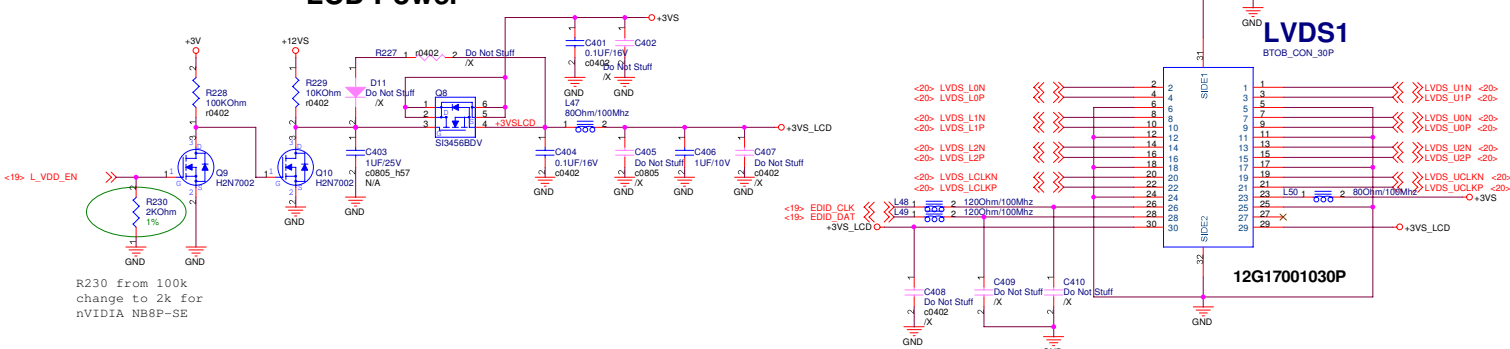
ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 01/30/2007		Sheet 26	of 67

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# LCD Backlight Control

# LCD LVDS Interface

## LCD Power

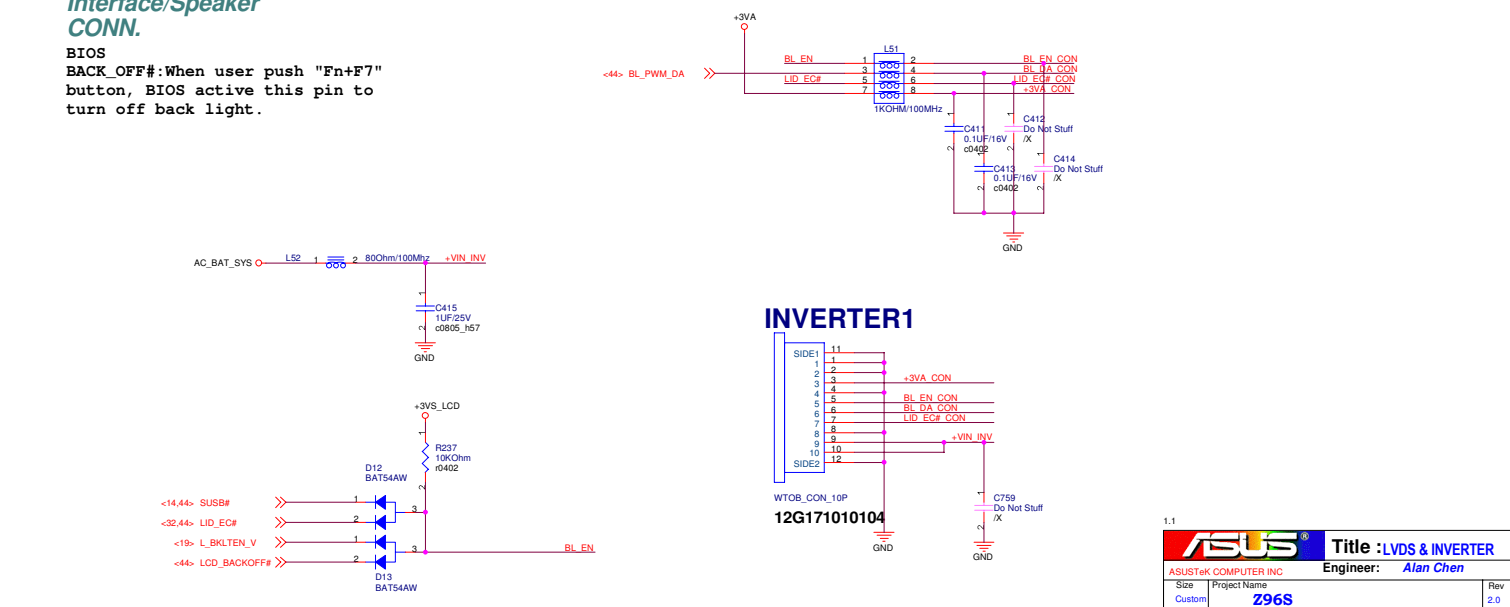


Sable Requirements:  
Impedance = 100 Ohm +/- 10%  
Length Mismatch <= 10 mils  
Twisted Pair(Not Ribbon)  
Maximum Length <= 16"

R230 from 100k change to 2k for NVIDIA NB8P-SE

## INVERTER Interface/Speaker CONN.

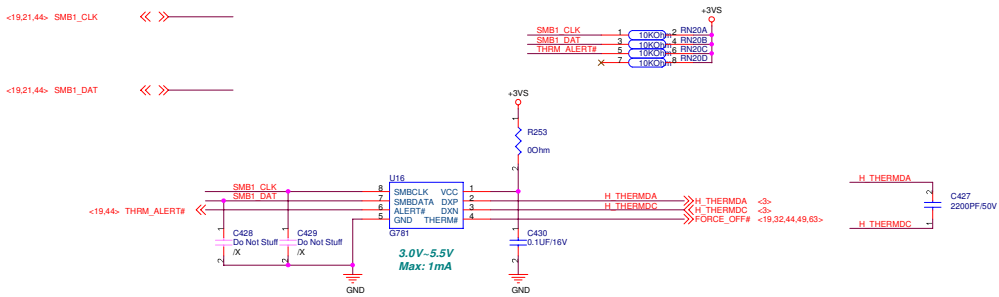
BIOS  
BACK\_OFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.



ASUS		Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007.07.30		Sheet 27	of 67

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**Thermal Sensor**

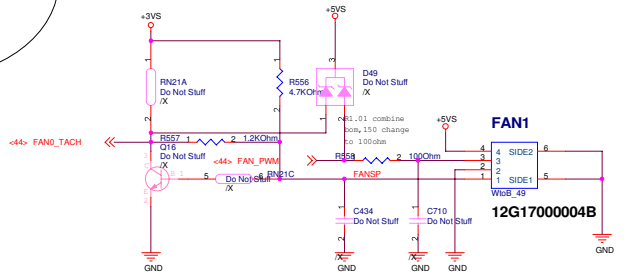
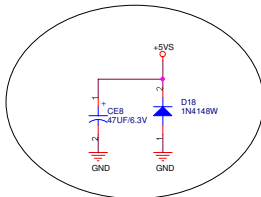


Route H\_THERMDA and H\_THERMDC on the same layer

OTHER SIGNALS  
 15 mils  
 =====GND  
 10 mils  
 =====H\_THERMDA(10 mils)  
 10 mils  
 =====H\_THERMDC(10 mils)  
 10 mils  
 =====GND  
 15 mils  
 -----OTHER SIGNALS

Avoid FSB,Power

**DC FAN Control**

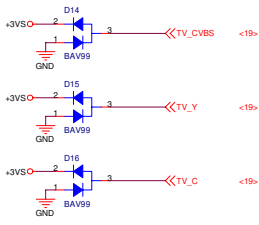


CPU FAN will be forced on:  
 1) Thermal Sensor Over-temperature  
 2) WATCHDOG asserted by EC

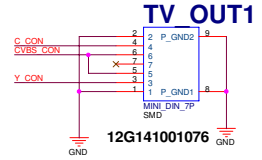
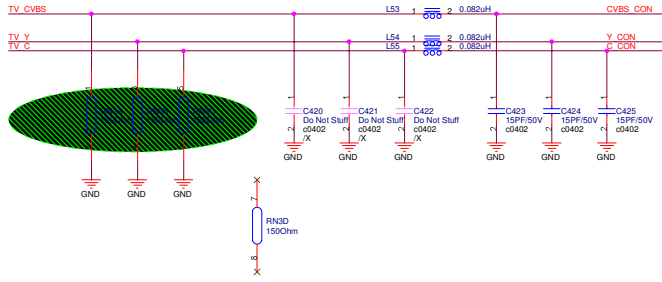
ASUS		Title : THER SENSOR & FAN	
ASUSTek COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	Rev
Custom	Z96S	2.0	2.0
Date: 11/13/2007	Sheet 28	of 87	

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TV OUT



PLACE ESD Diodes near TV port

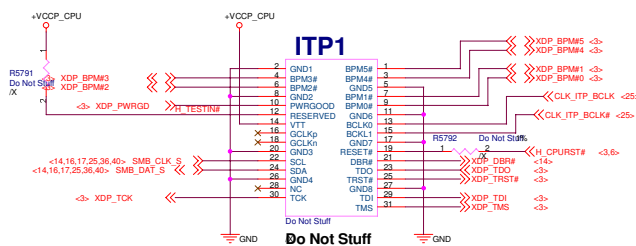


1.1

<b>ASUS</b>		<b>Title : TV OUT &amp; DVI CON.</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 29	of 67

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ITP

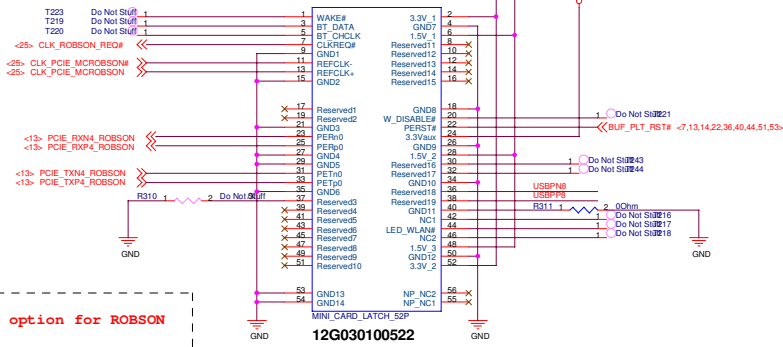


ASUS		Title : ITP	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/13/2011	Sheet	36	of 67

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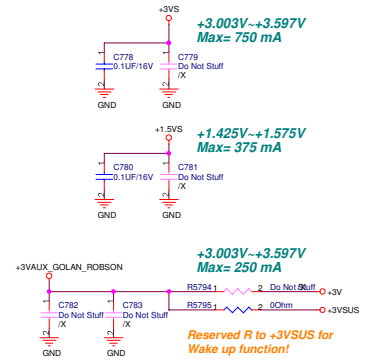
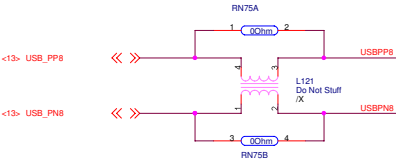
ROBSON

ROBSON1



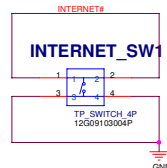
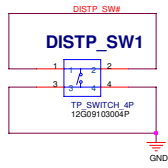
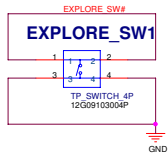
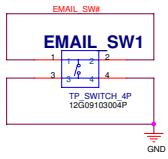
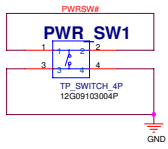
ES1 & ES2 option for ROBSON

	ES1	ES2
R310	N/A	Mount
R311	Mount	N/A

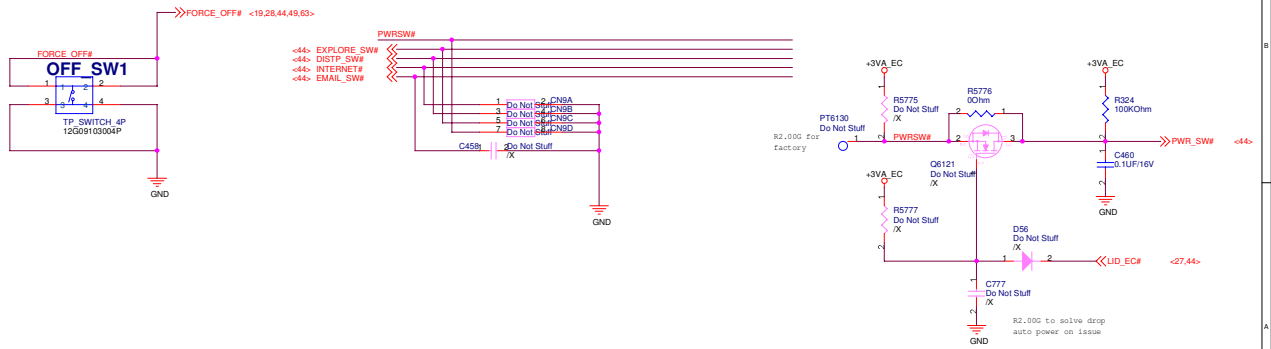


<b>ASUS</b>		<b>Title : Mini Card</b>	
ASUSTek Computer INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/21/2017	Sheet: 31	of 67	

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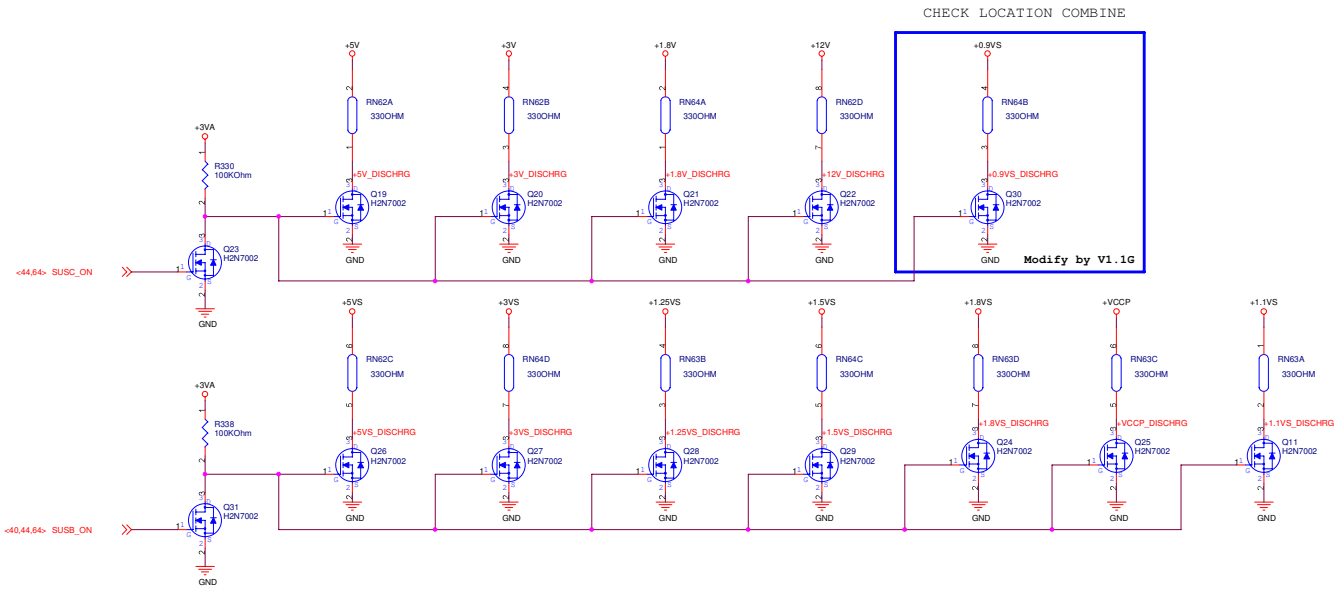
SHUT\_DOWN#



1.1		<b>ASUS</b> Title :Power on & Res Freq	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/13/2007	Sheet	32	of 87

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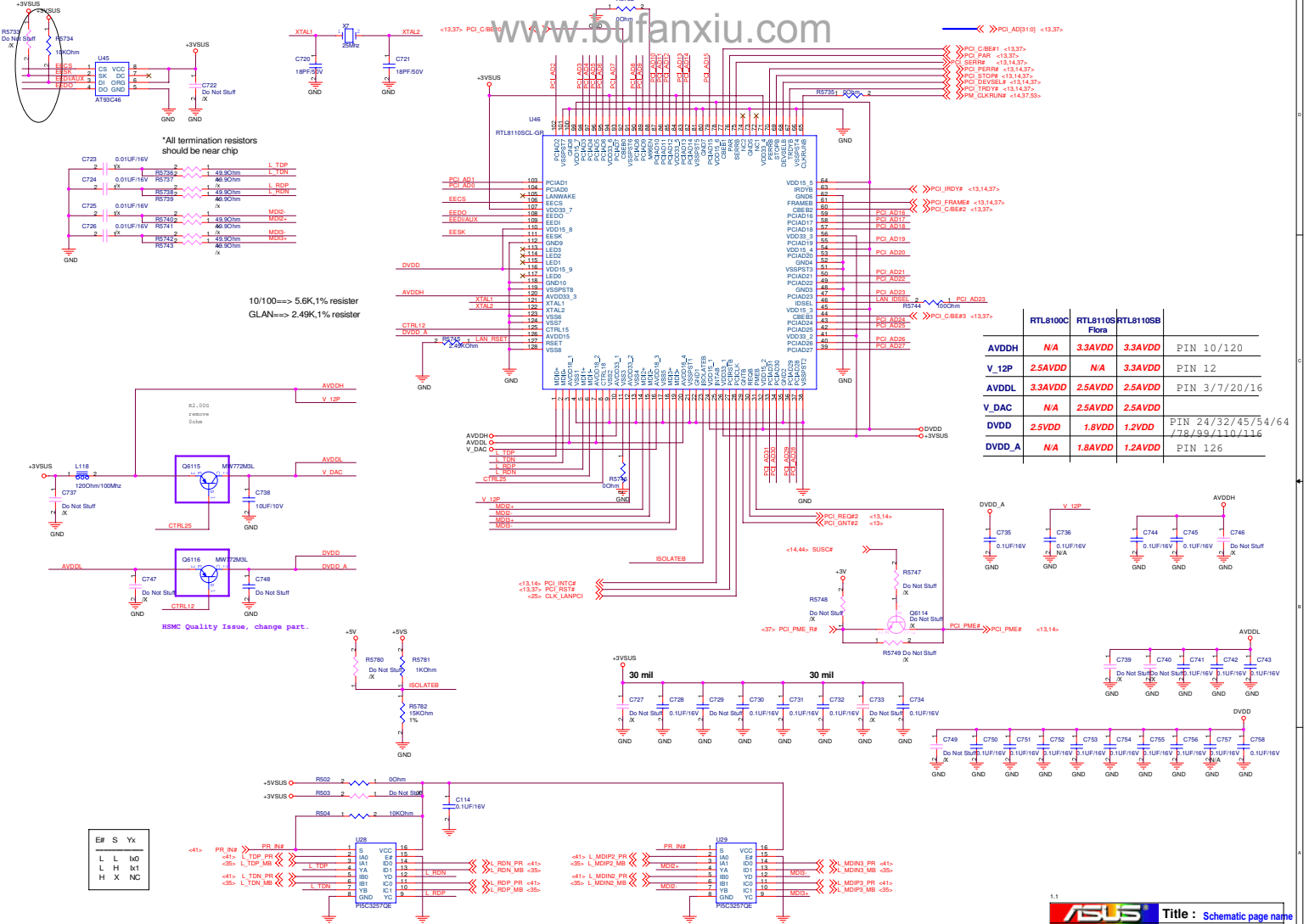




1.1

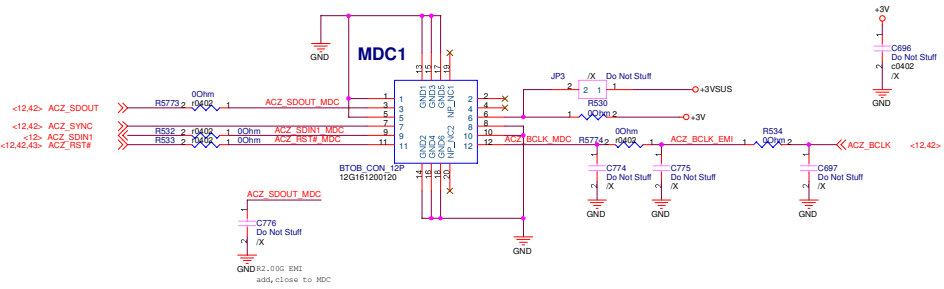
		<b>Title : DISCHARGE &amp; EMI CAP</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/11/2007		Sheet: 33	of 37

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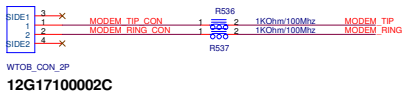


<< Kennedy\_Zhang >>

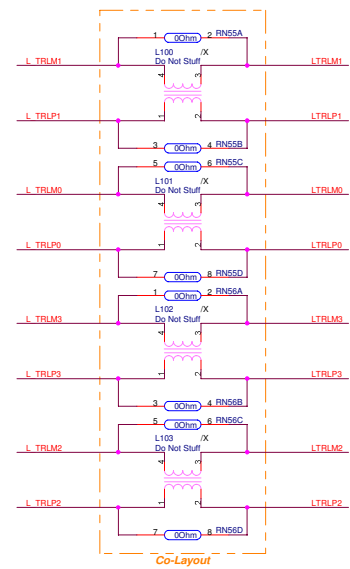
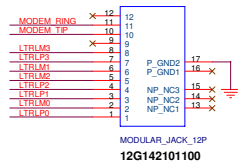
MDC CONN.



RING1



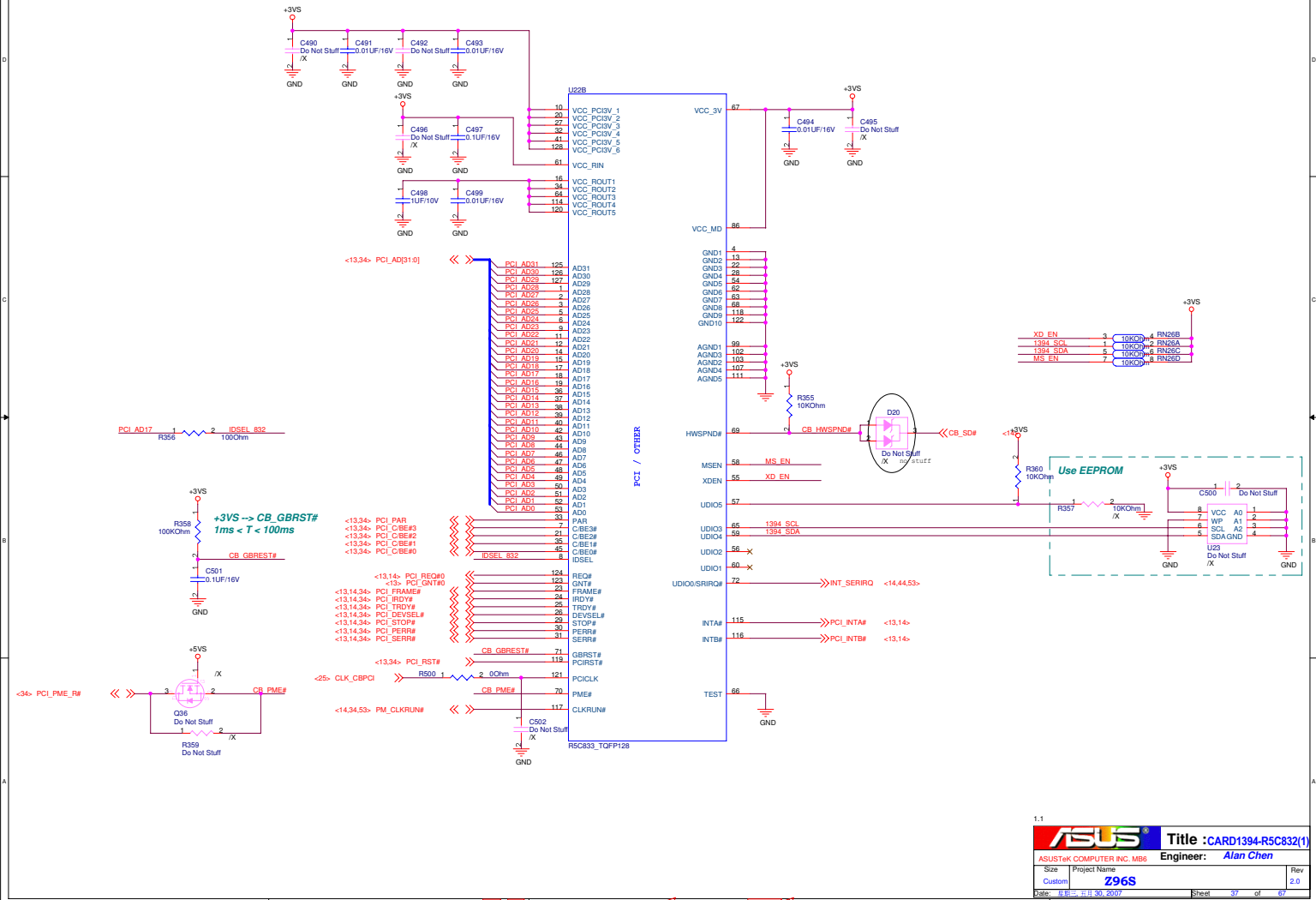
RJ45\_RJ11



ASUS		Title : RJ45&RJ11	
ASUSTEK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date	11/13/2007	Sheet	35 of 37

<< Kennedy\_Zhang >>

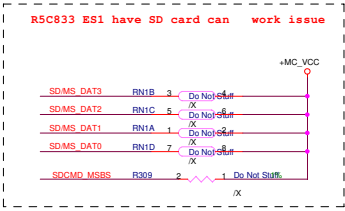
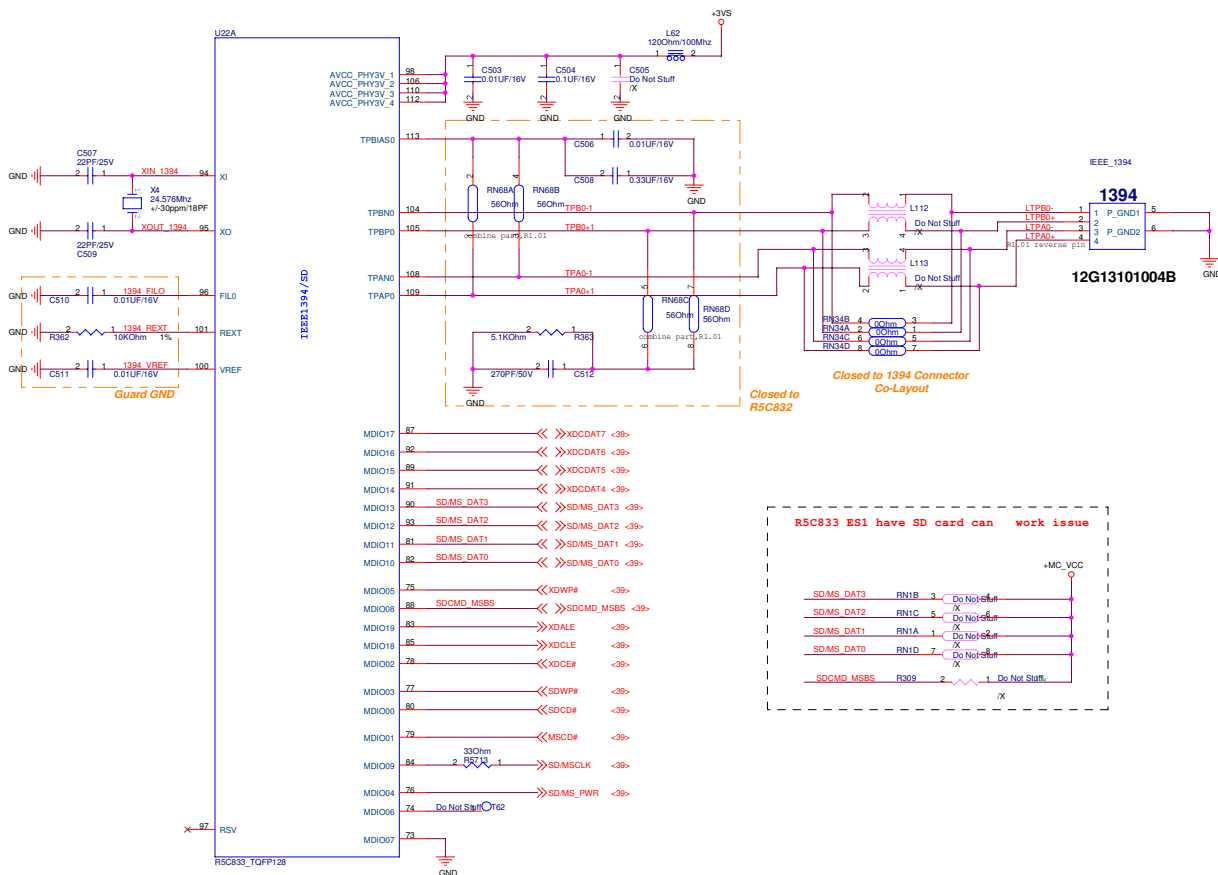




1.1

<b>ASUS</b>		<b>Title :CARD1394-R5C832(1)</b>	
ASUSTek COMPUTER INC. MBS		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/13/2007	Sheet	37	of 37

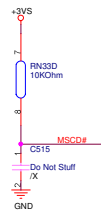
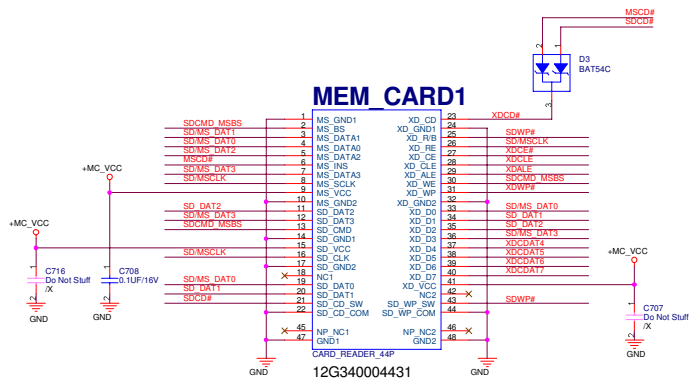
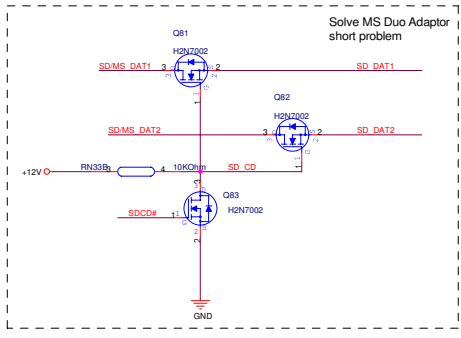
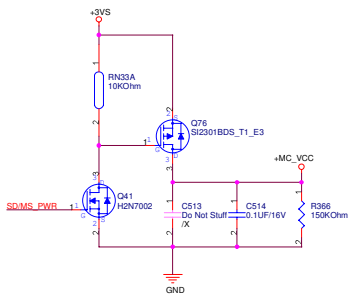
<< Kennedy\_Zhang >>



ASUS		Title : CARD1394-RSC832(2)	
ASUSTeK COMPUTER INC. MSB		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	Z96S	2.0	
Date: 11/30/2007	Sheet: 38	of	87

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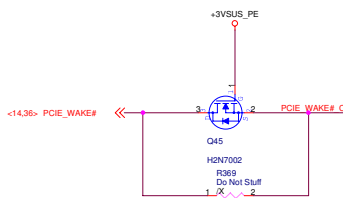
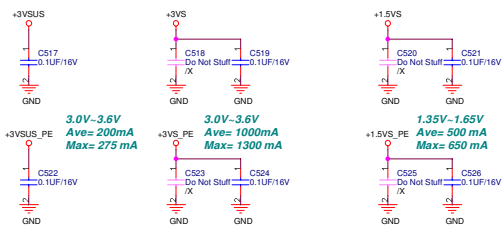
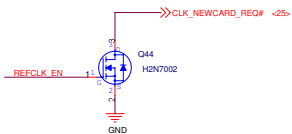
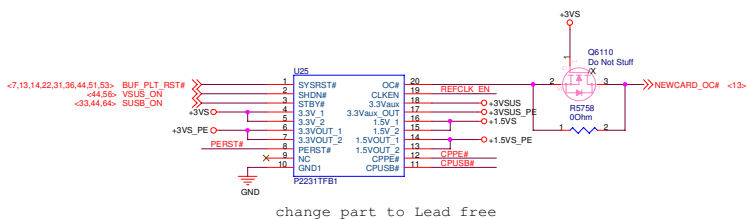
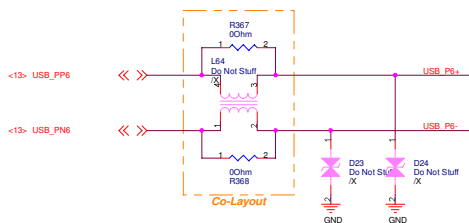
- << XDCDAT7 <-38>
- << XDCDAT6 <-38>
- << XDCDAT5 <-38>
- << XDCDAT4 <-38>
- << SDMS\_DAT3 <-38>
- << SDMS\_DAT2 <-38>
- << SDMS\_DAT1 <-38>
- << SDMS\_DAT0 <-38>
- << SDCMD\_MSBS <-38>
- << XDWP# <-38>
- << XDALE <-38>
- << XDCE# <-38>
- << XDCE# <-38>
- << SDWP# <-38>
- << SDCD# <-38>
- << MSCD# <-38>
- >> SDMSCLK <-38>
- >> SDMS\_PWR <-38>



1.1

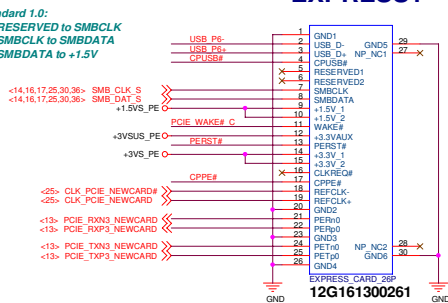
<b>ASUS</b>		<b>Title 3 in 1 CARD READER</b>	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007-03-30	Sheet 39	of 67	

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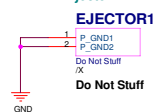


NewCard Header

EXPRESS1



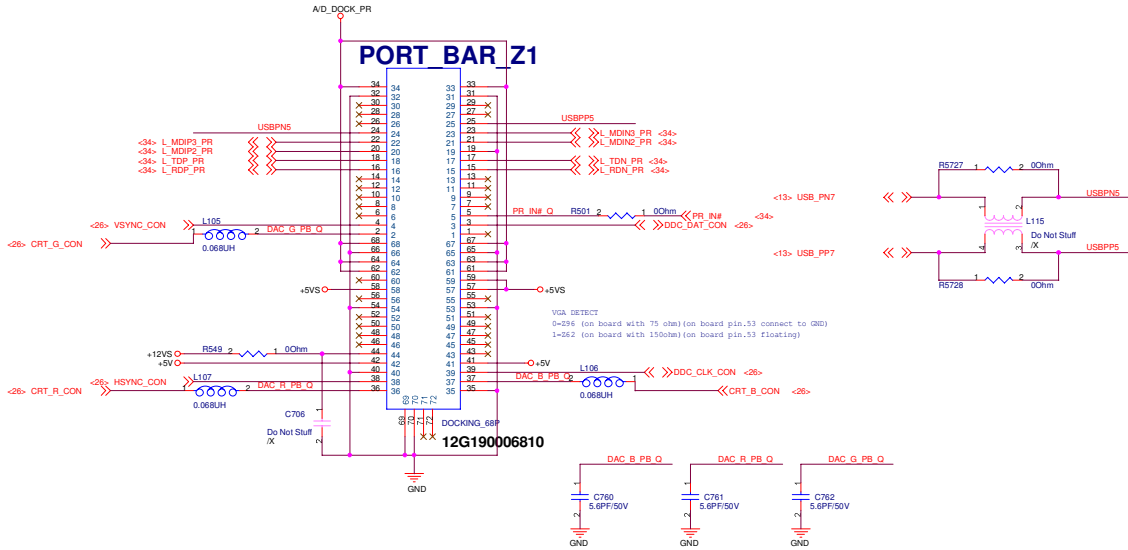
NewCard Ejector



ASUS		Title : NEWCARD	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name	Date	Rev
Custom	Z96S	11/30/2007	2.0
		Sheet	40 of 67

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1.1

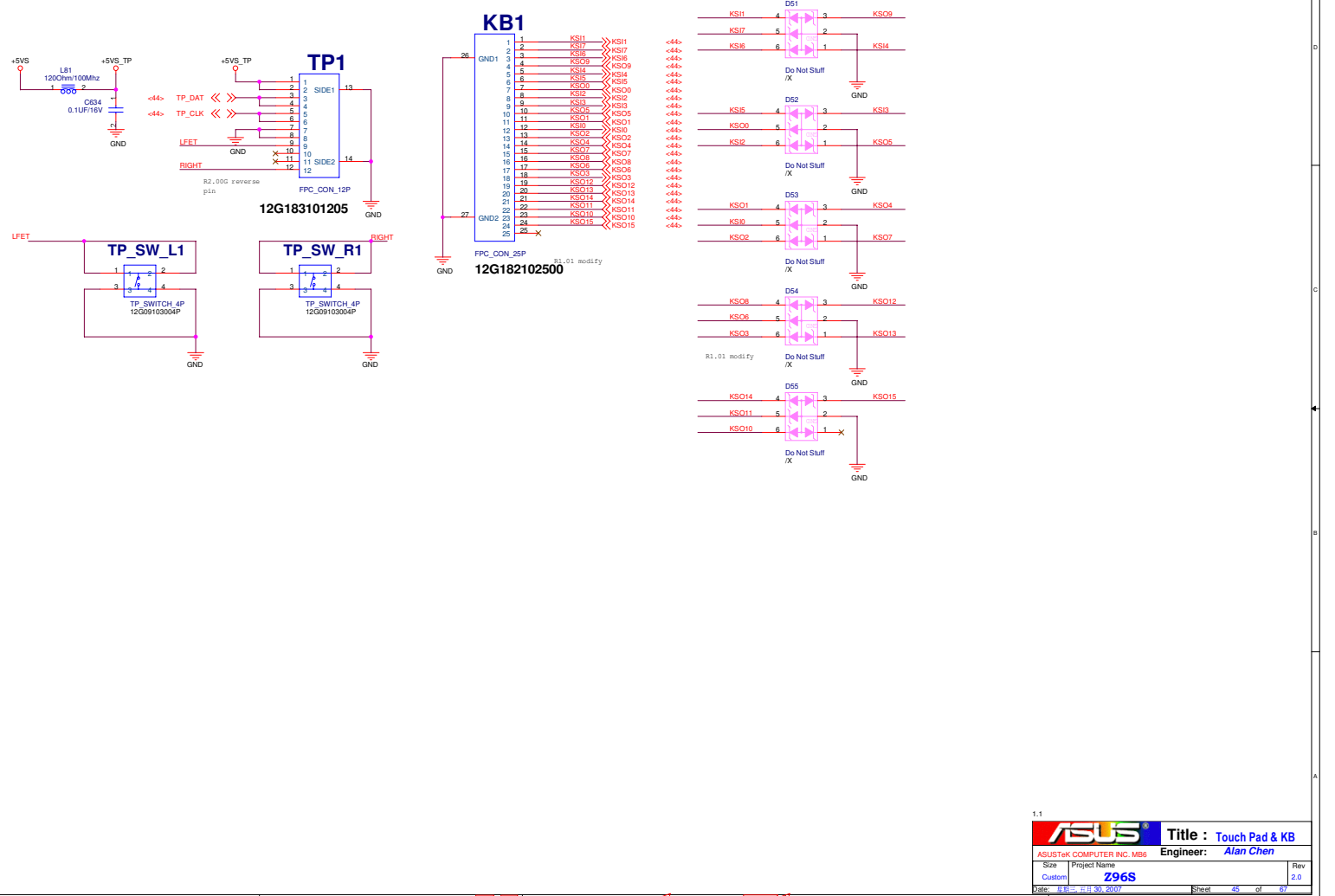
<b>ASUS</b>		Title : <Title>	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Rev	
Custom	296S	2.0	
Date: 2007-09-20		Sheet 41 of 67	

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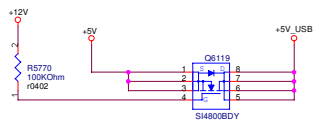




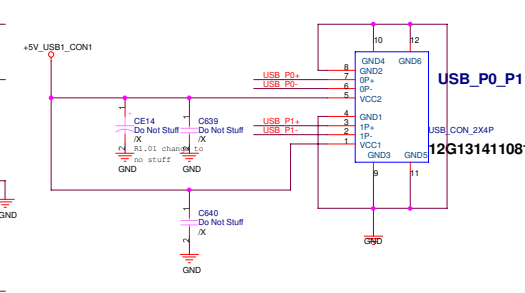
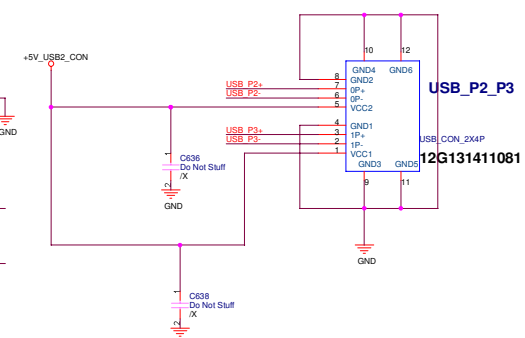
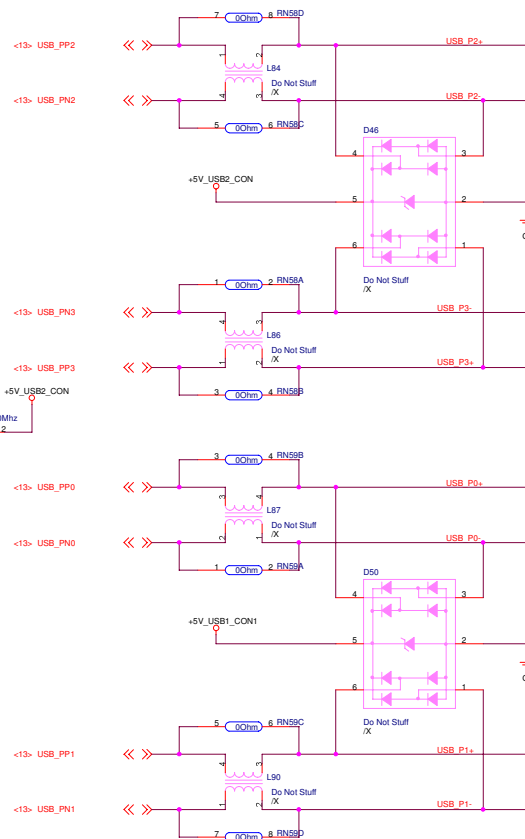
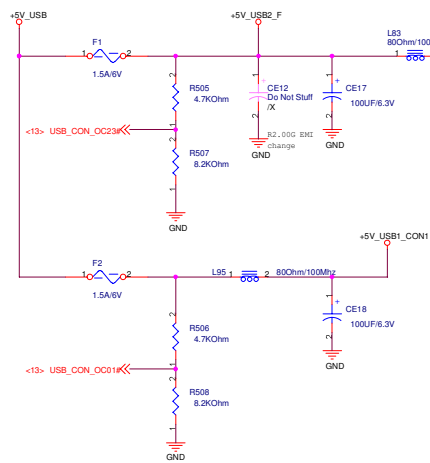
1.1

<b>ASUS</b>		<b>Title : Touch Pad &amp; KB</b>	
ASUSTek COMPUTER INC. MB6		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 2007.11.30		Sheet 45	of 87

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92.00 add protect circuit



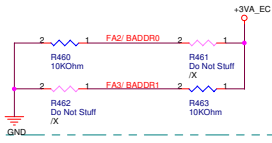
1.1		<b>ASUS</b> Title : USB CONN	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name	Custom	Z96S
Date	11/13/2007	Sheet	46 of 67
		Rev	2.0

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EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

00: PNPNG Access Register Pair Are 002Eh and 002Fh  
10: PNPNG Access Register Pair Are 004Eh and 004Fh  
01: PNPNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.  
11: Reserved



Note: Sampled at VSTBY Power Up Reset

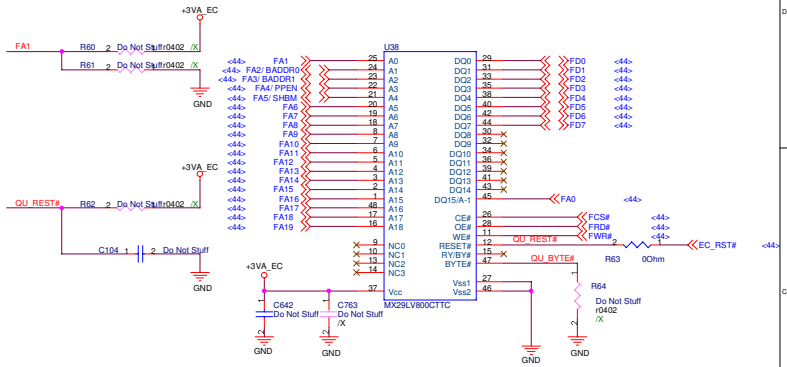
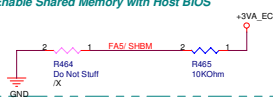
FA4/ PPEN

0: Normal  
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

0: Disable Shared Memory with Host BIOS  
1: Enable Shared Memory with Host BIOS

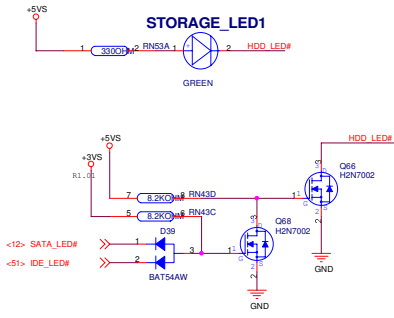


BIOS: 05G001204043

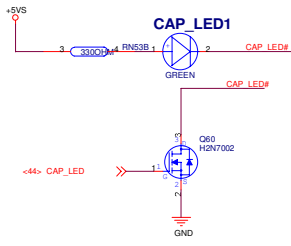
ASUS		Title :ISA ROM	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 47	of 67

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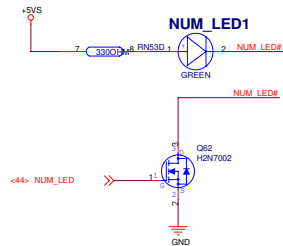
For SATA/IDE LED



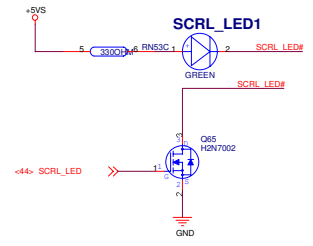
for Cap. Lock



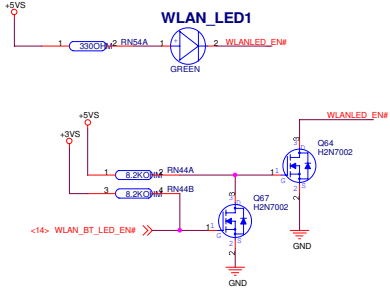
for Num Lock



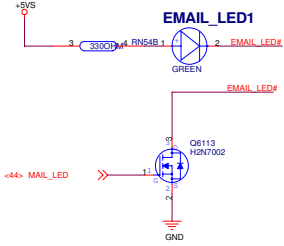
for Scroll Lock



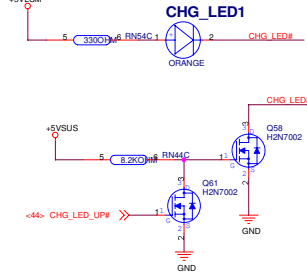
For WireLess LED



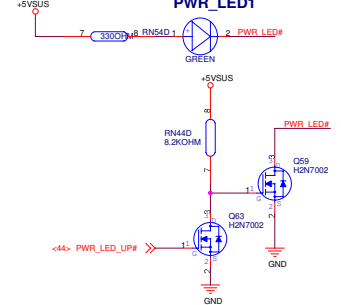
for email



For BATTERY LED



For POWER LED



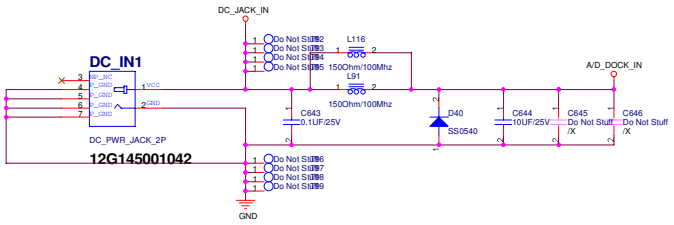
1.1

<b>ASUS</b>		<b>Title : LED</b>	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 48	of 67

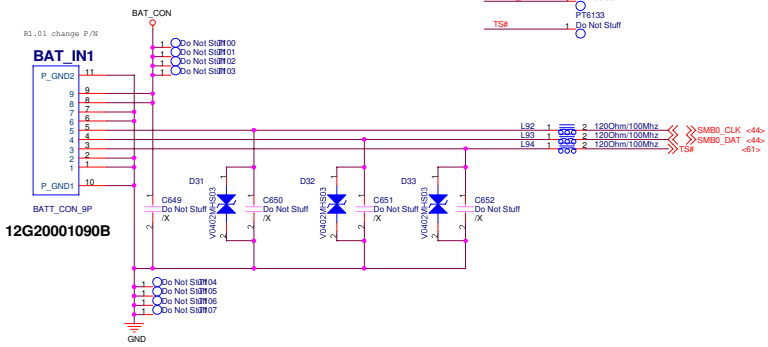
<< Kennedy\_Zhang >>



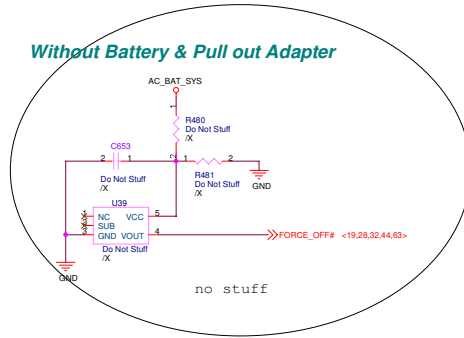
DC IN



BAT IN



Without Battery & Pull out Adapter

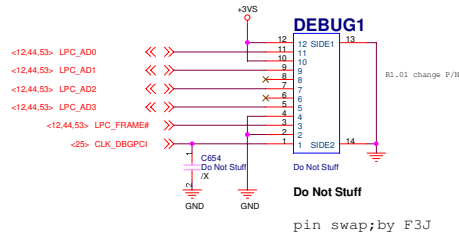


1.1

<b>ASUS</b>		<b>Title : DC &amp; BAT IN</b>	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 49	of 87

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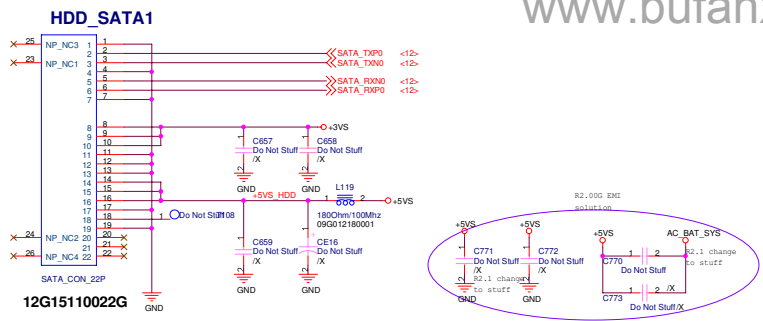
For Debug



1.1

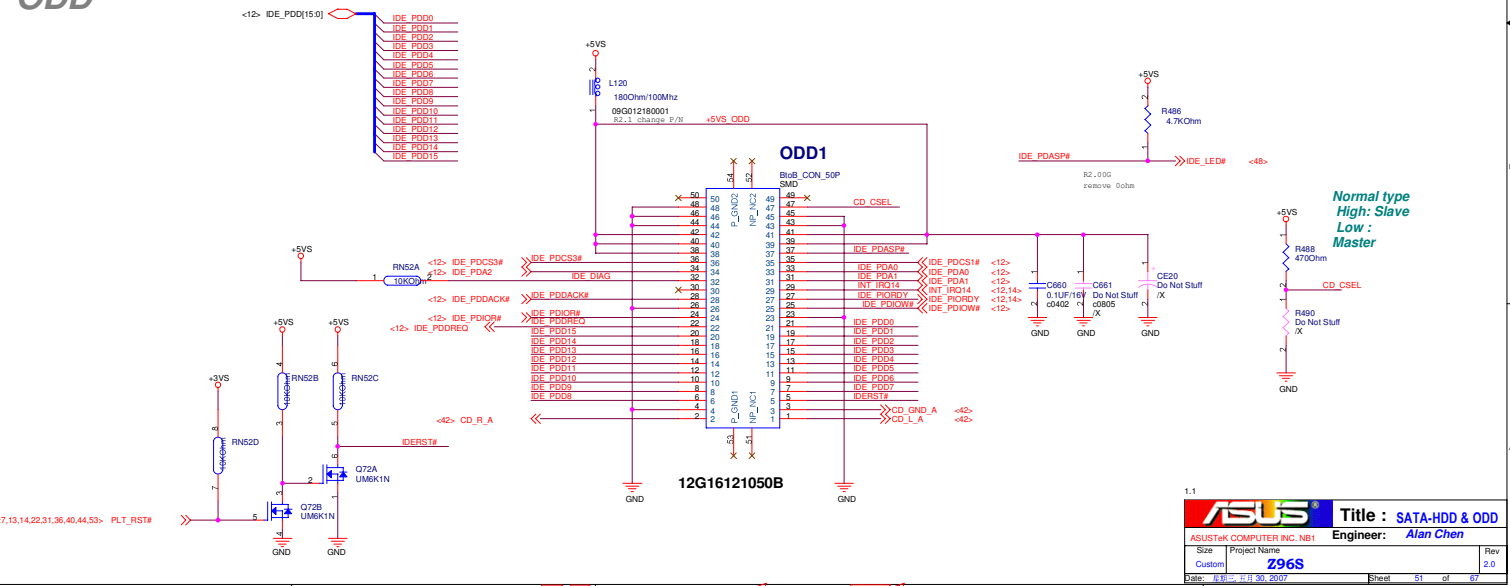
		<b>Title : Debug CONN.</b>	
ASUSTeK COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/11/10 09:20:07		Sheet	50 of 67

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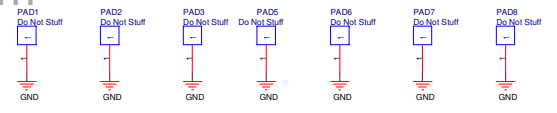
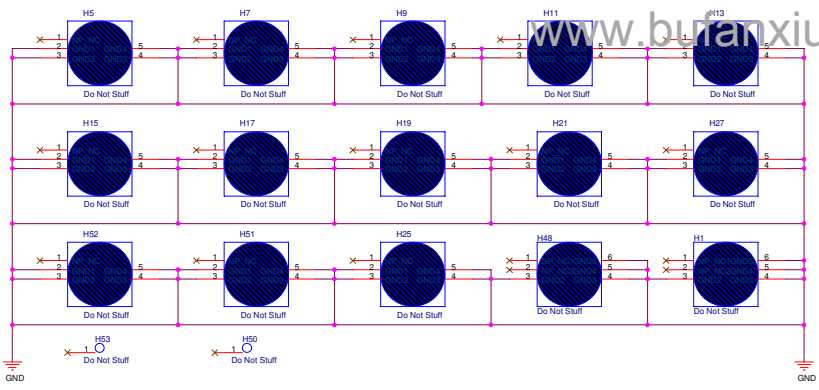
**SATA HDD**

**ODD**

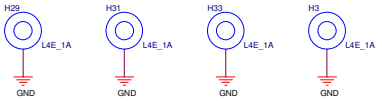


ASUS		Title : SATA-HDD & ODD	
ASUSTek COMPUTER INC. NB1		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007	Sheet 51	of 57	

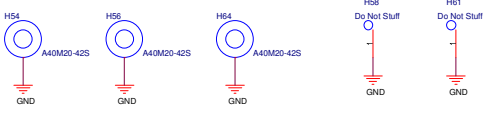
<< Kennedy\_Zhang >>



**FOR SCREW HOLE**



**FOR SCREW HOLE**

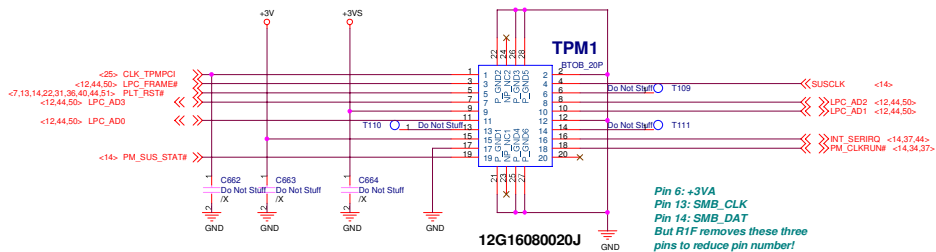


1.1

<b>ASUS</b>		<b>Title : SREW HOLE</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet	66 of 67

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For TPM Module

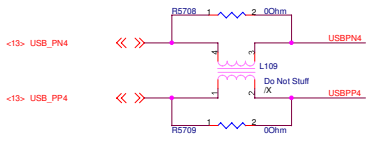
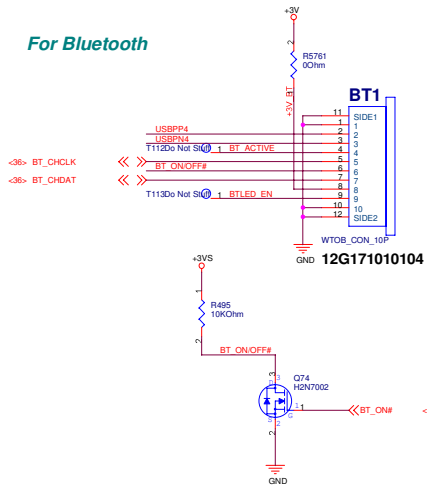


1.1

<b>ASUS</b>		<b>Title : TPM</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet: 53	of 57

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For Bluetooth

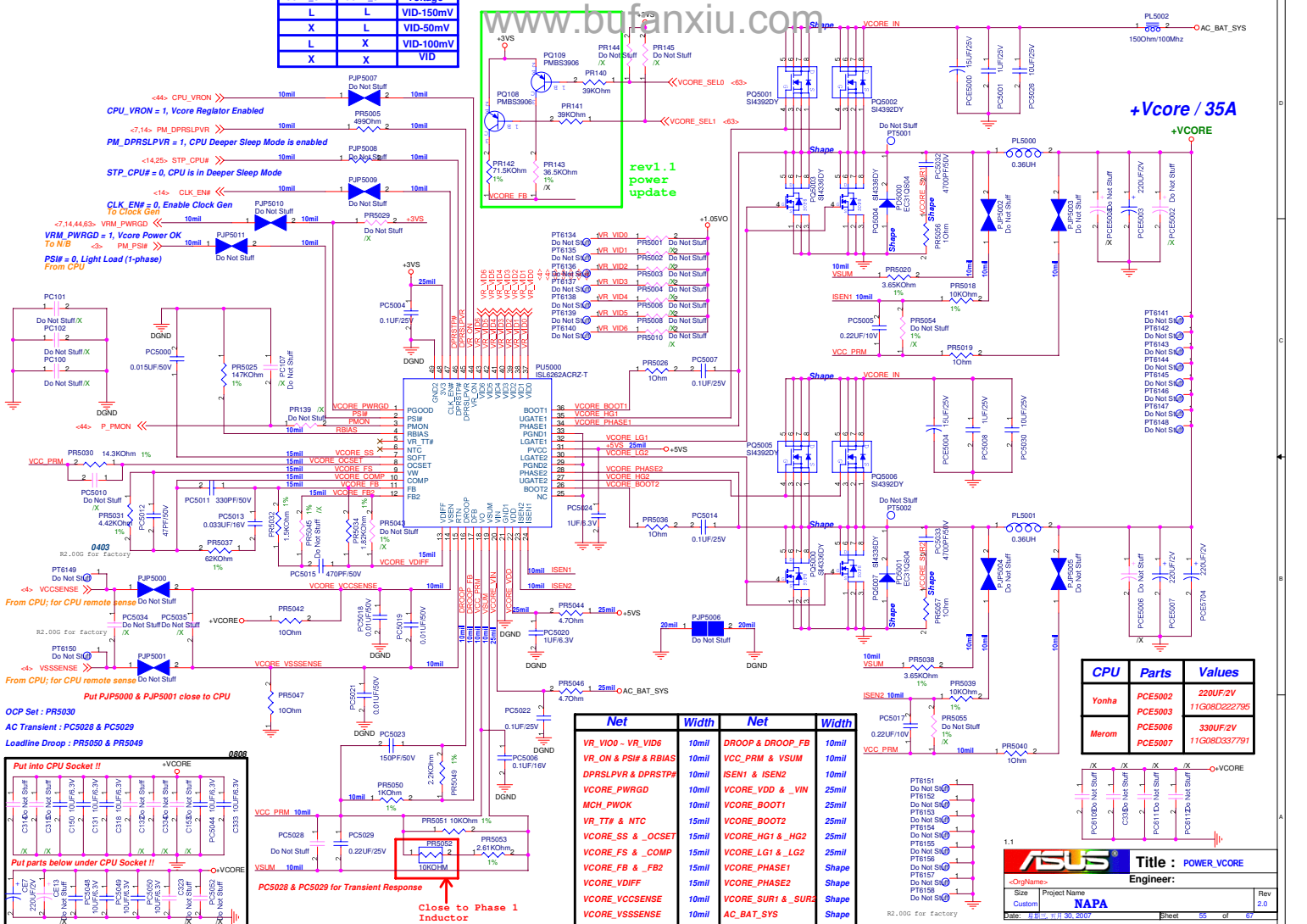
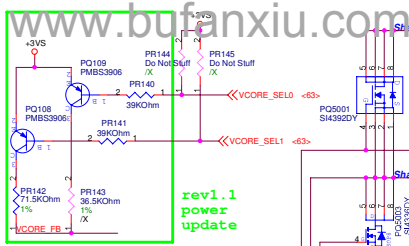


1.1

<b>ASUS</b>		<b>Title : Blue Tooth</b>	
ASUSTek COMPUTER INC		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	Z96S		2.0
Date: 11/13/2007		Sheet 54	of 67

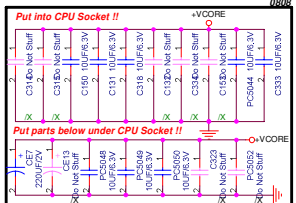
<< Kennedy\_Zhang >>

VCORE_SEL0	VCORE_SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID



CPU	Parts	Values
Yonha	PCE5002	220UF 2V
	PCE5003	11G08D222795
Merom	PCE5006	330UF 2V
	PCE5007	11G08D337791

Net	Width	Net	Width
VR_VIO0 - VR_VIO6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PS1H & RB1AS	10mil	VCC_PFM & VSUM	10mil
DPRLPVR & DPRSTP	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TTV & NTC	15mil	VCORE_HG1 & HG2	25mil
VCORE_SS & _OCSET	15mil	VCORE_LG1 & LG2	25mil
VCORE_FB & _COMP	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_SURT1 & SURT2	Shape
VCORE_VCSSENSE	10mil	AC_BAT_SYS	Shape



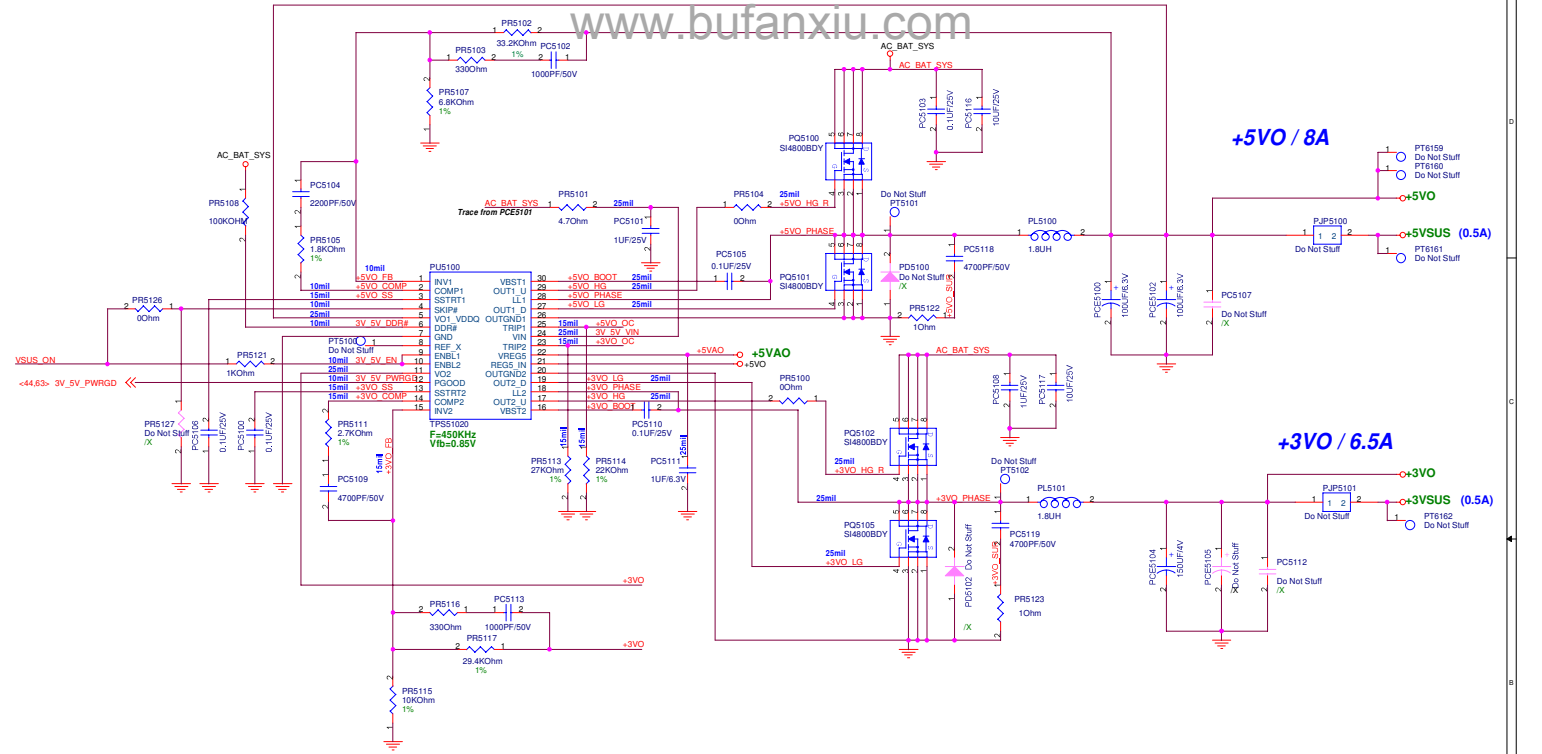
**ASUS** Title : POWER\_VCORE

Engineer: \_\_\_\_\_

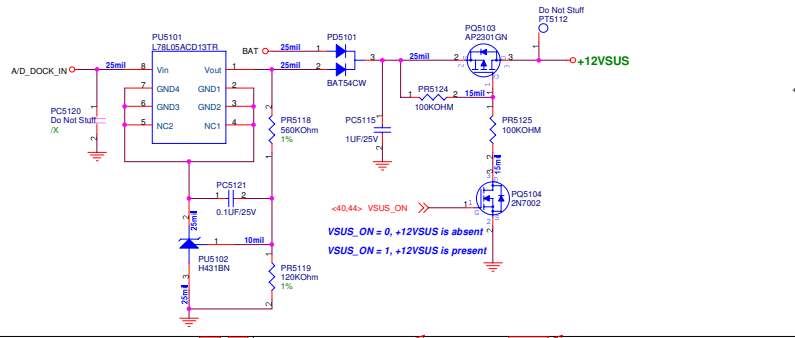
Size: Custom Project Name: NAPA

Date: 11/11/2007 Sheet: 55 of 67

<< Kennedy\_Zhang >>



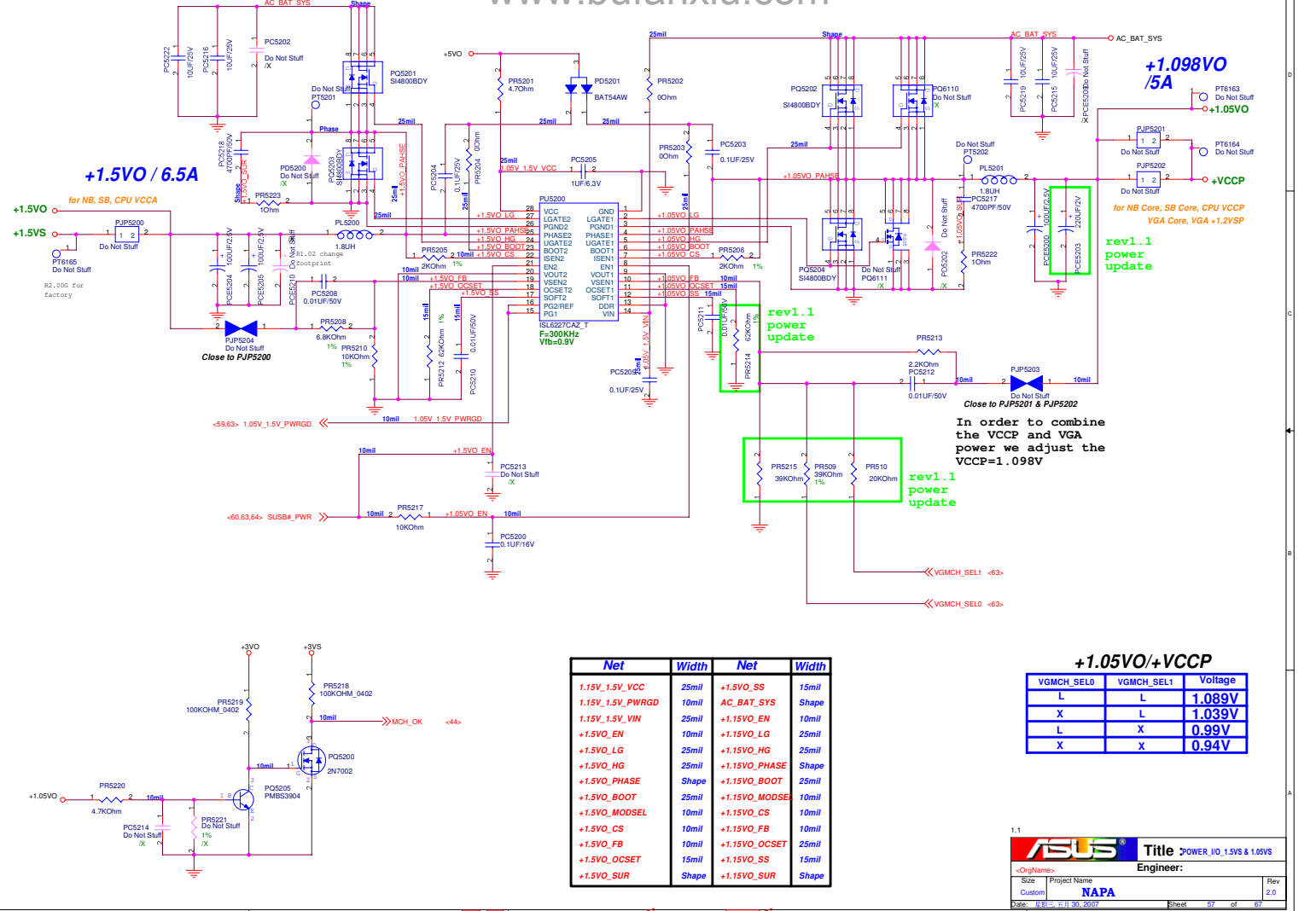
Net	Width	Net	Width
3V_V_DDR#	10mil	AC_BAT_SYS	Shape
3V_V_EN	10mil	+5VAO	25mil
3V_V_PWRGD	10mil	+3V0_FB	10mil
3V_V_VIN	25mil	+3V0_COMP	10mil
+SVO_FB	10mil	+3V0_SS	15mil
+SVO_COMP	10mil	+3V0_BOOT	25mil
+SVO_SS	15mil	+3V0_HG	25mil
+SVO_BOOT	25mil	+3V0_HG_R	25mil
+SVO_HG	25mil	+3V0_LG	25mil
+SVO_HG_R	25mil	+3V0_PHASE	Shape
+SVO_LG	25mil	+3V0_SUR	Shape
+SVO_PHASE	Shape	+3V0_OC	15mil
+SVO_SUR	Shape	+12VSUS_ADJ	10mil
+SVO_OC	15mil	+SVDVY	25mil



ASUS Title : POWER\_SYSTEM  
 Engineer:  
 Project Name  
 Date: 11/30/2007 Sheet 56 of 67

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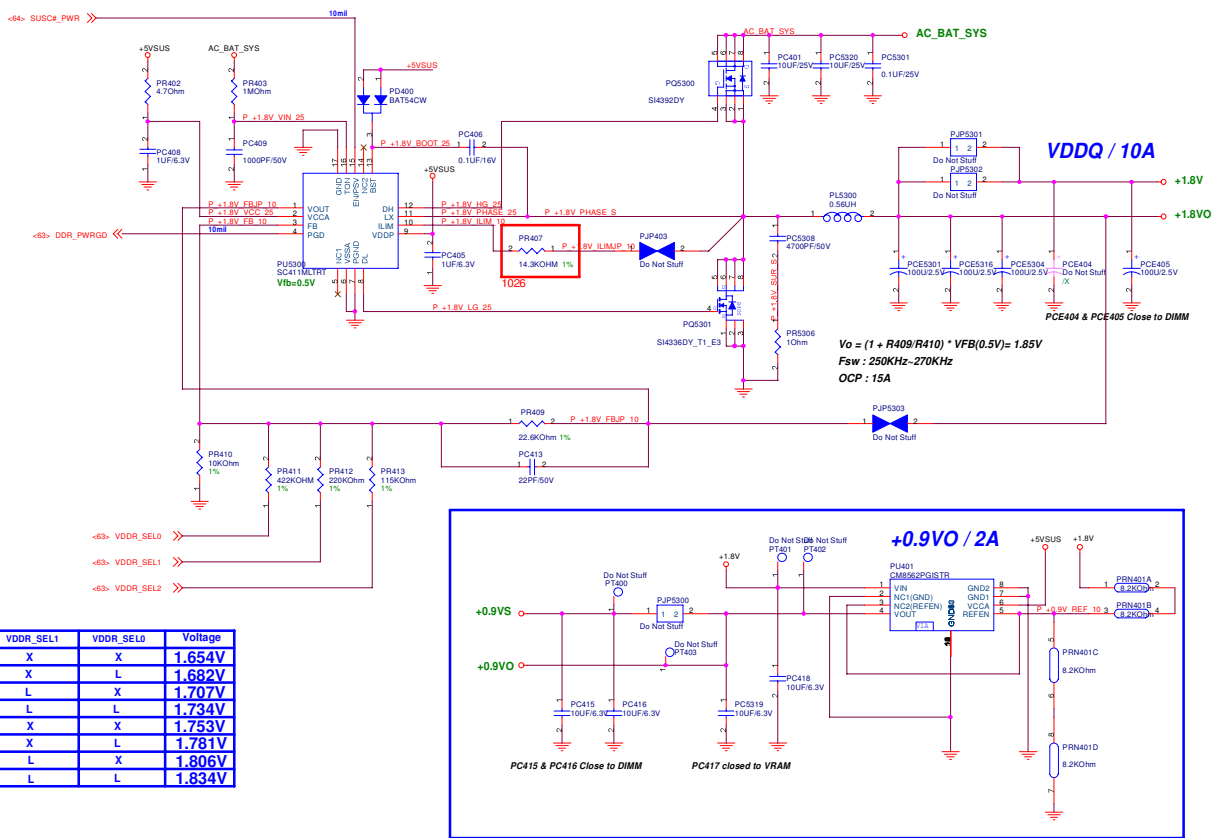
Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5V_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.5V_EN	10mil
+1.5V_EN	10mil	+1.5V_LG	25mil
+1.5V_LG	25mil	+1.5V_HG	25mil
+1.5V_PHASE	Shape	+1.5V_PHASE	Shape
+1.5V_BOOT	25mil	+1.5V_BOOT	25mil
+1.5V_BOOTSEL	10mil	+1.5V_MODSEL	10mil
+1.5V_CS	10mil	+1.5V_CS	10mil
+1.5V_FB	10mil	+1.5V_FB	10mil
+1.5V_OCSET	10mil	+1.5V_OCSET	25mil
+1.5V_OCSET	15mil	+1.5V_SS	15mil
+1.5V_SUR	Shape	+1.5V_SUR	Shape

**+1.05V/+VCCP**

VGMCH_SELO	VGMCH_SEL1	Voltage
L	L	1.089V
X	L	1.039V
L	X	0.99V
X	X	0.94V

ASUS Title POWER\_IO\_1.5VS & 1.05VS  
 Engineer: NAPA  
 Date: 11/30/2007 Sheet 57 of 57

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**+VDDQ**

VDDR_SEL2	VDDR_SEL1	VDDR_SEL0	Voltage
X	X	X	1.654V
X	X	L	1.682V
X	L	X	1.707V
X	L	L	1.734V
L	X	X	1.753V
L	X	L	1.781V
L	L	X	1.806V
L	L	L	1.834V

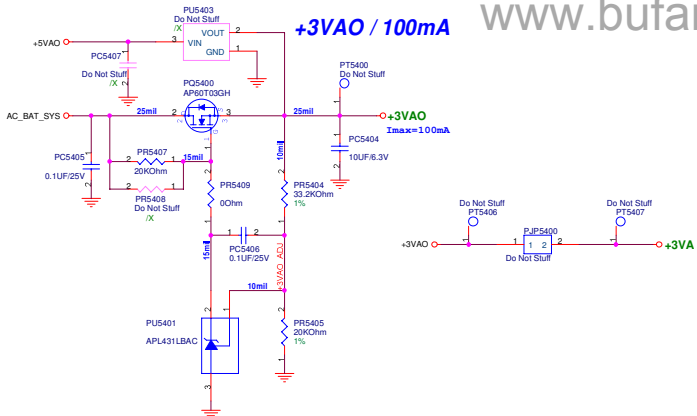
1.1

**ASUS** Title : POWER\_IO\_DDR & VTT

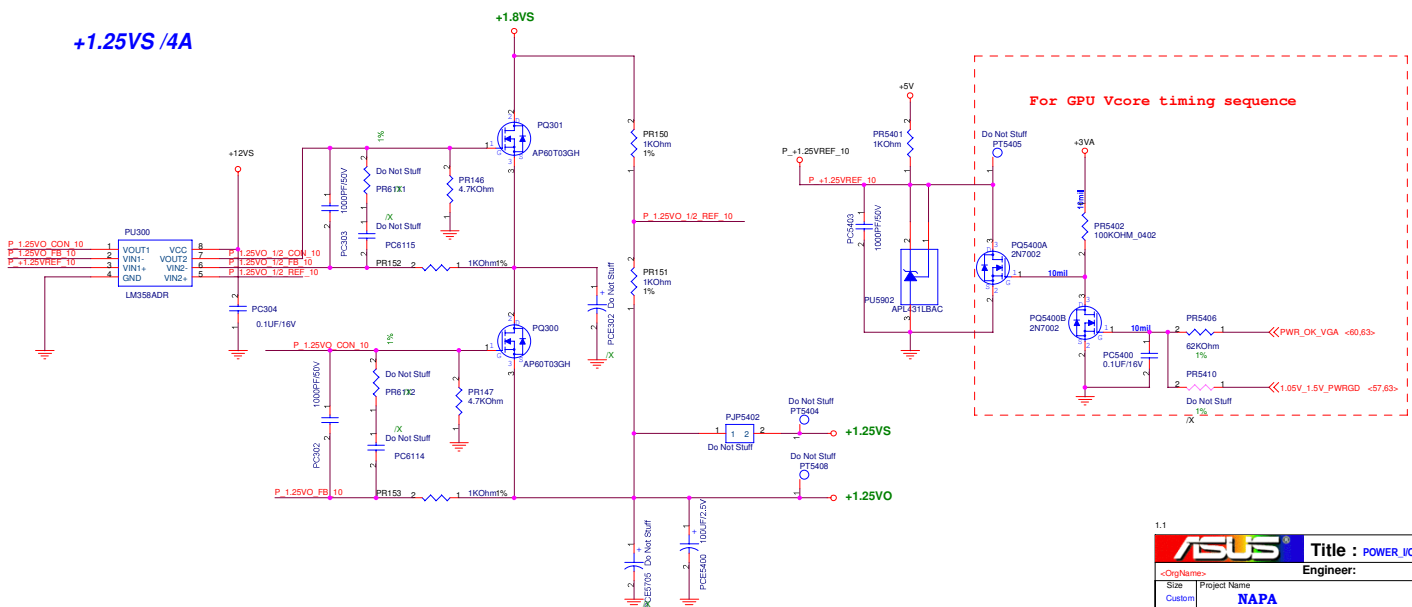
Engineer:

Size	Project Name	Rev
Custom	NAPA	#0
Date: 2007-11-29	Sheet: 58	of: 63

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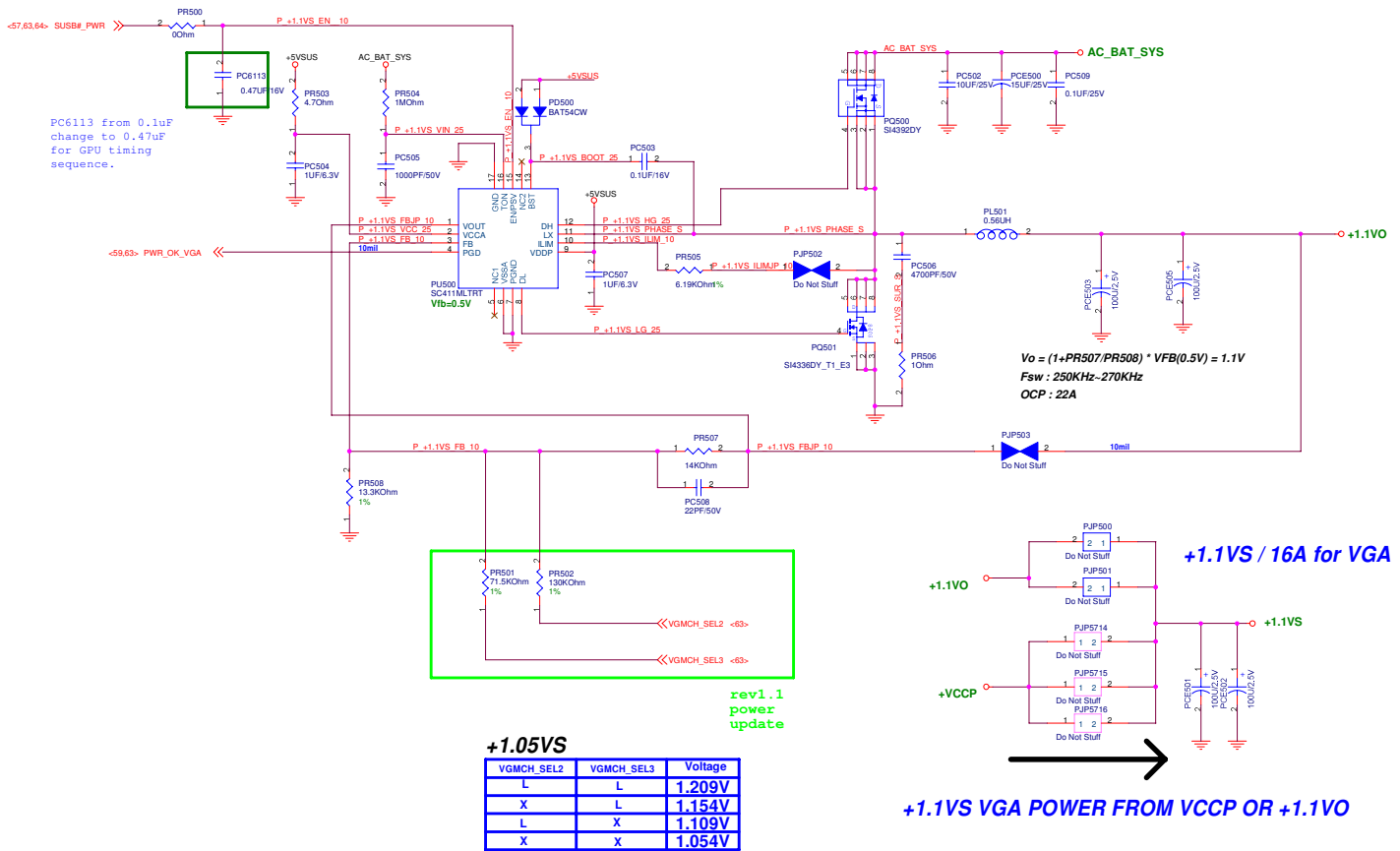


**+1.25VS / 4A**



ASUS		Title : POWER_IO_+3VA & +2.5V	
-OrigName:		Engineer:	
Size	Project Name		Rev
Custom	NAPA		2.0
Date: 08/11/2007		Sheet	66 of 67

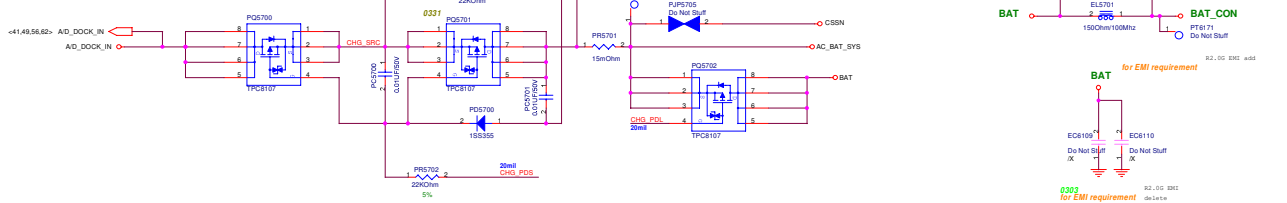
<< Kennedy\_Zhang >>



Title		<Title>
Size	Document Number	Rev 2.0
Date	11/30/2007	Sheet 66 of 67

<< Kennedy\_Zhang >>

### POWER PATH & BAT\_LEARN



- Charger shut down condition :**
1.  $V_{ictl} < 0.06V$
  2.  $PKPRES\# > 50\%$  of MAX8725\_LDO
  3. AC Adaptor Removed

**The timing of PDL & PDS switch :**  
 BAT - A/D\_DOCK\_IN > 100mV-> Battery mode

The current capacity of MAX8725\_LDO is 10mA

VBAT\_DLGV is a voltage for driving MOSFET.

MAX8725\_ACIN < 10.27V, AC Adaptor absent  
 MAX8725\_ACIN > 10.27V, AC Adaptor present

MODE (Pin#)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.0V < Vmode < 2V)	Battery Learn

MAX8725\_REF : 4.2235V  
 MAX8725\_LDO : 5.4V

**Battery Charging Voltage :**  
 $+V\_BAT = 3 \times [4.2235 + (V_{ictl} - 1.8) / 9.52]$

**Battery Charging Current :**  
 $I_{charge} = (0.075 / PRS706) \times (V_{ictl} / 3.6)$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (0.075 / PRS701) \times (V_{ics} / 4.2235)$

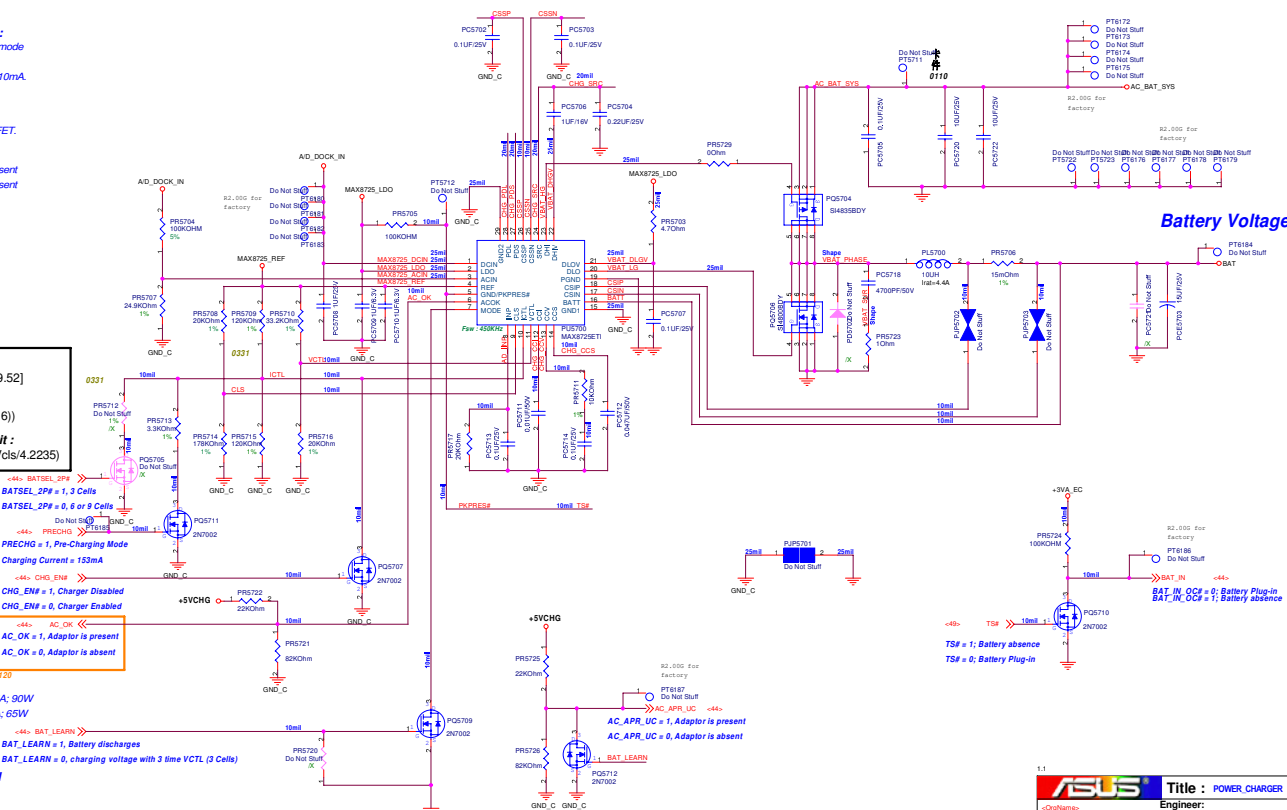
**Pre-Charging Mode :**  
 Precharging current = 150 - 160mA  
 $V_{ictl} = 0.100V - 0.120V$

**Battery Cell Selection :**  
 BATSEL\_2PF = 1, 3 Cells  
 BATSEL\_2PF = 0, 2 or 9 Cells

**Adaptor Max. Current :**  
 PRS714 = 178K;  $V_{ds} = 3.75V$ ,  $I_{limit} = 4.5A$ ; 90W  
 PRS714 = 47K;  $V_{ds} = 2.96V$ ,  $I_{limit} = 3.5A$ ; 65W

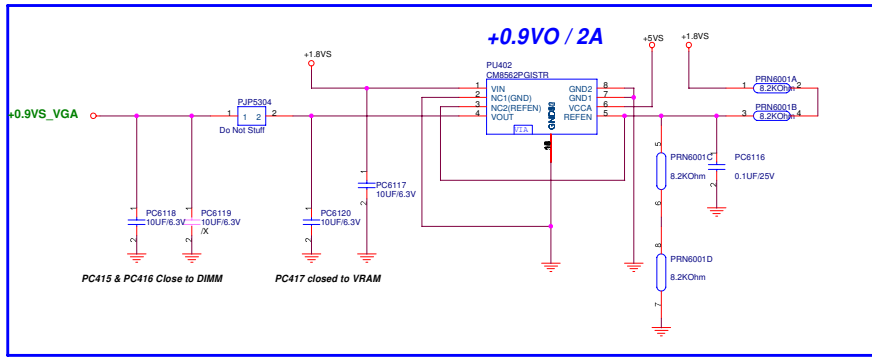
**BATSEL\_2PF = 1, 3-Cell**  
 $V_{ictl} = 1.22V$ ;  $I_{charge} = 1.69A$

**BATSEL\_2PF = 0, 6-Cell or 9-Cell**  
 $V_{ictl} = 2.11V$ ;  $I_{charge} = 2.93A$

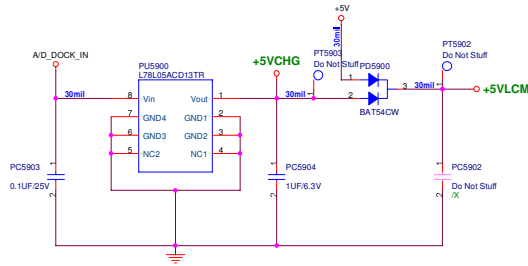


ASUS		Title : POWER CHARGER	
Rev	Project Name	Rev	Rev
1	NAPA	1	2.0
Date: 2011-01-20	Drawn: 61	By: 61	By: 61

« Kennedy\_Zhang »



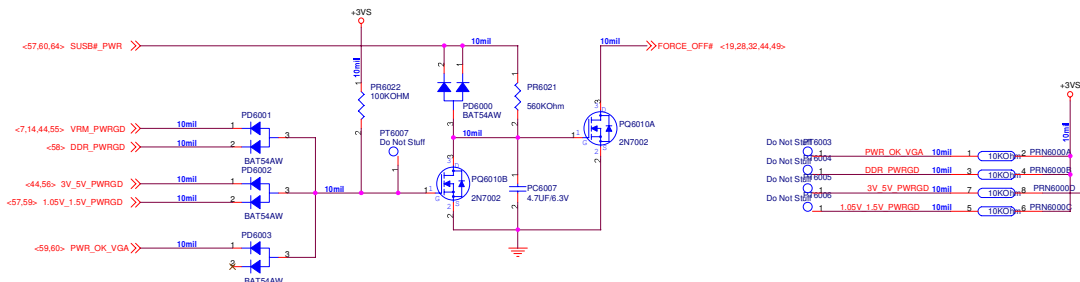
**+5VLCM / +5VCHG**



1.1

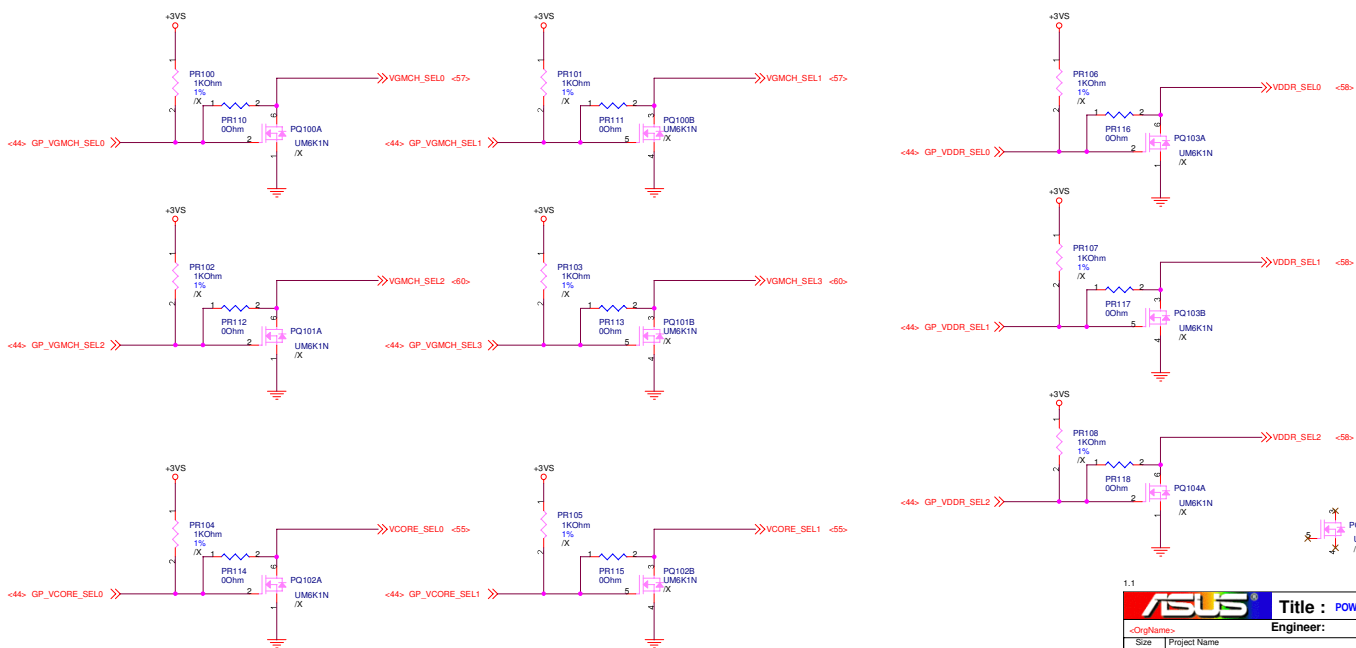
<b>ASUS</b>		<b>Title : POWER_DETECT</b>	
-<OrigName>		Engineer:	
Size	Project Name		Rev
Custom	<b>NAPA</b>		2.0
Date: 11/13/2007		Sheet	62 of 67

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Power Voltage control

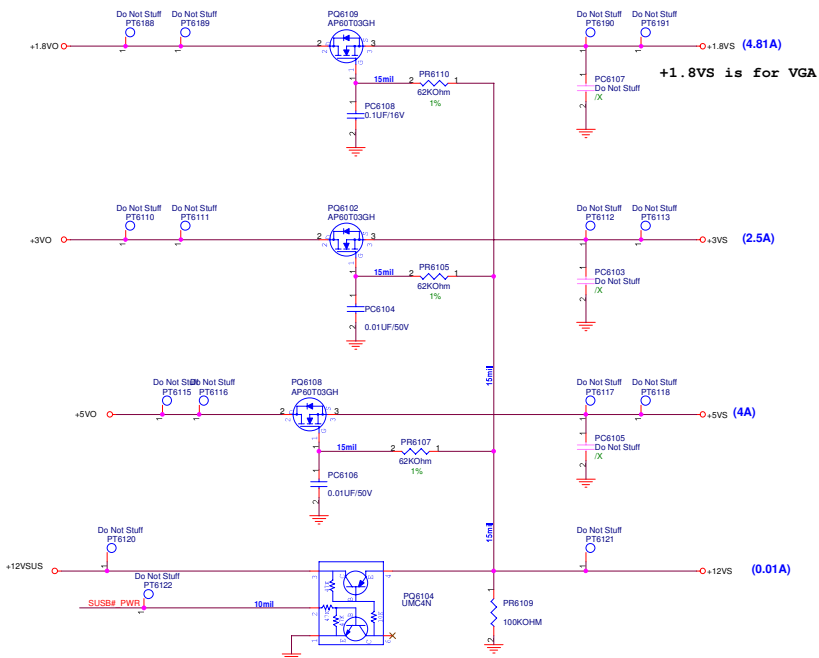
Modify V2.0G



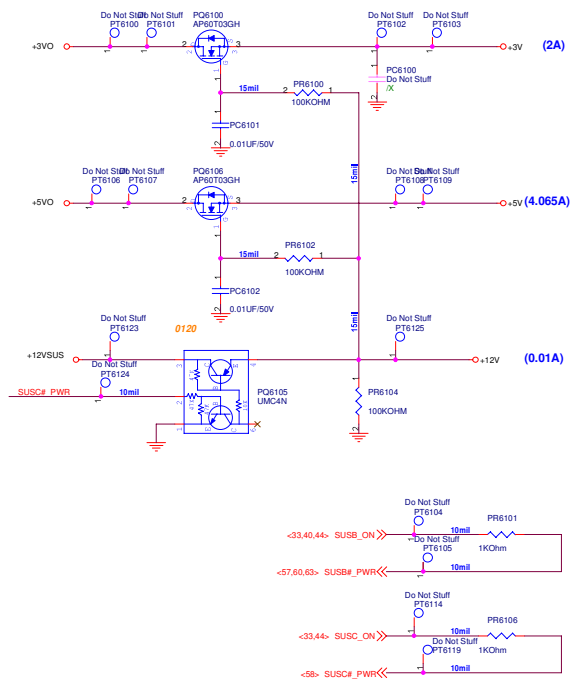
ASUS		Title : POWER_PROTECT	
Engineer:		Project Name:	
Size:	Custom	Rev:	2.0
Date:	11/30/2007	Sheet:	63 of 67

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### SUSB#\_PWR POWER



### SUSC#\_PWR POWER

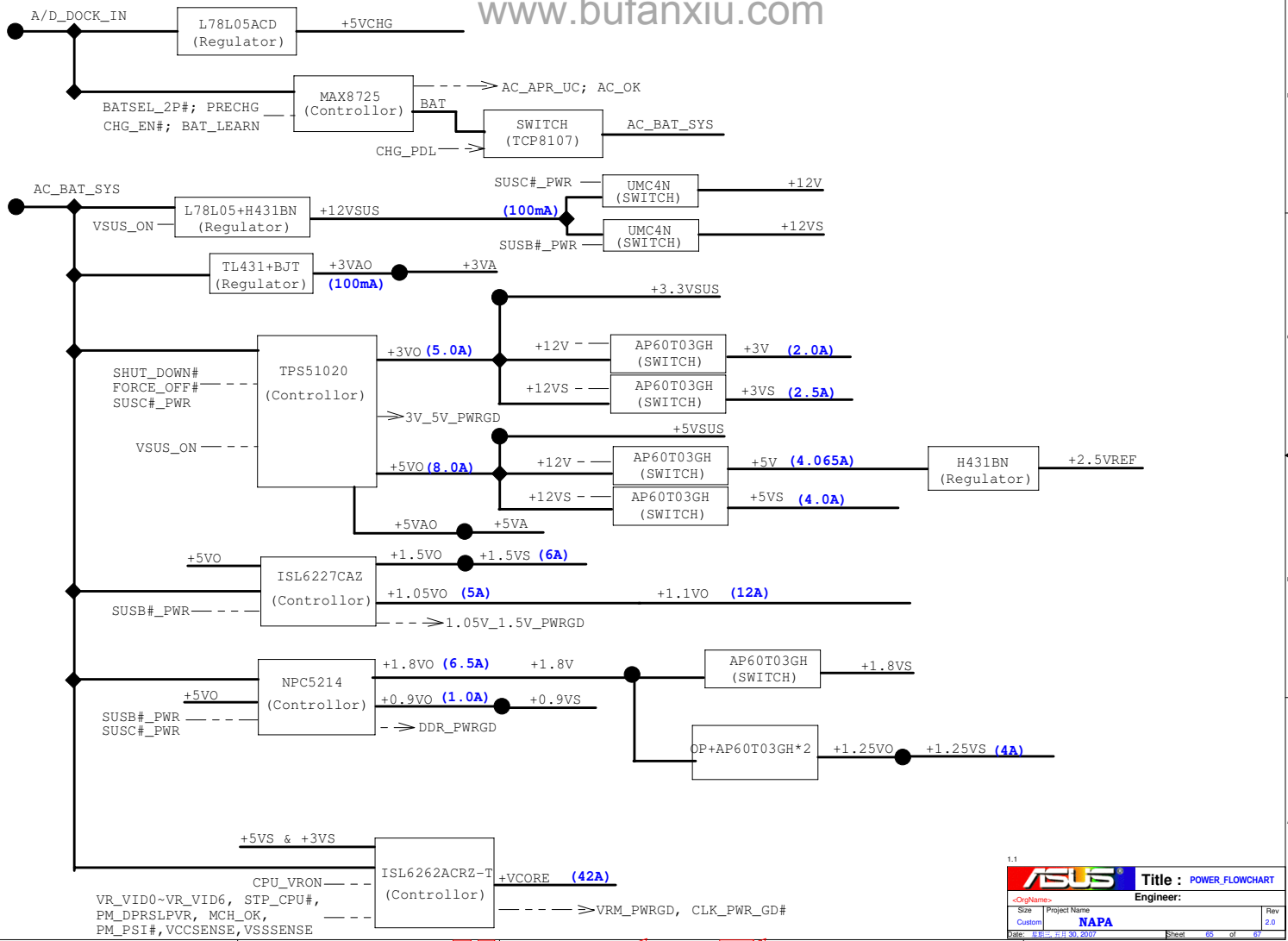


1.1

<b>ASUS</b>		<b>Title : POWER_LOAD_SWITCH</b>	
<OrigName>	Project Name	Engineer:	
Size	Custom	NAPA	Rev 2.0
Date: 11/30/2007	Sheet 64	of 67	

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1.1

		Title : POWER FLOWCHART	
Size	Project Name	Engineer:	
Custom	NAPA	Rev	2.0
Date: 11/30/2007	Sheet	66	of 67

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1.1

		Title : POWER_SIGNAL	
<OrigName>		Engineer: Alan Chen	
Size	Project Name		Rev
Custom	NAPA		2.0
Date: 11/30/2007		Sheet	66 of 67

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