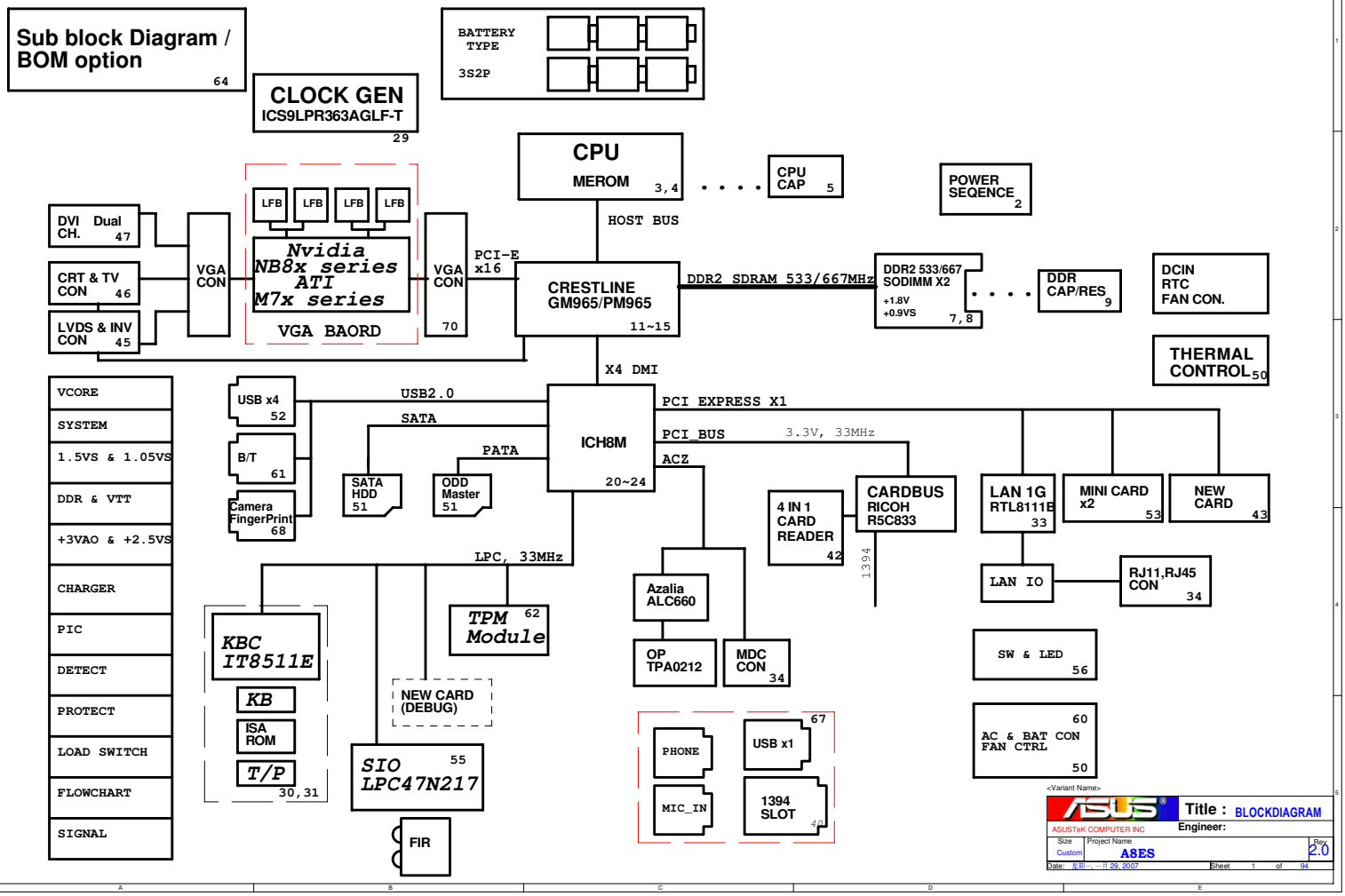
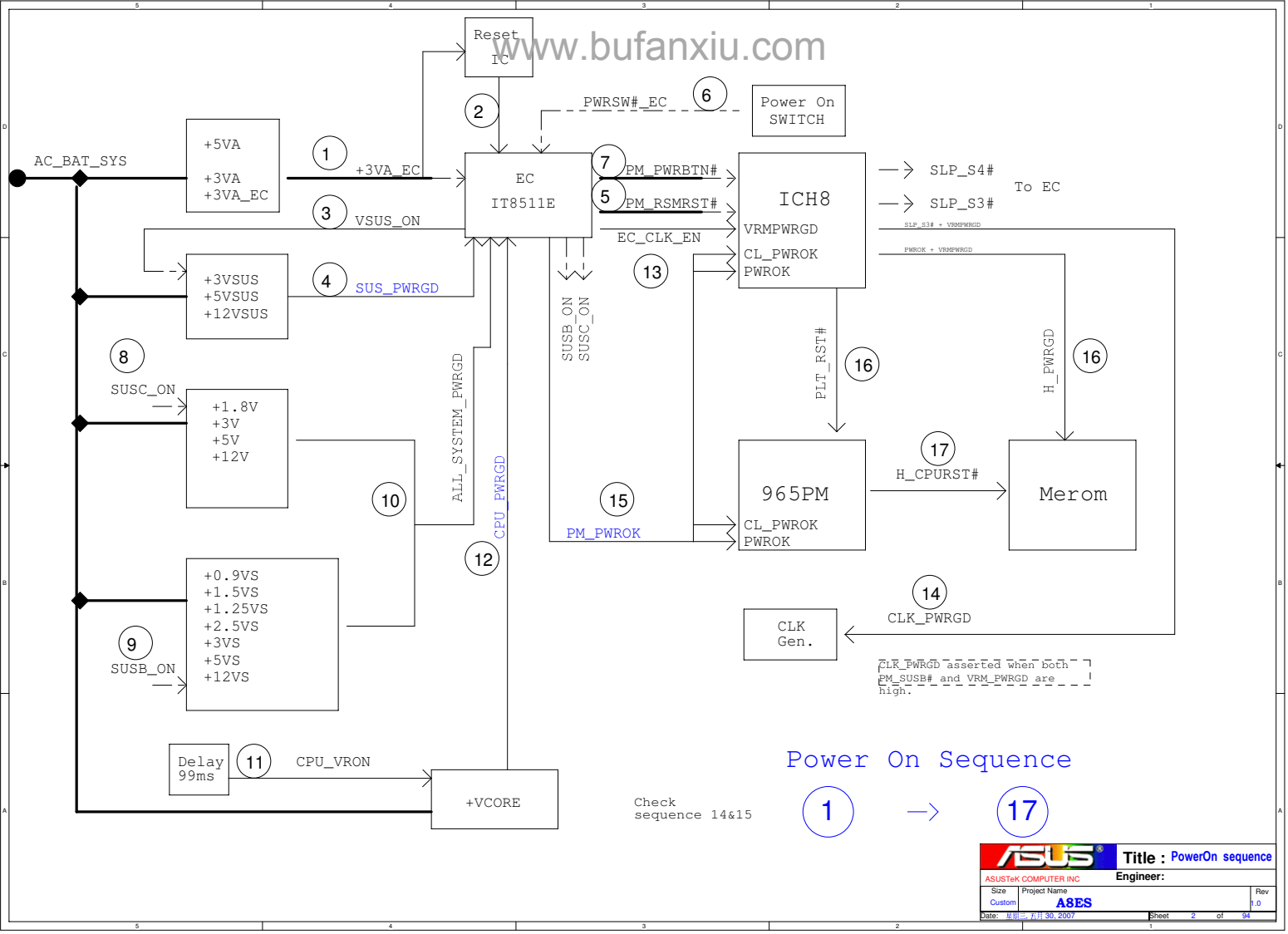
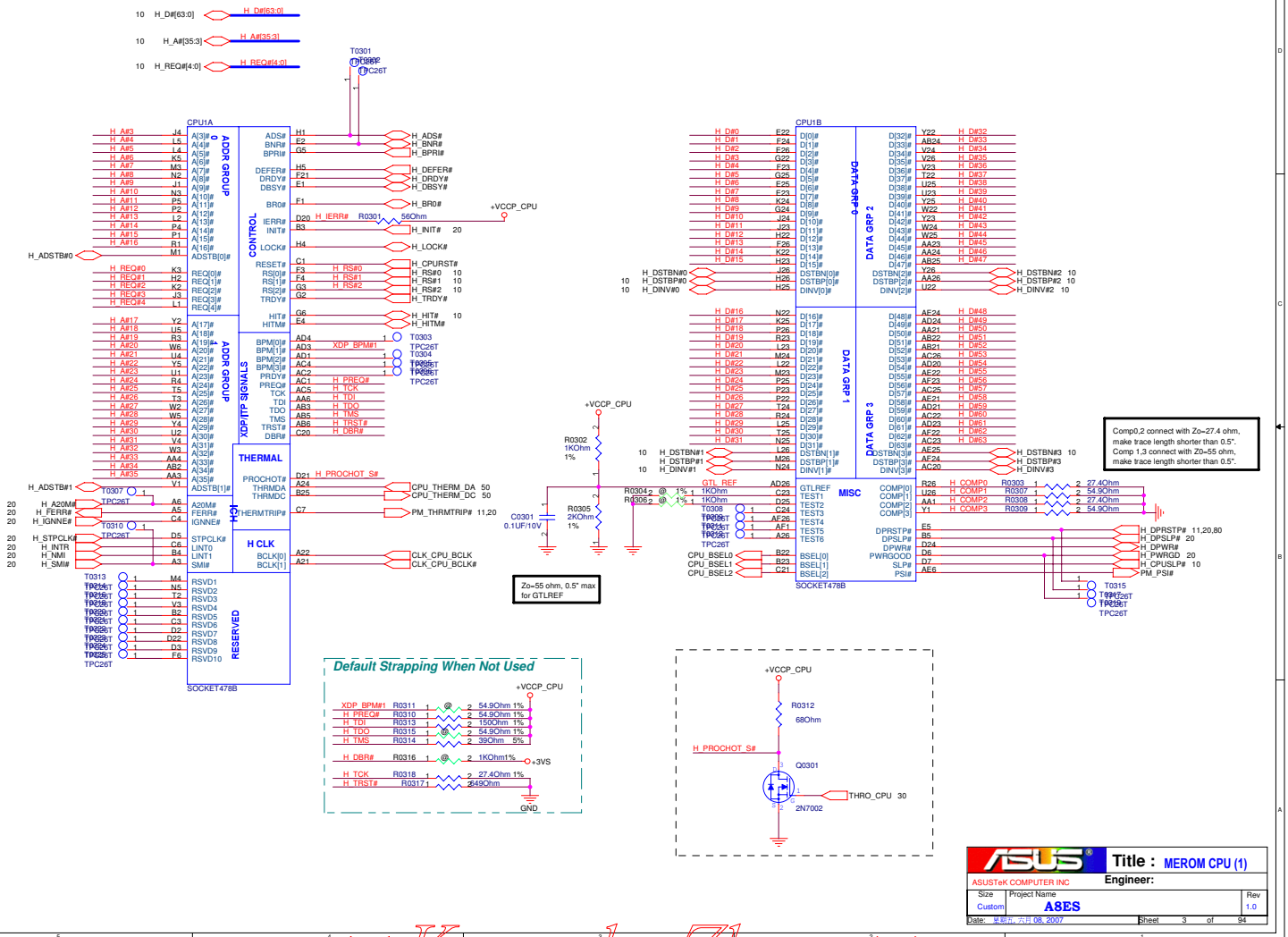
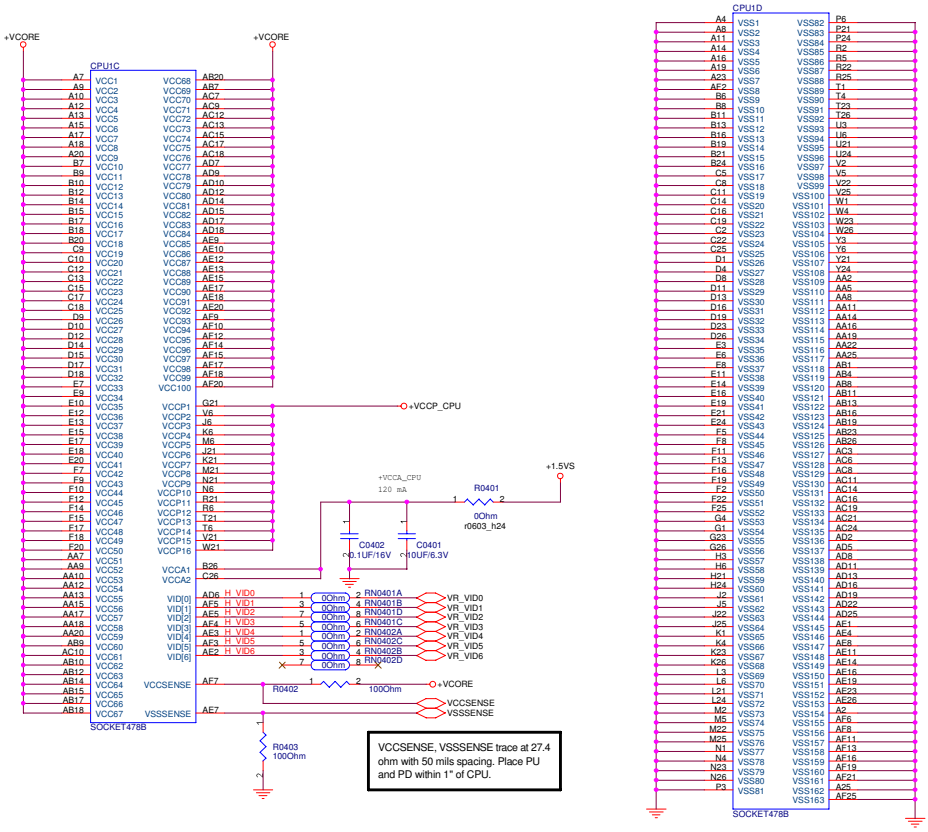
A8E/A8S Merom/GM965/PM965 BLOCK DIAGRAM



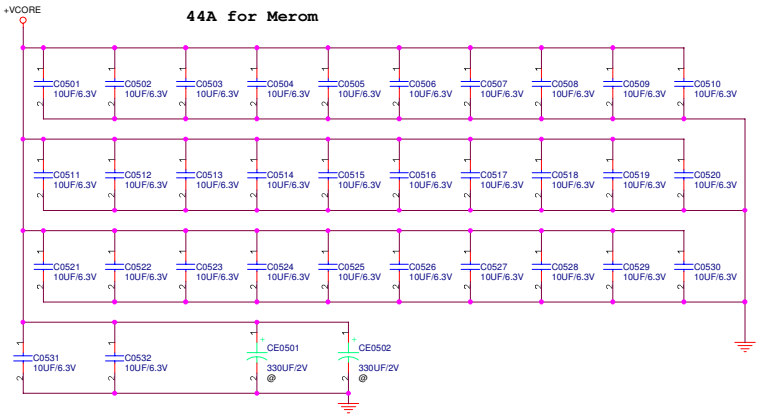




ASUSTeK COMPUTER INC	Title : MEROM CPU (1)		
	Engineer:		
Size: Custom	Project Name: A8ES		Rev: 1.0
Date: 星期六, 六月 09, 2007	Sheet 3 of 94		



ASUSTeK COMPUTER INC	Title : MEROM CPU (2)	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 星期六, 六月 09, 2007	Sheet 4 of 94	

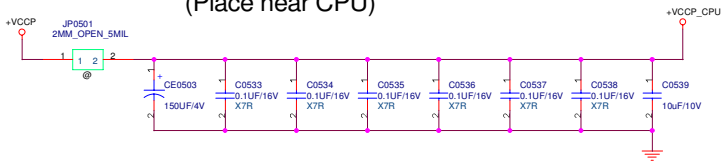


Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

VCORE	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs

+VCCP Decoupling Capacitor
(Place near CPU)



ASUSTeK COMPUTER INC

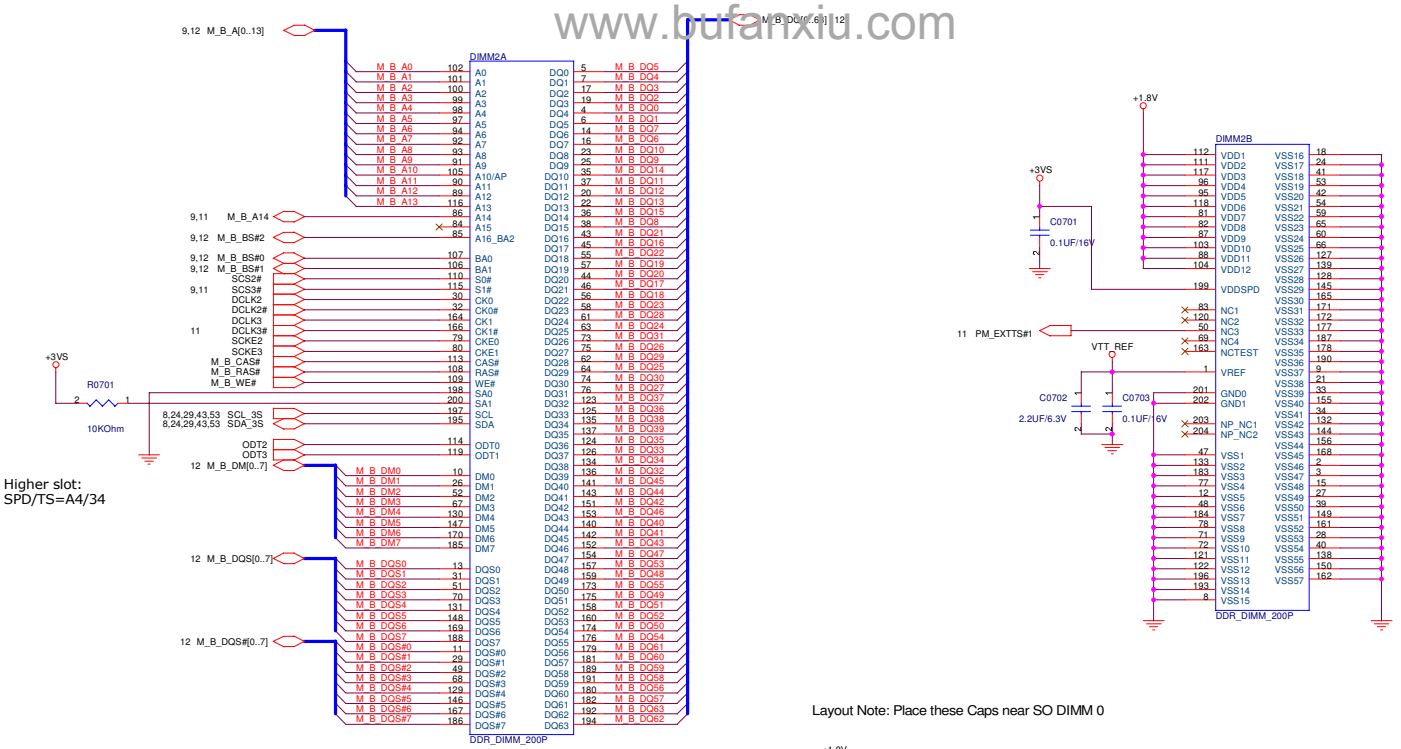
Title : CPU CAP

Engineer:

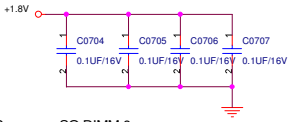
Size	Project Name	Rev
B	A8ES	1.0

Date: 星期六, 十月 13, 2006 Sheet 5 of 94

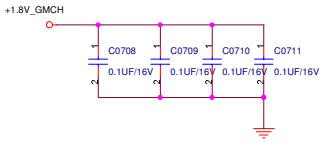
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 6 of 94	



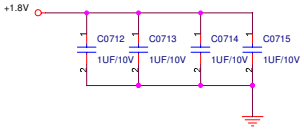
Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these High-Freq decoupling Caps near the GMCH

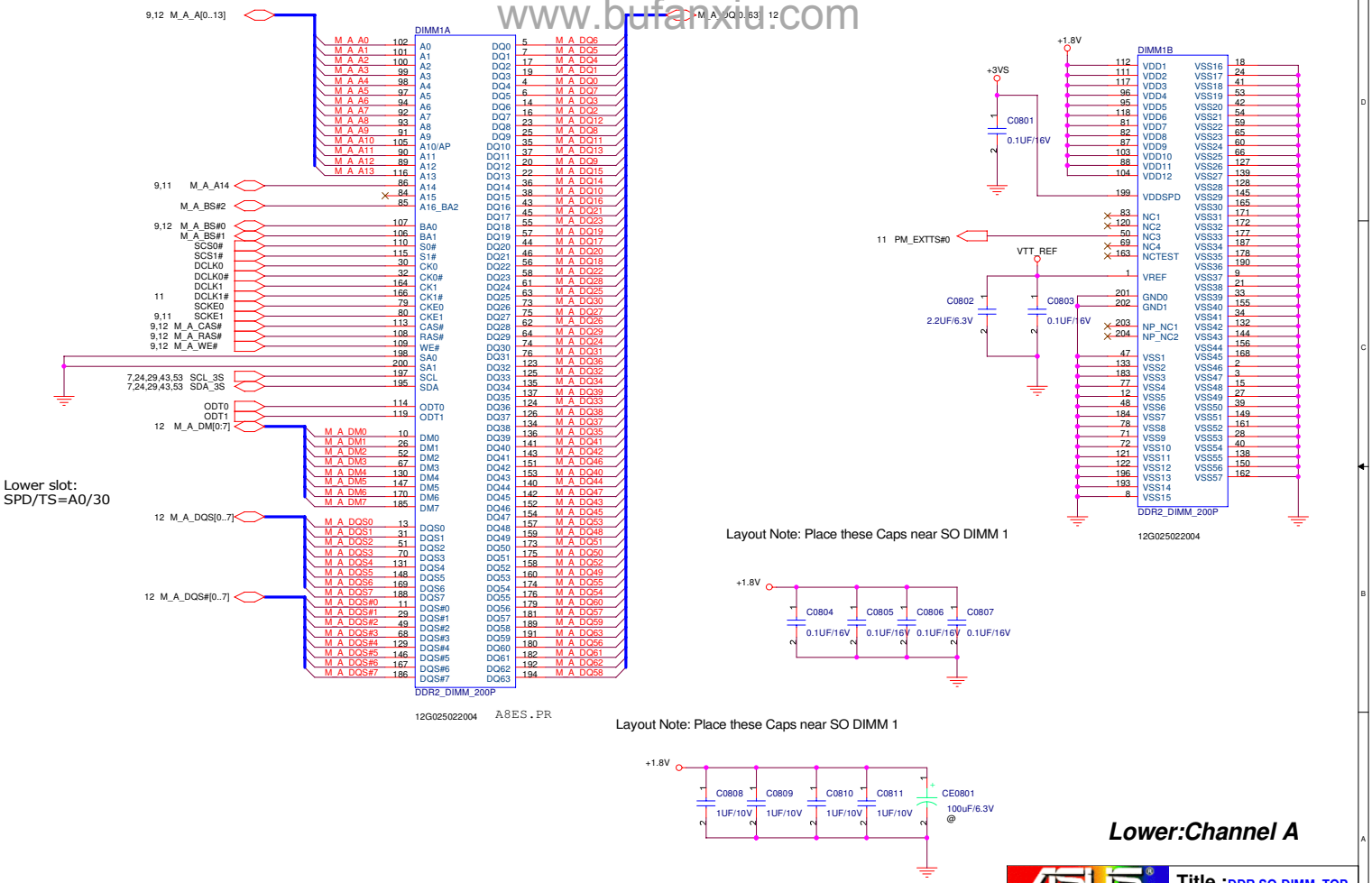


Layout Note: Place these Caps near SO DIMM 0

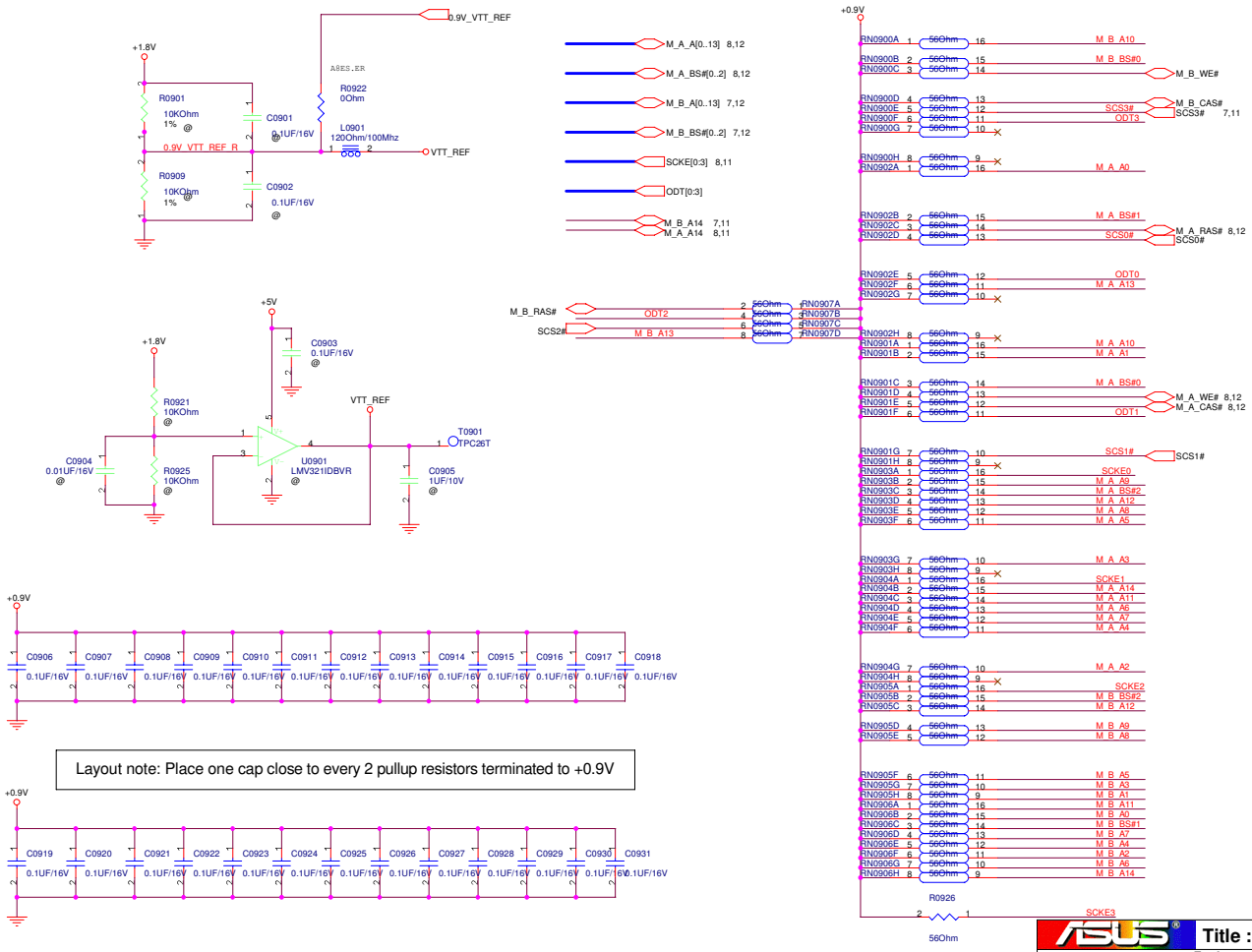


Upper:Channel B

ASUSTeK COMPUTER INC	Title : DDR SO-DIMM	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 星期五, 六月 29, 2007	Sheet 7 of 94	

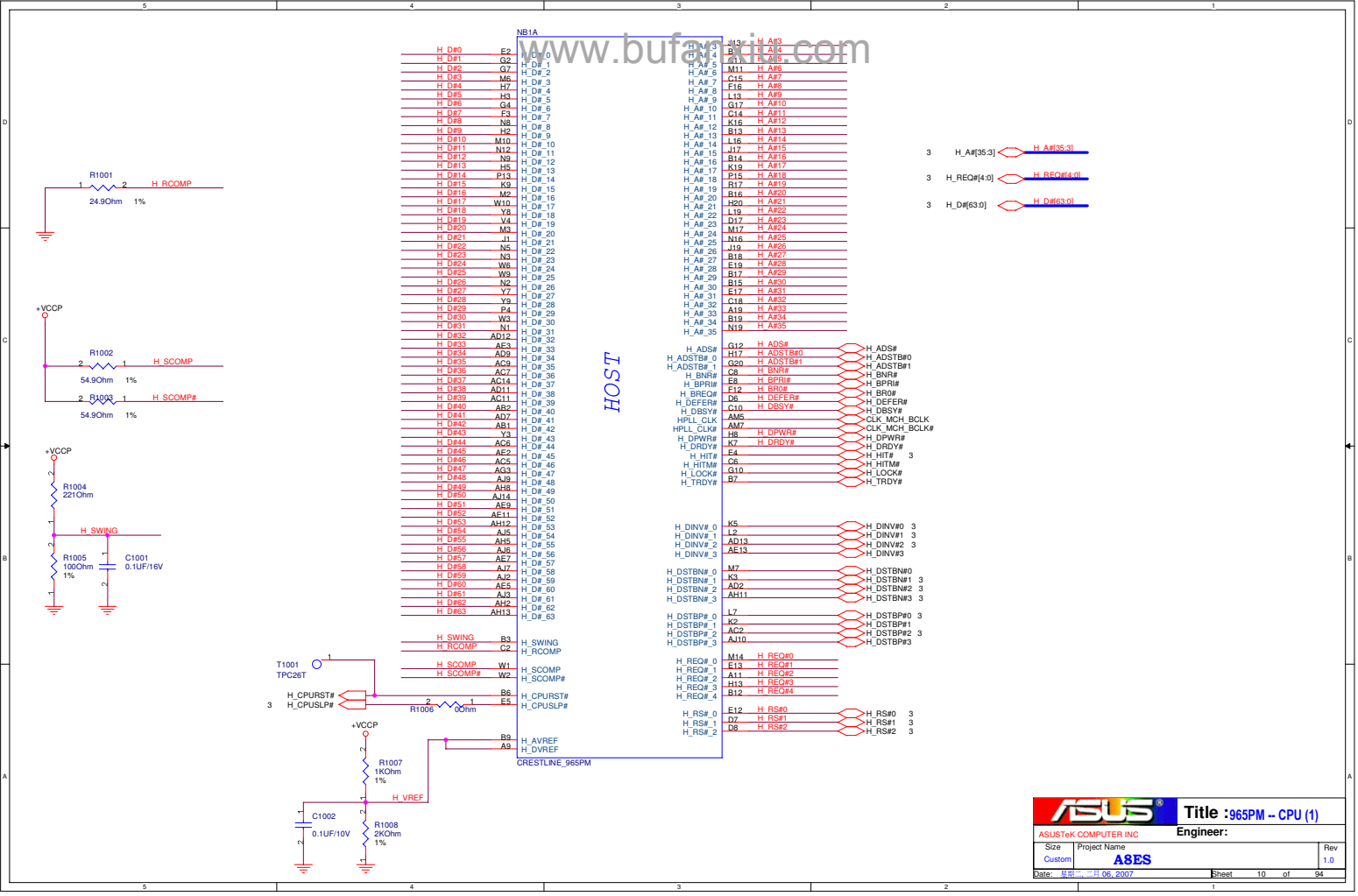


Title	DDR SO-DIMM_TOP
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: A8ES
Rev	1.0
Date: 星期二, 二月 06, 2007	Sheet 8 of 94



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V

ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 星期五, 六月 08, 2007	Sheet 9 of 94	



ASUSTeK COMPUTER INC

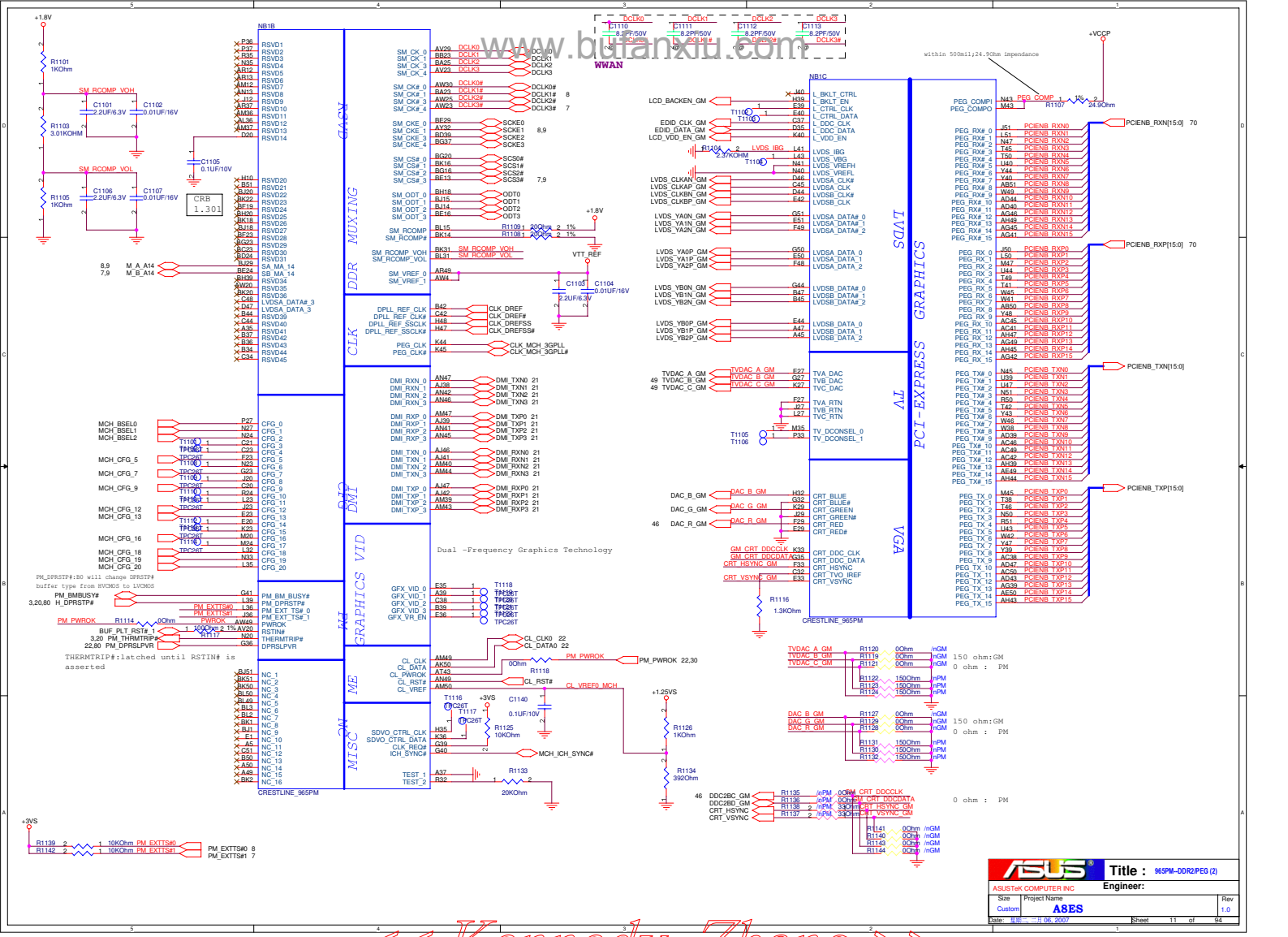
Title : 965PM -- CPU (1)

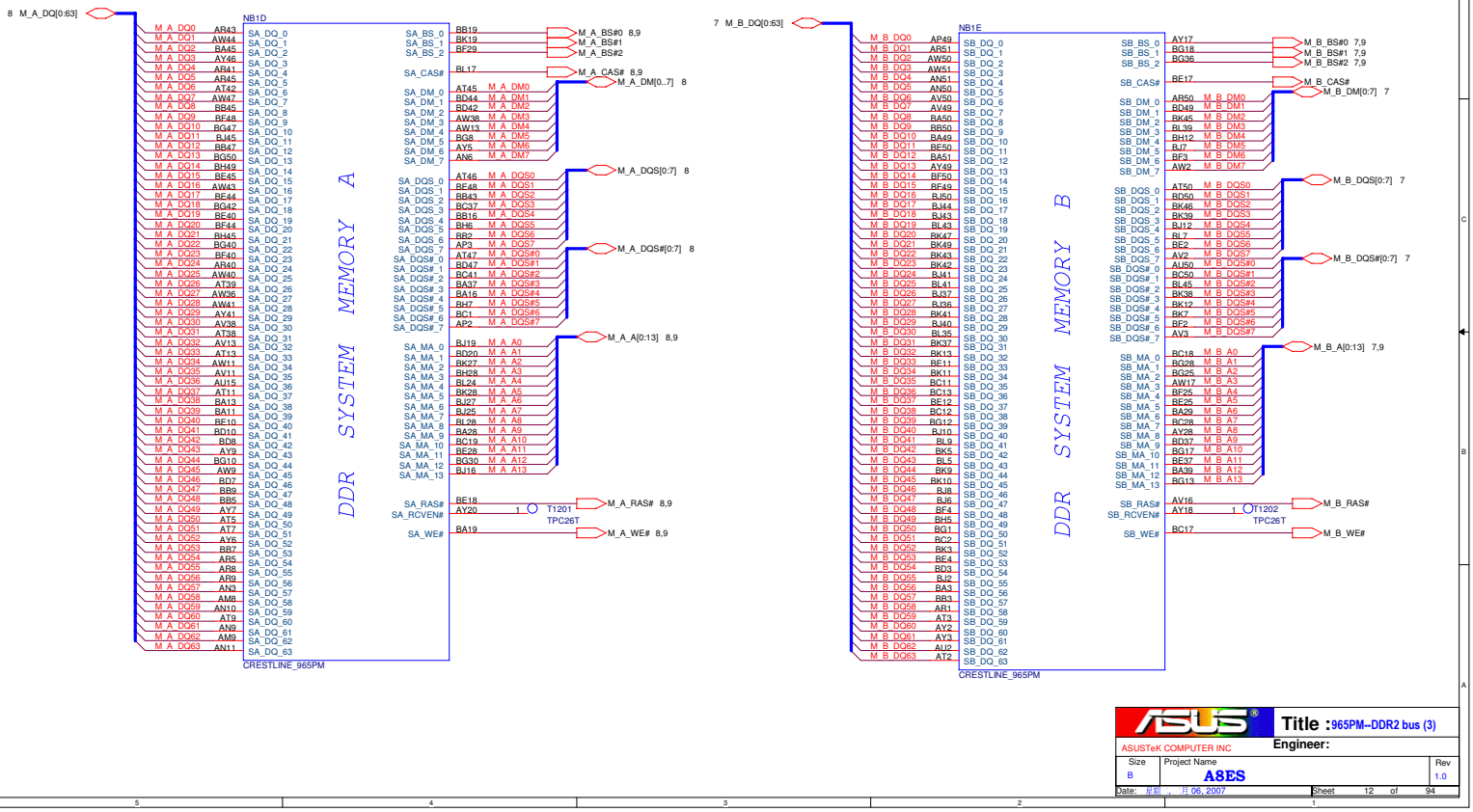
Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期二, 二月 06, 2007 Sheet 10 of 94

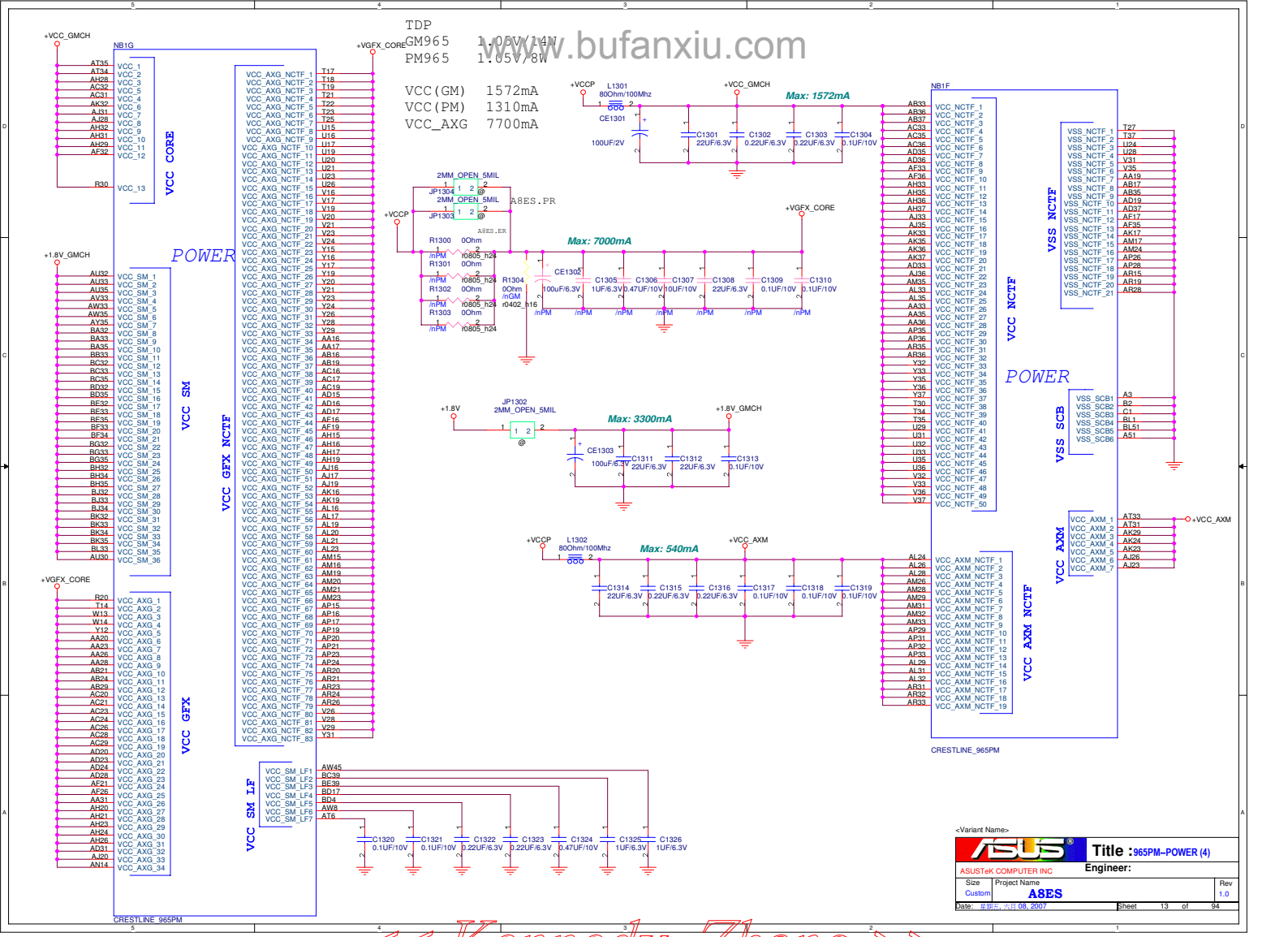
<< Kennedy_Zhang >>


www.butianxiu.com
NB1B
NB1C
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
SA_MA_14
SB_MA_14
RSVD34
RSVD35
RSVD38
LVDSA_DATA#_3
LVDSA_DATA_3
RSVD39
RSVD40
RSVD41
RSVD42
RSVD43
RSVD44
RSVD45
GMCH
DDR MUXING
CLK
DMI
PCI-EXPRESS GRAPHICS
LVDS
TV
VGA
GRAPHICS VID
MISC
CRESTLINE_965PM
WWAN
Dual -Frequency Graphics Technology
THERMTRIP#:latched until RSTIN# is asserted
PM_DPRSTP#:B0 will change DPRSTP# buffer type from HVCMOS to LVCMOS
within 500mil;24.9Ohm impendance
Title : 965PM-DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Project Name
A8ES
Rev
1.0
Sheet 11 of 94
<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC	Title : 965PM--DDR2 bus (3)	
	Engineer:	
Size: B	Project Name: A8ES	Rev: 1.0
Date: 星期 一 月 06, 2007	Sheet 12 of 94	

<< Kennedy_Zhang >>



<Variant Name>

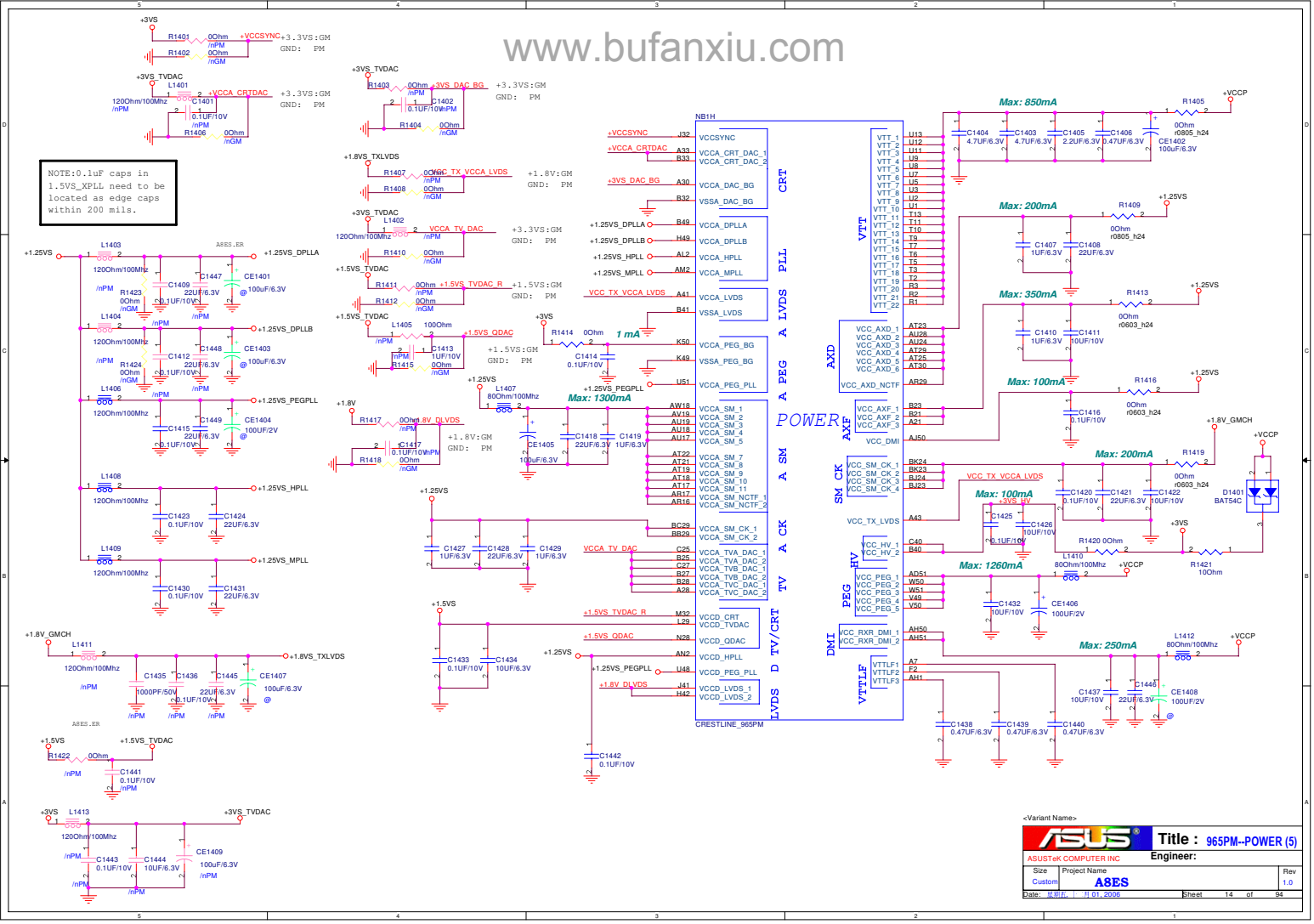
Title :965PM-POWER (4)

ASUSTeK COMPUTER INC

Engineer:

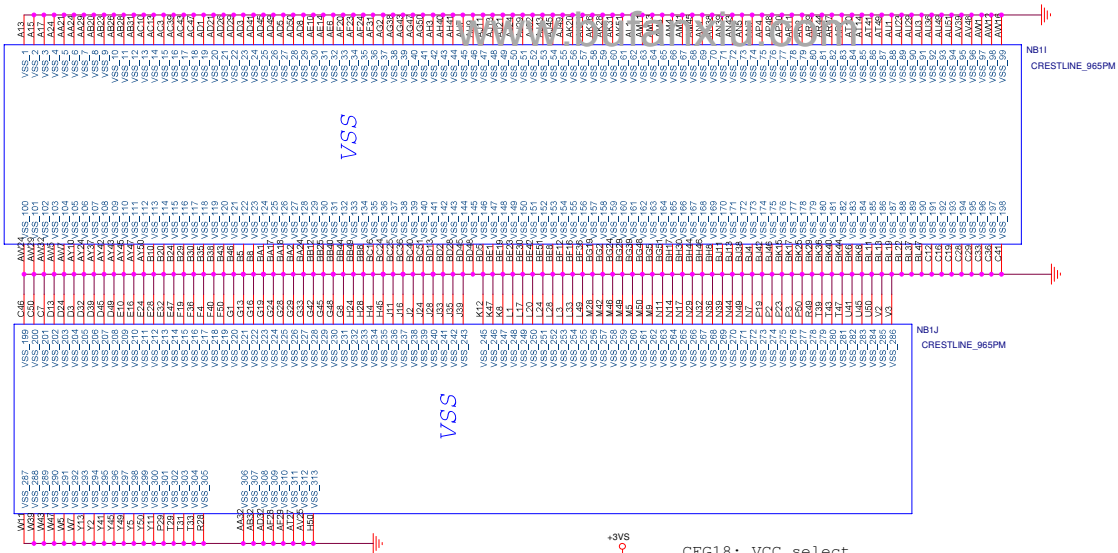
Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期五, 六月 08, 2007 Sheet 13 of 94



HIGH = LANES REVERSED

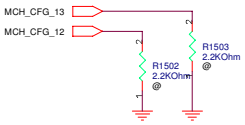
<< Kennedy_Zhang >>



CFG18: VCC select

LOW=1.05V (default)

HIGH= 1.5V



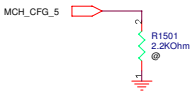
CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

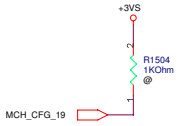
11= Normal Operation (Default)



CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

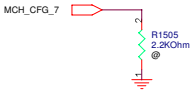
LOW = DMI X 2



CFG19 : DMI LANE REVERSAL

LOW = NORMAL (default)

HIGH = LANES REVERSED



CFG7 : CPU STRAP

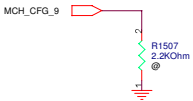
HIGH = Mobile CPU (Default)

LOW = Reserved

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational

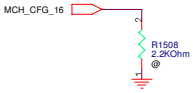
HIGH = SDVO and PCIE are operating simultaneously via the PEG port



CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

HIGH = Normal Operation (Default)



CFG16 : Dynamic ODT STRAP

Low = Dynamic ODT Disabled

HIGH = Dyanamic ODT Enabled (default)

ASUSTeK COMPUTER INC	Title : GND/Strapping (6)	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 星期一, 一月 08, 2007	Sheet 15 of 94	

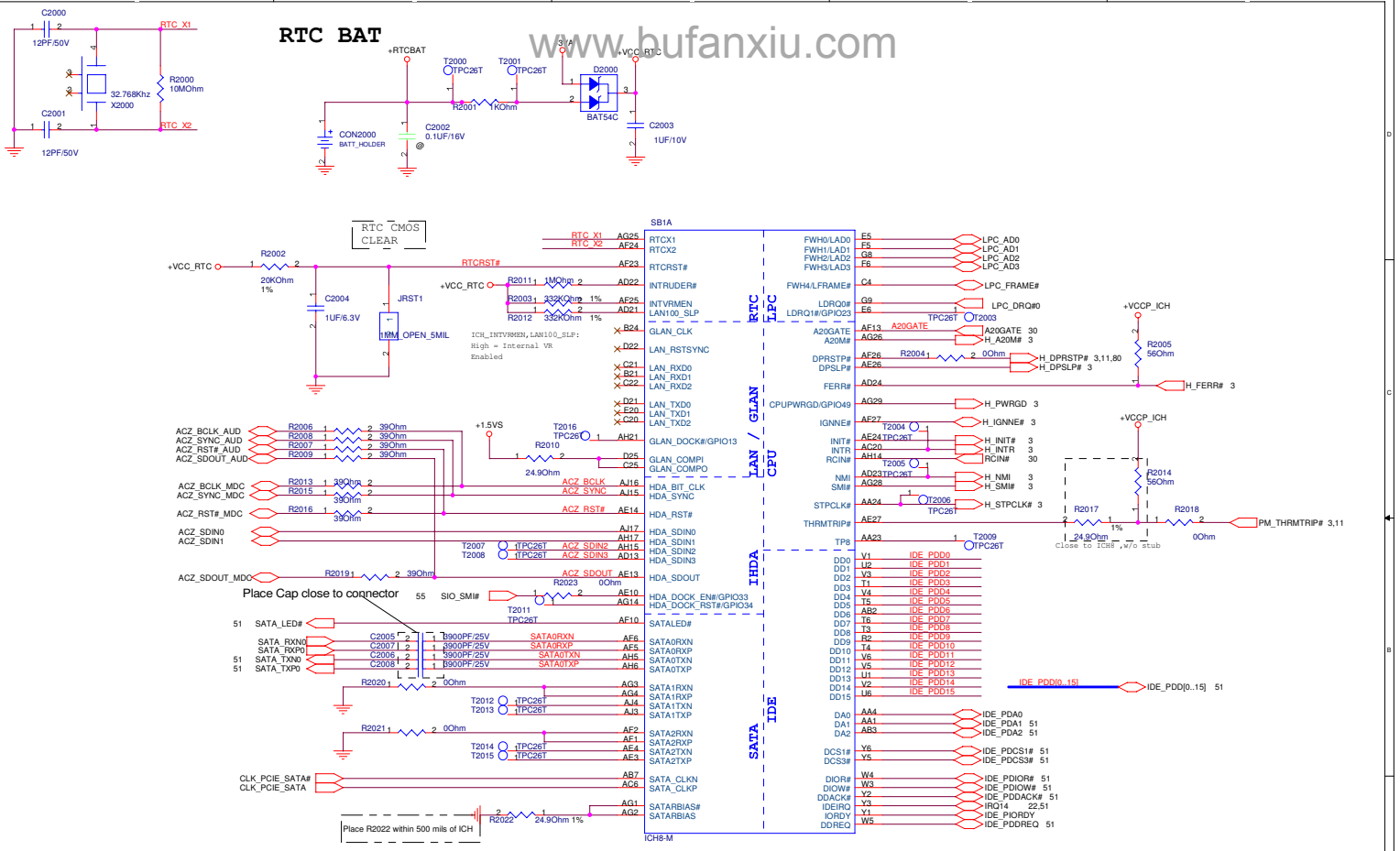
Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 16 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 17 of 94	

Title : BLANK		
ASUSTeK COMPUTER INC	Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 18 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 19 of 94	

RTC BAT



SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

<Variant Name>

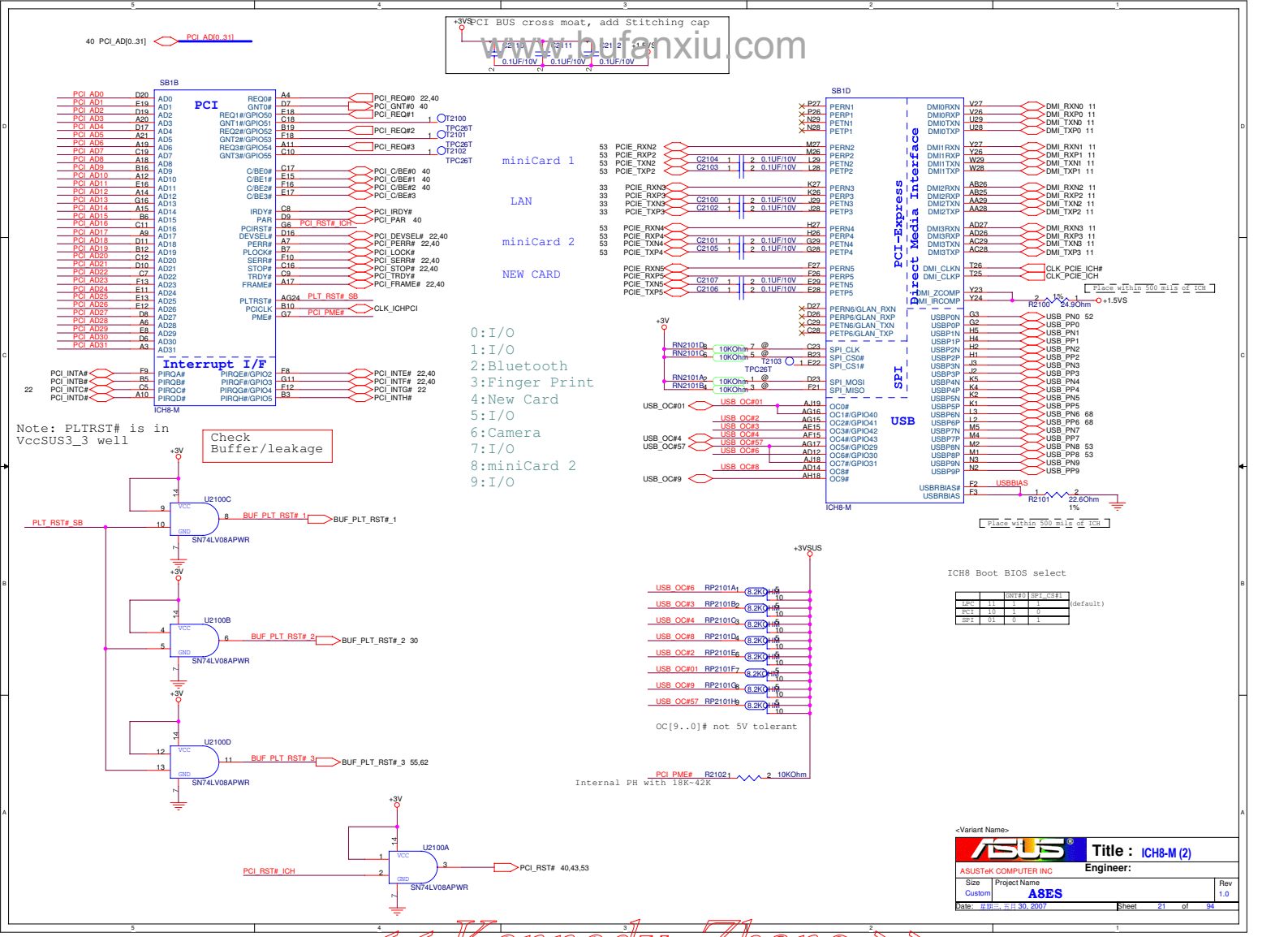
Title : ICH8-M (1)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期五, 六月 08, 2007 Sheet 20 of 94



<Variant Name>

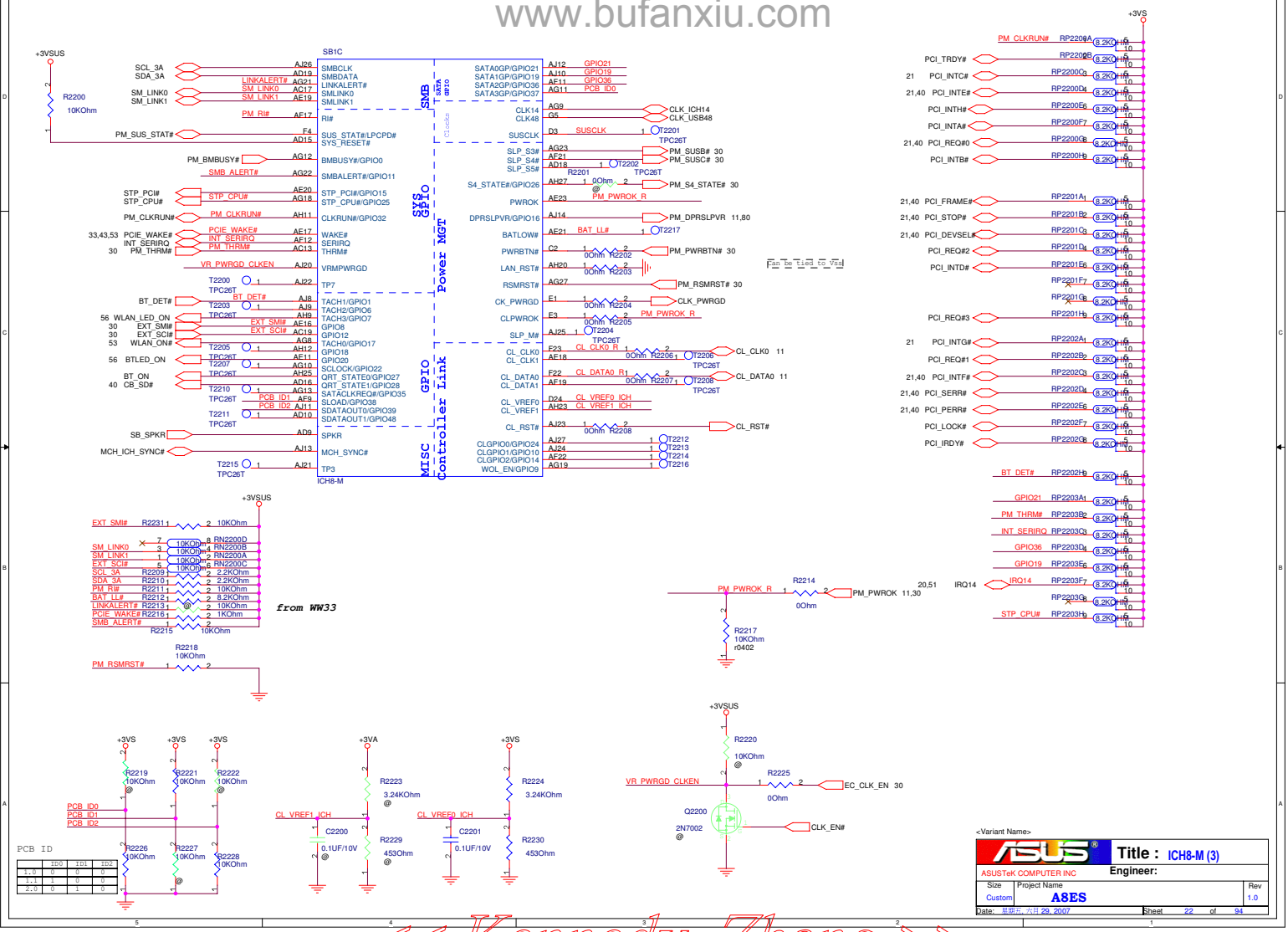
ASUSTeK COMPUTER INC

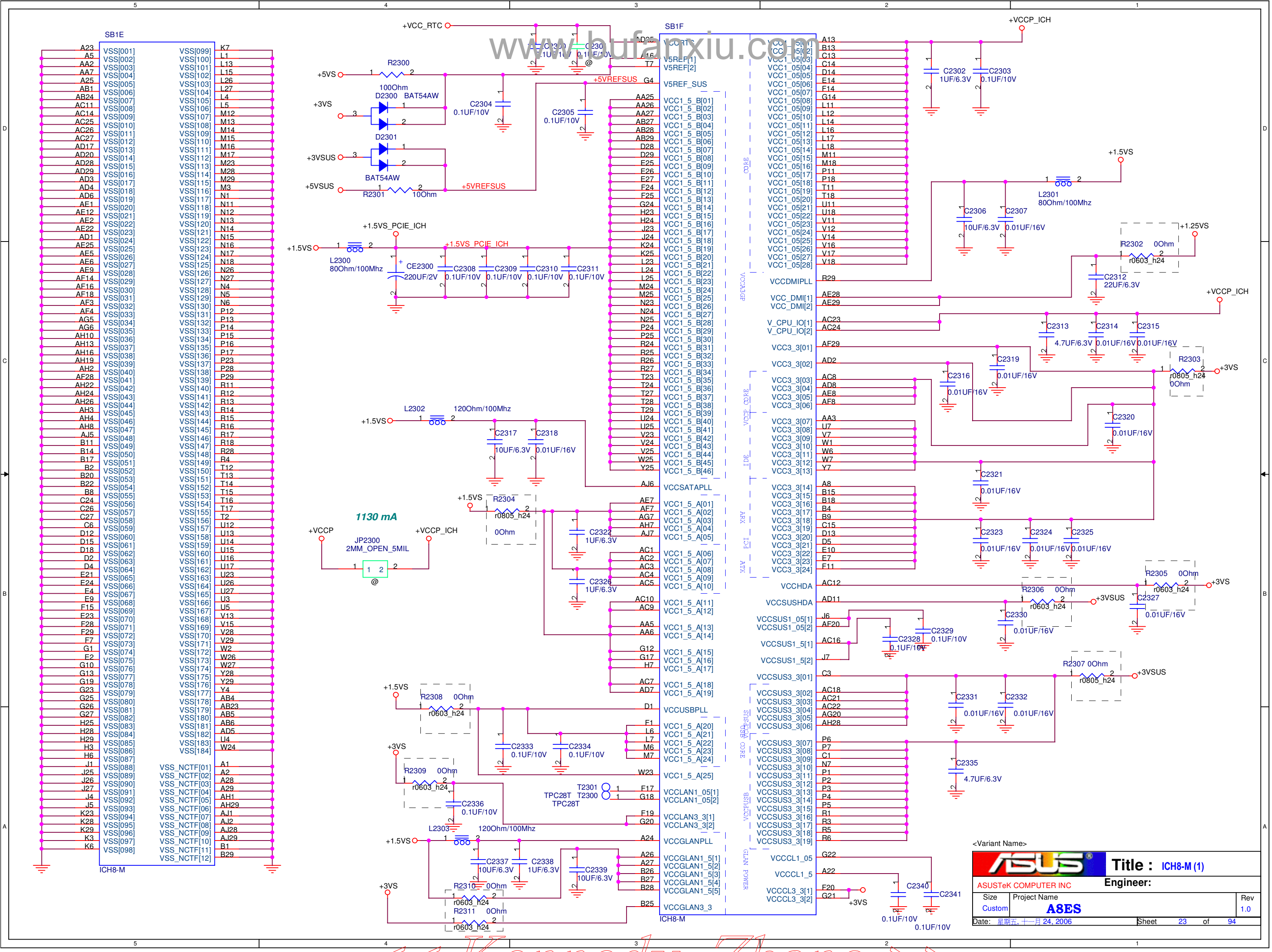
Title : ICH8-M (2)

Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

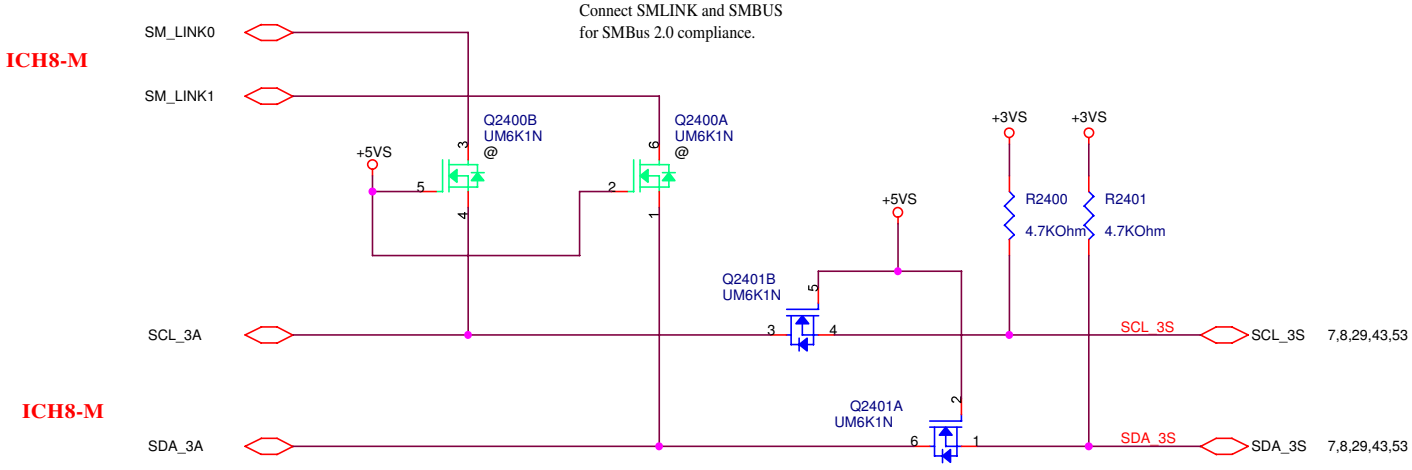
Date: 星期三, 五月 30, 2007 Sheet 21 of 94





Check

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer:

Size	Project Name	Rev
A	A8ES	1.0

Date: 星期二, 二月 06, 2007 Sheet 24 of 94

ICH8-M GPIO Assignment

Name	H/W Pin Definition	Type	Tolerance	Power Wel	Default	Mux	Native Name	Real Name	Note
GPIO0	PM_BMBUSY#	I/O	3.3V	Core	GPI	Yes	BMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	I/O	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	I/OD	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	I/OD	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	I/OD	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	I/OD	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	I/O	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	I/O	3.3V	Core	GPI	No			
GPIO8	EXT_SMI#	I/O	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	I/O	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	I/O	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		I/O	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SCI#	I/O	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	I/O	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	I/O	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PCI#	I/O	3.3V	Resume	Native	No	STP_PCI#	STP_PCI#	
GPIO16	PM_DPRSLPVR	I/O	3.3V	Core	Native	Yes	DPRSLPVR	PM_DPRSLPVR	
GPIO17	WLAN_ON#	I/O	3.3V	Core	GPI	No			
GPIO18		I/O	3.3V	Core	GPO	No			
GPIO19		I/O	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	I/O	3.3V	Core	GPO	No			
GPIO21		I/O	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		I/O	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		I/O	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	I/O	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC; note by Alan
GPIO25	STP_CPU#	I/O	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM_S4_STATE#	I/O	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON#/BT_ON	I/O	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	I/O	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	I/O	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	I/O	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	I/O	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	I/O	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	I/O	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	I/O	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	I/O	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	I/O	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	I/O	3.3V	Core	GPI	Yes	SDATAOUT0		
GPIO40	OC4#	I/O	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	I/O	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	I/O	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	I/O	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		I/O	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	I/O	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	I/O	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	I/O	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	I/O	3.3V	Core	Native	Yes	GNT2#		
GPIO54		I/O	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		I/O	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

Title : BLANK

Engineer:

ASUSTeK COMPUTER INC

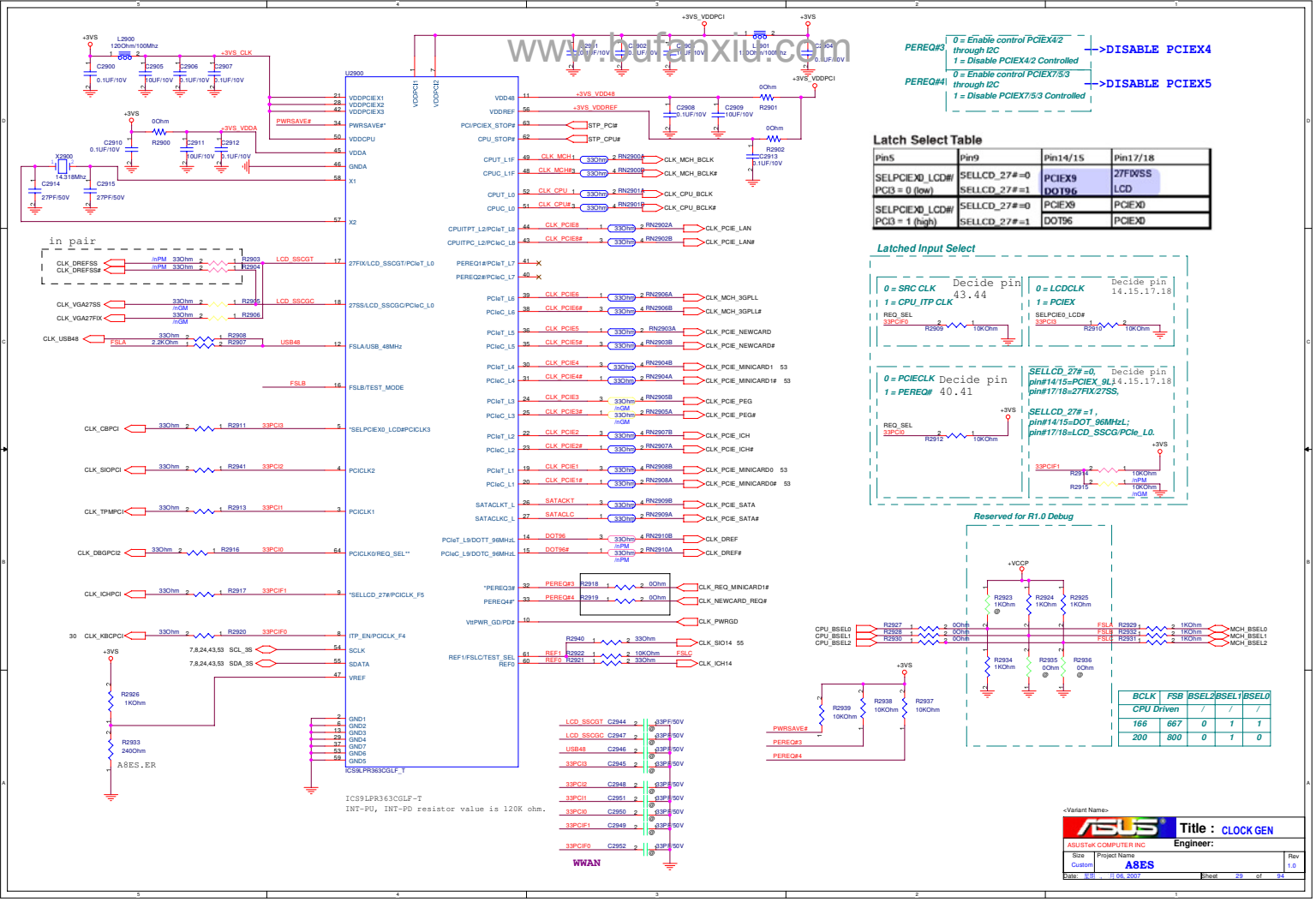
Size: A | Project Name: A8ES | Rev: 0

Date: 星期三, 十月 11, 2006 | Sheet 25 of 94

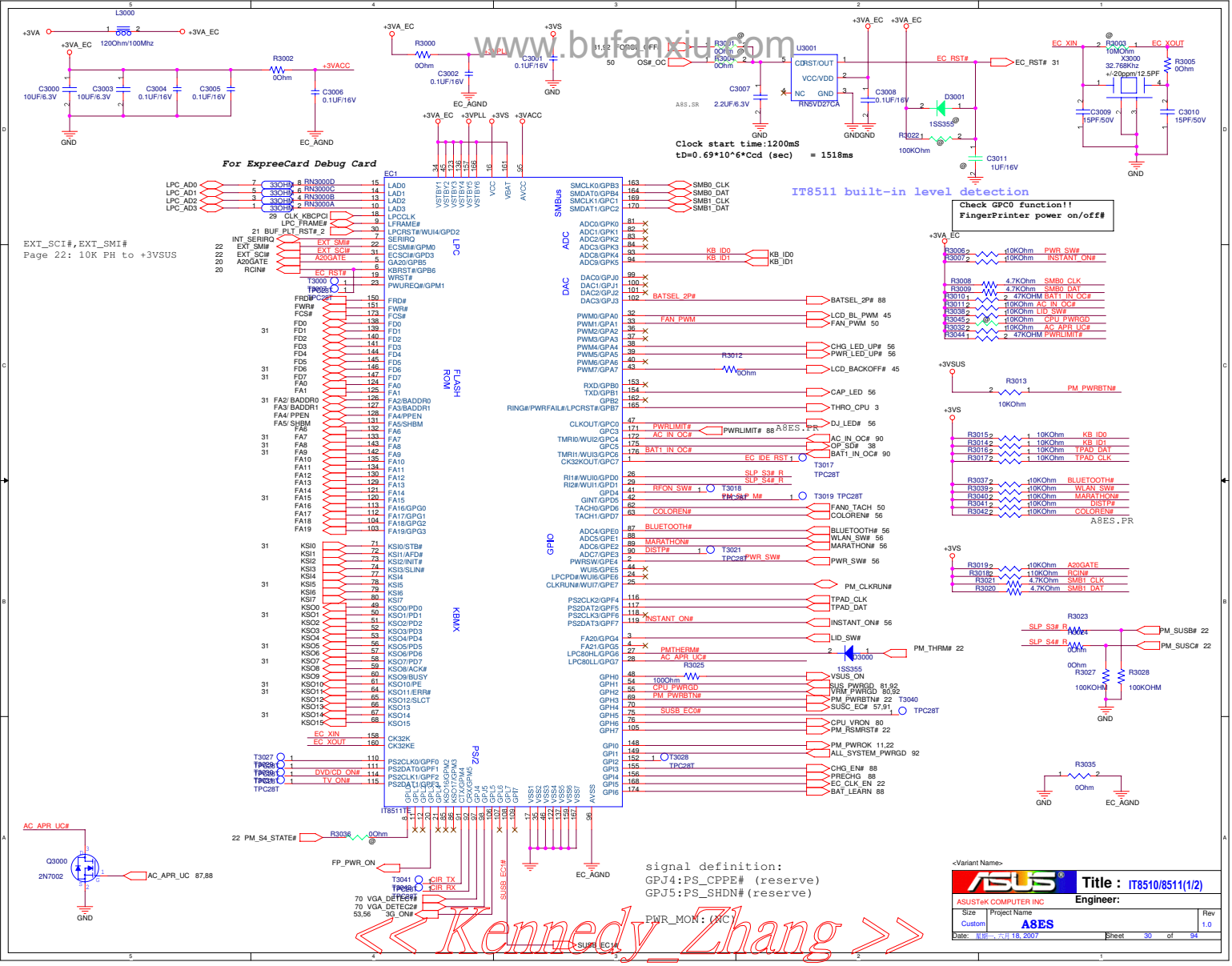
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 26 of 94	

ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 27 of 94	

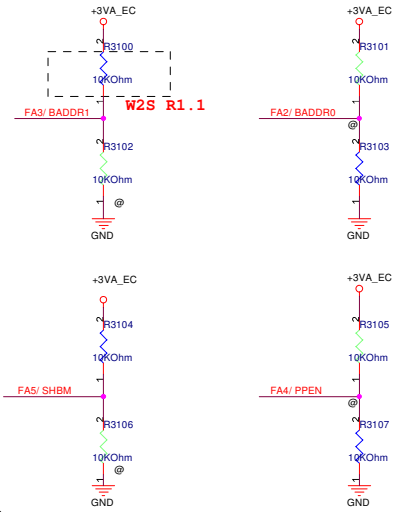
ASUSTeK COMPUTER INC	Title : BLANK	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 28 of 94	



<< Kennedy_Zhang >>

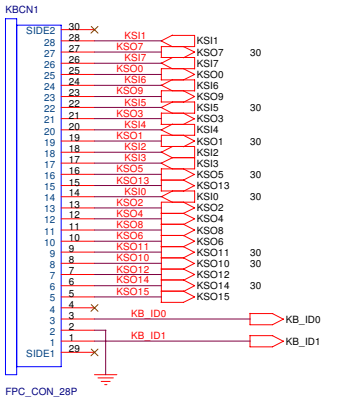

www.bufanxiu.com
For ExpreeCard Debug Card
EXT_SCI#,EXT_SMI#
Page 22: 10K PH to +3VSUS
IT8511 built-in level detection
Check GPC0 function!!
FingerPrinter power on/off#
Clock start time:1200mS
td=0.69*10^6*Ccd (sec) = 1518ms
signal definition:
GPJ4:PS_CPPE# (reserve)
GPJ5:PS_SHDN#(reserve)
PWR_MON: (NC)
<<Kennedy Zhang>>
Title : IT8510/8511(1/2)
ASUSTeK COMPUTER INC
Engineer:
A8ES
Date: 星期一, 六月 18, 2007

10:Determined by EC



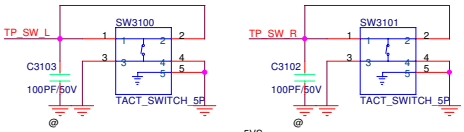
BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

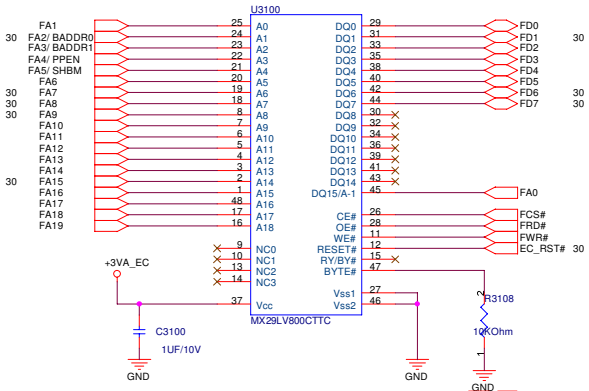


SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

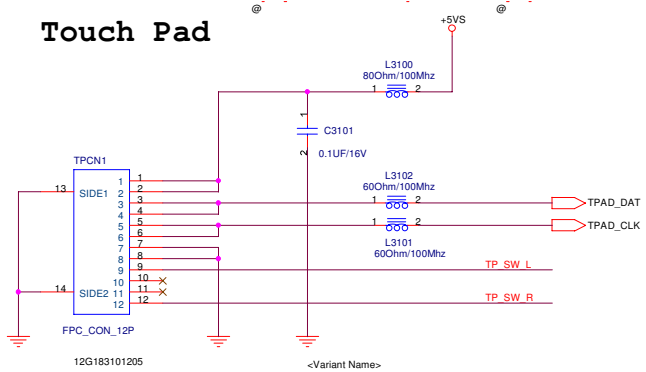
PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.



8M TSOP



Touch Pad



<Variant Name>

ASUSTeK COMPUTER INC

Title : IT8510/8511(2/2)

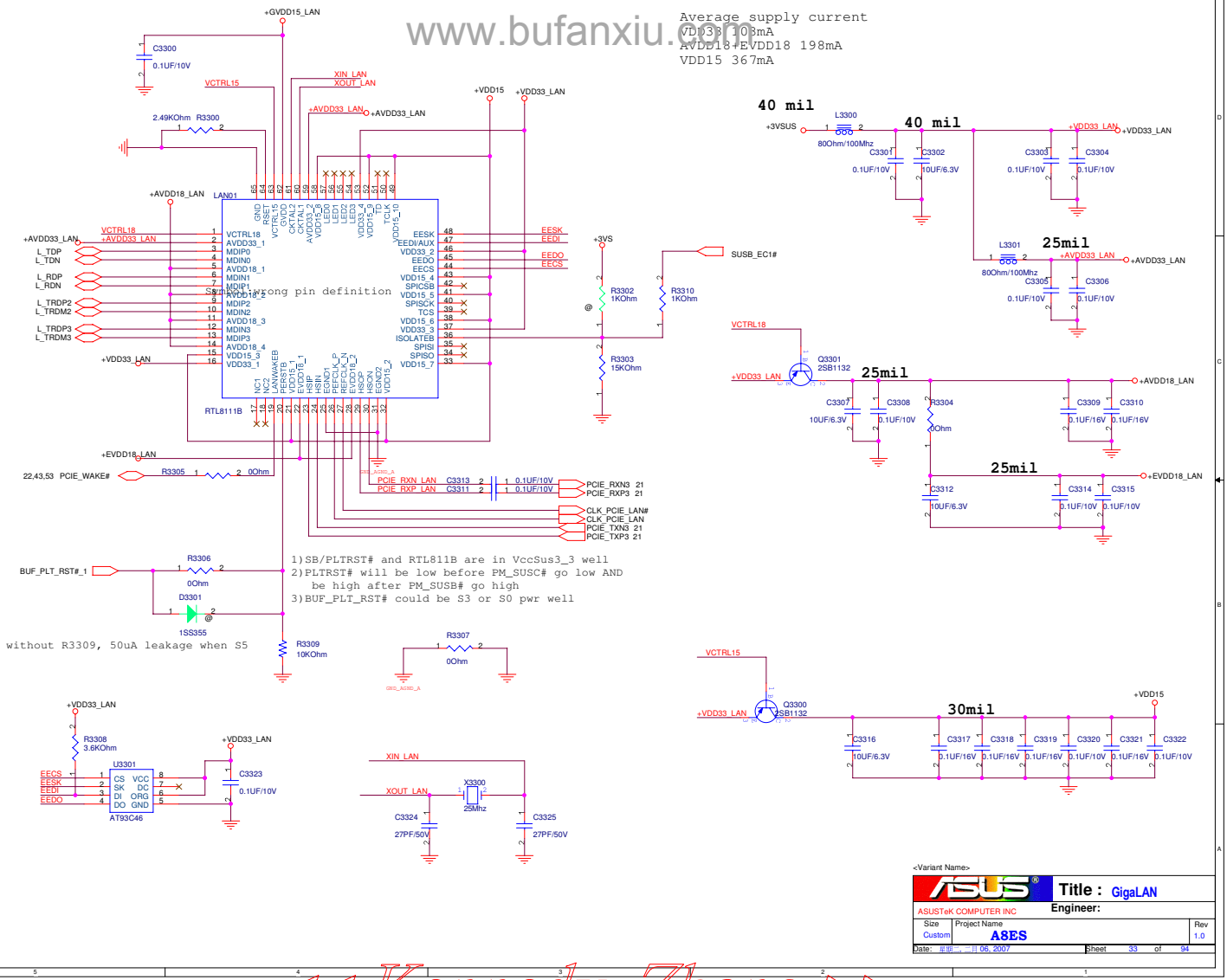
Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期日, 六月 24, 2007 Sheet 31 of 94

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 32 of 94	

Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



<Variant Name>

ASUSTeK COMPUTER INC

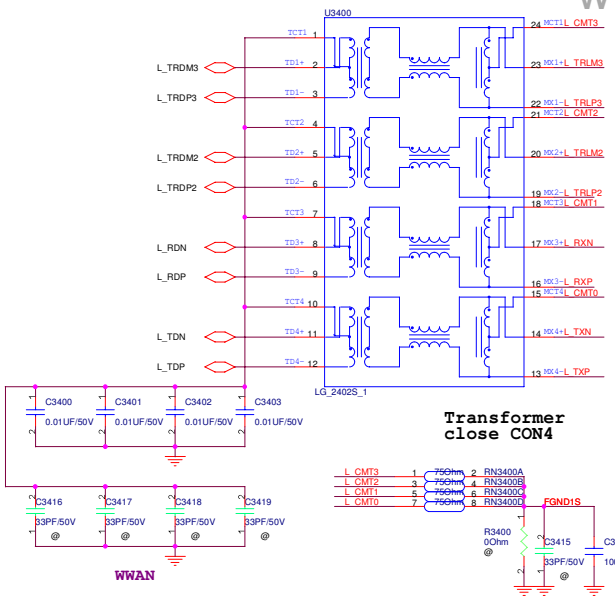
Title : GigaLAN

Engineer:

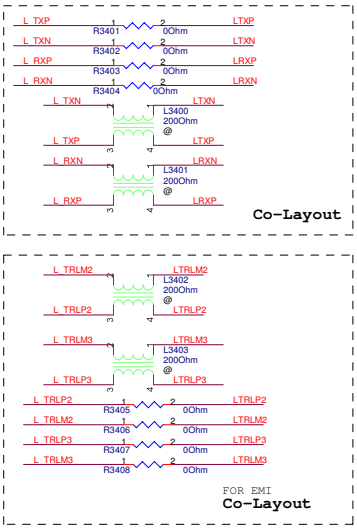
Size	Project Name	Rev
Custom	A8ES	1.0

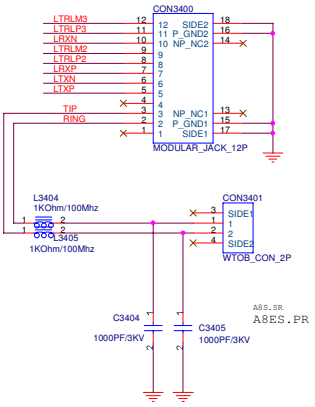
Date: 星期二, 一月 06, 2007 Sheet 33 of 94

2402S have issue after IR reflow,
alternative part:LG-2410S-1

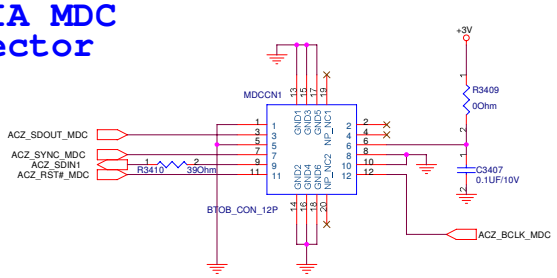


Transformer close CON4





AZALIA MDC Connector



<Variant Name>

ASUSTeK COMPUTER INC

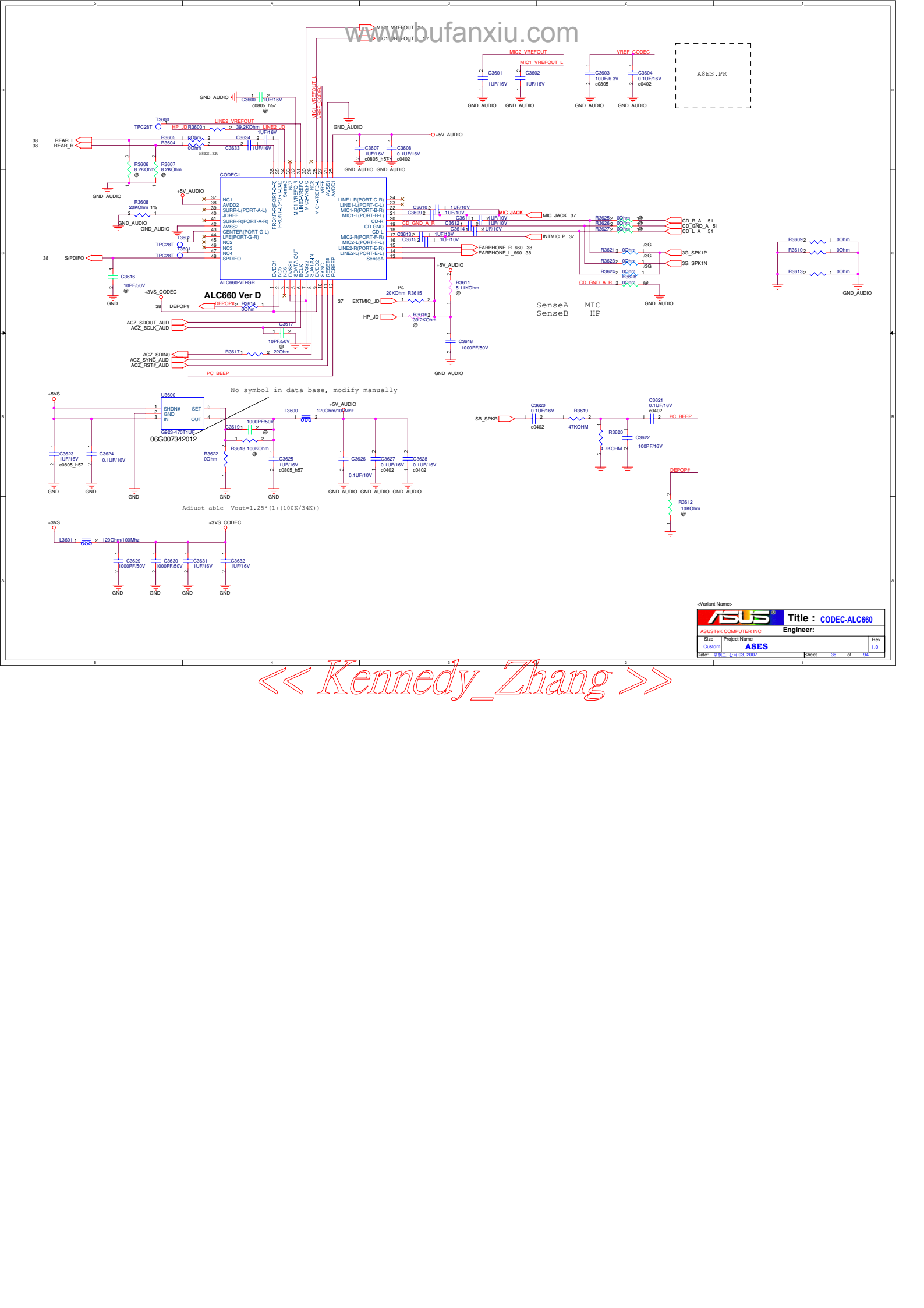
Title : RJ11+45 , MDC

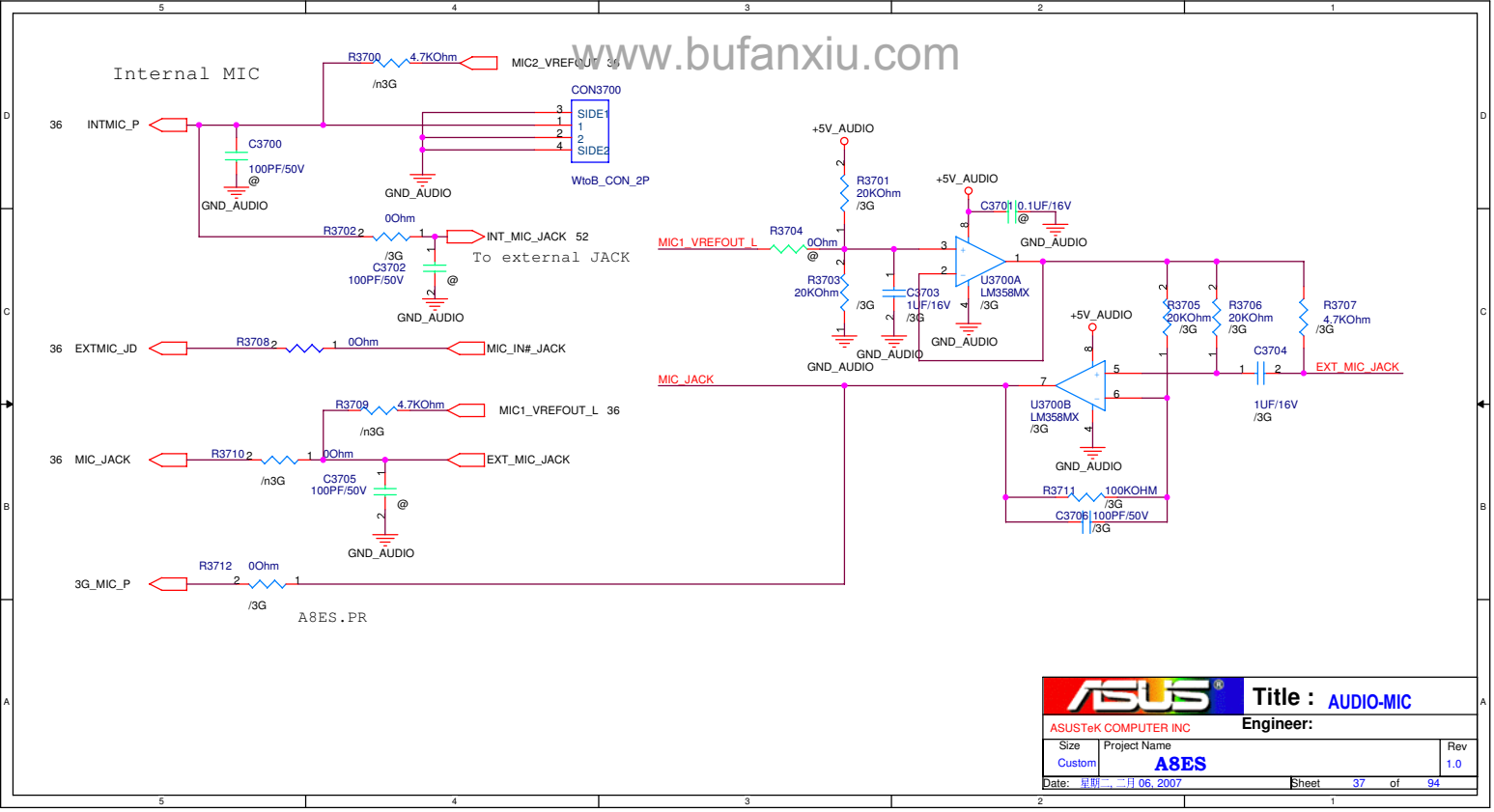
Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期二, 六月 12, 2007 Sheet 34 of 94

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 35 of 94	





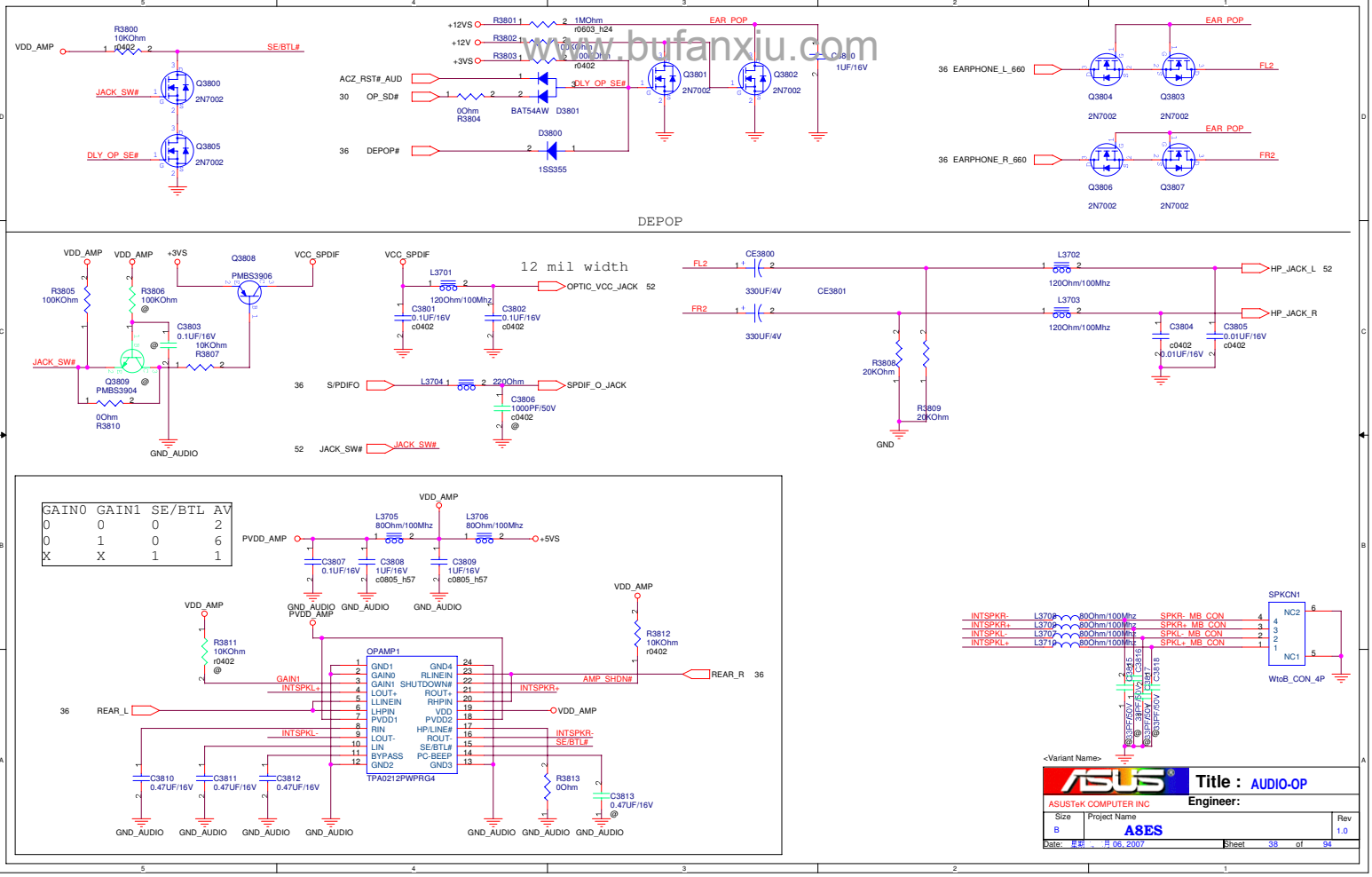
ASUSTeK COMPUTER INC

Title : AUDIO-MIC

Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期二, 二月 06, 2007 Sheet 37 of 94



DEPOP

<Variant Name>

ASUSTeK COMPUTER INC

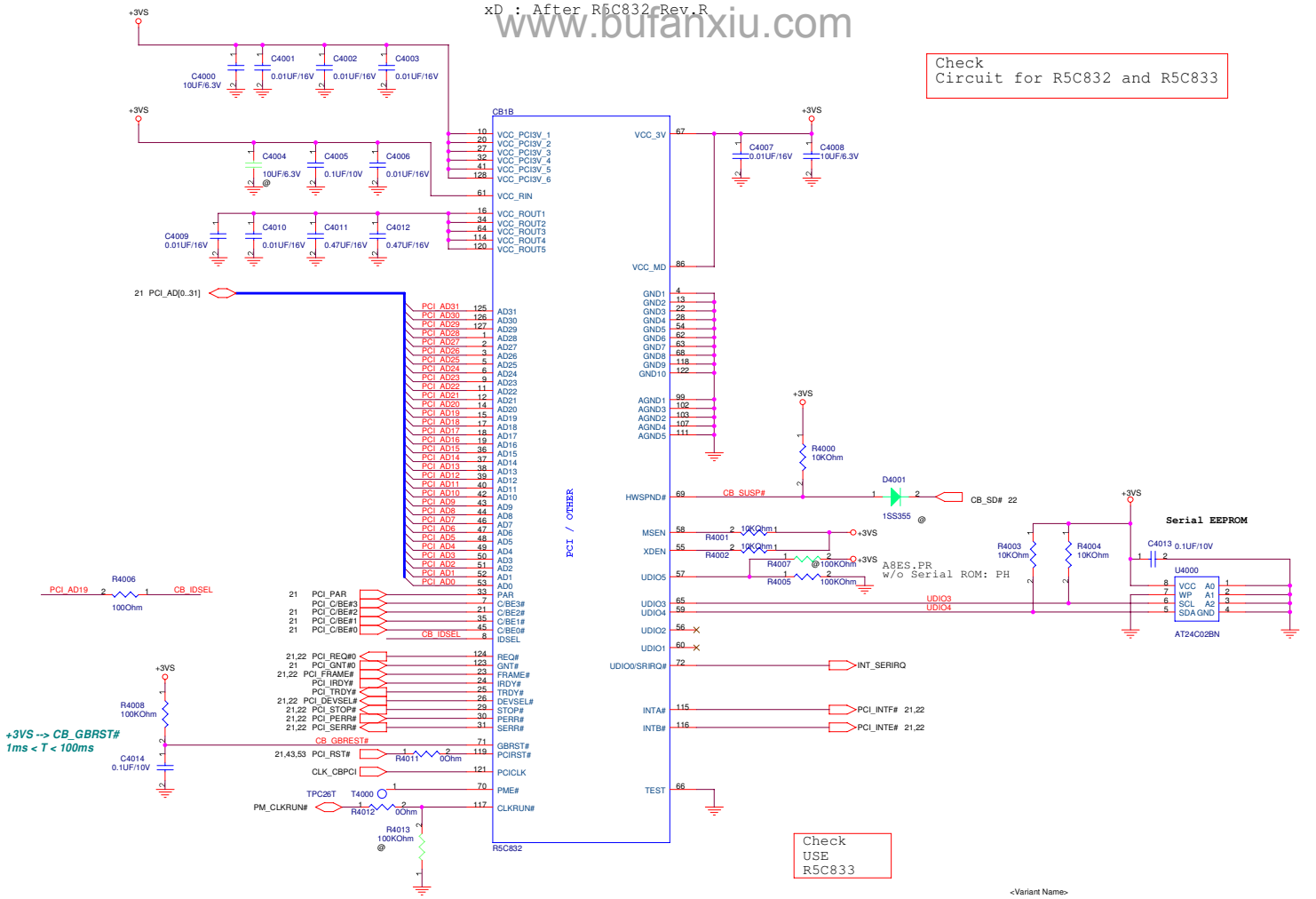
Title : AUDIO-OP

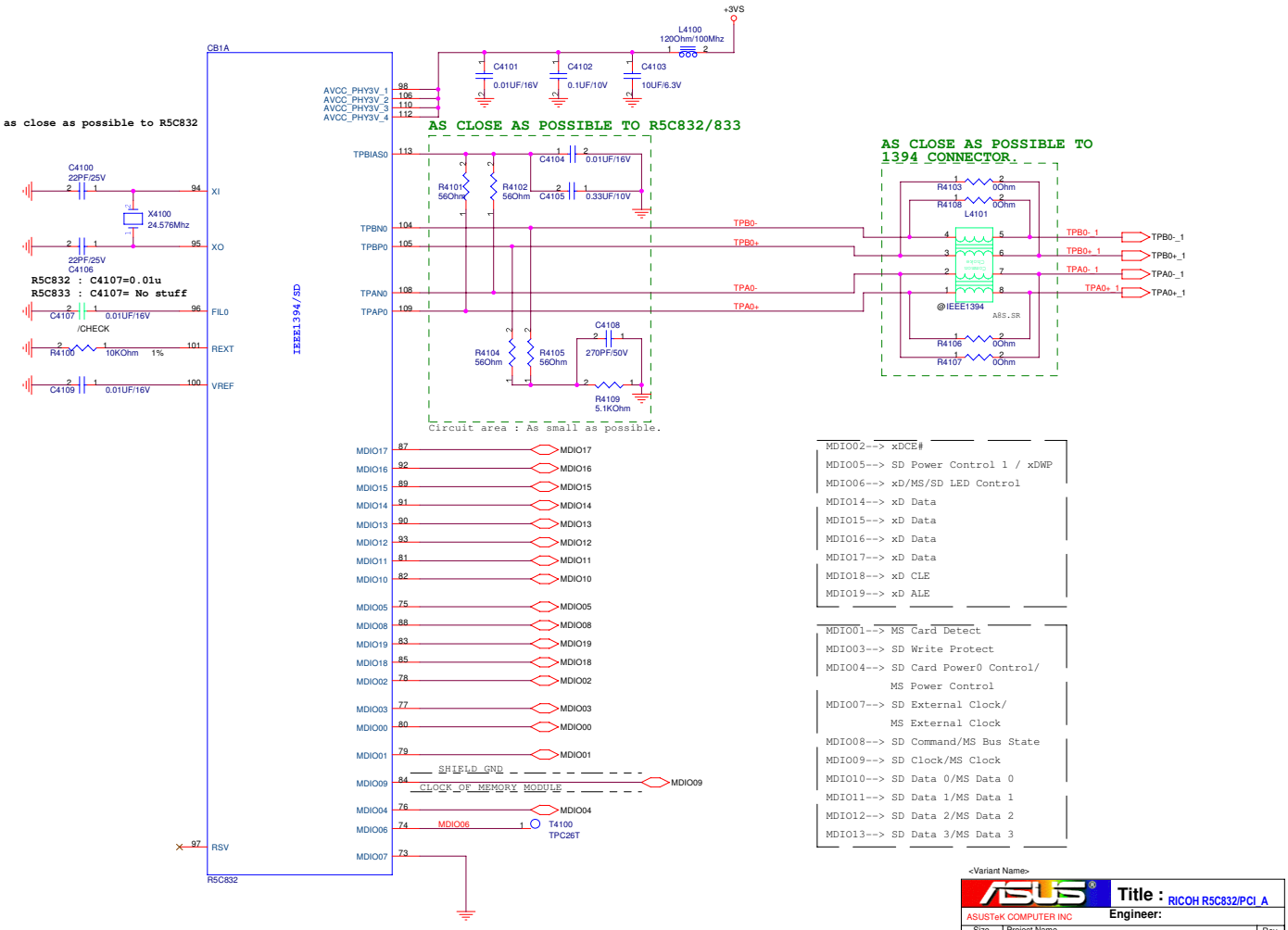
Engineer:

Size	Project Name	Rev
B	A8ES	1.0

Date: 星期 , 月 06, 2007 Sheet 38 of 94

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 39 of 94	





<Variant Name>

ASUSTeK COMPUTER INC

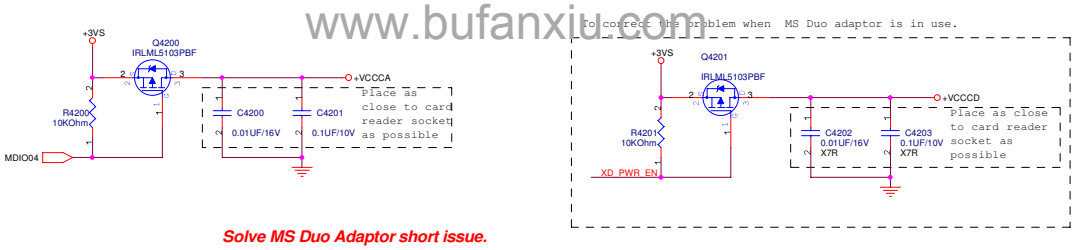
Title : RICOH R5C832/PCI_A

Engineer:

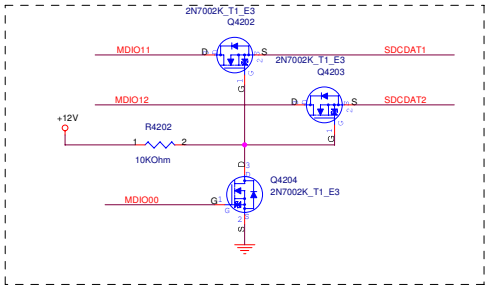
Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期一, 六月 28, 2007 Sheet 41 of 94

to correct the problem when MS Duo adaptor is in use.



Solve MS Duo Adaptor short issue.

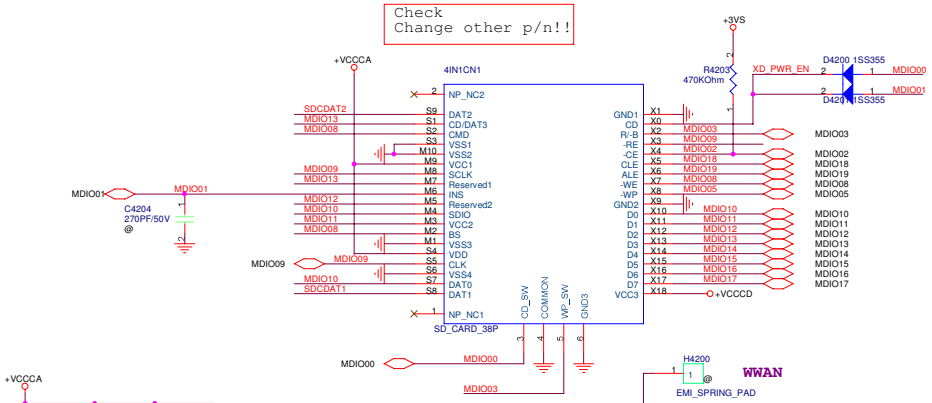


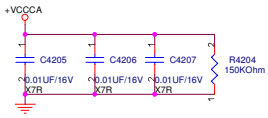
A8ES.PR
Change to 07G005000214, 2KV ESD

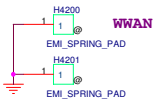
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

Check
Change other p/n!!

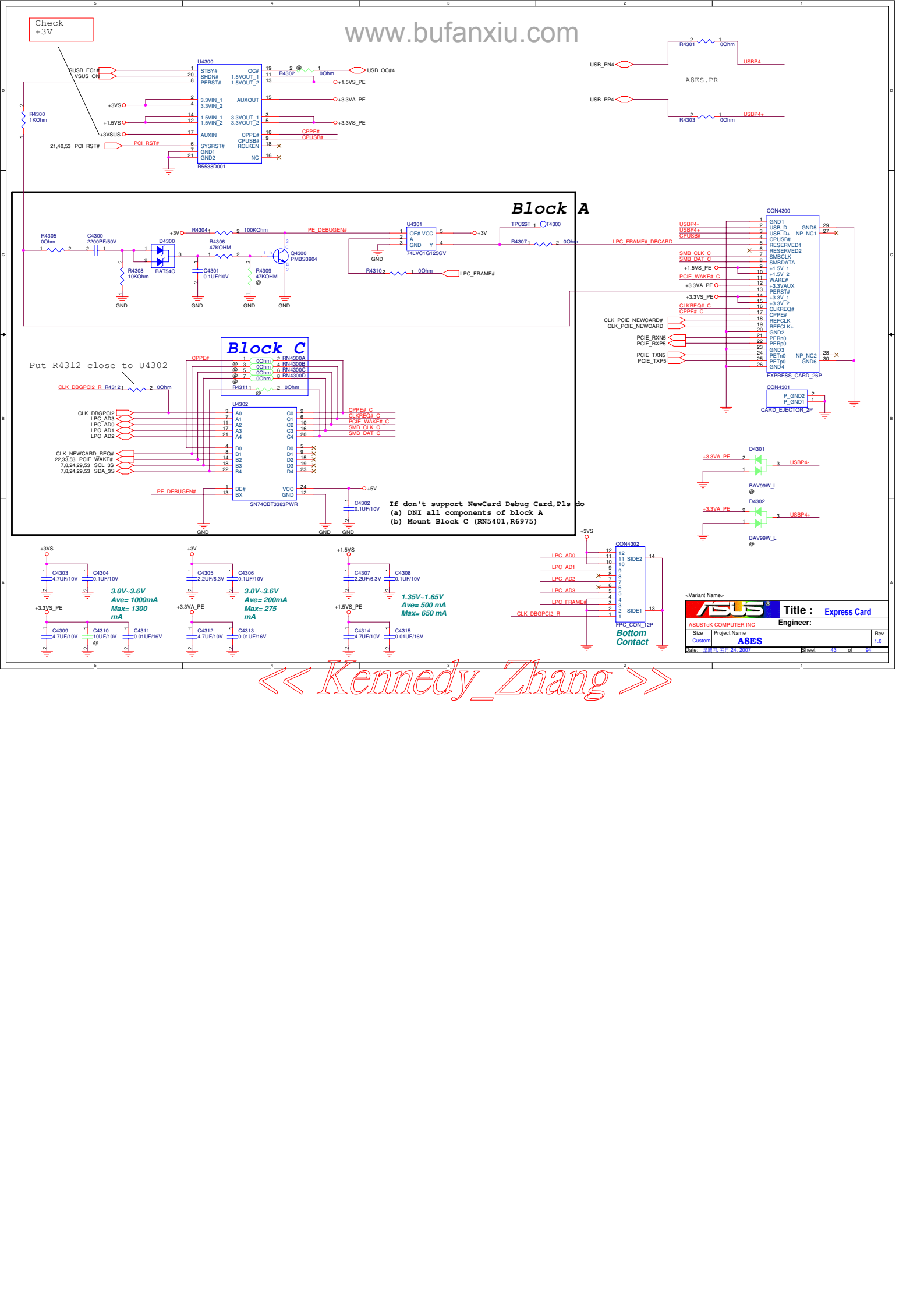






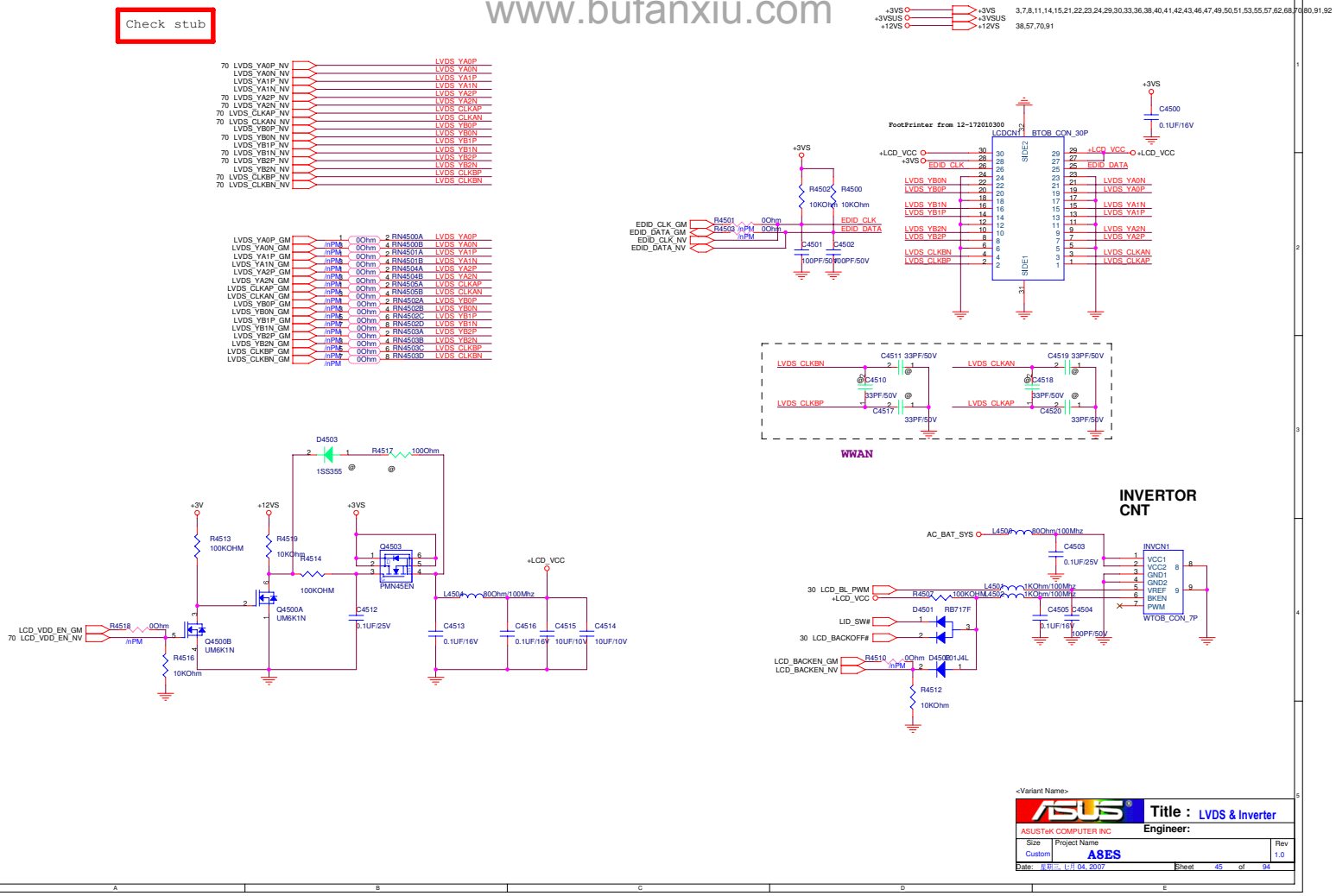
<Variant Name>

ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 星期六, 六月 29, 2007	Sheet 42 of 94	



ASUSTeK COMPUTER INC	Title : Blank			
	Engineer:			
Size: A	Project Name: A8ES			Rev: 1.0
Date: 星期三, 十月 11, 2006		Sheet 44 of 94		

Check stub



<Variant Name>

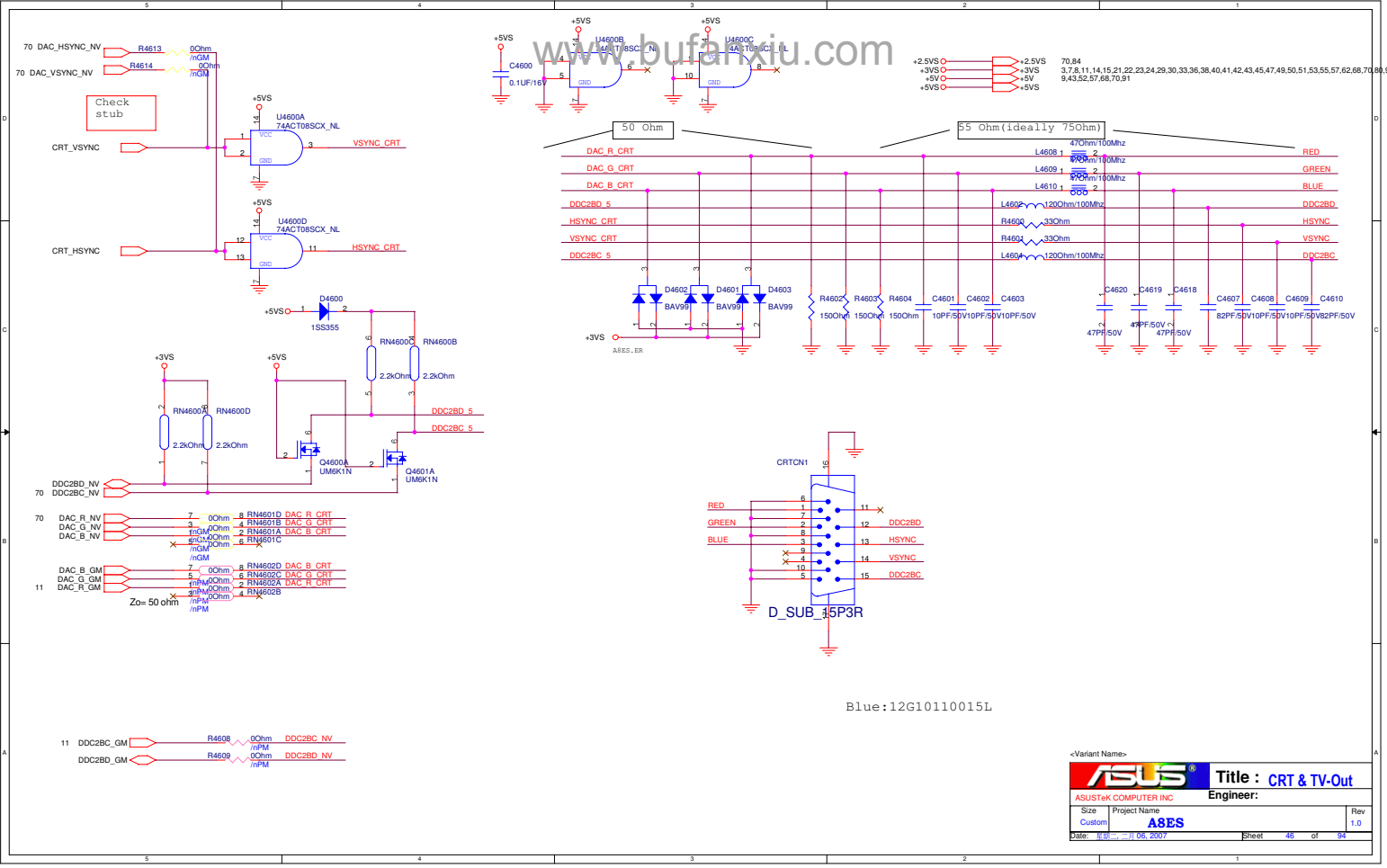
ASUSTeK COMPUTER INC

Title : LVDS & Inverter

Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期二, 七月 04, 2007 Sheet 45 of 94



Blue:12G10110015L

<Variant Name>

ASUSTeK COMPUTER INC

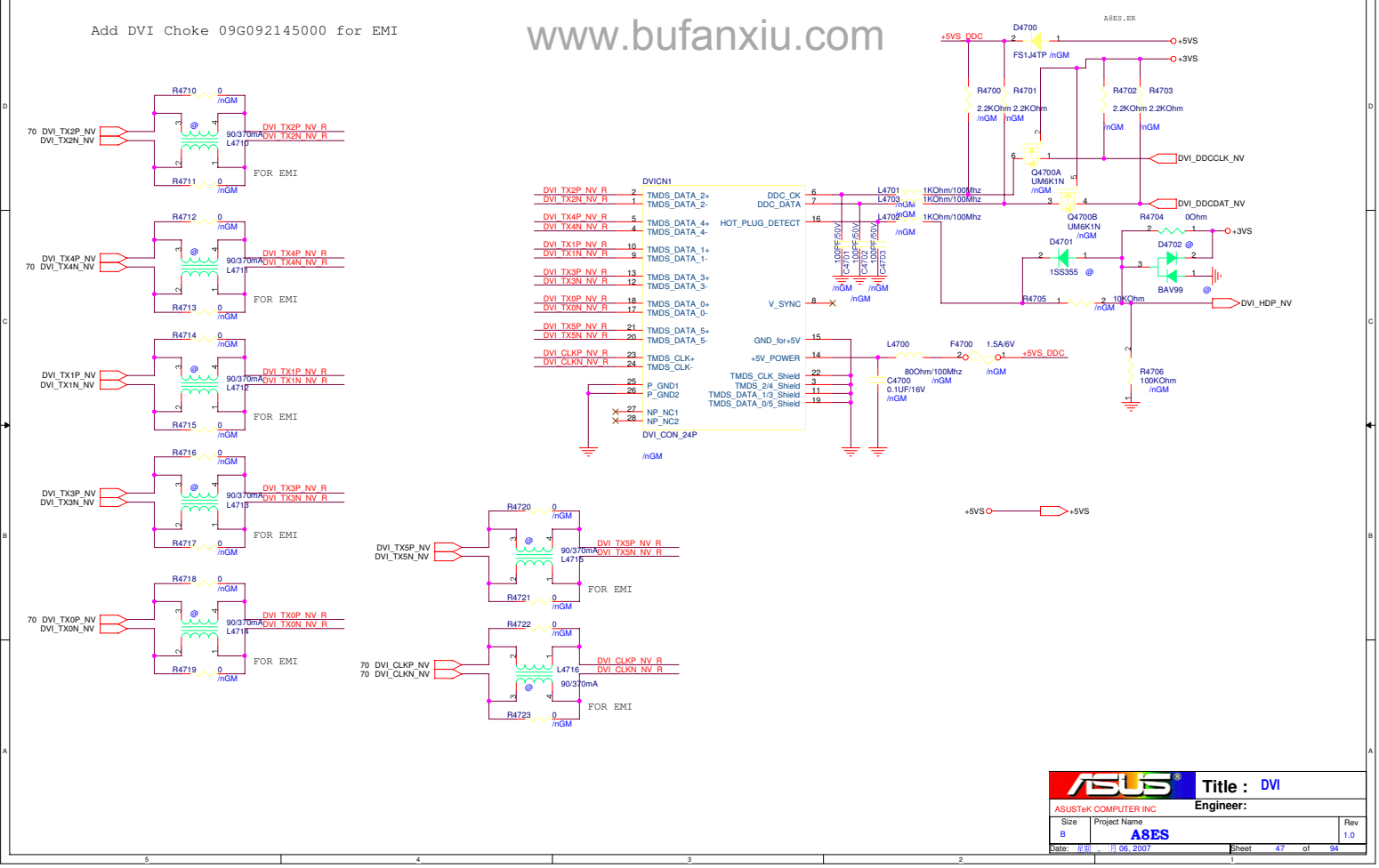
Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 星期二, 二月 06, 2007 Sheet 46 of 94

Add DVI Choke 09G092145000 for EMI



ASUSTeK COMPUTER INC

Title : DVI

Engineer:

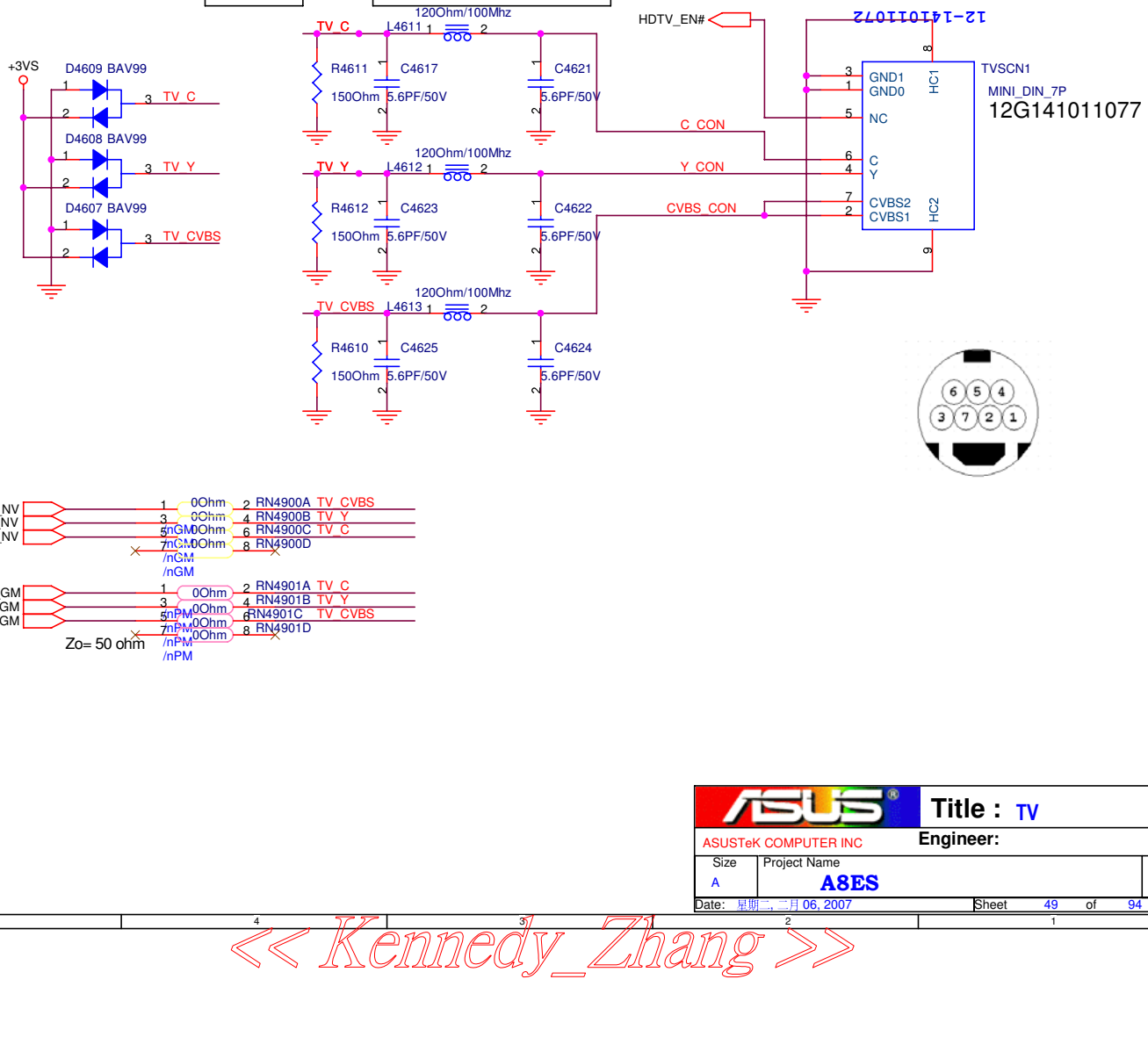
Size	Project Name	Rev
B	A8ES	1.0

Date: 星期二, 一月 06, 2007 Sheet 47 of 94

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 48 of 94	

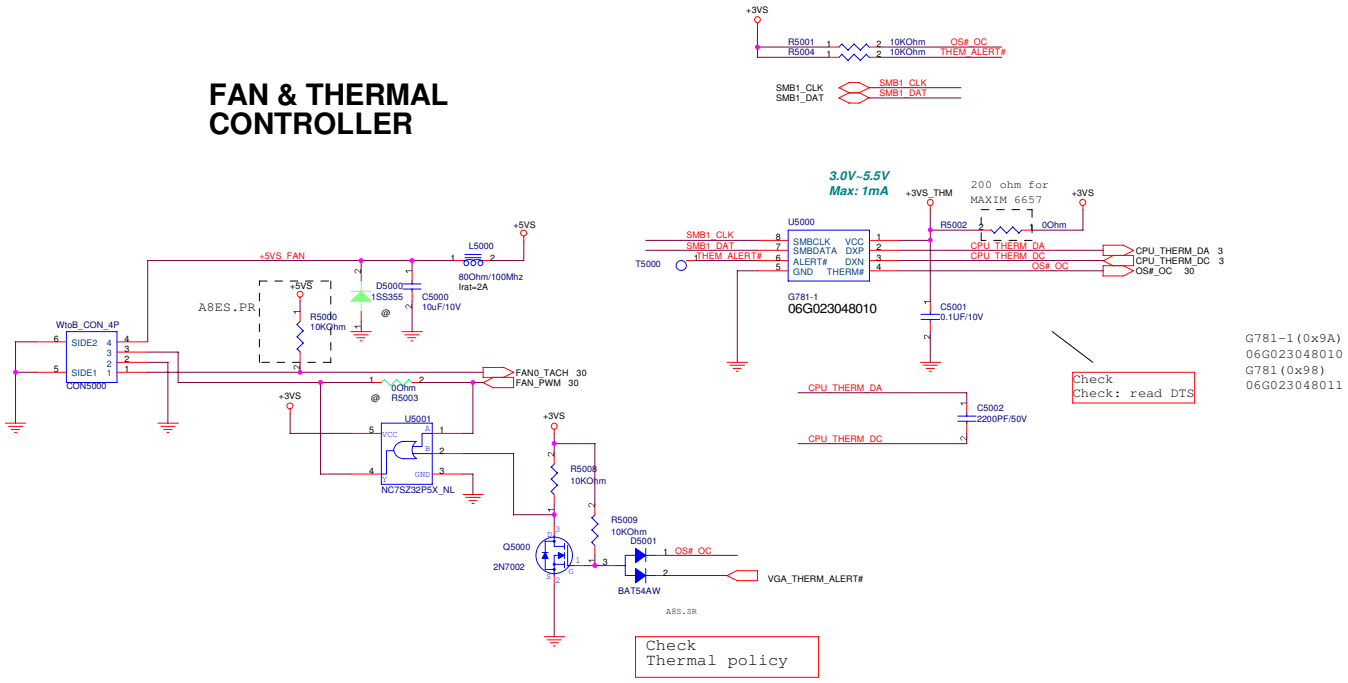
50 Ohm

55 Ohm(ideally 75Ohm)



ASUSTeK COMPUTER INC	Title : TV	Engineer:
Size: A	Project Name: A8ES	Rev: 1.0
Date: 星期二, 二月 06, 2007	Sheet 49 of 94	

FAN & THERMAL CONTROLLER



<Variant Name>

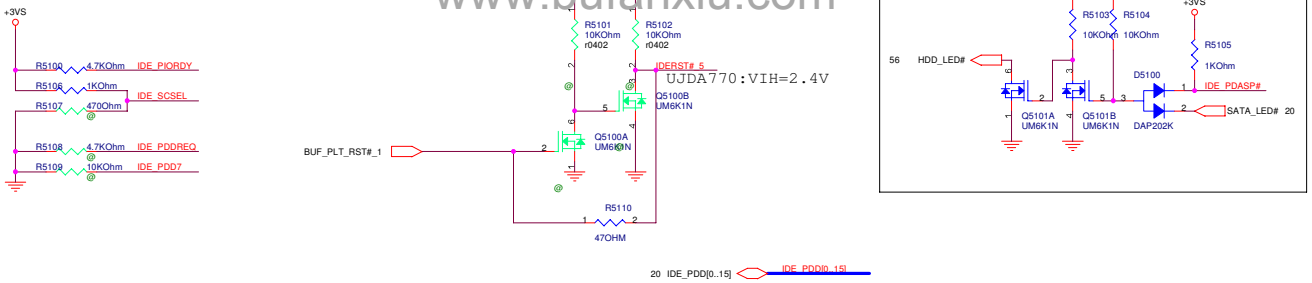
ASUSTeK COMPUTER INC

Title : FAN & THERMAL

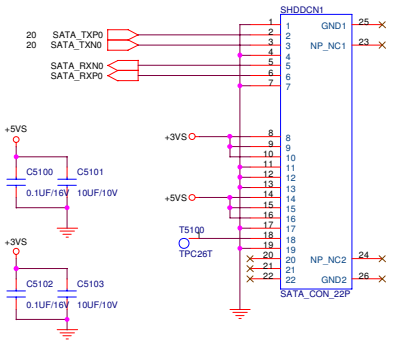
Engineer:

Size	Project Name	Rev
B	A8ES	1.0

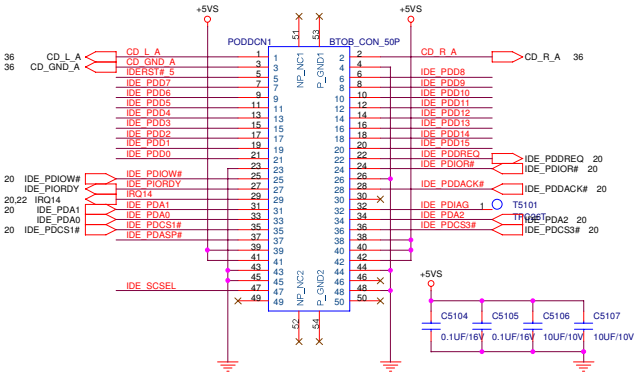
Date: 星期 , 月 06, 2007 Sheet 50 of 94



SATA HDD CON



PATA CD-ROM CON



+3VS
+5VS
+5V
3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92
9,43,52,57,68,70,91

ASUSTeK COMPUTER INC

Title : HDD & ODD

Engineer:

Size	Project Name	Rev
B	A8ES	1.0

Date: 星期 , 月 06, 2007 Sheet 51 of 94

A8ES.PR
Remove USB commom choke co-lay

A8ES.PR EMI

H5201 EMI_SPRING_PAD

USB_PN5 R5201 0Ohm USBP5-
USB_PP5 USBP5+
R5202 0Ohm
R5203 0Ohm
USB_PN7 USBP7-
USB_PP7 USBP7+
R5209 0Ohm

USB_PN1 R5211 0Ohm USBP1-
USB_PP1 USBP1+
R5212 0Ohm
R5213 0Ohm
USB_PN0 USBP0-
USB_PP0 USBP0+
R5218 0Ohm

USB_PN9 R5216 0Ohm USBP9-
USB_PP9 USBP9+
R5220 0Ohm
D5200 D5201 A8ES.PR
EGA10603V05A1 EGA10603V05A1

+5V +12V R5200 100KOHM Q5200 PMN45EN C5209 0.1UF/25V A8ES.ER
+5V_USB57 F5200 1.5A/6V +5VUSB_57 L5209 80Ohm/100Mhz +5VUSB57
C5200 10UF/10V CE5200 100U/6.3V C5201 0.1UF/16V C5202 0.1UF/16V
R5208 4.7KOhm @
USB_OC#57 R5210 8.2KOhm @

+5V +12V R5214 100KOHM Q5201 PMN45EN C5208 0.1UF/25V
+5V_USB01 F5201 1.5A/6V +5VUSB_01 L5204 80Ohm/100Mhz +5VUSB01
C5203 10UF/10V CE5201 100U/6.3V C5204 0.1UF/16V
R5215 4.7KOhm @
USB_OC#01 R5217 8.2KOhm @

+5V +12V R5219 100KOHM Q5202 PMN45EN C5207 0.1UF/25V
+5V_USB9 F5202 2.5A/6V +5VUSB_9 L5207 80Ohm/100Mhz +5VUSB9
C5205 10UF/10V CE5202 100U/6.3V C5206 0.1UF/16V
R5221 4.7KOhm R5222 8.2KOhm
USB_OC#9

USBCN2 +5VUSB57 USBP5- USBP5+ USB_CON_1X4P
USBCN1 +5VUSB57 USBP7- USBP7+ USB_CON_1X4P
USB-A
R5204 0Ohm @ R5205 0Ohm @ R5206 0Ohm @ R5207 0Ohm @
EMI
H5200 EMI_SPRING_PAD @
USB-B

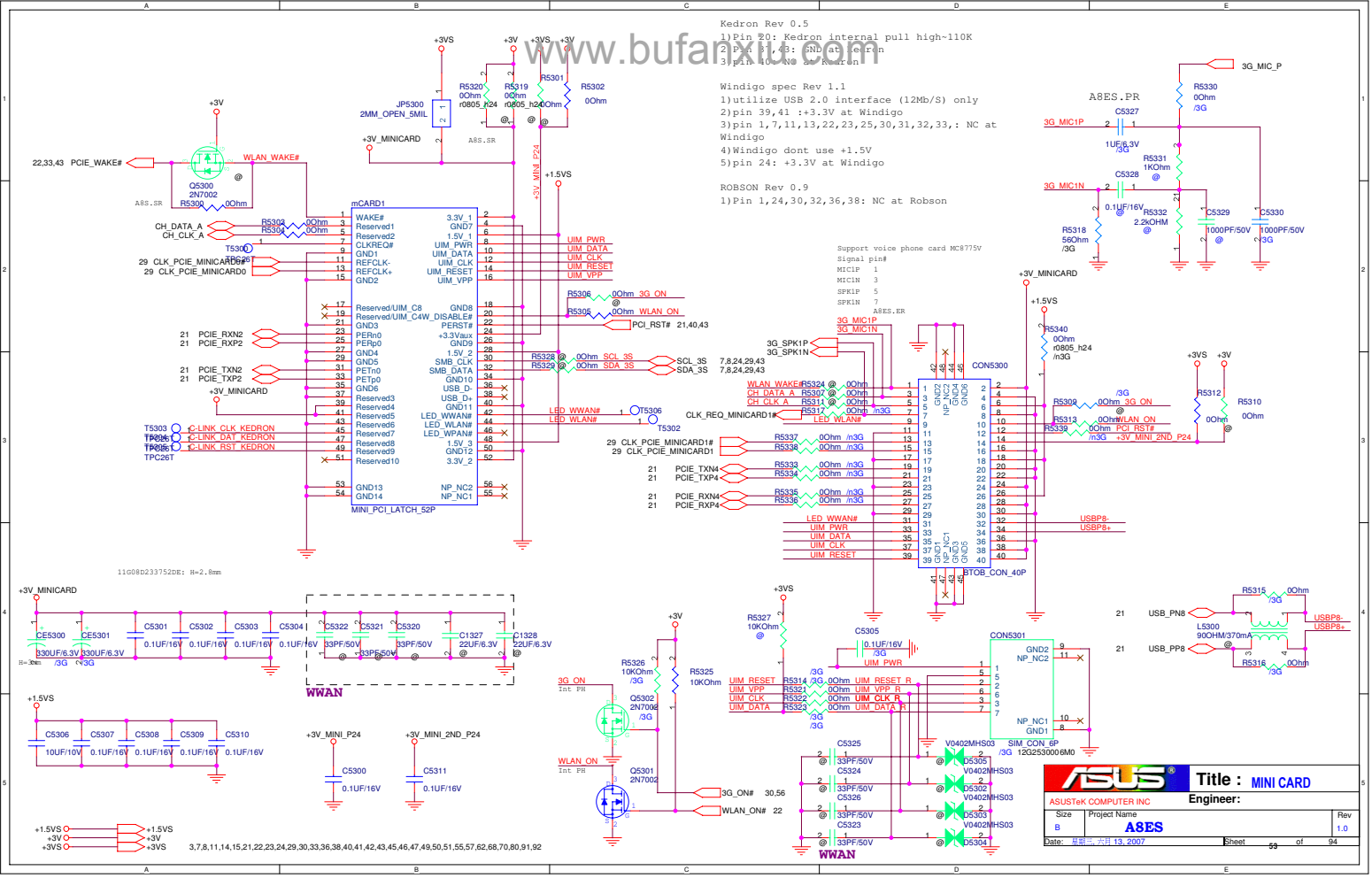
USBDUCN1 GND4 GND6 GND2 0P+ 0P- VCC2 GND1 1P+ 1P- VCC1 GND3 GND5
USBP1+ USBP1- +5VUSB01 USBP0+ USBP0- +5VUSB01
USB_CON_2X4P
USB-UP
USB-DOWN

+5V +5V 9,43,57,68,70,91

SUB-PCB: USB/1394/MIC/EARPHONE

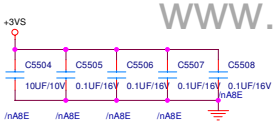
USB-C
CON5200 HEADER_2X10P
USBP9- USBP9+ +5VUSB9
TPA0-_1 TPA0+_1 TPB0-_1 TPB0+_1 MIC_IN#_JACK
EXT_MIC_JACK INT_MIC_JACK 37 OPTIC_VCC_JACK 38 SPDIF_O_JACK JACK_SW# 38 HP_JACK_L 38 HP_JACK_R HP_JD
L5209 80Ohm/100Mhz

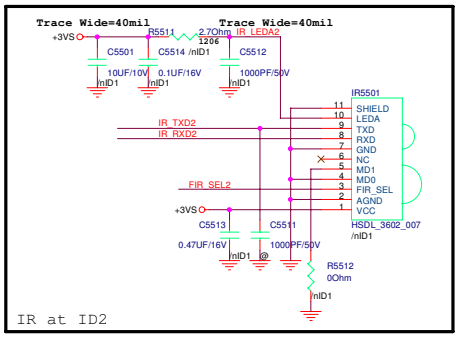
<Variant Name>
Title : USB/SUB PCB
ASUSTeK COMPUTER INC
Engineer:
Size: Custom | Project Name: A8ES | Rev: 1.0
Date: 星期一, 六月 06, 2007 | Sheet 52 of 94



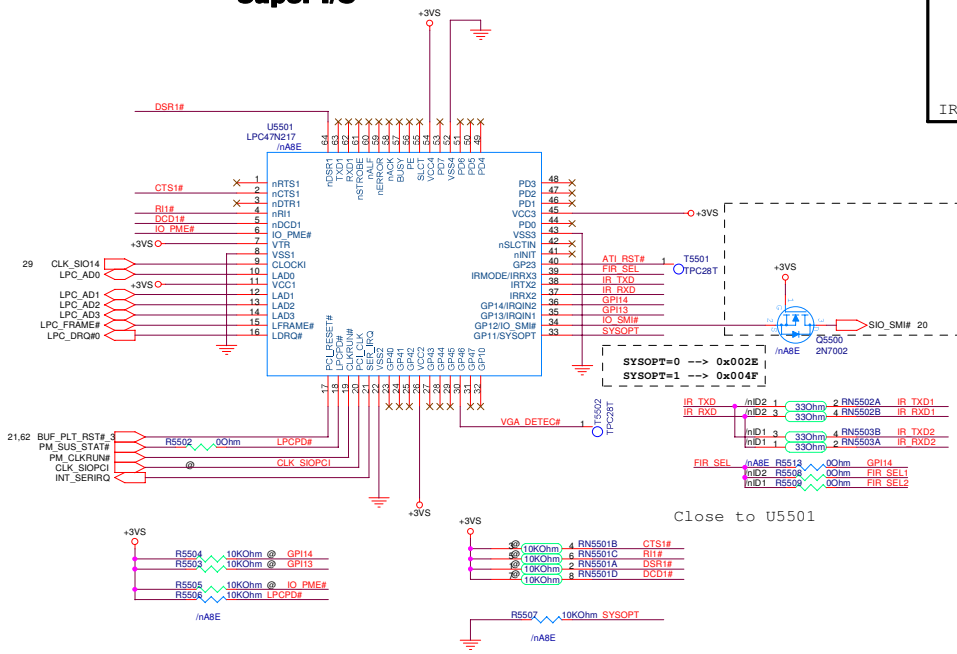
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: Custom	Project Name: A8ES	Rev: 0
Date: 星期二, 十月 11, 2006	Sheet 54 of 94	

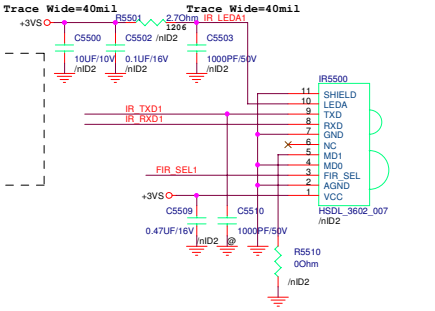
CIR
04G231020500
TSOP6238TR





Super I/O





Close to U5501

Transceiver Control Truth Table

Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
1	0	X	Shutdown	Shutdown
0	0	0	SIR	Full Distance Power
0	1	0	SIR	2/3 Distance Power
1	1	0	SIR	1/3 Distance Power
0	0	1	MIR/FIR	Full Distance Power
0	1	1	MIR/FIR	2/3 Distance Power
1	1	1	MIR/FIR	1/3 Distance Power

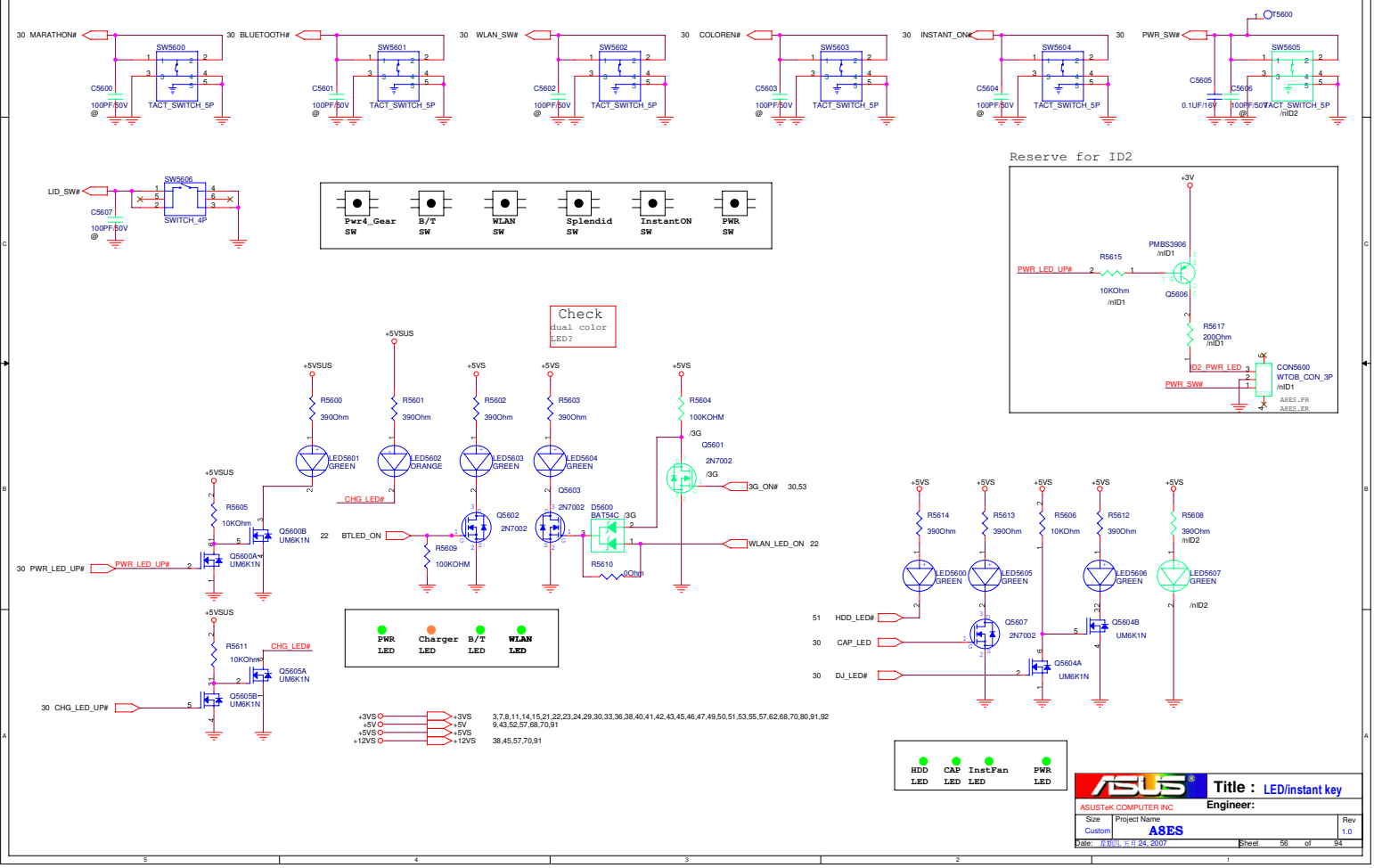
ASUSTeK COMPUTER INC

Title : IrDA

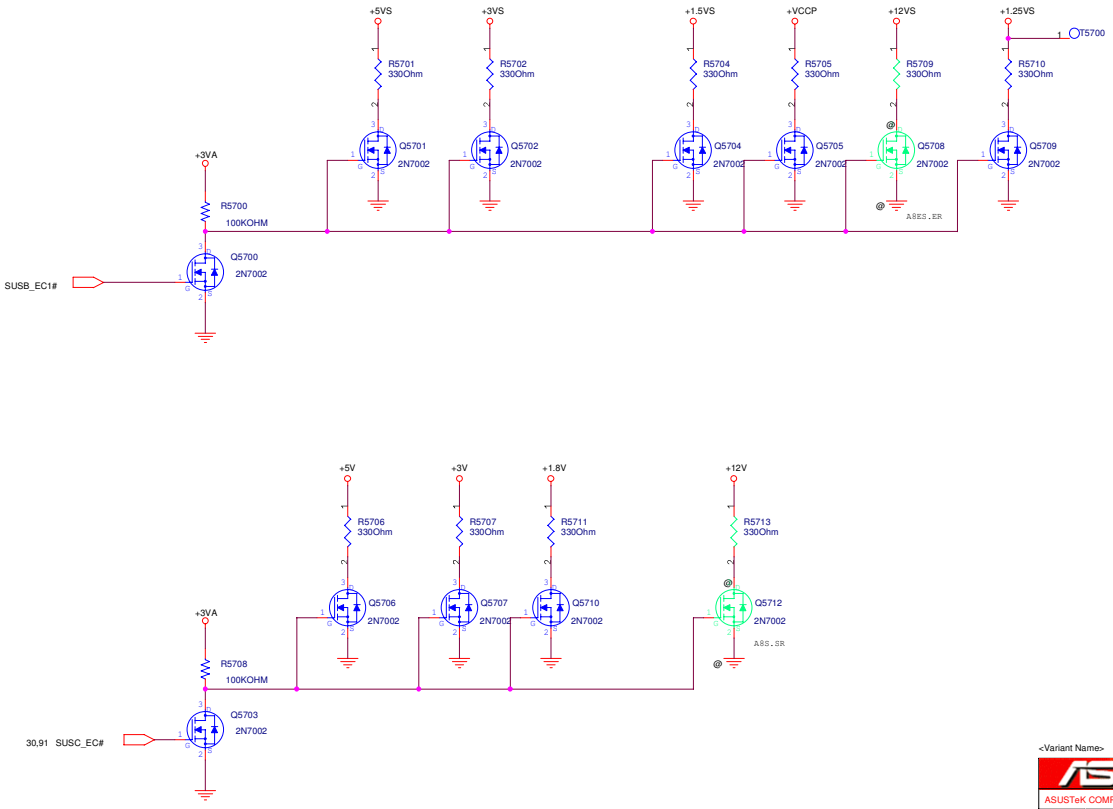
Engineer:

Size	Project Name	Rev
B	A8ES	2.0

Date: 星期二, 二月 06, 2007 Sheet 55 of 94



Discharge Circuit



<Variant Name>

ASUSTeK COMPUTER INC

Title : Discharge

Engineer:

Size	Project Name	Rev
B	A8ES	1.0

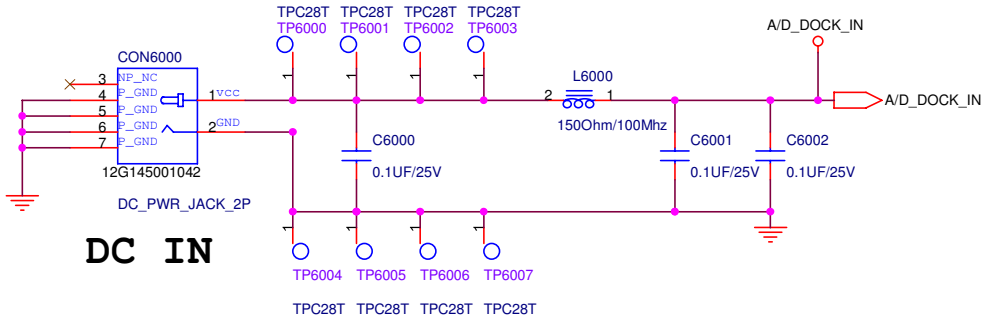
Date: 星期 . 月 06, 2007 Sheet 57 of 94

<< Kennedy_Zhang >>

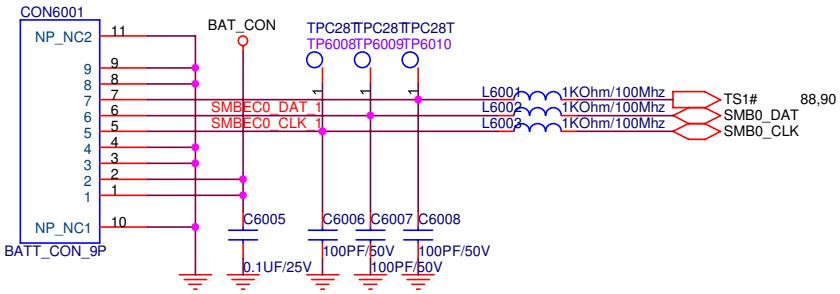
<Variant Name>

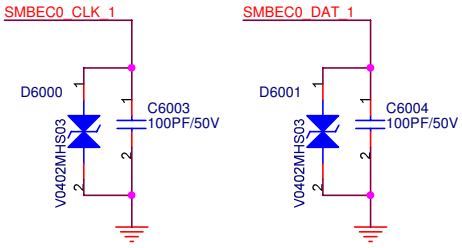
ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 1.0
Date: 星期三, 十月 11, 2006	Sheet of 94	

Title	<Title>	
Size A	Document Number W2S	Rev 1.1
Date: 星期三, 十月 11, 2006	Sheet 59 of 94	



DC IN

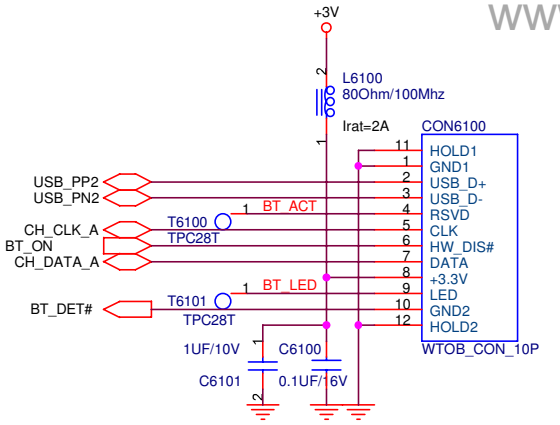




Battery Connector

<Variant Name>

ASUSTeK COMPUTER INC	Title : DC IN / BAT	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 1.0
Date: 星期四, 五月 24, 2007	Sheet 60 of 94	



Bluetooth Module CON

ASUSTeK COMPUTER INC

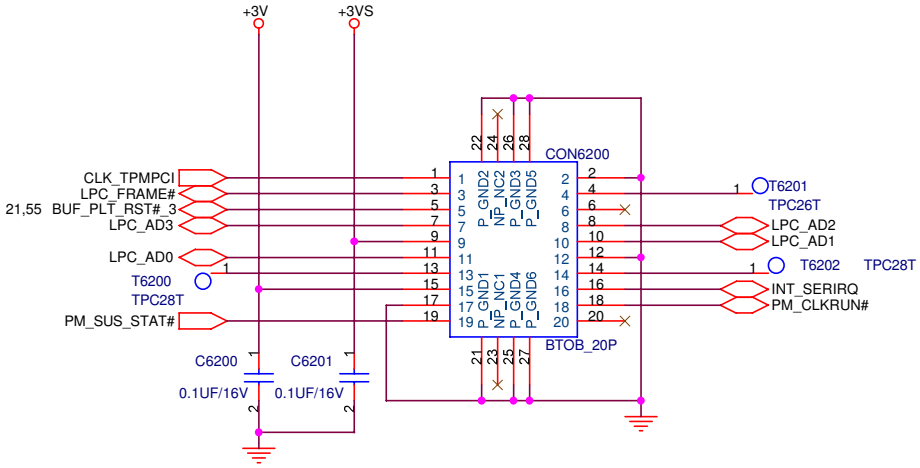
Title : BT/CAMERA

Engineer:

Size	Project Name	Rev
A	A8ES	1.0

Date: 星期二, 二月 06, 2007 Sheet 61 of 94

TPM 1.2 Module



<Variant Name>

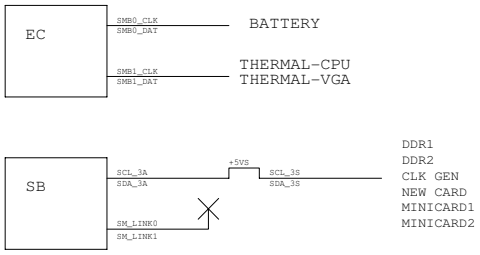
ASUSTeK COMPUTER INC	Title : TPM	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 1.0
Date: 星期二, 二月 06, 2007	Sheet 62 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 63 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



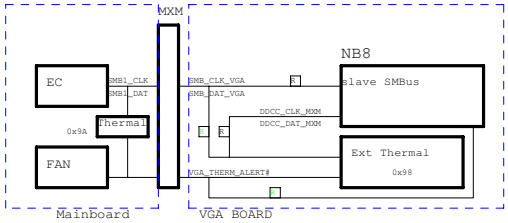
BOM option

```
nGM:yellow
nPM:light red
=========================
@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debuging A8S in advance
3G :for Windigo,SIERRA MC8775V
nA8E  :no stuff Irda for A8E
```

Support ID2:

```
Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED
```

Thermal block diagram



<Variant Name>

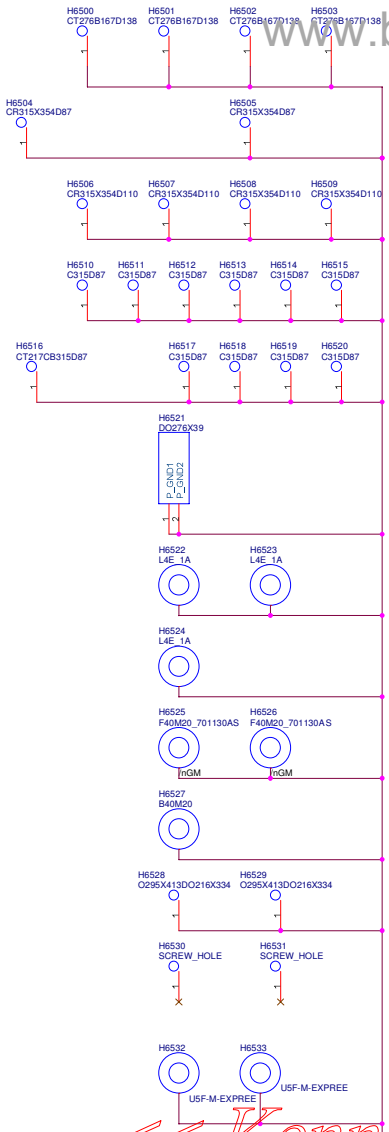
ASUSTeK COMPUTER INC

Title :

Engineer:

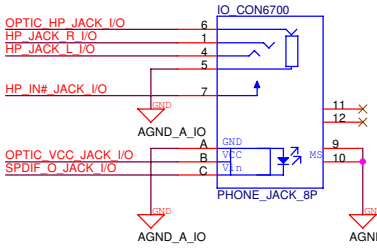
Size	Project Name	Rev
B	A8ES	1.0

Date: 星期 一, 月 06, 2007 Sheet 64 of 94

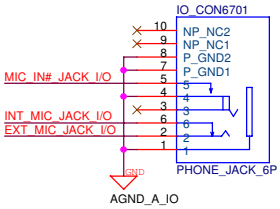


Title	<Title>	
Size	Document Number	Rev
CustomW2S		1.1
Date:	日 26, 2006	Sheet 65 of 94

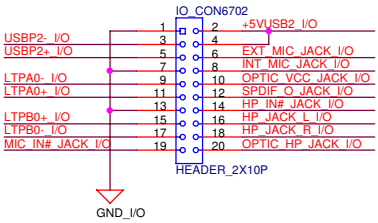
ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: B	Project Name: A8ES	Rev: 0
Date: 星期一, 1月 11, 2006	Sheet 66 of 94	

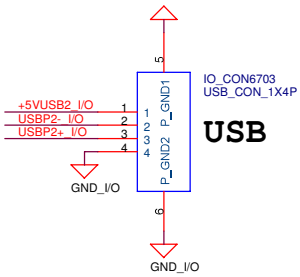


LINE_OUT SPDIF



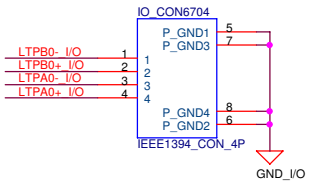
MIC

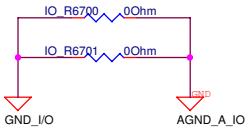


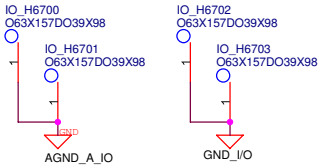


USB

1394A







<Variant Name>

ASUSTeK COMPUTER INC

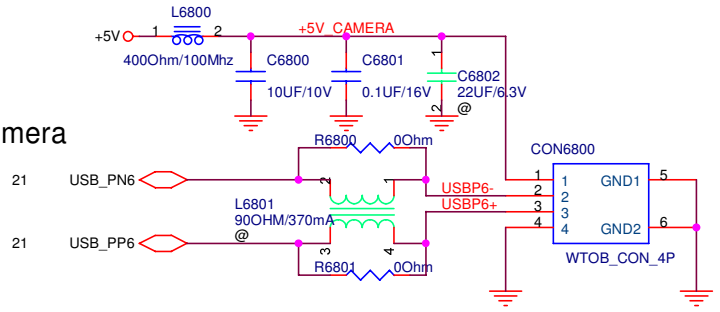
Title : SUB_PCB

Engineer:

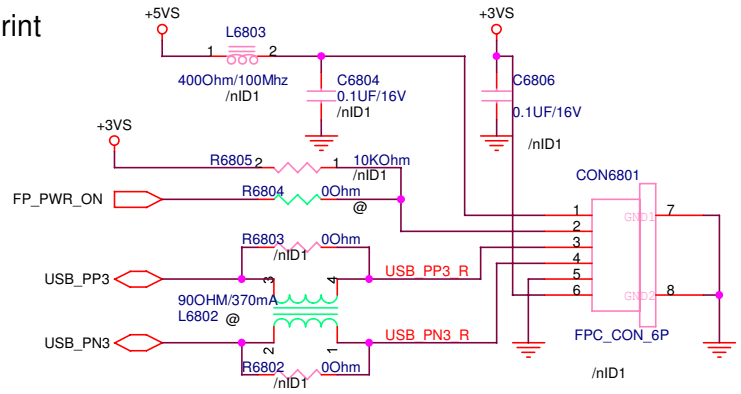
Size	Project Name	Rev
A4	A8ES	1.0

Date: 星期二, 一月 30, 2007 Sheet 67 of 94

Camera



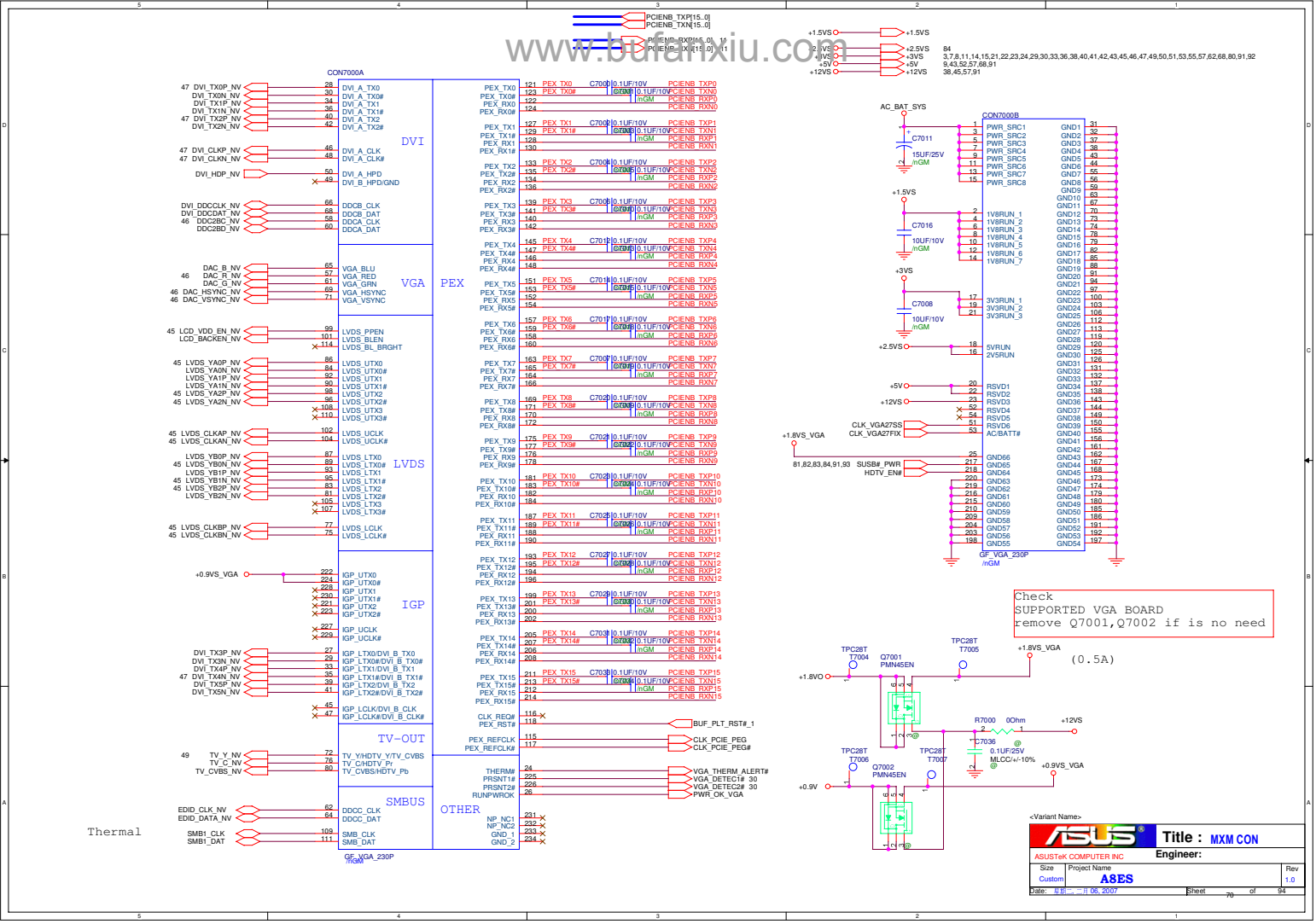
Finger Print



<Variant Name>

ASUSTeK COMPUTER INC	Title : CAMERA/FingerPrinter	
	Engineer:	
Size: A	Project Name: A8ES	Rev: 1.0
Date: 星期三, 六月 13, 2007	Sheet 68 of 94	

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: A	Project Name: A8ES	Rev: 0
Date: 星期三, 十月 11, 2006	Sheet 69 of 94	



Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 71 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 72 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 73 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 74 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 75 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 十月 11, 2006		Sheet 76 of 94		

Title	TITLE			
Size A3	Document Number <Doc>			Rev 1.0
Date: 星期一, 一月 11, 2006		Sheet 77 of 94		

ASUSTeK COMPUTER INC	Title : BLANK Engineer:	
Size: B	Project Name: A8ES	Rev: 0
Date: 星期一, 十月 11, 2006	Sheet 78 of 94	

W2S

Change Note:

EE :

1. 965PM pin defined modification, C48/D47/BJ29/BE24 from RSVD pin to LVDSA_DATA#_3 / LVDSA_DATA_3 / SA_MA_14 / SB_MA_14
2. CE46 / CE25 --> 11G08D210791
3. Rst button circuit
4. BT_SW pull-high to different plane issue.
5. Remove RN3104
6. VTT_REF reserve in S3.
7. VTT stop in S3.
8. CIR PME# function.

Layout :

1. CPU side, per GND pin within per Via, don't share vias.
2. 0.9V_VTT_REF trace width.
3. single end trace width more than 3.5mil

SMT :

1. 開鋼板JP1, JP2

<Variant Name>

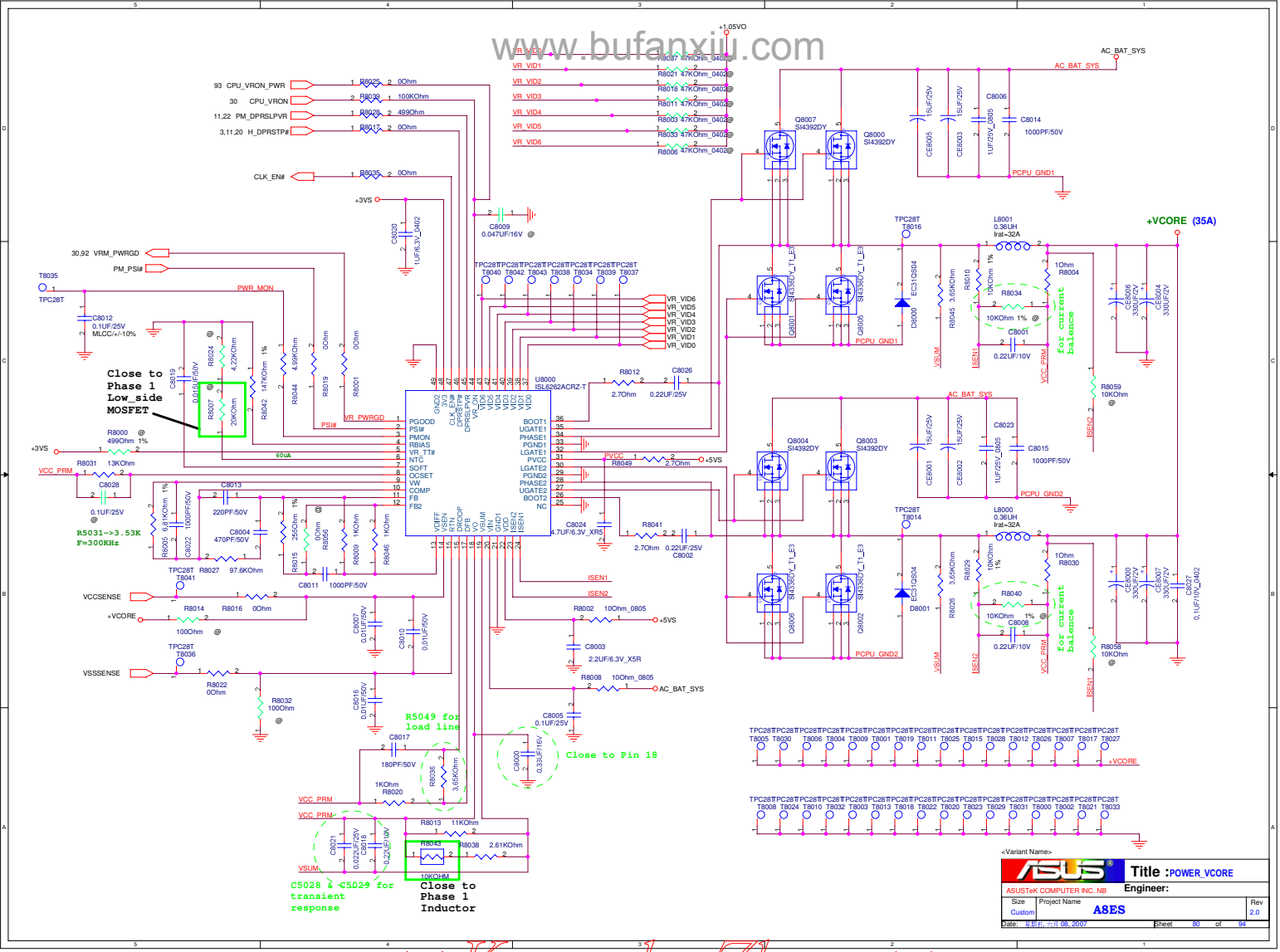
ASUSTeK COMPUTER INC

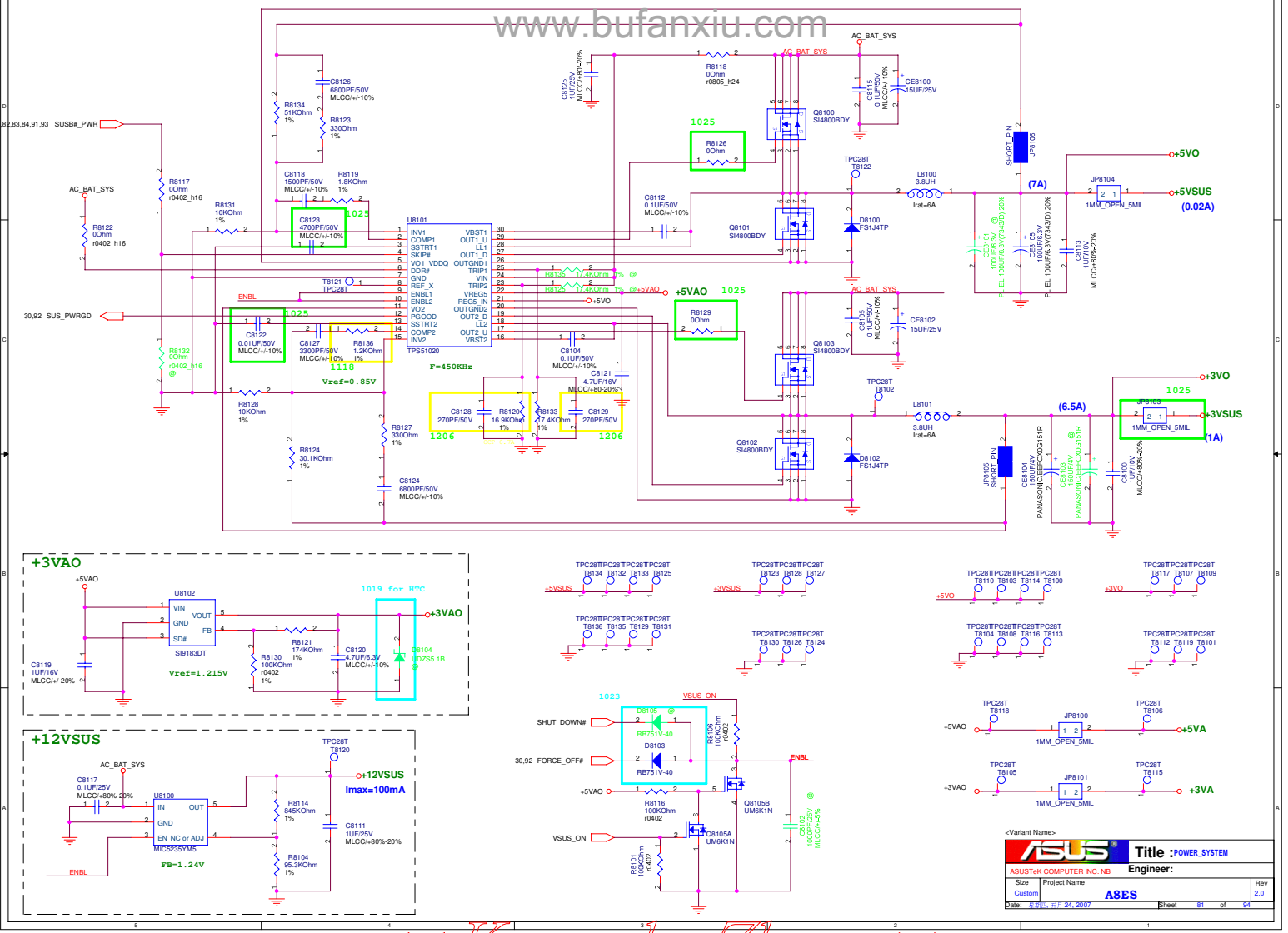
Title : History

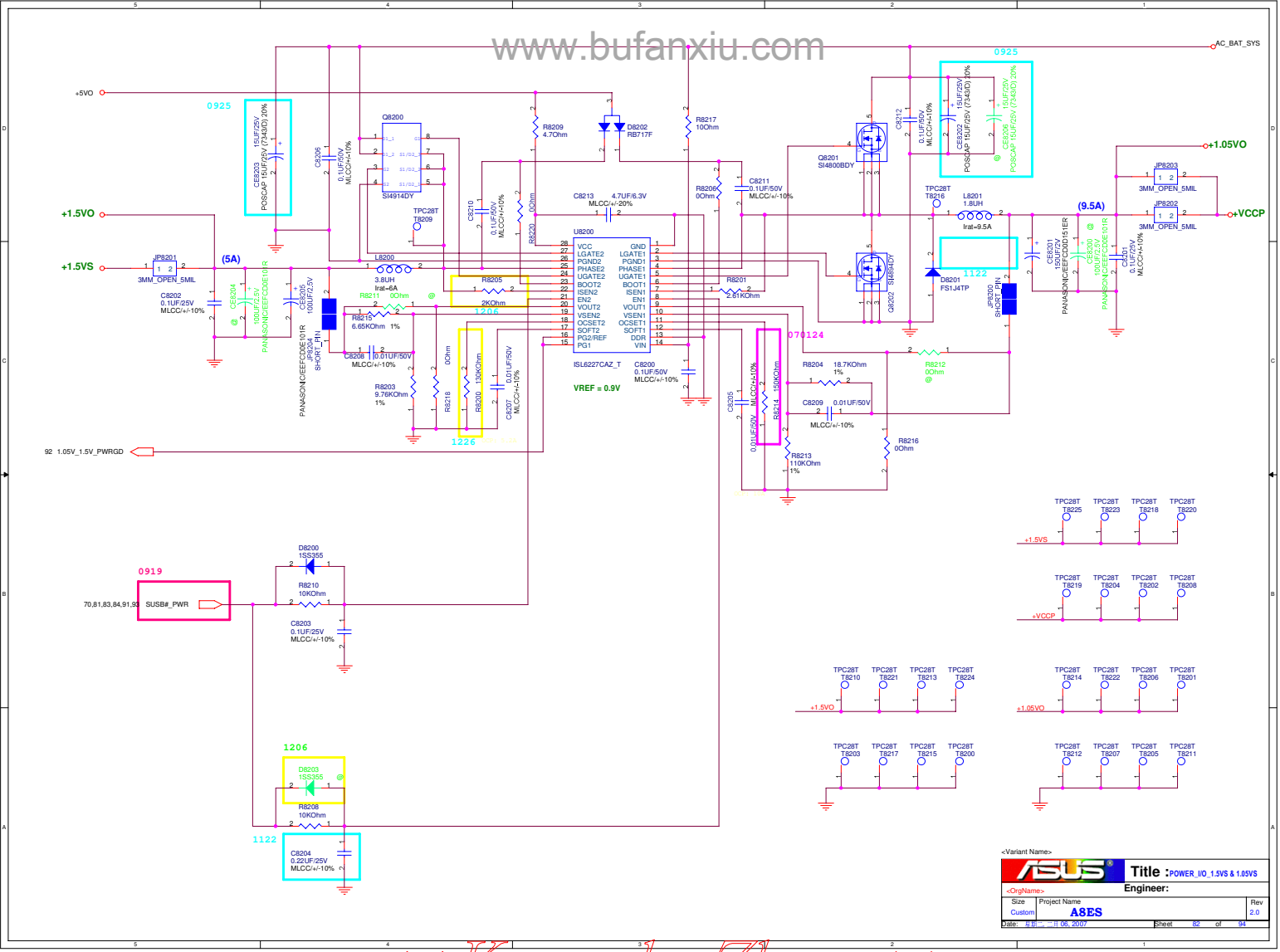
Engineer:

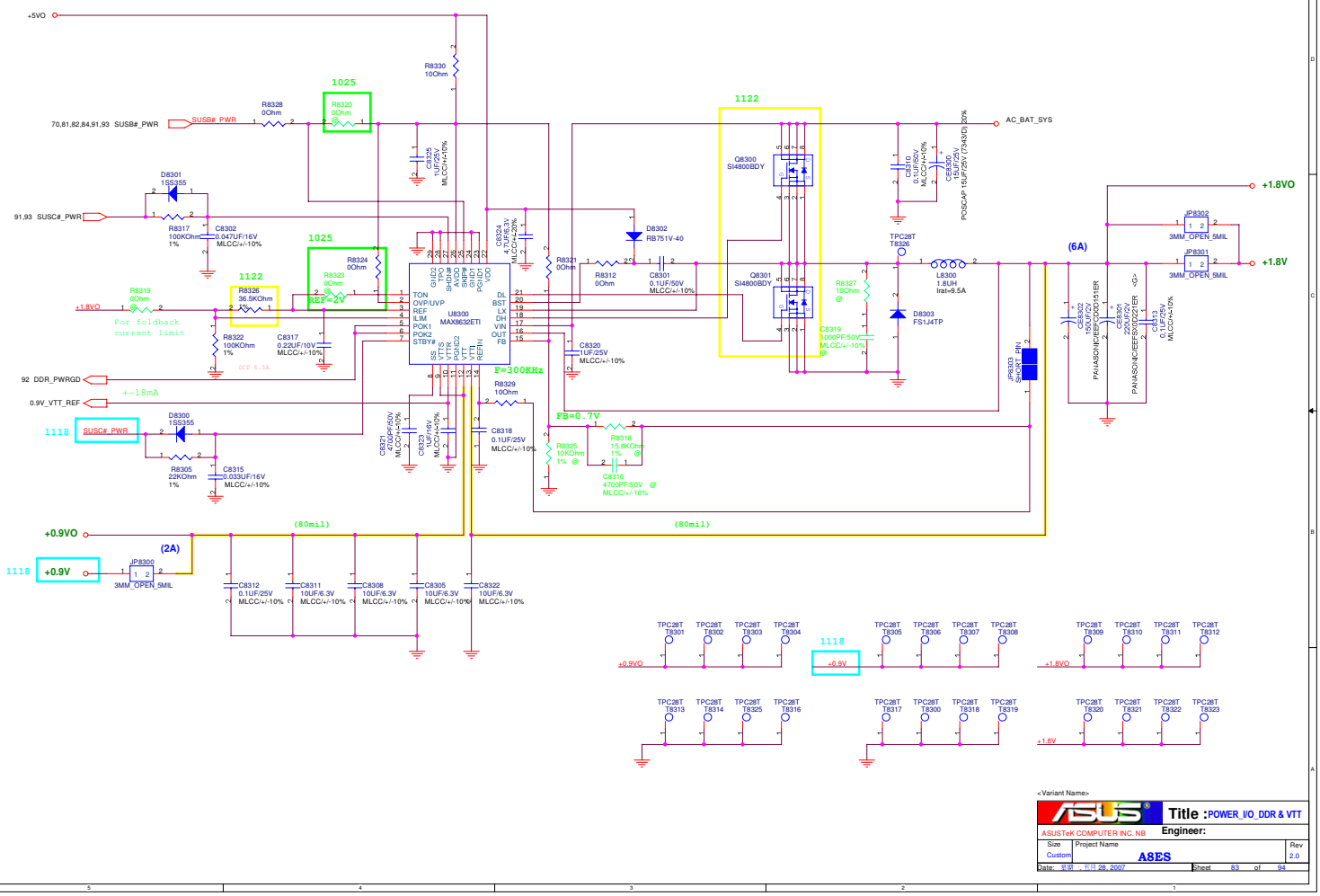
Size	Project Name	Rev
Custom	A8ES	1.0

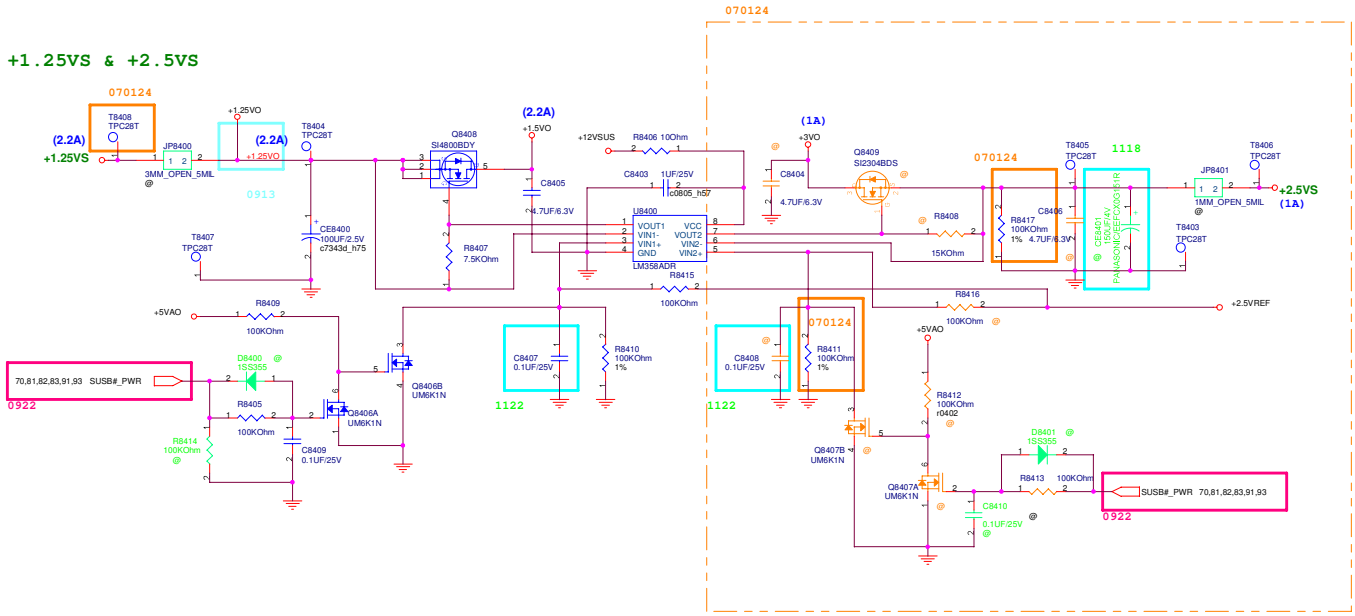
Date: 星期二, 十月 11, 2006 Sheet 79 of 94











<Variant Name>

Title : POWER_I/O_+3VA & +2.5V

<OrgName> Engineer:

Size	Project Name	Rev
Custom	A8ES	2.0

Date: 星期一, 二月 06, 2007 Sheet 84 of 94

<Variant Name>

Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
C	ROSA	1.1

Date: 日 四月 一日 25, 2007 Sheet 85 of 94

<Variant Name>

Title : N/A

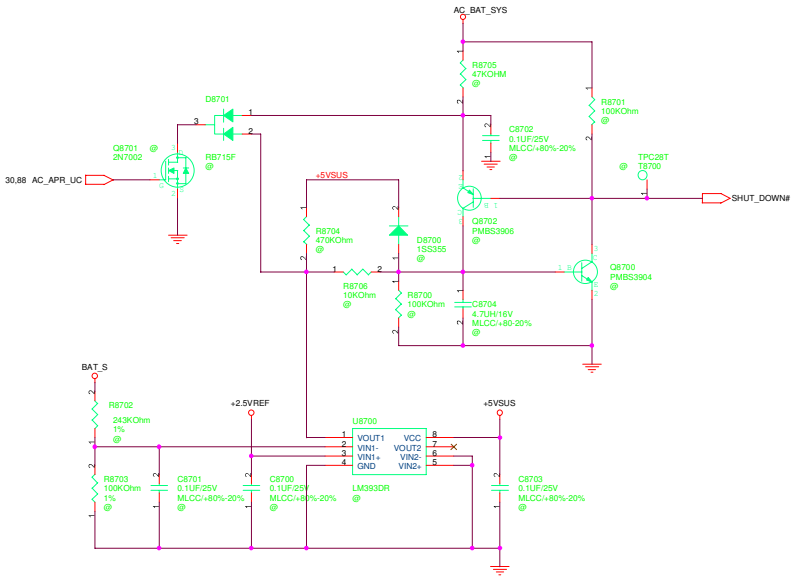
<OrgName>

Engineer:

Size	Project Name	Rev
B	ROSA	1.1

Date: 財四月, 月 25, 2007 Sheet 86 of 94

PIC only



<Variant Name>

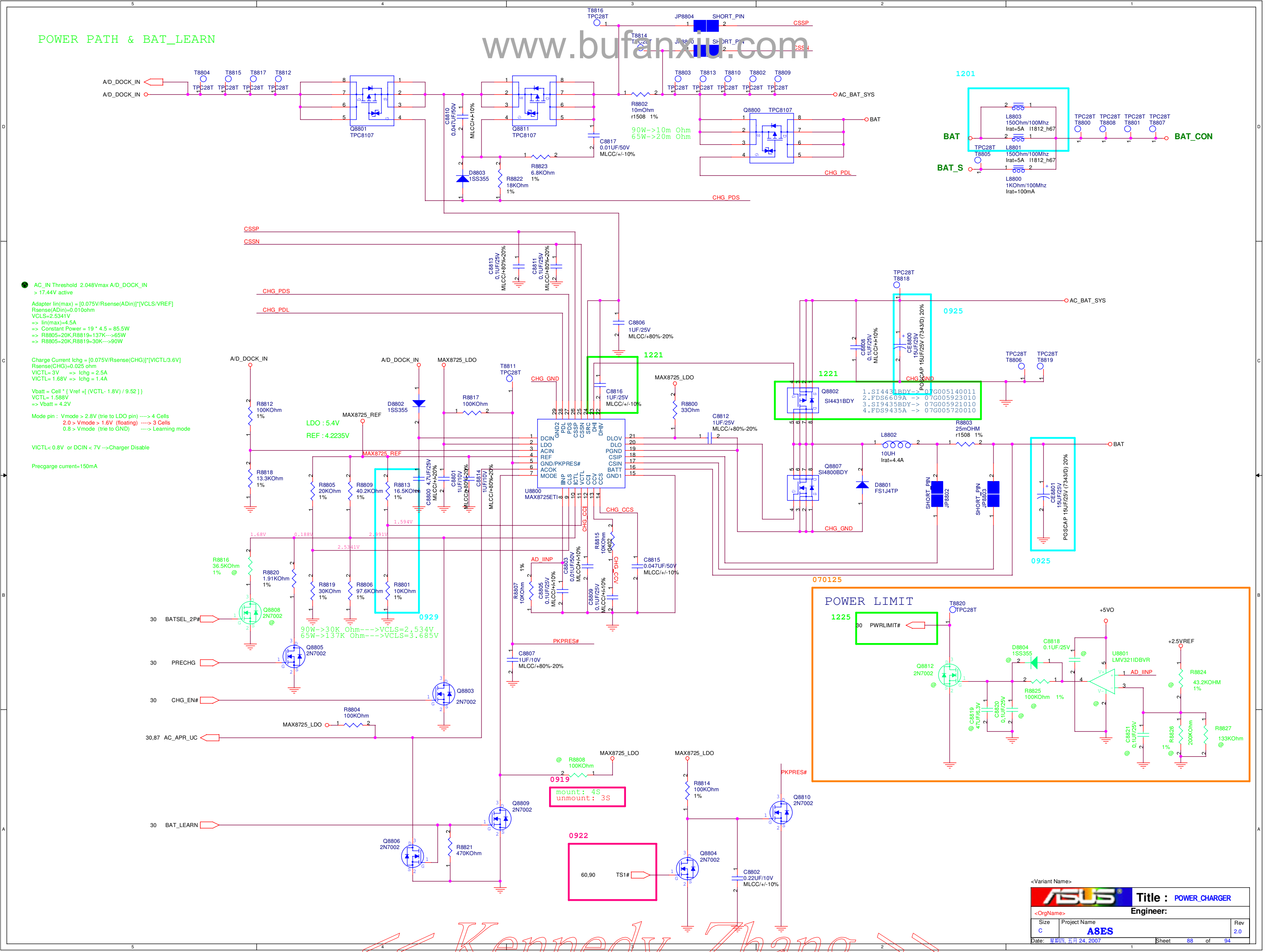
Title : POWER_SHUTDOWN#

<OrgName> Engineer:

Size	Project Name	Rev
Custom	A8ES	2.0

Date: 日期二, 一月 06, 2007 Sheet 87 of 94

POWER PATH & BAT_LEARN



Title : POWER_CHARGER

Engineer:

Size C | Project Name A8ES | Rev 2.0

Date: 星期四, 五月 24, 2007 | Sheet 88 of 94

<Variant Name>

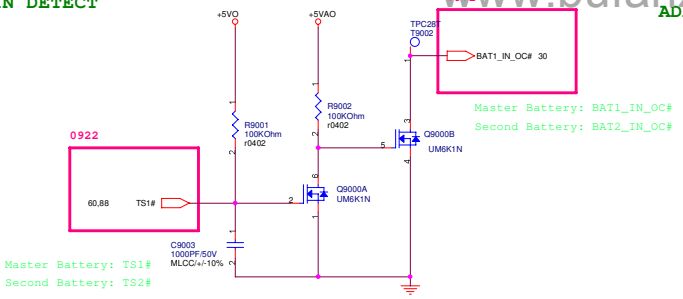
Title : N/A

<OrgName> Engineer:

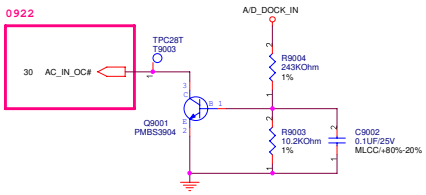
Size	Project Name	Rev
Custom	ROSA	1.1

Date: 星期四, 一月 25, 2007 Sheet 89 of 94

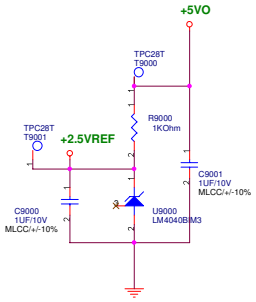
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF

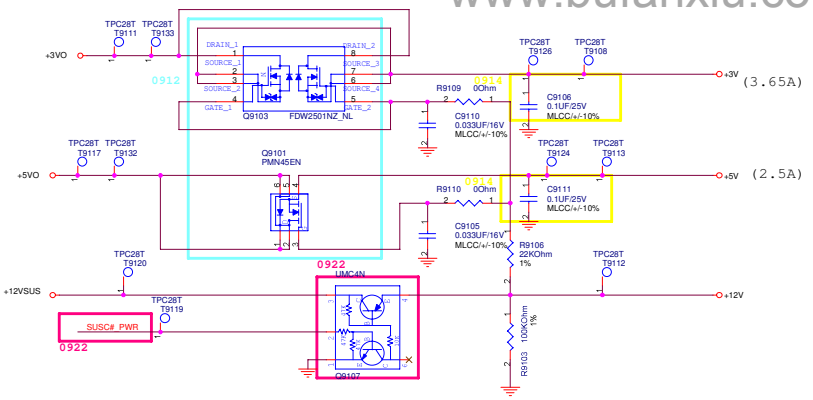


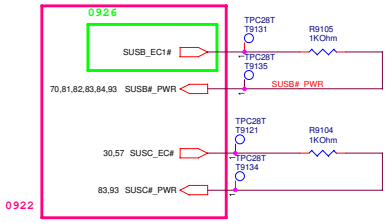
<Variant Name>

<OrgName>	Title : POWER_DETECT	
	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 2.0
Date: 星期四, 十月 24, 2007	Sheet 90 of 94	

SUSC#_PWR POWER

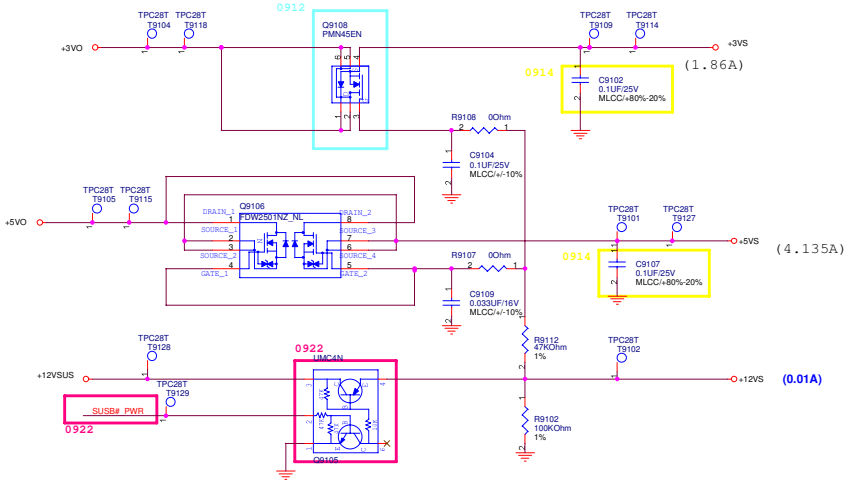
0922





SUSB#_PWR POWER

0922



<Variant Name>

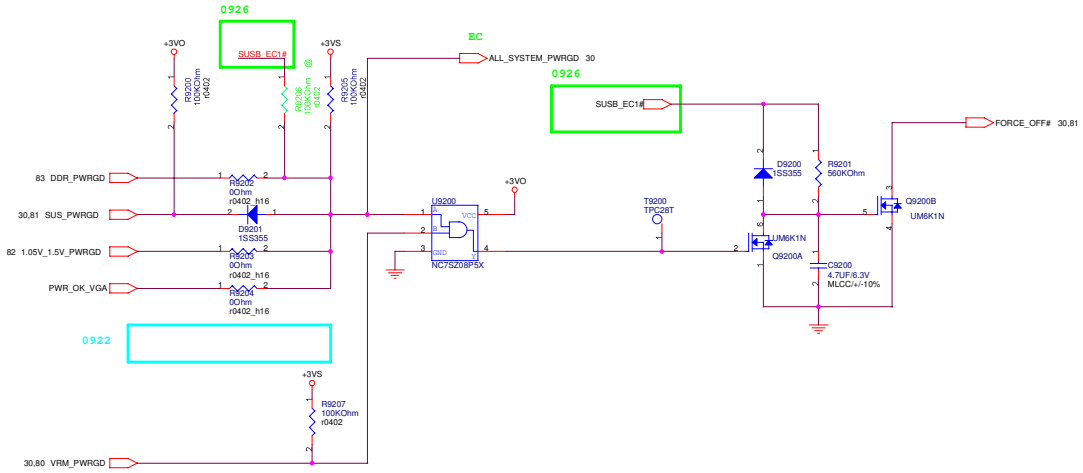
Title : POWER_LOAD SWITCH

<OrgName> Engineer:

Size	Project Name	Rev
Custom	A8ES	2.0

Date: 星期五, 十月 26, 2007 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: A8ES	Rev: 2.0
Date: 日期二, 一月 06, 2007	Sheet 92 of 94	

AC_BAT_SYS → AC_BAT_SYS 45,70,80,81,82,83,87,88
BAT → BAT 88
BAT_CON → BAT_CON
+2.5VREF → +2.5VREF 84,87,88,90
+3VA → +3VA
0922 +5VAO → +5VAO 81,84,90
+5VO → +5VO 81,82,83,88,90,91
+5VSUS → +5VSUS 23,56,81,87
+5V → +5V 9,43,52,57,68,70,91
+5VS → +5VS
+3VO → +3VO 81,84,91,92
+3VSUS → +3VSUS
+3V → +3V
+3VS → +3VS 3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,51,53,55,57,62,68,70,80,91,92

+12VSUS → +12VSUS 81,84,91
+12V → +12V
+12VS → +12VS 38,45,57,70,91

+1.8VO → +1.8VO
+1.8V → +1.8V
+1.8VS → +1.8VS
+0.9VS → +0.9VS
0922 +0.9VO → +0.9VO 83

0922 +1.05VO → +1.05VO 80,82
+VCCP → +VCCP
0922 +1.5VO → +1.5VO 82,84
+1.5VS → +1.5VS

+2.5VO → +2.5VO
+2.5VS → +2.5VS 70,84

+VCORE → +VCORE

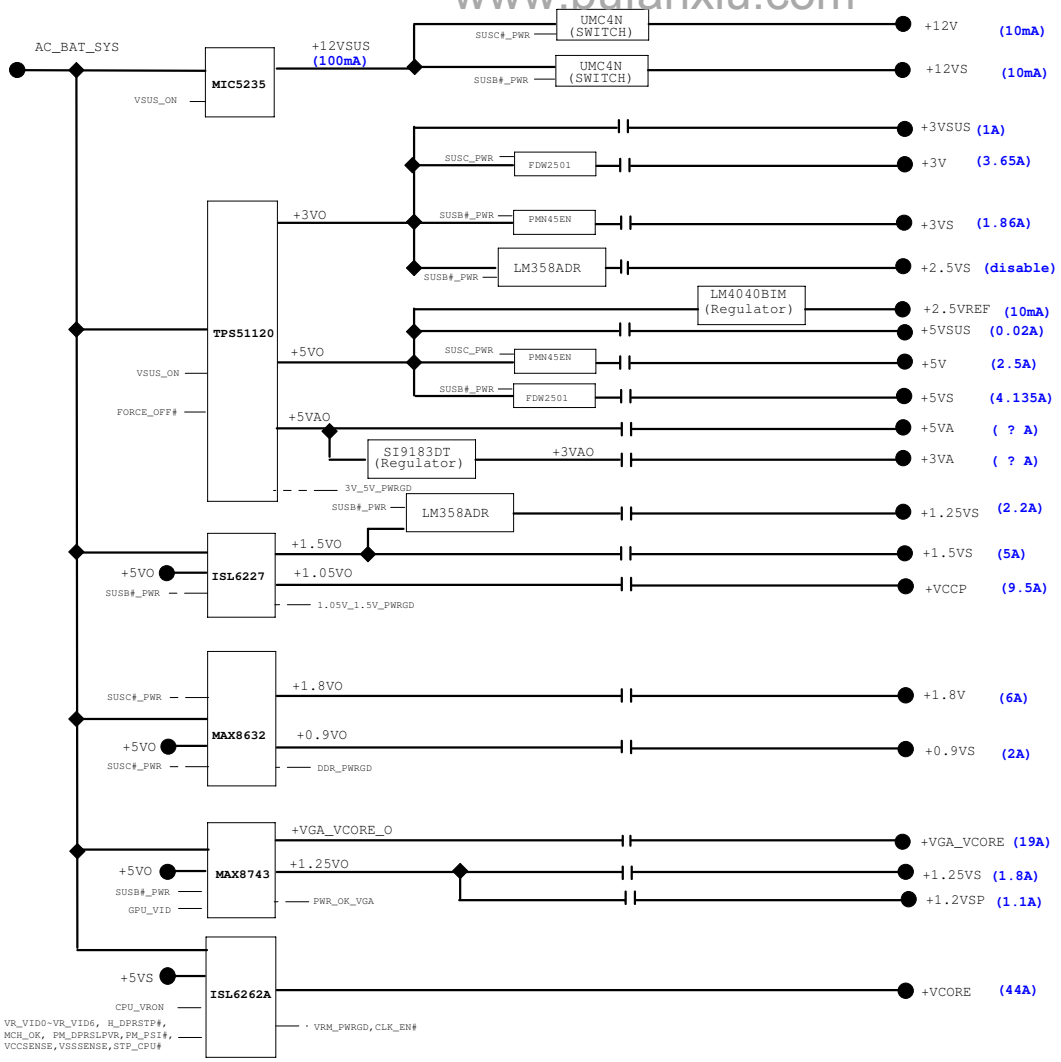
+VRAM → +VRAM
+1.2VSP → +1.2VSP
+1.25VS → +1.25VS

FOR POWER TEST

+3VA
JP9300 SGL_JUMP → CPU_VRON_PWR 80
0922
JP9301 SGL_JUMP → SUSB#_PWR → SUSB#_PWR 70,81,82,83,84,91
JP9302 SGL_JUMP → SUSC#_PWR → SUSC#_PWR 83,91
JP9303 SGL_JUMP → VSUS_ON → VSUS_ON

<Variant Name>

<OrgName>	Title : POWER_SIGNAL	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: A8ES	Rev: 2.0
Date: 星期四, 十月 24, 2007	Sheet 93 of 94	



<Variant Name>

Title : POWER_VCORE

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	A8ES	2.0

Date: 日 四月 25, 2007 Sheet 94 of 94