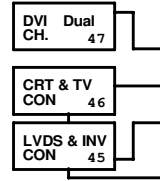
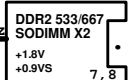
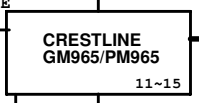
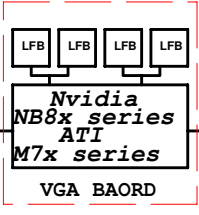
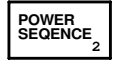
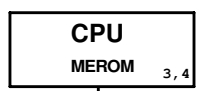
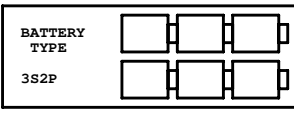
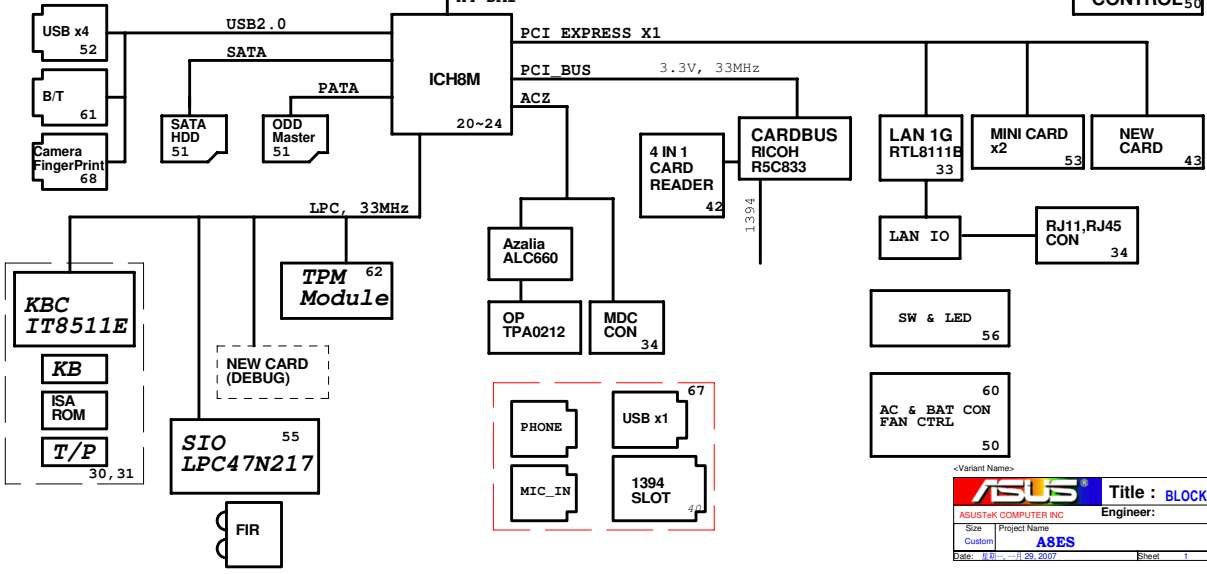


# A8E/A8S Merom/GM965/PM965 BLOCK DIAGRAM

Sub block Diagram / BOM option 64

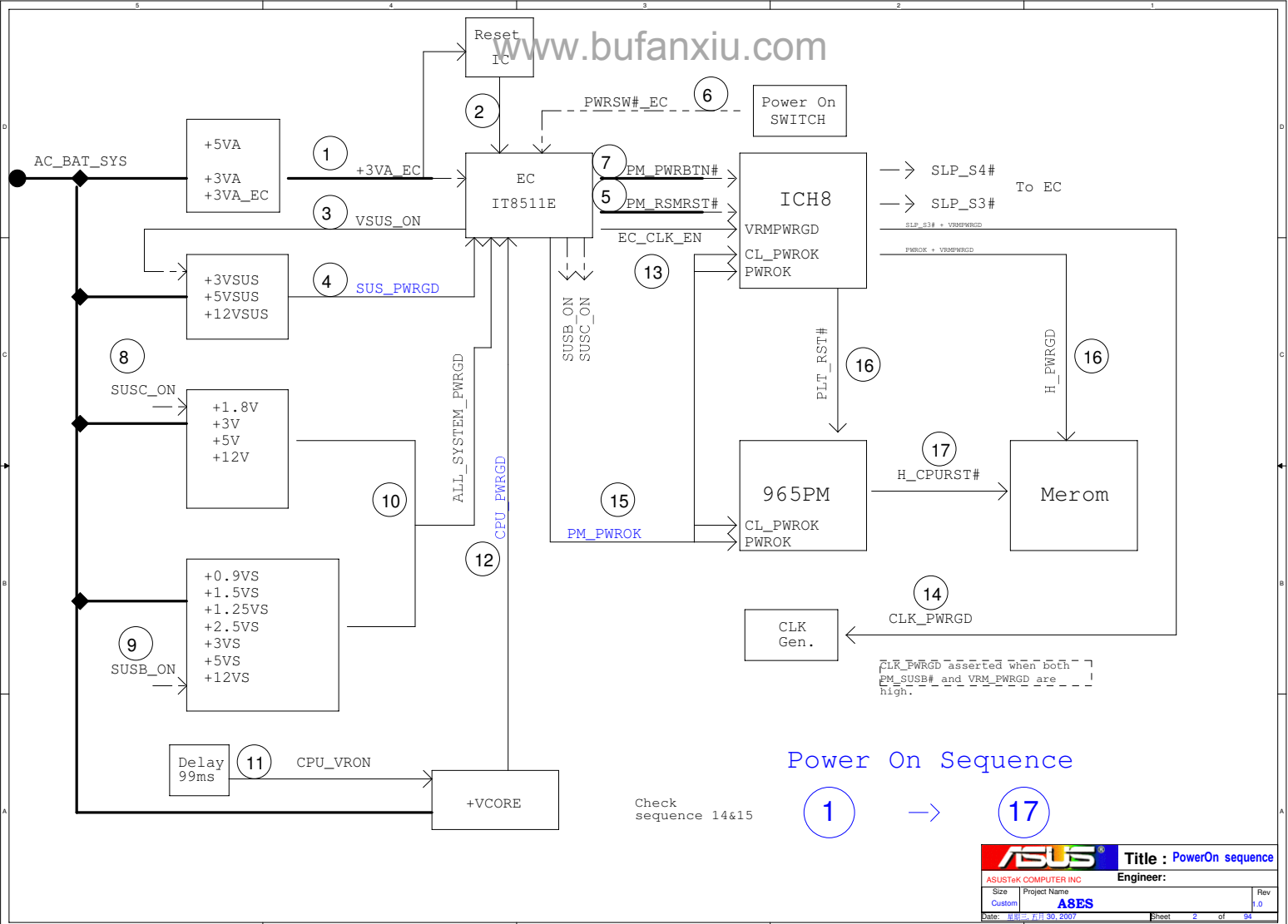


VCORE
SYSTEM
1.5VS & 1.05VS
DDR & VTT
+3VAO & +2.5VS
CHARGER
PIC
DETECT
PROTECT
LOAD SWITCH
FLOWCHART
SIGNAL

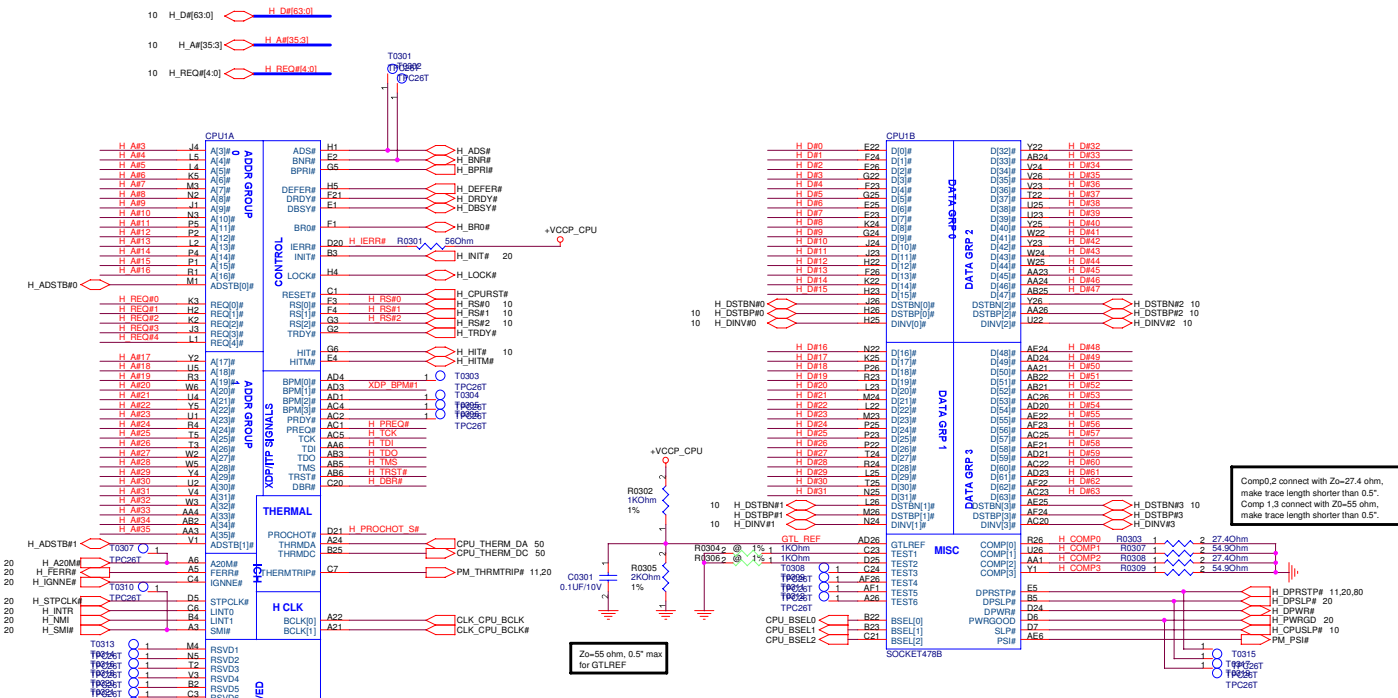


ASUS Title: BLOCKDIAGRAM  
 ASUSTeK COMPUTER INC. Engineer:  
 Size: Custom Project Name: A8ES Rev: 2.0  
 Date: 11/11/07 11:29:2007 Sheet 1 of 94

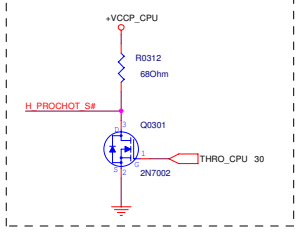
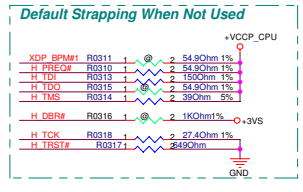
<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>



Comp0.2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".  
 Comp 1.3 connect with Zo=55 ohm, make trace length shorter than 0.5".



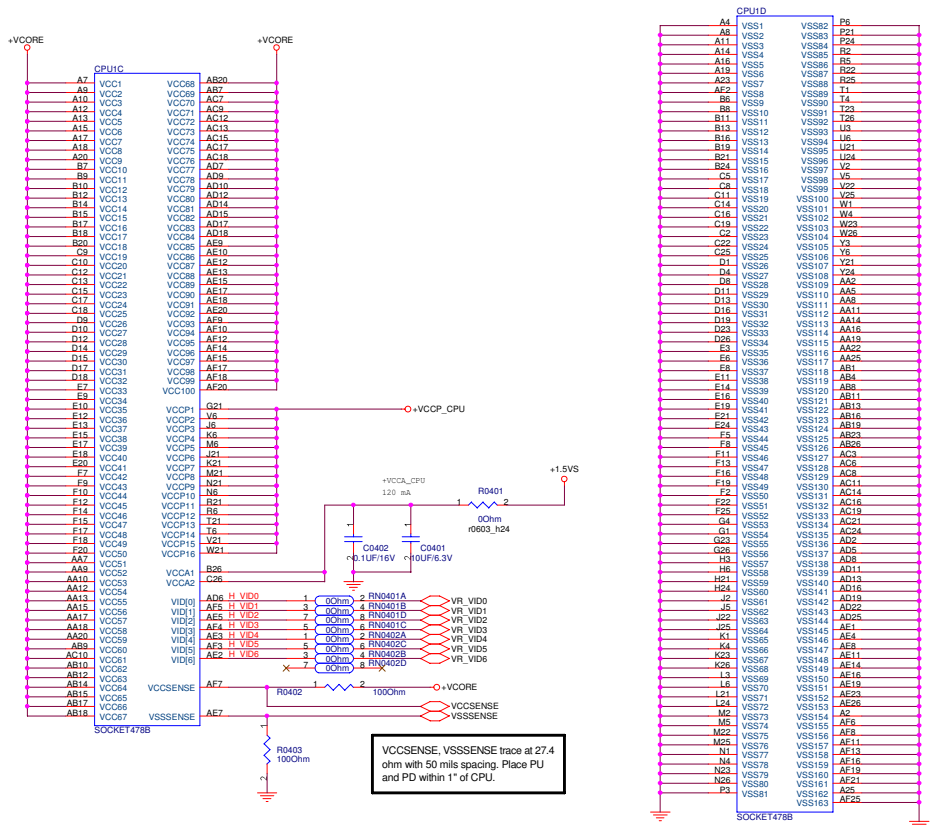
**ASUS** Title: **MEROM CPU (1)**

ASUSTeK COMPUTER INC. Engineer:

Size	Project Name	Rev
Custom	<b>A8ES</b>	1.0

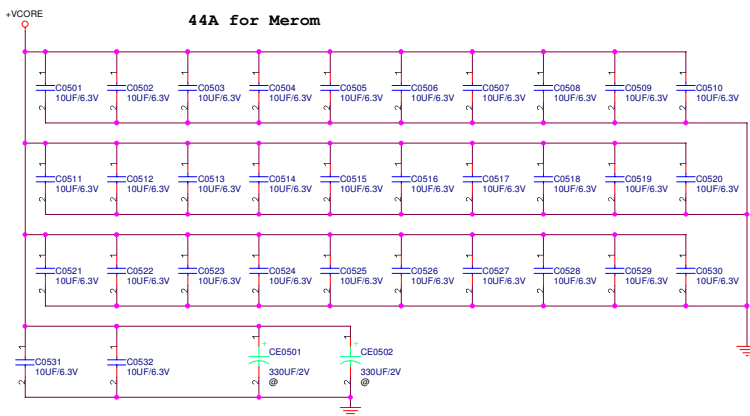
Date: 星期三, 五月 08, 2007 Sheet 3 of 94

<< Kennedy\_Zhang >>



		<b>Title : MEROM CPU (2)</b>	
ASUSTeK COMPUTER INC.		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>A8ES</b>	1.0	
Date: 星期日, 6月08, 2007	Sheet 4 of 94		

<< Kennedy\_Zhang >>

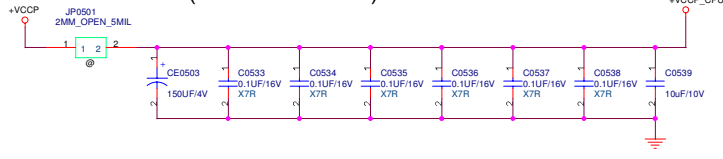


Decoupling guide from INTEL

- VCORE 22uF/10V \* 32pcs
- 330uF/2V \* 6pcs
- VCCP 0.1uF \* 6pcs for CPU
- 150uF \* 1pcs for CPU


- VCORE 10uF/10V \* 32pcs
- 330uF/2V \* 0pcs
- VCCP 0.1uF \* 6pcs for CPU
- 150uF/10V \* 1pcs

+VCCP Decoupling Capacitor (Place near CPU)

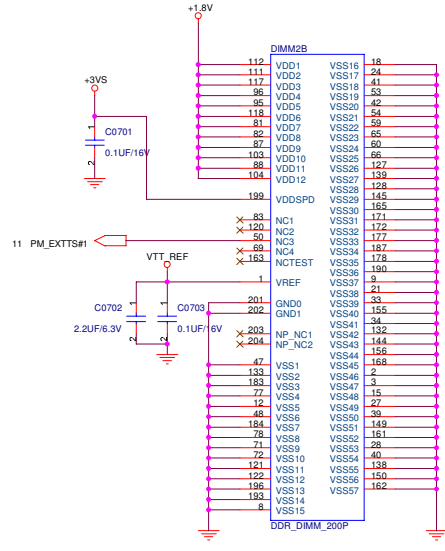
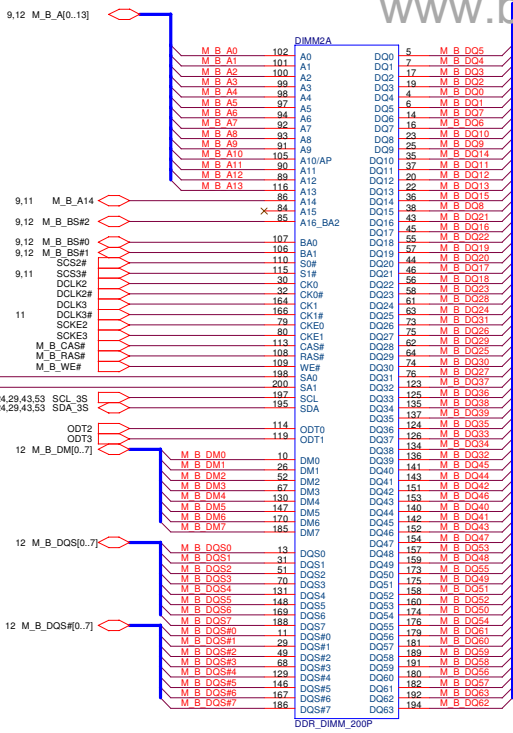


<b>ASUS</b>		<b>Title :CPU CAP</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8ES	1.0	
Date: 11/13/2006	Sheet 5 of 94		

<< Kennedy\_Zhang >>

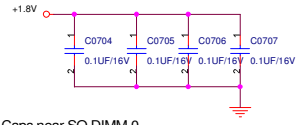
		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 6 of 94

<< Kennedy\_Zhang >>

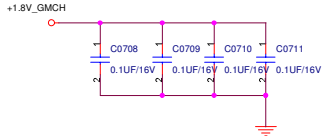


Higher slot: SPD/TS=A4/34

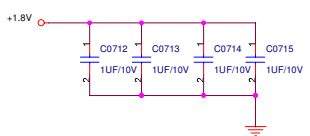
Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these Caps near SO DIMM 0



**Upper:Channel B**

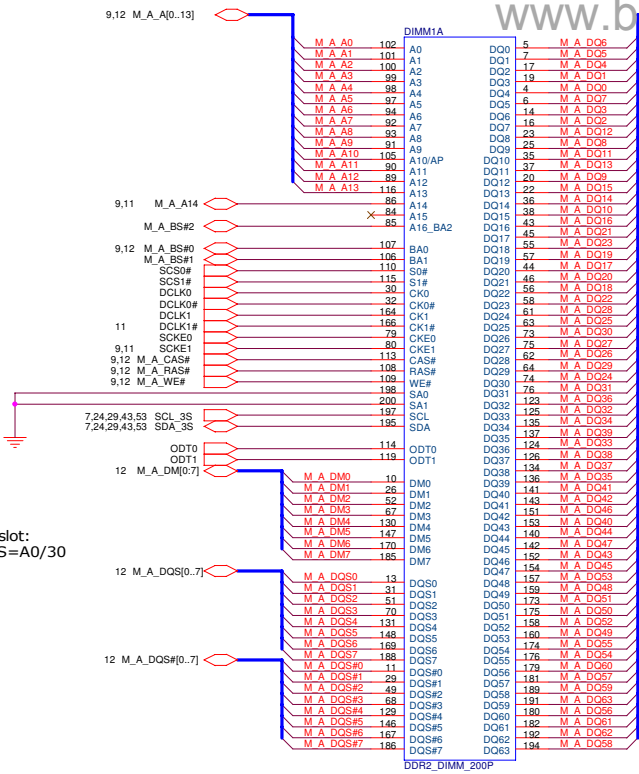
**ASUS** Title :DDR SO-DIMM

ASUSTeK COMPUTER INC Engineer:

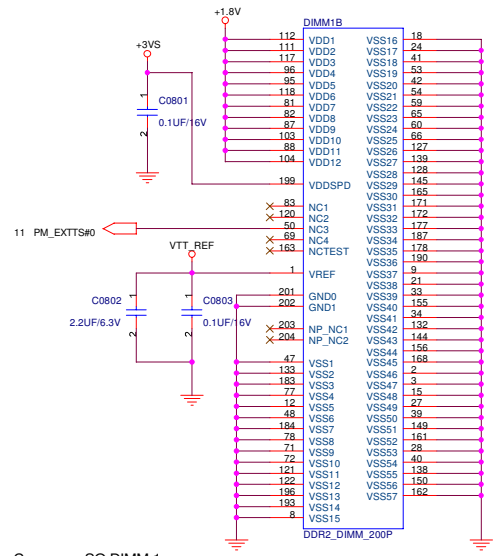
Size	Project Name	Rev
Custom	A8ES	1.0

Date: 2007.06.29 Sheet 7 of 94

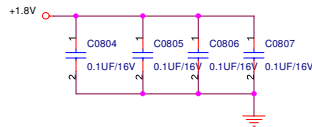
<< Kennedy\_Zhang >>



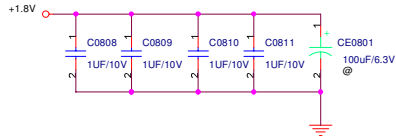
Lower slot:  
SPD/TS=A0/30



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1



Lower:Channel A

**ASUS** Title :DDR SO-DIMM\_TOP

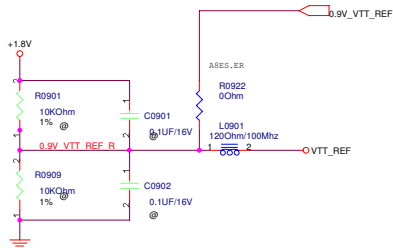
ASUSTek COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

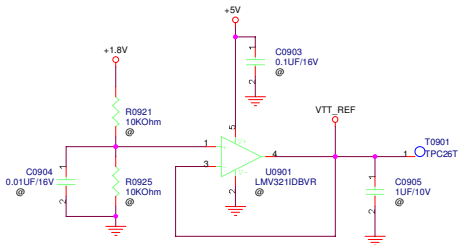
Date: 2007年06月06日 Sheet 8 of 94

<< Kennedy\_Zhang >>

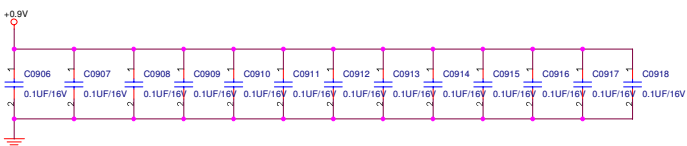
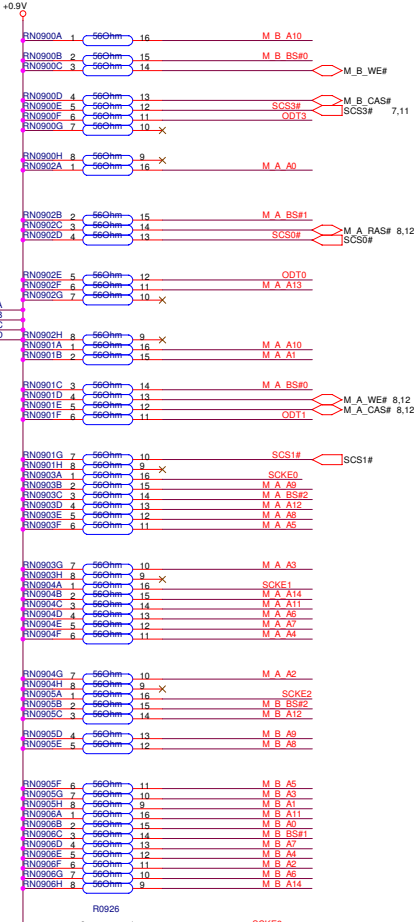




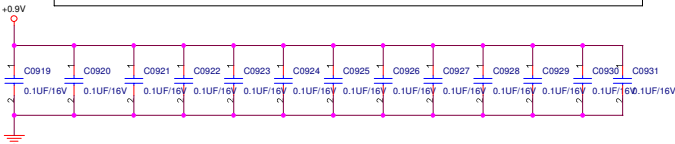
- M\_A\_A[0..13] 8,12
- M\_A\_BS[0..2] 8,12
- M\_B\_A[0..13] 7,12
- M\_B\_BS[0..2] 7,12
- SCKE[0..3] 8,11
- ODT[0..3]
- M\_B\_A14 7,11
- M\_A\_A14 8,11



- M\_B\_RAS# ODT2 2 560hm #N0907A
- SCS2# M\_B\_A13 4 560hm #N0907B
- 6 560hm #N0907C
- 8 560hm #N0907D



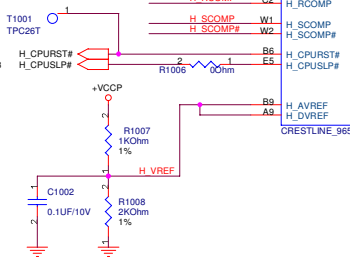
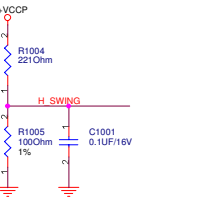
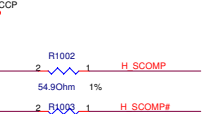
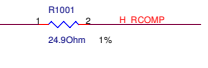
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



**ASUS** Title : DDR2 ADDR TERM  
 ASUSTek COMPUTER INC. Engineer:  
 Size Custom Project Name Rev 1.0  
 Date: 8/12/07 08:20:07 A8ES Sheet 9 of 94

<< Kennedy\_Zhang >>

H_DP0	E2	H_DP1	G2	H_DP2	H_DP1
H_DP3	M6	H_DP4	H7	H_DP5	H3
H_DP6	G4	H_DP7	H3	H_DP8	H_DP7
H_DP9	H2	H_DP10	M10	H_DP11	N12
H_DP12	N9	H_DP13	H_DP13	H_DP14	P13
H_DP15	K9	H_DP16	M2	H_DP17	W10
H_DP18	V4	H_DP19	V4	H_DP20	M3
H_DP21	J1	H_DP22	N5	H_DP23	N3
H_DP24	M6	H_DP25	W9	H_DP26	V2
H_DP27	V7	H_DP28	Y9	H_DP29	W3
H_DP30	W3	H_DP31	N1	H_DP32	AD12
H_DP33	AE3	H_DP34	AD9	H_DP35	AC9
H_DP36	AC7	H_DP37	AC14	H_DP38	AD11
H_DP39	AC11	H_DP40	AD7	H_DP41	AB1
H_DP42	AB1	H_DP43	Y3	H_DP44	AC6
H_DP45	AE2	H_DP46	AC5	H_DP47	AG3
H_DP48	AG3	H_DP49	AG3	H_DP50	AJ14
H_DP51	AE9	H_DP52	AE11	H_DP53	AH12
H_DP54	AS	H_DP55	AH5	H_DP56	AS
H_DP57	AE7	H_DP58	AJ7	H_DP59	AE5
H_DP60	AE5	H_DP61	AJ3	H_DP62	AS2
H_DP63	AH13				



HOST

H_DP3	H_DP3	H_DP3	H_DP3
H_DP4	H_DP4	H_DP4	H_DP4
H_DP5	H_DP5	H_DP5	H_DP5
H_DP6	H_DP6	H_DP6	H_DP6
H_DP7	H_DP7	H_DP7	H_DP7
H_DP8	H_DP8	H_DP8	H_DP8
H_DP9	H_DP9	H_DP9	H_DP9
H_DP10	H_DP10	H_DP10	H_DP10
H_DP11	H_DP11	H_DP11	H_DP11
H_DP12	H_DP12	H_DP12	H_DP12
H_DP13	H_DP13	H_DP13	H_DP13
H_DP14	H_DP14	H_DP14	H_DP14
H_DP15	H_DP15	H_DP15	H_DP15
H_DP16	H_DP16	H_DP16	H_DP16
H_DP17	H_DP17	H_DP17	H_DP17
H_DP18	H_DP18	H_DP18	H_DP18
H_DP19	H_DP19	H_DP19	H_DP19
H_DP20	H_DP20	H_DP20	H_DP20
H_DP21	H_DP21	H_DP21	H_DP21
H_DP22	H_DP22	H_DP22	H_DP22
H_DP23	H_DP23	H_DP23	H_DP23
H_DP24	H_DP24	H_DP24	H_DP24
H_DP25	H_DP25	H_DP25	H_DP25
H_DP26	H_DP26	H_DP26	H_DP26
H_DP27	H_DP27	H_DP27	H_DP27
H_DP28	H_DP28	H_DP28	H_DP28
H_DP29	H_DP29	H_DP29	H_DP29
H_DP30	H_DP30	H_DP30	H_DP30
H_DP31	H_DP31	H_DP31	H_DP31
H_DP32	H_DP32	H_DP32	H_DP32
H_DP33	H_DP33	H_DP33	H_DP33
H_DP34	H_DP34	H_DP34	H_DP34
H_DP35	H_DP35	H_DP35	H_DP35
H_DP36	H_DP36	H_DP36	H_DP36
H_DP37	H_DP37	H_DP37	H_DP37
H_DP38	H_DP38	H_DP38	H_DP38
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H_DP41	H_DP41	H_DP41	H_DP41
H_DP42	H_DP42	H_DP42	H_DP42
H_DP43	H_DP43	H_DP43	H_DP43
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H_DP45	H_DP45	H_DP45	H_DP45
H_DP46	H_DP46	H_DP46	H_DP46
H_DP47	H_DP47	H_DP47	H_DP47
H_DP48	H_DP48	H_DP48	H_DP48
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H_DP51	H_DP51	H_DP51	H_DP51
H_DP52	H_DP52	H_DP52	H_DP52
H_DP53	H_DP53	H_DP53	H_DP53
H_DP54	H_DP54	H_DP54	H_DP54
H_DP55	H_DP55	H_DP55	H_DP55
H_DP56	H_DP56	H_DP56	H_DP56
H_DP57	H_DP57	H_DP57	H_DP57
H_DP58	H_DP58	H_DP58	H_DP58
H_DP59	H_DP59	H_DP59	H_DP59
H_DP60	H_DP60	H_DP60	H_DP60
H_DP61	H_DP61	H_DP61	H_DP61
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H_DP63	H_DP63	H_DP63	H_DP63



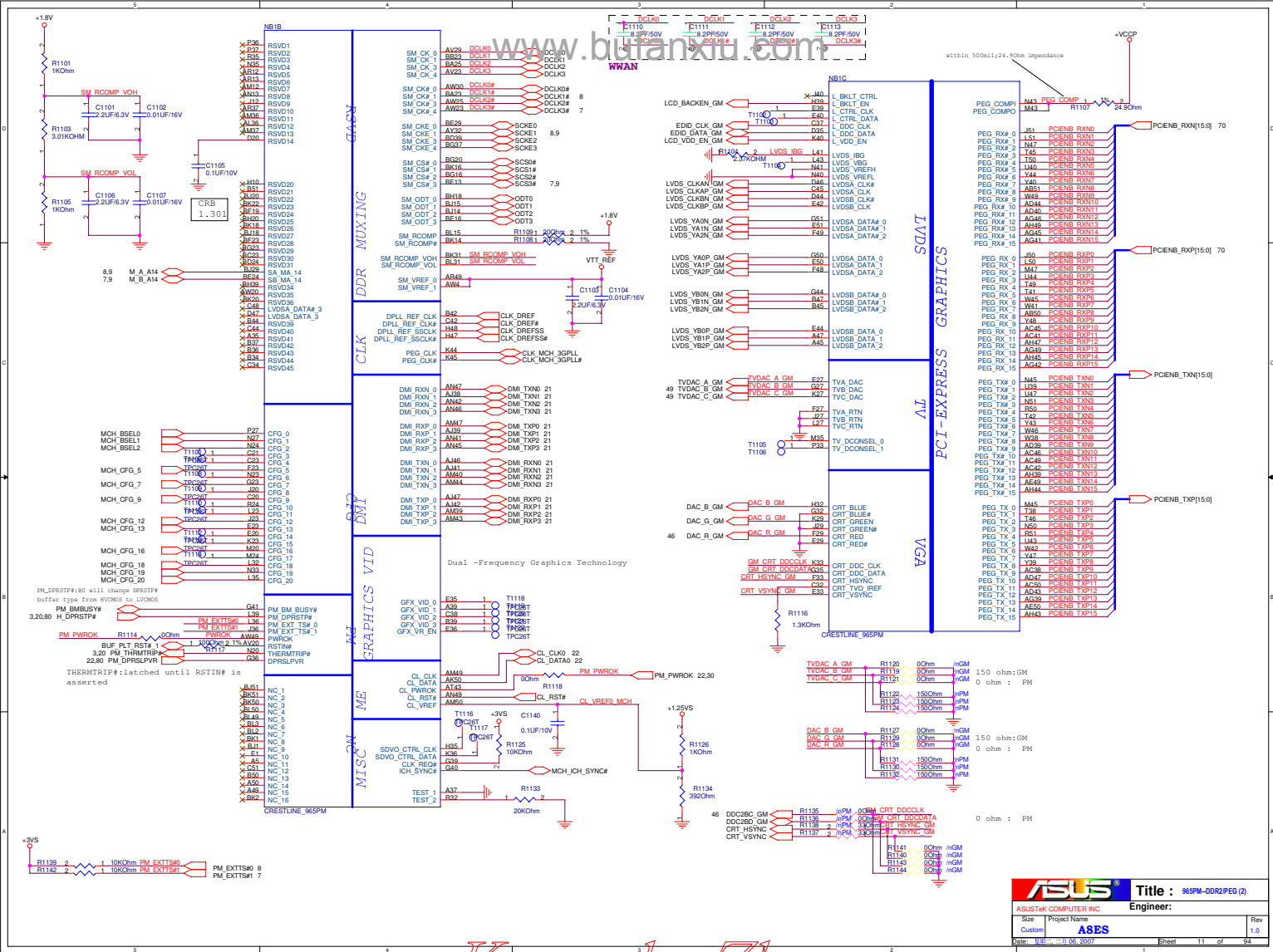
**ASUS** Title : 965PM - CPU (1)

ASUSTeK COMPUTER INC Engineer:

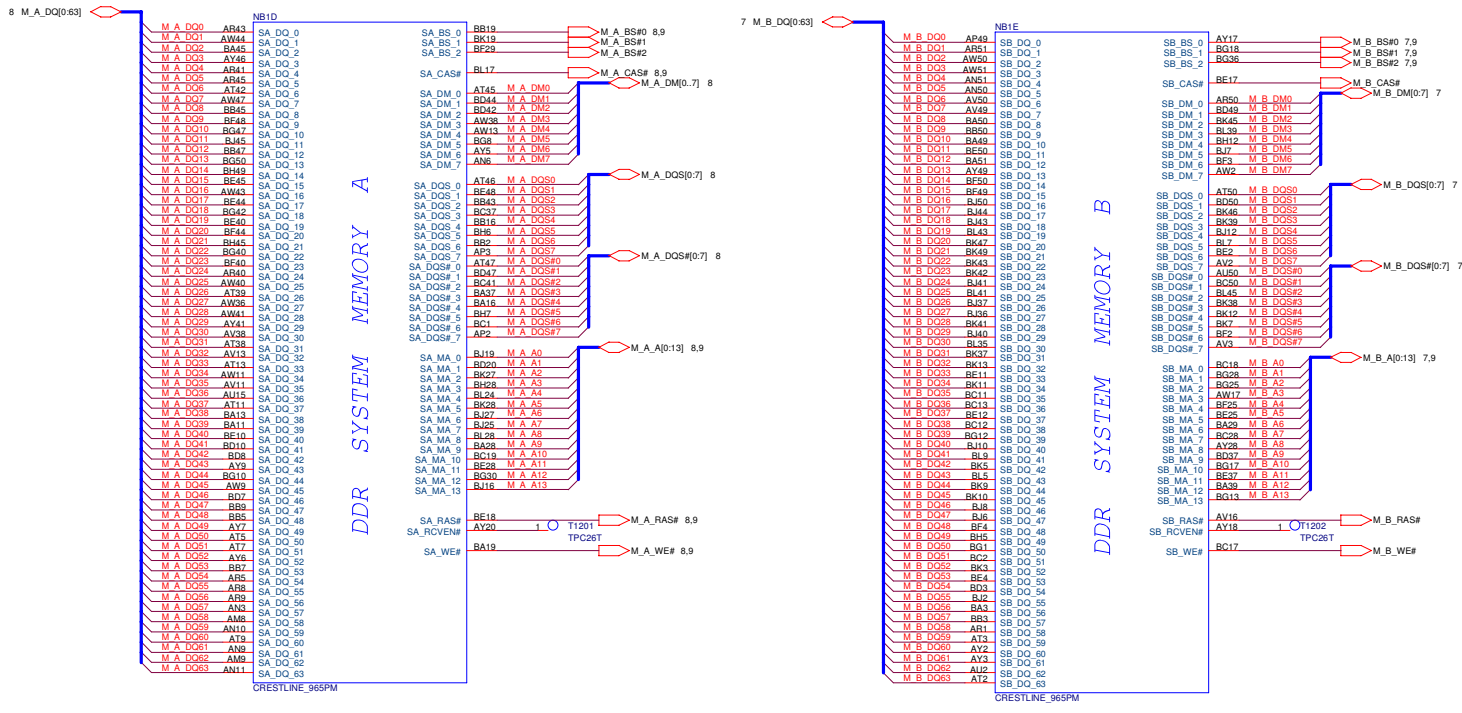
Size	Project Name	Rev
Custom	A8ES	1.0

Date: 11/05/2007 Sheet 10 of 94

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>



**ASUS** Title : 965PM-DDR2 bus (3)

ASUSTeK COMPUTER INC Engineer:

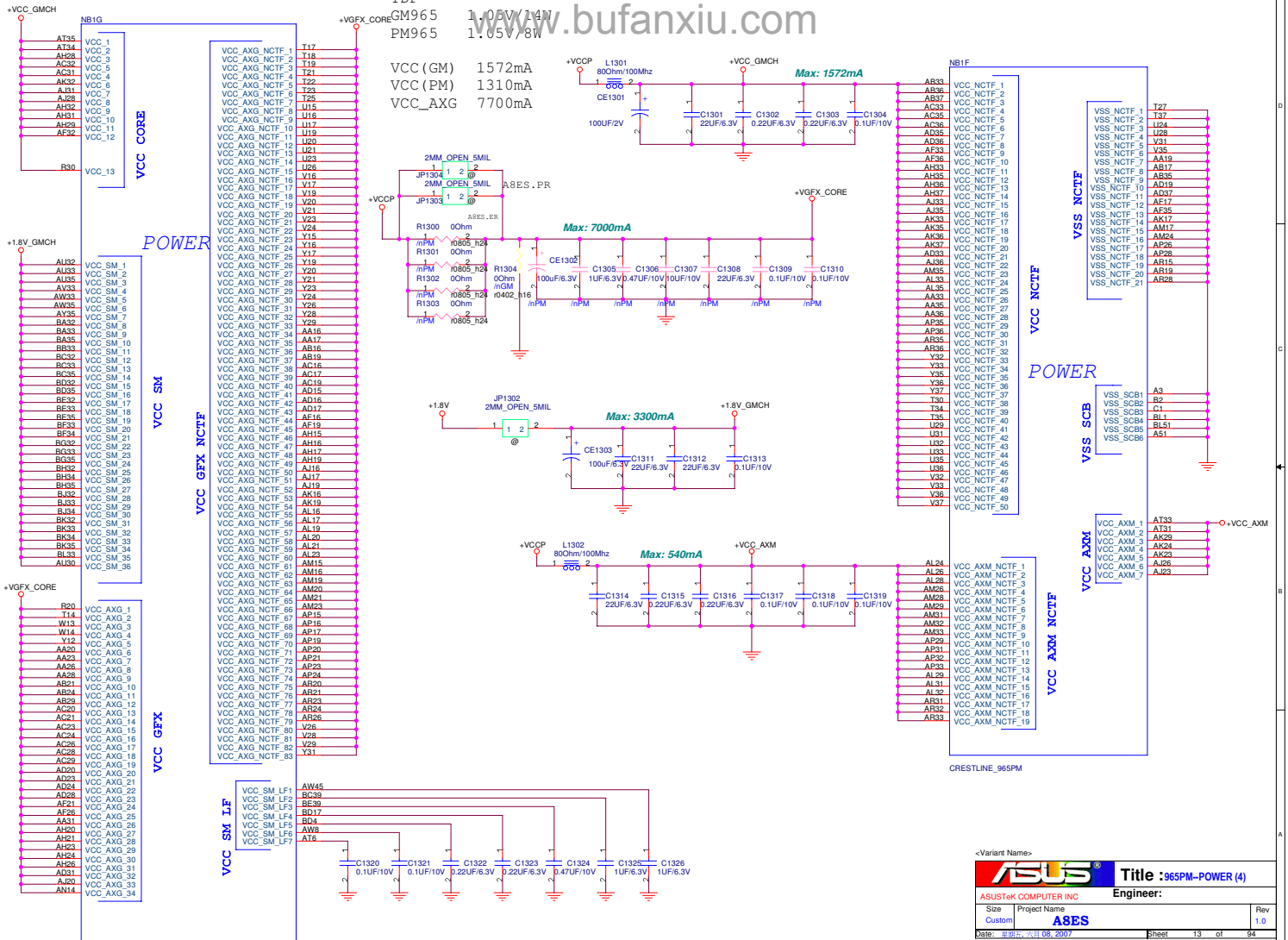
Size	Project Name	Rev
B	ABES	1.0

Date: #B# / #M# / #Y# 2007 Sheet 12 of 94

<< Kennedy\_Zhang >>

TDP  
GM965 1.05V/4W  
PM965 1.05V/8W

VCC (GM) 1572mA  
VCC (PM) 1310mA  
VCC\_AXG 7700mA



CRESTLINE\_965PM

<Variant Name>

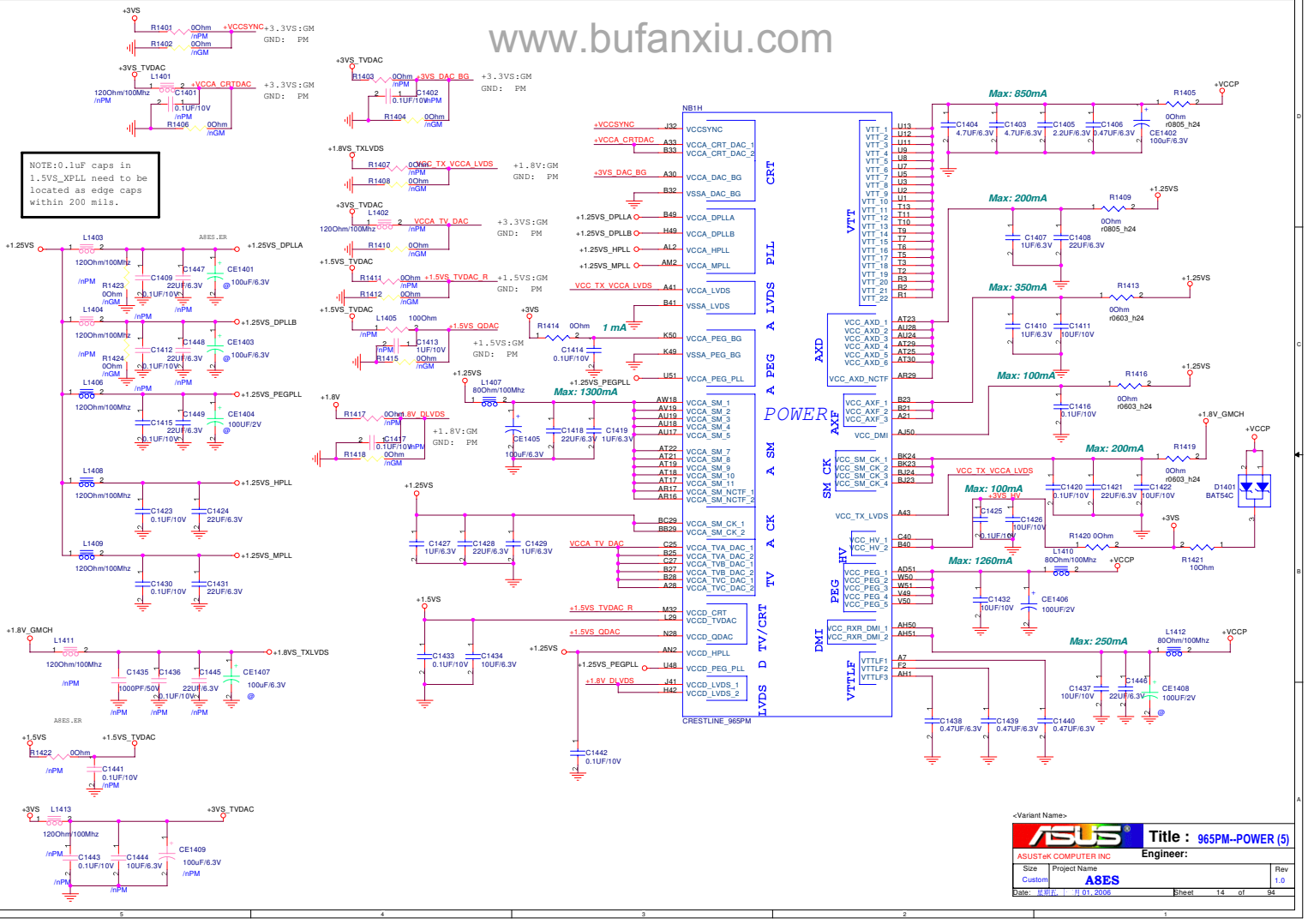
**ASUS** Title : 965PM-POWER (4)

ASUSTeK COMPUTER INC. Engineer:

Size	Project Name	Rev
Custom	A8ES	1.0

Date: 08/08/2007 Sheet 19 of 84

<< Kennedy\_Zhang >>



-Variant Name-

**ASUS** Title : 965PM-POWER (5)

ASUSTeK COMPUTER INC Engineer:

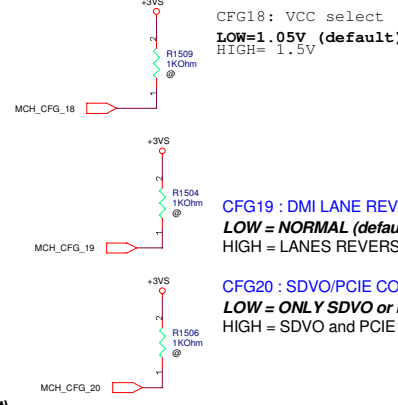
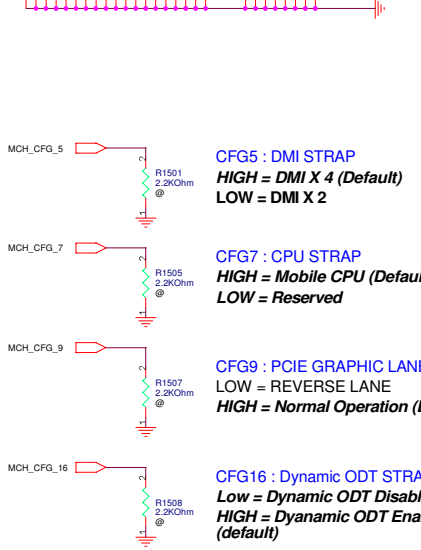
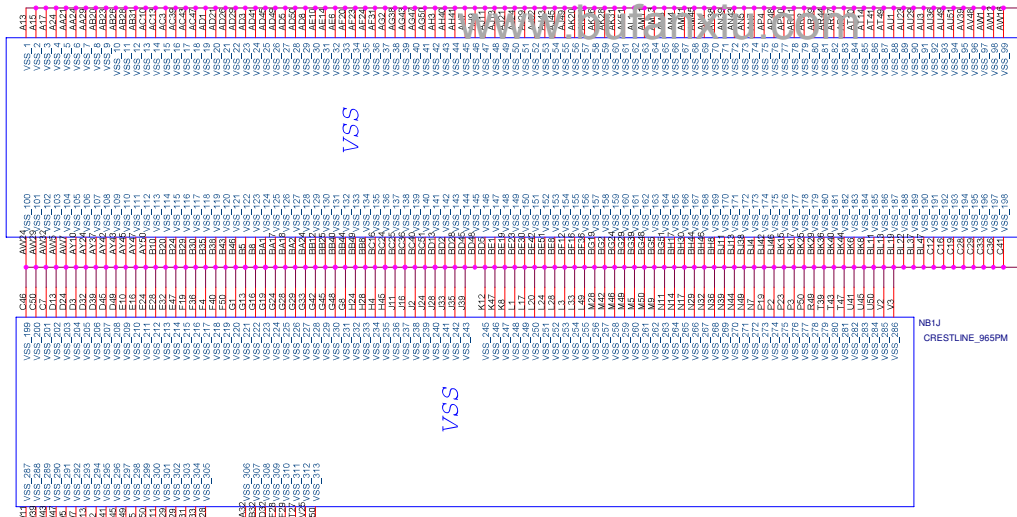
Size Project Name

Custom **ABES**

Date: 11/01/2008 Sheet 14 of 84

HIGH = LANES REVERSED


<< Kennedy\_Zhang >>



**CFG [13:12] : XOR/ALL-Z**  
00 = Reserved  
01= XOR Mode Enabled  
10= All-Z Mode Enabled  
11= Normal Operation (Default)


<b>ASUS</b>		<b>Title : GND/Strapping (6)</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	<b>A8ES</b>		1.0
Date:	11/06/2007	Sheet	15 of 84

<< Kennedy\_Zhang >>


		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 16 of 94

<< Kennedy\_Zhang >>




		<b>Title : BLANK</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 17 of 94

<< Kennedy\_Zhang >>

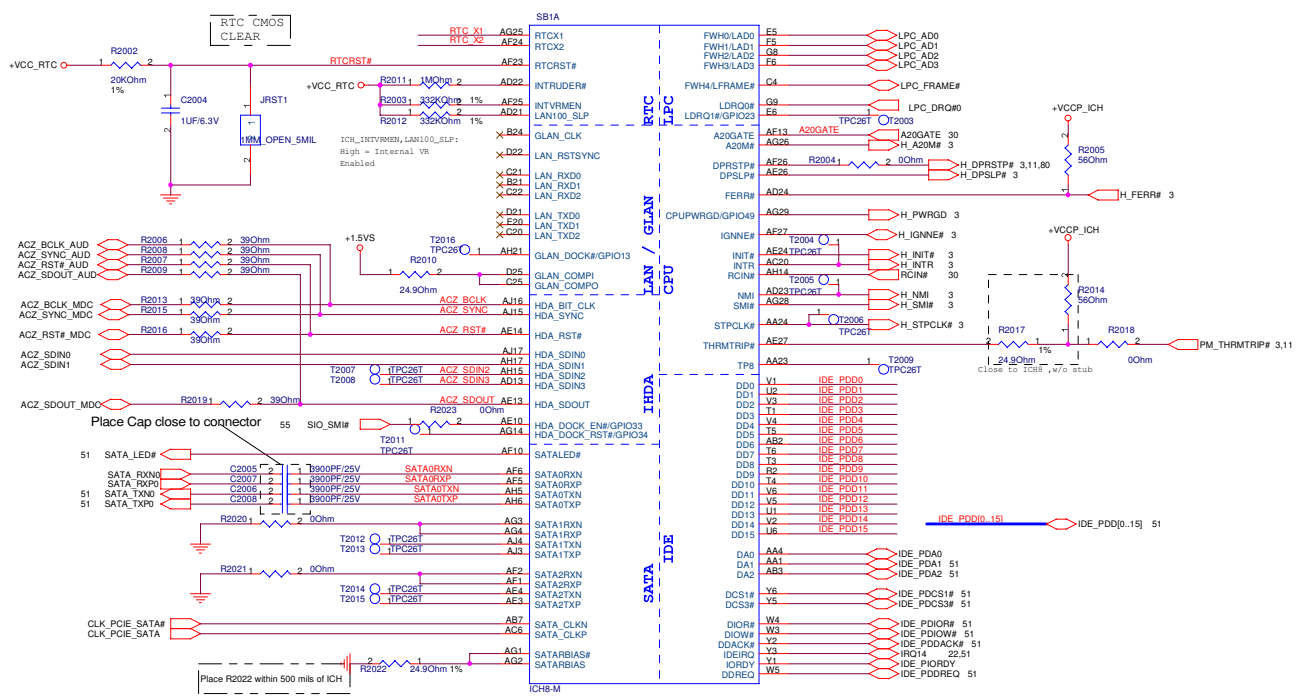
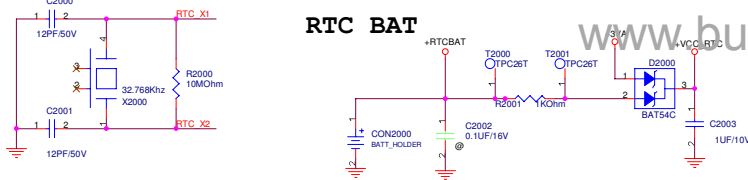
		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8ES</b>	Rev 0	
Date: 星期三, 十月 11, 2006		Sheet	18 of 94

<< Kennedy\_Zhang >>

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	19 of 94

<< Kennedy\_Zhang >>

RTC BAT

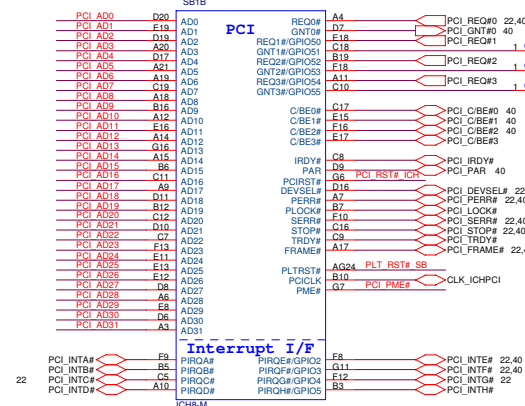


SATA if it non-used,  
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA\_CLKpn should be PD.  
2)SATA[0:3]TXpn and SATALED# NO connect.

<-Variant Name>

<b>ASUS</b>		<b>Title : ICH8-M (1)</b>
ASUSTek COMPUTER INC.		Engineer:
Size	Project Name	Rev
Custom	ABES	1.0
Date: 8/18/07	08_08_2007	Sheet 20 of 94

<< Kennedy\_Zhang >>

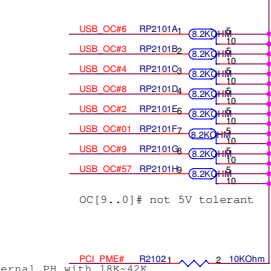
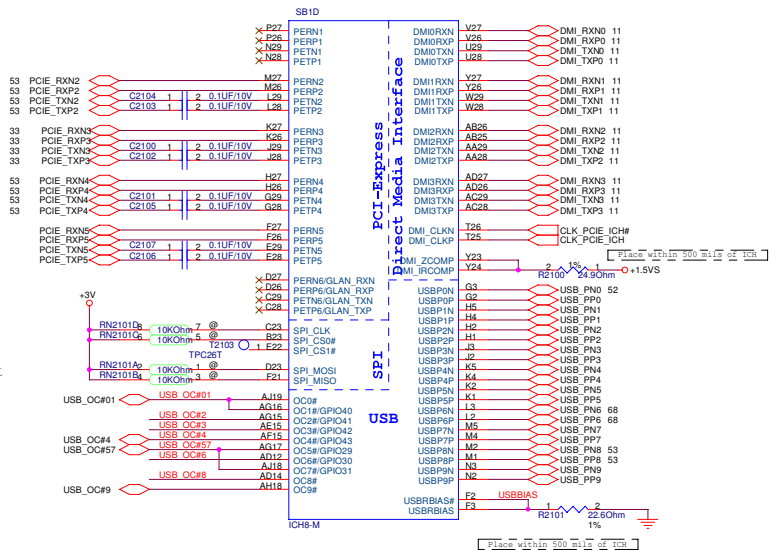
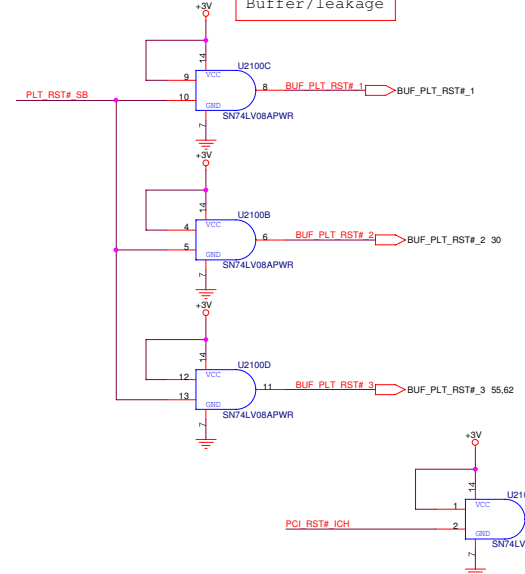


miniCard 1  
LAN  
miniCard 2  
NEW CARD

- 0: I/O
- 1: I/O
- 2: Bluetooth
- 3: Finger Print
- 4: New Card
- 5: I/O
- 6: Camera
- 7: I/O
- 8: miniCard 2
- 9: I/O

Note: PLTRST# is in VccSUS3\_3 well

Check Buffer/leakage



ICH8 Boot BIOS select

GPIO	INTF0	SPL_CS#1
GPIO0	1	1
GPIO1	1	1
SPL_D1	0	1

(default)

<Variant Name>

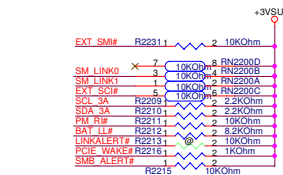
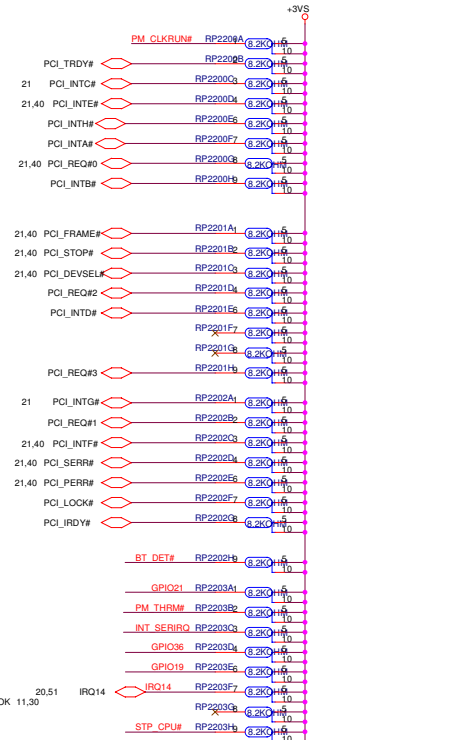
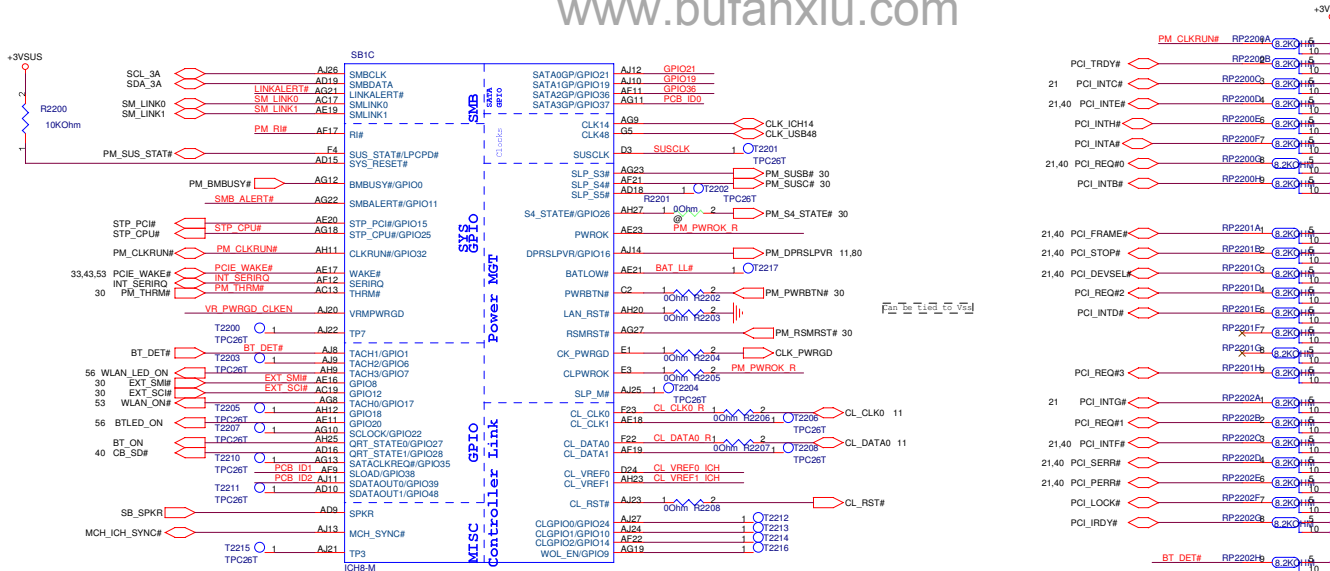
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ASUSTek COMPUTER INC. Engineer:

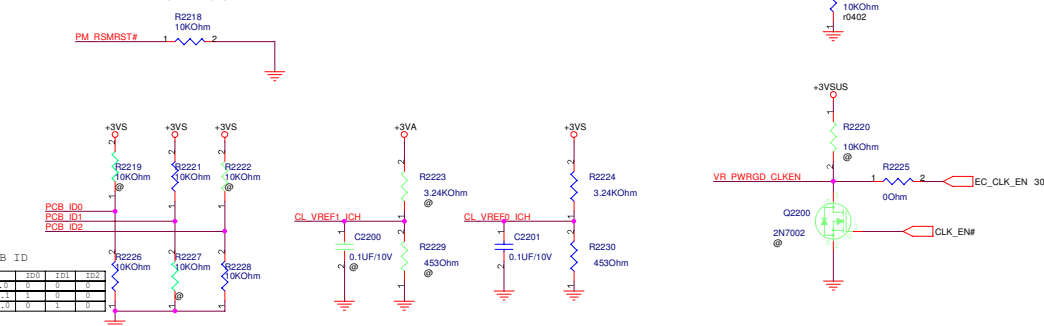
Size	Project Name	Rev
Custom	A8ES	1.0

Date: 8/18/2007 Sheet 21 of 94

<< Kennedy\_Zhang >>



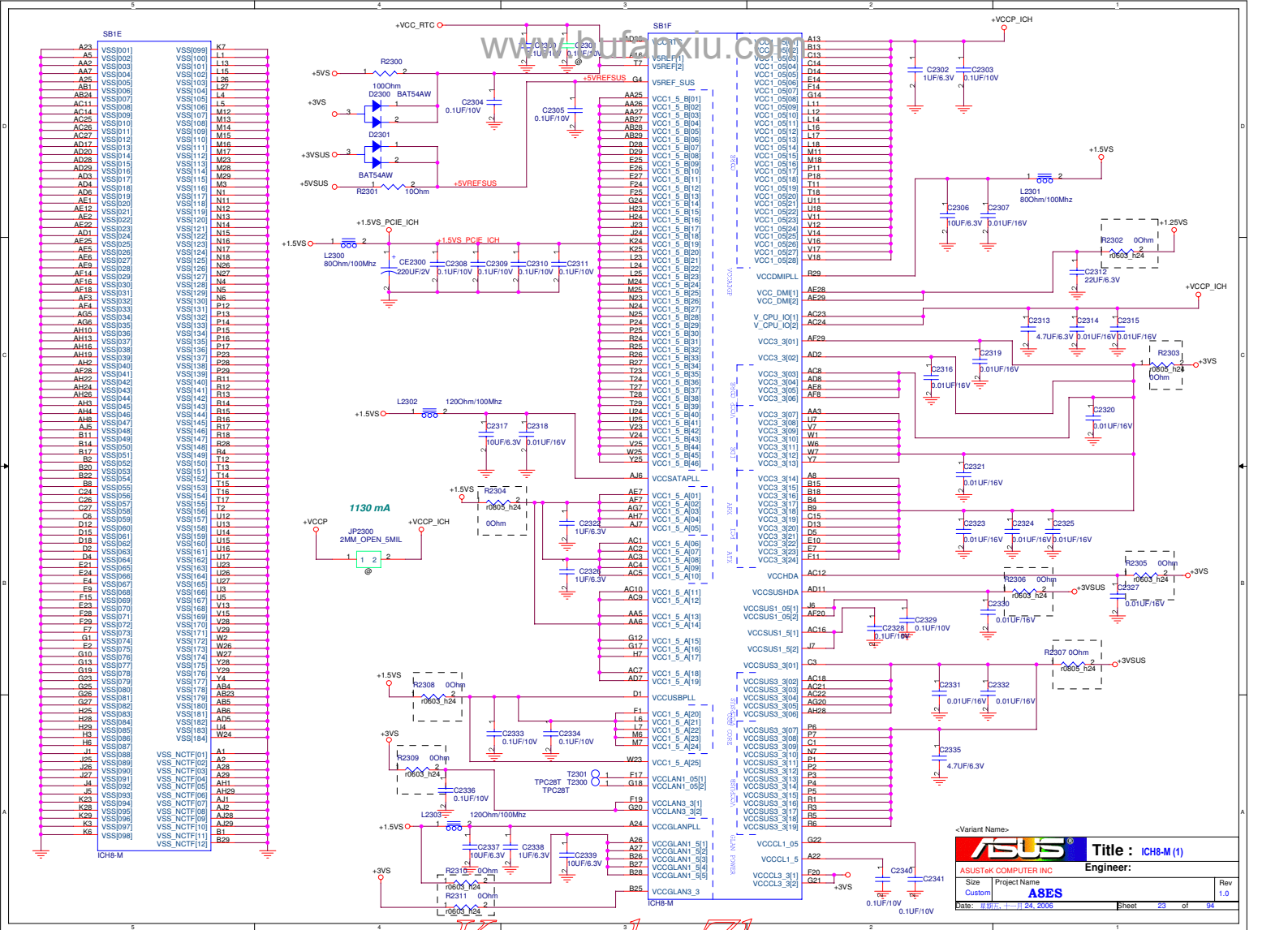
From WW33



PCB ID	FDI	FBI	FBI
1-0	0	0	0
1-1	0	0	0
1-2	0	0	0

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**ASUS** Title: ICH8-M (3)  
 ASUSTek COMPUTER INC Engineer:  
 Site: Project Name: Rev  
 Custom: ABE5  
 Date: 08/29/2007 Sheet 22 of 94

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

Title : ICH8-M (1)

ASUSTek COMPUTER INC. Engineer:

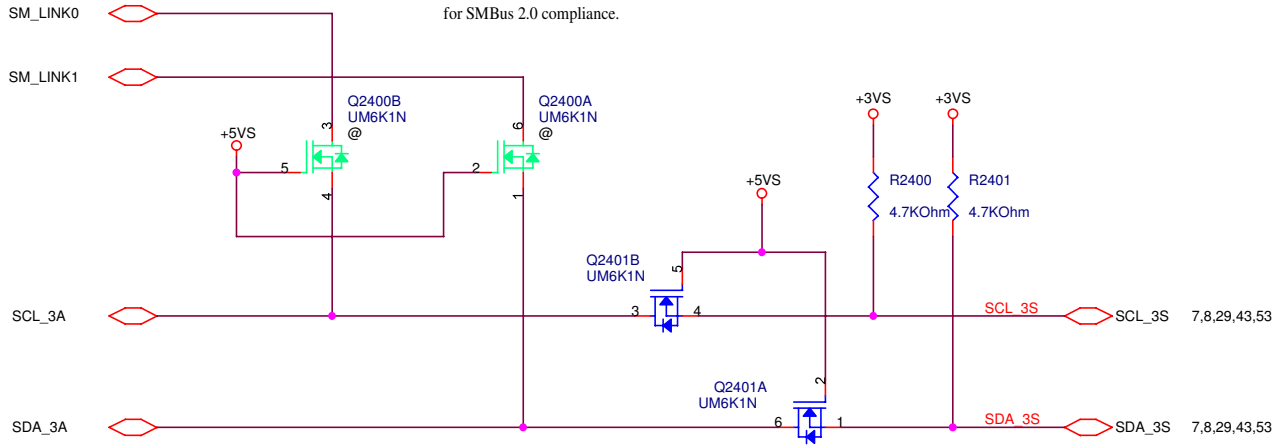
Size Custom Project Name A8ES Rev 1.0

Date: 2006-11-24 2006 Sheet 23 of 94

Check

Connect SMLINK and SMBUS for SMBus 2.0 compliance.

ICH8-M



ICH8-M

<Variant Name>

**ASUS** Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC Engineer:

Size Project Name Rev

A A8ES 1.0

Date: 星期二, 二月 06, 2007 Sheet 24 of 94

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ICH8-M GPIO Assignment

Name	HW Pin Definition	Type	Tolerance	Power Well	Default	Mux	Native Name	Real Name	Notes
GPIO0	PM_BMBUSY#	I/O	3.3V	Core	GPI	Yes	EMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	I/O	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	I/O	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	I/O	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	I/O	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	I/O	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	I/O	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	I/O	3.3V	Core	GPI	No			
GPIO8	EXT_SM#	I/O	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	I/O	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	I/O	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		I/O	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SC#	I/O	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	I/O	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	I/O	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PC#	I/O	3.3V	Resume	Native	No	STP_PC#	STP_PC#	
GPIO16	PM DPRSLPVR	I/O	3.3V	Core	Native	Yes	DPRSLPVR	PM DPRSLPVR	
GPIO17	WLAN_ON#	I/O	3.3V	Core	GPI	No			
GPIO18		I/O	3.3V	Core	GPO	No			
GPIO19		I/O	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	I/O	3.3V	Core	GPO	No			
GPIO21		I/O	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		I/O	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		I/O	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	I/O	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC, note by Alan
GPIO25	STP_CPU#	I/O	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM S4_STATE#	I/O	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON# <b>BT_ON</b>	I/O	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	I/O	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	I/O	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	I/O	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	I/O	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	I/O	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		I/O	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	I/O	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	I/O	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	I/O	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	I/O	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	I/O	3.3V	Core	GPI	Yes	SDATAOUT0		
GPIO40	OC4#	I/O	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	I/O	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	I/O	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	I/O	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		I/O	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		I/O	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	I/O	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	I/O	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	I/O	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	I/O	3.3V	Core	Native	Yes	GNT2#		
GPIO54		I/O	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		I/O	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

**Title : BLANK**


**Engineer:**

ASUSTeK COMPUTER INC  
**A8ES**


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Date: 2006年11月11日

Rev: 0  
Sheet: 25 of 94


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		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	26 of 94

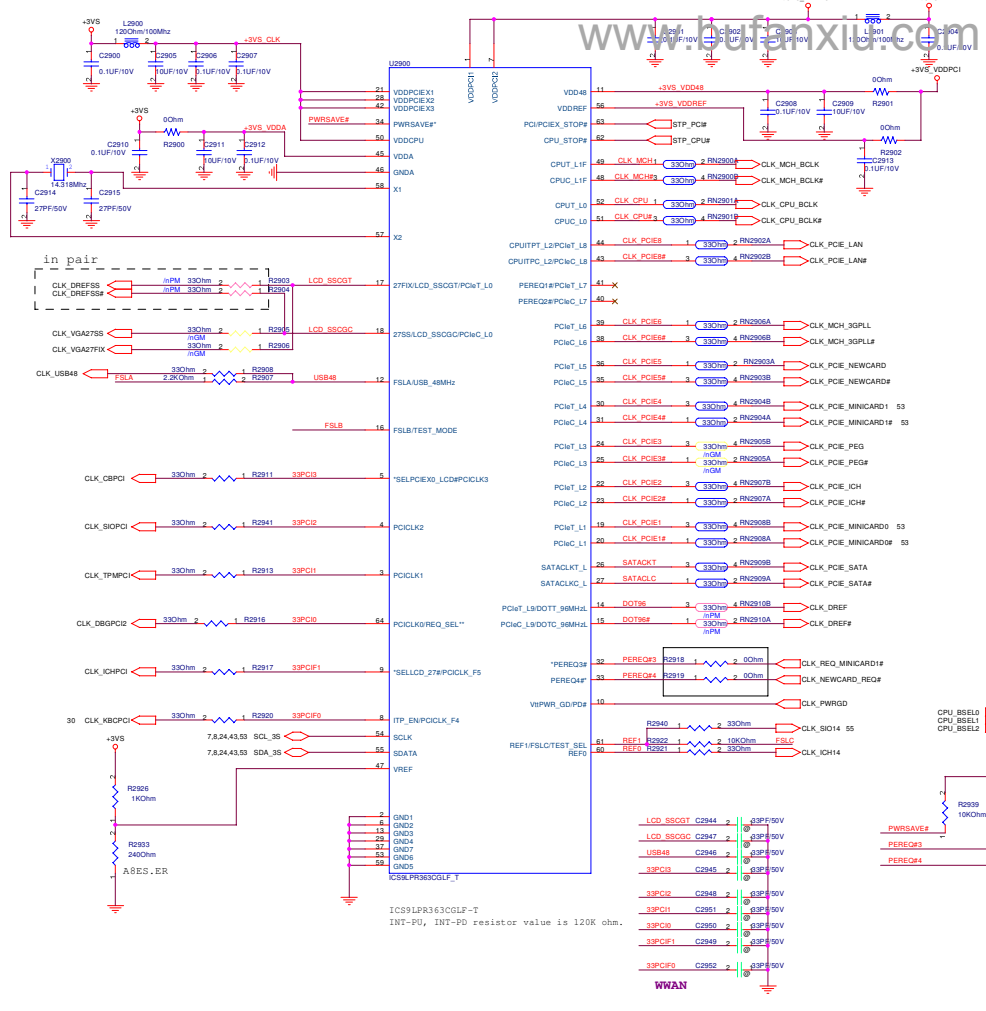
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ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 27 of 94

<< Kennedy\_Zhang >>

		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
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Date: 星期三, 十月 11, 2006		Sheet	28 of 94

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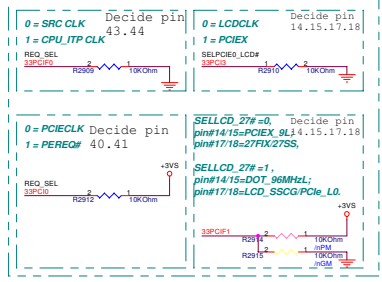


PEREQ3 0 = Enable control PCIe4/2 through I2C  
 1 = Disable PCIe4/2 Controlled  
 PEREQ4 0 = Enable control PCIe7/3 through I2C  
 1 = Disable PCIe7/3 Controlled

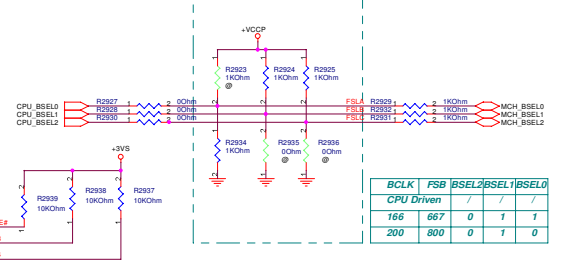
Latch Select Table

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD# PC3 = 0 (low)	SELLED_27# = 0 SELLED_27# = 1	PCIE9 DOT96	27FWSS LCD
SELPCIE0_LCD# PC3 = 1 (high)	SELLED_27# = 0 SELLED_27# = 1	PCIE9 DOT96	PCIE0

Latched Input Select



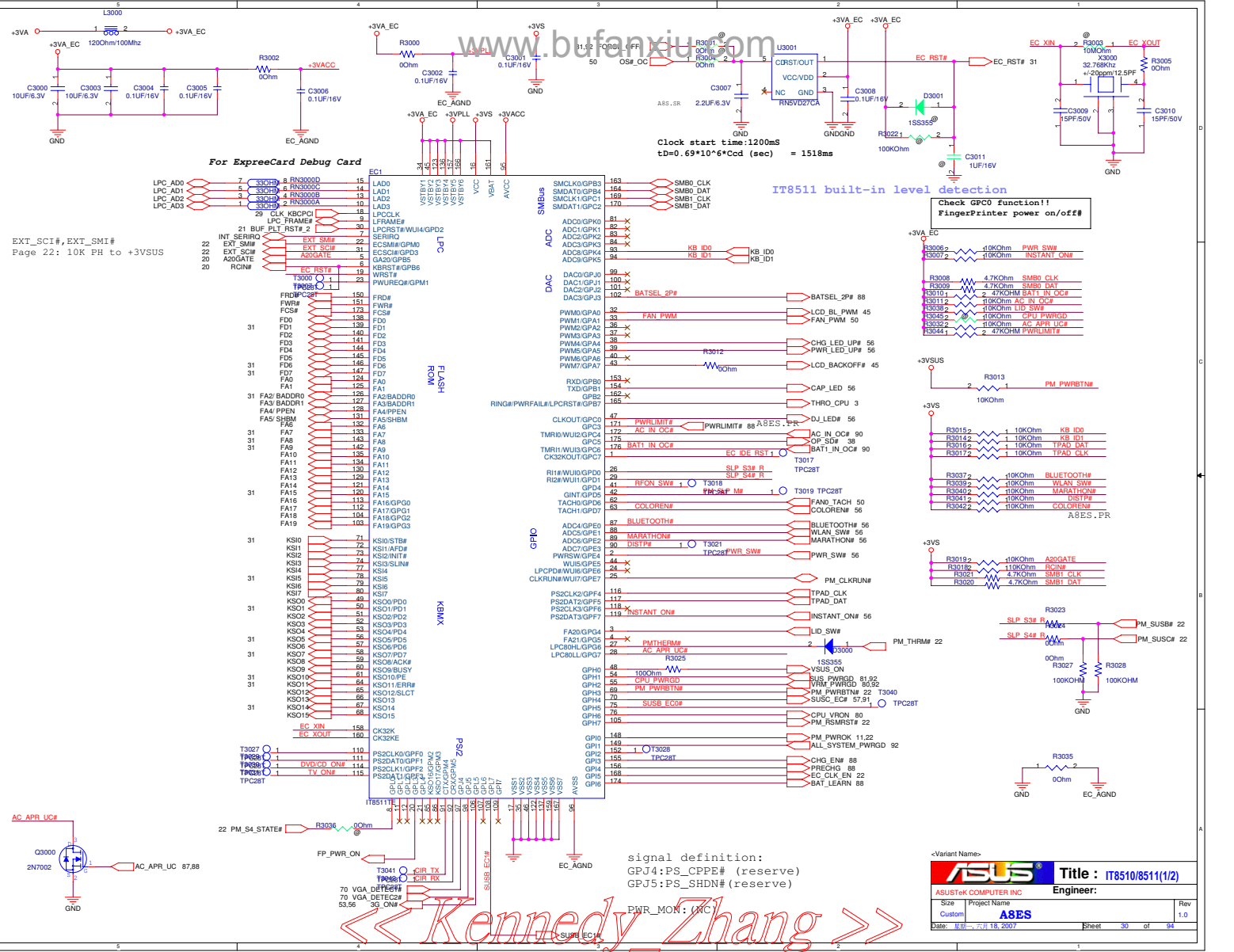
Reserved for R1.0 Debug



BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven	/	/	/	/
166	667	0	1	1
200	800	0	1	0

ASUS  
 ASUSTek COMPUTER INC  
 Project Name: **ABES**  
 Title: **CLOCK GEN**  
 Engineer:  
 Date: 11/08/2007 Page 39 of 34

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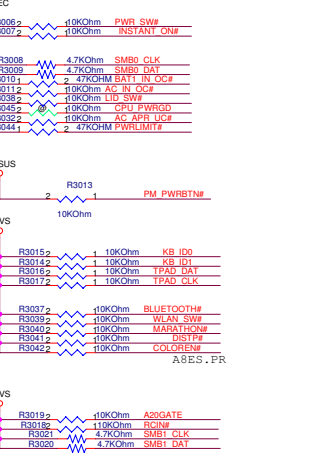
For ExpressCard Debug Card

Clock start time: 1200ms  
 $t_D = 0.69 \cdot 10^{-6} \cdot C_{cd} \text{ (sec)} = 1518\text{ms}$

IT8511 built-in level detection

Check GPIO function!  
 FingerPrinter power on/off#

EXT\_SCI#; EXT\_SMI#  
 Page 22: 10K PH to +3VSUS



signal definition:  
 GPJ4:PS\_CPPE# (reserve)  
 GPJ5:PS\_SHDN# (reserve)

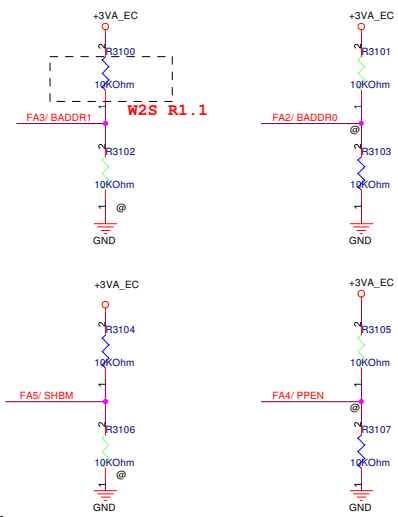
PWR\_MON: IXC

ASUS		Title: IT8510/8511(1/2)
ASUSTek COMPUTER INC		Engineer:
Size: Custom	Project Name: A8ES	Rev: 1.0
Date: 11/16 - 11/18, 2007	Sheet: 30	of 34

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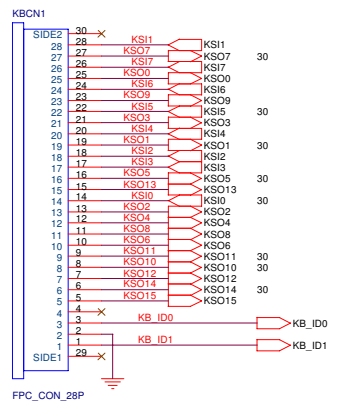
DVDDC0\_ON#

10:Determined by EC



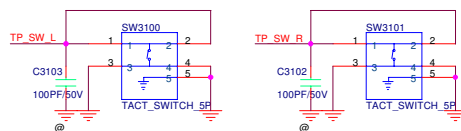
**BADDR[1:0]**  
**No pull up:**  
 The register pair to access PNPCFG is 002Eh and 002Fh.  
**Ext 10K up on BADDR0.**  
 The register pair to access PNPCFG is 004Eh and 004Fh.  
**Ext 10K up on BADDR1:**  
 The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

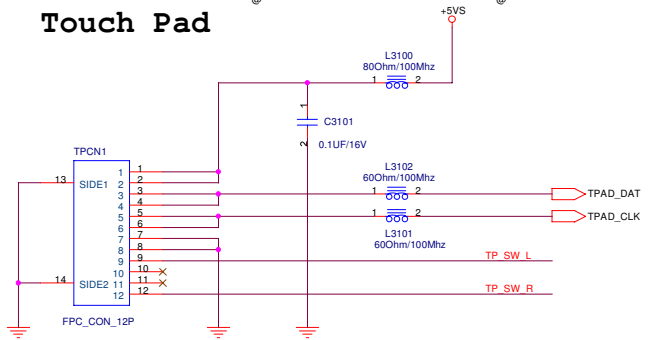


**PPEN**  
**No pull up:**  
 Normal  
**Ext 10K up:**  
 KBS interface pins are switched to parallel port interface for in-system programming.

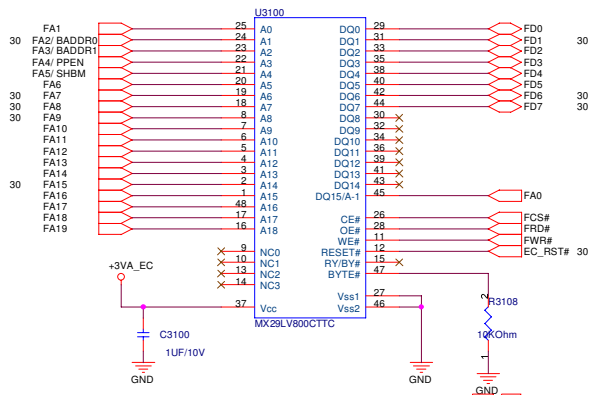
**SHBM**  
**No pull up:**  
 disable shared memory with host BIOS  
**Ext 10K up:**  
 enable shared memory with host BIOS



Touch Pad




8M TSOP



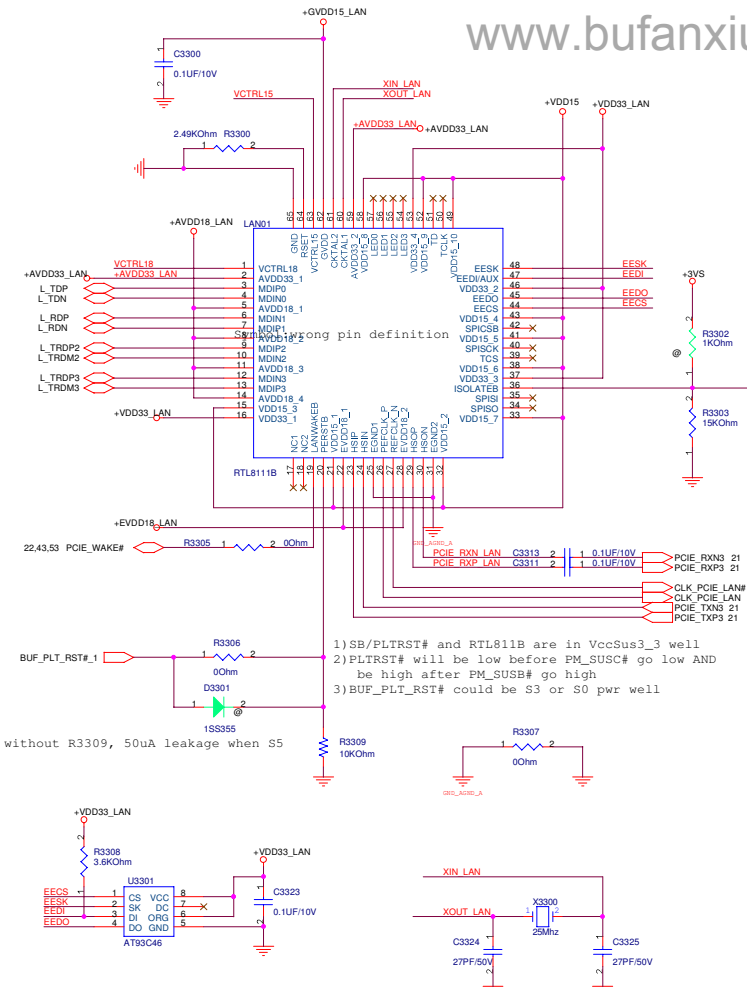
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**Title : IT8510/8511(2/2)**  
**ASUSTeK COMPUTER INC** **Engineer:**  
 Size Project Name  
 Custom **A8ES**  
 Date: 2007.05.24, 2007 Sheet 31 of 94 Rev 1.0

« Kennedy\_Zhang »

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ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8ES</b>	Rev 0	
Date: 星期三, 十月 11, 2006		Sheet	32 of 94

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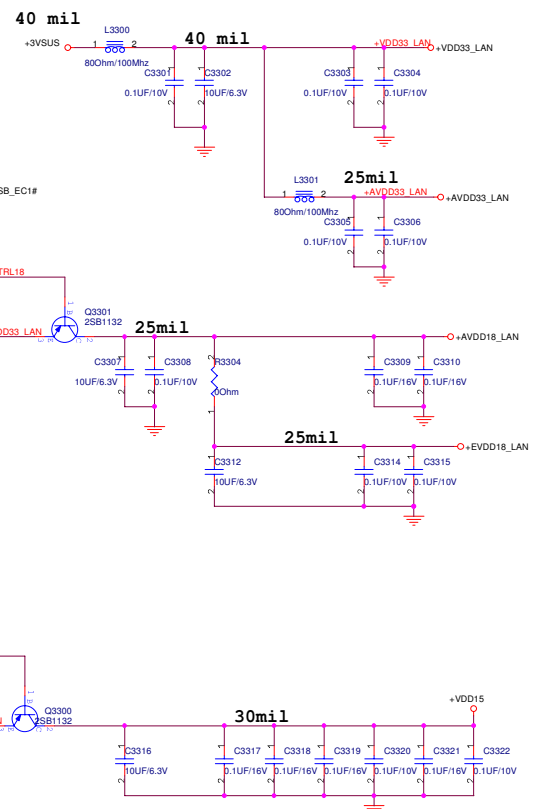




Pin definition

1	VCTRL18	48	EESK
2	+AVDD33_LAN	47	EEDI
3	AVDD33_1	46	EED0
4	MDI0	45	EED0
5	AVDD18_1	44	EED0
6	MDI0	43	EED0
7	MDI0	42	EED0
8	MDI0	41	EED0
9	MDI0	40	EED0
10	MDI0	39	EED0
11	MDI0	38	EED0
12	MDI0	37	EED0
13	MDI0	36	EED0
14	MDI0	35	EED0
15	MDI0	34	EED0
16	MDI0	33	EED0
17	MDI0	32	EED0
18	MDI0	31	EED0
19	MDI0	30	EED0
20	MDI0	29	EED0
21	MDI0	28	EED0
22	MDI0	27	EED0
23	MDI0	26	EED0
24	MDI0	25	EED0
25	MDI0	24	EED0
26	MDI0	23	EED0
27	MDI0	22	EED0
28	MDI0	21	EED0
29	MDI0	20	EED0
30	MDI0	19	EED0
31	MDI0	18	EED0
32	MDI0	17	EED0
33	MDI0	16	EED0

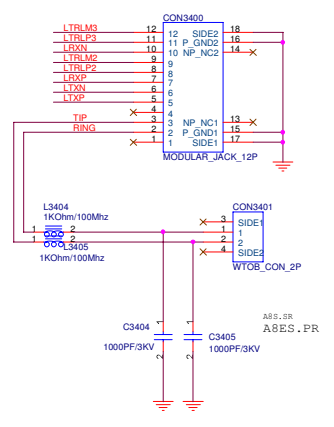
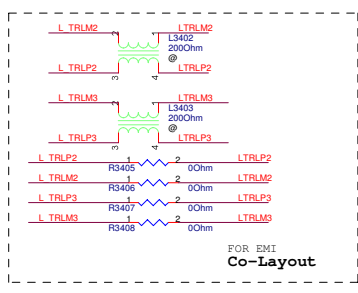
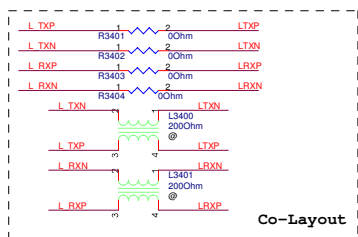
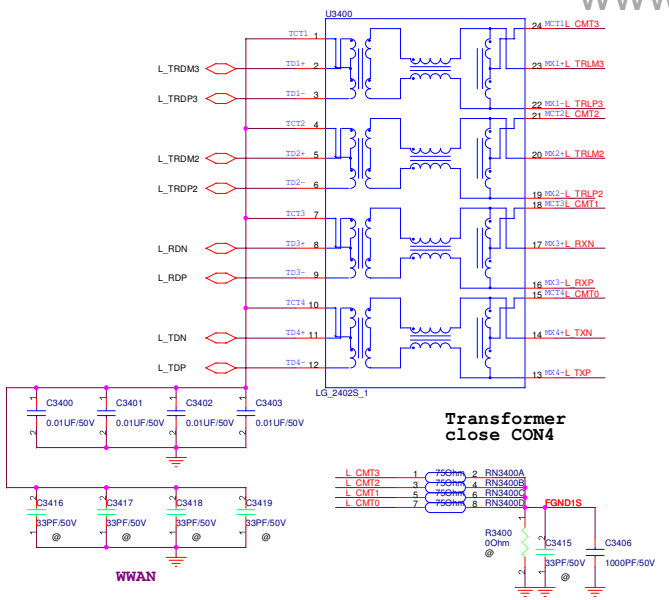
- 1) SB/PLTRST# and RTL811B are in VccSus3\_3 well
- 2) PLTRST# will be low before PM\_SUSC# go low AND be high after PM\_SUSB# go high
- 3) BUF\_PLT\_RST# could be S3 or S0 pwr well



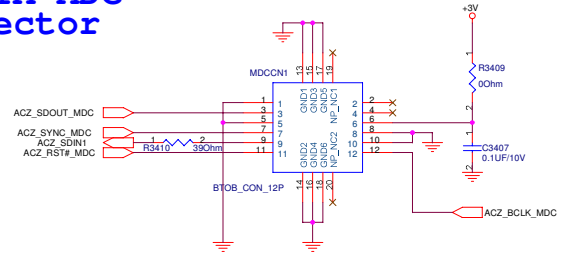
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<b>ASUS</b>		<b>Title : GigaLAN</b>	
ASUSTek COMPUTER INC.		Engineer:	
Size	Project Name		Rev
Custom	<b>ABES</b>		1.0
Date:	11/06/2007	Sheet	33 of 94

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### AZALIA MDC Connector



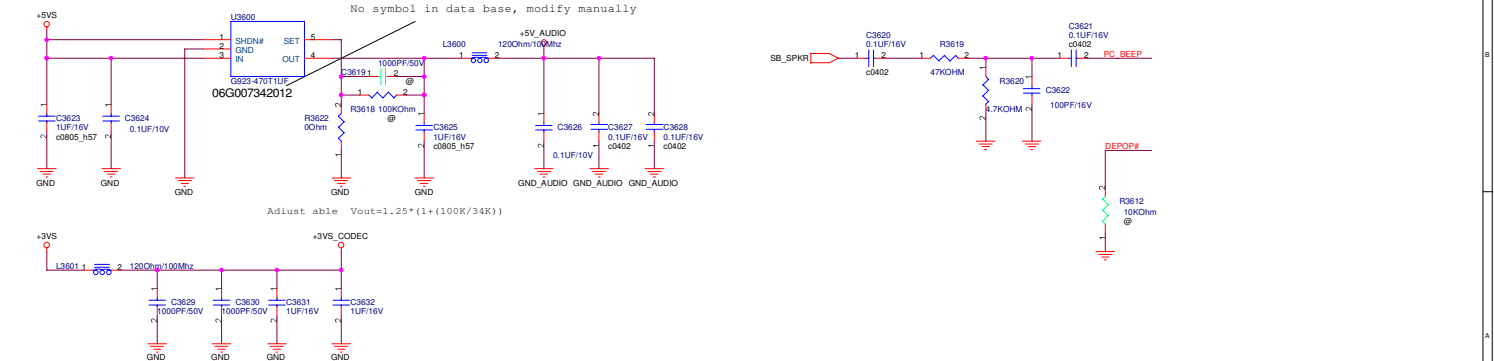
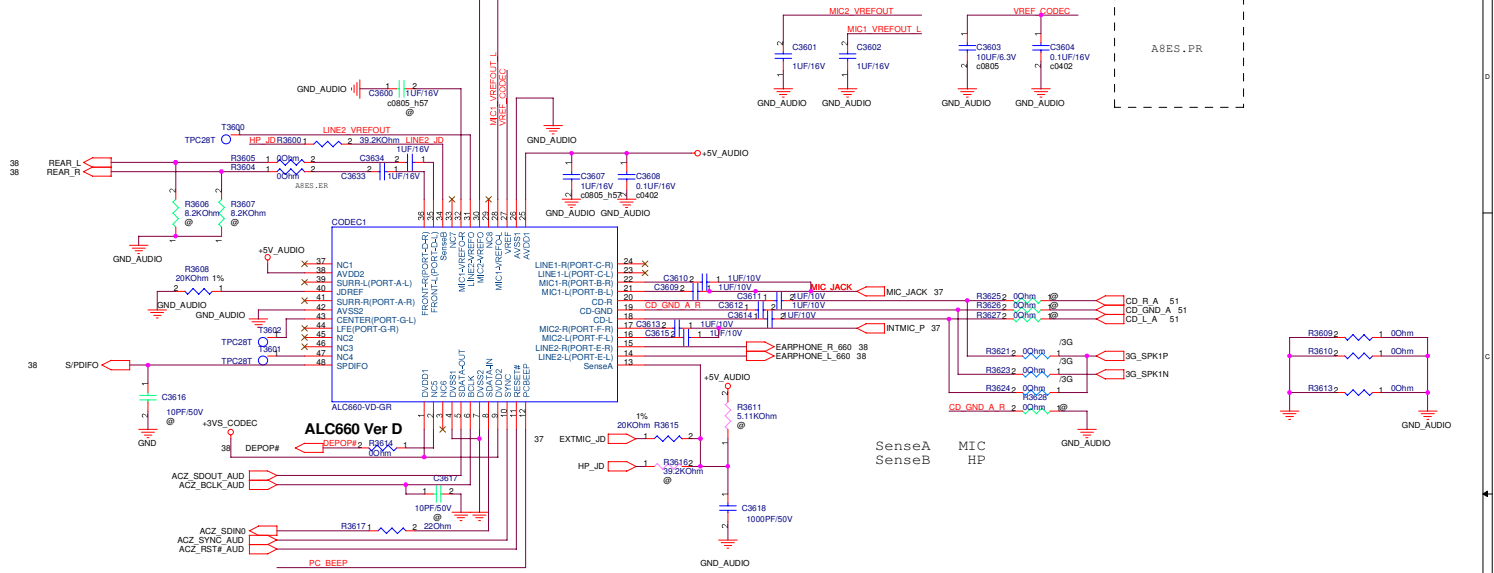
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<b>ASUS</b>		<b>Title : RJ11+45_MDC</b>
ASUSTeK COMPUTER INC.		Engineer:
Size	Project Name	Rev
Custom	<b>A8ES</b>	1.0
Date: 2007.12.12	Sheet 34	of 94

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		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8ES</b>		Rev 0
Date: 星期三, 十月 11, 2006		Sheet	35 of 94

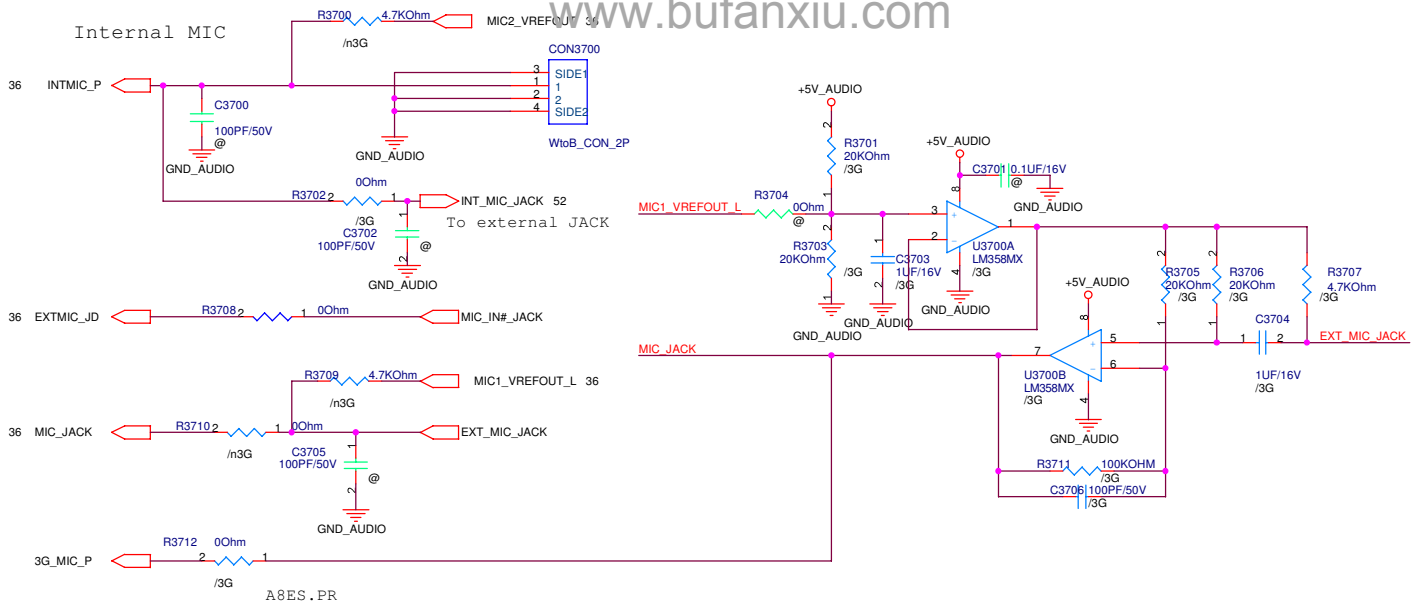
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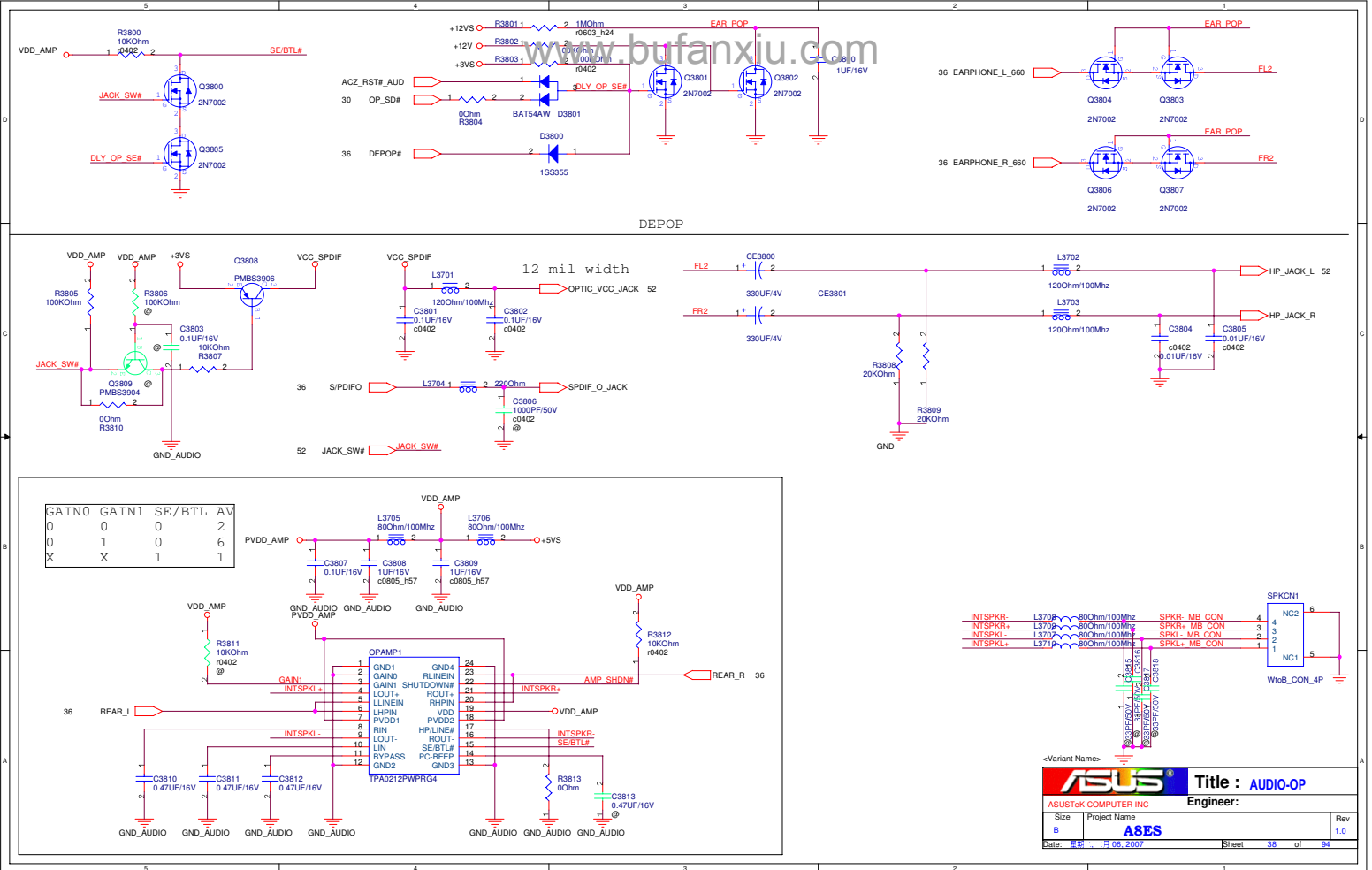
<b>ASUS</b>		<b>Title : CODEC-ALC660</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 11/03/2007	Sheet 38	of 94	

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		<b>Title : AUDIO-MIC</b>
ASUSTeK COMPUTER INC		Engineer:
Size Custom	Project Name <b>A8ES</b>	Rev 1.0
Date: 星期三, 二月 06, 2007		Sheet 37 of 94

<< Kennedy\_Zhang >>

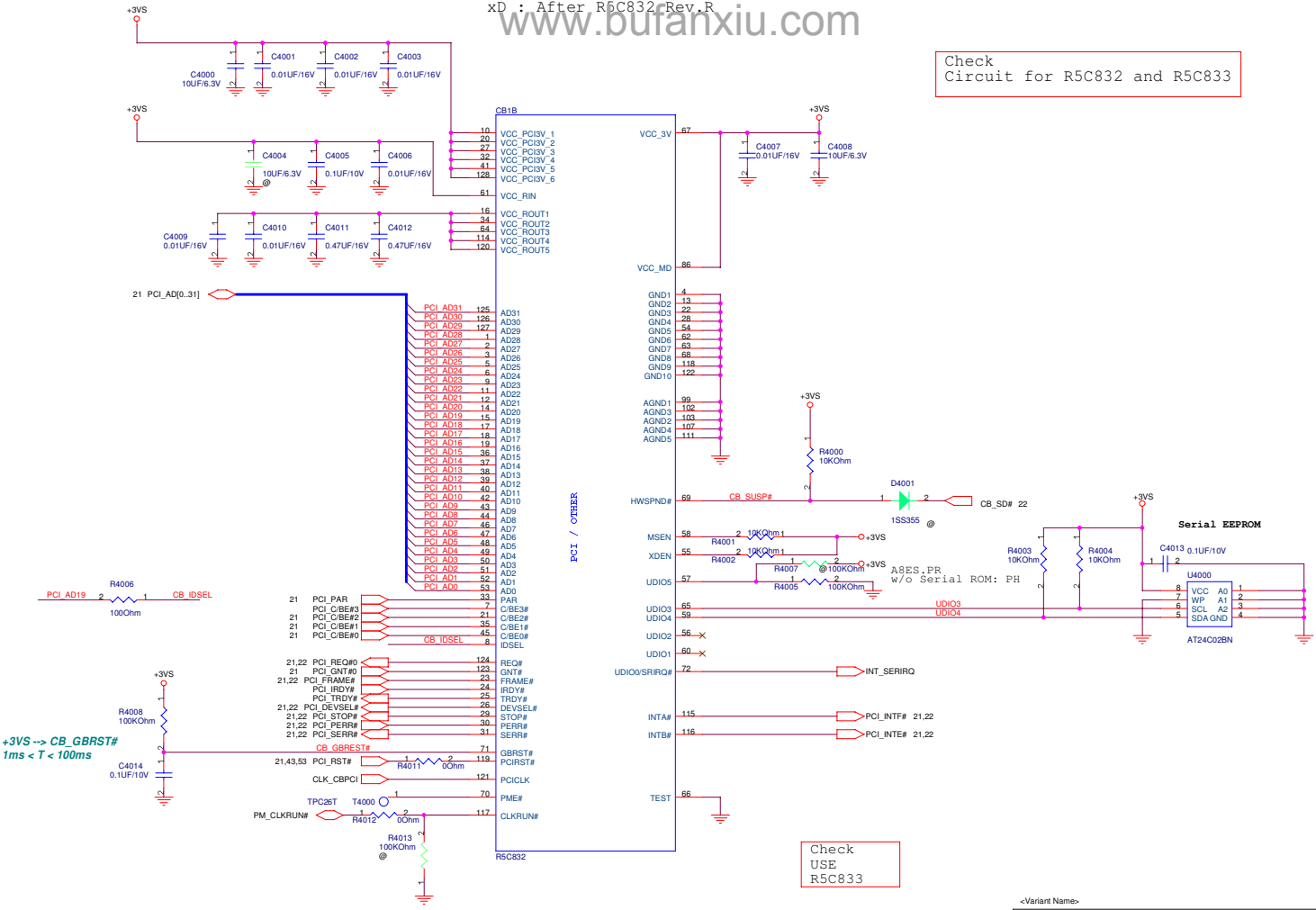


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ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8ES</b>		Rev 0
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Check  
Circuit for R5C832 and R5C833

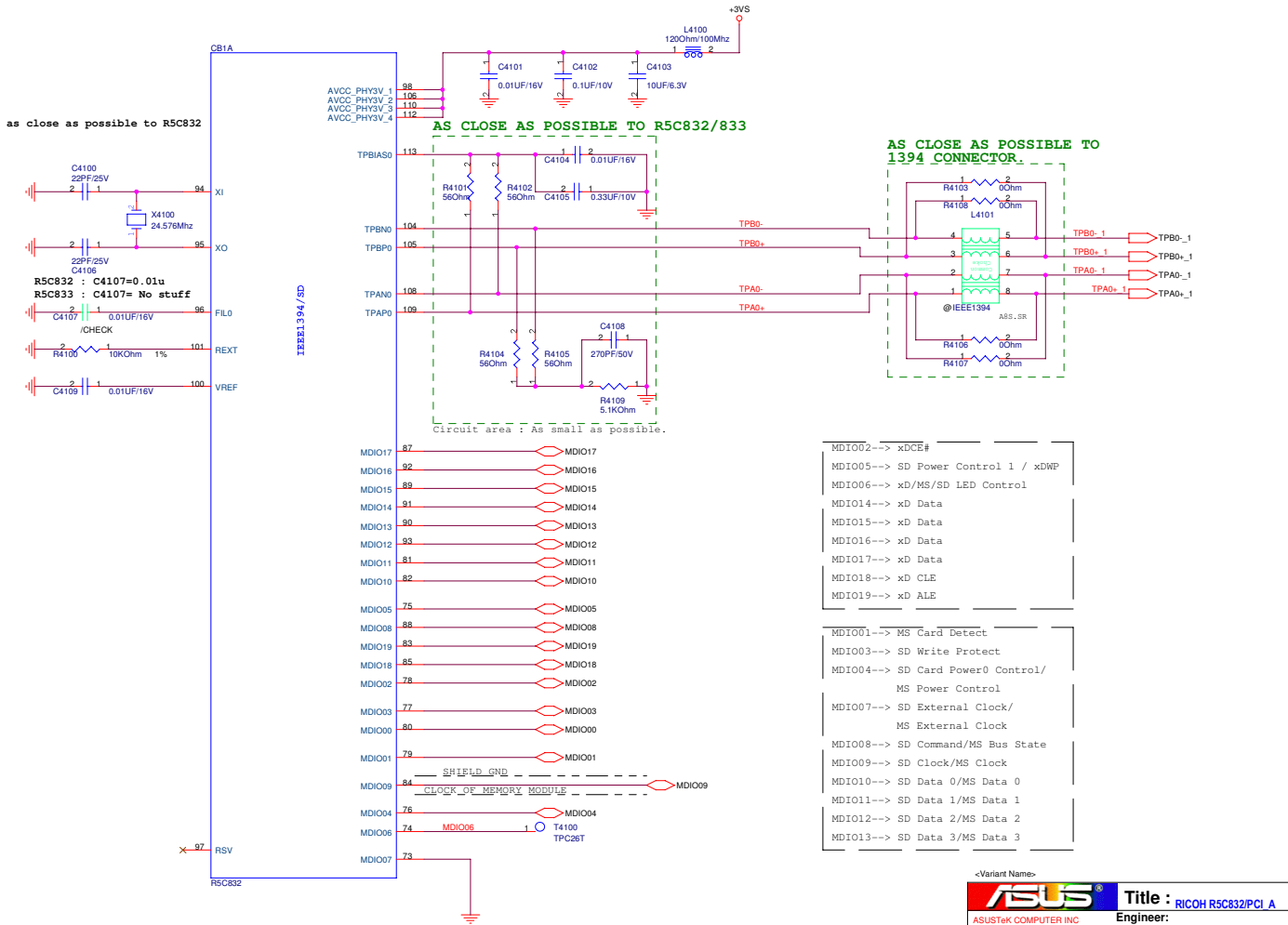


<-Variant Name>

<b>ASUS</b>		<b>Title : RICOH R5C832/PCI B</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	<b>ABES</b>		1.0
Date: 星期日, 7月29, 2007		Sheet: 40	of 94

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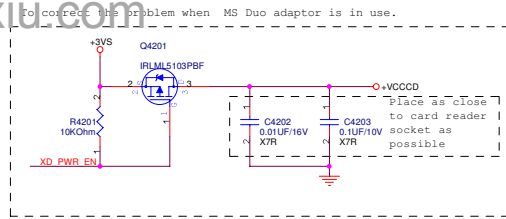
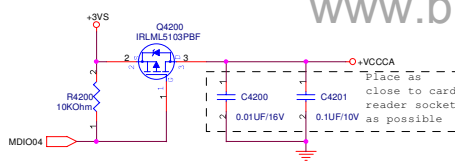
- MDIO17 --- MDIO17
- MDIO16 --- MDIO16
- MDIO15 --- MDIO15
- MDIO14 --- MDIO14
- MDIO13 --- MDIO13
- MDIO12 --- MDIO12
- MDIO11 --- MDIO11
- MDIO10 --- MDIO10
- MDIO08 --- MDIO08
- MDIO07 --- MDIO07
- MDIO06 --- MDIO06
- MDIO05 --- MDIO05
- MDIO04 --- MDIO04
- MDIO03 --- MDIO03
- MDIO02 --- MDIO02
- MDIO01 --- MDIO01
- MDIO09 --- MDIO09
- MDIO08 --- MDIO08
- MDIO07 --- MDIO07
- MDIO06 --- MDIO06
- MDIO05 --- MDIO05
- MDIO04 --- MDIO04
- MDIO03 --- MDIO03
- MDIO02 --- MDIO02
- MDIO01 --- MDIO01

- MDIO02--> xDCE#
  - MDIO05--> SD Power Control 1 / xDWP
  - MDIO06--> xD/MS/SD LED Control
  - MDIO14--> xD Data
  - MDIO15--> xD Data
  - MDIO16--> xD Data
  - MDIO17--> xD Data
  - MDIO18--> xD CLE
  - MDIO19--> xD ALE
- 
- MDIO01--> MS Card Detect
  - MDIO03--> SD Write Protect
  - MDIO04--> SD Card Power0 Control/ MS Power Control
  - MDIO07--> SD External Clock/ MS External Clock
  - MDIO08--> SD Command/MS Bus State
  - MDIO09--> SD Clock/MS Clock
  - MDIO10--> SD Data 0/MS Data 0
  - MDIO11--> SD Data 1/MS Data 1
  - MDIO12--> SD Data 2/MS Data 2
  - MDIO13--> SD Data 3/MS Data 3

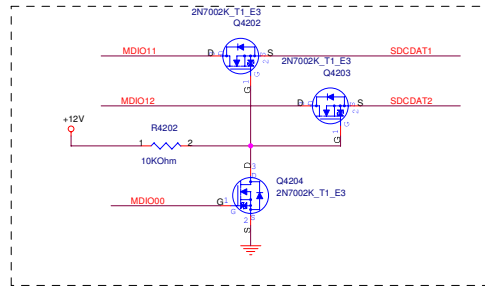
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<b>ASUS</b>		<b>Title : RICOH R5C832/PCI A</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	ABES		1.0
Date: 星期日, 七月 28, 2007	Sheet: 41	of 94	

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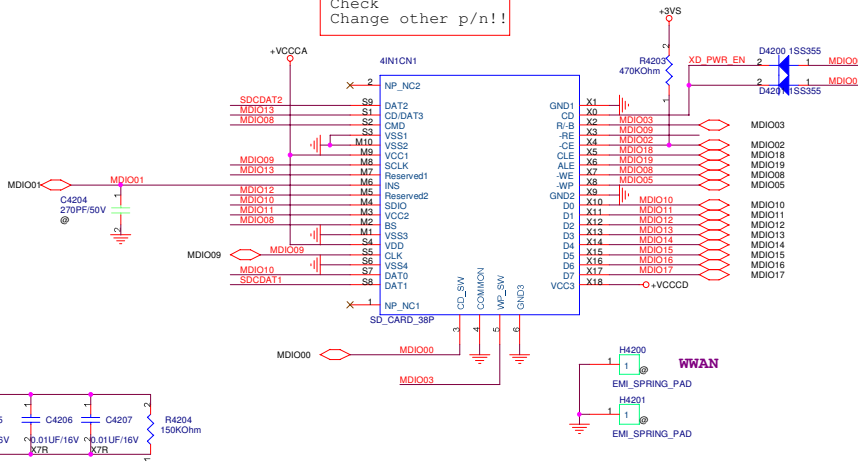
Solve MS Duo Adaptor short issue.



A8ES.PR  
Change to 07G005000214, 2KV ESD

MDIO00	->	SD Card Detect
MDIO01	->	MS Card Detect
MDIO03	->	SD Write Protect
MDIO04	->	SD Card Power0 Control/ MS Power Control
MDIO08	->	SD Command/MS Bus State
MDIO09	->	SD Clock/MS Clock
MDIO10	->	SD Data 0/MS Data 0
MDIO11	->	SD Data 1/MS Data 1
MDIO12	->	SD Data 2/MS Data 2
MDIO13	->	SD Data 3/MS Data 3

Check  
Change other p/n!!

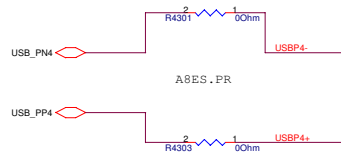
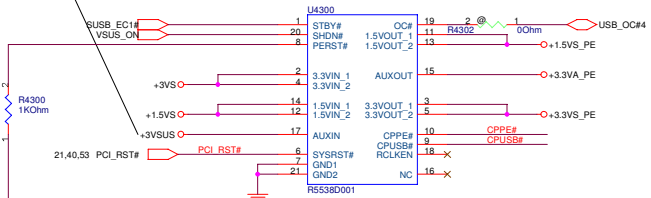


MDIO02	->	xDCE#
MDIO05	->	SD Power Control 1 / xDWP
MDIO06	->	xD/MS/SD LED Control
MDIO14	->	xD Data
MDIO15	->	xD Data
MDIO16	->	xD Data
MDIO17	->	xD Data
MDIO18	->	xD CLE
MDIO19	->	xD ALE

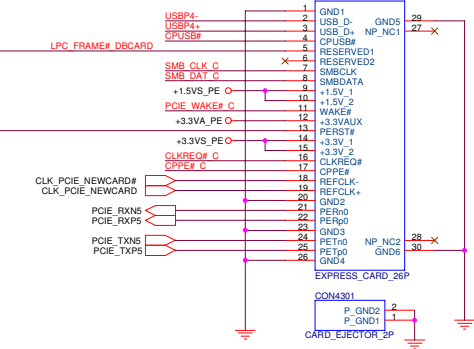
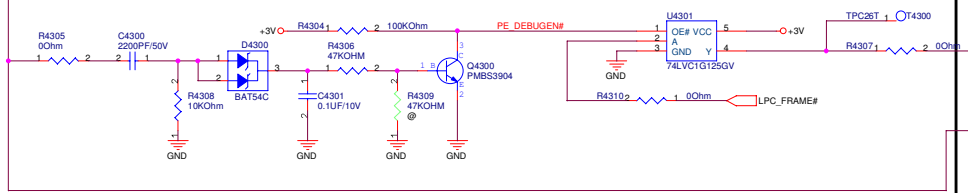
ASUS		Title :	CardReader
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8ES		1.0
Date:	星期二, 六月 29, 2007	Sheet	42 of 94

<< Kennedy\_Zhang >>

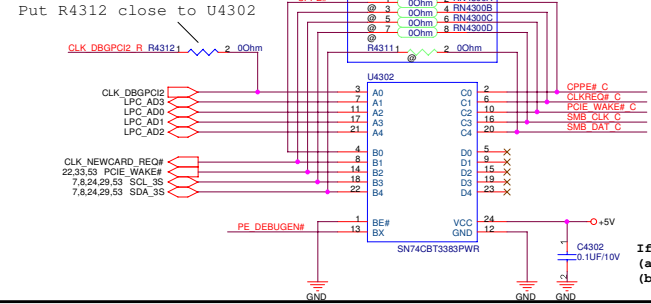
Check +3V



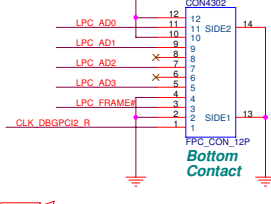
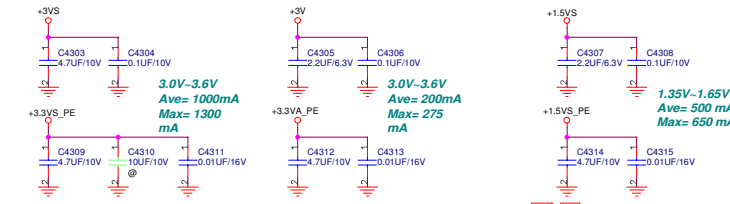
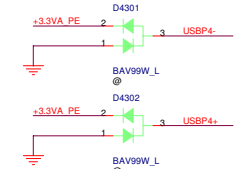
### Block A



### Block C




If don't support NewCard Debug Card, Pls do  
 (a) DNI all components of block A  
 (b) Mount Block C (RN5401, R6975)



ASUS Logo  
**ASUSTeK COMPUTER INC.** Title : Express Card  
 Engineer:  
 Size Project Name  
 Custom **A8ES**  
 Date: 8/10/07, C H 24, 2007 Sheet 43 of 94

<< Kennedy\_Zhang >>

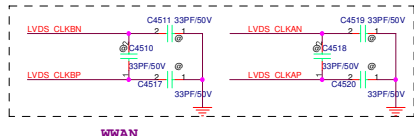
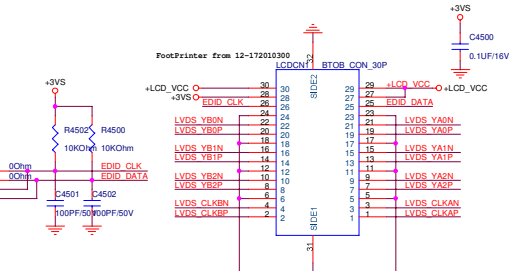
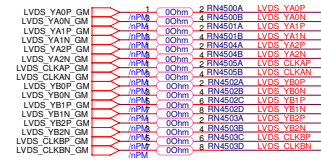
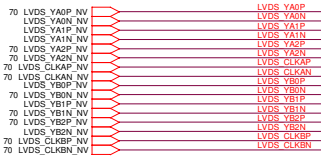


		<b>Title : Blank</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8ES</b>	1.0
Date: 星期三, 十月 11, 2006		Sheet 44 of 94

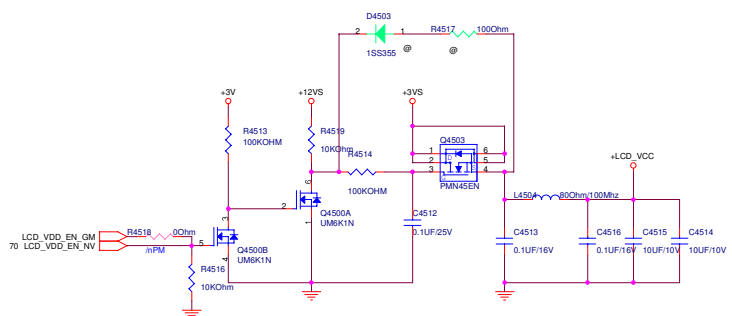
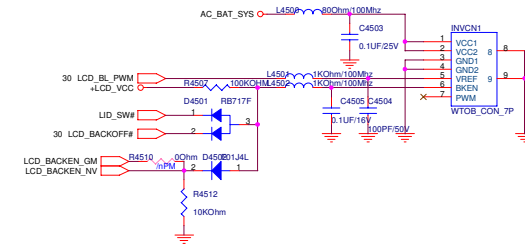
*<< Kennedy\_Zhang >>*

Check stub

+3VS 3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,46,47,49,50,51,53,55,57,62,68,70,80,91,92  
+3VSUS  
+12VS 38,57,70,91

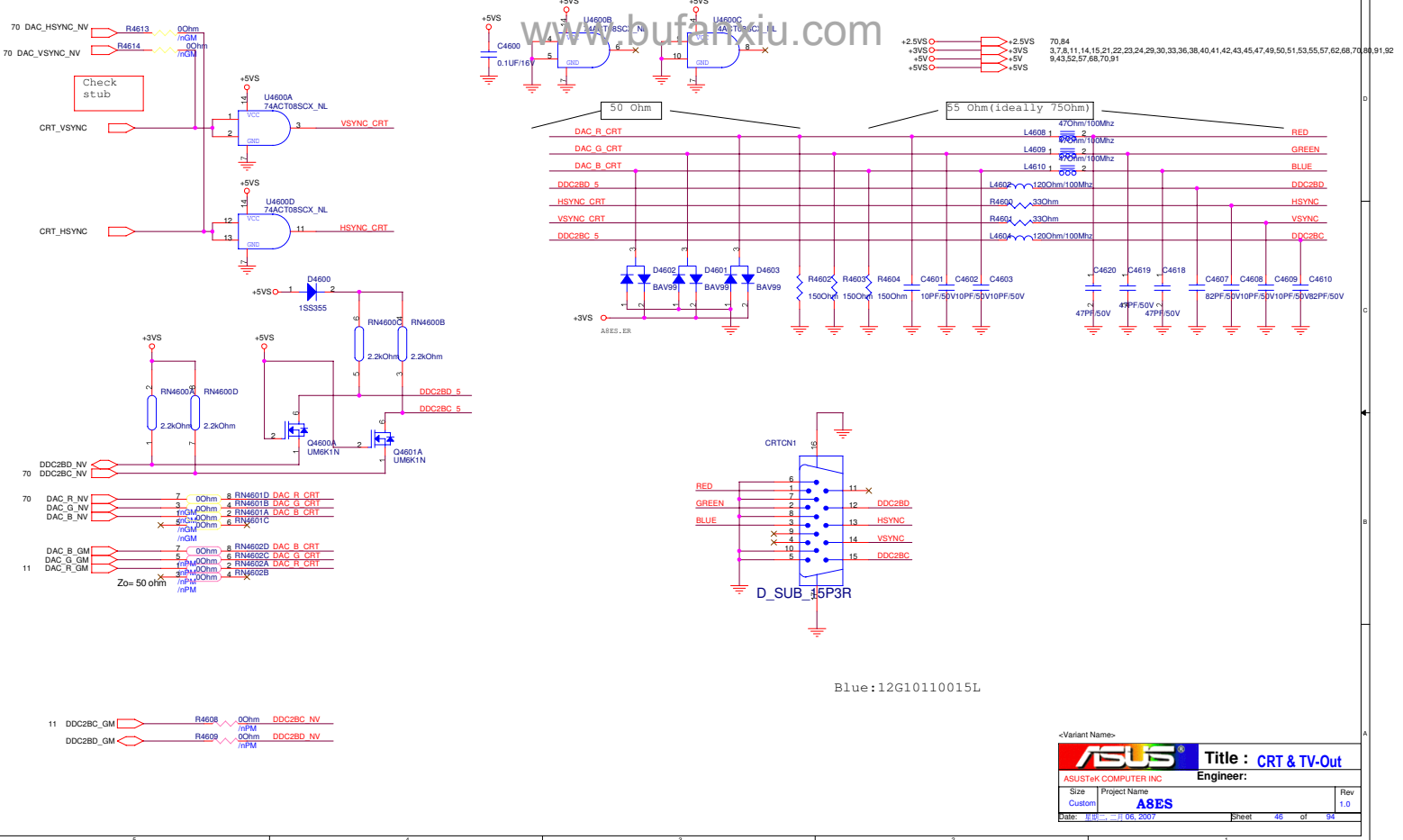


### INVERTOR CNT



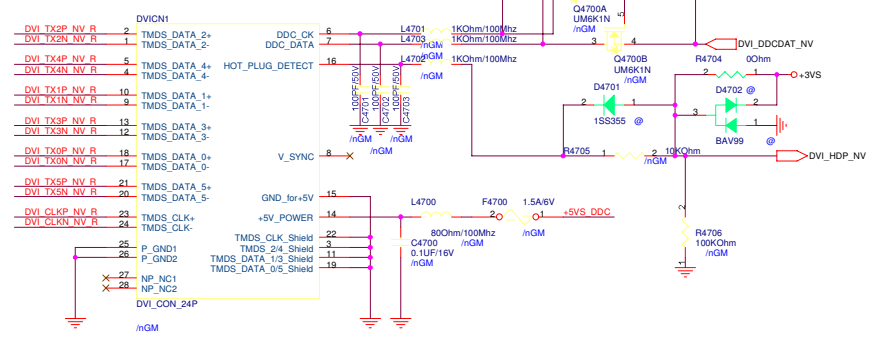
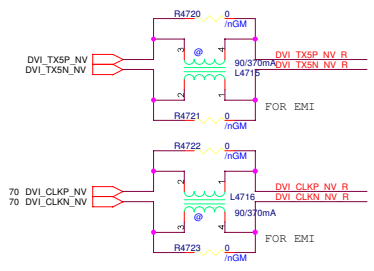
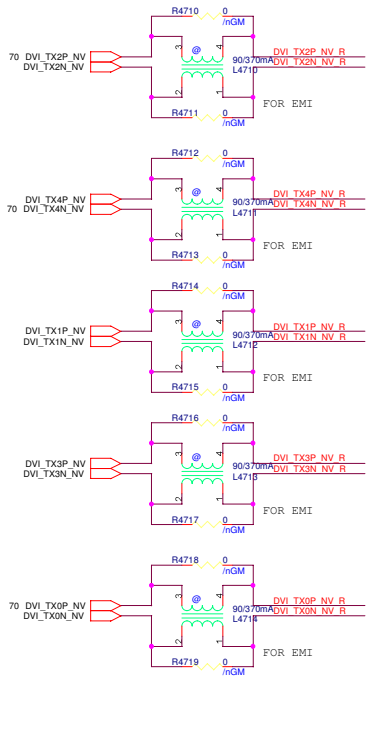
<-Variant Name>  
**ASUS** Title : LVDS & Inverter  
ASUSTeK COMPUTER INC Engineer:  
Size Custom Project Name **ABES** Rev 1.0  
Date: 11/11/04, 2007 Sheet 45 of 94

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<< Kennedy\_Zhang >>

<Variant Name>  
**ASUS** Title : CRT & TV-Out  
 ASUSTek COMPUTER INC Engineer:  
 Size Project Name  
 Custom **ABES** Rev  
 1.0  
 Date: 11/11/08:2007 Sheet 46 of 94



<b>ASUS</b>		<b>Title : DVI</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	ABES	1.0	
Date: 05/11/06 2007	Sheet 47 of 94		

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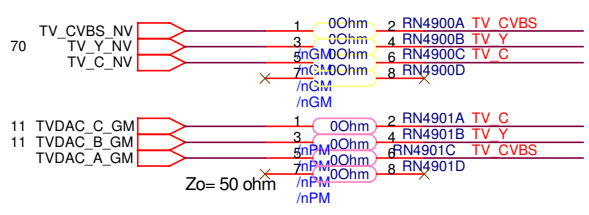
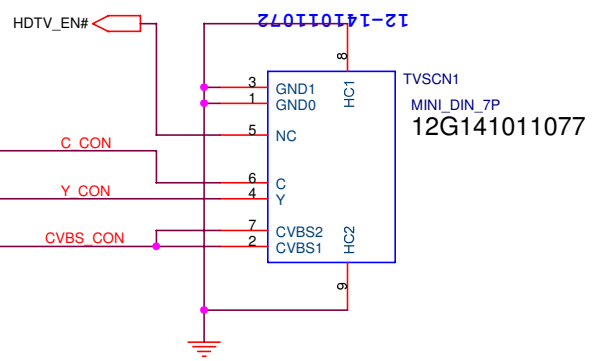
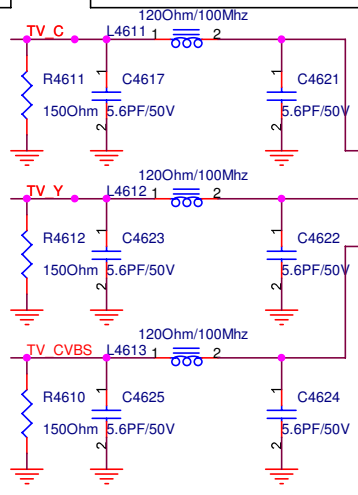
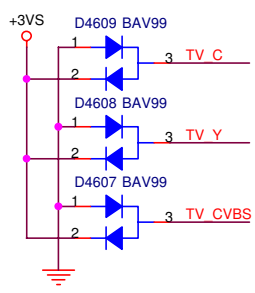
		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size A	Project Name <b>A8ES</b>	Rev 0	
Date: 星期三, 十月 11, 2006		Sheet 48 of 94	

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50 Ohm

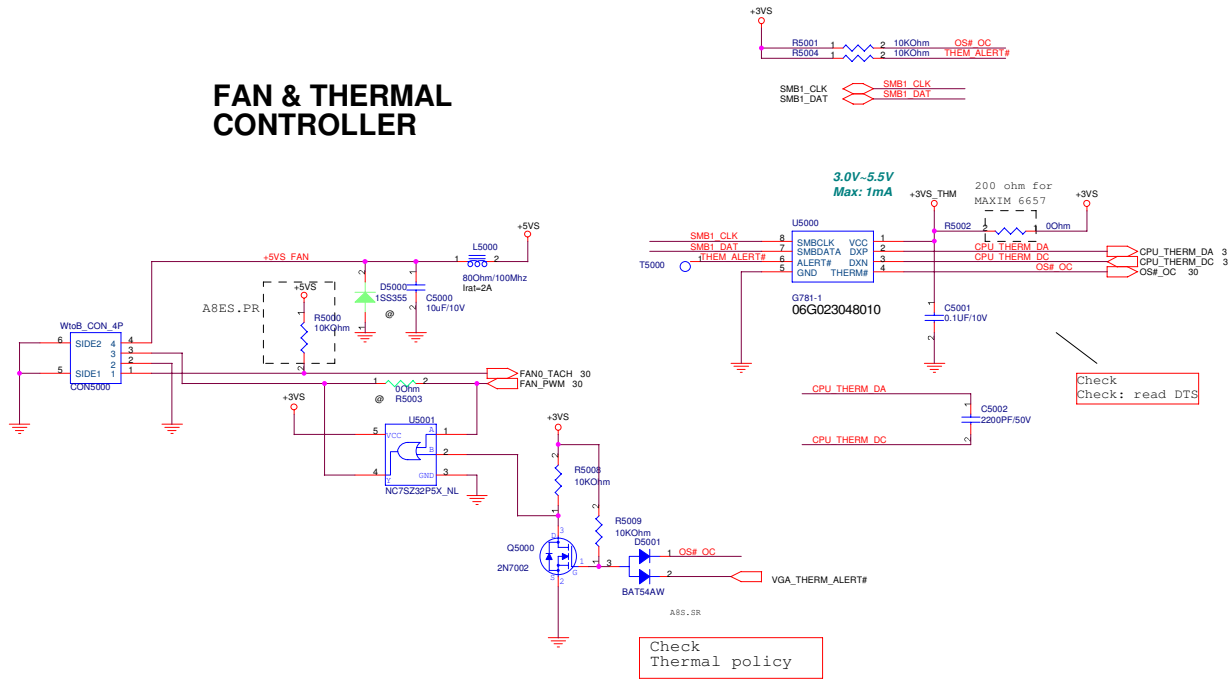
55 Ohm (Ideally 75Ohm)



<b>ASUS</b>		<b>Title : TV</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name <b>ASES</b>	Rev 1.0	
Date: 星期二, 二月 06, 2007		Sheet 49 of 94	

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# FAN & THERMAL CONTROLLER



Check Thermal policy

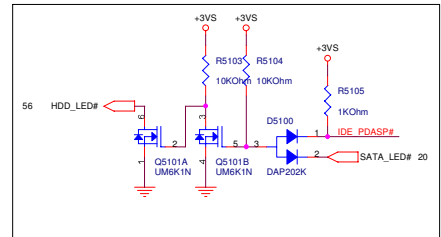
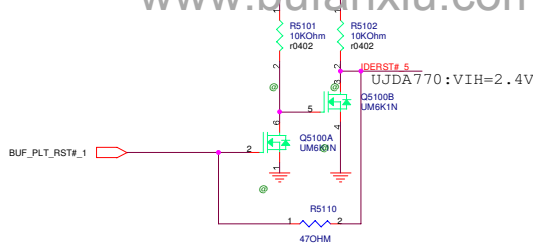
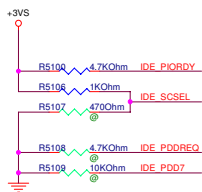
Check  
Check: read DIS

G781-1 (0x9A)  
06G023048010  
G781 (0x98)  
06G023048011

<Variant Name>

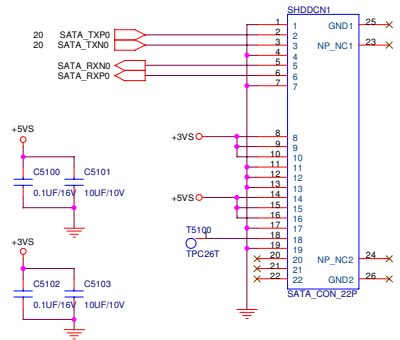
<b>ASUS</b>		<b>Title : FAN &amp; THERMAL</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	ABES		1.0
Date: #B	# 05, 2007	Sheet	50 of 94

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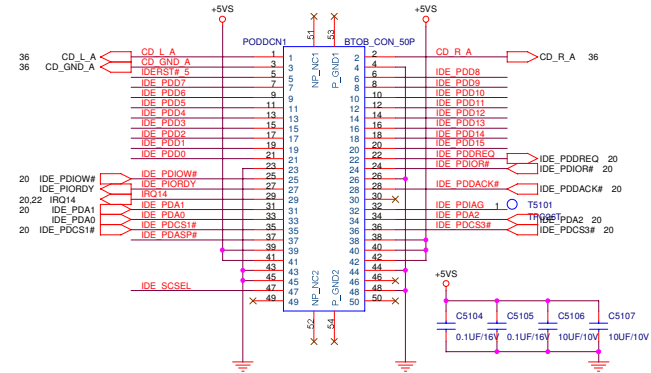


20 IDE\_PDD[0..15] IDE\_PDD0..15

**SATA HDD CON**



**PATA CD-ROM CON**

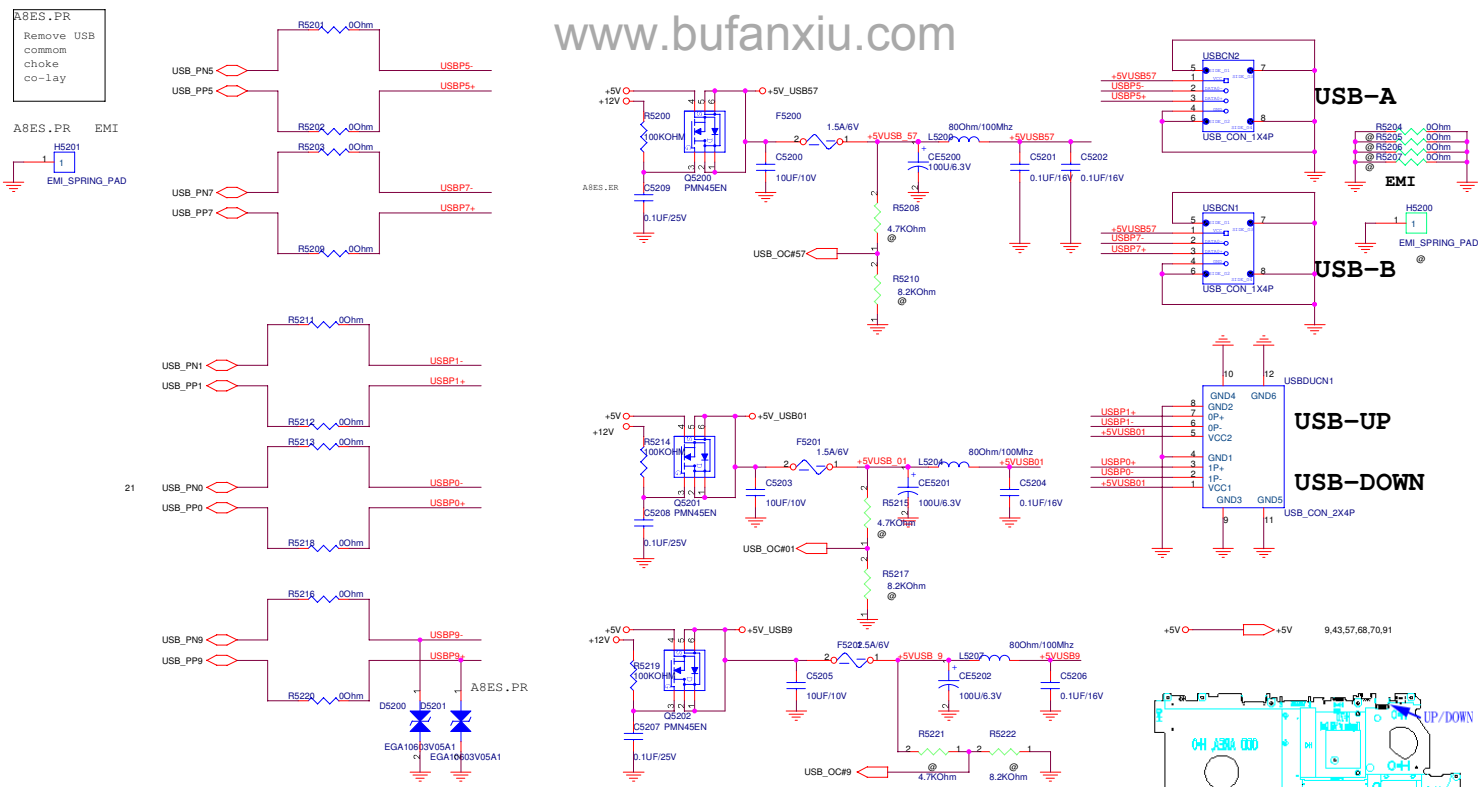


+3VS → +3VS  
 +5VS → +5VS  
 +5V → +5V

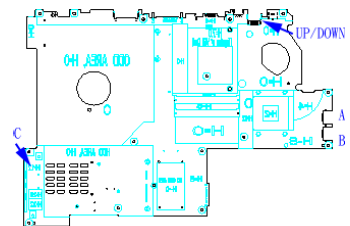
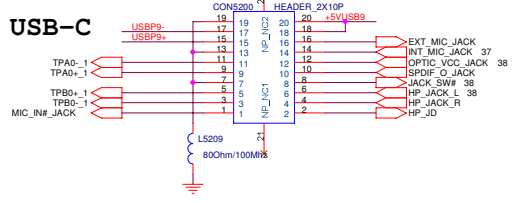
3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92  
 9,43,52,57,68,70,91

<b>ASUS</b>		<b>Title : HDD &amp; ODD</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	ABES	1.0	
Date: 11/06/2007	Sheet 51	of 94	

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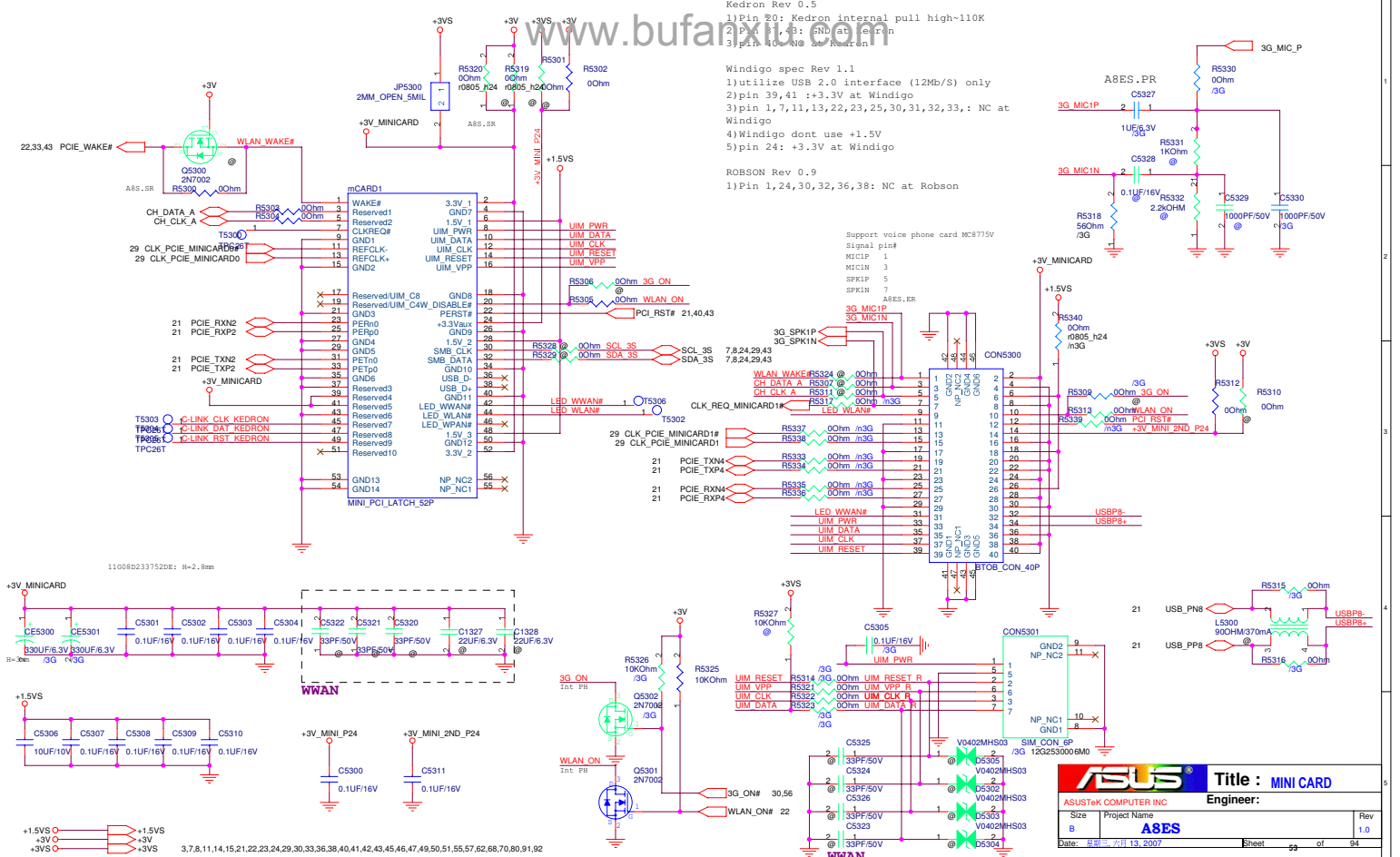


**SUB-PCB: USB/1394/MIC/EARPHONE**



<b>ASUS</b>		<b>Title : USB/SUB PCB</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	<b>ABES</b>		1.0
Date: 2007.08.08		Sheet 62	of 84

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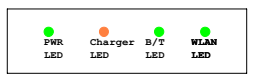
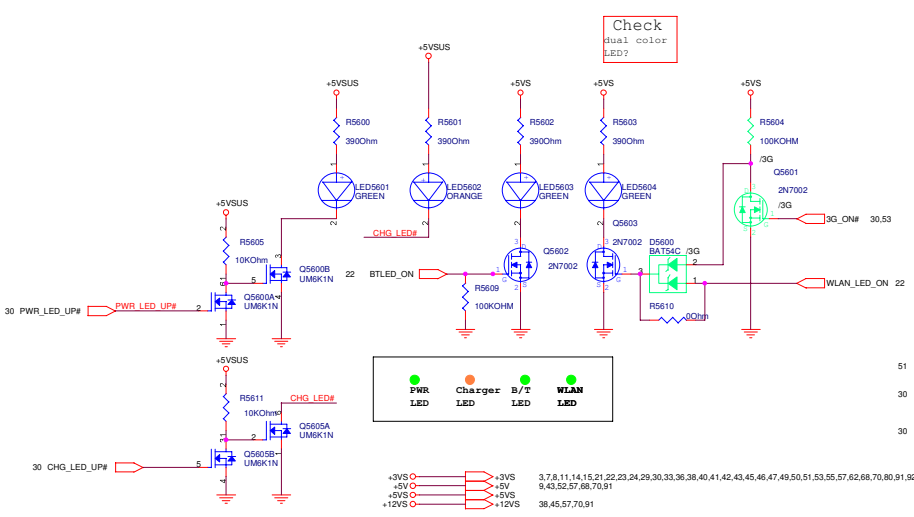
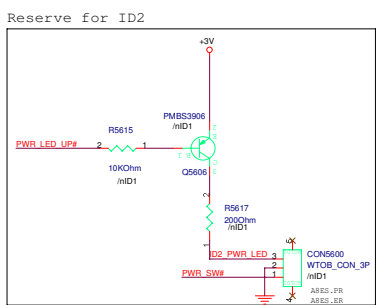
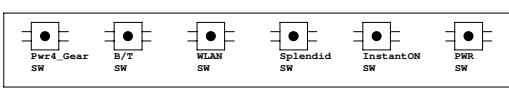
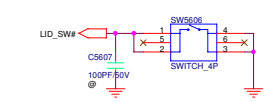
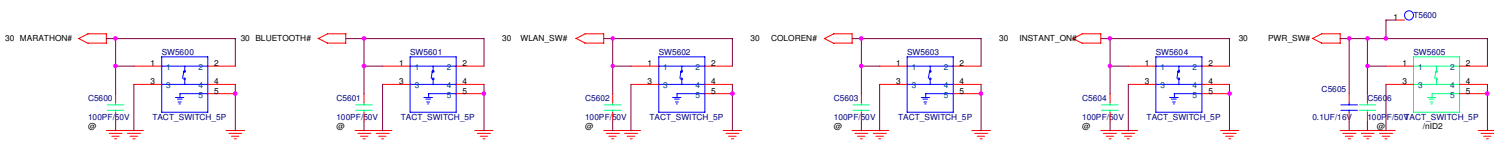
**ASUS** Title : **MINI CARD**  
 ASUSTek COMPUTER INC Engineer:  
 Size Project Name Rev  
 Date: 2007.06.13 A8ES Sheet 59 of 94

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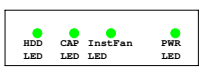
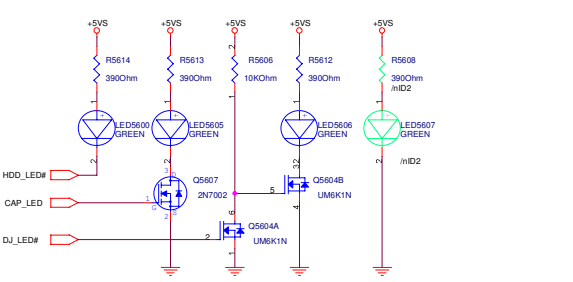
		Title : BLANK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABES	0	
Date: 2011-11-2008		Sheet 54 of 54	

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+3VS	+3VS	3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,51,53,55,57,62,68,70,80,91,92
+5V	+5V	9,43,52,57,68,70,91
+9VS	+9VS	
+12VS	+12VS	38,45,57,70,91



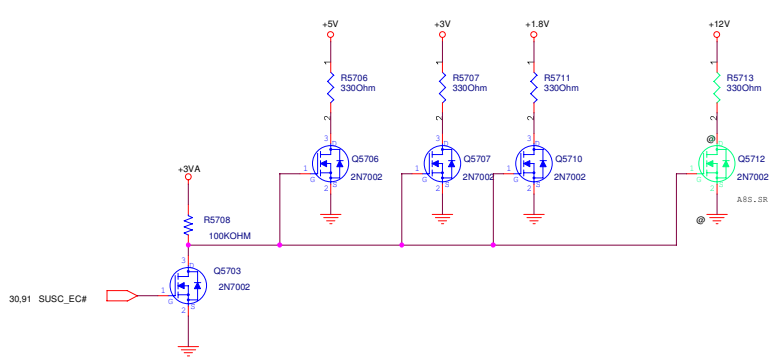
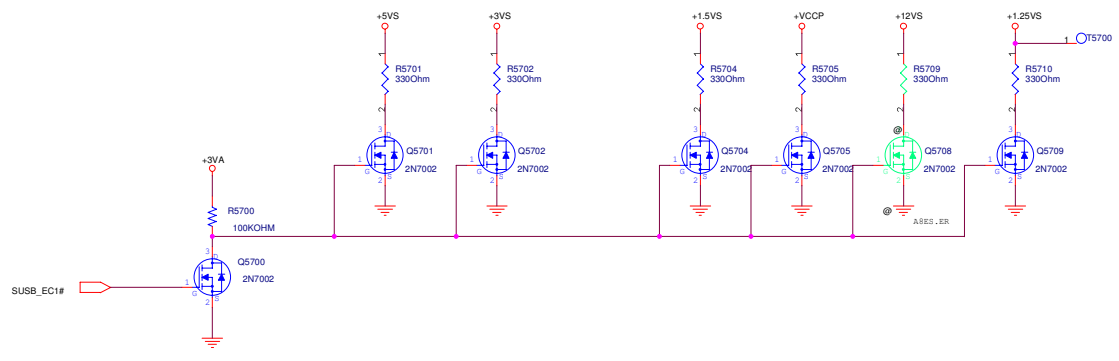
<b>ASUS</b>		<b>Title : LED/instant key</b>	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABES	1.0	
Date: 2007.11.24.2007		Sheet	56 of 84

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# Discharge Circuit

www.bufanxiu.com




<Variant Name>

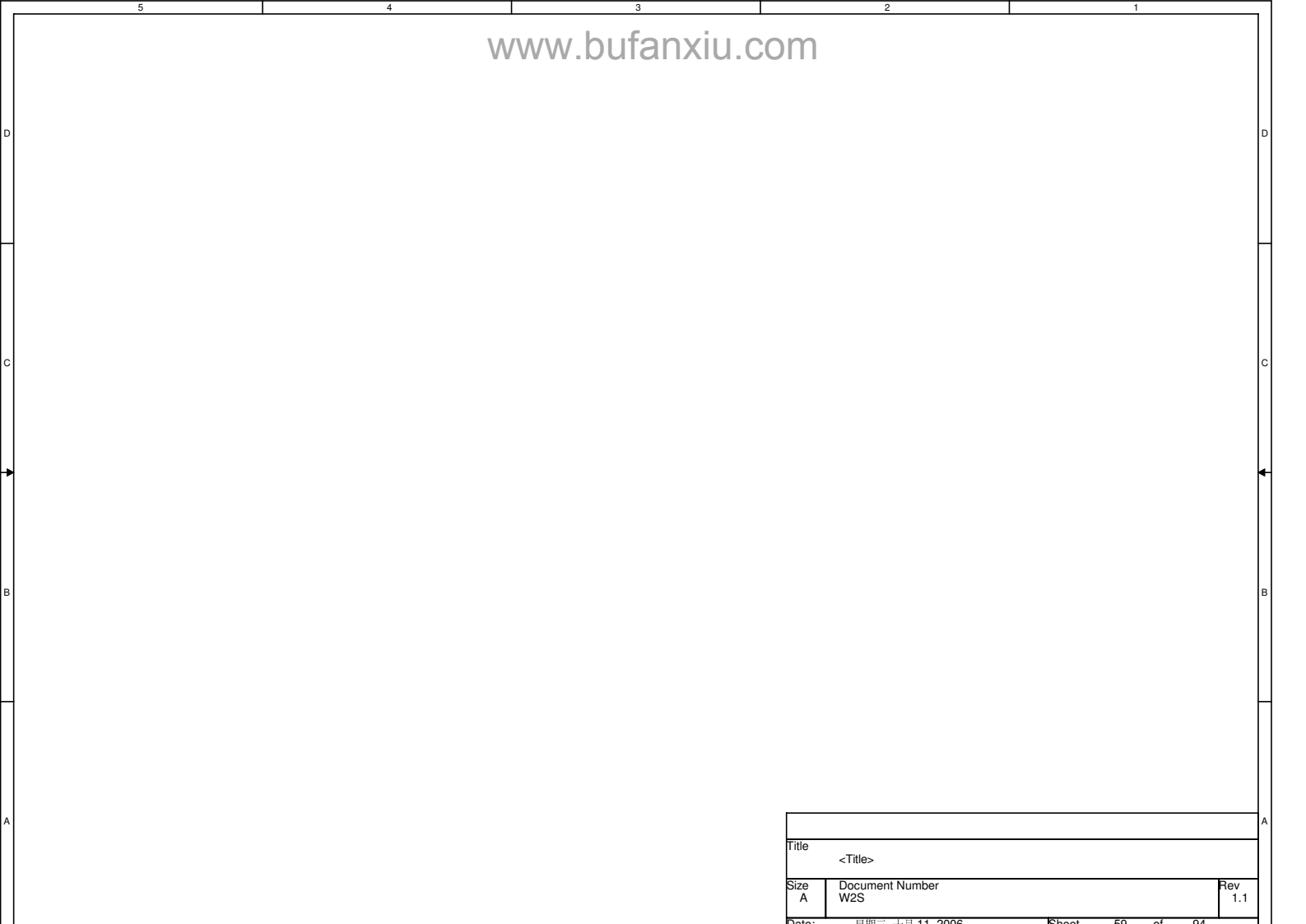
<b>ASUS</b>		<b>Title : Discharge</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size B	Project Name <b>A8ES</b>	Rev 1.0
Date: #SI... 11 06 2007	Sheet 57	of 94

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<Variant Name>

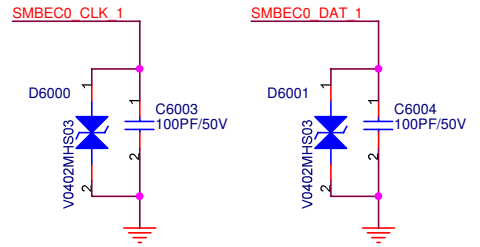
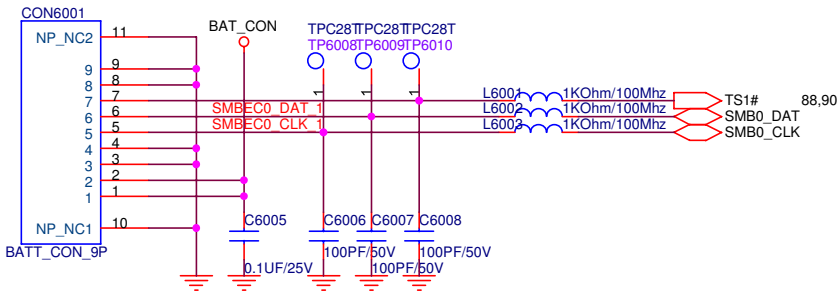
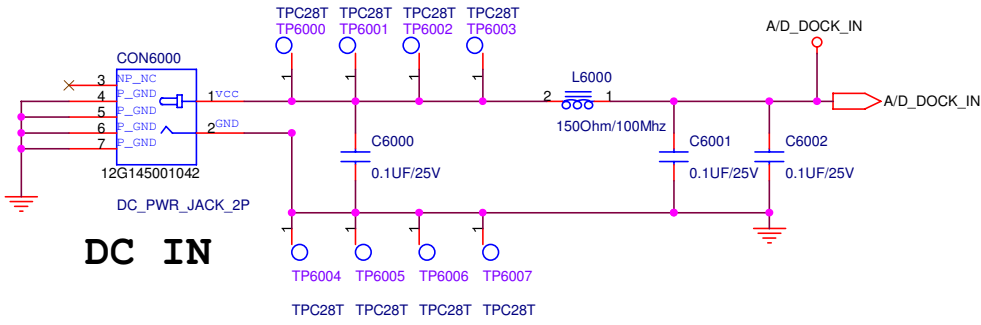
		<b>Title :</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 1.0
Date: 星期三, 十月 11, 2006		Sheet of 94

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Title		
<Title>		
Size	Document Number	Rev
A	W2S	1.1
Date:	星期三, 十月 11, 2006	Sheet 59 of 94

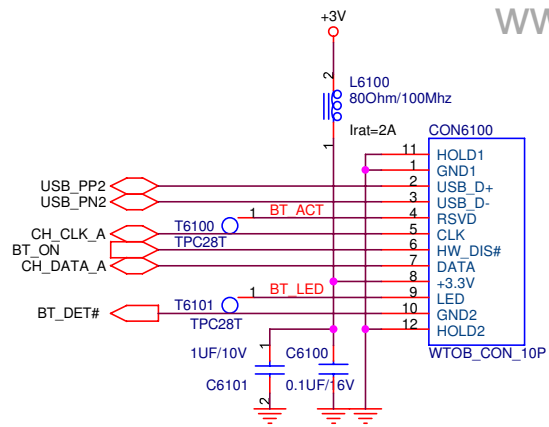
<< Kennedy\_Zhang >>



<Variant Name>

<b>ASUS</b>		<b>Title : DC IN / BAT</b>
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name <b>A8ES</b>	Rev 1.0
Date: 星期四, 五月 24, 2007		Sheet 60 of 94

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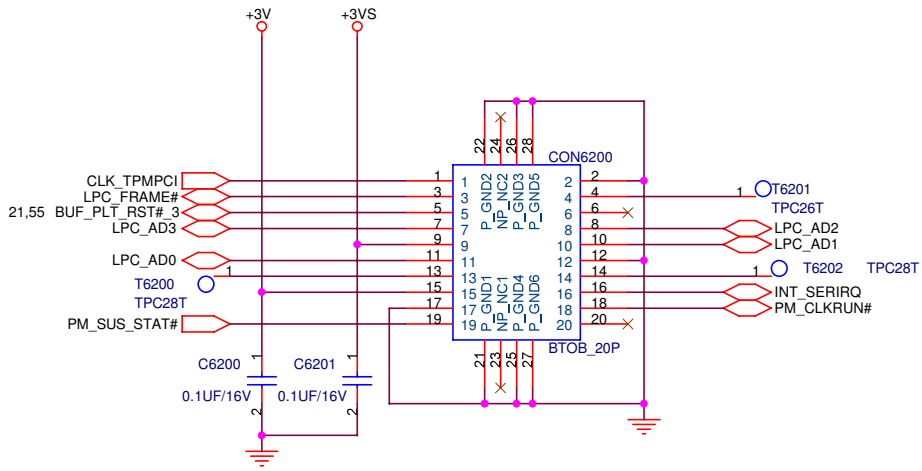


## Bluetooth Module CON

<b>ASUS</b>		<b>Title :BT/CAMERA</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size	Project Name	Rev
A	<b>A8ES</b>	1.0
Date: 星期二, 三月 06, 2007		Sheet 61 of 94

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# TPM 1.2 Module



<Variant Name>

		<b>Title :TPM</b>
ASUSTeK COMPUTER INC		<b>Engineer:</b>
Size A	Project Name <b>A8ES</b>	Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet 62 of 94

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		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
A	<b>A8ES</b>	0	
Date: 星期三, 十月 11, 2006		Sheet	63 of 94

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PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 ( Internal )		
CARDBUS	AD19	0	F,E

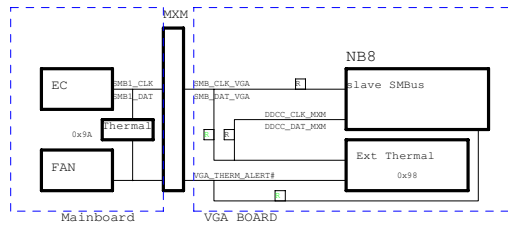
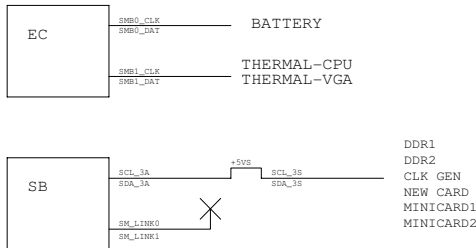
```
nGM:yellow
nPM:light red
=====
@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance
3G :For Windigo,SIERRA MC8775V
nA8E :no stuff Irda for A8E
```

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Support ID2:  
 Support ID2:  
 page 68,Finger print  
 page 55,IR  
 Page 56,pwr switch and LED

Thermal Sensor (CPU)  
 SM-Bus Mapping 1001100

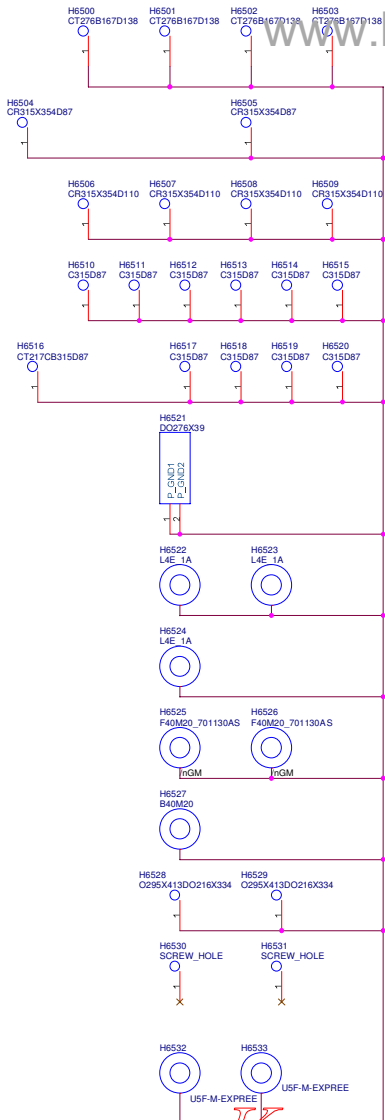
Thermal block diagram



<Variant Name>		Title :	
ASUS		ASUSTeK COMPUTER INC	
Size	Project Name	Engineer:	
B	A8ES		
Date: #B	# 05, 2007	Sheet	64 of 94

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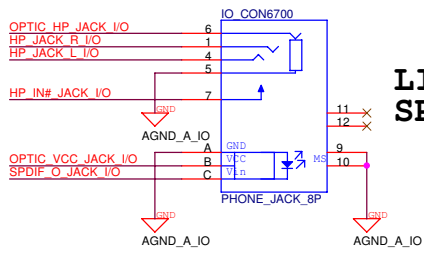


« Kennedy Zhang »

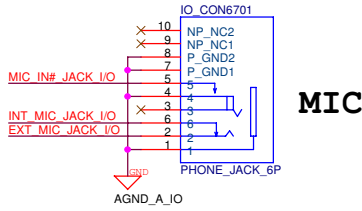
File	<Title>	Rev
Sheet	Document Number	1.1
Date	26, 2005	Sheet 65 of 94

		Title : BLANK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	ABES	0	
Date: 11/11/2006		Sheet 66 of 94	

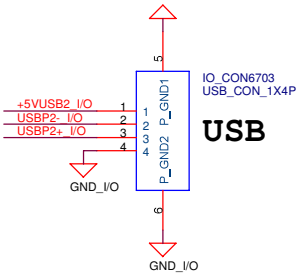
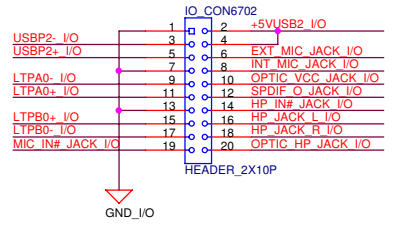
<< Kennedy\_Zhang >>



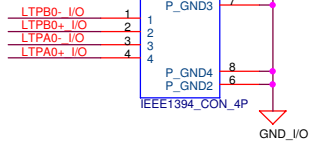
### LINE\_OUT SPDIF



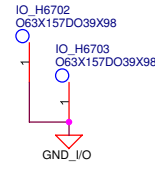
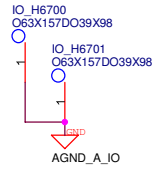
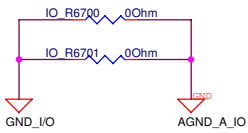
### MIC



### USB



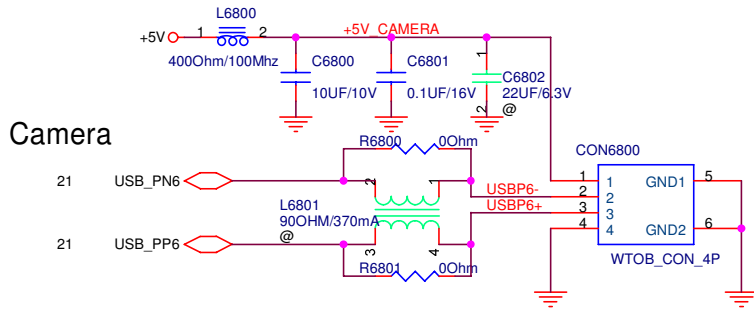
### 1394A



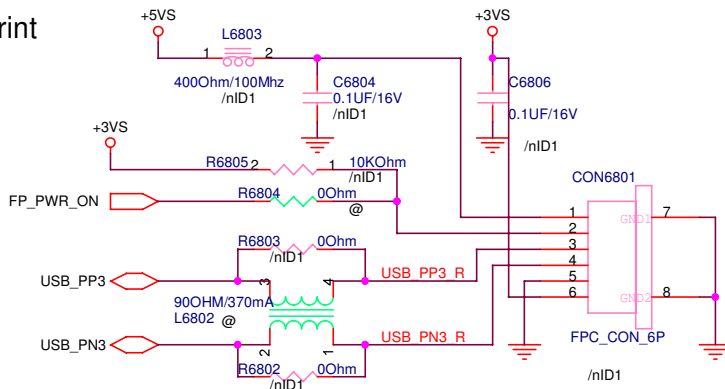
<Variant Name>

<b>ASUS</b>		<b>Title :SUB_PCB</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name <b>ABES</b>	Rev 1.0	
Date: 星期二, 2007年1月30日		Sheet 67 of 94	

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### Finger Print



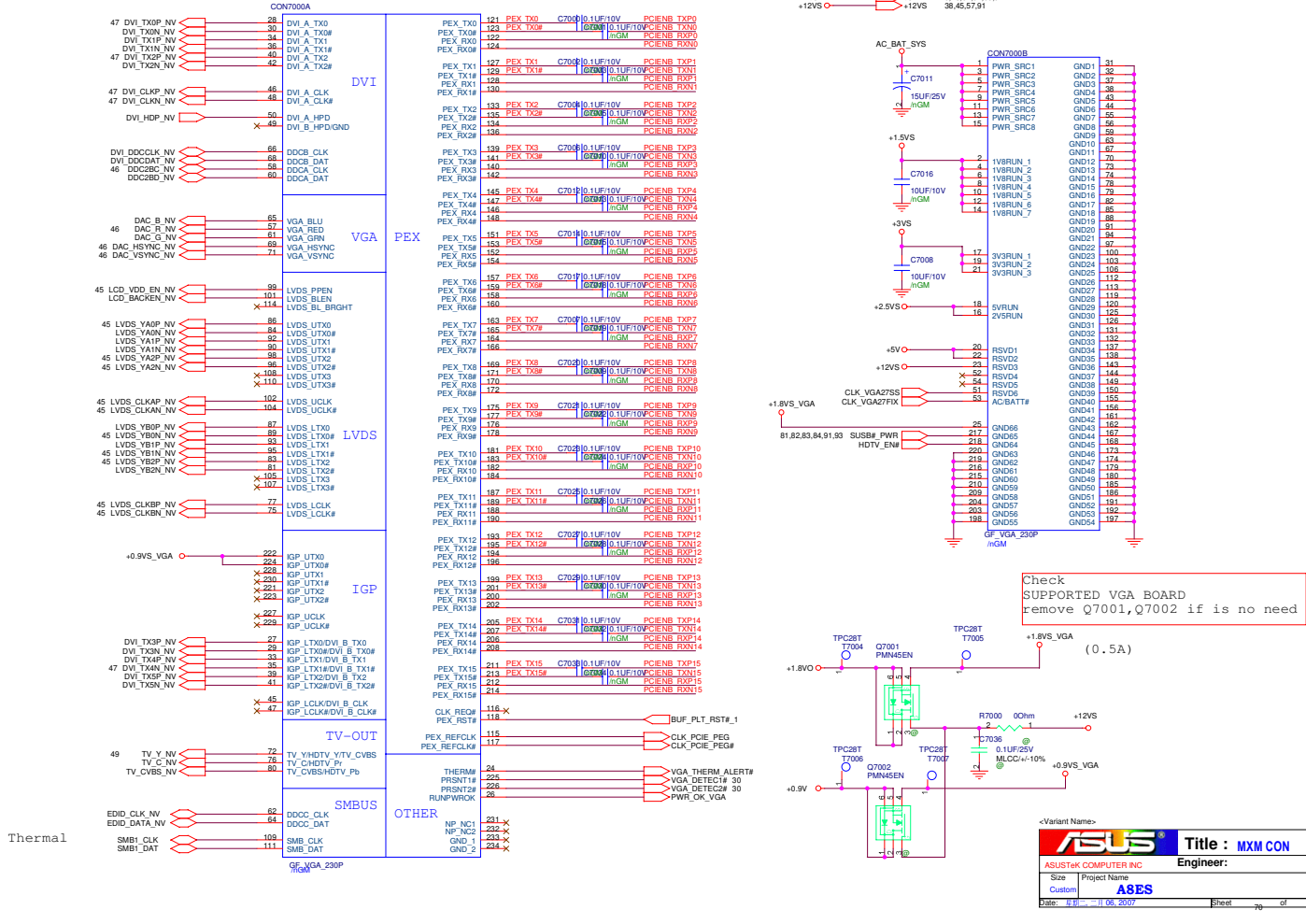
<Variant Name>

<b>ASUS</b>		<b>Title : CAMERA/FingerPrinter</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A	<b>A8ES</b>	1.0	
Date: 星期三, 六月 13, 2007		Sheet	60 of 94

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		<b>Title : BLANK</b>	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name		Rev
A	<b>A8ES</b>		0
Date: 星期三, 十月 11, 2006		Sheet	69 of 94

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D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 71 of 94

D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 72 of 94



D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 73 of 94

D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11, 2006	Sheet 74 of 94

D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 75 of 94

D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 76 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< Kennedy\_Zhang >>

Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date	日期: 11/11/2006	Sheet 77 of 94

		<b>Title : BLANK</b>	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	<b>A8ES</b>	0	
Date: 2006-11-11		Sheet 78 of 94	

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W2S

Change Note:

EE :

1. 965PM pin defined modification, C48/D47/BJ29/BE24 from RSVD pin to LVDSA\_DATA#\_3 / LVDSA\_DATA\_3 / SA\_MA\_14 / SB\_MA\_14
2. CE46 / CE25 --> 11G08D210791
3. Rst button circuit
4. BT\_SW pull-high to different plane issue.
5. Remove RN3104
6. VTT\_REF reserve in S3.
7. VTT stop in S3.
8. CIR PME# function.

Layout :

1. CPU side, per GND pin within per Via, don't share vias.
2. 0.9V\_VTT\_REF trace width.
3. single end trace width more than 3.5mil

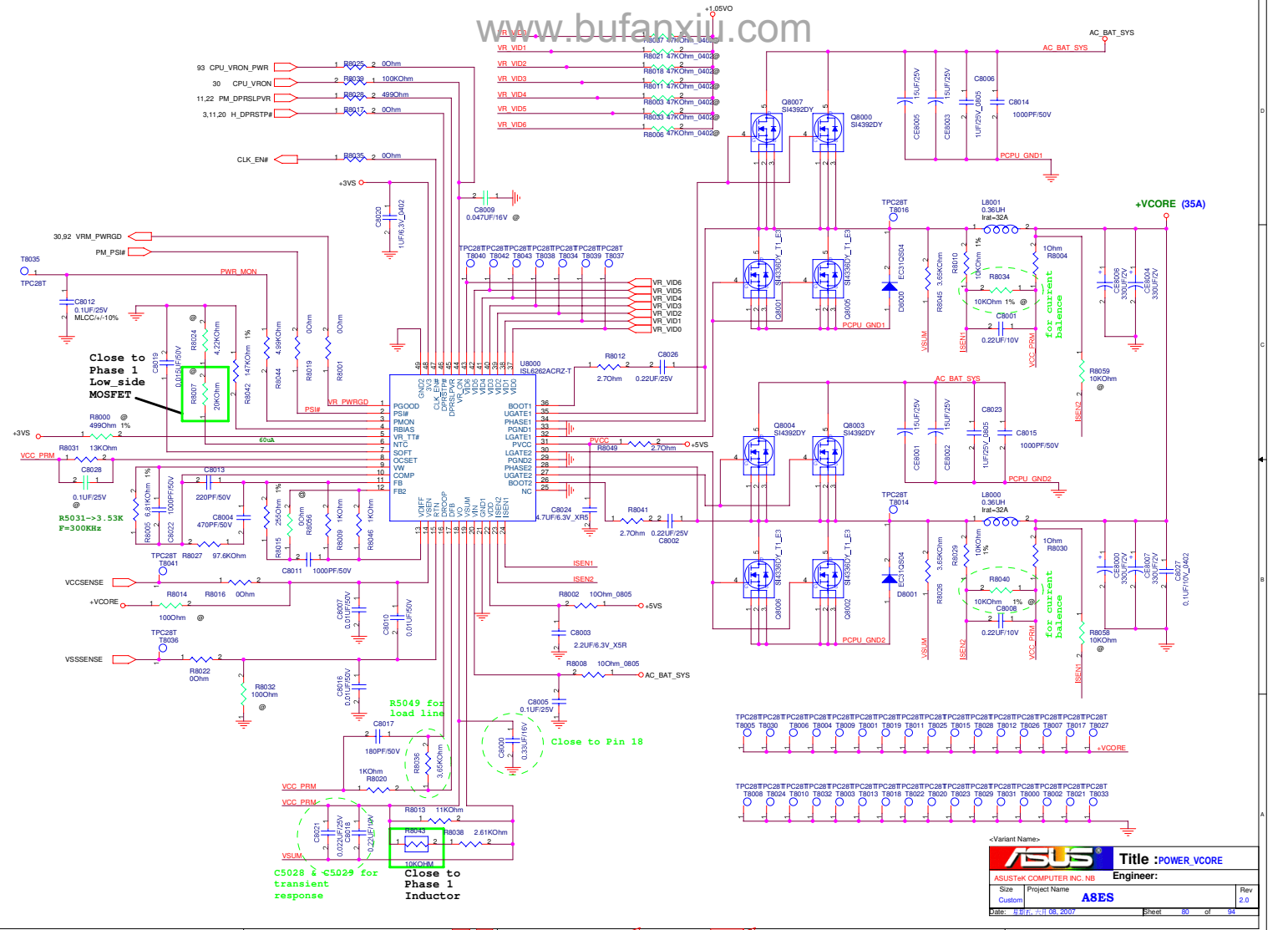
SMT :

1. 開鑄板JP1, JP2

<Variant Name>

		Title : History	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8ES		1.0
Date: 星期三, 十月 11, 2006		Sheet 79	of 94

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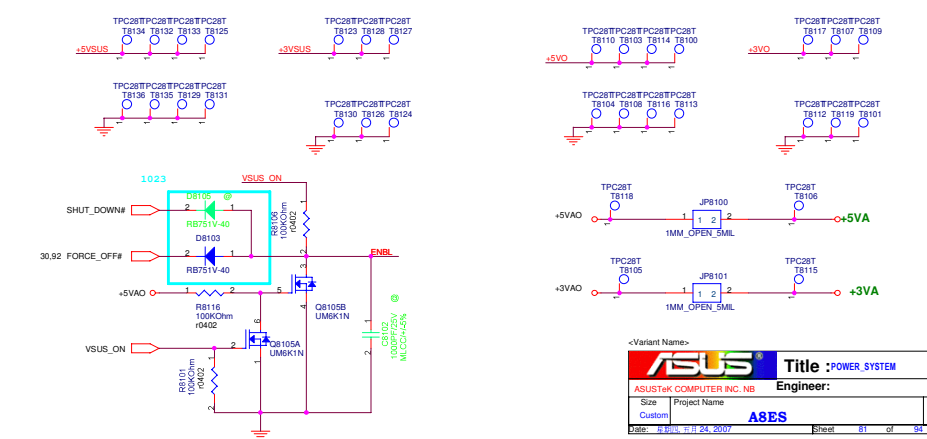
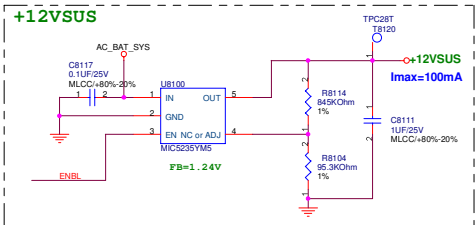
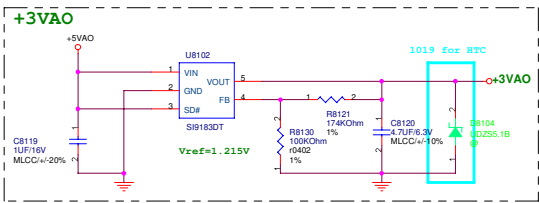
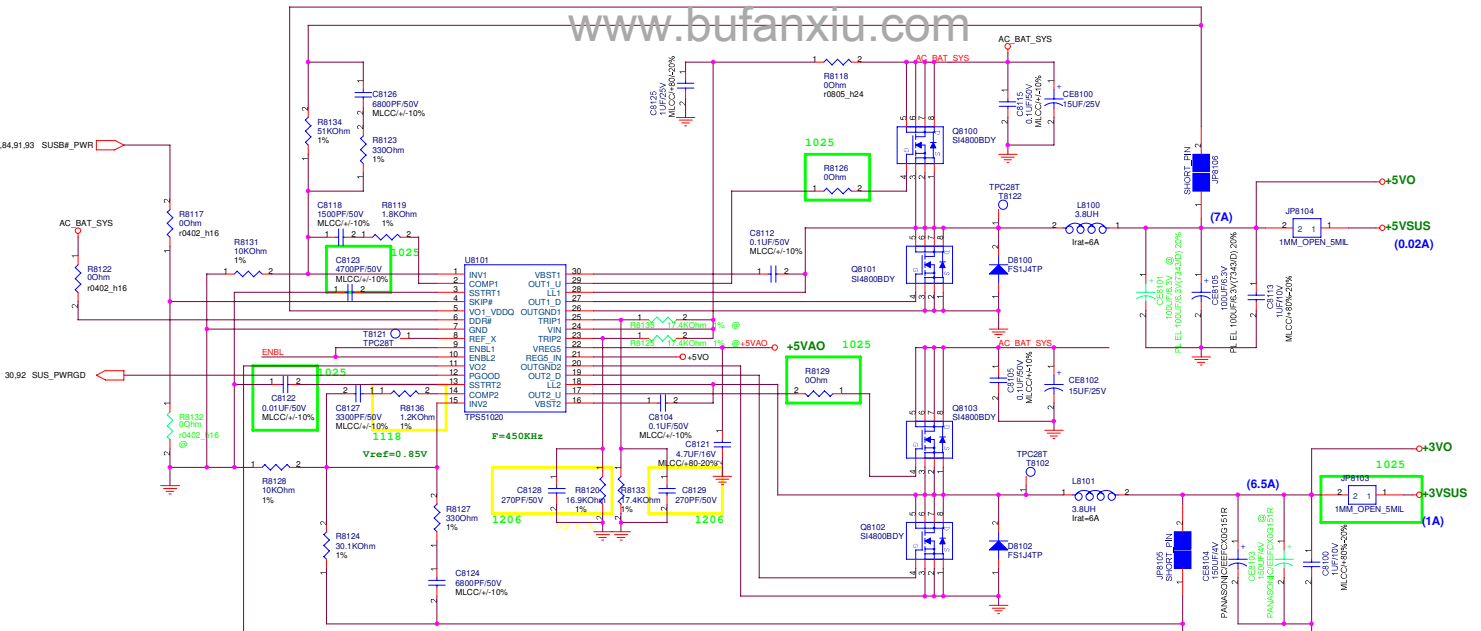


<Variant Names>

<b>ASUS</b>		<b>Title :POWER_VCORE</b>	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	A8ES	
Custom			
Date: 11/17/11 09:20:07	Sheet	80	of 94

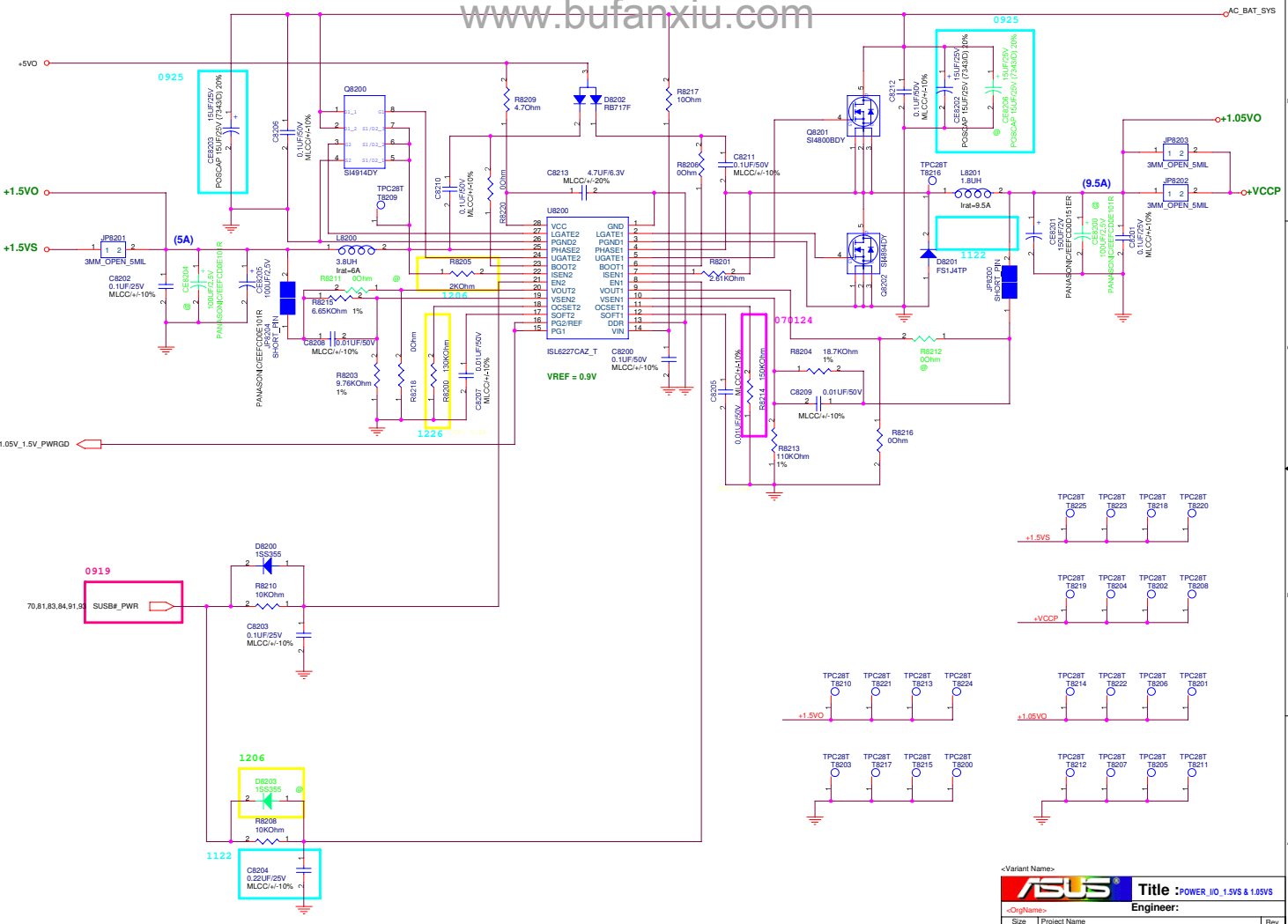
<< Kennedy\_Zhang >>





ASUS		Title :POWER_SYSTEM	
ASUSTeK COMPUTER INC. NB		Engineer:	
Size	Project Name	Rev	
Custom	ABES	2.0	
Date: 2007.01.24		Sheet	81 of 94

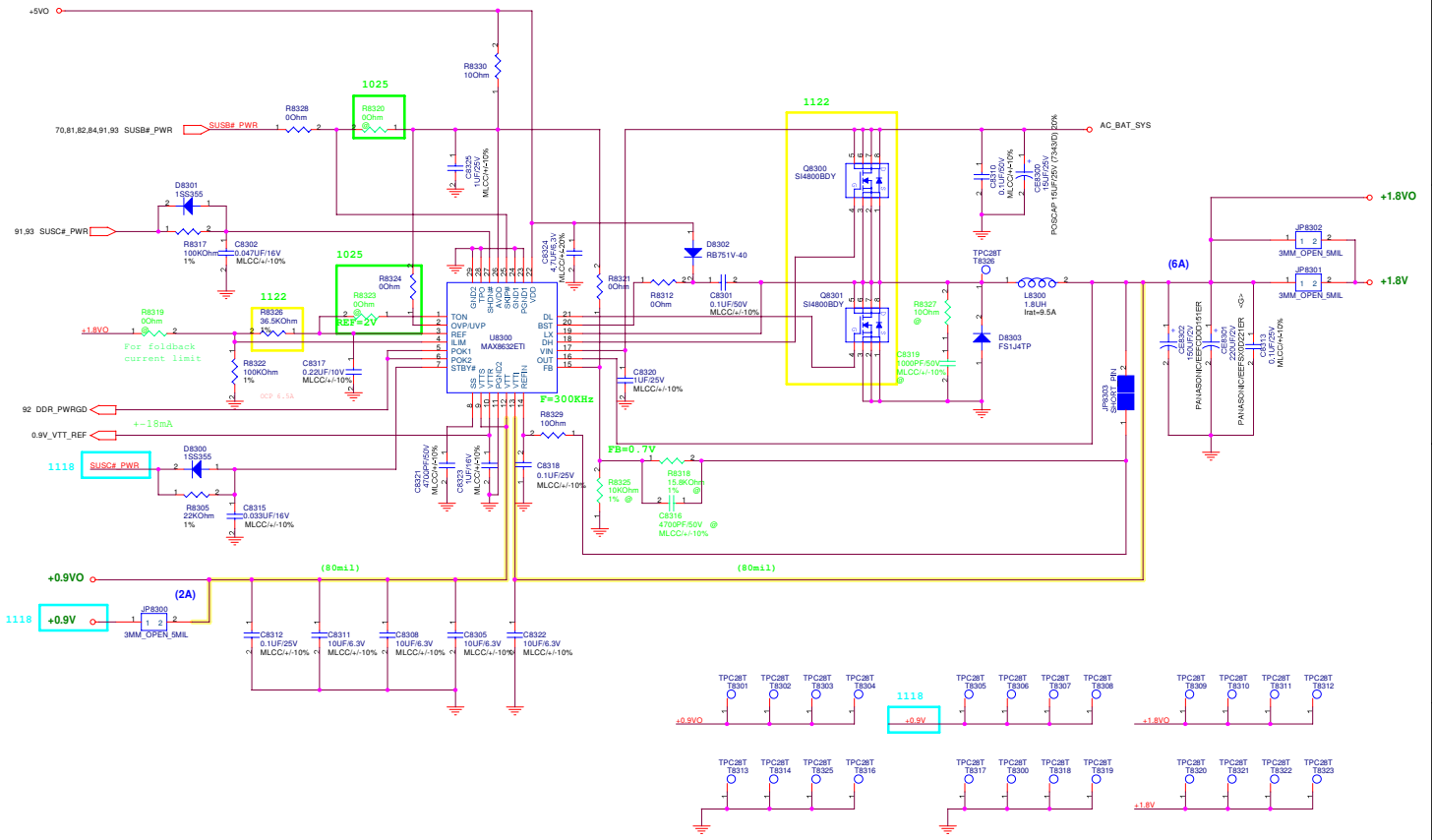
<< Kennedy\_Zhang >>



<Variant Name>

ASUS		Title :POWER_IIO_1.5VS & 1.9VS
Engineer:		
Size	Project Name	Rev
Custom	ABES	2.0
Date: 11/11/2007	Sheet	82 of 94

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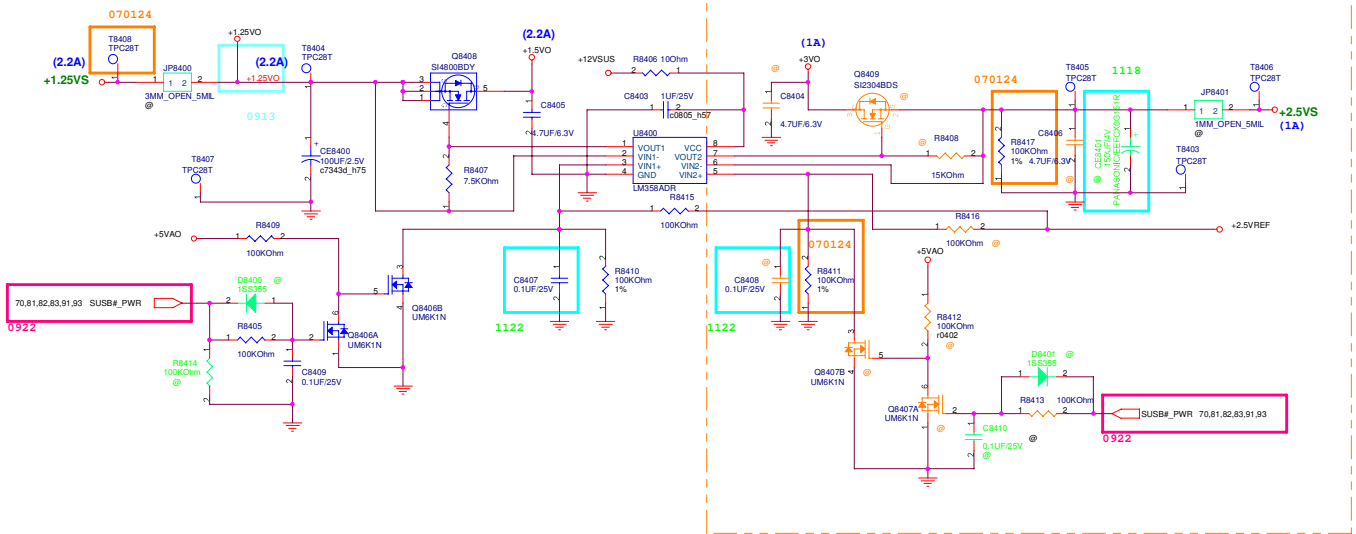


< Variant Name >

<b>ASUS</b>		<b>Title :POWER_IO_DDR &amp; VTT</b>
ASUS Tak COMPUTER INC. NB		Engineer:
Size	Project Name	Rev
Custom	<b>A8ES</b>	2.0
Date: 3/10/11 09:20:07	Sheet	83 of 94

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+1.25VS & +2.5VS



ASUS Title : POWER\_IO\_+3VA & +2.5V  
Engineer:  
Date: 06/06/2007 Sheet 84 of 84

Size	Project Name	Rev
Custom	ABES	2.0

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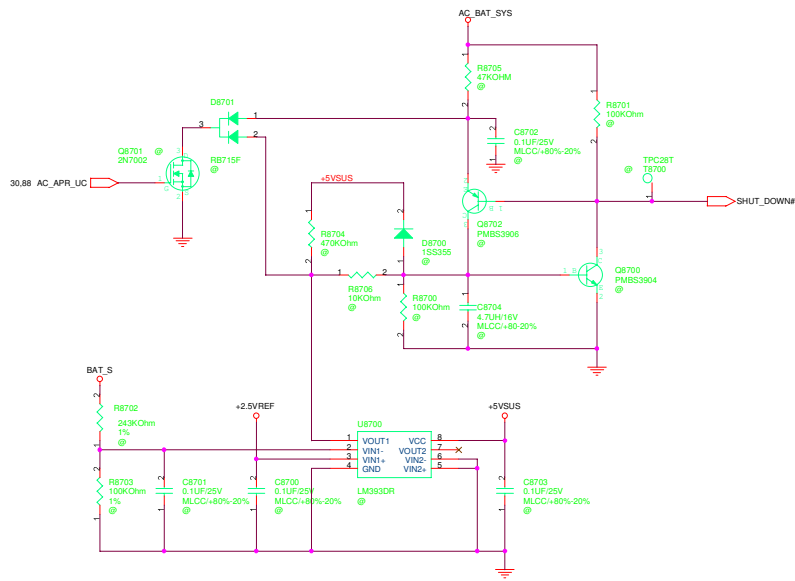
-Variant Name-		Title :POWER_VGA_CORE & RAM	
-Originals-		Engineer:	
Size	Project Name	Rev	
C	ROSA	1.1	
Code: 10011-11-26-2007	ESpec	85	of 84

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<Variant Name>		Title : NA	
<OrgName>		Engineer:	
Size	Project Name	Rev	
B	ROSA	1.1	
Date: 11/25/2007		Sheet 86 of 94	

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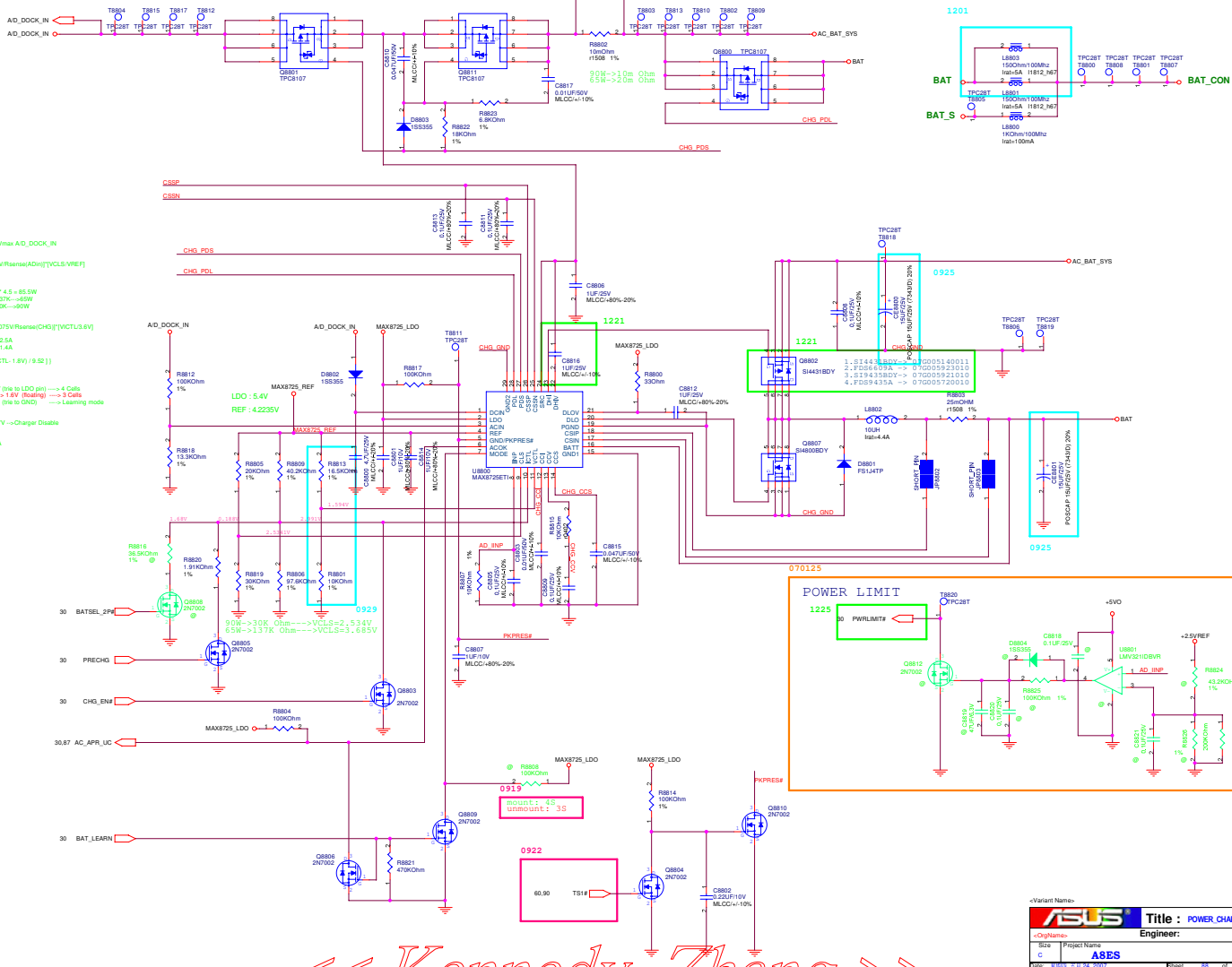
PIC only



<Variant Name>

		<b>Title :</b> POWER_SHUTDOWN#
Engineer:		
Size	Project Name	Rev
Custom	ABES	2.0
Date: 11/11/06, 2007	Sheet	87 of 94

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● AC\_IN Threshold > 2.048Vmax AD\_DOCK\_IN > 17.44V active  
 Adapter (InVmax) = (0.075V/Rsense/Adm)/(VCLS/VREF)  
 Resense/Adm=0.1000m  
 VCLS=2.534V  
 => InVmax=1.5A  
 => Constant Power = 1.5 \* 4.5 = 6.75W  
 => R885=20k,R881=137k->65W  
 => R885=20k,R881=33k->90W

Charge Current Idg = (0.075V/Rsense/CHG)/(VCTL3/V)  
 Resense/CHG=0.025 Ohm  
 VCTL=3V => Idg = 2.5A  
 VCTL=1.58V => Idg = 1.4A

Vbat = Cch \* (Vbat - (VCTL - 1.5V) / 9.52)  
 VCTL = 1.58V  
 => Vbat = 4.2V

Mode pin: Vinode > 2.8V (Vbat to LDO pin) => 4 Cells  
 2.8 > Vinode > 1.6V (Vbat pin) => 3 Cells  
 0.8 > Vinode (Vbat to GND) => Learning mode


VCTL=0.8V or DCIN = 7V -> Charger Disable

Precharge current=100mA

ASUS		Title : POWER CHARGER	
Site	Project Name	Engineer	Rev
C	ABES		2.0
Date	File	Path	Rev
2013.11.25.2013	11025201	E:\8801	2.0

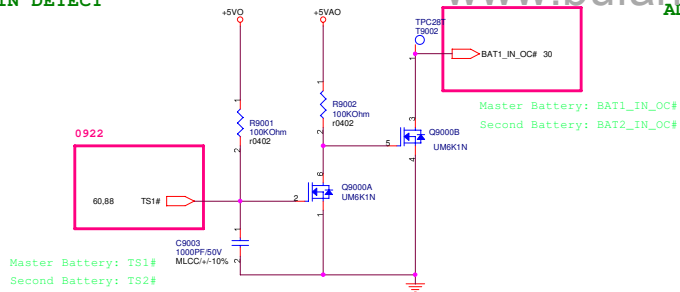
« Kennedy\_Zhang »



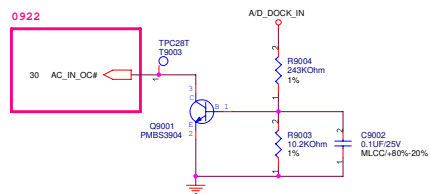
<Variant Name>				Title : NA	
<OrigName>		Engineer:			
Size	Project Name				Rev
Custom	ROSA				1.1
Date:	11/25/2007			Sheet	89 of 94

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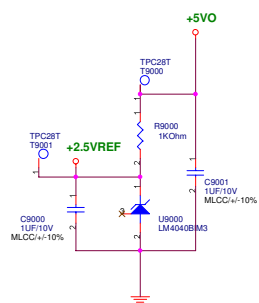
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



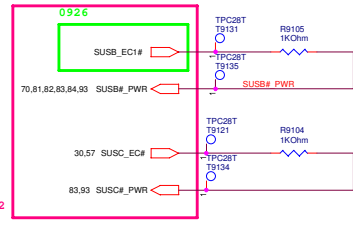
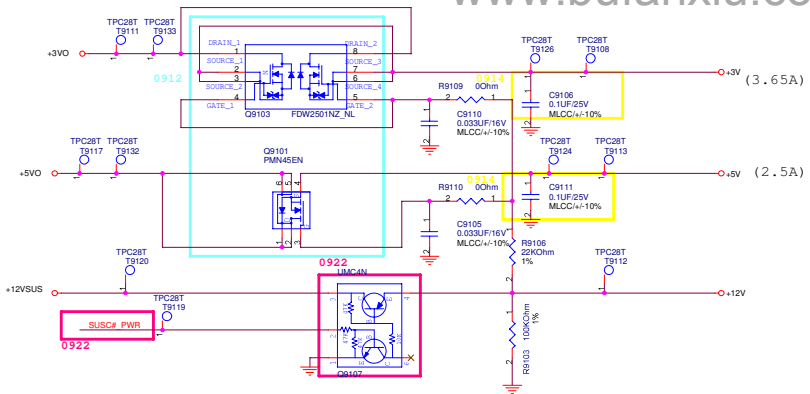
<Variant Name>

		Title : POWER_DETECT	
Engineer:			
Size	Project Name	Rev	
Custom	ABES	2.0	
Date: 2007.11.24.2007	Sheet	90	of 94

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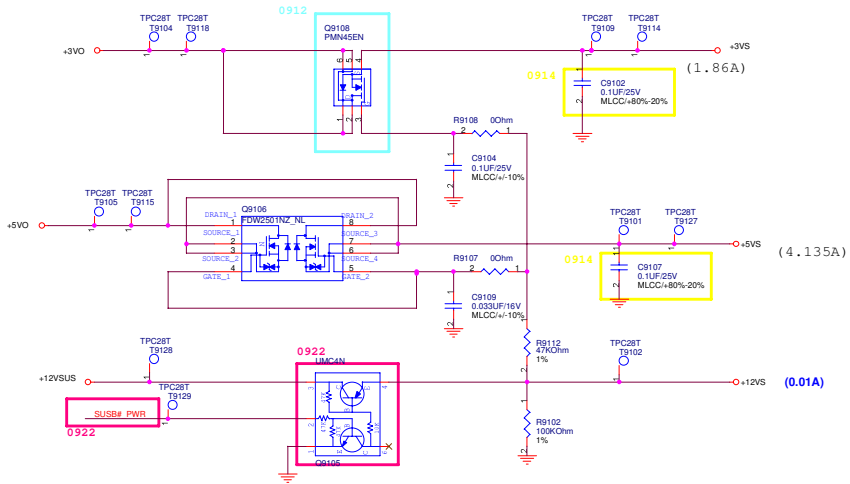
SUSC#\_PWR POWER

0922



SUSB#\_PWR POWER

0922

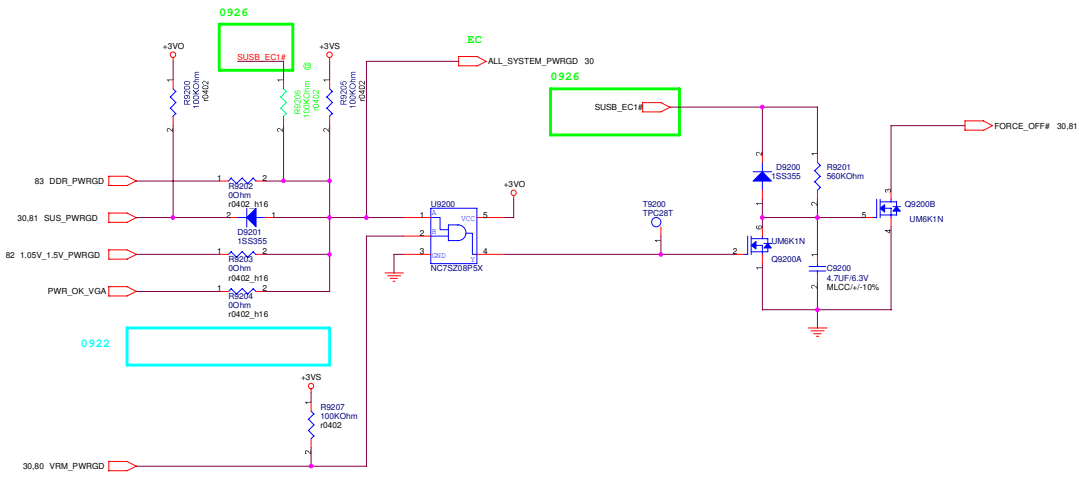


<Variant Name>

<b>ASUS</b>		<b>Title : POWER_LOAD_SWITCH</b>	
<OrgName>		Engineer:	
Size	Project Name		Rev
Custom	<b>ABES</b>		2.0
Date: 2007.11.24.2007		Sheet	81 of 84

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POWER GOOD DETECTOR



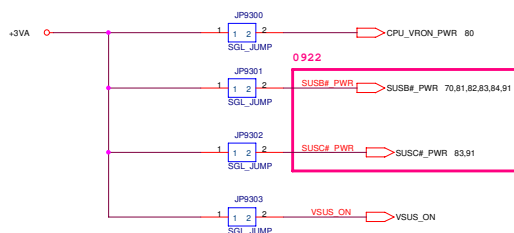
<Variant Name>

<b>ASUS</b>		<b>Title :</b> POWER_PROTECT
Engineer:		
<OrigName>	Project Name	Rev
Custom	<b>ABES</b>	2.0
Date: 11/11/06, 2007	Sheet	62 of 94

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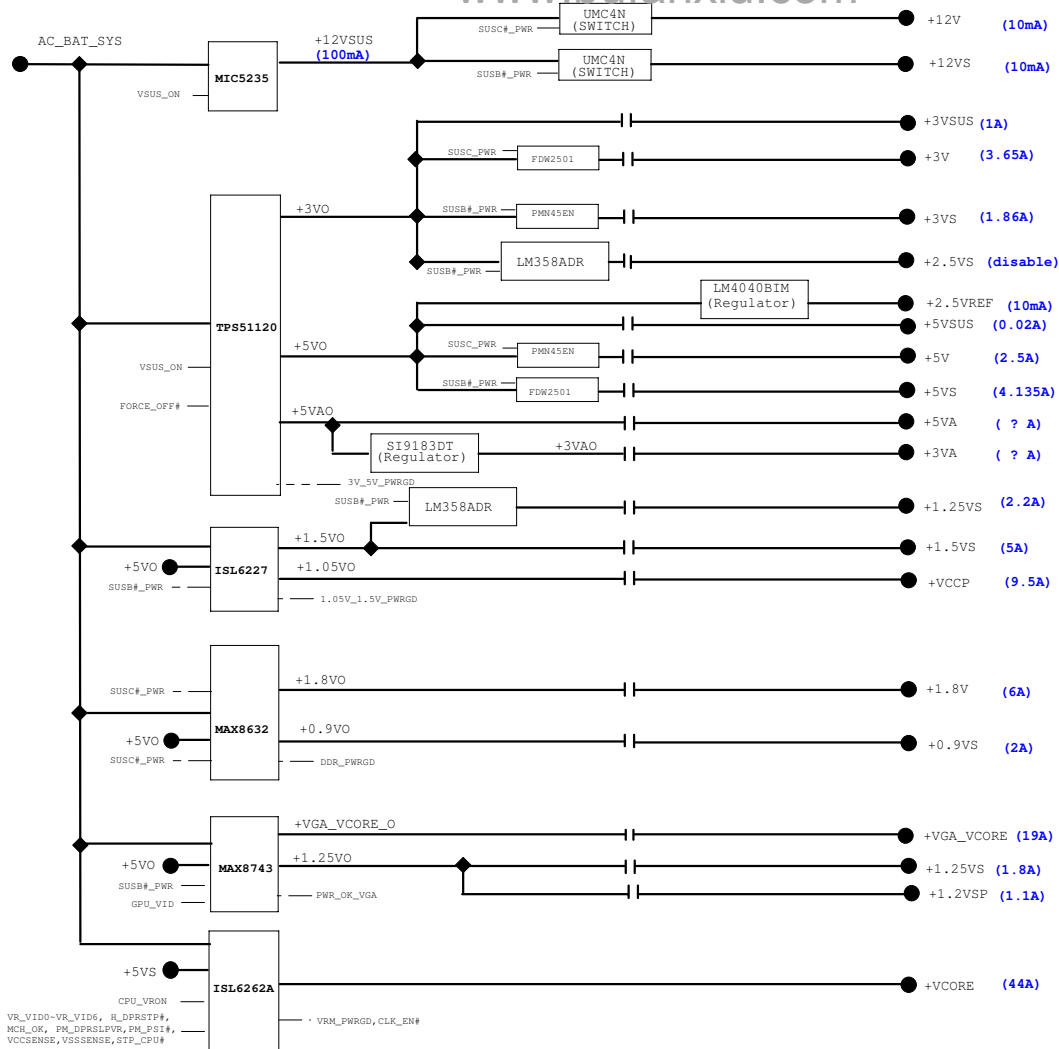
FOR POWER TEST



<Variant Name>

<b>ASUS</b>		<b>Title :</b> POWER_SIGNAL
Engineer: <OrgAddr1>		
Size	Project Name	Rev
Custom	ABES	2.0
Date: 2007.11.24.2007	Sheet	89 of 94

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