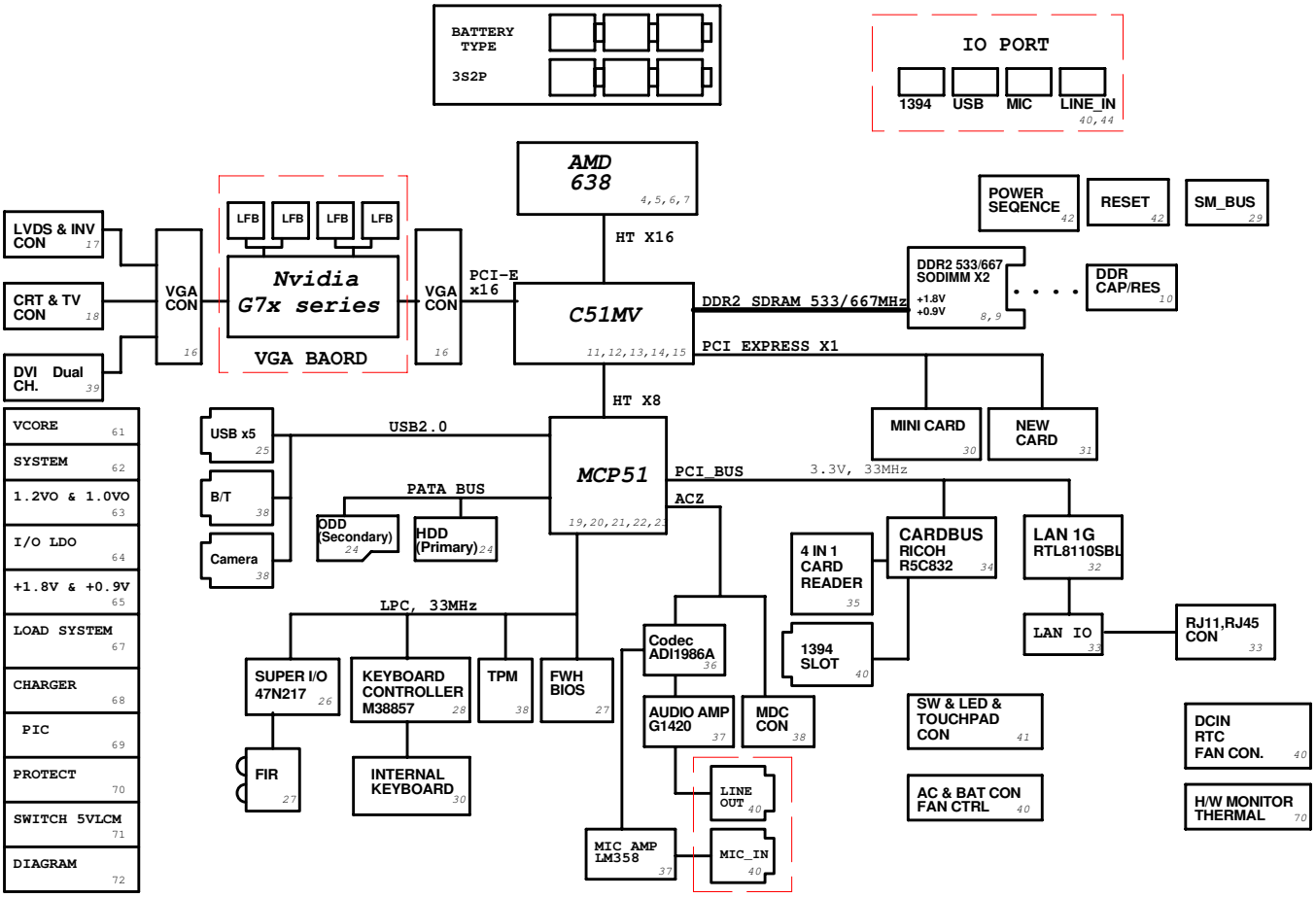
A8T/M SCHEMATIC R2.1

<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: PAGE REF.	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 1 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>

A8T/M AMD S1/C51MV BLOCK DIAGRAM



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PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 2 OF 55	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWRLMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_[11:16]		(CPU_VID[0:5])	+3VSUS
GPIO_17		(LFD#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDIN0_AUD	+3VSUS
GPIO_23		ACZ_SDIN1_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	SIO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(RI#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

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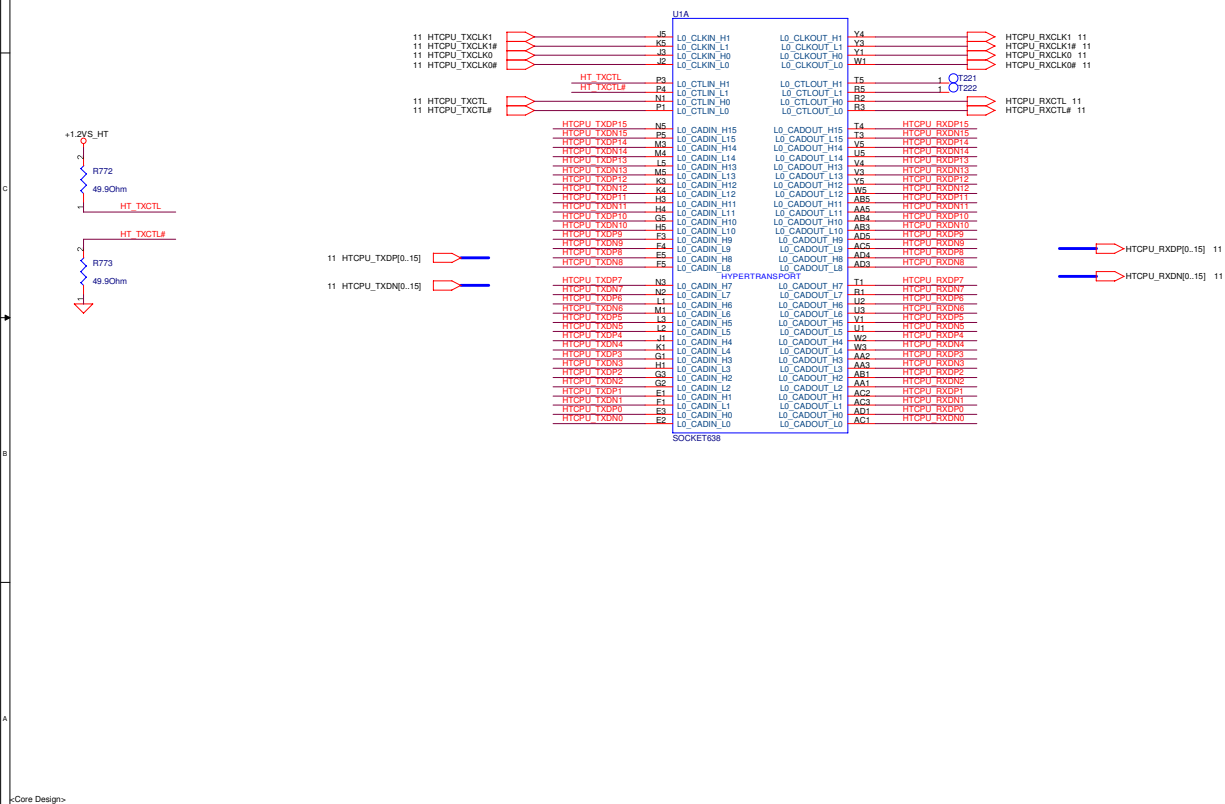
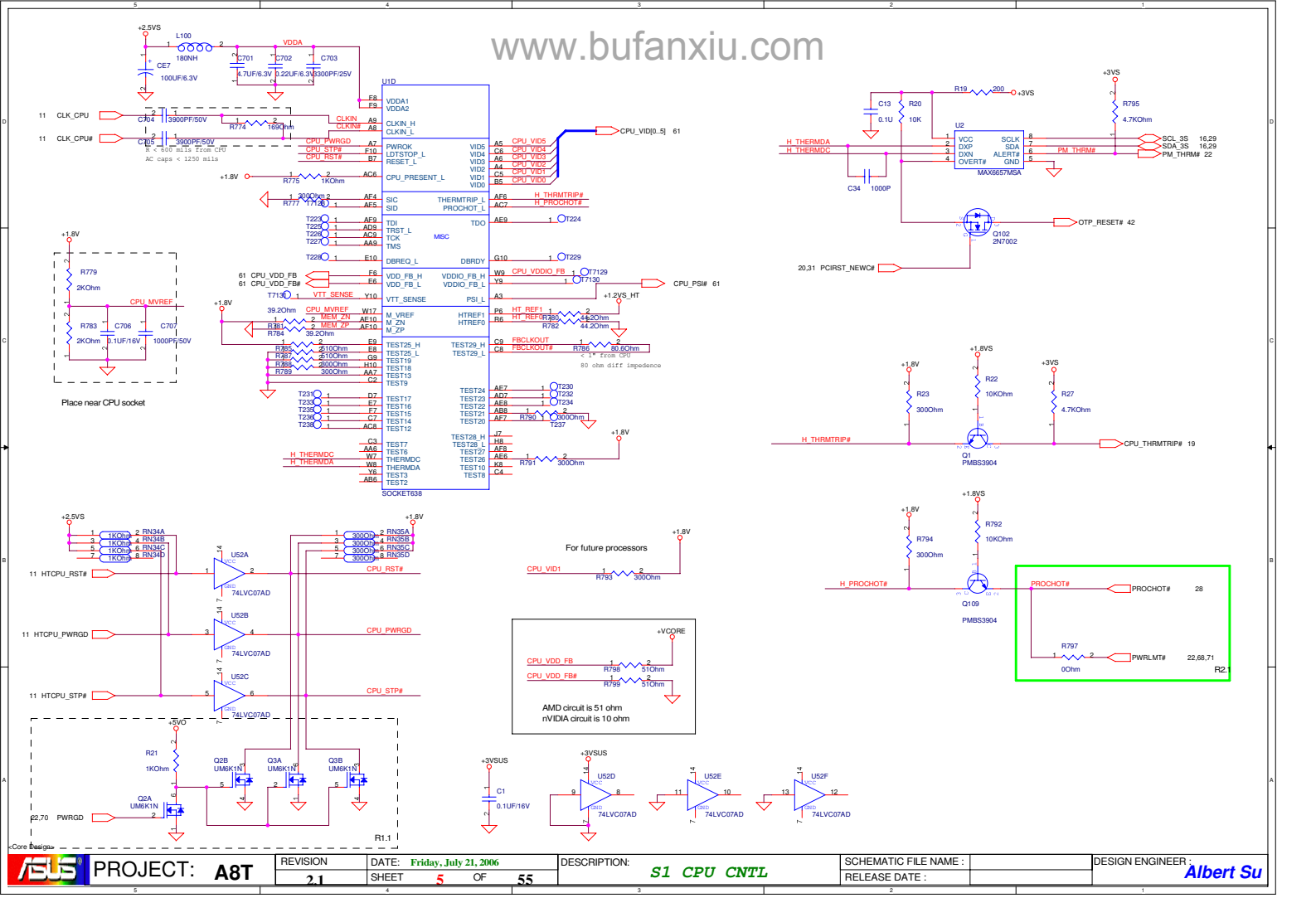
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 3 OF 55	DESCRIPTION: SCHEMATICS REF.	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

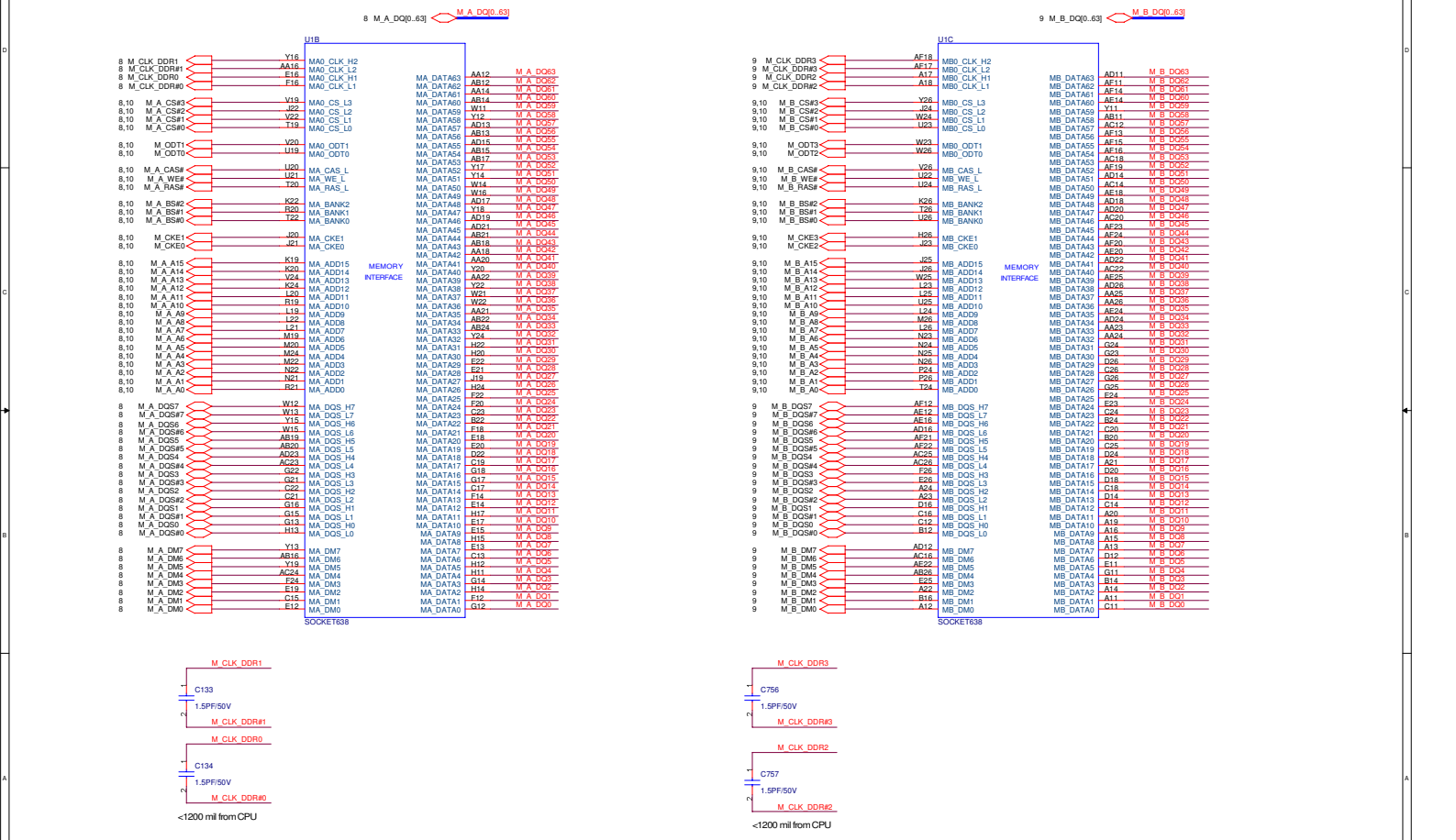


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 4 OF 55		RELEASE DATE :	

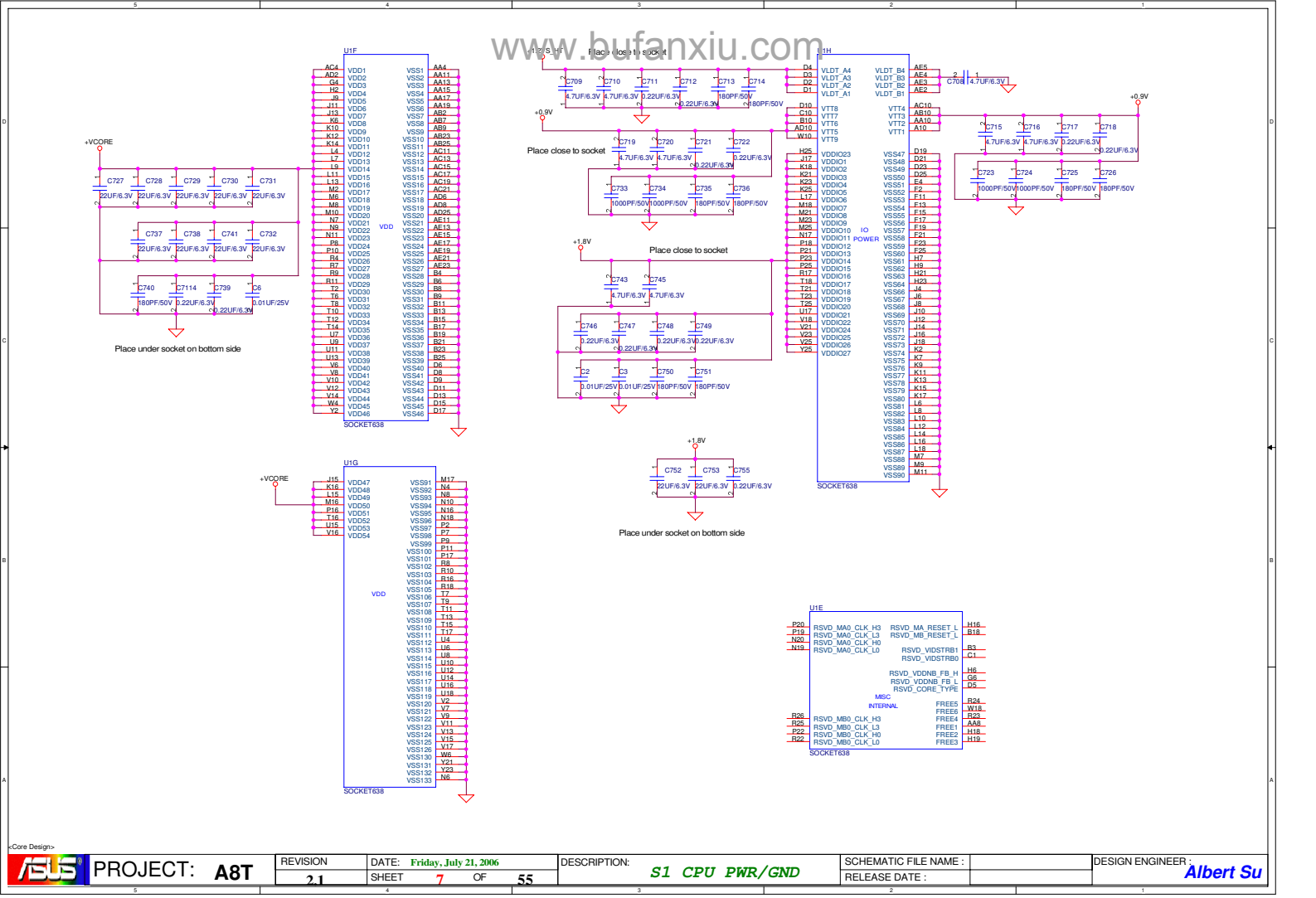


PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU CNTL	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 5 OF 55		RELEASE DATE :	



<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: S1 CPU MEM	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 6 OF 55		RELEASE DATE :		



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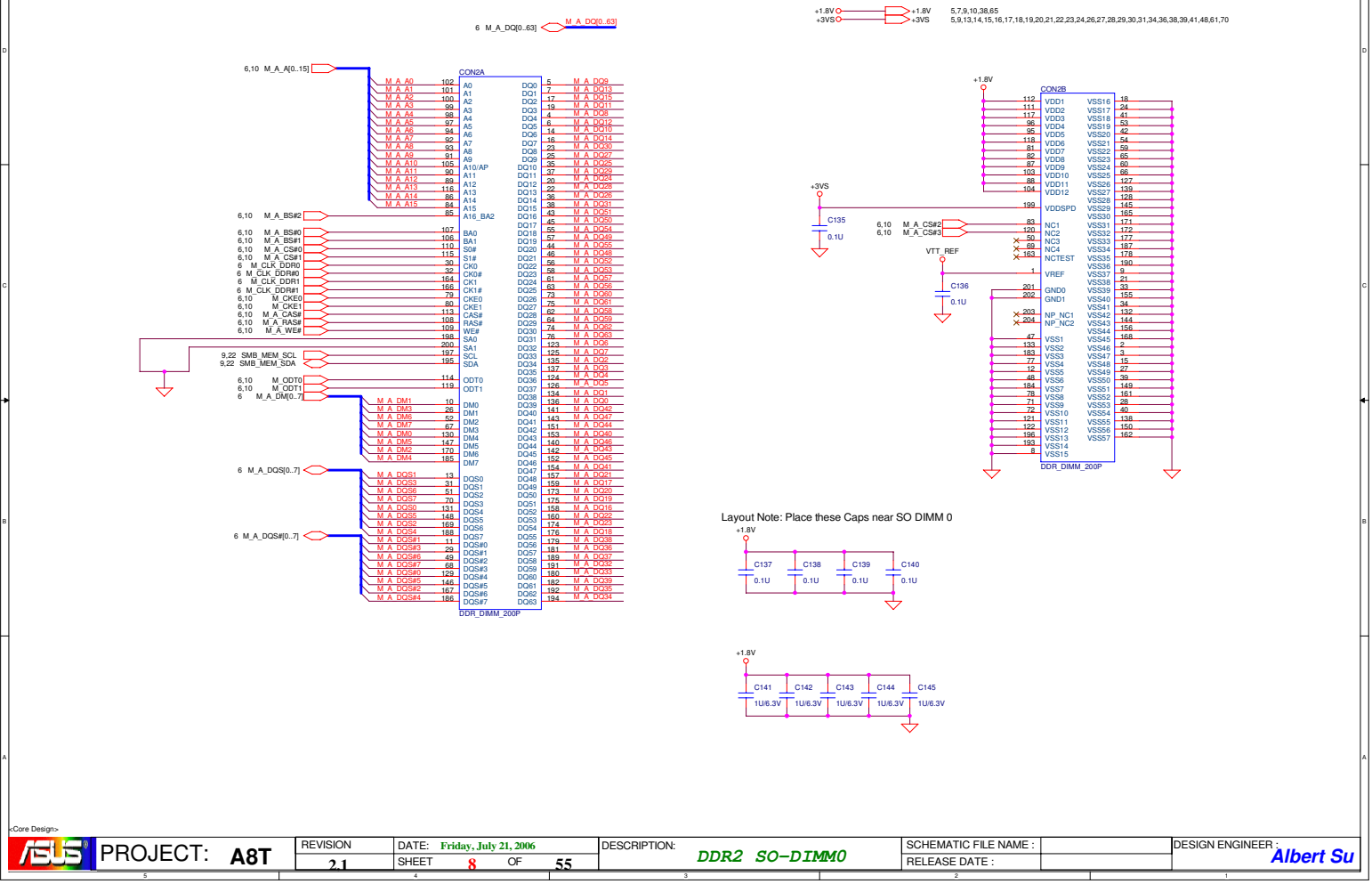
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 7 OF 55	DESCRIPTION: S1 CPU PWR/GND	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

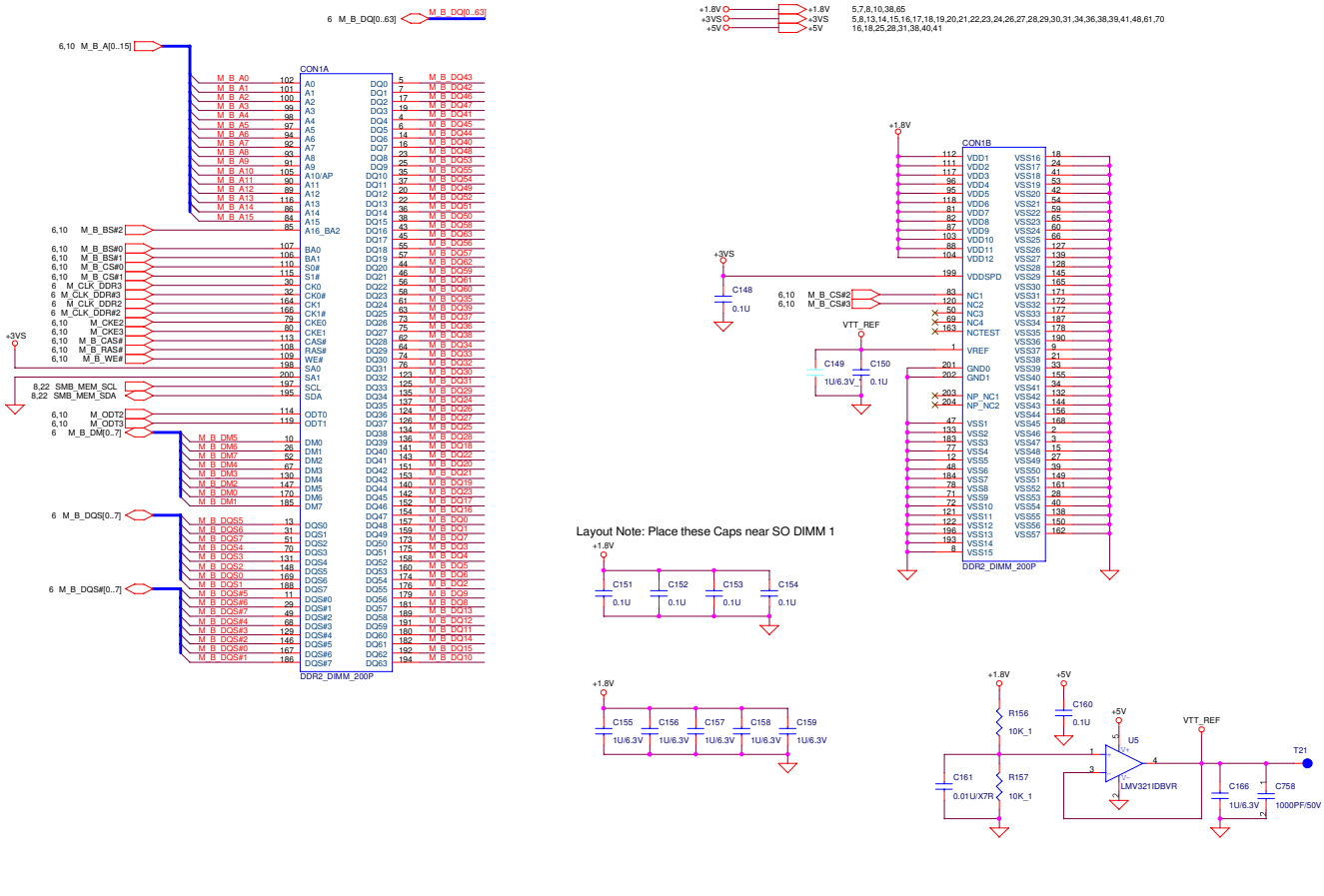
<< Kennedy_Zhang >>

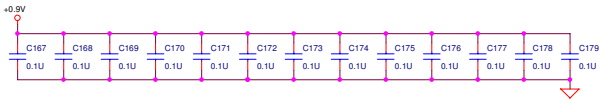


<Core Design>

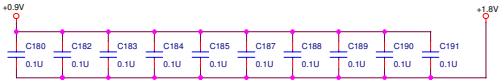
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 8 OF 55	DESCRIPTION: DDR2 SO-DIMM0	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

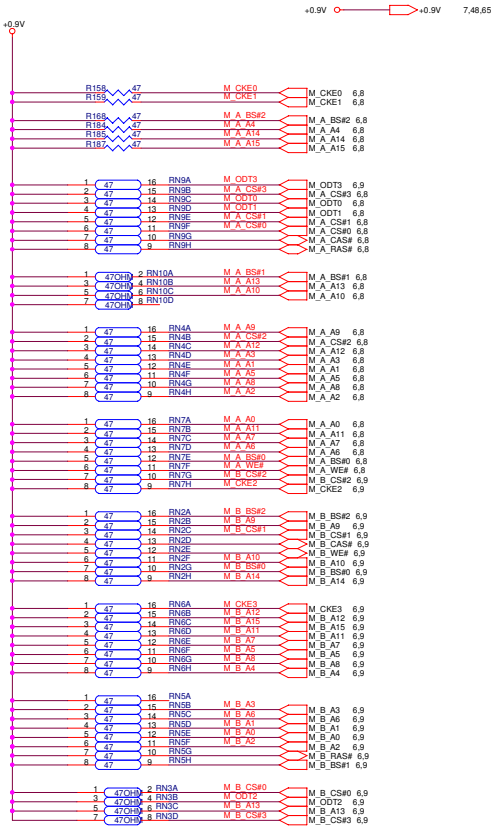
<< Kennedy_Zhang >>





Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V





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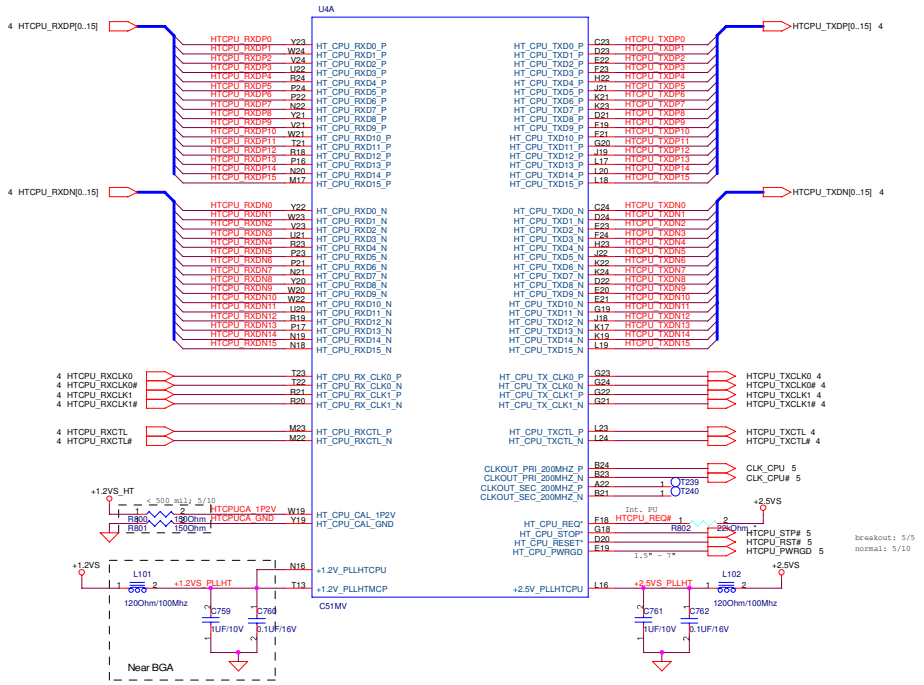
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 10 OF 55	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



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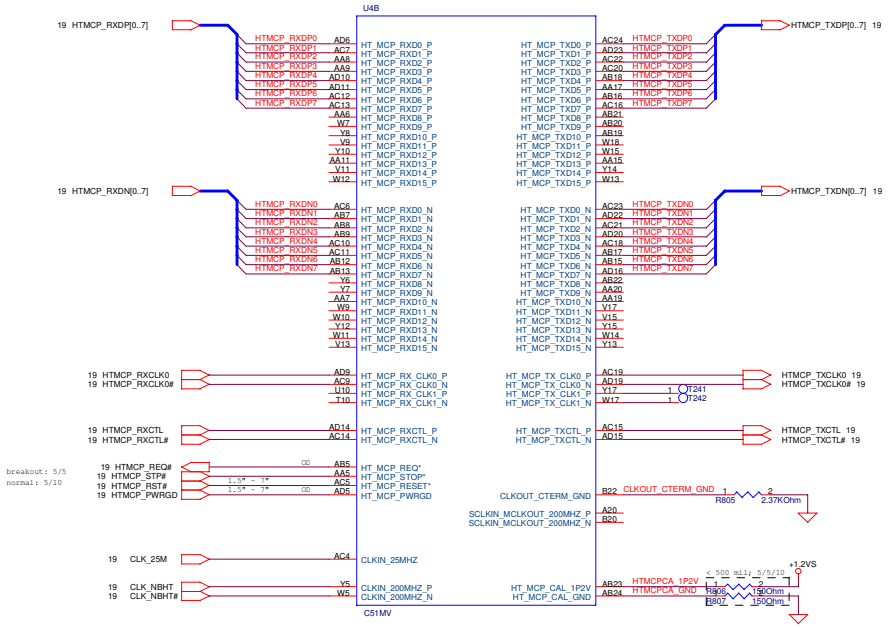
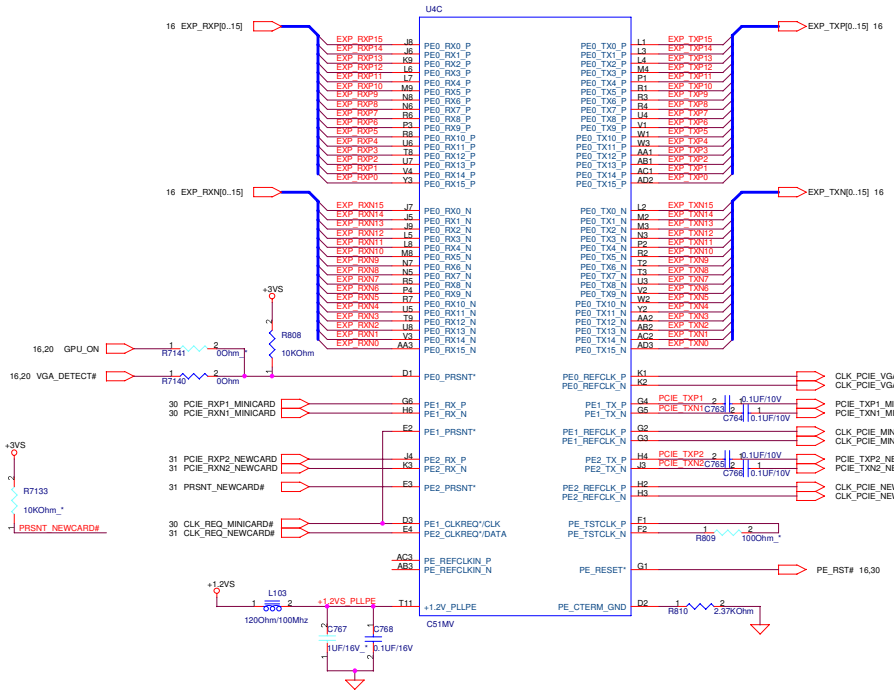
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 11 OF 55		RELEASE DATE :	



<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: C51M HT TO MCP	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 12 OF 55		RELEASE DATE :	Albert Su



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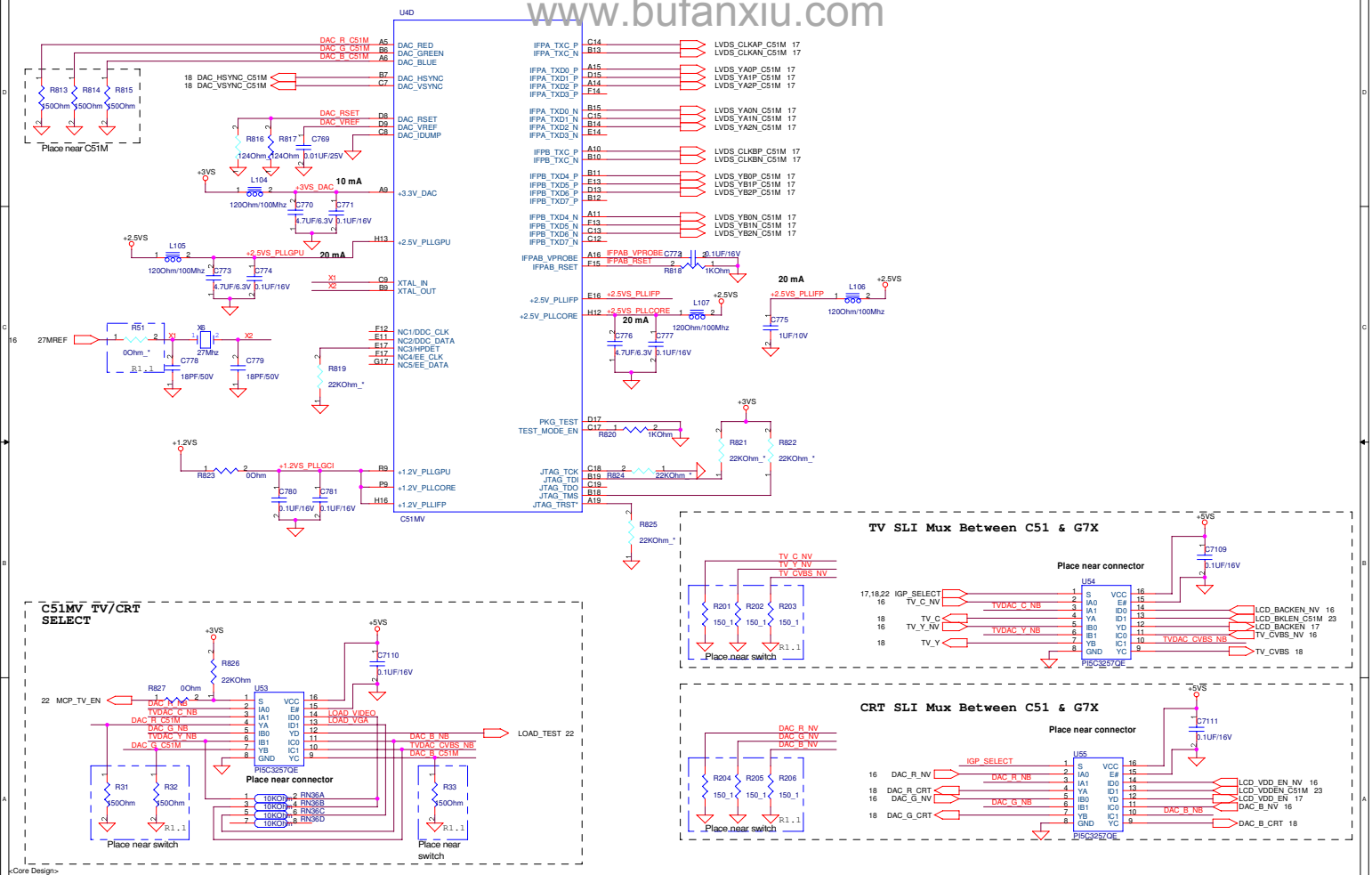
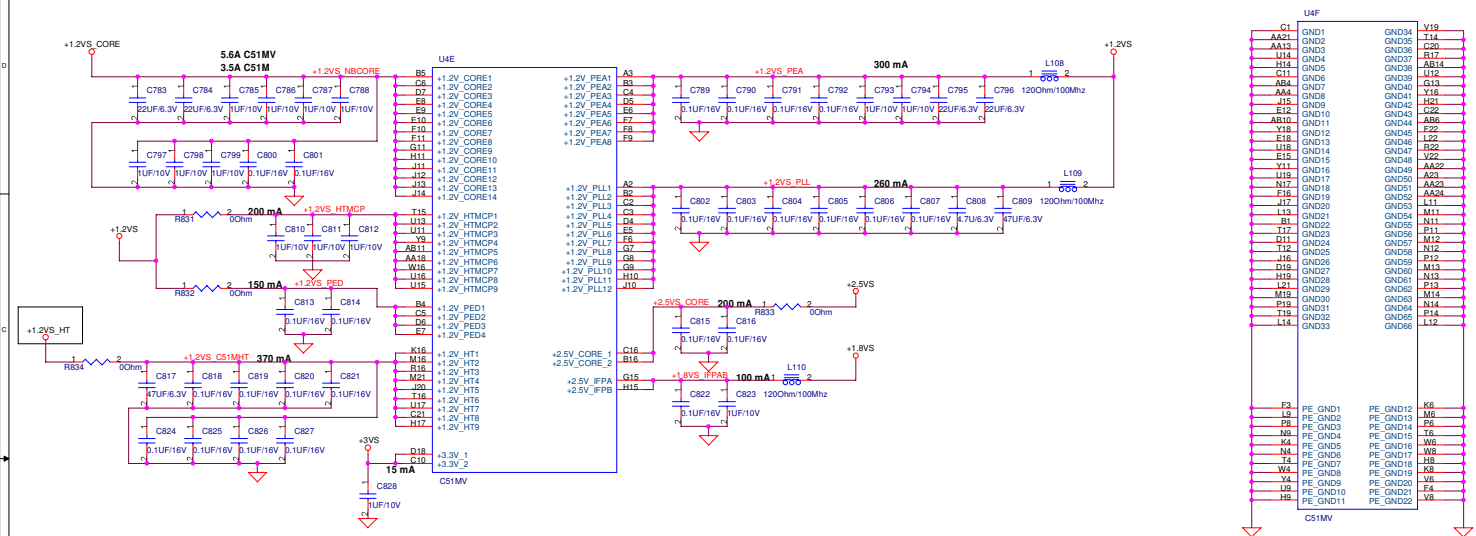
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 13 OF 55		RELEASE DATE :	





<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 15 OF 55		RELEASE DATE :	Albert Su

Polarity Inversion:
PEXP_TXP0, 2, 4, 6, 8, 14

CON3A GF_VGA_230P

DVI
39 DVI_TX0P_NV → 28 DVI_A_TX0
39 DVI_TX0N_NV → 30 DVI_A_TX0#
39 DVI_TX1P_NV → 34 DVI_A_TX1
39 DVI_TX1N_NV → 36 DVI_A_TX1#
39 DVI_TX2P_NV → 40 DVI_A_TX2
39 DVI_TX2N_NV → 42 DVI_A_TX2#
39 DVI_CLKP_NV → 46 DVI_A_CLK
39 DVI_CLKN_NV → 48 DVI_A_CLK#
39 DVI_HDP_NV → 50 DVI_A_HPD
49 DVI_B_HPD/GND

DDC
39 DVI_DDCCLK_NV → 66 DDCB_CLK
39 DVI_DDCDAT_NV → 68 DDCB_DAT
18 DDC2BC_NV → 58 DDCA_CLK
18 DDC2BD_NV → 60 DDCA_DAT

VGA
14 DAC_B_NV → 65 VGA_BLU
14 DAC_R_NV → 57 VGA_RED
14 DAC_G_NV → 61 VGA_GRN
18 DAC_HSYNC_NV → 69 VGA_HSYNC
18 DAC_VSYNC_NV → 71 VGA_VSYNC

LVDS
14 LCD_VDD_EN_NV → 99 LVDS_PPEN
14 LCD_BACKEN_NV → 101 LVDS_BLEN
114 LVDS_BL_BRGHT
17 LVDS_YA0P_NV → 86 LVDS_UTX0
17 LVDS_YA0N_NV → 84 LVDS_UTX0#
17 LVDS_YA1P_NV → 92 LVDS_UTX1
17 LVDS_YA1N_NV → 90 LVDS_UTX1#
17 LVDS_YA2P_NV → 98 LVDS_UTX2
17 LVDS_YA2N_NV → 96 LVDS_UTX2#
106 LVDS_UTX3
110 LVDS_UTX3#
17 LVDS_CLKAP_NV → 102 LVDS_UCLK
17 LVDS_CLKAN_NV → 104 LVDS_UCLK#
17 LVDS_YB0P_NV → 87 LVDS_LTX0
17 LVDS_YB0N_NV → 89 LVDS_LTX0#
17 LVDS_YB1P_NV → 93 LVDS_LTX1
17 LVDS_YB1N_NV → 95 LVDS_LTX1#
17 LVDS_YB2P_NV → 83 LVDS_LTX2
17 LVDS_YB2N_NV → 81 LVDS_LTX2#
105 LVDS_LTX3
107 LVDS_LTX3#
17 LVDS_CLKBP_NV → 77 LVDS_LCLK
17 LVDS_CLKBN_NV → 75 LVDS_LCLK#

IGP
+0.9VS → 222 IGP_UTX0
224 IGP_UTX0#
228 IGP_UTX1
230 IGP_UTX1#
221 IGP_UTX2
223 IGP_UTX2#
227 IGP_UCLK
229 IGP_UCLK#
39 DVI_TX3P_NV → 27 IGP_LTX0/DVI_B_TX0
39 DVI_TX3N_NV → 29 IGP_LTX0#/DVI_B_TX0#
39 DVI_TX4P_NV → 33 IGP_LTX1/DVI_B_TX1
39 DVI_TX4N_NV → 35 IGP_LTX1#/DVI_B_TX1#
39 DVI_TX5P_NV → 39 IGP_LTX2/DVI_B_TX2
39 DVI_TX5N_NV → 41 IGP_LTX2#/DVI_B_TX2#
45 IGP_LCLK/DVI_B_CLK
47 IGP_LCLK#/DVI_B_CLK#

TV-OUT
14 TV_Y_NV → 72 TV_Y/HDTV_Y/TV_CVBS
14 TV_C_NV → 76 TV_C/HDTV_Pr
14 TV_CVBS_NV → 80 TV_CVBS/HDTV_Pb

SMBUS
17 EDID_CLK_NV → 62 DDCC_CLK
17 EDID_DATA_NV → 64 DDCC_DAT
5,29 SCL_3S → 109 SMB_CLK
5,29 SDA_3S → 111 SMB_DAT

PEX
PEXP_TXP0# 121 → C194 0.1U/10V → EXP_TXN0 13
PEXP_TXP0 123 → C193 0.1U/10V → EXP_TXP0 13
PEX_TX0 → EXP_RXP0 13
PEX_TX0# → EXP_RXN0 13
PEX_RX0 124
PEXP_TXP1# 127 → C196 0.1U/10V → EXP_TXN1 13
PEXP_TXP1 129 → C195 0.1U/10V → EXP_TXP1 13
PEX_TX1 → EXP_RXP1 13
PEX_TX1# → EXP_RXN1 13
PEX_RX1 130
PEXP_TXP2# 133 → C198 0.1U/10V → EXP_TXN2 13
PEXP_TXP2 135 → C197 0.1U/10V → EXP_TXP2 13
PEX_TX2 → EXP_RXP2 13
PEX_TX2# → EXP_RXN2 13
PEX_RX2 136
PEXP_TXP3 139 → C199 0.1U/10V → EXP_TXP3 13
PEXP_TXP3# 141 → C200 0.1U/10V → EXP_TXN3 13
PEX_TX3 → EXP_RXP3 13
PEX_TX3# → EXP_RXN3 13
PEX_RX3 140
PEX_RX3# 142
PEXP_TXP4# 145 → C203 0.1U/10V → EXP_TXN4 13
PEXP_TXP4 147 → C202 0.1U/10V → EXP_TXP4 13
PEX_TX4 → EXP_RXP4 13
PEX_TX4# → EXP_RXN4 13
PEX_RX4 146
PEX_RX4# 148
PEXP_TXP5# 151 → C205 0.1U/10V → EXP_TXN5 13
PEXP_TXP5 153 → C204 0.1U/10V → EXP_TXP5 13
PEX_TX5 → EXP_RXP5 13
PEX_TX5# → EXP_RXN5 13
PEX_RX5 152
PEX_RX5# 154
PEXP_TXP6# 157 → C208 0.1U/10V → EXP_TXN6 13
PEXP_TXP6 159 → C207 0.1U/10V → EXP_TXP6 13
PEX_TX6 → EXP_RXP6 13
PEX_TX6# → EXP_RXN6 13
PEX_RX6 158
PEX_RX6# 160
PEXP_TXP7 163 → C209 0.1U/10V → EXP_TXP7 13
PEXP_TXP7# 165 → C210 0.1U/10V → EXP_TXN7 13
PEX_TX7 → EXP_RXP7 13
PEX_TX7# → EXP_RXN7 13
PEX_RX7 164
PEX_RX7# 166
PEXP_TXP8# 169 → C213 0.1U/10V → EXP_TXN8 13
PEXP_TXP8 171 → C212 0.1U/10V → EXP_TXP8 13
PEX_TX8 → EXP_RXP8 13
PEX_TX8# → EXP_RXN8 13
PEX_RX8 170
PEX_RX8# 172
PEXP_TXP9 175 → C214 0.1U/10V → EXP_TXP9 13
PEXP_TXP9# 177 → C215 0.1U/10V → EXP_TXN9 13
PEX_TX9 → EXP_RXP9 13
PEX_TX9# → EXP_RXN9 13
PEX_RX9 176
PEX_RX9# 178
PEXP_TXP10 C216 181 → C217 0.1U/10V → EXP_TXP10 13
PEXP_TXP10# 183 → EXP_TXN10 13
PEX_TX10 → EXP_RXP10 13
PEX_TX10# → EXP_RXN10 13
PEX_RX10 182
PEX_RX10# 184
PEXP_TXP11 C218 187 → C219 0.1U/10V → EXP_TXP11 13
PEXP_TXP11# 189 → EXP_TXN11 13
PEX_TX11 → EXP_RXP11 13
PEX_TX11# → EXP_RXN11 13
PEX_RX11 188
PEX_RX11# 190
PEXP_TXP12 C220 193 → C221 0.1U/10V → EXP_TXP12 13
PEXP_TXP12# 195 → EXP_TXN12 13
PEX_TX12 → EXP_RXP12 13
PEX_TX12# → EXP_RXN12 13
PEX_RX12 194
PEX_RX12# 196
PEXP_TXP13 C222 199 → C223 0.1U/10V → EXP_TXP13 13
PEXP_TXP13# 201 → EXP_TXN13 13
PEX_TX13 → EXP_RXP13 13
PEX_TX13# → EXP_RXN13 13
PEX_RX13 200
PEX_RX13# 202
PEXP_TXP14 C225 205 → C224 0.1U/10V → EXP_TXN14 13
PEXP_TXP14# 207 → EXP_TXP14 13
PEX_TX14 → EXP_RXP14 13
PEX_TX14# → EXP_RXN14 13
PEX_RX14 206
PEX_RX14# 208
PEXP_TXP15 C227 211 → C226 0.1U/10V → EXP_TXN15 13
PEXP_TXP15# 213 → EXP_TXP15 13
PEX_TX15 → EXP_RXP15 13
PEX_TX15# → EXP_RXN15 13
PEX_RX15 212
PEX_RX15# 214

OTHER
CLK_REQ# 116
PEX_RST# 118 → R101 0Ohm → PE_RST# → PE_RST# 13,30
PEX_REFCLK 115 → CLK_PCIE_VGA 13
PEX_REFCLK# 117 → CLK_PCIE_VGA# 13
THERM# 24
PRSNT1# 225 → VGA_DETECT# 13,20
PRSNT2# 226
RUNPWROK 26 → VGA_PWRGD 20,70

+1.5VS 19,21,22,23,30,31,38,48
+1.8VS 5,15,17,48
+2.5VS 5,11,14,15,18,38,48
+3VS 5,8,9,13,14,15,17,18,19,20,21,22,23,24,26,27,28,29,30,31,34,36,38,39,41,48,61,70
+5V 9,18,25,28,31,38,40,41
+12VS 17

AC_BAT_SYS
C201 15UF/25V

CON3B GF_VGA_230P
PWR_SRC1 1, PWR_SRC2 3, PWR_SRC3 5, PWR_SRC4 7, PWR_SRC5 9, PWR_SRC6 11, PWR_SRC7 13, PWR_SRC8 15
GND1 31, GND2 32, GND3 37, GND4 38, GND5 43, GND6 44, GND7 55, GND8 56, GND9 59, GND10 63, GND11 67, GND12 70, GND13 73, GND14 74, GND15 78, GND16 79, GND17 82, GND18 85, GND19 88, GND20 91, GND21 94, GND22 97, GND23 100, GND24 103, GND25 106, GND26 112, GND27 113, GND28 119, GND29 120, GND30 125, GND31 126, GND32 131, GND33 132, GND34 137, GND35 138, GND36 143, GND37 144, GND38 149, GND39 150, GND40 155, GND41 156, GND42 161, GND43 162, GND44 167, GND45 168, GND46 173, GND47 174, GND48 179, GND49 180, GND50 185, GND51 186, GND52 191, GND53 192, GND54 197

+1.5VS_VG
C206 10U/10V
1V8RUN_1 2, 1V8RUN_2 4, 1V8RUN_3 6, 1V8RUN_4 8, 1V8RUN_5 10, 1V8RUN_6 12, 1V8RUN_7 14

+3VS
C211 10U/10V
3V3RUN_1 17, 3V3RUN_2 19, 3V3RUN_3 21

+2.5VS
5VRUN 18, 2V5RUN 16

+5V
RSVD1 20, RSVD2 22, RSVD3 23, RSVD4 52, RSVD5 54, RSVD6 53, AC/BATT# 51

+12VS
CLK_VGA27SS
CLK_VGA27FIX

+1.8VS
GND66 25, GND65 217, GND64 218, GND63 220, GND62 219, GND61 216, GND60 215, GND59 210, GND58 209, GND57 204, GND56 203, GND55 198

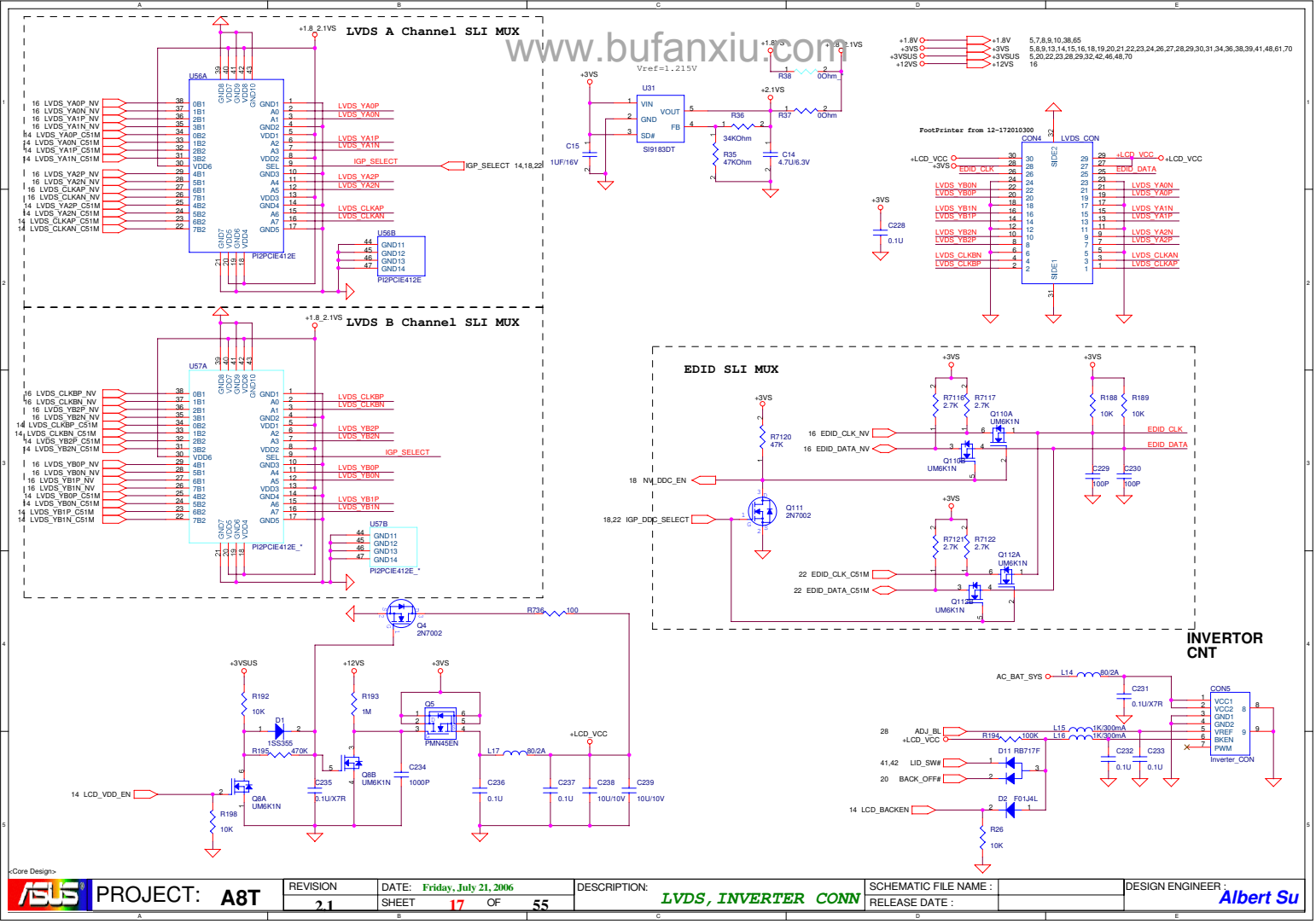
20 MXM_PWR_ON → R7139 0Ohm_* → HDTV_EN#
47,67 SUSB#_PWR → R7138 0Ohm → HDTV_EN#
18 HDTV_EN#

+3VS
R100 100K_*
PEX_RST#
Q116 2N7002_*
GPU_ON 13,20

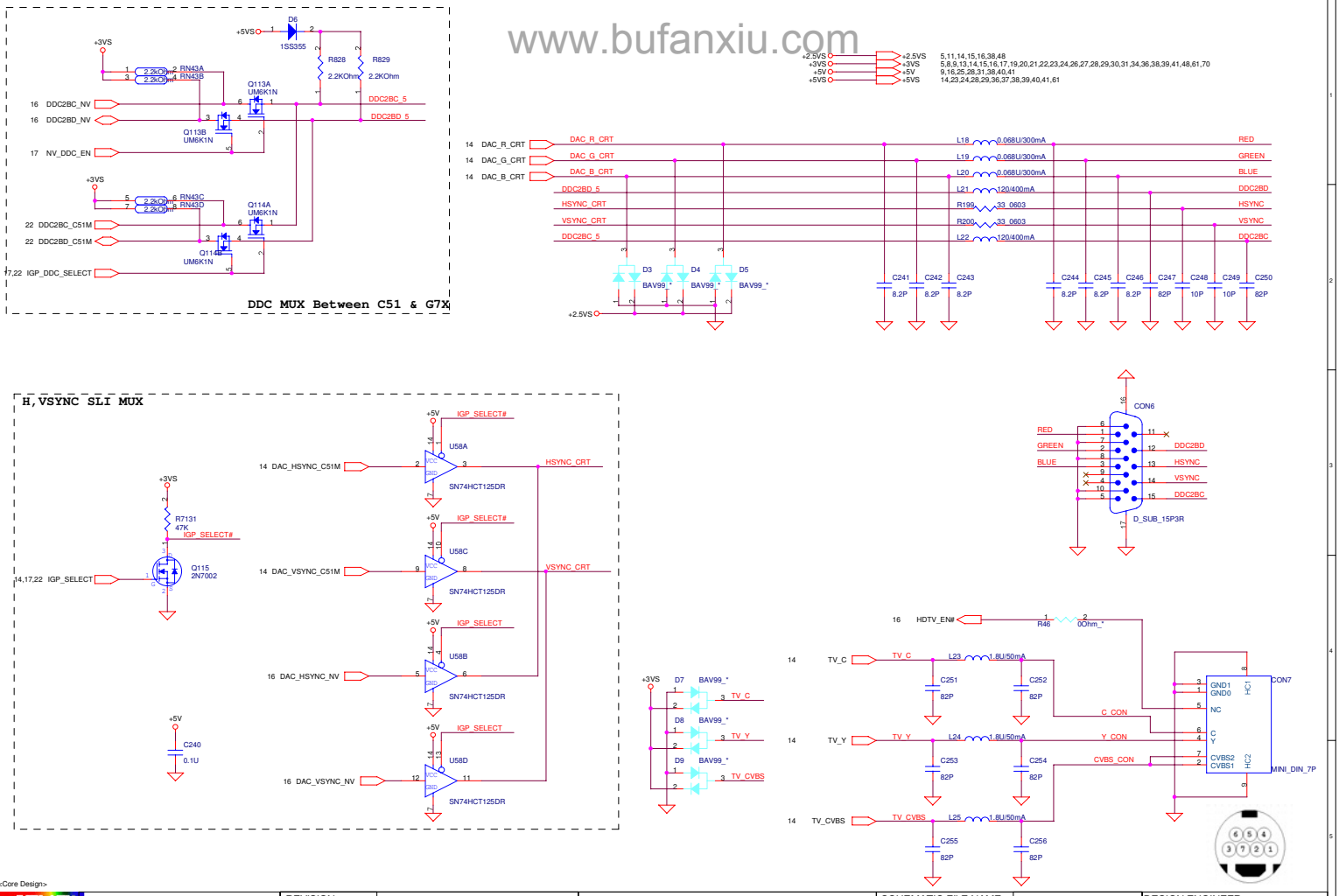
14 27MREF → R41 220hm_*
CLK_VGA27FIX → R42 220hm_* → REFCLK
CLK_VGA27SS → R44 220hm_*
U42 MK1726_08STR
X1/ICLK 1, GND 2, S0 3, SSCLK 4, X2 8, VDD 7, PD# 6, REFCLK 5
R43 10KOhm_*
X2 27Mhz
27M_X1 C38 18PF/50V_*
27M_X2 C39 18PF/50V_*
+3VS → 120Ohm/100Mhz_* → L1
C240 0.1UF/16V_*

<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 16 OF 55	DESCRIPTION: VGA CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

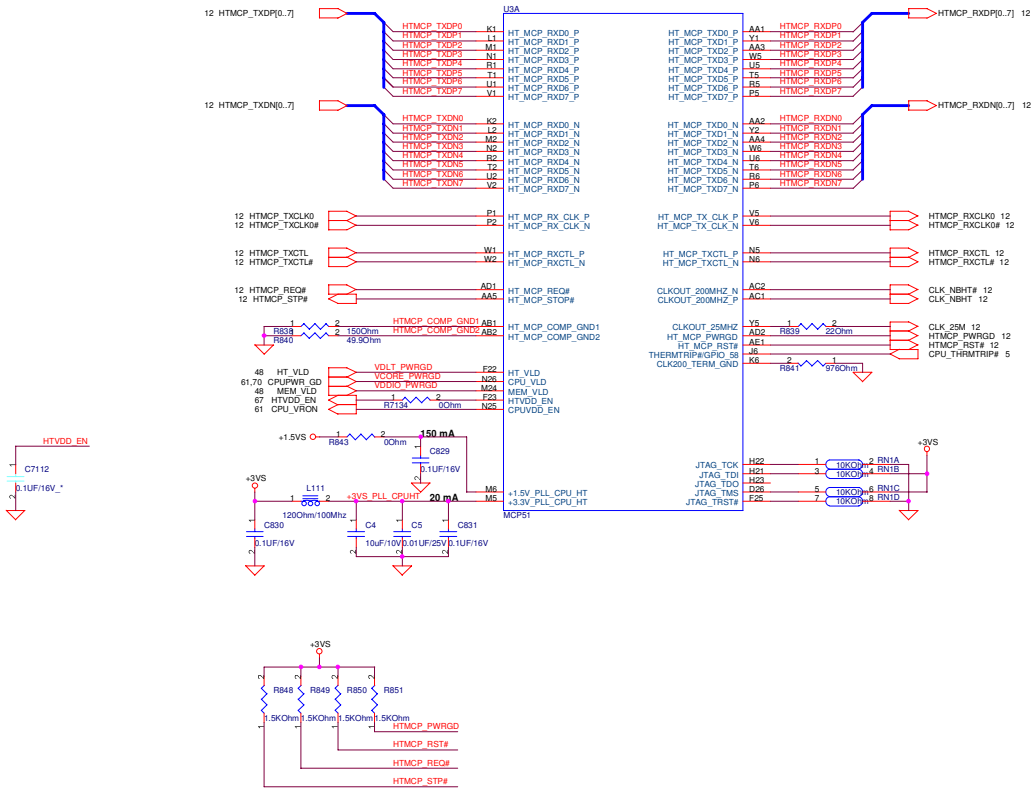


<< Kennedy_Zhang >>



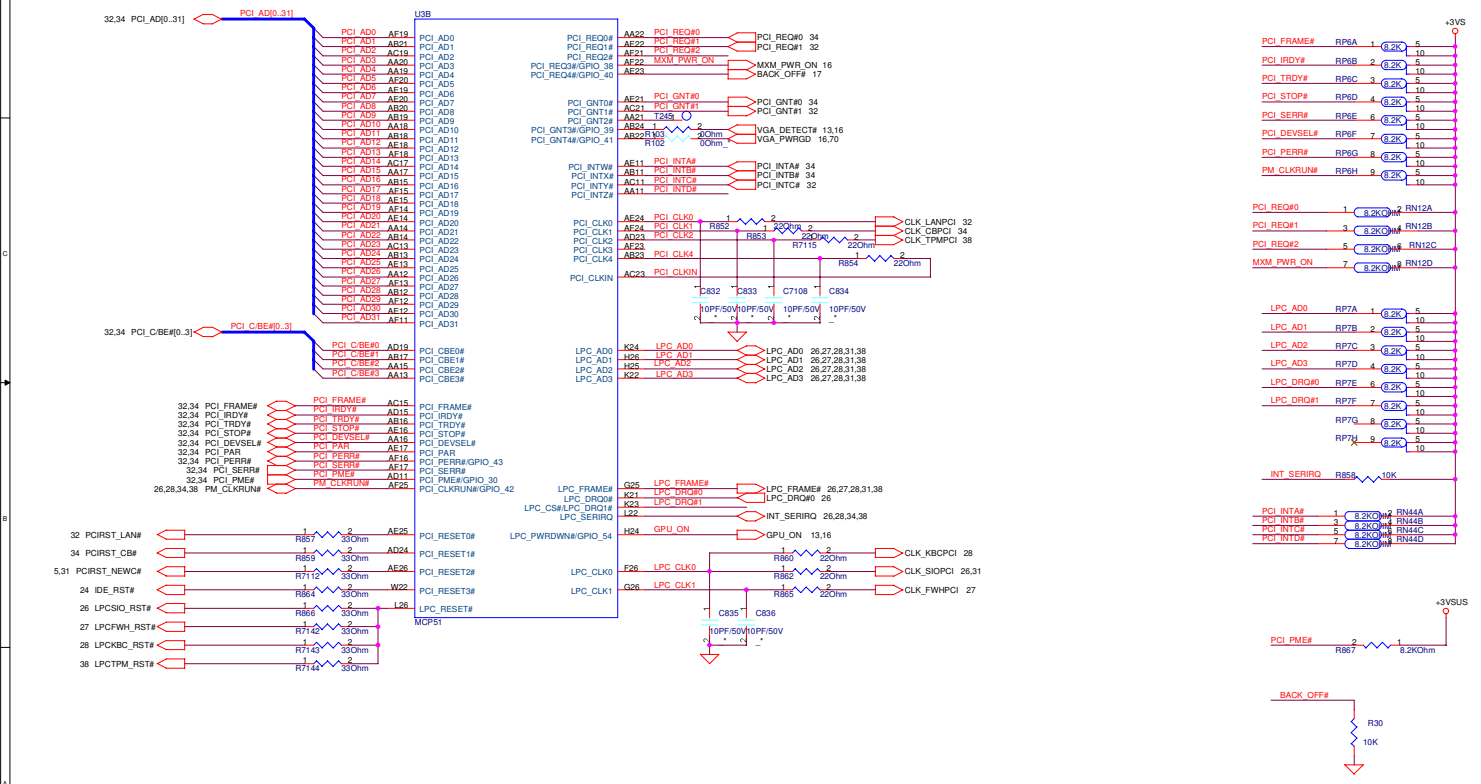
<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 18 OF 55	CRT & TV OUT	RELEASE DATE :	Albert Su



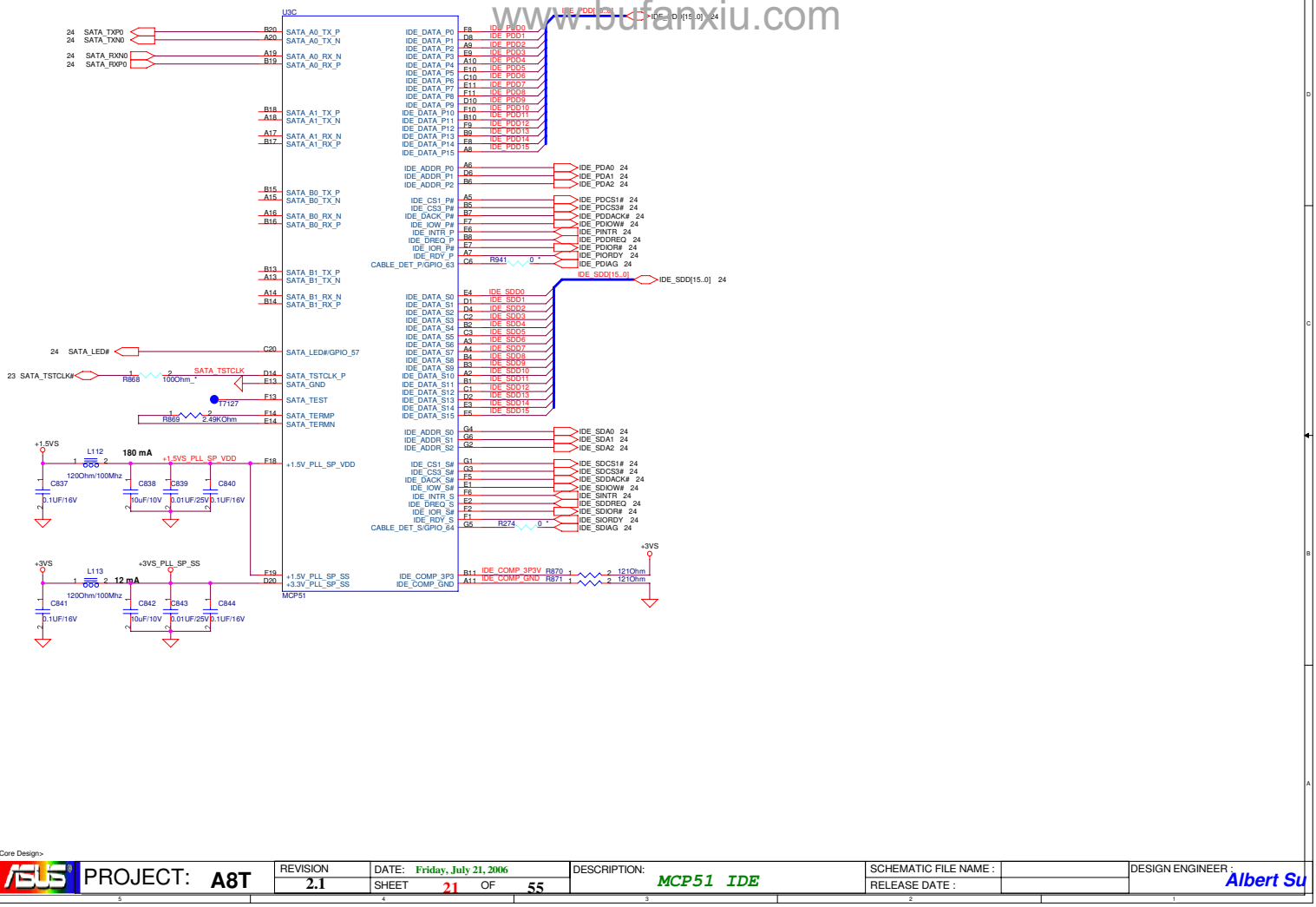
<Core Design>

PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 19 OF 55		RELEASE DATE :	Albert Su



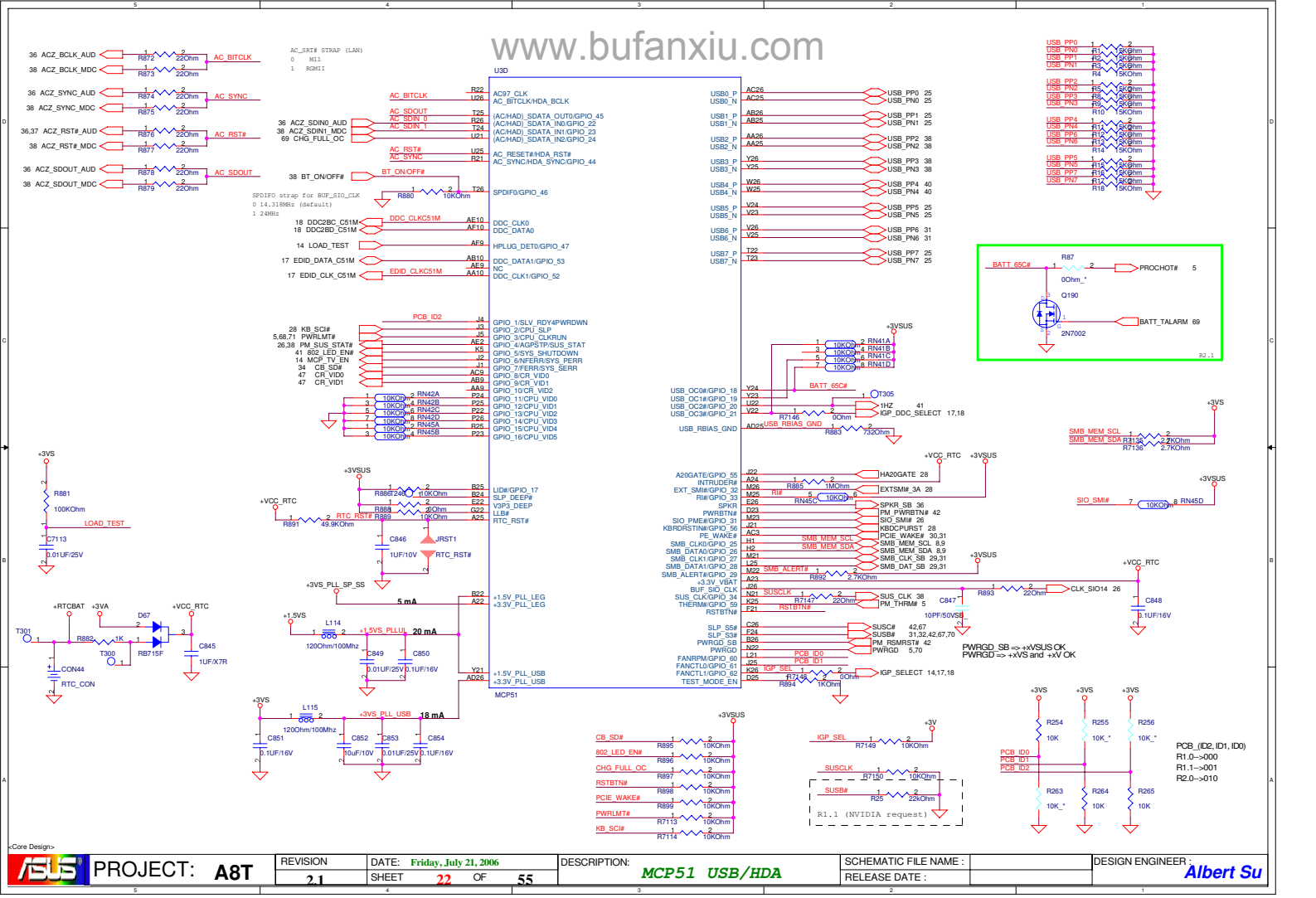
<Core Design>

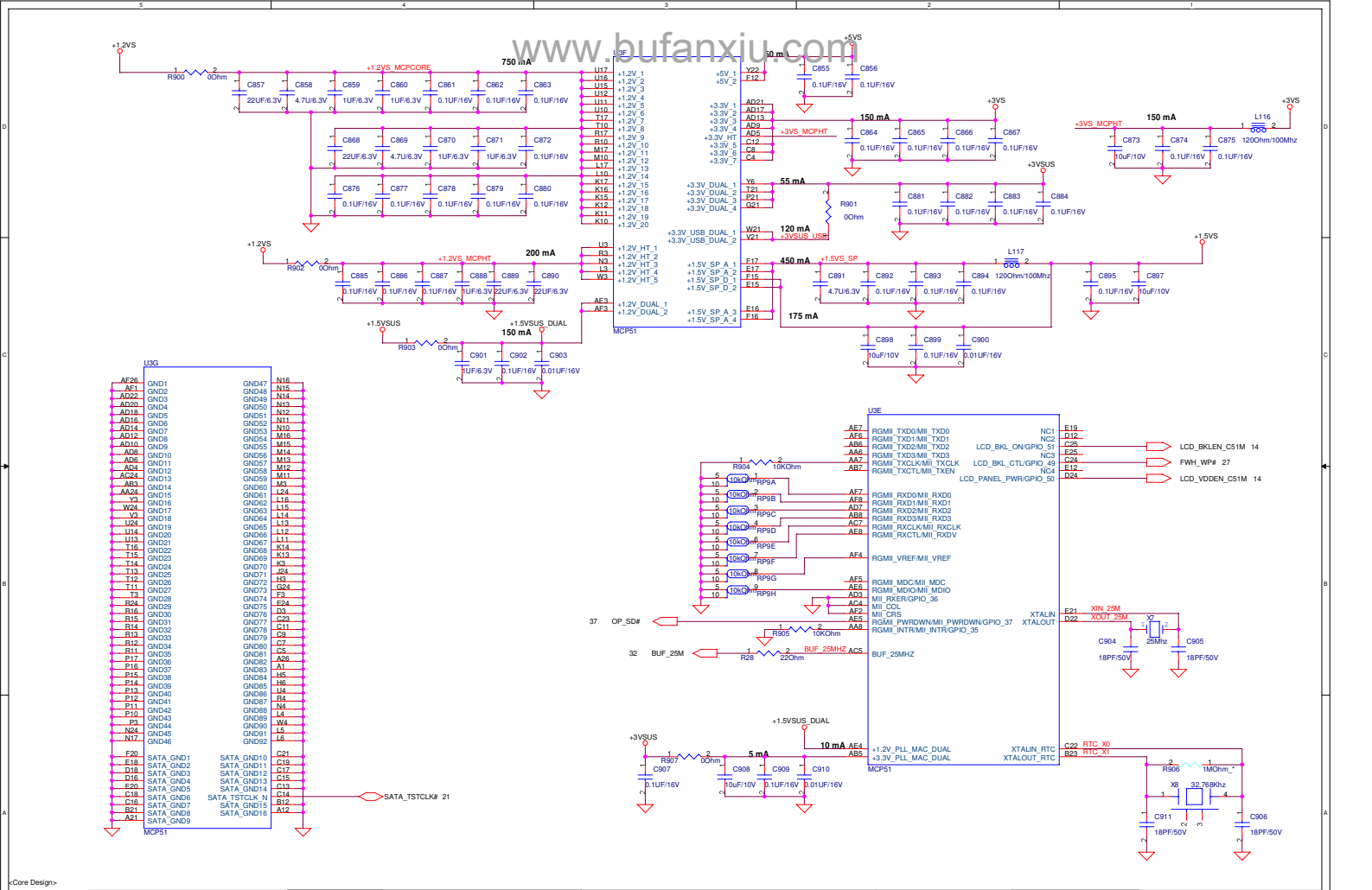
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 20 OF 55	DESCRIPTION: MCP51 PCI	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

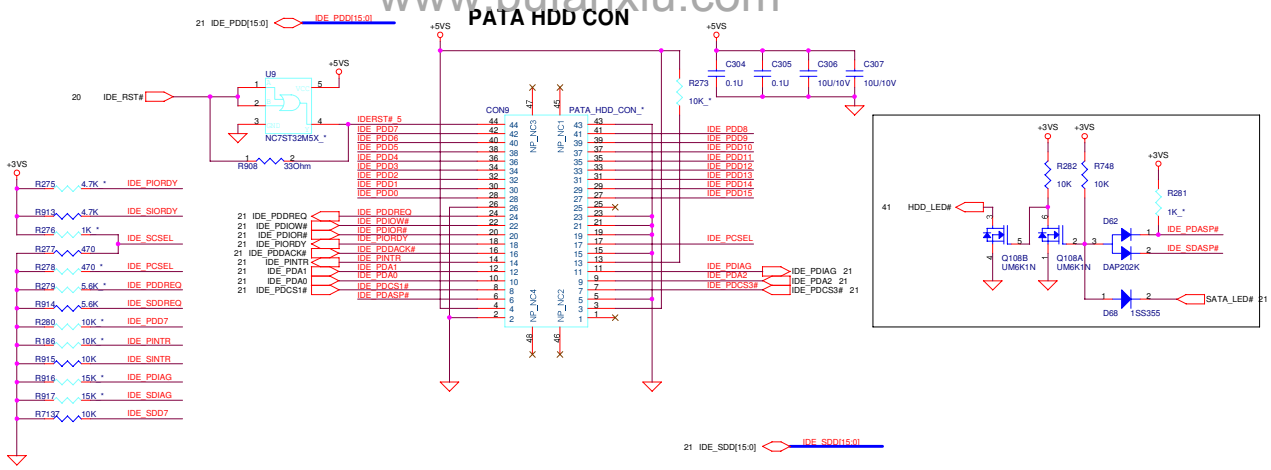
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 21 OF 55		RELEASE DATE :	

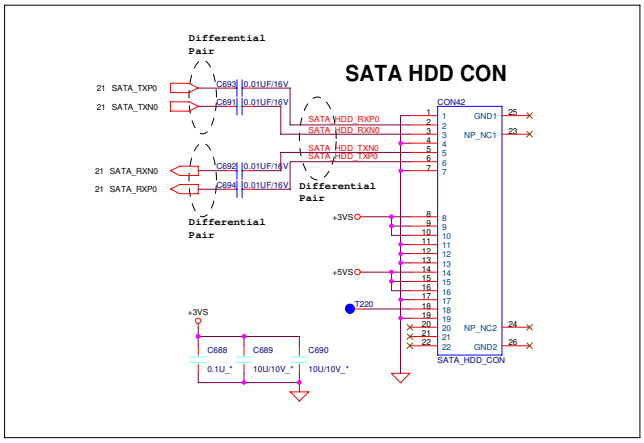


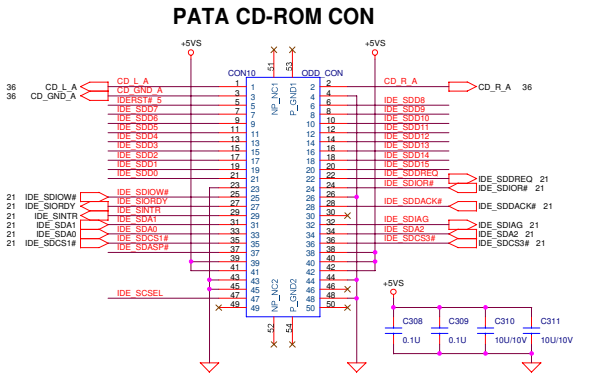


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PWR/GND	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 23 OF 55		RELEASE DATE :	



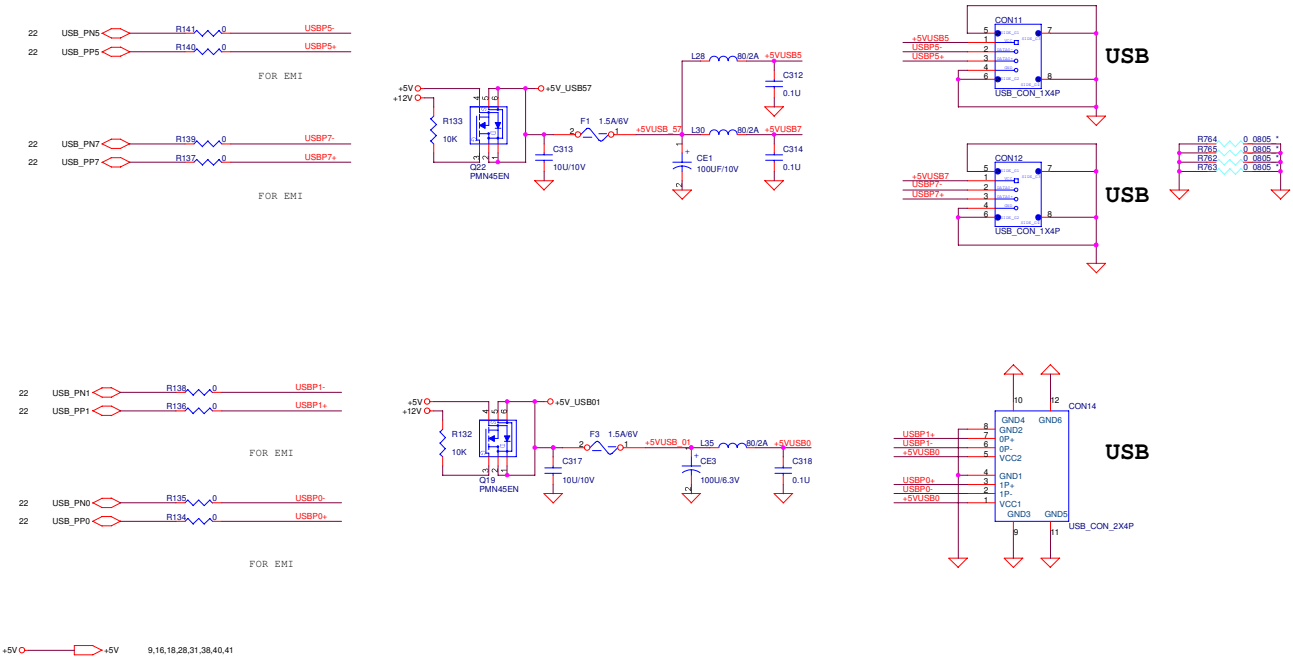




+3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30,31,34,36,38,39,41,48,61,70
+5VS 14,18,23,28,29,36,37,38,39,40,41,61
+5V 9,16,18,25,28,31,38,40,41

<Core Design>

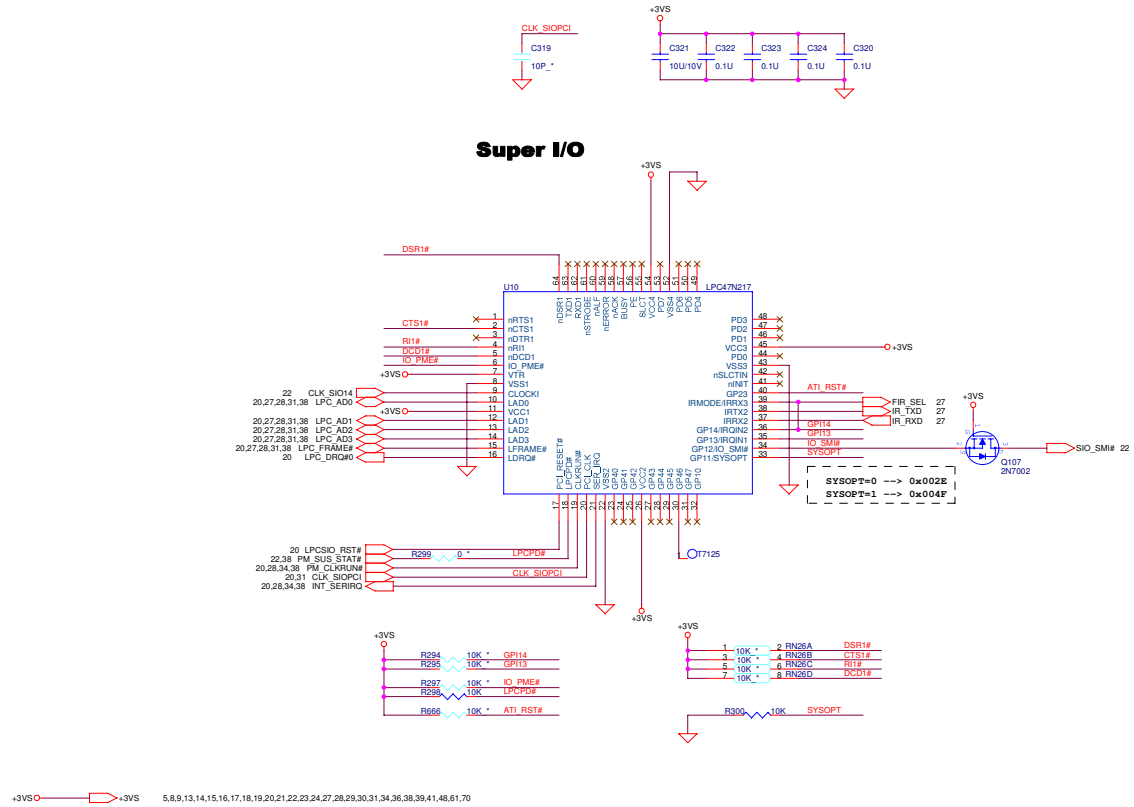
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 24 OF 55	DESCRIPTION: HDD & CD-ROM CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME :
		SHEET 25 OF 55		RELEASE DATE :

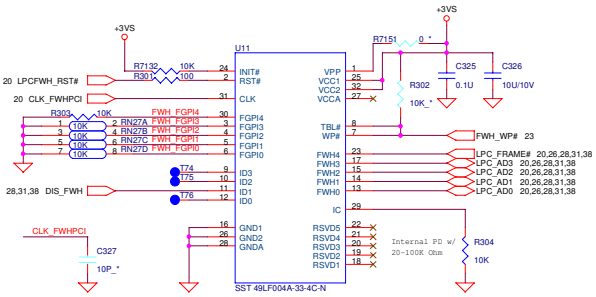
DESIGN ENGINEER : Albert Su



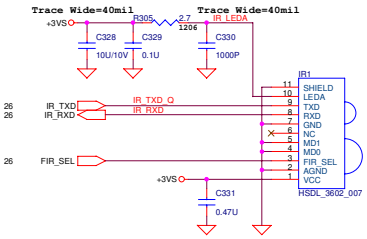
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,27,28,29,30,31,34,36,38,39,41,48,61,70

<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 26 OF 55		RELEASE DATE :	



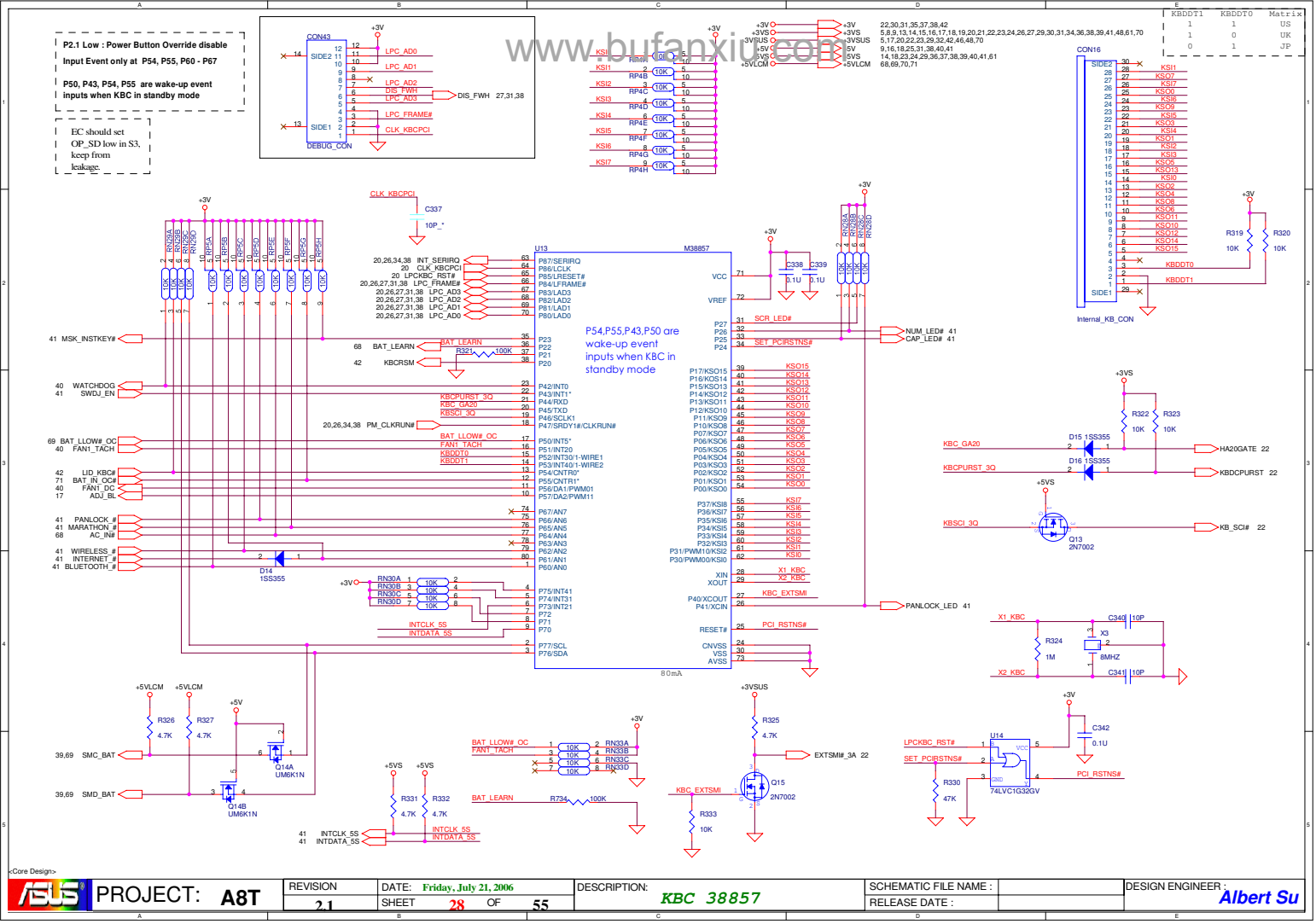
PLCC32 Socket Part Number :
12G043400324
Graphics from:
05-001005111



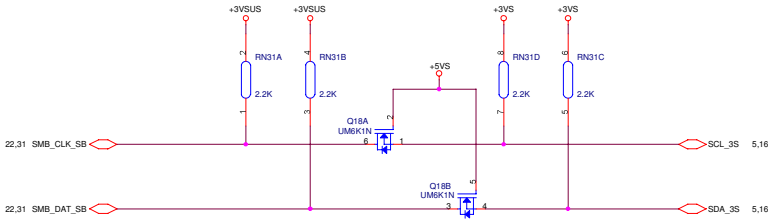
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

<Core Design>

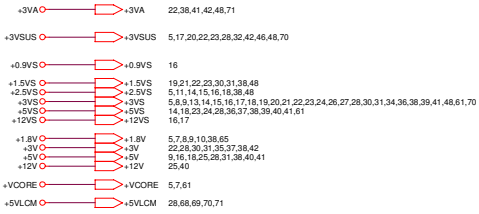
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: BIOS , IR	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 27 OF 55		RELEASE DATE :	



MCP51

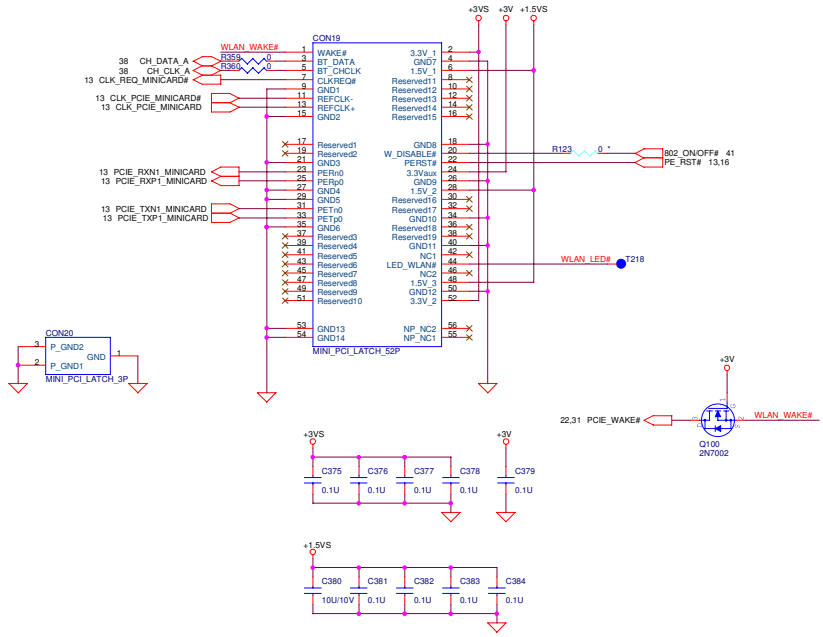


Termal Sensor,
TPM



<Core Design>

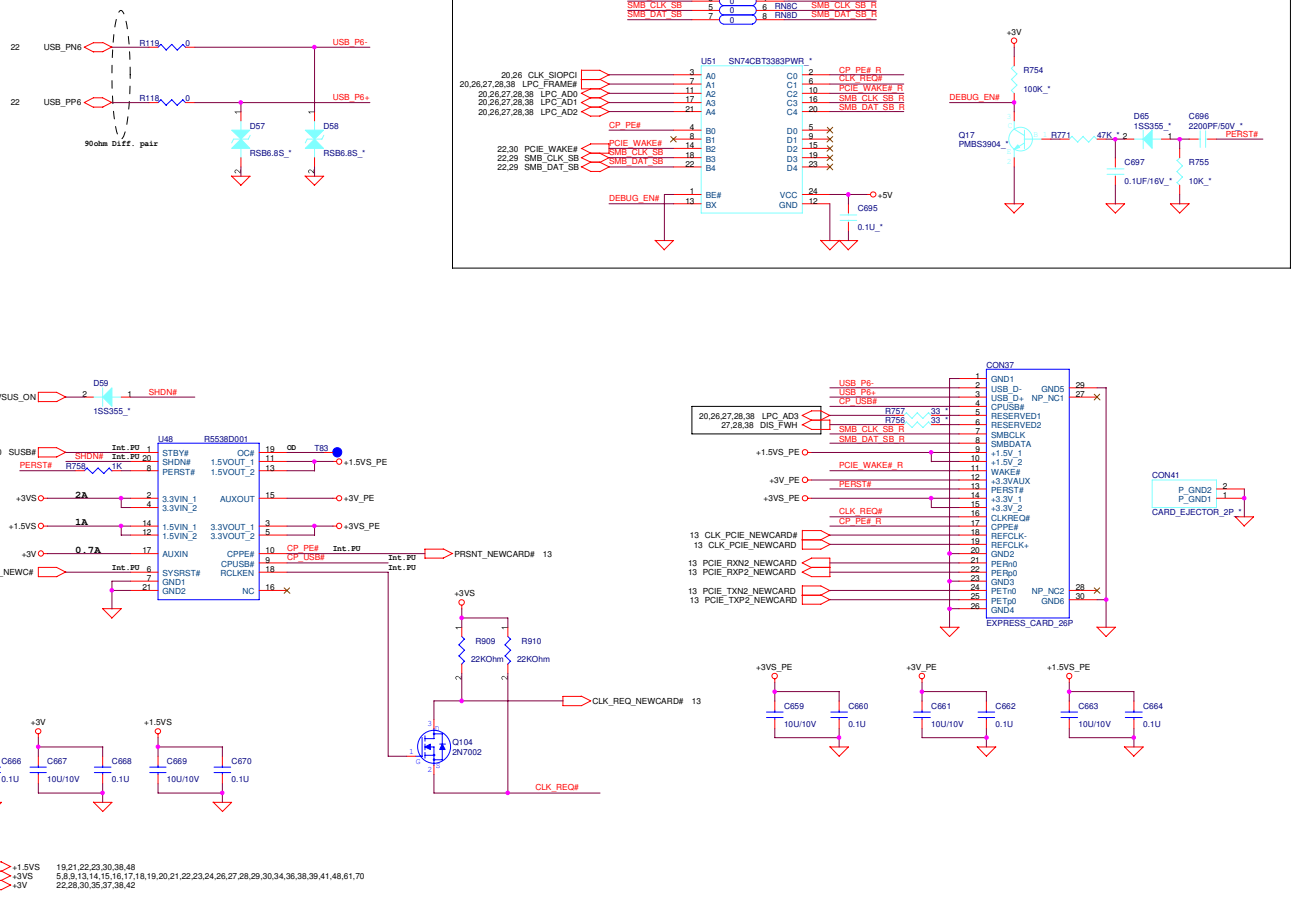
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 29 OF 55		RELEASE DATE :	



+1.5VS +1.5VS 19,21,22,23,31,38,48
+3V +3V 22,28,31,35,37,38,42
+3VS +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,31,34,36,38,39,41,48,61,70

<Core Design>

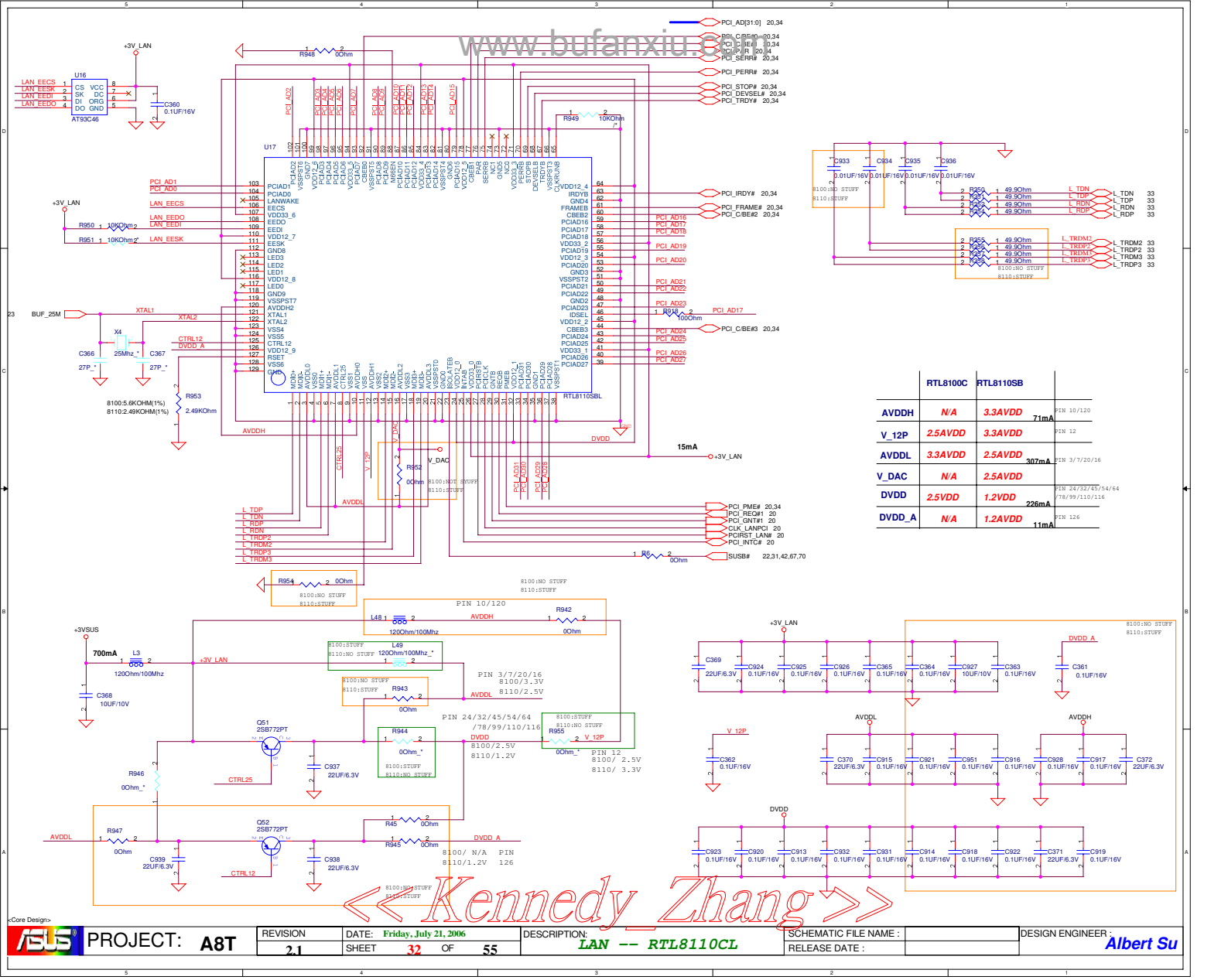
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 30 OF 55	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



+1.5VS 19,21,22,23,30,38,48
+3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,34,36,38,39,41,48,61,70
+3V 22,28,30,35,37,38,42

<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 31 OF 55	DESCRIPTION: NEW CARD	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

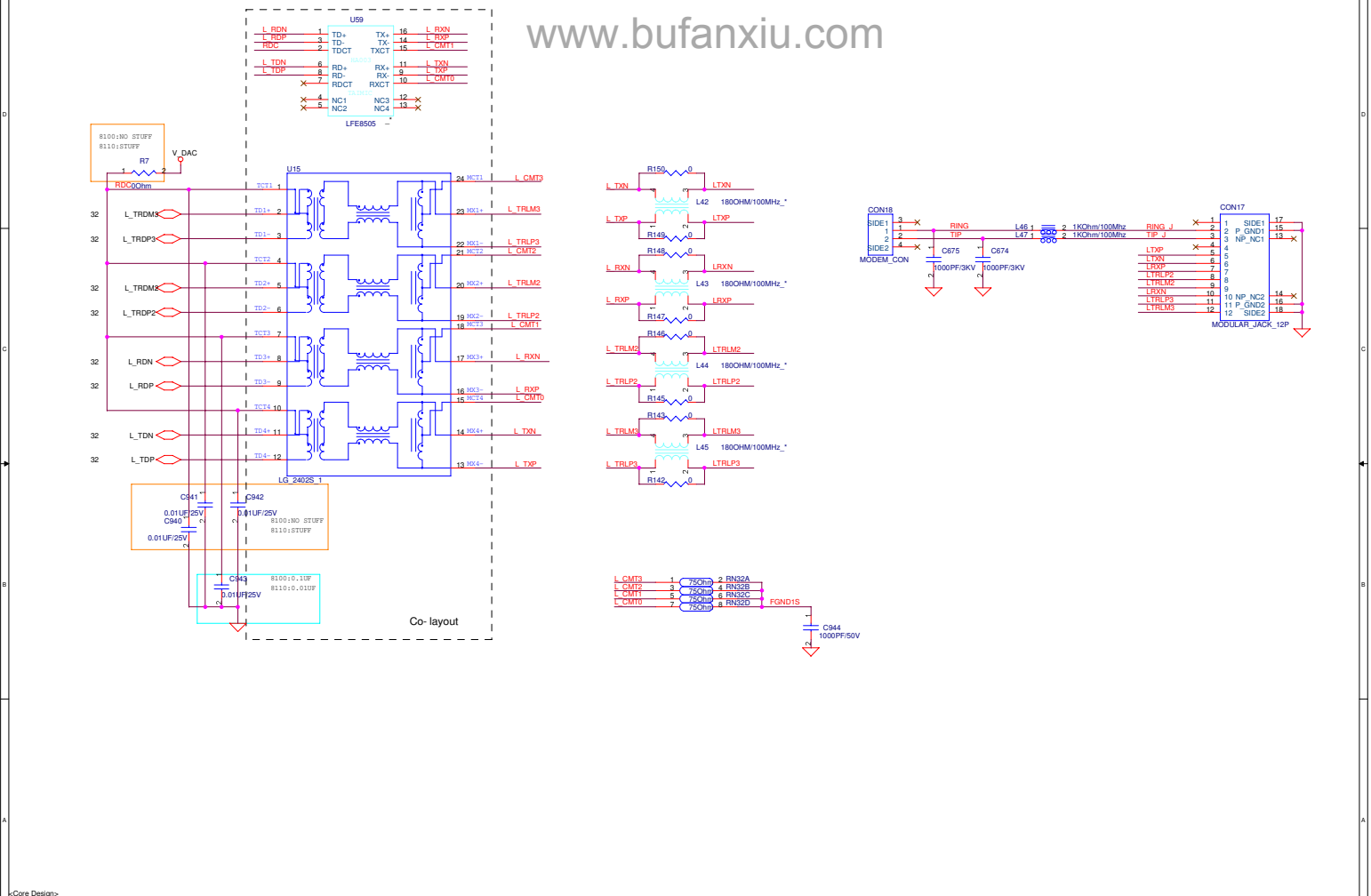


	RTL8100C	RTL8110SB	
AVDDH	N/A	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	307mA PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	
DVDD	2.5VDD	1.2VDD	226mA PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.2AVDD	11mA PIN 126

71mA

<Core Design>

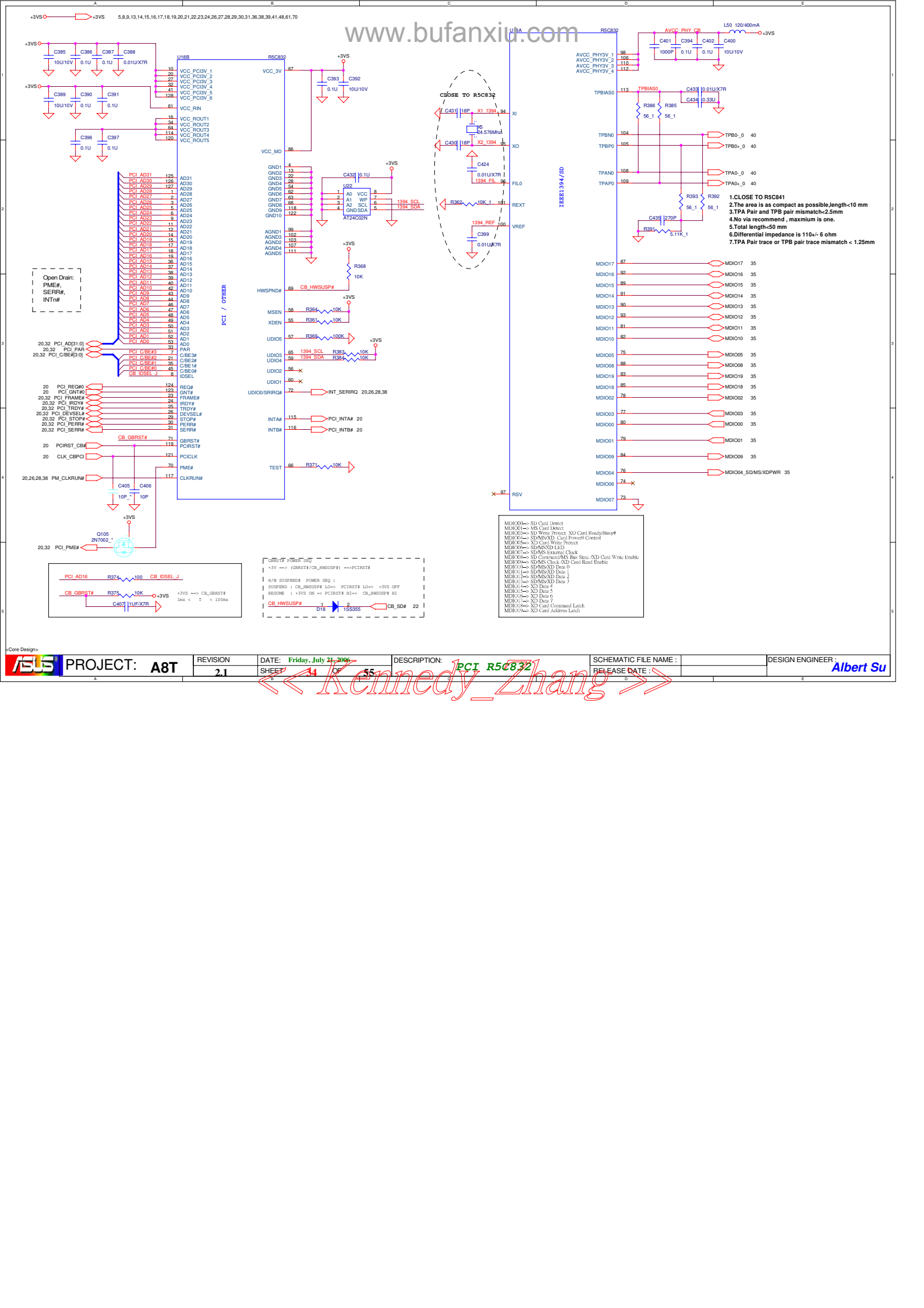
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 32 OF 55	DESCRIPTION: LAN -- RTL8110CL	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



<Core Design>

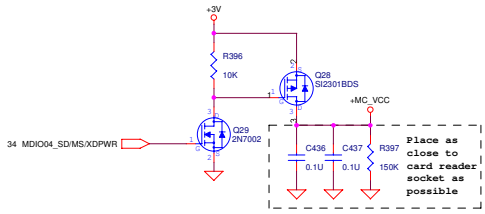
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME :		DESIGN ENGINEER : Albert Su
		SHEET 33 OF 55		RELEASE DATE :		

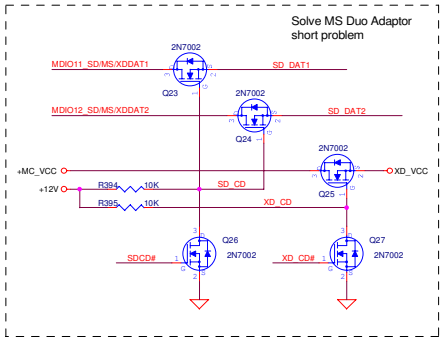
<< Kennedy_Zhang >>

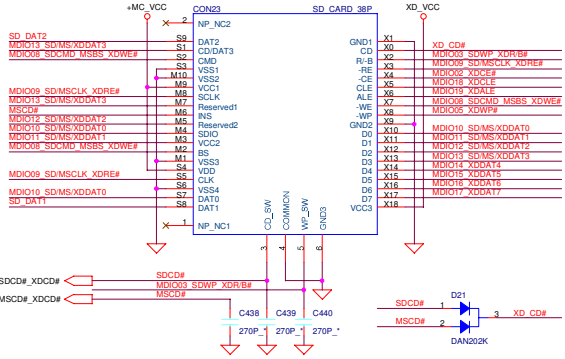


<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: PCI R5C832	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 44 OF 55		RELEASE DATE :	



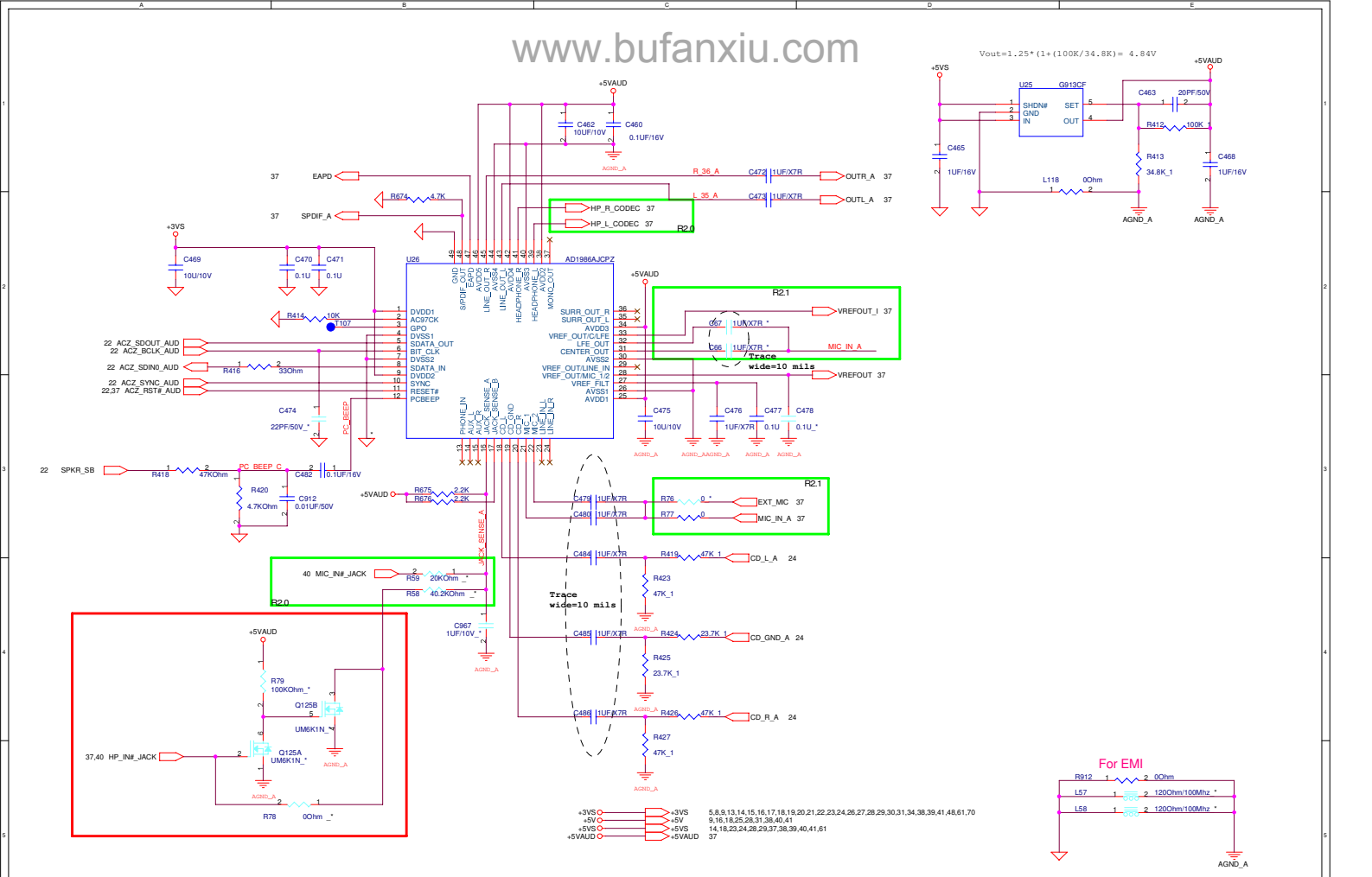




+3V +3V 22,28,30,31,37,38,42
+12V +12V 25,37,40,67

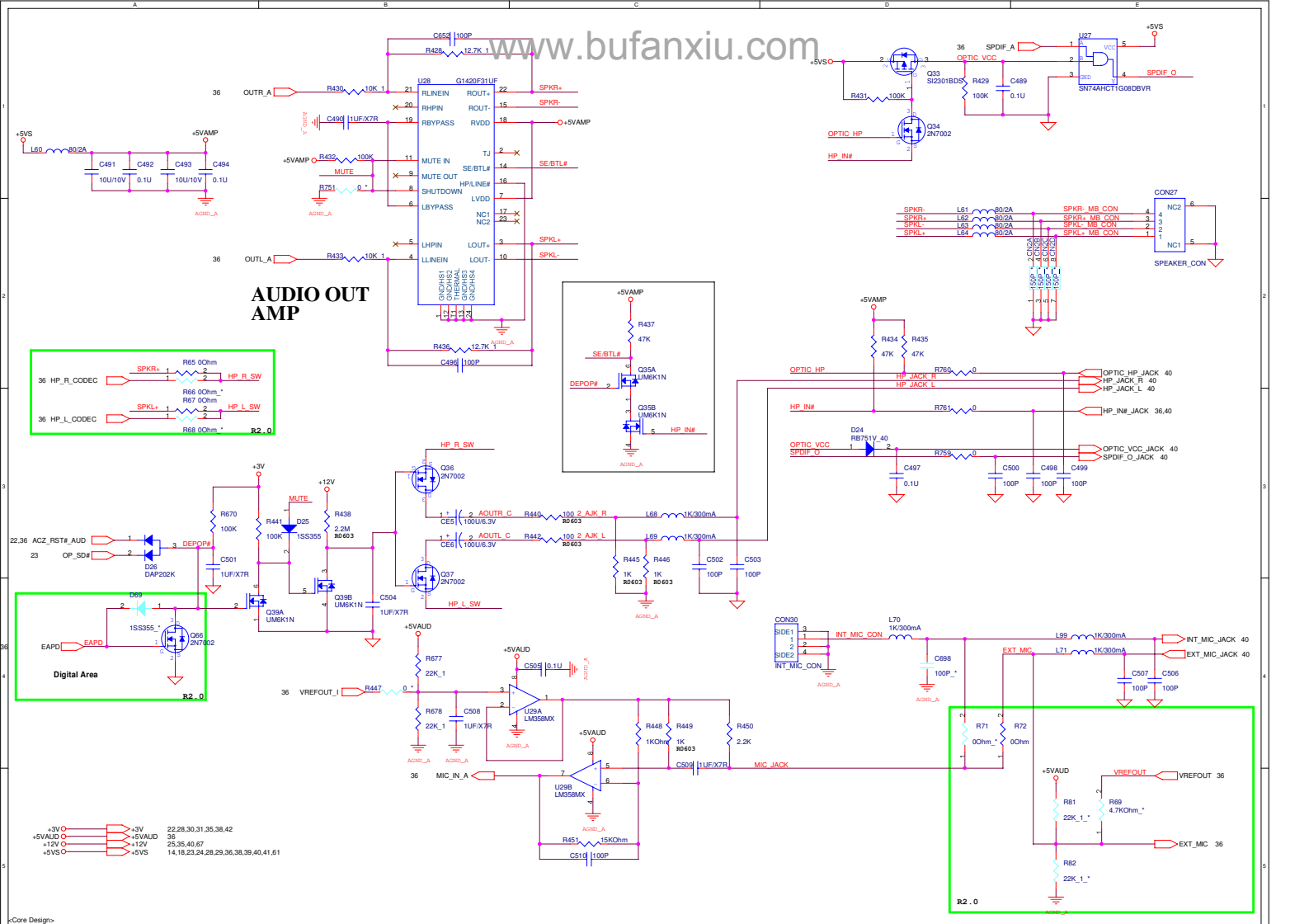
<Core Design>

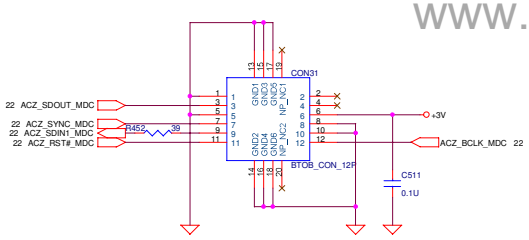
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 35 OF 55	DESCRIPTION: 4 IN 1 CONN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



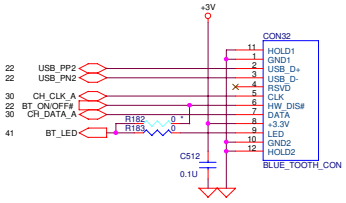
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 36 OF 55	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
					RELEASE DATE :	

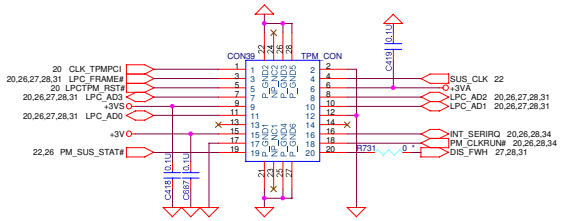




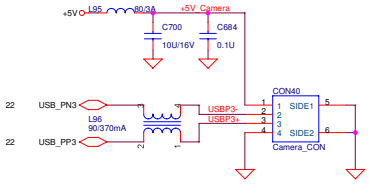
Azalia MDC MODEM CON



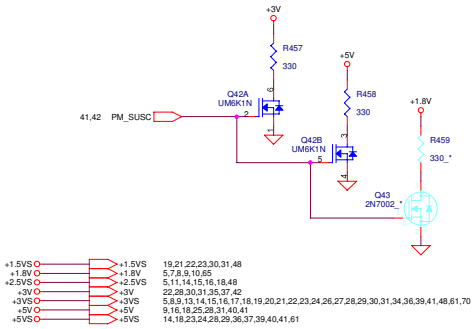
Bluetooth Module CON

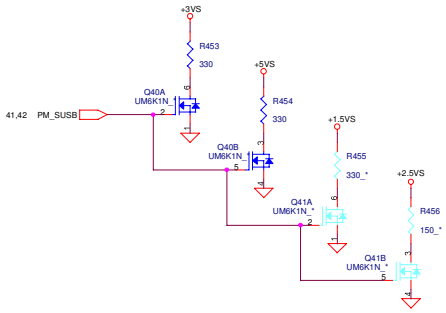


TPM Module CON



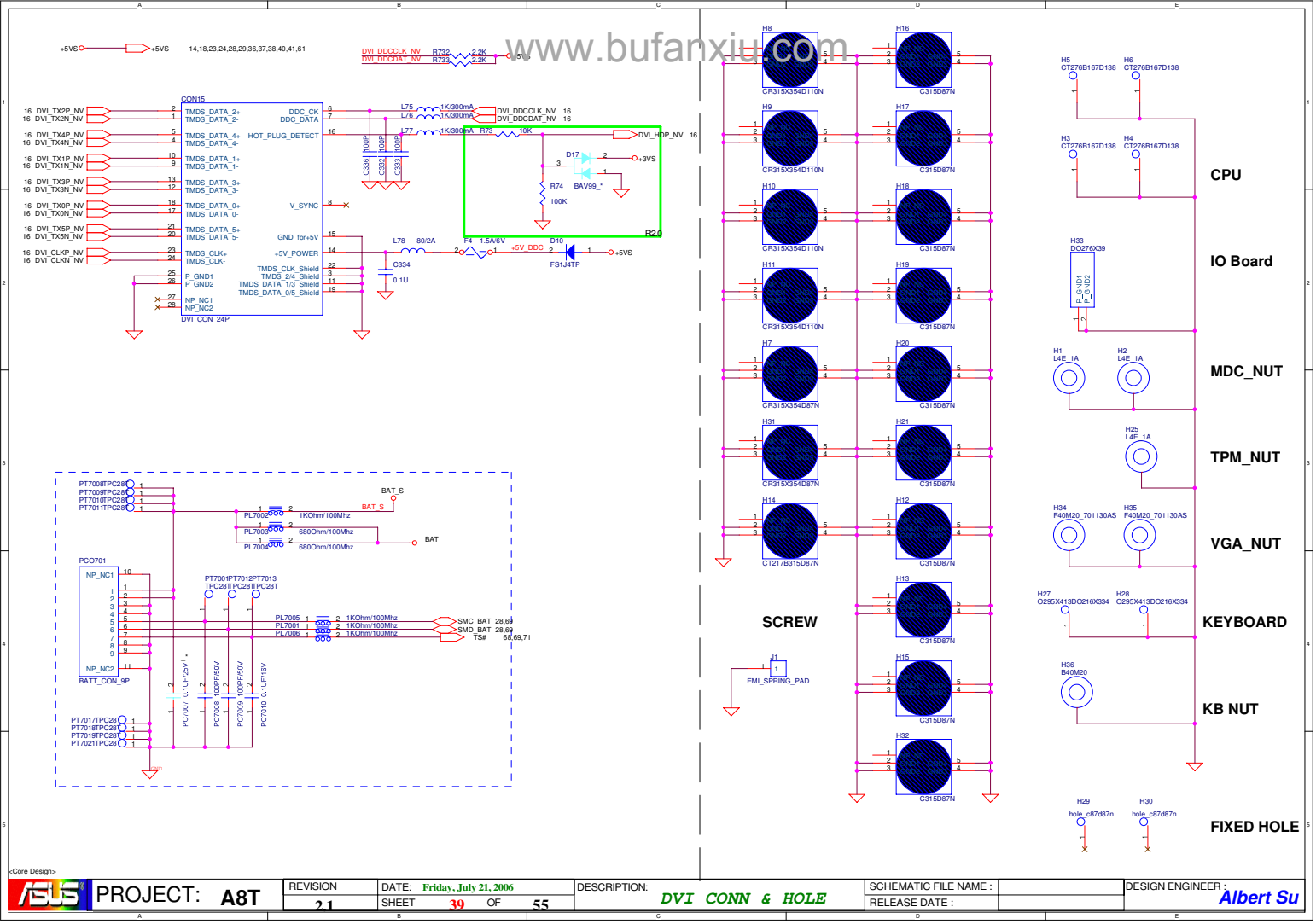
Camera Module CON





<Core Design>

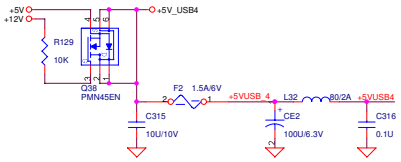
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MDC,B/T,TPM,Camera & DISCHG	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 38 OF 55		RELEASE DATE :	

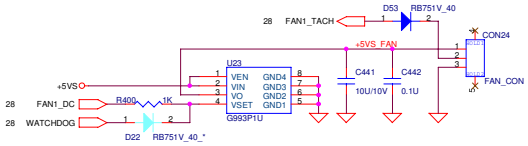


<Core Design>

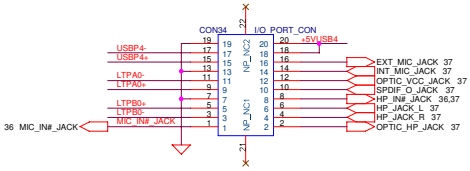
PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 39 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>

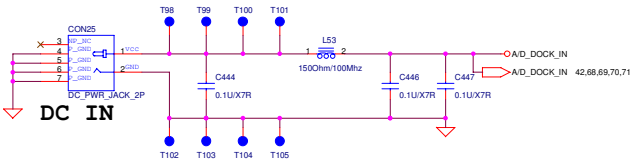




FAN CONTROL



I/O PORT

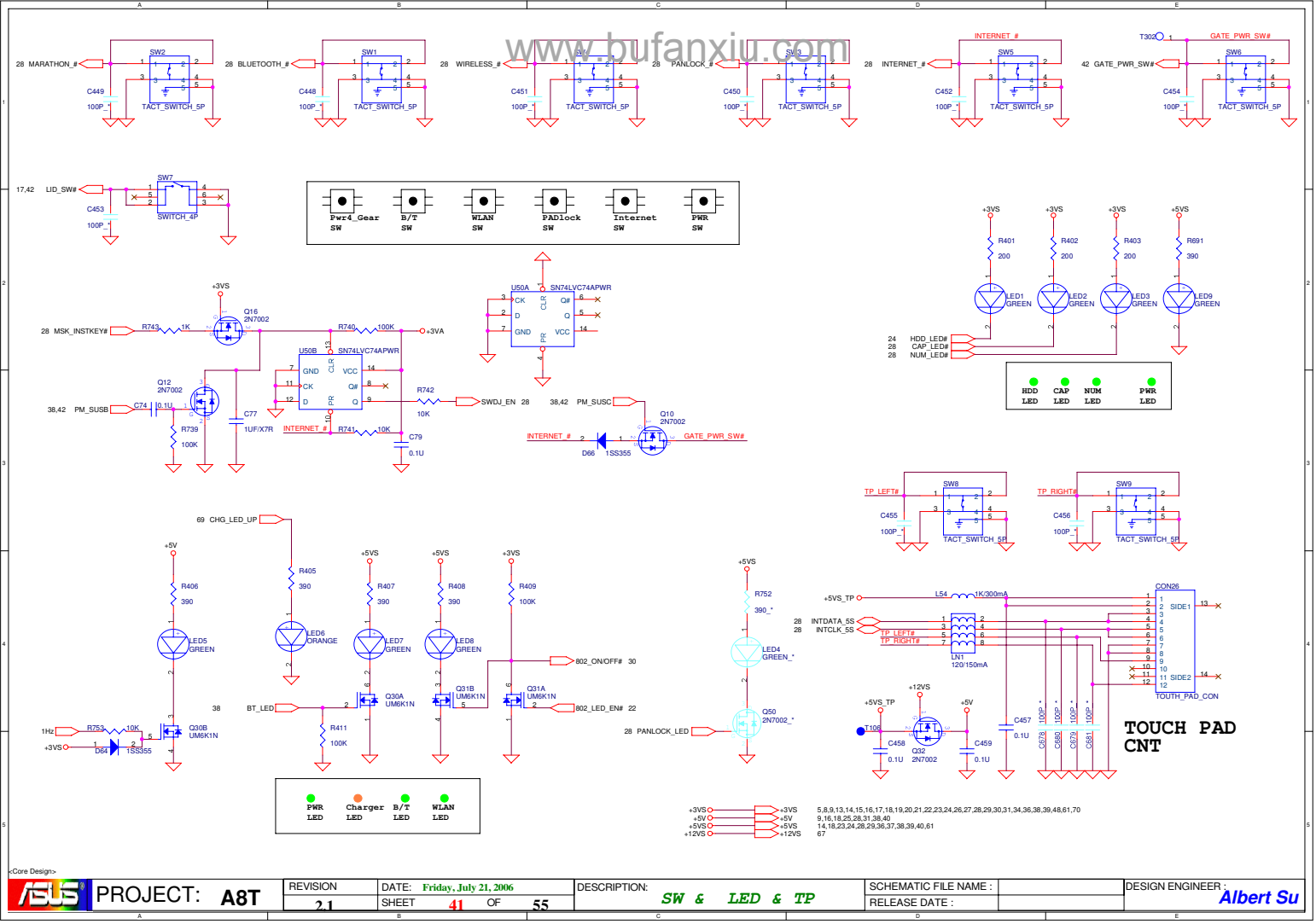


DC IN

ACIN_CONN

<Core Design>

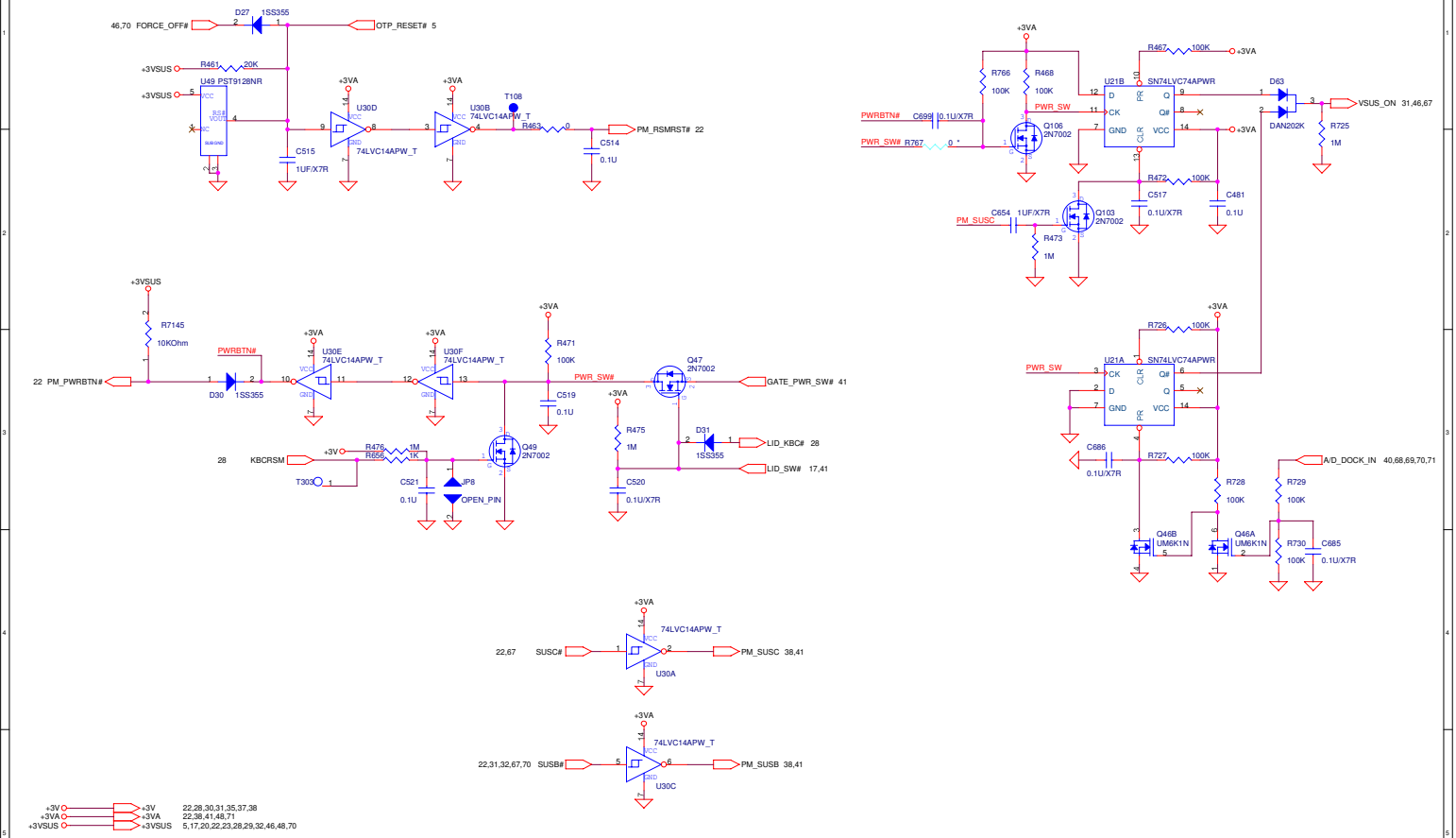
PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET 40 OF 55	DESCRIPTION: FAN_CTRL & ACIN	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su



TOUCH PAD CNT

<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 41 OF 55		RELEASE DATE :	



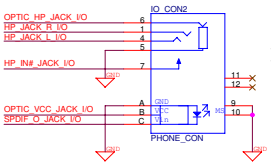
<Core Design>

PROJECT: A8T	REVISION 2.1	DATE: Friday, July 21, 2006	SHEET 42 OF 55	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : Albert Su

Revision History

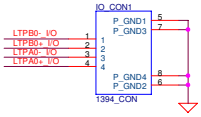
Power:

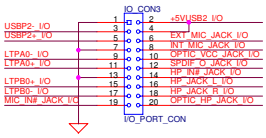
System:

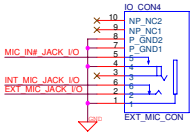


LINE_OUT
SPDIF

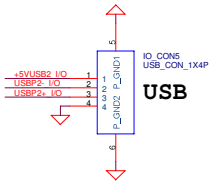
1394A



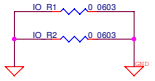




MIC



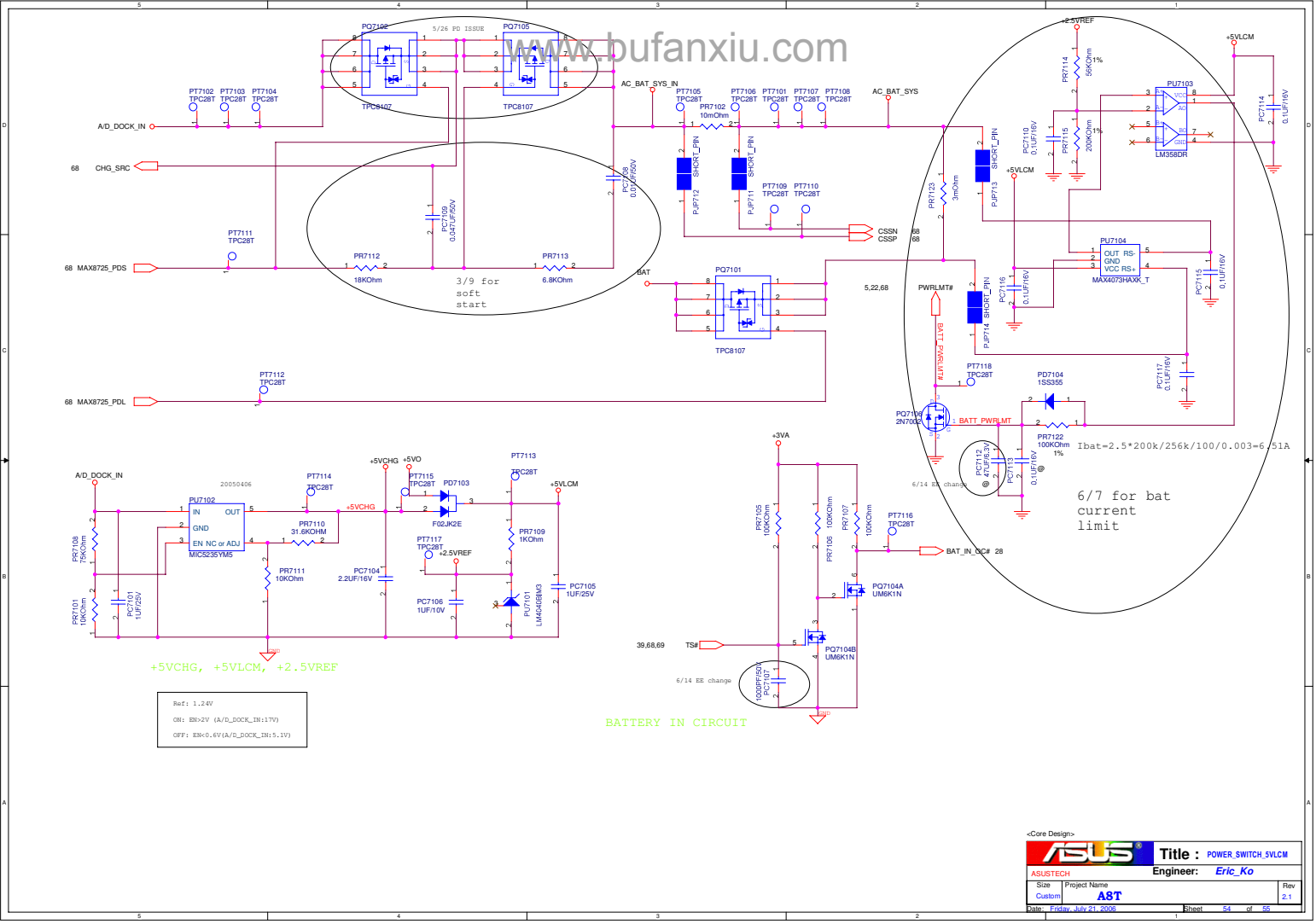
USB



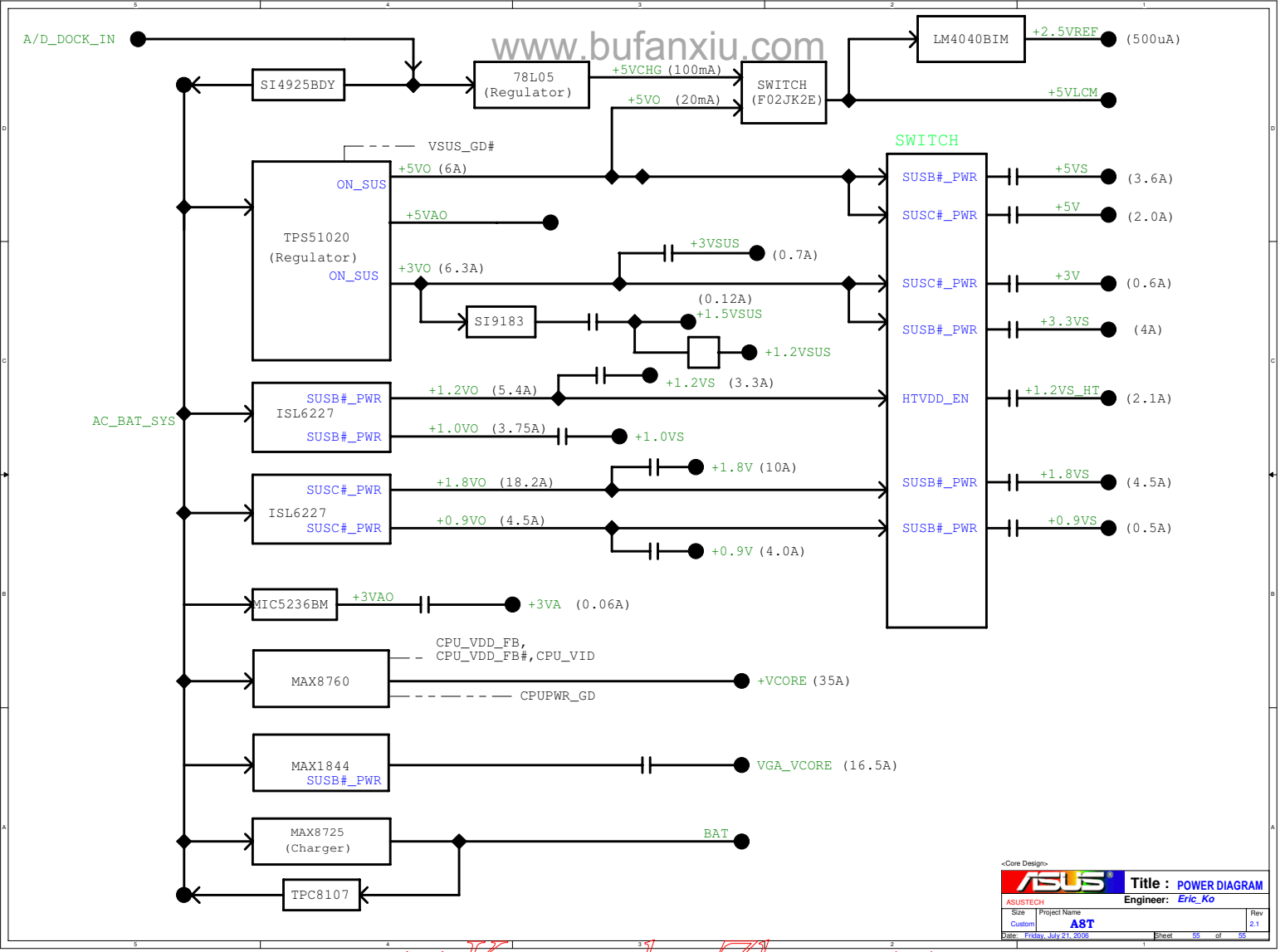
<Core Design>

PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: I/O PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 44 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



<Core Design>

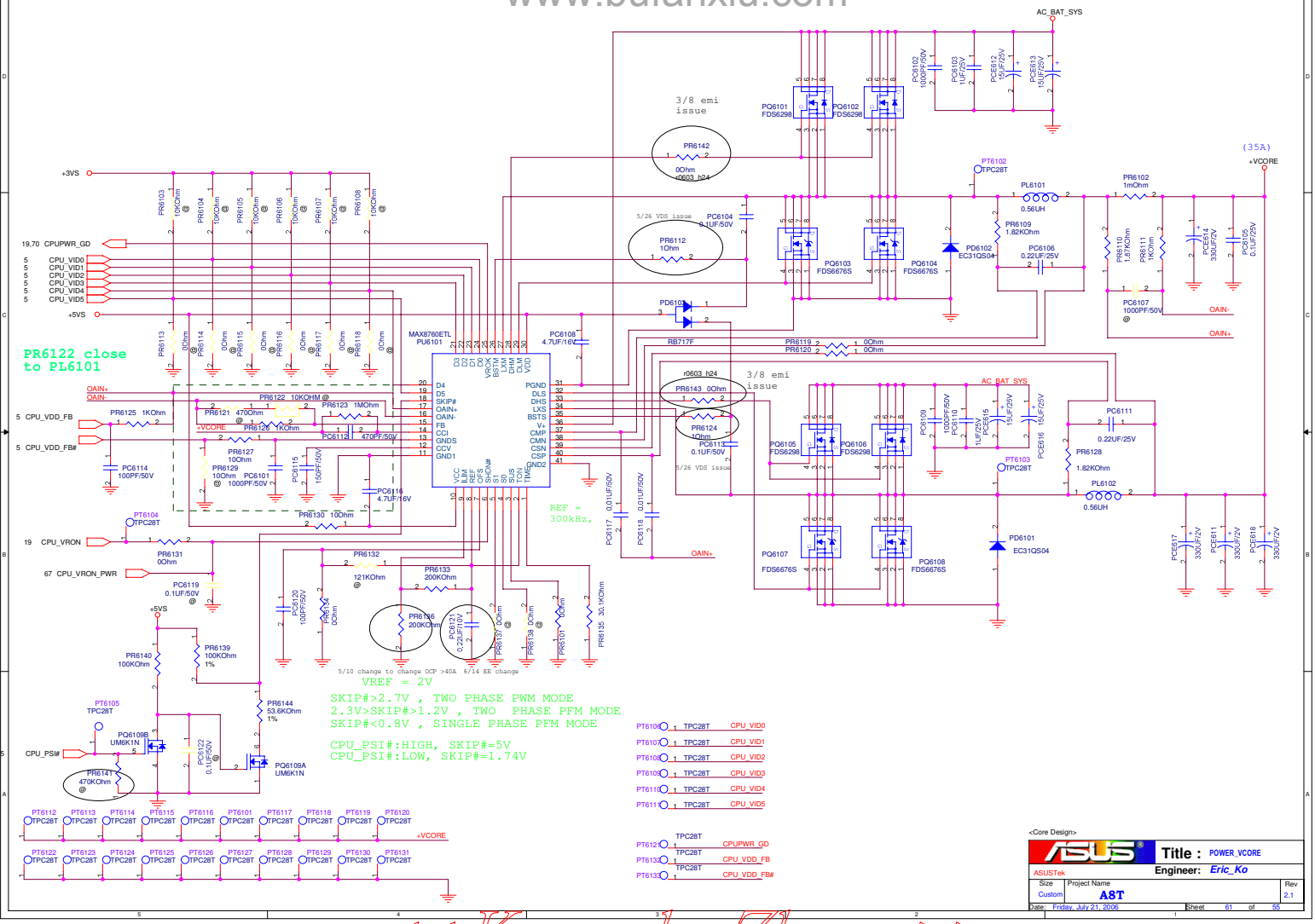
ASUSTECH

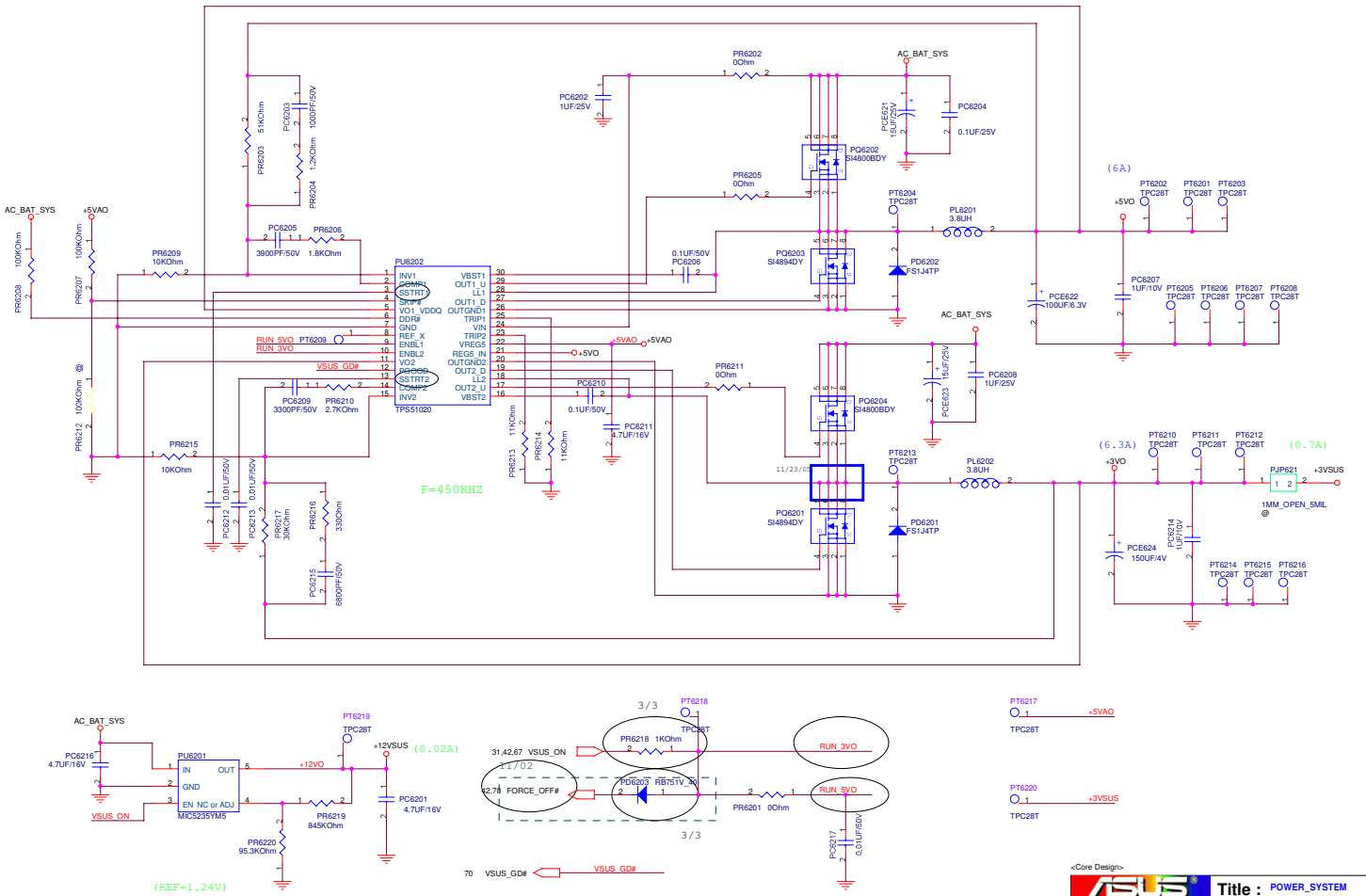
Title : POWER DIAGRAM

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

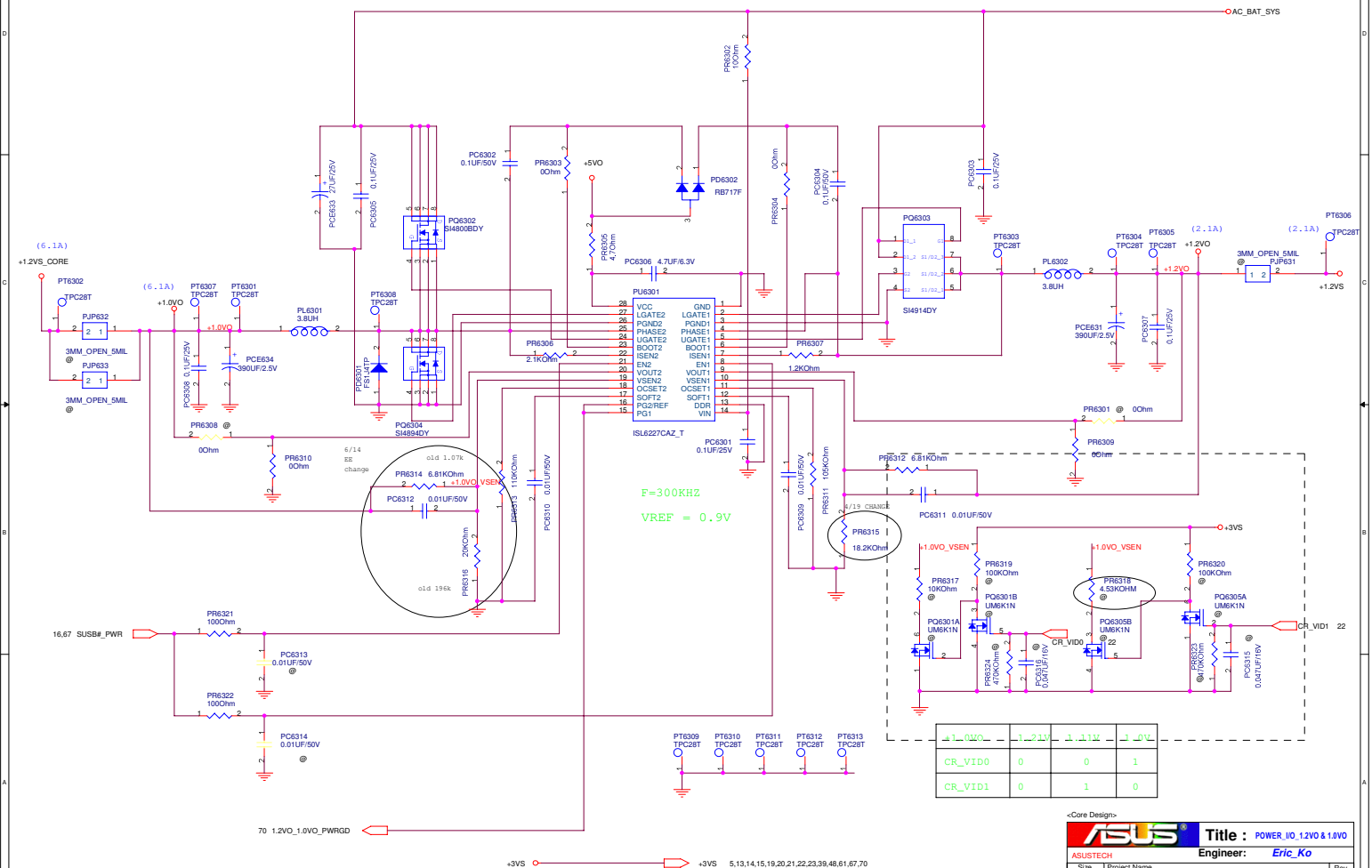
Date: Friday, July 21, 2006 Sheet 55 of 55





<Core Design>

ASUSTECH	Title : POWER_SYSTEM	
	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 62 of 55	



+1.0VO	1.2VO	1.1VO	1.0VO
CR_VID0	0	0	1
CR_VID1	0	1	0

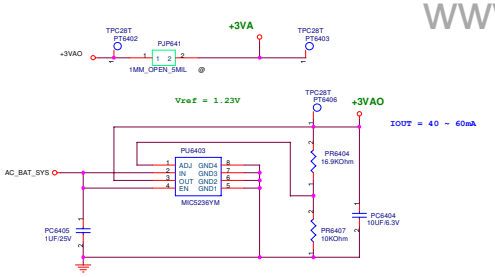
<Core Design>

Title : POWER_I/O_1.2VO & 1.0VO

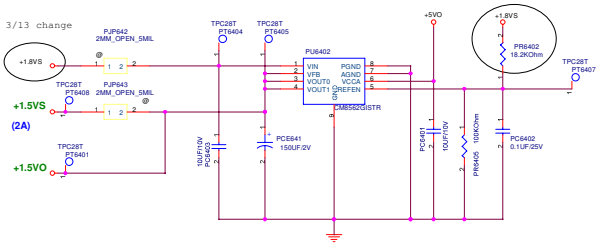
ASUSTECH Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

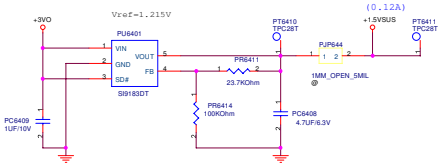
Date: Friday, July 21, 2006 Sheet 63 of 55



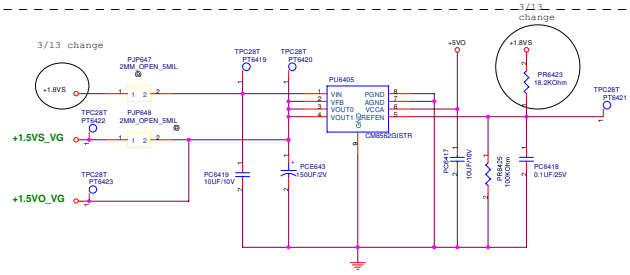
+3VA



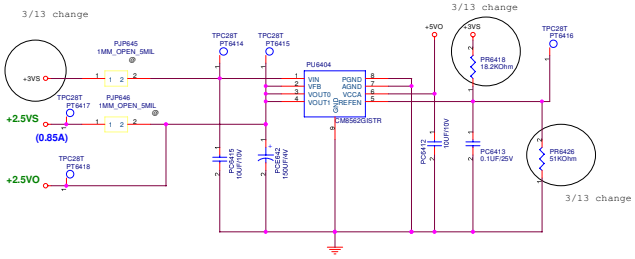
+1.5VS



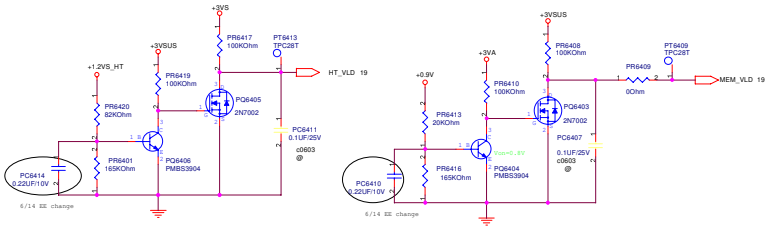
+1.5VSUS



+1.5VS_VGA

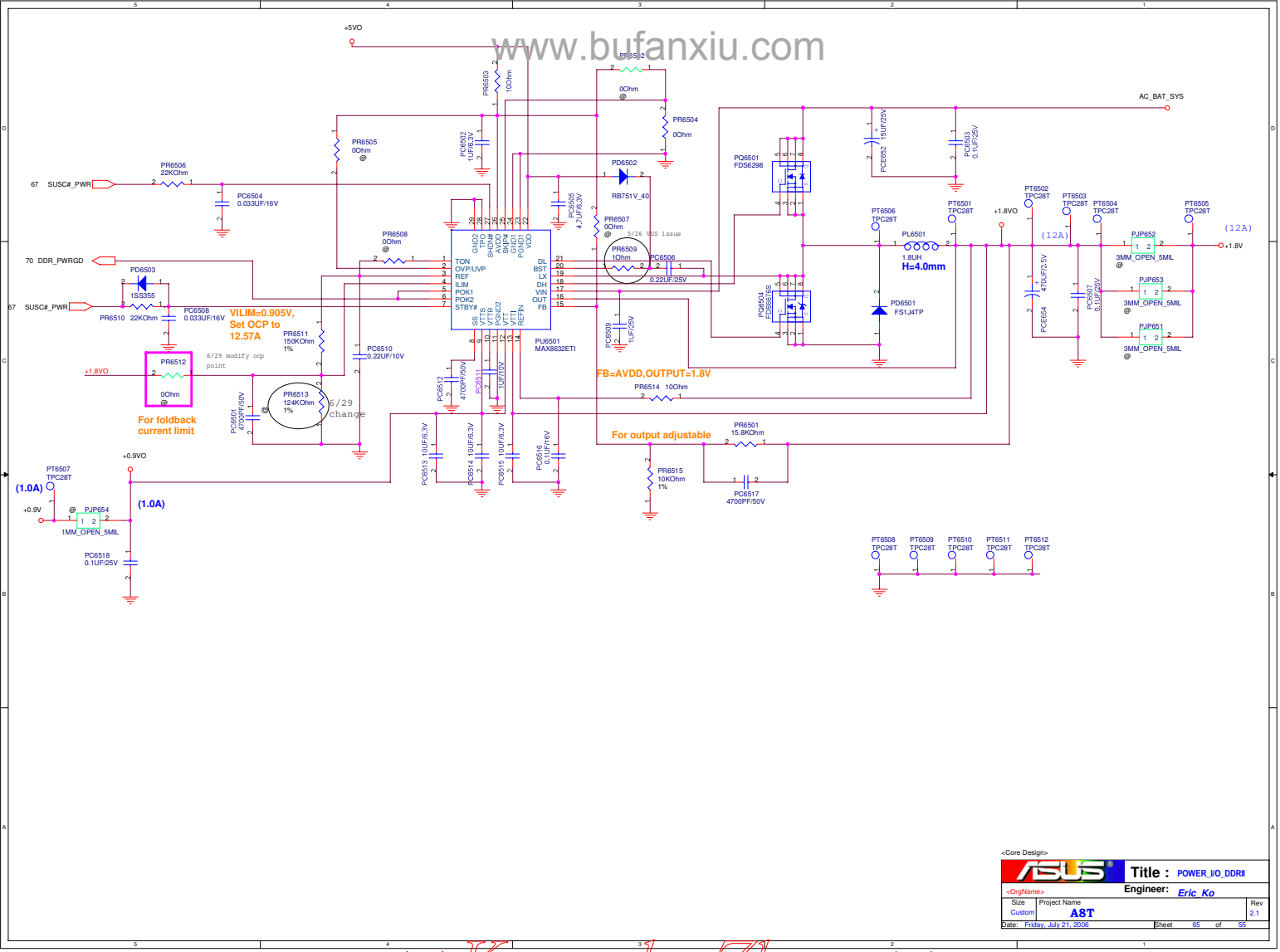


+2.5VS



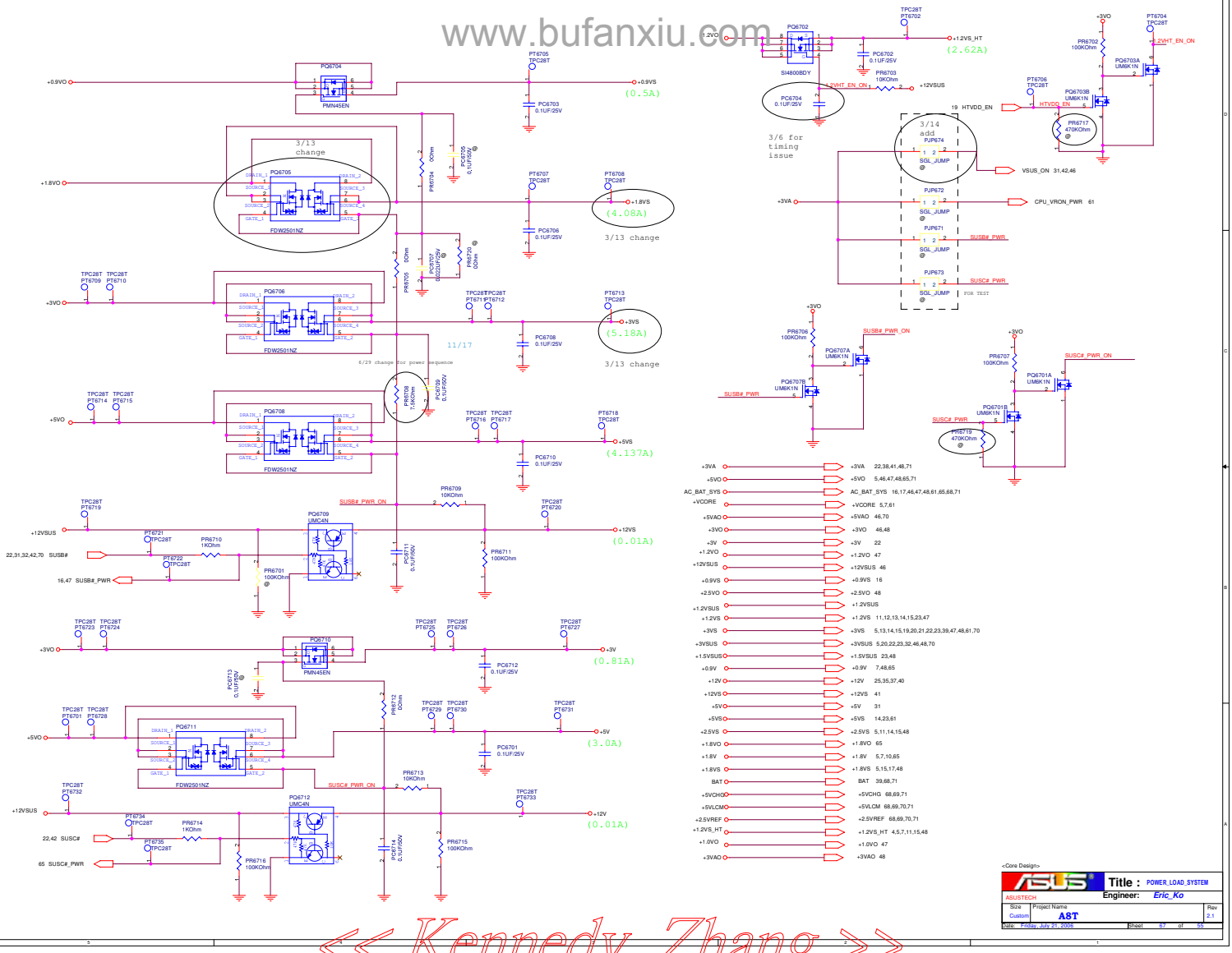
<Core Design>

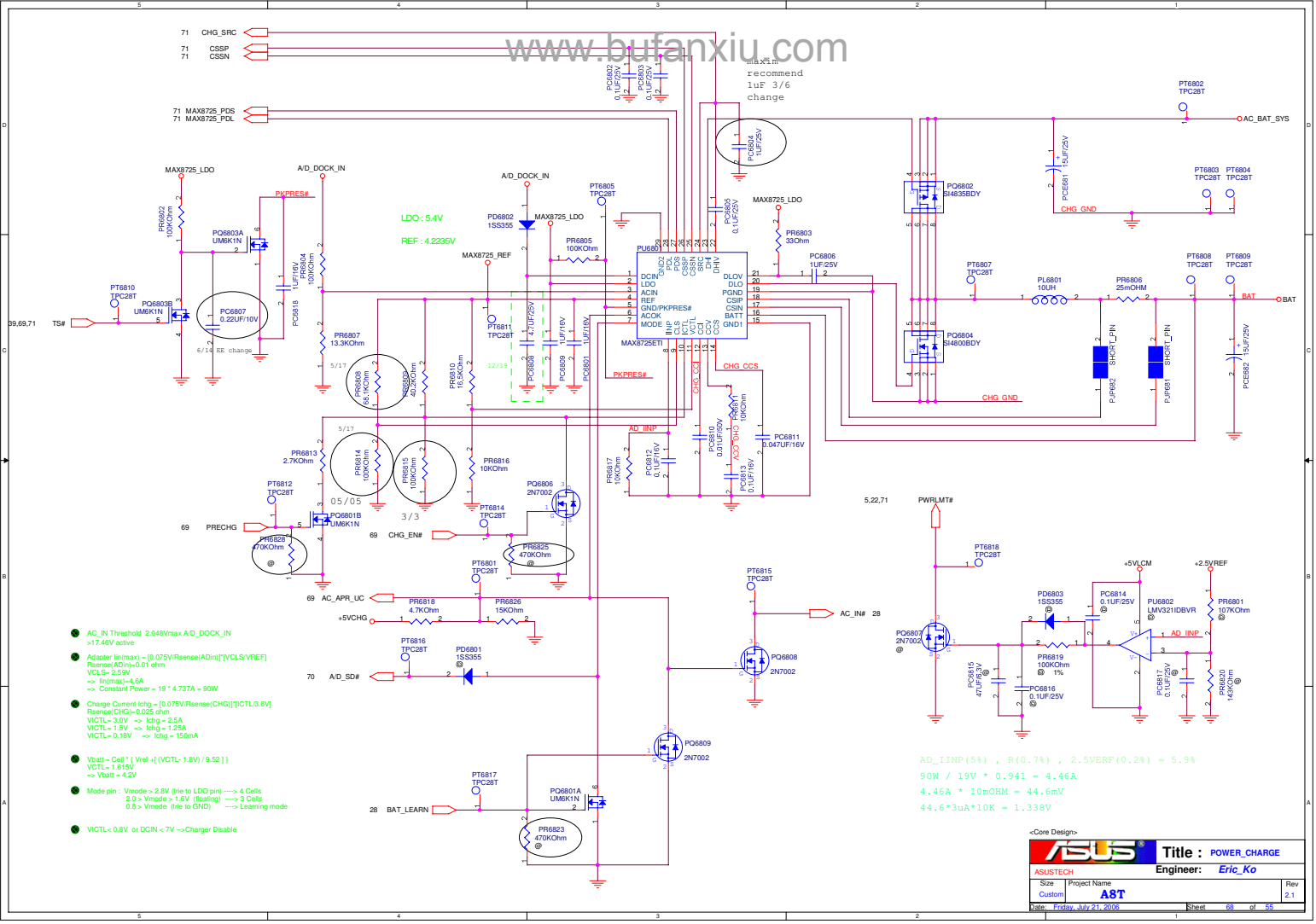
ASUSTeK	Title : POWER_IIO_LDO	
	Engineer: Eric_Ko	
Size: C	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 64 of 66	



<Core Design>

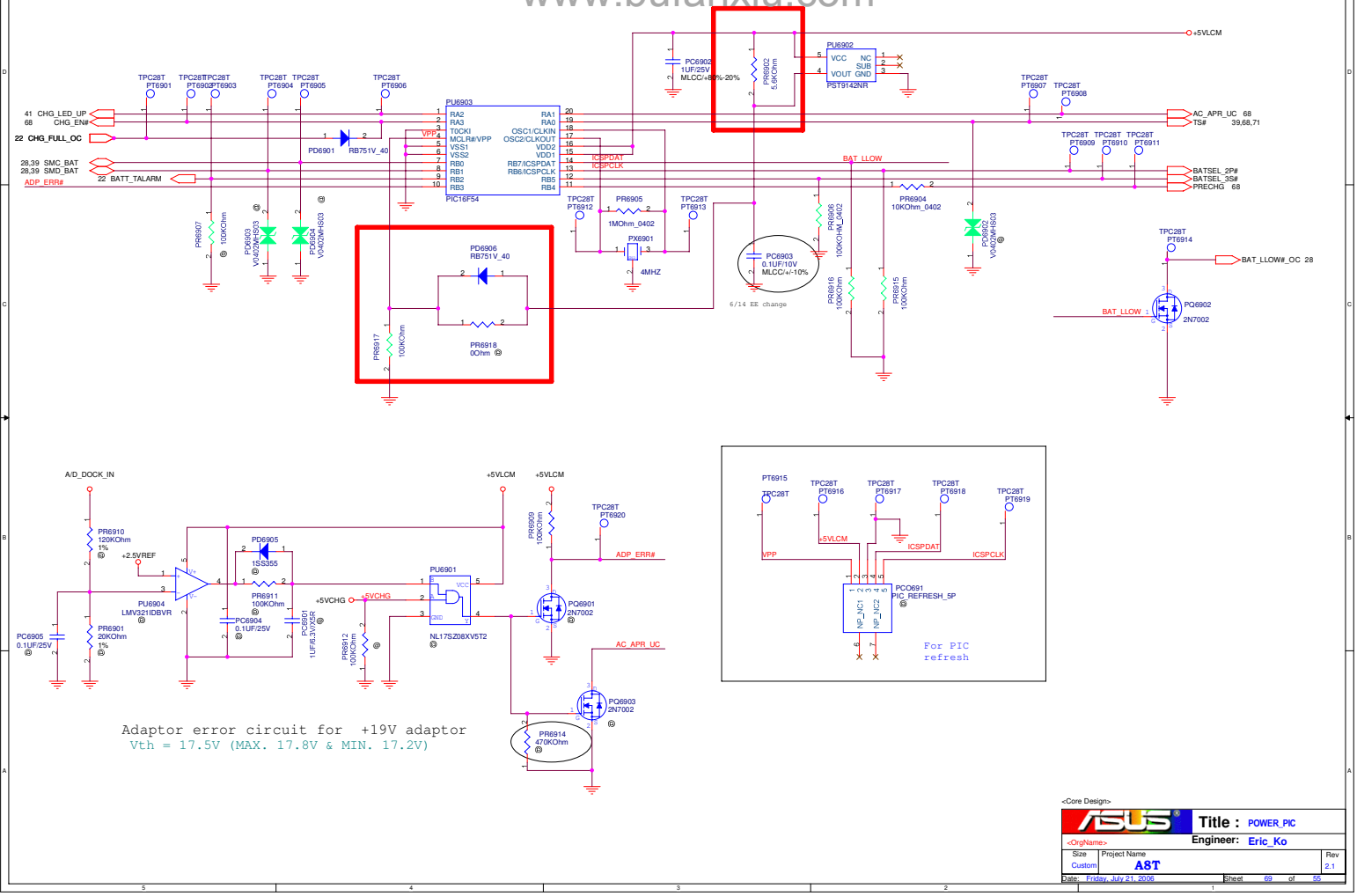
ASUS	Title : POWER_I/O_DDRII	
<OrgName>	Engineer: Eric_Ko	
Size: Custom	Project Name: A8T	Rev: 2.1
Date: Friday, July 21, 2006	Sheet 65 of 55	





<< Kennedy_Zhang >>

PIC16F54



<Core Design>

ASUS

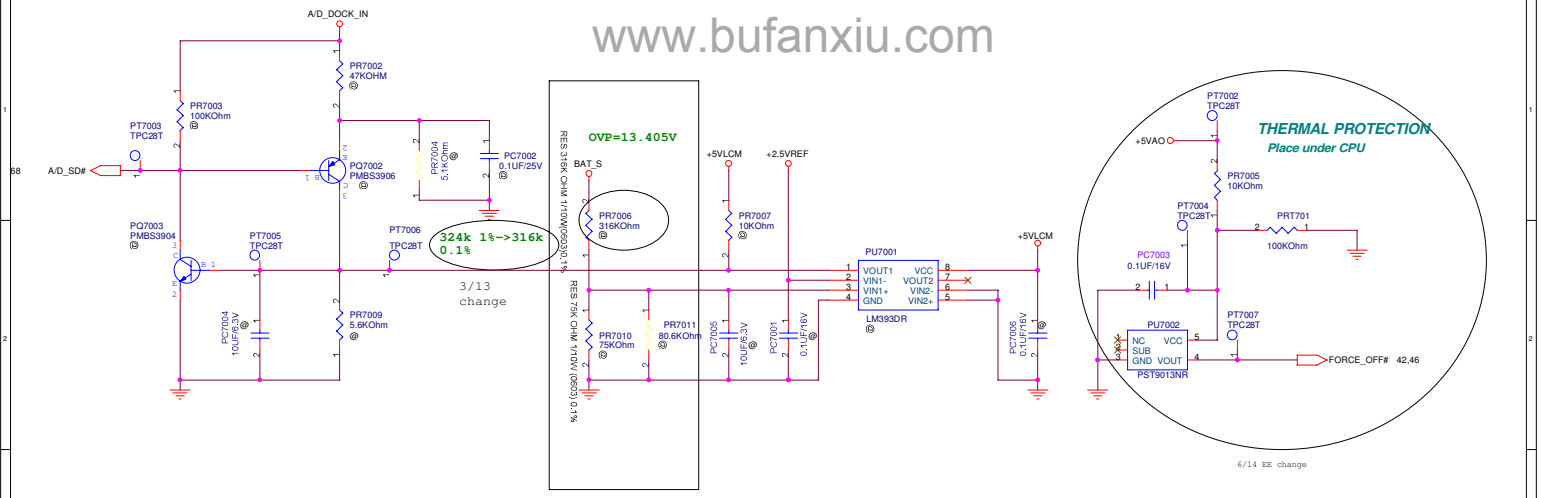
Title : POWER_PIC

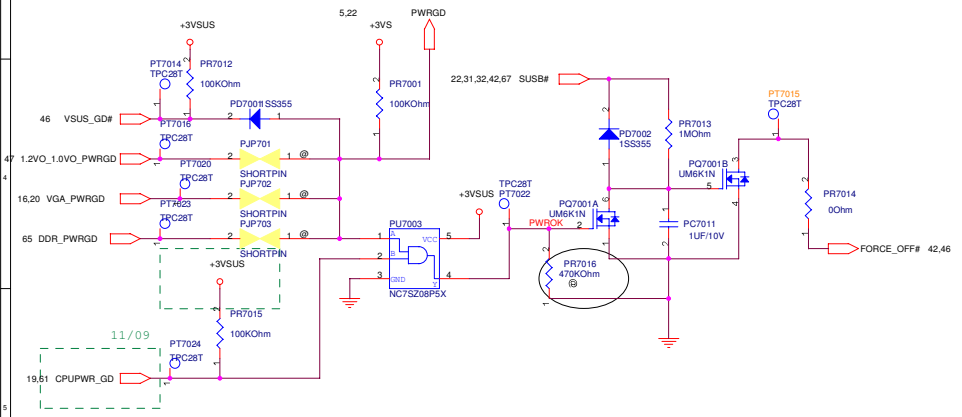
<OrgName>

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

Date: Friday, July 21, 2006 Sheet 69 of 55





<Core Design>

ASUSTECH

Title : POWER_PROTECT

Engineer: Eric_Ko

Size	Project Name	Rev
Custom	A8T	2.1

Date: Friday, July 21, 2006 Sheet 70 of 55