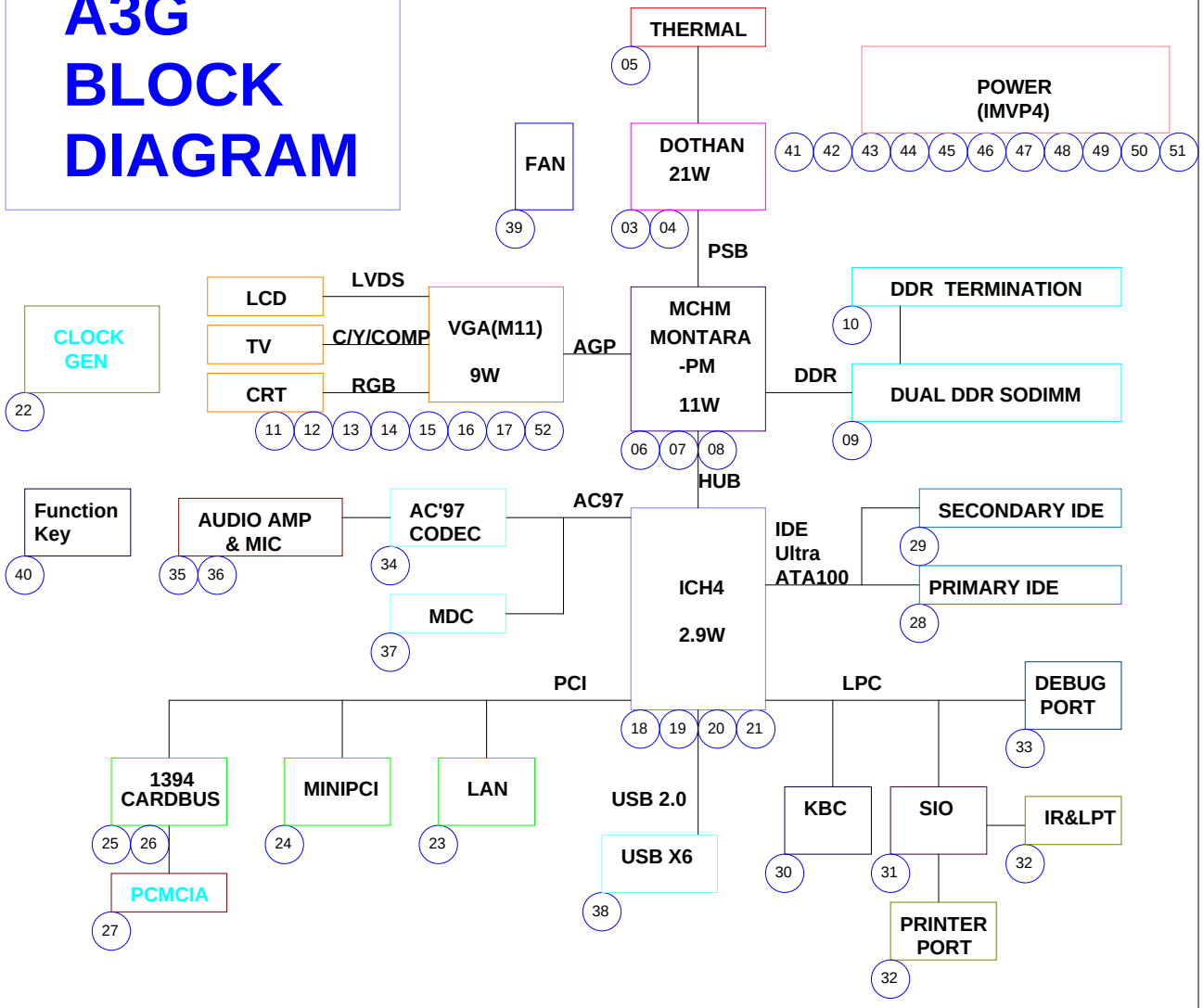
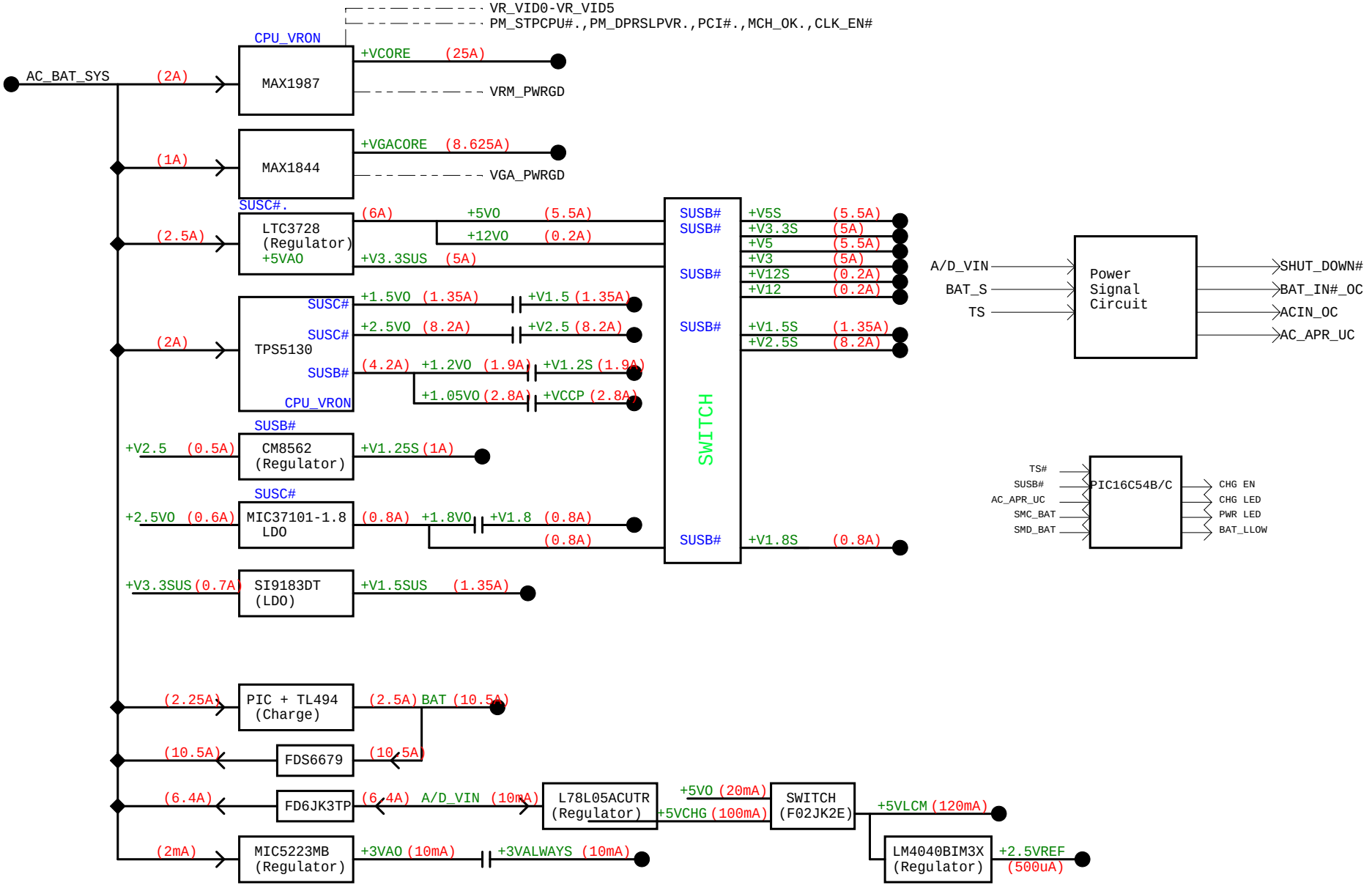
A3G BLOCK DIAGRAM



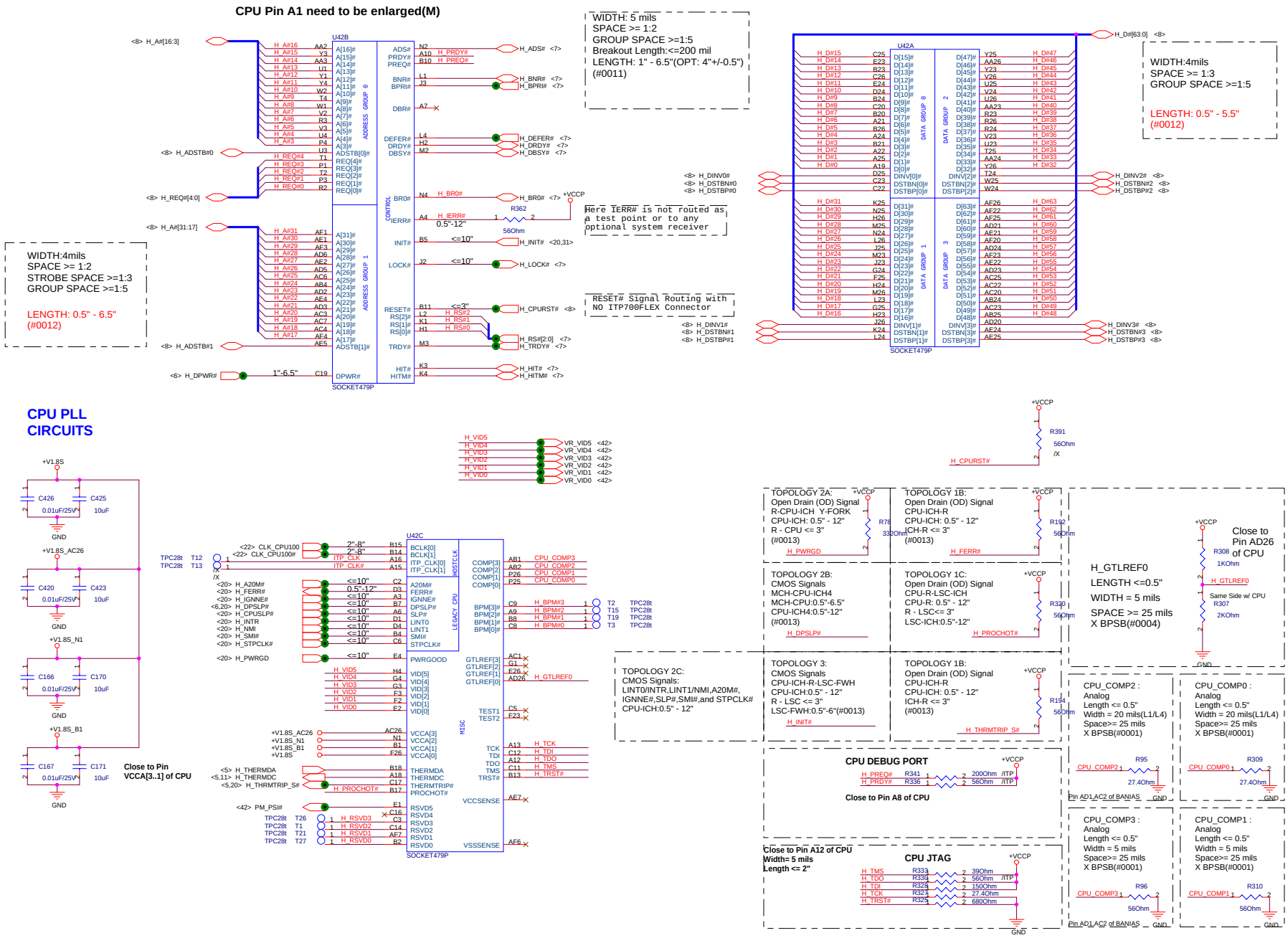
FILE LIST

01

ASUSTEK CO.,LTD.	Title : BLOCK DIAGRAM	
	Engineer: HD_NB TEAM	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 1 of 53	

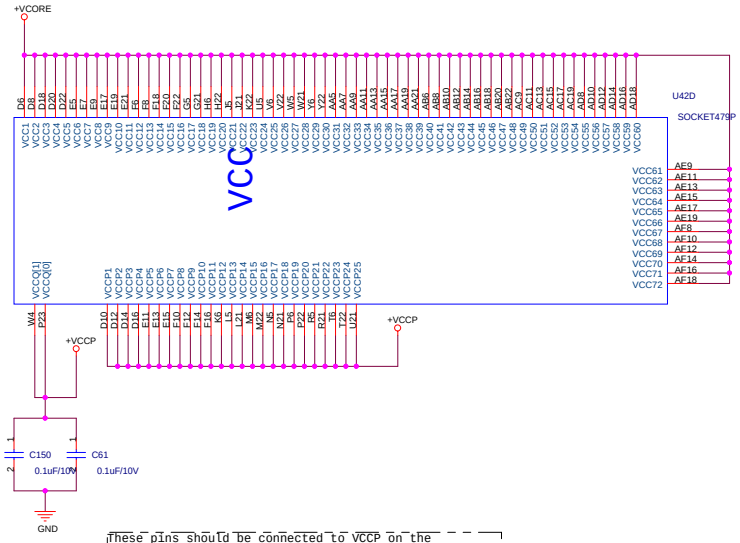


ASUSTECH CO.,LTD.	Title : POWER DIAGRAM	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 2 of 57	

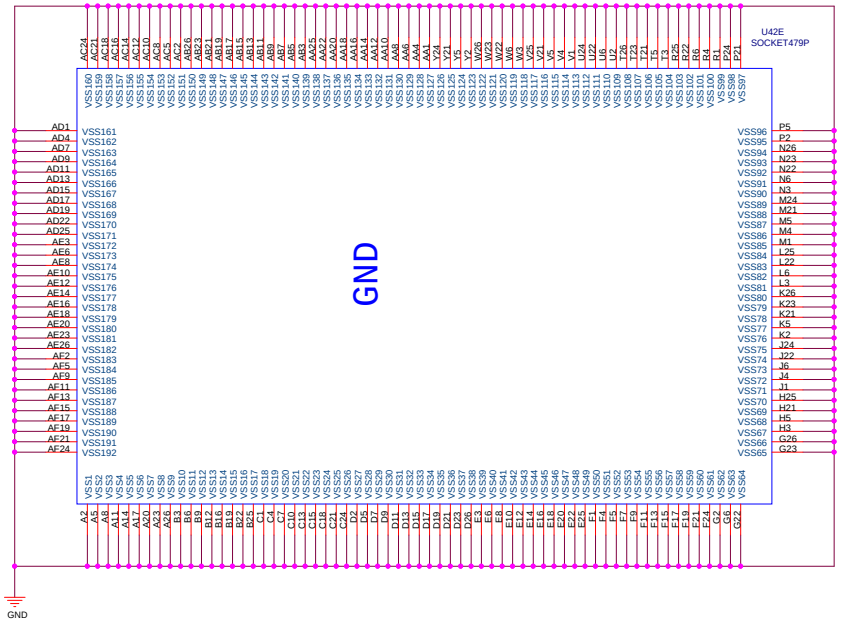

CPU Pin A1 need to be enlarged(M)
U42B
SOCKET479P
WIDTH: 5 mils
SPACE >= 1:2
GROUP SPACE >=1:5
Breakout Length:<=200 mil
LENGTH: 1" - 6.5"(OPT: 4"+/-0.5")
(#0011)
WIDTH:4mils
SPACE >= 1:3
GROUP SPACE >=1:5
LENGTH: 0.5" - 5.5"
(#0012)
U42A
SOCKET479P
WIDTH:4mils
SPACE >= 1:2
STROBE SPACE >=1:3
GROUP SPACE >=1:5
LENGTH: 0.5" - 6.5"
(#0012)
Here IERR# is not routed as a test point or to any optional system receiver
RESET# Signal Routing with NO ITP700FLEX Connector
CPU PLL CIRCUITS
U42C
SOCKET479P
Close to Pin VCCA[3..1] of CPU
TOPOLOGY 2A:
Open Drain (OD) Signal
R-CPU-ICH Y-FORK
CPU-ICH: 0.5" - 12"
R - CPU <= 3"
(#0013)
TOPOLOGY 1B:
Open Drain (OD) Signal
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
TOPOLOGY 2B:
CMOS Signals
MCH-CPU-ICH4
MCH-CPU:0.5"-6.5"
CPU-ICH4:0.5"-12"
(#0013)
TOPOLOGY 1C:
Open Drain (OD) Signal
CPU-R-LSC-ICH
CPU-R: 0.5" - 12"
R - LSC<= 3"
LSC-ICH:0.5"-12"
TOPOLOGY 2C:
CMOS Signals:
LINT0/INTR,LINT1/NMI,A20M#,
IGNNE#,SLP#,SMI#,and STPCLK#
CPU-ICH:0.5" - 12"
TOPOLOGY 3:
CMOS Signals
CPU-ICH-R-LSC-FWH
CPU-ICH:0.5" - 12"
R - LSC <= 3"
LSC-FWH:0.5"-6"(#0013)
TOPOLOGY 1B:
Open Drain (OD) Signal
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
H_GTLREF0
LENGTH <=0.5"
WIDTH = 5 mils
SPACE >= 25 mils
X BPSB(#0004)
Close to Pin AD26 of CPU
CPU DEBUG PORT
Close to Pin A8 of CPU
Close to Pin A12 of CPU
Width= 5 mils
Length <= 2"
CPU JTAG
CPU_COMP2 :
Analog
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)
CPU_COMP0 :
Analog
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)
CPU_COMP3 :
Analog
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
CPU_COMP1 :
Analog
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
Pin AD1,AC2 of BANIAS
Title : CPU-DOTHAN(HOST)
ASUSTECH CO.,LTD.
Engineer: EDDY ZHAO
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 3 of 57

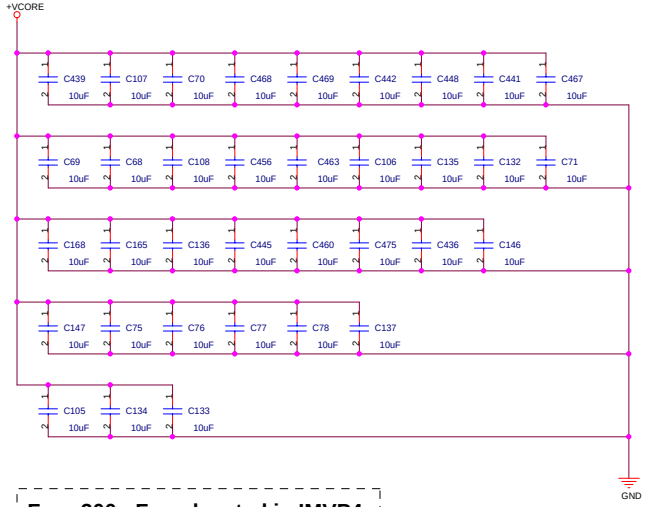
Target VCC (Std Voltage) :
HFM: 1.308V
LFM: 0.956V
Target Deeper Sleep Vcc = 0.745 V

TDP:
21W (Std Voltage)
10W (Low Voltage)
5W (Ultra Low Voltage)



These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.





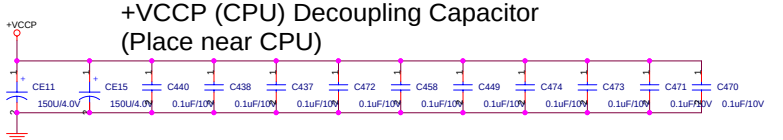
Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

Four 200 uF are located in IMVP4

+VCCP (CPU) Decoupling Capacitor (Place near CPU)



Two 150-UF POSCAPs with an ESR of 36 mOhm(typ) should be used for bulk decoupling. One capacitor should be placed next to the processor socket and one capacitor in close proximity to the MCH package.

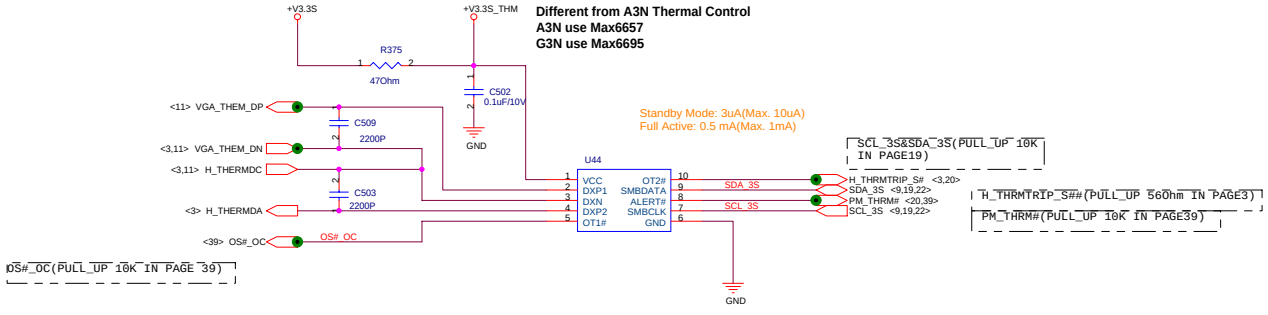
Ten 0.1-UF X7R capacitors in a 0603 form factor should be placed on the secondary side of the motherboard under the processor socket cavity next to the VCCP pins of the processor. Five capacitors should be spread out near the Data signal side and five capacitors near the Address signal side of the processor socket's pin-map.

ASUSTECH CO.,LTD.	Title : CPU-DOTHAN(PWR)	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 4 of 57	

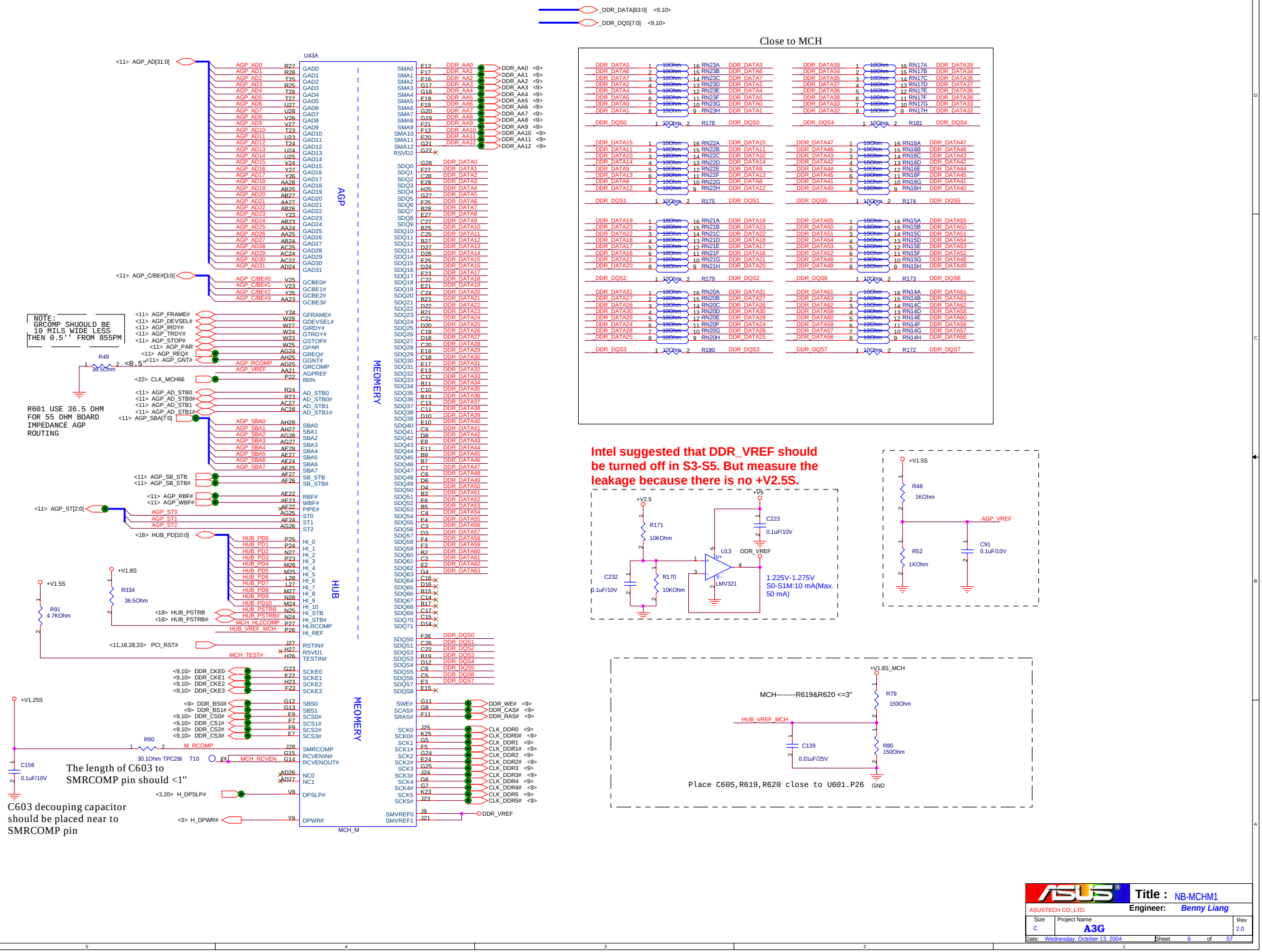
Route H_THERMDA and H_THERMDC on the same layer
Route VGA_THEM_DP and VGA_THEM_DN on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

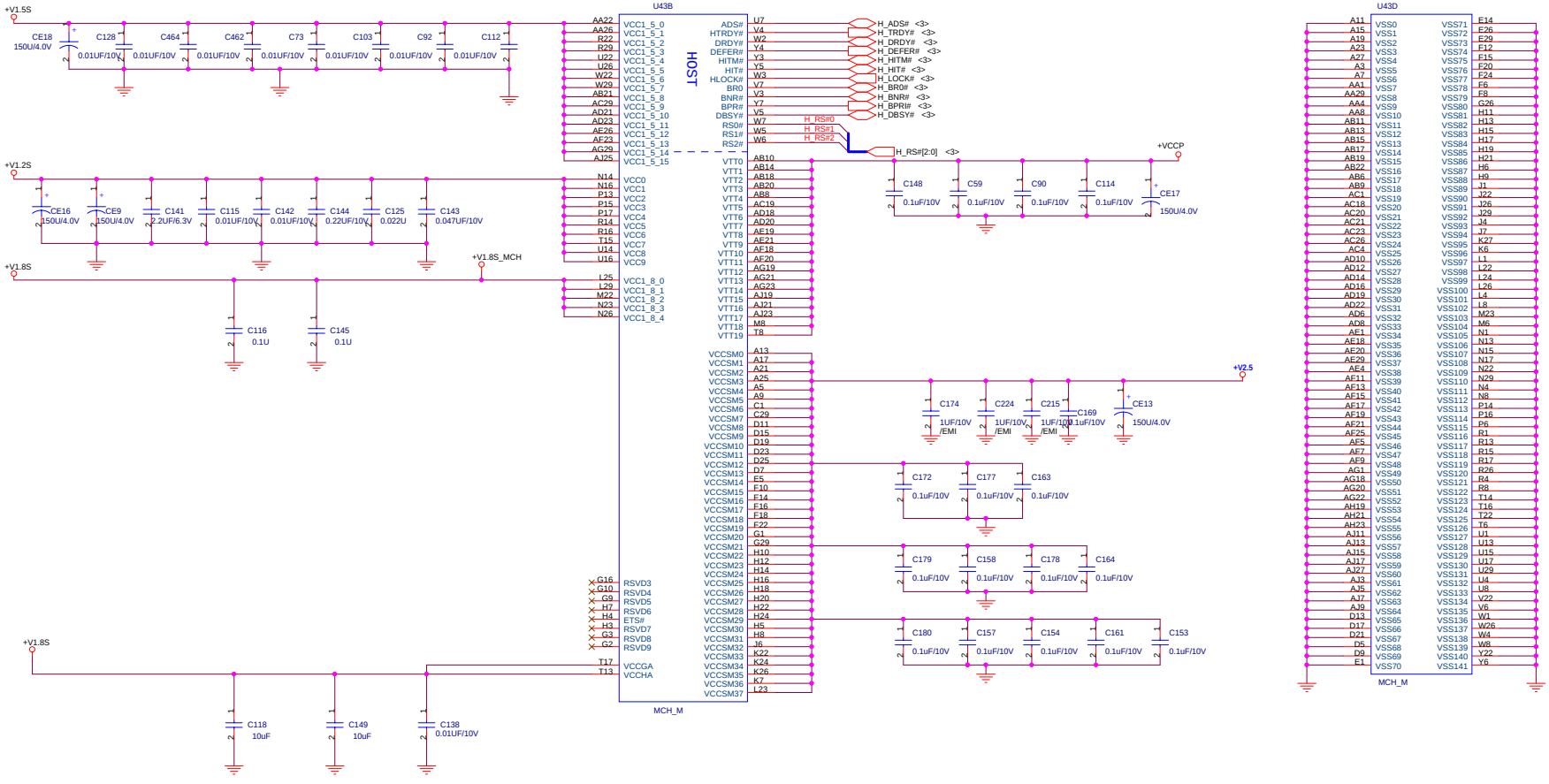


ASUSTEK CO.,LTD.	Title : THERMAL	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 5 of 57	

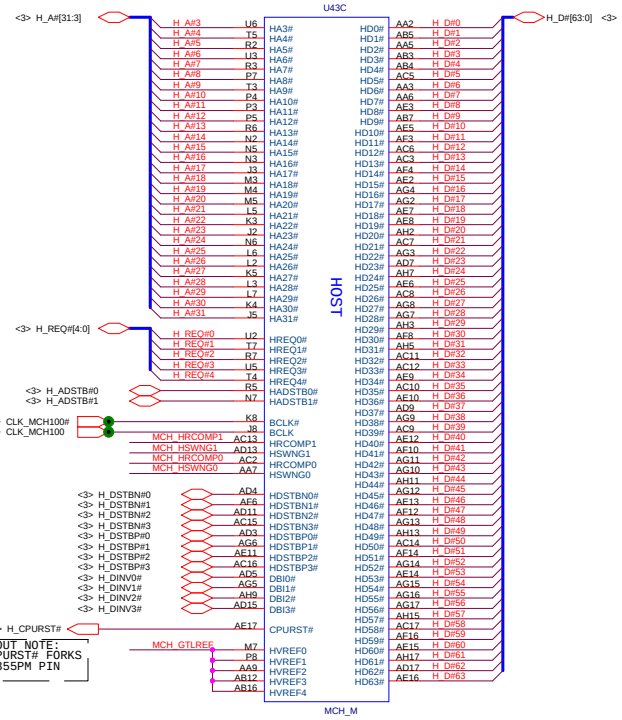


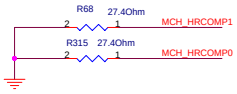
ASUSTECH COMPUTER INC.	Title : NB-MCHM1		
	Engineer: Benny Liang		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 6 of 57		

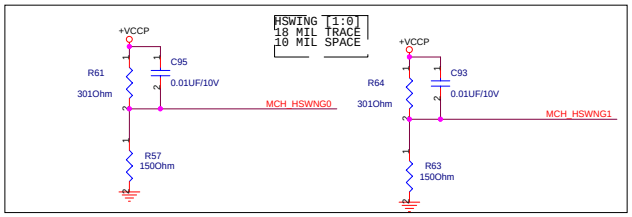
All decoupling capacitances should Be
placed near to the associated pins.



ASUSTEK CO.,LTD.	Title : NB-MCHM2	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 7 of 57	

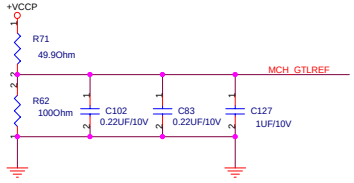






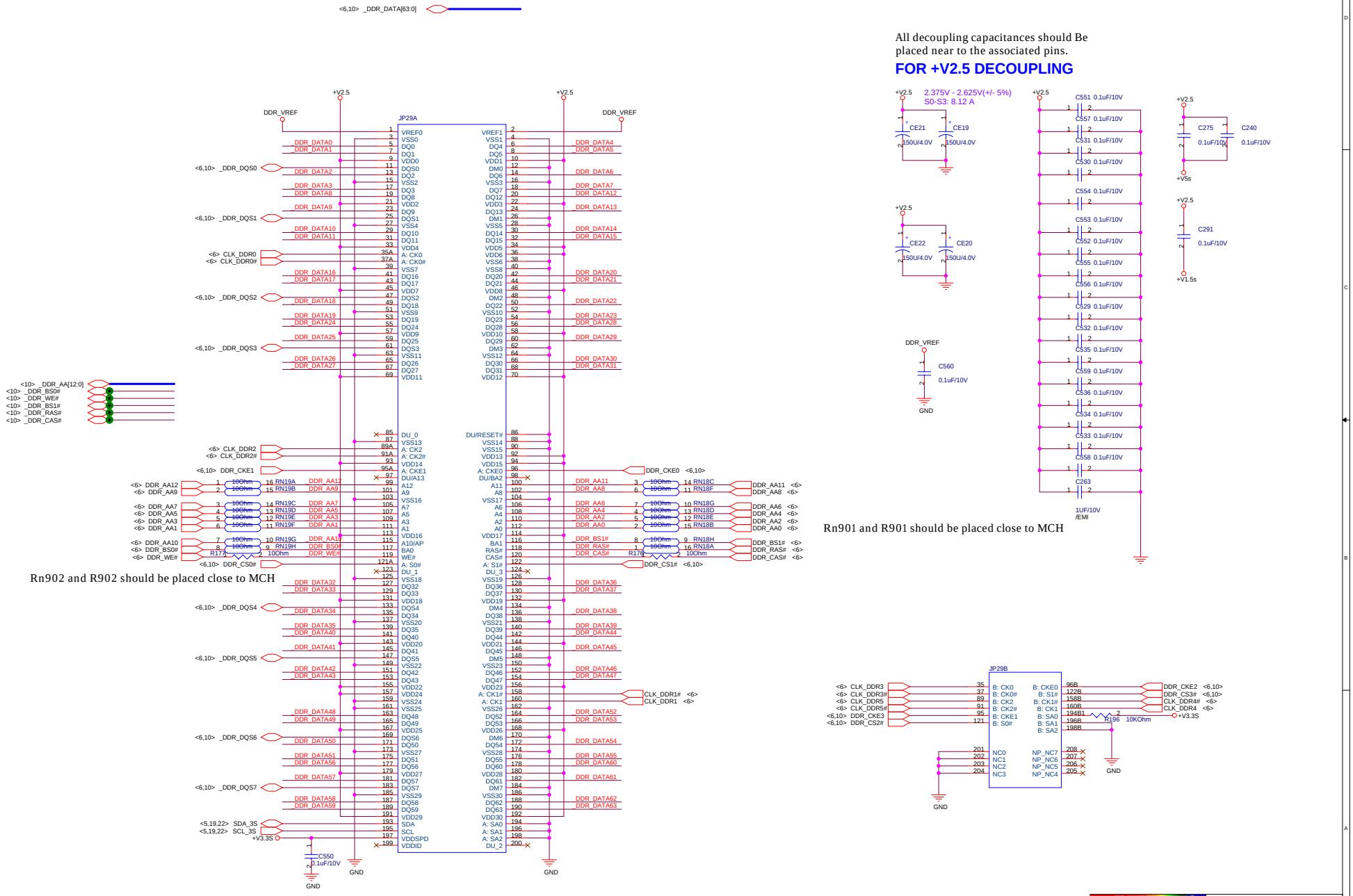
C801 should be placed closer to de HSWNG0 than R805 and R807

C802 should be placed closer to de HSWNG1 than R806 and R808



Place R809 close to HVREF4 and R810 close to HVREF1

ASUSTECH CO.,LTD.	Title : NB-MCHM3	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 8 of 57	


JP29A
JP29B
DDR_VREF
+V2.5
GND
Rn902 and R902 should be placed close to MCH
All decoupling capacitances should Be placed near to the associated pins.
FOR +V2.5 DECOUPLING
2.375V - 2.625V(+/- 5%)
S0-S3: 8.12 A
Rn901 and R901 should be placed close to MCH
1UF/10V /EMI
Title : DUAL_DDR
ASUSTECH CO.,LTD.
Engineer: Benny Liang
Project Name A3G
Size C
Rev 2.0
Date: Wednesday, October 13, 2004
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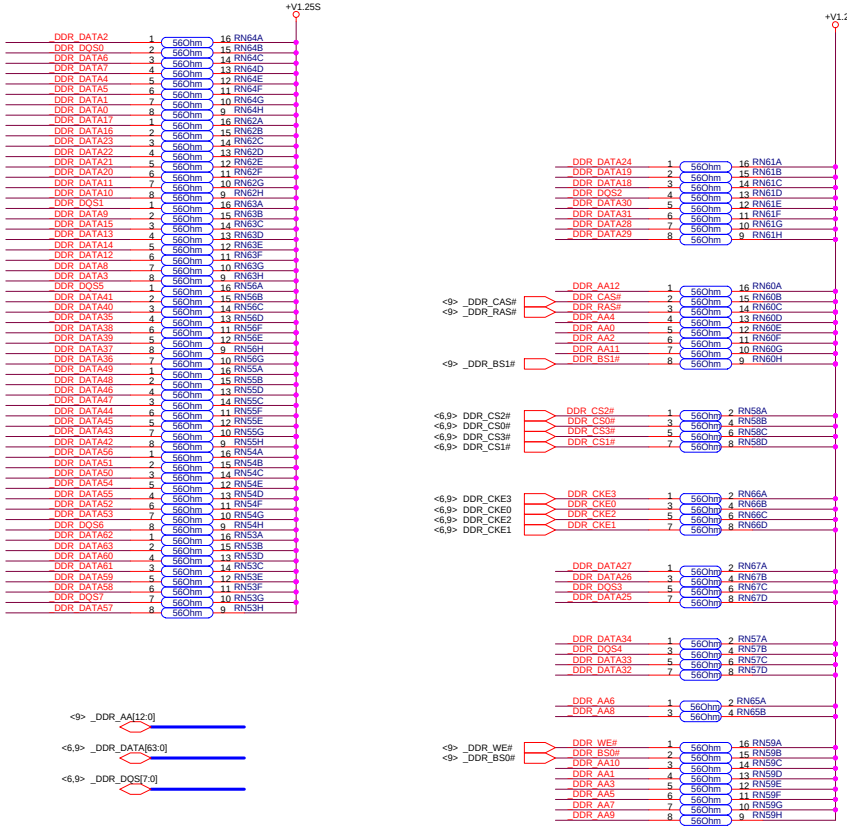
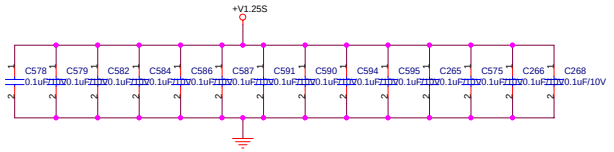
All termination registers should Be placed near to the associated pins of SO-DIMM1

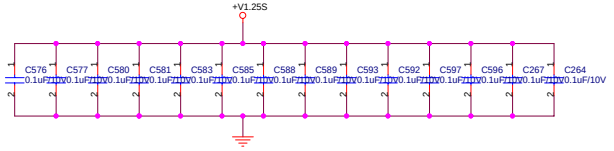


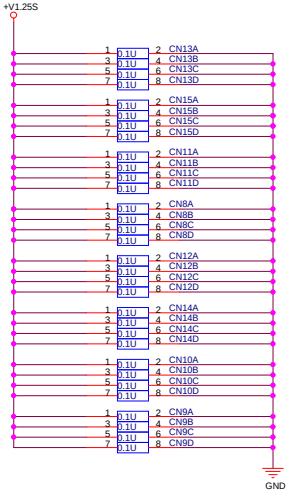
FOR +V1.25S DECOUPLING

Place one cap between every 2 pullup resistors to +V1.25S

All decoupling capacitances should Be placed near to the associated pins.

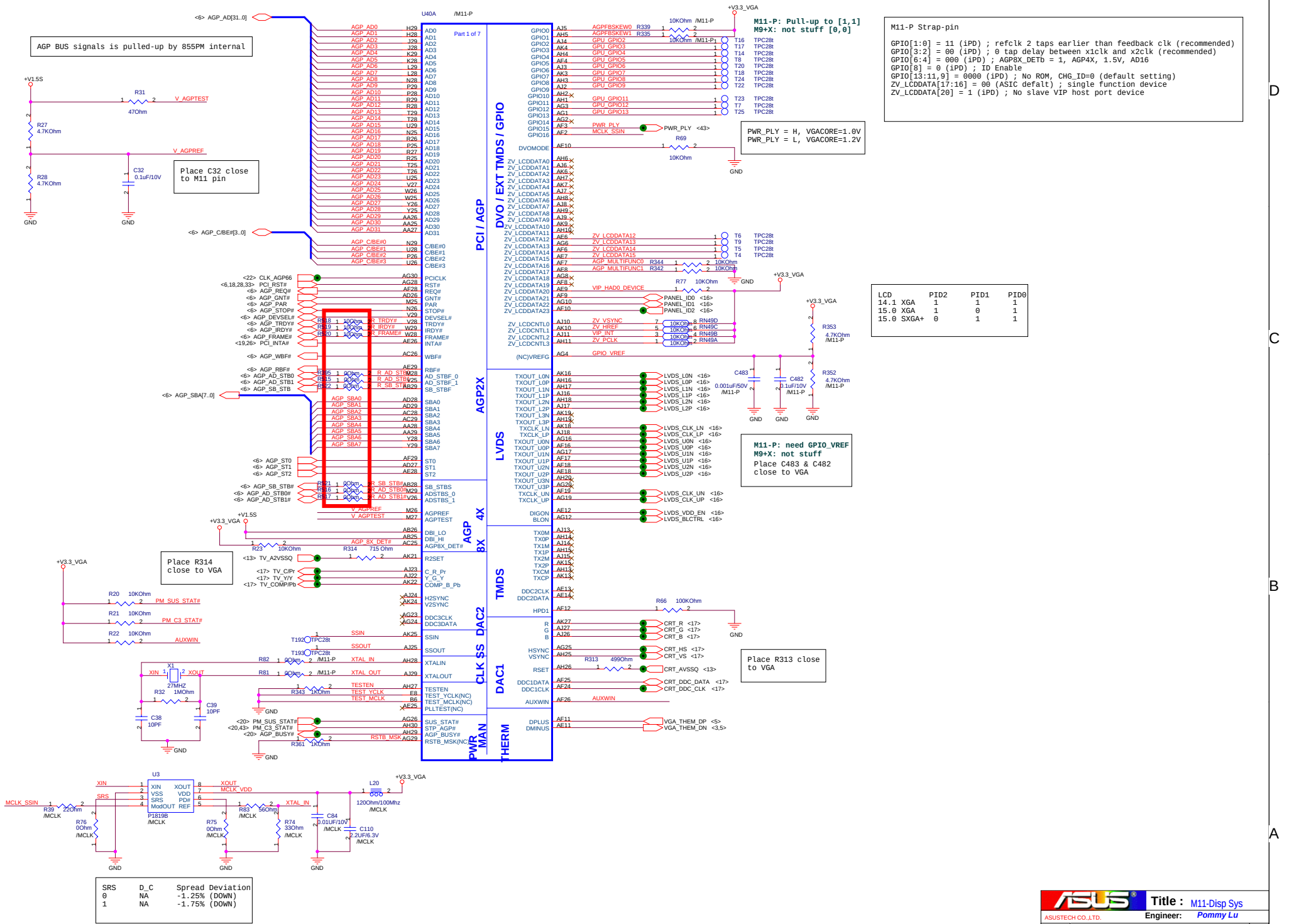






These chip capacitors should be placed equationally near the termination resistors

ASUSTEK CO.,LTD.	Title : DDR_TERMINATION	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 10 of 57	


AGP BUS signals is pulled-up by 855PM internal
Place C32 close to M11 pin
Place R314 close to VGA
M11-P: Pull-up to [1,1]
M9+X: not stuff [0,0]
PWR_PLY = H, VGACORE=1.0V
PWR_PLY = L, VGACORE=1.2V
M11-P Strap-pin
GPIO[1:0] = 11 (iPD) ; refclk 2 taps earlier than feedback clk (recommended)
GPIO[3:2] = 00 (iPD) ; 0 tap delay between x1clk and x2clk (recommended)
GPIO[6:4] = 000 (iPD) ; AGP8X_DETb = 1, AGP4X, 1.5V, AD16
GPIO[8] = 0 (iPD) ; ID Enable
GPIO[13:11,9] = 0000 (iPD) ; No ROM, CHG_ID=0 (default setting)
ZV_LCDDATA[17:16] = 00 (ASIC defalt) ; single function device
ZV_LCDDATA[20] = 1 (iPD) ; No slave VIP host port device
LCD PID2 PID1 PID0
14.1 XGA 1 1 1
15.0 XGA 1 0 1
15.0 SXGA+ 0 1 1
M11-P: need GPIO_VREF
M9+X: not stuff
Place C483 & C482 close to VGA
Place R313 close to VGA
SRS D_C Spread Deviation
0 NA -1.25% (DOWN)
1 NA -1.75% (DOWN)
Title : M11-Disp Sys
Engineer: Pommy Lu
ASUSTECH CO.,LTD.
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
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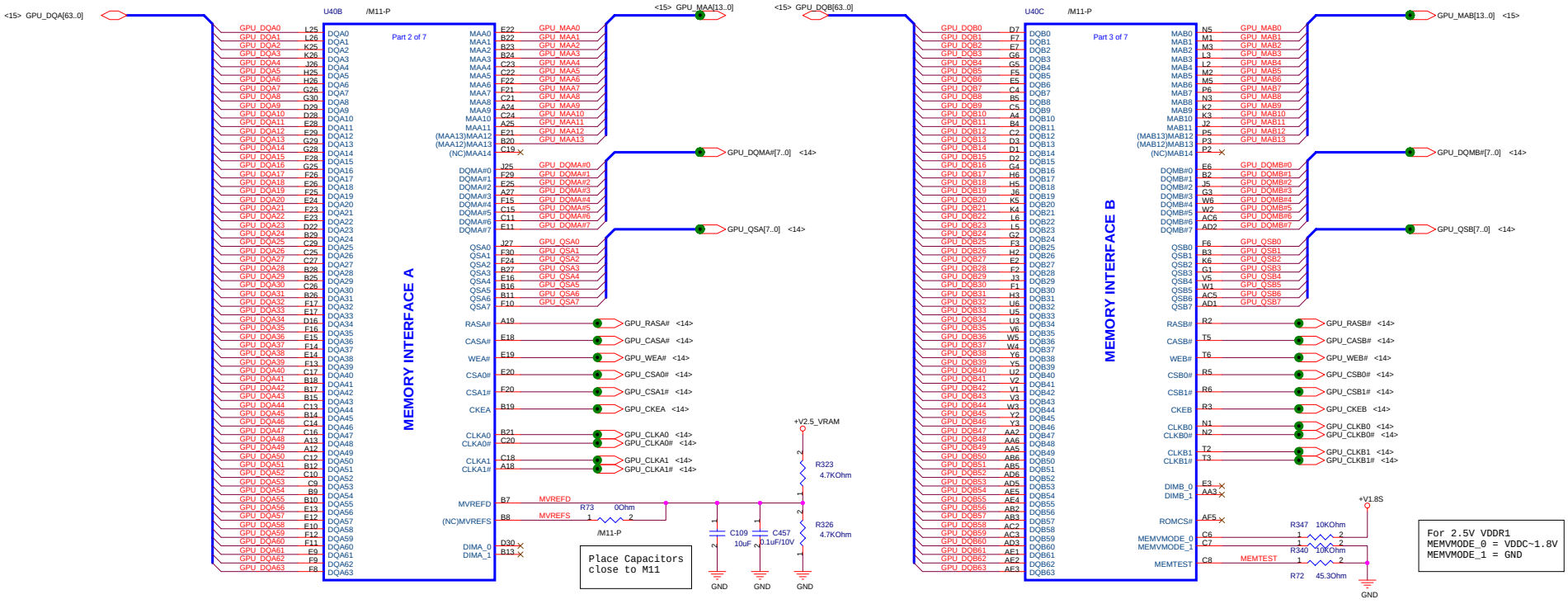


ASUSTEK CO.,LTD.	Title : M11-Mem IF		
	Engineer: Pommy Lu		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 12 of 57		

place Decoupling Capacitors close to M11

Memory I/O Power
S0-S3: 530mA

LVDS I/O Power
S0-S3: 100mA

LVDS Digital Logic Power
S0-S3: 30mA

LVDS/TMDS PLL Power
S0-S3: 6mA

TMDS I/O Power
S0-S3: 30mA

Memory Clock Power
S0-S3: 530mA

S0-S3: 120mA

S0-S3: 66mA

S0-S3: 66mA

DAC Digital Power
S0-S3: 7mA

PLL Power
S0-S3: 21mA

S0-S3 MAX: 8.625A

Power Between core and I/O
S0-S3: 160mA

I/O Power
S0-S3: 2mA

VDO Power
S0-S3: 2mA

AGP I/O Power
S0-S3: 90mA

Memory PLL Power
S0-S3: 6mA

I/O POWER

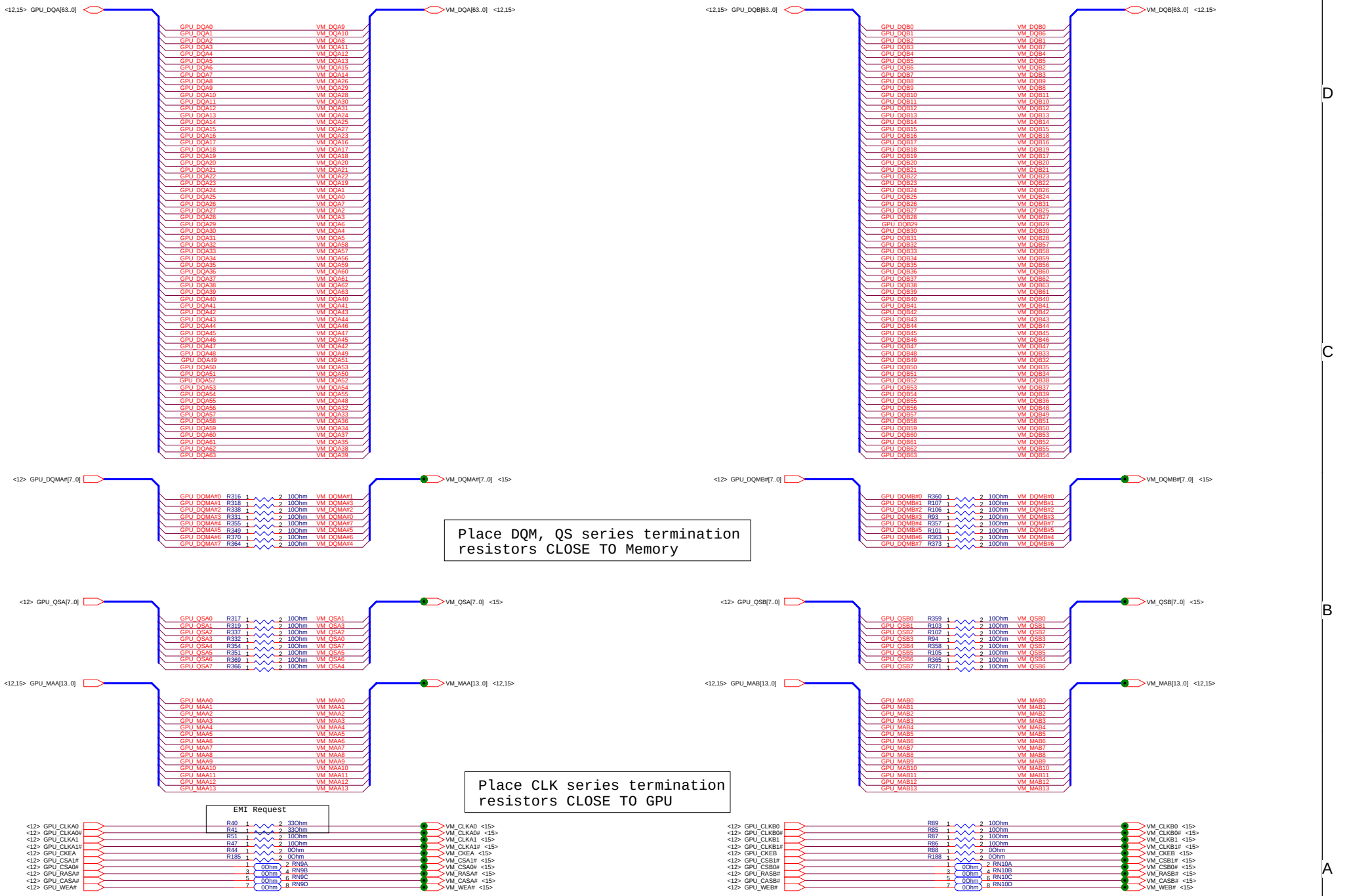
CORE GND

M10-P (708 BGA) / M9+X (708 BGA) CENTER ARRAY

MASK OFF CENTER BALL ARRAY WITH M9+X (684BGA)

M9+X (708 BGA) INNER ROWS

Title :	M11-PWR/GND
ASUSTECH CO.,LTD.	Engineer: Pommy Lu
Size: C	Project Name: A3G
Rev: 2.0	
Date: Wednesday, October 13, 2004	Sheet 13 of 57


5
4
3
2
1
D
C
B
A
<12,15> GPU_DQA[63..0]
VM_DQA[63..0] <12,15>
<12,15> GPU_DQB[63..0]
VM_DQB[63..0] <12,15>
<12> GPU_DQMA#[7..0]
VM_DQMA#[7..0] <15>
<12> GPU_DQMB#[7..0]
VM_DQMB#[7..0] <15>
Place DQM, QS series termination resistors CLOSE TO Memory
<12> GPU_QSA[7..0]
VM_QSA[7..0] <15>
<12> GPU_QSB[7..0]
VM_QSB[7..0] <15>
<12,15> GPU_MAA[13..0]
VM_MAA[13..0] <12,15>
<12,15> GPU_MAB[13..0]
VM_MAB[13..0] <12,15>
Place CLK series termination resistors CLOSE TO GPU
EMI Request
<12> GPU_CLKA0
<12> GPU_CLKA0#
<12> GPU_CLKA1
<12> GPU_CLKA1#
<12> GPU_CKEA
<12> GPU_CSA1#
<12> GPU_CSA0#
<12> GPU_RASA#
<12> GPU_CASA#
<12> GPU_WEA#
VM_CLKA0 <15>
VM_CLKA0# <15>
VM_CLKA1 <15>
VM_CLKA1# <15>
VM_CKEA <15>
VM_CSA1# <15>
VM_CSA0# <15>
VM_RASA# <15>
VM_CASA# <15>
VM_WEA# <15>
<12> GPU_CLKB0
<12> GPU_CLKB0#
<12> GPU_CLKB1
<12> GPU_CLKB1#
<12> GPU_CKEB
<12> GPU_CSB1#
<12> GPU_CSB0#
<12> GPU_RASB#
<12> GPU_CASB#
<12> GPU_WEB#
VM_CLKB0 <15>
VM_CLKB0# <15>
VM_CLKB1 <15>
VM_CLKB1# <15>
VM_CKEB <15>
VM_CSB1# <15>
VM_CSB0# <15>
VM_RASB# <15>
VM_CASB# <15>
VM_WEB# <15>
Title : VRAM DAMPING
ASUSTECH CO.,LTD.
Engineer: Pommy Lu
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
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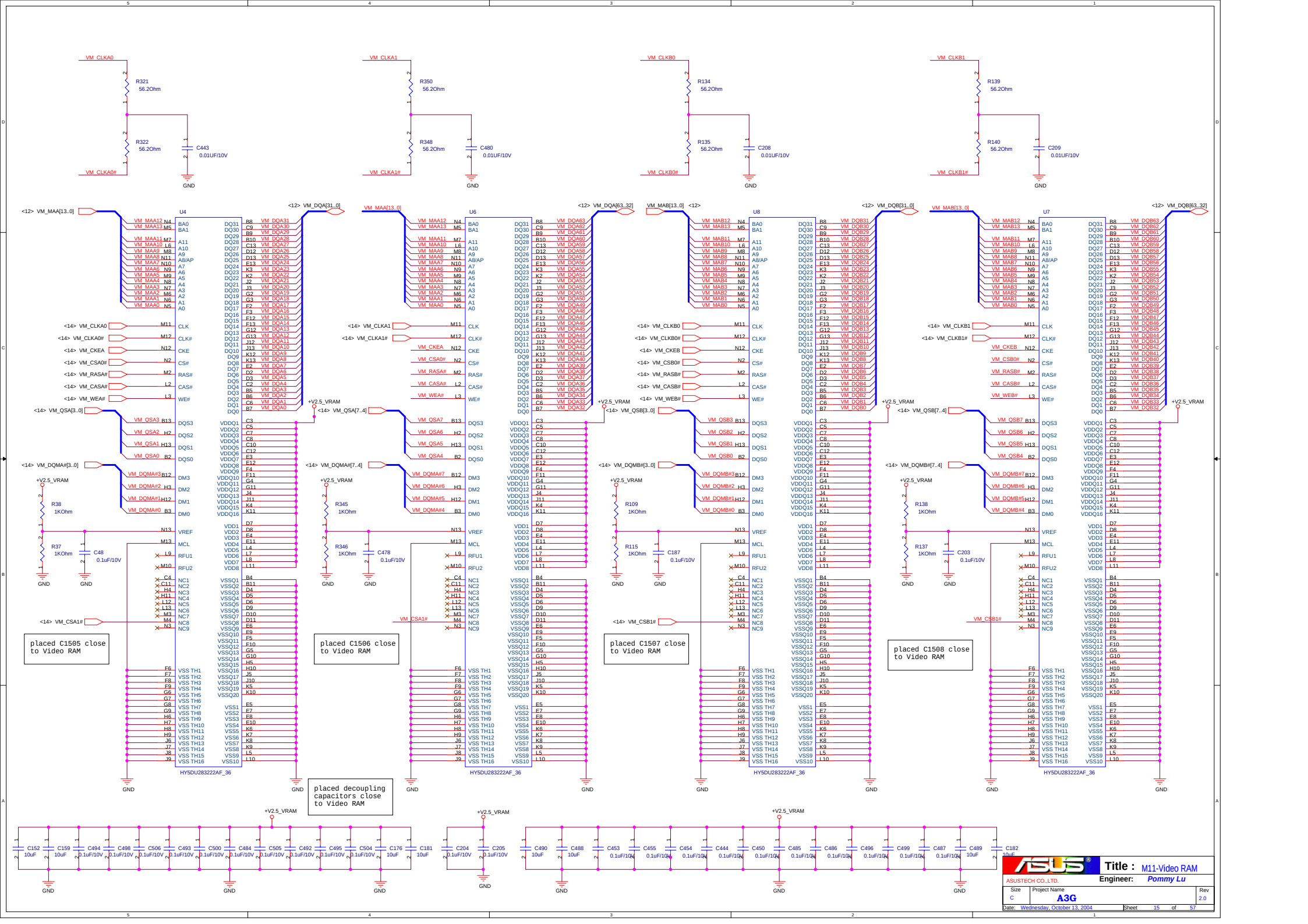
VM_CLKA0
R321 56.2Ohm
R322 56.2Ohm
C443 0.01UF/10V
VM_CLKA0#
GND
VM_CLKA1
R350 56.2Ohm
R348 56.2Ohm
C480 0.01UF/10V
VM_CLKA1#
VM_CLKB0
R134 56.2Ohm
R135 56.2Ohm
C208 0.01UF/10V
VM_CLKB0#
VM_CLKB1
R139 56.2Ohm
R140 56.2Ohm
C209 0.01UF/10V
VM_CLKB1#
U4
U6
U8
U7
HY5DU283222AF_36
+V2.5_VRAM
R38 1KOhm
R37 1KOhm
C48 0.1uF/10V
R345 1KOhm
R346 1KOhm
C478 0.1uF/10V
R109 1KOhm
R115 1KOhm
C187 0.1uF/10V
R138 1KOhm
R137 1KOhm
C203 0.1uF/10V
placed C1505 close to Video RAM
placed C1506 close to Video RAM
placed C1507 close to Video RAM
placed C1508 close to Video RAM
placed decoupling capacitors close to Video RAM
C152 10uF
C159 10uF
C494 0.1uF/10V
C498 0.1uF/10V
C506 0.1uF/10V
C493 0.1uF/10V
C500 0.1uF/10V
C484 0.1uF/10V
C505 0.1uF/10V
C492 0.1uF/10V
C495 0.1uF/10V
C504 0.1uF/10V
C176 10uF
C181 10uF
C204 0.1uF/10V
C205 0.1uF/10V
C490 10uF
C488 10uF
C453 0.1uF/10V
C455 0.1uF/10V
C454 0.1uF/10V
C444 0.1uF/10V
C450 0.1uF/10V
C485 0.1uF/10V
C486 0.1uF/10V
C496 0.1uF/10V
C499 0.1uF/10V
C487 0.1uF/10V
C489 10uF
C182 10uF
Title : M11-Video RAM
ASUSTEK CO.,LTD.
Engineer: Pommy Lu
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
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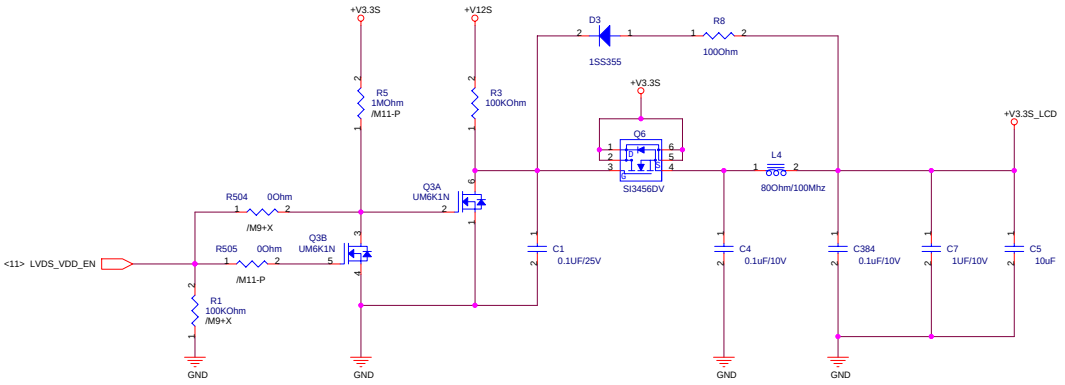
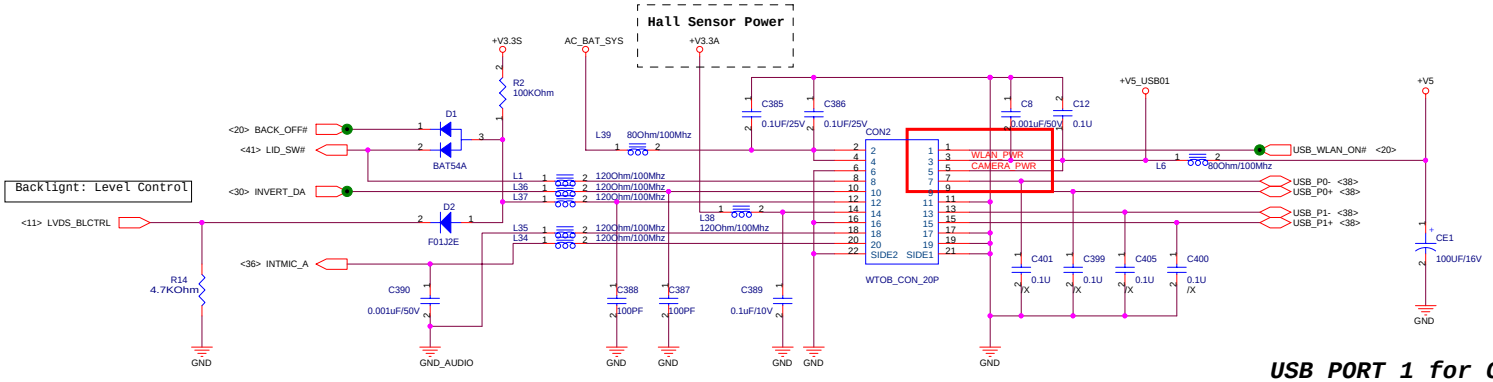


M11-P: Internal PD, not stuff R1
M9+X: stuff R1

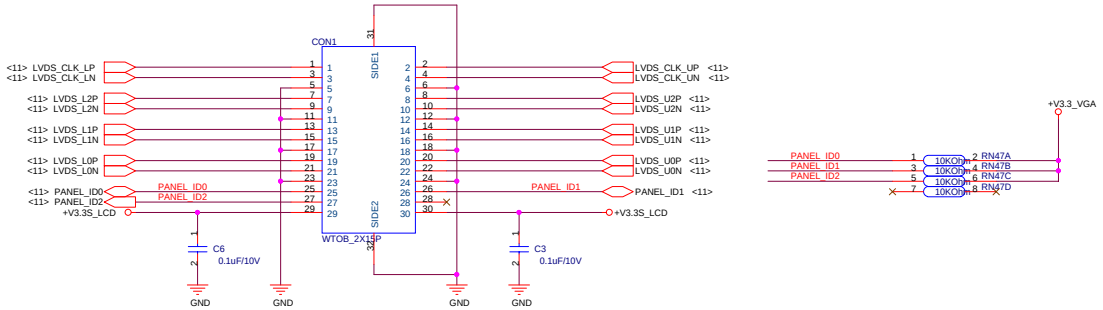
placed BEAD close to CON1



placed BEAD close to CON1603

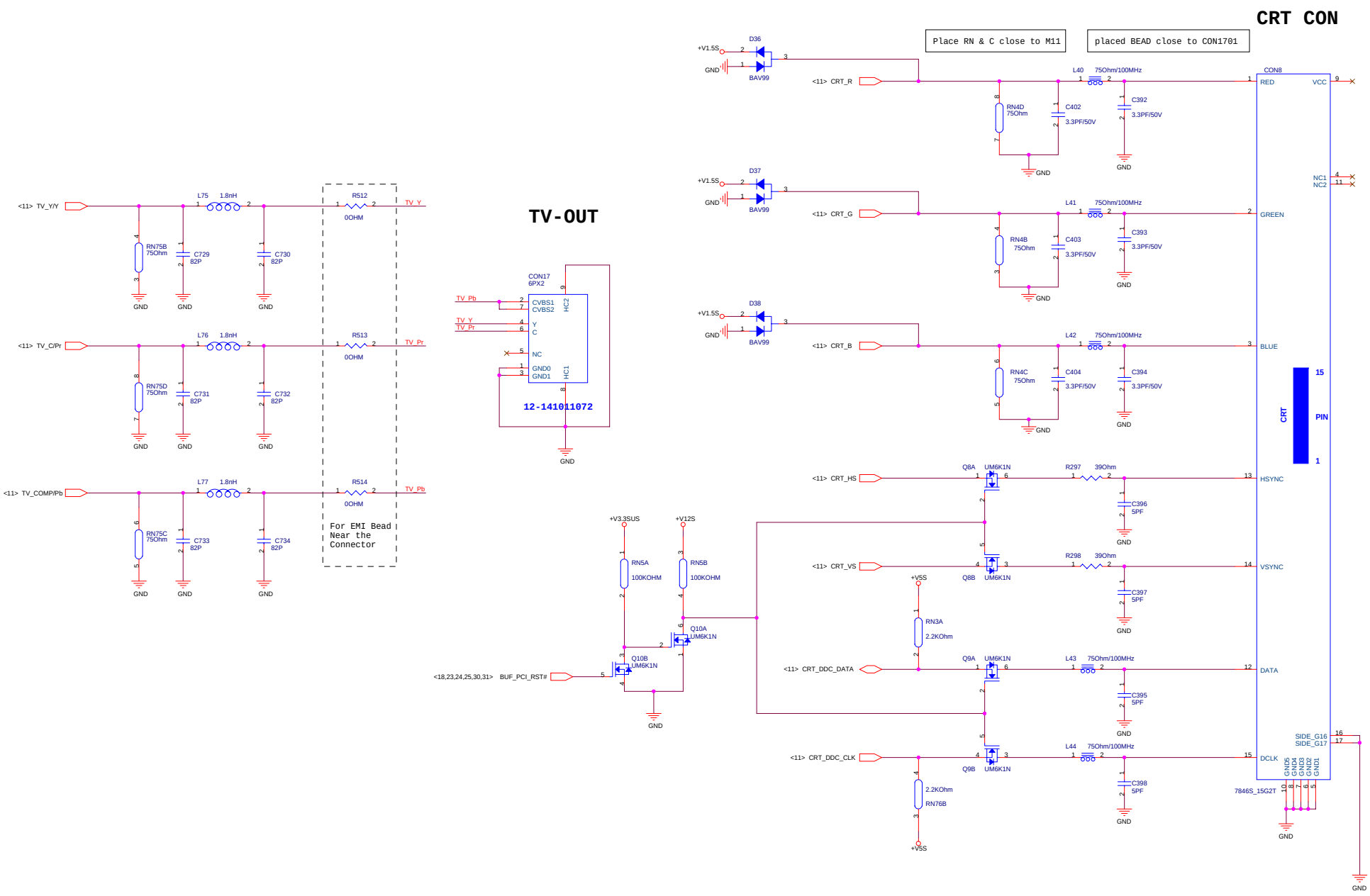
USB PORT 1 for CAMERA
USB PORT 0 for WLAN

CON1
first source: 12-172010300
second source: 12-17001030L

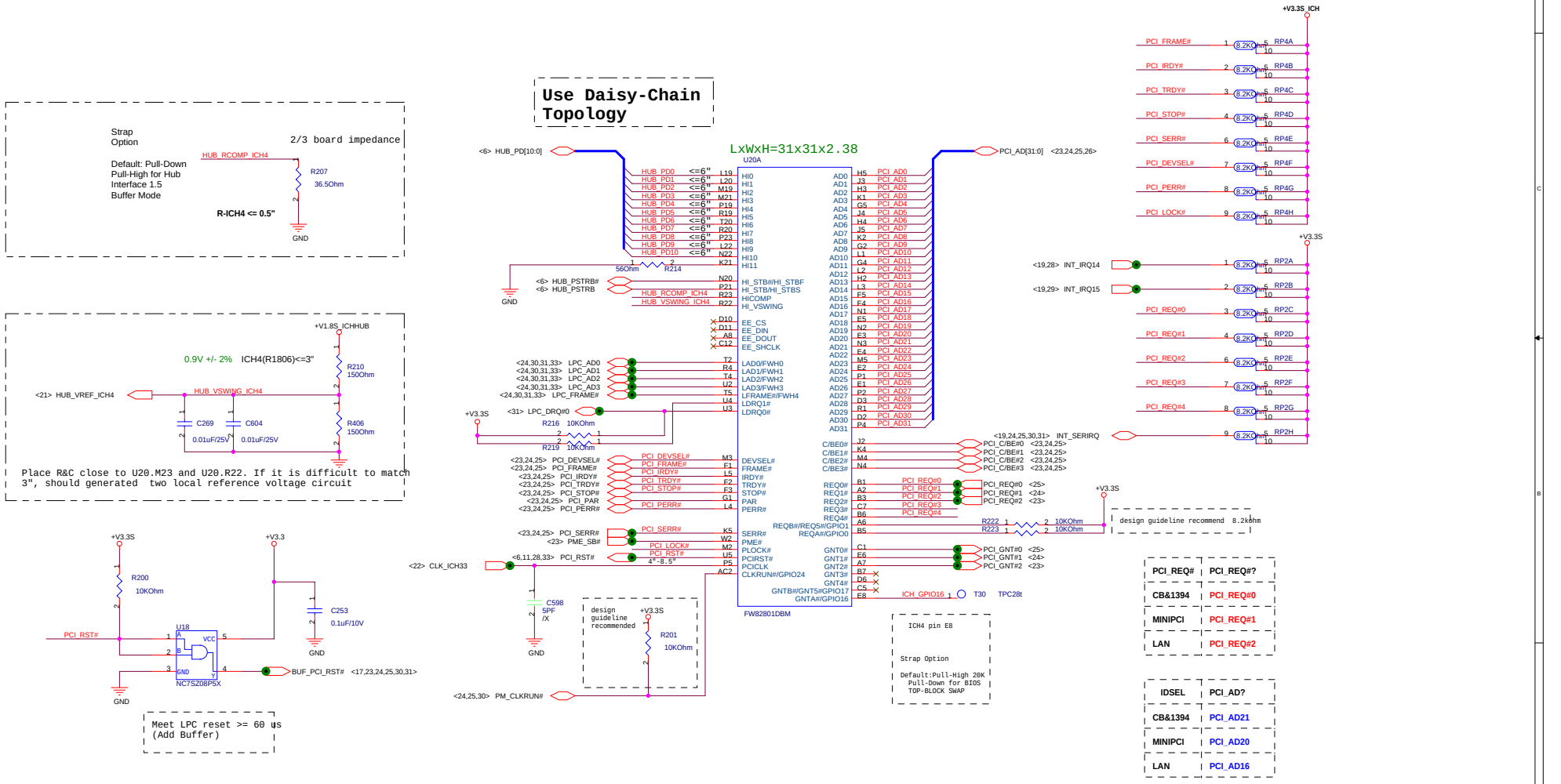


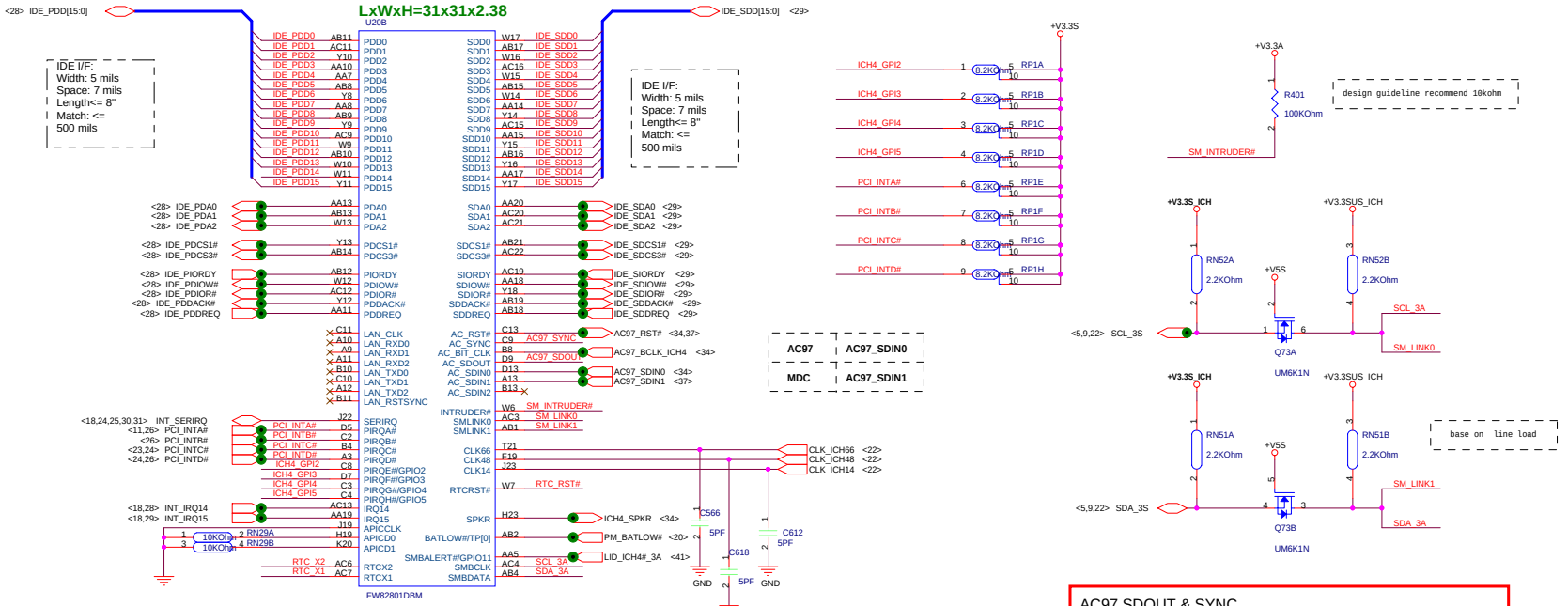
LCD CON

ASUSTECH CO.,LTD.	Title : BL&LCD CON	
	Engineer: Pommy Lu	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 16 of 57	

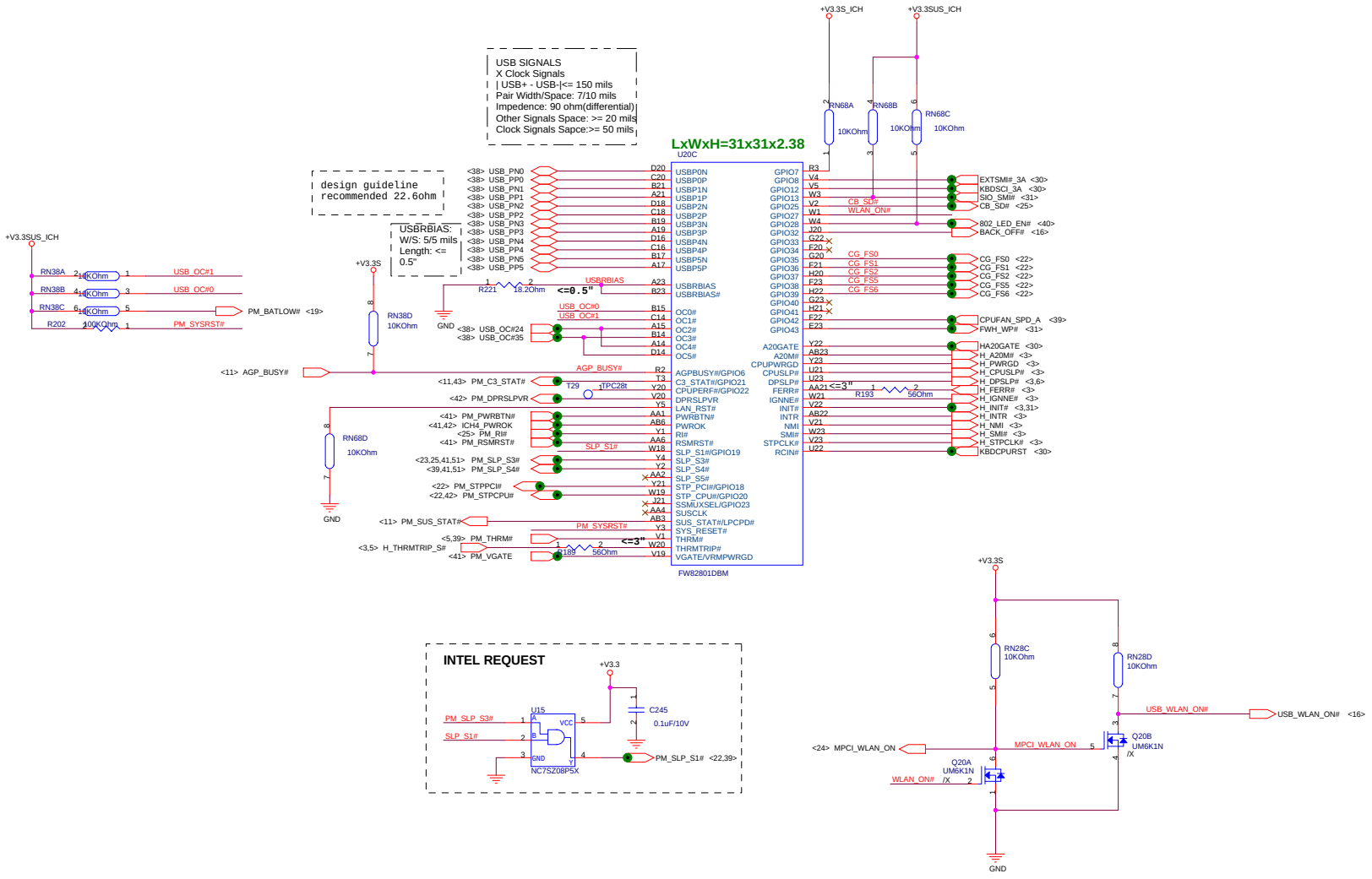


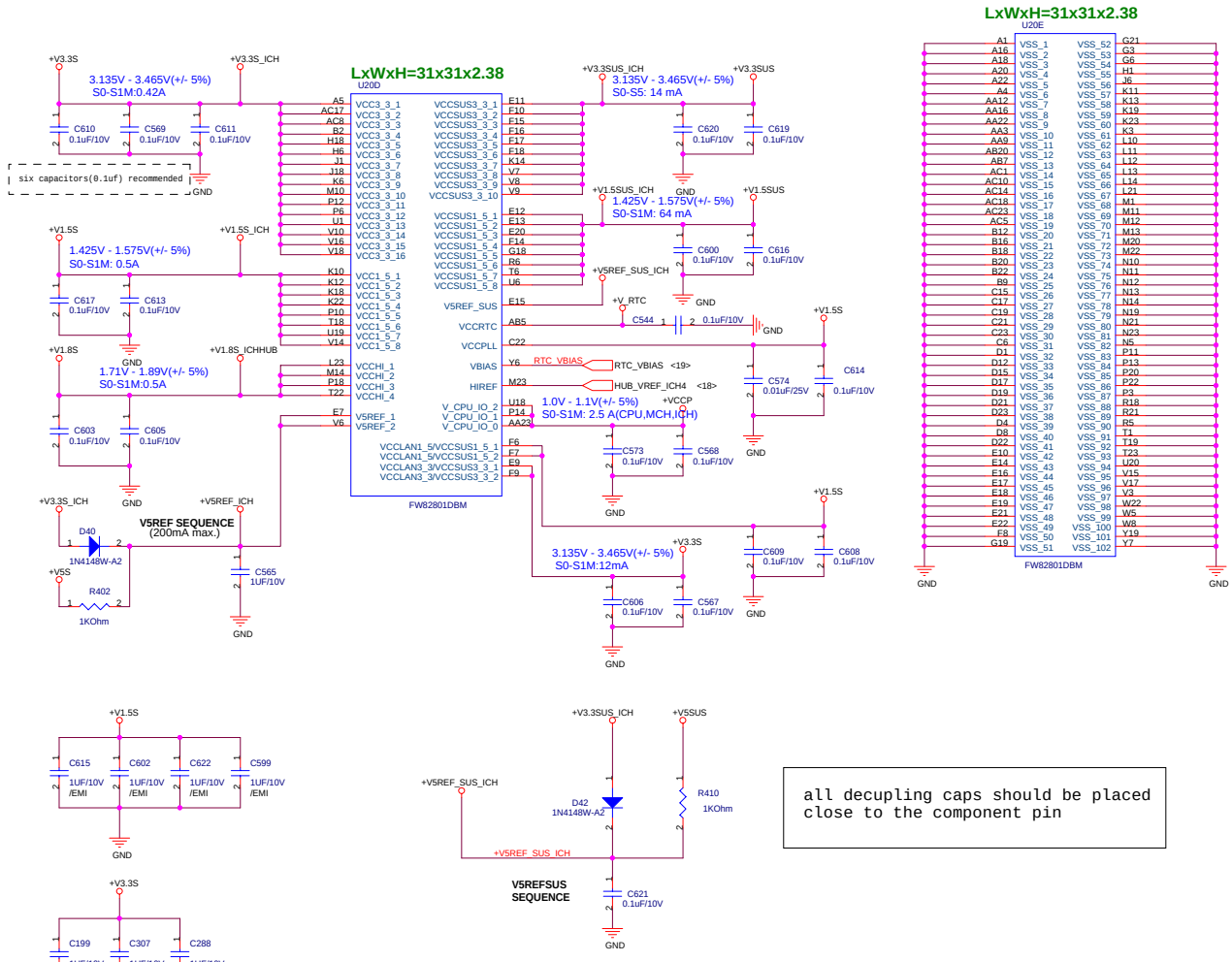
ASUSTEK CO.,LTD.	Title : TV-OUT & CRT CON		
	Engineer: Pommy Lu		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 17 of 57		

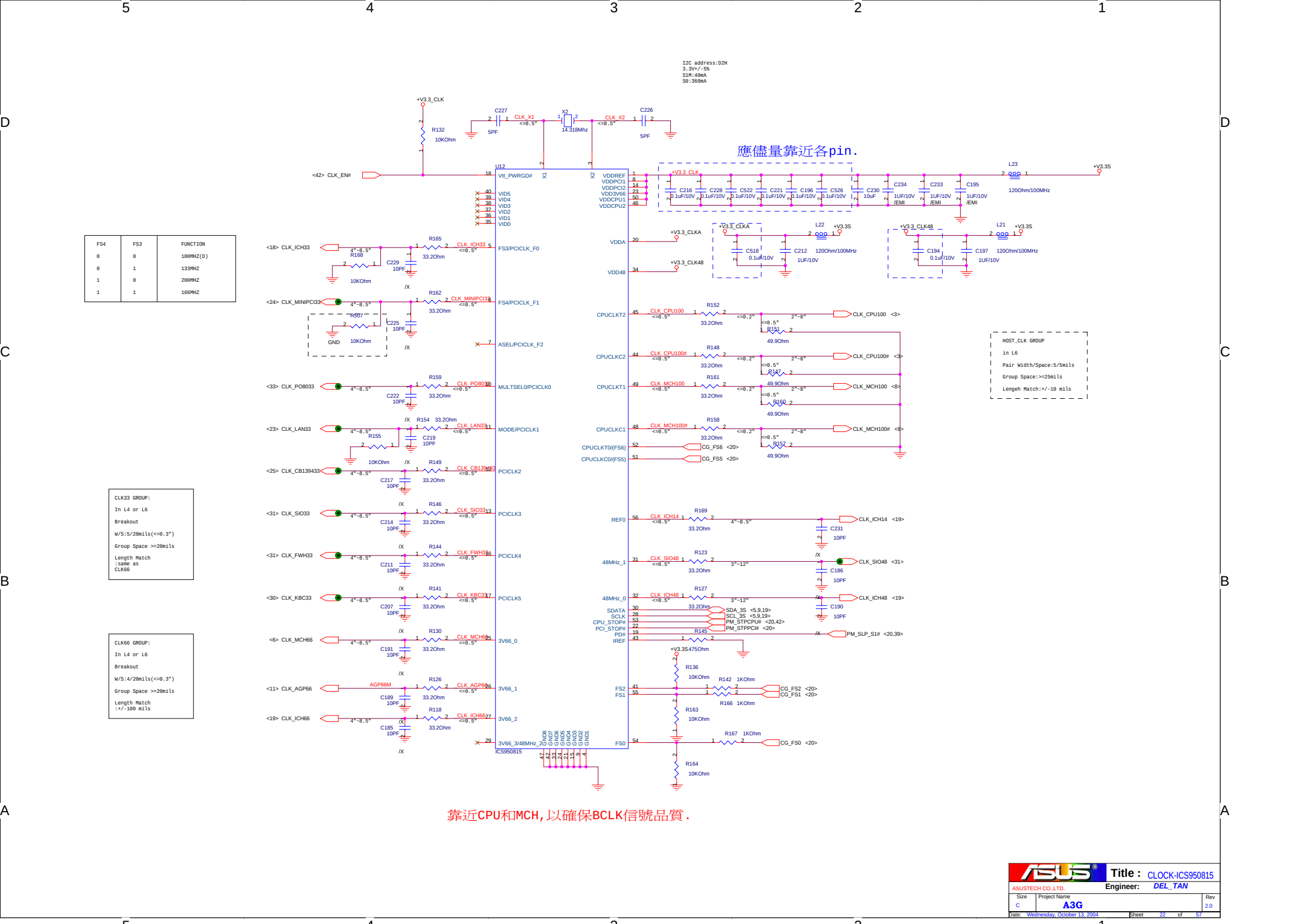

Use Daisy-Chain Topology
LxWxH=31x31x2.38
U20A
FW82801DBM
Strap Option
2/3 board impedance
Default: Pull-Down
Pull-High for Hub Interface 1.5 Buffer Mode
R-ICH4 <= 0.5"
HUB_RCOMP_ICH4
R207
36.5Ohm
GND
+V1.8S_ICHHUB
0.9V +/- 2%
ICH4(R1806)<=3"
<21> HUB_VREF_ICH4
HUB_VSWING_ICH4
R210
150Ohm
R406
150Ohm
C269
0.01uF/25V
C604
0.01uF/25V
Place R&C close to U20.M23 and U20.R22. If it is difficult to match 3", should generated two local reference voltage circuit
<6> HUB_PD[10:0]
HUB_PD0 <=6" L19
HUB_PD1 <=6" L20
HUB_PD2 <=6" M19
HUB_PD3 <=6" M21
HUB_PD4 <=6" P19
HUB_PD5 <=6" R19
HUB_PD6 <=6" T20
HUB_PD7 <=6" R20
HUB_PD8 <=6" P23
HUB_PD9 <=6" L22
HUB_PD10 <=6" N22
56Ohm R214
<6> HUB_PSTRB#
<6> HUB_PSTRB
HUB_RCOMP_ICH4 R23
HUB_VSWING_ICH4 R22
HI0 HI1 HI2 HI3 HI4 HI5 HI6 HI7 HI8 HI9 HI10 HI11
HI_STB#/HI_STBF
HI_STB/HI_STBS
HICOMP
HI_VSWING
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LFRAME#/FWH4
LDRQ1#
LDRQ0#
<24,30,31,33> LPC_AD0
<24,30,31,33> LPC_AD1
<24,30,31,33> LPC_AD2
<24,30,31,33> LPC_AD3
<24,30,31,33> LPC_FRAME#
<31> LPC_DRQ#0
R216 10KOhm
R219 10KOhm
+V3.3S
<23,24,25> PCI_DEVSEL#
<23,24,25> PCI_FRAME#
<23,24,25> PCI_IRDY#
<23,24,25> PCI_TRDY#
<23,24,25> PCI_STOP#
<23,24,25> PCI_PAR
<23,24,25> PCI_PERR#
DEVSEL# FRAME# IRDY# TRDY# STOP# PAR PERR#
<23,24,25> PCI_SERR#
<23> PME_SB#
PCI_LOCK#
PCI_RST#
SERR# PME# PLOCK# PCIRST# PCICLK CLKRUN#/GPIO24
<6,11,28,33> PCI_RST#
4"-8.5"
<22> CLK_ICH33
C598
5PF
/X
design guideline recommended
R201
10KOhm
<24,25,30> PM_CLKRUN#
REQ0# REQ1# REQ2# REQ3# REQ4# REQB#/REQ5#/GPIO1 REQA#/GPIO0
GNT0# GNT1# GNT2# GNT3# GNT4# GNTB#/GNT5#/GPIO17 GNTA#/GPIO16
ICH_GPIO16
T30
TPC28t
ICH4 pin E8
Strap Option
Default:Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP
PCI_AD[31:0] <23,24,25,26>
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25 PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C/BE#0 <23,24,25>
PCI_C/BE#1 <23,24,25>
PCI_C/BE#2 <23,24,25>
PCI_C/BE#3 <23,24,25>
<19,24,25,30,31> INT_SERIRQ
PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 PCI_REQ#3 PCI_REQ#4
PCI_REQ#0 <25>
PCI_REQ#1 <24>
PCI_REQ#2 <23>
R222 10KOhm
R223 10KOhm
design guideline recommend 8.2kohm
PCI_GNT#0 <25>
PCI_GNT#1 <24>
PCI_GNT#2 <23>
+V3.3S_ICH
PCI_FRAME# RP4A
PCI_IRDY# RP4B
PCI_TRDY# RP4C
PCI_STOP# RP4D
PCI_SERR# RP4E
PCI_DEVSEL# RP4F
PCI_PERR# RP4G
PCI_LOCK# RP4H
8.2KOhm
<19,28> INT_IRQ14
<19,29> INT_IRQ15
PCI_REQ#0 RP2C
PCI_REQ#1 RP2D
PCI_REQ#2 RP2E
PCI_REQ#3 RP2F
PCI_REQ#4 RP2G
RP2A RP2B RP2H
PCI_REQ# | PCI_REQ#?
CB&1394 | PCI_REQ#0
MINIPCI | PCI_REQ#1
LAN | PCI_REQ#2
IDSEL | PCI_AD?
CB&1394 | PCI_AD21
MINIPCI | PCI_AD20
LAN | PCI_AD16
R200
10KOhm
C253
0.1uF/10V
U18
NC7SZ08P5X
BUF_PCI_RST# <17,23,24,25,30,31>
Meet LPC reset >= 60 us
(Add Buffer)
ASUSTEK CO.,LTD.
Title : ICH4-M(HUB_PCI)
Engineer: charlie_xie
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 18 of 57



ASUSTEK CO.,LTD.	Title : ICH4-M(IDE_AC97)		
	Engineer: charlie_xie		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 19 of 57		


USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils
LxWxH=31x31x2.38
U20C
FW82801DBM
design guideline
recommended 22.6ohm
USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"
+V3.3S_ICH
+V3.3SUS_ICH
+V3.3
GND
RN38A
RN38B
RN38C
RN38D
RN68A
RN68B
RN68C
RN68D
RN28C
RN28D
10KOhm
R202
100KOhm
R221
18.2Ohm
R193
56Ohm
R189
C245
0.1uF/10V
USB_OC#1
USB_OC#0
PM_BATLOW# <19>
PM_SYSRST#
USBRBIAS
AGP_BUSY#
PM_C3_STAT#
PM_DPRSLPVR
PM_PWRBTN#
ICH4_PWROK
PM_RI#
PM_RSMRST#
SLP_S1#
PM_SLP_S3#
PM_SLP_S4#
PM_STPPCI#
PM_STPCPU#
PM_SUS_STAT#
PM_THRM#
H_THRMTRIP_S#
PM_VGATE
CB_SD#
WLAN_ON#
CG_FS0
CG_FS1
CG_FS2
CG_FS5
CG_FS6
EXTSMI#_3A <30>
KBDSCI_3A <30>
SIO_SMI# <31>
CB_SD# <25>
802_LED_EN# <40>
BACK_OFF# <16>
CG_FS0 <22>
CG_FS1 <22>
CG_FS2 <22>
CG_FS5 <22>
CG_FS6 <22>
CPUFAN_SPD_A <39>
FWH_WP# <31>
HA20GATE <30>
H_A20M# <3>
H_PWRGD <3>
H_CPUSLP# <3>
H_DPSLP# <3,6>
H_FERR# <3>
H_IGNNE# <3>
H_INIT# <3,31>
H_INTR <3>
H_NMI <3>
H_SMI# <3>
H_STPCLK# <3>
KBDCPURST <30>
USB_WLAN_ON# <16>
MPCI_WLAN_ON <24>
Q20A
Q20B
UM6K1N
INTEL REQUEST
U15
NC7SZ08P5X
PM_SLP_S1# <22,39>
Title : ICH4-M(USB_PM)
ASUSTECH CO.,LTD.
Engineer: charlie_xie
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 20 of 57


LxWxH=31x31x2.38
U20D
FW82801DBM
3.135V - 3.465V(+/- 5%)
S0-S1M:0.42A
six capacitors(0.1uf) recommended
1.425V - 1.575V(+/- 5%)
S0-S1M: 0.5A
1.71V - 1.89V(+/- 5%)
S0-S1M:0.5A
V5REF SEQUENCE
(200mA max.)
3.135V - 3.465V(+/- 5%)
S0-S5: 14 mA
1.425V - 1.575V(+/- 5%)
S0-S1M: 64 mA
1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5 A(CPU,MCH,ICH)
3.135V - 3.465V(+/- 5%)
S0-S1M:12mA
RTC_VBIAS <19>
HUB_VREF_ICH4 <18>
LxWxH=31x31x2.38
U20E
FW82801DBM
V5REFSUS
SEQUENCE
all decupling caps should be placed
close to the component pin
Title : ICH4-M(POWER)
ASUSTECH CO.,LTD.
Engineer: charlie_xie
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 21 of 57


I2C address:D2H
3.3V+/-5%
S1M:40mA
S0:360mA
應儘量靠近各pin.
靠近CPU和MCH,以確保BCLK信號品質.
U12
ICS950815
Vtt_PWRGD#
VID5
VID4
VID3
VID2
VID1
VID0
FS3/PCICLK_F0
FS4/PCICLK_F1
ASEL/PCICLK_F2
MULTSEL0/PCICLK0
MODE/PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
3V66_0
3V66_1
3V66_2
3V66_3/48MHz_2
VDDREF
VDDPCI1
VDDPCI2
VDD3V66
VDDCPU1
VDDCPU2
VDDA
VDD48
CPUCLKT2
CPUCLKC2
CPUCLKT1
CPUCLKC1
CPUCLKT0(FS6)
CPUCLKC0(FS5)
REF0
48MHz_1
48MHz_0
SDATA
SCLK
CPU_STOP#
PCI_STOP#
PD#
IREF
FS2
FS1
FS0
+V3.3_CLK
+V3.3_CLKA
+V3.3_CLK48
+V3.3S
CLK_EN#
CLK_X1
CLK_X2
14.318Mhz
CLK_ICH33
CLK_MINIPCI33
CLK_PO8033
CLK_LAN33
CLK_CB139433
CLK_SIO33
CLK_FWH33
CLK_KBC33
CLK_MCH66
CLK_AGP66
CLK_ICH66
CLK_CPU100
CLK_CPU100#
CLK_MCH100
CLK_MCH100#
CLK_ICH14
CLK_SIO48
CLK_ICH48
CG_FS6
CG_FS5
CG_FS2
CG_FS1
CG_FS0
SDA_3S
SCL_3S
PM_STPCPU#
PM_STPPCI#
PM_SLP_S1#
HOST_CLK GROUP
in L6
Pair Width/Space:5/5mils
Group Space:>=25mils
Lengeh Match:+/-10 mils
CLK33 GROUP:
In L4 or L6
Breakout
W/S:5/20mils(<=0.3")
Group Space >=20mils
Length Match
:same as
CLK66
CLK66 GROUP:
In L4 or L6
Breakout
W/S:4/20mils(<=0.3")
Group Space >=20mils
Length Match
:+/-100 mils
FS4 FS3 FUNCTION
0 0 100MHZ(D)
0 1 133MHZ
1 0 200MHZ
1 1 166MHZ
Title : CLOCK-ICS950815
ASUSTECH CO.,LTD.
Engineer: DEL_TAN
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
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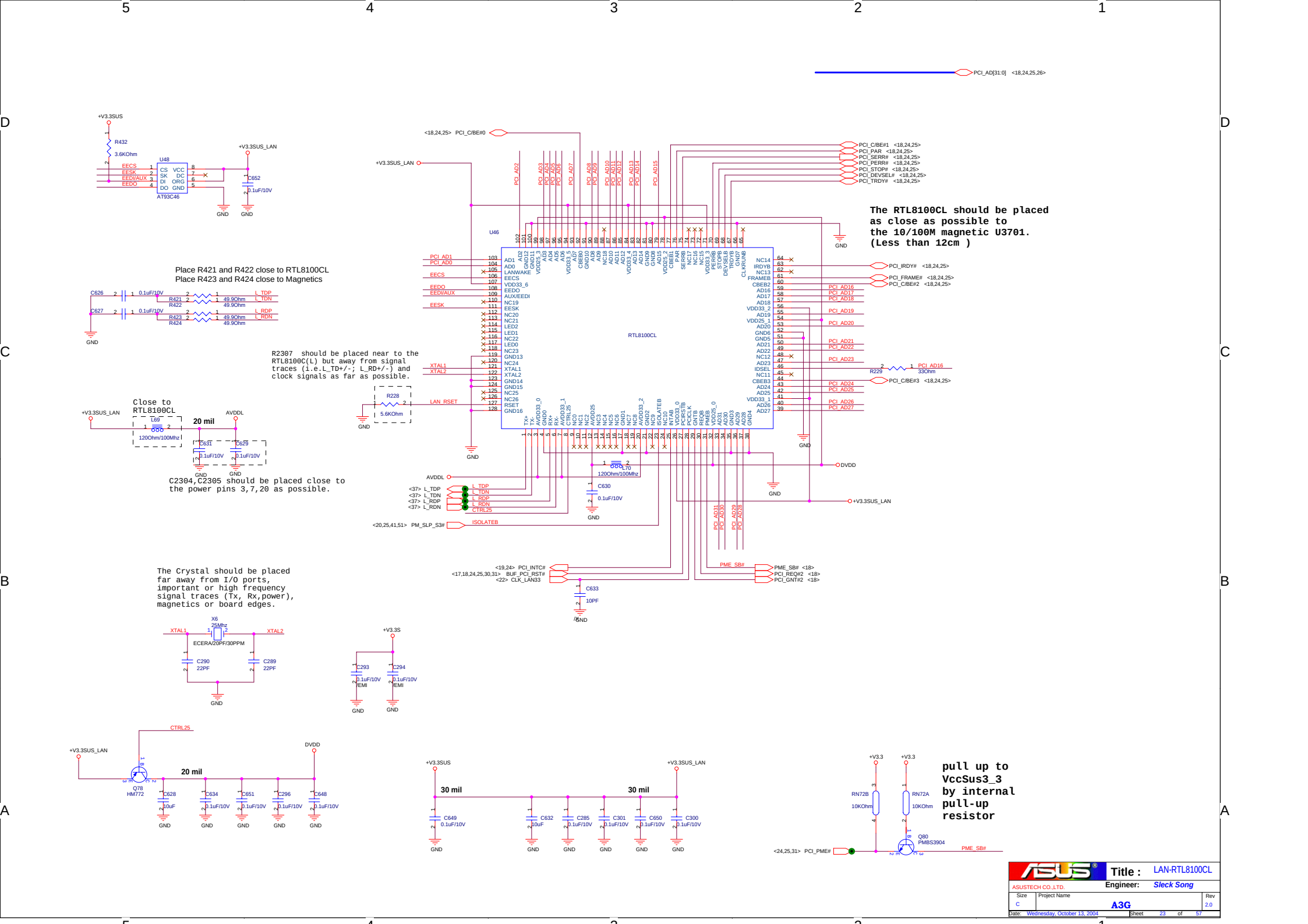
PCI_AD[31:0] <18,24,25,26>
+V3.3SUS
R432
3.6KOhm
U48
EECS
EESK
EEDI/AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46
+V3.3SUS_LAN
C652
0.1uF/10V
GND
<18,24,25> PCI_C/BE#0
+V3.3SUS_LAN
U46
RTL8100CL
PCI_C/BE#1 <18,24,25>
PCI_PAR <18,24,25>
PCI_SERR# <18,24,25>
PCI_PERR# <18,24,25>
PCI_STOP# <18,24,25>
PCI_DEVSEL# <18,24,25>
PCI_TRDY# <18,24,25>
The RTL8100CL should be placed as close as possible to the 10/100M magnetic U3701. (Less than 12cm)
PCI_IRDY# <18,24,25>
PCI_FRAME# <18,24,25>
PCI_C/BE#2 <18,24,25>
PCI_C/BE#3 <18,24,25>
Place R421 and R422 close to RTL8100CL
Place R423 and R424 close to Magnetics
C626
C627
R421
R422
R423
R424
49.9Ohm
L_TDP
L_TDN
L_RDP
L_RDN
R2307 should be placed near to the RTL8100C(L) but away from signal traces (i.e.L_TD+/-; L_RD+/-) and clock signals as far as possible.
R228
5.6KOhm
LAN_RSET
XTAL1
XTAL2
Close to RTL8100CL
L69
120Ohm/100Mhz
20 mil
AVDDL
C631
C629
0.1uF/10V
C2304,C2305 should be placed close to the power pins 3,7,20 as possible.
L70
C630
DVDD
<37> L_TDP
<37> L_TDN
<37> L_RDP
<37> L_RDN
CTRL25
ISOLATEB
<20,25,41,51> PM_SLP_S3#
<19,24> PCI_INTC#
<17,18,24,25,30,31> BUF_PCI_RST#
<22> CLK_LAN33
C633
10PF
PME_SB#
PCI_REQ#2 <18>
PCI_GNT#2 <18>
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
X6
25Mhz
ECERA/20PF/30PPM
C290
22PF
C289
22PF
+V3.3S
C293
C294
/EMI
Q78
HM772
C628
10uF
C634
C651
C296
C648
0.1uF/10V
30 mil
C649
C632
C285
C301
C650
C300
pull up to VccSus3_3 by internal pull-up resistor
RN72B
RN72A
10KOhm
Q80
PMBS3904
<24,25,31> PCI_PME#
Title : LAN-RTL8100CL
ASUSTECH CO.,LTD.
Engineer: Sleck Song
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
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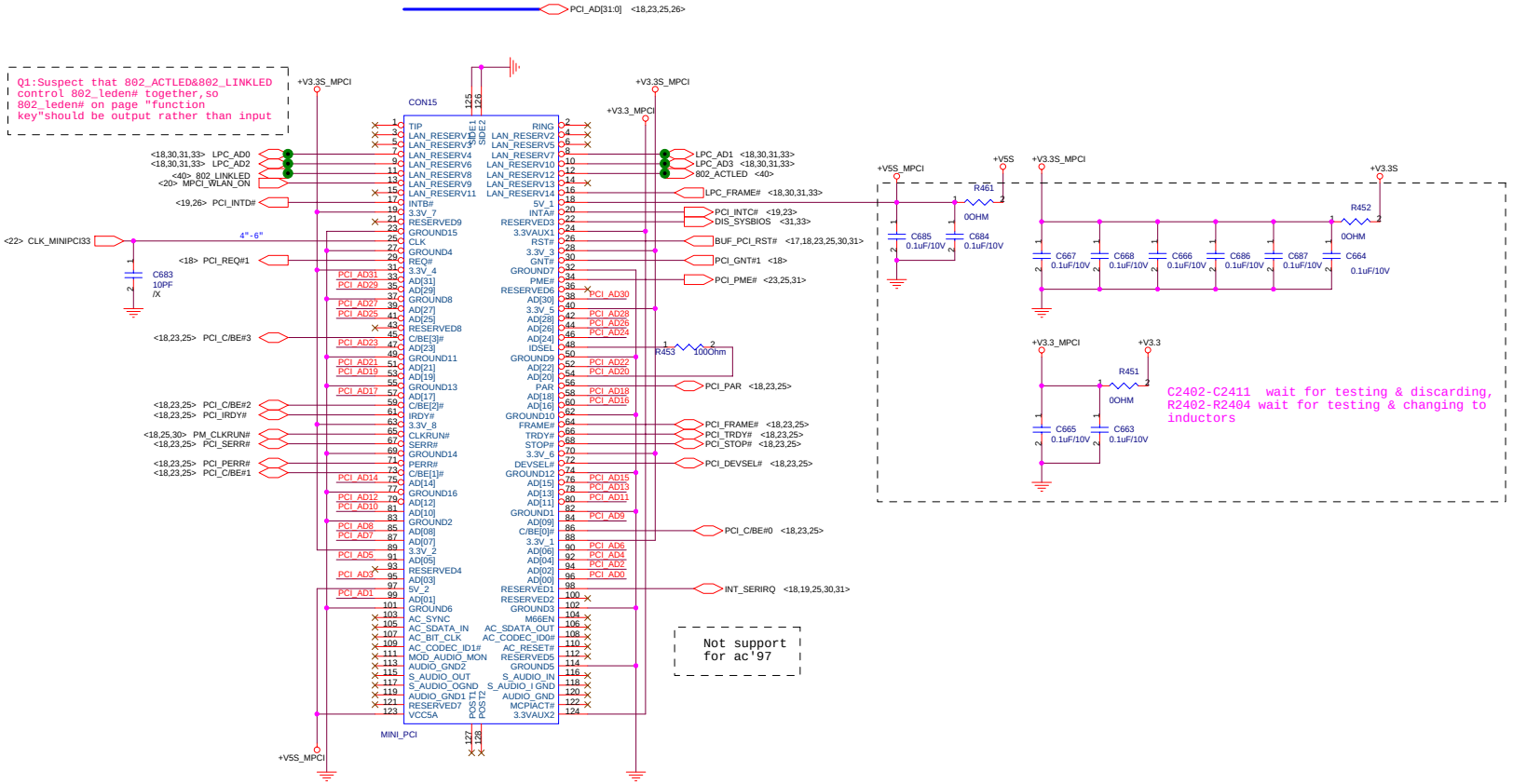
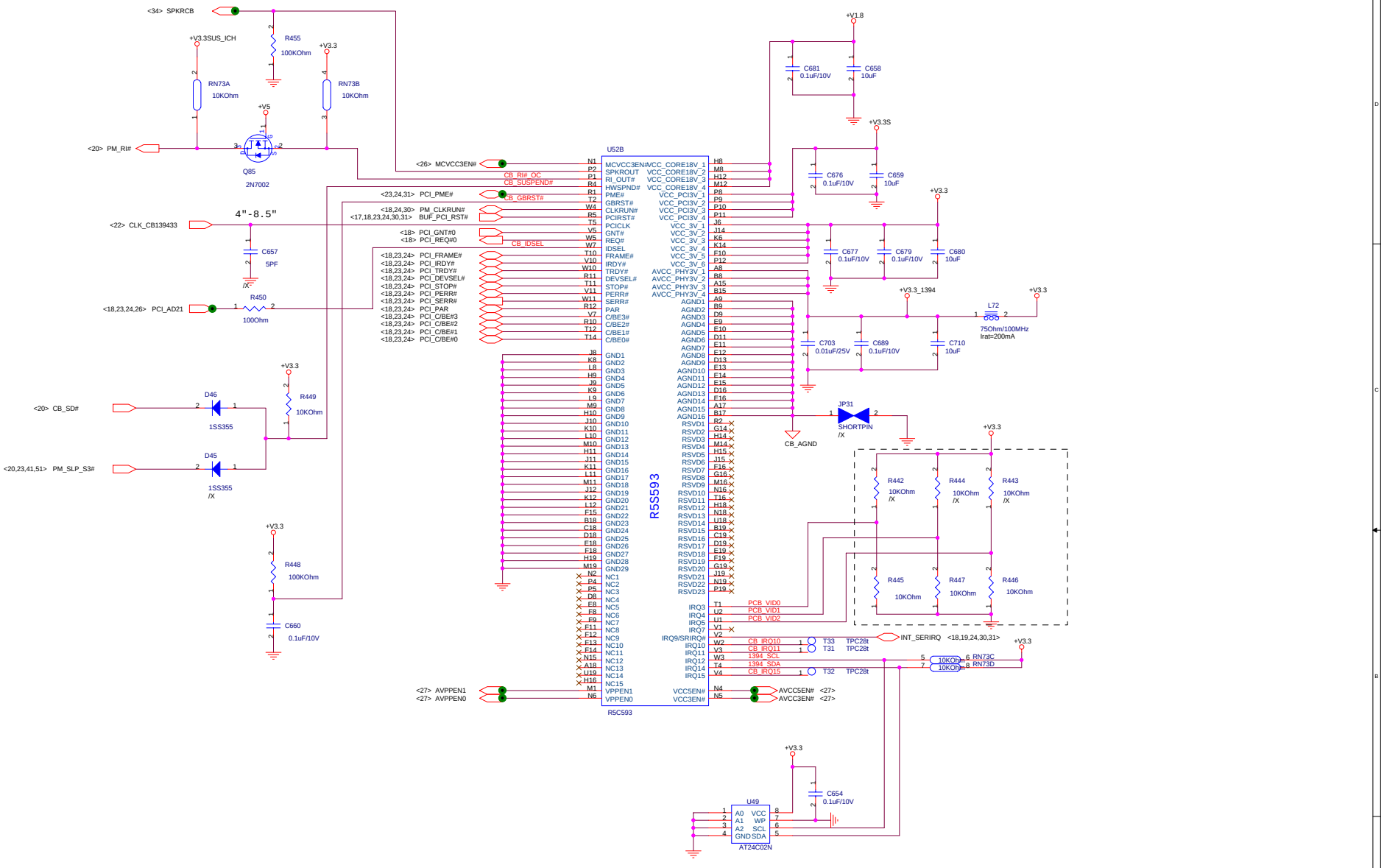


ASUSTECH CO.,LTD.	Title : MINIPCI	
	Engineer: July Ma	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 24 of 57	

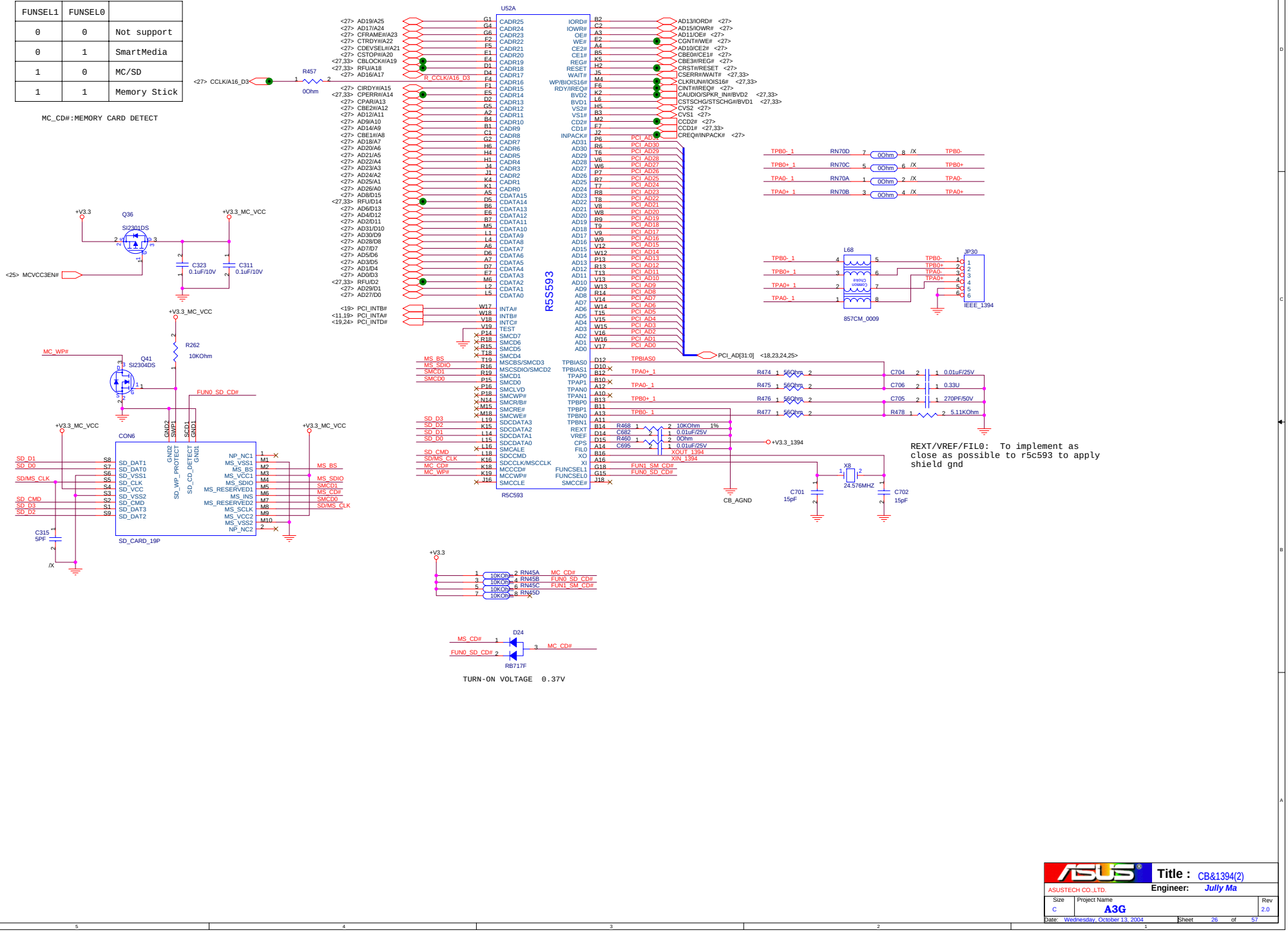


ASUSTEK CO.,LTD.	Title : CB&1394(1)	
	Engineer: Jully Ma	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 25 of 57	

Memory Card Detect

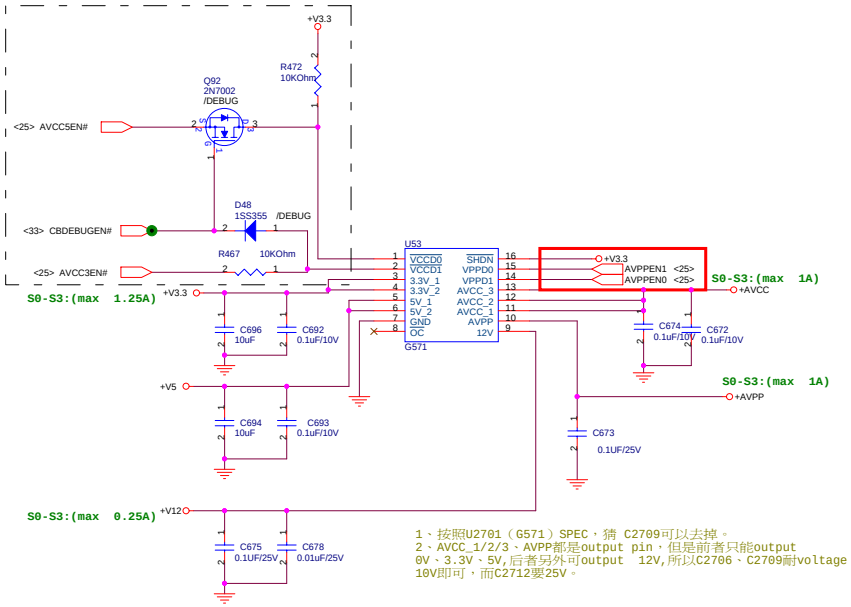
FUNSEL1	FUNSEL0	
0	0	Not support
0	1	SmartMedia
1	0	MC/SD
1	1	Memory Stick

MC_CD#:MEMORY CARD DETECT



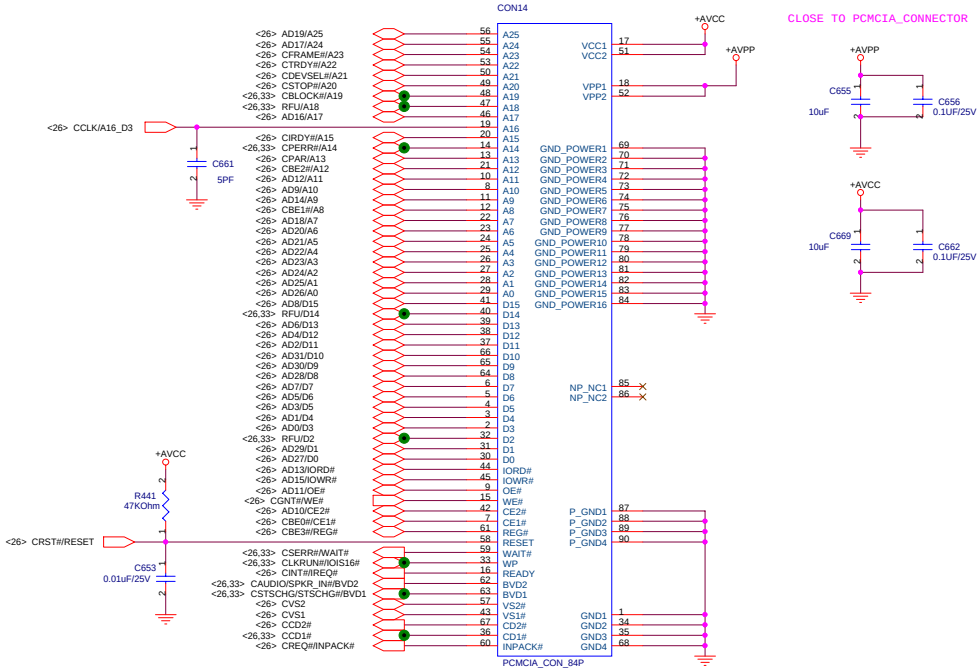
ASUSTECH CO.,LTD.		Title : CB&1394(2)		
		Engineer: Jully Ma		
Size C	Project Name A3G			Rev 2.0
Date: Wednesday, October 13, 2004		Sheet 26 of 57		

CB POWER SWITCH

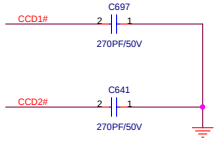


1、按照U2701（G571）SPEC，猜 C2709可以去掉。
2、AVCC_1/2/3、AVPP都是output pin，但是前者只能output 0V、3.3V、5V,后者另外可output 12V,所以C2706、C2709耐voltage 10V即可，而C2712要25V。

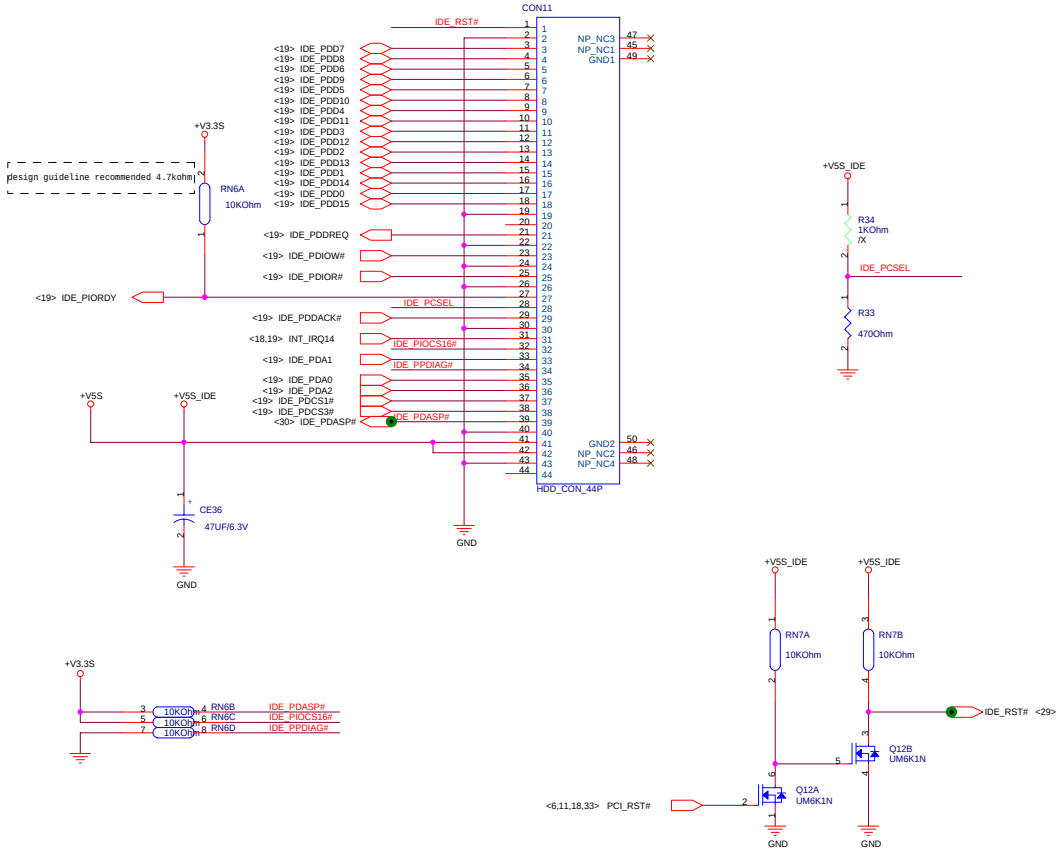
CB SOCKET



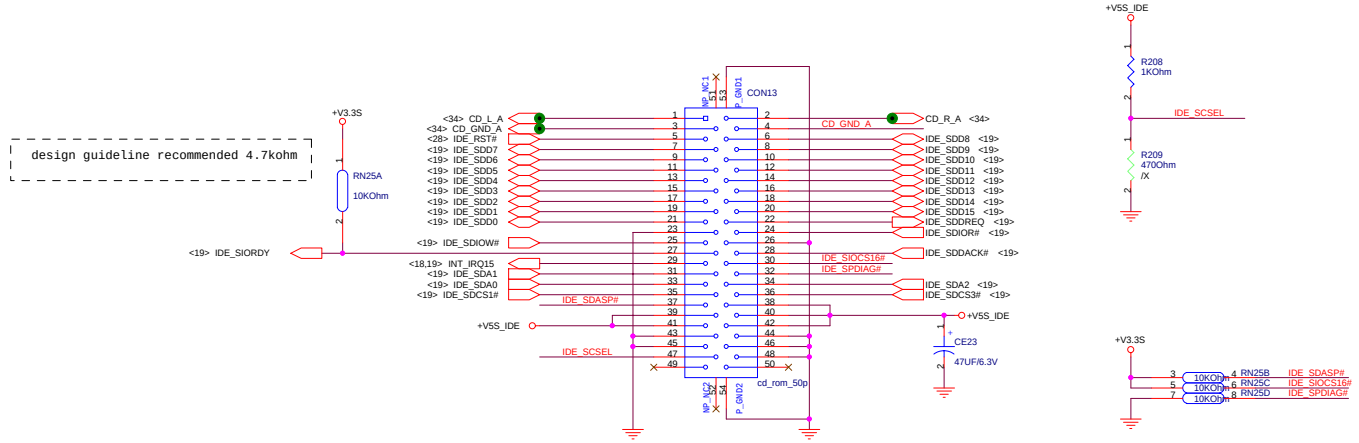
CB DE-BOUNCE



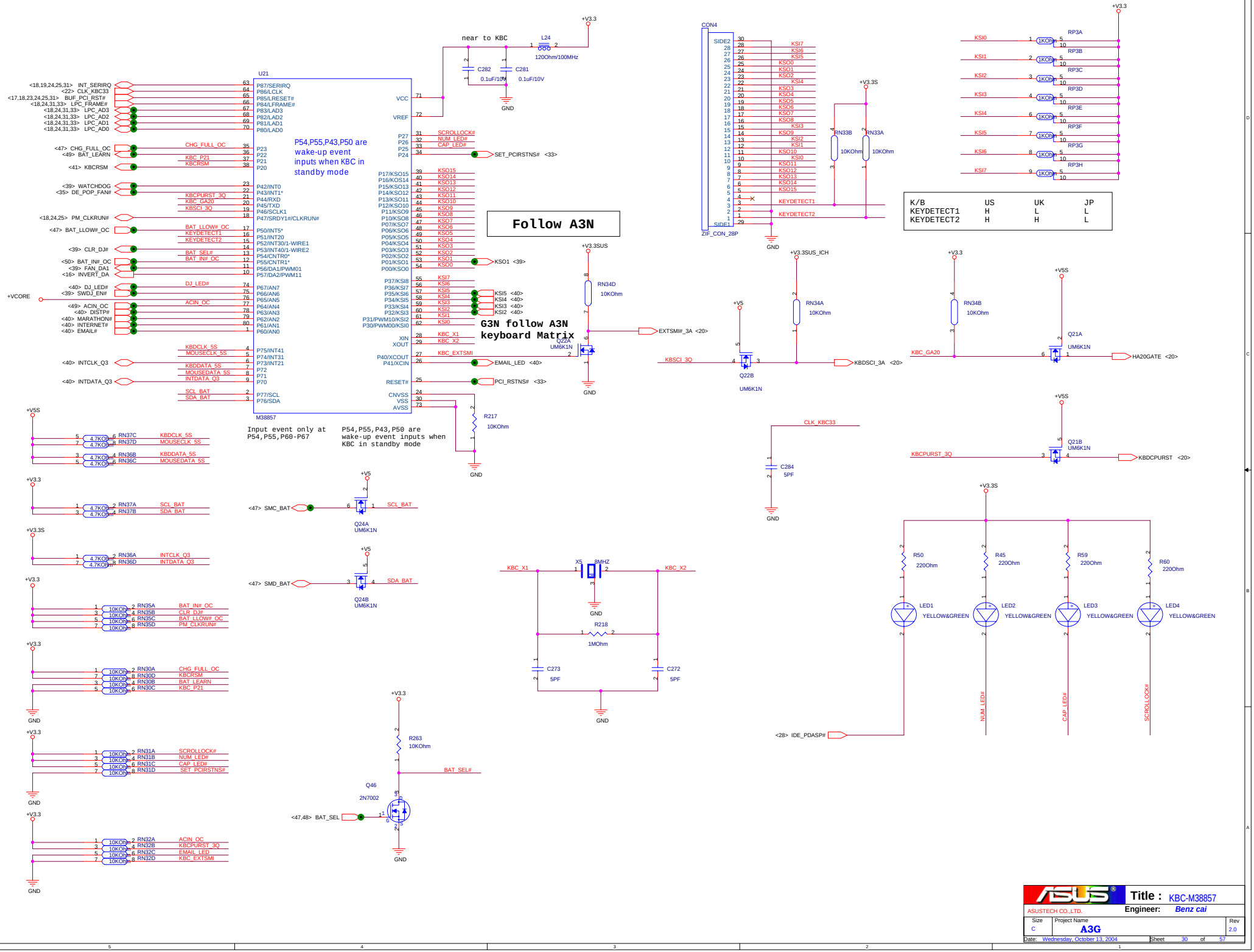
ASUSTEK CO.,LTD.	Title : PCMCIA SOCKET	
	Engineer: Jully_ma	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 27 of 57	



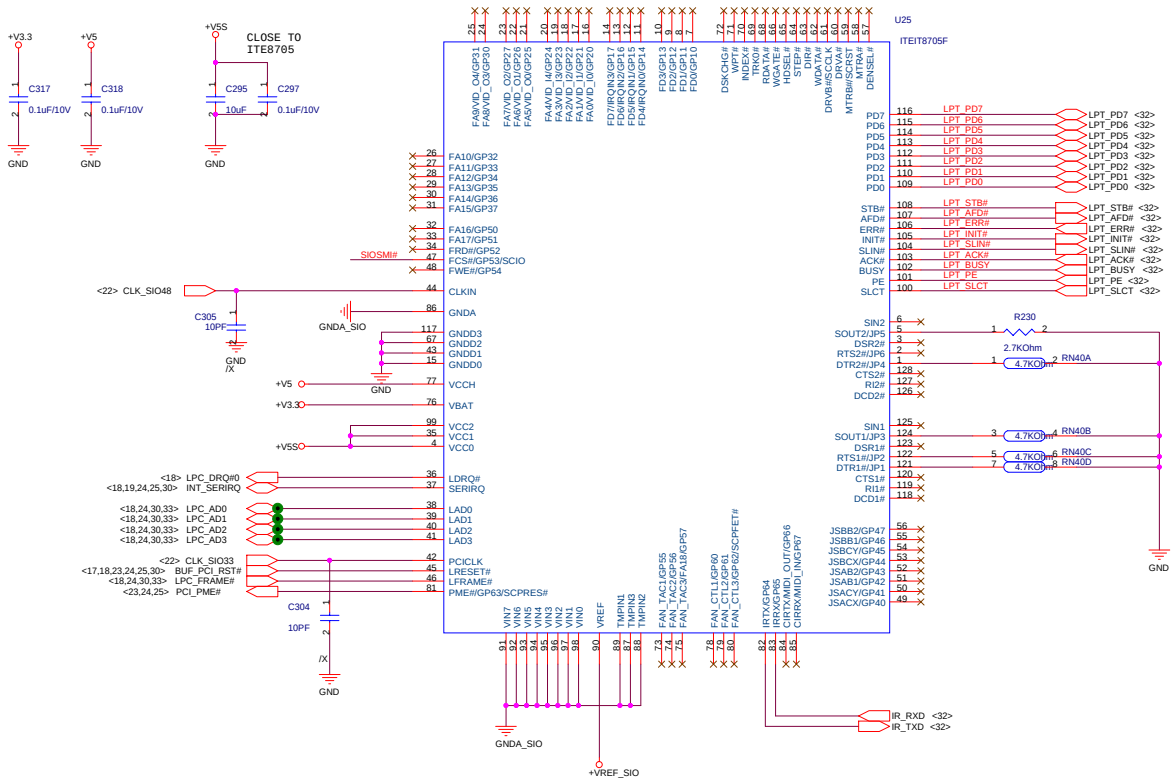
ASUSTECH CO.,LTD.	Title : IDE(HDD)	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 28 of 57	



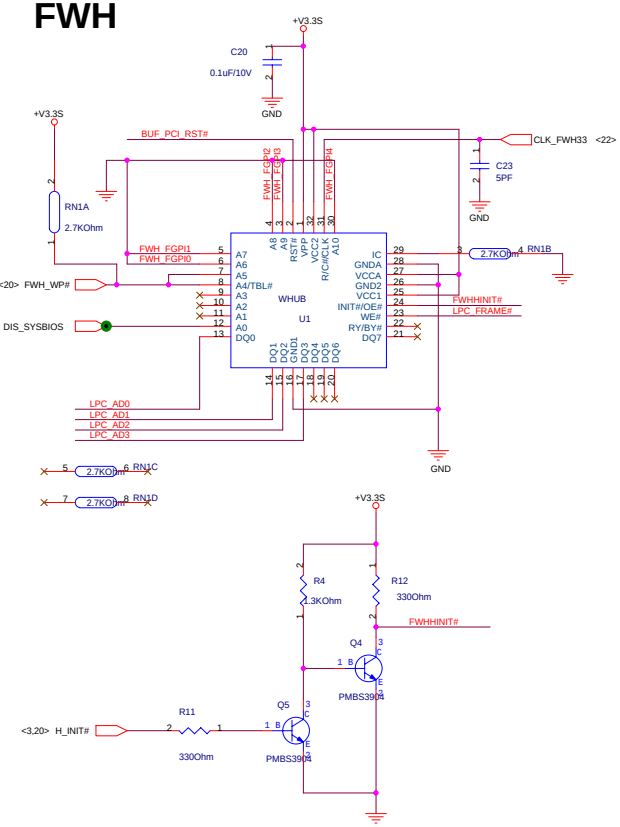
ASUSTECH CO.,LTD.	Title : IDE(ODD)	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 29 of 57	

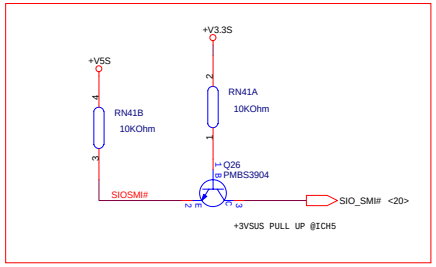

U21
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Follow A3N
G3N follow A3N keyboard Matrix
Input event only at P54,P55,P60-P67
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
near to KBC
L24
120Ohm/100MHz
C282
0.1uF/10V
C281
0.1uF/10V
CON4
ZIF_CON_28P
K/B US UK JP
KEYDETECT1 H L L
KEYDETECT2 H H L
RP3A
RP3B
RP3C
RP3D
RP3E
RP3F
RP3G
RP3H
RN33B
RN33A
RN34D
RN34A
RN34B
Q22A
Q22B
Q21A
Q21B
Q24A
Q24B
UM6K1N
X5
8MHZ
R218
1MOhm
C273
C272
5PF
C284
R217
10KOhm
R263
Q46
2N7002
R50
R45
R59
R60
220Ohm
LED1
LED2
LED3
LED4
YELLOW&GREEN
NUM_LED#
CAP_LED#
SCROLLOCK#
ASUSTECH CO.,LTD.
Title : KBC-M38857
Engineer: Benz cai
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 30 of 57

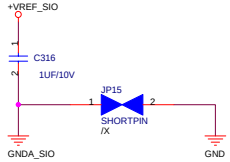
Super I/O



FWH



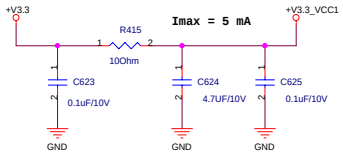


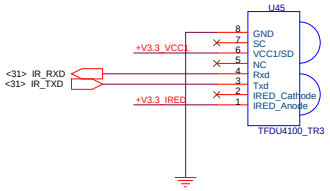


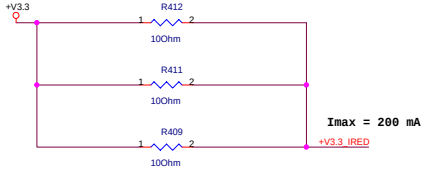
CLOSE TO ITE8705

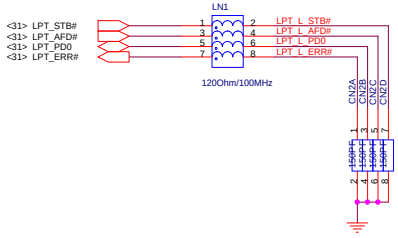
ASUSTEK CO.,LTD.	Title : SuperI/O&FWH	
	Engineer: Lassie_Bao	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 31 of 57	

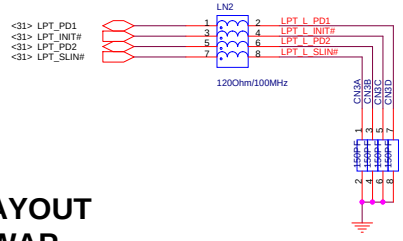
IR

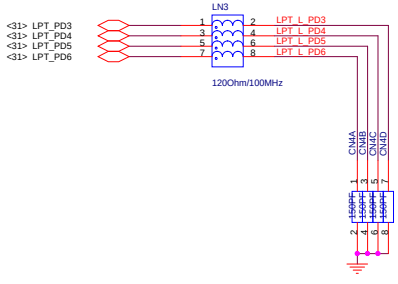


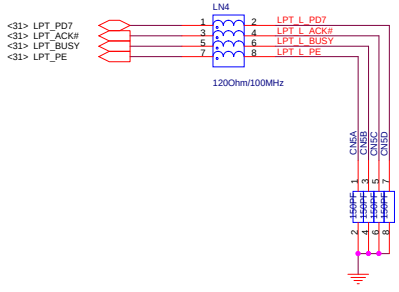




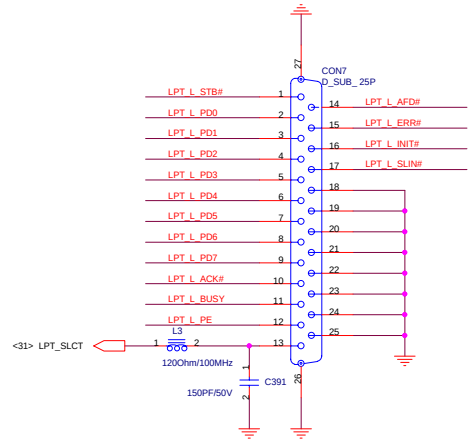








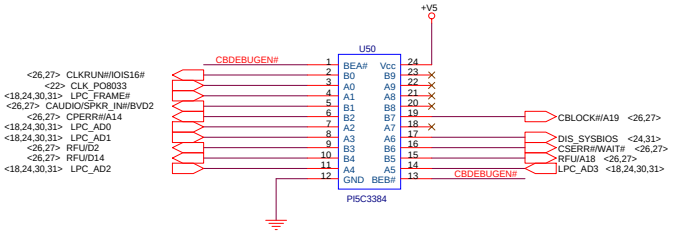
LAYOUT SWAP

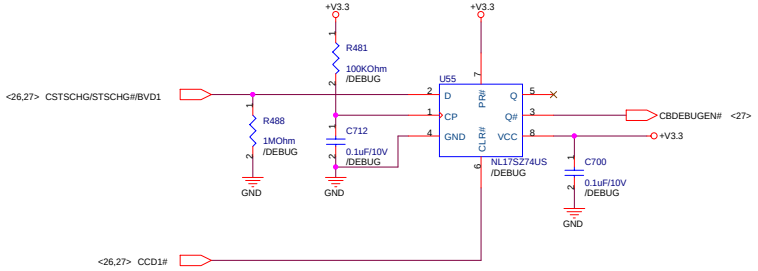


PRINT PORT

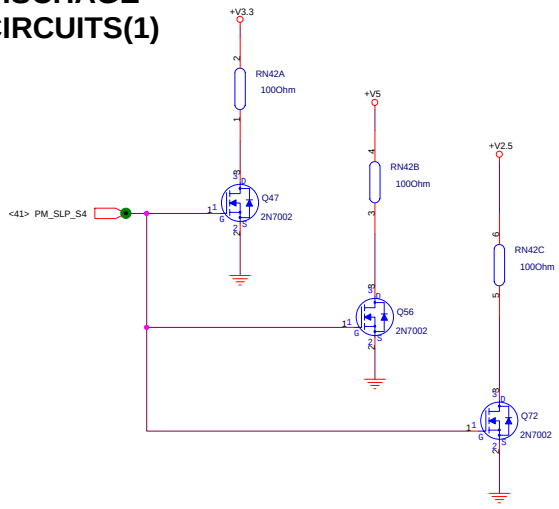
ASUSTECH CO.,LTD.	Title : IR&LPT PORT	
	Engineer: Lassie_Bao	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 32 of 57	

PCMCIA DEBUG CARD

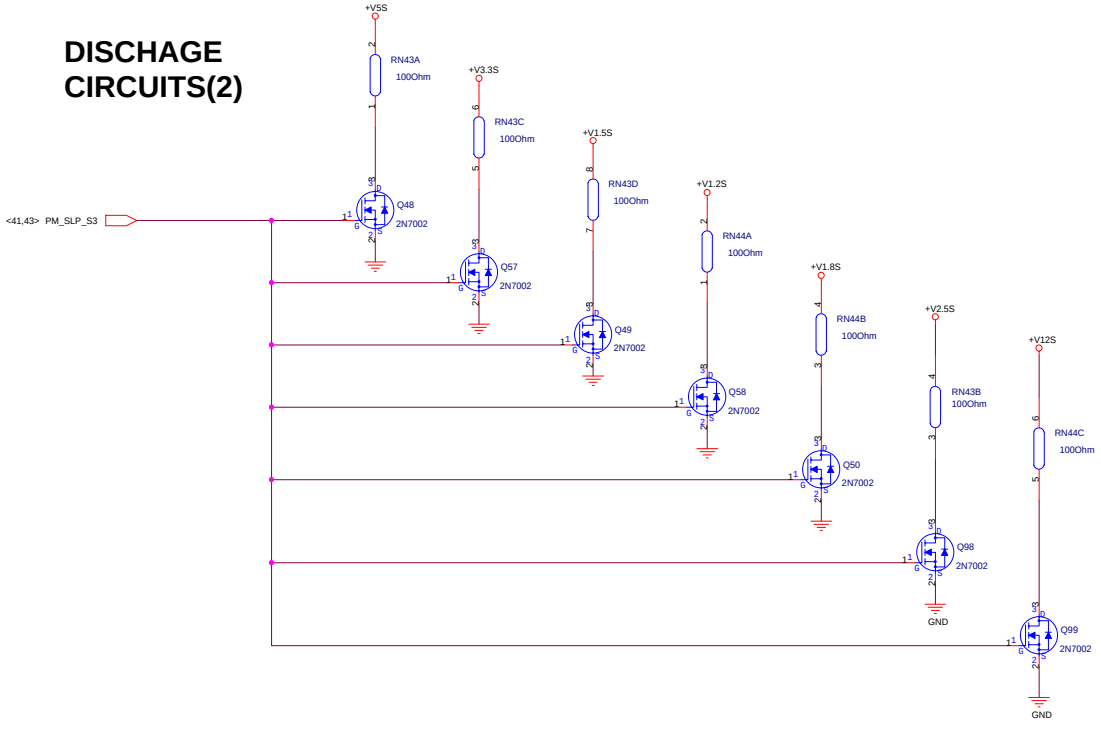




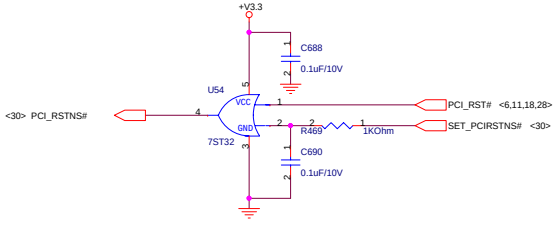
DISCHAGE CIRCUITS(1)



DISCHAGE CIRCUITS(2)



PCI_RSTNS# Gen Circuit



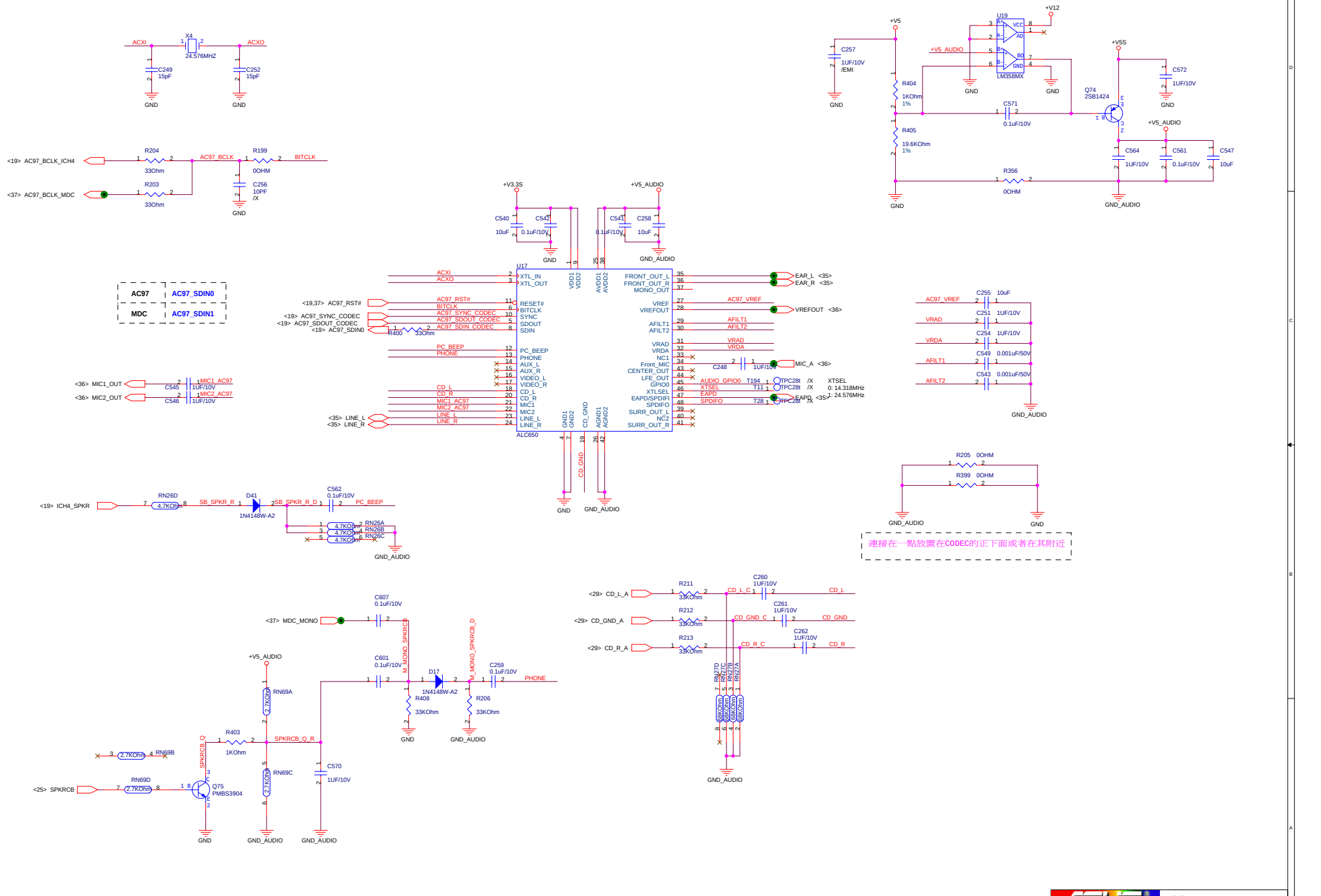
ASUSTEK CO.,LTD.

Title : DEBUG PORT

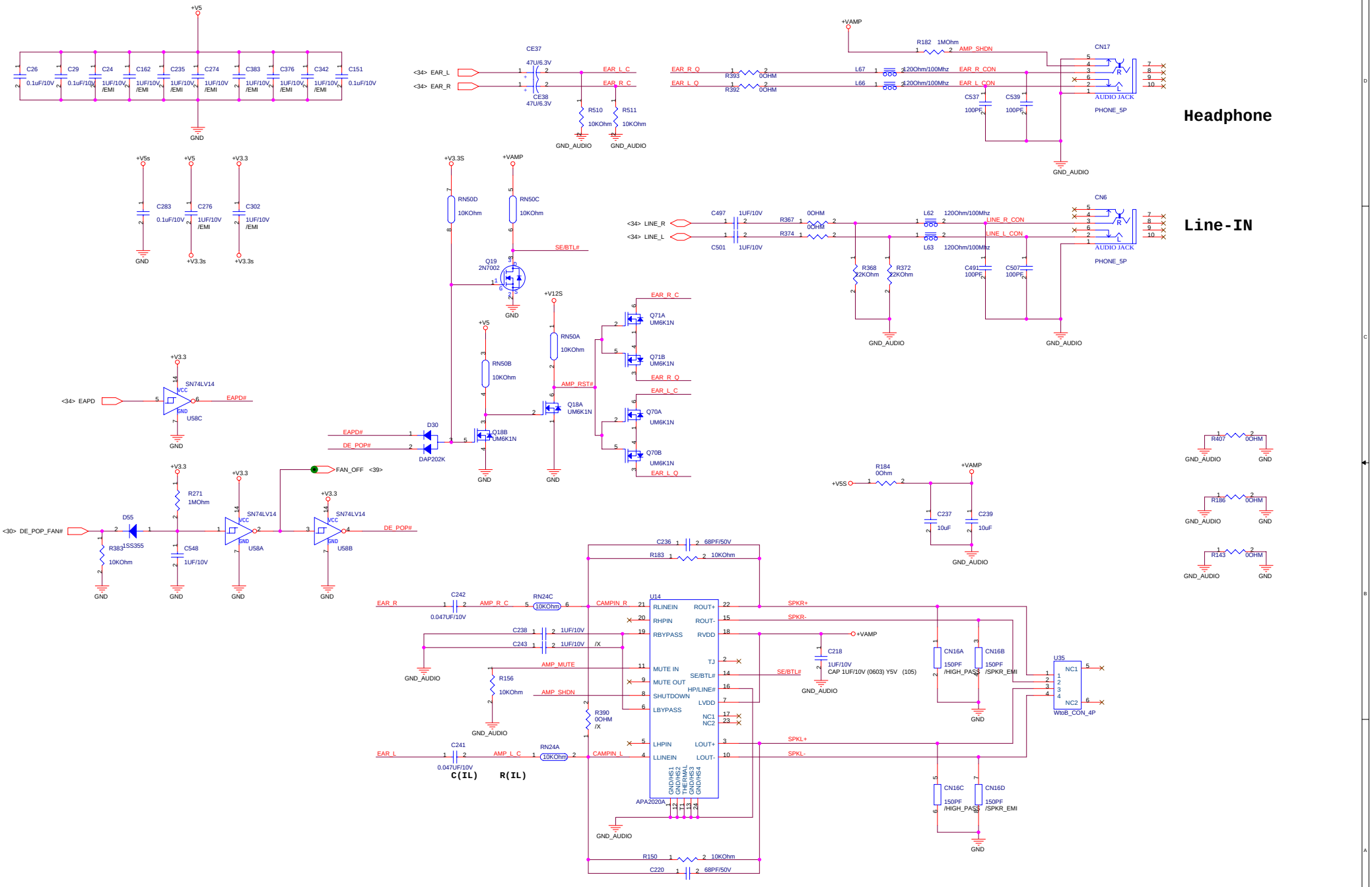
Engineer: Lassie_Bao

Size	Project Name	Rev
C	A3G	2.0

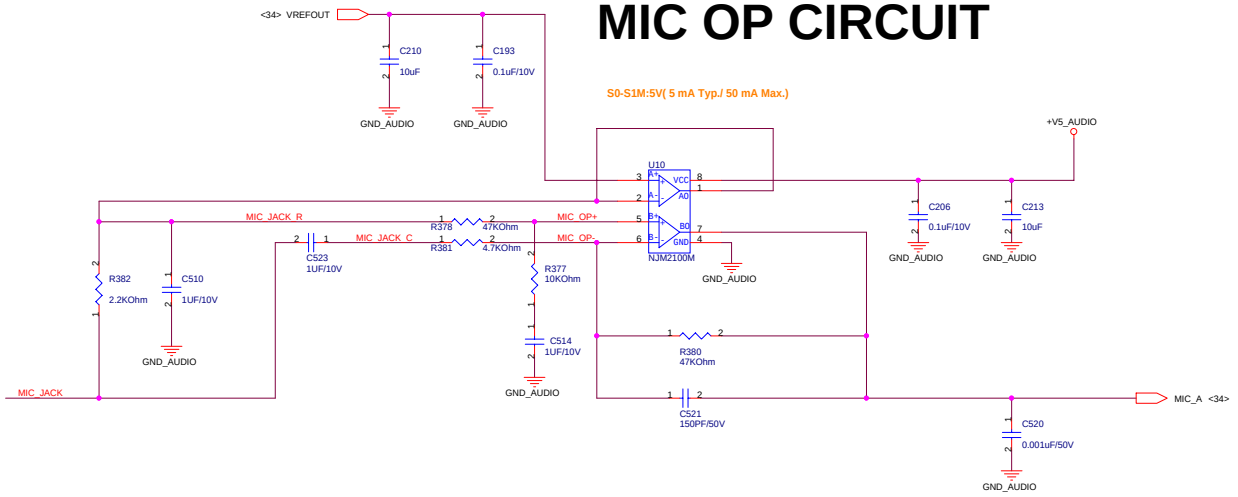
Date: Wednesday, October 13, 2004 Sheet 33 of 57



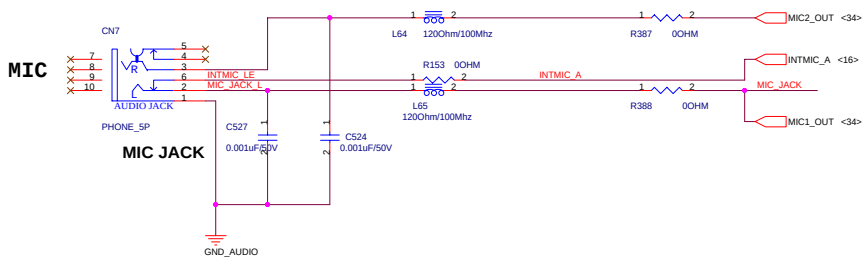
ASUSTEK CO.,LTD.	Title : CODEC-ALC650		
	Engineer: Nanny Zhang		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 34 of 57		


Headphone
Line-IN
C(IL) R(IL)
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
Title : AUDIO AMP
ASUSTECH CO.,LTD.
Engineer: Nanny Zhang
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 35 of 57

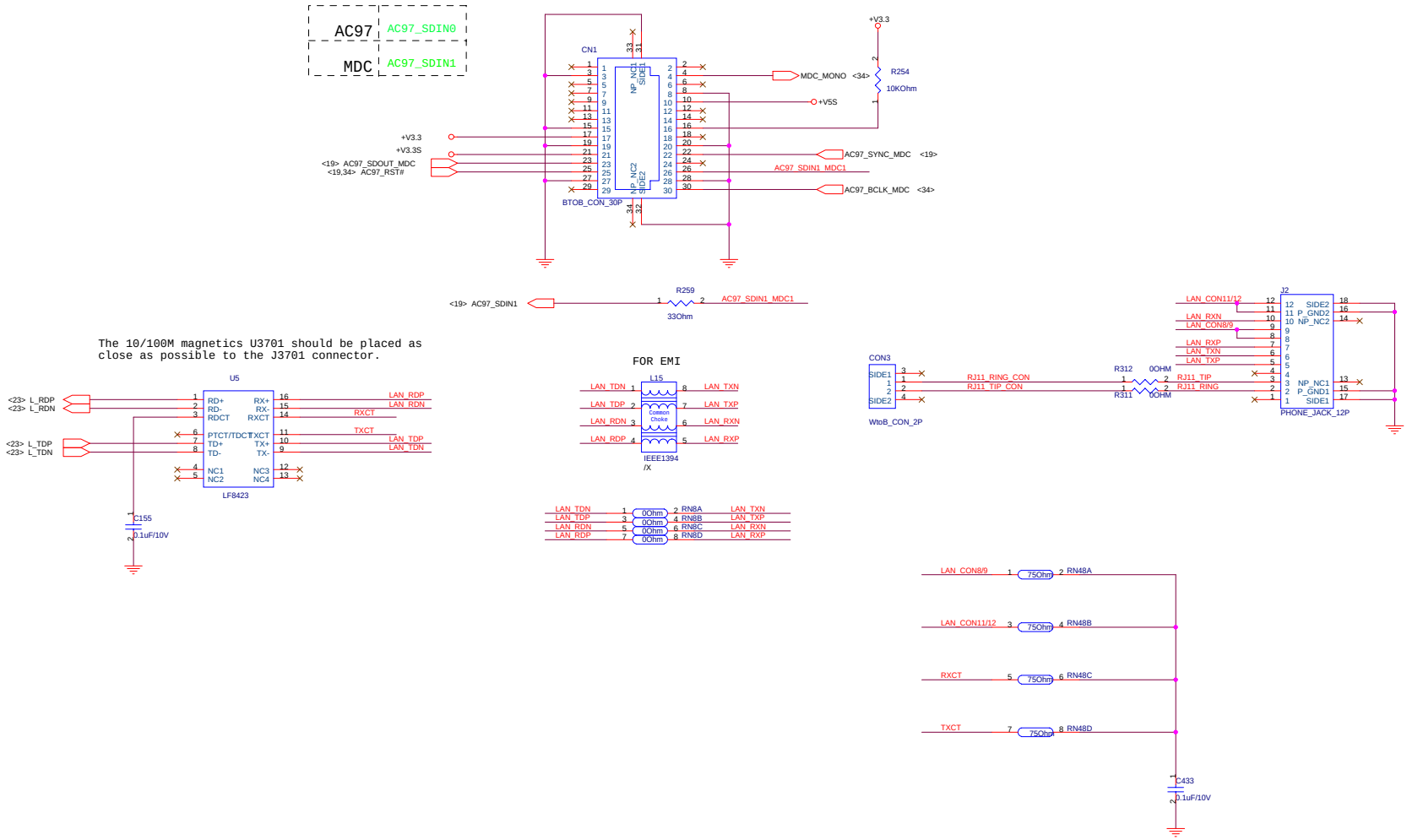
MIC OP CIRCUIT



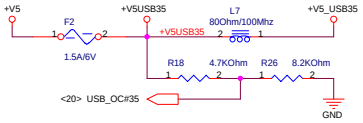
MIC JACK

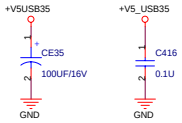


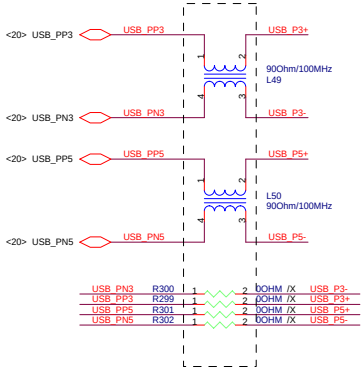
ASUSTECH CO.,LTD.	Title : MIC	
	Engineer: Nanny Zhang	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 36 of 57	



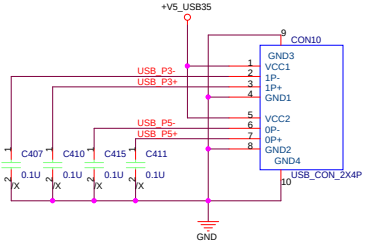
Title :	MDC&RJ45&RJ11
ASUSTECH CO.,LTD.	Engineer: Sleck Song
Size: C	Project Name: A3G
Rev: 2.0	
Date: Wednesday, October 13, 2004	Sheet 37 of 57





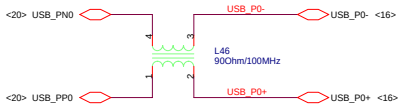


C & L Co-Lay

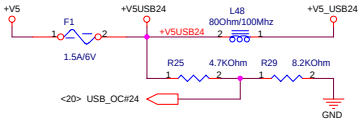


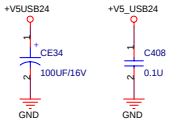
USB PORT 3 & PORT 5

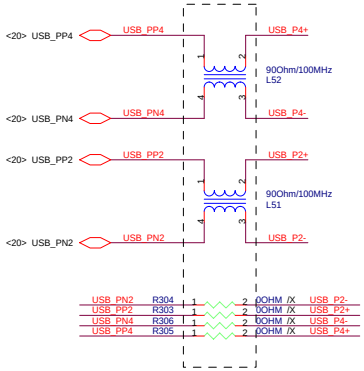
USB PORT 0 for WLAN



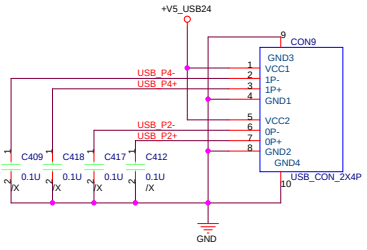
choke位置的原因,Port 0 正負與其他Port相反 (03/17)





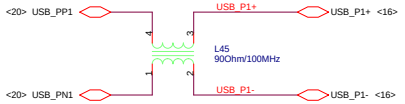


C & L Co-Lay



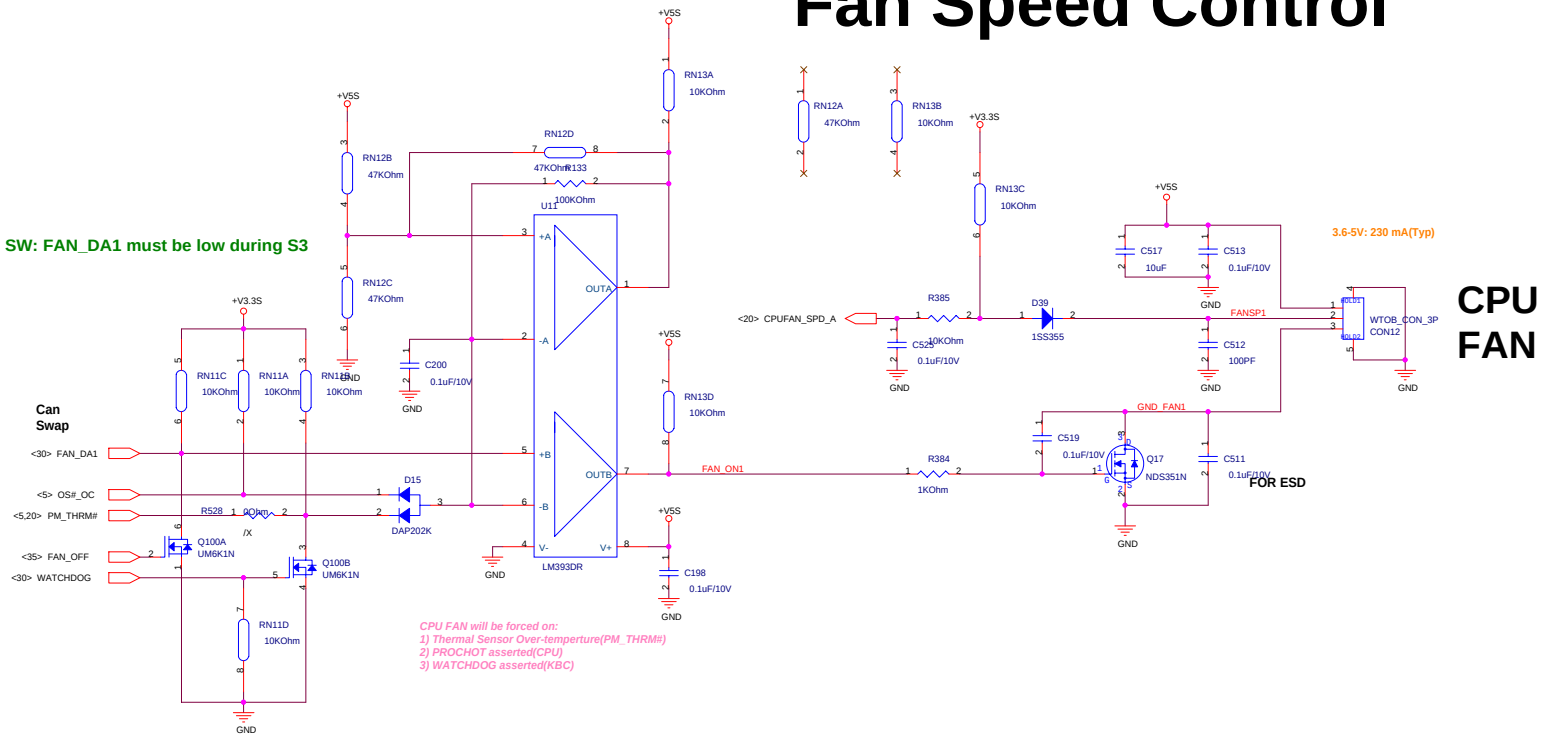
USB PORT 2 & PORT 4

USB PORT 1 for CAMERA



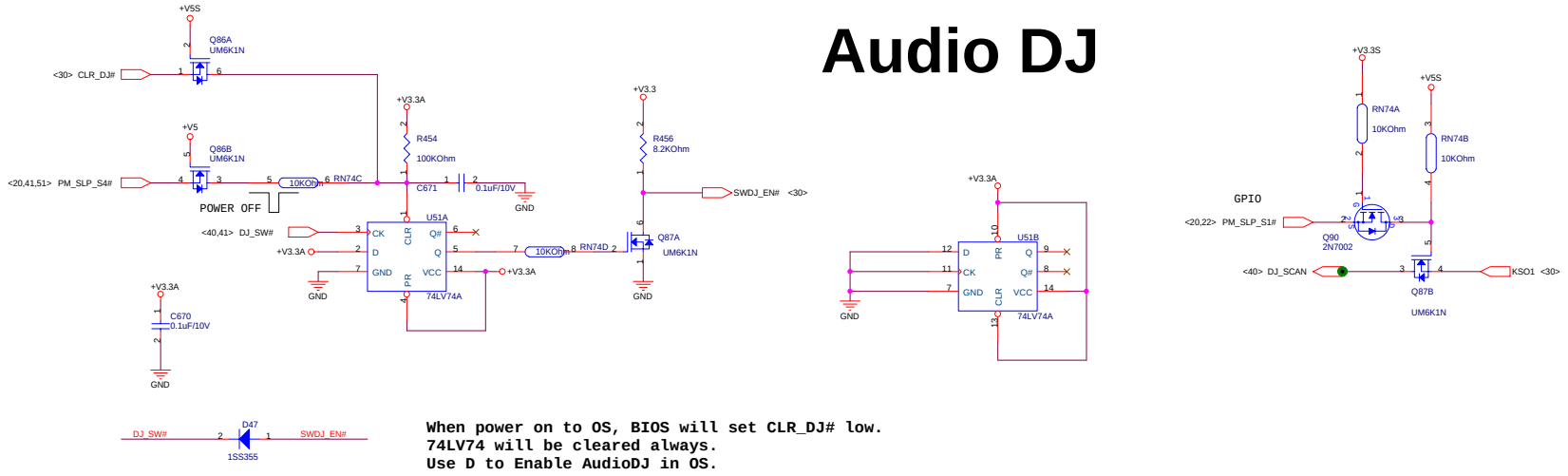
ASUSTEK CO.,LTD.	Title : USBPORT	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 38 of 57	

Fan Speed Control



CPU FAN

Audio DJ



When power on to OS, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D to Enable AudioDJ in OS.

ASUSTECH CO.,LTD.	Title : FAN&Audio DJ	
	Engineer: BENZ CAI	
Size: C	Project Name: A3G	Rev: 2.0
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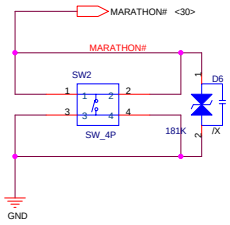
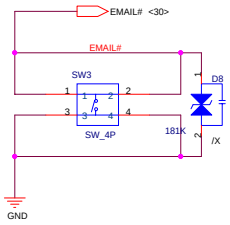
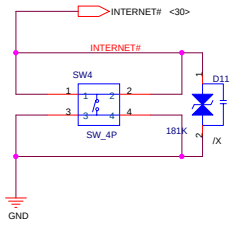


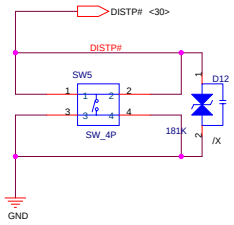
Power4 Gear
FOLLOW A3N



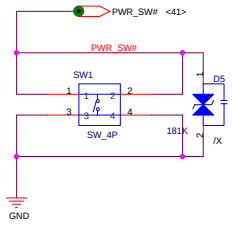
E-Mail
FOLLOW A3N



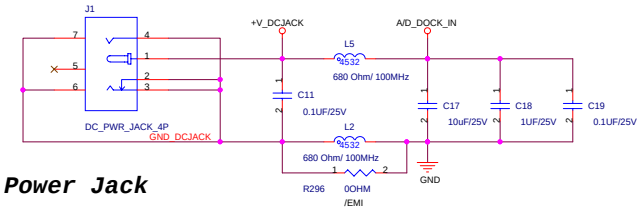
Internet
FOLLOW A3N



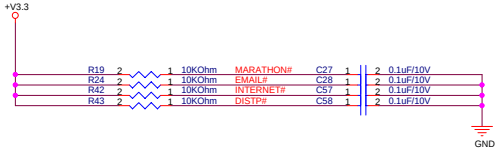
Touchpad Disable
FOLLOW A3N

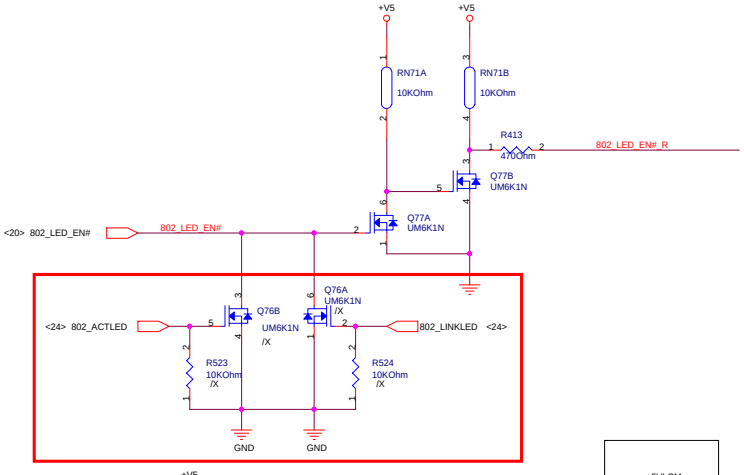


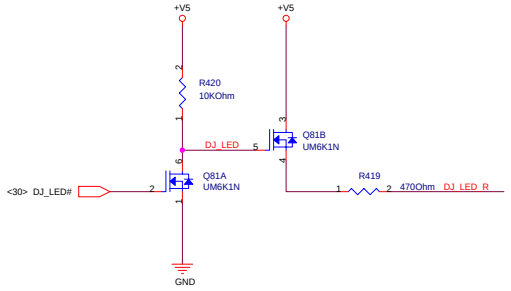
Power Switch
FOLLOW A3N

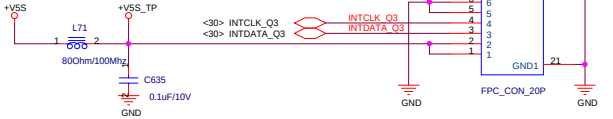


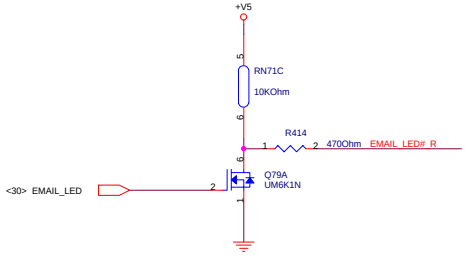
DC Power Jack

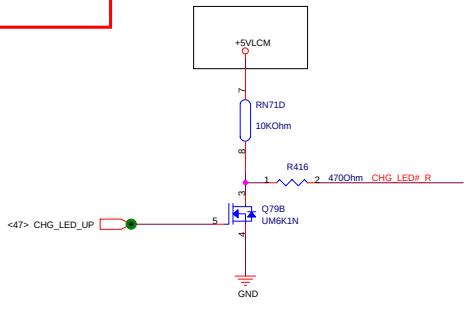


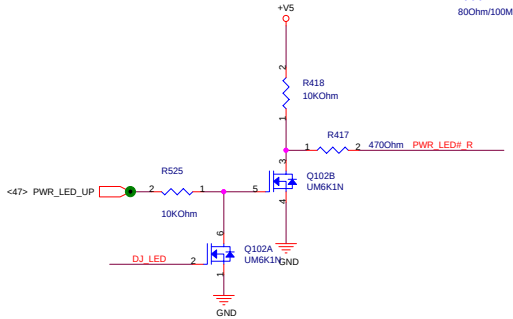












ASUSTEK CO.,LTD.

Title : FUNCTION KEY

Engineer: BENZ CAI

Size	Project Name	Rev
C	A3G	2.0

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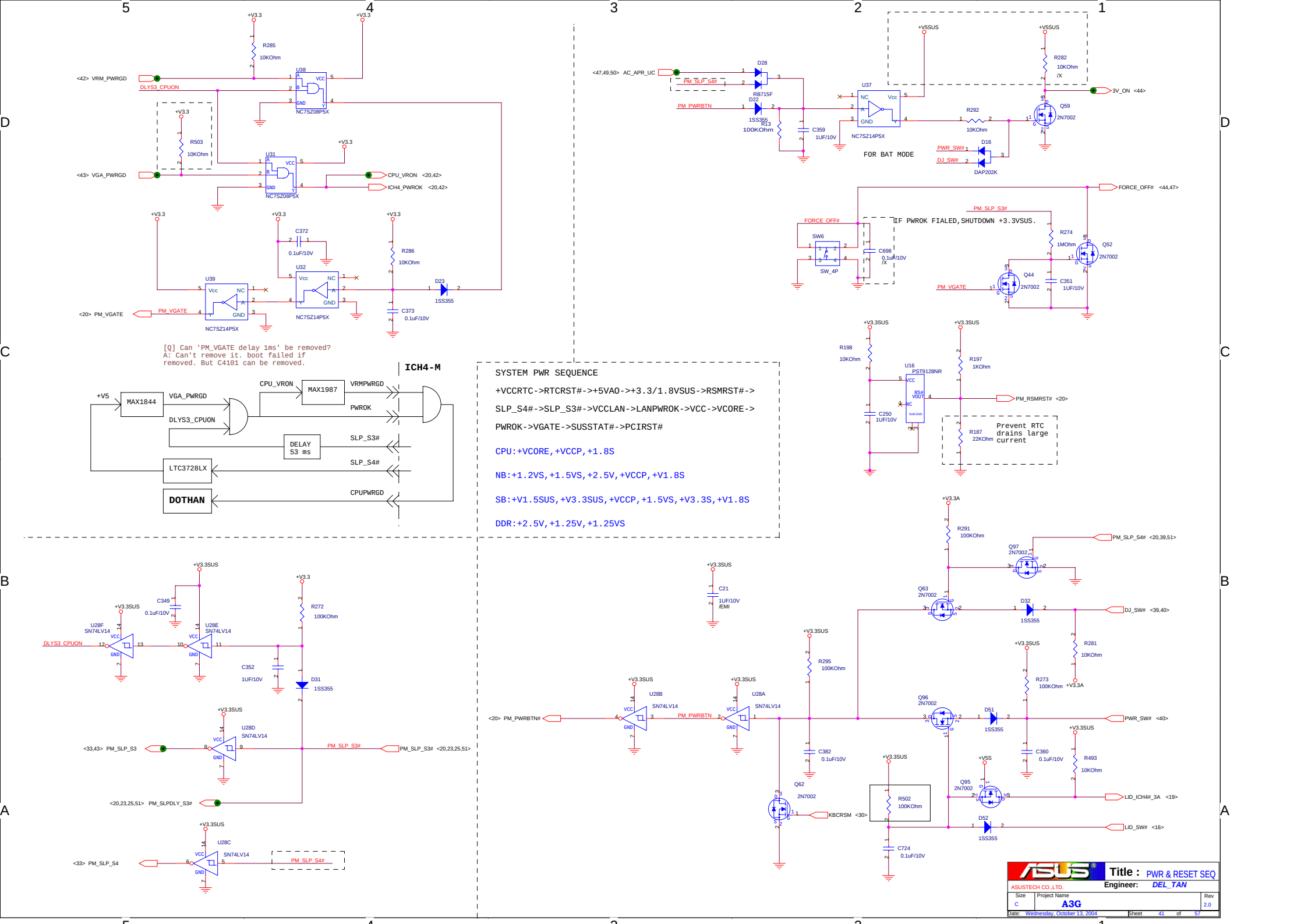
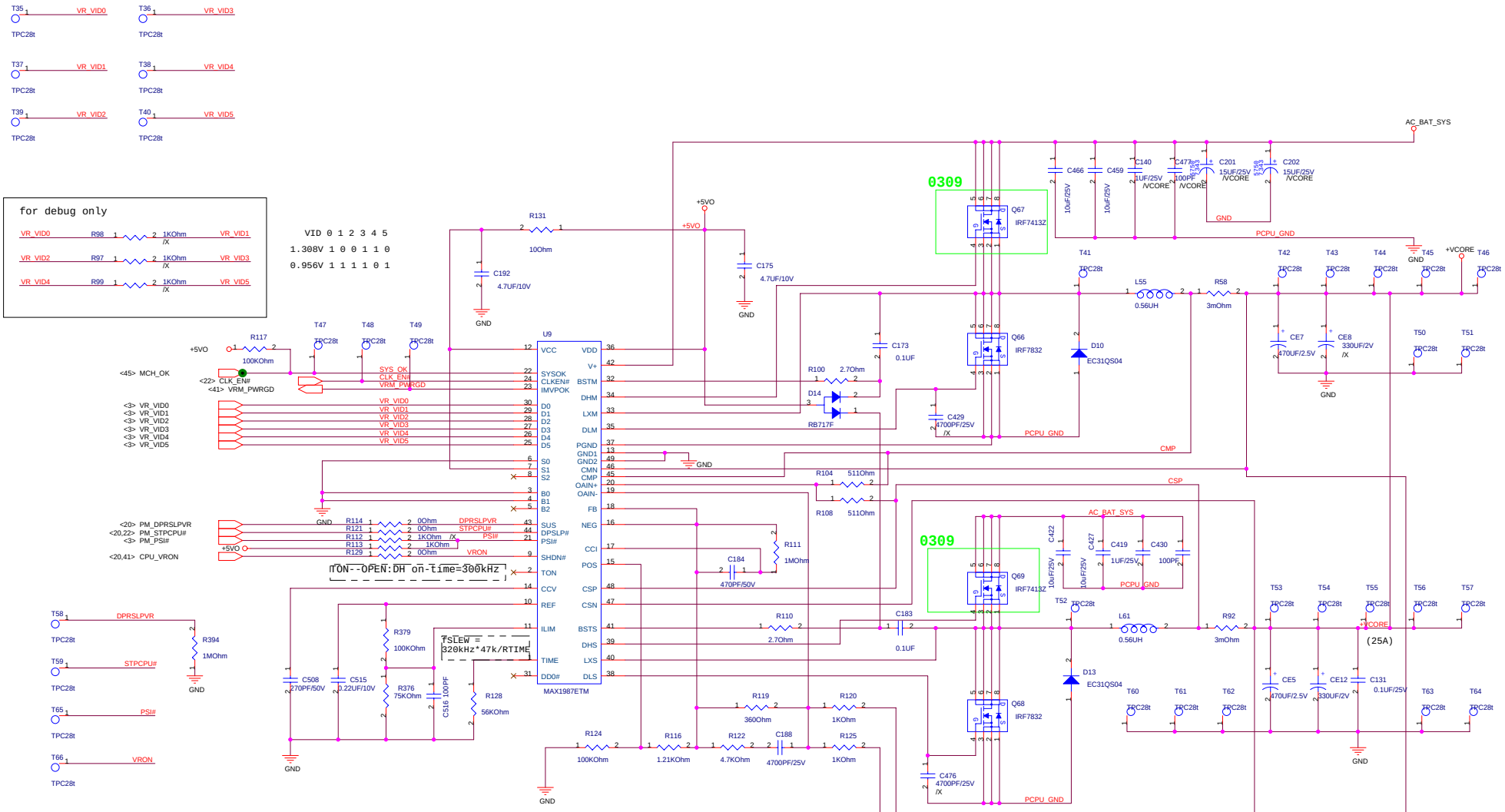
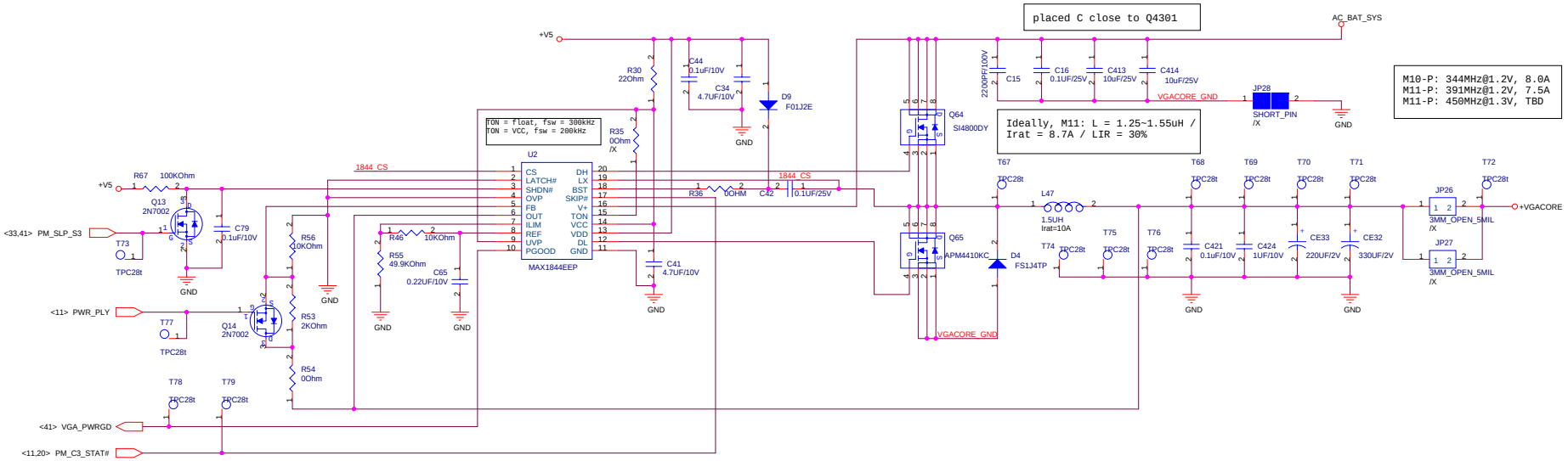

R285
10KOhm
<42> VRM_PWRGD
DLYS3_CPUON
U38
NC7SZ08P5X
R503
10KOhm
<43> VGA_PWRGD
U31
NC7SZ08P5X
CPU_VRON <20,42>
ICH4_PWROK <20,42>
C372
0.1uF/10V
U39
U32
NC7SZ14P5X
R286
10KOhm
D23
1SS355
C373
0.1uF/10V
<20> PM_VGATE
PM_VGATE
NC7SZ14P5X
[Q] Can 'PM_VGATE delay 1ms' be removed?
A: Can't remove it. boot failed if
removed. But C4101 can be removed.
ICH4-M
+V5
MAX1844
VGA_PWRGD
DLYS3_CPUON
CPU_VRON
MAX1987
VRMPWRGD
PWROK
DELAY
53 ms
SLP_S3#
SLP_S4#
LTC3728LX
CPUPWRGD
DOTHAN
SYSTEM PWR SEQUENCE
+VCCRTC->RTCRST#->+5VAO->+3.3/1.8VSUS->RSMRST#->
SLP_S4#->SLP_S3#->VCCLAN->LANPWROK->VCC->VCORE->
PWROK->VGATE->SUSSTAT#->PCIRST#
CPU:+VCORE,+VCCP,+1.8S
NB:+1.2VS,+1.5VS,+2.5V,+VCCP,+V1.8S
SB:+V1.5SUS,+V3.3SUS,+VCCP,+1.5VS,+V3.3S,+V1.8S
DDR:+2.5V,+1.25V,+1.25VS
<47,49,50> AC_APR_UC
PM_SLP_S4#
D28
RB715F
D22
1SS355
PM_PWRBTN
R13
100KOhm
C359
1UF/10V
U37
NC7SZ14P5X
FOR BAT MODE
R282
10KOhm
/X
3V_ON <44>
R292
10KOhm
Q59
2N7002
PWR_SW#
DJ_SW#
D16
DAP202K
FORCE_OFF# <44,47>
IF PWROK FIALED,SHUTDOWN +3.3VSUS.
SW6
SW_4P
C698
0.1uF/10V
/X
R274
1MOhm
Q52
2N7002
Q44
2N7002
C351
1UF/10V
PM_VGATE
R198
10KOhm
U16
PST9128NR
R197
1KOhm
PM_RSMRST# <20>
C250
1UF/10V
R187
22KOhm
Prevent RTC
drains large
current
U28F
SN74LV14
U28E
SN74LV14
C349
0.1uF/10V
R272
100KOhm
C352
1UF/10V
D31
1SS355
U28D
SN74LV14
<33,43> PM_SLP_S3
PM_SLP_S3#
PM_SLP_S3# <20,23,25,51>
<20,23,25,51> PM_SLPDLY_S3#
U28C
SN74LV14
<33> PM_SLP_S4
PM_SLP_S4#
C21
1UF/10V
/EMI
U28B
U28A
<20> PM_PWRBTN#
PM_PWRBTN
R295
100KOhm
C382
0.1uF/10V
Q62
2N7002
KBCRSM <30>
R502
100KOhm
C724
0.1uF/10V
R291
100KOhm
Q97
2N7002
PM_SLP_S4# <20,39,51>
Q63
2N7002
D32
1SS355
DJ_SW# <39,40>
R281
10KOhm
R273
100KOhm
Q96
2N7002
D51
1SS355
PWR_SW# <40>
C360
0.1uF/10V
R493
10KOhm
Q95
2N7002
LID_ICH4#_3A <19>
D52
1SS355
LID_SW# <16>
Title : PWR & RESET SEQ
ASUSTECH CO.,LTD.
Engineer: DEL_TAN
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 41 of 57


T35 VR_VID0
T36 VR_VID3
T37 VR_VID1
T38 VR_VID4
T39 VR_VID2
T40 VR_VID5
TPC28t
for debug only
VR_VID0 R98 1KOhm /X VR_VID1
VR_VID2 R97 1KOhm /X VR_VID3
VR_VID4 R99 1KOhm /X VR_VID5
VID 0 1 2 3 4 5
1.308V 1 0 0 1 1 0
0.956V 1 1 1 1 0 1
U9
MAX1987ETM
VCC VDD SYSOK CLKEN# IMVPOK D0 D1 D2 D3 D4 D5 S0 S1 S2 B0 B1 B2 SUS DPSLP# PSI# SHDN# TON CCV REF ILIM TIME DD0# V+ BSTM DHM LXM DLM PGND GND1 GND2 CMN CMP OAIN+ OAIN- FB NEG CCI POS CSP CSN BSTS DHS LXS DLS
ton--OPEN:DH on-time=300kHz
fSLEW = 320kHz*47k/RTIME
0309
Q67 IRF7413Z
Q66 IRF7832
Q69 IRF7413Z
Q68 IRF7832
D10 EC31QS04
D13 EC31QS04
D14 RB717F
AC_BAT_SYS
+5VO
+VCORE
PCPU_GND
GND
CMP
CSP
(25A)
<45> MCH_OK
<22> CLK_EN#
<41> VRM_PWRGD
<3> VR_VID0
<3> VR_VID1
<3> VR_VID2
<3> VR_VID3
<3> VR_VID4
<3> VR_VID5
<20> PM_DPRSLPVR
<20,22> PM_STPCPU#
<3> PM_PSI#
<20,41> CPU_VRON
SYS_OK
CLK_EN#
VRM_PWRGD
DPRSLPVR
STPCPU#
PSI#
VRON
R131 10Ohm
R117 100KOhm
R114 0Ohm
R121 0Ohm
R112 1KOhm /X
R113 1KOhm
R129 0Ohm
R100 2.7Ohm
R104 511Ohm
R108 511Ohm
R111 1MOhm
R110 2.7Ohm
R379 100KOhm
R376 75KOhm
R128 56KOhm
R124 100KOhm
R116 1.21KOhm
R119 360Ohm
R120 1KOhm
R122 4.7KOhm
R125 1KOhm
R394 1MOhm
R58 3mOhm
R92 3mOhm
L55 0.56UH
L61 0.56UH
C192 4.7UF/10V
C175 4.7UF/10V
C173 0.1UF
C183 0.1UF
C429 4700PF/25V /X
C476 4700PF/25V /X
C184 470PF/50V
C188 4700PF/25V
C508 270PF/50V
C515 0.22UF/10V
C516 100PF
C466 10uF/25V
C459 10uF/25V
C140 1UF/25V /VCORE
C477 100PF /VCORE
C201 15UF/25V /VCORE
C202 15UF/25V /VCORE
C422 10uF/25V
C427 10uF/25V
C419 1UF/25V
C430 100PF
CE7 470UF/2.5V
CE8 330UF/2V /X
CE5 470UF/2.5V
CE12 330UF/2V
C131 0.1UF/25V
T41 T42 T43 T44 T45 T46 T47 T48 T49 T50 T51 T52 T53 T54 T55 T56 T57 T58 T59 T60 T61 T62 T63 T64 T65 T66
TPC28t
Title : Vcore
ASUSTECH CO.,LTD.
Engineer: EDDY ZHAO
Size C
Project Name A3G
Rev 2.0
Date: Wednesday, October 13, 2004
Sheet 42 of 57



M9+X:	M10/M11:
R4306 = 8KOhm, 10-003418026-21 R4308 = R4309 = 2KOhm, 10-004412020 PWR_PLY=H, VGACORE=1.25V PWR_PLY=L, VGACORE=1.5V	R4306 = 10KOhm, 10-004401030 R4308 = 2KOhm, 10-004412020 R4309 = 0Ohm, 10-004400000 PWR_PLY = H, VGACORE=1.0V PWR_PLY = L, VGACORE=1.2V

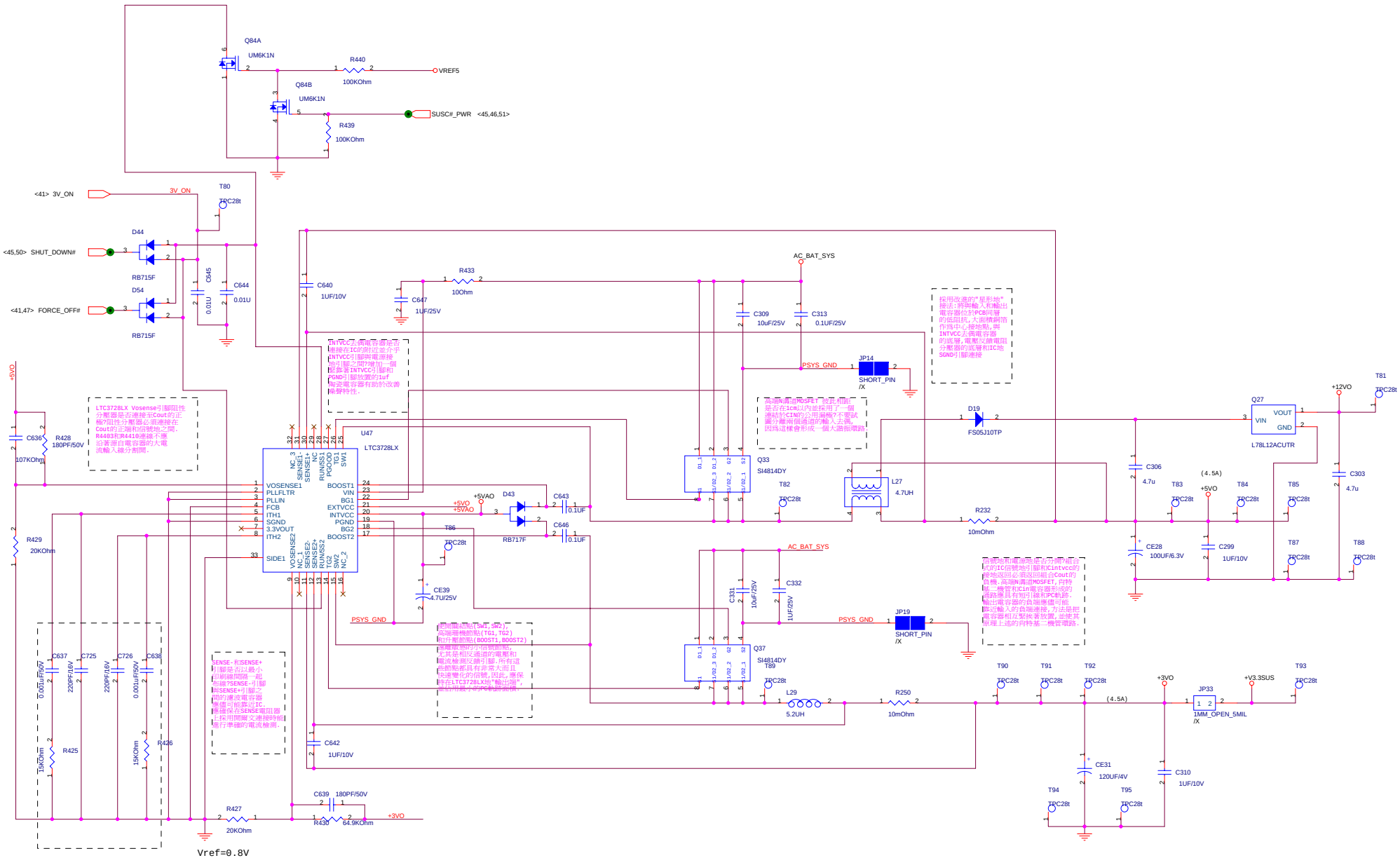
ASUSTECH CO.,LTD.

Title : VGACORE

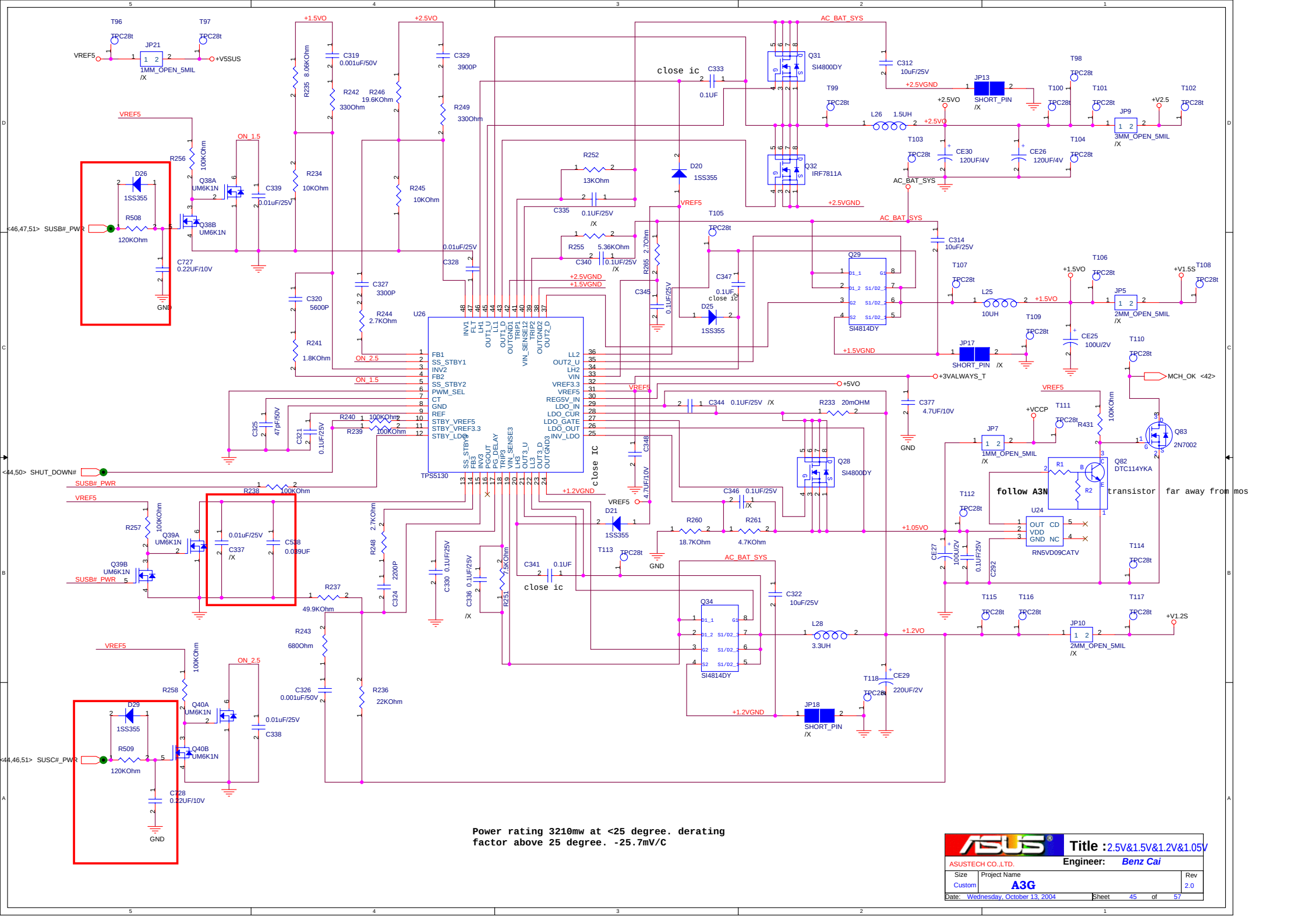
Engineer: Pommy Lu

Size	Project Name	Rev
C	A3G	2.0

Date: Wednesday, October 13, 2004 Sheet 43 of 57

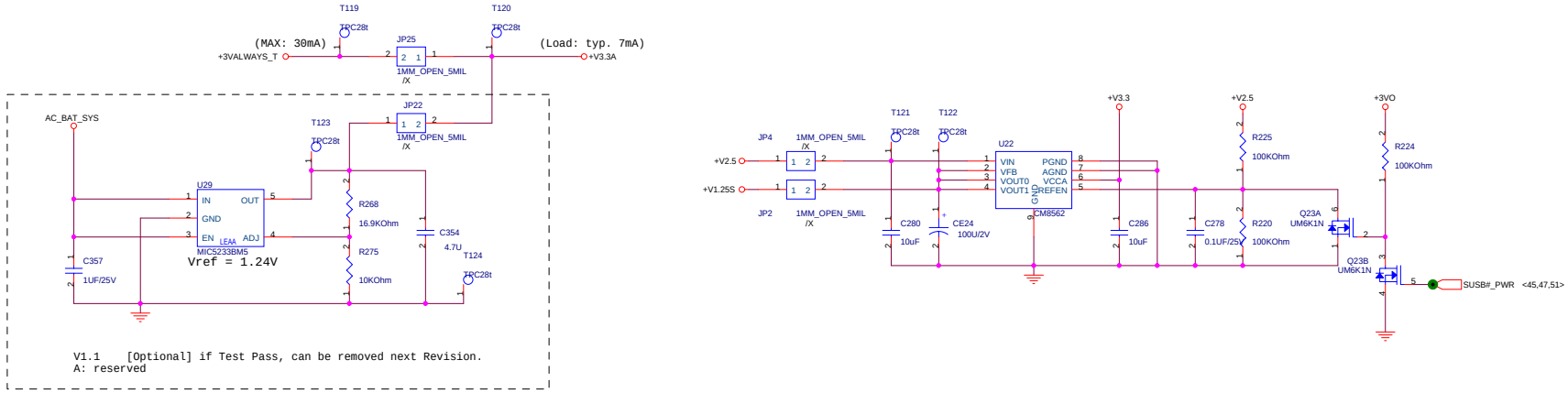


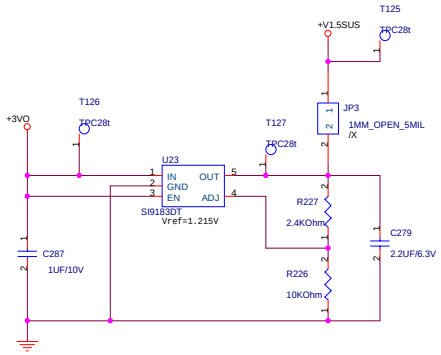
ASUSTEK CO.,LTD.	Title : SYSTEM		
	Engineer: NANNY ZHANG		
Size: C	Project Name: A3G		Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 44 of 57		

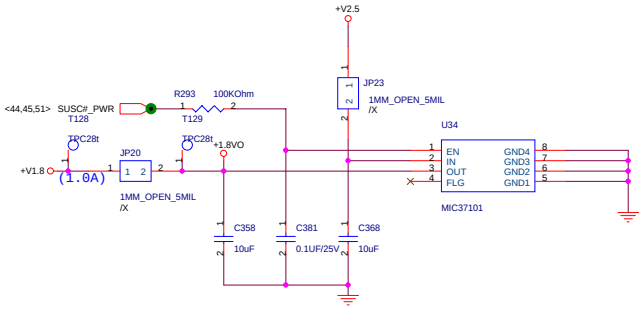


Power rating 3210mw at <25 degree. derating factor above 25 degree. -25.7mV/C

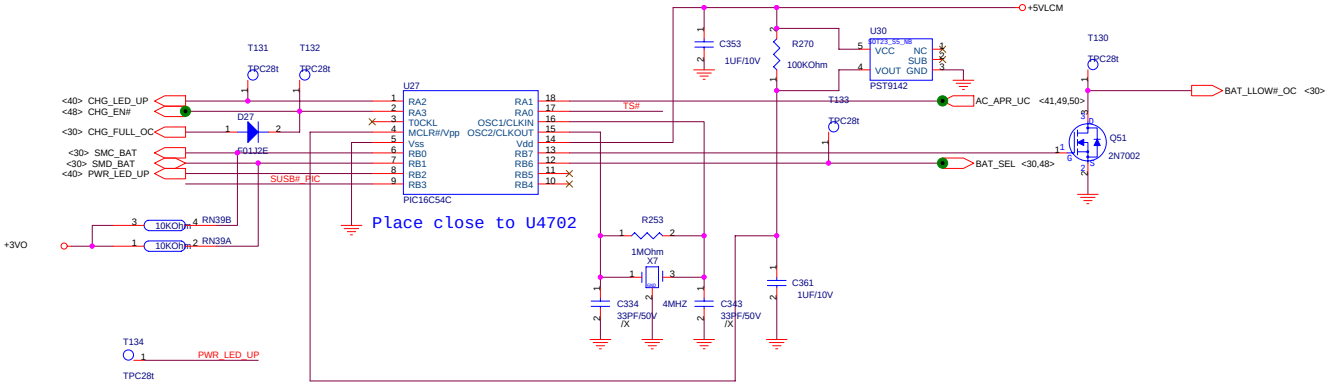
ASUSTECH CO.,LTD.	Title : 2.5V&1.5V&1.2V&1.05V	
	Engineer: Benz Cai	
Size: Custom	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 45 of 57	

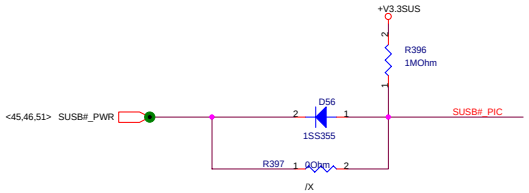


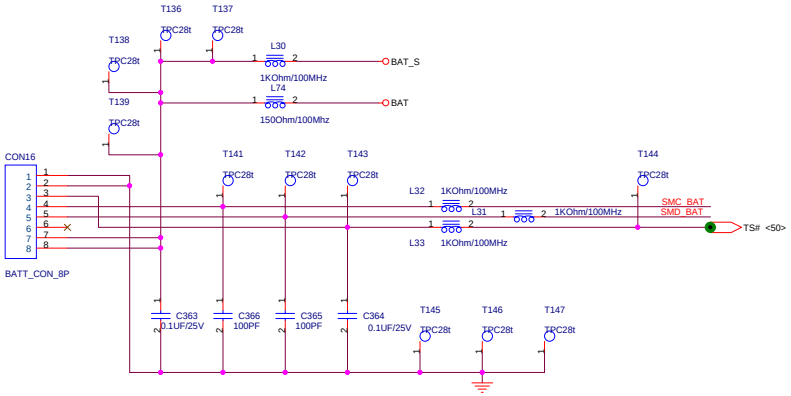


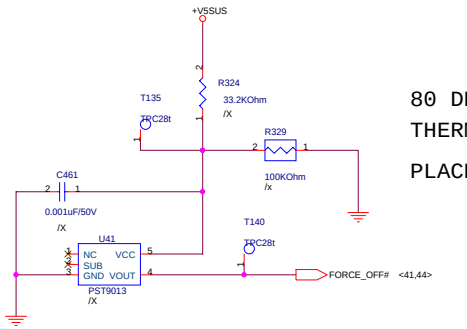


ASUSTECH CO.,LTD.	Title : 1.25V&1.8V	
	Engineer: Sleck Song	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 46 of 57	





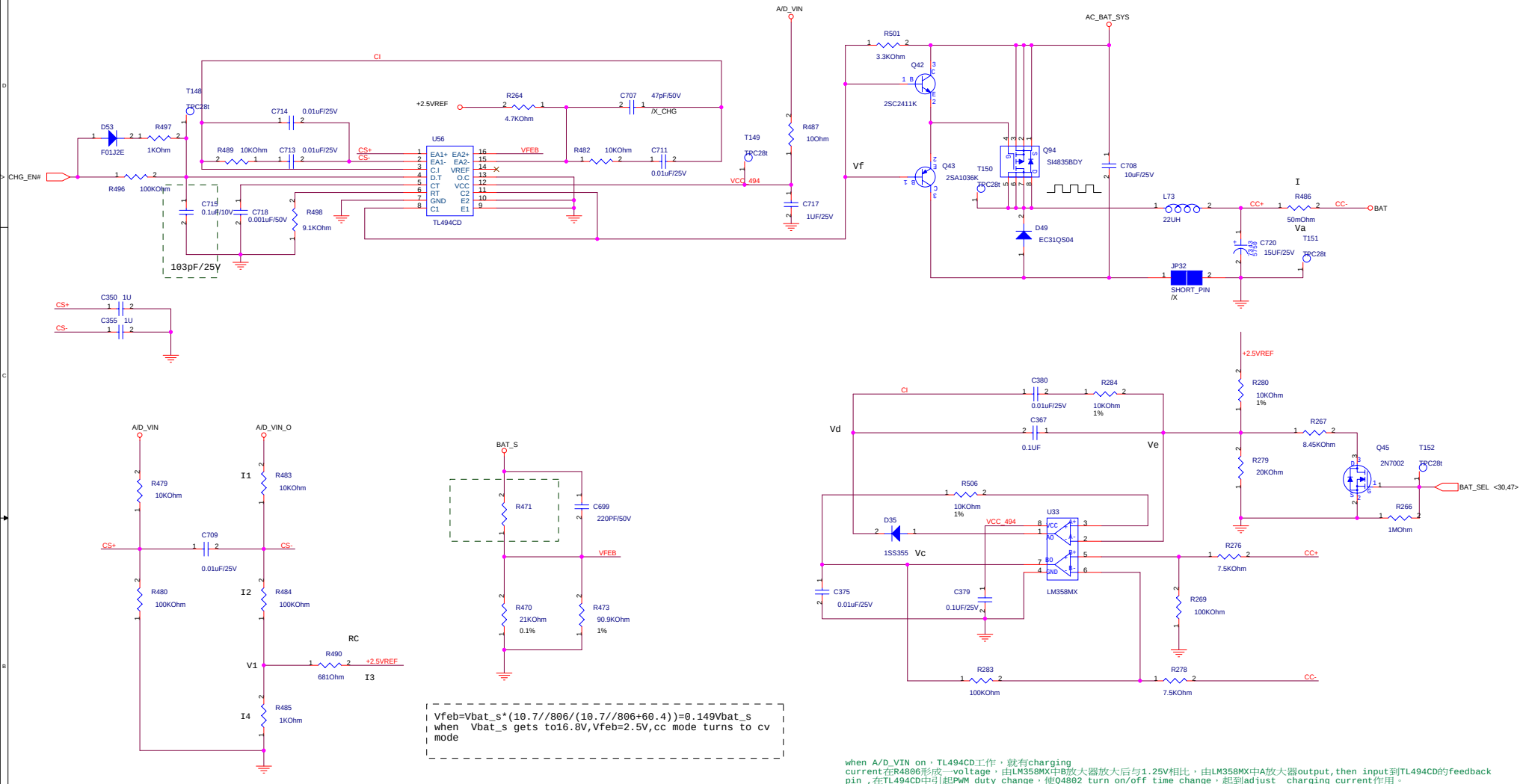




80 DEGREE C
THERMAL PROTECTION

PLACE UNDER CPU

ASUSTECH CO.,LTD.	Title : PIC16C54C	
	Engineer: DEL_TAN	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 47 of 57	




```
Vfeb=Vbat_s*(10.7//806/(10.7//806+60.4))=0.149Vbat_s
when  Vbat_s gets to16.8V,Vfeb=2.5V,cc mode turns to cv
mode
```

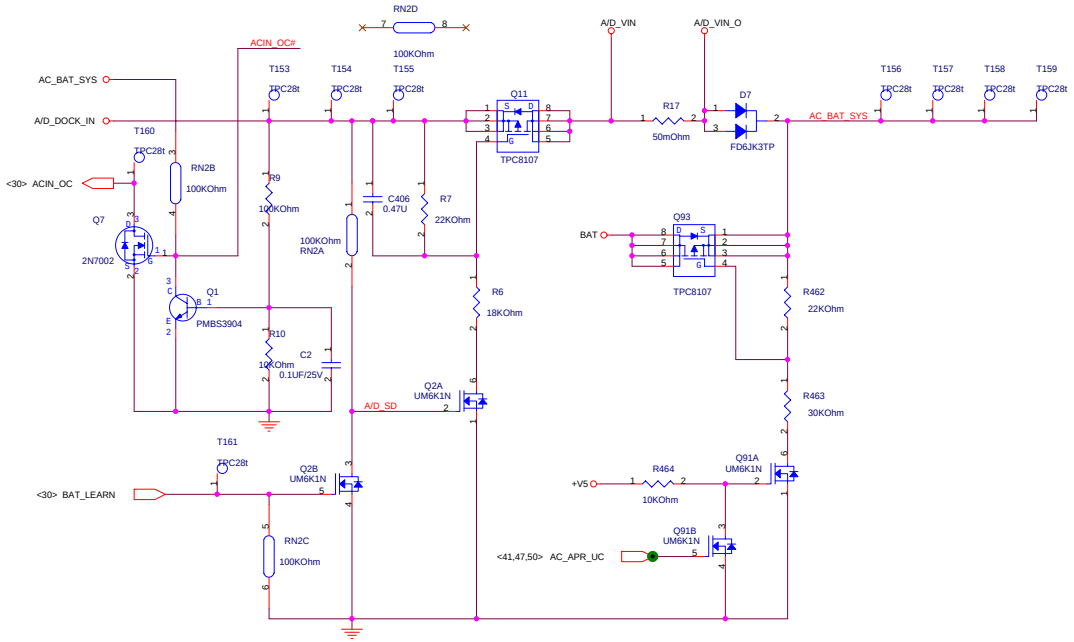
when A/D_VIN on，TL494CD工作，就有charging
current在R4806形成一voltage，由LM358MX中B放大器放大后与1.25V相比，由LM358MX中A放大器output,then input到TL494CD的feedback
pin ,在TL494CD中引起PWM duty change，使Q4802 turn on/off time change，起到adjust charging current作用。
例：I增大,致Va增大,致Vc增大,致Vc>Ve(=1.25V) ,致Vd增大,致PWM   duty增大,致 Vf降低,致Q4802 turn on time降低,致I降低
由上起到cc模式控制。when平衡,Vc=1.25V,可算出I。I*20mOHM*24.9/25.9*(1+24.9/1)=1.25,so I=2.51A

current sharing=3.1A

```
A/D_VIN=19V      A/D_VIN_O=19V-3.1A*50mohm=18.845V
CS+=CS-=19V*100/(10+100)=17.272727V
I1=(18.845V-17.272727V)/10K=0.15723mA
V1=17.272727V-0.15723mA*100K=1.5497V
I4=1.5497V/1K=1.5497mA
I3=I4-I1=1.39247mA
RC=(2.5V-1.5497V)/1.39247mA=681 Ohm
```

Q1:How to get 3.1A?
Q2:CS+=CS-,Why or the purpose? and with EA1?

ASUSTEK CO.,LTD.	Title : CHARGER	
	Engineer: Jully_ma	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 48 of 57	



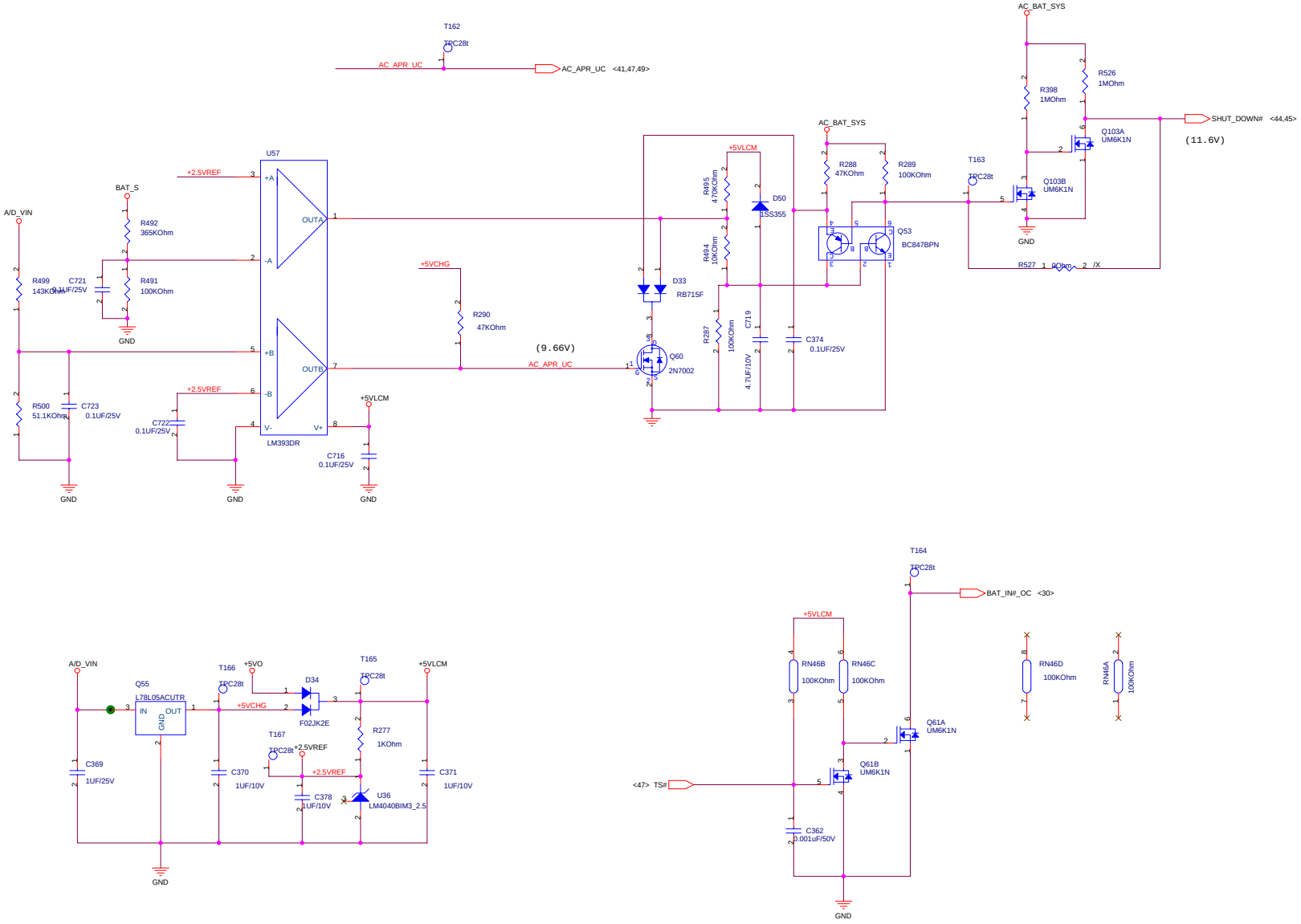
ASUSTECH CO.,LTD.

Title : AC_BAT_SYS

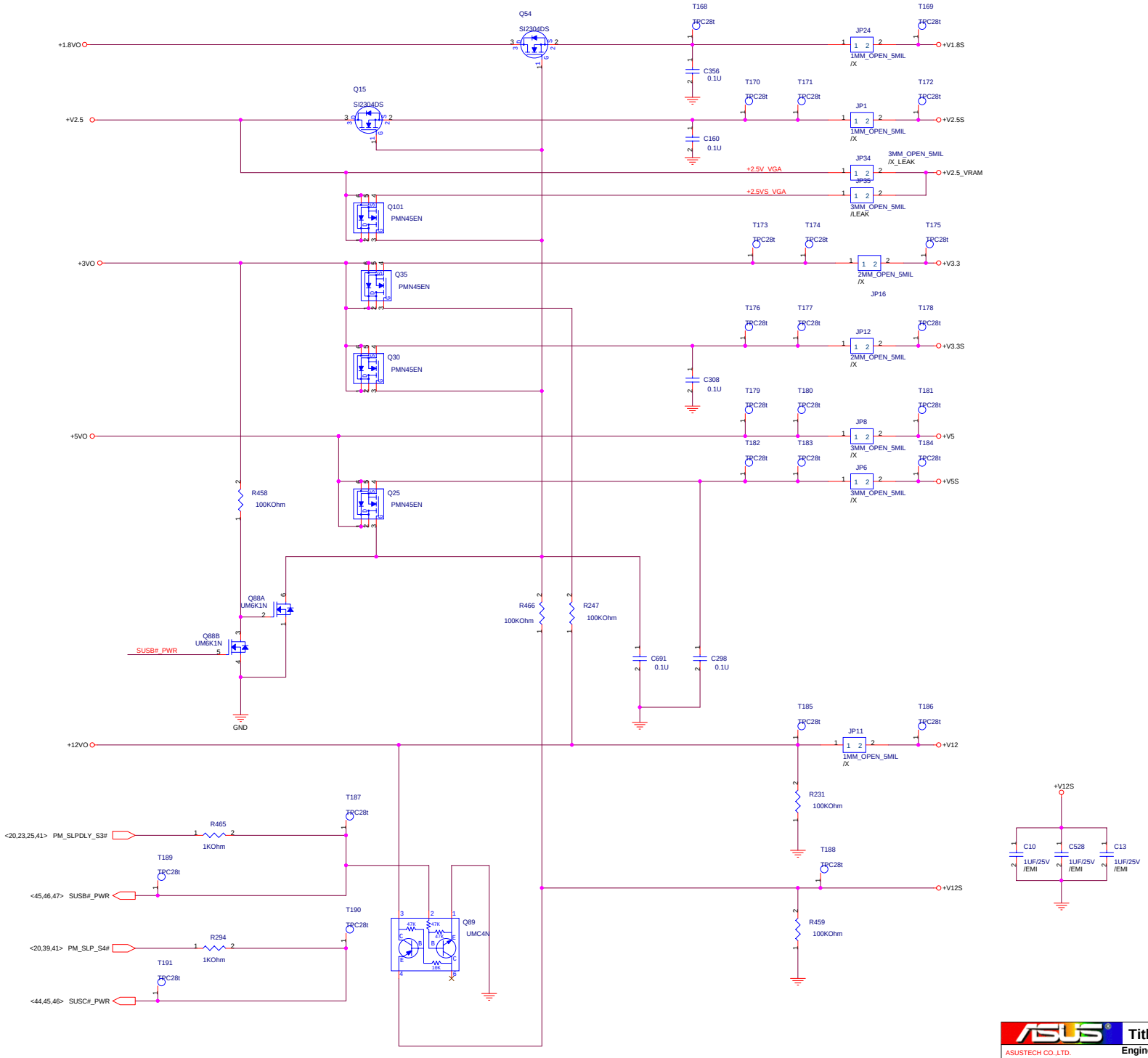
Engineer: *charlie_xie*

Size	Project Name	Rev
C	A3G	2.0

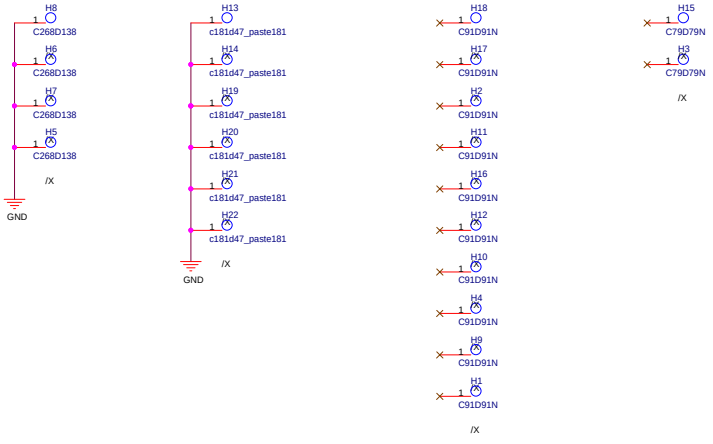
Date: Wednesday, October 13, 2004 Sheet 49 of 57



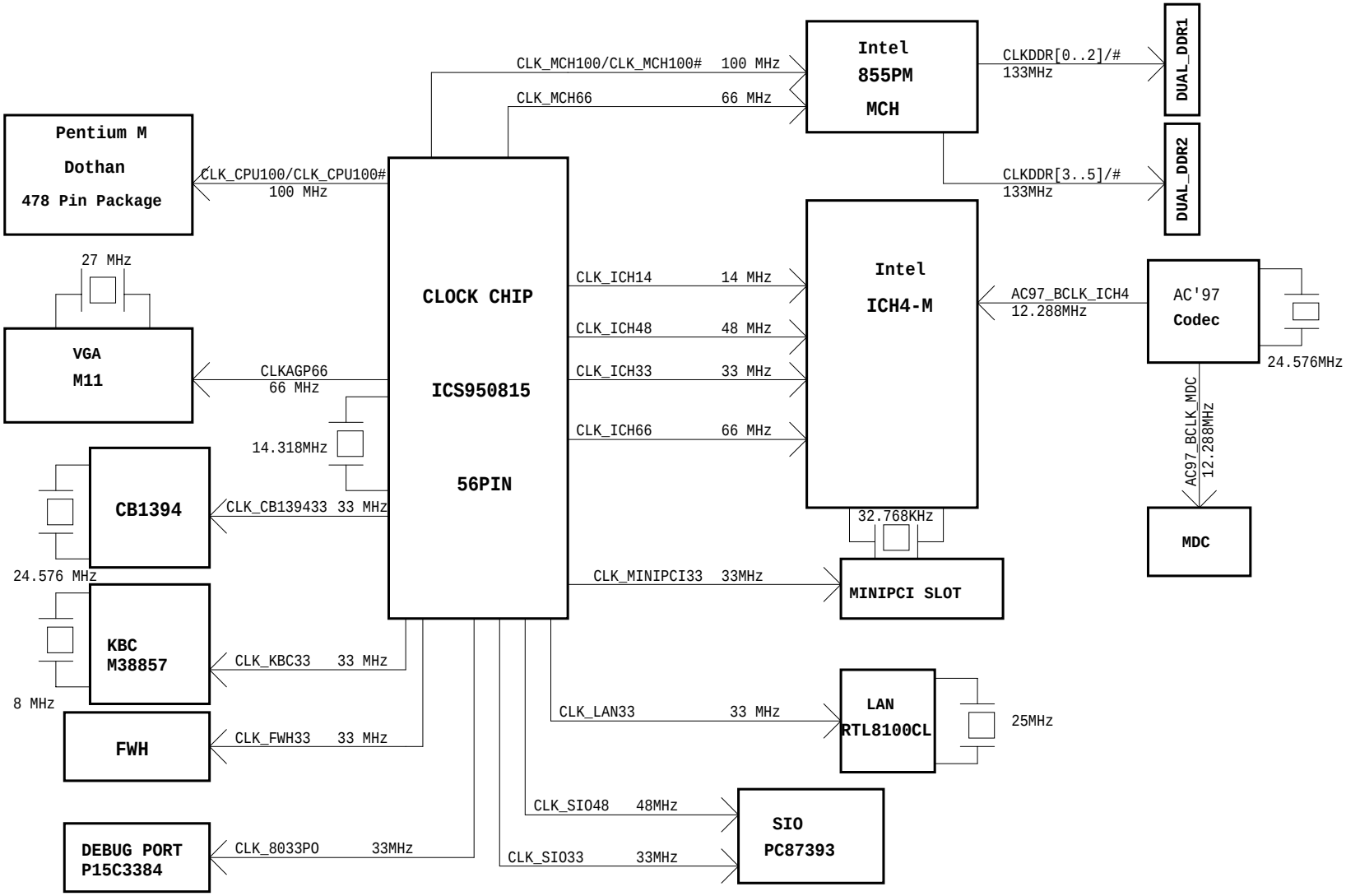
ASUSTECH CO.,LTD.	Title : BATLOW/SD#	
	Engineer: Lassie Bao	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 50 of 57	



ASUSTEK CO.,LTD.	Title : LOAD SWITCH	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 51 of 57	

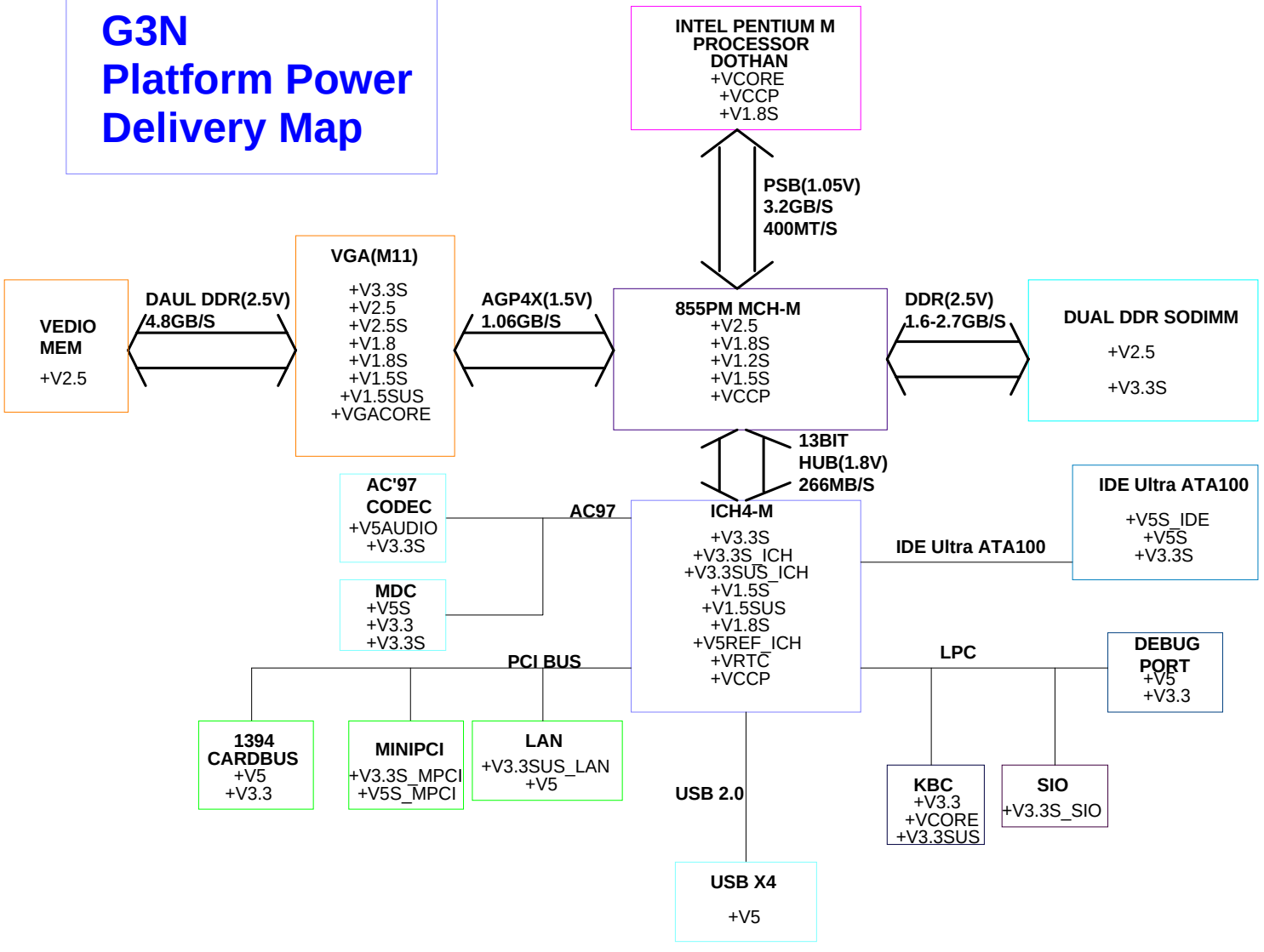


ASUSTECH CO.,LTD.	Title : SCREW_HOLES	
	Engineer: Pommy Lu	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 52 of 57	



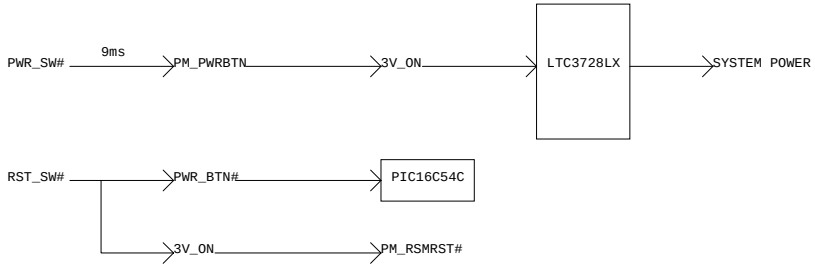
ASUSTECH CO.,LTD.	Title : Clock Map	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 53 of 57	

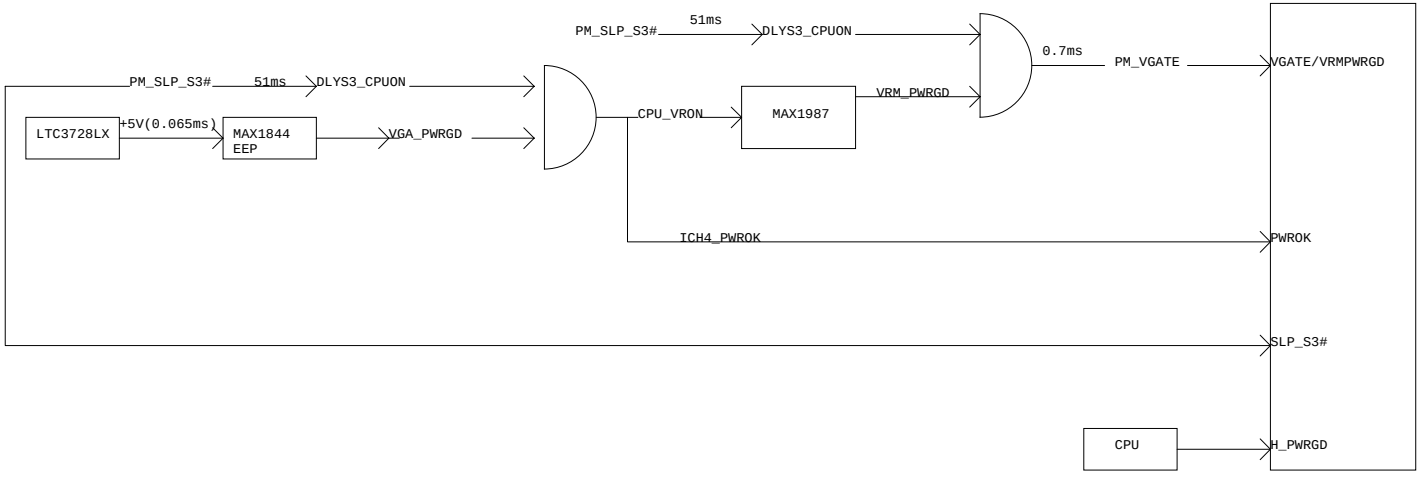
G3N Platform Power Delivery Map



ASUSTECH CO.,LTD.	Title : Power Delivery Map	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 54 of 57	

AC Mode:





ASUSTECH CO.,LTD.

Title : Power Sequence(1)

Engineer: Lassie_Bao

Size	Project Name	Rev
C	A3G	2.0

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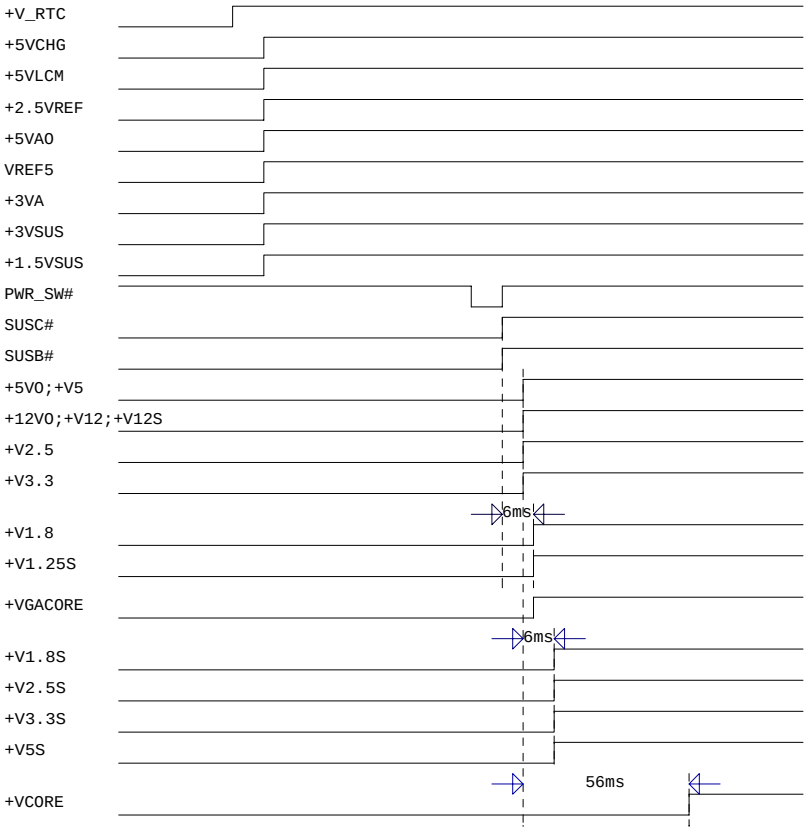
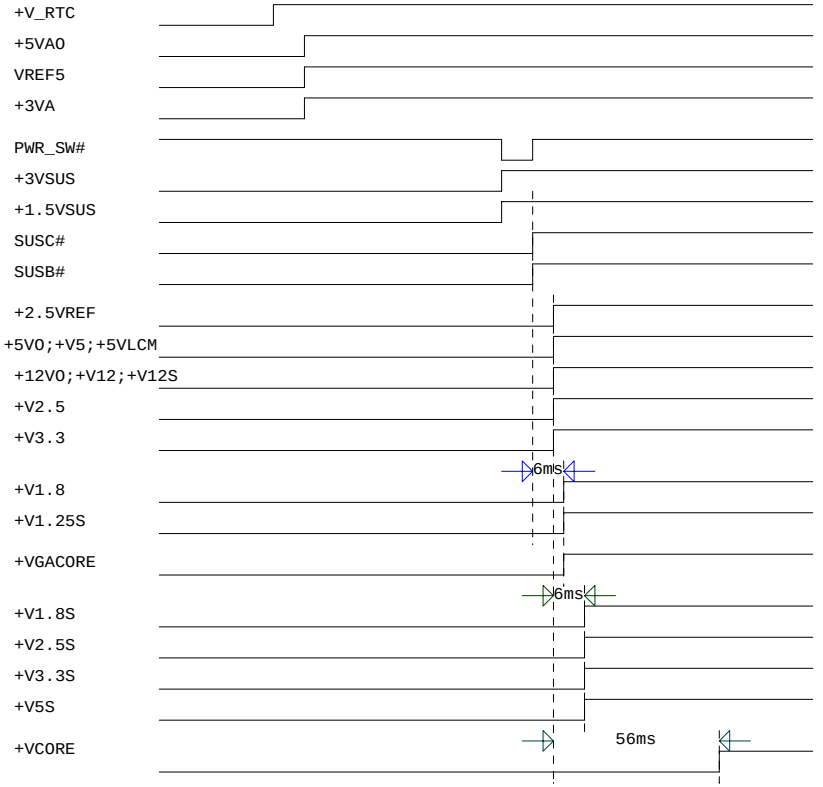
AC MODE



BAT MODE



ASUSTECH	Title : Power Sequence(2)	
	Engineer: DEL_TAN	
Size: C	Project Name: A3G	Rev: 2.0
Date: Wednesday, October 13, 2004	Sheet 56 of 57	

REVISION HISTORY

SCHEME REV.	DATE	REVISION DESCRIPTION
0.1	2004/02/04	Preliminary based on A3N/M3N Add M11-P
0.2	2004/02/06	Fix DRC errors P51: Remove +1.5VO to +V1.5S switch P46: one of +V3.3A source is Optional, need be Identifed Add Power Jumpers
0.3	2004/02/10	Add 54_Clock Map and 55_Platform Power Delivery Map (Created by Eddy) Fix Power Sequence error Change some Circuit to optional Update parts status and part type
0.4	2004/03/18	Add audio codec to 6 channel output Add VGA compatible with M9+X Add comment on Comp. placement Remove TV-OUT function Merge USB CON of WLAN and Camera with Planel Power CON Remove series termination resistors of DQ and MA between VRAM and GPU Change part package Add WLAN RF en/disable Add Battery Selection Modify Audio Amplifier Circuit Modify Audio DJ & Function Key Add System Power Sequence Add Screw Holes
1.0	2004/04/12	Add two local Hublink Ref. Voltage cirtcuit Rename the parts reference Release for Sample Run

ASUSTECH CO.,LTD.

Title : Revision History

Engineer: Pommy Lu

Size	Project Name	Rev
C	A3G	2.0

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