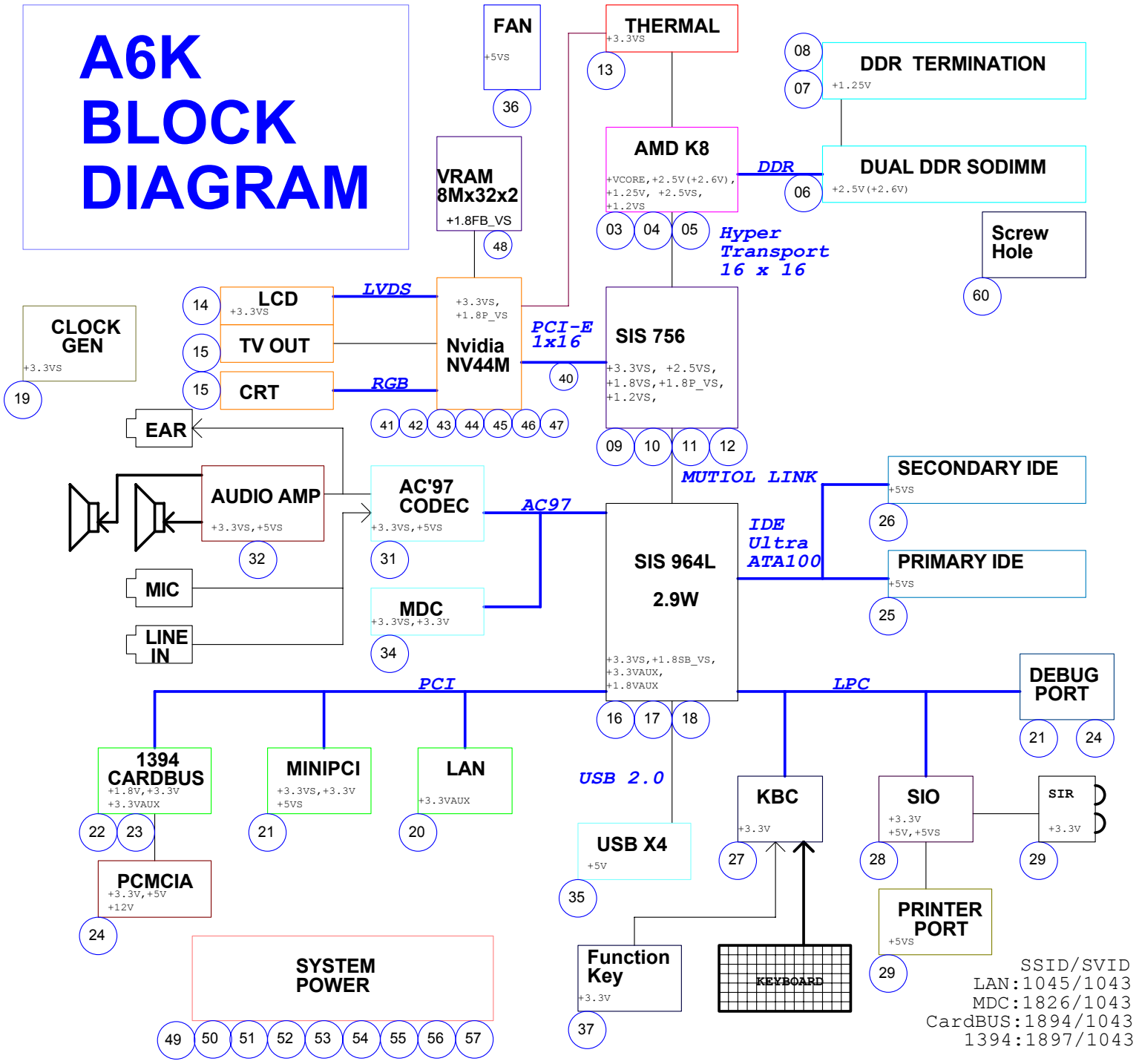
A6K BLOCK DIAGRAM



SSID/SVID
LAN:1045/1043
MDC:1826/1043
CardBUS:1894/1043
1394:1897/1043

FILE LIST 01

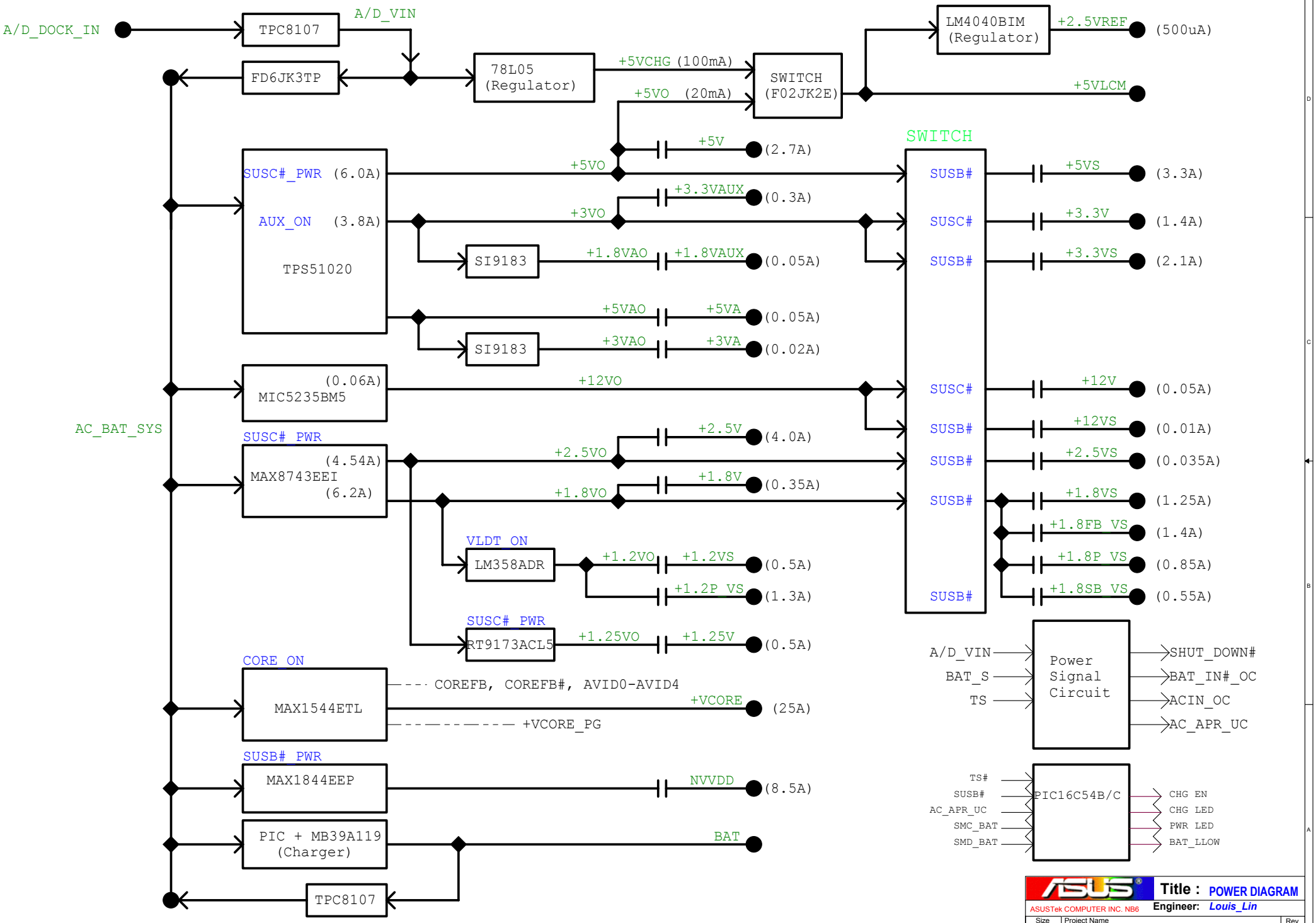
ASUSTek COMPUTER INC. NB6

Title : BLOCK DIAGRAM

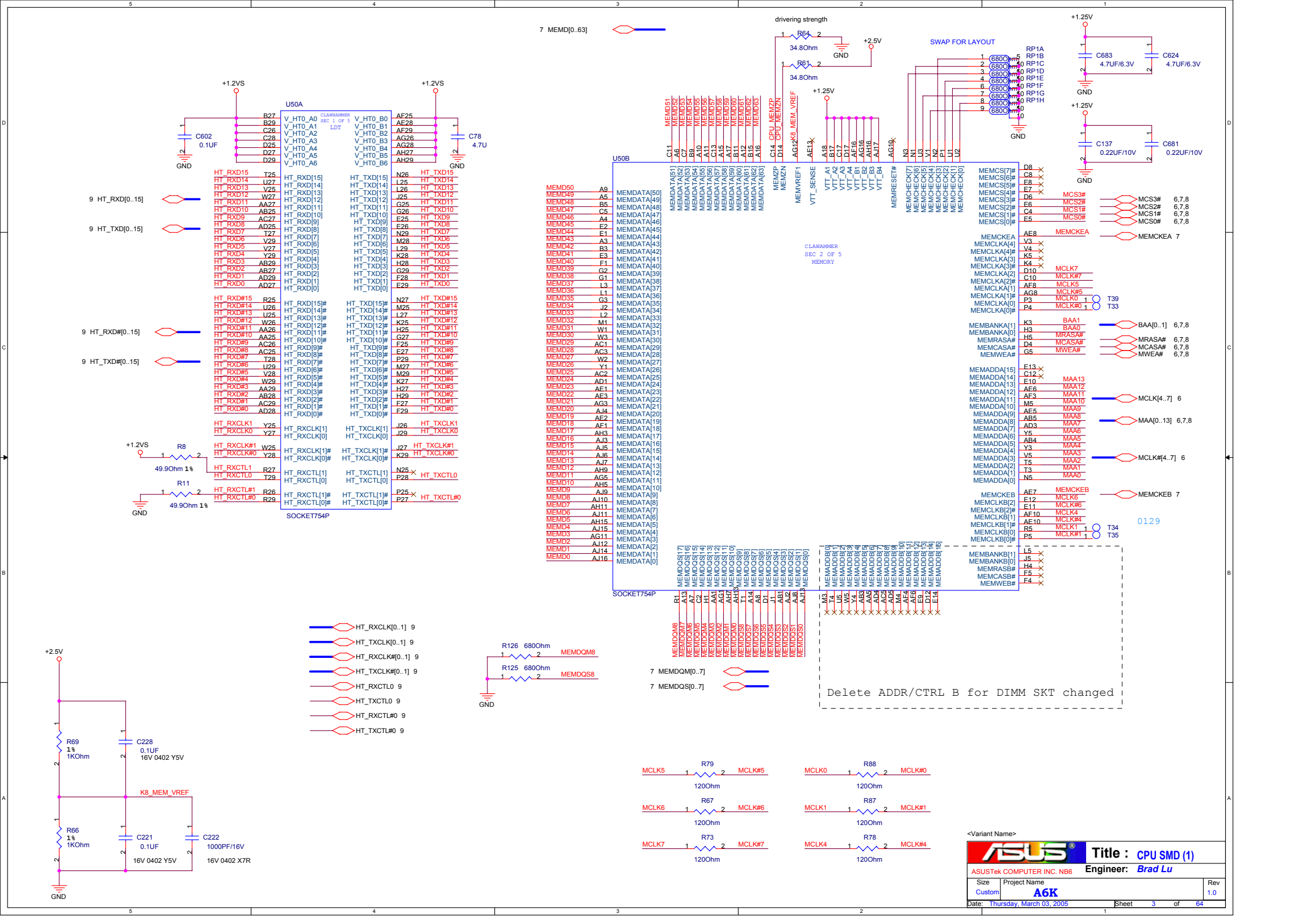
Engineer: Brad Lu

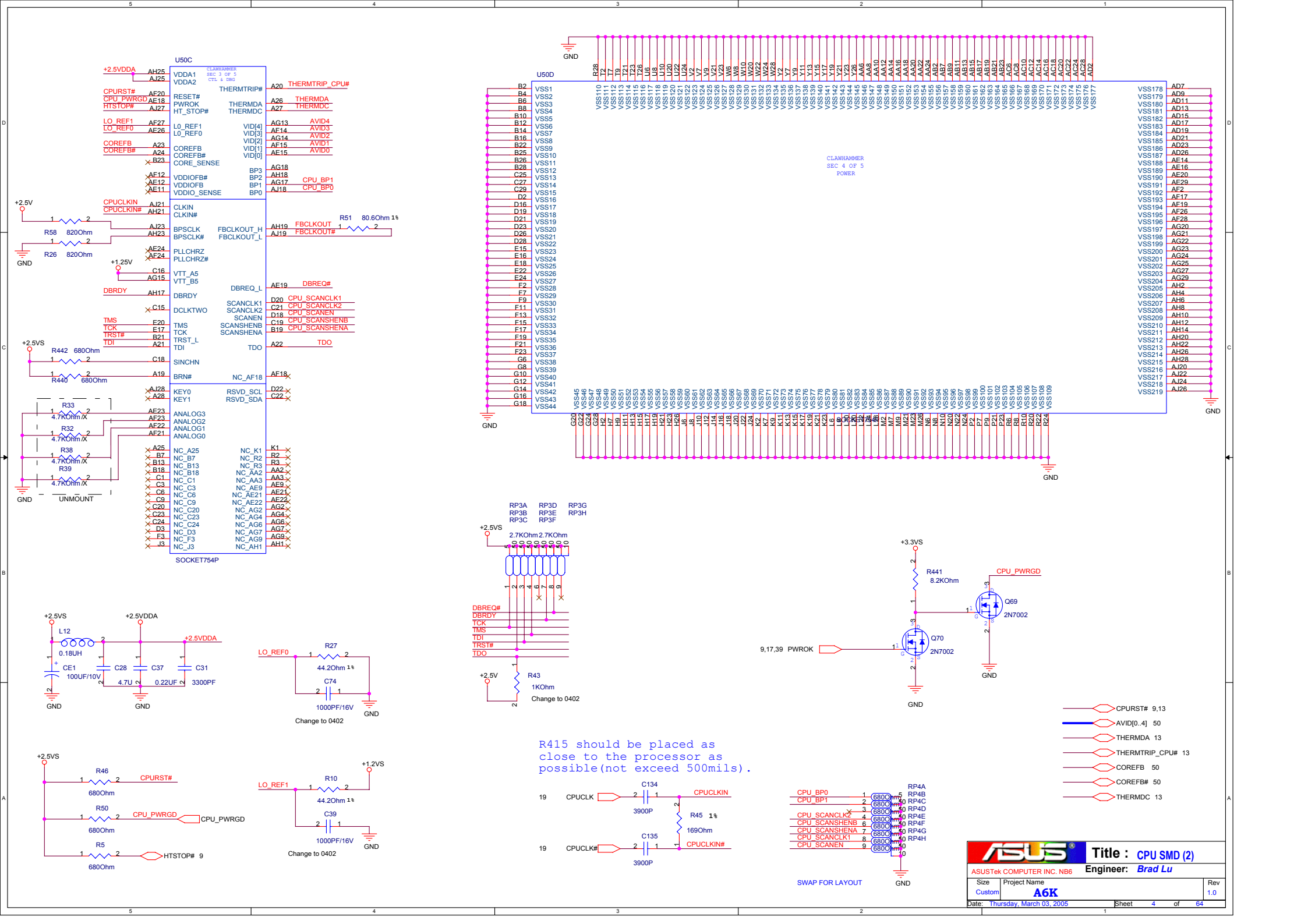
Size	Project Name	Rev
Custom	A6K	1.0

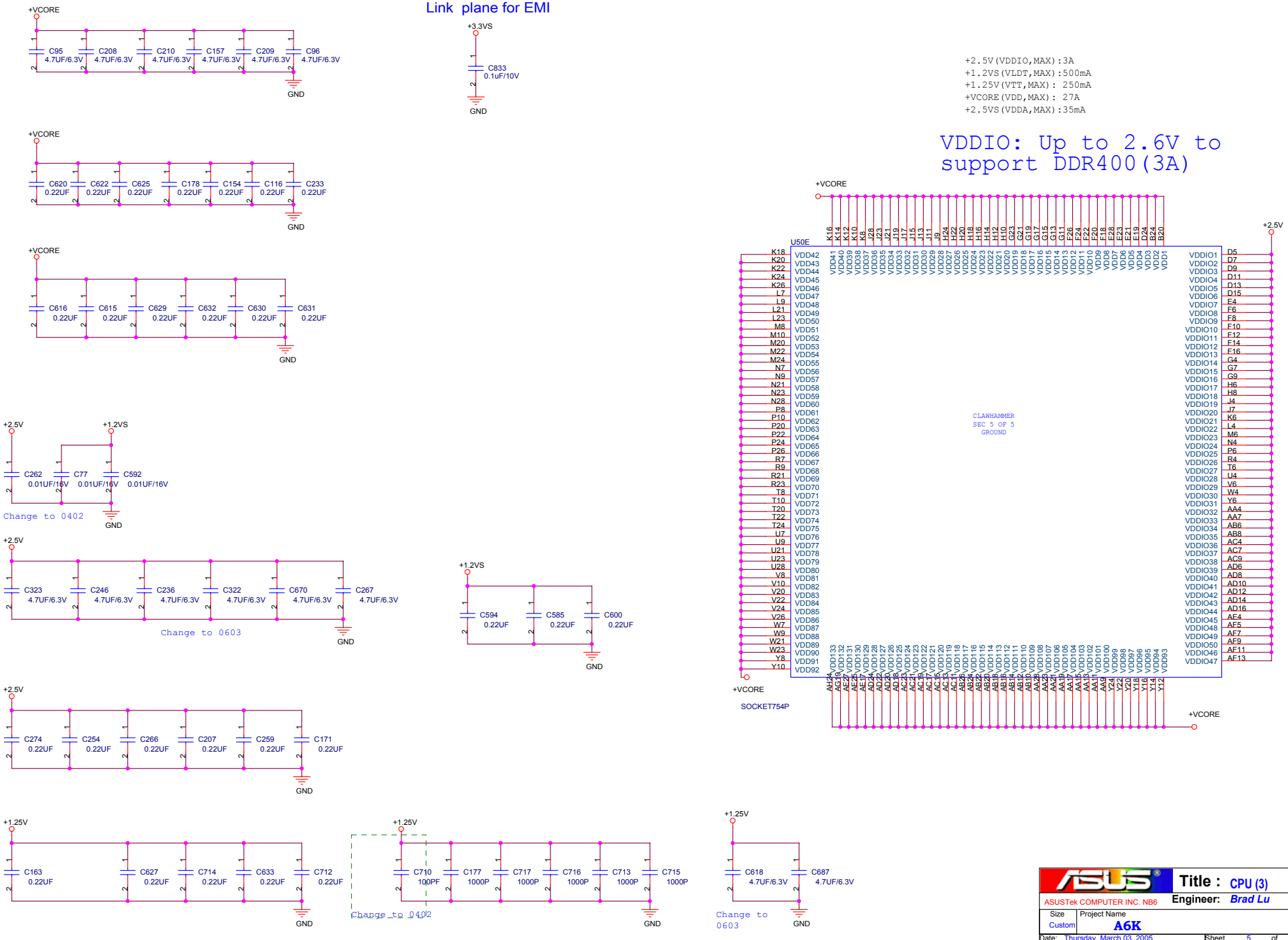
Date: Thursday, March 03, 2005 Sheet 1 of 64



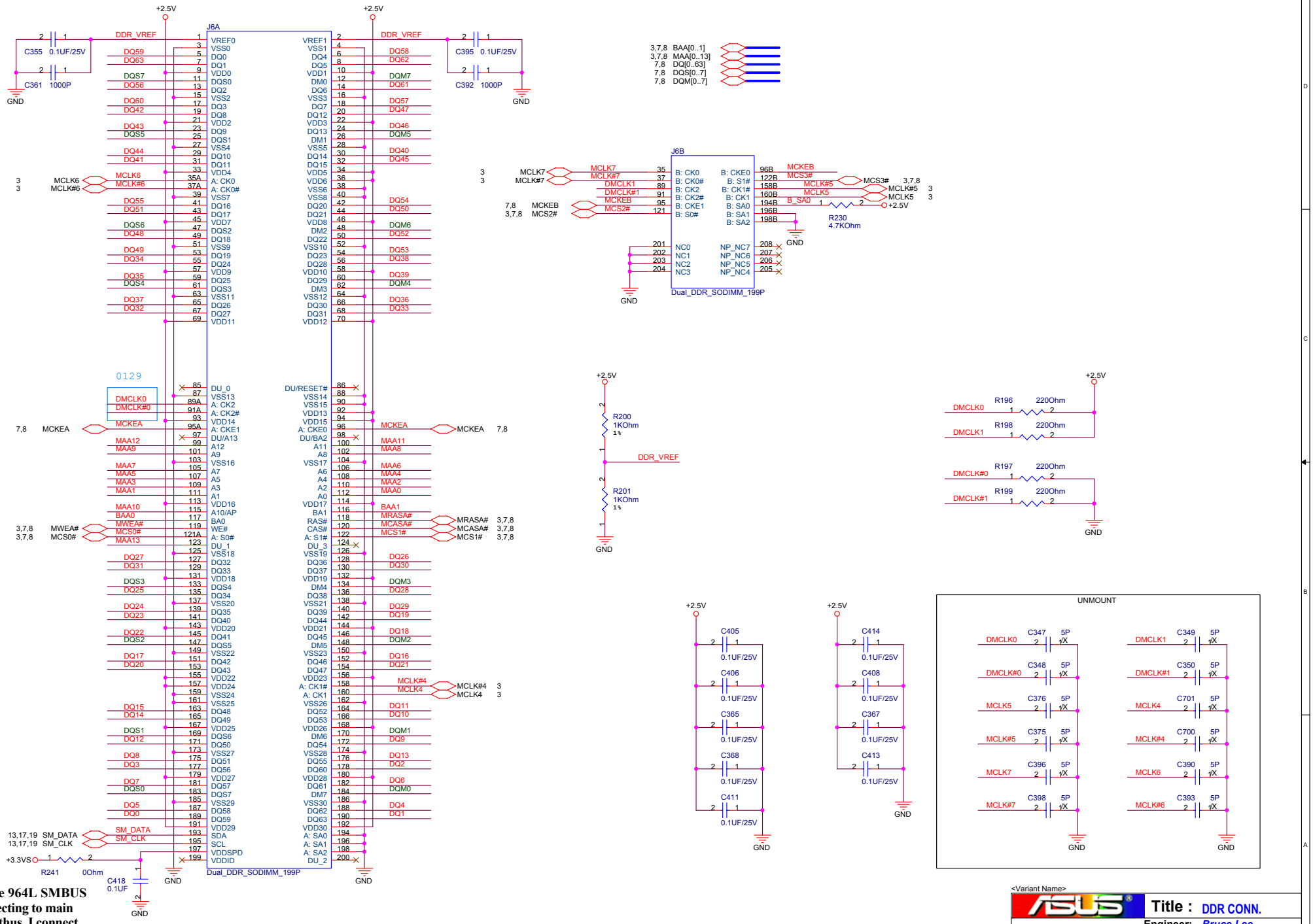
Title : POWER DIAGRAM		
ASUSTek COMPUTER INC. NB6	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 2 of 64	


U50A
SOCKET754P
U50B
SOCKET754P
CLAWHAMMER SEC 1 OF 5 LDT
CLAWHAMMER SEC 2 OF 5 MEMORY
drivering strength
SWAP FOR LAYOUT
Delete ADDR/CTRL B for DIMM SKT changed
0129
+1.2VS
+2.5V
+1.25V
GND
C602 0.1UF
C78 4.7U
R8 49.9Ohm 1%
R11 49.9Ohm 1%
R64 34.8Ohm
R61 34.8Ohm
C683 4.7UF/6.3V
C624 4.7UF/6.3V
C137 0.22UF/10V
C681 0.22UF/10V
R69 1% 1KOhm
R66 1% 1KOhm
C228 0.1UF 16V 0402 Y5V
C221 0.1UF 16V 0402 Y5V
C222 1000PF/16V 16V 0402 X7R
K8_MEM_VREF
R126 680Ohm
R125 680Ohm
MEMDQM8
MEMDQS8
R79 120Ohm
R67 120Ohm
R73 120Ohm
R88 120Ohm
R87 120Ohm
R78 120Ohm
MCLK5
MCLK#5
MCLK6
MCLK#6
MCLK7
MCLK#7
MCLK0
MCLK#0
MCLK1
MCLK#1
MCLK4
MCLK#4
9 HT_RXD[0..15]
9 HT_TXD[0..15]
9 HT_RXD#[0..15]
9 HT_TXD#[0..15]
7 MEMD[0..63]
7 MEMDQM[0..7]
7 MEMDQS[0..7]
HT_RXCLK[0..1] 9
HT_TXCLK[0..1] 9
HT_RXCLK#[0..1] 9
HT_TXCLK#[0..1] 9
HT_RXCTL0 9
HT_TXCTL0 9
HT_RXCTL#0 9
HT_TXCTL#0 9
MCS3# 6,7,8
MCS2# 6,7,8
MCS1# 6,7,8
MCS0# 6,7,8
MEMCKEA 7
BAA[0..1] 6,7,8
MRASA# 6,7,8
MCASA# 6,7,8
MWEA# 6,7,8
MCLK[4..7] 6
MAA[0..13] 6,7,8
MCLK#[4..7] 6
MEMCKEB 7
T39
T33
T34
T35
RP1A RP1B RP1C RP1D RP1E RP1F RP1G RP1H
680Ohm
Title : CPU SMD (1)
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 3 of 64
<Variant Name>


U50C
CLAWHAMMER
SEC 3 OF 5
CTL & DBG
VDDA1
VDDA2
THERMTRIP#
RESET#
PWROK
HT_STOP#
THERMDA
THERMDC
L0_REF1
L0_REF0
VID[4]
VID[3]
VID[2]
VID[1]
VID[0]
COREFB
COREFB#
CORE_SENSE
BP3
BP2
BP1
BP0
VDDIOFB#
VDDIOFB
VDDIO_SENSE
CLKIN
CLKIN#
BPSCLK
BPSCLK#
FBCLKOUT_H
FBCLKOUT_L
PLLCHRZ
PLLCHRZ#
VTT_A5
VTT_B5
DBREQ_L
DBRDY
SCANCLK1
SCANCLK2
DCLKTWO
SCANEN
TMS
TCK
TRST_L
TDI
SCANSHENB
SCANSHENA
TDO
SINCHN
BRN#
NC_AF18
KEY0
KEY1
RSVD_SCL
RSVD_SDA
ANALOG3
ANALOG2
ANALOG1
ANALOG0
NC_A25
NC_B7
NC_B13
NC_B18
NC_C1
NC_C3
NC_C6
NC_C9
NC_C20
NC_C23
NC_C24
NC_D3
NC_F3
NC_J3
NC_K1
NC_R2
NC_R3
NC_AA2
NC_AA3
NC_AE9
NC_AE21
NC_AE22
NC_AG2
NC_AG4
NC_AG6
NC_AG7
NC_AG9
NC_AH1
SOCKET754P
+2.5VDDA
CPURST#
CPU_PWRGD
HTSTOP#
LO_REF1
LO_REF0
COREFB
COREFB#
CPUCLKIN
CPUCLKIN#
DBRDY
TMS
TCK
TRST#
TDI
+2.5VS
+1.25V
GND
R58 820Ohm
R26 820Ohm
R51 80.6Ohm 1%
FBCLKOUT
FBCLKOUT#
DBREQ#
CPU_SCANCLK1
CPU_SCANCLK2
CPU_SCANEN
CPU_SCANSHENB
CPU_SCANSHENA
TDO
R442 680Ohm
R440 680Ohm
C18
C16
C15
R33 4.7KOhm /X
R32 4.7KOhm /X
R38 4.7KOhm /X
R39 4.7KOhm /X
UNMOUNT
U50D
CLAWHAMMER
SEC 4 OF 5
POWER
L12
0.18UH
CE1 100UF/10V
C28 4.7U
C37 0.22UF
C31 3300PF
+2.5VDDA
R27 44.2Ohm 1%
C74 1000PF/16V
LO_REF0
Change to 0402
RP3A RP3B RP3C
RP3D RP3E RP3F
RP3G RP3H
2.7KOhm 2.7KOhm
DBREQ#
DBRDY
TCK
TMS
TDI
TRST#
TDO
R43 1KOhm
Change to 0402
+3.3VS
R441 8.2KOhm
CPU_PWRGD
Q69 2N7002
Q70 2N7002
9,17,39 PWROK
R46 680Ohm
R50 680Ohm
R5 680Ohm
CPURST#
CPU_PWRGD
HTSTOP# 9
+1.2VS
R10 44.2Ohm 1%
C39 1000PF/16V
LO_REF1
R415 should be placed as close to the processor as possible(not exceed 500mils).
C134 3900P
C135 3900P
R45 1% 169Ohm
19 CPUCLK
19 CPUCLK#
CPUCLKIN
CPUCLKIN#
RP4A RP4B RP4C RP4D RP4E RP4F RP4G RP4H
6800hm
CPU_BP0
CPU_BP1
CPU_SCANCLK2
CPU_SCANSHENB
CPU_SCANSHENA
CPU_SCANCLK1
CPU_SCANEN
SWAP FOR LAYOUT
CPURST# 9,13
AVID[0..4] 50
THERMDA 13
THERMTRIP_CPU# 13
COREFB 50
COREFB# 50
THERMDC 13
Title : CPU SMD (2)
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 4 of 64



ASUSTek COMPUTER INC. NB6	Title : CPU (3)	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 5 of 64	



Because 964L SMBUS is connecting to main power, thus, I connect VDDSPD to +V3.3S

<Variant Name>

Title : DDR CONN.

ASUSTek COMPUTER INC. NB6 Engineer: Bruce Lee

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 6 of 64

3 MEMD[0..63]
6,8 DQ[0..63]

3 MEMDQS[0..7]
6,8 DQS[0..7]
3,6,8 MAA[0..13]

3,6,8 BAA[0..1]

6,8 DQM[0..7]
3 MEMDQM[0..7]

RN17 10Ohm
MEMD59 1 2 DQ59
MEMD63 3 4 DQ63
MEMD58 5 6 DQ58
MEMD62 7 8 DQ62

RN16 10Ohm
MEMD56 1 2 DQ56
MEMD60 3 4 DQ60
MEMD61 5 6 DQ61
MEMD57 7 8 DQ57

RN12 10Ohm
MEMD32 2 1 DQ32
MEMD36 4 3 DQ36
MEMD33 6 5 DQ33
MEMD37 8 7 DQ37

RN13 10Ohm
MEMD35 1 2 DQ35
MEMD34 3 4 DQ34
MEMD39 5 6 DQ39
MEMD38 7 8 DQ38

RN14 10Ohm
MEMD44 2 1 DQ44
MEMD41 4 3 DQ41
MEMD45 6 5 DQ45
MEMD40 8 7 DQ40

RN15 10Ohm
MEMD43 1 2 DQ43
MEMD42 3 4 DQ42
MEMD47 5 6 DQ47
MEMD46 7 8 DQ46

RN54 10Ohm
MEMD51 2 1 DQ51
MEMD55 4 3 DQ55
MEMD54 6 5 DQ54
MEMD50 8 7 DQ50

RN53 10Ohm
MEMD48 1 2 DQ48
MEMD49 3 4 DQ49
MEMD53 5 6 DQ53
MEMD52 7 8 DQ52

RN60 10Ohm
MEMD18 1 2 DQ18
MEMD19 3 4 DQ19
MEMD23 5 6 DQ23
MEMD22 7 8 DQ22

RN59 10Ohm
MEMD20 1 2 DQ20
MEMD21 3 4 DQ21
MEMD16 5 6 DQ16
MEMD17 7 8 DQ17

RN20 10Ohm
MEMD10 1 2 DQ10
MEMD11 3 4 DQ11
MEMD14 5 6 DQ14
MEMD15 7 8 DQ15

RN19 10Ohm
MEMD13 1 2 DQ13
MEMD9 3 4 DQ9
MEMD12 5 6 DQ12
MEMD8 7 8 DQ8

RN56 10Ohm
MEMD30 1 2 DQ30
MEMD26 3 4 DQ26
MEMD27 5 6 DQ27
MEMD31 7 8 DQ31

RN55 10Ohm
MEMD24 1 2 DQ24
MEMD25 3 4 DQ25
MEMD29 5 6 DQ29
MEMD28 7 8 DQ28

RN58 10Ohm
MEMD6 1 2 DQ6
MEMD2 3 4 DQ2
MEMD7 5 6 DQ7
MEMD3 7 8 DQ3

RN57 10Ohm
MEMD0 1 2 DQ0
MEMD5 3 4 DQ5
MEMD1 5 6 DQ1
MEMD4 7 8 DQ4

BAA1 1 22P 2 CN10A
MAA0 3 22P 4 CN10B
MAA2 5 22P 6 CN10C
MAA3 7 22P 8 CN10D

MAA7 1 22P 2 CN9A
3,6,8 MCS0# MCS0# 3 22P 4 CN9B
3,6,8 MWEA# MWEA# 5 22P 6 CN9C
3,6,8 MCS1# MCS1# 7 22P 8 CN9D

BAA0 1 22P 2 CN13A
MAA6 3 22P 4 CN13B
6,8 MCKEB MCKEB 5 22P 6 CN13C
6,8 MCKEA MCKEA 7 22P 8 CN13D

GND

C425 MAA4 2 1 22P
C426 MAA1 2 1 22P
3,6,8 MRASA# C427 MRASA# 2 1 22P
C424 MAA10 2 1 22P
C429 MAA8 2 1 22P
3,6,8 MCS3# C428 MCS3# 2 1 22P

3,6,8 MCASA# MCASA# 1 22P 2 CN8A
3,6,8 MCS2# MCS2# 3 22P 4 CN8B
MAA13 5 22P 6 CN8C
7 22P 8 CN8D

MAA11 1 22P 2 CN12A
MAA5 3 22P 4 CN12B
MAA12 5 22P 6 CN12C
MAA9 7 22P 8 CN12D

GND

TO fine tune DQS

MEMDQM7 1 R190 2 DQM7 10Ohm
MEMDQS6 1 R498 2 DQS6 10Ohm
MEMDQS5 1 R188 2 DQS5 10Ohm
MEMDQS4 1 R186 2 DQS4 10Ohm
MEMDQS3 1 R503 2 DQS3 10Ohm
MEMDQS1 1 R194 2 DQS1 10Ohm
MEMDQS2 1 R501 2 DQS2 10Ohm
MEMDQS0 1 R505 2 DQS0 10Ohm

TO fine tune DQM

MEMDQS7 1 R191 2 DQS7 10Ohm
MEMDQM6 1 R497 2 DQM6 10Ohm
MEMDQM5 1 R189 2 DQM5 10Ohm
MEMDQM4 1 R187 2 DQM4 10Ohm
MEMDQM3 1 R504 2 DQM3 10Ohm
MEMDQM1 1 R195 2 DQM1 10Ohm
MEMDQM2 1 R502 2 DQM2 10Ohm
MEMDQM0 1 R506 2 DQM0 10Ohm

3 MEMCKEA MEMCKEA 1 R500 10Ohm 2 MCKEA
3 MEMCKEB MEMCKEB 1 R499 10Ohm 2 MCKEB

#24665 Rev. 2.17 October 2003

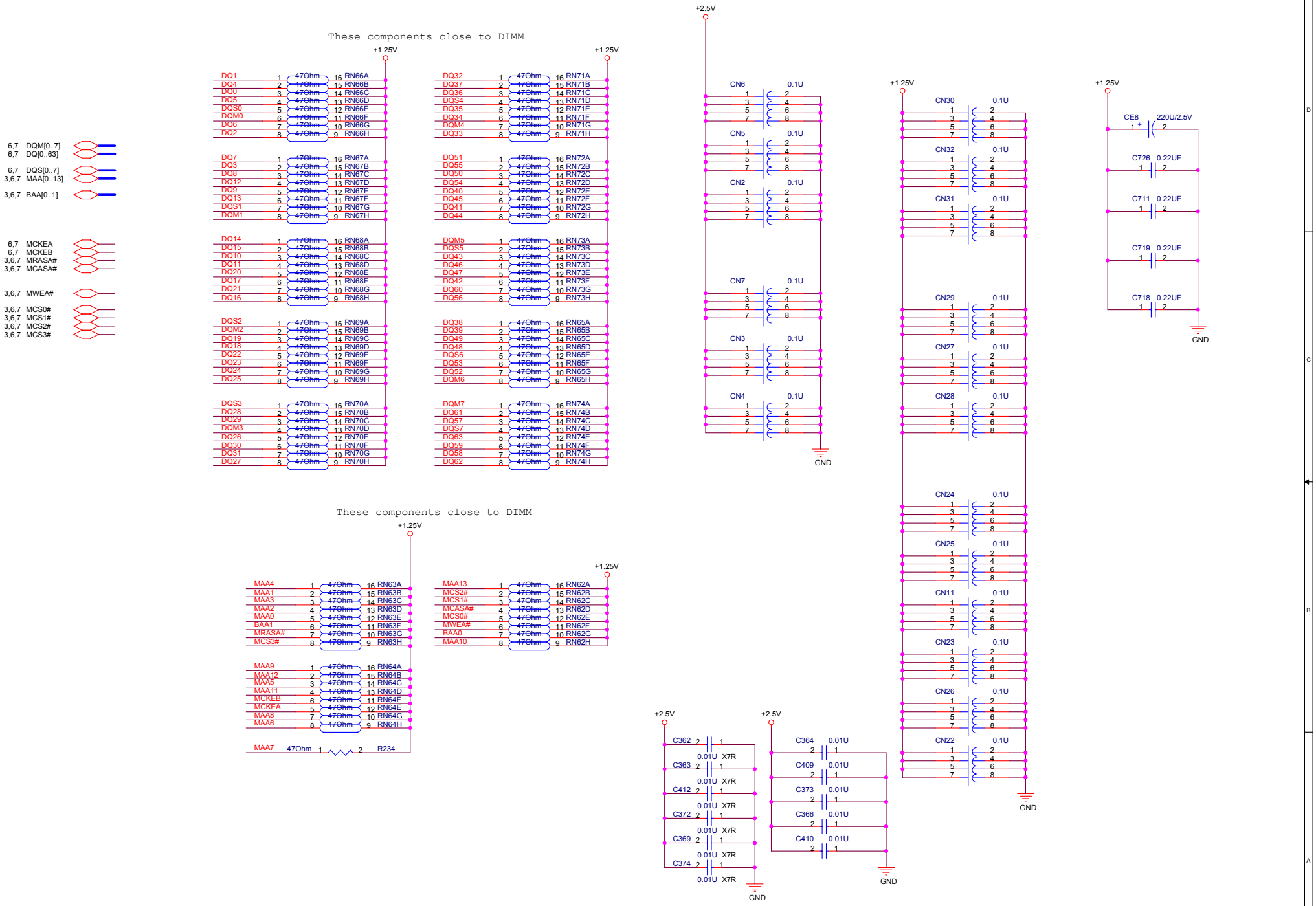
ASUSTek COMPUTER INC. NB6

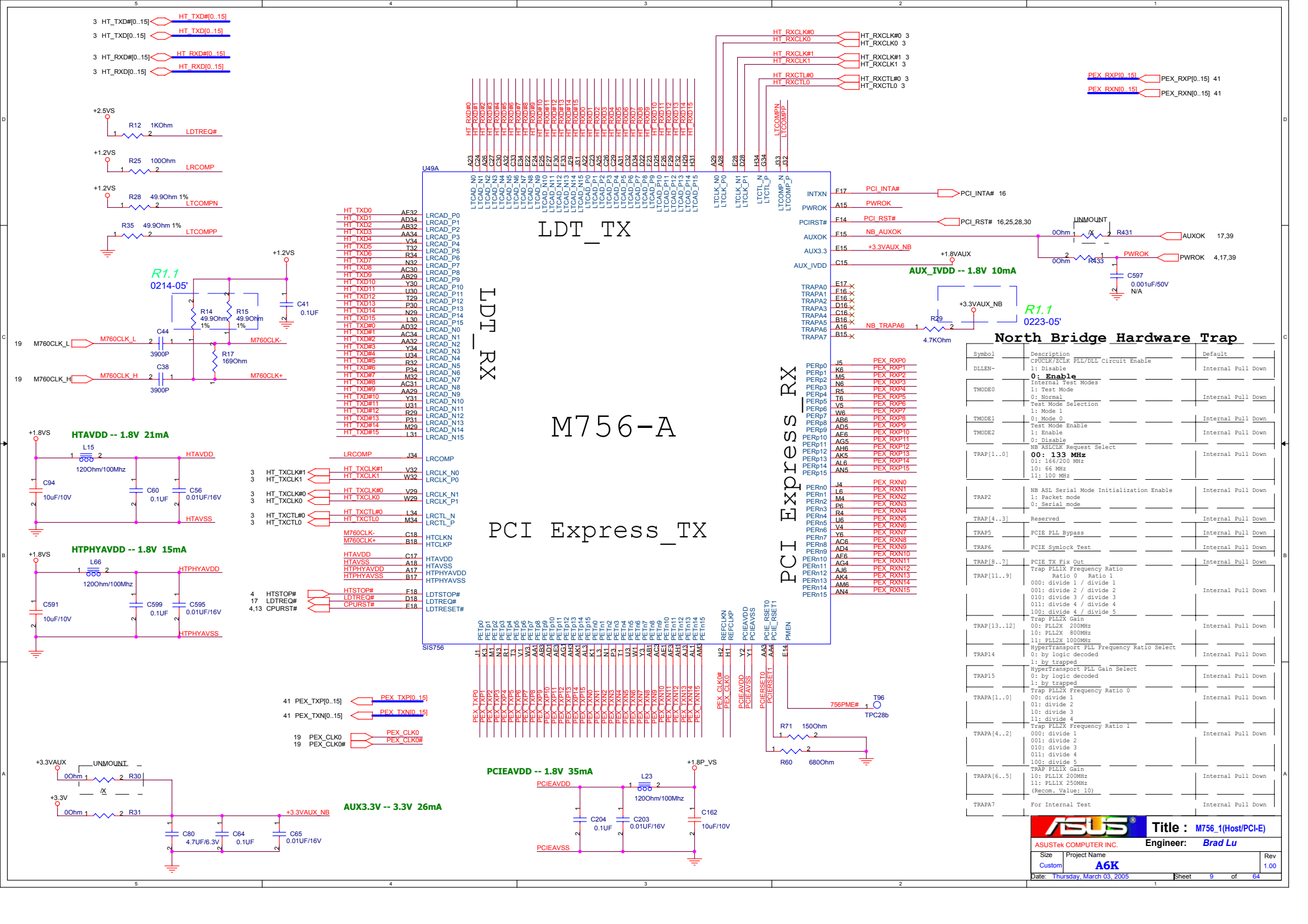
Title : DDR Series Term.

Engineer: Bruce Lee

Size	Project Name	Rev
Custom	A6k	1.0

Date: Thursday, March 03, 2005 Sheet 7 of 64


These components close to DIMM
+1.25V
DQ1 DQ4 DQ0 DQ5 DQS0 DQM0 DQ6 DQ2 RN66A RN66B RN66C RN66D RN66E RN66F RN66G RN66H
DQ7 DQ3 DQ8 DQ12 DQ9 DQ13 DQS1 DQM1 RN67A RN67B RN67C RN67D RN67E RN67F RN67G RN67H
DQ14 DQ15 DQ10 DQ11 DQ20 DQ17 DQ21 DQ16 RN68A RN68B RN68C RN68D RN68E RN68F RN68G RN68H
DQS2 DQM2 DQ19 DQ18 DQ22 DQ23 DQ24 DQ25 RN69A RN69B RN69C RN69D RN69E RN69F RN69G RN69H
DQS3 DQ28 DQ29 DQM3 DQ26 DQ30 DQ31 DQ27 RN70A RN70B RN70C RN70D RN70E RN70F RN70G RN70H
DQ32 DQ37 DQ36 DQS4 DQ35 DQ34 DQM4 DQ33 RN71A RN71B RN71C RN71D RN71E RN71F RN71G RN71H
DQ51 DQ55 DQ50 DQ54 DQ40 DQ45 DQ41 DQ44 RN72A RN72B RN72C RN72D RN72E RN72F RN72G RN72H
DQM5 DQS5 DQ43 DQ46 DQ47 DQ42 DQ60 DQ56 RN73A RN73B RN73C RN73D RN73E RN73F RN73G RN73H
DQ38 DQ39 DQ49 DQ48 DQS6 DQ53 DQ52 DQM6 RN65A RN65B RN65C RN65D RN65E RN65F RN65G RN65H
DQM7 DQ61 DQ57 DQS7 DQ63 DQ59 DQ58 DQ62 RN74A RN74B RN74C RN74D RN74E RN74F RN74G RN74H
47Ohm
6,7 DQM[0..7]
6,7 DQ[0..63]
6,7 DQS[0..7]
3,6,7 MAA[0..13]
3,6,7 BAA[0..1]
6,7 MCKEA
6,7 MCKEB
3,6,7 MRASA#
3,6,7 MCASA#
3,6,7 MWEA#
3,6,7 MCS0#
3,6,7 MCS1#
3,6,7 MCS2#
3,6,7 MCS3#
These components close to DIMM
+1.25V
MAA4 MAA1 MAA3 MAA2 MAA0 BAA1 MRASA# MCS3# RN63A RN63B RN63C RN63D RN63E RN63F RN63G RN63H
MAA9 MAA12 MAA5 MAA11 MCKEB MCKEA MAA8 MAA6 RN64A RN64B RN64C RN64D RN64F RN64E RN64G RN64H
MAA7 47Ohm R234
MAA13 MCS2# MCS1# MCASA# MCS3# MWEA# BAA0 MAA10 RN62A RN62B RN62C RN62D RN62E RN62F RN62G RN62H
+2.5V
CN6 CN5 CN2 CN7 CN3 CN4 0.1U
GND
+1.25V
CN30 CN32 CN31 CN29 CN27 CN28 CN24 CN25 CN11 CN23 CN26 CN22 0.1U
GND
+1.25V
CE8 220U/2.5V
C726 C711 C719 C718 0.22UF
GND
+2.5V
C362 C363 C412 C372 C369 C374 0.01U X7R
GND
+2.5V
C364 C409 C373 C366 C410 0.01U
GND
ASUSTek COMPUTER INC. NB6
Title : DDR VTT Term.
Engineer: Bruce Lee
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 8 of 64


HT_TXD#[0..15]
HT_TXD[0..15]
HT_RXD#[0..15]
HT_RXD[0..15]
HT_RXCLK#0
HT_RXCLK0
HT_RXCLK#1
HT_RXCLK1
HT_RXCTL#0
HT_RXCTL0
PEX_RXP[0..15]
PEX_RXN[0..15]
+2.5VS
R12 1KOhm
LDTREQ#
+1.2VS
R25 100Ohm
LRCOMP
R28 49.9Ohm 1%
LTCOMPN
R35 49.9Ohm 1%
LTCOMPP
R1.1
0214-05'
R14 49.9Ohm 1%
R15 49.9Ohm 1%
C41 0.1UF
C44 3900P
C38 3900P
R17 169Ohm
M760CLK_L
M760CLK-
M760CLK_H
M760CLK+
U49A
LDT_TX
LDT_RX
M756-A
PCI Express_TX
PCI Express_RX
SIS756
INTXN
PWROK
PCIRST#
AUXOK
AUX3.3
AUX_IVDD
PCI_INTA#
PCI_RST#
NB_AUXOK
+3.3VAUX_NB
AUX_IVDD -- 1.8V 10mA
TRAPA0
TRAPA1
TRAPA2
TRAPA3
TRAPA4
TRAPA5
TRAPA6
TRAPA7
NB_TRAPA6
R29 4.7KOhm
+3.3VAUX_NB
R1.1
0223-05'
UNMOUNT
0Ohm R431
0Ohm R433
AUXOK 17,39
PWROK 4,17,39
C597 0.001uF/50V N/A
North Bridge Hardware Trap
Symbol | Description | Default
DLLEN- | CPUCLK/ZCLK PLL/DLL Circuit Enable 1: Disable | Internal Pull Down
TMODE0 | 0: Enable Internal Test Modes 1: Test Mode 0: Normal | Internal Pull Down
TMODE1 | Test Mode Selection 1: Mode 1 0: Mode 0 | Internal Pull Down
TMODE2 | Test Mode Enable 1: Enable 0: Disable | Internal Pull Down
TRAP[1..0] | NB ASLCLK Request Select 00: 133 MHz 01: 166/200 MHz 10: 66 MHz 11: 100 MHz | Internal Pull Down
TRAP2 | NB ASL Serial Mode Initialization Enable 1: Packet mode 0: Serial mode | Internal Pull Down
TRAP[4..3] | Reserved | Internal Pull Down
TRAP5 | PCIE PLL Bypass | Internal Pull Down
TRAP6 | PCIE Symlock Test | Internal Pull Down
TRAP[8..7] | PCIE TX Fix Out | Internal Pull Down
TRAP[11..9] | Trap PLL1X Frequency Ratio Ratio 0 Ratio 1 000: divide 1 / divide 1 001: divide 2 / divide 2 010: divide 3 / divide 3 011: divide 4 / divide 4 100: divide 4 / divide 5 | Internal Pull Down
TRAP[13..12] | Trap PLL2X Gain 00: PLL2X 200MHz 10: PLL2X 800MHz 11: PLL2X 1000MHz | Internal Pull Down
TRAP14 | HyperTransport PLL Frequency Ratio Select 0: by logic decoded 1: by trapped | Internal Pull Down
TRAP15 | HyperTransport PLL Gain Select 0: by logic decoded 1: by trapped | Internal Pull Down
TRAPA[1..0] | Trap PLL2X Frequency Ratio 0 00: divide 1 01: divide 2 10: divide 3 11: divide 4 | Internal Pull Down
TRAPA[4..2] | Trap PLL2X Frequency Ratio 1 000: divide 1 001: divide 2 010: divide 3 011: divide 4 100: divide 5 | Internal Pull Down
TRAPA[6..5] | TRAP PLL1X Gain 10: PLL1X 200MHz 11: PLL1X 250MHz (Recom. Value: 10) | Internal Pull Down
TRAPA7 | For Internal Test | Internal Pull Down
+1.8VS
HTAVDD -- 1.8V 21mA
L15 120Ohm/100Mhz
C94 10uF/10V
C60 0.1UF
C56 0.01UF/16V
HTPHYAVDD -- 1.8V 15mA
L66 120Ohm/100Mhz
C591 10uF/10V
C599 0.1UF
C595 0.01UF/16V
HTSTOP#
LDTREQ#
CPURST#
LDTSTOP#
LDTREQ#
LDTRESET#
M760CLK-
M760CLK+
PEX_TXP[0..15]
PEX_TXN[0..15]
PEX_CLK0
PEX_CLK0#
+3.3VAUX
+3.3V
R30 0Ohm
R31 0Ohm
C80 4.7UF/6.3V
C64 0.1UF
C65 0.01UF/16V
AUX3.3V -- 3.3V 26mA
PCIEAVDD -- 1.8V 35mA
+1.8P_VS
L23 120Ohm/100Mhz
C204 0.1UF
C203 0.01UF/16V
C162 10uF/10V
PCIEAVSS
756PME#
T96 TPC28b
R71 150Ohm
R60 680Ohm
ASUSTek COMPUTER INC.
Title : M756_1(Host/PCI-E)
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.00
Date: Thursday, March 03, 2005
Sheet 9 of 64

The differences between the traces of MuTIOL Strobes and Data in each group should be smaller than 0.05",and strobes need guide GND trace

U49B

M756-2

MuTIOL

Trap

0105-05'

19 CLK_ZIP_NB — CLK_ZIP_NB — AM16 ZCLK

16 ZUREQ — ZUREQ — AL24 ZUREQ
16 ZDREQ — ZDREQ — AP23 ZDREQ

16 ZSTB0# — ZSTB0# — AL20 ZSTB0#
16 ZSTB0 — ZSTB0 — AM20 ZSTB0

16 ZSTB1# — ZSTB1# — AN19 ZSTB1#
16 ZSTB1 — ZSTB1 — AP19 ZSTB1

16 ZAD[0..16] — ZAD[0..16]

ZAD2 AJ23 ZAD2
ZAD0 AK23 ZAD0
ZAD5 AJ21 ZAD5
ZAD3 AK21 ZAD3
ZAD10 AJ19 ZAD10
ZAD8 AK19 ZAD8
ZAD13 AJ17 ZAD13
ZAD11 AK17 ZAD11
ZAD4 AL22 ZAD4
ZAD1 AM22 ZAD1
ZAD7 AN21 ZAD7
ZAD6 AP21 ZAD6
ZAD12 AL18 ZAD12
ZAD9 AM18 ZAD9
ZAD15 AN17 ZAD15
ZAD14 AP17 ZAD14
ZAD16 AN23 ZAD16

The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"

ZVREF AP24 ZVREF

ZCMP_N AN24 ZCMP_N
ZCMP_P AM24 ZCMP_P

Z1XAVDD AK16 Z1XAVDD
Z1XAVSS AL16 Z1XAVSS

Z4XAVDD AP16 Z4XAVDD
Z4XAVSS AN16 Z4XAVSS

AP9 VSSP16
AP11 VSSP17
AN11 VSSP18
AP10 VSSP19
AN10 VSSP20

ENTEST AK31 ENTEST — R101 1 2 0Ohm

DLLEN# AK29 CPUDLLENN — T108 TPC28b

TESTMODE2 AL34
TESTMODE1 AL33
TESTMODE0 AL32

TRAP15 AM33
TRAP14 AM34
TRAP13 AN33
TRAP12 AM32
TRAP11 AN32
TRAP10 AP32
TRAP9 AL31
TRAP8 AM31
TRAP7 AN31
TRAP6 AP31
TRAP5 AK30
TRAP4 AL30
TRAP3 AM30
TRAP2 AN30
TRAP1 AP30
TRAP0 AJ29

DB15 AP27
DB14 AN27
DB13 AM27
DB12 AL27
DB11 AK27
DB10 AJ27
DB9 AP28
DB8 AN28
DB7 AM28
DB6 AL28
DB5 AK28
DB4 AJ28
DB3 AP29
DB2 AN29
DB1 AM29
DB0 AL29

SIS756

Place near M756 chip.

+1.8VS
R108 56Ohm ZCMP_N
MuTIOL 1.0 Vref=0.5 *VCC1.8
R116 150Ohm 1%
C295 0.1uF/10V
C294 10uF/10V
MuTIOL 2.0 Vref=0.25 *VCC1.8 ZVREF
R123 49.9Ohm 1%
C298 0.1uF/10V
R106 56Ohm ZCMP_P

+1.8VS
L29 120Ohm/100Mhz
Z1XAVDD
C278 0.1UF
C279 0.01UF/16V
Z1XAVSS
Z1XAVDD-- 1.8V 9mA

+1.8VS
L34 120Ohm/100Mhz
Z4XAVDD
C297 10uF/10V
C291 0.01UF/16V
C292 0.1UF
Z4XAVSS
Z4XAVDD-- 1.8V 14mA

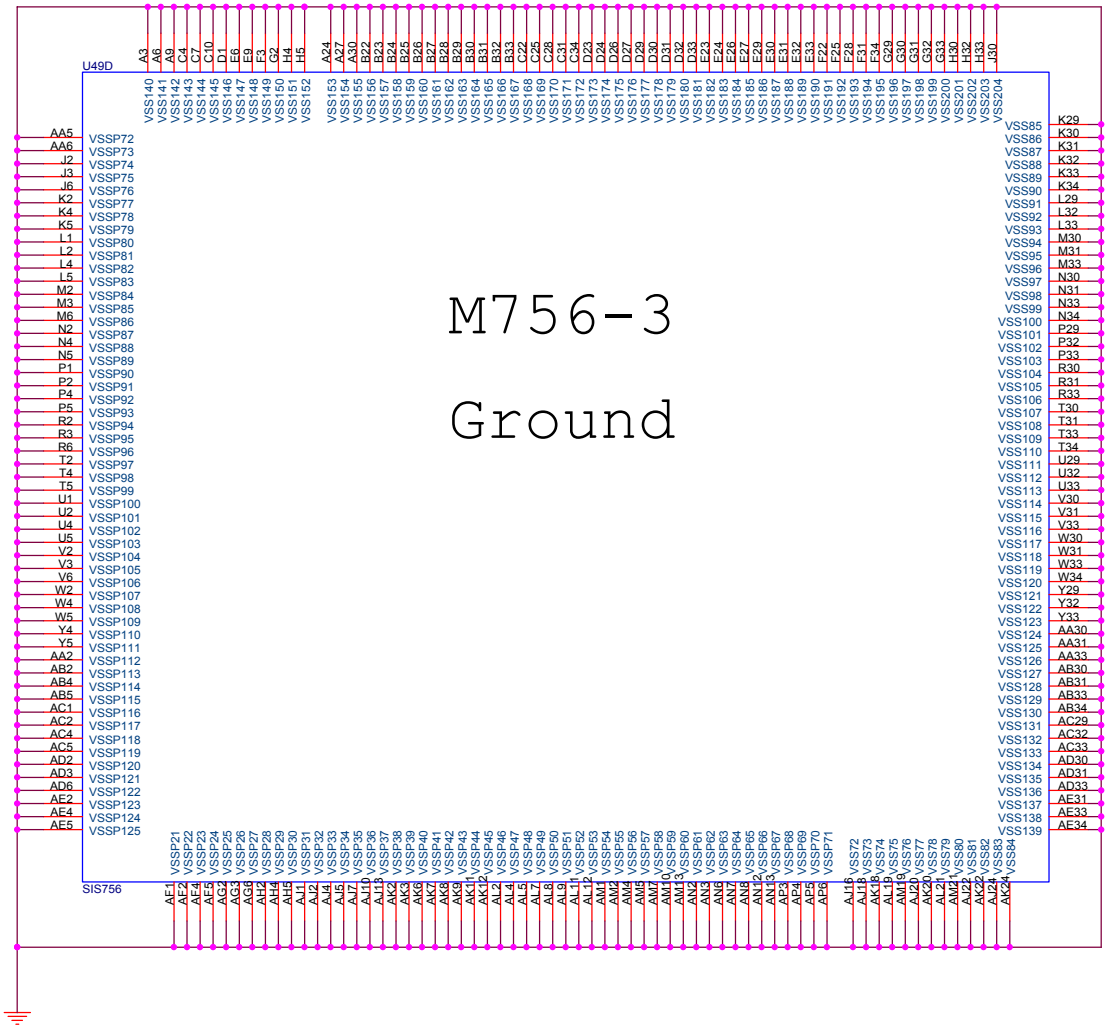
ASUSTek COMPUTER INC.

Title : SIS756-2 MuTIOL

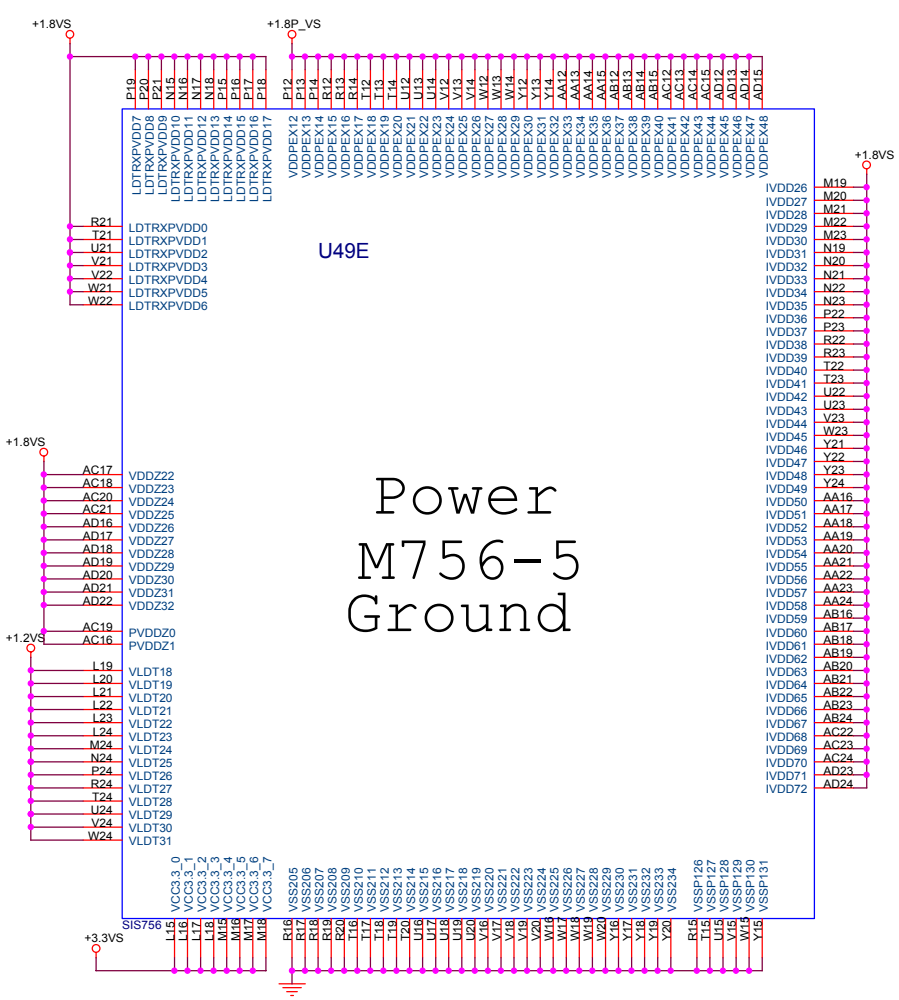
Engineer: Brad Lu

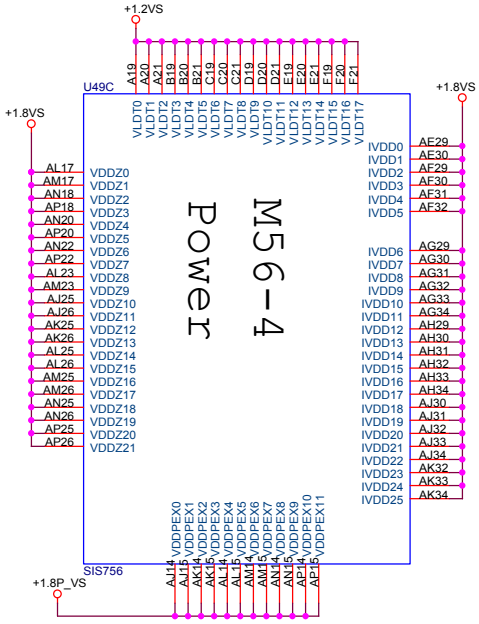
Size	Project Name	Rev
Custom	A6K	1.00

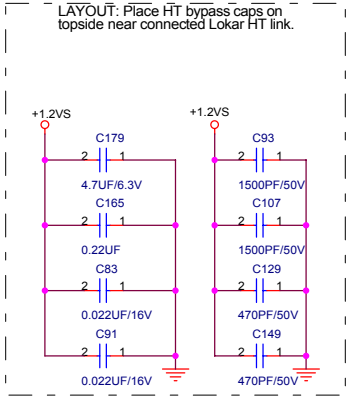
Date: Thursday, March 03, 2005 Sheet 10 of 64

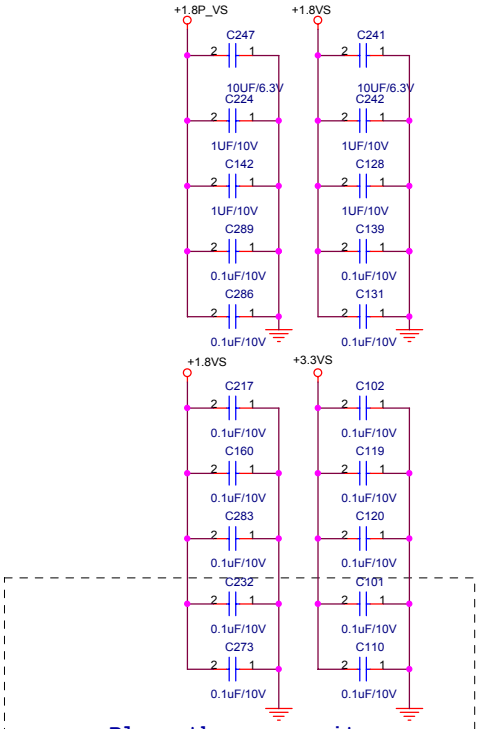


ASUSTek COMPUTER INC.	Title : M756_3		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 1.00
Date: Thursday, March 03, 2005	Sheet 11 of 64		









+3.3VS(VCC3, MAX):29mA
+1.8VS(VDDZ, MAX):119mA
+1.8VS(IVDD, MAX):1.783A
+1.8VS(VDDPEX, MAX):1164mA
+1.2VS(VLDT, MAX):153mA

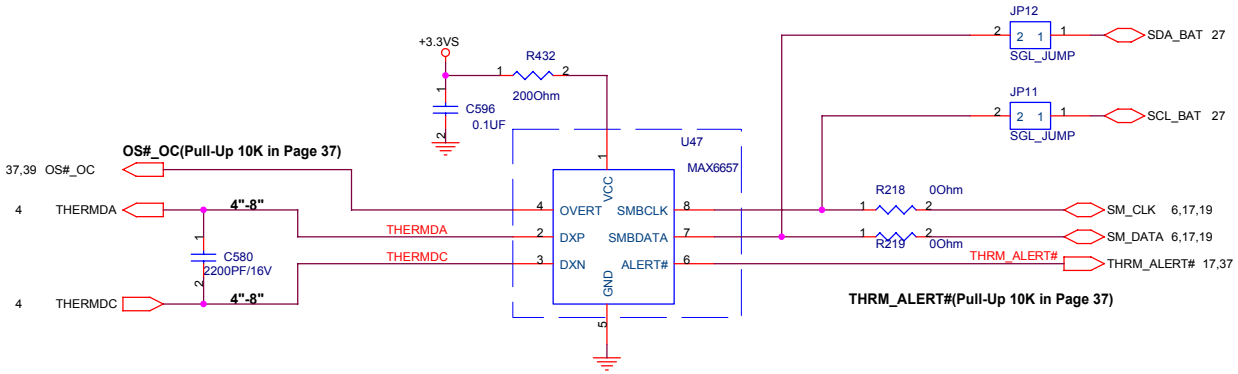
ASUSTek COMPUTER INC.

Title : M756_4(POWER)

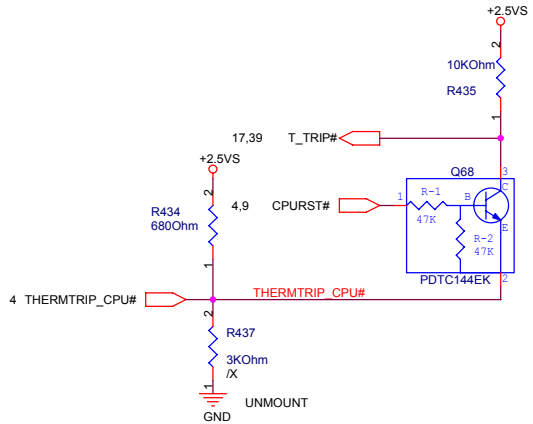
Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	1.00

Date: Thursday, March 03, 2005 Sheet 12 of 64



0222-05' *R1.1*



THERMAL

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTek COMPUTER INC. NB6	Title : THERMAL	
	Engineer: Brad Lu	
Size: A3	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 13 of 64	

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

A3K used D1 R:1.0
Inverter Board

USB PORT 3 for CAMERA

LCD Power

SI3865: US$0.22

LCD CABLE ID:	PID3	PID2	PID1	PID0
15.1 XGA	1	1	0	1
15.1 SXGA+	1	0	1	1
15.4 WXGA	1	1	1	0
15.4 WSXGA+	0	1	1	1

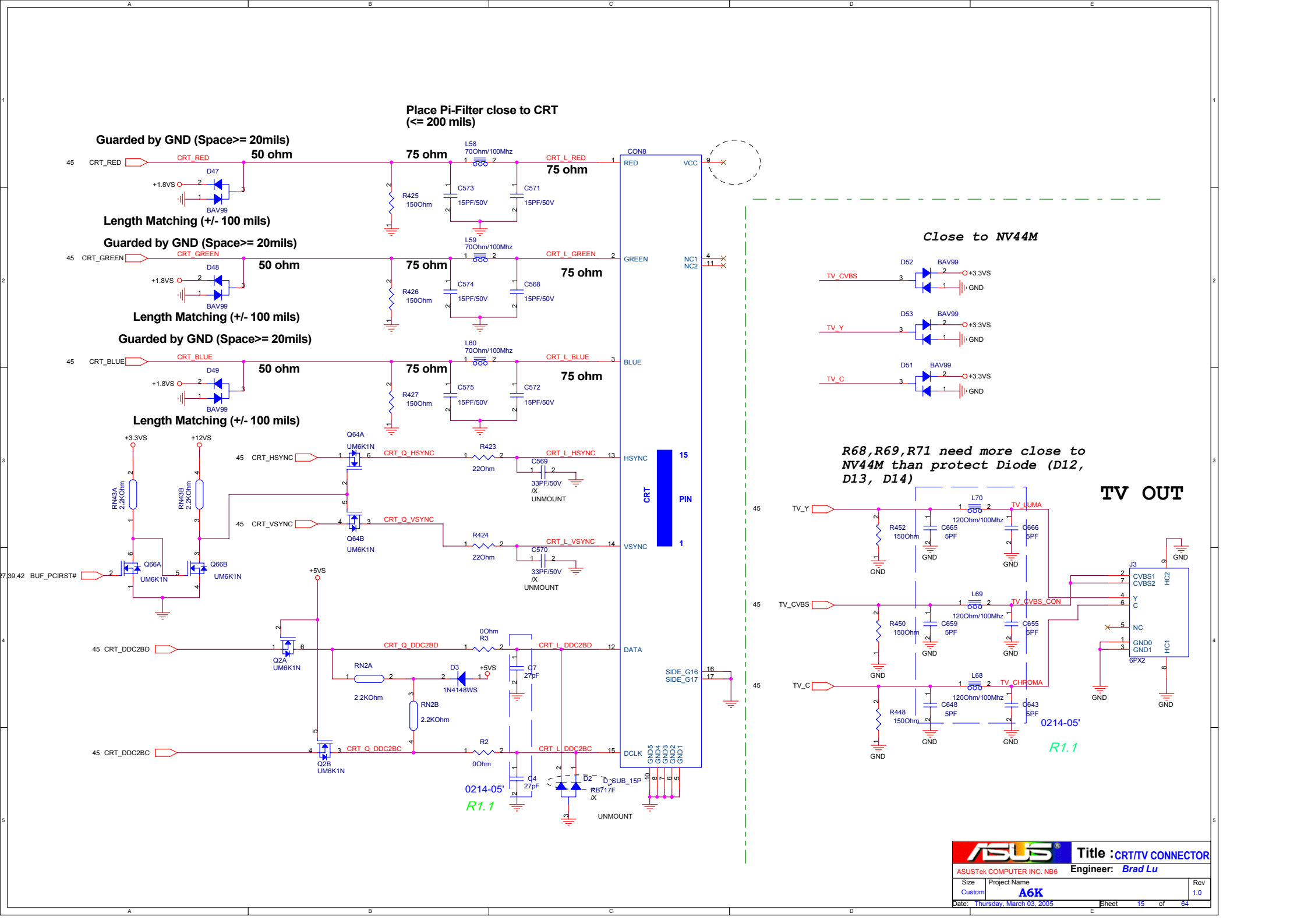
0222-05' R1.1

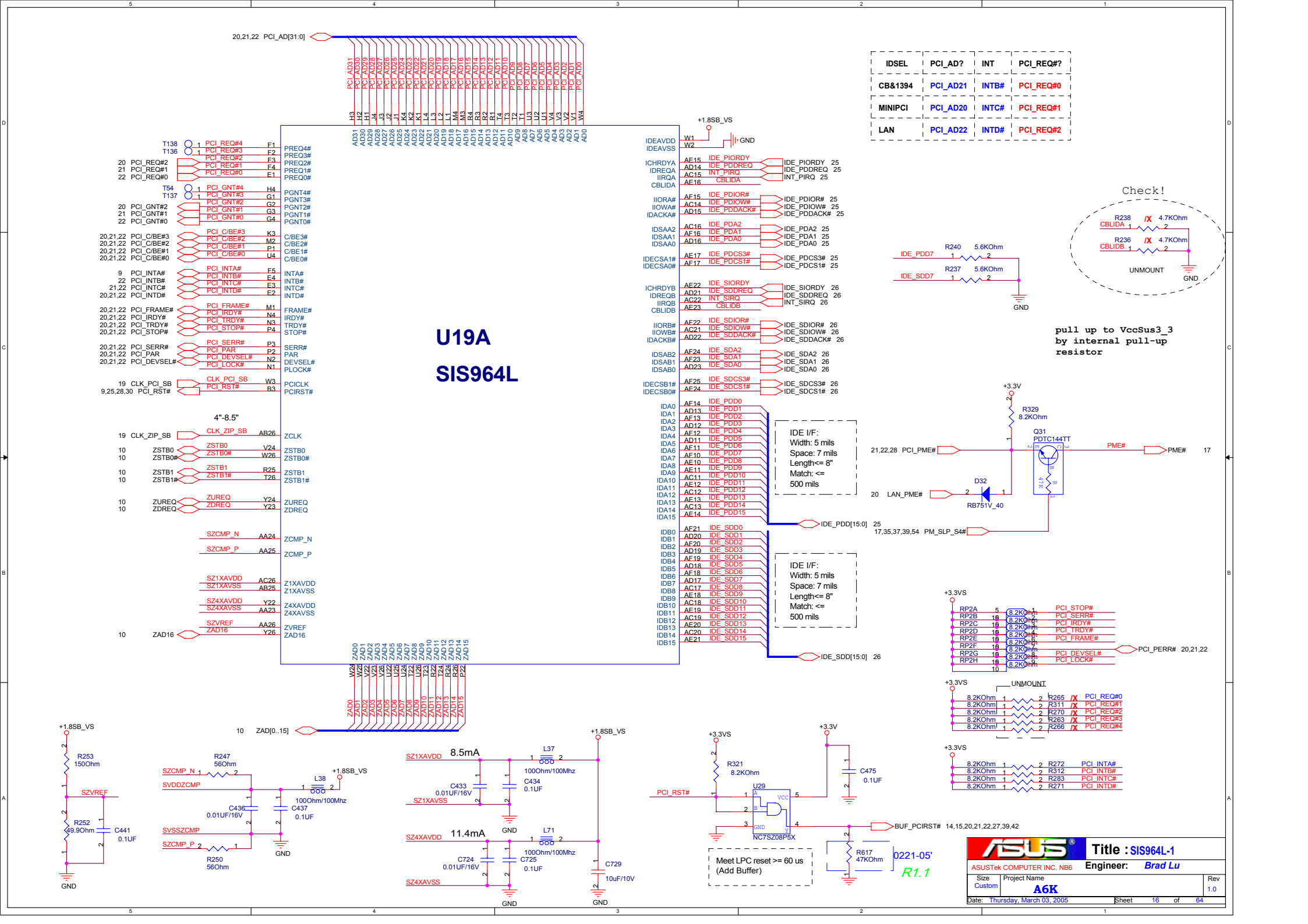
R1.1 0225-05' cancel next version

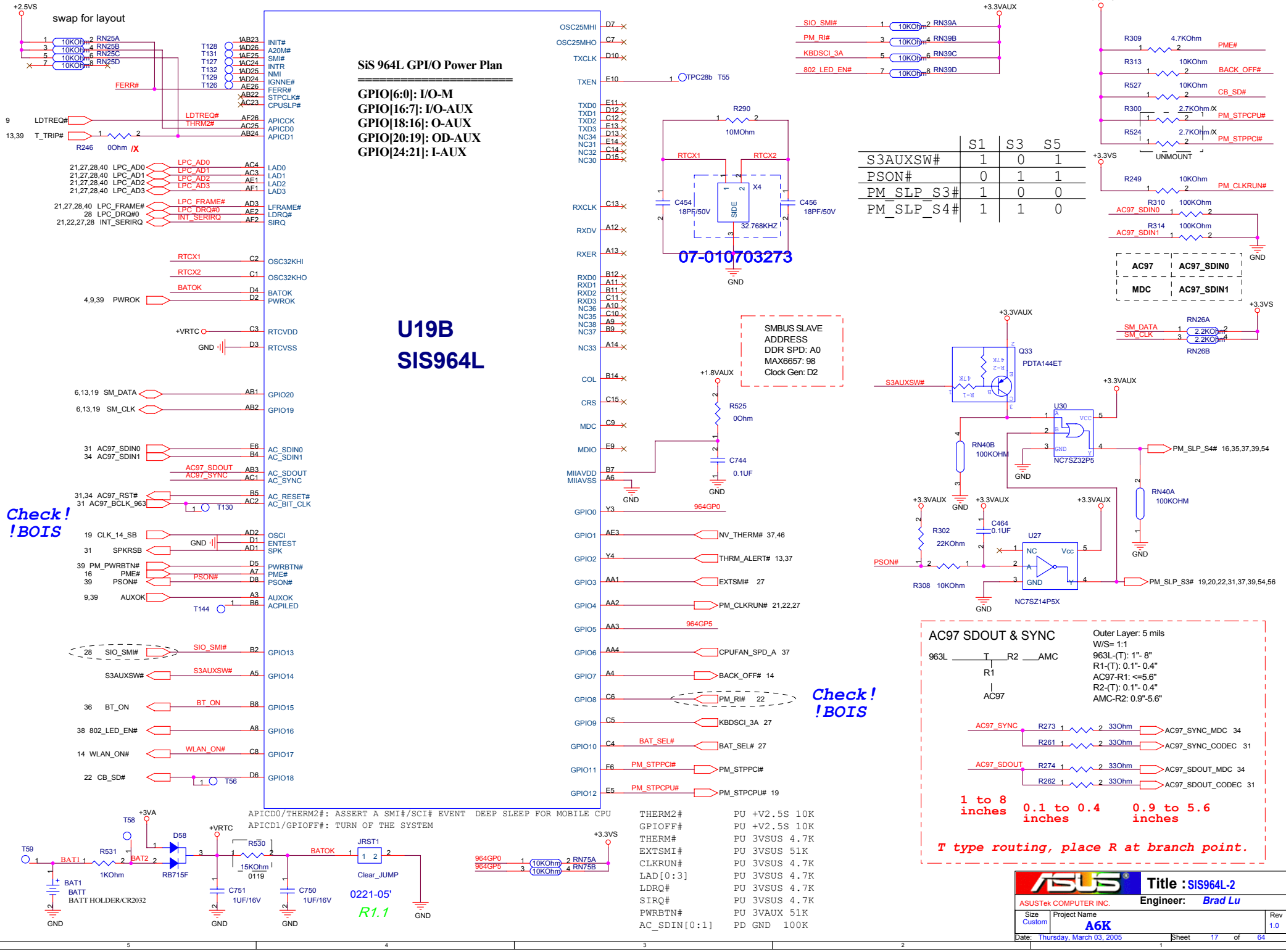
0114-05' CON1 Changed to "12-17001030A"

Caution:
Must tune R1404 & C1415 to meet Panel Spec

Title :	LVDS & BACKLIGHT		
ASUSTek COMPUTER INC. NB6	Engineer:	Brad Lu	
Size: Custom	Project Name: A6K		Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 14 of 64		


Place Pi-Filter close to CRT
(<= 200 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
50 ohm
75 ohm
75 ohm
Length Matching (+/- 100 mils)
CRT_RED
CRT_GREEN
CRT_BLUE
D47
D48
D49
BAV99
+1.8VS
L58 70Ohm/100Mhz
L59 70Ohm/100Mhz
L60 70Ohm/100Mhz
R425 150Ohm
R426 150Ohm
R427 150Ohm
C573 15PF/50V
C571 15PF/50V
C574 15PF/50V
C568 15PF/50V
C575 15PF/50V
C572 15PF/50V
CRT_L_RED
CRT_L_GREEN
CRT_L_BLUE
CON8
RED
GREEN
BLUE
VCC
NC1
NC2
HSYNC
VSYNC
DCLK
DATA
CRT
15
PIN
1
SIDE_G16
SIDE_G17
GND5
GND4
GND3
GND2
GND1
+3.3VS
+12VS
RN43A 2.2KOhm
RN43B 2.2KOhm
Q64A UM6K1N
Q64B UM6K1N
Q66A UM6K1N
Q66B UM6K1N
CRT_HSYNC
CRT_VSYNC
CRT_Q_HSYNC
CRT_Q_VSYNC
R423 22Ohm
R424 22Ohm
C569 33PF/50V /X UNMOUNT
C570 33PF/50V /X UNMOUNT
CRT_L_HSYNC
CRT_L_VSYNC
BUF_PCIRST#
+5VS
Q2A UM6K1N
Q2B UM6K1N
CRT_DDC2BD
CRT_DDC2BC
CRT_Q_DDC2BD
CRT_Q_DDC2BC
CRT_L_DDC2BD
CRT_L_DDC2BC
0Ohm R3
R2 0Ohm
RN2A 2.2KOhm
RN2B 2.2KOhm
D3 1N4148WS
C7 27pF
C4 27pF
D2 RB717F /X
D_SUB_15P
UNMOUNT
0214-05'
R1.1
Close to NV44M
TV_CVBS
TV_Y
TV_C
D52 BAV99
D53 BAV99
D51 BAV99
+3.3VS
GND
R68,R69,R71 need more close to NV44M than protect Diode (D12, D13, D14)
TV OUT
L70 120Ohm/100Mhz
L69 120Ohm/100Mhz
L68 120Ohm/100Mhz
R452 150Ohm
R450 150Ohm
R448 150Ohm
C665 5PF
C666 5PF
C659 5PF
C655 5PF
C648 5PF
C643 5PF
TV_LUMA
TV_CVBS_CON
TV_CHROMA
J3
CVBS1
CVBS2
Y
C
NC
GND0
GND1
6PX2
HC2
HC1
0214-05'
R1.1
ASUSTek COMPUTER INC. NB6
Title : CRT/TV CONNECTOR
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 15 of 64


20,21,22 PCI_AD[31:0]
U19A
SIS964L
IDSEL | PCI_AD? | INT | PCI_REQ#?
CB&1394 | PCI_AD21 | INTB# | PCI_REQ#0
MINIPCI | PCI_AD20 | INTC# | PCI_REQ#1
LAN | PCI_AD22 | INTD# | PCI_REQ#2
Check!
R238 /X 4.7KOhm
R236 /X 4.7KOhm
CBLIDA
CBLIDB
UNMOUNT
GND
pull up to VccSus3_3 by internal pull-up resistor
IDE I/F: Width: 5 mils Space: 7 mils Length<= 8" Match: <= 500 mils
IDE_PDD[15:0] 25
IDE_SDD[15:0] 26
4"-8.5"
10 ZAD[0..15]
Meet LPC reset >= 60 us (Add Buffer)
BUF_PCIRST# 14,15,20,21,22,27,39,42
PCI_PERR# 20,21,22
PME# 17
Title : SIS964L-1
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 16 of 64



ASUSTek COMPUTER INC.

Title : SIS964L-2

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 17 of 64

+3.3VS
OVDD/PVDD: 55 mA

+1.8SB_VS
IVDD: 517.4 mA
VDDZ : 19.9 mA
IDEAVDD: 6.9 mA

+1.8VAUX
IVDDAUX: 31.1 mA
MIIAVDD: 2.3 mA
USBPVDD: 7.9 mA
USBCMPAVDD18: 8.5 mA

+3.3VAUX
OVDD_AUX/PVDD_AUX: 52 mA
MIIAVDD: 10 mA
USBVDD33: 1 mA
USBCMPAVDD33: 3.6 mA

+1.8V
USBVDD18: 274.1 mA

UNMOUNT
R526 10MOhm /X
X8
12MHZ
OSC12MOUT
OSC12MIN
CHANGE TO 30PPM
C749 15PF/50V
C733 15PF/50V
GND

U19C
SIS964L

OSC12MIN E25 OSC12MHI
OSC12MOUT E26 OSC12MHO

USB_PP0 G26 UV0+
USB_PN0 G25 UV0-
USB_PP1 H24 UV1+
USB_PN1 H23 UV1-
USB_PP2 C21 UV2+
USB_PN2 D21 UV2-
USB_PP3 A22 UV3+
USB_PN3 B22 UV3-
USB_PP4 C19 UV4+
USB_PN4 D19 UV4-
USB_PP5 A20 UV5+
USB_PN5 B20 UV5-
C17 UV6+
D17 UV6-
A18 UV7+
B18 UV7-

USBOC#0 SL6 C26 OC0#
USBOC#1 SL8 C24 OC1#
USBOC#2 SL4 D26 OC2#
USBOC#3 SL5 D25 OC3#
USBOC#4 SL7 D24 OC4#
USBOC#5 SL3 E24 OC5#
USBOC#6 SL2 E23 OC6#
USBOC#7 SL1 F22 OC7#

R305 127Ohm USBREF A24 USBREF

+3.3V L73 120Ohm/100Mhz +3.3V_UVDD
C746 0.1UF C739 0.1UF
G16 UVDD33_1
G18 UVDD33_2
H20 UVDD33_3

+1.8V L74 120Ohm/100Mhz +1.8V_UVDD
C737 0.1UF C735 0.1UF C732 10uF/10V
E18 UVDD18_1
E20 UVDD18_2
E22 UVDD18_3
F17 UVDD18_4
F18 UVDD18_5
F19 UVDD18_6
F20 UVDD18_7
F21 UVDD18_8
G22 UVDD18_9
H22 UVDD18_10

+IVDD_AUX
C738 0.1UF
C742 0.1UF
C740 0.1UF
F24 USBPVDD18
F23 USBPVSS18
A25 USBCMPAVDD18
B24 USBCMPAVSS18
D23 USBCMPAVDD33
C23 USBCMPAVSS33
G21 IVDD_AUX4
H21 IVDD_AUX5

+1.8VAUX L72 120Ohm/100Mhz +IVDD_AUX
C736 0.1UF

Connect to +V1.8AUX if USB wakeup has supported in S3 & S5

964L Strap Pin

NC47 AE4
NC48 AF4
NC42 AC5
NC43 AD7
NC41 AC7
NC49 AF6
NC46 AE6
NC44 AD9
NC40 AC9
NC50 AF8
NC45 AE8
NC39 AB4

IVDD3 AA6
IVDD4 AA7
IVDD5 AA8
IVDD6 AA9
IVDD1 AA10
IVDD12 AB6
+1.8SB_VS

IVDD22 Y2
VSS55 Y1
IVDD13 AF3
VSS8 AD4
IVDD11 AB5
VSS9 AD5
GND

EESK/GPIO21 A16
EEDI/GPIO22 A15
EEDO/GPIO23 B16
EECS/GPIO24 B15
EECS_964
EEDO_964
R307 4.7KOhm +3.3VAUX
R306 4.7KOhm GND

IPB_OUT0 A26 IPB_OUT0 T146
IPB_OUT1 B25 IPB_OUT1 T145
TRAP0 B26
TRAP1 C25
R304 22Ohm
R303 22Ohm
GND GND

SiS 964L Strap Pin	0	1	Default
IPB_OUT0(MuTIOL 1G Clock PLL)	enable	disable	0
IPB_OUT1(MuTIOL Operation Mode Select)	Partial-Swin	Full-Swin	0
AC_SYNC(PCI Clock PLL)	enable	disable	0
Trap [1:0] (MuTIOL Operation Frequency Select)	133MHz	66MHz	0
OC4-(SB debug mode)	enable	disable	1

+3.3VAUX
10KOhm RN34A USBOC#7
10KOhm RN34B USBOC#6
10KOhm RN34C USBOC#5
10KOhm RN34D USBOC#2
10KOhm RN37A USBOC#3
10KOhm RN37B USBOC#0
10KOhm RN37C USBOC#4
10KOhm RN37D USBOC#1

+3.3VAUX C748 0.1UF C741 0.1UF GND
+2.5VS C721 0.1UF GND
+3.3VS C723 0.1UF C731 0.1UF GND
+1.8VAUX C734 0.1UF GND
+1.8SB_VS C728 0.1UF C720 0.1UF C438 0.1UF C445 0.1UF GND
Placed under 964

USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils

U19D
SIS964L

+1.8SB_VS
P26 VDDZ2
P21 VDDZ1
R21 VDDZ3
T25 VDDZ4
V25 VDDZ6
V21 VDDZ5
W21 VDDZ7
Y25 VDDZ9
Y21 VDDZ8

M21 IVDD16
N21 IVDD17
T21 IVDD19
U21 IVDD21
AB18 IVDD10
AB16 IVDD9
AB14 IVDD8
AB11 IVDD7
AA5 IVDD2
Y5 IVDD23
T5 IVDD20
R5 IVDD18
L5 IVDD15
G5 IVDD14

L21 PVDD5
AA21 PVDD1
AB19 PVDD3
AB13 PVDD2
U5 PVDD7
M5 PVDD6
H5 PVDD4

+3.3VS
K21 OVDD8
J21 OVDD6
AB20 OVDD5
AB17 OVDD4
AB15 OVDD3
AB12 OVDD2
AB10 OVDD1
W5 OVDD13
V5 OVDD12
P5 OVDD11
N5 OVDD10
K5 OVDD9
J5 OVDD7

+2.5VS
AA22 VTT1
AB21 VTT2

+1.8VAUX
F9 IVDD_AUX3
F12 IVDD_AUX1
F15 IVDD_AUX2

B10 OVDD_AUX1
B13 OVDD_AUX2
E7 OVDD_AUX5
E12 OVDD_AUX3
E15 OVDD_AUX4
E10 OVDD_AUX6
F11 OVDD_AUX7
+3.3VAUX F13 OVDD_AUX8
F7 OVDD_AUX9
G20 OVDD_AUX10
E8 PVDD_AUX1
F14 PVDD_AUX2

W22 NC1
P25 NC2
P24 NC3
P23 NC4
N26 NC5
N25 NC6
N24 NC7
N23 NC8
N22 NC9
M26 NC10
M25 NC11
M24 NC12
M23 NC13
M22 NC14
L26 NC15
L25 NC16
L24 NC17
L23 NC18
L22 NC19

K26 NC20
K25 NC21
K24 NC22
K23 NC23
J26 NC24
J25 NC25
J24 NC26
J22 NC27
K22 NC28
F16 NC29
E16

VSS20 D9
VSS18 D11
VSS19 D14
VSS25 R23
VSS29 U23
VSS210 W23
GND

VSS21 L10
VSS22 L11
VSS23 L12
VSS24 M10
VSS25 M11
VSS26 M12
VSS27 N10
VSS28 N11
VSS29 N12
VSS30 N13
VSS31 N14
VSS32 N15
VSS33 N16
VSS34 P10
VSS35 P11
VSS36 P12
VSS37 P13
VSS38 P14
VSS39 R10
VSS40 R11
VSS41 R12
VSS42 R13
VSS43 R14
VSS44 T10
VSS47 T13
VSS48 T14
VSS49 U10
VSS52 U13
VSS53 U14
VSS54 U15

VSSZ1 P15
VSSZ2 P16
VSSZ3 R15
VSSZ4 R16
VSSZ6 T15
VSSZ7 T16
VSSZ8 U16

USBVSS20 F25
USBVSS21 F26
USBVSS22 G23
USBVSS23 G24
USBVSS24 H25
USBVSS25 H26
USBVSS26 J23
USBVSS27 J24
USBVSS4 A23
USBVSS8 B23
USBVSS12 C22
USBVSS16 D22
USBVSS3 A21
USBVSS7 B21
USBVSS19 E21
USBVSS11 C20
USBVSS15 D20
USBVSS2 A19
USBVSS6 B19
USBVSS18 E19
USBVSS10 C18
USBVSS14 D18
USBVSS1 A17
USBVSS5 B17
USBVSS17 E17
USBVSS9 C16
USBVSS13 D16

USBVSS28 L13
USBVSS29 L14
USBVSS30 L15
USBVSS31 L16
USBVSS32 M13
USBVSS33 M14
USBVSS34 M15
USBVSS35 M16

VSS7 AD10
VSS4 AC10
VSS17 AF9
VSS14 AE9
VSS3 AB9
VSS11 AD8
VSS6 AC8
VSS2 AB8
VSS16 AE7
VSS13 AE7
VSS1 AB7
VSS10 AD6
VSS5 AC6
VSS15 AF5
VSS12 AE5
VSS45 T11
VSS46 T12
VSS50 U11
VSS51 U12
GND

ASUSTek COMPUTER INC.

Title : SIS964L-3

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 18 of 64

Main Clock Generator

CLK33 GROUP:
In L3
Breakout:
Group Space >= 25 mils
Length Match: same as CLK66

CLK66 GROUP:
In L3
Breakout:
(<=0.3")
Group Space >= 25 mils
Length Match: +/- 100 mils

Check A6G RD BOM

ECERA 20PF/30PPM (TYPE GF)

Damping Resistors
Place near to the Clock Outputs.

+3.3VS, L36 120Ohm/100Mhz, 350mA MAX, VCC3_CLKGN

C343 10uF/10V
C336 0.1U, C335 0.1U, C334 0.1U, C333 0.1U, C357 0.1U, C356 0.1U, C360 0.1U, C359 0.1U

CLK_X1 <=0.5" C352 22P — X2 14.318Mhz — <=0.5" C344 22P

U12 ICS953805

1	VDDREF	VDDCPU	56
2	FS0/REF0	CPUCLKT	55
3	FS1/REF1	CPUCLKC	54
4	PD#/CLKSTOP#	GNDCPU	53
5	GNDREF	VDDA	52
6	X1	NBCLKT	51
7	X2	NBCLKC	50
8	GNDZ	GNDA	49
9	ZCLK0	IREF	48
10	ZCLK1	VDDSRC	47
11	VDDZ	SRCCLKT	46
12	VDDPCI1	SRCCLKC	45
13	(Reset_IN#)/Reset#	GNDSRC	44
14	PCICLK0	SCLK	43
15	PCICLK1	PCIEXT0	42
16	(PECLKREQ#)/PCICLK2	PCIEXC0	41
17	Mode/PCICLK3	VDDPCIEX2	40
18	GNDPCI1	PCIEXT1	39
19	VDDPCI2	PCIEXC1	38
20	(CPU_STOP#)PCICLK4	GNDPCIEX	37
21	FS2/PCICLK5	PCIEXT2	36
22	FS3/PCICLK6	PCIEXC2	35
23	PCICLK7	VDDPCIEX1	34
24	GNDPCI2	PCIEXT3_F	33
25	VDD48	PCIEXC3_F	32
26	12_48MHz/SEL12#_48MHz	PCIEXT4_F	31
27	24_48MHz/SEL24_48#MHz	PCIEXC4_F	30
28	GND48	SDATA	29

VCC3_CLKGN_AVDD

17 CLK_14_SB, 28 CLK_14_SIO — CLK_14_SB, CLK_14_SIO — 33Ohm 22Ohm — R204 R205 — FS0 FS1 MGN_PD#

CLK_X1, CLK_X2

10 CLK_ZIP_NB, 16 CLK_ZIP_SB — CLK_ZIP_NB, CLK_ZIP_SB — 22Ohm — R206 R207 — MGN_ZCLK0 MGN_ZCLK1

UNMOUNT

39 ICS_RESET#, 16 CLK_PCI_SB, 22 CLK_PCI_CB — 0Ohm /X, 33Ohm — R208 R209 R210 — CG_RESET# CLK_PCI0 CLK_PCI1 CLK_LANPCI MODE

21 CLK_MINIPCI — CLK_MINIPCI 33Ohm R211

20 CLK_LAN_PCI — CLK_LAN_PCI 10Ohm R213 — MGN_CPUSTOP#

28 CLK_PCI_SIO, 27 CLK_PCI_KBC, 28 CLK_PCI_BIOS — 10Ohm, 33Ohm — R212 R214 R215 — FS2 FS3 CLK_PCI6

Watch out length mismatch!

BIOS need to disable PIN 26,27,SRCCLK, PCIE2-4

MGN_CPU0T R176 15Ohm — CPUCLK 4, CPUCLK# 4
MGN_CPU0C R177 15Ohm
MGN_CPU1T R178 15Ohm — M760CLK_H 9, M760CLK_L 9
MGN_CPU1C R179 15Ohm
IREF
CLKPE0 R174 33Ohm — SM_CLK 6,13,17, PEX_CLK0 9
CLKPE0# R175 33Ohm — PEX_CLK0# 9
CLKPE1 R180 33Ohm — PEX_CLK1 42
CLKPE1# R181 33Ohm — PEX_CLK1# 42
SM_DATA 6,13,17

VCC3_CLKGN
RN18A 10KOhm, RN18B 10KOhm
17 PM_STPCPU# — D19 RB751V_40 — MGN_CPUSTOP#
17,20,22,31,37,39,54,56 PM_SLP_S3# — D18 RB751V_40 — MGN_PD#

10PF/50V C385 /X — CLK_ZIP_NB
10PF/50V C386 /X — CLK_ZIP_SB
UNMOUNT
22PF/50V C384 /X — CLK_14_SIO
22PF/50V C381 /X — CLK_LAN_PCI
22PF/50V C377 /X — CLK_PCI_SB
22PF/50V C378 /X — CLK_PCI_CB
22PF/50V C379 /X — CLK_MINIPCI
22PF/50V C380 /X — CLK_PCI_SIO
22PF/50V C382 /X — CLK_PCI_KBC
22PF/50V C387 /X — CLK_PCI_BIOS

IREF — R164 475Ohm 1%

UNMOUNT
22PF/50V C383 /X — CLK_14_SB

49.9Ohm R166 — PEX_CLK0
49.9Ohm R167 — PEX_CLK0#
49.9Ohm R168 — PEX_CLK1
49.9Ohm R169 — PEX_CLK1#

VCC3_CLKGN, VCC3_CLKGN_AVDD
L35 120Ohm/100Mhz
C318 10uF/10V, C327 0.1U, C337 0.01UF/16V

Near CLK-Gen's Pin 52 & 49.

C339 10uF/10V

Frequency Selection

R510 10KOhm /X, R513 10KOhm /X, R509 10KOhm, R508 10KOhm
FS0 FS1 FS2 FS3
R223 10KOhm, R512 10KOhm, R221 10KOhm /X, R220 10KOhm /X

R507 47KOhm — CLK_LANPCI

R222 10KOhm — CG_RESET#
R511 10KOhm — MODE

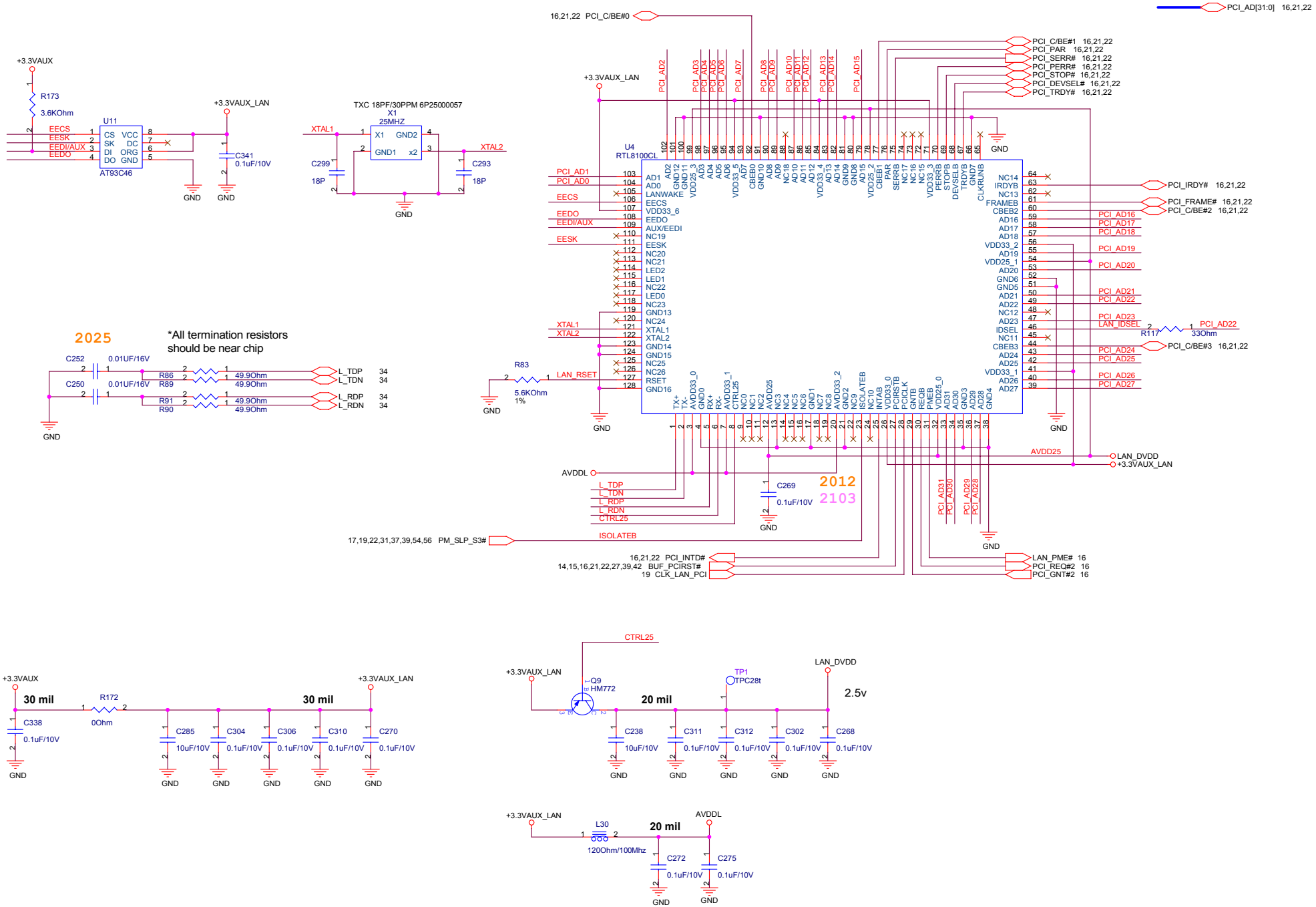
CLK Table for SiS M756 (ICS-953805)

SiS M760 CLOCK

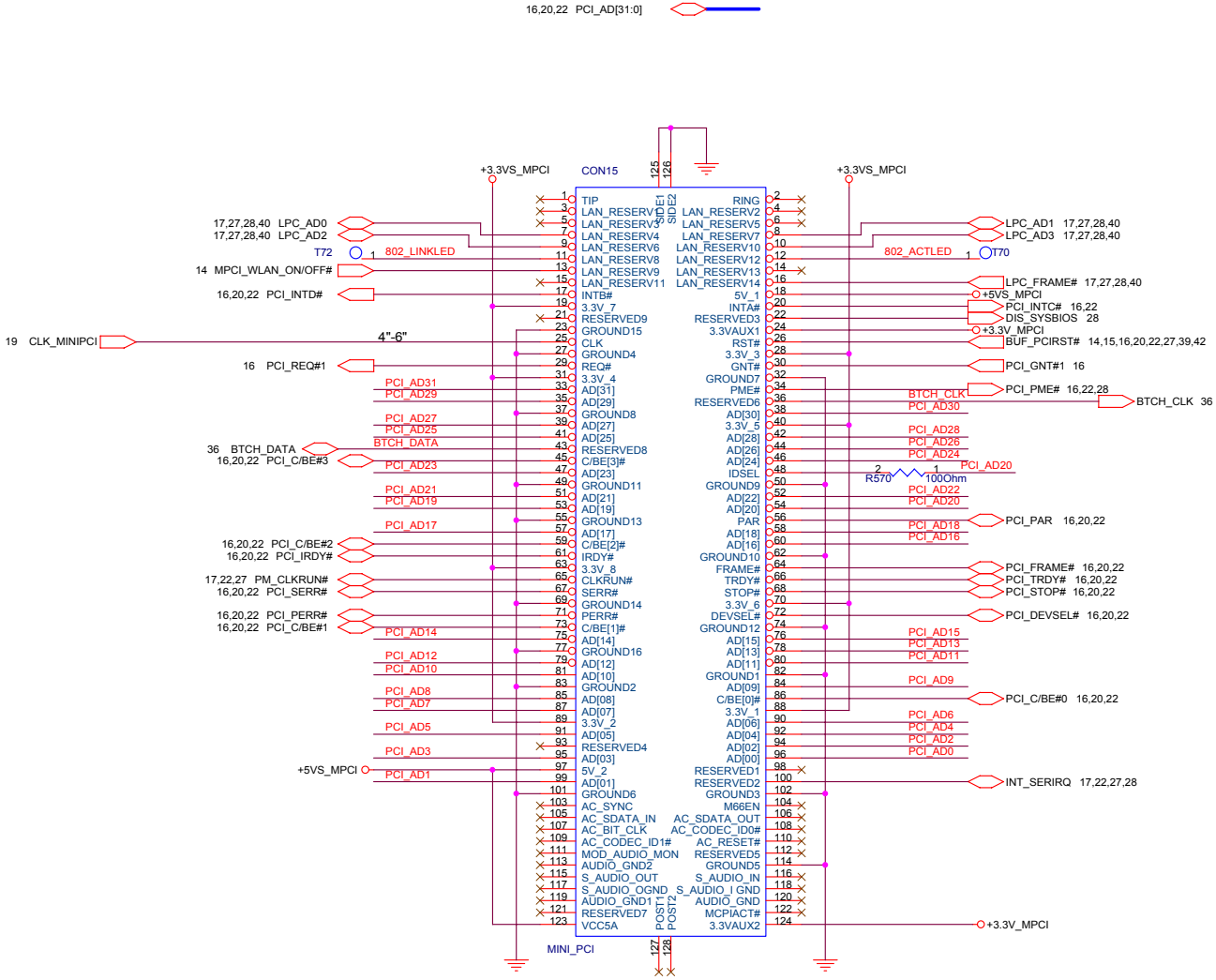
(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	NB CLK (MHz)	ZCLK (MHz)	PCIEX (MHz)	PCI (MHz)	
0	0	0	0	100	100	133.33	100.00	33.33	
0	0	0	1	133.33	133.33	133.33	100.00	33.33	
0	0	1	0	166.66	166.66	133.33	100.00	33.33	
0	**0**	**1**	**1**	**200.00**	**200.00**	**133.33**	**100.00**	**33.33**	***Trap Default***
0	1	0	0	250.00	250.00	133.33	100.00	33.33	
0	1	0	1	266.66	266.66	133.33	100.00	33.33	
0	1	1	0	100.00	125.00	133.33	100.00	33.33	
0	1	1	1	133.33	166.66	133.33	100.00	33.33	
1	0	0	0	166.66	222.22	133.33	100.00	33.33	
1	0	0	1	200.00	250.00	133.33	100.00	33.33	
1	0	1	0	250.00	333.33	133.33	100.00	33.33	
1	0	1	1	266.66	400.00	133.33	100.00	33.33	
1	1	0	0	202.00	202.00	134.66	100.00	33.66	
1	1	0	1	204.00	204.00	136.00	100.00	34.00	
1	1	1	0	206.00	206.00	137.33	100.00	34.33	
1	1	1	1	208.00	208.00	138.66	100.00	34.66	

ASUSTek COMPUTER INC. NB6

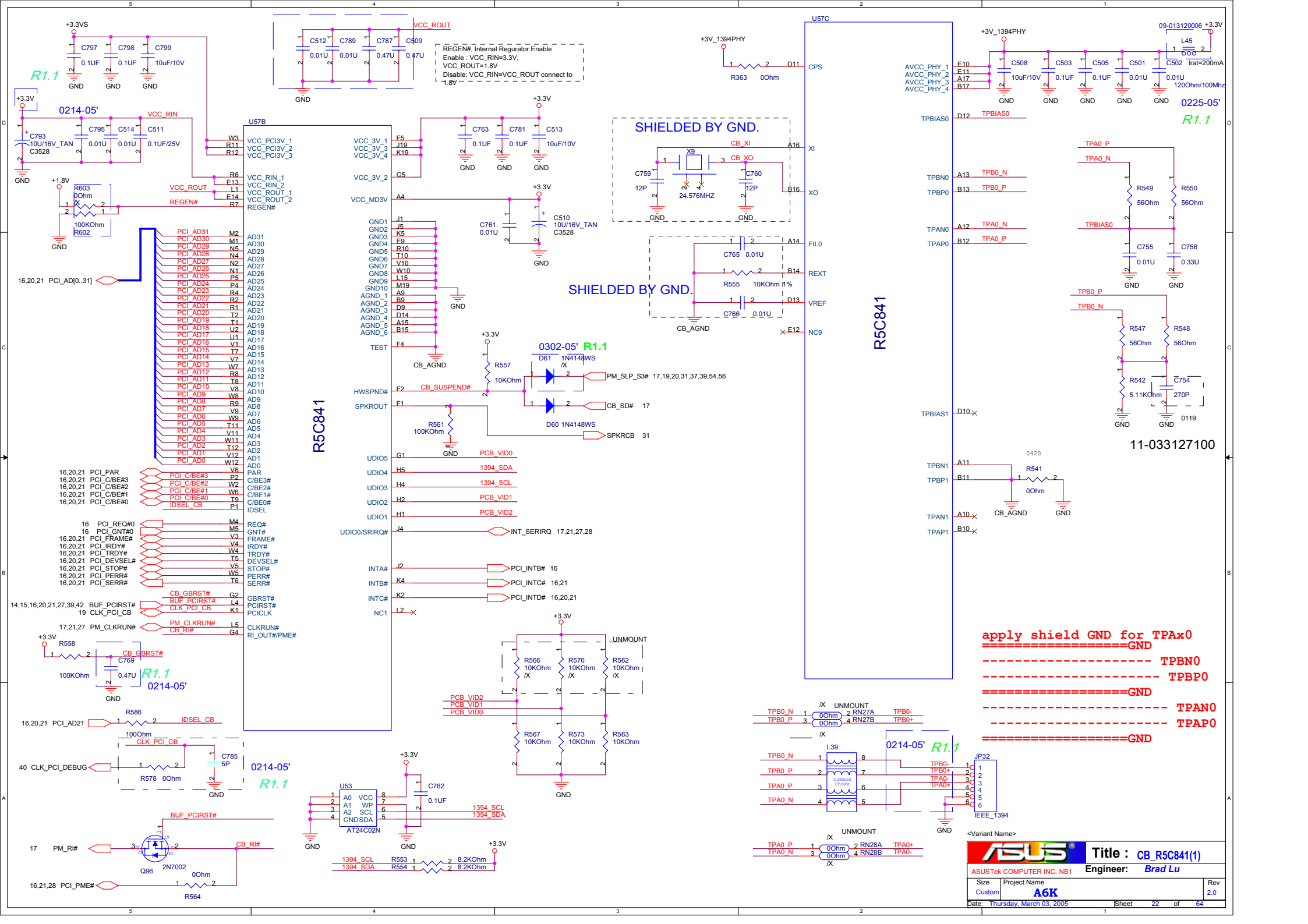
Title : CLOCK-ICS953805
Engineer: Brad Lu
Size: Custom | Project Name: A6K | Rev: 1.0
Date: Thursday, March 03, 2005 | Sheet 19 of 64



ASUSTek COMPUTER INC. NB6	Title : LAN-RTL8100CL	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 20 of 64	



ASUSTek COMPUTER INC. NB6	Title : MINIPCI	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 21 of 64	


U57B
R5C841
U57C
R5C841
REGEN#, Internal Regurator Enable
Enable : VCC_RIN=3.3V,
VCC_ROUT=1.8V
Disable: VCC_RIN=VCC_ROUT connect to 1.8V
SHIELDED BY GND.
SHIELDED BY GND.
0214-05' R1.1
0302-05' R1.1
0225-05' R1.1
0214-05' R1.1
0214-05' R1.1
11-033127100
apply shield GND for TPAx0
GND
TPBN0
TPBP0
GND
TPAN0
TPAP0
GND
Title : CB_R5C841(1)
ASUSTek COMPUTER INC. NB1
Engineer: Brad Lu
Size: Custom
Project Name: A6K
Rev: 2.0
Date: Thursday, March 03, 2005
Sheet 22 of 64

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

藍色pin腳名稱的訊號
是要經由MUX分離的訊號
以避免841的假的LPC訊號
跟SYSTEM的LPC訊號相衝突

U57A

C1 NC2
D1 NC3
E1 NC4
C2 NC5
D2 NC6
E2 NC7
E4 NC8

CADR25 J18 AD19/A25 24
CADR24 J15 AD17/A24 24
CADR23 K16 CFRAME#/A23 24
CADR22 L16 CTRDY#/A22 24
CADR21 L18 CDEVSEL#/A21 24
CADR20 M16 CSTOP#/A20 24
CADR19 N19 CBLOCK#/A19 24,40
CADR18 N16 C_RFU/A18 40
CADR17 P16 AD16/A17 24
CADR16 L19 R_CCLK/A16_D3
R581 22Ohm
CCLK/A16_D3 24
C780 5P
CADR15 K15 CIRDY#/A15 24
CADR14 N18 C_CPERR#/A14 40
CADR13 N15 CPAR/A13 24
CADR12 K18 CBE2#/A12 24
CADR11 R18 AD12/A11 24
CADR10 U19 AD9/A10 24
CADR9 R19 AD14/A9 24
CADR8 P15 CBE1#/A8 24
CADR7 J16 AD18/A7 24
CADR6 H15 AD20/A6 24
CADR5 H18 AD21/A5 24
CADR4 G15 AD22/A4 24
CADR3 G18 AD23/A3 24
CADR2 F15 AD24/A2 24
CADR1 F18 AD25/A1 24
CADR0 E16 AD26/A0 24

CDATA15 U18 AD8/D15 24
CDATA14 W18 C_RFU/D14 40
CDATA13 V17 AD6/D13 24
CDATA12 V16 AD4/D12 24
CDATA11 V15 AD2/D11 24
CDATA10 B19 AD31/D10 24
CDATA9 C18 AD30/D9 24
CDATA8 D18 AD28/D8 24
CDATA7 W17 AD7/D7 24
CDATA6 W16 AD5/D6 24
CDATA5 W15 AD3/D5 24
CDATA4 T15 AD1/D4 24
CDATA3 R14 AD0/D3 24
CDATA2 C19 C_RFU/D2 40
CDATA1 D19 AD29/D1 24
CDATA0 E19 AD27/D0 24

+VCCCB
R556 100KOhm

E8 MDIO19
D8 MDIO18
B8 MDIO17
A8 MDIO16
E7 MDIO15
D7 MDIO14
B7 MDIO13
A7 MDIO12
E6 MDIO11
D6 MDIO10
B6 MDIO09
A6 MDIO08
D5 MDIO07
B5 MDIO06
A5 MDIO05
B4 MDIO04
B3 MDIO03
A3 MDIO02
A2 MDIO01
B1 MDIO00

SD_D3/MSCD3
SD_D2/MSCD2
SD_D1/MSCD1
SD_D0/MSCD0
SD/MS_CLK [2] R551 0Ohm
SD_CMD/MS_BS
GND R552 0Ohm

OE# T19 AD11/OE# 24
WE# M15 CGNT#/WE# 24
CE2# T18 AD10/CE2# 24
CE1# V19 CBE0#/CE1# 24
REG# F16 CBE3#/REG# 24
RESET H19 CRST#/RESET 24
WAIT# G16 C_CSERR#/WAIT# 40
WP/IOIS16# A18 C_CCLKRUN#/IOIS16# 40
RDY/IREQ# M18 CINT#/IREQ# 24
BVD2 F19 C_CAUDIO/SPKR_IN#/BVD2 40
BVD1 E18 C_STSCHG/STSCHG#/BVD1 40
VS2# H16 CVS2 24
VS1# R16 CVS1 24
CD2# D15 CCD2# 24
CD1# T14 CCD1# 24,40
INPACK# G19 CREQ#/INPACK# 24

IORD# P18 AD13/IORD# 24
IOWR# P19 AD15/IOWR# 24

USBDP V14
USBDM W14

+3.3V
R599 100KOhm

VPPEN1 W13 VPP_EN1 24
VPPEN0 V13 VPP_EN0 24
VCC3EN# T13 VCC3_EN# 24
VCC5EN# R13 VCC5_EN# 24

R5C841

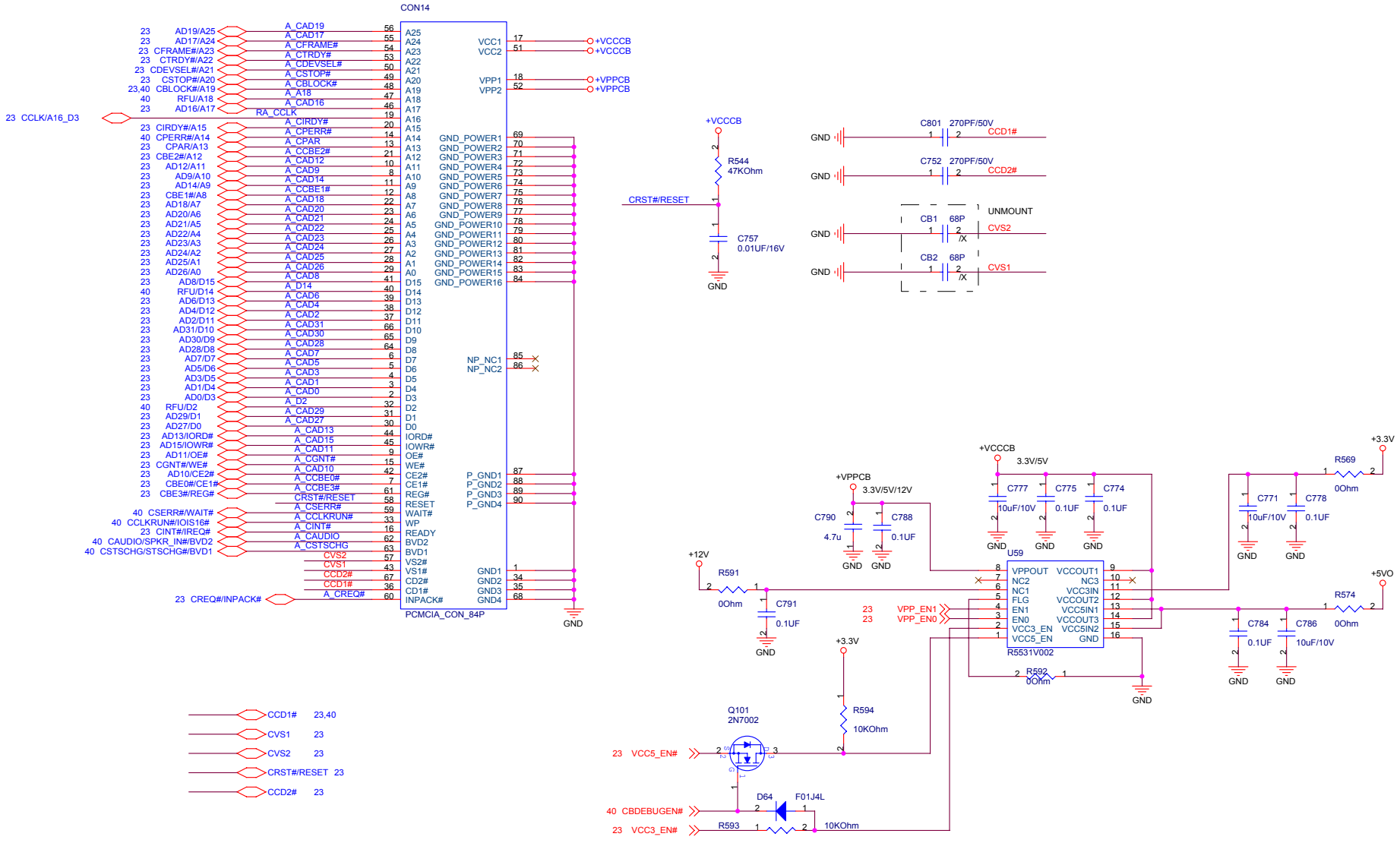
+3.3V
Q98 SI2301DS
+3.3V_MC_VCC
C782 0.1UF
C783 0.1UF
GND
+12V
R579 100KOhm
Q99
SD/MS_PWR_EN#
R-1 47K
R-2 47K
PDTC144EK
GND

SD_WP#
SD_CD#
+3.3V_MC_VCC
GND
CON6
SD_D1/MSCD1
SD_D0/MSCD0
SD/MS_CLK
SD_CMD/MS_BS
SD_D3/MSCD3
SD_D2/MSCD2
SD_DAT1
SD_DAT0
SD_VSS1
SD_CLK
SD_VCC
SD_VSS2
SD_CMD
SD_DAT3
SD_DAT2
SD_WP_PROTECT
SD_CD_DETECT
NP_NC1
MS_VSS1
MS_BS
MS_VCC1
MS_SDIO
MS_RESERVED1
MS_INS
MS_RESERVED2
MS_SCLK
MS_VCC2
MS_VSS2
NP_NC2
SD_CMD/MS_BS
SD_D1/MSCD1
SD_D0/MSCD0
SD_D2/MSCD2
MS_CD#
SD_D3/MSCD3
SD/MS_CLK
C767 5P /X
UNMOUNT
SD_CARD_19P
GND

<Variant Name>

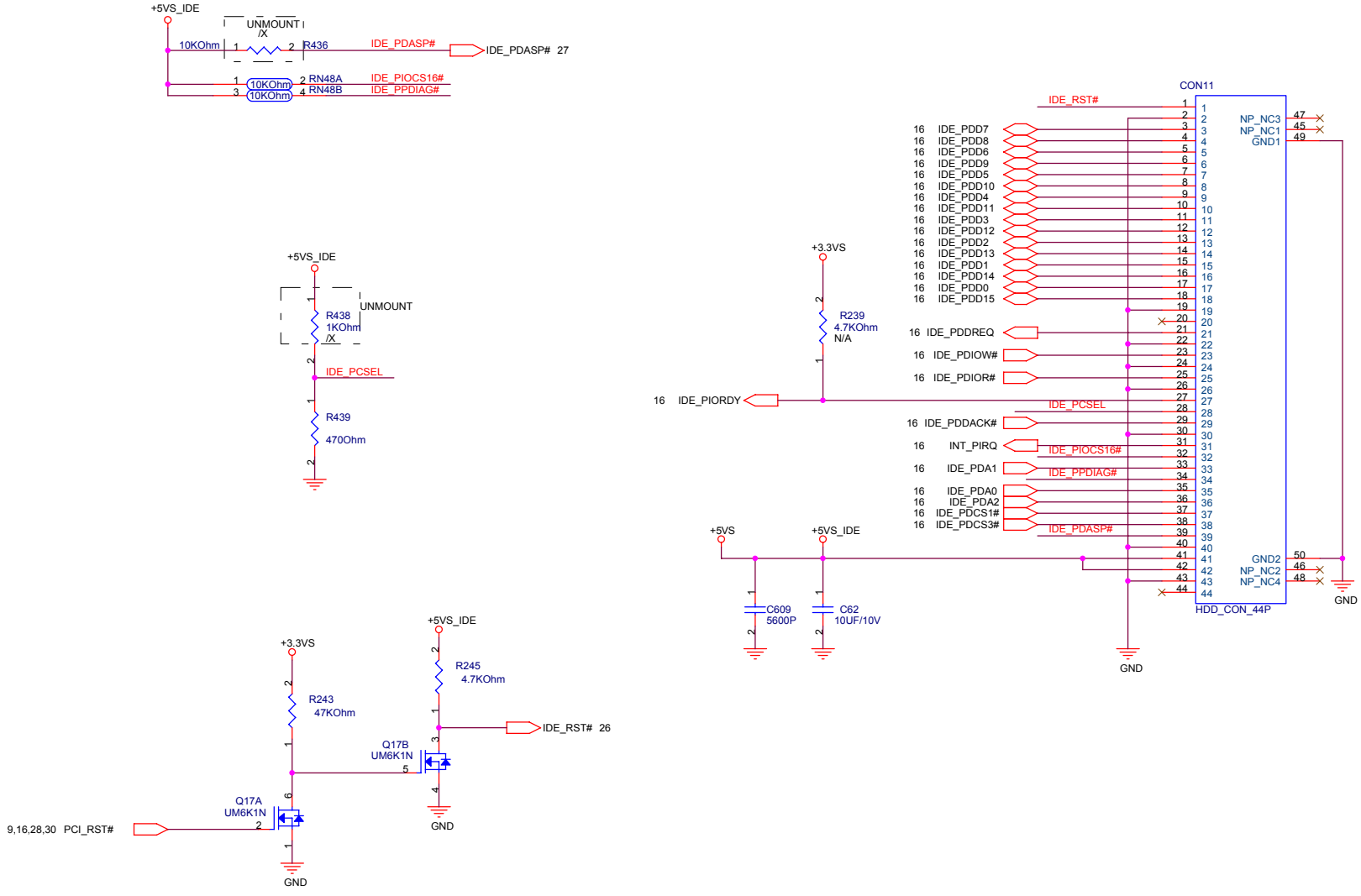
ASUSTek COMPUTER INC. NB1	Title : CB_R5C841 (2)	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Thursday, March 03, 2005	Sheet 23 of 64	

PCMCIA SOCKET

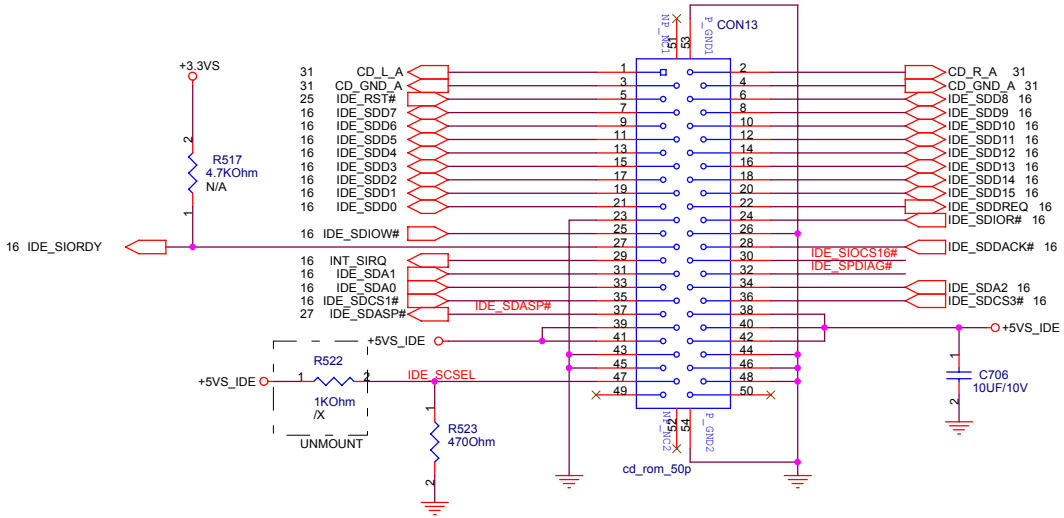


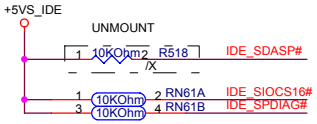
<Variant Name>

ASUSTek COMPUTER INC. NB1	Title : PCMCIA	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 2.0
Date: Thursday, March 03, 2005	Sheet 24 of 64	



ASUSTek COMPUTER INC. NB6	Title : HDD Connector	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6X	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 25 of 64	





ASUSTek COMPUTER INC. NB6	Title : ODD Connector	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6X	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 26 of 64	

P23,P43 excahnged by BIOS's request

Daisy-Chain in layout

S0-S3: (2.5 mA Typ, 7 mA Max.)

LxWxH=14x14x1.7

U22

M38857

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

Audio DJ pin depends on Keyboard Matrix.

Follow M6N

A3N follow M6N Keyboard Matrix

BAT_SEL#:
Hi : 8 Cell
Low: 4 Cell

P21: Power button overwrite disable. Only can be pulled down as default value than can be used as a input.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

4 Cell battery mode:
1.Banias CPU run 600MHz
2.Celeron CPU throttling 50%

OC MEAN OPEN DRAIN

CON4

ZIF_CON_28P

K/B	US	UK	JP
KEYDETECT1	H	L	L
KEYDETECT2	H	H	L

IDE

NUM CAP SCR

R1.1

ASUSTek COMPUTER INC. NB6

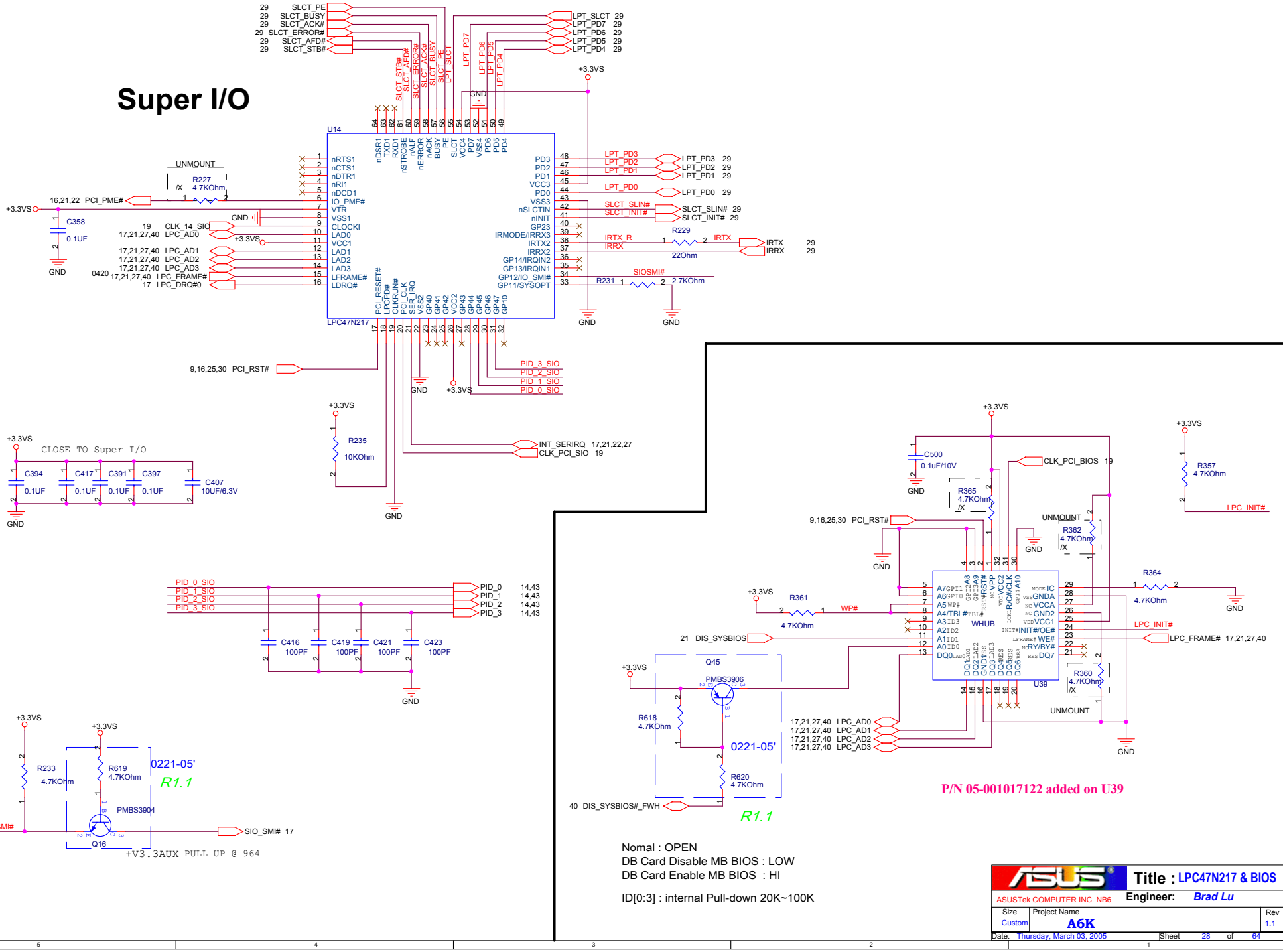
Title : KBC-M38857

Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 27 of 64

Super I/O

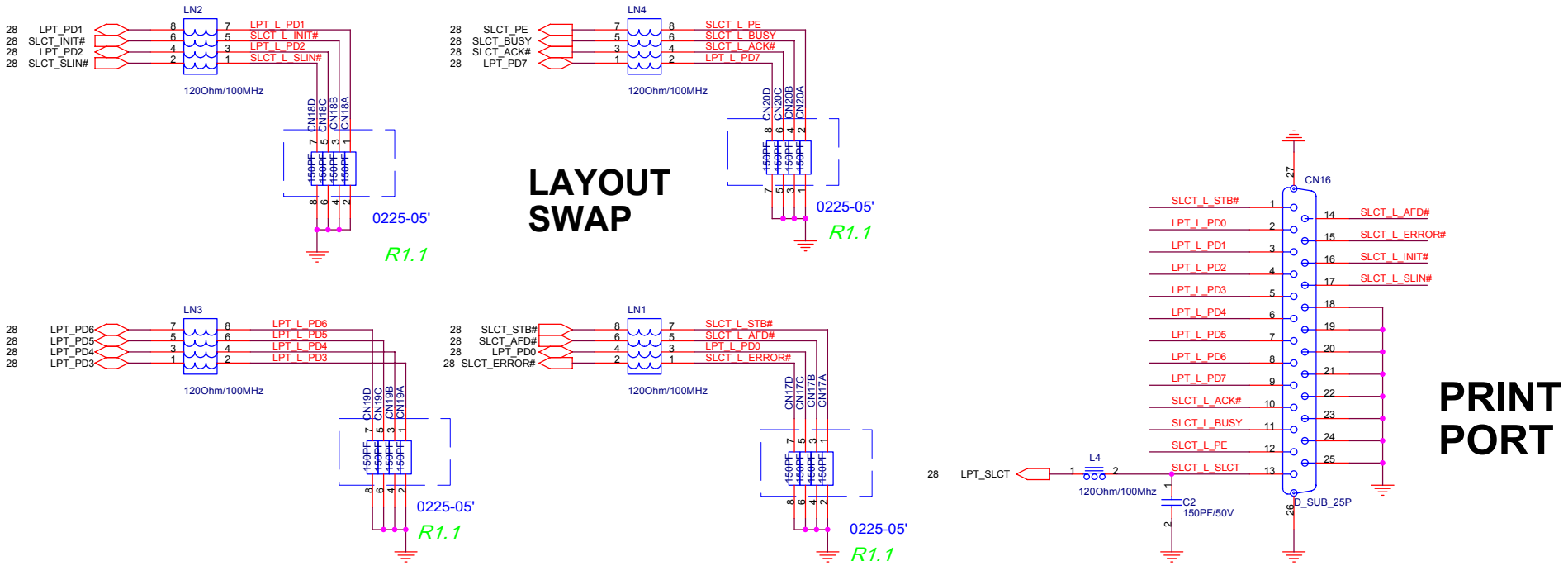


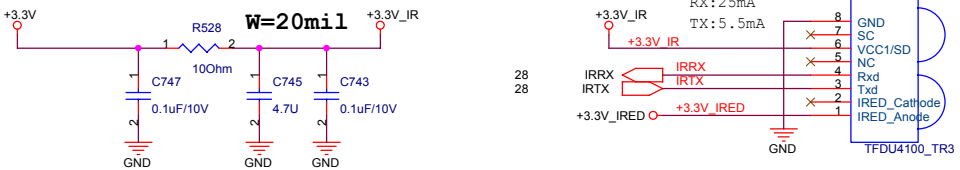
P/N 05-001017122 added on U39

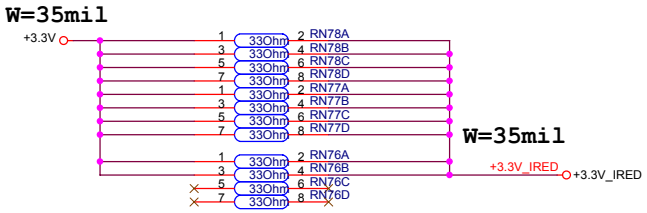
Nomal : OPEN
DB Card Disable MB BIOS : LOW
DB Card Enable MB BIOS : HI

ID[0:3] : internal Pull-down 20K~100K

ASUSTek COMPUTER INC. NB6	Title : LPC47N217 & BIOS	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.1
Date: Thursday, March 03, 2005	Sheet 28 of 64	





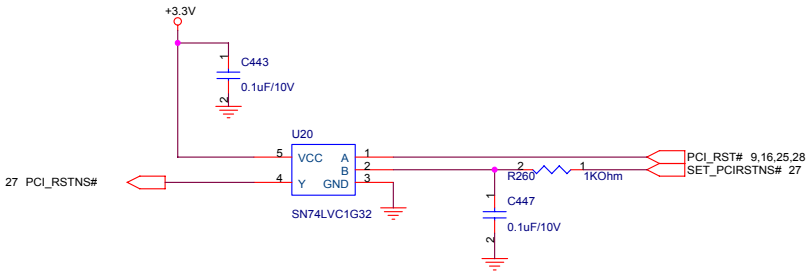


ASUSTek COMPUTER INC. NB6	Title : IR & LPT PORT	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 29 of 64	

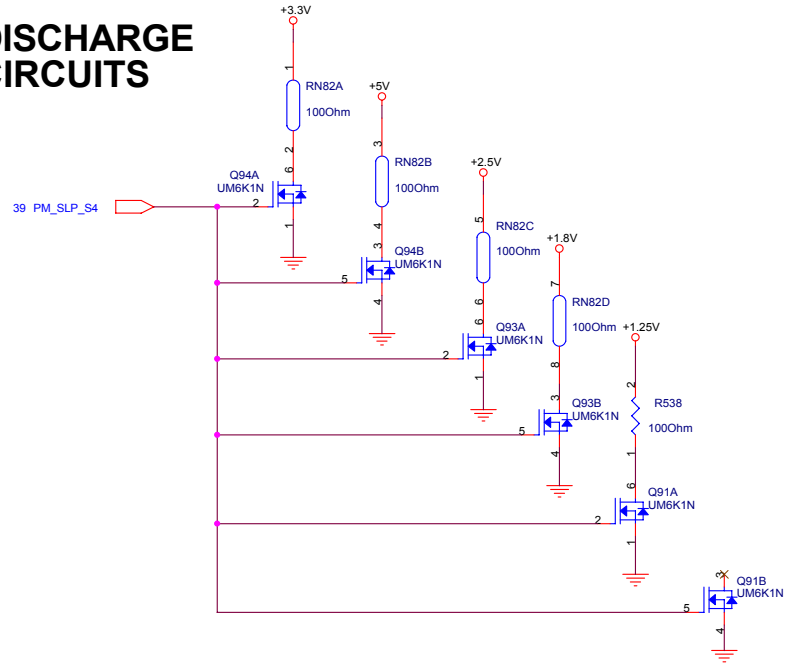
PCMCIA DEBUG Card

1105

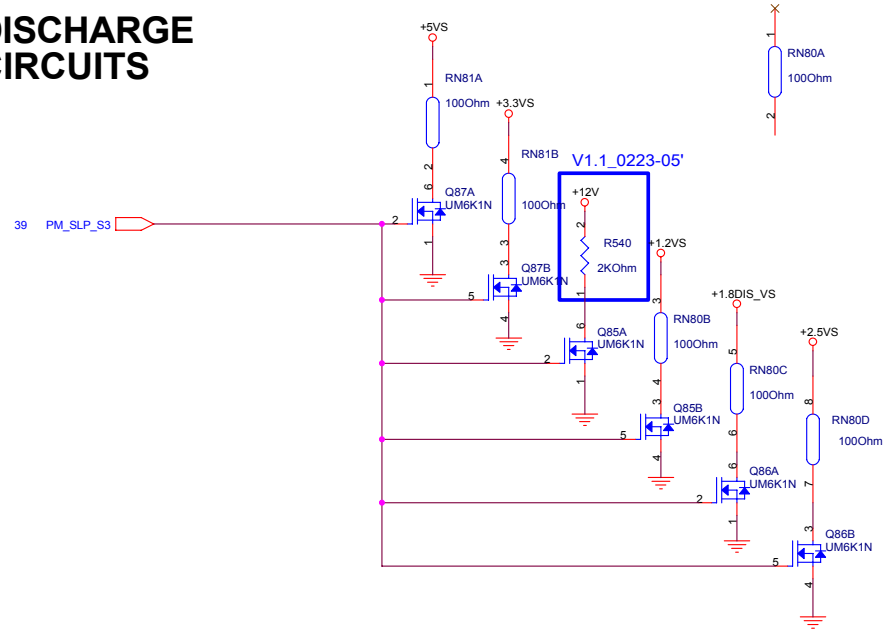
PCI_RSTNS# Gen Circuit



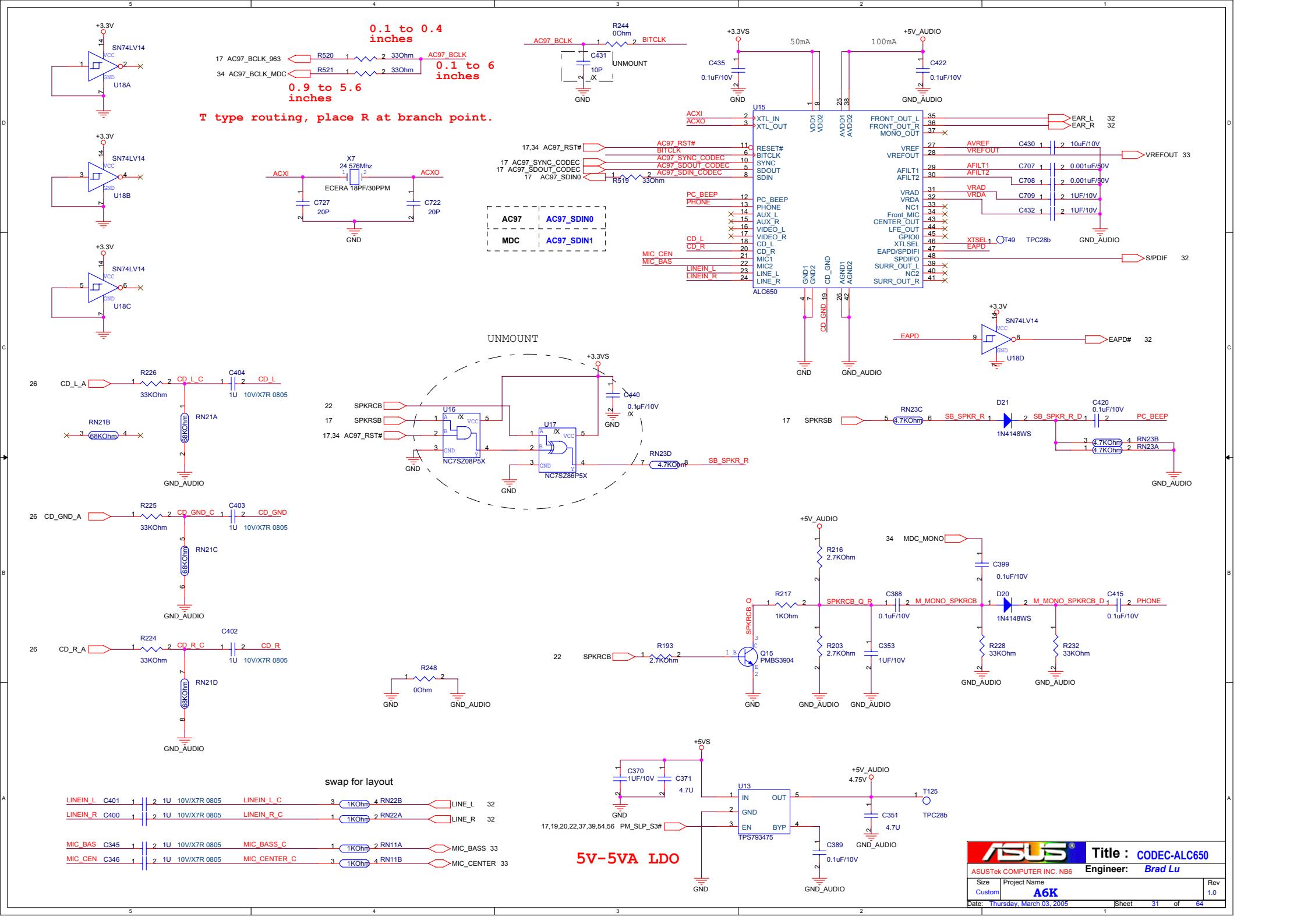
DISCHARGE CIRCUITS

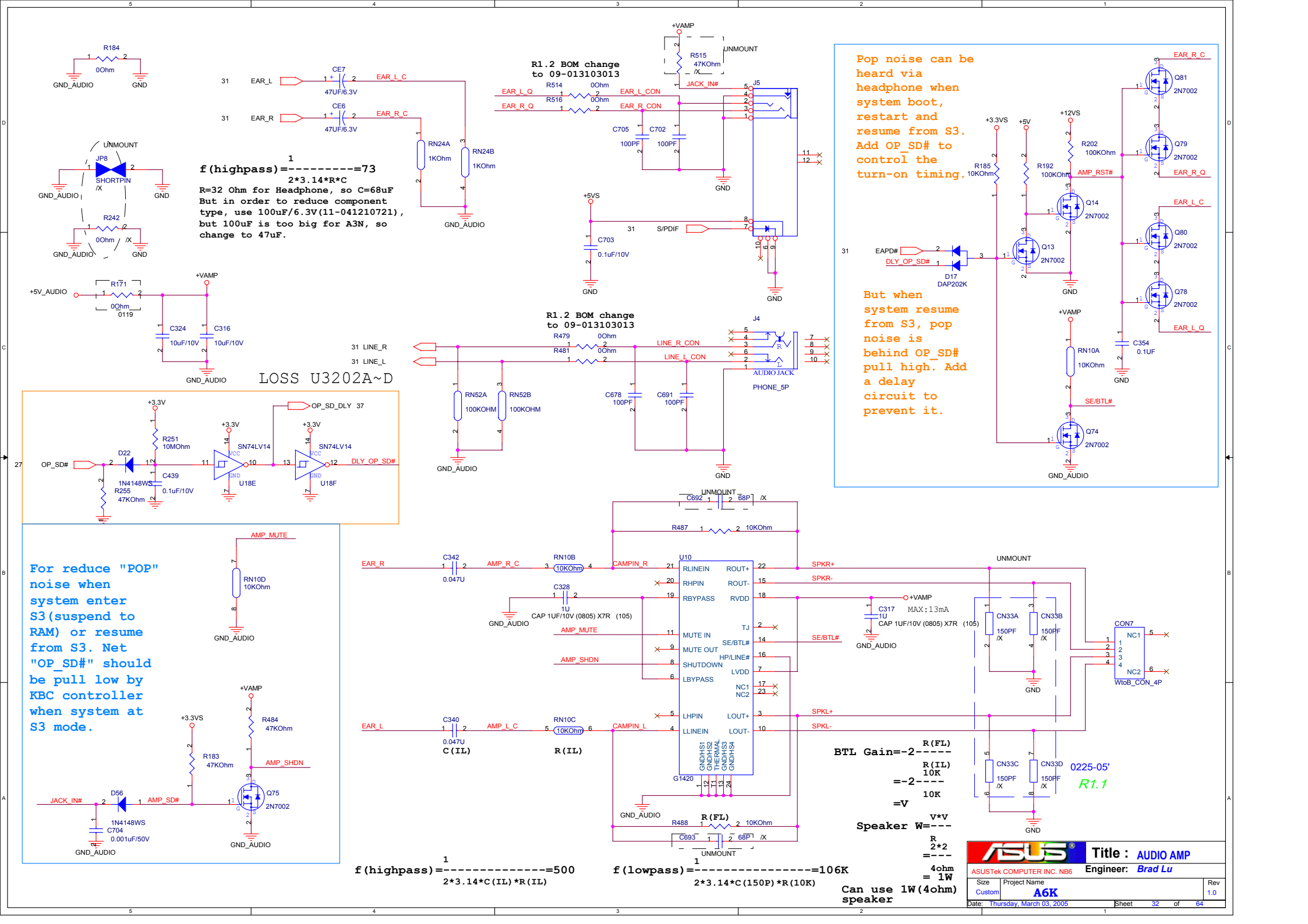


DISCHARGE CIRCUITS



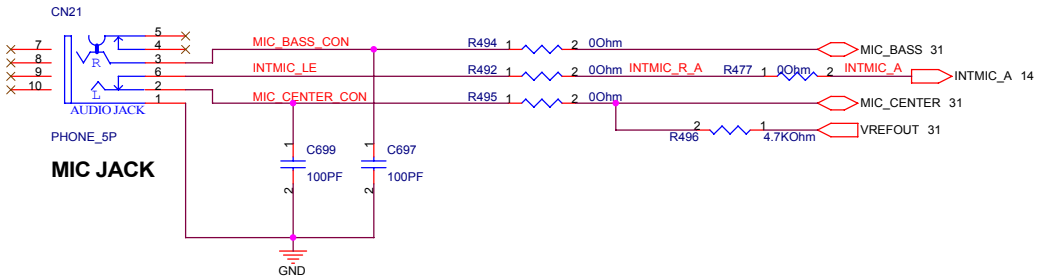
ASUSTek COMPUTER INC. NB6	Title : Discharge circuit	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 30 of 64	

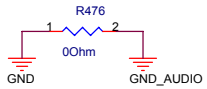

0.1 to 0.4 inches
0.1 to 6 inches
0.9 to 5.6 inches
T type routing, place R at branch point.
UNMOUNT
swap for layout
5V-5VA LDO
ALC650
SN74LV14
U18A
U18B
U18C
U18D
U15
U16
U17
U13
Q15 PMBS3904
TPS793475
NC7SZ08P5X
NC7SZ86P5X
1N4148WS
ECERA 18PF/30PPM
AC97 SDIN0
MDC AC97_SDIN1
Title : CODEC-ALC650
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Project Name A6K
Date: Thursday, March 03, 2005
Sheet 31 of 64

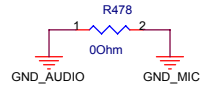

R184
0Ohm
GND_AUDIO
GND
UNMOUNT
JP8
SHORTPIN
/X
R242
0Ohm
+5V_AUDIO
R171
0Ohm
0119
+VAMP
C324
10uF/10V
C316
10uF/10V
GND_AUDIO
LOSS U3202A~D
31 EAR_L
31 EAR_R
CE7
CE6
47UF/6.3V
EAR_L_C
EAR_R_C
RN24A
RN24B
1KOhm
f(highpass)=1/(2*3.14*R*C)=73
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
R1.2 BOM change to 09-013103013
+VAMP
R515
47KOhm
/X
UNMOUNT
JACK_IN#
J5
EAR_L_Q
EAR_R_Q
R514
R516
0Ohm
EAR_L_CON
EAR_R_CON
C705
C702
100PF
+5VS
31 S/PDIF
C703
0.1uF/10V
GND
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
+3.3VS
+5V
+12VS
R185
10KOhm
R192
100KOhm
R202
100KOhm
AMP_RST#
EAPD#
DLY_OP_SD#
D17
DAP202K
Q13
Q14
Q74
Q78
Q79
Q80
Q81
2N7002
EAR_R_C
EAR_R_Q
EAR_L_C
EAR_L_Q
C354
0.1UF
RN10A
10KOhm
SE/BTL#
+3.3V
R251
10MOhm
D22
1N4148WS
R255
47KOhm
C439
0.1uF/10V
SN74LV14
U18E
U18F
OP_SD_DLY 37
27 OP_SD#
DLY_OP_SD#
31 LINE_R
31 LINE_L
R1.2 BOM change to 09-013103013
R479
R481
0Ohm
LINE_R_CON
LINE_L_CON
J4
AUDIO JACK
PHONE_5P
RN52A
RN52B
100KOHM
C678
C691
100PF
For reduce "POP" noise when system enter S3(suspend to RAM) or resume from S3. Net "OP_SD#" should be pull low by KBC controller when system at S3 mode.
AMP_MUTE
RN10D
10KOhm
+VAMP
R484
47KOhm
R183
47KOhm
AMP_SHDN
JACK_IN#
D56
AMP_SD#
Q75
2N7002
1N4148WS
C704
0.001uF/50V
C692
68P
R487
10KOhm
EAR_R
C342
0.047U
AMP_R_C
RN10B
CAMPIN_R
U10
RLINEIN
RHPIN
RBYPASS
MUTE IN
MUTE OUT
SHUTDOWN
LBYPASS
LHPIN
LLINEIN
ROUT+
ROUT-
RVDD
TJ
SE/BTL#
HP/LINE#
LVDD
NC1
NC2
LOUT+
LOUT-
SPKR+
SPKR-
SPKL+
SPKL-
C328
1U
CAP 1UF/10V (0805) X7R (105)
C317
MAX:13mA
CN33A
CN33B
CN33C
CN33D
150PF
CON7
WtoB_CON_4P
EAR_L
C340
0.047U
AMP_L_C
RN10C
CAMPIN_L
C(IL)
R(IL)
R(FL)
R488
C693
G1420
BTL Gain=-2-----R(FL)/R(IL)=-2----10K/10K=V
Speaker W=V*V/R=---2*2/4ohm=1W
Can use 1W(4ohm) speaker
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
0225-05'
R1.1
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 32 of 64

MIC OP CIRCUIT

MIC JACK





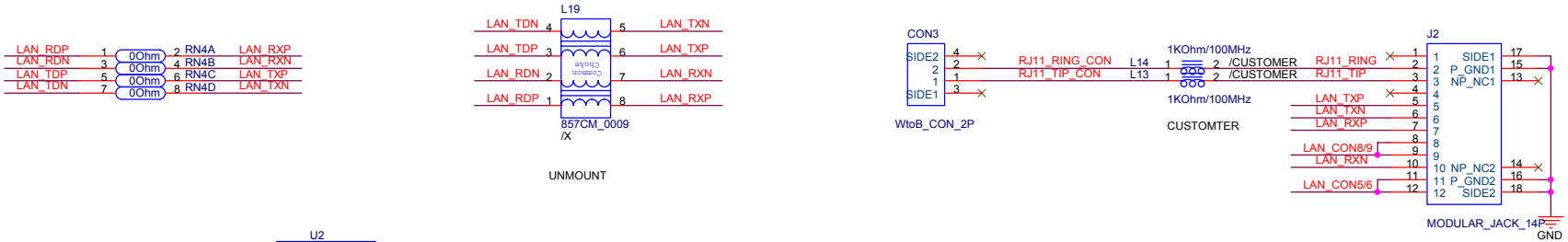


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

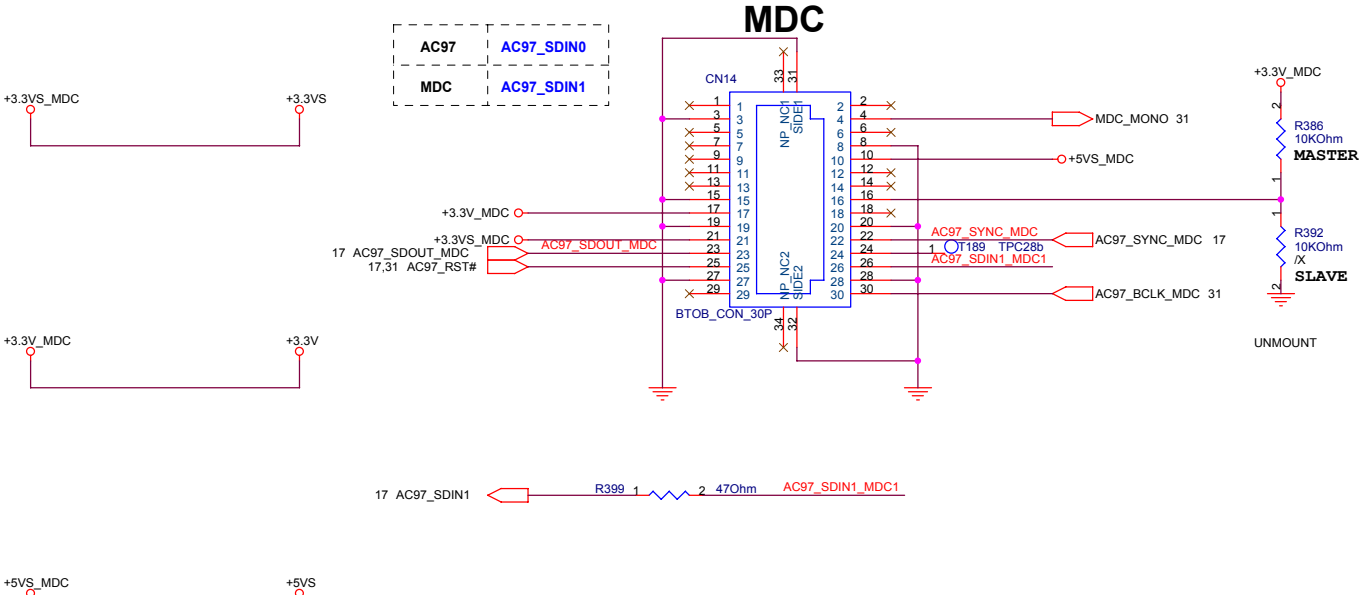
R111 & R112
change to
09-013103013
in R1.2 BOM

ASUSTek COMPUTER INC. NB6	Title : MIC	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 33 of 64	

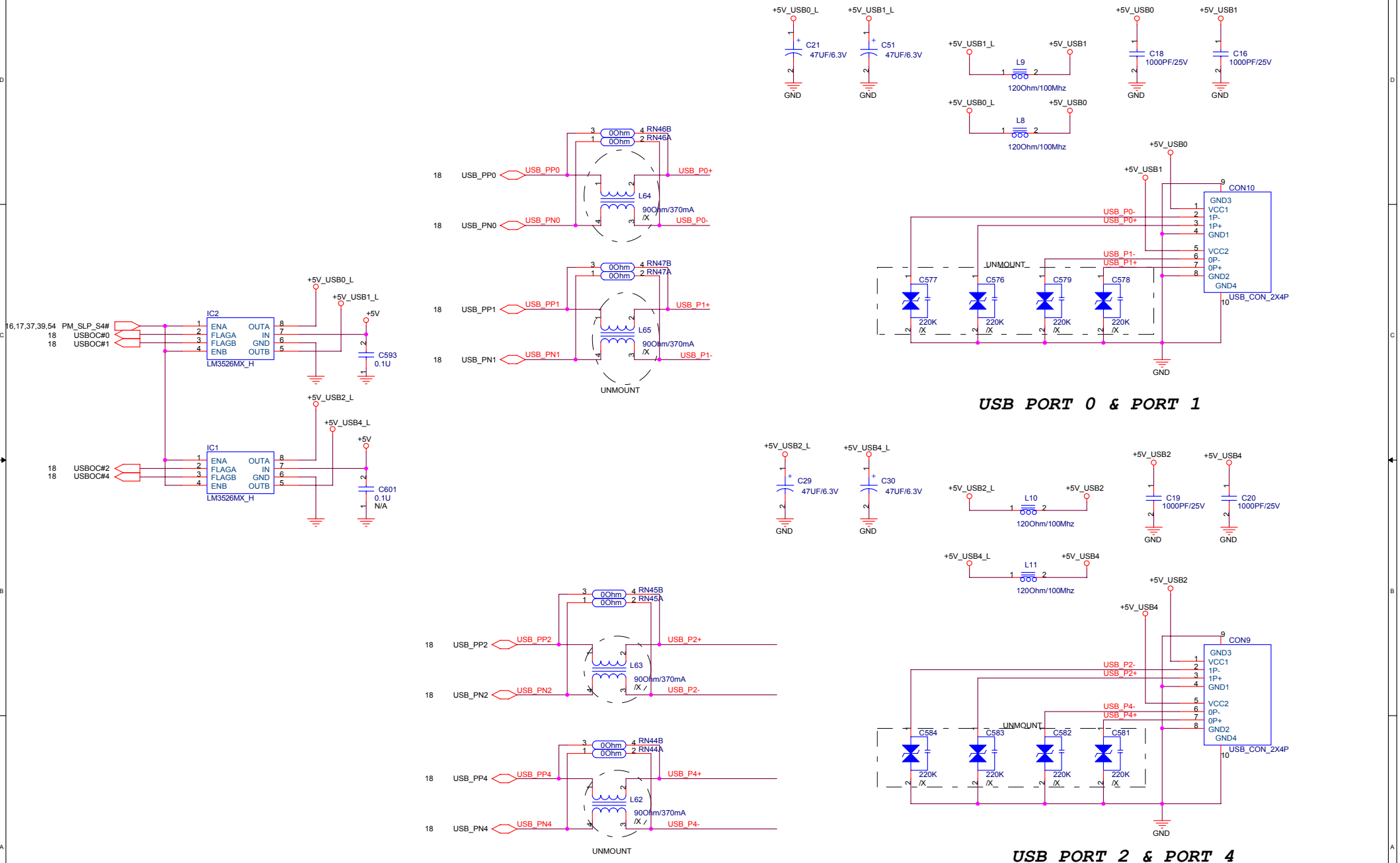
OP: FOR EMI



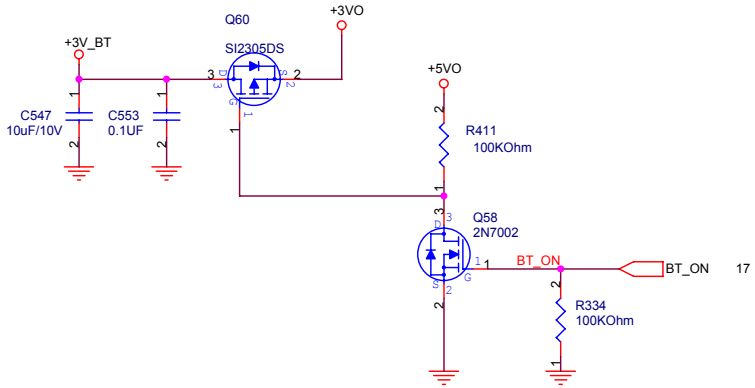
MDC



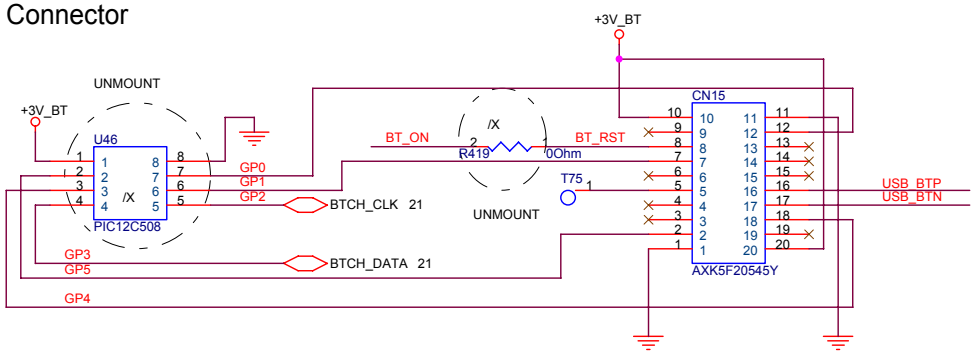
ASUSTek COMPUTER INC. NB6	Title : MDC & RJ45 & RJ11	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 34 of 64	

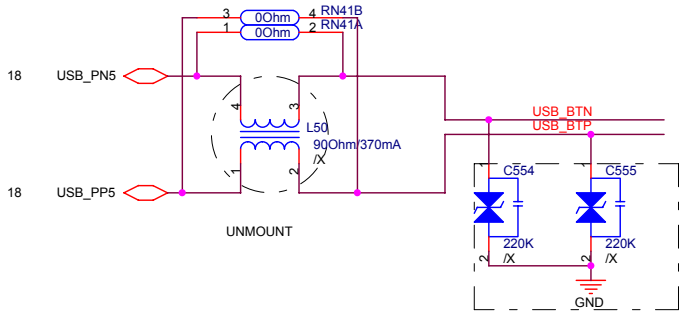


ASUSTek COMPUTER INC. NB6	Title : USB	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 35 of 64	



Bluetooth Module Connector





USB PORT 5 for Bluetooth Module

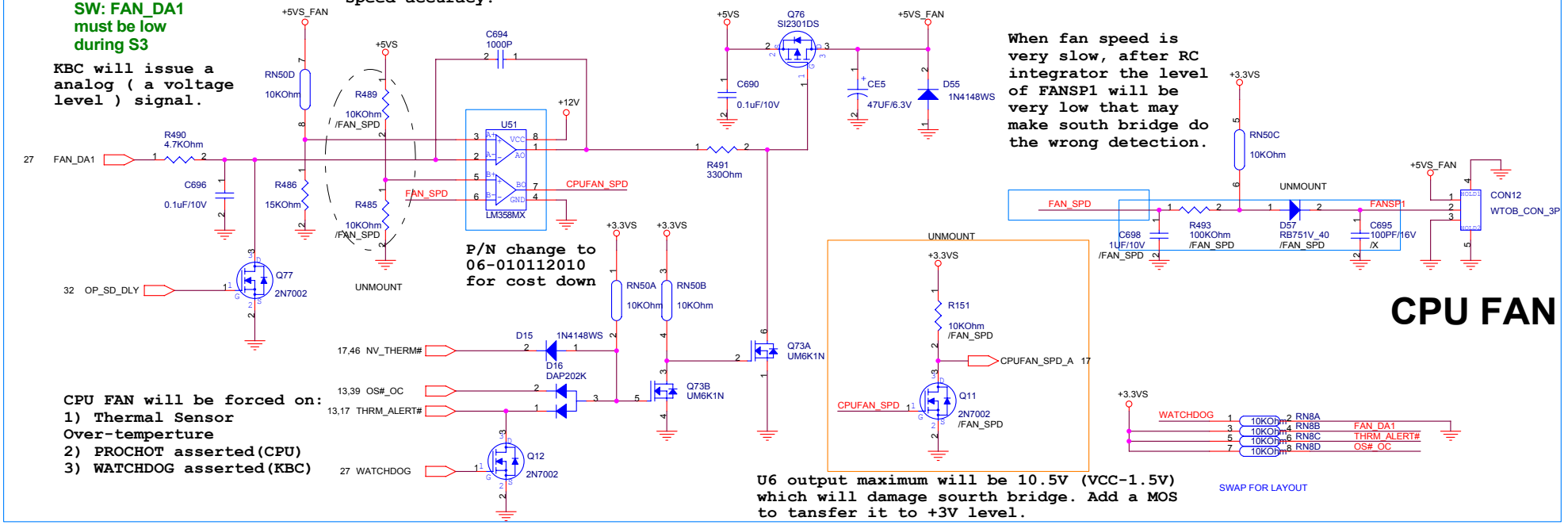
ASUSTek COMPUTER INC. NB6	Title : BT_UGPZ5	
	Engineer: *Bruce Lee*	
Size: B	Project Name: **A6K**	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 36 of 64	

Fan Speed Control

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

SW: FAN_DA1 must be low during S3

KBC will issue a analog (a voltage level) signal.



When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

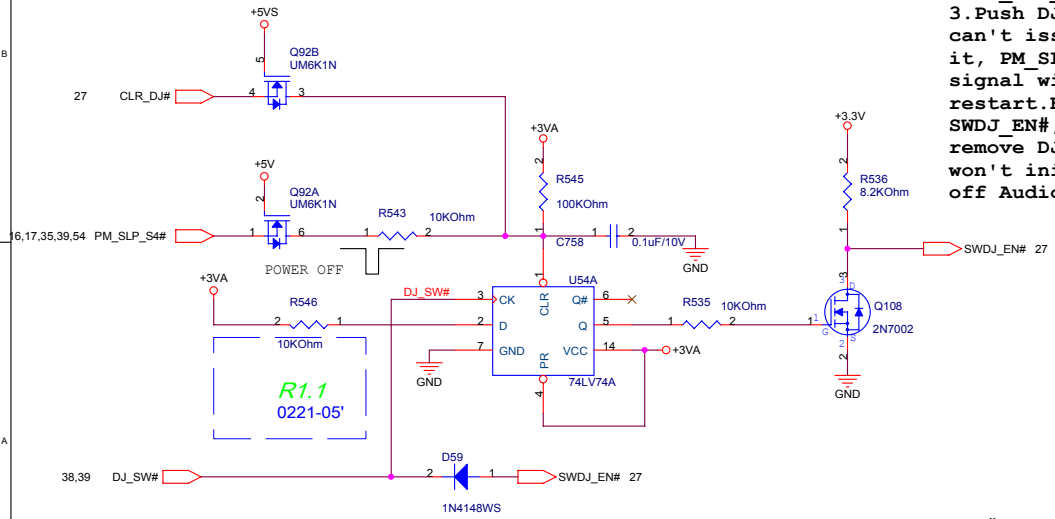
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

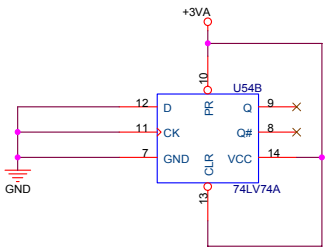
U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

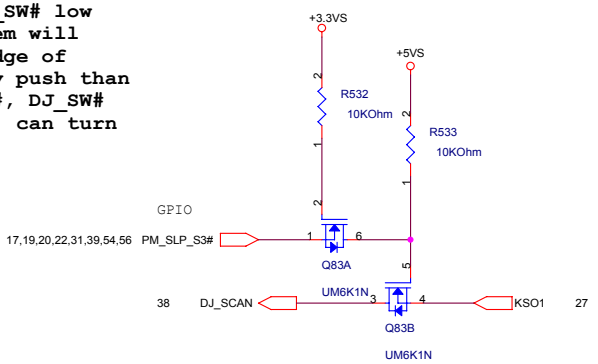
SWAP FOR LAYOUT

Audio DJ

SWDJ_EN# function :
1.Push DJ_SW#, turn on Audio DJ.
2.PM_SLP_S4# will keep high.
3.Push DJ_SW# again, KBC will receive SWDJ_EN#. KBC can't issue SUSC#(PM_SLP_S4#) immediately. If KBC do it, PM_SLP_S4#(page 37) will go low, DJ_SW# low signal will go to PM_PWRBTN#, then system will restart.KBC need trigger the righting edge of SWDJ_EN#, for make sure end user already push than remove DJ Switch button than issue SUSC#, DJ_SW# won't initial low to page37 PM_PWRBTN# , can turn off Audio DJ and won't restart.

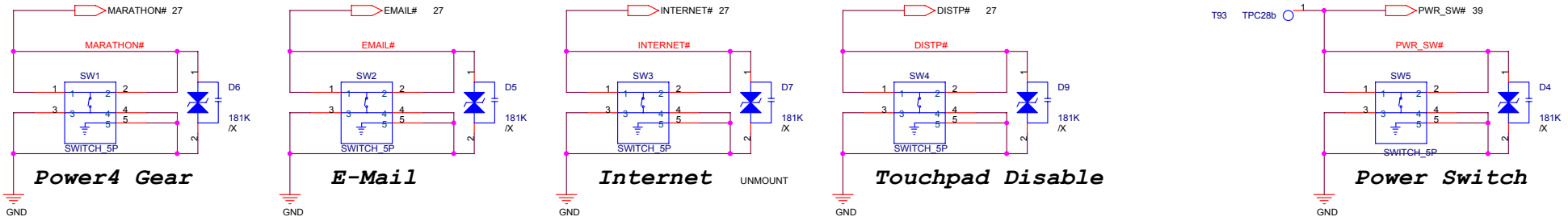


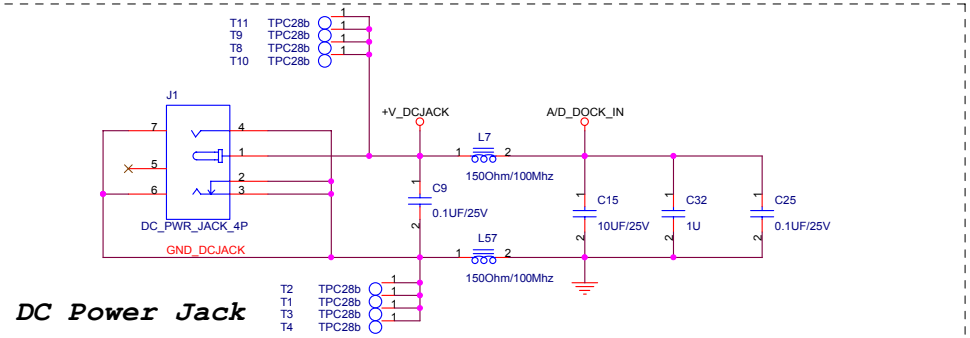


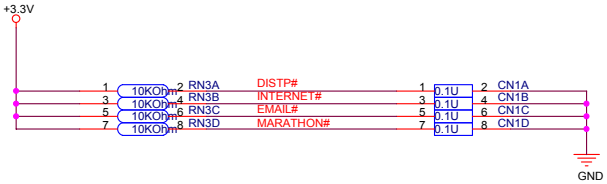


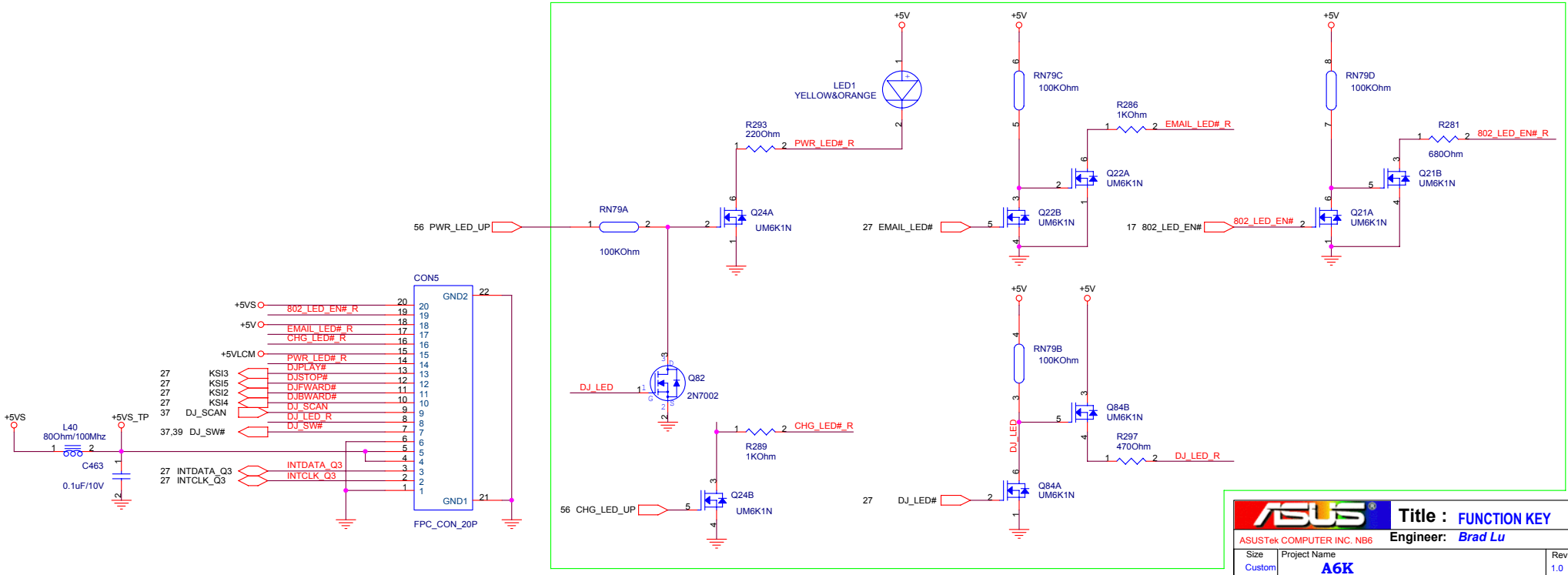
When power on, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D34 to Enable AudioDJ in OS.
Use D34 to Turn off AudioDJ when system be turned on in DJ mode.

ASUSTek COMPUTER INC. NB6	Title : FAN&Audio DJ	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 37 of 64	









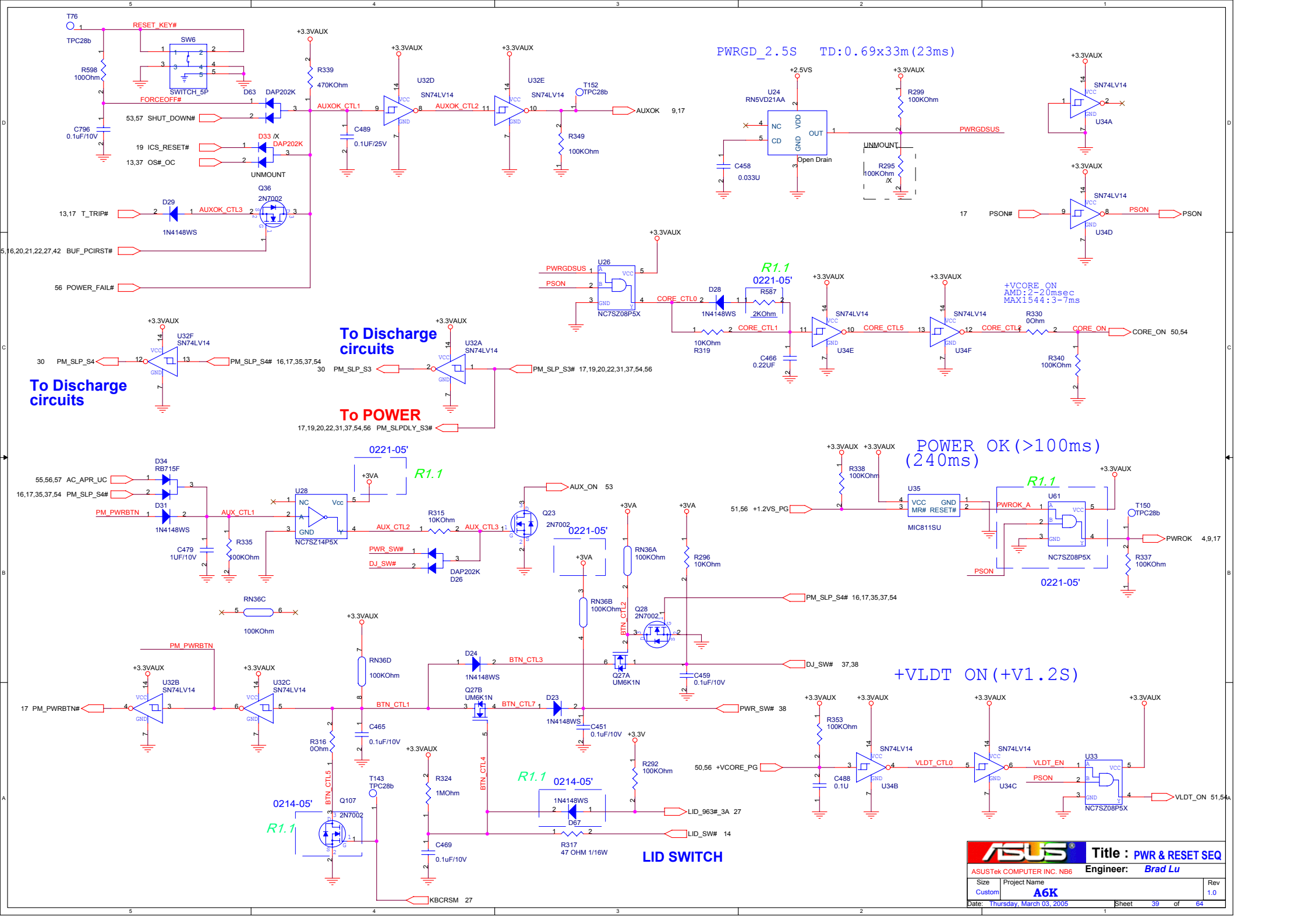
ASUSTek COMPUTER INC. NB6

Title : FUNCTION KEY

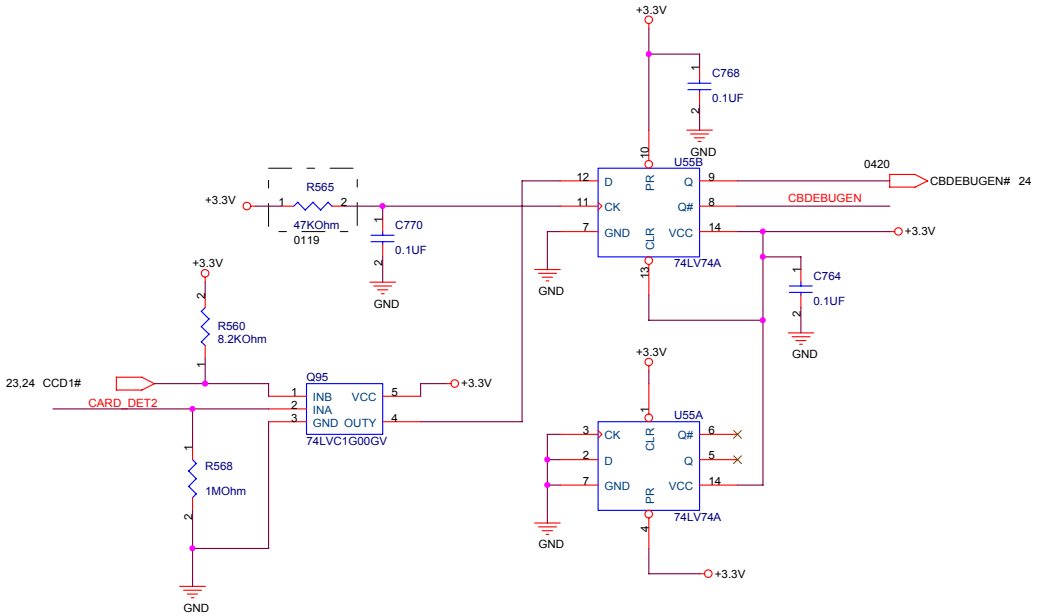
Engineer: Brad Lu

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 38 of 64

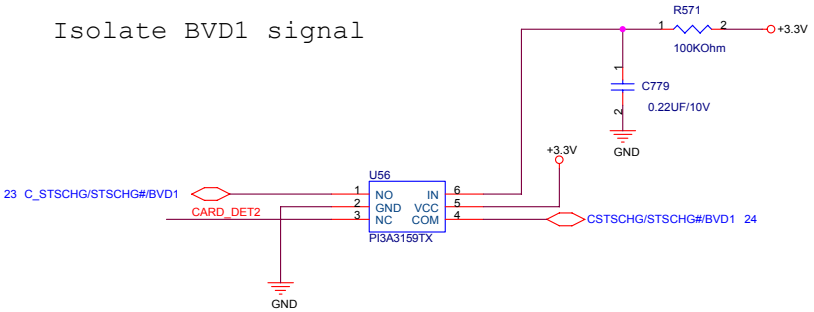

PWRGD_2.5S TD:0.69x33m(23ms)
To Discharge circuits
To Discharge circuits
To POWER
POWER OK(>100ms) (240ms)
+VLDT ON(+V1.2S)
LID SWITCH
+VCORE_ON
AMD:2-20msec
MAX1544:3-7ms
R1.1
0221-05'
0214-05'
Title : PWR & RESET SEQ
ASUSTek COMPUTER INC. NB6
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 39 of 64

PCMCIA DEBUG PORT



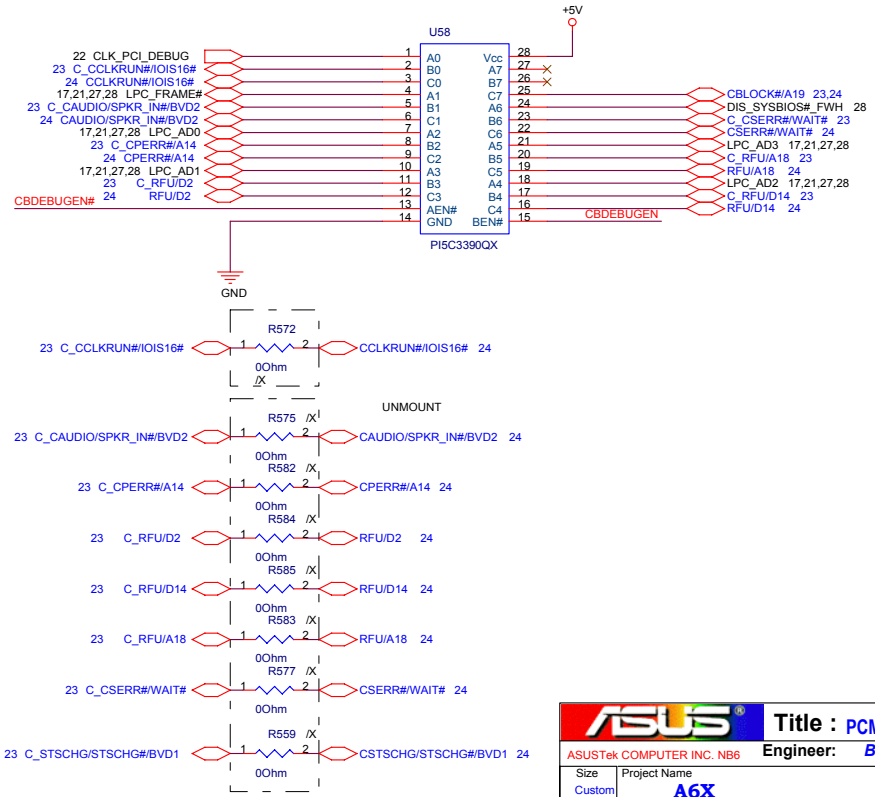
RC value may need to tuned for each product.

Isolate BVD1 signal



When +3V on, select BVD1 to CARD_DET2 for RC delay time

Isolate card bus control and slot signal when debug card plug in



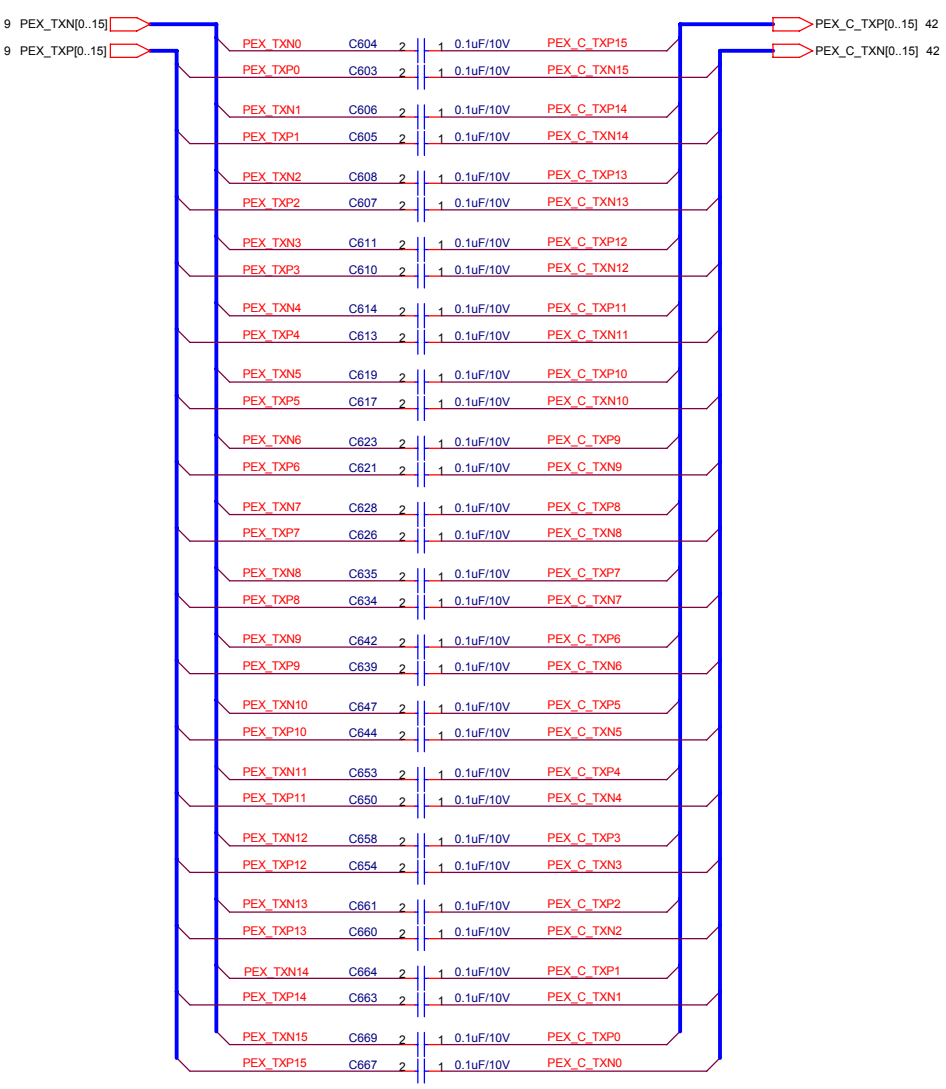
ASUSTek COMPUTER INC. NB6

Title : PCMCIA DEBUG

Engineer: Brad Lu

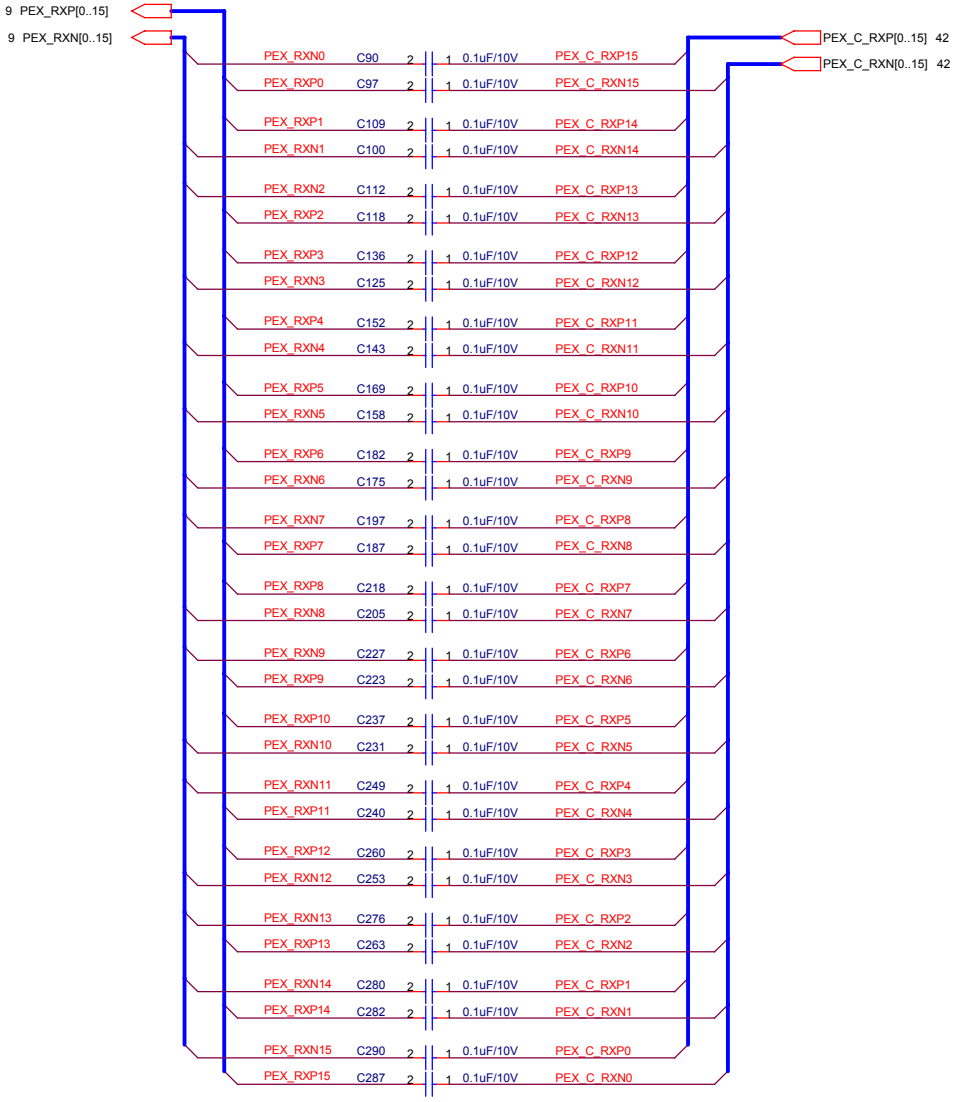
Size	Project Name	Rev
Custom	A6X	1.0

Date: Thursday, March 03, 2005 Sheet 40 of 64



PLACE these 0402 AC coupling caps close to sis756.

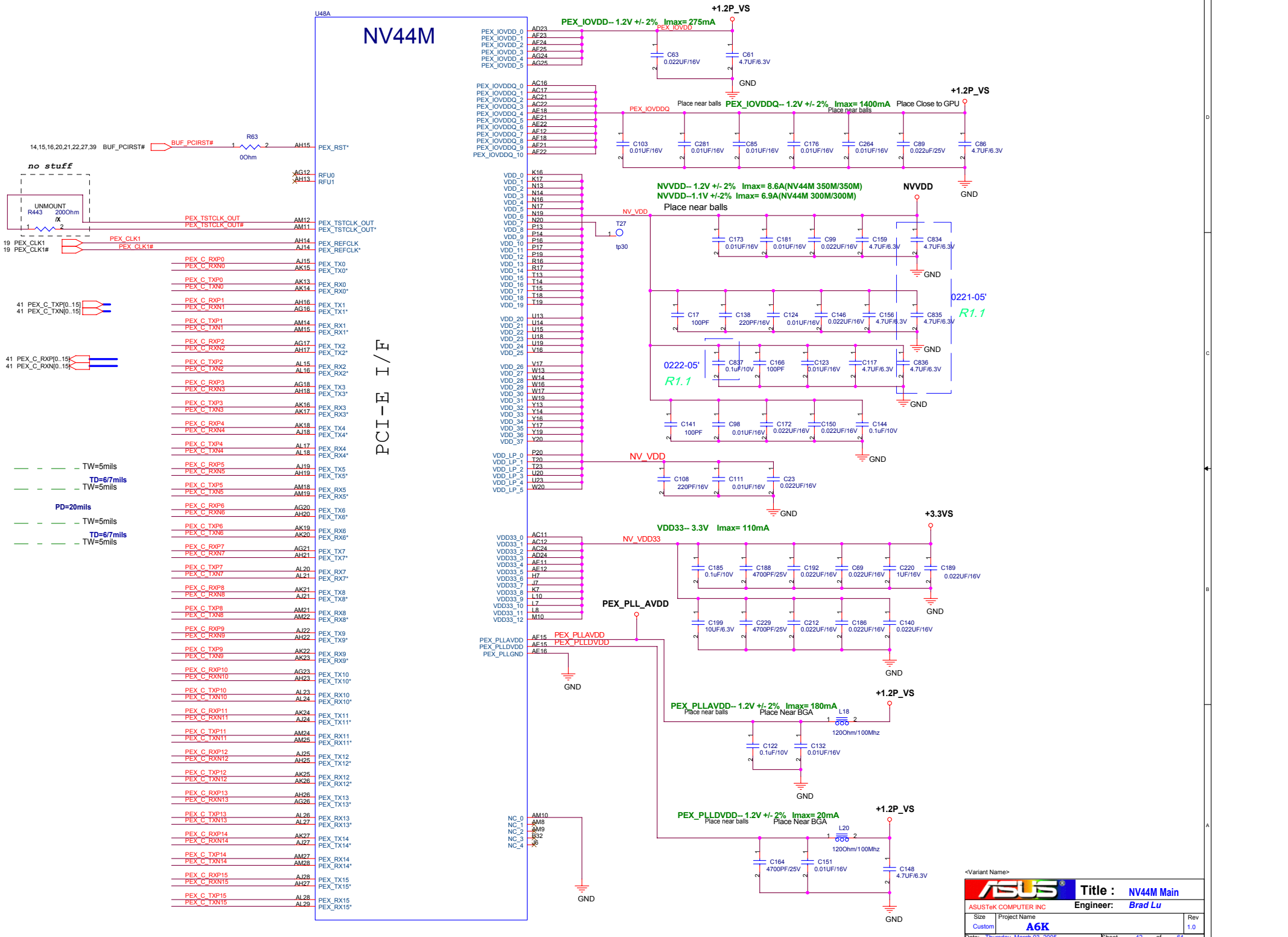
TX P&N [0..15] PIN SWAP FOR LAYOUT



PLACE these 0402 AC coupling caps close to nv44m

RX P&N 0.2.7.9.11.13.14.15 PIN SWAP FOR LAYOUT

ASUSTeK COMPUTER INC	Title : PCIE AC COUPLE	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 41 of 64	



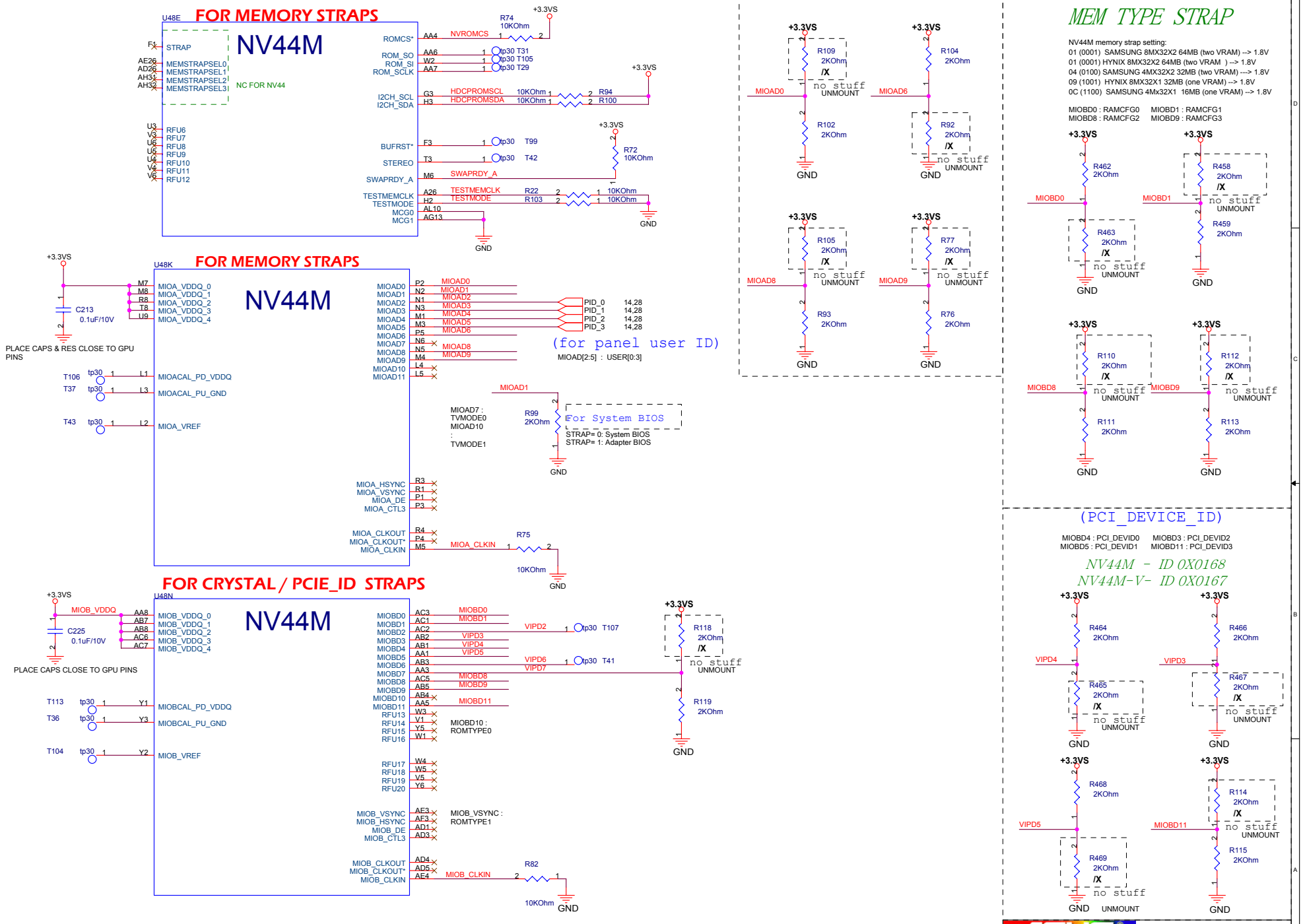
<Variant Name>

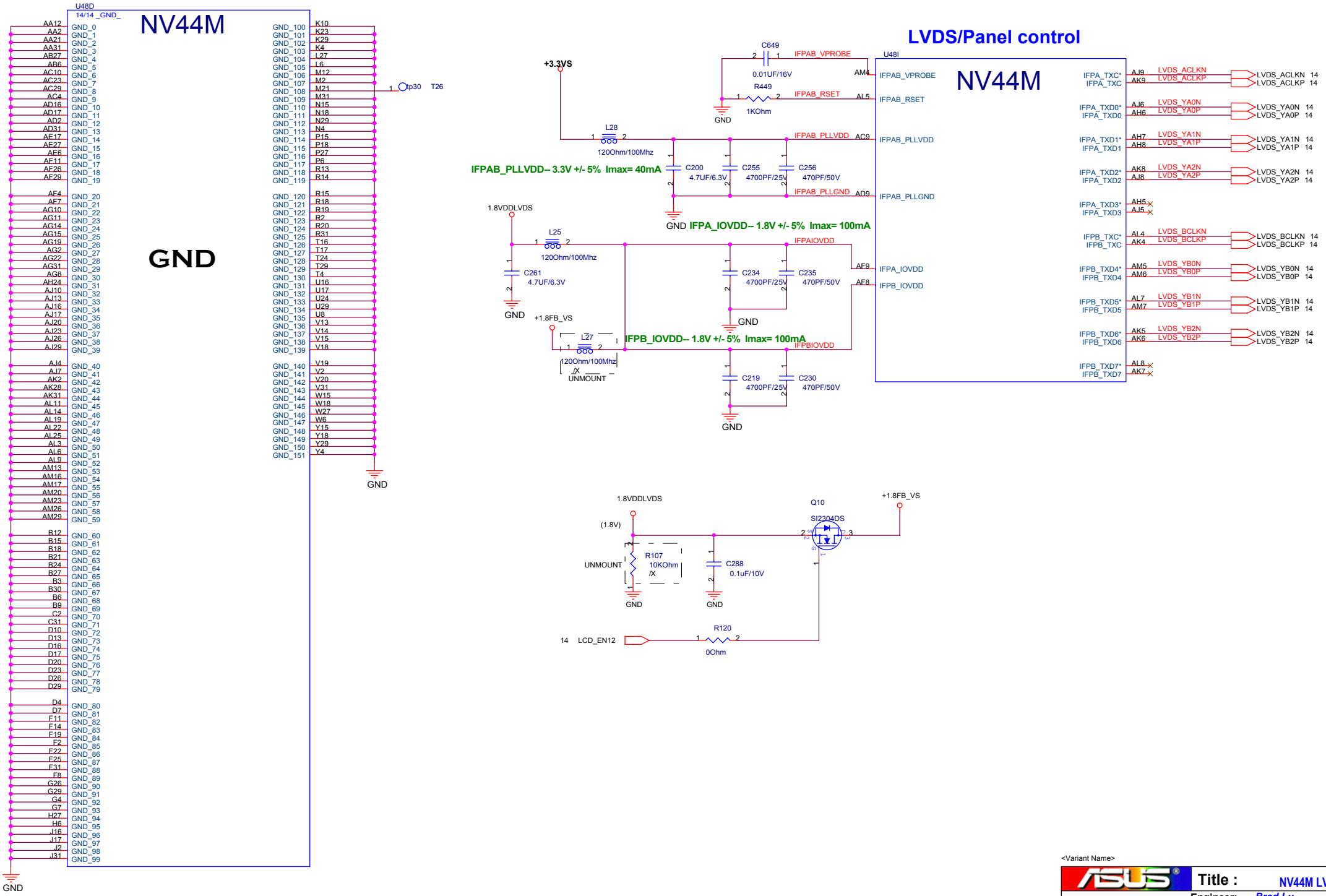
Title : NV44M Main

ASUSTeK COMPUTER INC Engineer: Brad Lu

Size: Custom | Project Name: A6K | Rev: 1.0

Date: Thursday, March 03, 2005 | Sheet 42 of 64

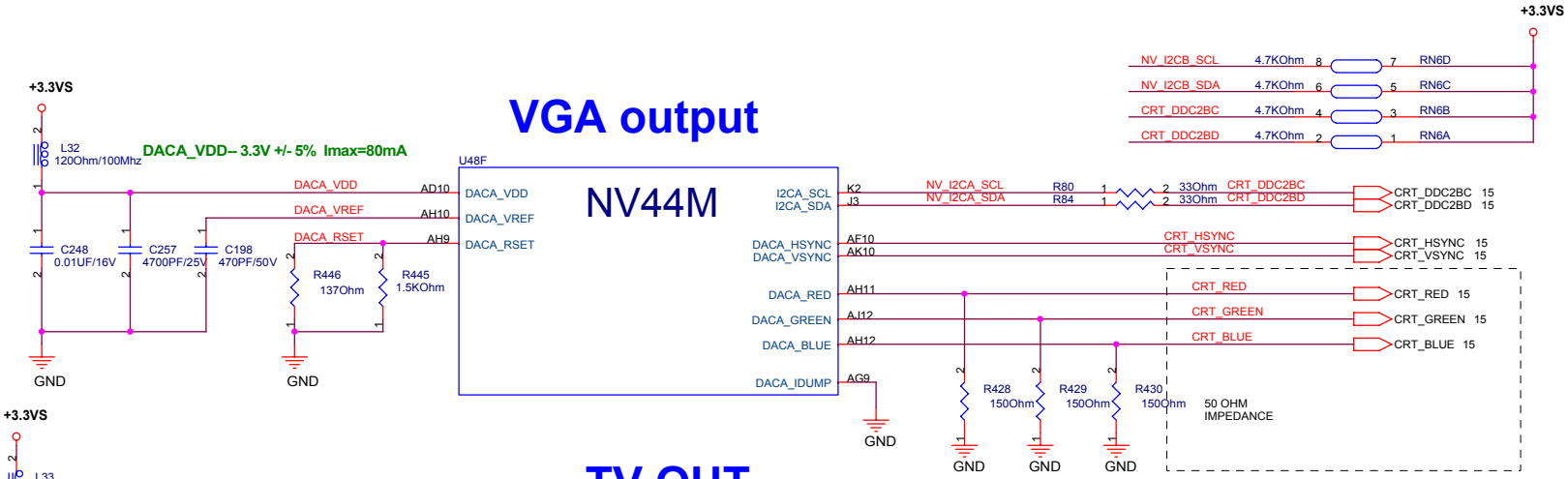

FOR MEMORY STRAPS
U48E
NV44M
STRAP
MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3
NC FOR NV44
RFU6
RFU7
RFU8
RFU9
RFU10
RFU11
RFU12
ROMCS*
NVROMCS
ROM_SO
ROM_SI
ROM_SCLK
I2CH_SCL
I2CH_SDA
HDCPROMSCL
HDCPROMSDA
BUFRST*
STEREO
SWAPRDY_A
TESTMEMCLK
TESTMODE
MCG0
MCG1
+3.3VS
R74 10KOhm
R94
R100
R72 10KOhm
R22
R103
10KOhm
GND
tp30 T31
tp30 T105
tp30 T29
tp30 T99
tp30 T42
FOR MEMORY STRAPS
U48K
NV44M
MIOA_VDDQ_0
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4
C213
0.1uF/10V
PLACE CAPS & RES CLOSE TO GPU PINS
MIOACAL_PD_VDDQ
MIOACAL_PU_GND
MIOA_VREF
MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11
PID_0 14,28
PID_1 14,28
PID_2 14,28
PID_3 14,28
(for panel user ID)
MIOAD[2:5] : USER[0:3]
MIOAD7 : TVMODE0
MIOAD10 : TVMODE1
R99 2KOhm
For System BIOS
STRAP= 0: System BIOS
STRAP= 1: Adapter BIOS
MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CTL3
MIOA_CLKOUT
MIOA_CLKOUT*
MIOA_CLKIN
R75
10KOhm
FOR CRYSTAL / PCIE_ID STRAPS
U48N
NV44M
MIOB_VDDQ_0
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4
C225
0.1uF/10V
PLACE CAPS CLOSE TO GPU PINS
MIOBCAL_PD_VDDQ
MIOBCAL_PU_GND
MIOB_VREF
MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
R118 2KOhm
R119 2KOhm
MIOBD10 : ROMTYPE0
MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3
MIOB_VSYNC : ROMTYPE1
MIOB_CLKOUT
MIOB_CLKOUT*
MIOB_CLKIN
R82
10KOhm
R109 2KOhm /X
R102 2KOhm
R104 2KOhm
R92 2KOhm /X
R105 2KOhm /X
R93 2KOhm
R77 2KOhm /X
R76 2KOhm
no stuff UNMOUNT
MEM TYPE STRAP
NV44M memory strap setting:
01 (0001) SAMSUNG 8MX32X2 64MB (two VRAM) --> 1.8V
01 (0001) HYNIX 8MX32X2 64MB (two VRAM) --> 1.8V
04 (0100) SAMSUNG 4MX32X2 32MB (two VRAM) --> 1.8V
09 (1001) HYNIX 8MX32X1 32MB (one VRAM) --> 1.8V
0C (1100) SAMSUNG 4Mx32X1 16MB (one VRAM) --> 1.8V
MIOBD0 : RAMCFG0
MIOBD1 : RAMCFG1
MIOBD8 : RAMCFG2
MIOBD9 : RAMCFG3
R462 2KOhm
R463 2KOhm /X
R458 2KOhm /X
R459 2KOhm
R110 2KOhm /X
R111 2KOhm
R112 2KOhm /X
R113 2KOhm
(PCI_DEVICE_ID)
MIOBD4 : PCI_DEVID0
MIOBD3 : PCI_DEVID2
MIOBD5 : PCI_DEVID1
MIOBD11 : PCI_DEVID3
NV44M - ID 0X0168
NV44M-V- ID 0X0167
R464 2KOhm
R465 2KOhm /X
R466 2KOhm
R467 2KOhm /X
R468 2KOhm
R469 2KOhm /X
R114 2KOhm /X
R115 2KOhm
Title : NV44 Strapping
ASUSTek COMPUTER INC.
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.00
Date: Thursday, March 03, 2005
Sheet 43 of 64



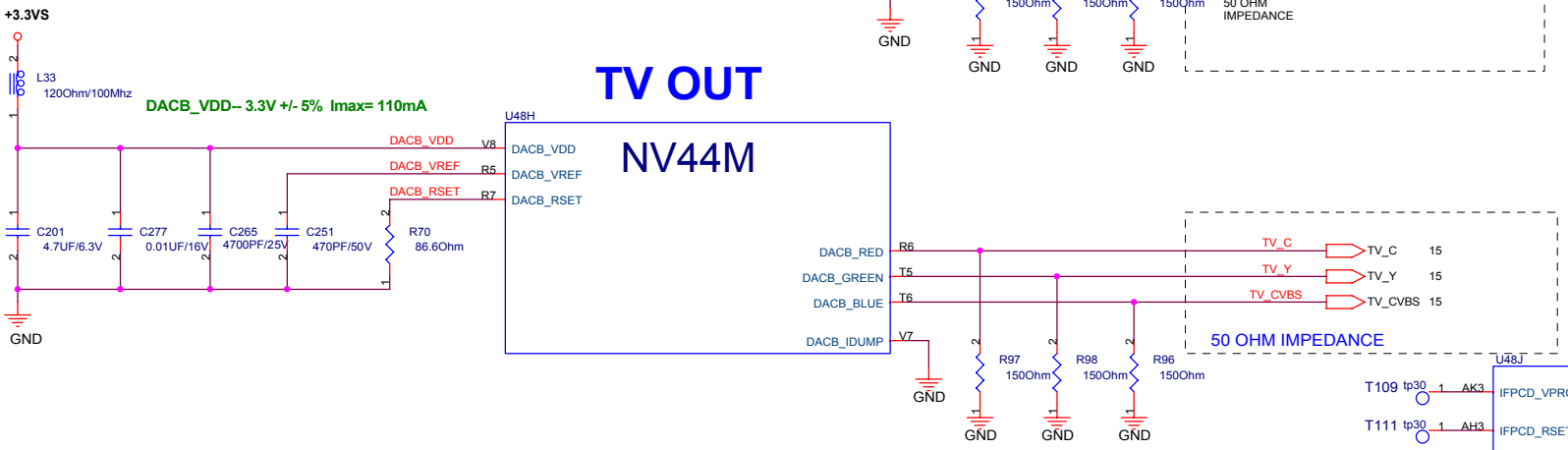
<Variant Name>

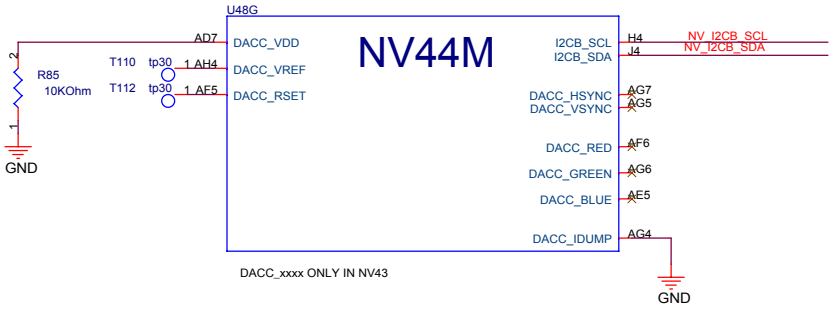
ASUSTeK COMPUTER INC	Title : NV44M LVDS	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 44 of 64	

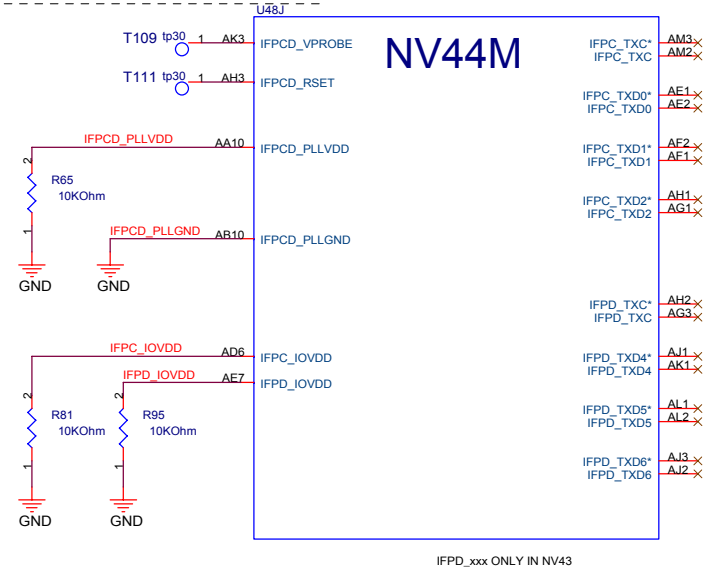
VGA output



TV OUT



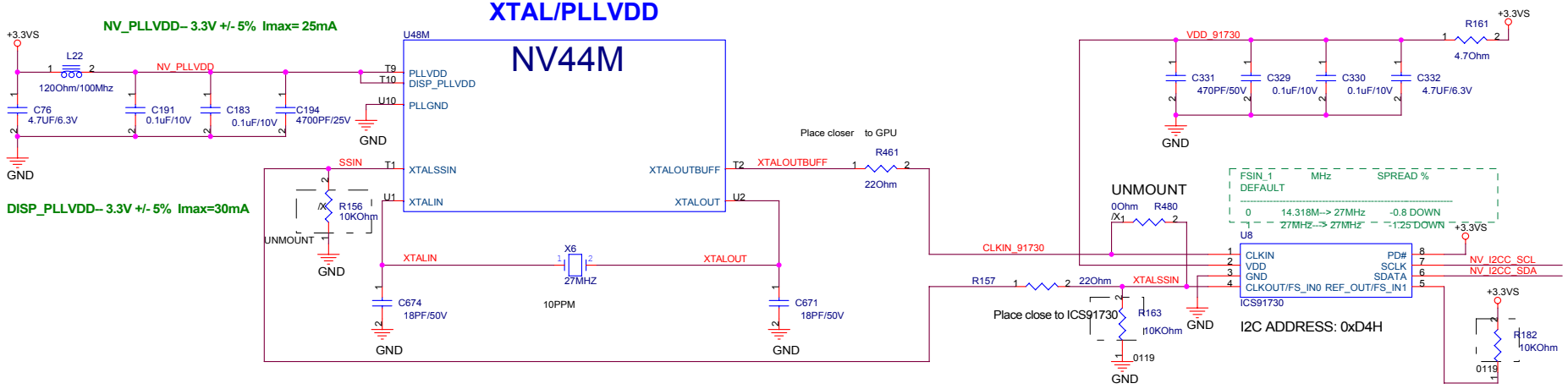


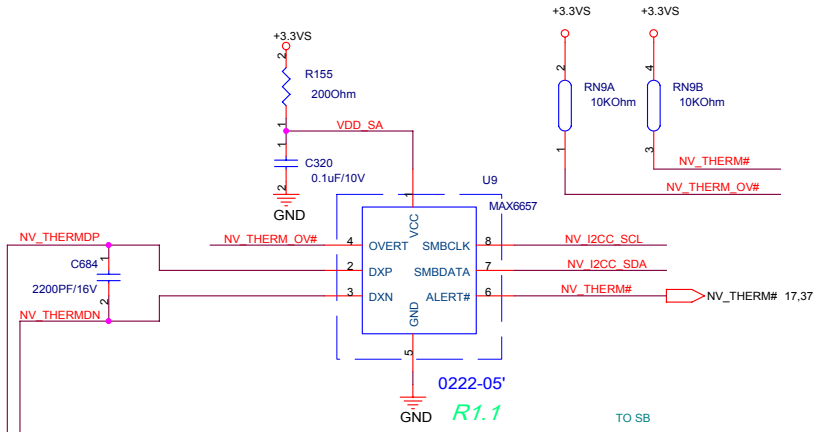


<Variant Name>

ASUSTeK COMPUTER INC	Title : MV44 VGA/TV Out	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 45 of 64	

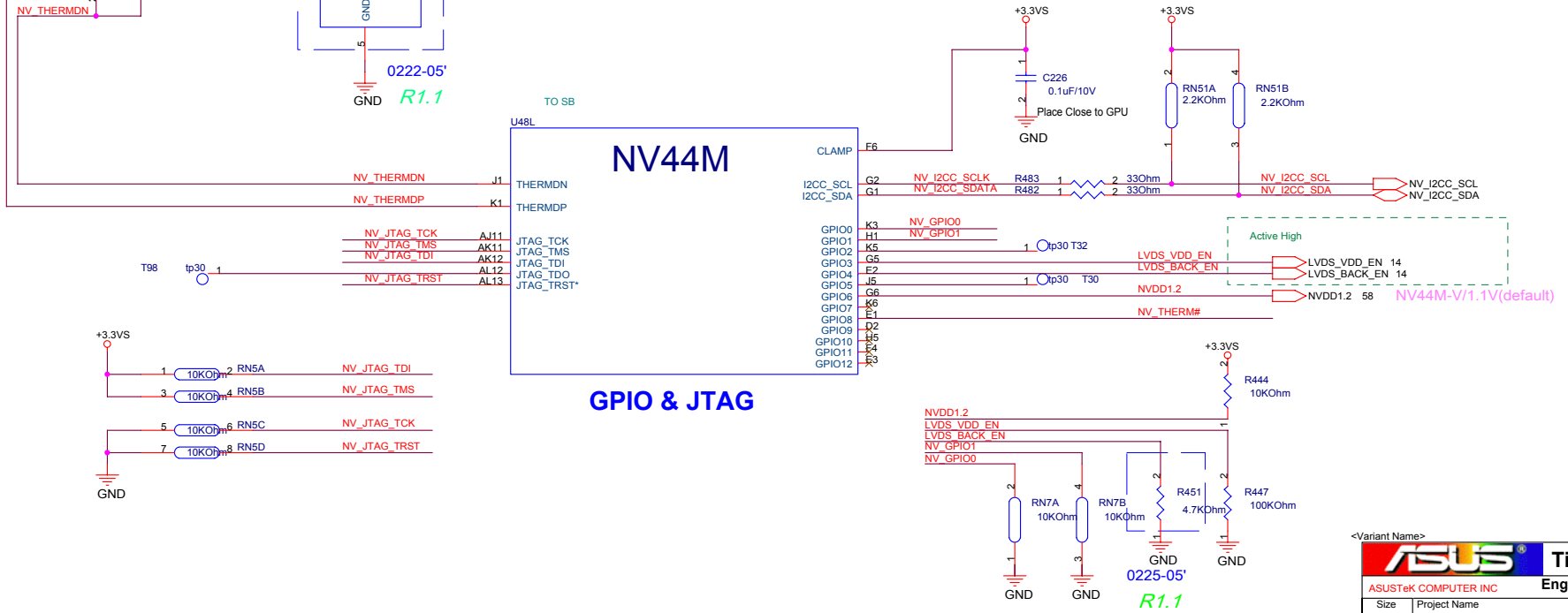
XTAL/PLLVDD





GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOT PLUG
1	IN	N/A	2ND DVI HOT PLUG
2	OUT	HIGH	BACKLIGHT BRIGHTNESS
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID0
6	OUT	HIGH	NVVDD VID1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	THERMAL SHUTDOWN
9	OUT	LOW	FAN PWM

GPIO & JTAG



<Variant Name>

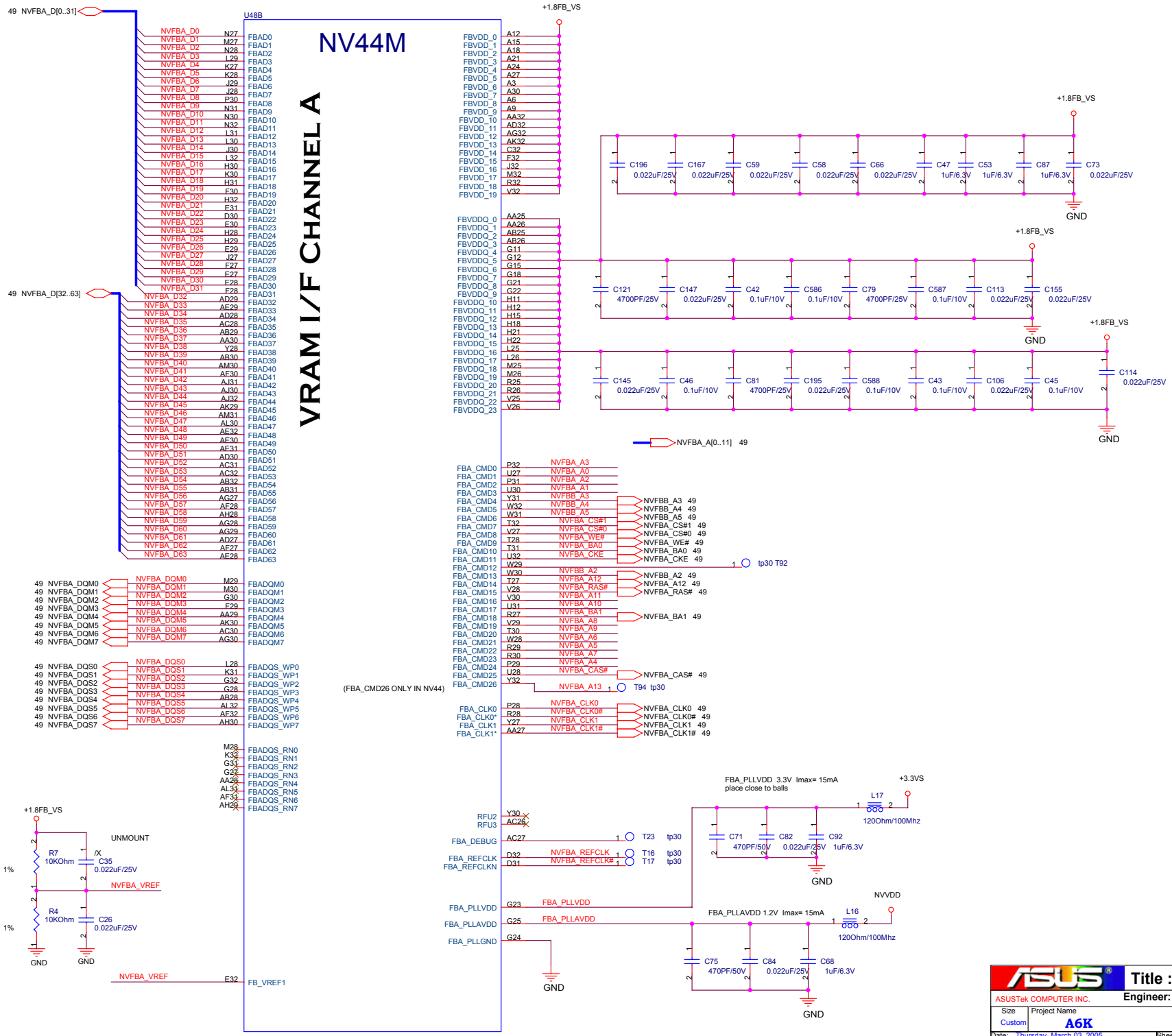
ASUSTeK COMPUTER INC

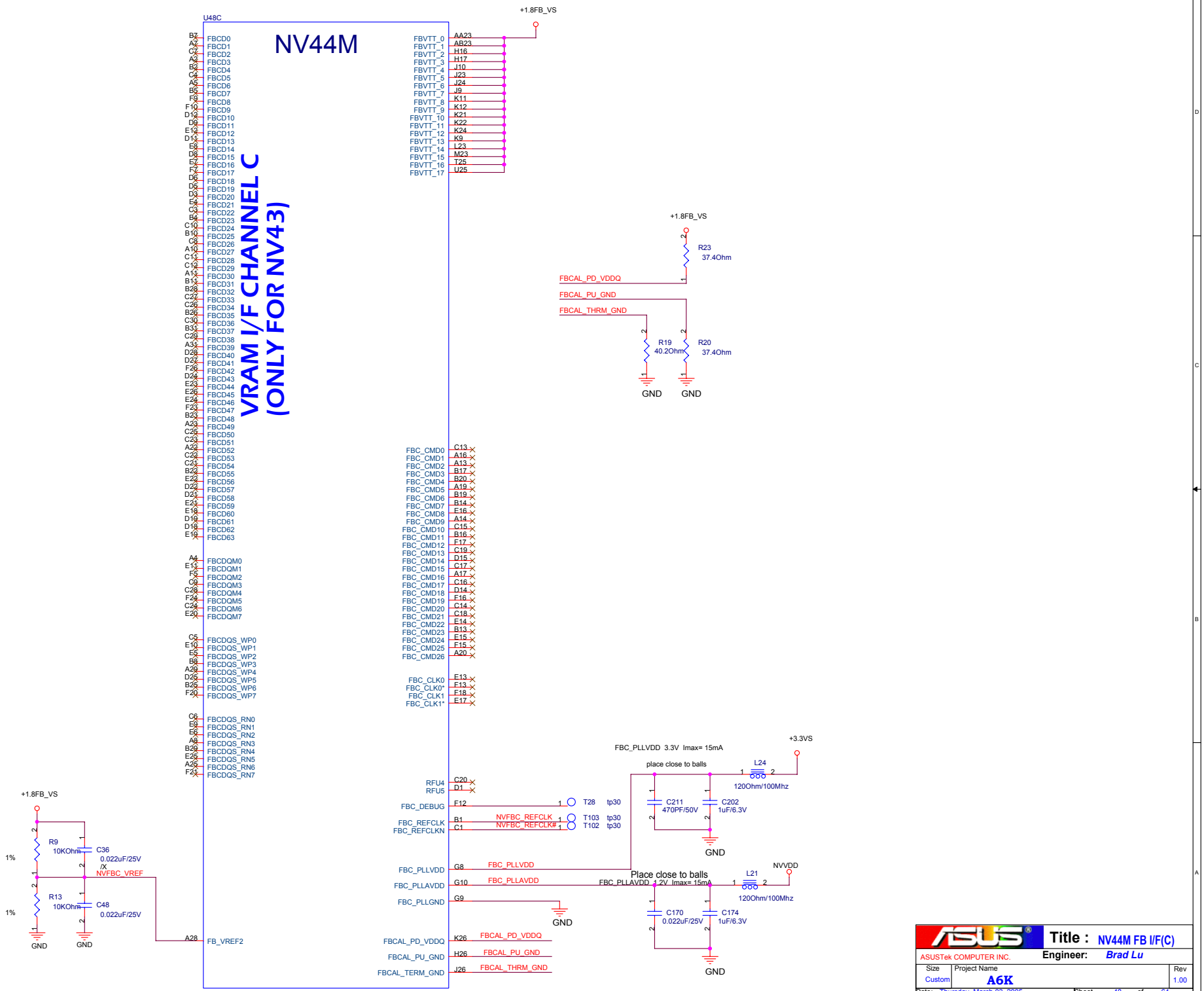
Title : NV Spread Spectrum

Engineer: Brad Lu

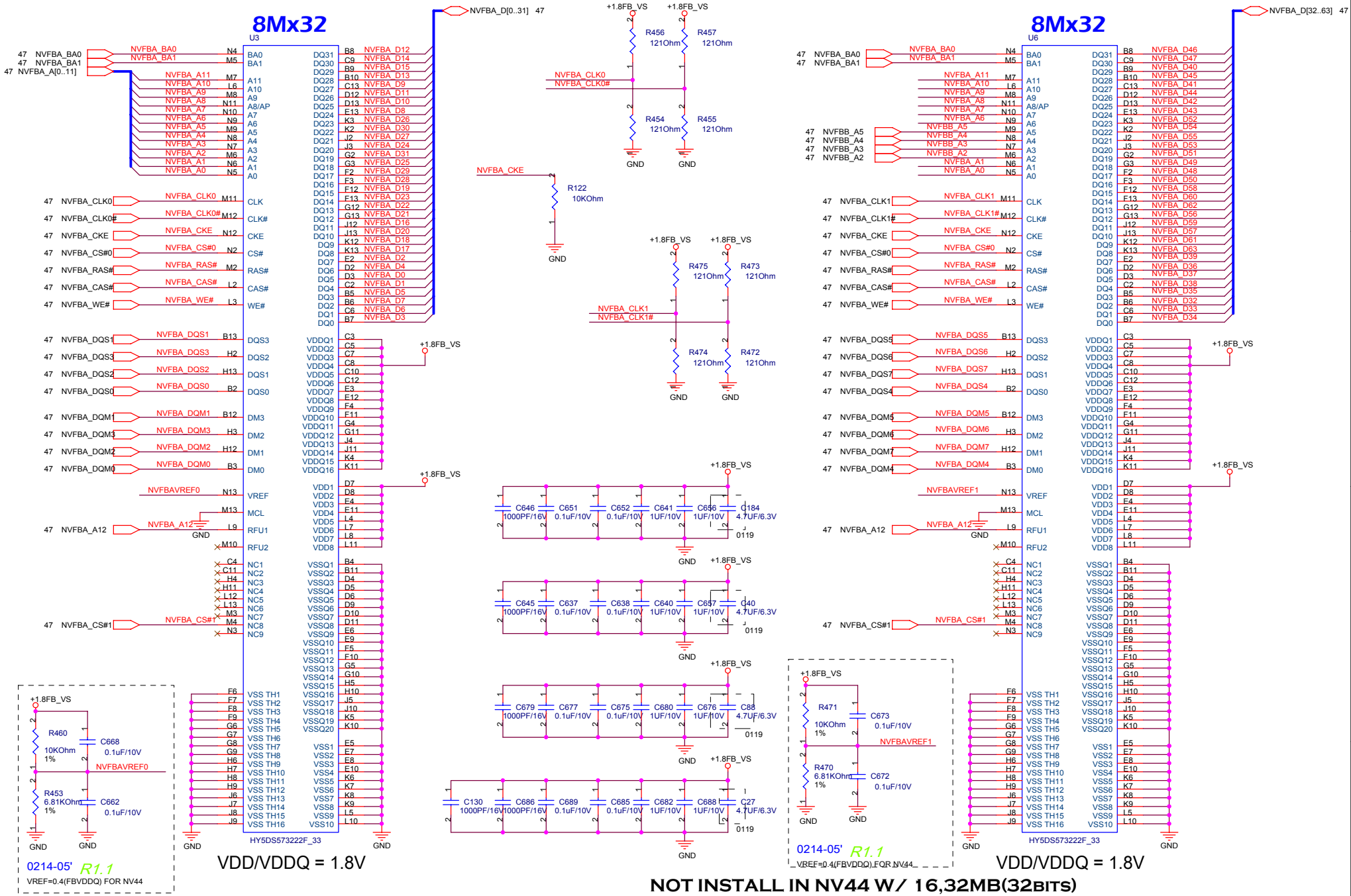
Size	Project Name	Rev
Custom	A6K	1.1

Date: Thursday, March 03, 2005 Sheet 46 of 64


NV44M
VRAM I/F CHANNEL A
U48B
49 NVFBA_D[0..31]
49 NVFBA_D[32..63]
NVFBA_D0 NVFBA_D1 NVFBA_D2 NVFBA_D3 NVFBA_D4 NVFBA_D5 NVFBA_D6 NVFBA_D7 NVFBA_D8 NVFBA_D9 NVFBA_D10 NVFBA_D11 NVFBA_D12 NVFBA_D13 NVFBA_D14 NVFBA_D15 NVFBA_D16 NVFBA_D17 NVFBA_D18 NVFBA_D19 NVFBA_D20 NVFBA_D21 NVFBA_D22 NVFBA_D23 NVFBA_D24 NVFBA_D25 NVFBA_D26 NVFBA_D27 NVFBA_D28 NVFBA_D29 NVFBA_D30 NVFBA_D31
NVFBA_D32 NVFBA_D33 NVFBA_D34 NVFBA_D35 NVFBA_D36 NVFBA_D37 NVFBA_D38 NVFBA_D39 NVFBA_D40 NVFBA_D41 NVFBA_D42 NVFBA_D43 NVFBA_D44 NVFBA_D45 NVFBA_D46 NVFBA_D47 NVFBA_D48 NVFBA_D49 NVFBA_D50 NVFBA_D51 NVFBA_D52 NVFBA_D53 NVFBA_D54 NVFBA_D55 NVFBA_D56 NVFBA_D57 NVFBA_D58 NVFBA_D59 NVFBA_D60 NVFBA_D61 NVFBA_D62 NVFBA_D63
FBAD0 FBAD1 FBAD2 FBAD3 FBAD4 FBAD5 FBAD6 FBAD7 FBAD8 FBAD9 FBAD10 FBAD11 FBAD12 FBAD13 FBAD14 FBAD15 FBAD16 FBAD17 FBAD18 FBAD19 FBAD20 FBAD21 FBAD22 FBAD23 FBAD24 FBAD25 FBAD26 FBAD27 FBAD28 FBAD29 FBAD30 FBAD31 FBAD32 FBAD33 FBAD34 FBAD35 FBAD36 FBAD37 FBAD38 FBAD39 FBAD40 FBAD41 FBAD42 FBAD43 FBAD44 FBAD45 FBAD46 FBAD47 FBAD48 FBAD49 FBAD50 FBAD51 FBAD52 FBAD53 FBAD54 FBAD55 FBAD56 FBAD57 FBAD58 FBAD59 FBAD60 FBAD61 FBAD62 FBAD63
NVFBA_DQM0 NVFBA_DQM1 NVFBA_DQM2 NVFBA_DQM3 NVFBA_DQM4 NVFBA_DQM5 NVFBA_DQM6 NVFBA_DQM7
FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7
NVFBA_DQS0 NVFBA_DQS1 NVFBA_DQS2 NVFBA_DQS3 NVFBA_DQS4 NVFBA_DQS5 NVFBA_DQS6 NVFBA_DQS7
FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7
FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7
+1.8FB_VS
UNMOUNT
R7 10KOhm 1%
C35 /X 0.022uF/25V
NVFBA_VREF
R4 10KOhm 1%
C26 0.022uF/25V
GND
NVFBA_VREF
FB_VREF1
FBVDD_0 FBVDD_1 FBVDD_2 FBVDD_3 FBVDD_4 FBVDD_5 FBVDD_6 FBVDD_7 FBVDD_8 FBVDD_9 FBVDD_10 FBVDD_11 FBVDD_12 FBVDD_13 FBVDD_14 FBVDD_15 FBVDD_16 FBVDD_17 FBVDD_18 FBVDD_19
FBVDDQ_0 FBVDDQ_1 FBVDDQ_2 FBVDDQ_3 FBVDDQ_4 FBVDDQ_5 FBVDDQ_6 FBVDDQ_7 FBVDDQ_8 FBVDDQ_9 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23
C196 0.022uF/25V
C167 0.022uF/25V
C59 0.022uF/25V
C58 0.022uF/25V
C66 0.022uF/25V
C47 1uF/6.3V
C53 1uF/6.3V
C87 1uF/6.3V
C73 0.022uF/25V
C121 4700PF/25V
C147 0.022uF/25V
C42 0.1uF/10V
C586 0.1uF/10V
C79 4700PF/25V
C587 0.1uF/10V
C113 0.022uF/25V
C155 0.022uF/25V
C145 0.022uF/25V
C46 0.1uF/10V
C81 4700PF/25V
C195 0.022uF/25V
C588 0.1uF/10V
C43 0.1uF/10V
C106 0.022uF/25V
C45 0.1uF/10V
C114 0.022uF/25V
NVFBA_A[0..11] 49
FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26
NVFBA_A3 NVFBA_A0 NVFBA_A2 NVFBA_A1 NVFBB_A3 NVFBB_A4 NVFBB_A5 NVFBA_CS#1 NVFBA_CS#0 NVFBA_WE# NVFBA_BA0 NVFBA_CKE NVFBB_A2 NVFBA_A12 NVFBA_RAS# NVFBA_A11 NVFBA_A10 NVFBA_BA1 NVFBA_A8 NVFBA_A9 NVFBA_A6 NVFBA_A5 NVFBA_A7 NVFBA_A4 NVFBA_CAS# NVFBA_A13
NVFBB_A3 49
NVFBB_A4 49
NVFBB_A5 49
NVFBA_CS#1 49
NVFBA_CS#0 49
NVFBA_WE# 49
NVFBA_BA0 49
NVFBA_CKE 49
tp30 T92
NVFBB_A2 49
NVFBA_A12 49
NVFBA_RAS# 49
NVFBA_BA1 49
NVFBA_CAS# 49
T94 tp30
(FBA_CMD26 ONLY IN NV44)
FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*
NVFBA_CLK0 NVFBA_CLK0# NVFBA_CLK1 NVFBA_CLK1#
NVFBA_CLK0 49
NVFBA_CLK0# 49
NVFBA_CLK1 49
NVFBA_CLK1# 49
RFU2 RFU3
FBA_DEBUG
FBA_REFCLK FBA_REFCLKN
NVFBA_REFCLK NVFBA_REFCLK#
T23 tp30
T16 tp30
T17 tp30
FBA_PLLVDD FBA_PLLAVDD FBA_PLLGND
FBA_PLLVDD 1.2V Imax= 15mA
FBA_PLLVDD 3.3V Imax= 15mA
place close to balls
+3.3VS
NVVDD
L17 120Ohm/100Mhz
L16 120Ohm/100Mhz
C71 470PF/50V
C82 0.022uF/25V
C92 1uF/6.3V
C75 470PF/50V
C84 0.022uF/25V
C68 1uF/6.3V
GND
Title : NV44M FB I/F(A)
ASUSTeK COMPUTER INC.
Engineer: Brad Lu
Size Custom
Project Name A6K
Rev 1.00
Date: Thursday, March 03, 2005
Sheet 47 of 64



ASUSTeK COMPUTER INC.	Title : NV44M FB I/F(C)		
	Engineer: Brad Lu		
Size: Custom	Project Name: A6K		Rev: 1.00
Date: Thursday, March 03, 2005	Sheet 48 of 64		

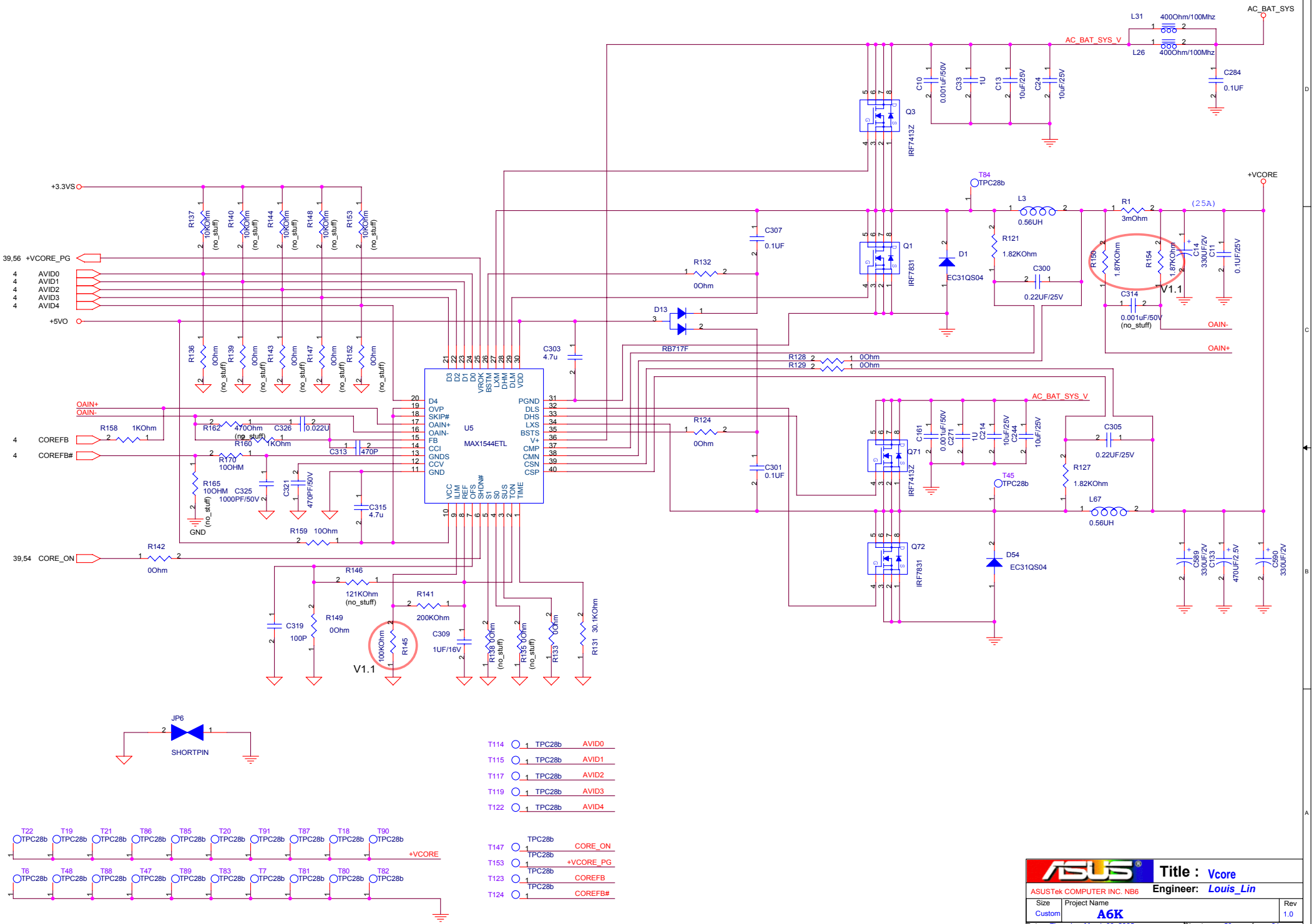


NOT INSTALL IN NV44 W/ 16,32MB(32BITS)

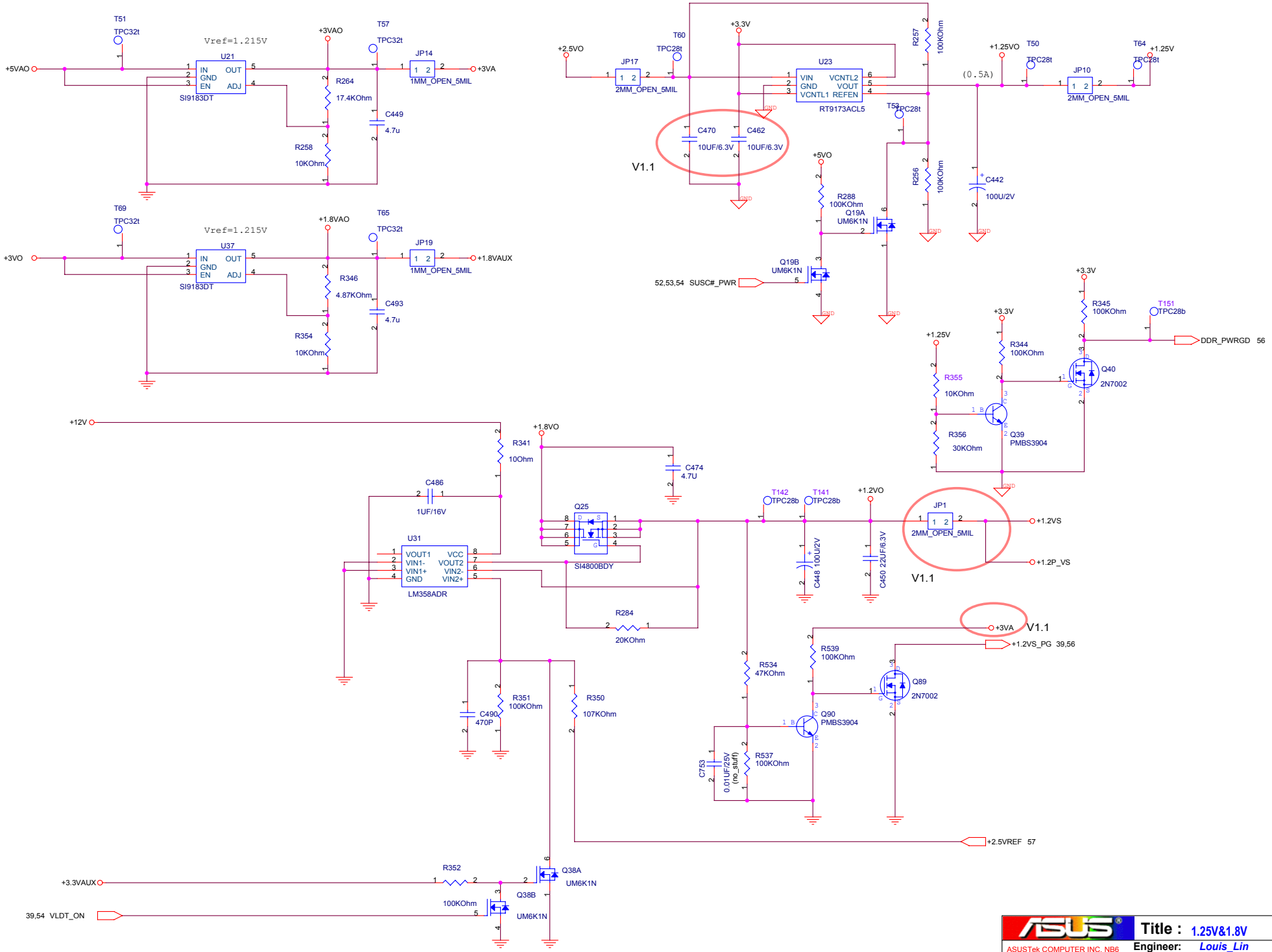
VRAM 16MB/32MB CHANNEL A (NOT INSTALL FOR MEP43/44)

Samsung "03-15124E013" for K4D553235F-GC33 300MHz 600Mbps/pin

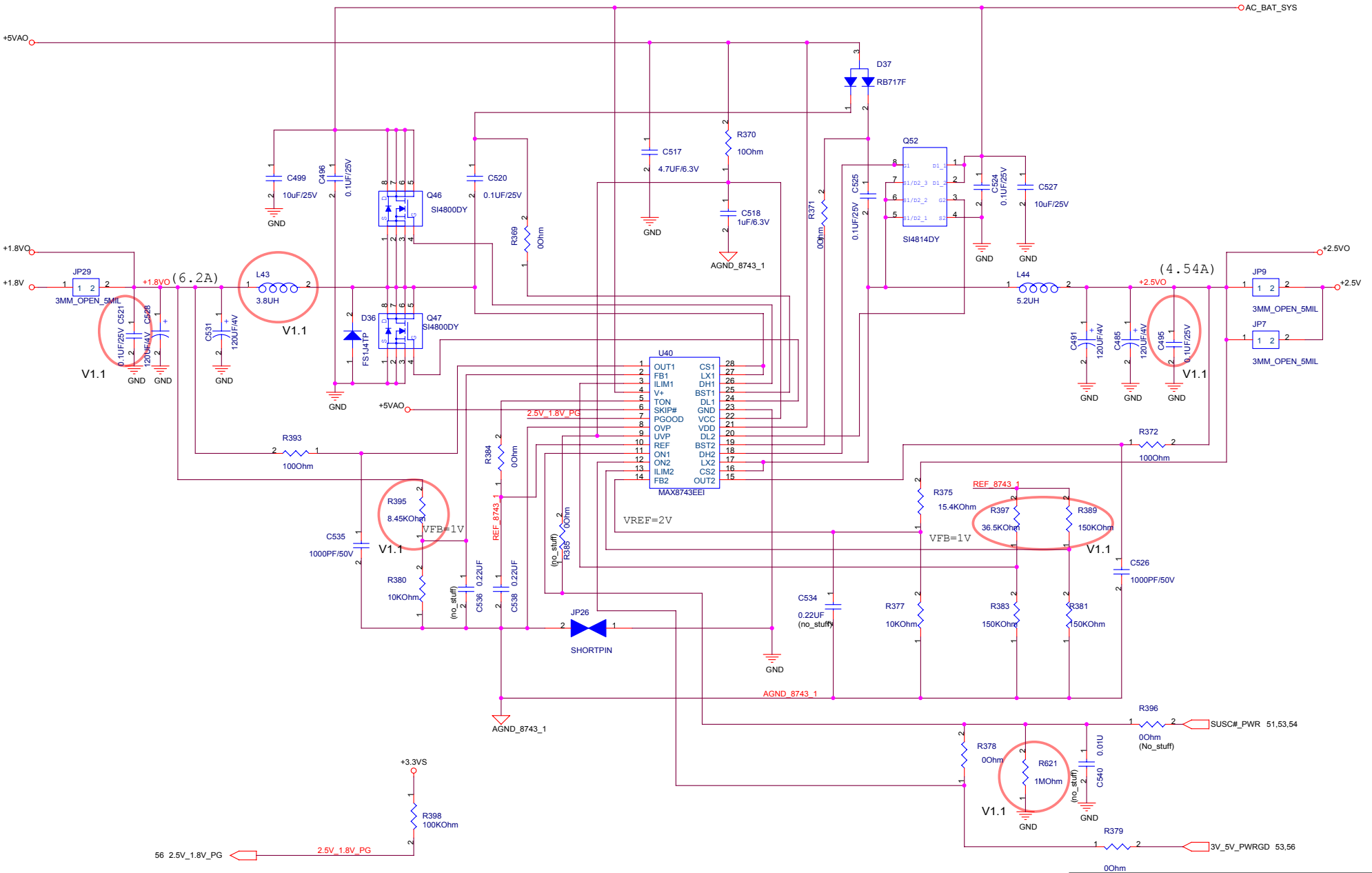
ASUSTek COMPUTER INC.	Title : NV44M VRAM	
	Engineer: Brad Lu	
Size: Custom	Project Name: A6K	Rev: 1.00
Date: Thursday, March 03, 2005	Sheet 49 of 64	



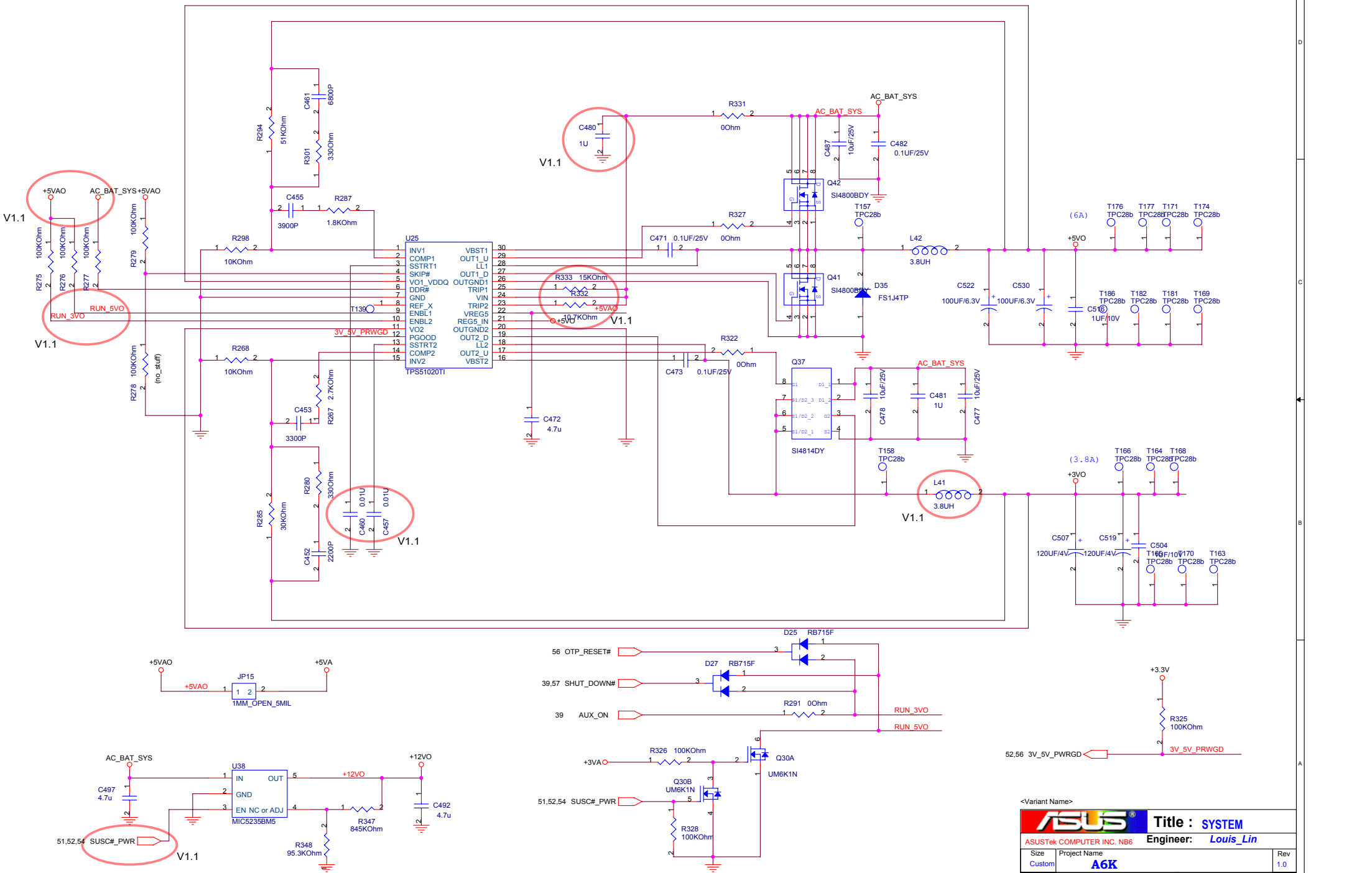
ASUSTek COMPUTER INC. NB6	Title : Vcore		
	Engineer: Louis_Lin		
Size: Custom	Project Name: A6K		Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 50 of 64		



ASUSTek COMPUTER INC. NB6	Title : 1.25V&1.8V	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 51 of 64	

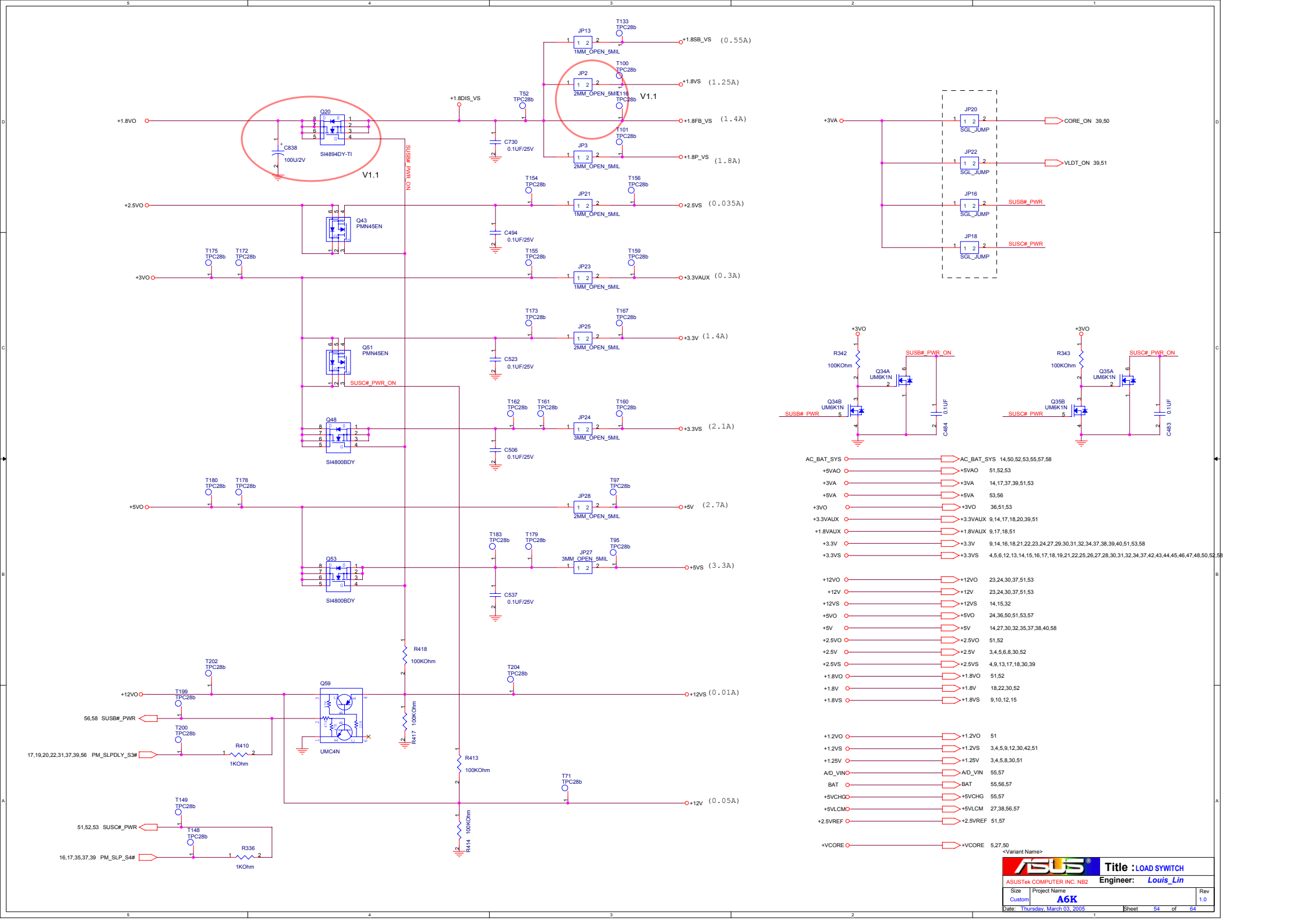


ASUSTek COMPUTER INC. NB6	Title : 1.8V & 2.5V	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 52 of 64	



<Variant Name>

ASUSTek COMPUTER INC. NB6	Title : SYSTEM	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 53 of 64	

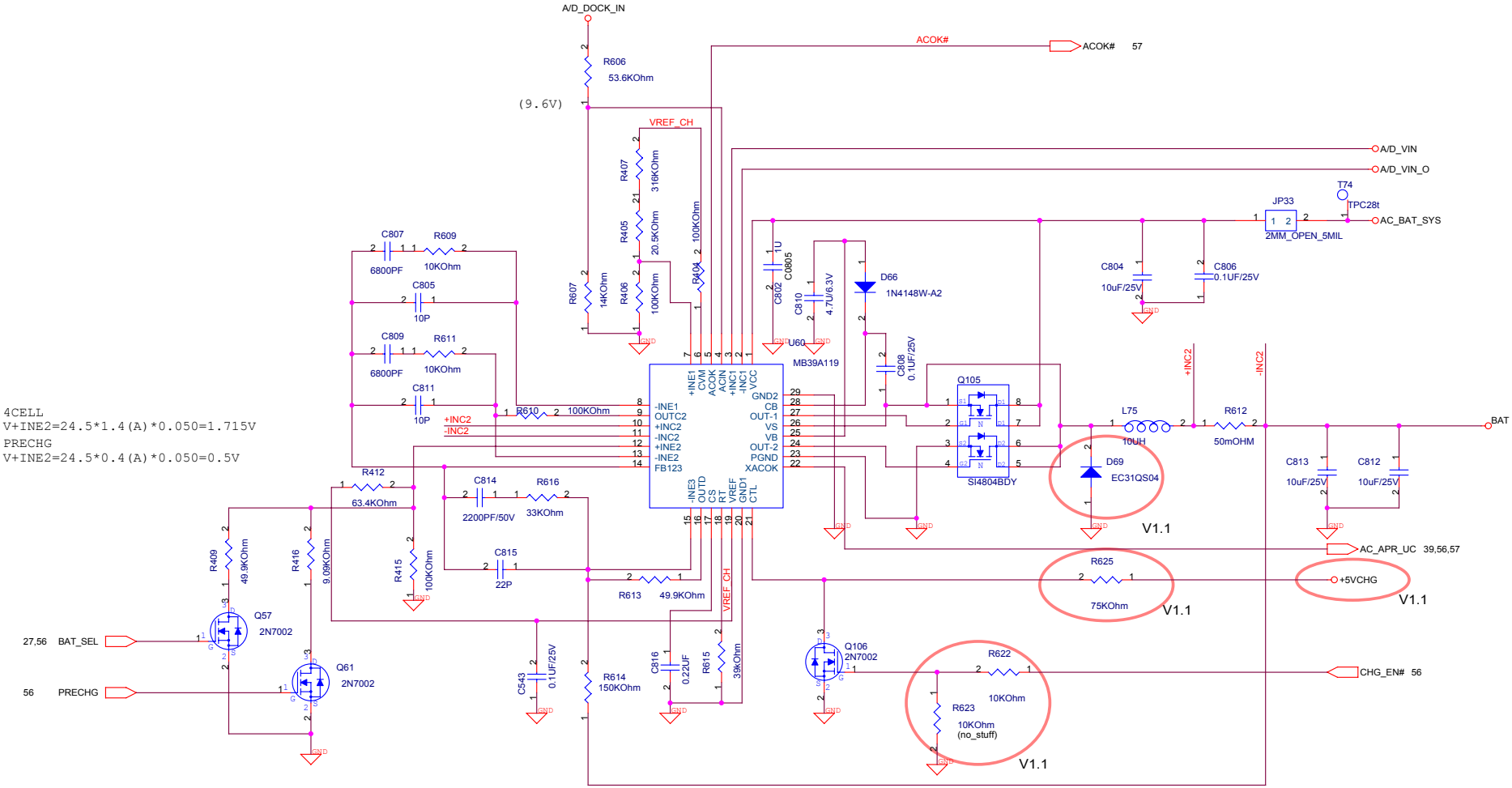

+1.8VO
Q20
SI4894DY-TI
C838
100U/2V
V1.1
+1.8DIS_VS
T52 TPC28b
C730 0.1UF/25V
JP13 1MM_OPEN_5MIL
T133 TPC28b
+1.8SB_VS (0.55A)
JP2 2MM_OPEN_5MIL
T100 TPC28b
+1.8VS (1.25A)
T116 TPC28b
V1.1
JP3 2MM_OPEN_5MIL
T101 TPC28b
+1.8P_VS (1.8A)
+1.8FB_VS (1.4A)
SUS#_PWR_ON
+2.5VO
Q43 PMN45EN
C494 0.1UF/25V
T154 TPC28b
T156 TPC28b
JP21 1MM_OPEN_5MIL
+2.5VS (0.035A)
+3VO
T175 TPC28b
T172 TPC28b
T155 TPC28b
T159 TPC28b
JP23 1MM_OPEN_5MIL
+3.3VAUX (0.3A)
Q51 PMN45EN
SUSC#_PWR_ON
C523 0.1UF/25V
T173 TPC28b
T167 TPC28b
JP25 2MM_OPEN_5MIL
+3.3V (1.4A)
Q48
SI4800BDY
T162 TPC28b
T161 TPC28b
T160 TPC28b
JP24 3MM_OPEN_5MIL
+3.3VS (2.1A)
C506 0.1UF/25V
+5VO
T180 TPC28b
T178 TPC28b
T97 TPC28b
JP28 2MM_OPEN_5MIL
+5V (2.7A)
Q53
SI4800BDY
T183 TPC28b
T179 TPC28b
T95 TPC28b
JP27 3MM_OPEN_5MIL
+5VS (3.3A)
C537 0.1UF/25V
R418 100KOhm
T202 TPC28b
T204 TPC28b
+12VO
T199 TPC28b
Q59
UMC4N
R417 100KOhm
+12VS (0.01A)
56,58 SUSB#_PWR
T200 TPC28b
17,19,20,22,31,37,39,56 PM_SLPDLY_S3#
R410 1KOhm
R413 100KOhm
T71 TPC28b
+12V (0.05A)
R414 100KOhm
T149 TPC28b
51,52,53 SUSC#_PWR
T148 TPC28b
16,17,35,37,39 PM_SLP_S4#
R336 1KOhm
+3VA
JP20 SGL_JUMP
CORE_ON 39,50
JP22 SGL_JUMP
VLDT_ON 39,51
JP16 SGL_JUMP
SUSB#_PWR
JP18 SGL_JUMP
SUSC#_PWR
+3VO
R342 100KOhm
Q34A UM6K1N
Q34B UM6K1N
SUSB#_PWR_ON
SUSB#_PWR
C484 0.1UF
R343 100KOhm
Q35A UM6K1N
Q35B UM6K1N
SUSC#_PWR_ON
SUSC#_PWR
C483 0.1UF
AC_BAT_SYS AC_BAT_SYS 14,50,52,53,55,57,58
+5VAO +5VAO 51,52,53
+3VA +3VA 14,17,37,39,51,53
+5VA +5VA 53,56
+3VO +3VO 36,51,53
+3.3VAUX +3.3VAUX 9,14,17,18,20,39,51
+1.8VAUX +1.8VAUX 9,17,18,51
+3.3V +3.3V 9,14,16,18,21,22,23,24,27,29,30,31,32,34,37,38,39,40,51,53,58
+3.3VS +3.3VS 4,5,6,12,13,14,15,16,17,18,19,21,22,25,26,27,28,30,31,32,34,37,42,43,44,45,46,47,48,50,52,58
+12VO +12VO 23,24,30,37,51,53
+12V +12V 23,24,30,37,51,53
+12VS +12VS 14,15,32
+5VO +5VO 24,36,50,51,53,57
+5V +5V 14,27,30,32,35,37,38,40,58
+2.5VO +2.5VO 51,52
+2.5V +2.5V 3,4,5,6,8,30,52
+2.5VS +2.5VS 4,9,13,17,18,30,39
+1.8VO +1.8VO 51,52
+1.8V +1.8V 18,22,30,52
+1.8VS +1.8VS 9,10,12,15
+1.2VO +1.2VO 51
+1.2VS +1.2VS 3,4,5,9,12,30,42,51
+1.25V +1.25V 3,4,5,8,30,51
A/D_VIN A/D_VIN 55,57
BAT BAT 55,56,57
+5VCHG +5VCHG 55,57
+5VLCM +5VLCM 27,38,56,57
+2.5VREF +2.5VREF 51,57
+VCORE +VCORE 5,27,50
<Variant Name>
Title : LOAD SYWITCH
ASUSTek COMPUTER INC. NB2
Engineer: Louis_Lin
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 54 of 64

+Vbat=(R1+R2)/R2*4.2
+Vbat=(30k+10k)/10k*4.2=16.8V

V+INE2=24.5*Ichg(A)*Rs1
V+INE2=24.5*2.5(A)*0.050=3.062V Vref=5.000V
DEFAULT R(low)=100K
R(hi)=(5/3.062-1)*100K=63.3K

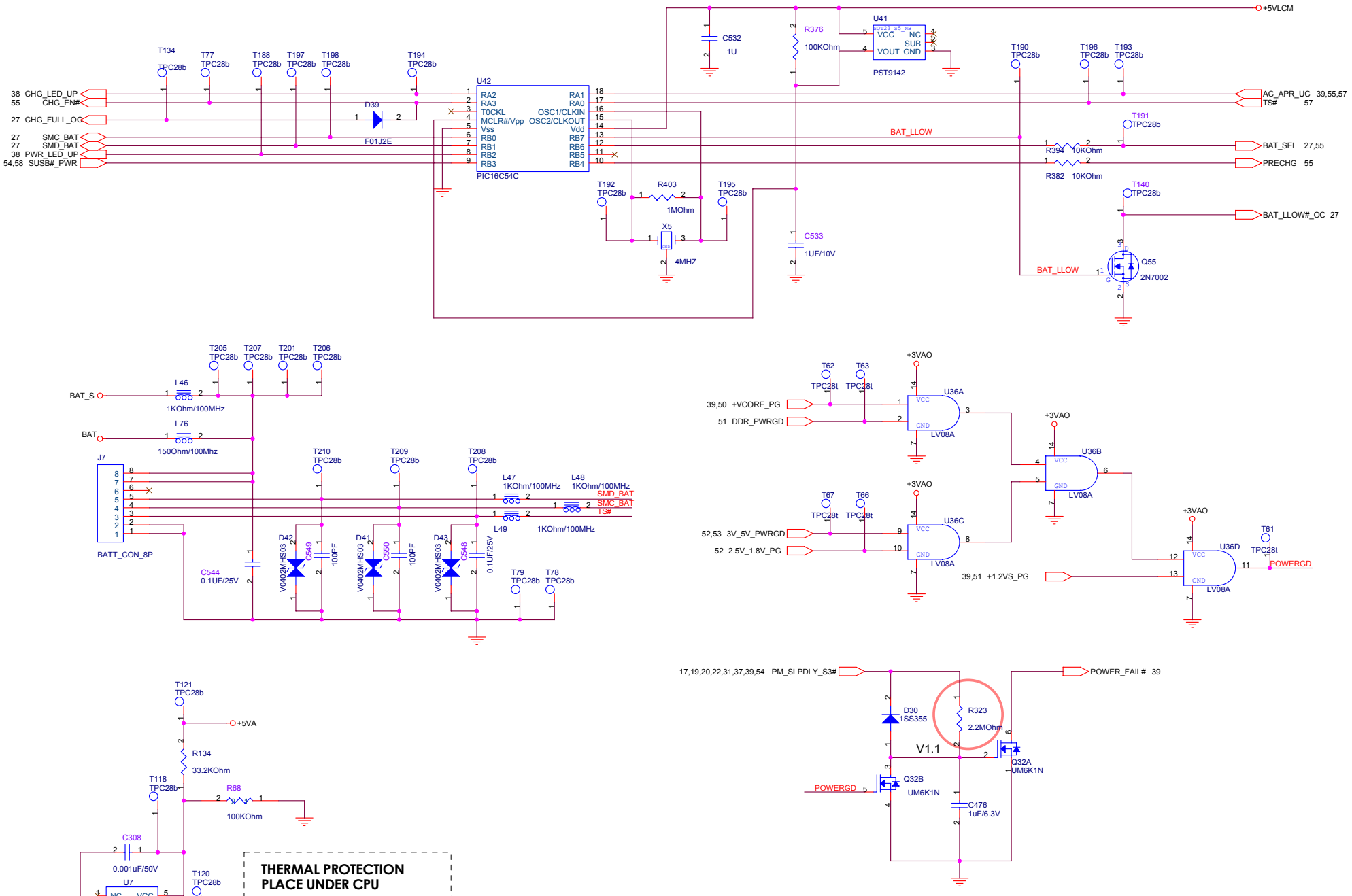
V+INE1=25*Iin(A)*Rs2
V+INE1=25*4.58(A)*0.010=1.145V
DEFAULT R(low)=100K
R(hi)=(5/1.145-1)*10K=336.68K

4CELL
V+INE2=24.5*1.4(A)*0.050=1.715V
PRECHG
V+INE2=24.5*0.4(A)*0.050=0.5V



<Variant Name>

ASUSTek COMPUTER INC. NB6	Title : CHARGER	
	Engineer: Louis_Lin	
Size: Custom	Project Name: A6K	Rev: 1.0
Date: Thursday, March 03, 2005	Sheet 55 of 64	



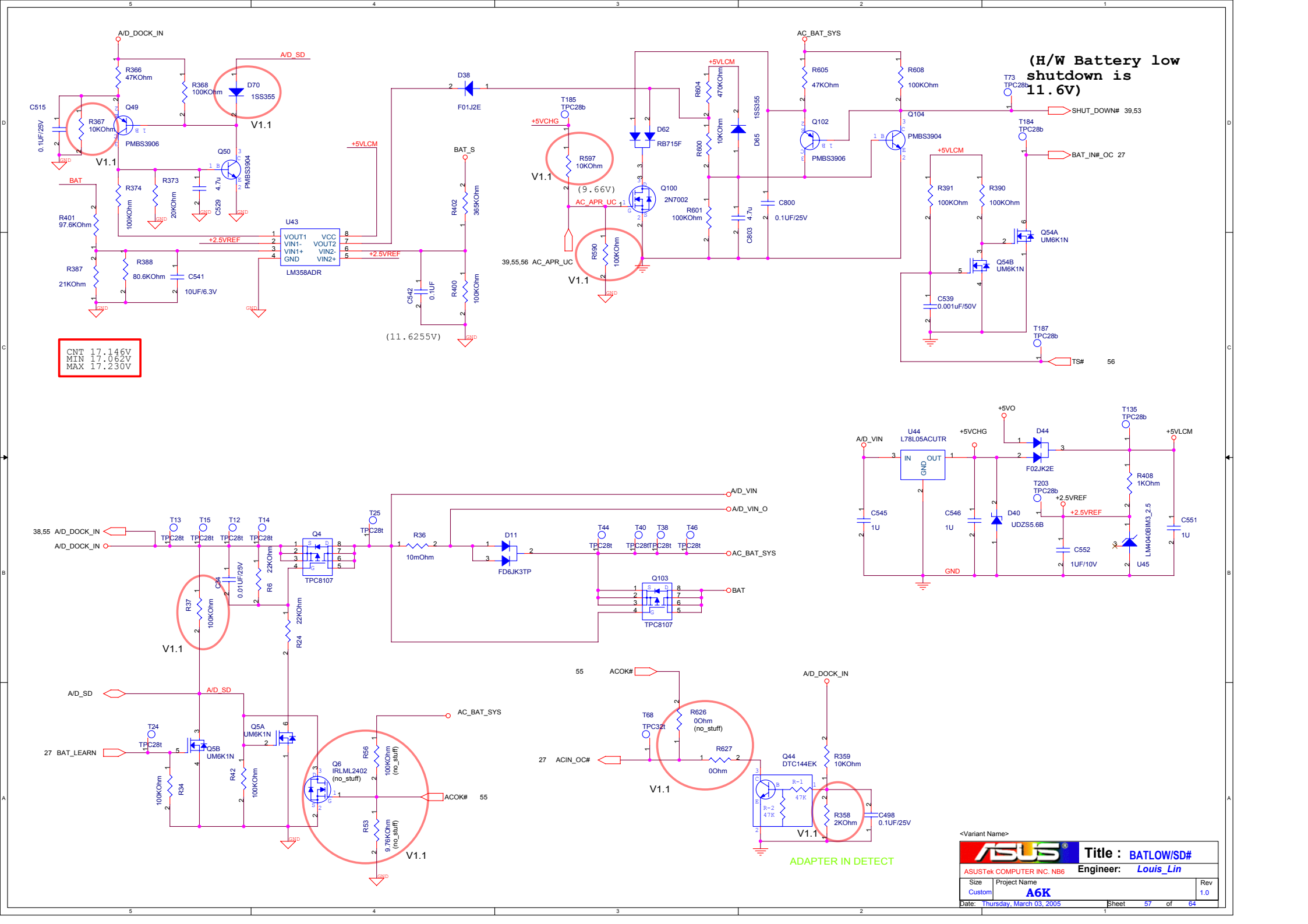
<Variant Name>

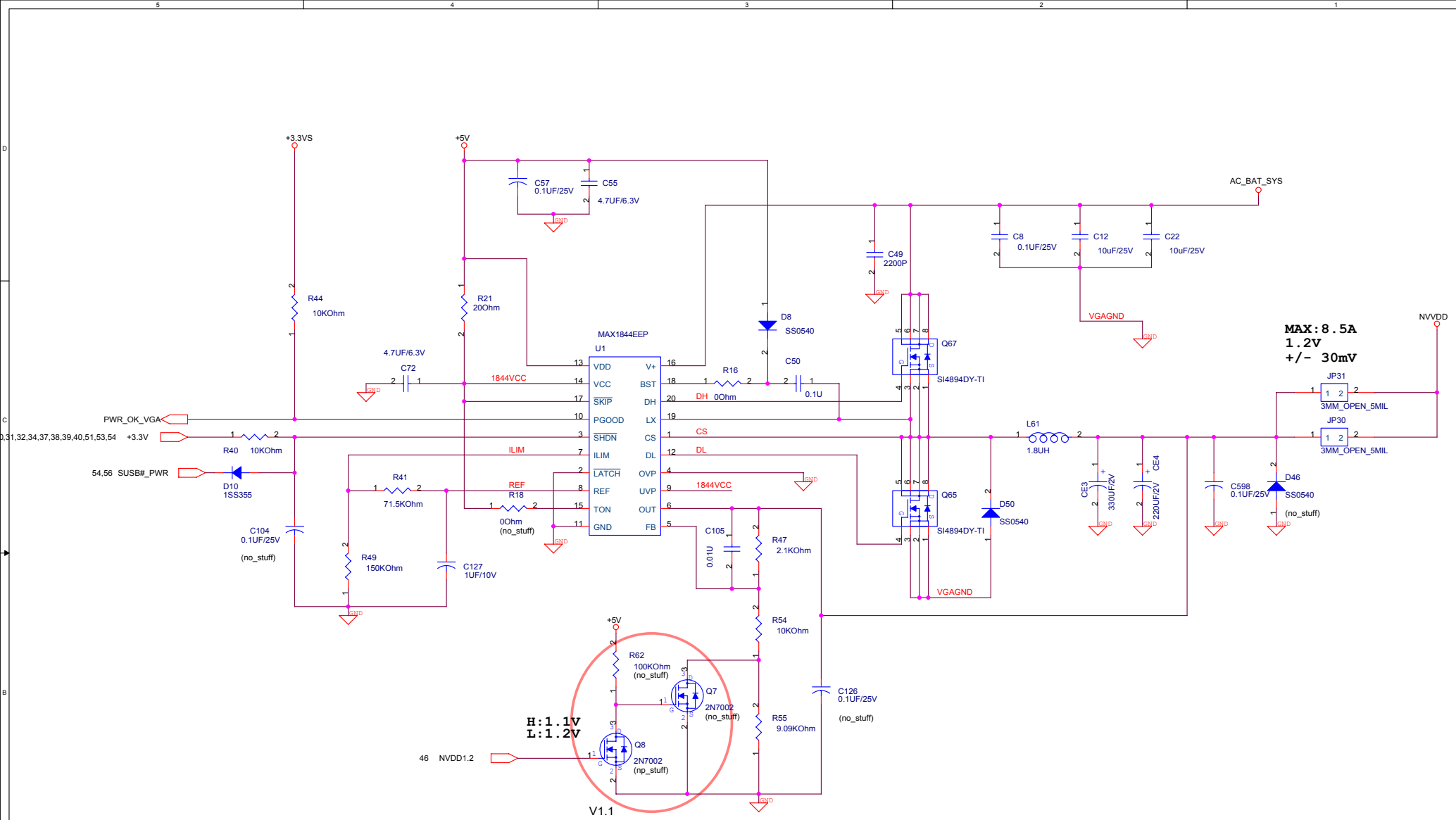
Title : PIC16C54

ASUSTek COMPUTER INC. NB6 Engineer: Louis_Lin

Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 56 of 64


(H/W Battery low shutdown is 11.6V)
A/D_DOCK_IN
A/D_SD
AC_BAT_SYS
BAT_S
BAT
+5VLCM
+2.5VREF
+5VCHG
AC_APR_UC
SHUT_DOWN# 39,53
BAT_IN#_OC 27
TS# 56
39,55,56 AC_APR_UC
LM358ADR
PMBS3906
PMBS3904
TPC8107
F01J2E
RB715F
2N7002
1SS355
F02JK2E
UDZS5.6B
L78L05ACUTR
LM4040BIM3_2.5
CNT 17.146V
MIN 17.062V
MAX 17.230V
(9.66V)
(11.6255V)
V1.1
A/D_VIN
A/D_VIN_O
38,55 A/D_DOCK_IN
27 BAT_LEARN
ACOK# 55
27 ACIN_OC#
ADAPTER IN DETECT
<Variant Name>
Title : BATLOW/SD#
ASUSTek COMPUTER INC. NB6
Engineer: Louis_Lin
Size Custom
Project Name A6K
Rev 1.0
Date: Thursday, March 03, 2005
Sheet 57 of 64



<Variant Name>

Title : VGACORE

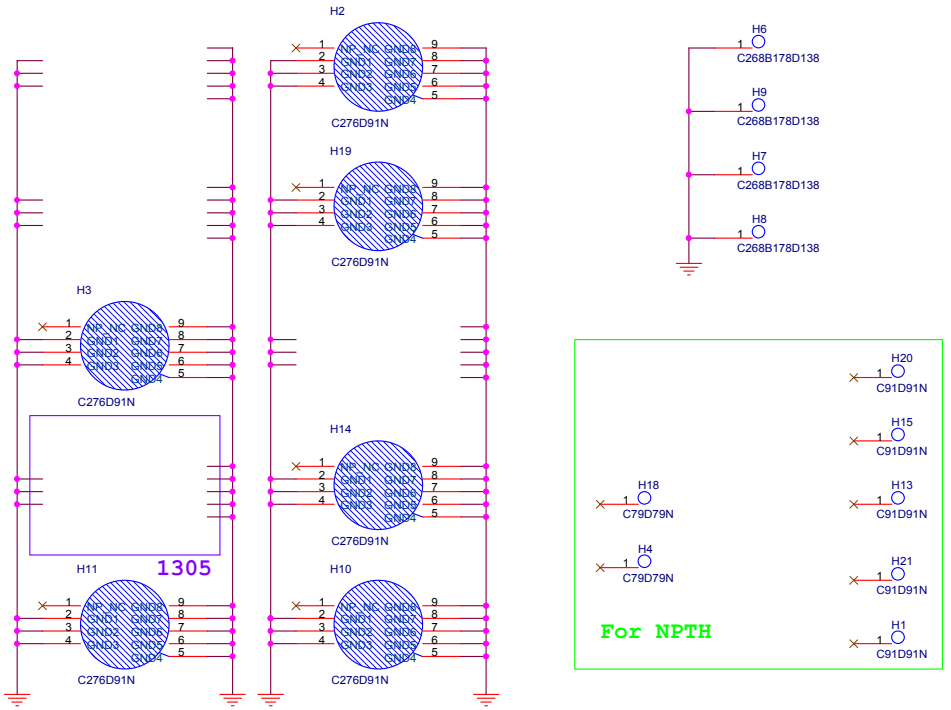
ASUSTek COMPUTER INC. NB6

Engineer: Louis_Lin

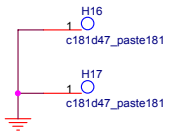
Size	Project Name	Rev
Custom	A6K	1.0

Date: Thursday, March 03, 2005 Sheet 58 of 64

SCREW HOLE

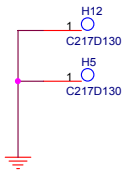


For MDC module



P/N 13-N7510M270

For NB fix sink



P/N 13-NCF10M010

For NV44M-V fix sink

CPU Throttling(BIOS setting): 90 degree C.
System shutdown(BIOS setting) : 100 degree C.
H/W shutdown(page 44, U47 , no load) : 105 degree C.

Short Pad location:
Page39: JP4,5,15,16,19,26,27
Page40: JP6,7,9,22,24
Page42: JP13,14,17,18,28,29

Don't Short Pad: JP26

JP4:+V2.5 --Power In
JP5:+V1.25S
JP6:+V2.5
JP7:+V1.2S
JP9:+VCCP
JP13:+V5S
JP14:+V5
JP15:+V1.5SUS
JP16:+V2.5 --Power IN
JP17:+V1.8S
JP18:+V12
JP19:+V1.8
JP22:+V1.5S
JP24: VREF5-->+V5A
JP26:+3VALWAYS_T-->+V3.3A(open)
JP27:+3VALWAYS_M-->+V3.3A(short)
JP28:+V3.3S
JP29:+V3.3

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 GND
L4 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	20 mils

37.5 OHM	WIDTH
TOP/BOT	12 mils

42 OHM	WIDTH
TOP/BOT	10 mils

55 OHM	WIDTH
TOP/BOT	5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	7 mils/ 10 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

PCI_GNT#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD16

PCI_INT#

CB&1394	PCI_INTB/A/D#
MINIPCI	PCI_INTC/D#
LAN	PCI_INTC#

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3S_CLK
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+V3.3SUS
VRM_PWRGD	I	+V3.3S
PM_STPCPU#	O	+V3.3S
CHG_LED	I	+5VLCM
RST_BTN#	O	OD
OTP_RESET#	I	+V5
SHUT_DOWN#	I	AC_BAT_SYS
+5VLCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3SUS
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_FULL_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3S
AC_APR_UC	I	+V5A
+V5A	PWR	VREF5
3V_ON	O	OD
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT	IO	+V3.3
SMD_BAT	IO	+V3.3

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.4A(Max),1A(Real)
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5SUS	1.5V	64 mA
+V1.8	1.8V	0.14A
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

<Variant Name>

Title : SCREW HOLE

ASUSTek COMPUTER INC. NB6 Engineer:

Size	Project Name	Rev
Custom	A6U	1.0

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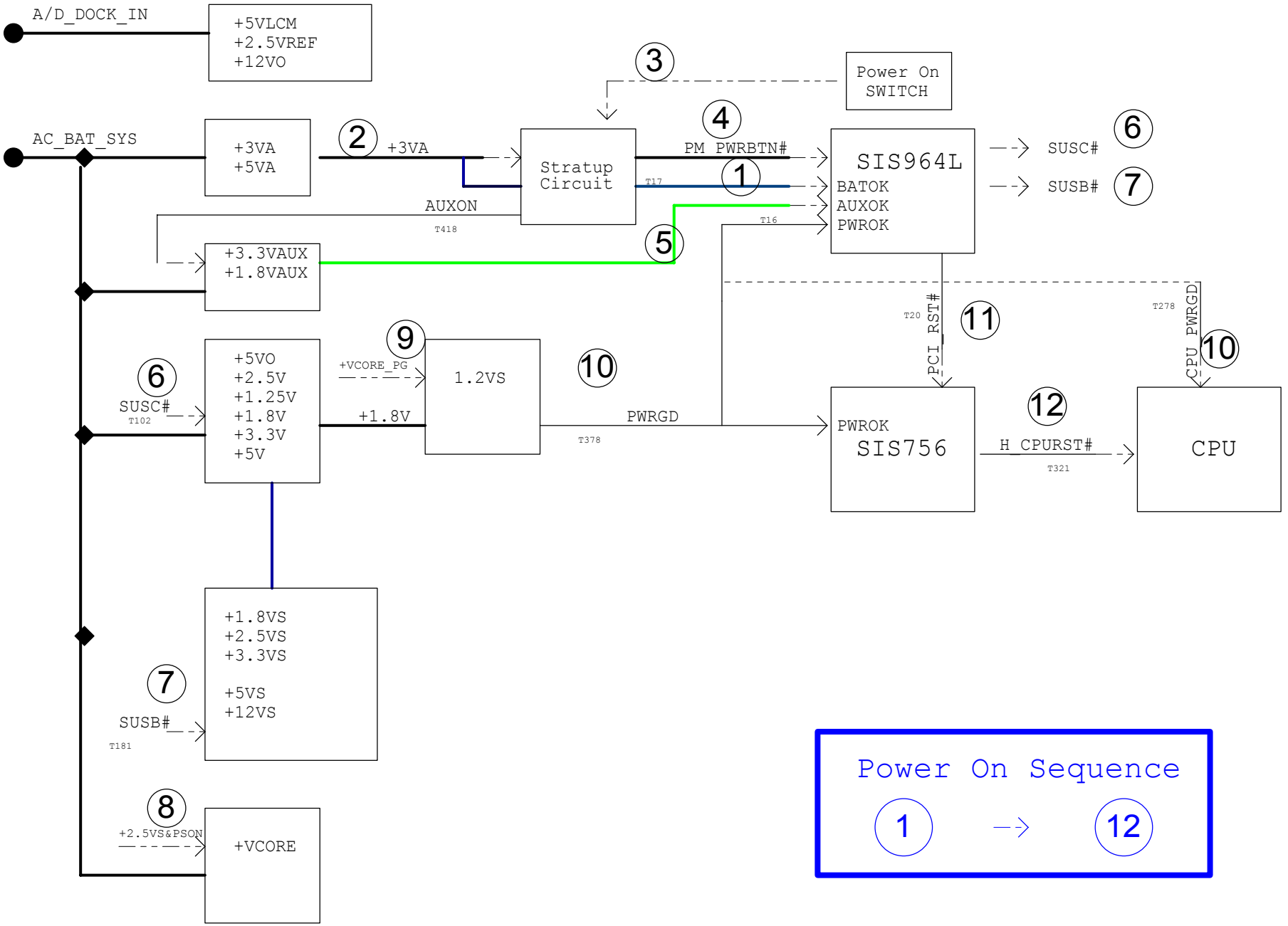

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ASUSTeK COMPUTER INC		Title : Power On Sequence	
		Engineer:	
Size: Custom	Project Name: A6K		Rev: 1.0
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PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN_RTL8100CL	AD22	2	D
CARD READER	AD21	0	B
CARDBUS	AD21	0	C
1394	AD21	0	D
MINIPCI (802.11a/b/g)	AD20	1	C,D

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010010x (A4)
Thermal Sensor (SA56004)	0101110x (5C)
PIC	1001001x (92)

SiS964L GPIO	SIGNAL NAME	I/O	Volt
GPIO 0		P-U	+3.3VS
GPIO 1	NV_THERM#	INPUT	+3.3VS
GPIO 2	THRM_ALERT#	INPUT	+3.3VS
GPIO 3	EXTSMI#	INPUT	+3.3VS
GPIO 4	PM_CLKRUN#	OUTPUT	+3.3VS
GPIO 5		P-U	+3.3VS
GPIO 6	CPUFAN_SPD_A	INPUT	+3.3VS
GPIO 7	BACK_OFF#	OUTPUT	+3.3VAUX
GPIO 8	PM_RI#	INPUT	+3.3VAUX
GPIO 9	KBDSCI_3A	INPUT	+3.3VAUX
GPIO 10	LID_963#_3A	INPUT	+3.3VAUX
GPIO 11	PM_STPPCI#	OUTPUT	+3.3VAUX
GPIO 12	PM_STPCPU#	OUTPUT	+3.3VAUX
GPIO 13	SIO_SMI#	INPUT	+3.3VAUX
GPIO 14	S3AUXSW#	OUTPUT	+3.3VAUX
GPIO 15	BT_ON	P-L	+3.3VAUX
GPIO 16	802_LED_EN#	OUTPUT	+3.3VAUX
GPIO 17	WLAN_ON#	OUTPUT	+3.3VAUX
GPIO 18	CB_SD#	OUTPUT	+3.3VAUX
GPIO 19	SM_CLK	OUTPUT	+3.3VS
GPIO 20	SM_DATA	I/O	+3.3VS
GPIO 21		NC	+3.3VAUX
GPIO 22		NC	+3.3VAUX
GPIO 23		P-L	+3.3VAUX
GPIO 24		P-U	+3.3VAUX

KBC GPIO	A6K	
P23	OP_SD#	
P22	BAT_LEARN	
P21	(KB_P21)	
P20	KBCRSM	
P42	(WATCHDOG)	
P43	CHG_FULL_OC	
P44	KB_CPURST	
P45	KB_GATEA20	
P46	KBCSCI	
P47	PM_CLKRUN#	
P50	KBC_BAT_LLOW#	
P51	KEYDETECT1	
P52	KEYDETECT2	
P53	CLR_DJ#	
P54	BAT_SEL	
P55	BAT1_IN#_OC	
P56	(FAN_DA1)	
P57	ADJ_BL	
P67	DJ_LED#	
P66	SWDJ_EN#	
P65	+VCORE	
P64	ACIN_OC	
P63	DISTP	
P62	MARATHON#	
P61	INTERNET#	
P60	EMAIL#	
P75	(KB_CLK)	
P74	(MS_CLK)	
P73	TPAD_CLK	
P72	(KB_DAT)	
P71	(MS_DAT)	
P70	TPAD_DAT	
P77	BAT_SMC	
P76	BAT_SMD	
P27	SCROLLLOCK#	
P26	NUM_LED#	
P25	CAP_LED#	
P24	SET_PLTRSTNS#	
P40	EXT_SMI	
P41	EMAIL_LED#	

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Brad Lu

Size	Project Name	Rev
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FIRST SOURCE	SECOND SOURCE	NOTE
05-001005111	05-001017122	L5 NA10643
	05-001005310	
06-006002411	06-006002001	
06-010008000	06-010008100	L5 NA10601
06-017001000	06-017001200	
07-005000010	07-005000210	L5 NA10473
	07-005000410	
07-005261010	07-005357010	Power RD Request
07-010303271	07-010303273	L5 NA10603
07-010Q02501	07-010812500	
07-014150220	07-014150120	
07-016202032	07-016402032	
	07-016102032	
09-013103013	09-013103010	L5 NA10512
09-091090000	09-091090001	L5 NA10512
	09-091090005	
10-093111041	10-093111040	L5 NA10334
10-124901000	10-12490100A	L5 NA10298
10-12490560A	10-124905600	
11-032310661	11-032310662	For MC request
	11-032310663	
11-033410400	11-033410401	Follow L5G R2.0 2nd source
	11-033410405	
	11-033410406	
11-033410500	11-033410502	
11-03B210620	11-031110621	L5 NA10407
	11-031210621	*11-03B110623 for Power RD Request
	11-03B110621	
	11-03B110622	
	11-03B210621	
	11-03B110623	

ASUSTek COMPUTER INC. NB6

Title : SECOND SOURCE

Engineer:

Size	Project Name	Rev
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REVISION LIST

POWER INTERFACE

SIGNALS	TYPE	POWER

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.55V	27.3A
+1.25V	1.25V	0.725A
NVVDD	1.1/1.2V	8.62A
+2.5V	2.5V	5.55A
+1.8VAUX	1.8V	50mA
+1.2P_VS	1.2V	1.875A
+1.2VS	1.2V	635mA
+1.8VS	1.8V	2.521A
+1.8V	1.8V	415 mA
+1.8FB_VS	1.8V	2A
+2.5VS	2.5V	0.035A
+3.3V	3.3V	1.925A
+3.3VS	3.3V	2.955A
+5VS	5V	4.7A
+5V	5V	3.865A
+5VA	5V	0.05A
+12V	12V	0.05A
+12VS	12V	0.01A
+3.3VAUX	3.3V	0.417A
+3VA	3.3V	0.02A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	22 mils
IN1/IN3	16 mils

37.5 OHM	WIDTH
TOP/BOT	13.5 mils
IN1/IN3	10 mils

42 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN3	8.5 mils

55 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN3	5 mils

75 OHM	WIDTH
TOP/BOT	2.5 mils
IN1/IN3	2 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	8 mils/ 4 mils
IN1/IN3	8 mils/ 3.5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 5 mils
IN1/IN3	5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	4 mils/ 6 mils
IN1/IN3	4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1
LAN	PCI_REQ#2

IDSEL

CB&1394	PCI_AD21
MINIPCI	PCI_AD20
LAN	PCI_AD22

PCIE Device

PEG

NVIDIA NV44M

PCIE Giga NIC

N/A

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 VCC
L3 IN1
L4 IN2
L5 GND
L6 BOT

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SIGNAL	IN:	AVID[0:4]
		CORE_ON
		COREFB
		COREFB#
	OUT:	+VCORE_PG
POWER	IN:	AC_BAT_SYS
		+5VO
		+3.3VS
	OUT:	+VCORE

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SIGNAL	IN:	VLDT_ON
		+2.5VREF
		SUSC#_PWR
	OUT:	DDR_PWRGD
		+1.2VS_PG
POWER	IN:	+5VAO
		+12V
		+3VO
		+3VAUX
		+2.5VO
		+1.25V
		+3.3V
		+5VO
		+1.8VO
	OUT:	+3VA
		+1.8VAUX
		+1.25V
		+1.2VS
		+1.2P_VS

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SIGNAL	IN:	SUSC#_PWR
	OUT:	2.5V_1.8V_PG
POWER	IN:	AC_BAT_SYS
		+3.3VS
		+5VAO
	OUT:	+2.5V
		+1.8V

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SIGNAL	IN:	SUSC#_PWR
		OTP_RESET#
		SHUT_DOWN#
		AUX_ON
	OUT:	3V_5V_PWRGD
POWER	IN:	AC_BAT_SYS
		+3VA
		+3.3VS
		+VCC_GMCH_CORE
		+5VAO
	OUT:	+5VA
		+5VO
		+12VO
		+3VO

ASUSTeK COMPUTER INC

Title : REVISION LIST

Engineer: Brad Lu

Size	Project Name	Rev
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Rev	Date	Description
R1.00	04/6/28	1. Initial release.
R1.1	02/14/05'	1.R14&R15 be changed from 75 ohm to 49.9 ohm,P-9.follow SIS. 2.Q26A be changed to "D67" to prevent body diode leakage current,p-39. 3.Q26B be changed to "Q107",P-39. 4.R453&R475 be changed from 10kohm to 6.81kohm,P-49.follow NVIDIA. 5.R578 & C758 be changed to mounting. 6.JP32 CON pin definition be corrected. 7.Enable R5C841 internal regulator,P-22. VCC_RIN= +3.3V 8.C769 be changed from 0.1uf to 0.47uf,P-22. globe reset timing. 9.Audio Jack "J5" be changed from "12-140001088" to "12-140001081",P-32. 10.C665,C666,C659,C655,C643,C648 be changed from 330pf to 5pf,P-15. 11.C4 & C7 be changed from 5pf to 27pf and mounted,P-15
	02/21/05'	1.Added C834,C835,C836 at NVVDD,P-42. reduce ripple. 2.Added R587 and U61 ,P-39. meet K8 CPU power off sequency. 3.Changed U28 power source from +5VA to +3VA,P-39.prevent quiescent current. 4.Changed RN28B pull up power source from +3.3VAUX to +3VA,P-39.prevent quiescent current. 5.Removed Q88B ,P-37.DJ_SW# latched sequency . 6.Q16 and Q45 be changed ,P-28.parts Preparing. 7.Added D68 ,P27.LED flash when ODD running. 8.Added JRST1,P-17. subbattery reset asserted. 9.Added R617 47KOHM pull low ,P-16
	02/22/05'	1.Added R624 and changed R130 from 10k ohm to 47kohm,P-14. white screen when entry and resuming in S3. 2.Added C837,P-42.EMI 3.Changed thermal sensor for cost.
	02/23/05'	1.Changed R29 pin2 power source from +3.3VAUX to +3.3VAUX_NB,P-9.
	02/25/05'	1.CN17/CN18/CN19/CN20/CN33 parts be changed for cost! 2.R264 unmount,p-9.duplicate

Rev	Date	Description

ASUSTek COMPUTER INC. NB6

Title : REVISION(1)

Engineer:

Size	Project Name	Rev
Custom	A6U	1.0

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