

**Z62H**

### EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSV#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	R11#WUI0/GPD0	SUSB#	I
29	R12#WUI1/GPD1	SUSC#	I
30	LPCRST#WUI4/GPD2	PLT_RST#	I
31	ECSC#GPD3	EXT_SC#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#WUI6/GPE6	LID_EC#	I
25	CLKRUN#WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

### ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCL_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCL_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCL_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCL_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCL_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCL_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCL_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCL_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

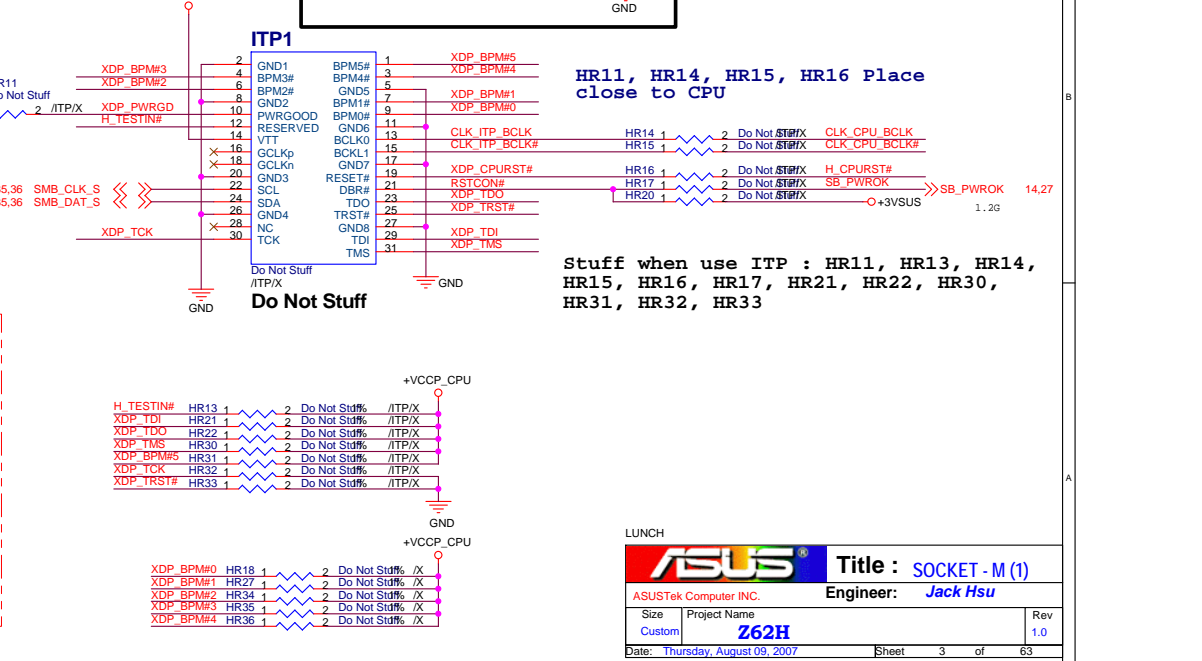
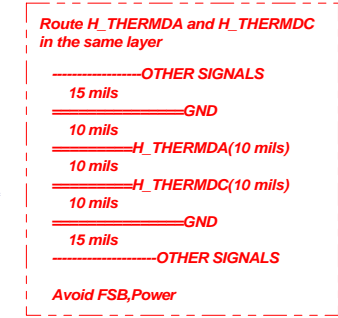
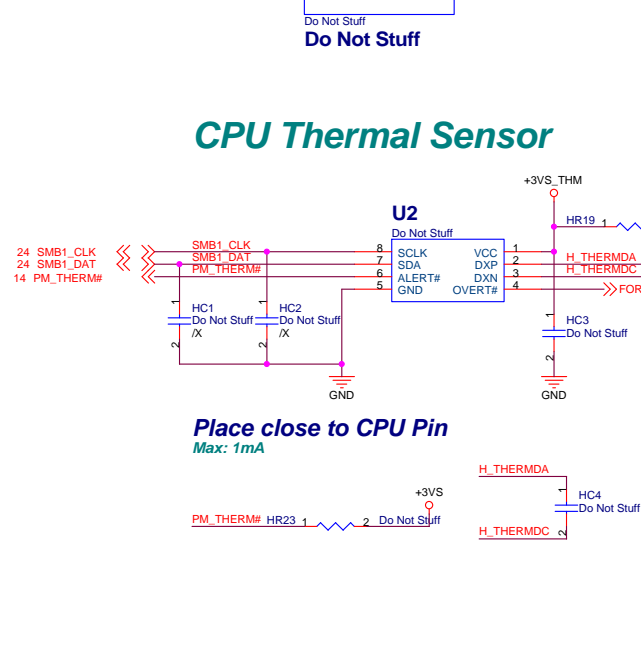
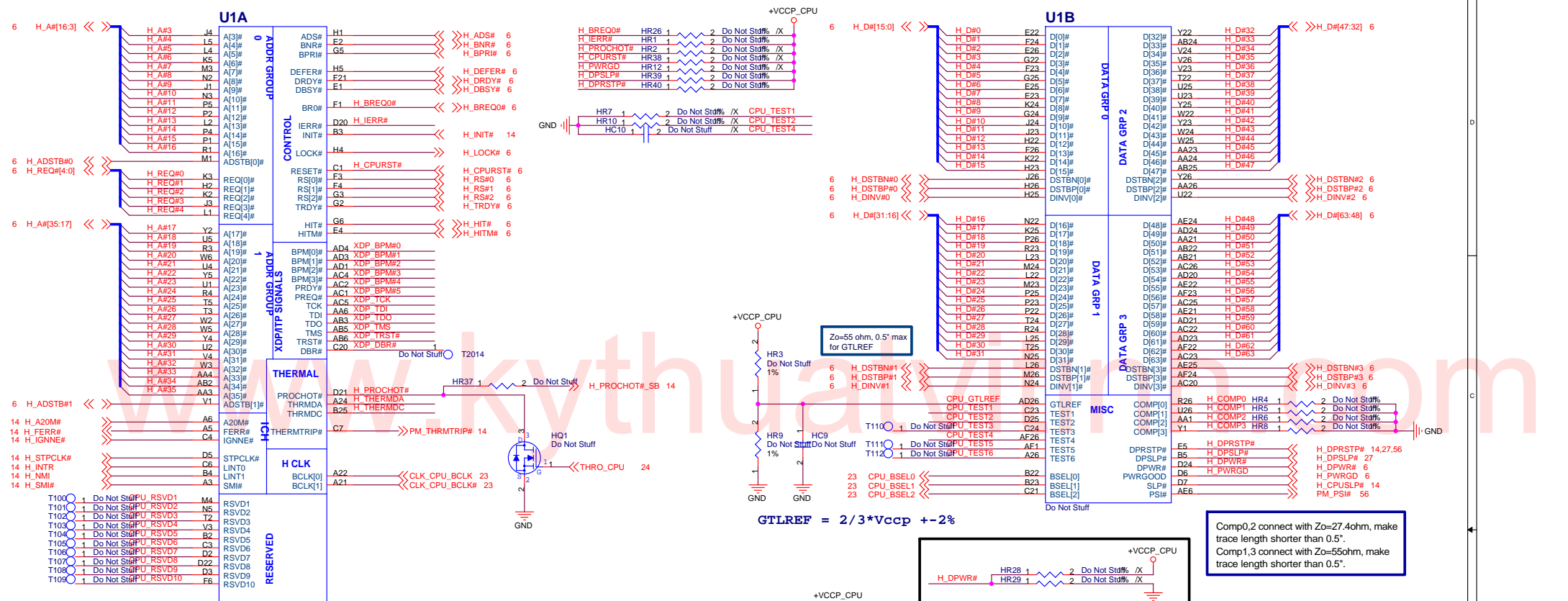
LUNCH

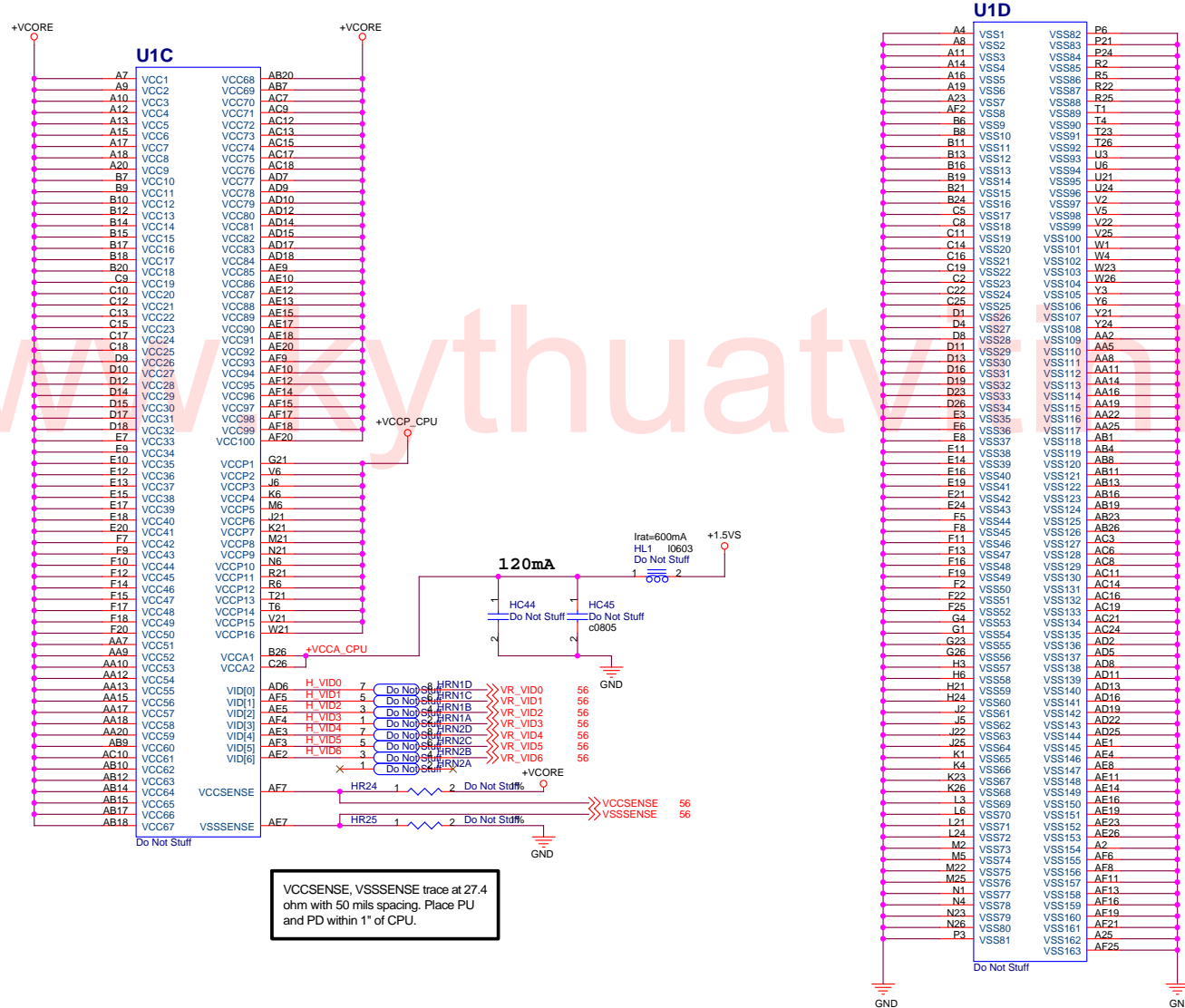


**Title : System Setting**  
**Engineer: Jack Hsu**

ASUSTek Computer INC.  
 Size Project Name  
 Custom **Z62H**

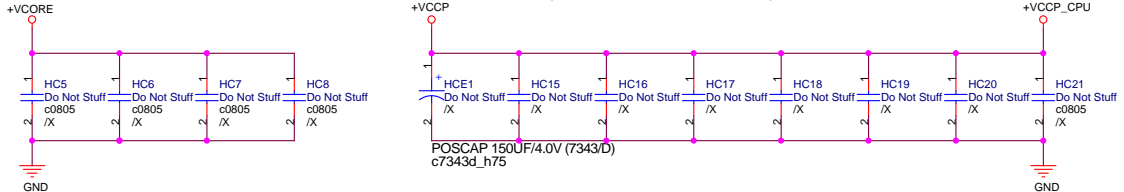
Date: Thursday, August 09, 2007 Sheet 2 of 63 Rev 1.0





VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

**+VCCP Decoupling Capacitor  
(Place near CPU)**

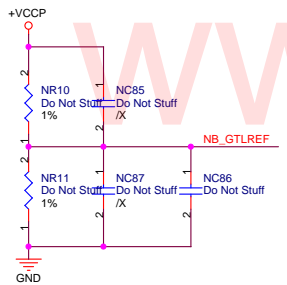
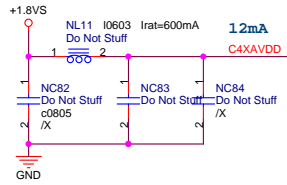
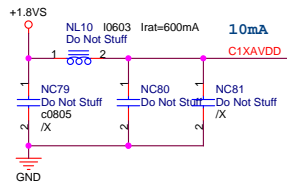


**Non-Stuff**

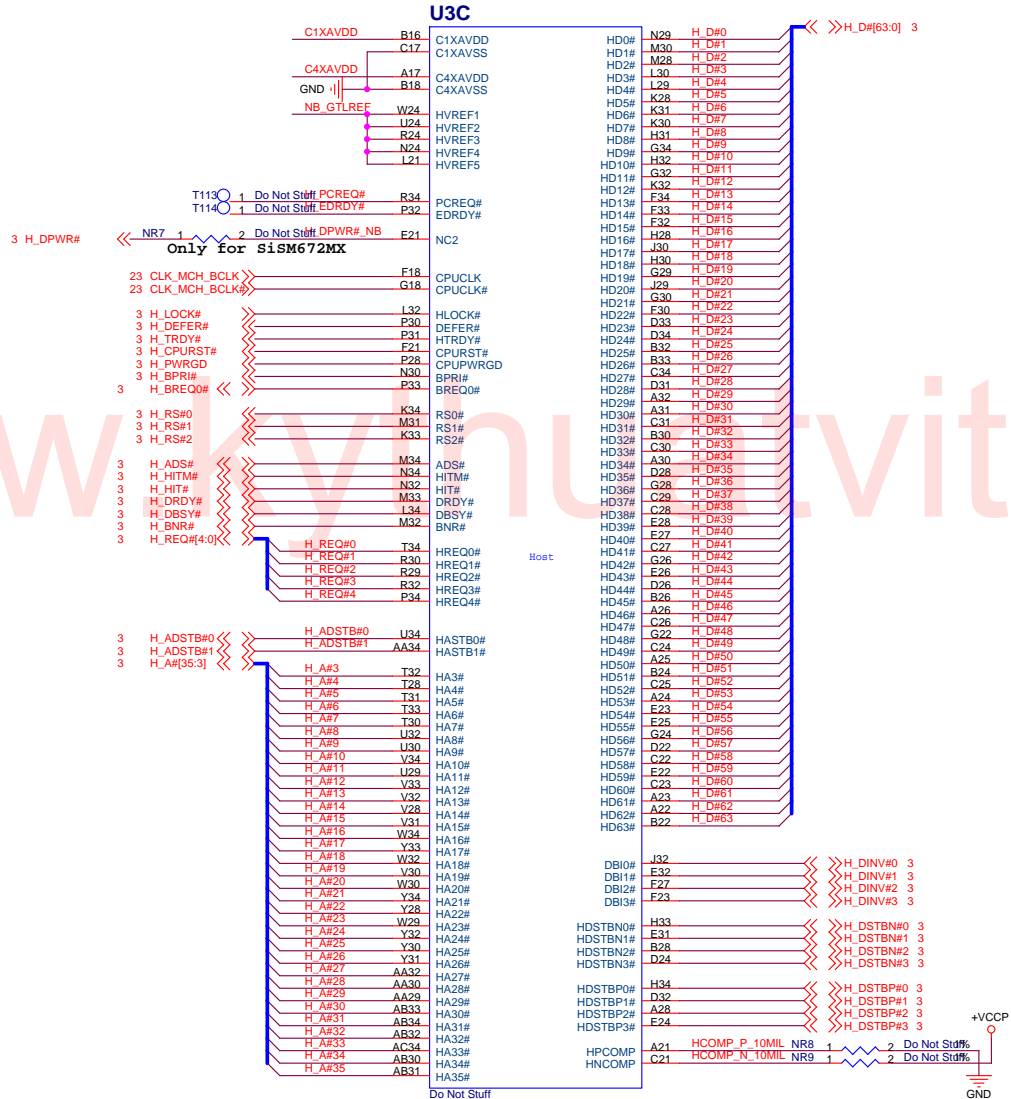
**Decoupling guide from INTEL  
44A for Merom**

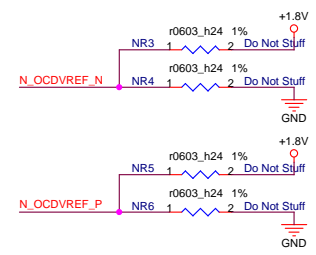
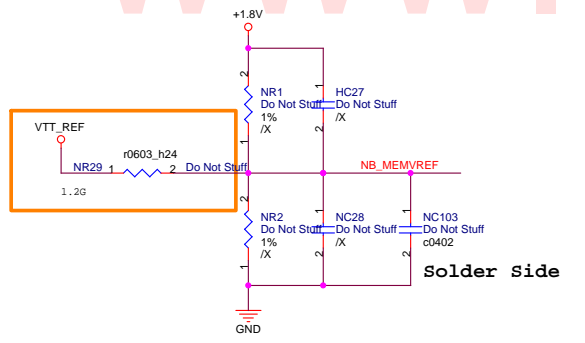
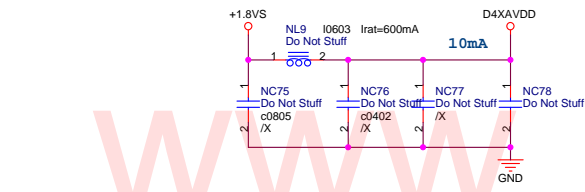
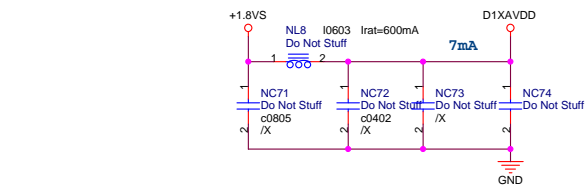
VCORE 22uF/10V \* 32pcs, 330uF/2V \* 6pcs  
VCCP 0.1uF \* 6pcs, 150uF \* 1pcs

www.kythuativinh.com



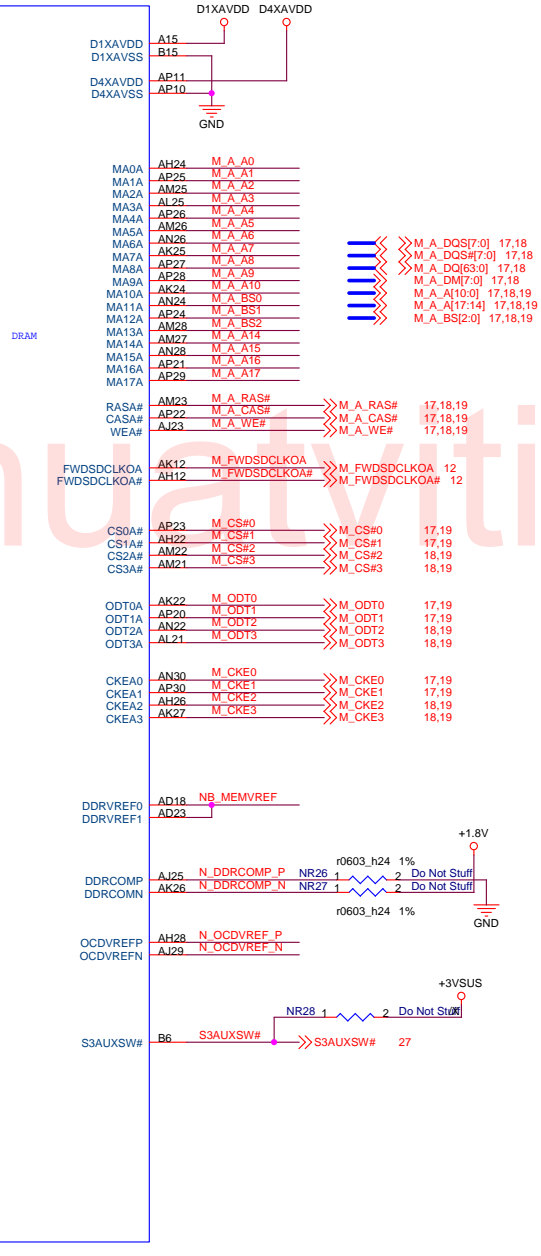
Place 0.1uF under M672 solder side, less 100mils from M672 Pin



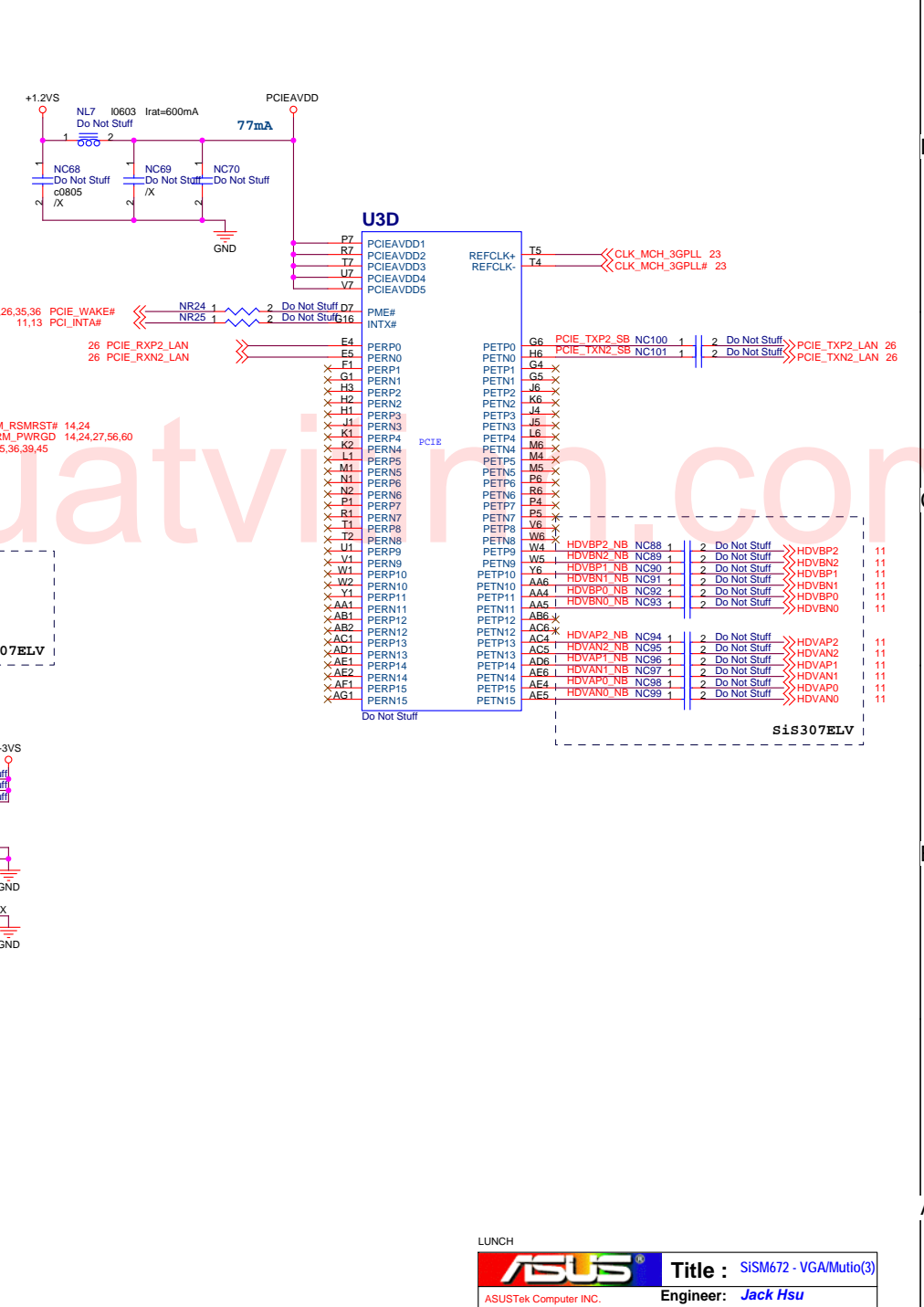
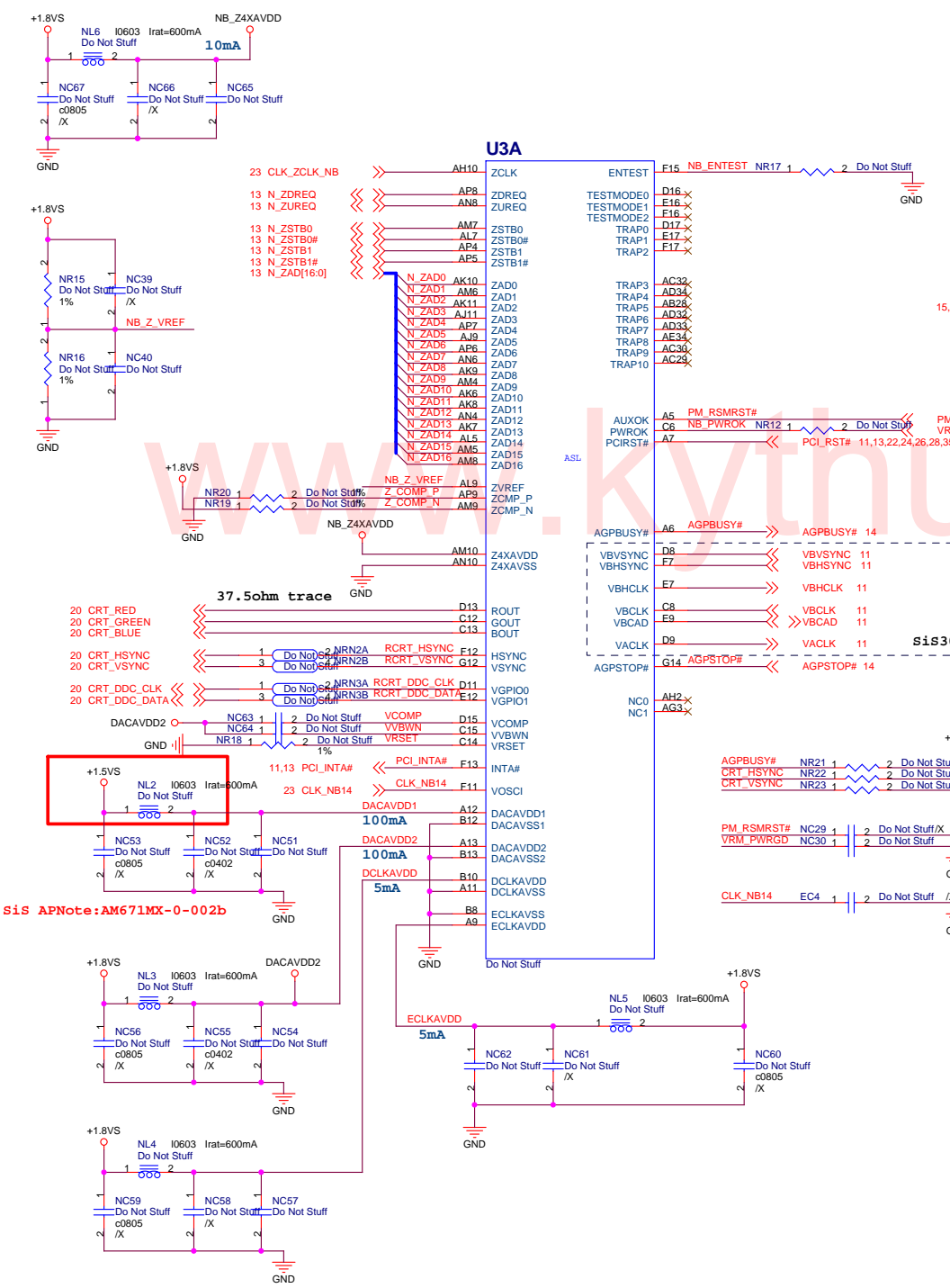


**U3B**

M A DQ0 AD31	MD0A
M A DQ1 AD30	MD1A
M A DQ2 AG34	MD2A
M A DQ3 AE29	MD3A
M A DQ4 AE32	MD4A
M A DQ5 AF34	MD5A
M A DQ6 AF31	MD6A
M A DQ7 AE30	MD7A
M A DM0 AD28	DQM0A
M A DQS0 AF32	DQS0A
M A DQS#0 AF33	DQS0A#
M A DQ8 AF28	MD8A
M A DQ9 AJ34	MD9A
M A DQ10 AH31	MD10A
M A DQ11 AG30	MD11A
M A DQ12 AF30	MD12A
M A DQ13 AG32	MD13A
M A DQ14 AJ32	MD14A
M A DM1 AH34	MD15A
M A DQS1 AH32	DQM1A
M A DQS#1 AH33	DQS1A
M A DQ16 AK34	MD16A
M A DQ17 AH30	MD17A
M A DQ18 AL32	MD18A
M A DQ19 AH33	MD19A
M A DQ20 AK32	MD20A
M A DQ21 AG29	MD21A
M A DQ22 AM34	MD22A
M A DQ23 AH31	MD23A
M A DM2 AJ33	DQM2A
M A DQS2 AK33	DQS2A
M A DQS#2 AL34	DQS2A#
M A DQ24 AK32	MD24A
M A DQ25 AP32	MD25A
M A DQ26 AP31	MD26A
M A DQ27 AM29	MD27A
M A DQ28 AK30	MD28A
M A DQ29 AK28	MD29A
M A DQ30 AJ27	MD30A
M A DQ31 AK28	MD31A
M A DM3 AN32	DQM3A
M A DQS3 AN30	DQS3A
M A DQS#3 AM31	DQS3A#
M A DQ32 AK20	MD32A
M A DQ33 AM20	MD33A
M A DQ34 AH19	MD34A
M A DQ35 AH19	MD35A
M A DQ36 AN20	MD36A
M A DQ37 AJ21	MD37A
M A DQ38 AP19	MD38A
M A DQ39 AH20	MD39A
M A DM4 AK20	DQM4A
M A DQS4 AK19	DQS4A
M A DQS#4 AL19	DQS4A#
M A DQ40 AK18	MD40A
M A DQ41 AH17	MD41A
M A DQ42 AK17	MD42A
M A DQ43 AP16	MD43A
M A DQ44 AH18	MD44A
M A DQ45 AP18	MD45A
M A DQ46 AN18	MD46A
M A DQ47 AP17	MD47A
M A DM5 AM18	DQM5A
M A DQS5 AL17	DQS5A
M A DQS#5 AM17	DQS5A#
M A DQ48 AN16	MD48A
M A DQ49 AK16	MD49A
M A DQ50 AN14	MD50A
M A DQS1 AH15	MD51A
M A DQS2 AP15	MD52A
M A DQS3 AM16	MD53A
M A DQS4 AK15	MD54A
M A DQS5 AH14	MD55A
M A DM6 AH16	DQM6A
M A DQS6 AL15	DQS6A
M A DQS#6 AM15	DQS6A#
M A DQ56 AL13	MD56A
M A DQ57 AM13	MD57A
M A DQ58 AM12	MD58A
M A DQ59 AJ13	MD59A
M A DQ60 AM14	MD60A
M A DQ61 AK14	MD61A
M A DQ62 AN12	MD62A
M A DQ63 AH14	MD63A
M A DM7 AK13	DQM7A
M A DQ67 AP12	DQS7A
M A DQS#7 AP13	DQS7A#



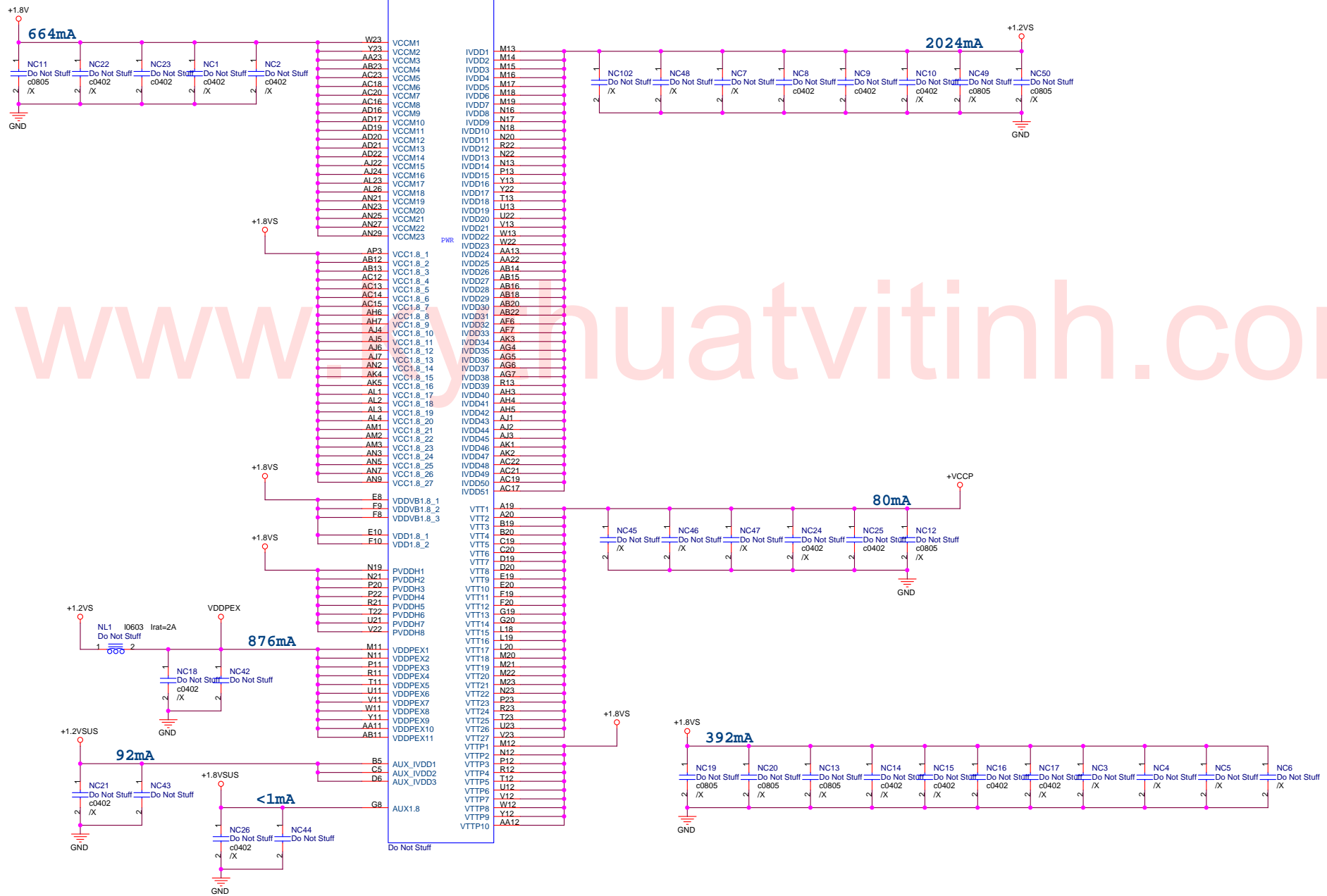
LUNCH



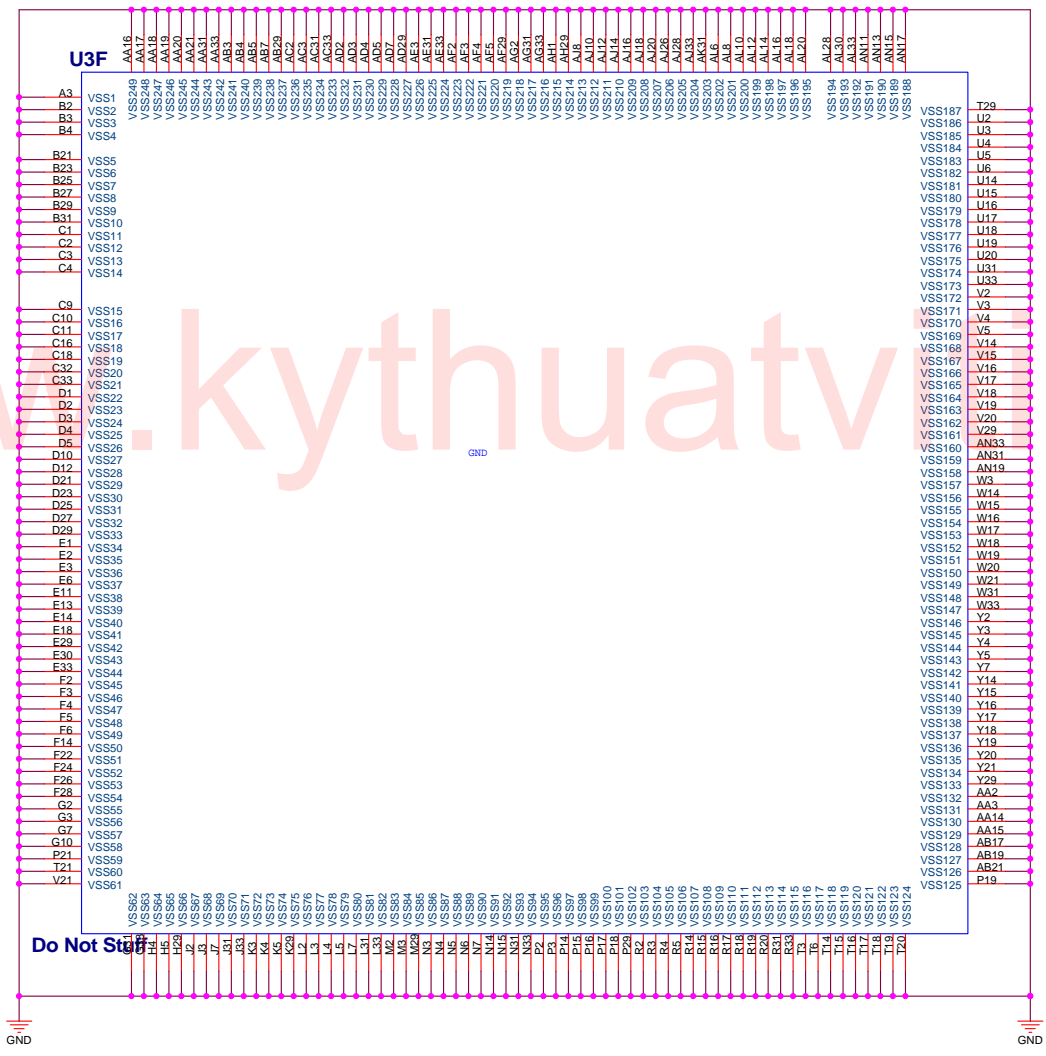
Sis APNote:AM671MX-0-002b

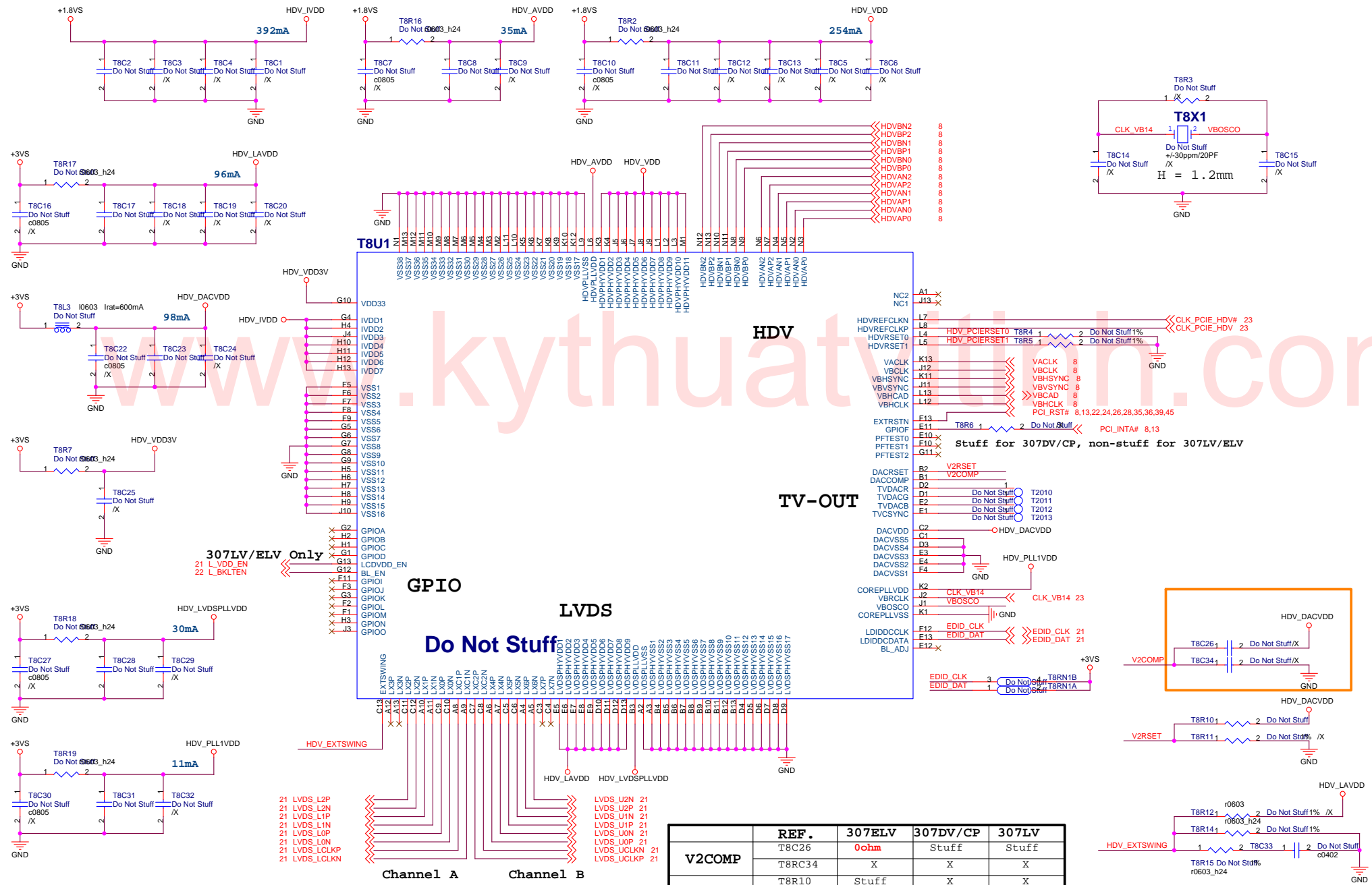


# U3E



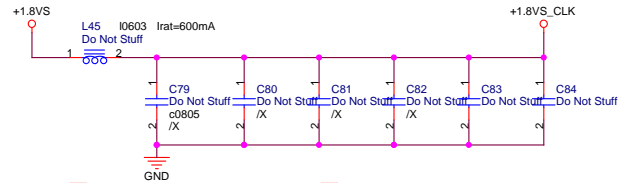
www.kythuatvi.com



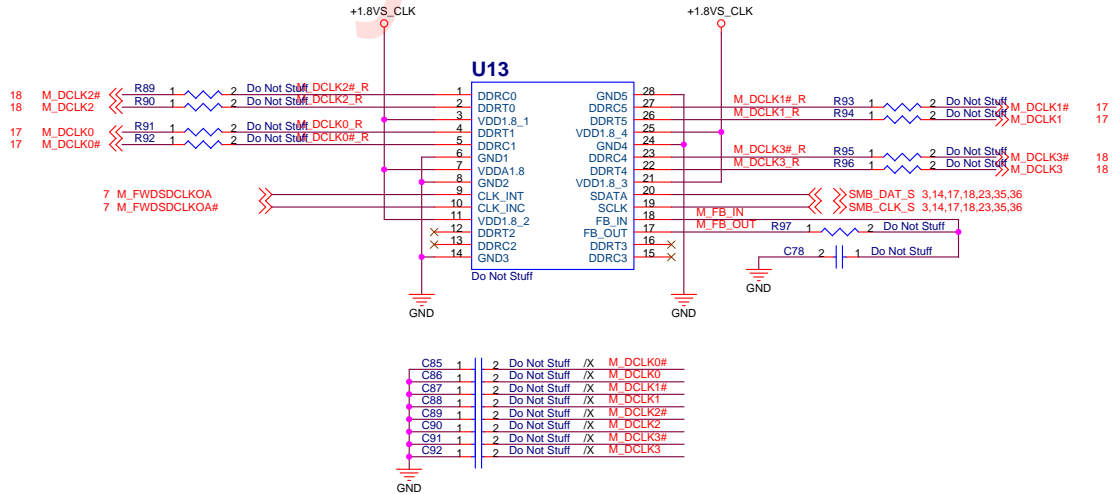


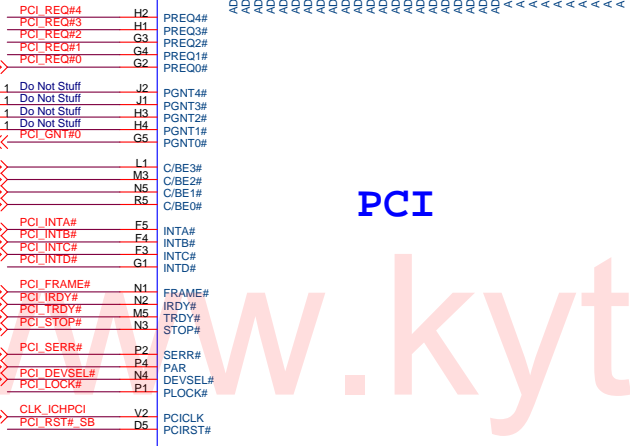
02G020003600 C.S SIS307LVMV(B0) BGA169 SIS SIS307LV  
 02G020003601 C.S SIS307ELV(B0) BGA167 SIS SIS307ELV

	REF.	307ELV	307DV/CP	307LV
V2COMP	T8C26	0ohm	Stuff	Stuff
	T8RC34	X	X	X
V2RSET	T8R10	Stuff	X	X
	T8R11	X	Stuff	Stuff
EXTSWING	T8R12	X	Stuff	X
	T8R14	Stuff	X	Stuff
	T8R15	Stuff	X	Stuff
	T8C33	Stuff	X	Stuff



www.kythuatchitinh.com

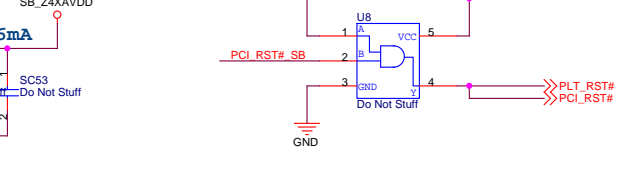
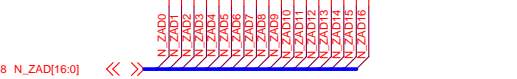
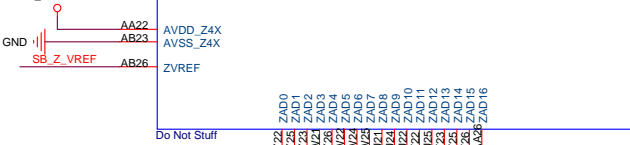




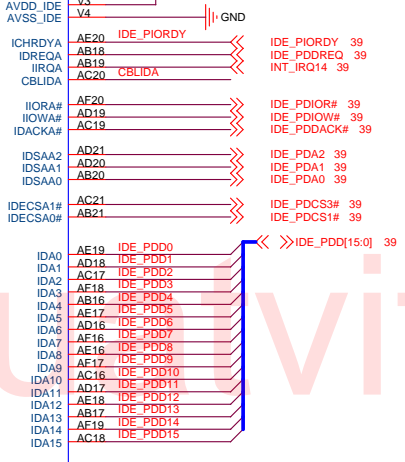
**PCI**



**MuTIOL**

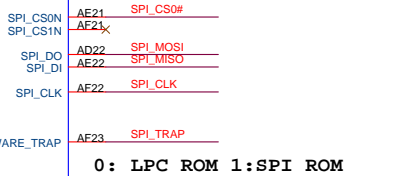


**IDE**

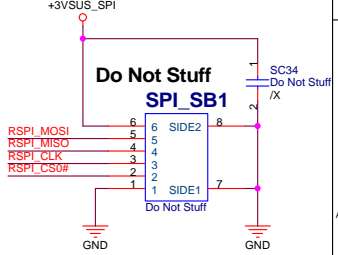
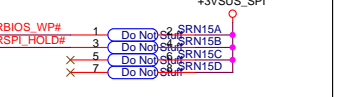
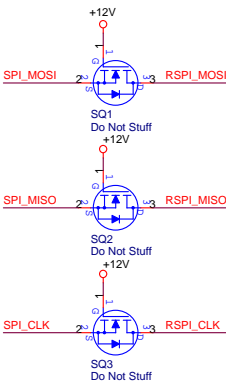
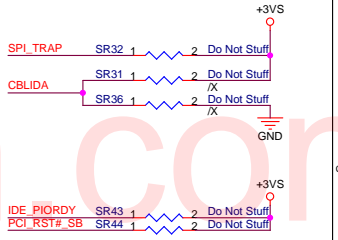
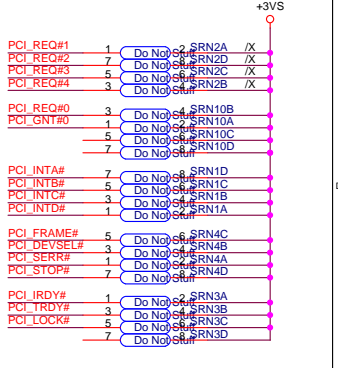
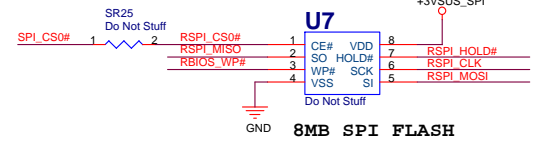


**IDE**

**SPI**

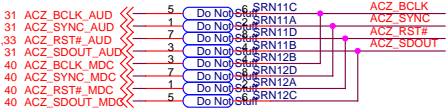
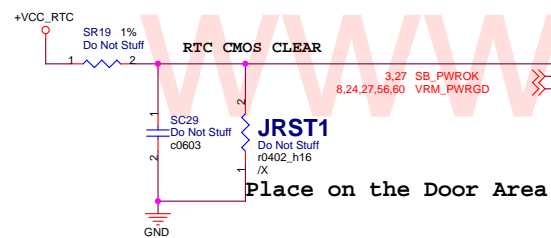
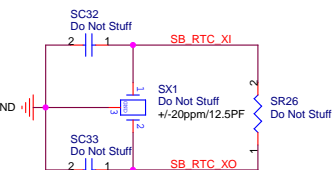
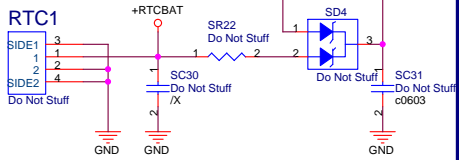


0 : LPC ROM 1 : SPI ROM

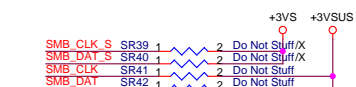
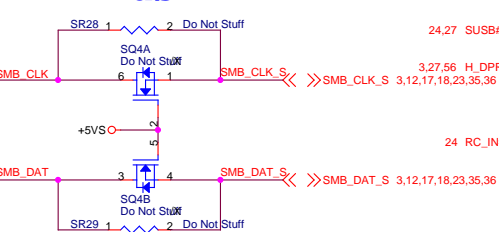


# RTC BATTERY

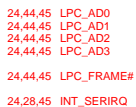
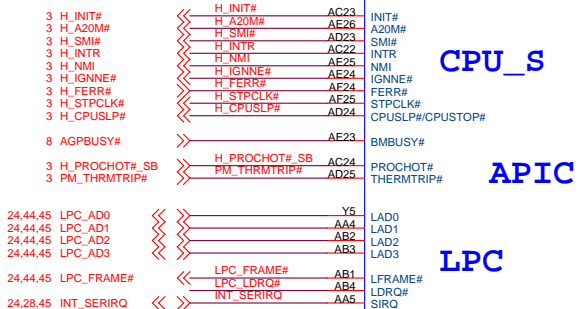
Do Not Stuff



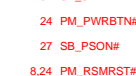
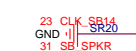
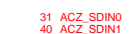
## SMBus



## U6B



Place on the Door Area



## CPU\_S

## APIC

## LPC

## RTC

## SMBUS

## HD Audio

## ACPI/Others

## GPIO



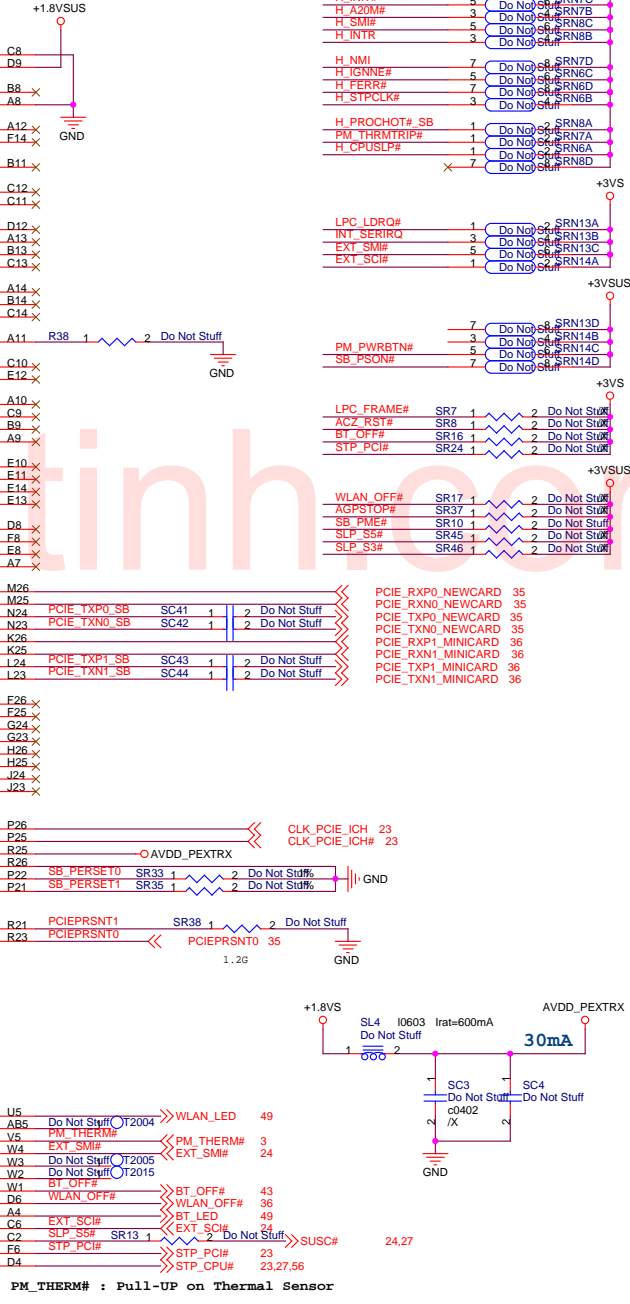
## GMAC

## PCI Express

## HDA\_SDIN2

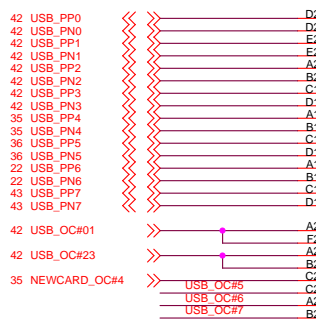
## PM\_THERM# : Pull-UP on Thermal Sensor

## LUNCH



ASUS		Title : SIS968 (1)
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	Z62H	1.0
Date: Thursday, August 09, 2007	Sheet	14 of 63

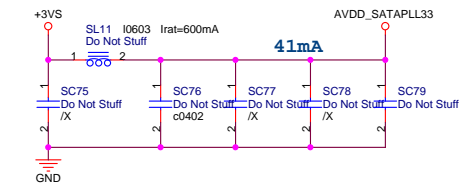
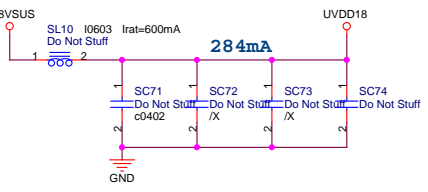
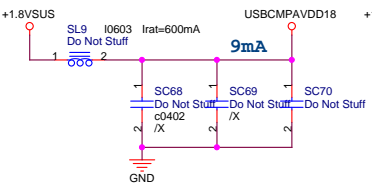
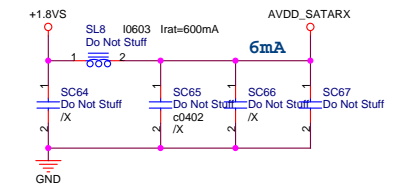
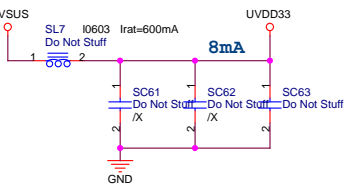
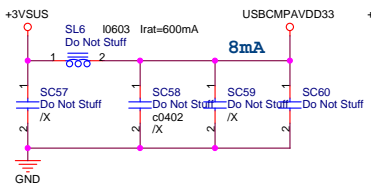
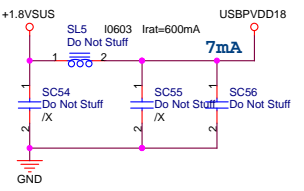
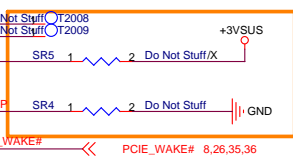
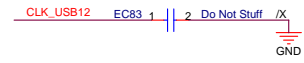
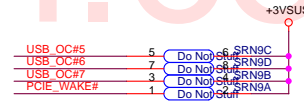
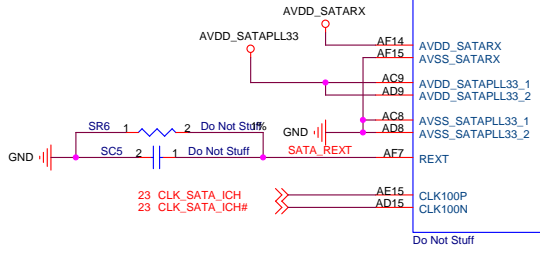
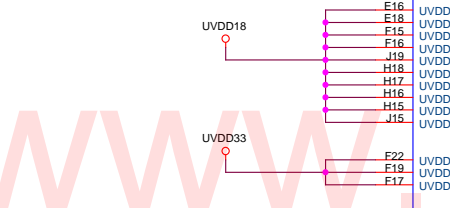
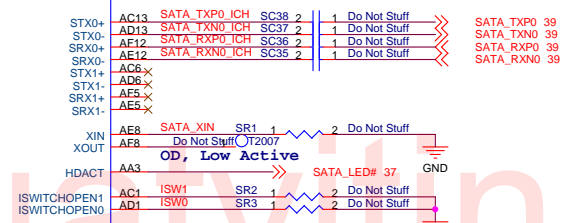
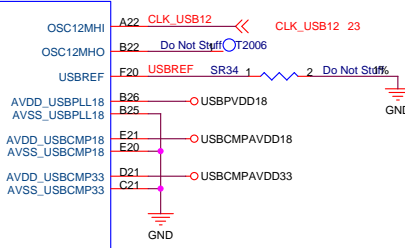
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth



**U6C**

**USB**

**SATA**



LUNCH

**Title : SIS968 (3)**

ASUSTek Computer INC. **Engineer: Jack Hsu**

Size	Project Name	Rev
Custom	<b>Z62H</b>	1.0

Date: Thursday, August 09, 2007 Sheet 15 of 63

# U6D

## Power / Ground

+1.8VS  
522mA

+3VS  
33mA

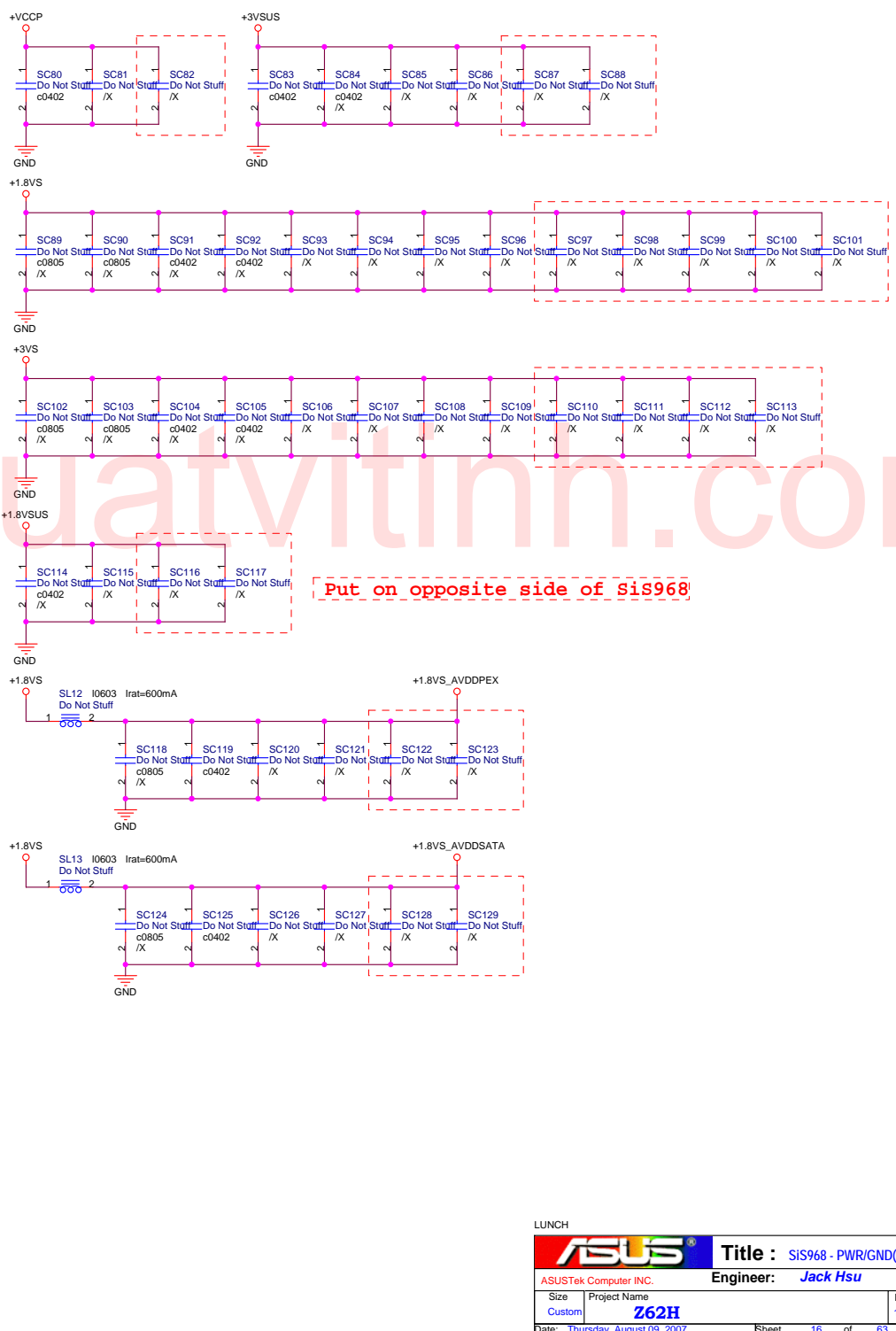
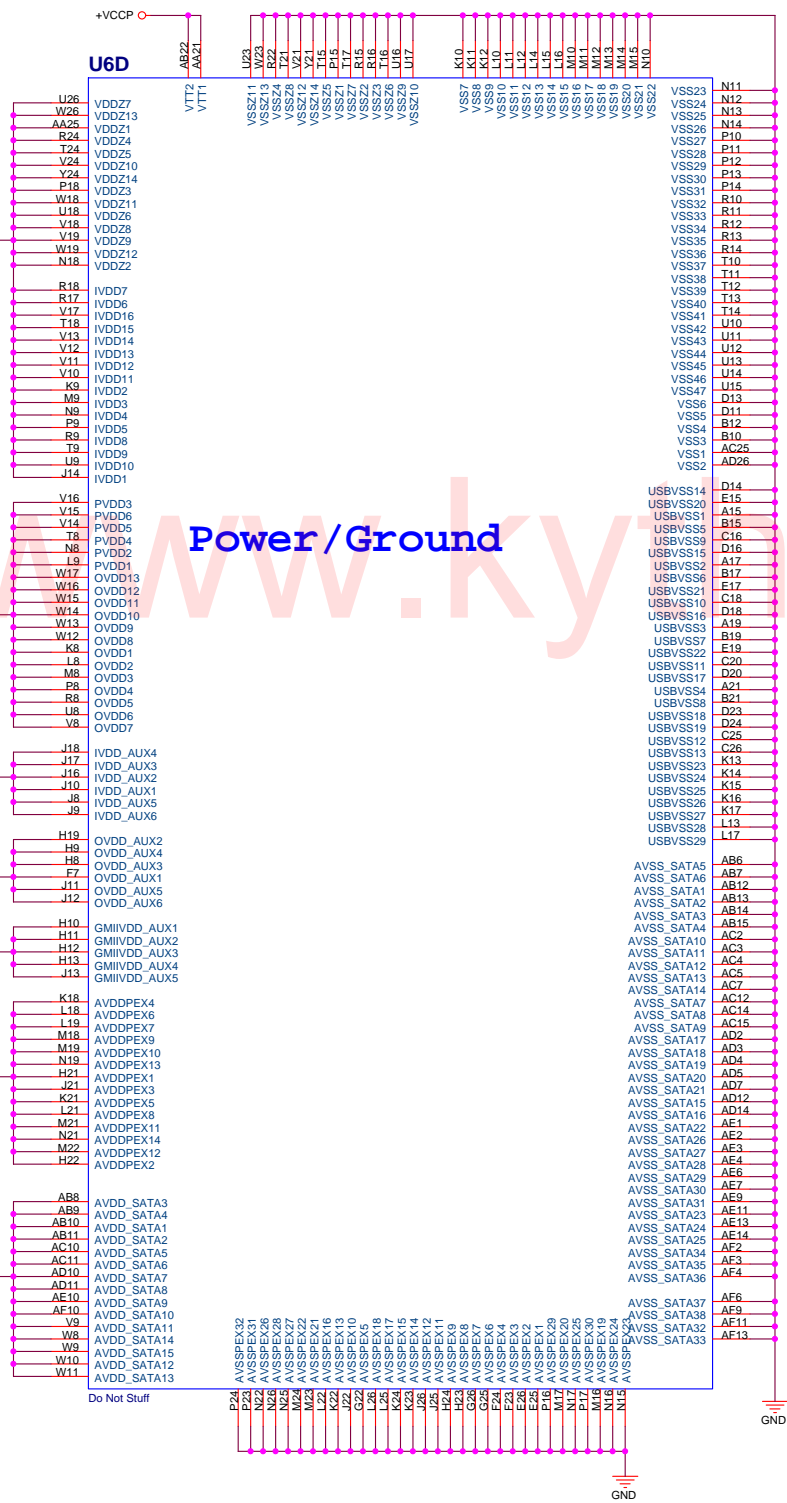
+1.8VSUS  
19mA

+3VSUS  
4mA

+3VSUS  
8mA

+1.8VS\_AVDDPEX  
153mA

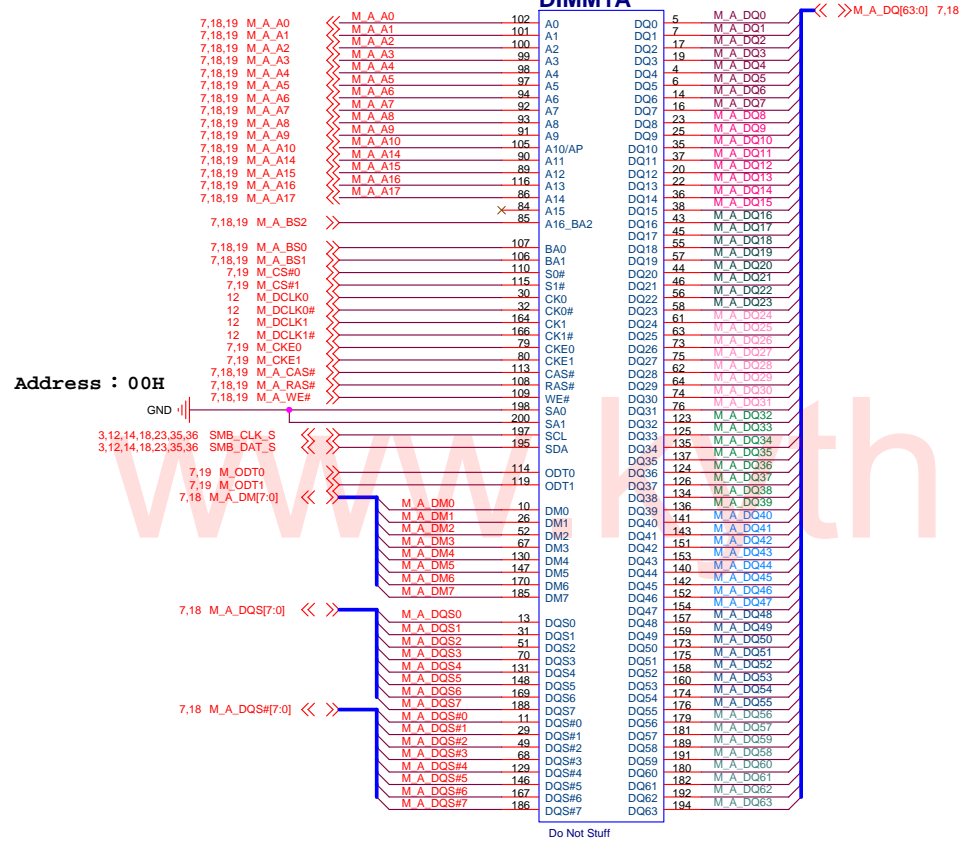
+1.8VS\_AVDDSDATA  
190mA



Put on opposite side of S1S968

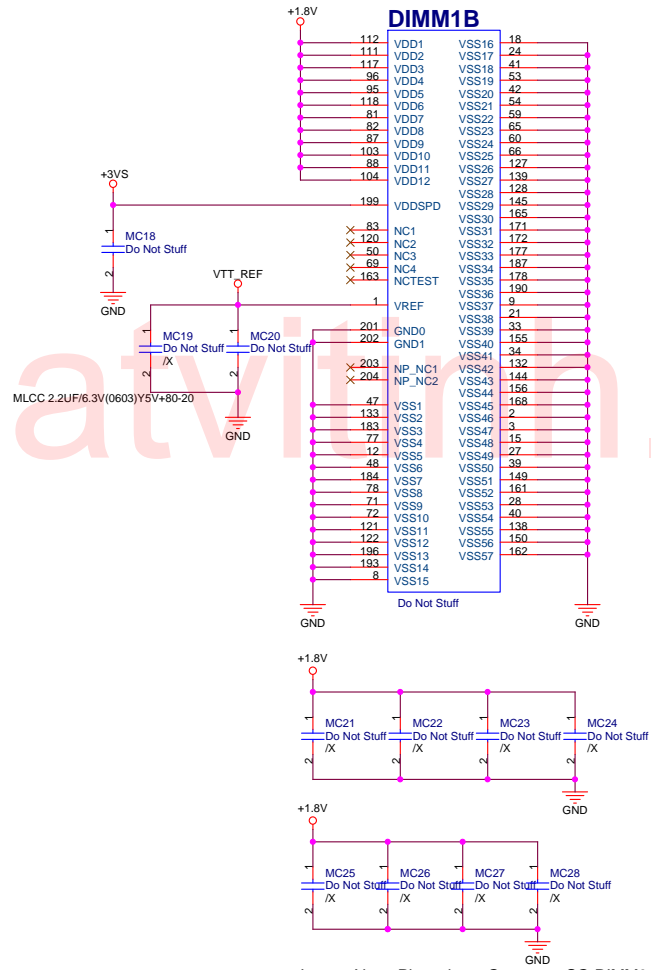


**DIMM1A**

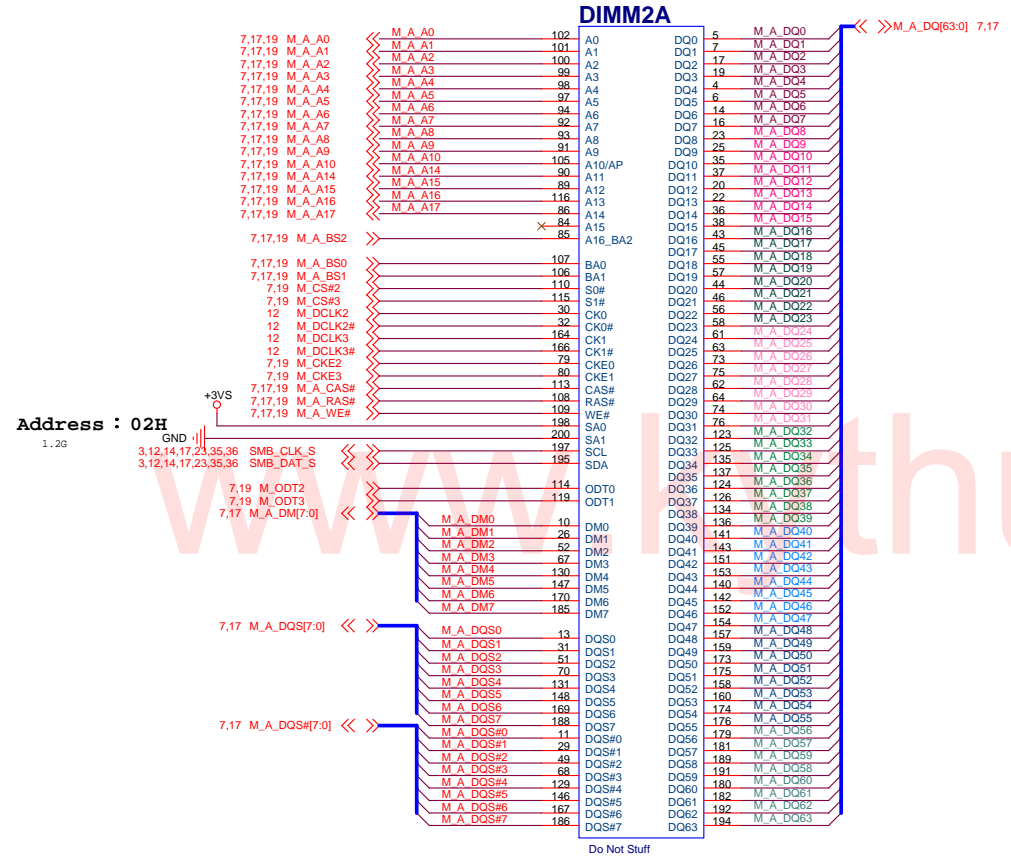


**H=9.2mm Standard Type, 12G025C22000**  
**Channel A, DIMM 0**

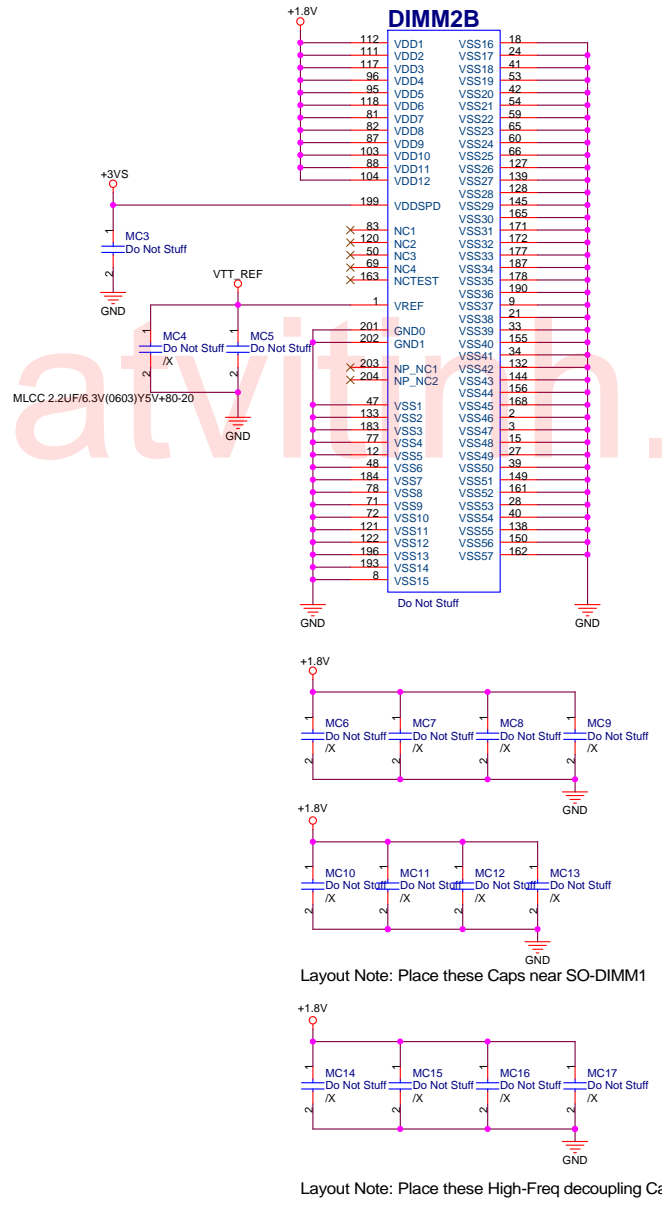
**DIMM1B**

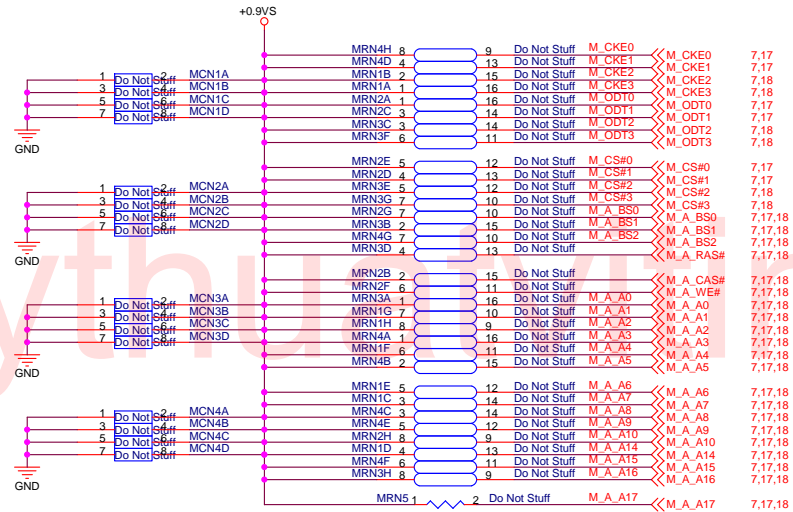
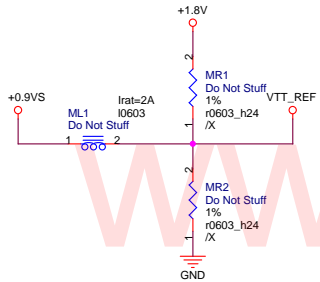


Layout Note: Place these Caps near SO-DIMM0



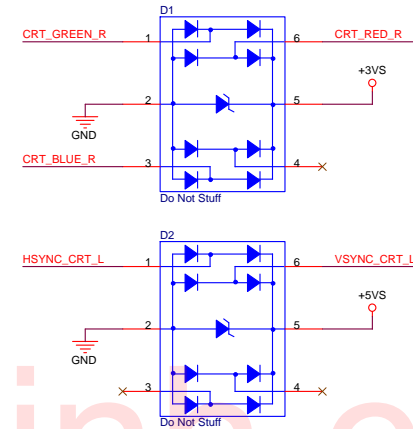
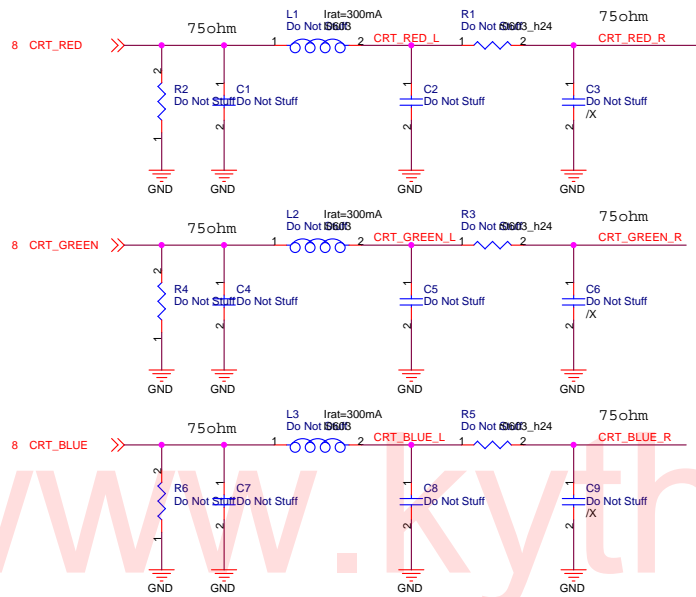
**H=5.2mm Standard Type, 12G025122007**  
**Channel A, DIMM 1**



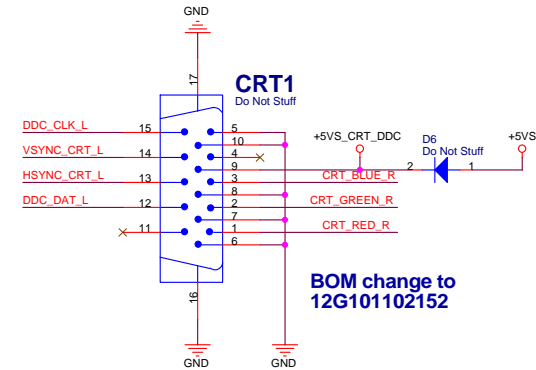
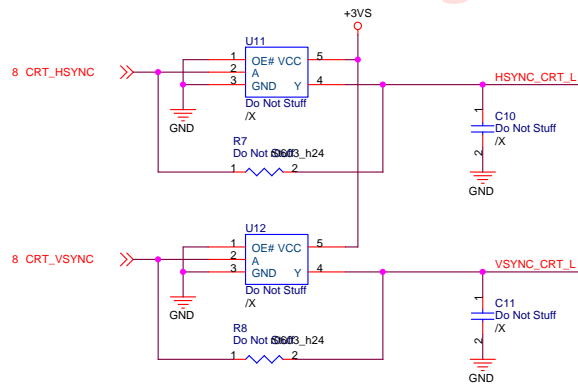


**DDR2: Command, Control Signal need termination**

Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V

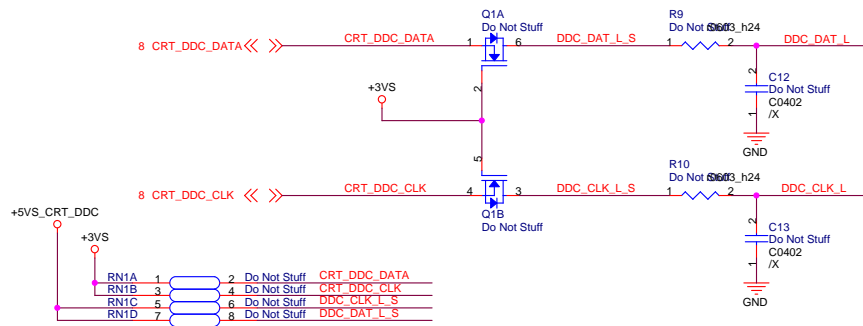


**ESD Diodes**  
Place ESD Diodes near CRT Connector



**BOM change to 12G101102152**

## CRT Connector

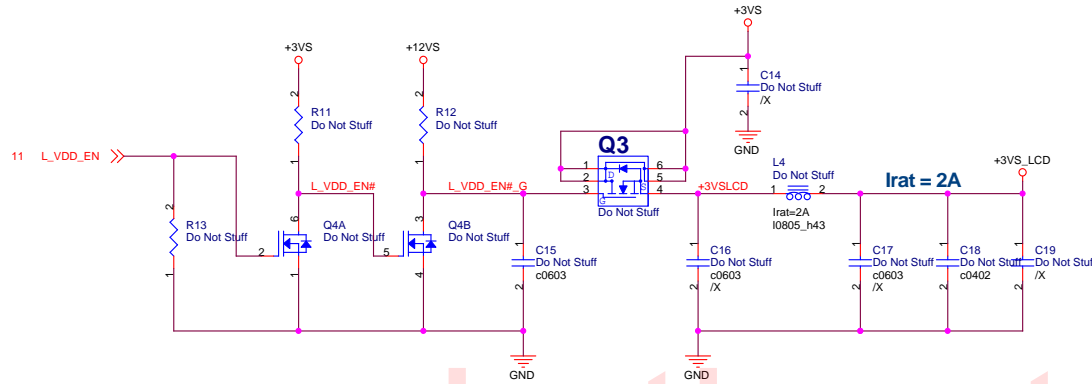


+3V	RN1A	1	2	Do Not Stuff	CRT_DDC_DATA
	RN1B	3	4	Do Not Stuff	CRT_DDC_CLK
	RN1C	5	6	Do Not Stuff	DDC_CLK_L_S
	RN1D	7	8	Do Not Stuff	DDC_DAT_L_S

LUNCH

<b>ASUS</b>		<b>Title : CRT Connector</b>	
ASUSTek Computer INC.		Engineer: <b>Jack Hsu</b>	
Size	Project Name	Rev	
Custom	<b>Z62H</b>	1.0	
Date: Thursday, August 09, 2007	Sheet	20	of 63

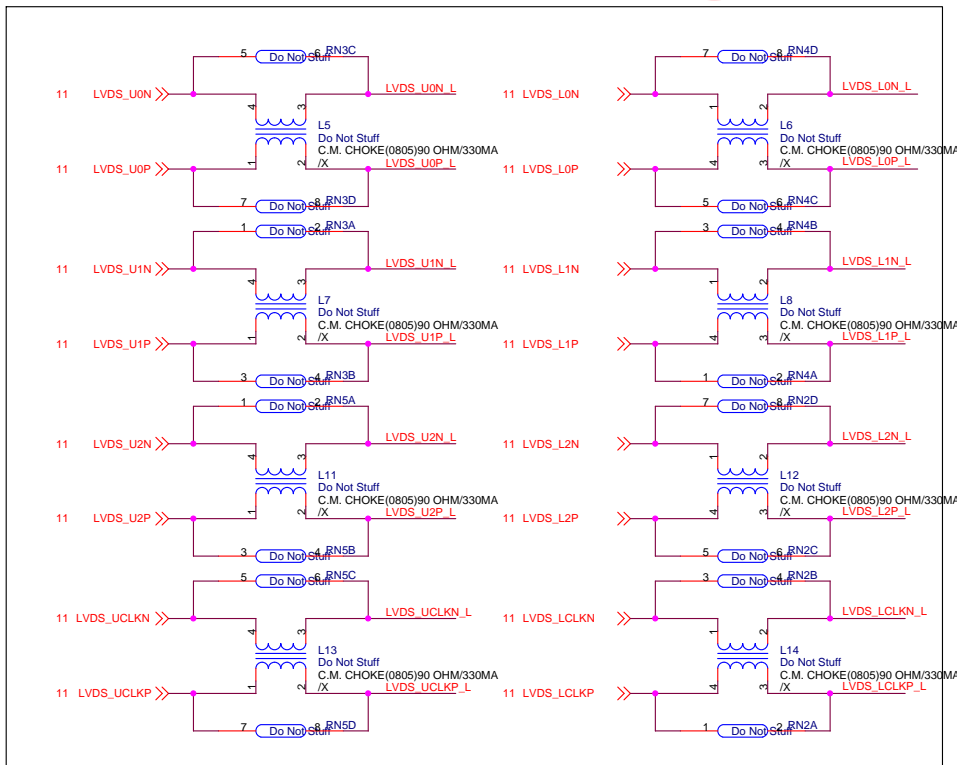
# LCD Power Switch



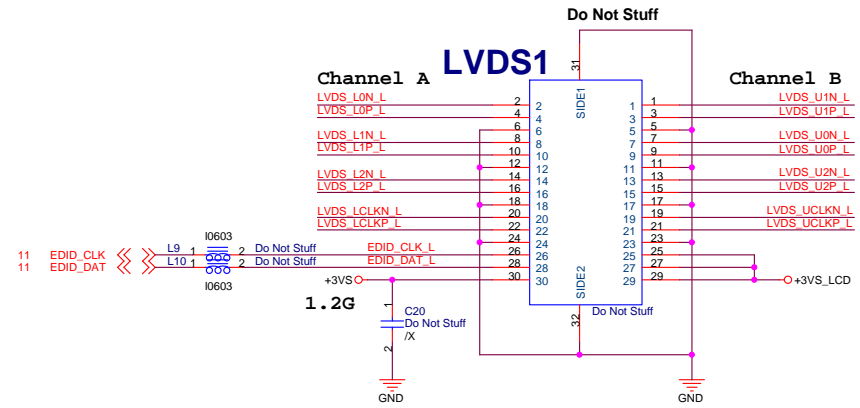
## LVDS NUT



www.kythuatvithinh.com



# LVDS Connector



Cable Requirement:  
 Impedance: 100 ohm +/- 10%  
 Length Mismatch <= 10 mils  
 Twisted Pair(Not Ribbon)  
 Maximum Length <= 16"

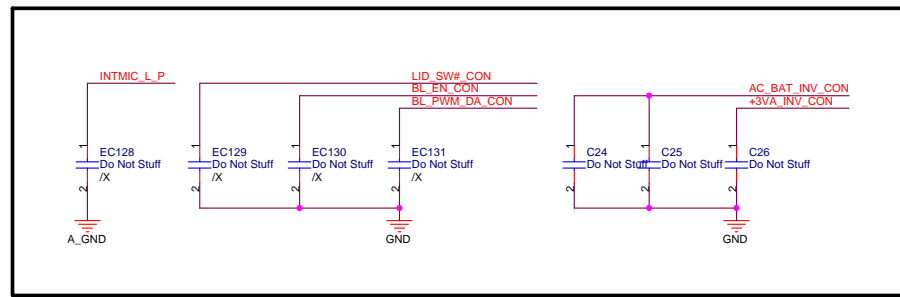
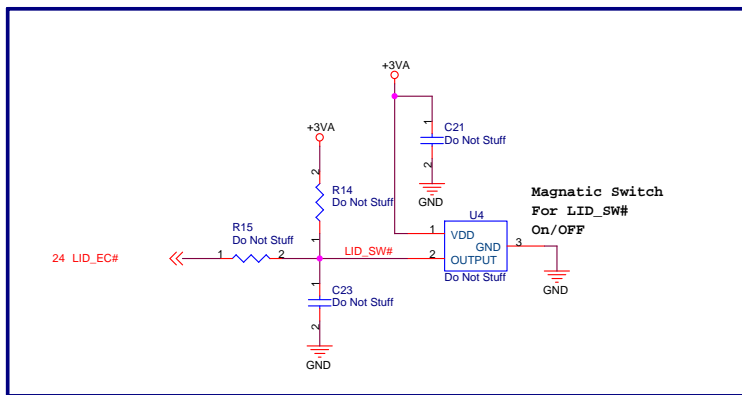
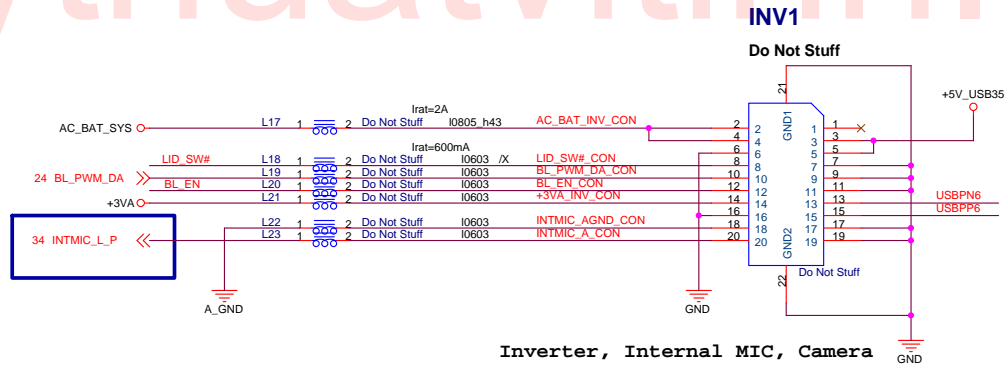
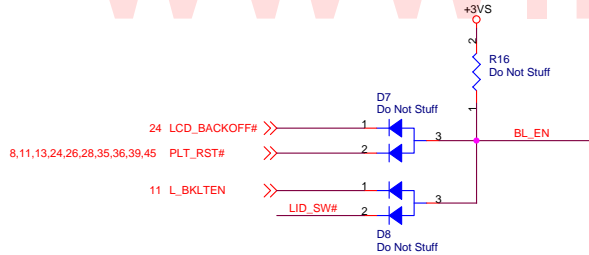
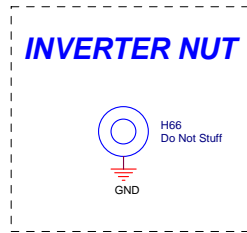
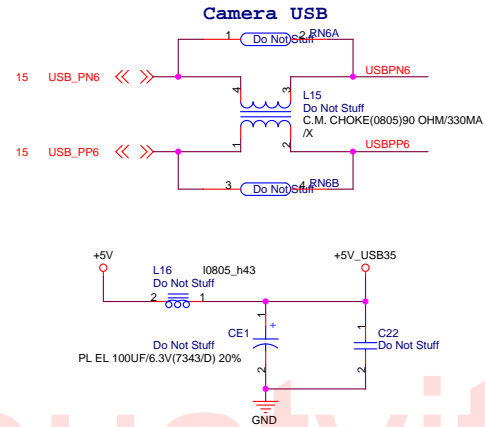
LUNCH		<b>ASUS</b>		Title : LVDS Connector	
ASUSTek Computer INC.		Project Name		Engineer: Jack Hsu	
Size	Custom	Z62H		Rev	1.0
Date:	Thursday, August 09, 2007	Sheet	21	of	63

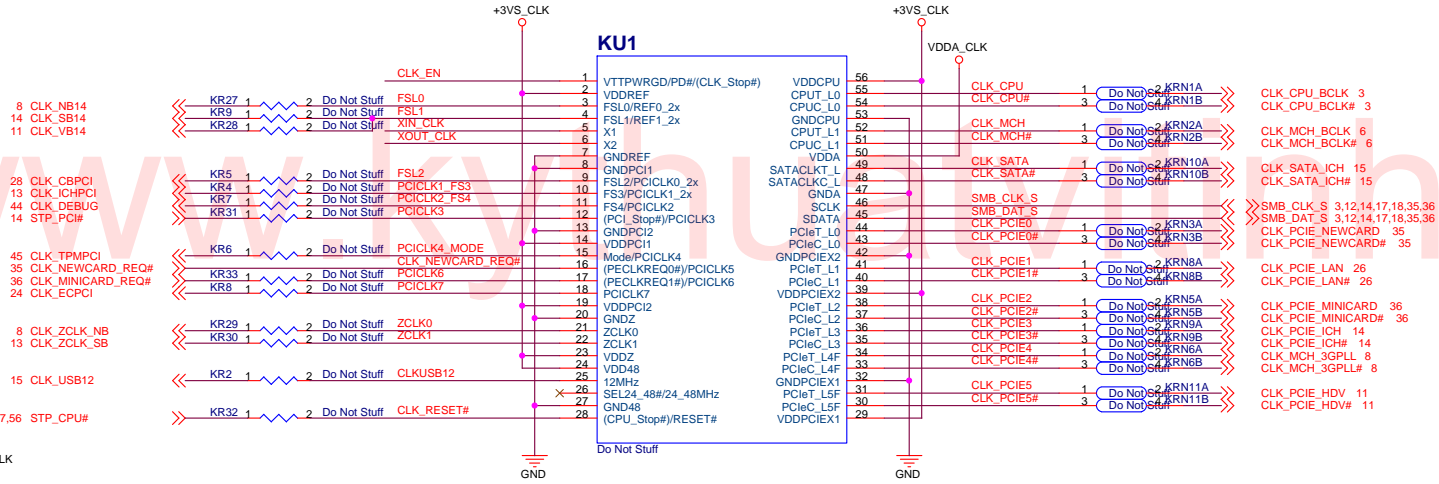
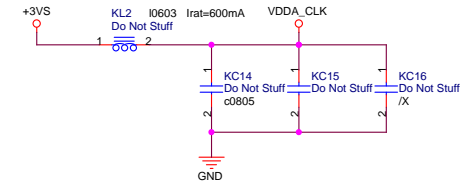
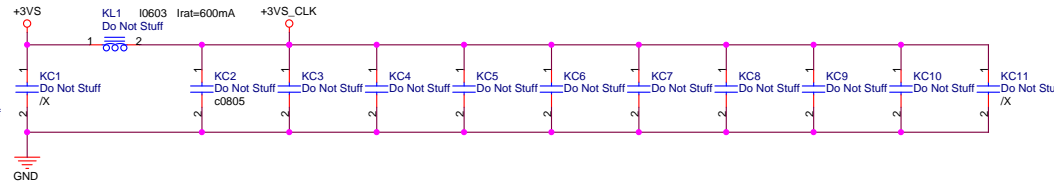
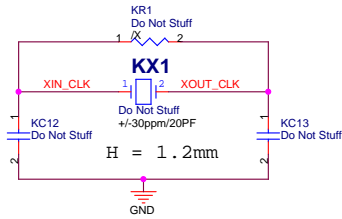
# INVERTER Interface

BIOS  
LCD\_BACKOFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS  
BACK\_ADJ: KBC output PWM signal ( adjust pulse width ) to adjust Back light.

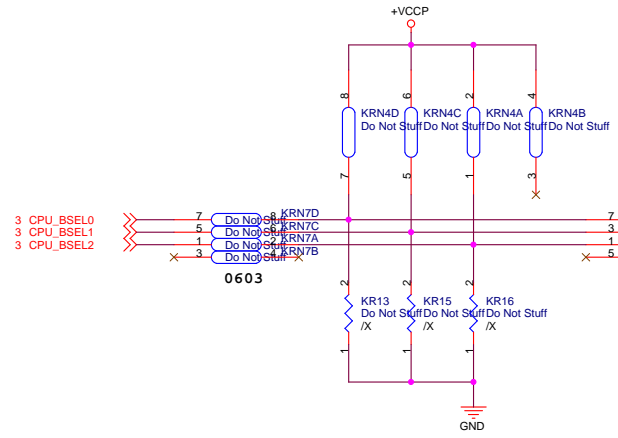
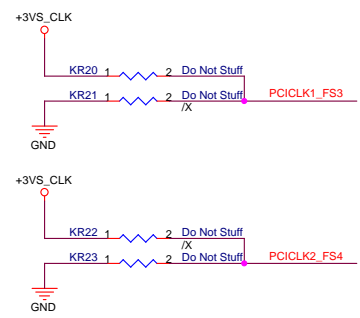
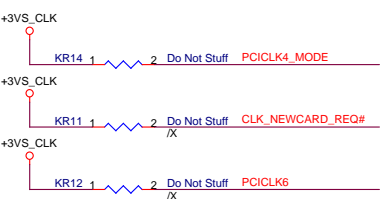
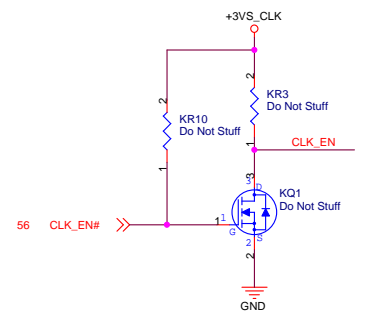
Inverter Board built in 14.1W LCD Panel





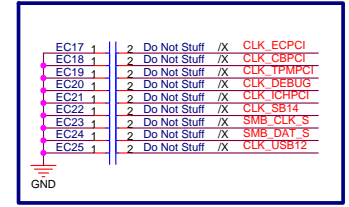
- 8 CLK\_NB14
- 14 CLK\_SB14
- 11 CLK\_VB14
  
- 28 CLK\_CBPCI
- 13 CLK\_ICHPCI
- 44 CLK\_DEBUG
- 14 STP\_PCI#
  
- 45 CLK\_TPMPCI
- 35 CLK\_NEWCARD\_REQ#
- 36 CLK\_MINICARD\_REQ#
- 24 CLK\_ECPCI
  
- 8 CLK\_ZCLK\_NB
- 13 CLK\_ZCLK\_SB
  
- 15 CLK\_USB12
  
- 14,27,56 STP\_CPU#

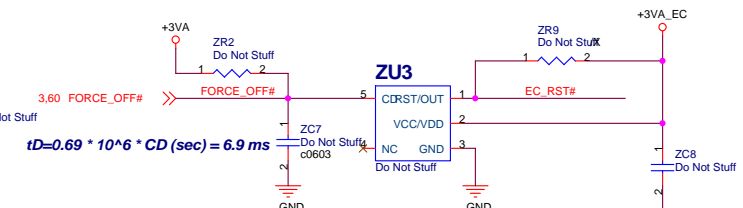
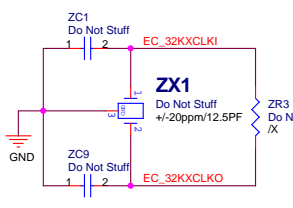
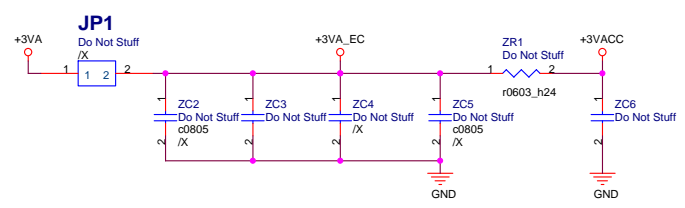
- CLK\_CPU\_BCLK 3
- CLK\_CPU\_BCLK# 3
- CLK\_MCH\_BCLK 6
- CLK\_MCH\_BCLK# 6
- CLK\_SATA\_ICH 15
- CLK\_SATA\_ICH# 15
- SMB\_CLK\_S 3,12,14,17,18,35,36
- SMB\_DAT\_S 3,12,14,17,18,35,36
- CLK\_PCIE\_NEWCARD 35
- CLK\_PCIE\_NEWCARD# 35
- CLK\_PCIE\_LAN 26
- CLK\_PCIE\_LAN# 26
- CLK\_PCIE\_MINICARD 36
- CLK\_PCIE\_MINICARD# 36
- CLK\_PCIE\_ICH 14
- CLK\_PCIE\_ICH# 14
- CLK\_MCH\_3GPLL 8
- CLK\_MCH\_3GPLL# 8
- CLK\_PCIE\_HDV 11
- CLK\_PCIE\_HDV# 11



**CLK trapped by CPU's BSEL**

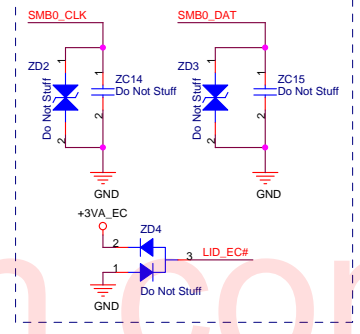
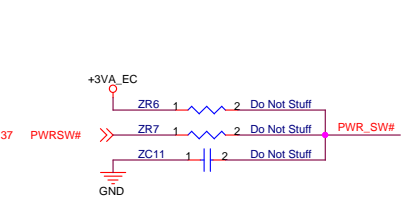
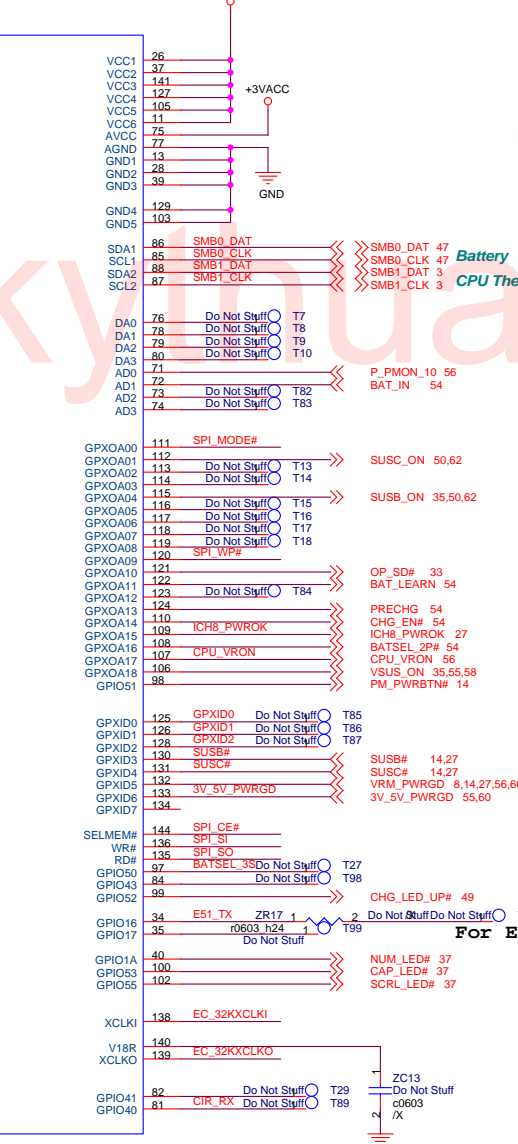
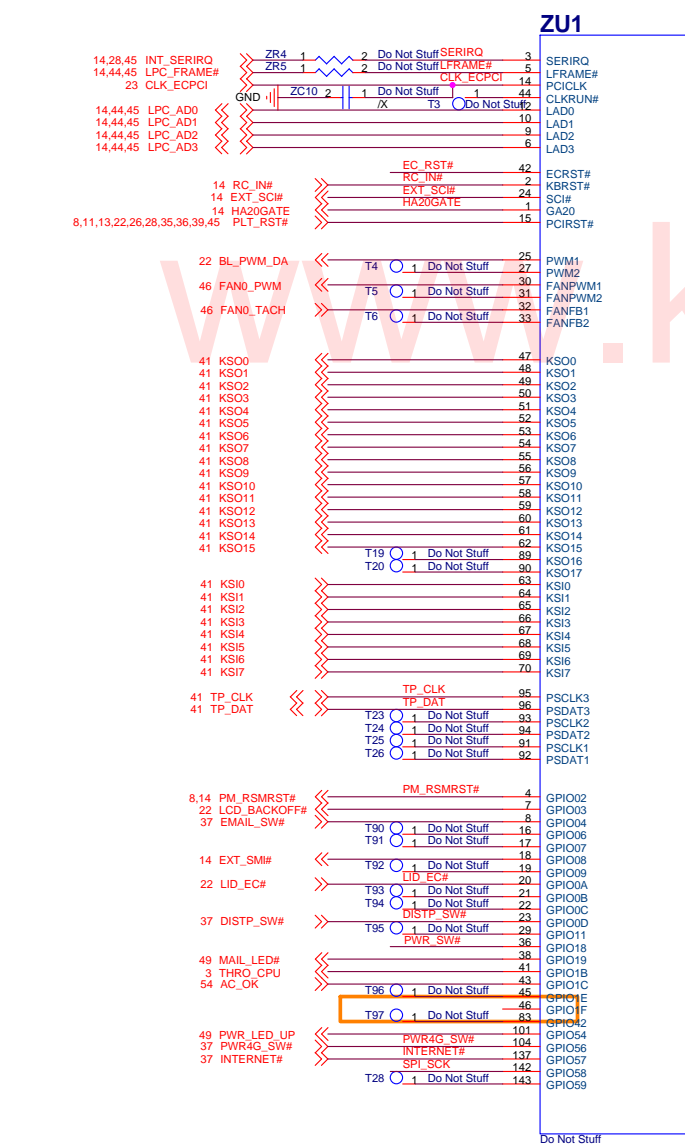
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz



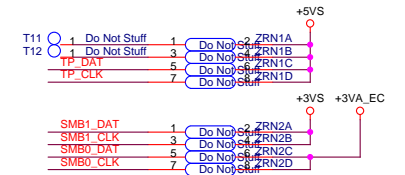


Detector Threshold: 2.7V, CMOS OUTPUT

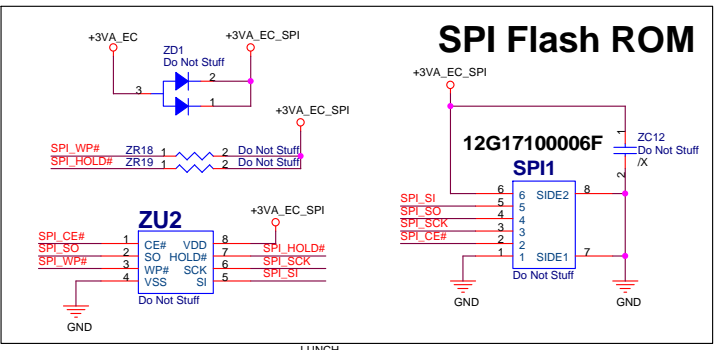
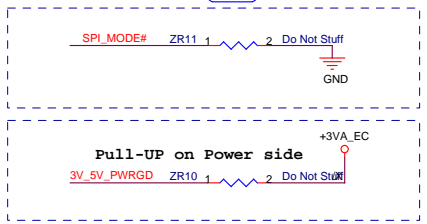
$$tD=0.69 * 10^6 * CD \text{ (sec)} = 6.9 \text{ ms}$$



layout note: place close to connector



STRAPPING TP\_SPI (GPXOA00)  
 TP\_SPI: SPI flash mode  
 0: select SPI flash mode (need external pull-low)  
 1: select ISA flash mode (Power-On Default)




ASUS P/N:  
 A0 : 02G890000400  
 B1 : 02G890000410

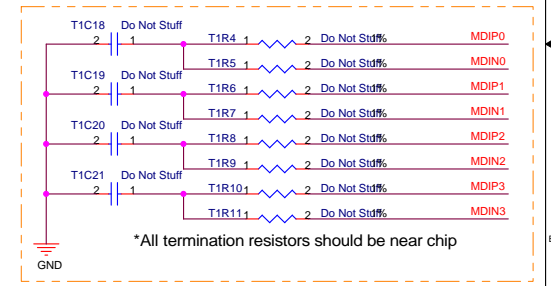
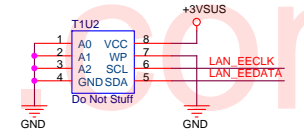
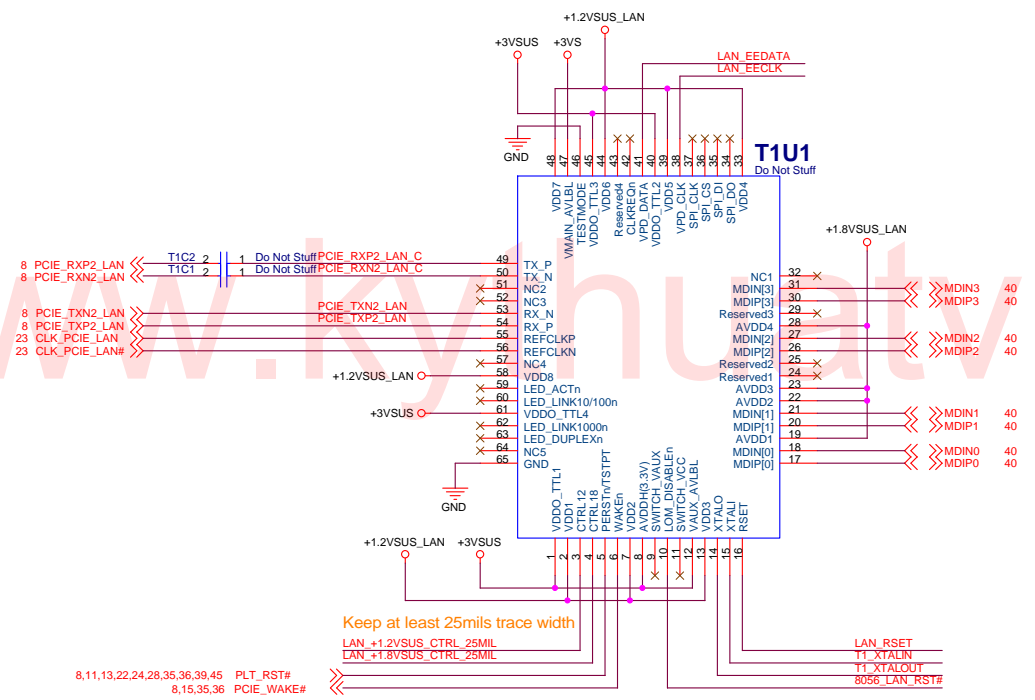
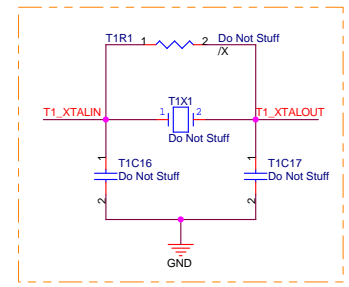
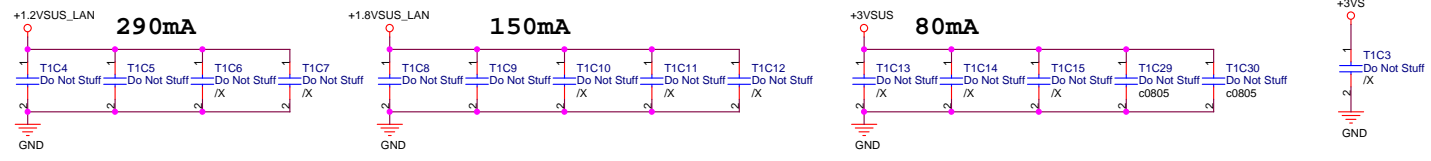


www.kythuatvitinh.com

LUNCH

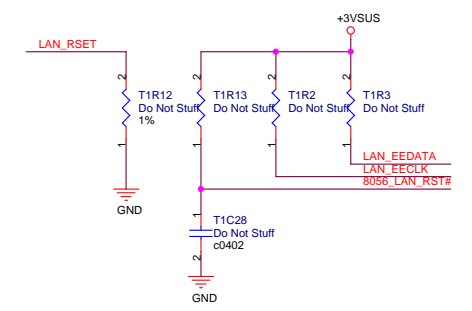
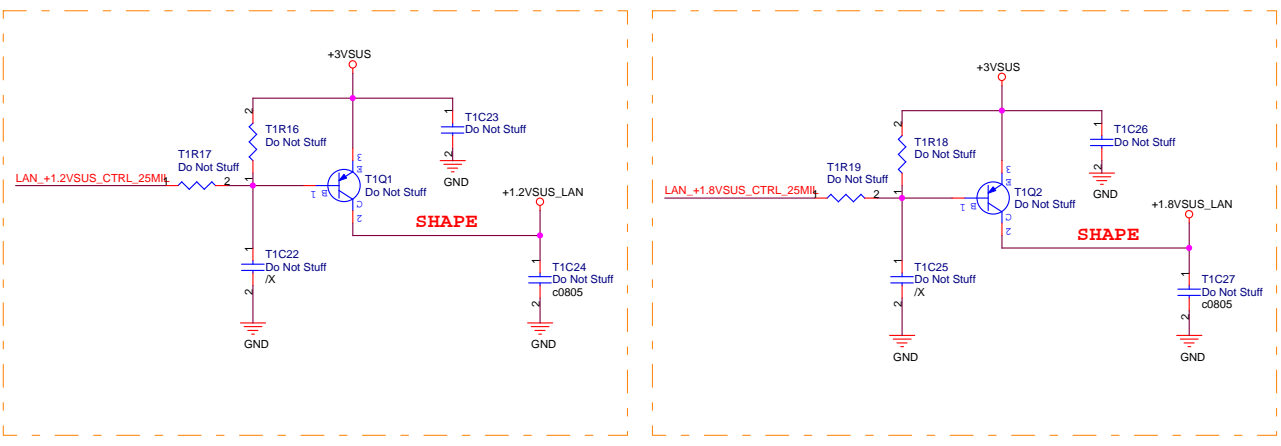
		<b>Title :</b> BLANK
ASUSTek Computer INC.		<b>Engineer:</b> Jack Hsu
Size Custom	Project Name <b>Z62H</b>	Rev 1.0
Date: Thursday, August 09, 2007		Sheet 25 of 63

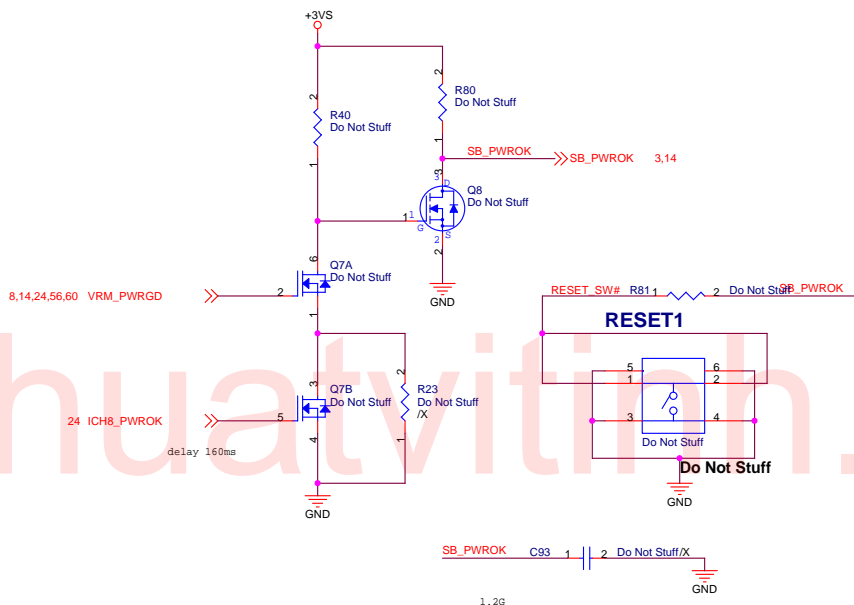
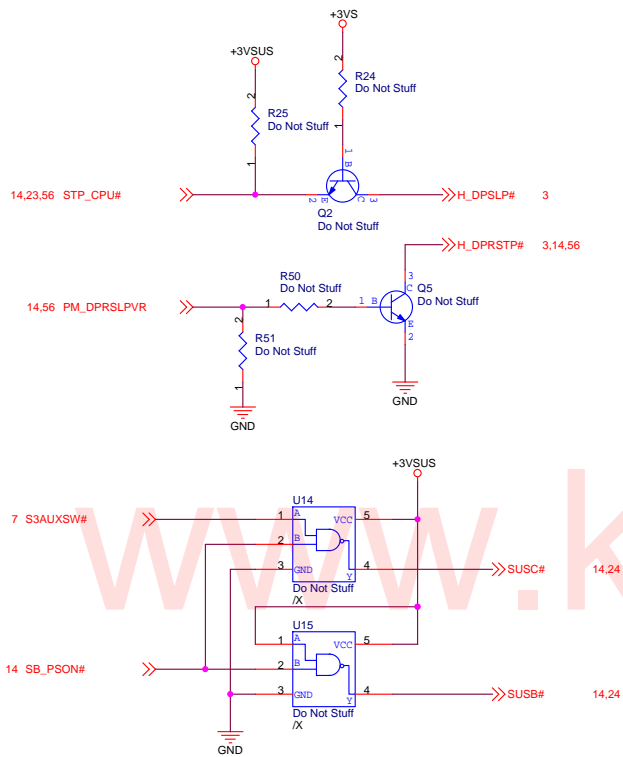
ASUS P/N:  
A2:02G751006700  
B0:02G751006710



Keep at least 25mils trace width  
LAN +1.2VSUS\_CTRL\_25MIL  
LAN +1.8VSUS\_CTRL\_25MIL  
LAN\_RST#  
T1\_XTALIN  
T1\_XTALOUT  
8056 LAN\_RST#

8,11,13,22,24,28,35,36,39,45 PLT\_RST#  
8,15,35,36 PCIE\_WAKE#





**Power ON & OFF:**

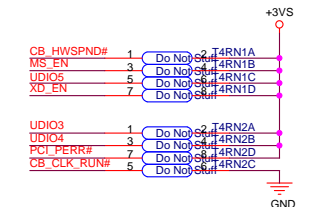
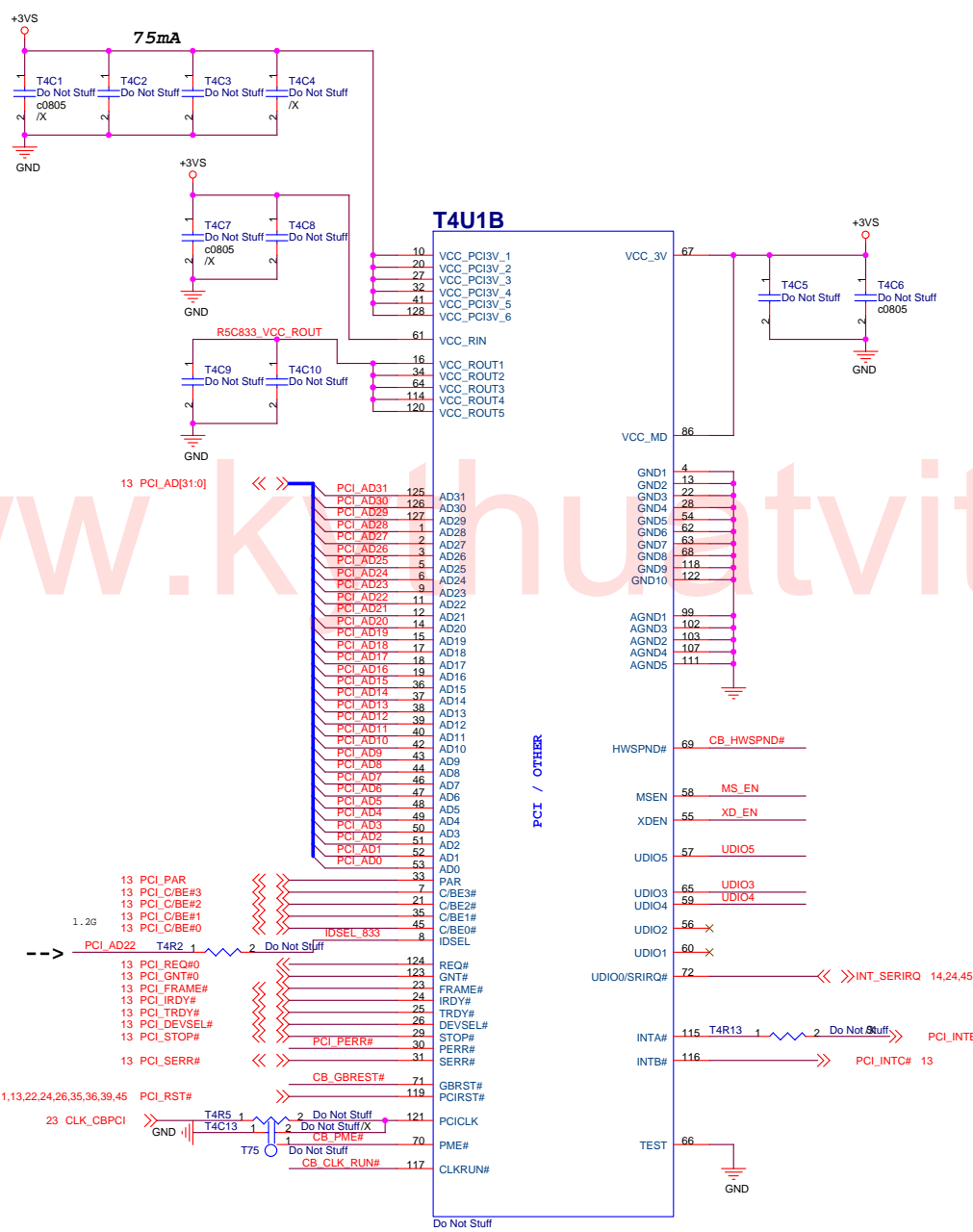
	S5	S0	S5
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC# (S4)	0	1	0
SUSB# (S3)	0	1	0
Power Status	System	Main	System

**Sleep & Wake up**

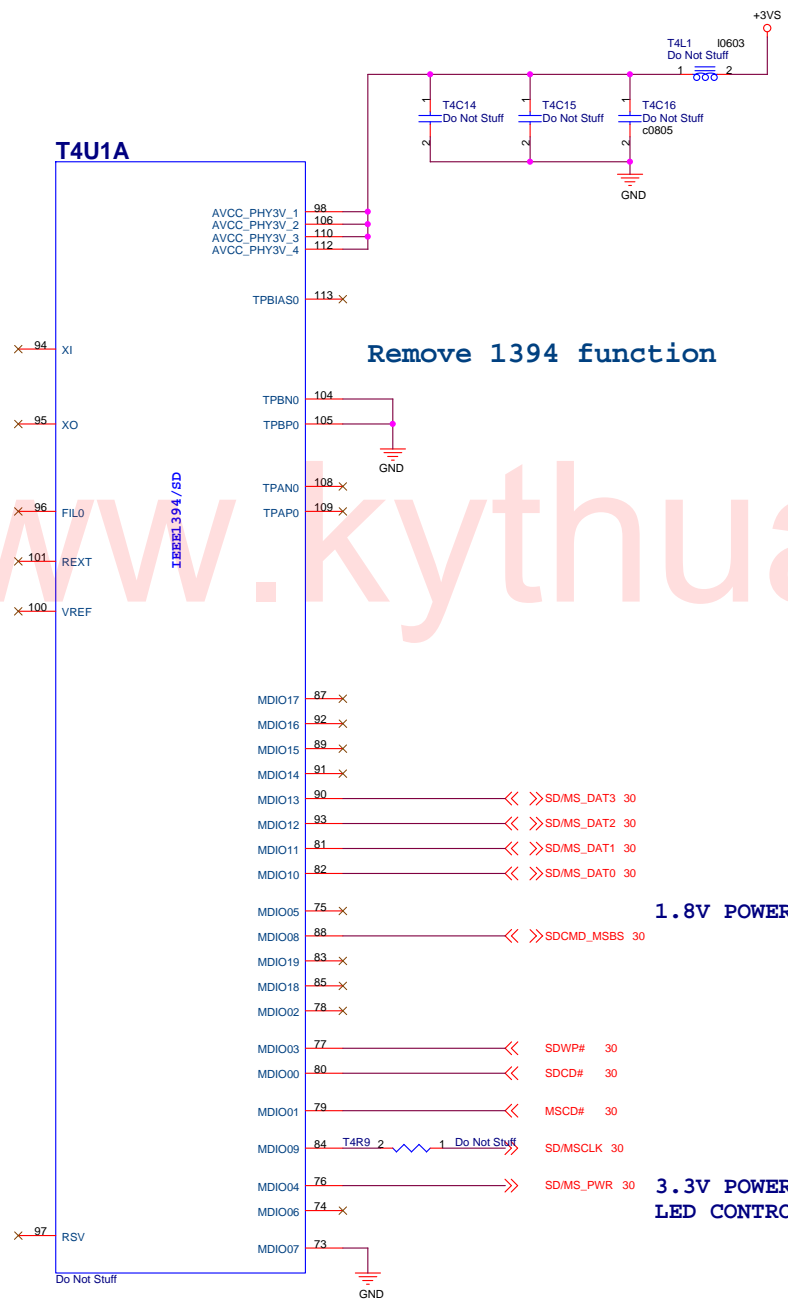
	S0	S3	S0
S3AUXSW#	1	0	0
SB_PSON#	0	0	1
SUSC# (S4)	1	1	1
SUSB# (S3)	1	1	0
Power Status	Main	Main	System, S4

LUNCH

<b>ASUS</b>		<b>Title : OTHER</b>
ASUSTek Computer INC.		Engineer: Jack Hsu
Size	Project Name	Rev
Custom	<b>Z62H</b>	1.0
Date: Thursday, August 09, 2007	Sheet 27 of 63	



SD enable : UDIO3 pull-up  
 MMC enable : UDIO4 pull-up  
 Use EPROM : UDIO5 pull-down  
 Otherwise : disable or non-use



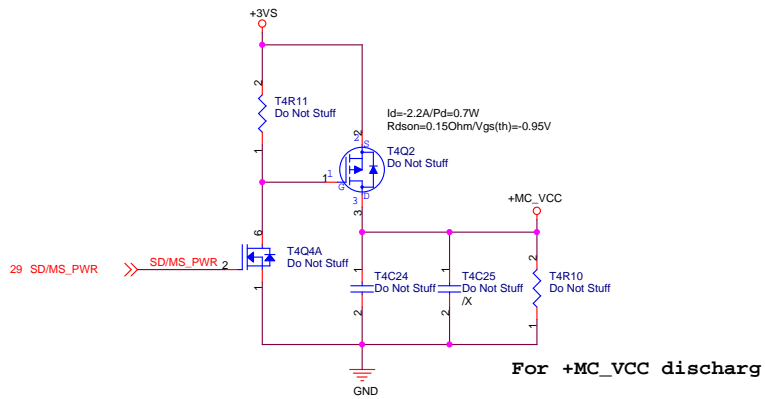
Remove 1394 function

IEEE1394 / SD

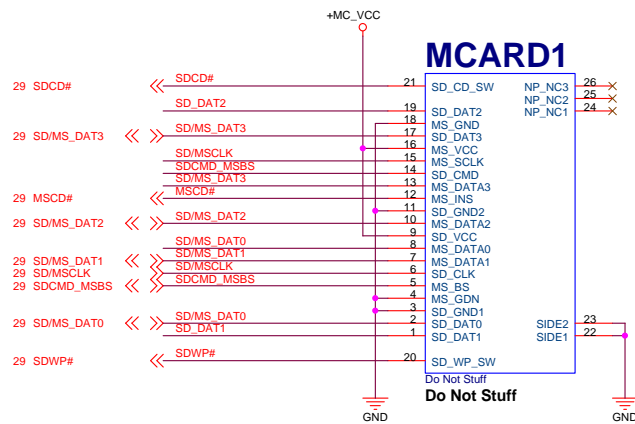
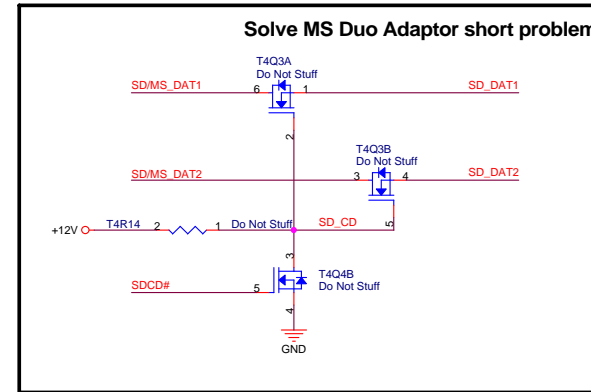
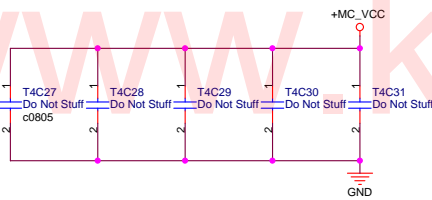
1.8V POWER CONTROL

3.3V POWER CONTROL  
LED CONTROL

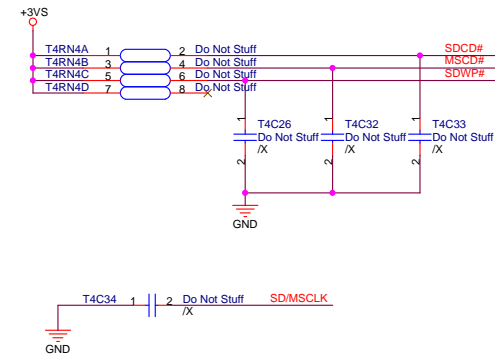
www.kythuatvithinh.com



### Card Reader Power Switch

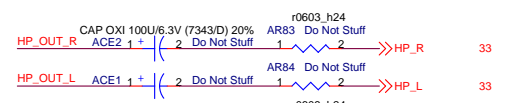
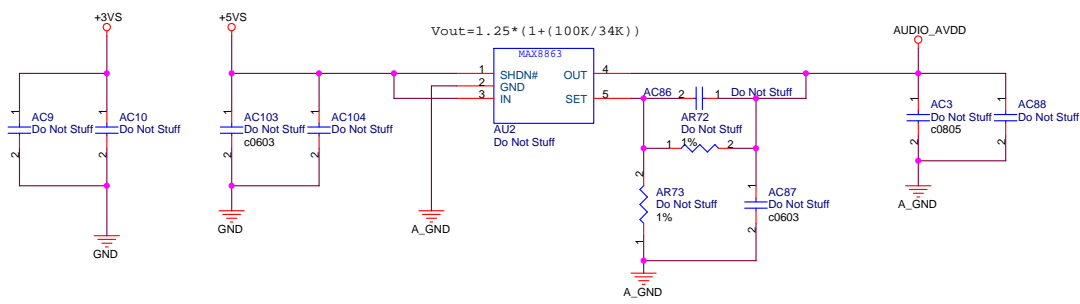
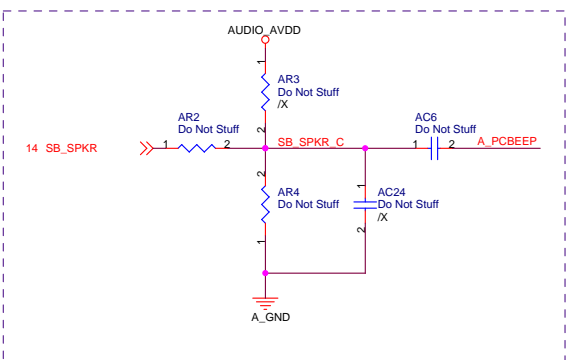


### 3 in 1 Card Reader

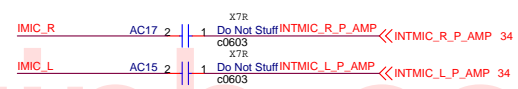


LUNCH

<b>ASUS</b>		<b>Title 3 in 1 Card Reader</b>	
ASUSTek Computer INC.		Engineer: <b>Jack Hsu</b>	
Size	Project Name	Rev	
Custom	<b>Z62H</b>	1.0	
Date: Thursday, August 09, 2007	Sheet	30	of 63



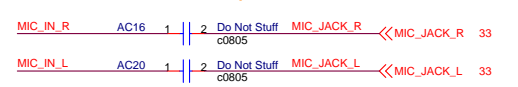
Headphone Output



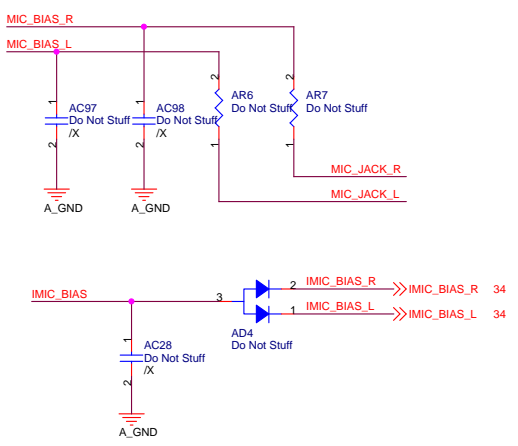
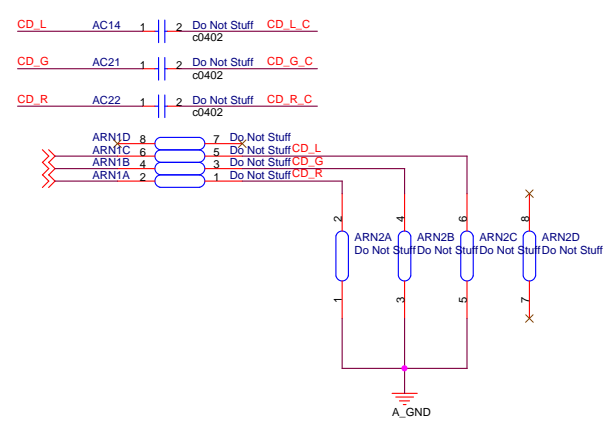
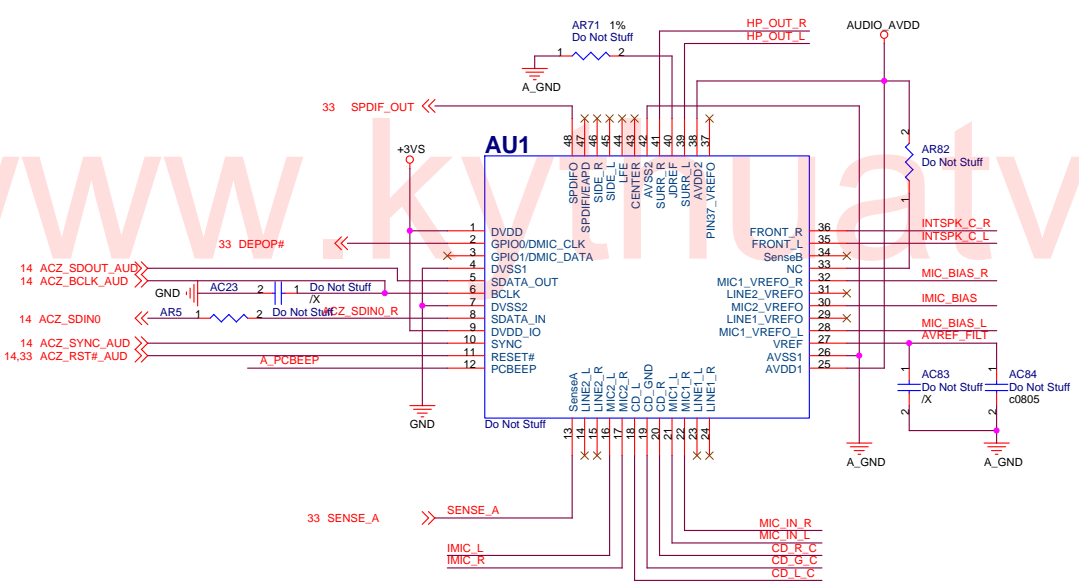
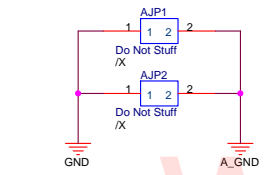
Internal MIC Input



Internal Speaker



MIC Input



02G611102200 C.S ALC883-GR LQFP-48 REALTEK AUDIO CODEC;HP ALC883

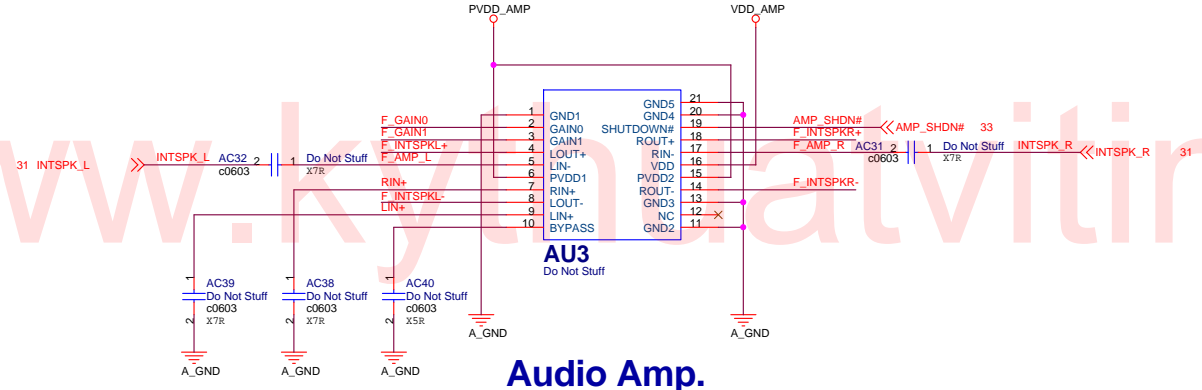
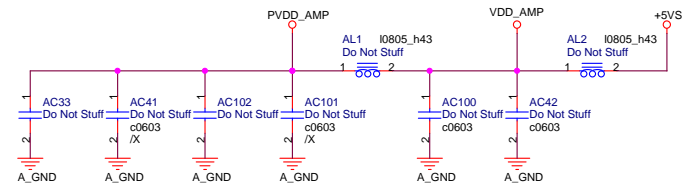
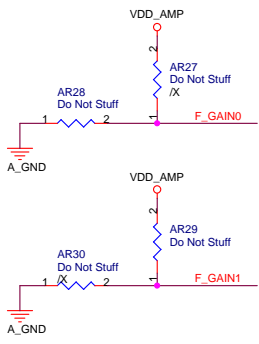
02G611001310 C.S ALC882 Rev:B1 LQFP-48 REALTEK AUDIO CODEC ALC882

02G611002910 C.S ALC888-GR A1 LQFP-48 REALTEK AUDIO CODEC ALC888\_GR

LUNCH		<b>ASUS</b> Title : Audio ALC882H	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	31	of 63

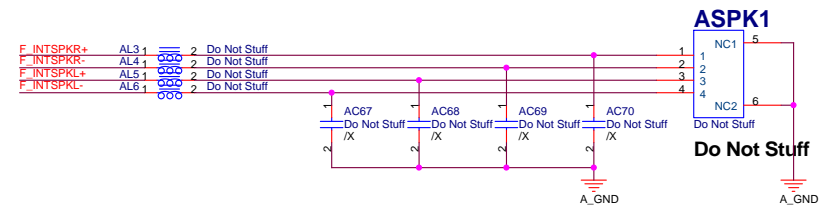
# GAIN Control

GAIN0	GAIN1	Gain
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



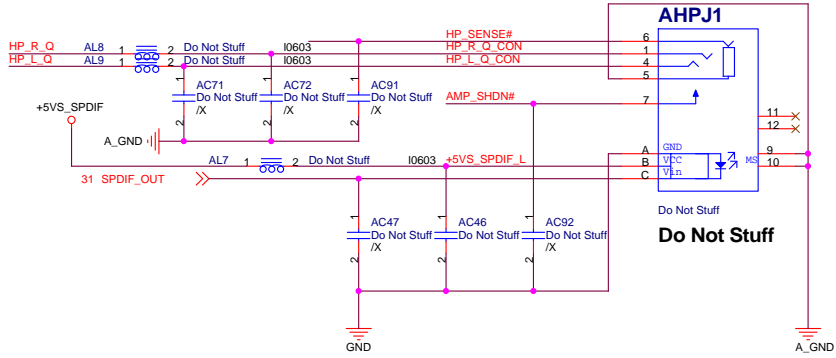
**Audio Amp.**  
f<sub>c</sub> = 1kHz

## 12G171000047 Internal Speaker Connector

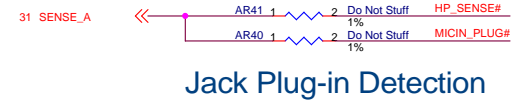
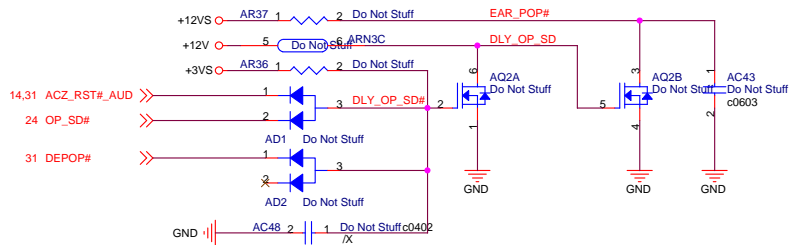
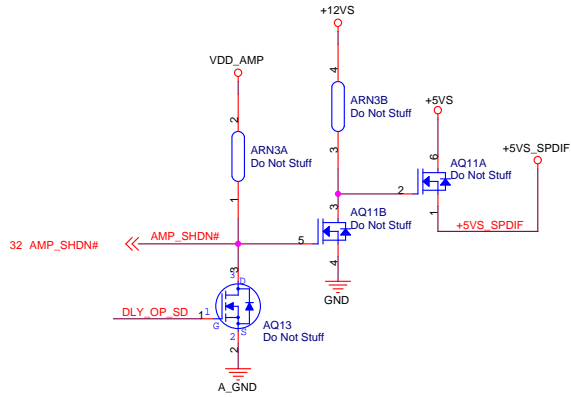
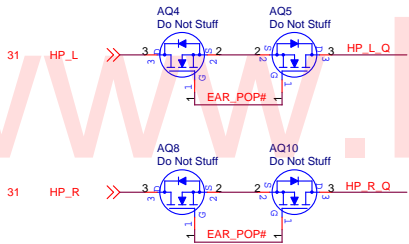
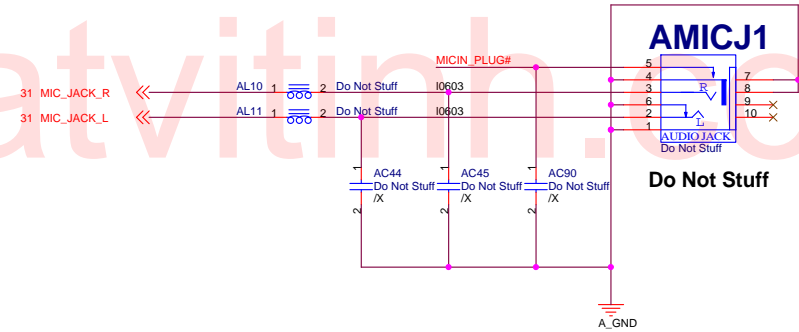




# Headphone & S/PDIF Jack

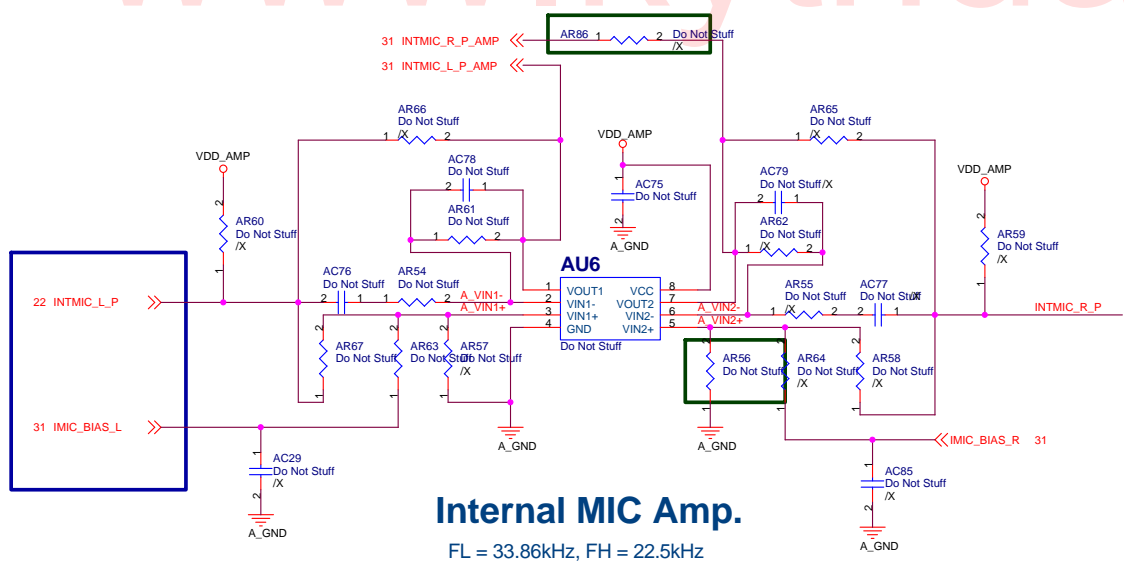


# Microphone-In Jack

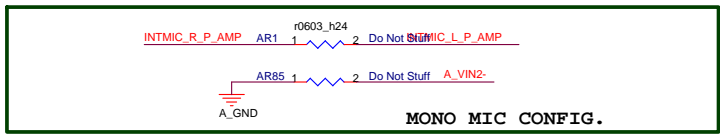


LUNCH

<b>ASUS</b>		<b>Title :</b> Audio JACK
ASUSTek Computer INC.		<b>Engineer:</b> Jack Hsu
Size	Project Name	Rev
Custom	<b>Z62H</b>	1.0
Date: Thursday, August 09, 2007		Sheet 33 of 63

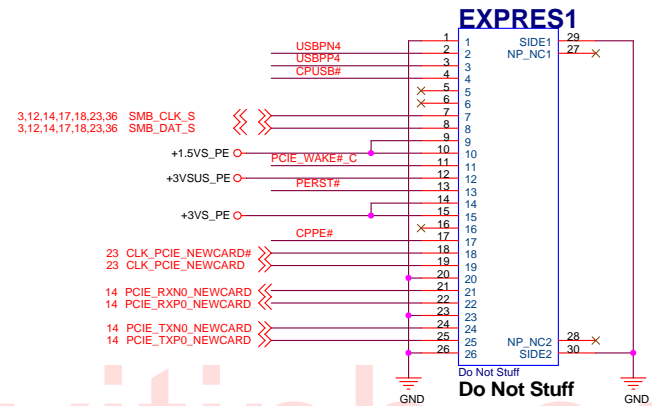
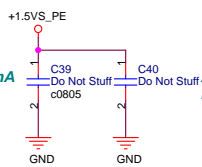
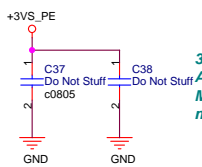
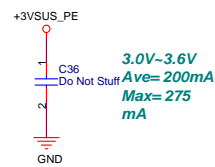
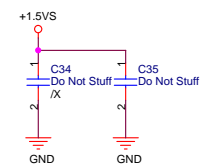
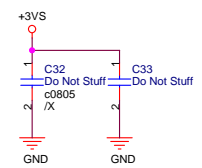
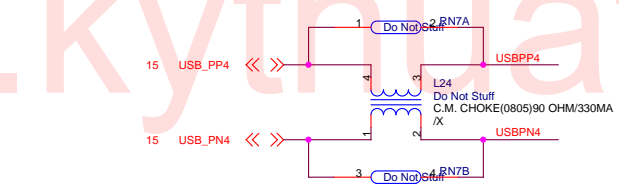
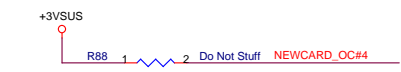
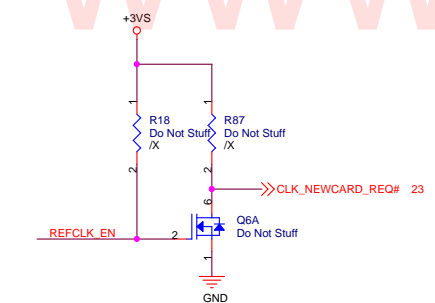
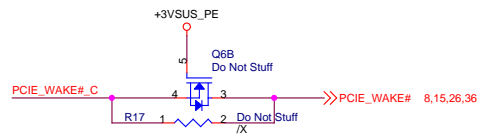
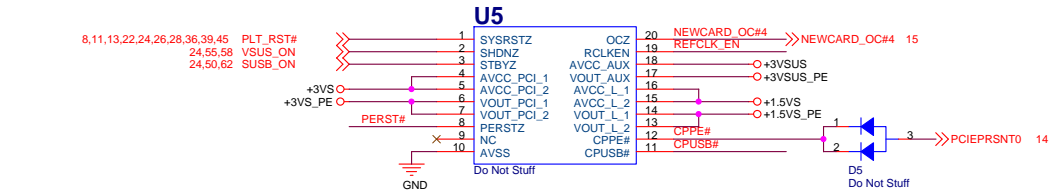


**Internal MIC Amp.**  
 FL = 33.86kHz, FH = 22.5kHz



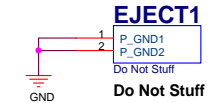
06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1  
 06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

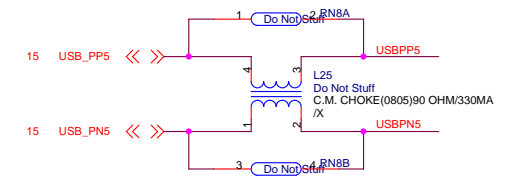
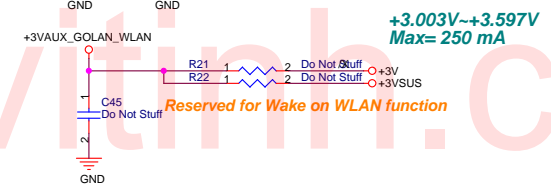
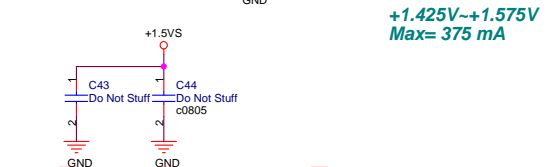
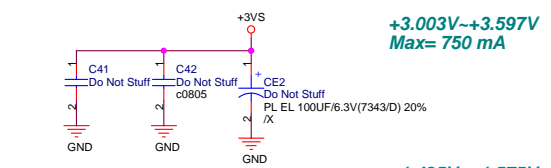
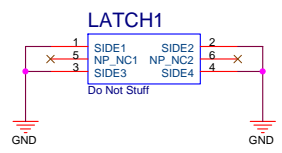
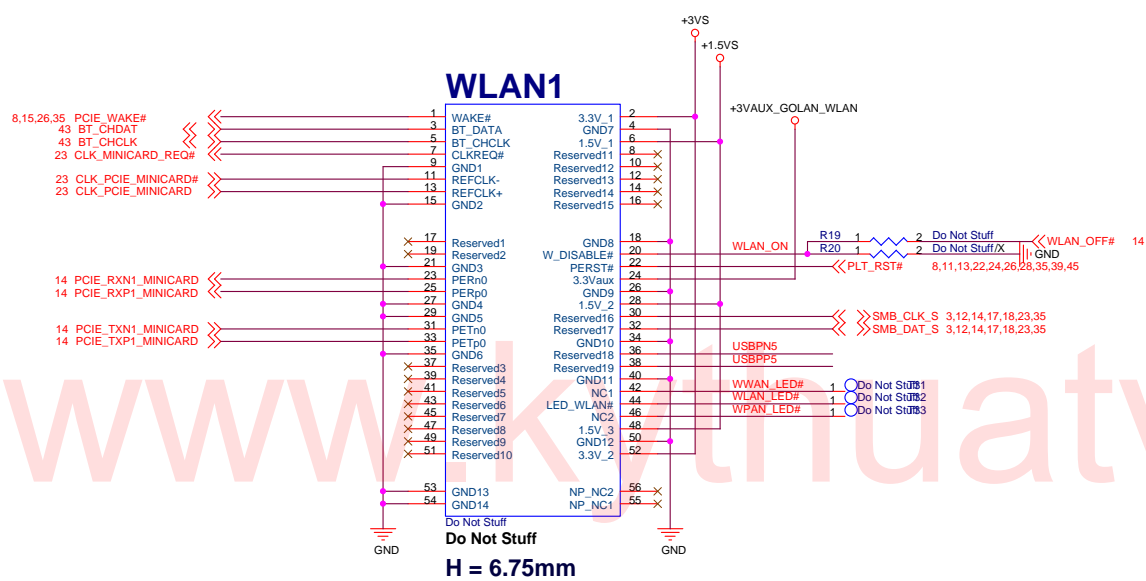
# NewCard Header



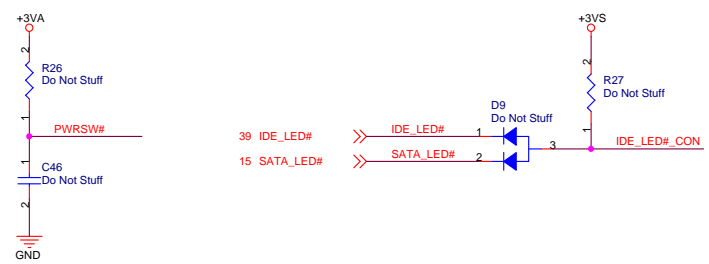
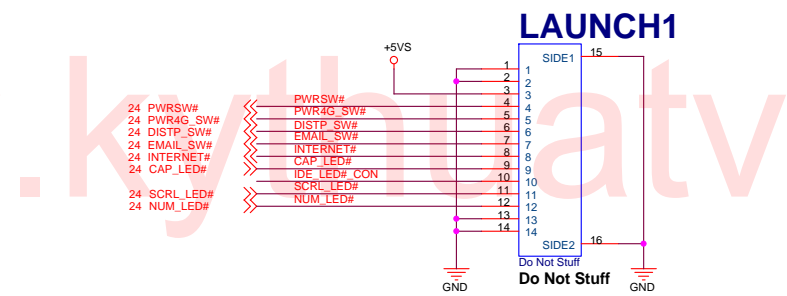
**ExpressCard Standard 1.0:**  
 Change Pin7 from RESERVED to SMBCLK  
 Change Pin8 from SMBCLK to SMBDATA  
 Change Pin9 from SMBDATA to +1.5V

## NewCard Ejector





# LAUNCH BOARD Connector



EC56	1	2	Do Not Stuff/X	PWR4G_SW#
EC57	1	2	Do Not Stuff/X	PWR4G_SW#
EC58	1	2	Do Not Stuff/X	DISTP_SW#
EC59	1	2	Do Not Stuff/X	EMAIL_SW#
EC60	1	2	Do Not Stuff/X	INTERNET#
EC61	1	2	Do Not Stuff/X	CAP_LED#
EC62	1	2	Do Not Stuff/X	IDE_LED# CON
EC63	1	2	Do Not Stuff/X	SCRL_LED#
EC64	1	2	Do Not Stuff/X	NUM_LED#

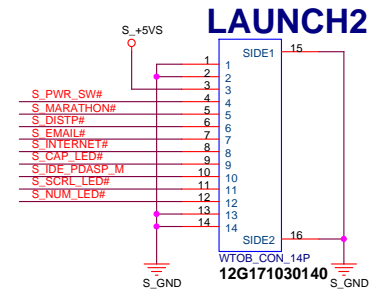
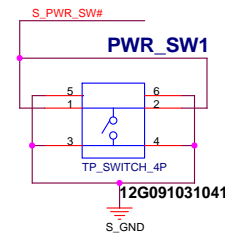
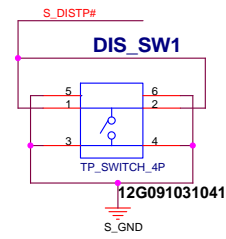
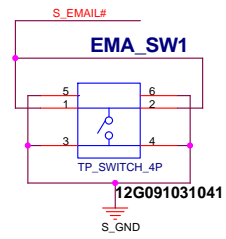
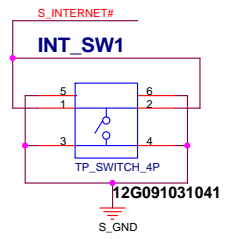
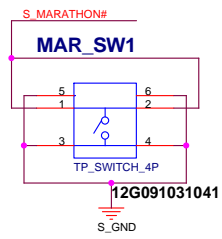
5

4

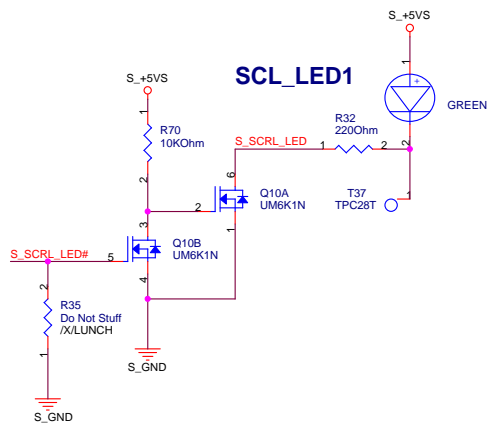
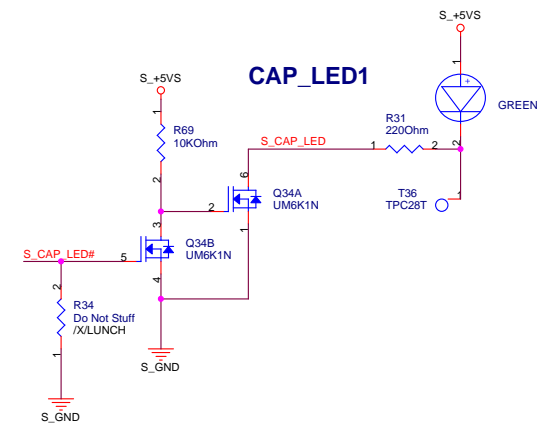
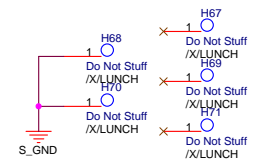
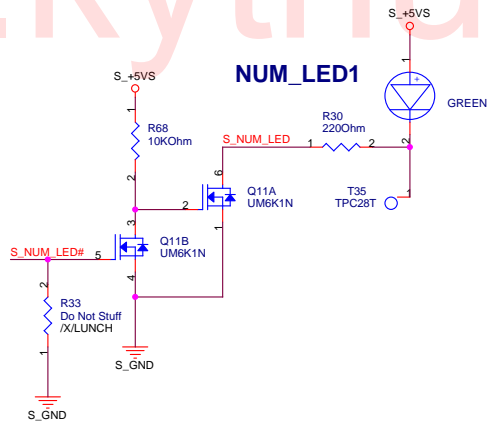
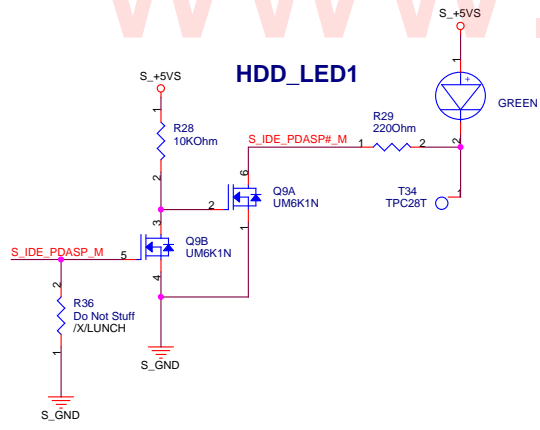
3

2

1



www.kythuovatvinh.com



LUNCH		Title : LAUNCH BOARD	
ASUS		ASUSTek Computer INC. Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Monday, August 13, 2007	Sheet 38 of 63		

5

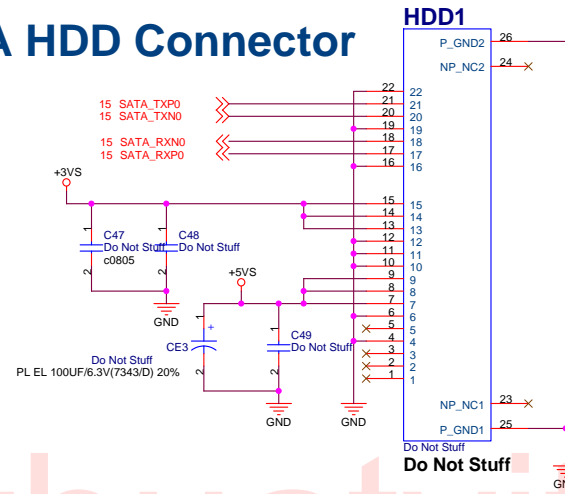
4

3

2

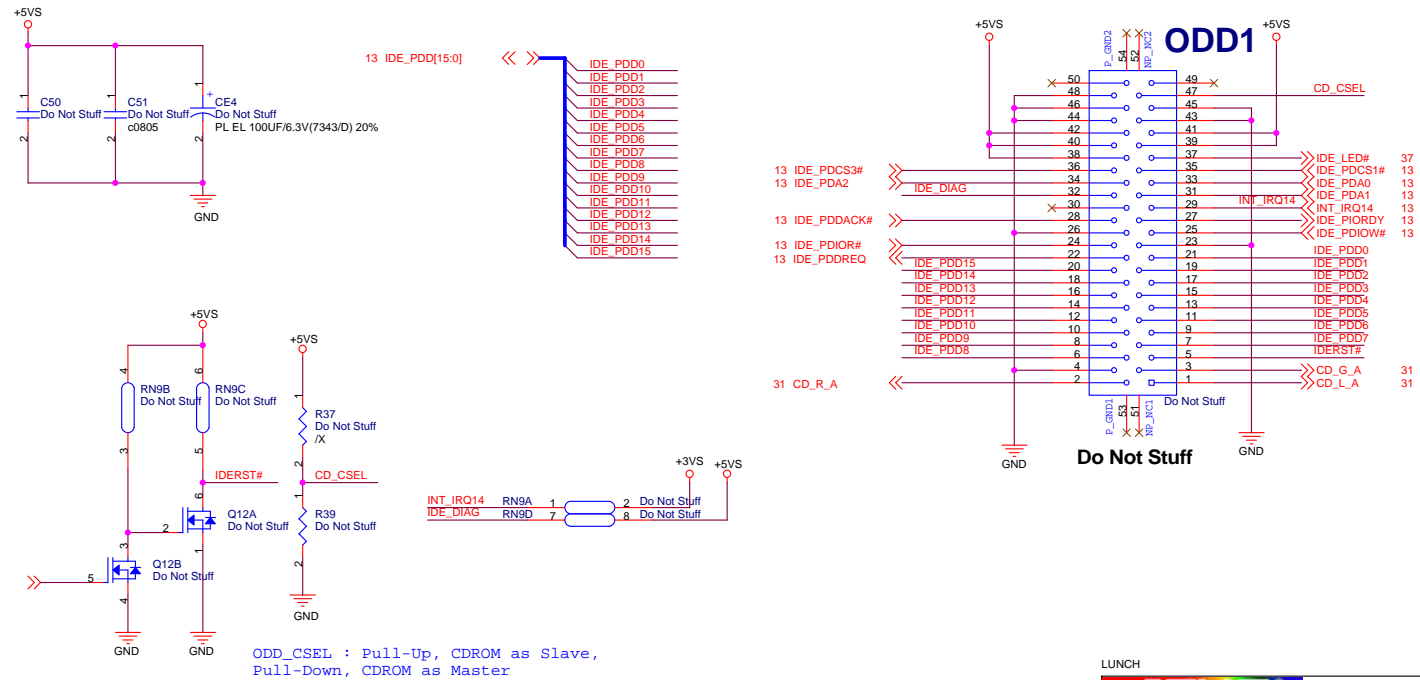
1

# SATA HDD Connector

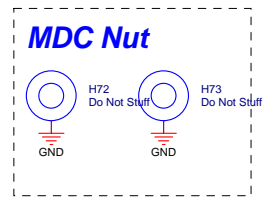
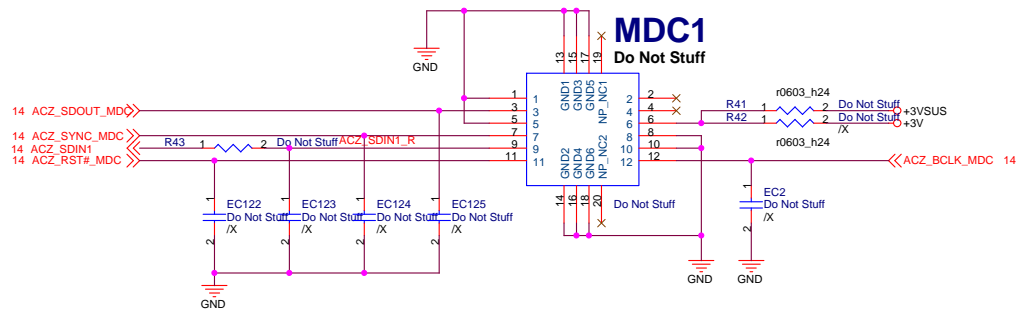


www.kythuatchinh.com

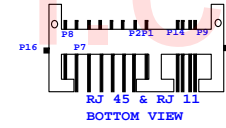
# ODD Connector



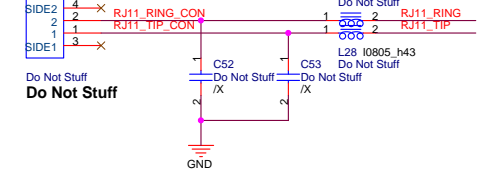
# MDC Connector



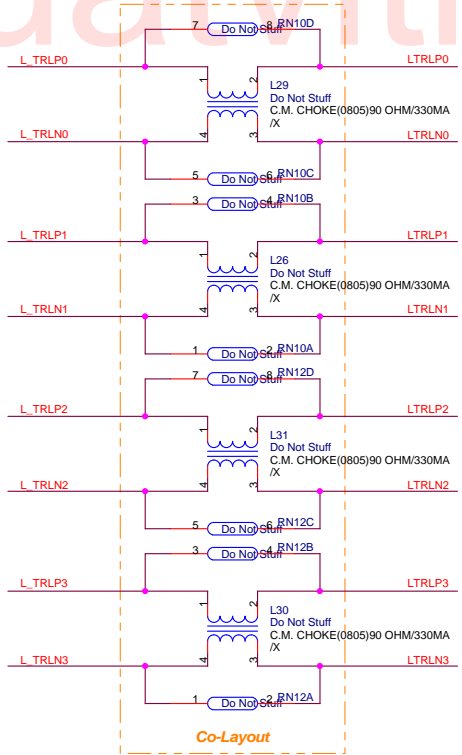
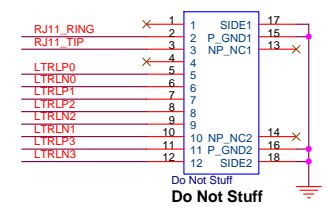
12-142313122



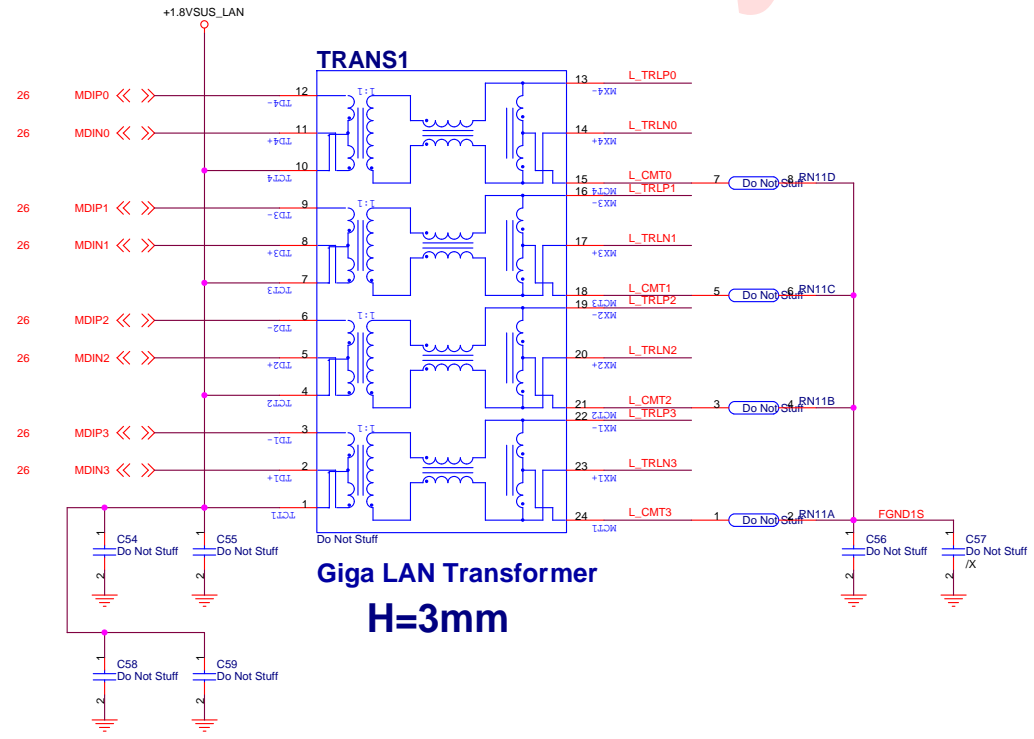
## RING1



## RJ45\_11



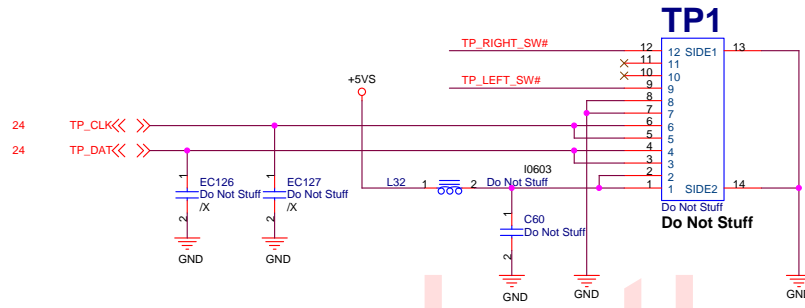
## TRANS1



Giga LAN Transformer  
H=3mm



## TouchPad Connector

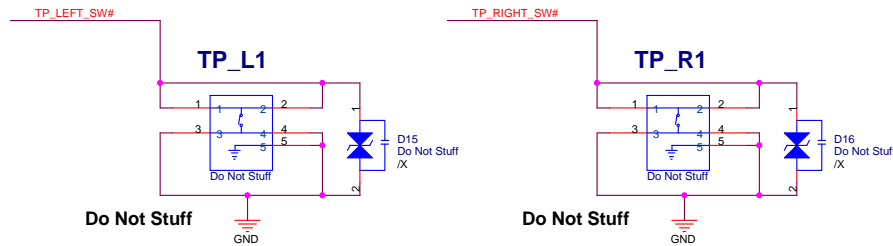
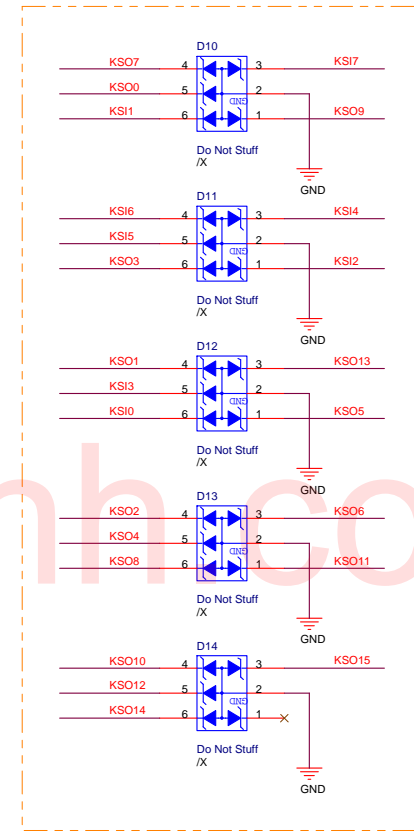
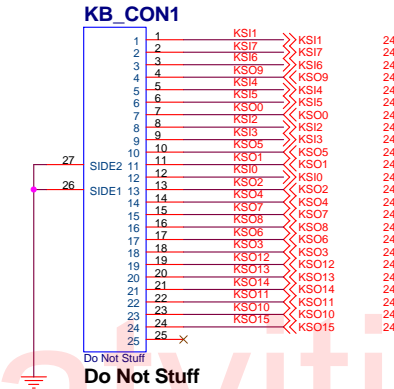


Touch pad Definition

1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

Z62F: pin1 reversal

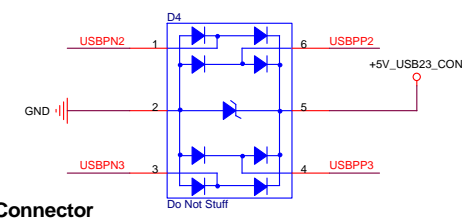
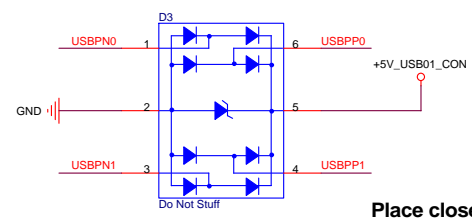
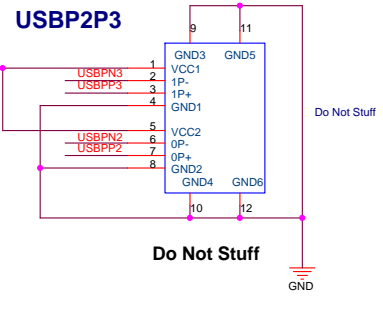
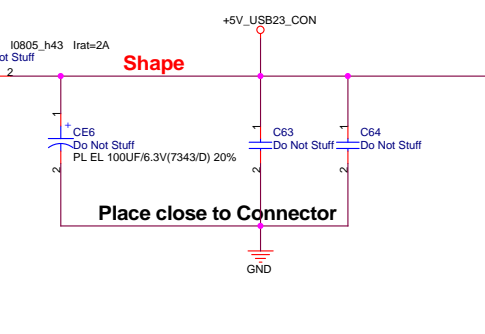
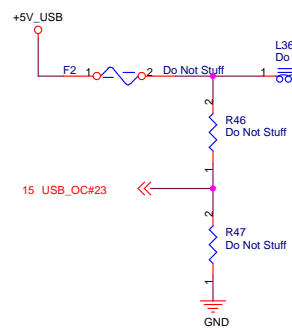
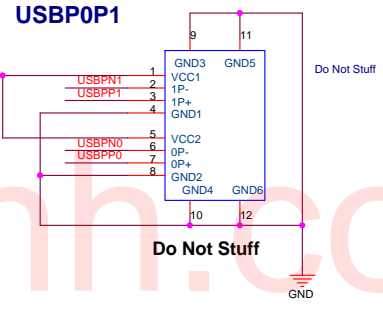
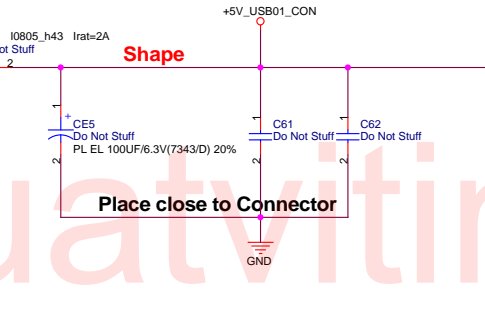
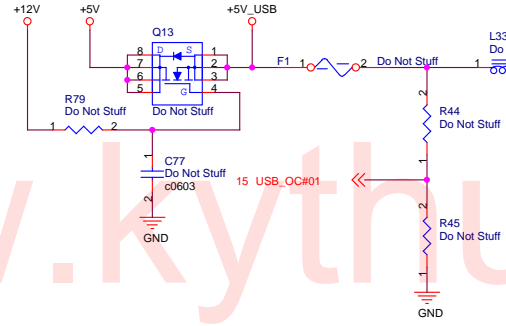
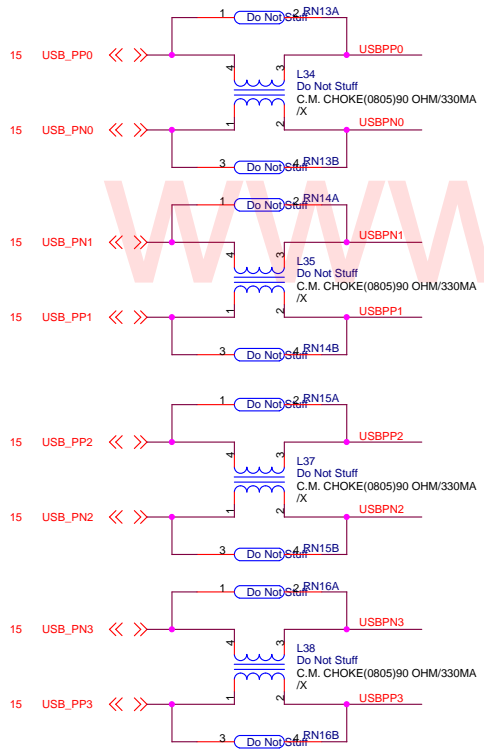
## Keyboard Connector



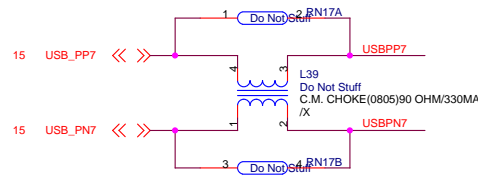
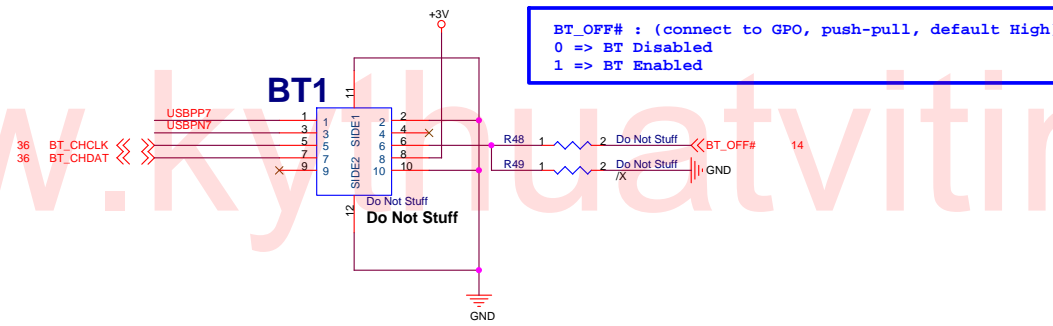
## TOUCH PAD SWITCH

LUNCH

# USB Power & OC Alert

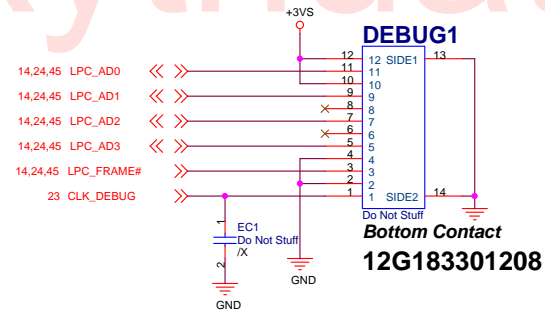


# Bluetooth Connector



www.kythuovatvith.com

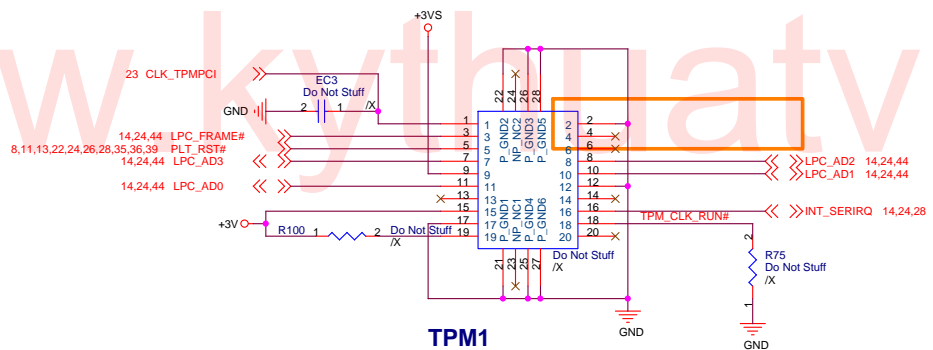
### Debug Connector



LUNCH

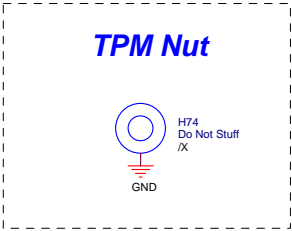
		Title : Debug Port	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet 44	of 63	

## TPM Connector

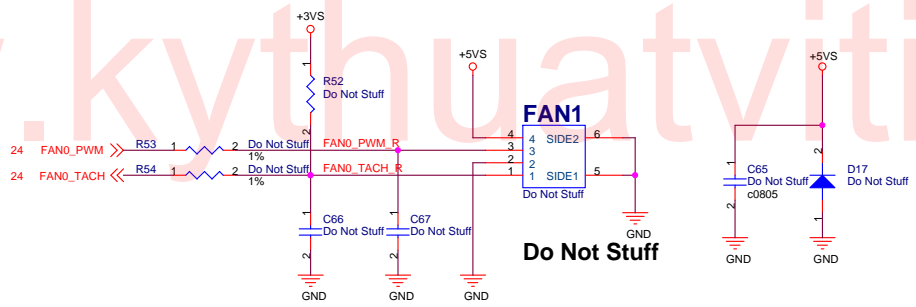


**TPM1**  
**12G16080020J**

**Pin 6: +3VA**  
**Pin 13: SMB\_CLK**  
**Pin 14: SMB\_DAT**  
**Removed!!**



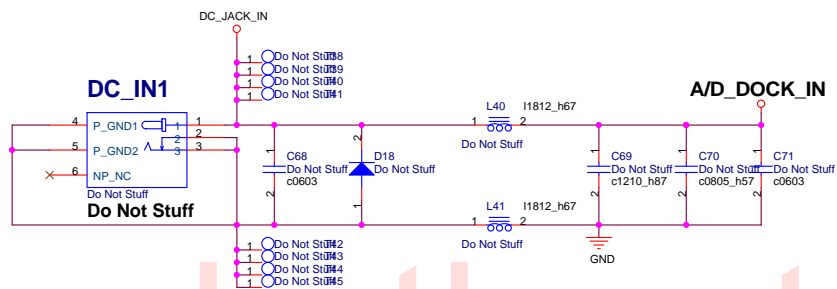
www.kythuovatvinh.com



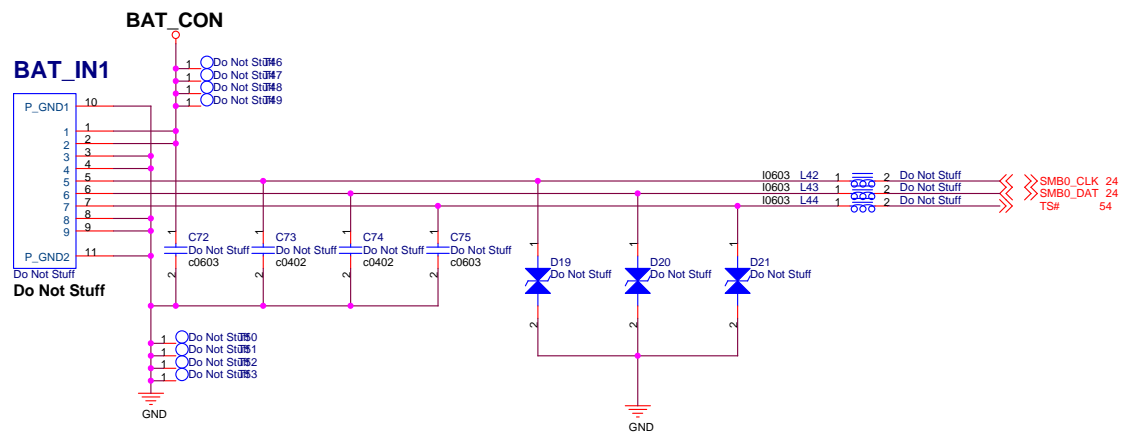
### SYSTEM Fan Connector

LUNCH

		Title : Fan Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62H		1.0
Date: Thursday, August 09, 2007		Sheet	46 of 63



www.kythuativinh.com




LUNCH

<b>ASUS</b>		<b>Title : DC-IN &amp; BAT-IN</b>	
ASUSTek Computer INC.		Engineer: <b>Jack Hsu</b>	
Size	Project Name	Rev	
Custom	<b>Z62H</b>	1.0	
Date: Thursday, August 09, 2007		Sheet	47 of 63

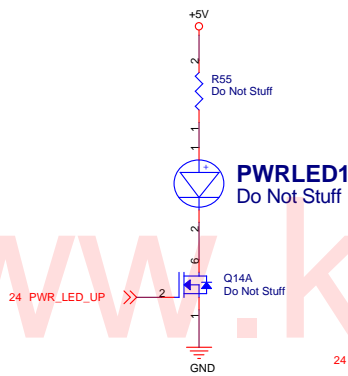
www.kythuatvitinh.com

LUNCH

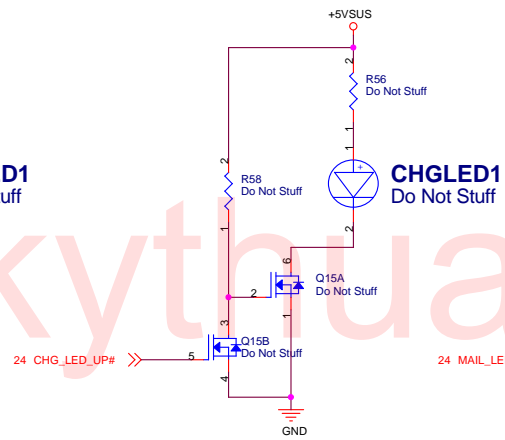
		Title : <b>BLANK</b>	
ASUSTek Computer INC.		Engineer: <i>Jack Hsu</i>	
Size Custom	Project Name <b>Z62H</b>	Date: <i>Thursday, August 09, 2007</i>	Rev 1.0
Date: <i>Thursday, August 09, 2007</i>		Sheet	48 of 63



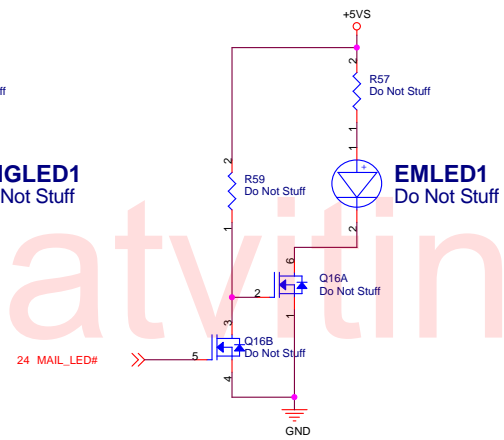
**POWER LED**



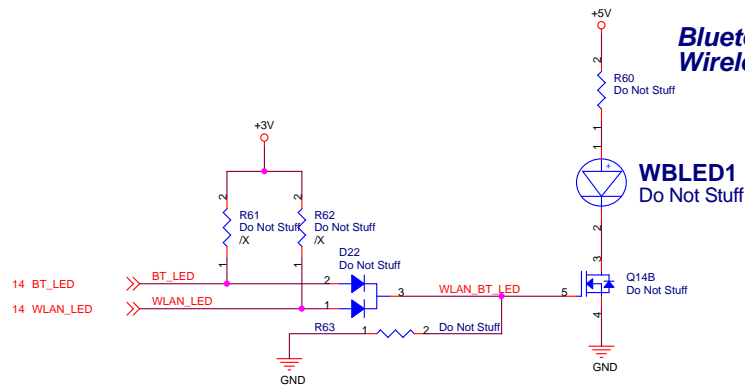
**Battery Charge LED**



**Email LED**

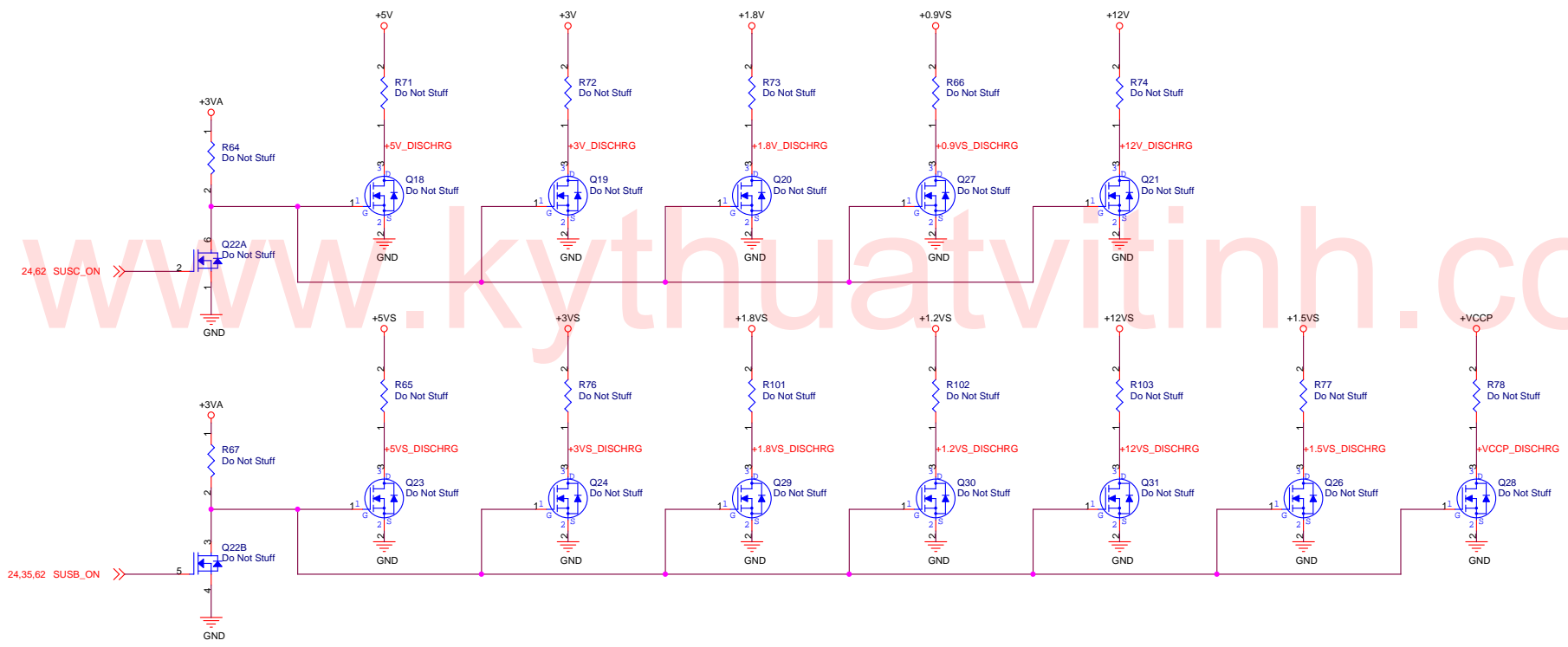


**Bluetooth LED  
Wireless LED**

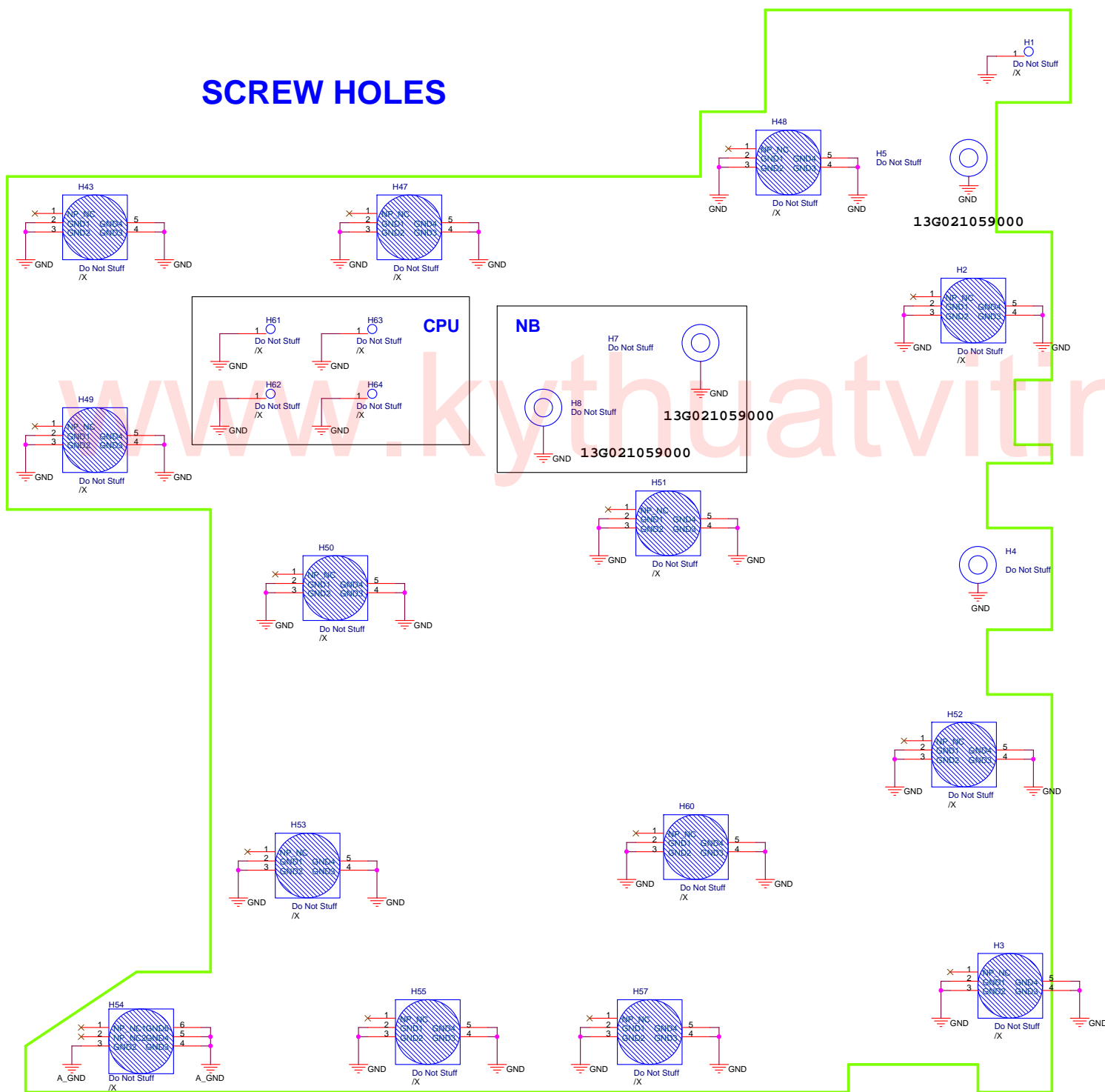


LUNCH

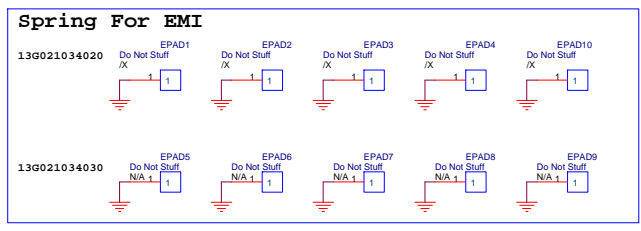
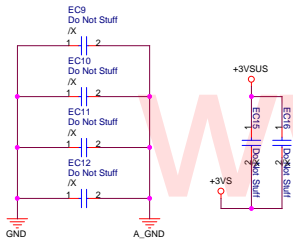
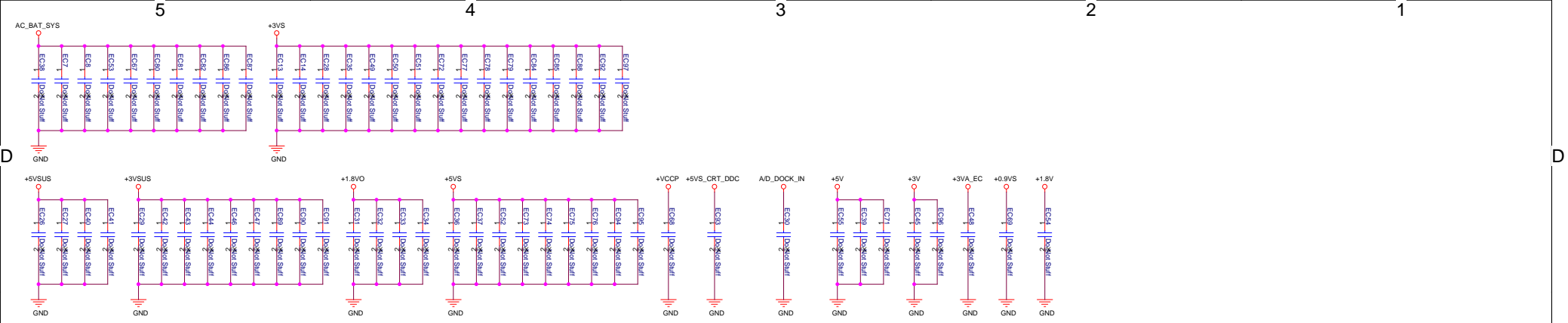
		<b>Title :</b> LED
ASUSTek Computer INC.		<b>Engineer:</b> Jack Hsu
Size	Project Name	Rev
Custom	Z62H	1.0
Date: Thursday, August 09, 2007	Sheet 49 of 63	

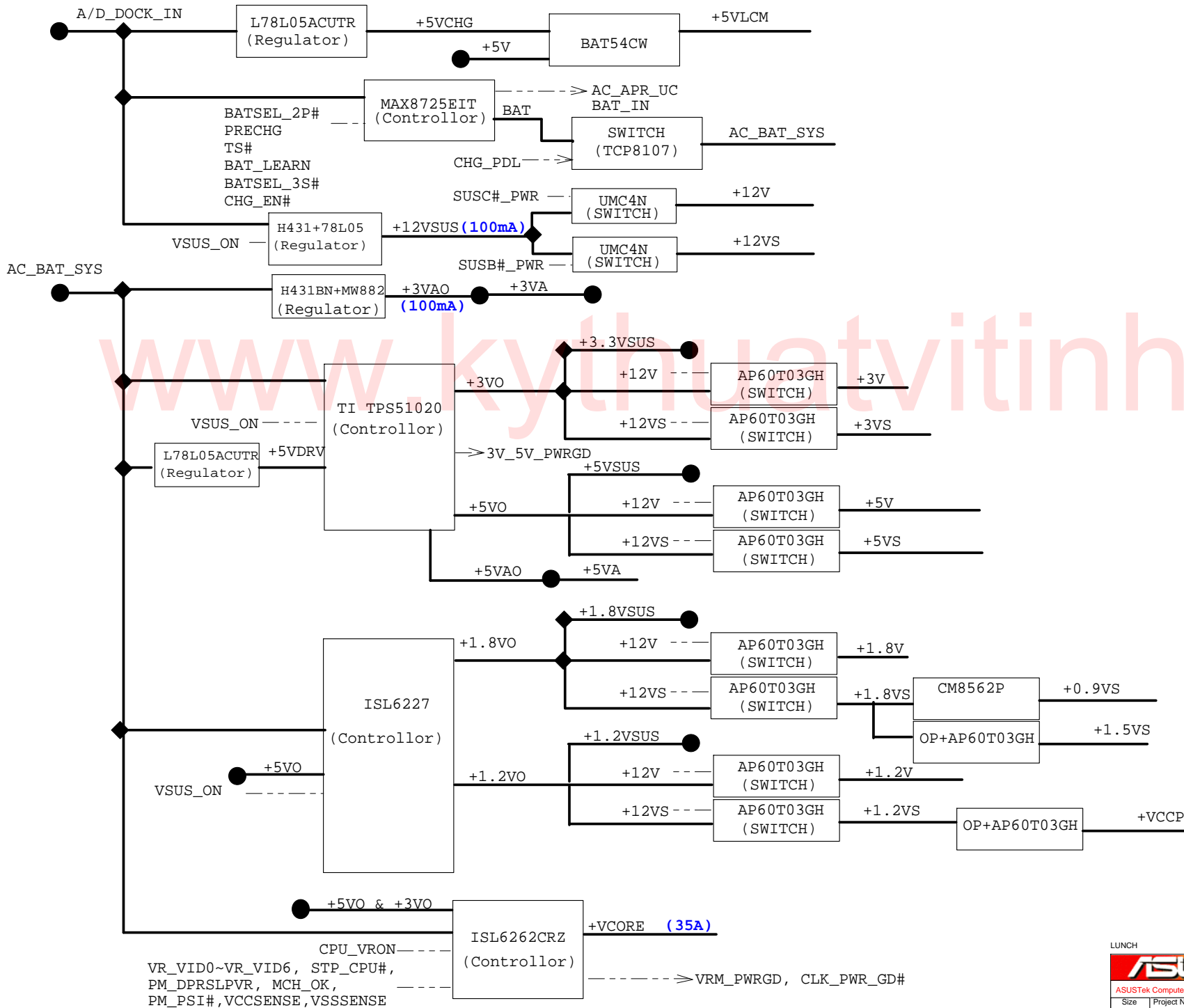


# SCREW HOLES



LUNCH		<b>ASUS</b> Title : Screw Hole	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z62H	1.0	
Date: Thursday, August 09, 2007	Sheet	51	of 63





**Setting the Adapter Input Current Limit**  
 Adapter I<sub>in</sub>(max) = [0.075V/R<sub>sense</sub>(ADin)]\*[V<sub>CLS</sub>/V<sub>REF</sub>]  
 V<sub>CLS</sub>= 2.865V  
**Adaptor Max. Current :**  
 PR5708=20K PR5714 = 178K; I<sub>limit</sub> = 4.5A; 81W  
 PR5708=27K PR5714 = 47K; I<sub>limit</sub> = 3.175A; 60W

**Setting the Charge Voltage**  
 V<sub>batt</sub> = Cell \* ( V<sub>ref</sub> + ( V<sub>CTL</sub> - 1.8V) / 9.52 )  
 V<sub>CTL</sub>= 1.588V => V<sub>batt</sub> = 4.2V

**Setting the Charge Current**  
 Charge Current I<sub>chg</sub> = [0.075V/R<sub>sense</sub>(CHG)]\*[V<sub>CTL</sub>/3.6V]  
 R<sub>sense</sub>(CHG)= 15m Ohm  
**Pre-Charging Mode :**  
 Precharging current = 148 - 152mA  
 V<sub>ctl</sub> = 0.107V - 0.109V  
**Battery Cell Selection :**  
 BATSEL\_2P# = 1, 3 Cells; V<sub>ctl</sub> = 2.084V  
 => I<sub>charge</sub> = 1.6933A  
 BATSEL\_2P# = 0, 6 or 9 Cells; V<sub>ctl</sub> = 2.111V  
 => I<sub>charge</sub> = 2.9329A  
 PR5709=120K PR5715 = 120K; I<sub>charge</sub> = 2.9329A

Mode pin : V<sub>mode</sub> > 2.8V (try to LDO pin) ----> 4 Cells  
 2.0 > V<sub>mode</sub> > 1.6V (floating) ----> 3 Cells  
 0.8 > V<sub>mode</sub> (try to GND) ----> Learning mode  
 V<sub>CTL</sub> < 0.8V or DCIN < 7V ----> Charger Disable

MAX8725\_REF : 4.2235V  
 MAX8725\_LDO : 5.4V

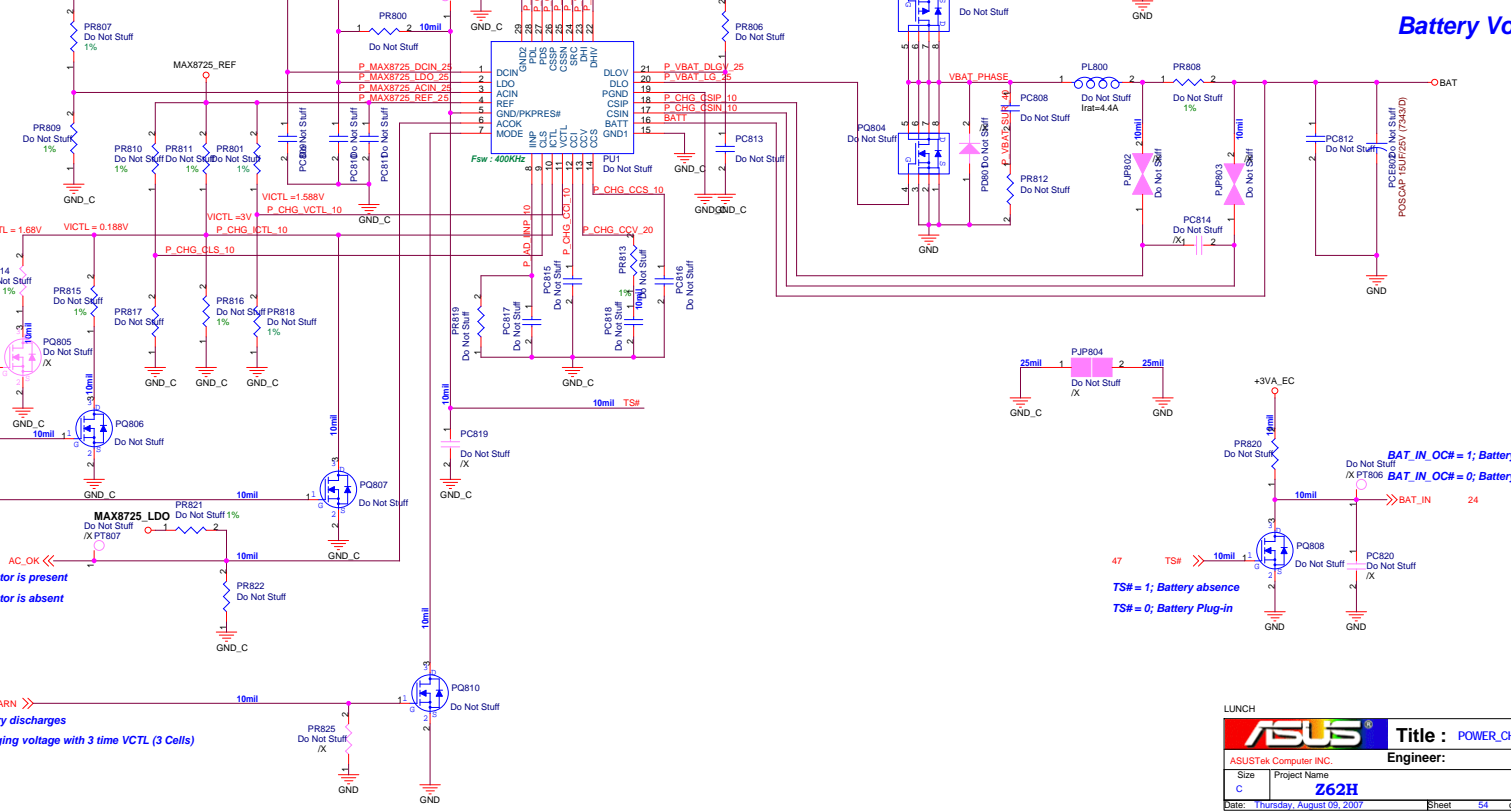
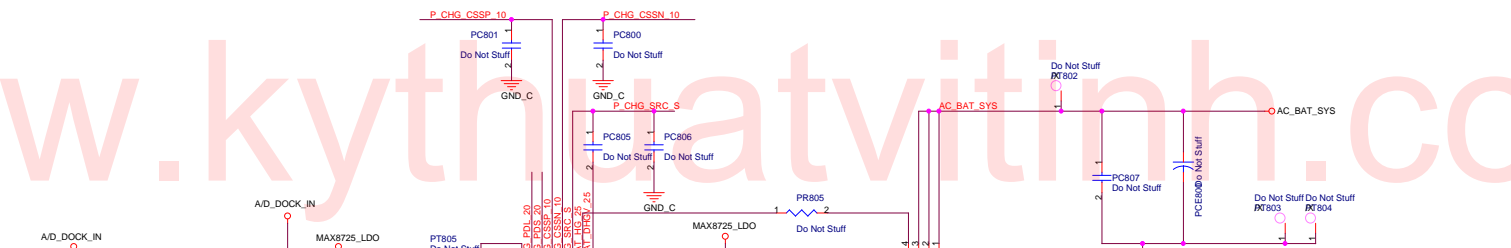
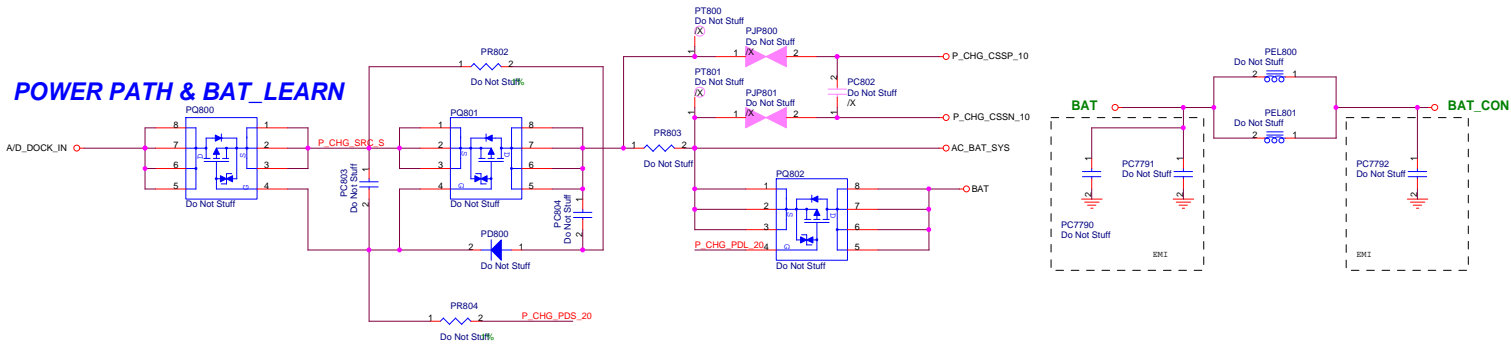
24 BATSEL\_2P#  
 BATSEL\_2P# = 1, 3 Cells  
 BATSEL\_2P# = 0, 6 or 9 Cells

24 PRECHG  
 PRECHG = 1, Pre-Charging Mode  
 Charging Current = 156mA

24 CHG\_EN#  
 CHG\_EN# = 1, Charger Disabled  
 CHG\_EN# = 0, Charger Enabled

24 AC\_OK  
 AC\_OK = 1, Adaptor is present  
 AC\_OK = 0, Adaptor is absent

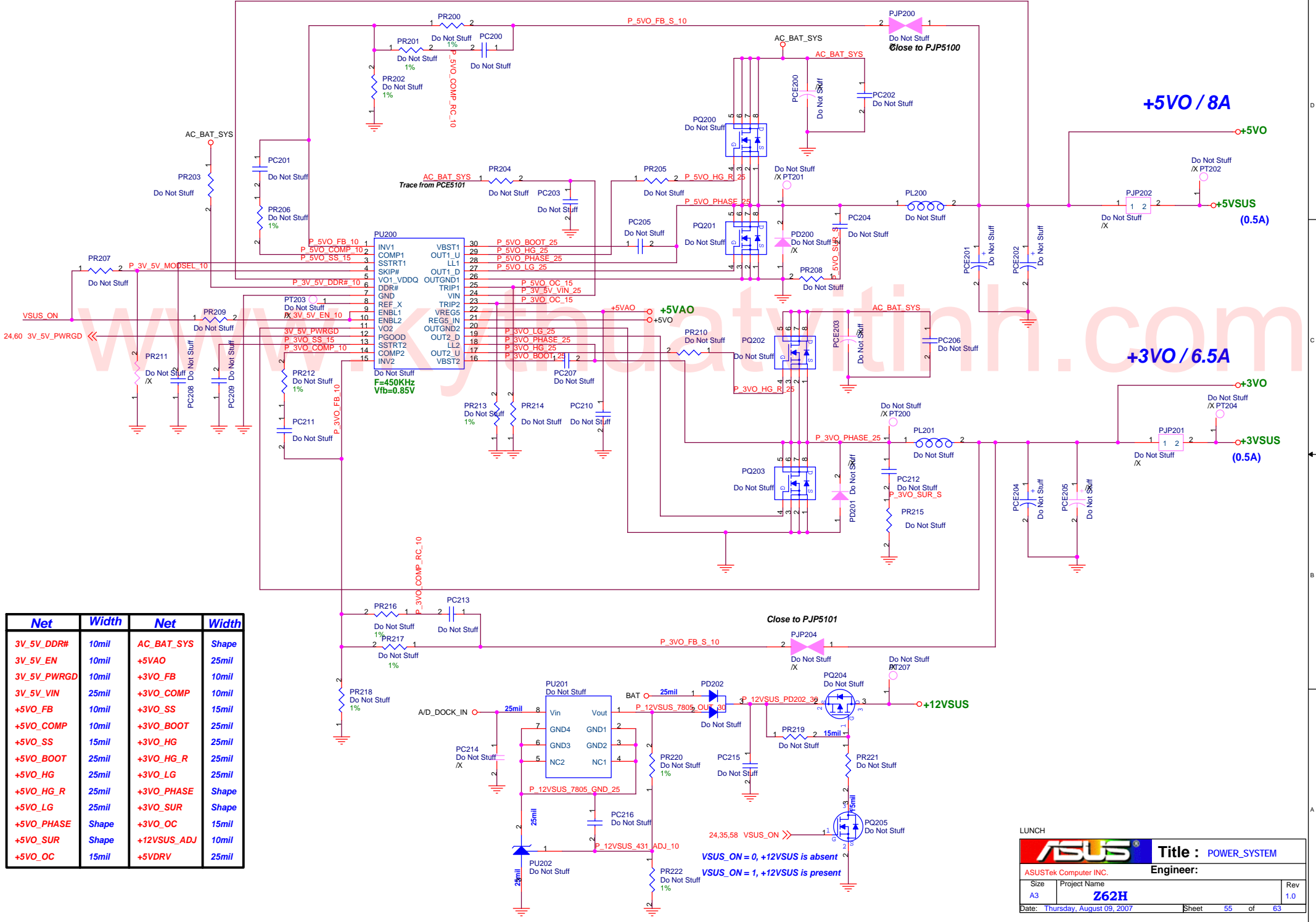
24 BAT\_LEARN  
 BAT\_LEARN = 1, Battery discharges  
 BAT\_LEARN = 0, charging voltage with 3 time V<sub>CTL</sub> (3 Cells)



Battery Voltage

BAT\_IN\_OC# = 1; Battery absence  
 BAT\_IN\_OC# = 0; Battery Plug-in

TS# = 1; Battery absence  
 TS# = 0; Battery Plug-in



**+5V0 / 8A**

**+5VSUS (0.5A)**

**+3V0 / 6.5A**

**+3VSUS (0.5A)**

Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5V0_FB	10mil	+3VO_SS	15mil
+5V0_COMP	10mil	+3VO_BOOT	25mil
+5V0_SS	15mil	+3VO_HG	25mil
+5V0_BOOT	25mil	+3VO_HG_R	25mil
+5V0_HG	25mil	+3VO_LG	25mil
+5V0_HG_R	25mil	+3VO_PHASE	Shape
+5V0_LG	25mil	+3VO_SUR	Shape
+5V0_PHASE	Shape	+3VO_OC	15mil
+5V0_SUR	Shape	+12VSUS_ADJ	10mil
+5V0_OC	15mil	+5VDRV	25mil

**Close to PJP5101**

**VSUS\_ON = 0, +12VSUS is absent**  
**VSUS\_ON = 1, +12VSUS is present**

LUNCH

<b>ASUS</b>		<b>Title : POWER_SYSTEM</b>	
ASUSTek Computer INC.		Engineer:	
Size	A3	Project Name	<b>Z62H</b>
Date:	Thursday, August 09, 2007	Sheet	55 of 63
Rev	1.0		

24 CPU\_VRON >>>  
**CPU\_VRON = 1, Vcore Regulator Enabled**  
**PM\_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled**  
 14.27 PM\_DPRSLPVR >>>

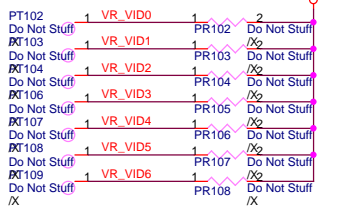
3.14,27 H\_DPRSTP# >>>  
 14.23,27 STP\_CPU# >>>

23 CLK\_EN# <<<  
**CLK\_EN# = 0, Enable Clock Gen**  
**To Clock Gen**

8.14,24,27,60 VRM\_PWRGD <<<  
**VRM\_PWRGD = 1, Vcore Power OK**  
**To N/B**

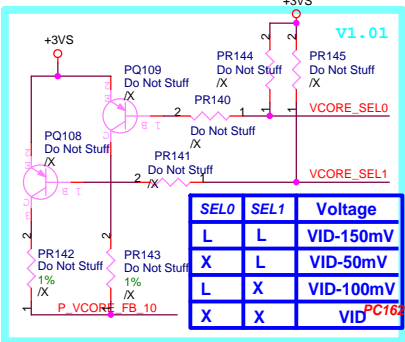
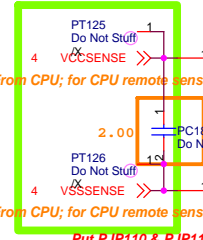
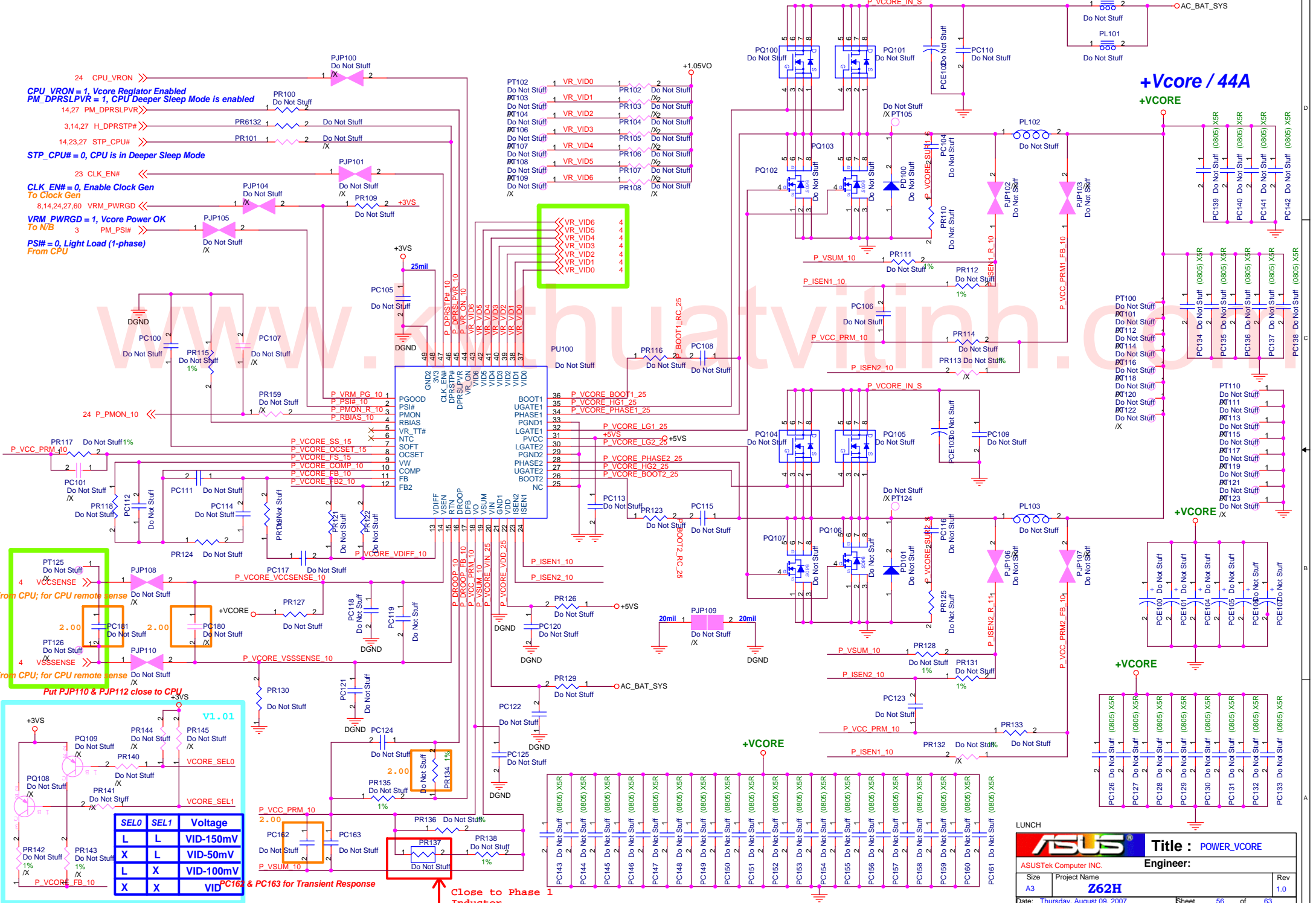
3 PM\_PSH# <<<  
**PSH# = 0, Light Load (1-phase)**  
**From CPU**

24 P\_PMON\_10 <<<



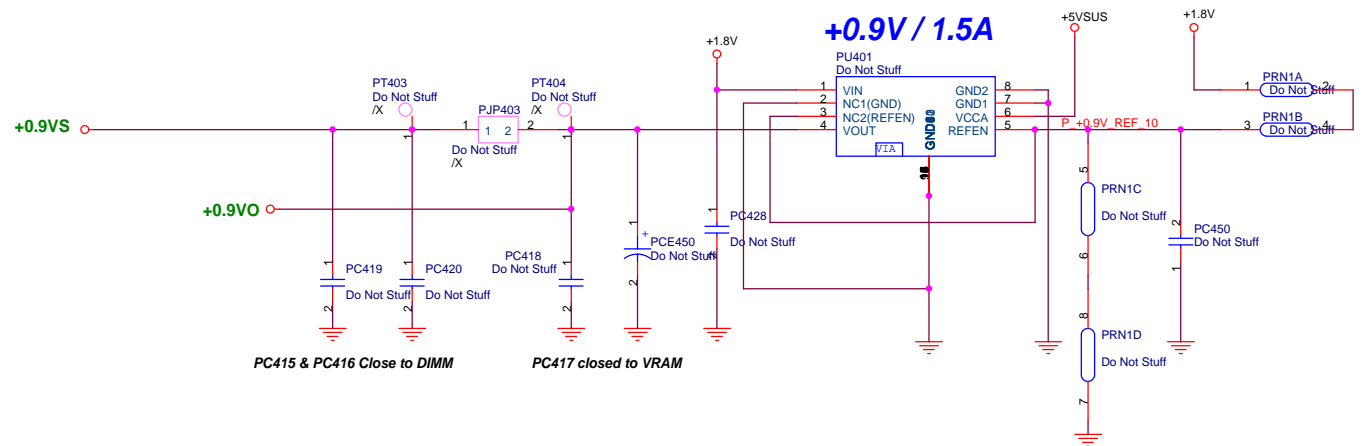
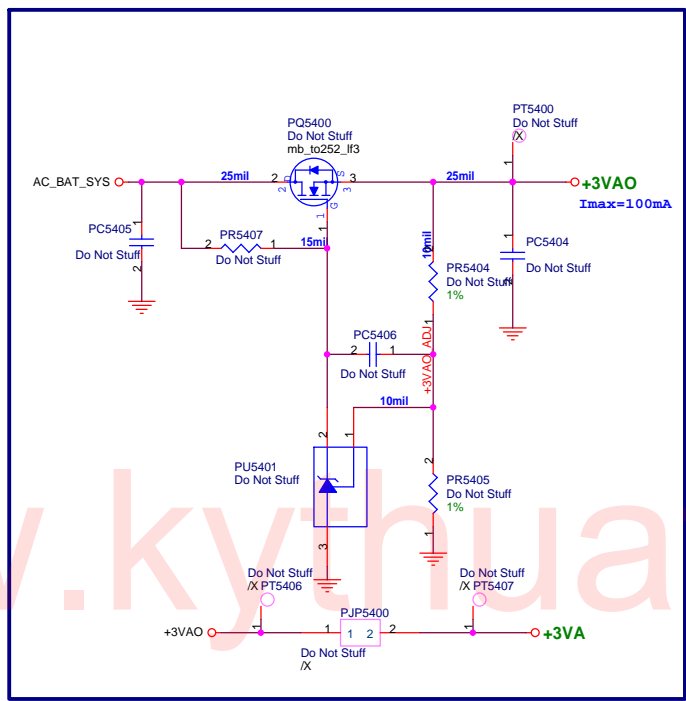
### +Vcore / 44A

+VCORE



Close to Phase 1 Inductor

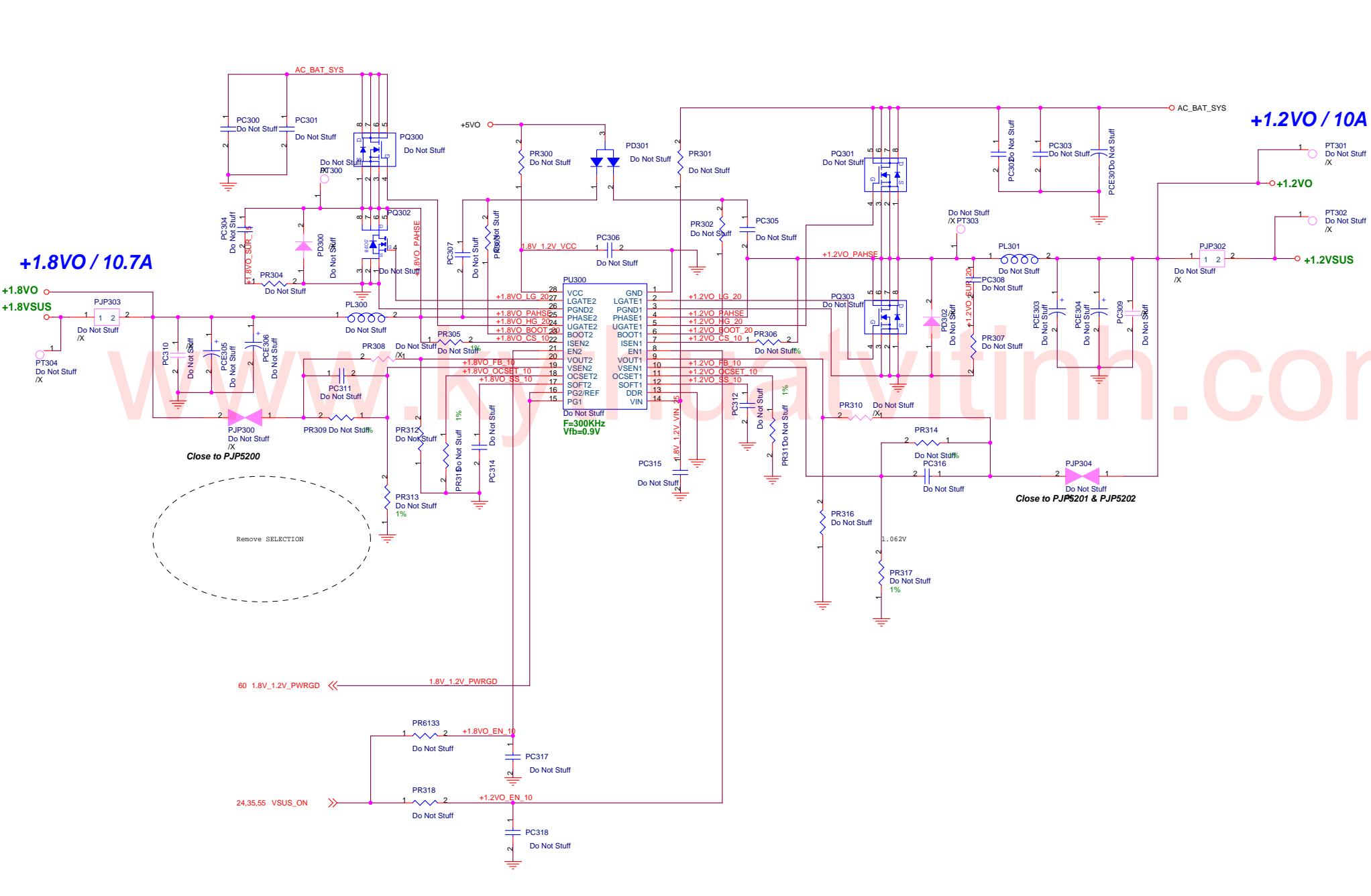




www.kyhuatvith.com

DDR Power Rev:1.00  
LUNCH

<b>ASUS</b>		<b>Title :</b>	
ASUSTek Computer INC.		<b>Engineer:</b>	
Size	Project Name		Rev
A3			1.0
Date: Thursday, August 09, 2007			Sheet 57 of 63



**+1.8VO / 10.7A**

**+1.2VO / 10A**

**+1.8VO**  
**+1.8VSUS**

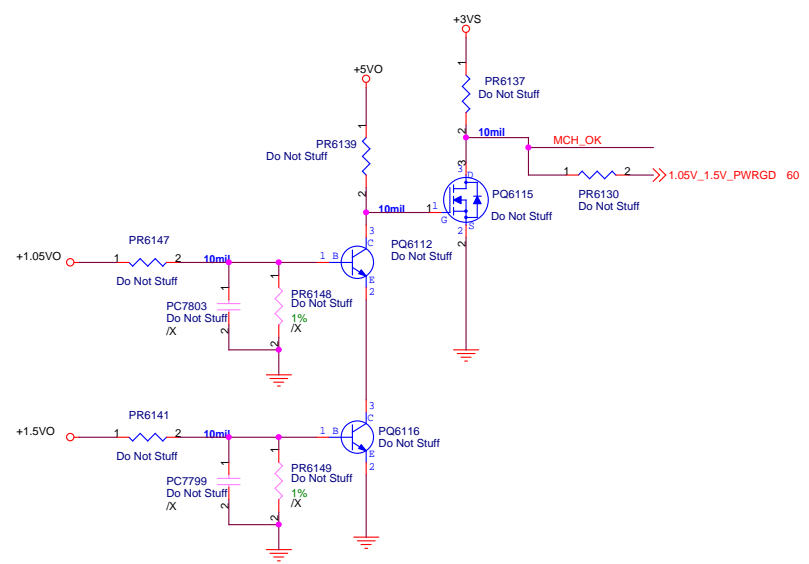
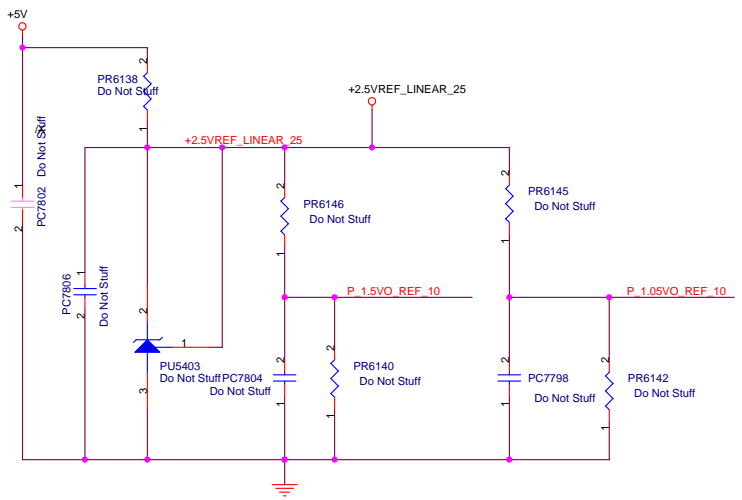
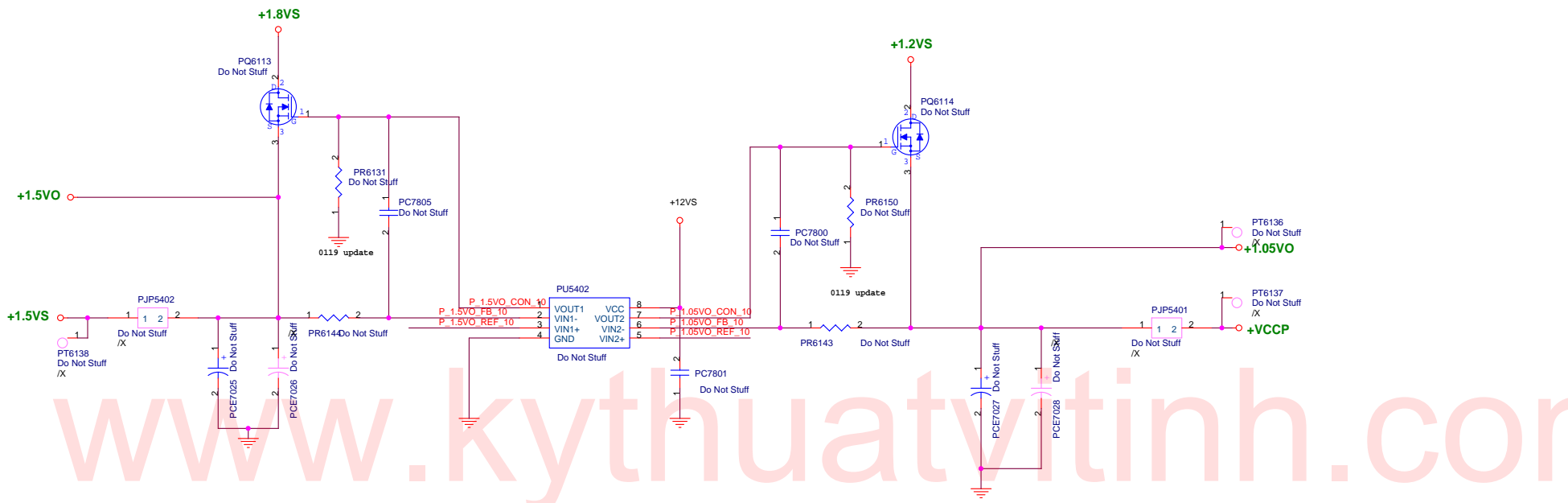
Remove SELECTION

Close to PJP5200

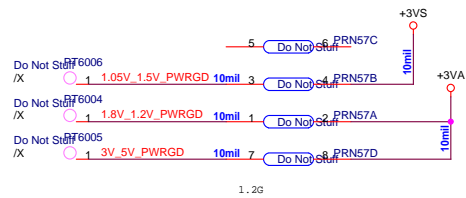
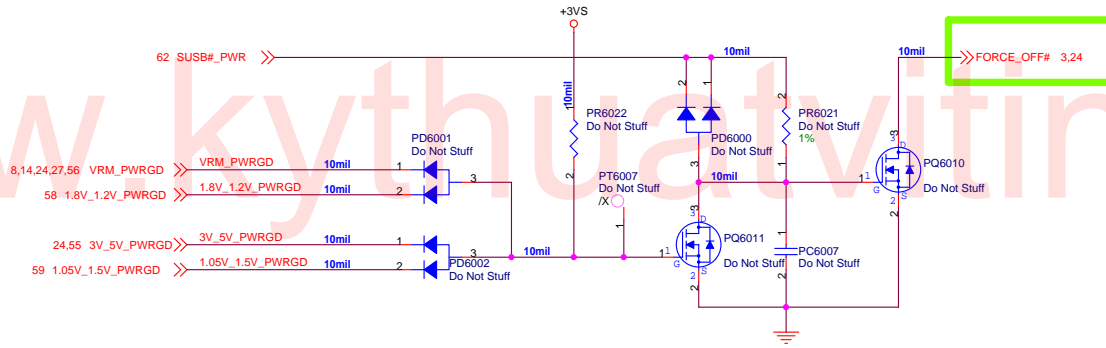
Close to PJP5201 & PJP5202

LUNCH

<b>ASUS</b>		Title :POWER_UO_1.5VS & 1.0VS	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	<b>Z62H</b>	1.0	
Date:	Thursday, August 09, 2007	Sheet	58 of 63



### Power Good Detector



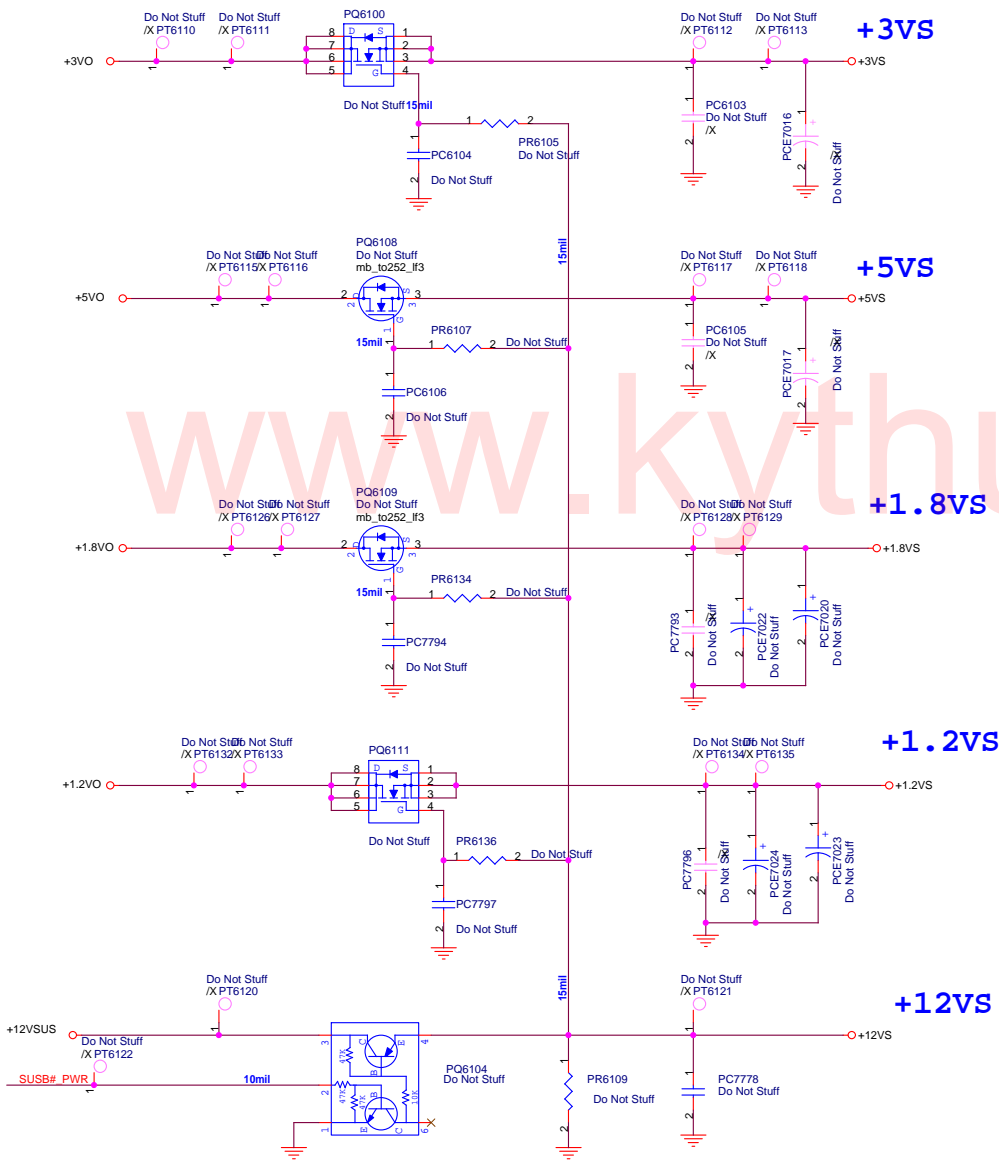
LUNCH

<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
ASUSTek Computer INC.		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	<b>Z62H</b>	1.0	
Date:	Friday, August 10, 2007	Sheet	60 of 63

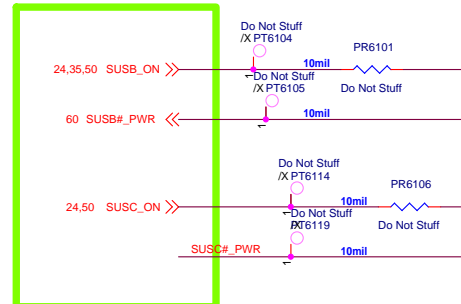
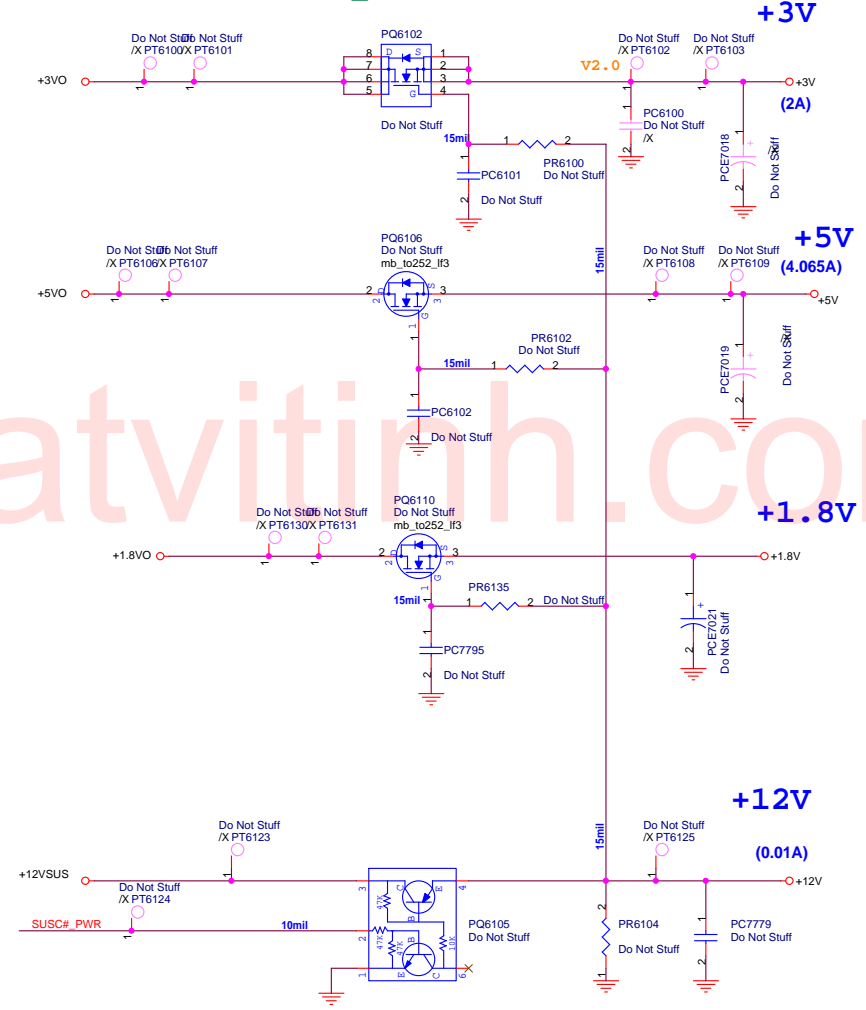
www.kythuatvitinh.com

LUNCH		
		Title : POWER_BLANK
ASUSTek Computer INC.		Engineer:
Size	Project Name	Rev
Custom	Z62H	1.0
Date:	Thursday, August 09, 2007	Sheet 61 of 63

### SUSB#\_PWR POWER



### SUSC#\_PWR POWER



LUNCH

**ASUS** Title : POWER\_LOAD SWITCH

ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 62 of 63

Rev	Date	Description
1.0	2007/02/14	1. Initial release.
1.1	2007/05/29	1. Change to SiSM672, SiS968, SiS307

Rev	Date	Description
-----	------	-------------

www.kythuatvithinh.com