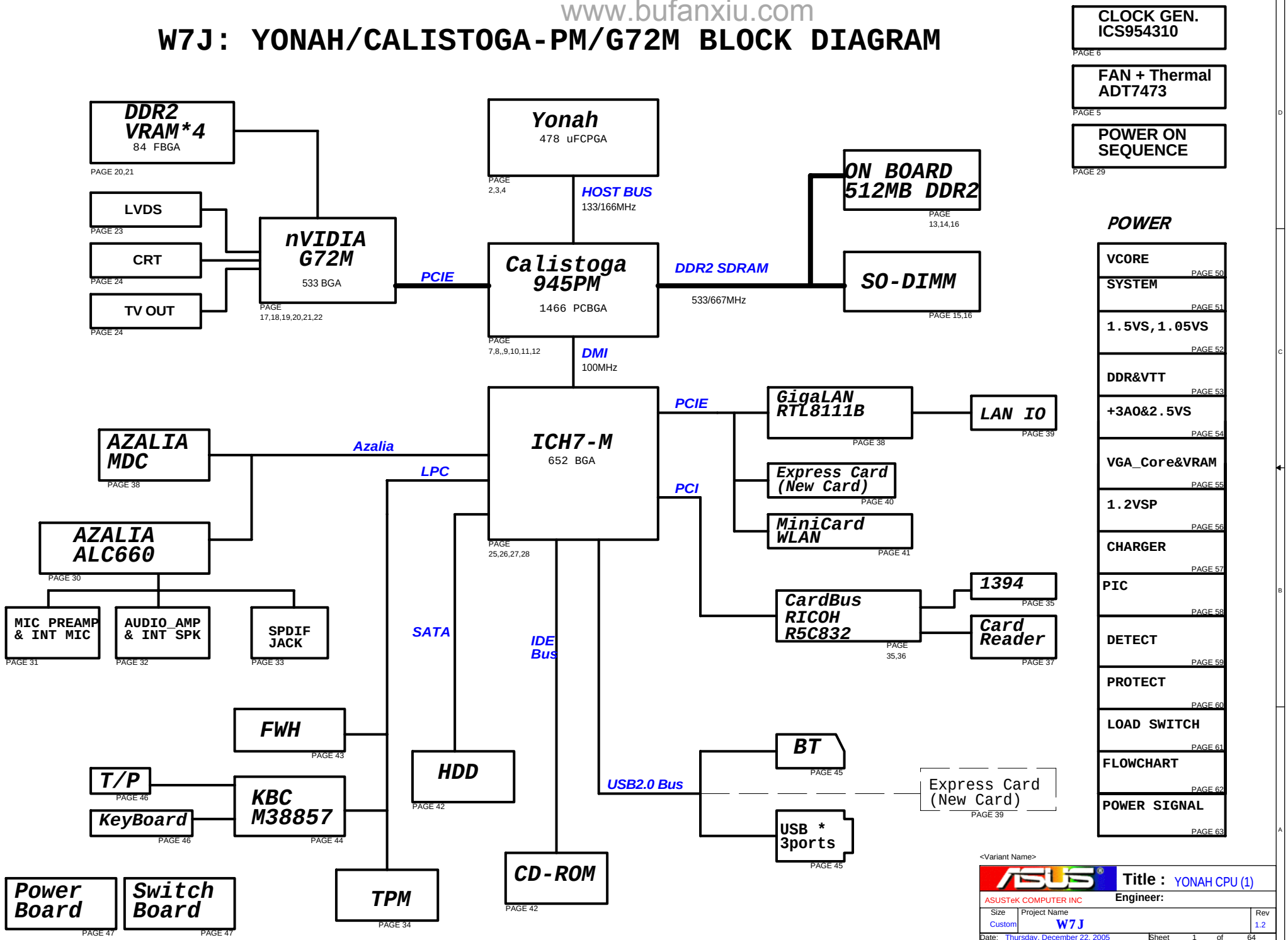
W7J: YONAH/CALISTOGA-PM/G72M BLOCK DIAGRAM



POWER

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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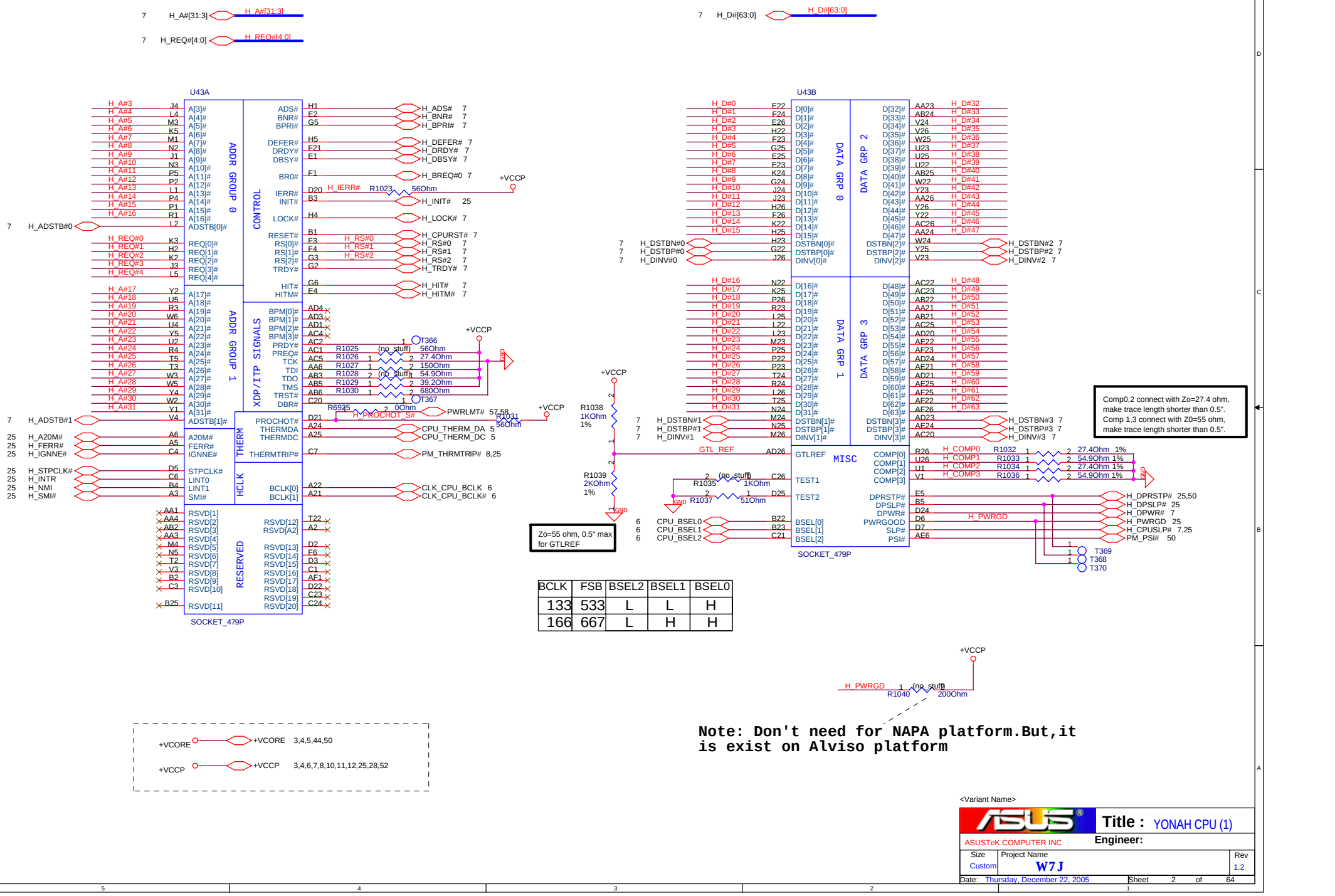

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Note: Don't need for NAPA platform.But,it is exist on Alviso platform

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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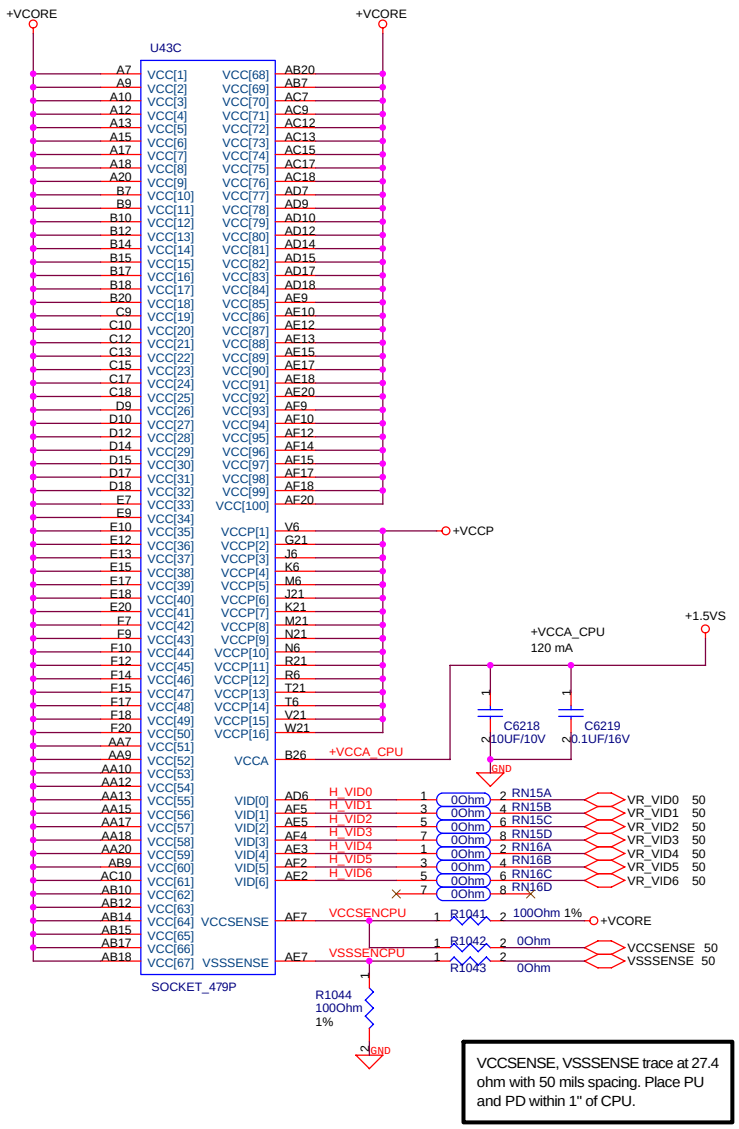
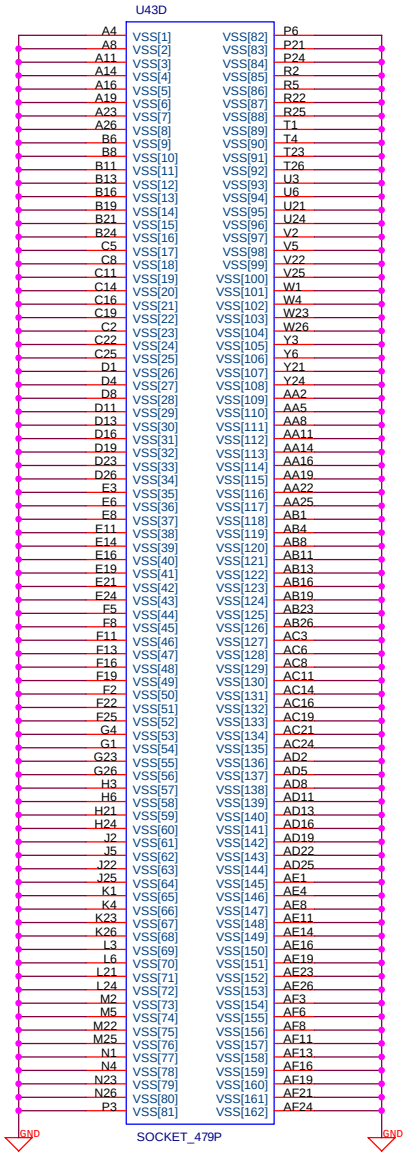
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



<Variant Name>

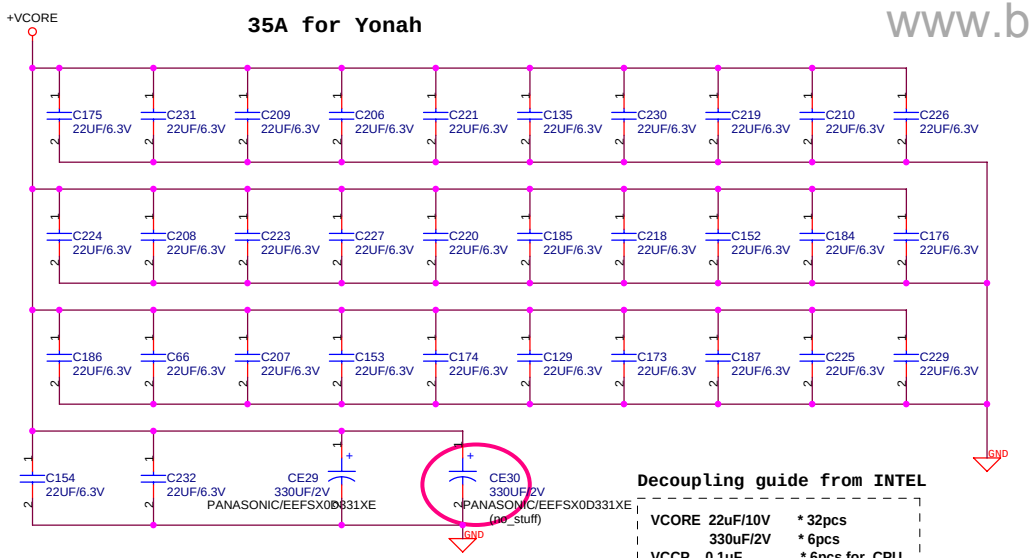
ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

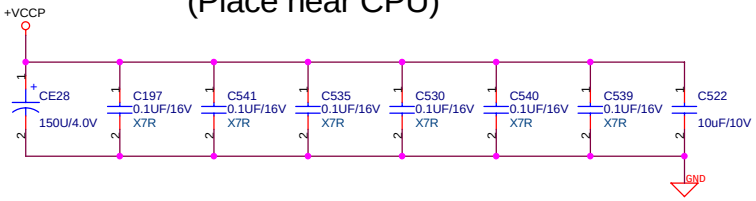
Date: Thursday, December 22, 2005 Sheet 3 of 64



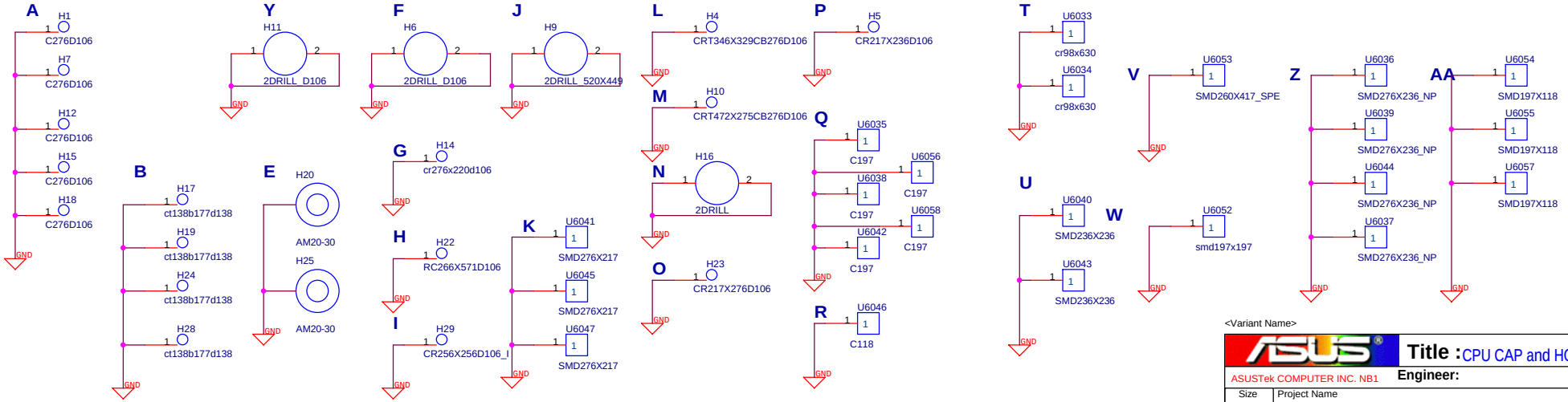
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



SCREW HOLE



<Variant Name>

Title : CPU CAP and HOLES

ASUSTek COMPUTER INC. NB1 **Engineer:**

Size	Project Name	Rev
Custom	W7J	1.2

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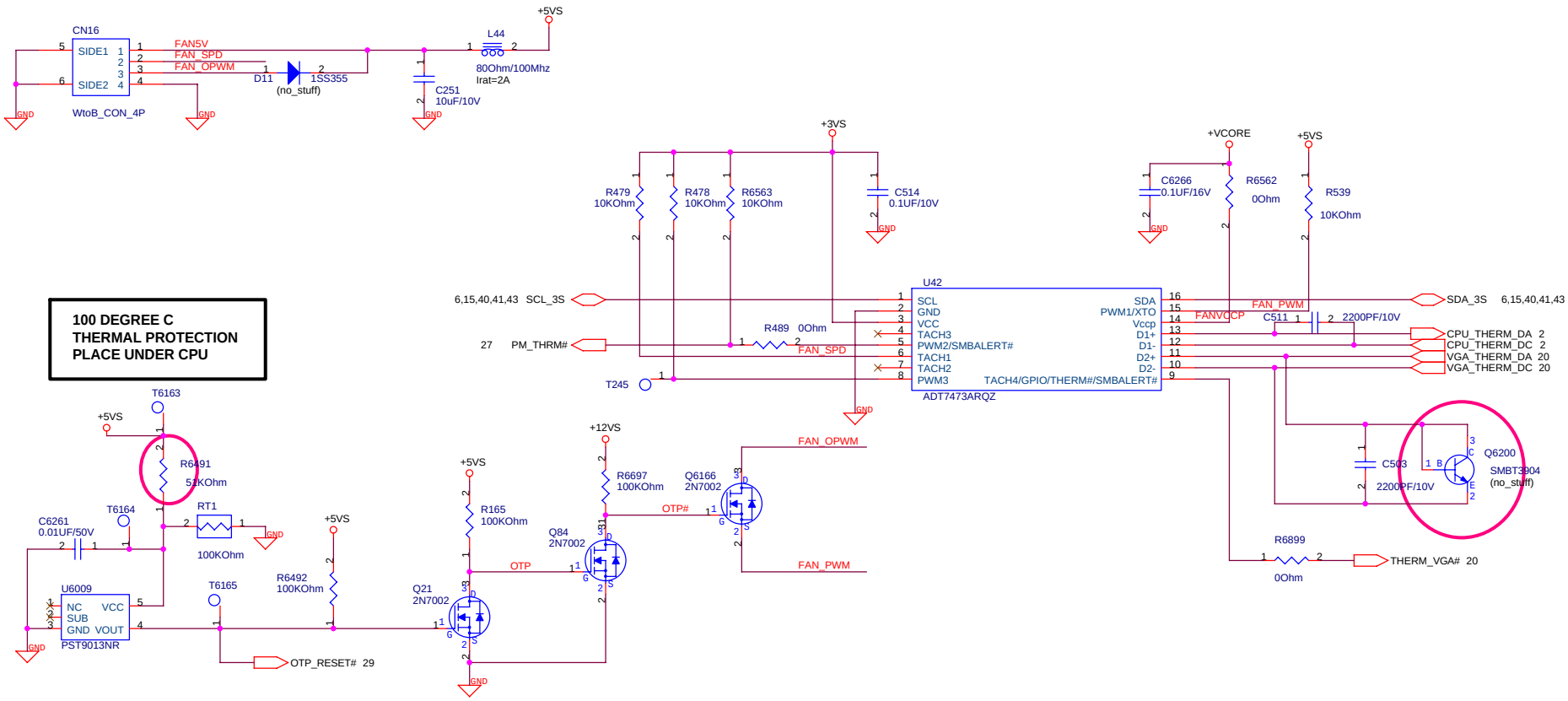
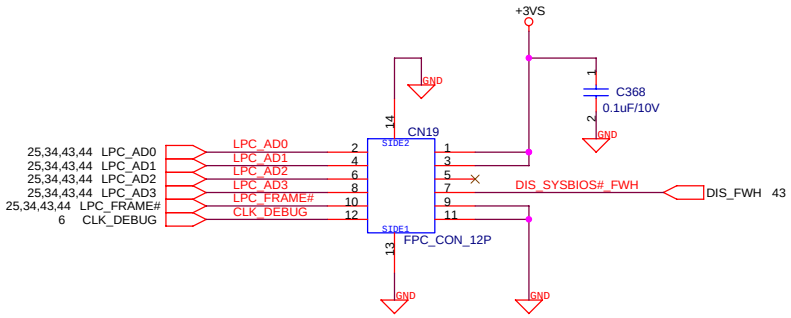
FAN & THERMAL CONTROLLER



LPC DEBUG PORT



<Variant Name>

Title : FAN & debug port

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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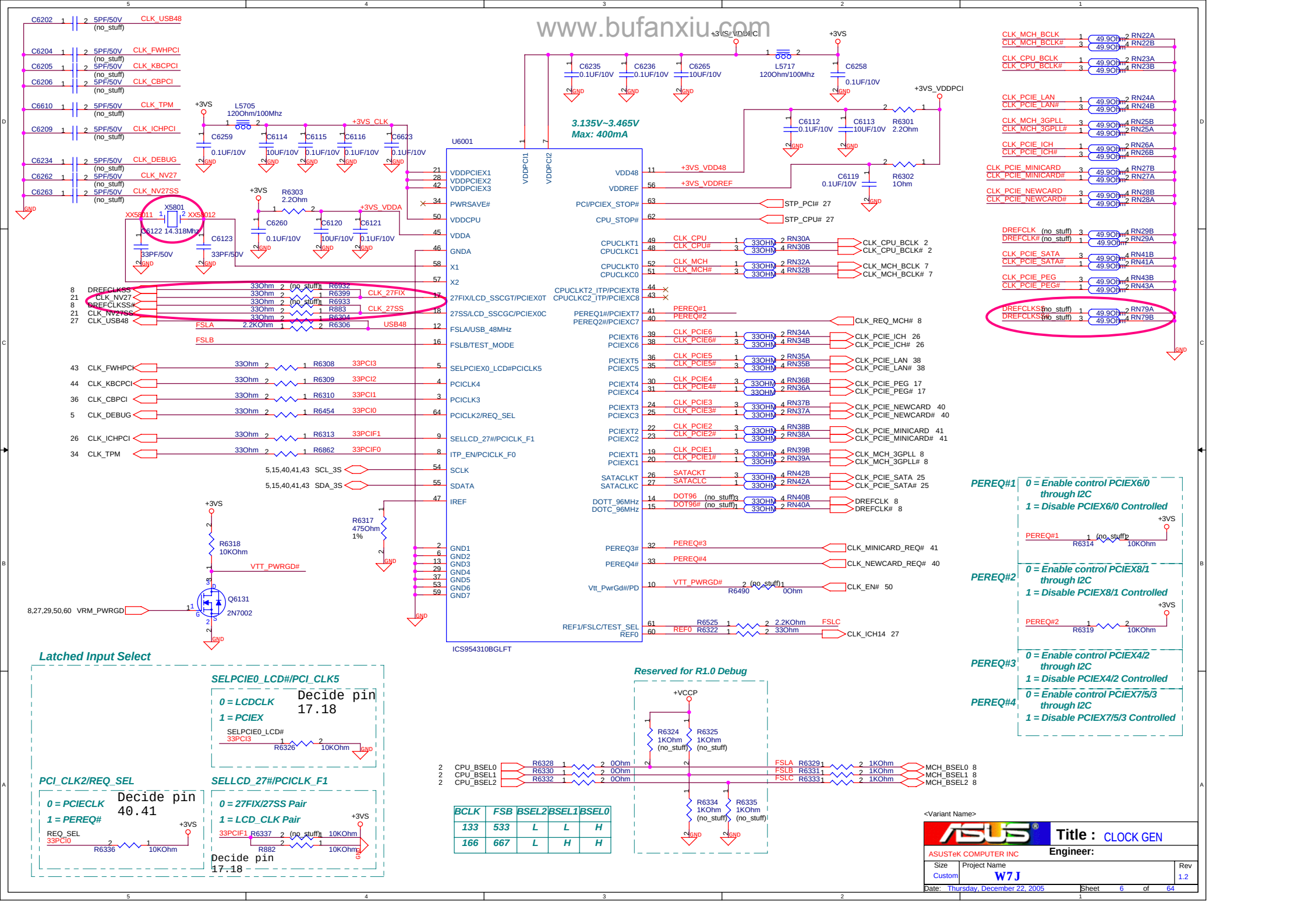

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

<variant_name>

ASUSTeK COMPUTER INC

Title : CLOCK GEN

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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2 H_A#[31:3] H_A#[31:3]

2 H_REQ#[4:0] H_REQ#[4:0]

2 H_D#[63:0] H_D#[63:0]

R1045 24.9Ohm 1% H_XRCOMP

R1046 24.9Ohm 1% H_YRCOMP

GND

Trace should be 10 mil wide with 20 mil spacing

+VCCP

R1047 54.9Ohm 1% H_XSCOMP

R1048 54.9Ohm 1% H_YSCOMP

+VCCP

R1051 221Ohm

H_XSWING

R1052 100Ohm 1%

C953 0.1UF/16V

GND GND

Trace should be 10 mil wide with 20 mil spacing

+VCCP

R1053 221Ohm

H_YSWING

R1055 100Ohm 1%

C954 0.1UF/16V

GND GND

U39A

HOST

CALISTOGA_Q137

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	
H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
6 CLK_MCH_BCLK	AG2	H_CLKIN	
6 CLK_MCH_BCLK#	AG1	H_CLKIN#	

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	
H_ADS#	E8	H_ADS#	H_ADS# 2
H_ADSTB#_0	B9	H_ADSTB#0	H_ADSTB#0 2
H_ADSTB#_1	C13	H_ADSTB#1	H_ADSTB#1 2
H_AVREF	J13		
H_BNR#	C6	H_BNR#	H_BNR# 2
H_BPRI#	F6	H_BPRI#	H_BPRI# 2
H_BREQ#0	C7	H_BREQ#0	H_BREQ#0 2
H_CPURST#	B7	H_CPURST#	H_CPURST# 2
H_DBSY#	A7	H_DBSY#	H_DBSY# 2
H_DEFER#	C3	H_DEFER#	H_DEFER# 2
H_DPWR#	J9	H_DPWR#	H_DPWR# 2
H_DRDY#	H8	H_DRDY#	H_DRDY# 2
H_DVREF	K13		
H_DINV#_0	J7		H_DINV#0 2
H_DINV#_1	W8		H_DINV#1 2
H_DINV#_2	U3		H_DINV#2 2
H_DINV#_3	AB10		H_DINV#3 2
H_DSTBN#_0	K4		H_DSTBN#0 2
H_DSTBN#_1	T7		H_DSTBN#1 2
H_DSTBN#_2	Y5		H_DSTBN#2 2
H_DSTBN#_3	AC4		H_DSTBN#3 2
H_DSTBP#_0	K3		H_DSTBP#0 2
H_DSTBP#_1	T6		H_DSTBP#1 2
H_DSTBP#_2	AA5		H_DSTBP#2 2
H_DSTBP#_3	AC5		H_DSTBP#3 2
H_HIT#	D3		H_HIT# 2
H_HITM#	D4		H_HITM# 2
H_LOCK#	B3		H_LOCK# 2
H_REQ#_0	D8	H_REQ#0	
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	
H_RS#_0	B4	H_RS#0	H_RS#0 2
H_RS#_1	E6	H_RS#1	H_RS#1 2
H_RS#_2	D6	H_RS#2	H_RS#2 2
H_SLPCPU#	E3	R1054 0Ohm	H_CPUSLP# 2,25
H_TRDY#	E7		H_TRDY# 2

+VCCP

R1049 100Ohm 1%

H_VREF

R1050 200Ohm 1%

C952 0.1UF/10V

GND GND

Close to GMCH in 100 mil

<Variant Name>

Title : Calistoga -- CPU (1)

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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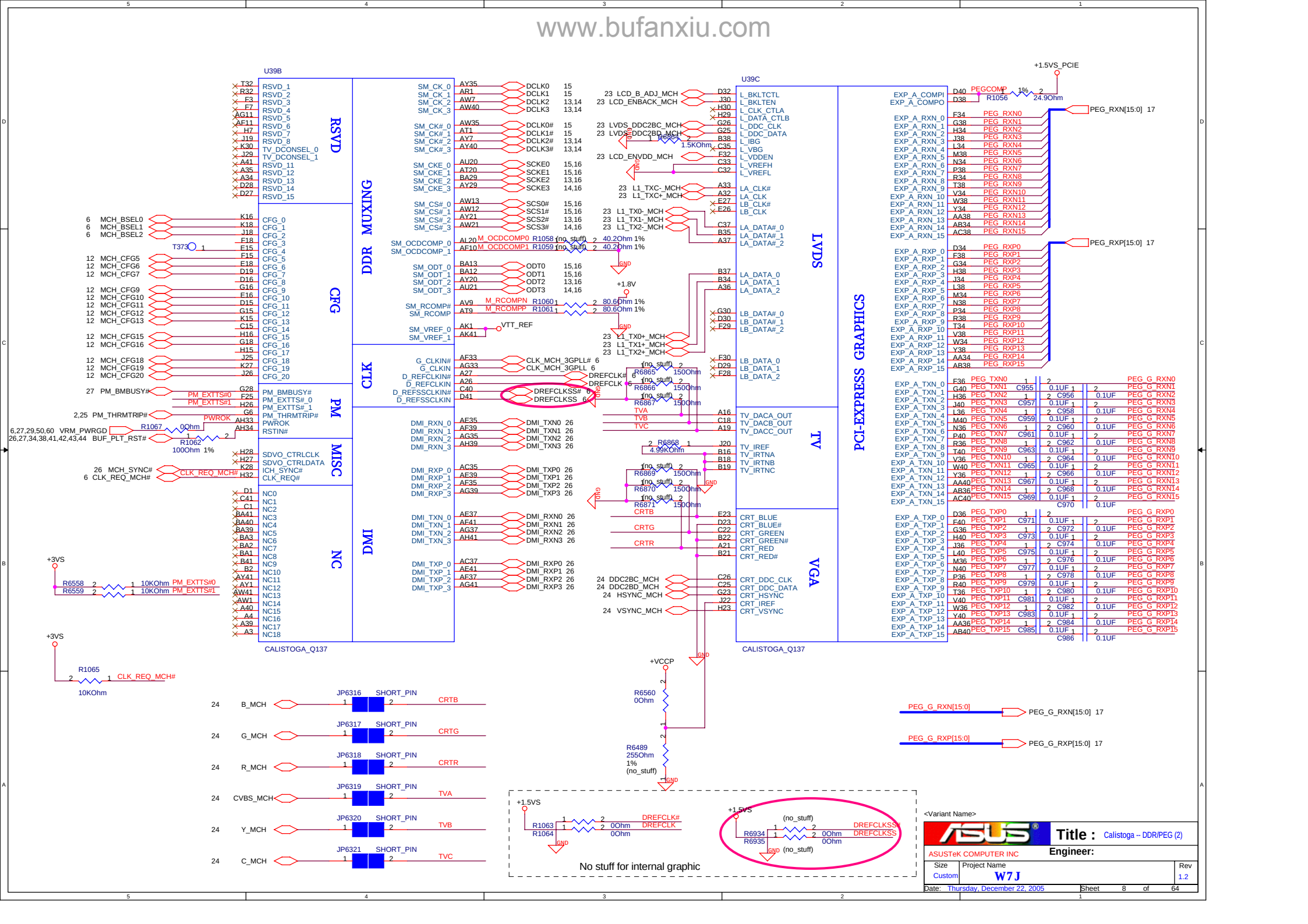

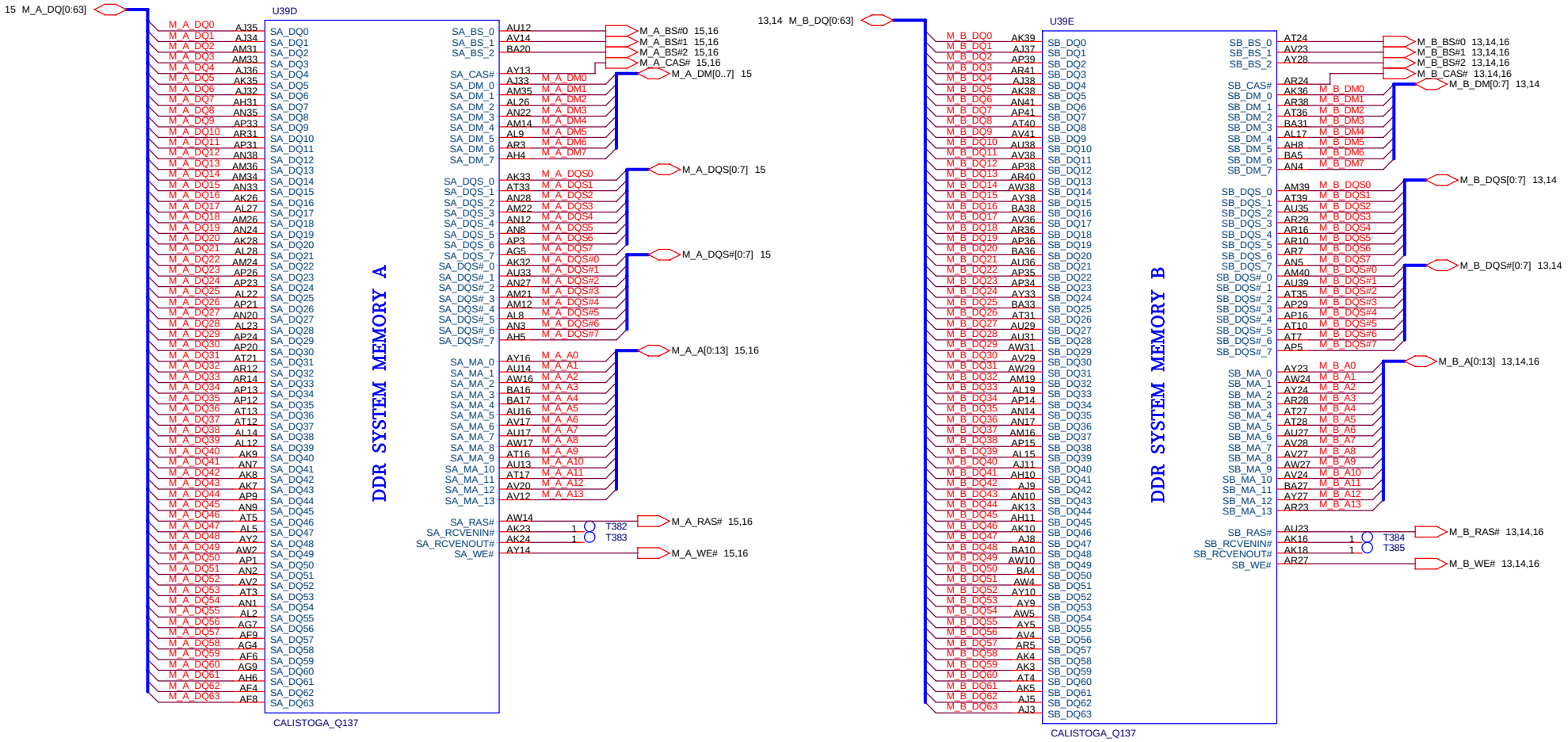

<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga -- DDR bus (3)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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+VCCP
+2.5VS
D6036
BAT54C
R6872
10Ohm
+2.5VS_CRTDAC_R
L5778
180Ohm/100Mhz
+2.5VS_CRTDAC
C6612
0.1UF/16V
C6613
0.022UF/25V
+1.5VS
D6037
BAT54C
R6873
10Ohm
+3VS

VCCA_DPLLA<50mA
VCCA_DPLLB<50mA
VCCA_HPLL<45mA

+1.5VS_PCIE
L146
80Ohm/100Mhz
CE37
220UF/2.5V
C1016
10UF/6.3V
C1017
10UF/6.3V

NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.

VCCA_3GBG
C988
10UF/6.3V
C989
0.1UF/10V

L142
120Ohm/100Mhz
C992
0.1UF/10V
C991
10UF/6.3V
+1.5VS_3GPLL
L143
120Ohm/100Mhz
C1010
0.1UF/10V
CE35
470UF/2.5V
(no_stuff)
+1.5VS_DPLLA
L144
120Ohm/100Mhz
C1013
0.1UF/10V
CE36
470UF/2.5V
(no_stuff)
+1.5VS_DPLLB
L145
120Ohm/100Mhz
C1014
0.1UF/10V
C1015
22UF/6.3V
+1.5VS_HPLL
L147
120Ohm/100Mhz
C1018
0.1UF/10V
C1019
22UF/6.3V
+1.5VS_MPLL
L5779
120Ohm/100Mhz
C6615
22NF/50V
+1.5VS_TVDAC
L5780
120Ohm/100Mhz
C6617
22NF/50V
+1.5VS_QTVDAC

+3VS
VCC_HV
C1004
0.1UF/10V
C1005
10UF/6.3V

+1.5VS
C993
0.1UF/10V
C994
22UF/6.3V
C995
0.1UF/10V
C996
0.1UF/10V

PLACE IN CAVITY
C1001
4.7UF/6.3V
C1002
2.2UF/6.3V

PLACE ON THE EDGE
+VCCP
C1003
0.22UF/6.3V
CE34
100UF/4V

+2.5VS
C6611
0.1UF/16V
c0402

U39H

VCCSYNC H22
VCC_TXLVDS0 C30
VCC_TXLVDS1 B30
VCC_TXLVDS2 A30

VCC3G+VCCA_3GPLL<1500mA
+1.5VS_PCIE
VCC3G0 AJ41
VCC3G1 AB41
VCC3G2 Y41
VCC3G3 V41
VCC3G4 R41
VCC3G5 N41
VCC3G6 L41
+1.5VS_3GPLL
VCCA_3GBG
VCCA_3GPLL AC33
VCCA_3GBG G41
VSSA_3GBG H41
VCCA_3GBG<2mA

+2.5VS_CRTDAC
VCCA_CRTDAC0 F21
VCCA_CRTDAC1 E21
VSSA_CRTDAC G21

+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
VCCA_DPLLA B26
VCCA_DPLLB C39
VCCA_HPLL AF1
+2.5VS
R6908 0Ohm (no_stuff)
R6832 0Ohm (no_stuff)
VCCA_LVDS A38
VSSA_LVDS B39
+1.5VS_MPLL
VCCA_3MPLL<45mA
VCCA_MPLL AF2
+3VS_TVBG
VCCA_TVBG H20
VSSA_TVBG G20

+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
VCCA_TVDACA0 E19
VCCA_TVDACA1 F19
VCCA_TVDACB0 C20
VCCA_TVDACB1 D20
VCCA_TVDACC0 E20
VCCA_TVDACC1 F20

VCCD_HMPLL[0:1]<150mA
+1.5VS
VCCD_HMPLL0 AH1
VCCD_HMPLL1 AH2
VCCD_LVDS0 A28
VCCD_LVDS1 B28
VCCD_LVDS2 C28
+1.5VS_TVDAC
VCCD_TVDAC D21
C1006
0.1UF/10V
VCC_HV
VCC_HV0 A23
VCC_HV1 B23
VCC_HV2 B25
VCC_HV[0:2]<40mA
+1.5VS_QTVDAC
VCCD_QTVDAC H19
C1007
0.1UF/10V

+1.5VS
VCCAUX0 AK31
VCCAUX1 AF31
VCCAUX2 AE31
VCCAUX3 AC31
VCCAUX4 AL30
VCCAUX5 AK30
VCCAUX6 AJ30
VCCAUX7 AH30
VCCAUX8 AG30
VCCAUX9 AE30
VCCAUX10 AE30
VCCAUX11 AD30
VCCAUX12 AC30
VCCAUX13 AG29
VCCAUX14 AF29
VCCAUX15 AE29
VCCAUX16 AD29
VCCAUX17 AC29
VCCAUX18 AG28
VCCAUX19 AF28
VCCAUX20 AE28
VCCAUX21 AH22
VCCAUX22 AJ21
VCCAUX23 AH21
VCCAUX24 AJ20
VCCAUX25 AH20
VCCAUX26 AH19
VCCAUX27 P19
VCCAUX28 P16
VCCAUX29 AH15
VCCAUX30 P15
VCCAUX31 AH14
VCCAUX32 AG14
VCCAUX33 AF14
VCCAUX34 AE14
VCCAUX35 Y14
VCCAUX36 AF13
VCCAUX37 AE13
VCCAUX38 AF12
VCCAUX39 AE12
VCCAUX40 AD12

CALISTOGA_Q137

POWER

+VCCP
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 V14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1

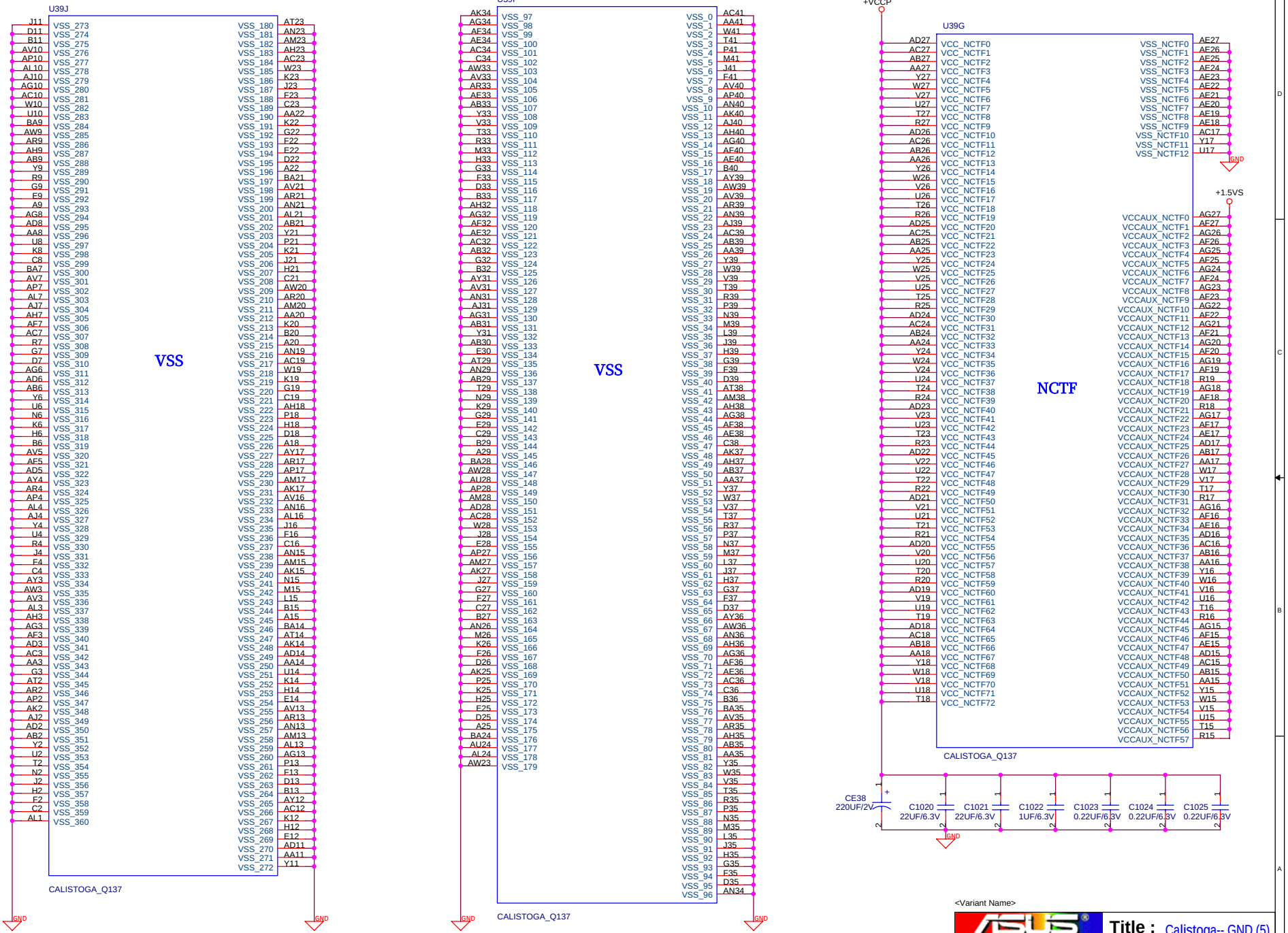
VTT < 1500mA
L2
180Ohm/100Mhz
C48
10UF/6.3V
+3VS
C6619
22UF/6.3V
X5R

+3VS_TVDACA
C6622
22NF/50V
+3VS_TVDACB
C6621
22NF/50V
C54
0.1UF/16V
+3VS_TVDACC
C6620
22NF/50V
C58
0.1UF/16V
+3VS_TVBG
C6618
22NF/50V

VTTLF_CAP3
C1009
0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C1011
0.47UF/16V
C1012
0.22UF/6.3V

<Variant Name>

Title : Calistoga -- POWER (4)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: W7J
Rev: 1.2
Date: Thursday, December 22, 2005
Sheet 10 of 64



<Variant Name>

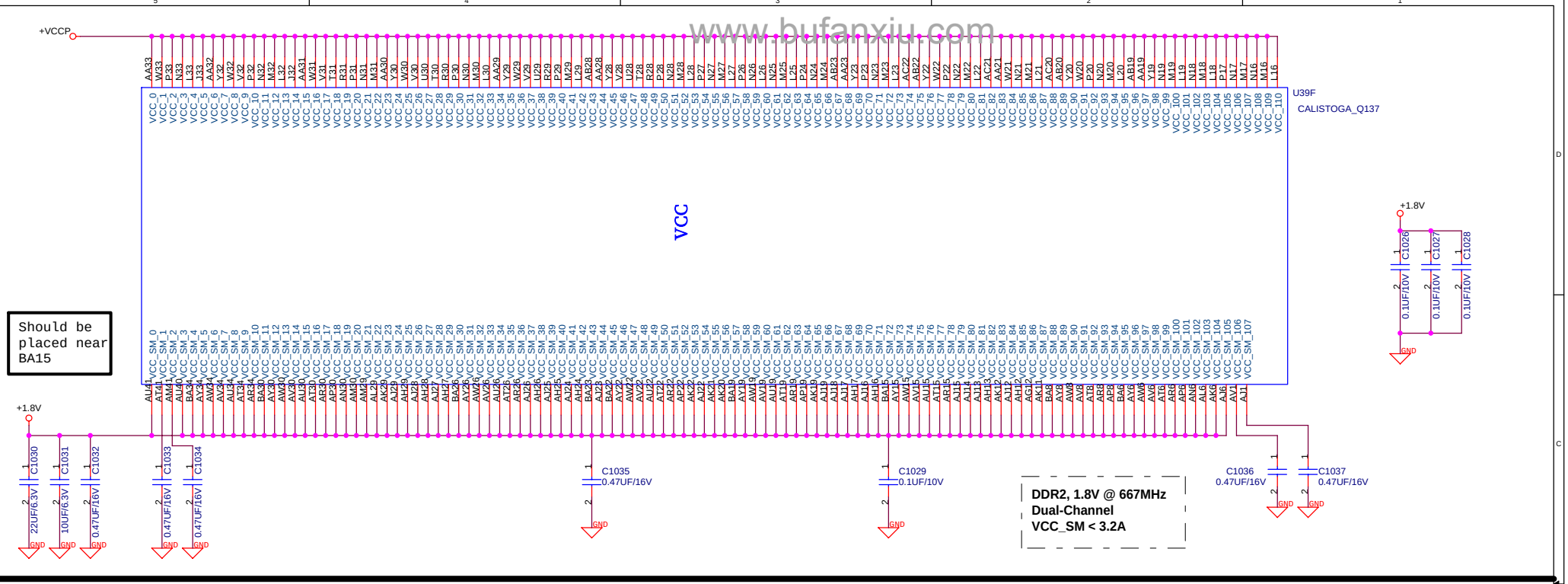
ASUSTeK COMPUTER INC

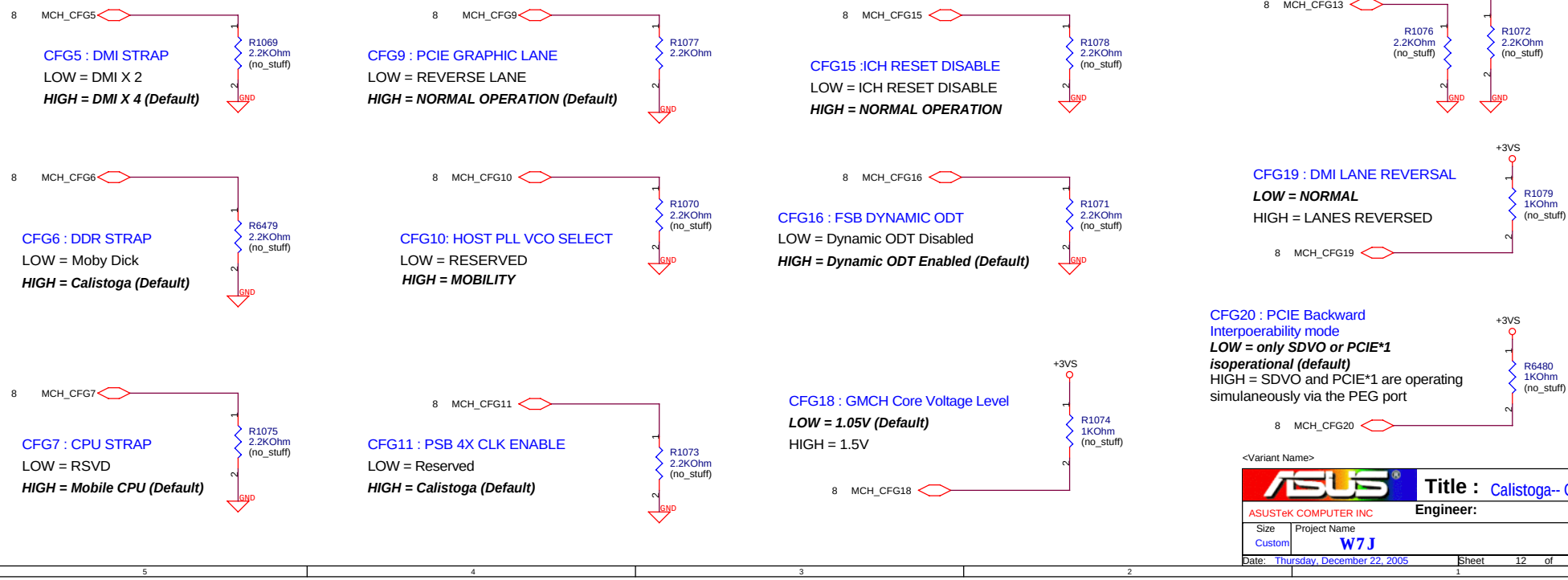
Title : Calistoga-- GND (5)

Engineer:

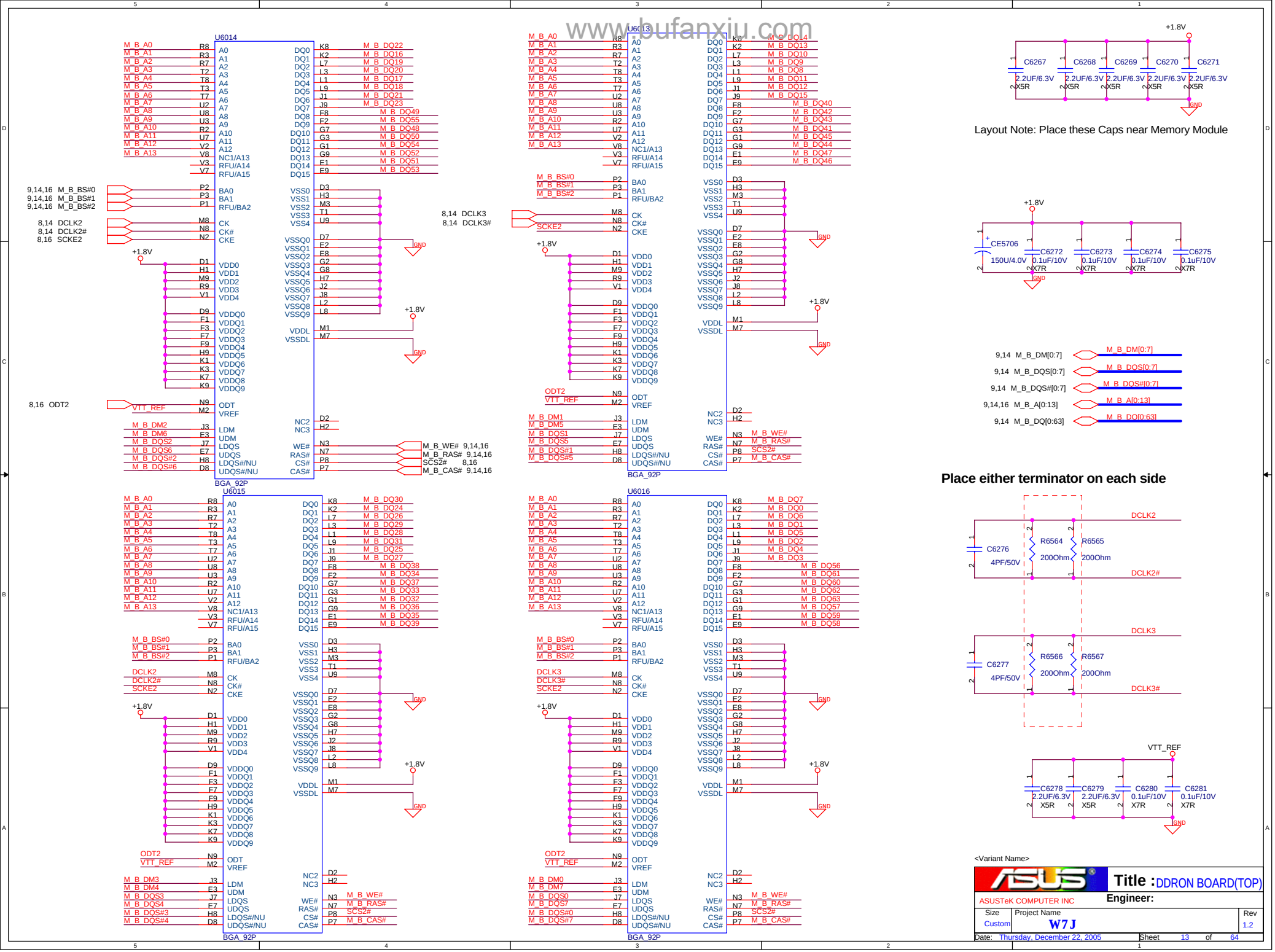
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 11 of 64





HIGH = LANES REVERSED



Layout Note: Place these Caps near Memory Module

Place either terminator on each side

<Variant Name>

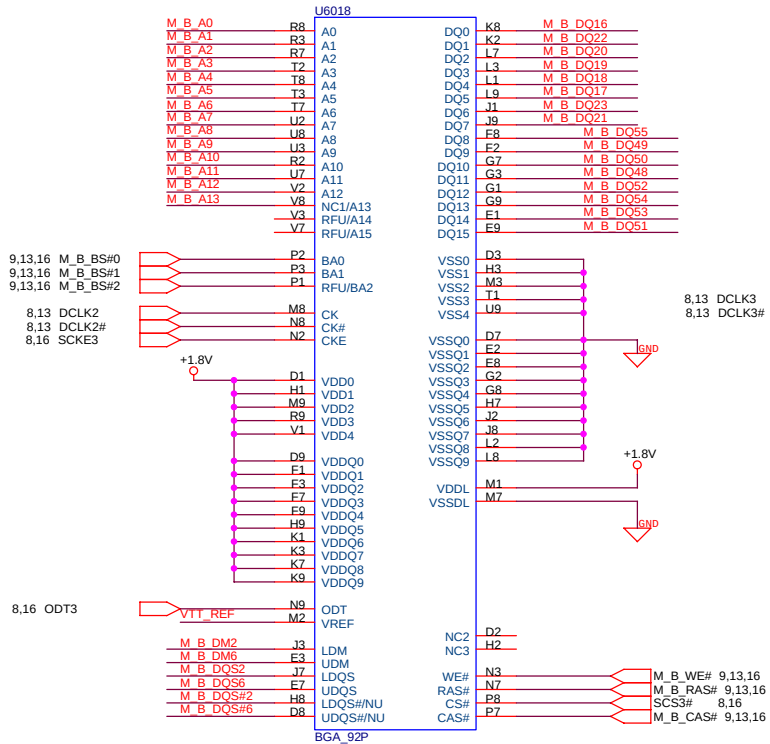
ASUSTeK COMPUTER INC

Title : DDRON BOARD(TOP)

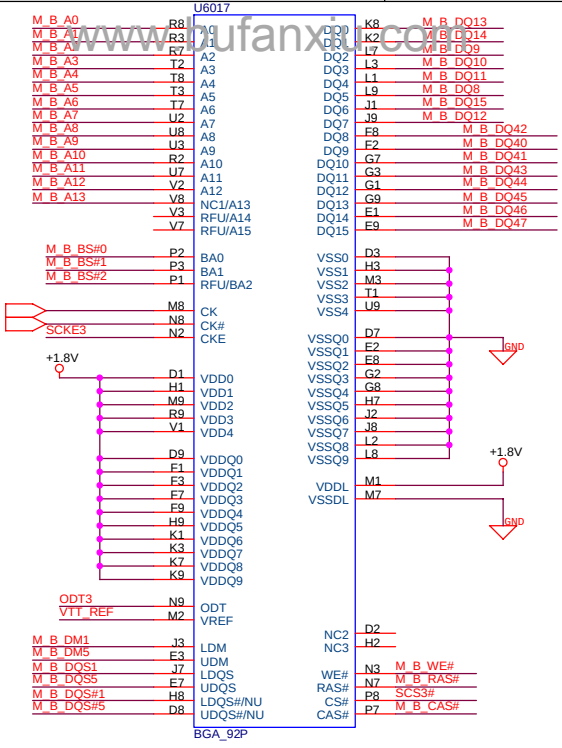
Engineer:

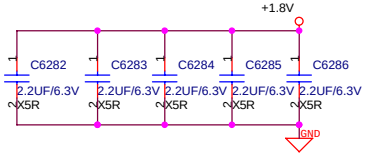
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 13 of 64

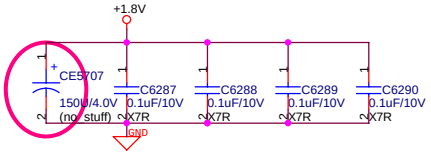


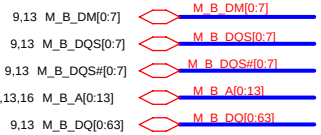
8,13 DCLK3
8,13 DCLK3#

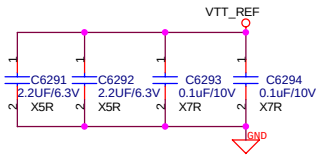


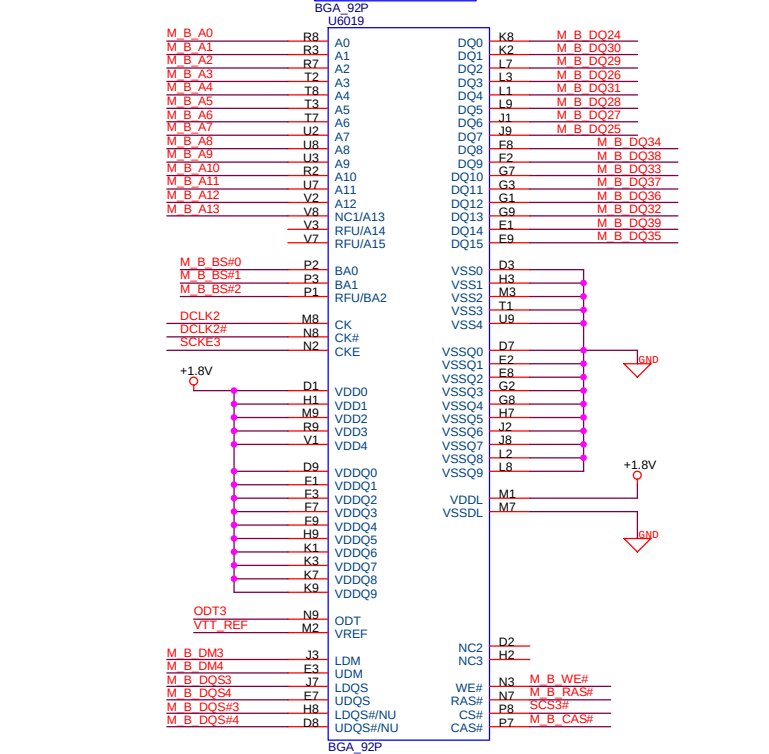


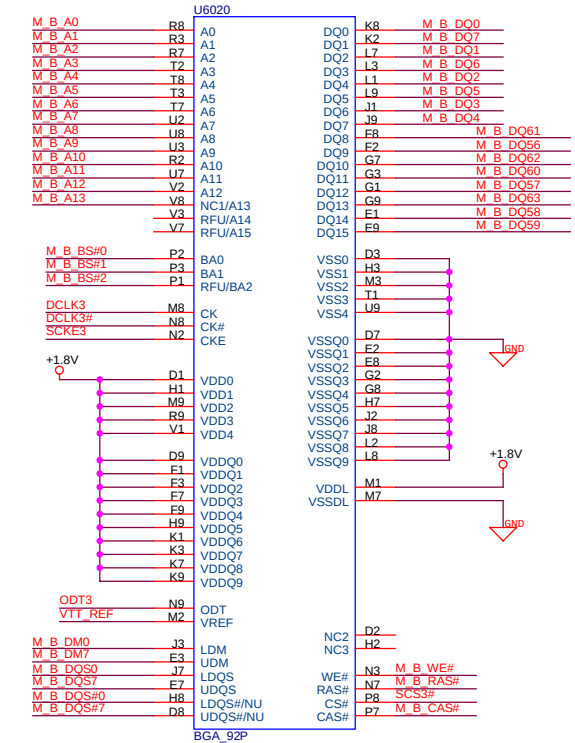
Layout Note: Place these Caps near Memory Module





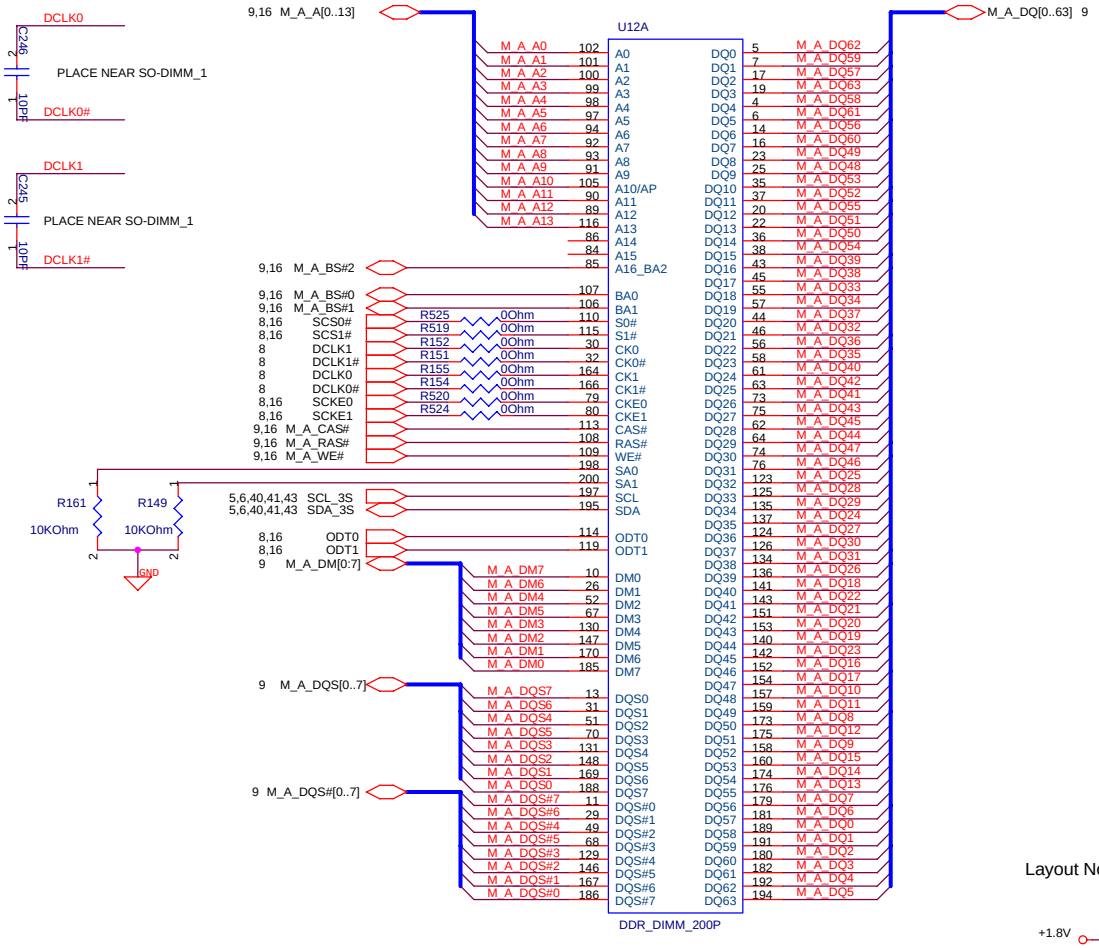




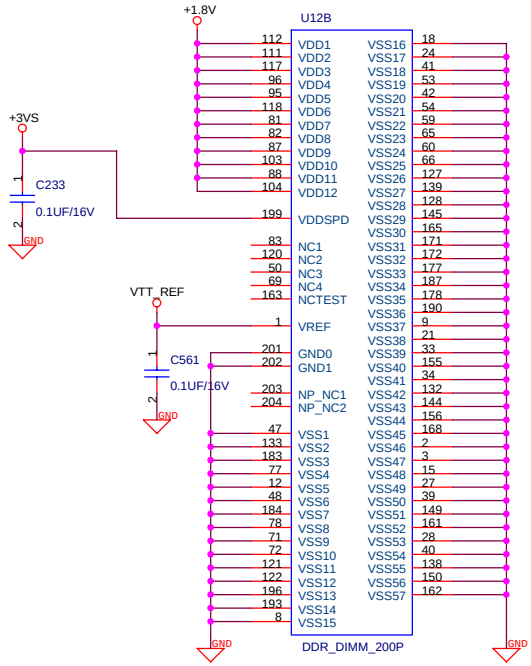


<Variant Name>

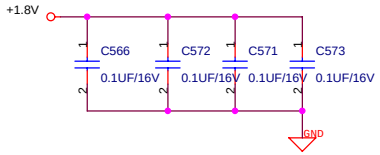
ASUSTeK COMPUTER INC	Title : DDR2 ON BOARD(BOT)	
	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 14 of 64	



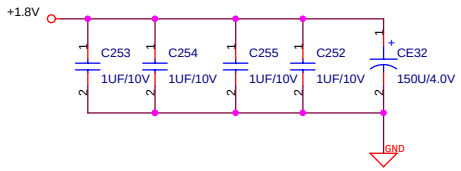
Top SO-DIMM:
12-025122005



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1



TOP SIDE:
Channel A

<Variant Name>

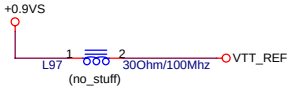
Title : DDR2 SO-DIMM

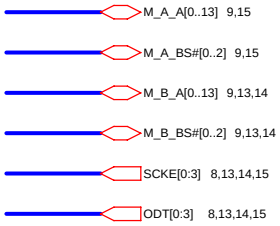
ASUSTeK COMPUTER INC

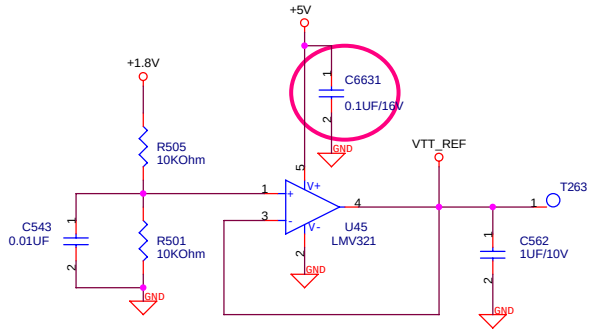
Engineer:

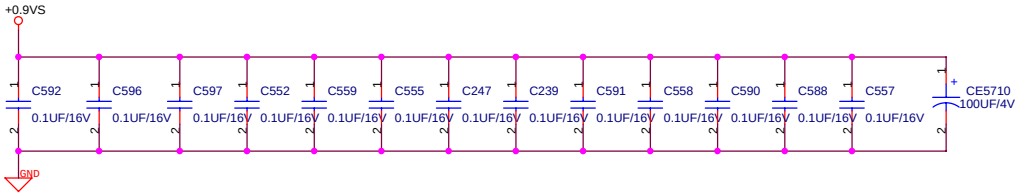
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 15 of 64

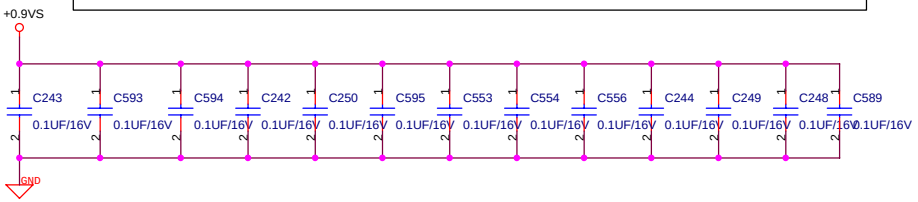


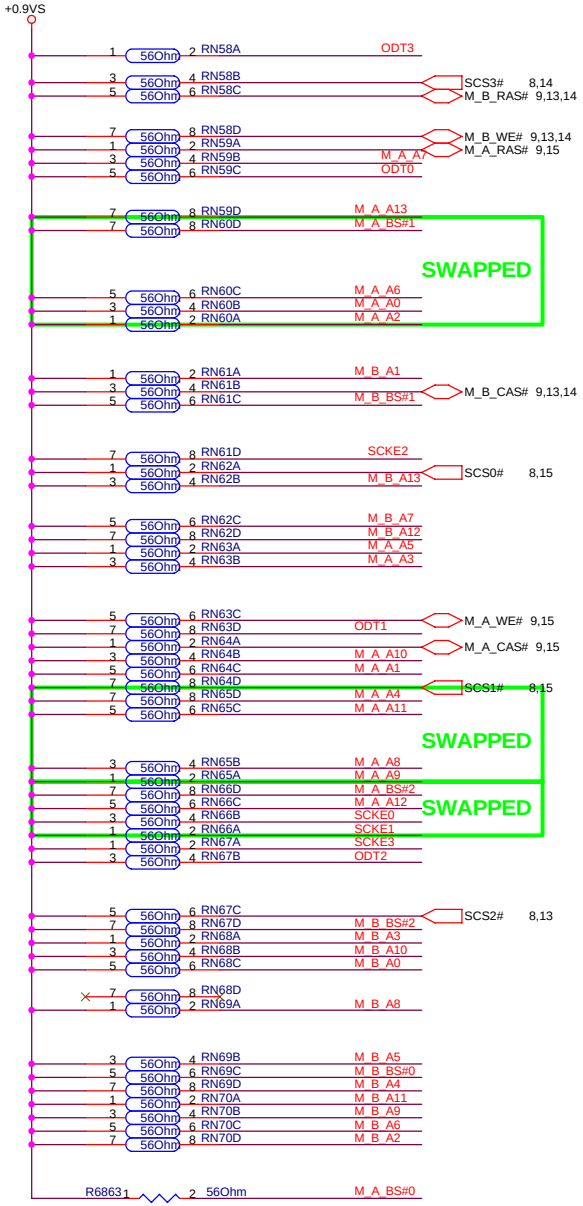






Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 16 of 64	

Escape use difference wire trace

PCIE LAN REVERSE

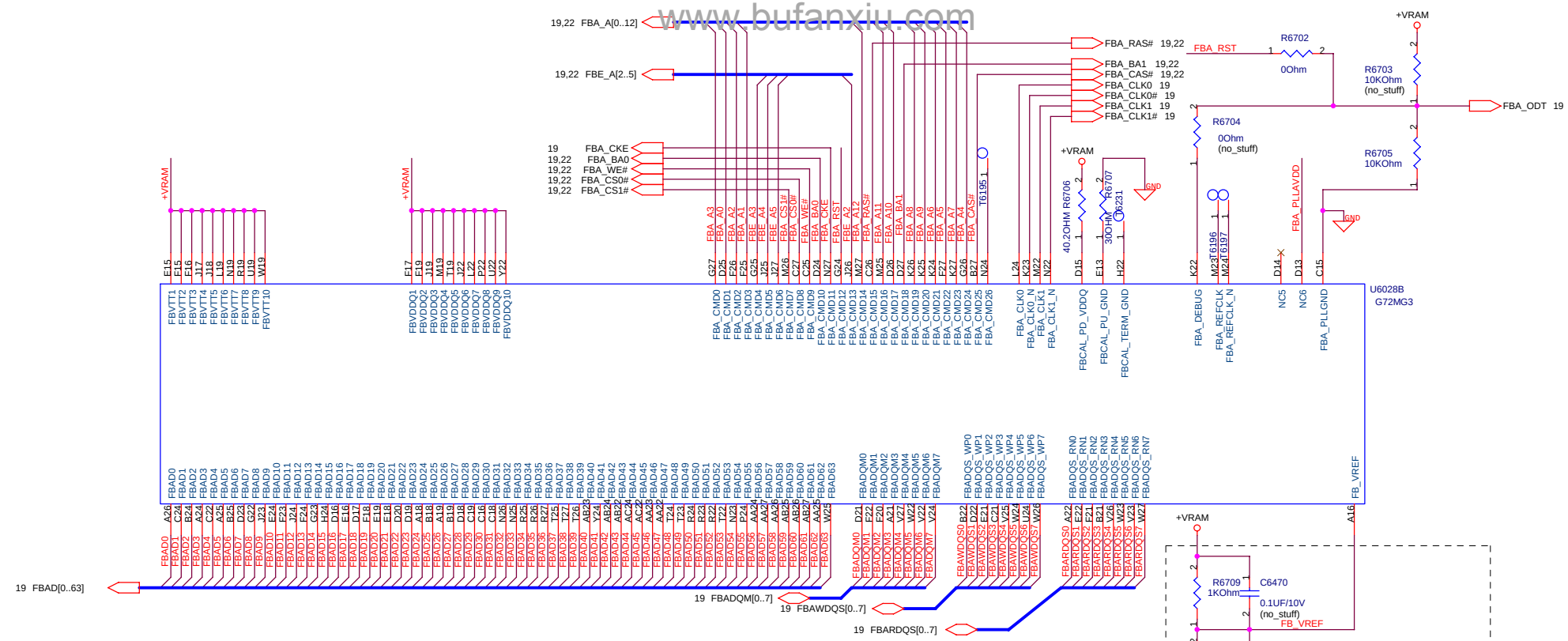
U6028A
G72MG3

PLACE NEAR BALLS
PLACE NEAR GPU

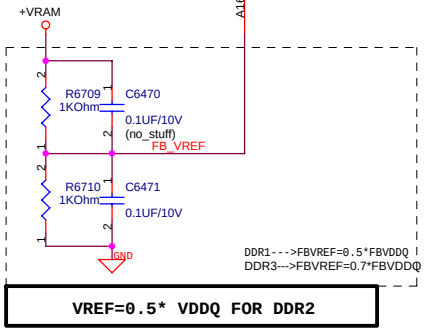
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS

<Variant Name>

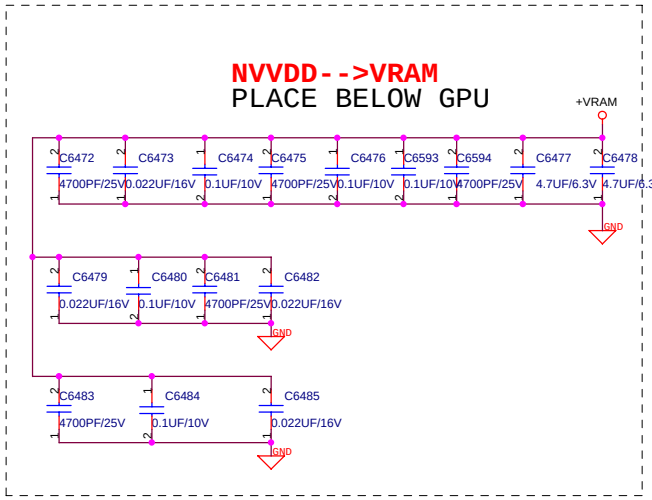
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005 SHEET 17 OF 64	DESCRIPTION: G72M64: PCIE
	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER :

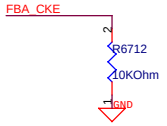


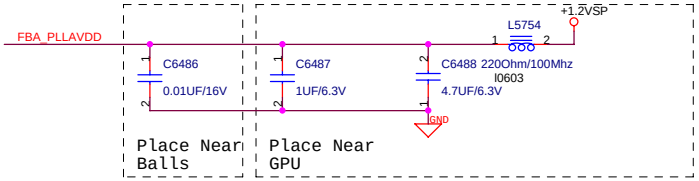
GDDR2 16x16 FBVDDQ 1.8V 84PIN



VREF=0.5* VDDQ FOR DDR2

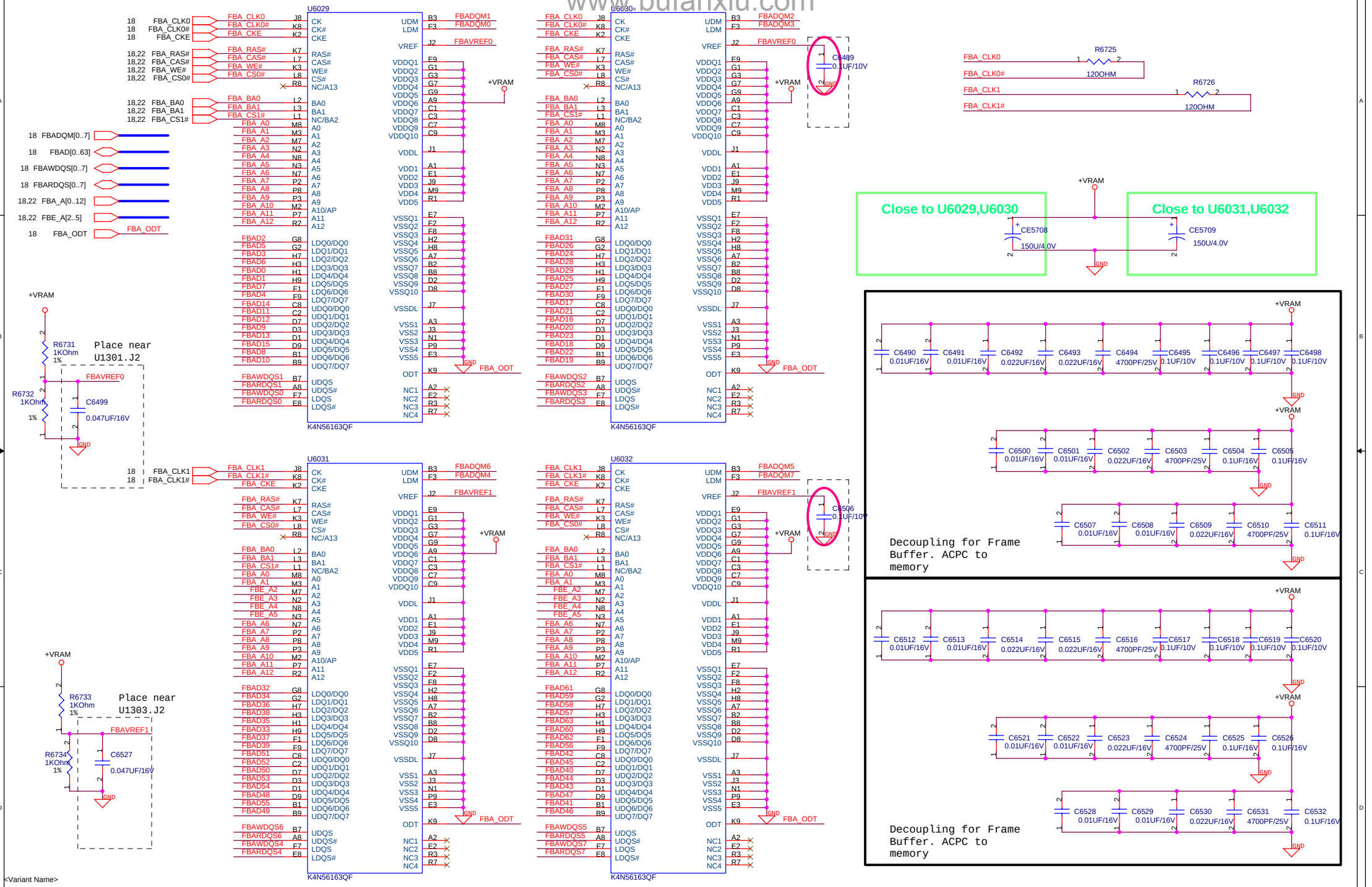






<Variant Name>

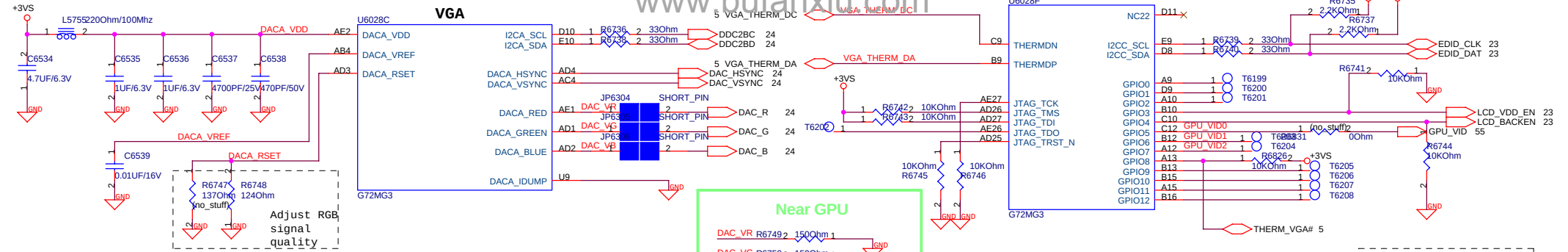
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: FB	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER :
		SHEET 18 OF 64			



<Variant Name>

PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: VRAM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 19 OF 64		RELEASE DATE :	

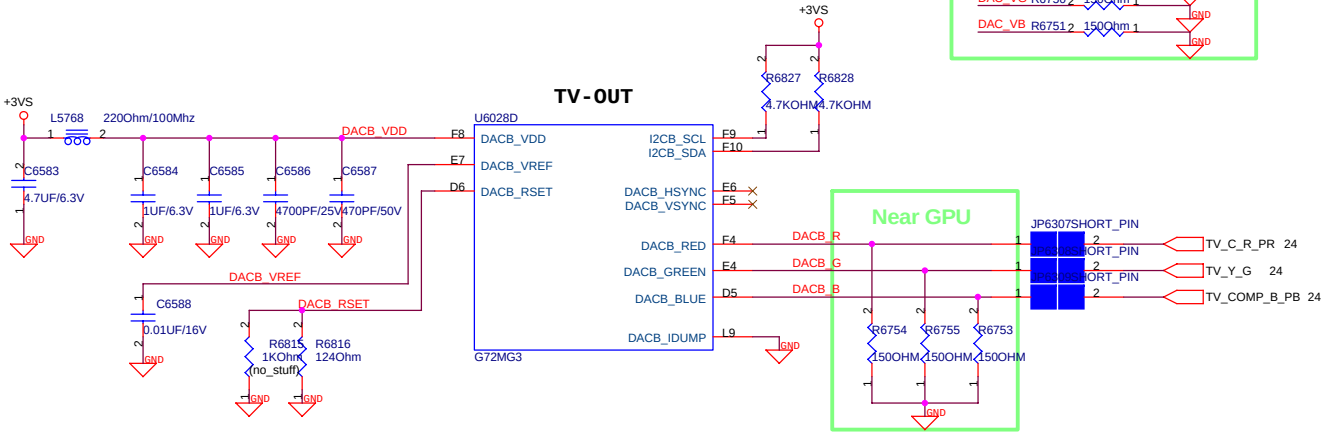
VGA



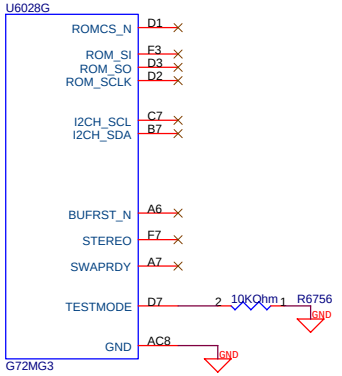
Near GPU

Internal Pull-down
GPIO 0,1,2,4,5,6,7

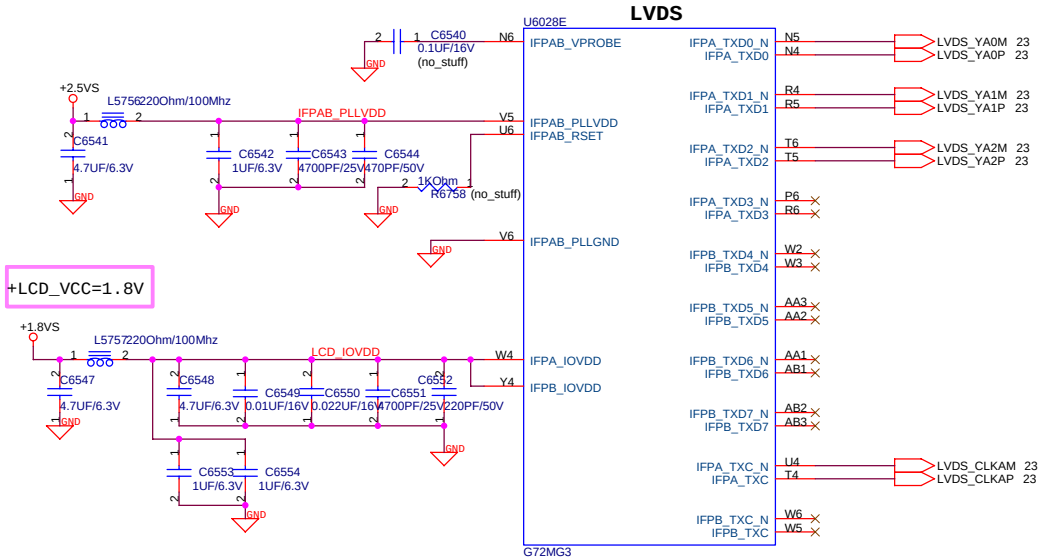
TV-OUT

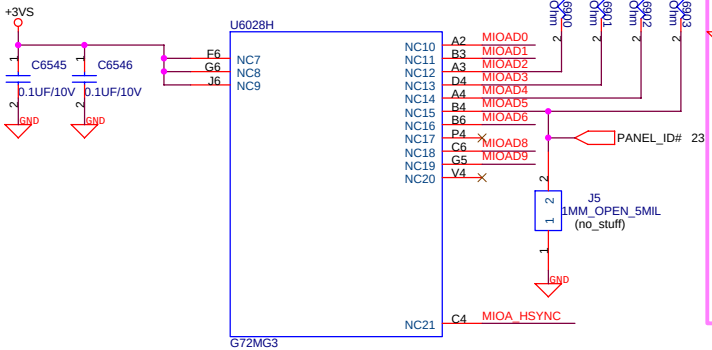


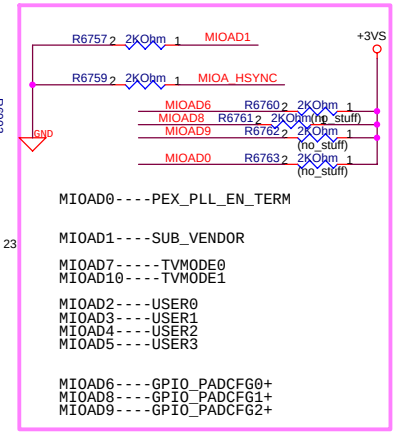
Near GPU



LVDS

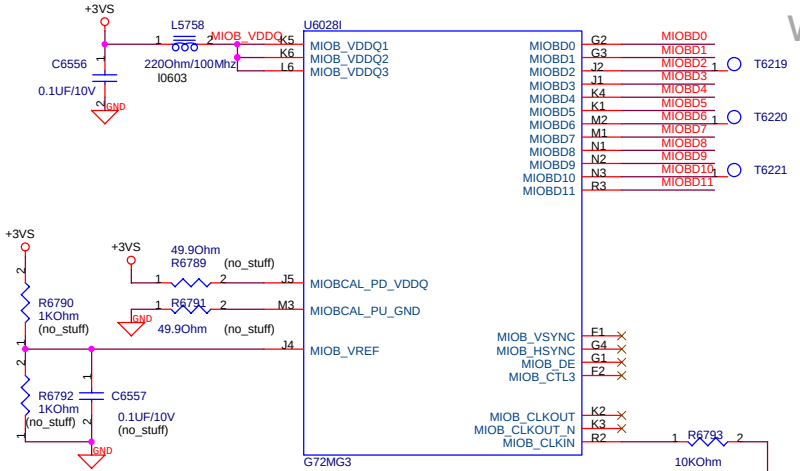


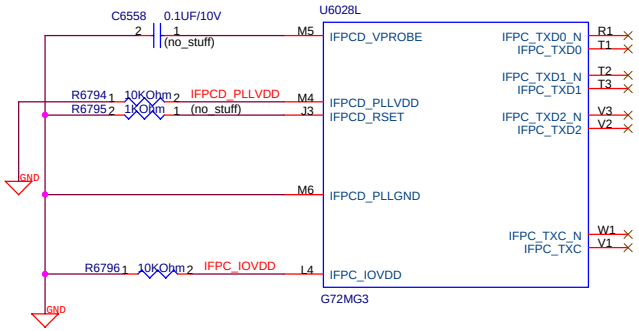


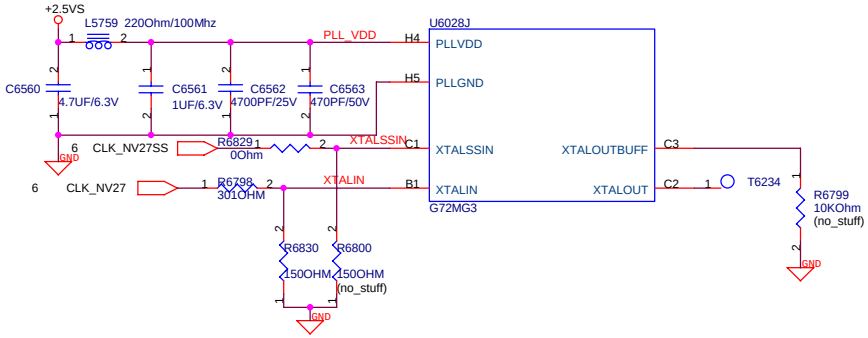


<Variant Name>

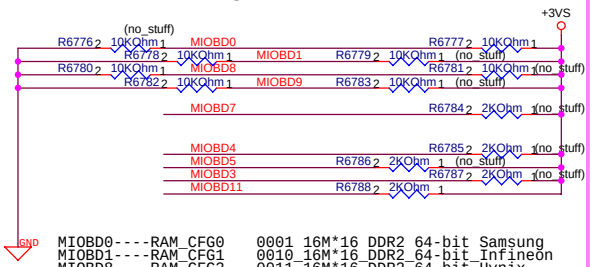
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: RGB/LCD/ROM/GPIO	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 20 OF 64		RELEASE DATE :	



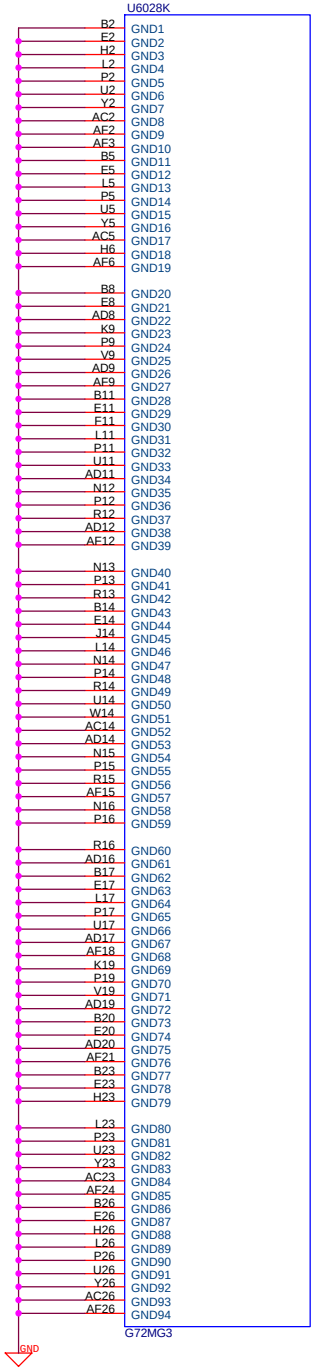




STRAP



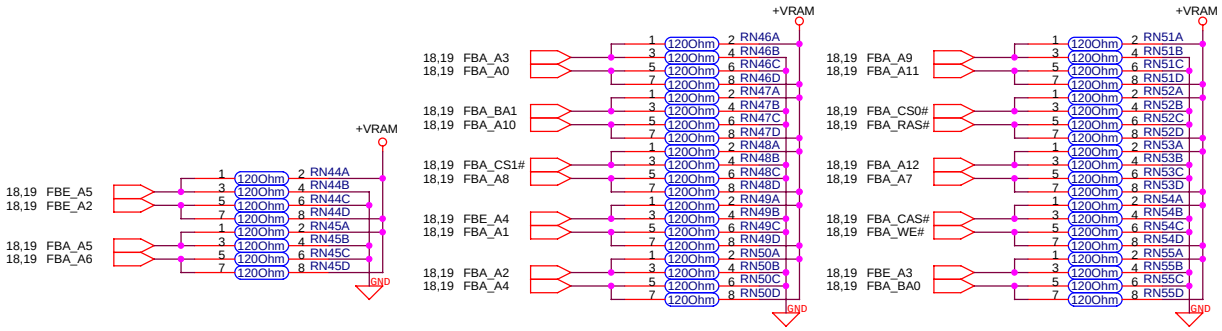

```
MIOBD0----RAM_CFG0    0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1    0010 16M*16 DDR2 64-bit Infineon
MIOBD8----RAM_CFG2    0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3
                      0101 32M*16 DDR2 64-bit Samsung
                      0110 32M*16 DDR2 64-bit Infineon
                      0111 32M*16 DDR2 64-bit Hynix


MIOBD9----RAM_CFG3    0 Full width of the frame buffer
                      1 Half width of the frame buffer


MIOBD2----CRYSTAL0    00,13.5MHZ
MIOBD6----CRYSTAL1    01,14.318MHZ
                      10,27MHZ(Default)
                      11,RESERVED

MIOBD4----PCI_DEVID0  0111 G72MV
MIOBD5----PCI_DEVID1  1000 G72M
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3


MIOBD10----ROMTYPE0   00,PARALLEL
MIOB_VSYNC-ROMTYPE1   01,SERIAL_AT25F
                      10,RESERVED
                      11,LPC

MIOBD7----MOBILE_MODE
```



<Variant Name>

PROJECT: **W7J**	REVISION **1.2**	DATE: **Thursday, December 22, 2005** SHEET **21** OF **64**	DESCRIPTION: ***G72M64: MIOB/CRYSTAL/TMDS***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**	DESIGN ENGINEER :

FBA CMD/ADDR Termination



<Variant Name>

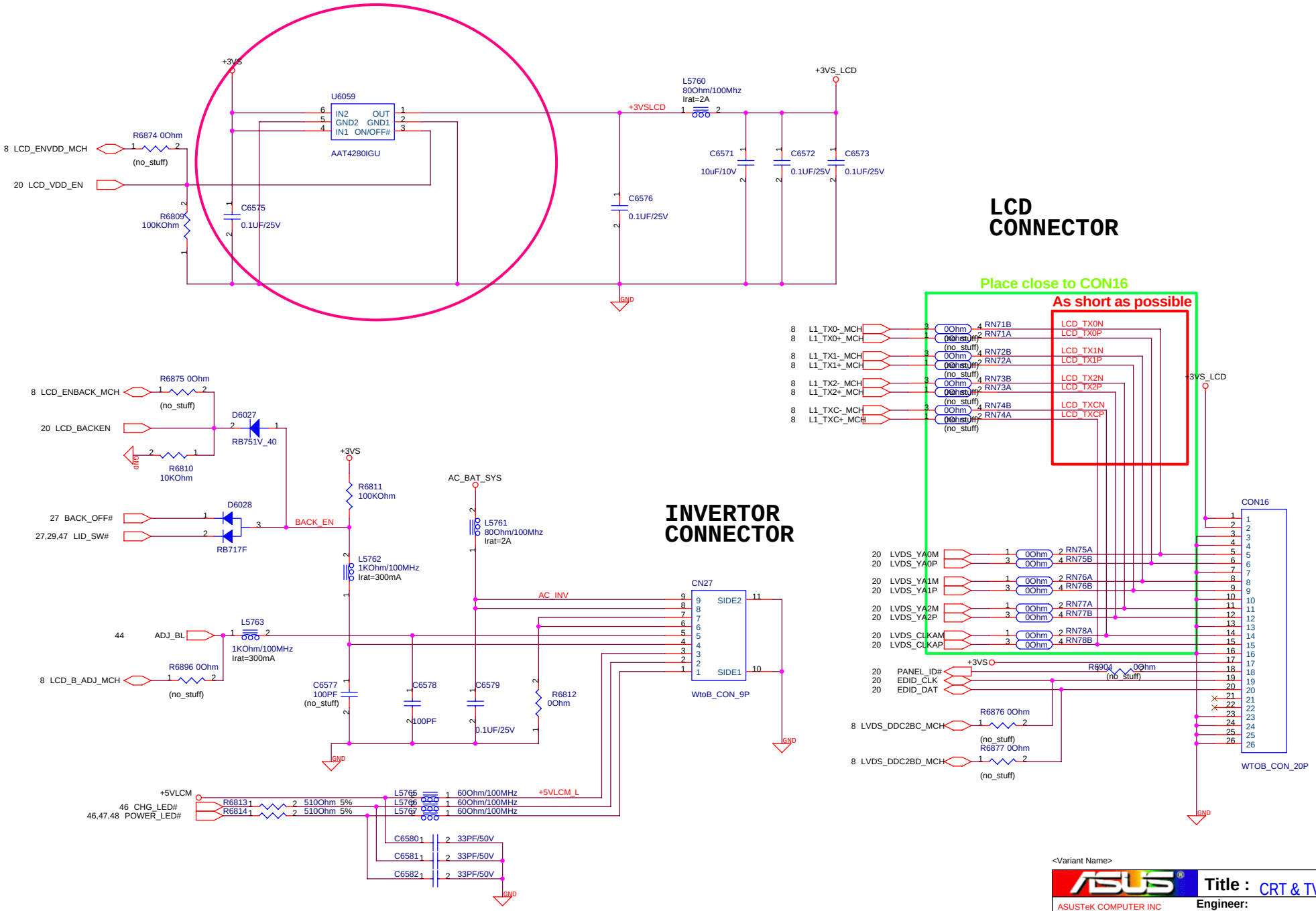
Title : G72M-Terminator

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 22 of 64



<Variant Name>

Title : CRT & TV-Out

ASUSTeK COMPUTER INC

Engineer:

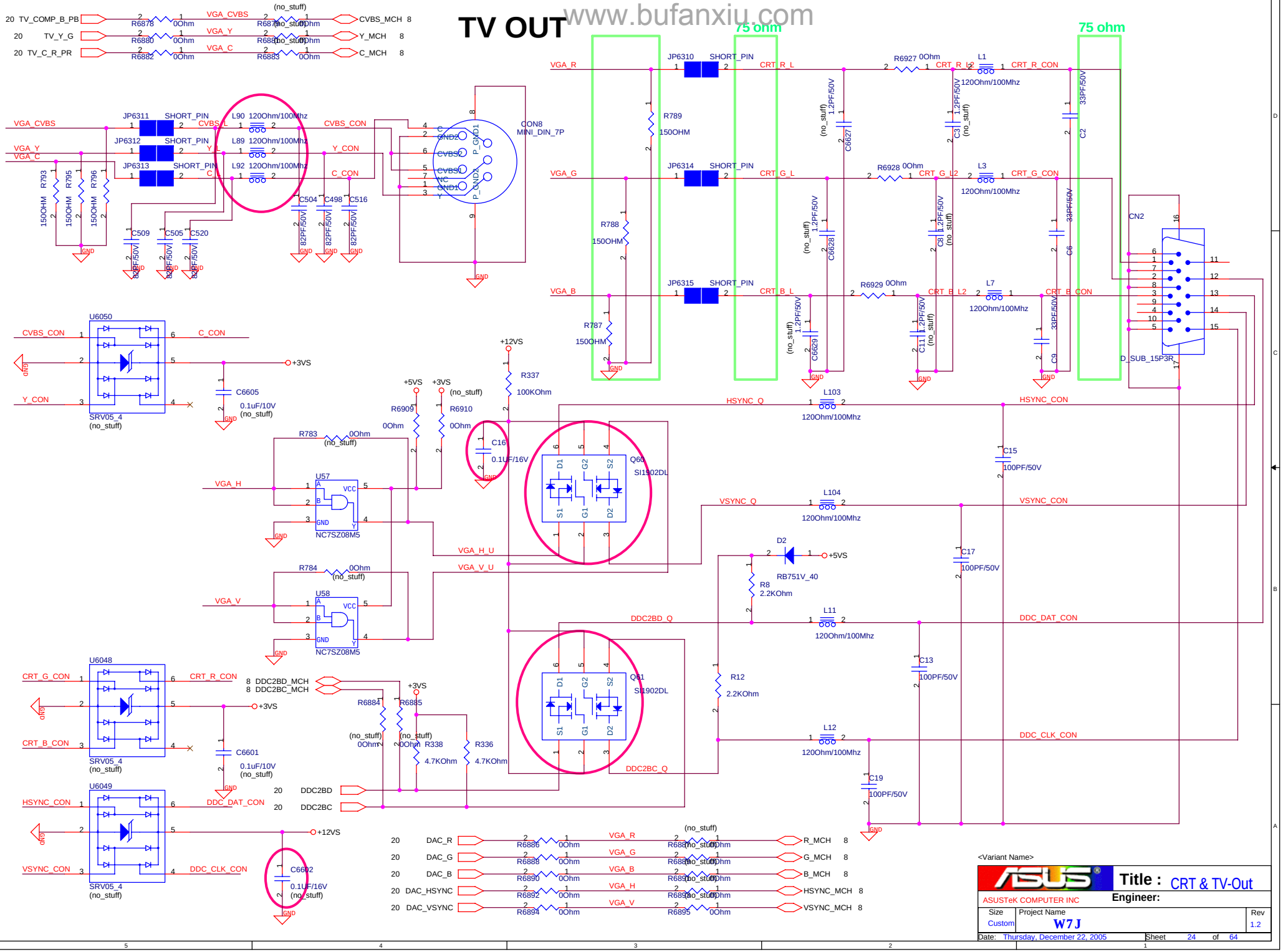
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 23 of 64

TV OUT

75 ohm

75 ohm



<Variant Name>

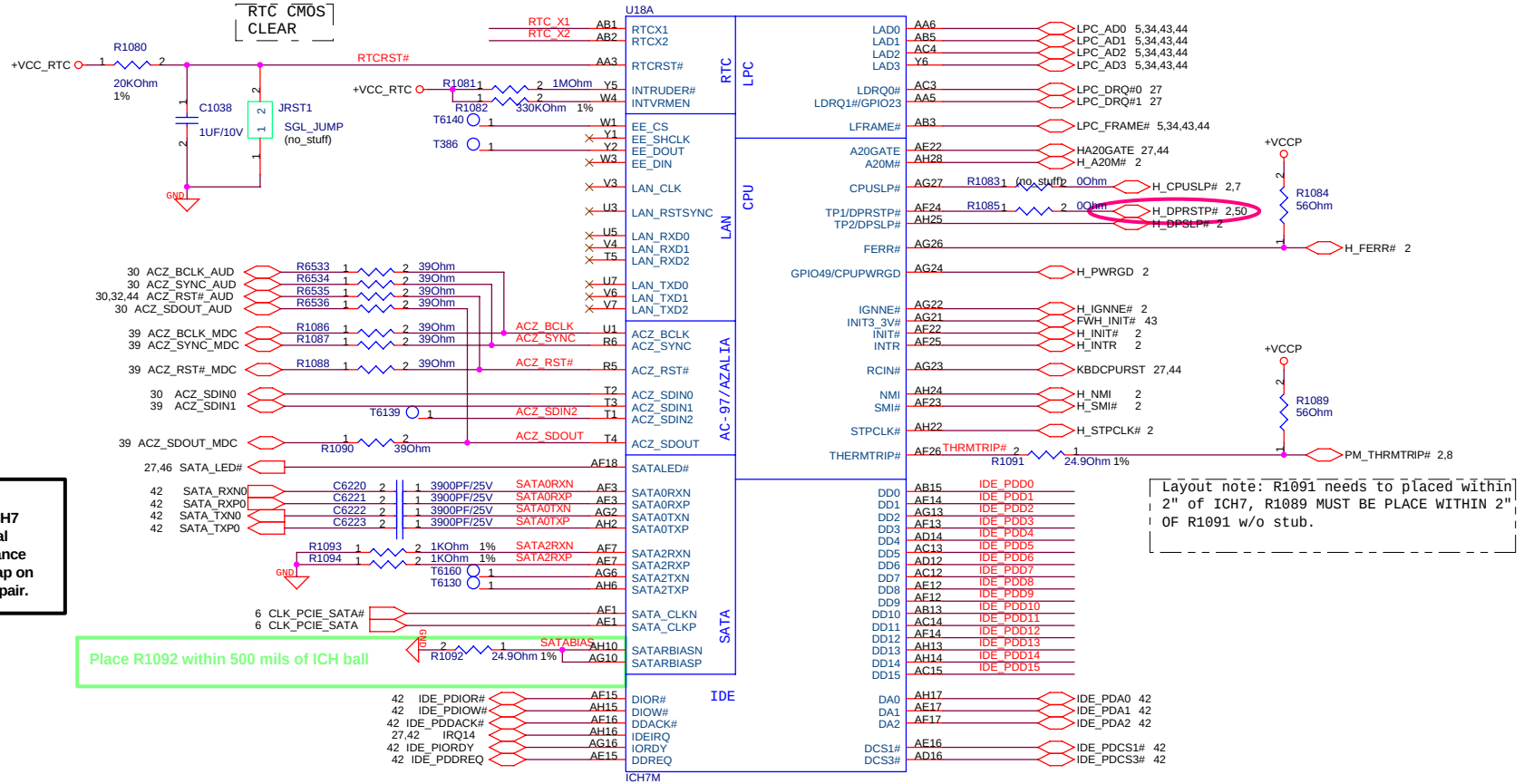
ASUSTeK COMPUTER INC

Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

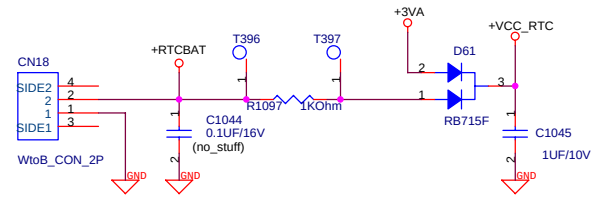
Date: Thursday, December 22, 2005 Sheet 24 of 64



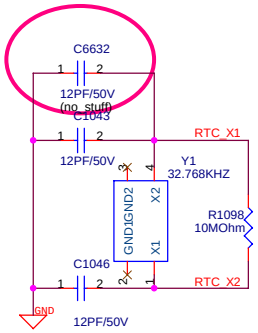
SATA:
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

RTC BAT



RTC Battery
P/N=07-016322032



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 25 of 64

36 PCI_AD[0..31] — PCI_AD[0..31]

ICH7 Boot BIOS select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

GNT#3 without PD, if NOT top-block swap(inter high)

U18B — ICH7M

PCI: PCI_AD0–PCI_AD31 (E18, C18, A16, F18, E16, A18, E17, A17, A15, C14, E14, D14, B12, C13, G15, G13, E12, C11, D11, A11, A10, F11, E10, E9, D9, B9, A8, A6, C7, B6, E6, D6)

PCI signals: REQ0# D7 → PCI_REQ#0 27,36; GNT0# E7 → PCI_GNT#0 36; REQ1# C16 → PCI_REQ#1 27 → T6133; GNT1# D16; REQ2# C17 → PCI_REQ#2 27 → T6170; GNT2# D17; REQ3# E13 → PCI_REQ#3 27 → R6403 1KOhm (no_stuff) → GND; GNT3# F13; REQ4#/GPIO22 A13 → PCI_REQ#4 27 → T6135; GNT4#/GPIO48 A14; GPIO1/REQ5# C8 → PCI_REQ#5 27 → T6136; GPIO17/GNT5# D8

C/BE0# B15 → PCI_C/BE#0 36; C/BE1# C12 → PCI_C/BE#1 36; C/BE2# D12 → PCI_C/BE#2 36; C/BE3# C15 → PCI_C/BE#3 36

IRDY# A7 → PCI_IRDY# 27,36; PAR E10 → PCI_PAR 36; PCIRST# B18 → PCI_RST#_ICH

DEVSEL# A12 → PCI_DEVSEL# 27,36; PERR# C9 → PCI_PERR# 27,36; PLOCK# E11 → PCI_LOCK# 27; SERR# B10 → PCI_SERR# 27,36; STOP# F15 → PCI_STOP# 27,36; TRDY# F14 → PCI_TRDY# 27,36; FRAME# F16 → PCI_FRAME# 27,36

PLTRST# C26 → PLT_RST#_SB; PCICLK A9 → CLK_ICHPCI 6; PME# B19

+3VSUS → R6568 10KOhm

Interrupt I/F: PIRQA# A3 ← 27 PCI_INTA#; PIRQB# B4 ← 27 PCI_INTB#; PIRQC# C5 ← 27 PCI_INTC#; PIRQD# B5 ← 27 PCI_INTD#

GPIO2/PIRQE# G8 → PCI_INTE# 27,36; GPIO3/PIRQF# F7 → PCI_INTF# 27,36; GPIO4/PIRQG# F8 → PCI_INTG# 27; GPIO5/PIRQH# G7 → PCI_INTH# 27

MISC: RSVD_1 AE5 ← T400; RSVD_2 AD5 ← T403; RSVD_3 AG4 ← T406; RSVD_4 AH4 ← T409; RSVD_5 AD9 ← T411

RSVD_6 AE9 → T401; RSVD_7 AG8 → T404; RSVD_8 AH8 → T407; RSVD_9 F21 → T410; MCH_SYNC# AH20 → MCH_SYNC# 8

pull up to +3VS by internal pull-up resistor

U18D — ICH7M

PCI-Express / Direct Media Interface:

PERn1 F26 ← PCIE_RXN1 40; PERp1 F25 ← PCIE_RXP1 40; PETn1 E28 → C1047 0.1UF/10V → PCIE_TXN1 40; PETp1 E27 → C1048 0.1UF/10V → PCIE_TXP1 40

PERn2 H26 ← PCIE_RXN2 38; PERp2 H25 ← PCIE_RXP2 38; PETn2 G28 → C1049 0.1UF/10V → PCIE_TXN2 38; PETp2 G27 → C1050 0.1UF/10V → PCIE_TXP2 38

PERn3 K26 ← PCIE_RXN3 41; PERp3 K25 ← PCIE_RXP3 41; PETn3 J28 → C1051 0.1UF/10V → PCIE_TXN3 41; PETp3 J27 → C1052 0.1UF/10V → PCIE_TXP3 41

PERn4 M26; PERp4 M25; PETn4 L28; PETp4 L27

PERn5 P26; PERp5 P25; PETn5 N28; PETp5 N27

PERn6 T25; PERp6 T24; PETn6 R28; PETp6 R27

DMI0RXN V26 ← DMI_RXN0 8; DMI0RXP V25 ← DMI_RXP0 8; DMI0TXN U28 → DMI_TXN0 8; DMI0TXP U27 → DMI_TXP0 8

DMI1RXN Y26 ← DMI_RXN1 8; DMI1RXP Y25 ← DMI_RXP1 8; DMI1TXN W28 → DMI_TXN1 8; DMI1TXP W27 → DMI_TXP1 8

DMI2RXN AB26 ← DMI_RXN2 8; DMI2RXP AB25 ← DMI_RXP2 8; DMI2TXN AA28 → DMI_TXN2 8; DMI2TXP AA27 → DMI_TXP2 8

DMI3RXN AD25 ← DMI_RXN3 8; DMI3RXP AD24 ← DMI_RXP3 8; DMI3TXN AC28 → DMI_TXN3 8; DMI3TXP AC27 → DMI_TXP3 8

DMI_CLKN AE28 ← CLK_PCIE_ICH# 6; DMI_CLKP AE27 ← CLK_PCIE_ICH 6

DMI_ZCOMP C25; DMI_IRCOMP D25 → DMICOMP → R1099 24.9Ohm 1% → +1.5VS

Place within 500 mils of ICH

SPI / USB:

SPI_CLK R2; SPI_CS# P6; SPI_ARB P1; SPI_MOSI P5; SPI_MISO P2

+3V → RN18A 10KOhm (no_stuff) R2; RN18B 10KOhm (no_stuff) P6; RN18C 10KOhm (no_stuff) P5; RN18D 10KOhm (no_stuff) P2

USBP0N F1 → USB_PN0 40; USBP0P F2 → USB_PP0 40; USBP1N G4 → USB_PN1 45; USBP1P G3 → USB_PP1 45; USBP2N H1 → USB_PN2 47; USBP2P H2 → USB_PP2 47; USBP3N J4 → USB_PN3 45; USBP3P J3 → USB_PP3 45; USBP4N K1 → USB_PN4 45; USBP4P K2 → USB_PP4 45; USBP5N L4 → USB_PN5 45; USBP5P L5 → USB_PP5 45; USBP6N M1; USBP6P M2; USBP7N N4 → T405; USBP7P N3 → T408

USBRBIAS# D2; USBRBIAS D1 → USBBIAS → R1100 22.6Ohm 1% → GND

Place within 500 mils of ICH

OC0# D3 ← USB_OC#0; OC1# C4; OC2# D5 ← USB_OC#2 27; OC3# D4 ← USB_OC#3 27,45; OC4# E5 ← USB_OC#4 27,45; OC5#/GPIO29 C3 ← USB_OC#5 27; OC6#/GPIO30 A2 ← USB_OC#6 27; OC7#/GPIO31 B3 ← USB_OC#7 27

U68D 74HC08: BUF_PLT_RST# 8,27,34,38,41,42,43,44 → 11; 12 → PLT_RST#_SB; +3V; C1056 0.01UF (no_stuff) → GND

U68C 74HC08: PLT_RST# 17 → R6408 0Ohm (no_stuff) → 8; 9 → R1104 0Ohm (no_stuff) → SW_RST# 27; 10 → PLT_RST#_SB; R1106 0Ohm

+3V → R1102 10KOhm; C1054 0.1UF/16V → GND

U68A 74HC08: PCI_RST# 36,40,42 → 3; 1 → PCI_RST#_ICH; +3V; C1053 0.1UF/16V → GND

U69 74LVC1G32GV: SET_PCIRSTNS# 44 → R1108 10KOhm; PCI_RST# → R1109 47KOhm; C1057 0.01UF → GND; +3V; C1055 0.1UF/16V → GND; → PCI_RSTNS# 36,44

Can be issue SCI or SMI List: GPIO0~GPIO15
Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28

Only GPI Pin: GPI0~8,11~15,26,29,30,31,40(5V),41
Only GPO Pin: GPIO16~17,19,21,23,48
Can be GPIO: GPIO24,25,27,28,33,34
Resume Power Input Pin List:
BATLOW#,AC_SDIN[0:1],LAN_RST#,
OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#

<Variant Name>

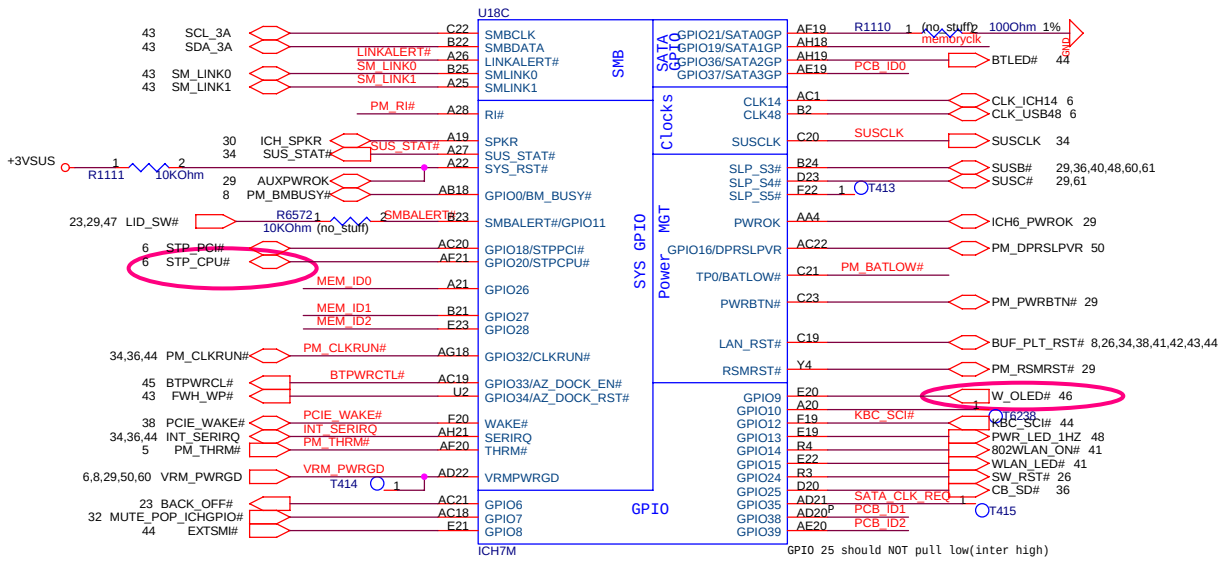
Title : ICH7-M (2)

ASUSTeK COMPUTER INC Engineer:

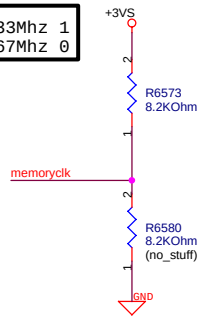
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 26 of 64

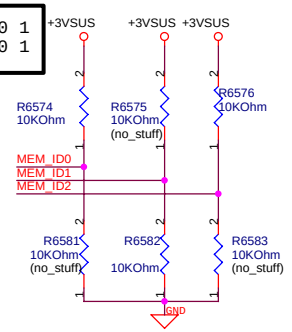
The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

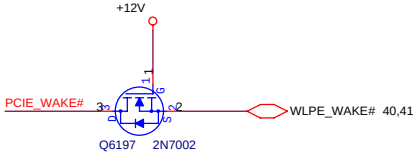


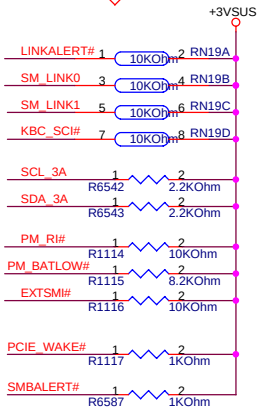
533Mhz 1
667Mhz 0

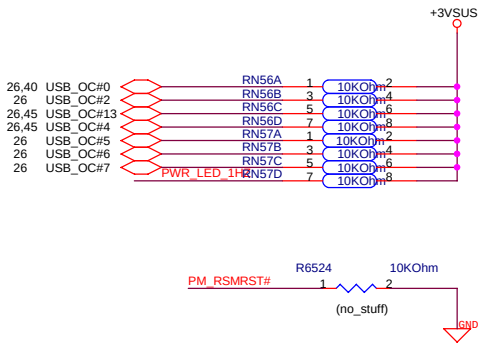


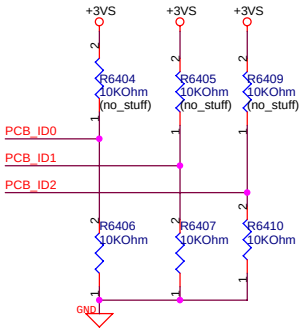
512M 1 0 1
256M 0 0 1

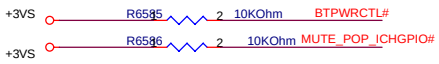


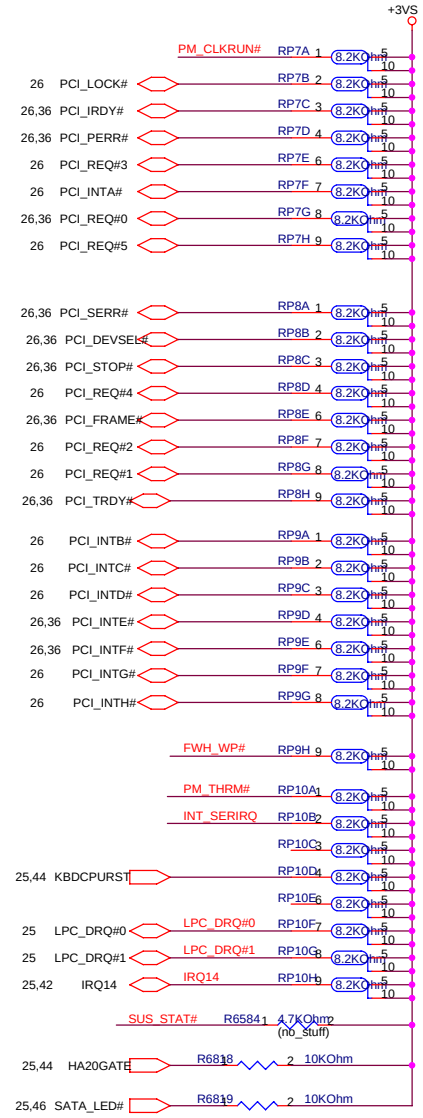












<Variant Name>

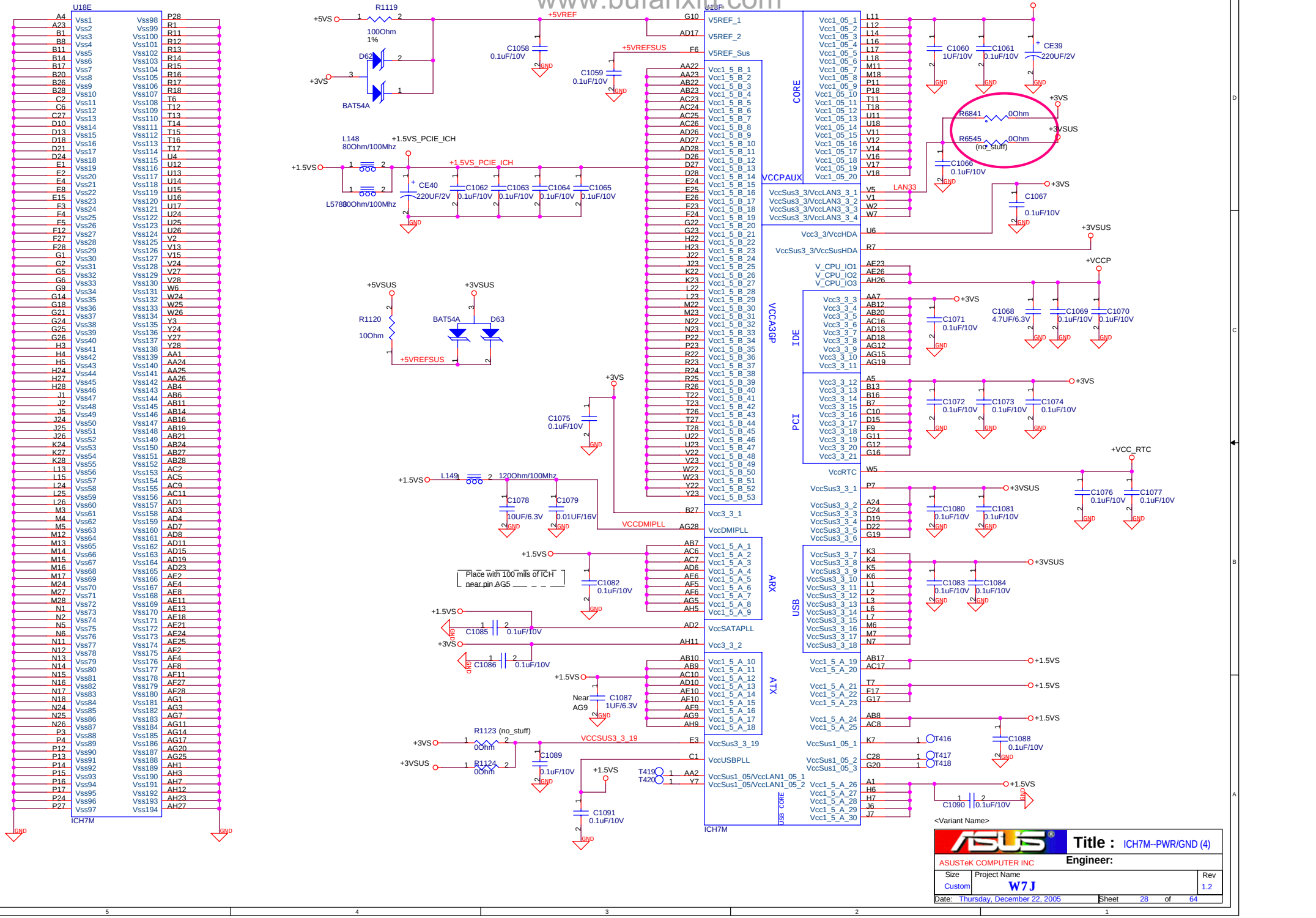
ASUSTeK COMPUTER INC

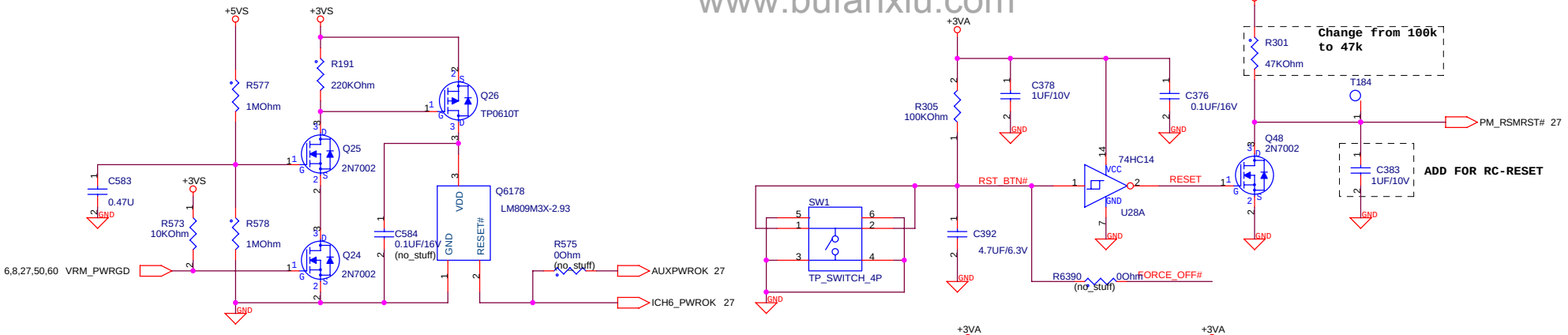
Title : ICH7M--(3)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

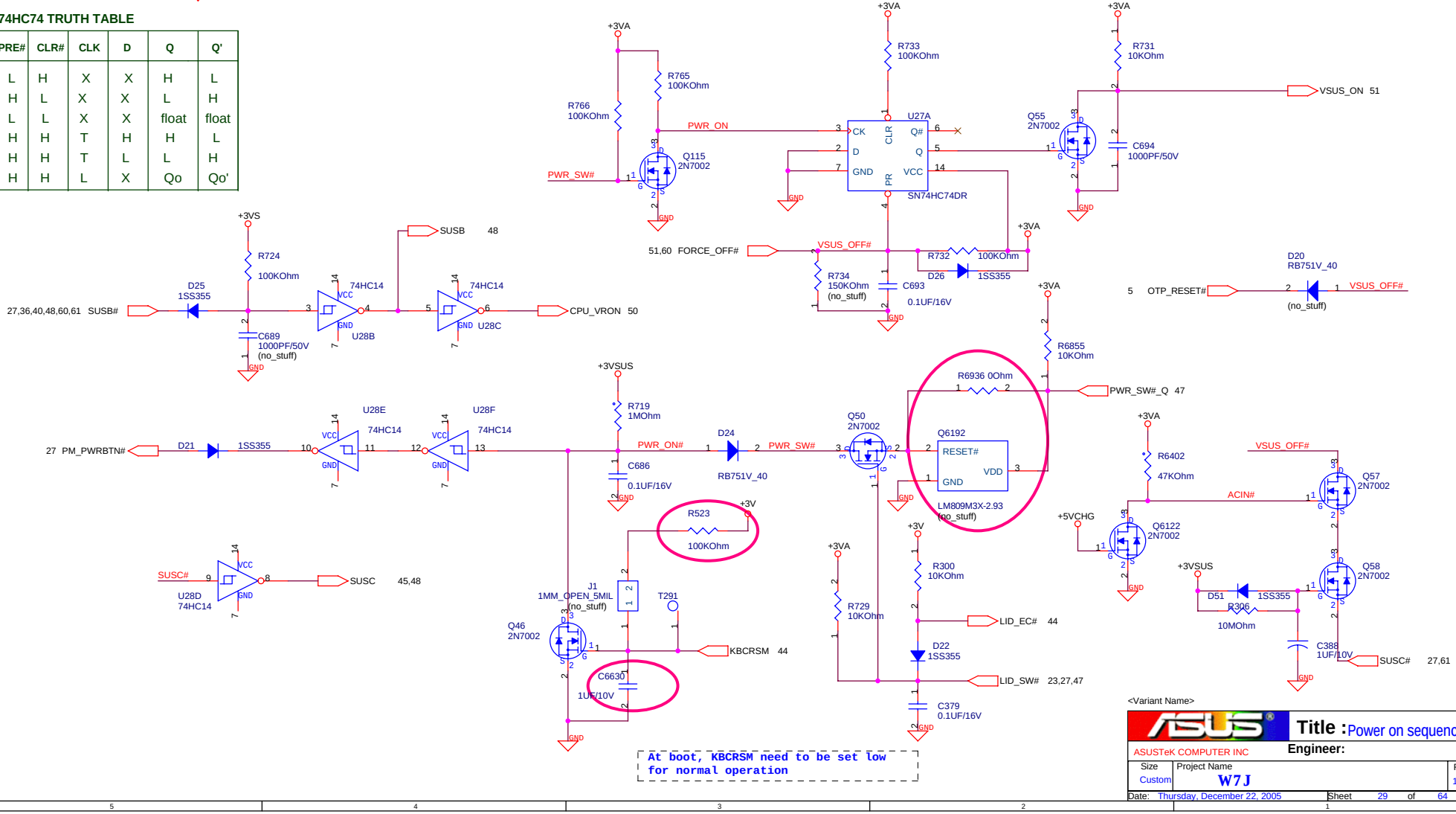
Date: Thursday, December 22, 2005 Sheet 27 of 64





74HC74 TRUTH TABLE

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'



At boot, KBCRSM need to be set low for normal operation

<Variant Name>

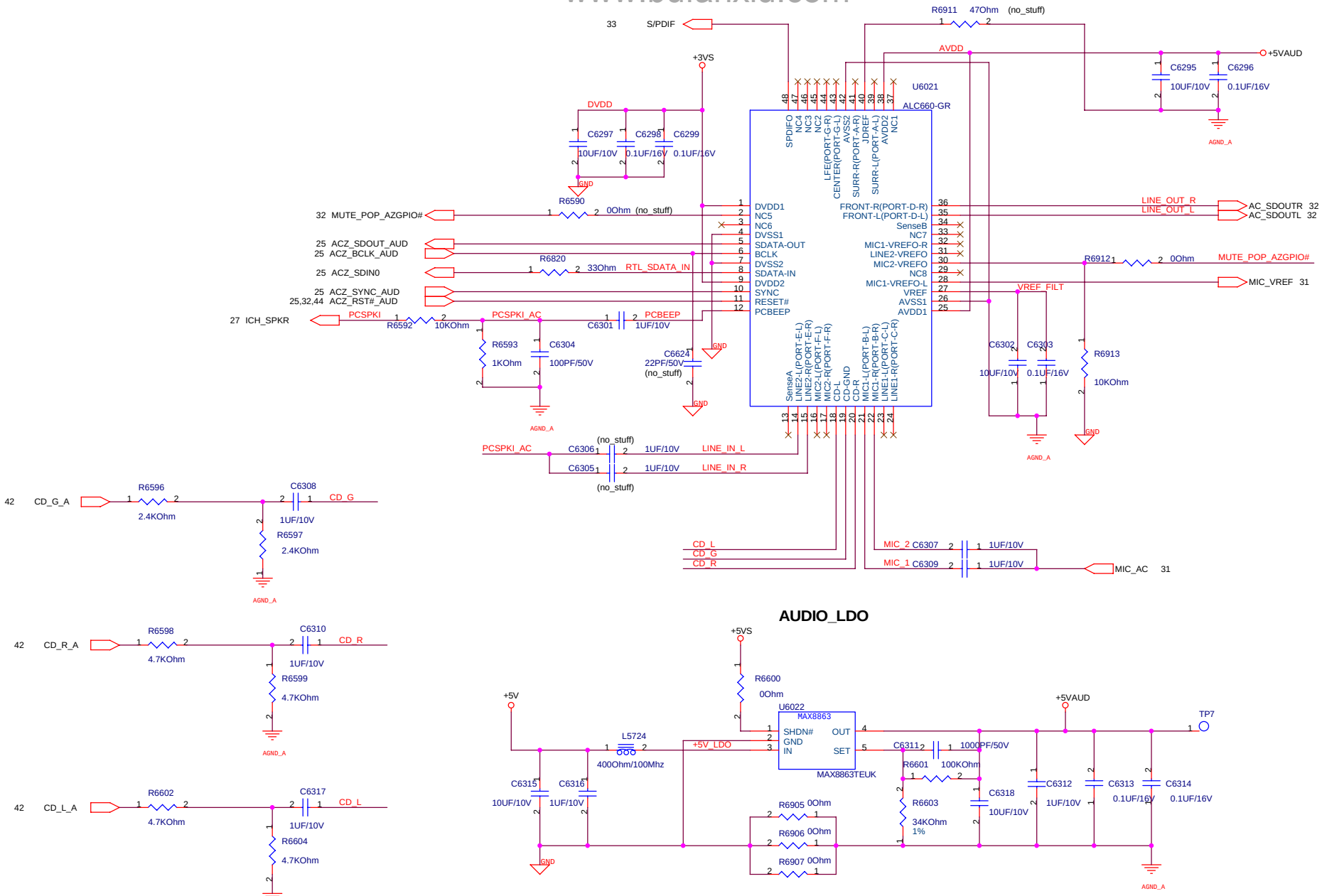
ASUSTeK COMPUTER INC

Title : Power on sequence

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

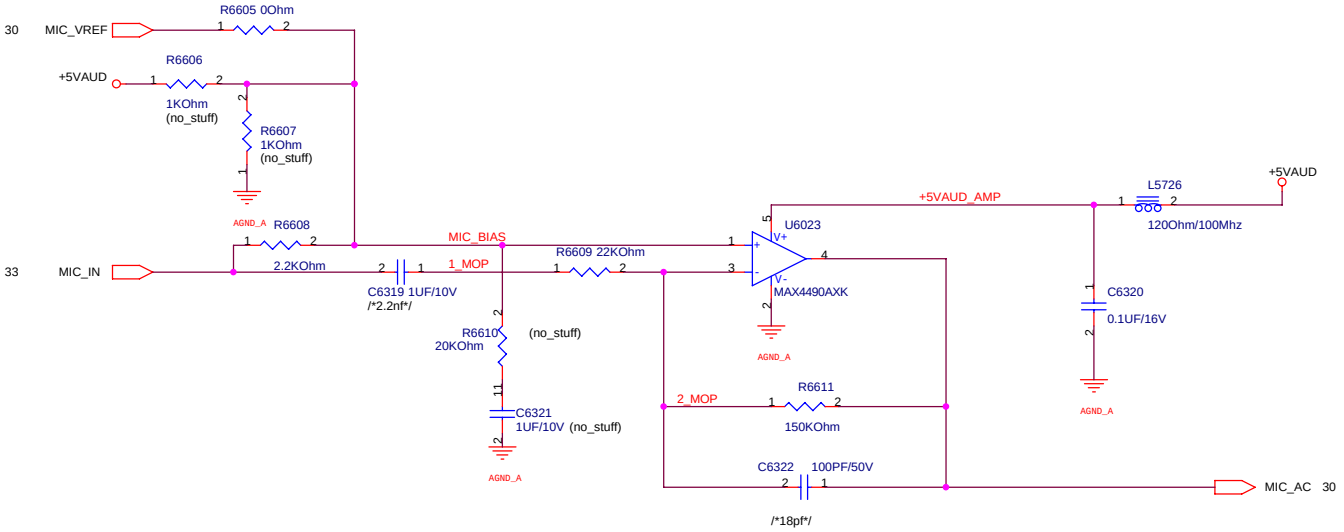
Date: Thursday, December 22, 2005 Sheet 29 of 64

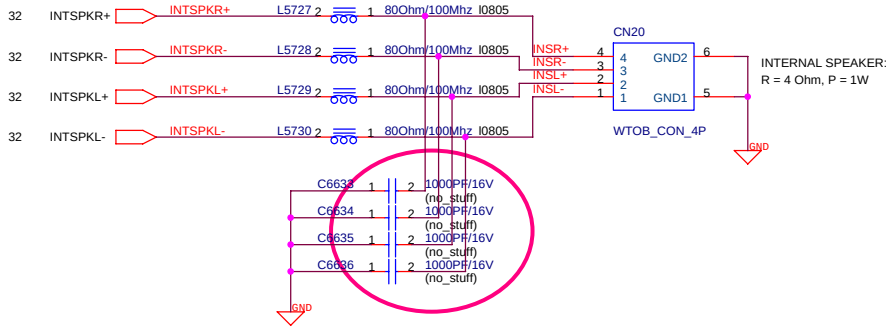


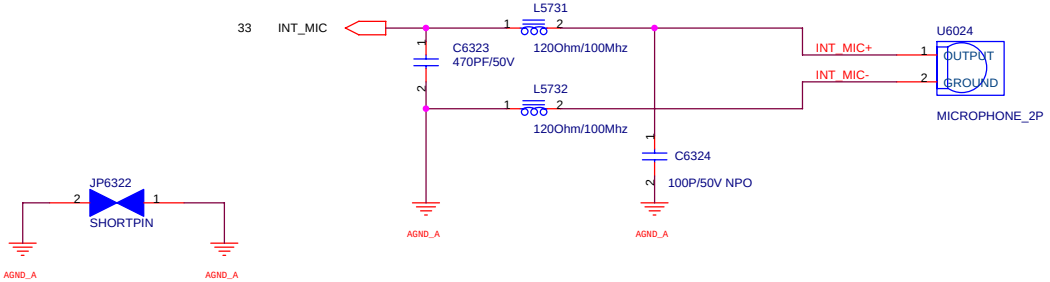
<Variant Name>

ASUSTeK COMPUTER INC	Title : AZALIA_ALC660	
	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 30 of 64	

MIC PreAmp & Mic Jack







<Variant Name>

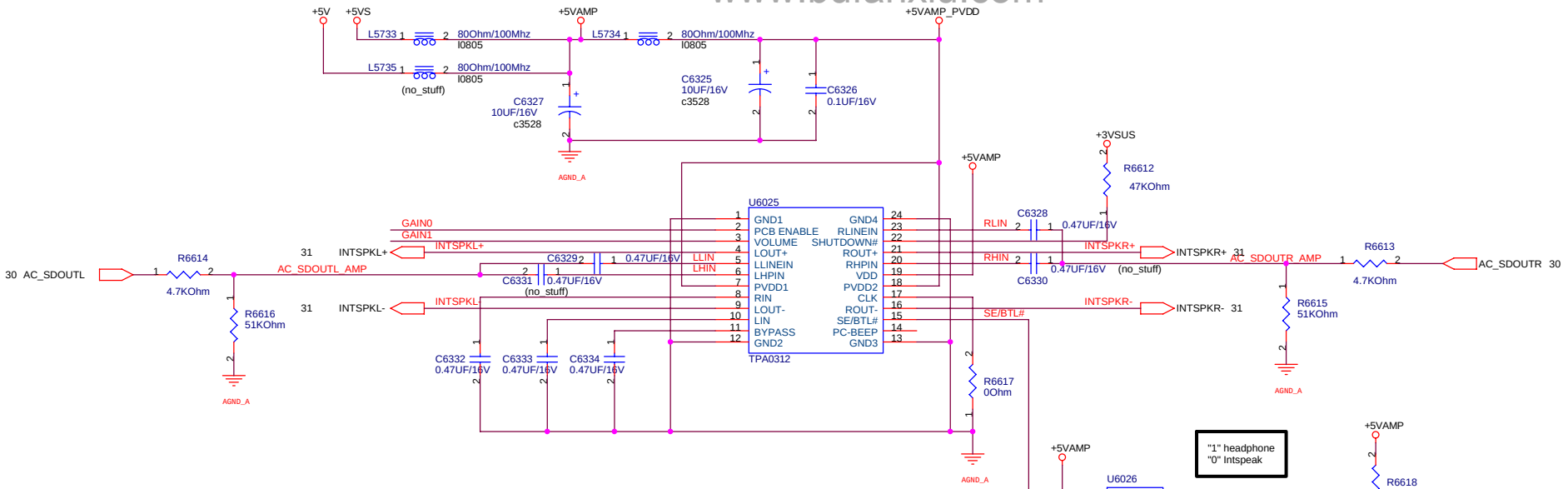
Title : MIC PREAMP & INT MIC

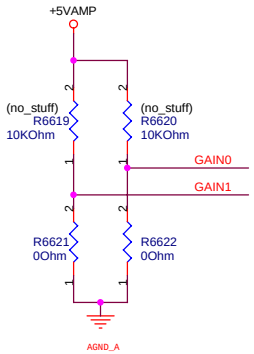
ASUSTeK COMPUTER INC

Engineer:

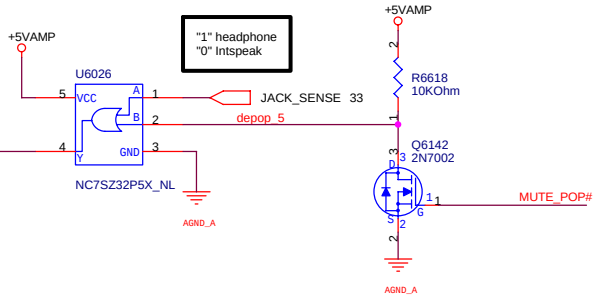
Size	Project Name	Rev
Custom	W7 J	1.2

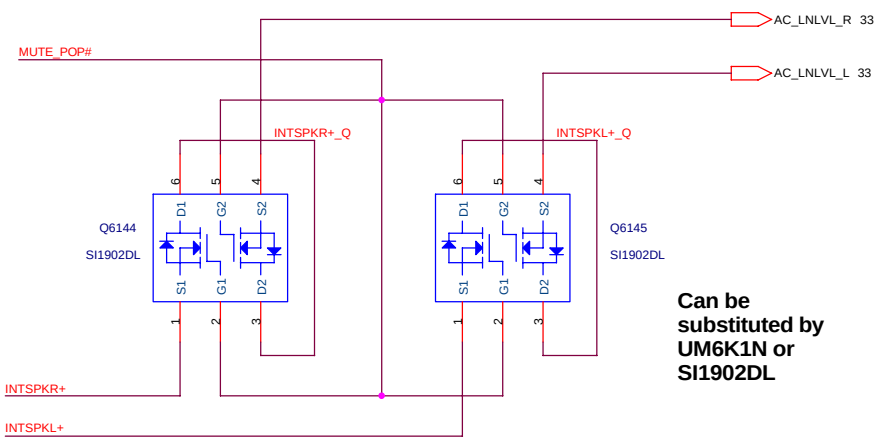
Date: Thursday, December 22, 2005 Sheet 31 of 64



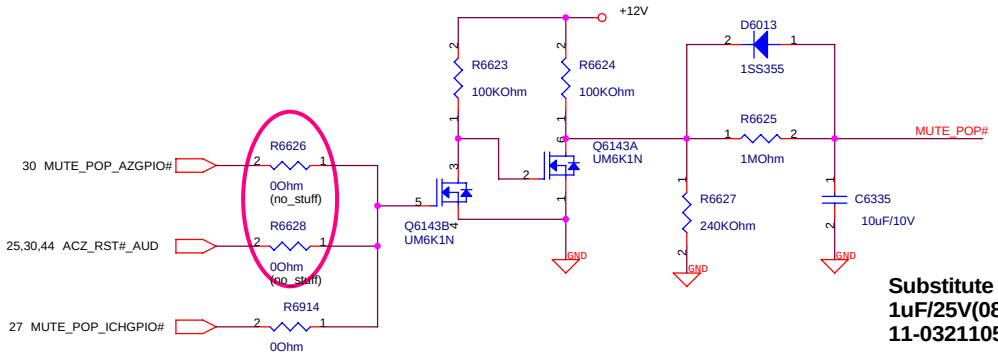


GAIN0	GAIN1	SE/BTL#	Av (inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB





Can be substituted by UM6K1N or SI1902DL



Substitute by a 1uF/25V(0805) 11-032110520

<Variant Name>

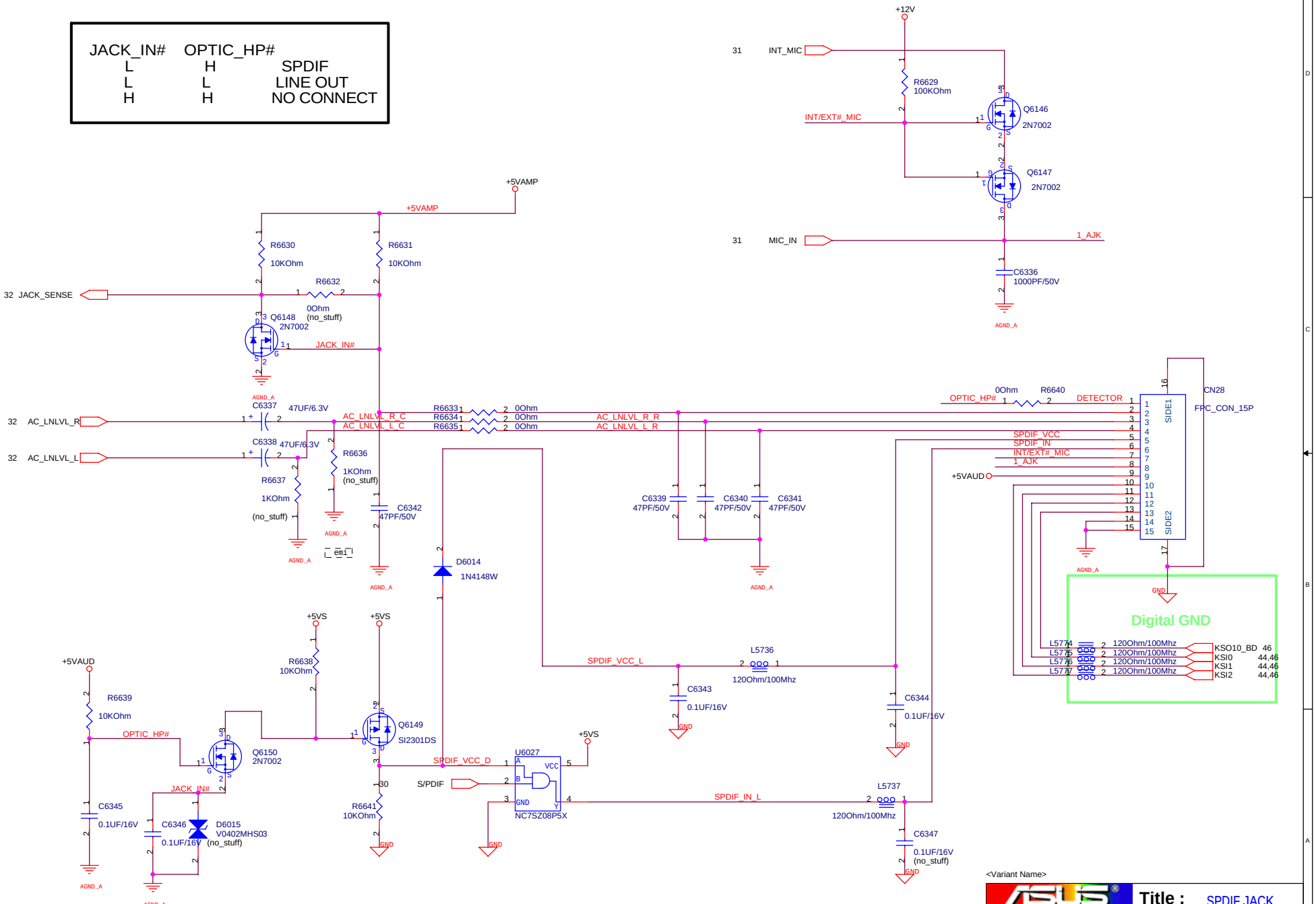
Title : AUDIO_AMP & INT SPK

ASUSTeK COMPUTER INC **Engineer:**

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 32 of 64

JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

ASUSTeK COMPUTER INC

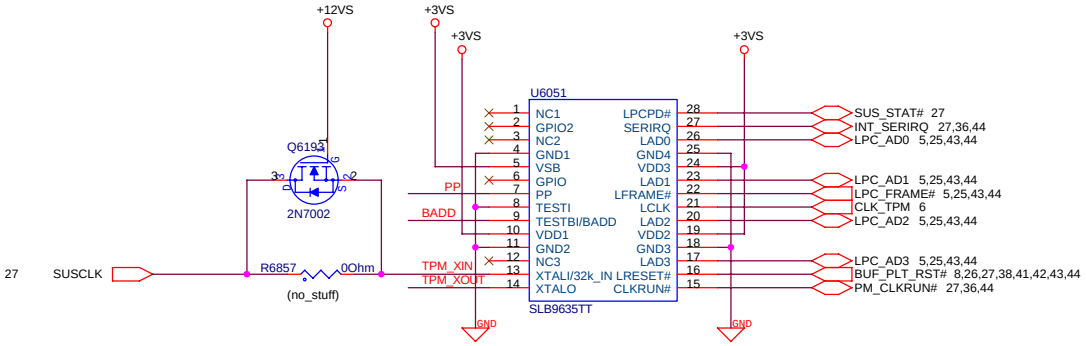
Title : SPDIF JACK

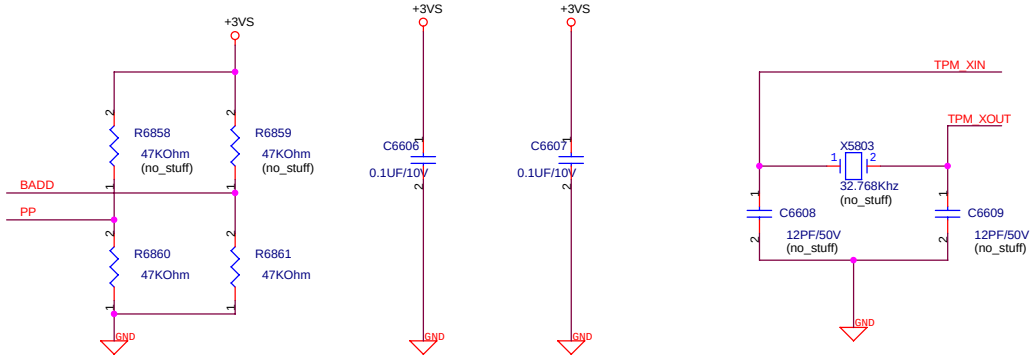
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 33 of 64

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.





<Variant Name>

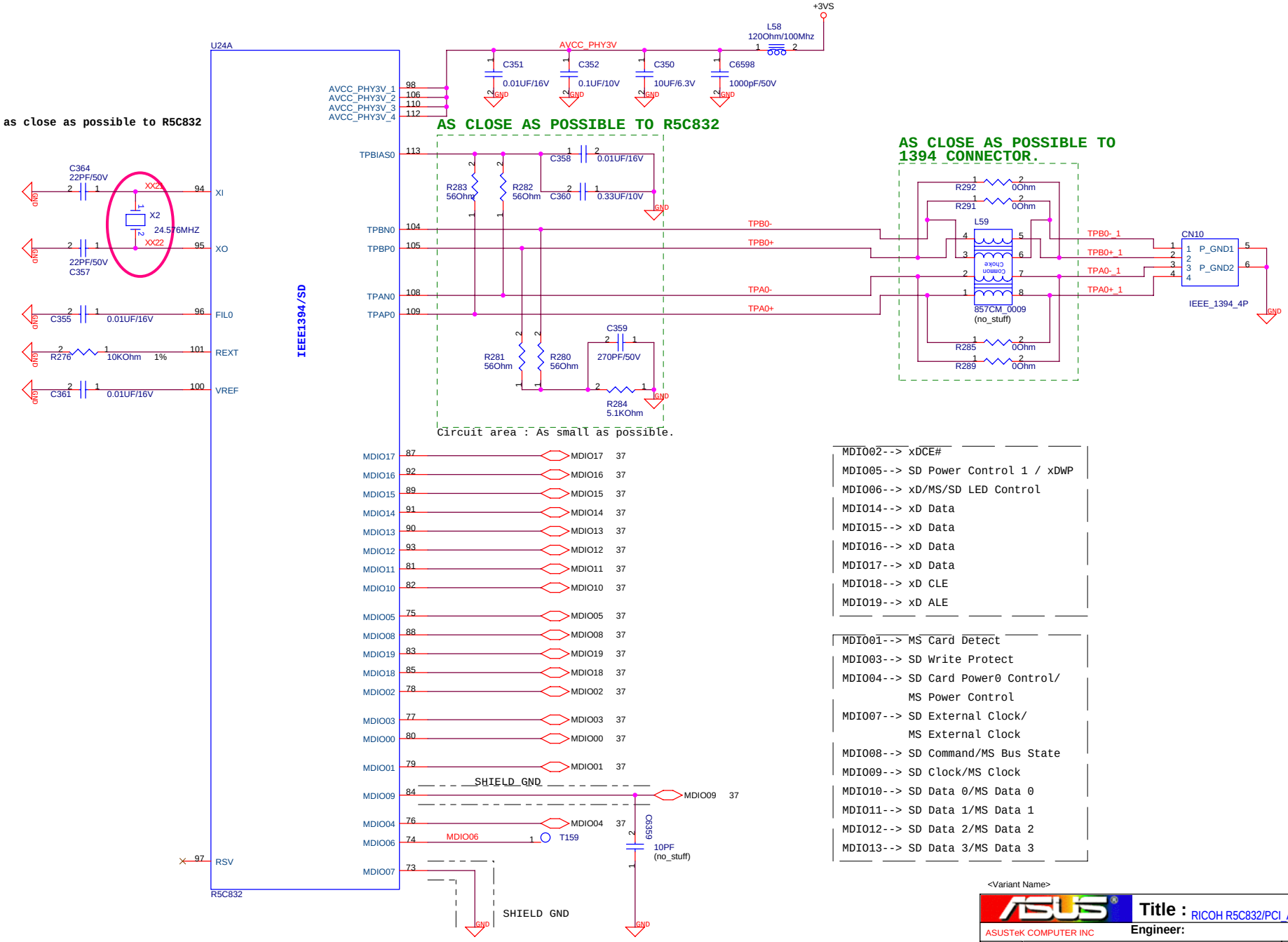
Title : TPM 1.2

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 34 of 64



<Variant Name>

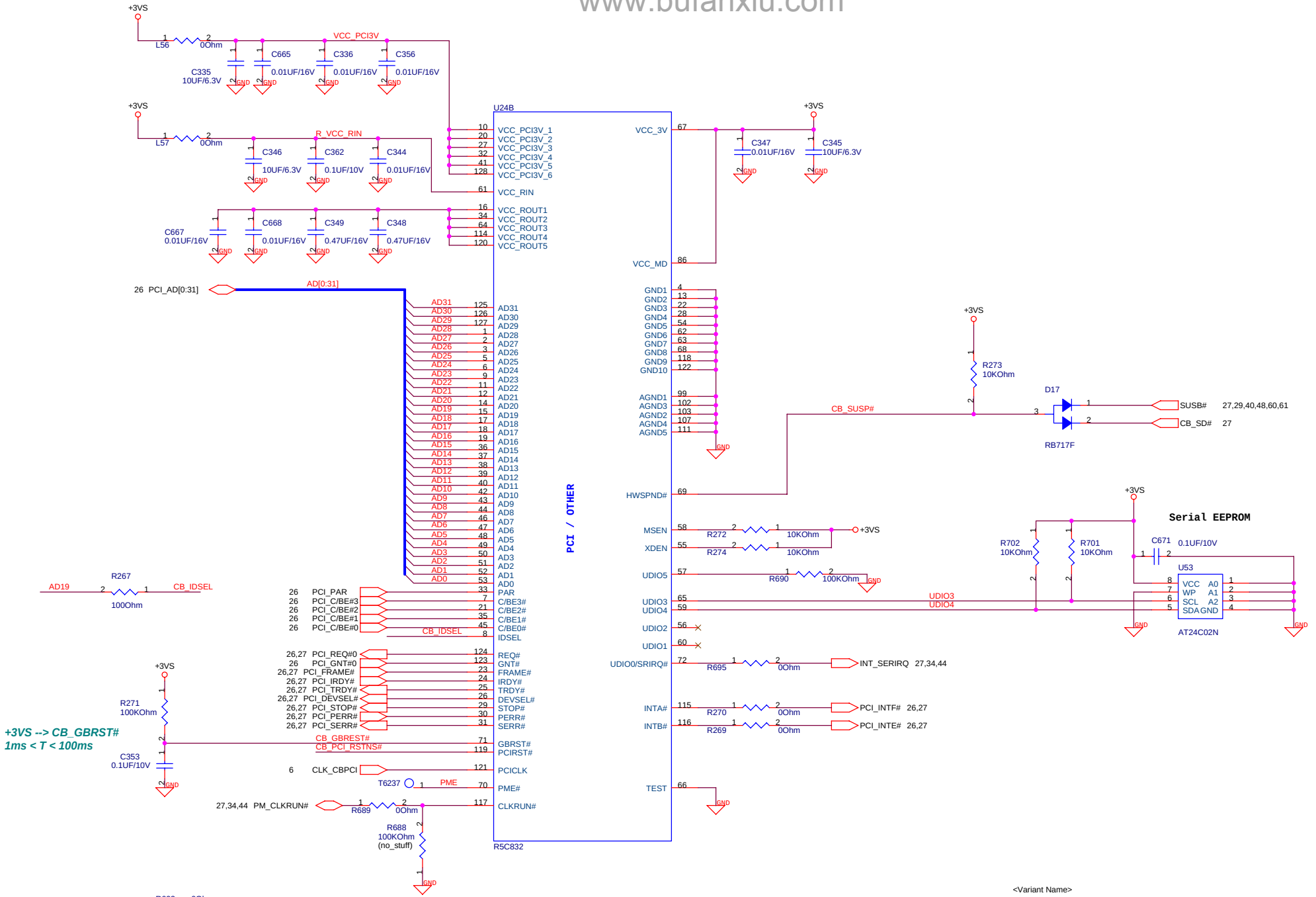
ASUSTeK COMPUTER INC

Title : RICOH R5C832/PCI_A

Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

Date: Thursday, December 22, 2005 Sheet 35 of 64



<Variant Name>

ASUSTeK COMPUTER INC

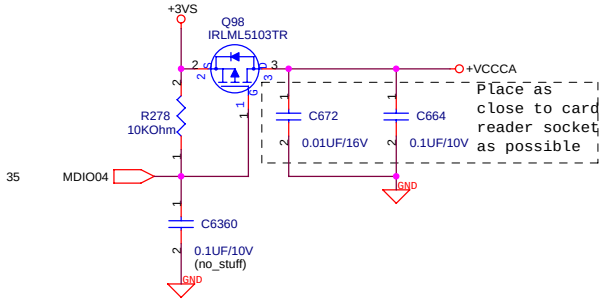
Title : RICOH R5C832/PCI_B

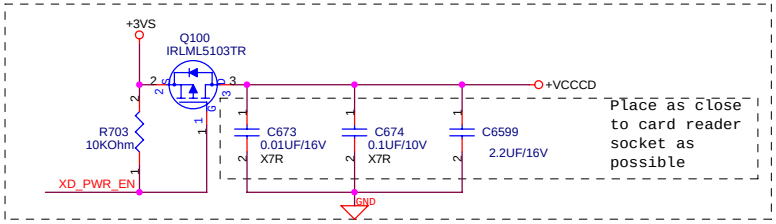
Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

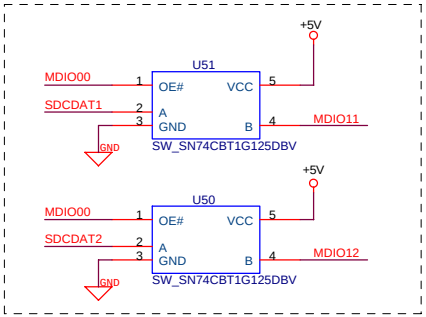
Date: Thursday, December 22, 2005 Sheet 36 of 64

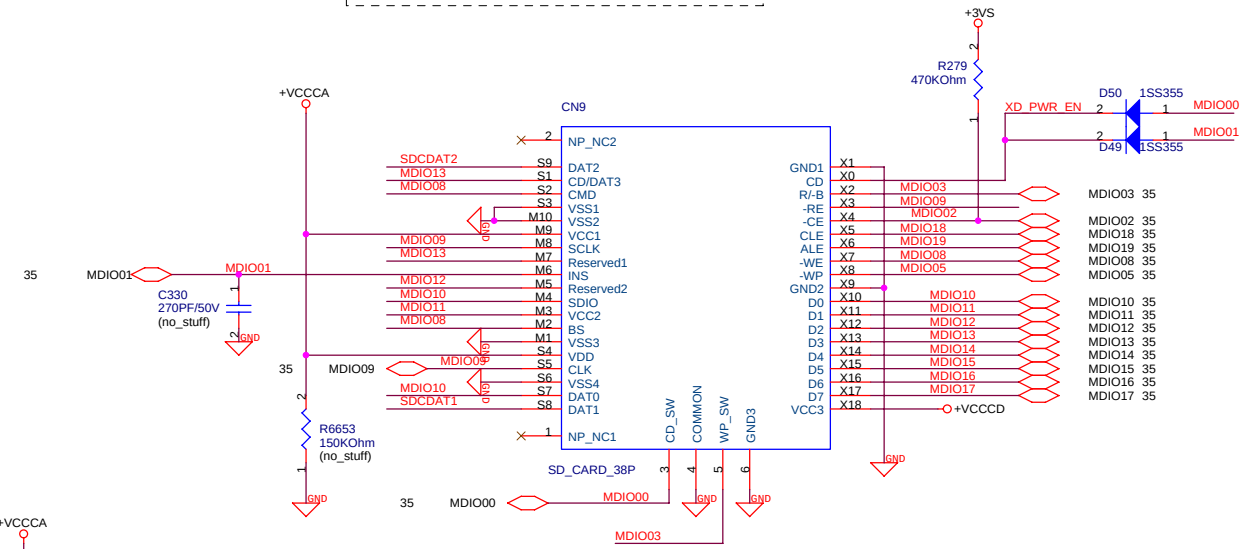
To correct the problem when MS Duo adaptor is in use.





SD/MMC/MS/MS-PRO Card Reader Socket





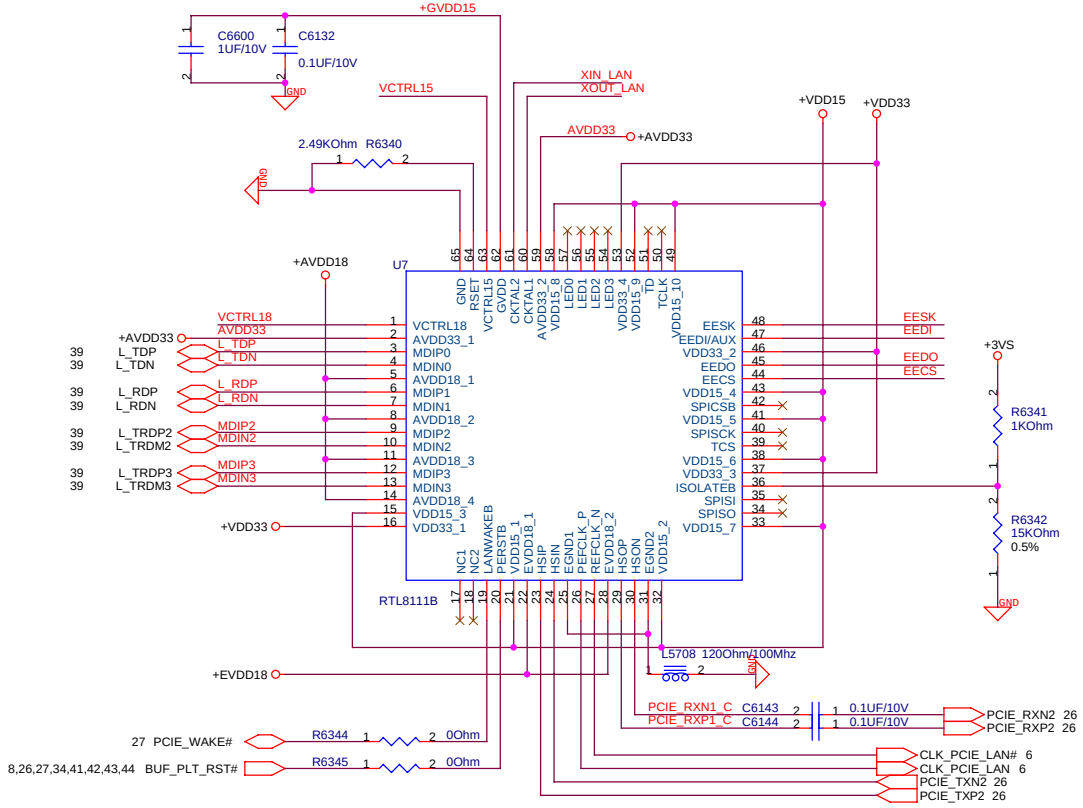
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

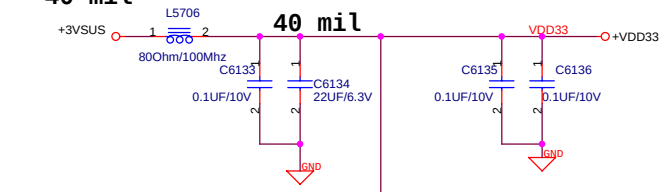
<Variant Name>

ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 37 of 64	

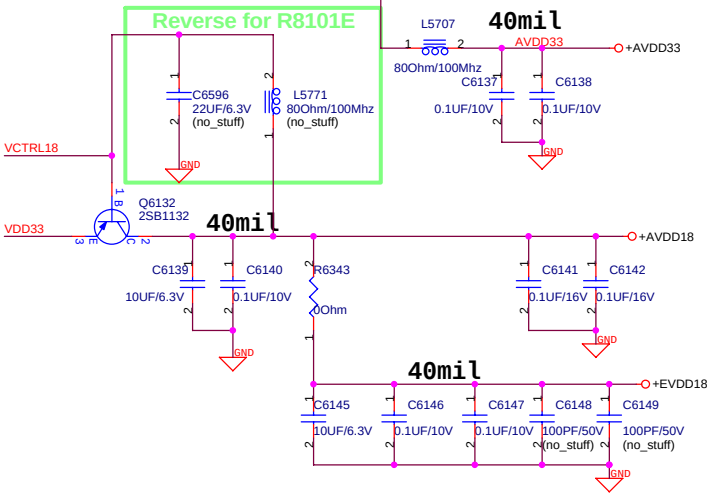
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



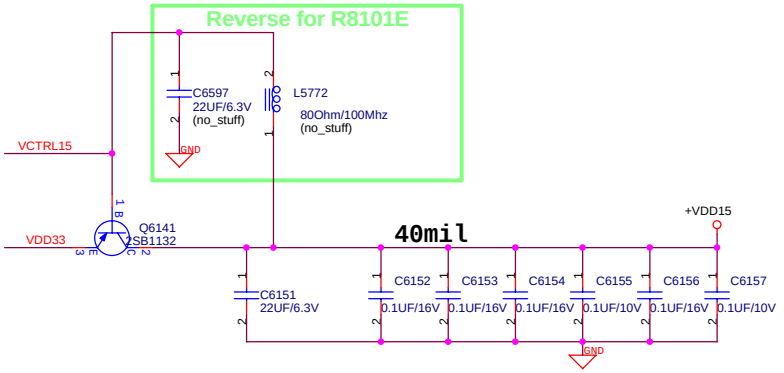
40 mil

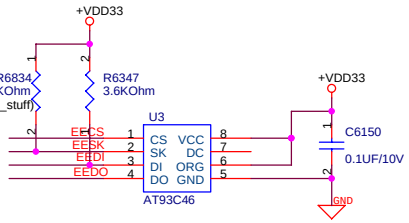


Reverse for R8101E



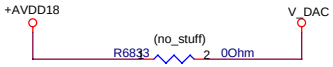
Reverse for R8101E

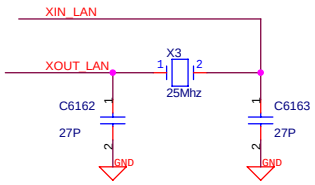




Reserve for R8101E ,Make stub as short as possible

Reserve for R8101E





<Variant Name>

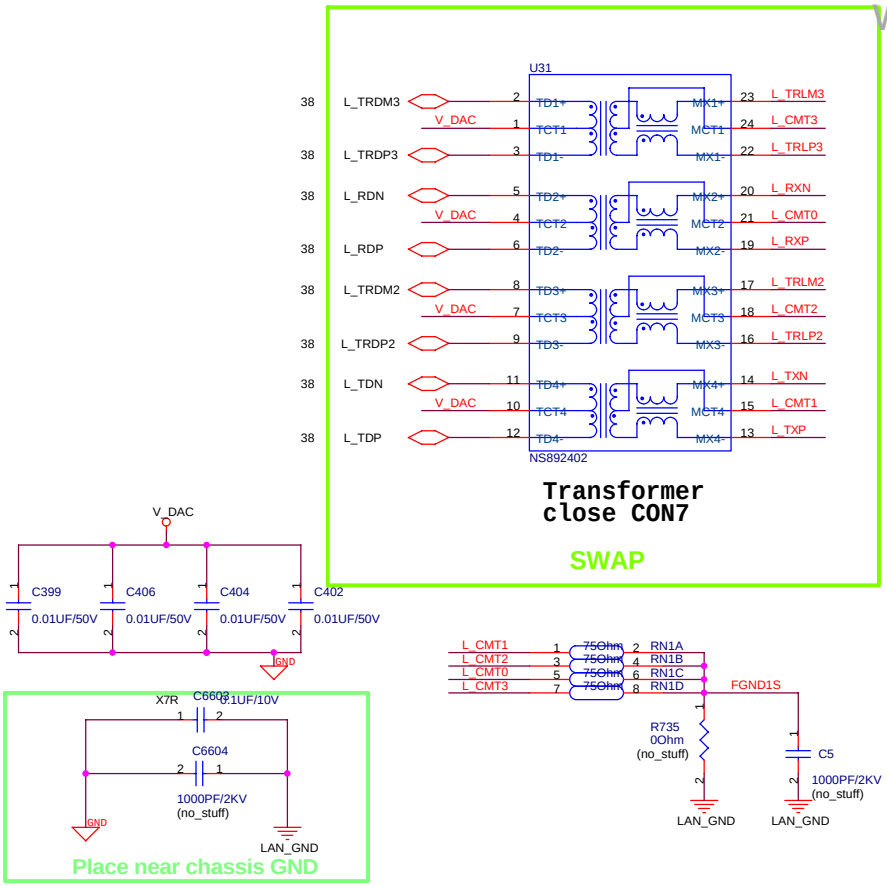
ASUSTeK COMPUTER INC

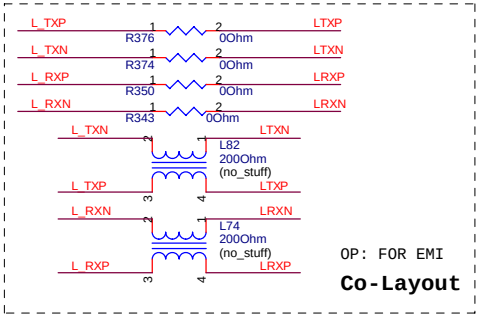
Title : GigaLAN

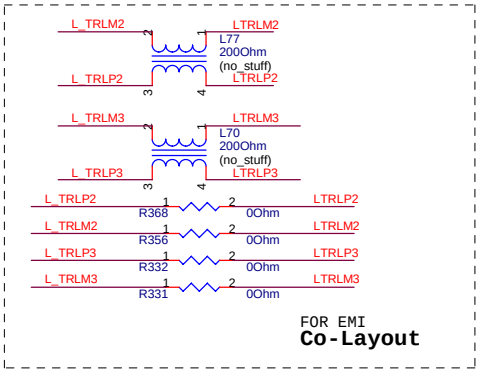
Engineer:

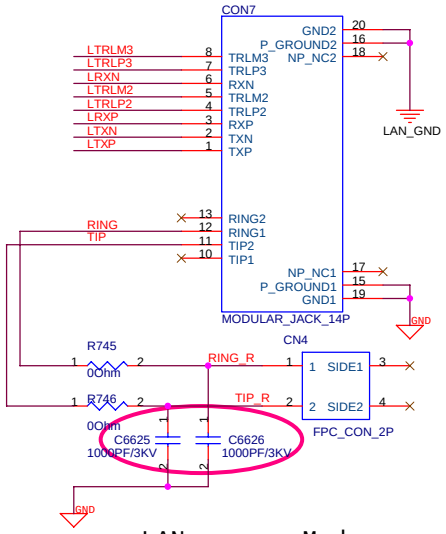
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 38 of 64

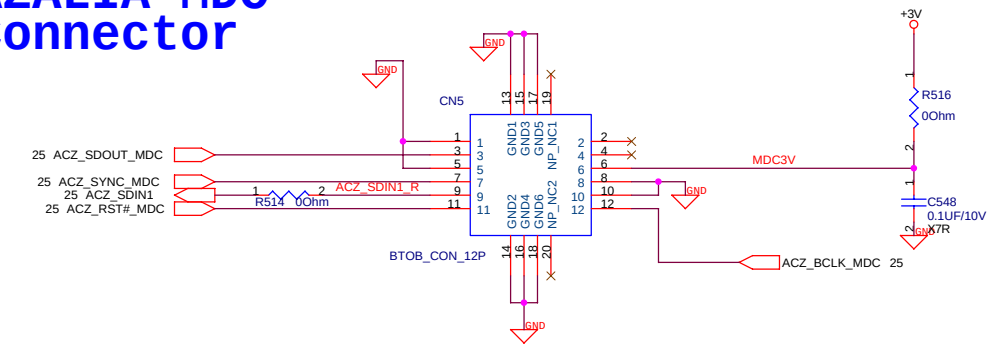






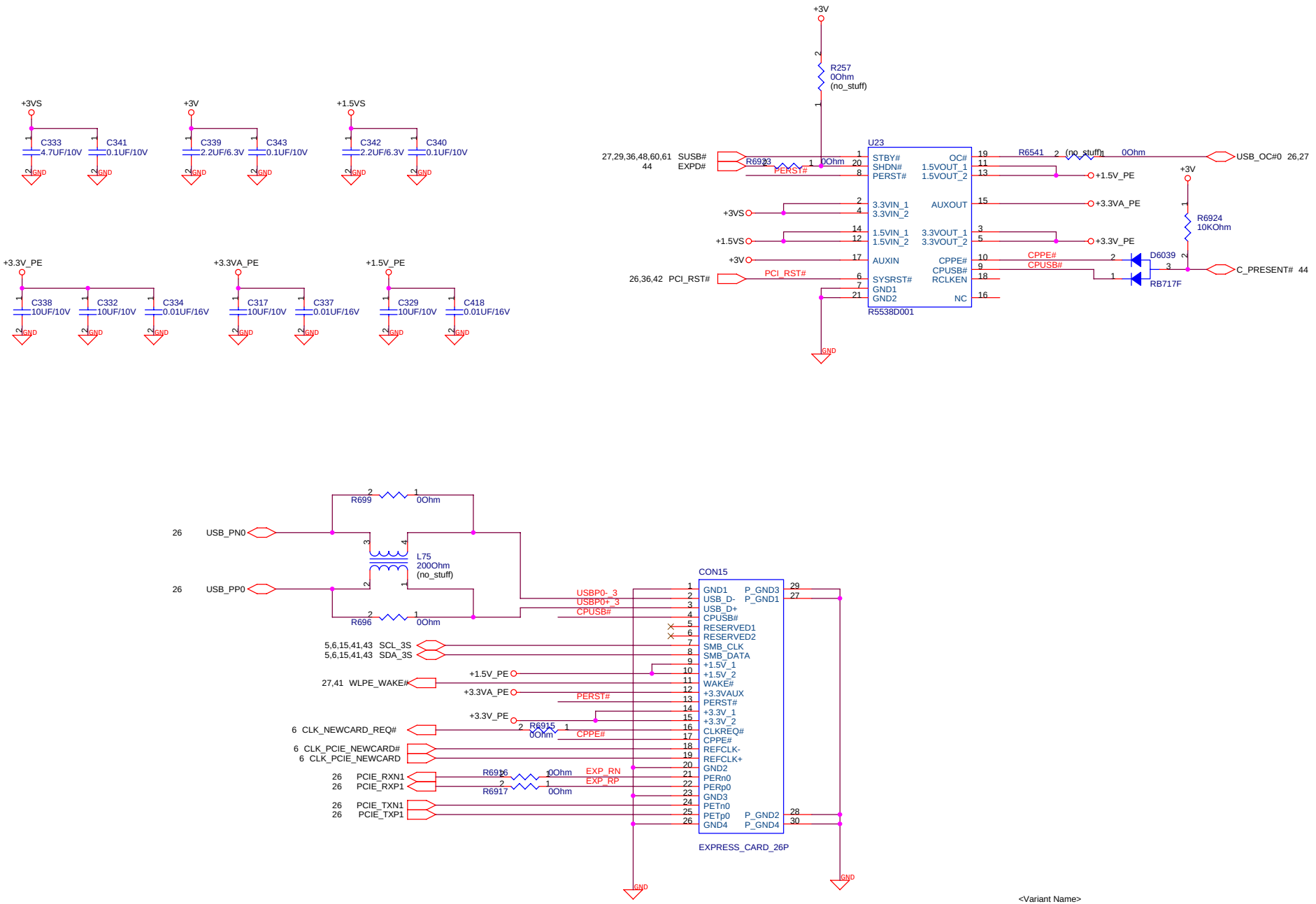


AZALIA MDC Connector



<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 39 of 64	



<Variant Name>

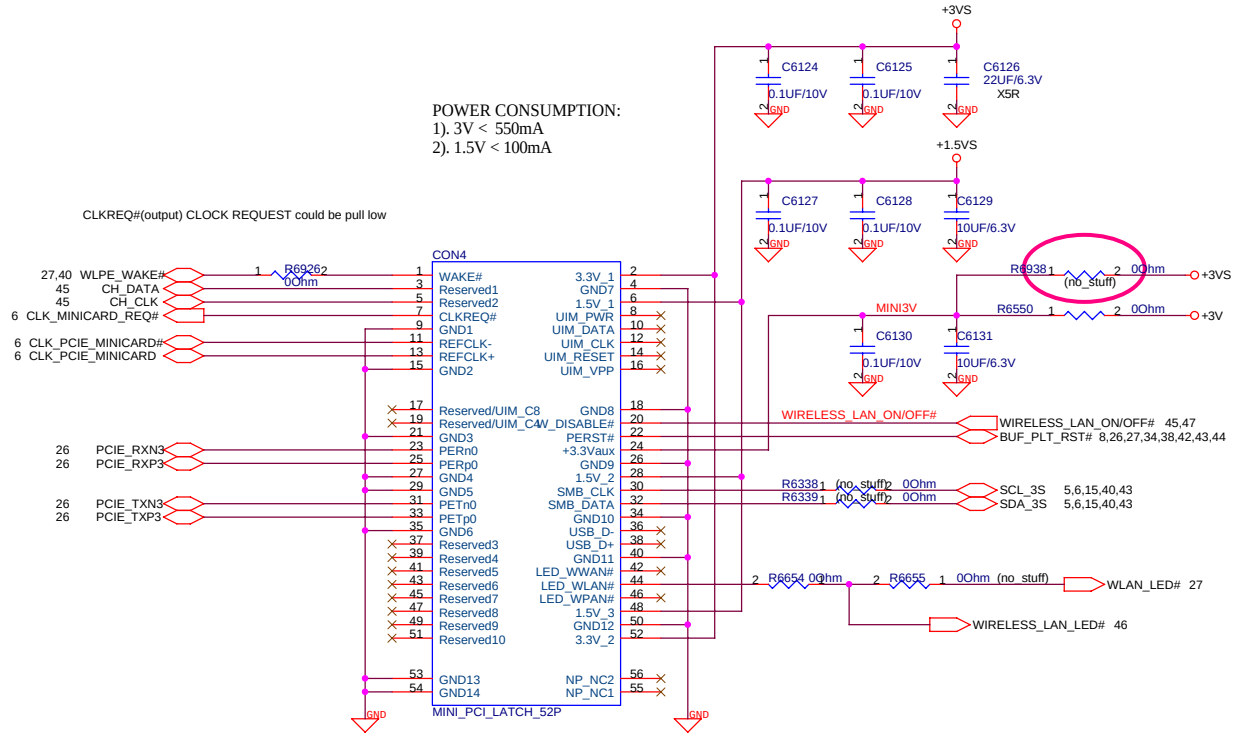
ASUSTeK COMPUTER INC

Title : Express Card

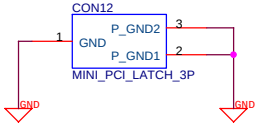
Engineer:

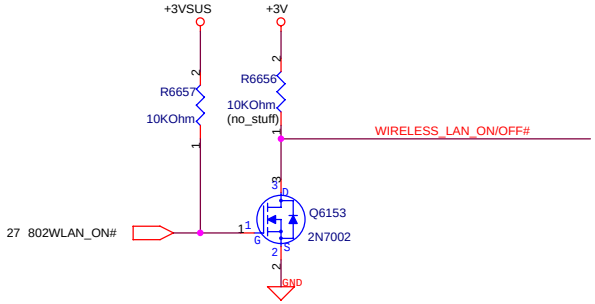
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 40 of 64



Mini Card Latch





<Variant Name>

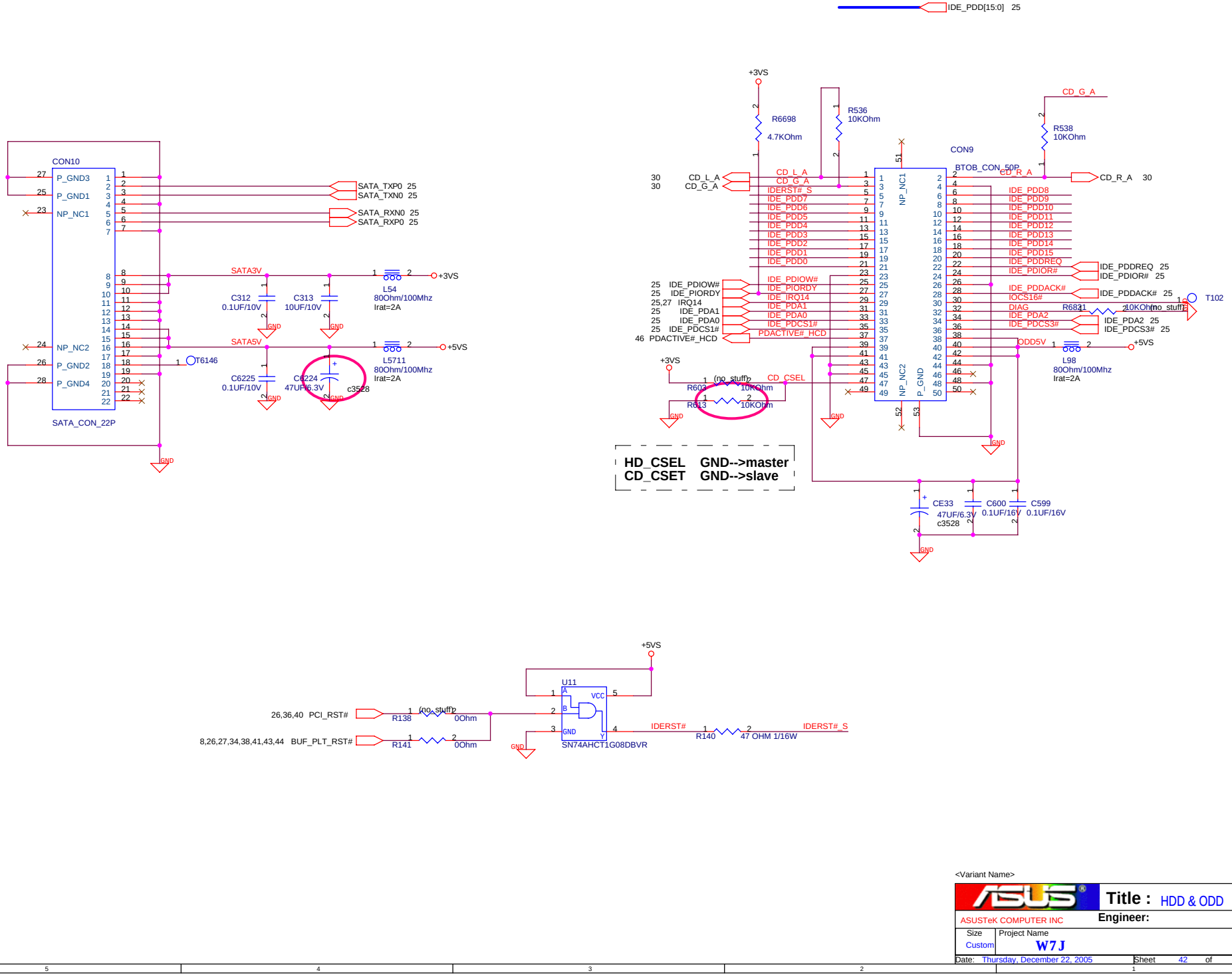
Title : MINICARD (802.11)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 41 of 64



<Variant Name>

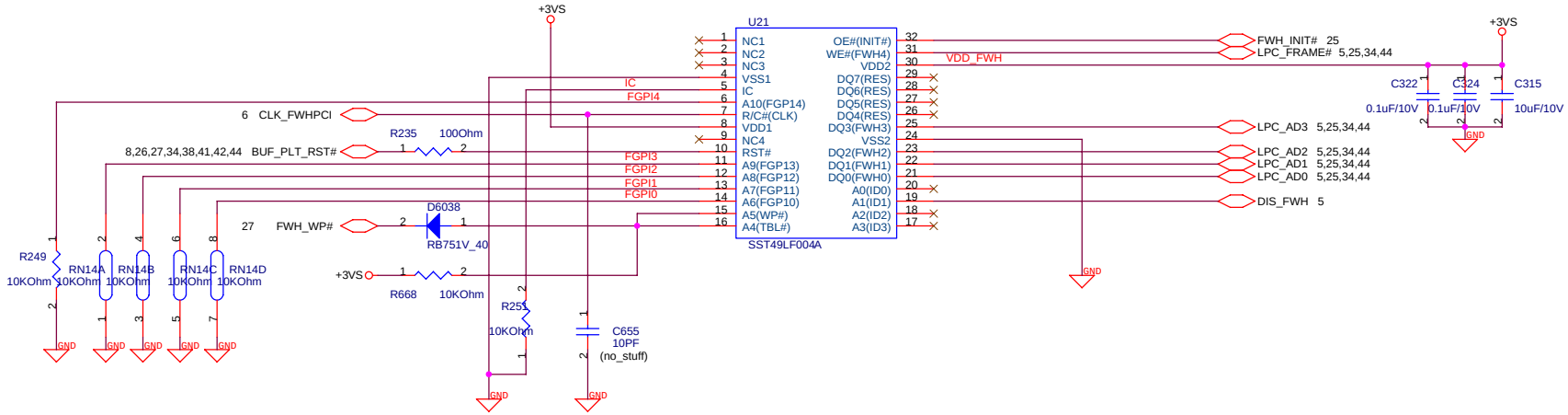
Title : HDD & ODD

ASUSTeK COMPUTER INC

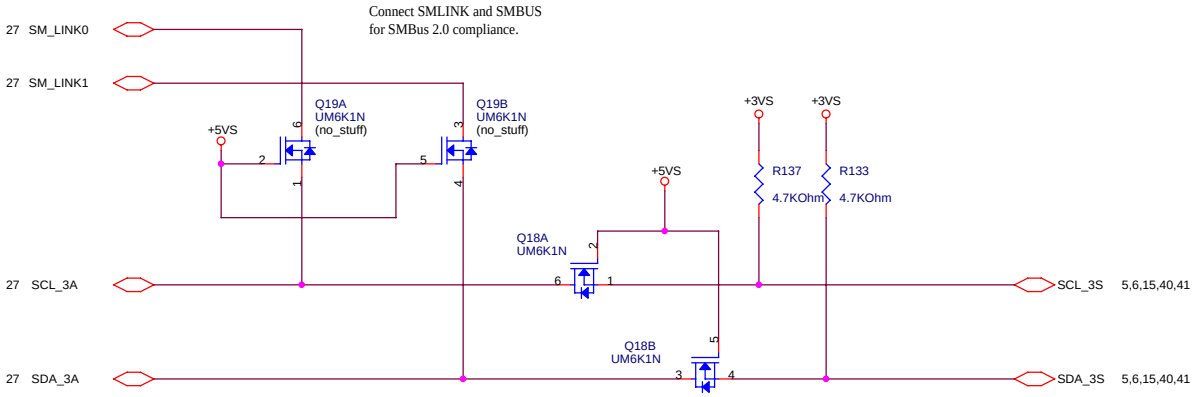
Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

Date: Thursday, December 22, 2005 Sheet 42 of 64



ICH7-M



ICH7-M

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
EXPRESS CARD
MINI-CARD

<Variant Name>

ASUSTeK COMPUTER INC	Title : FWH , SM BUS	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 43 of 64	

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

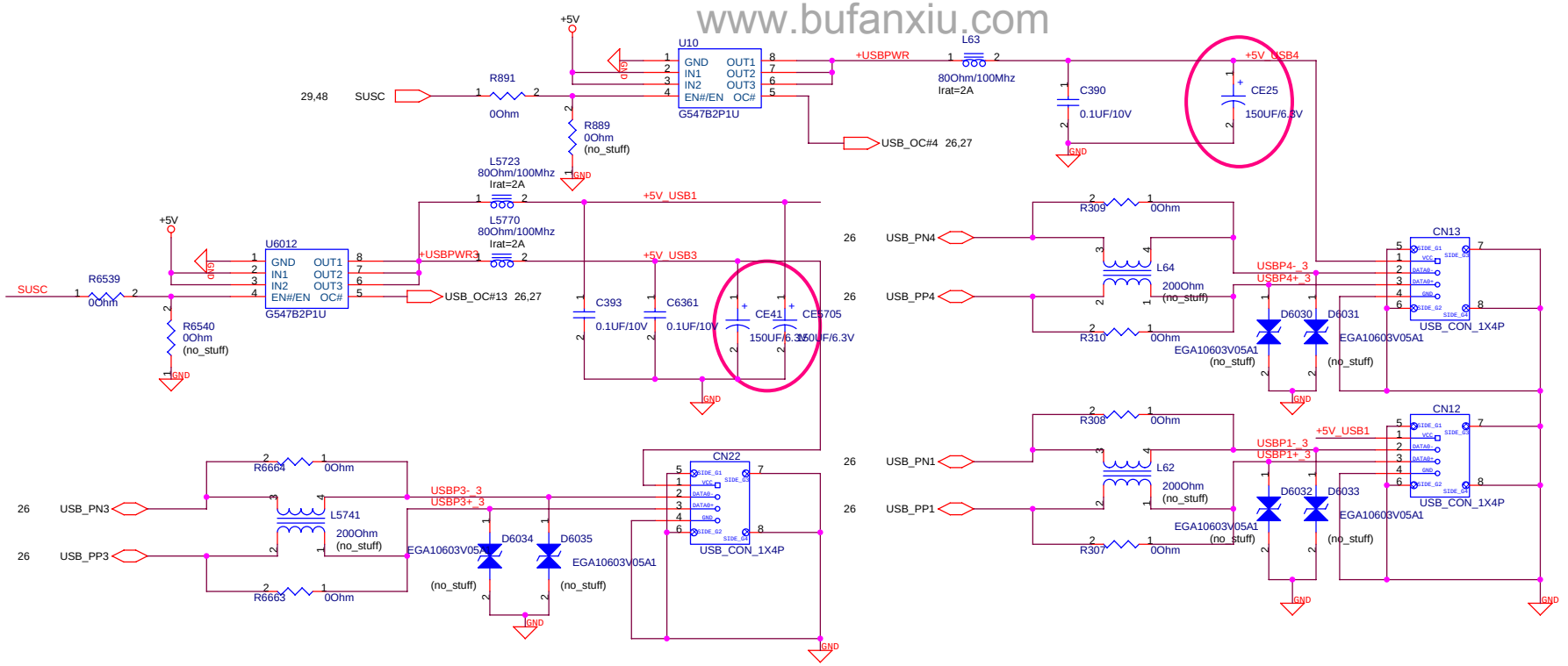
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

U46

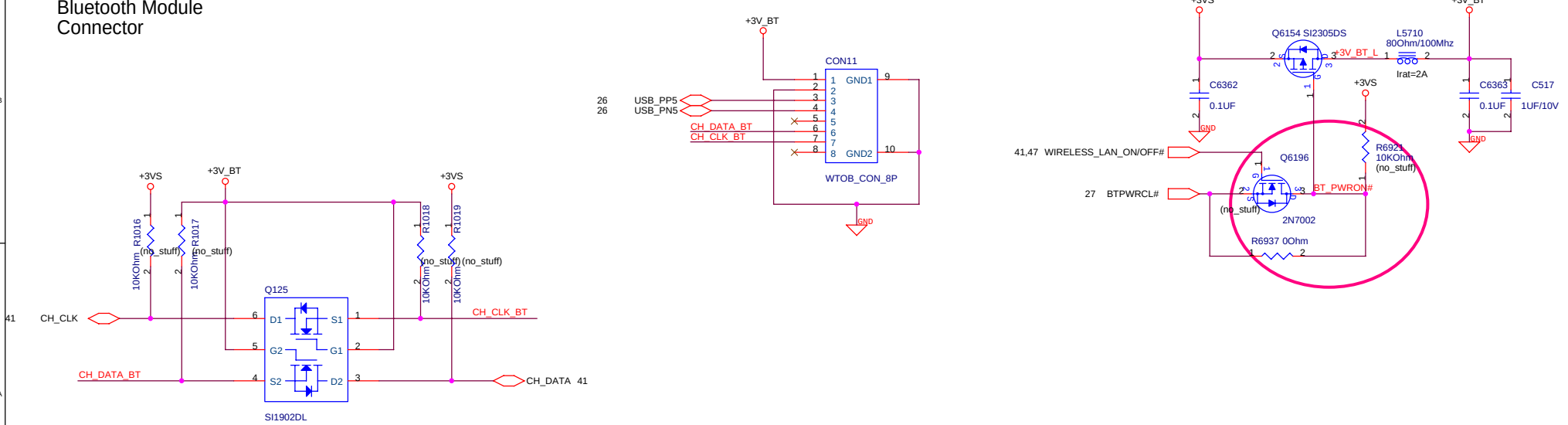
M38857

80mA

KID1	KID0	Matrix
0	0	US
1	1	UK
0	1	JP



Bluetooth Module Connector

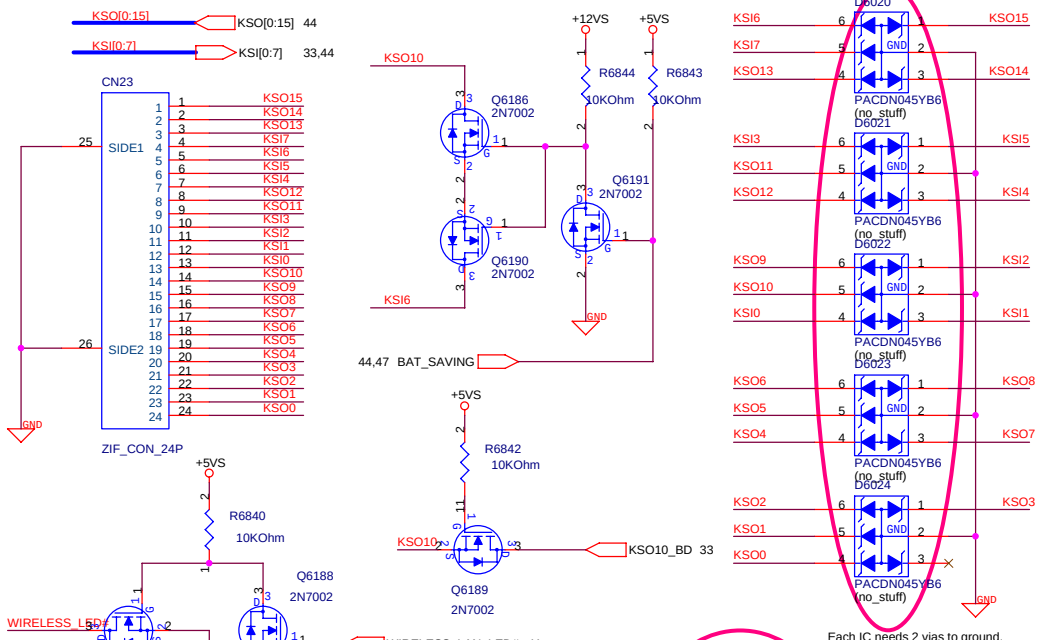


<Variant Name>

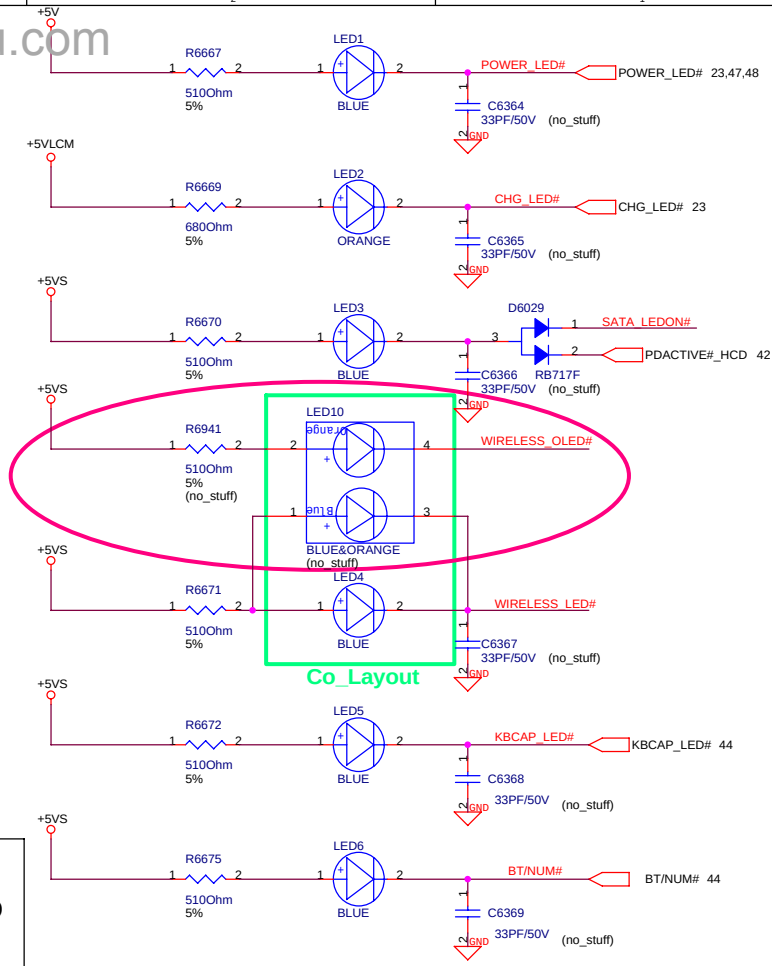
ASUSTeK COMPUTER INC	Title : USB * 3ports & BT	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 45 of 64	

Internal Keyboard Connector

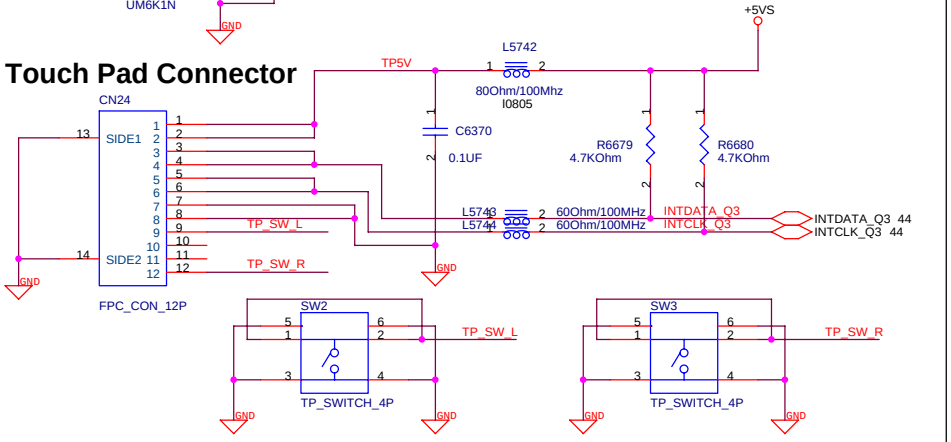
EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC and close to the connector as possible.



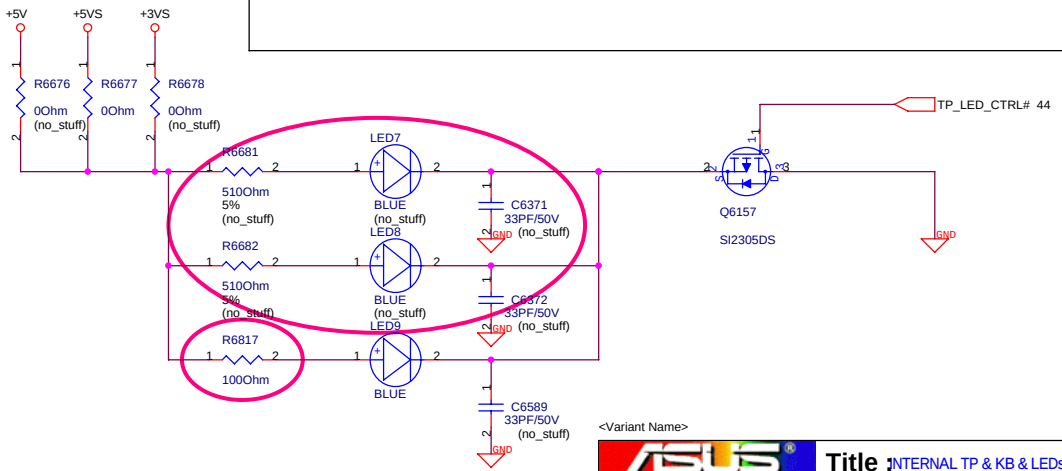
LEDs



Touch Pad Connector



Touch Pad LED



<Variant Name>

Title : INTERNAL TP & KB & LEDs

ASUSTeK COMPUTER INC

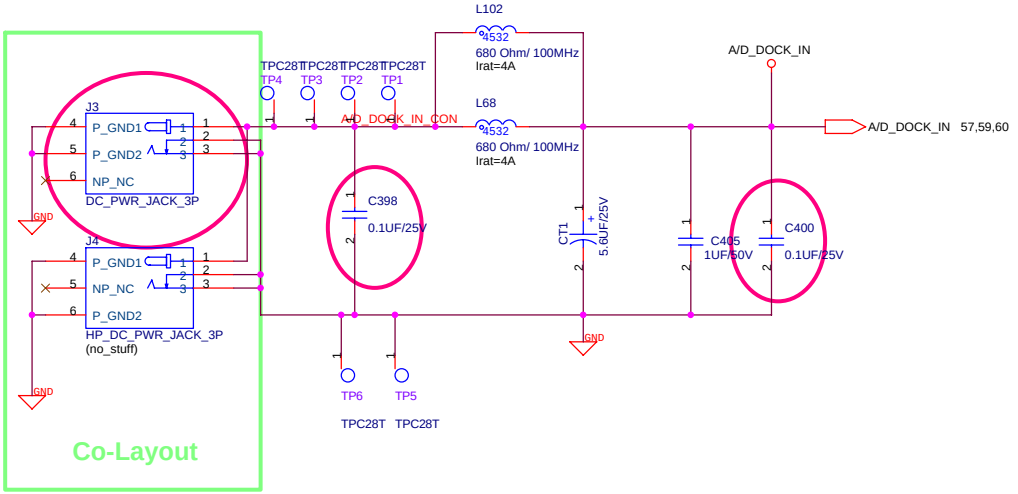
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

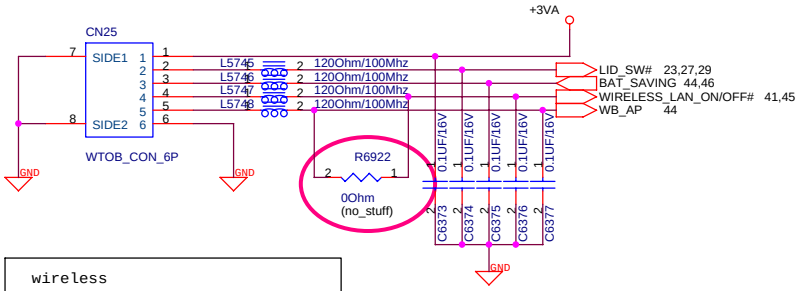
Date: Thursday, December 22, 2005 Sheet 46 of 64

EXT BOARD

DC-IN

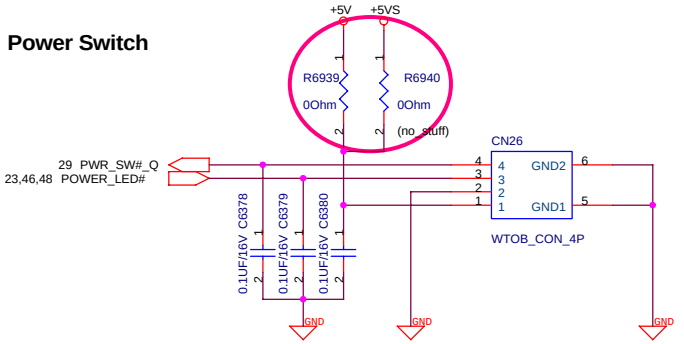


LID_SW_BD CN

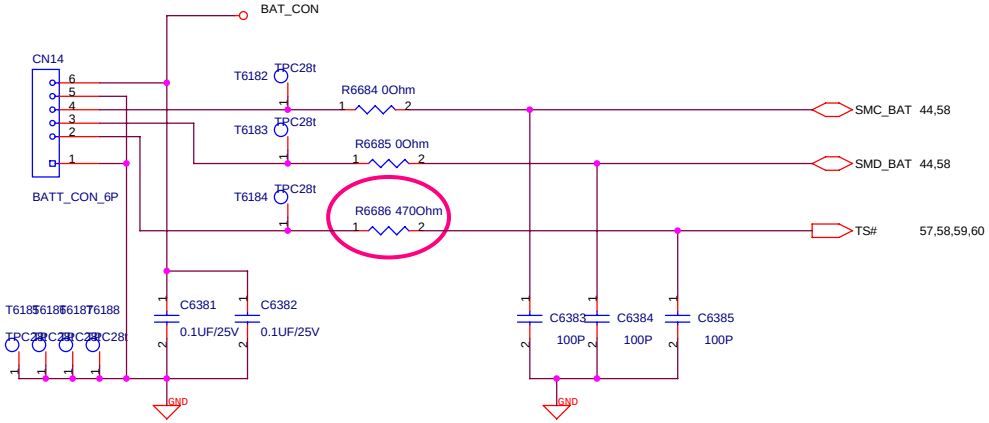



```
wireless
-----------------------------
right on ---> active high
left off ---> active low

WB_AP
-----------------------------
right off ---> active high
left  on  ---> active low
```

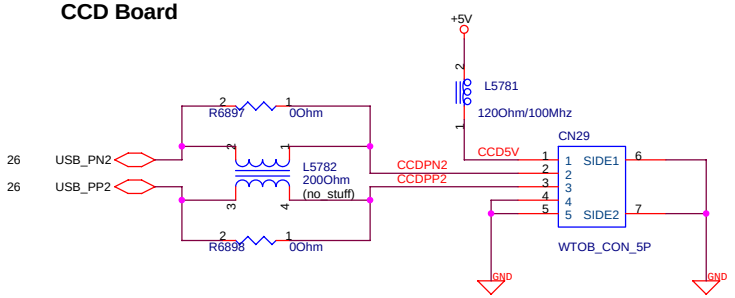
Power Switch



Battery Connector



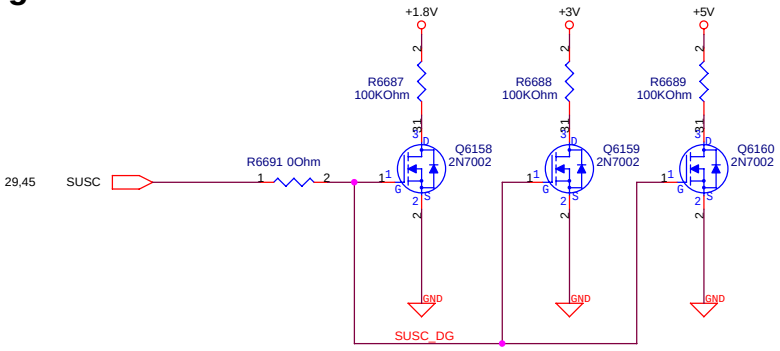
CCD Board

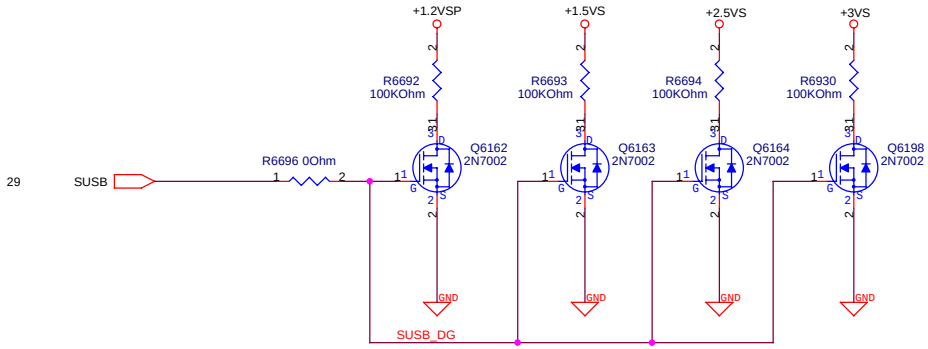


<Variant Name>

ASUSTeK COMPUTER INC	Title : DC IN,BATT CON,EXT BOARD	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 47 of 64	

Discharge



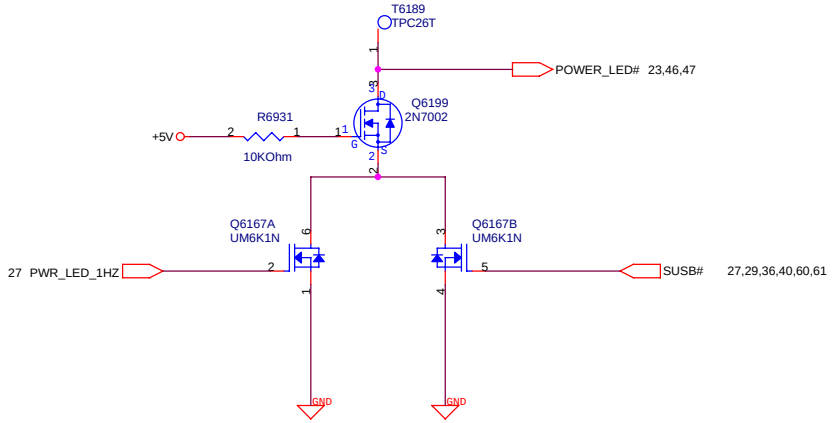


Poewr List

+3VA	+3VA	25,29,47,54,63
+3VSUS	+3VSUS	26,27,28,29,32,38,41,51
+5VA	+5VA	51,54,60
+5VSUS	+5VSUS	28,51,60
+3V	+3V	26,29,39,40,41,44,54,61
+5V	+5V	16,30,32,37,44,45,46,47,59,61
+12V	+12V	27,32,33,61
+3VS	+3VS	5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,50,52,60,61
+5VS	+5VS	5,24,28,29,30,32,33,42,43,44,46,47,50,61
+12VS	+12VS	5,24,34,46,61
+VCORE	+VCORE	3,4,5,44,50
+VCCP	+VCCP	2,3,4,6,7,8,10,11,12,25,28,52
+1.2VSP	+1.2VSP	17,18,56
+2.5VS	+2.5VS	10,20,21,54
+1.8VS	+1.8VS	20,61
+0.9VS	+0.9VS	16,53
+1.5VS	+1.5VS	3,8,10,11,26,28,40,41,52
+VCC_RTC	+VCC_RTC	25,28
+1.8V	+1.8V	8,12,13,14,15,16,53
VTT_REF	VTT_REF	8,13,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	47,57,59,60
+VGA_VCORE	+VGA_VCORE	17,55

GND

Power LED On



<Variant Name>

Discharge,Power Rail & Power LED On

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 48 of 64

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARD READER	AD19	0	E
1394	AD19	0	F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor	0101110x (2E)
PIC	1001001x (92)
Express Card	TBD
Mini Card	TBD

ICH7-M GPIO	W7J
GPIO 0	PM_BMBUSY#
GPIO 1	PCI_REQ#5
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 6	BACK_OFF#
GPIO 7	MUTE_POP_ICHGPIO#
GPIO 8	EXTSMI#
GPIO 9	W_OLED#
GPIO 10	(PWRLMT#)
GPIO 11	SMBALERT#
GPIO 12	KBC_SCI#
GPIO 13	PWR_LED_1HZ
GPIO 14	WLAN_ON#
GPIO 15	802_LED_EN#
GPIO 16	DPRSLPVR
GPIO 17	GNT5#
GPIO 18	STP_PCI#
GPIO 19	Memoryclk
GPIO 20	STP_CPU#
GPIO 21	
GPIO 22	PCI_REQ#4
GPIO 23	LPC_DRQ#1
GPIO 24	SW_RST#
GPIO 25	CB_SD#
GPIO 26	MEM ID0
GPIO 27	MEM ID1
GPIO 28	MEM ID2
GPIO 29	USB_OC#5
GPIO 30	USB_OC#6
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 33	BT_ON#
GPIO 34	FWH_WP#
GPIO 35	SATACLKREQ#
GPIO 36	BT_LED_EN#
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 48	GNT4#
GPIO 49	CPUPWRGD

KBC GPIO	W7J
P23	
P22	BAT_LEARN
P21	
P20	KBCRSM
P42	WATCHDOG
P43	
P44	xKBRC
P45	GA20
P46	KBDSCI
P47	CLKRUN#
P50	BAT_LLOW#
P51	TP_LED_CTRL#
P52	
P53	EXPD#
P54	LID_EC#
P55	BAT_IN#
P56	CPU_FAN_PWM
P57	ADJ_BL
P67	WB_AP
P66	M_MODE#
P65	
P64	ACIN#
P63	EOC#_LED
P62	C_PRESENT#
P61	ACZ_RST#_AUD
P60	
P75	KBDCLK_5S
P74	MOUSECLK_5S
P73	INTCLK_Q3
P72	KBDDATA_5S
P71	MOUSEDATA_5S
P70	INTDATA_Q3
P77	SMC_KBC
P76	SMD_KBC
P27	SCROLL_LED#
P26	NUM_LED#
P25	CAP_LED#
P24	SET_RSTNS#
P40	EXT_SMI#
P41	

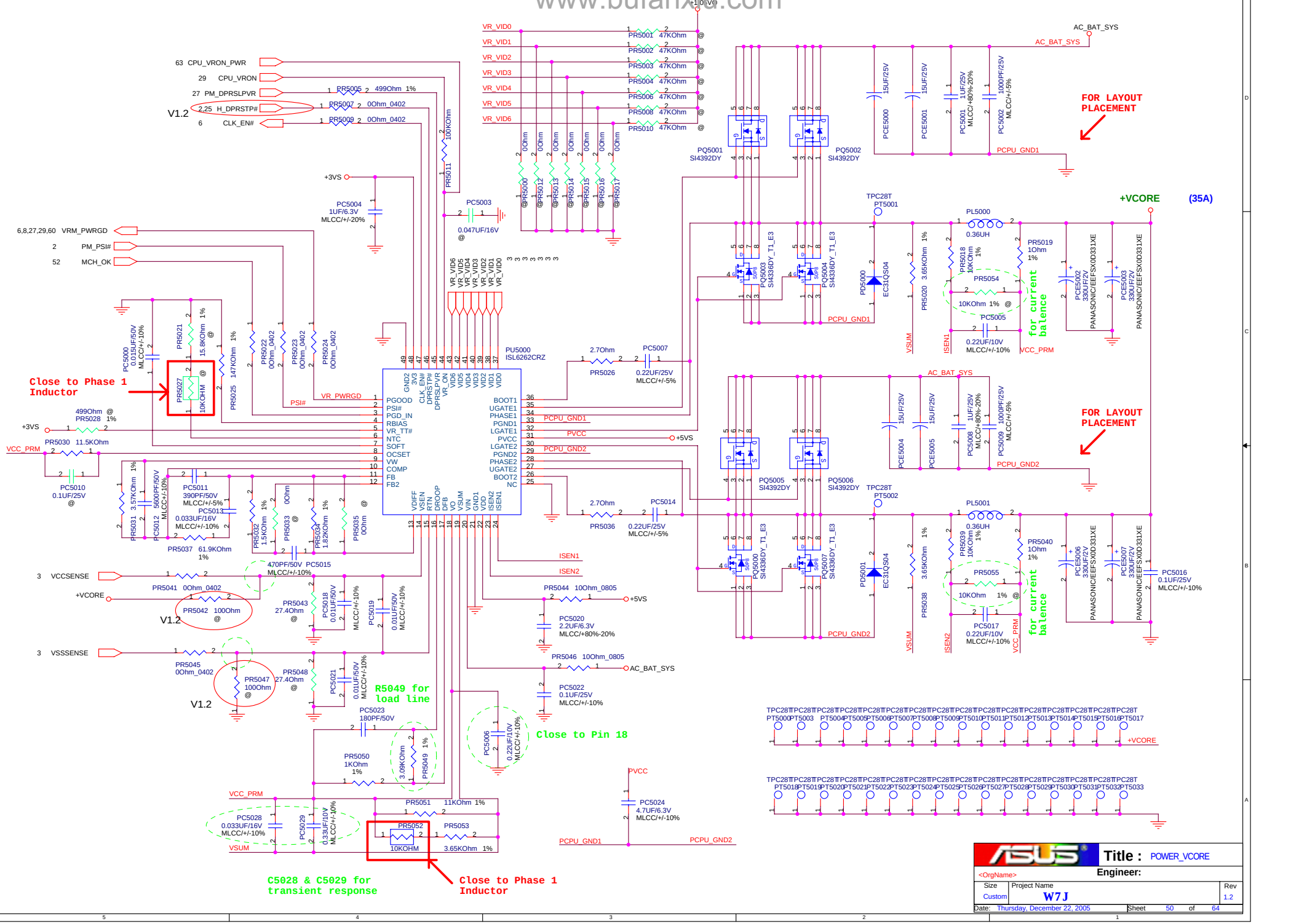
<Variant Name>

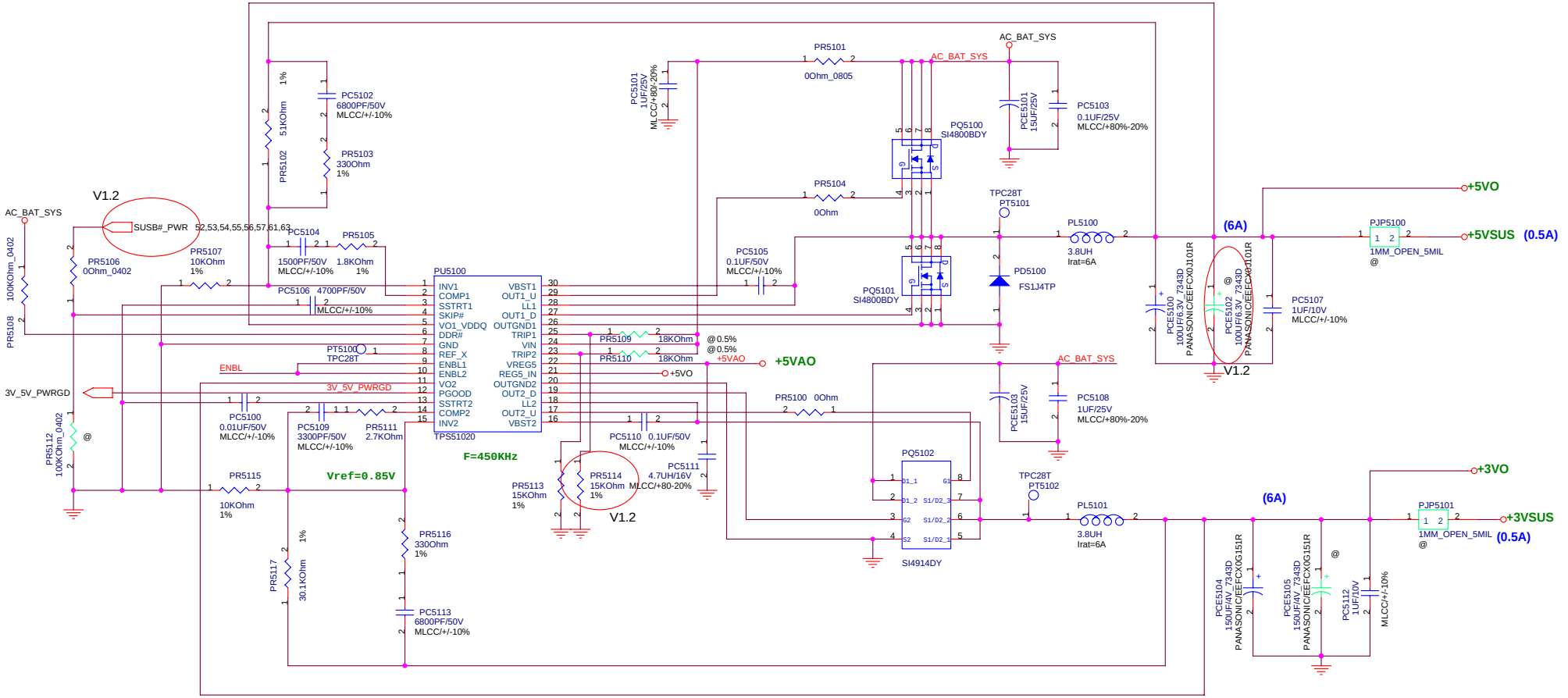
Title : System Resource

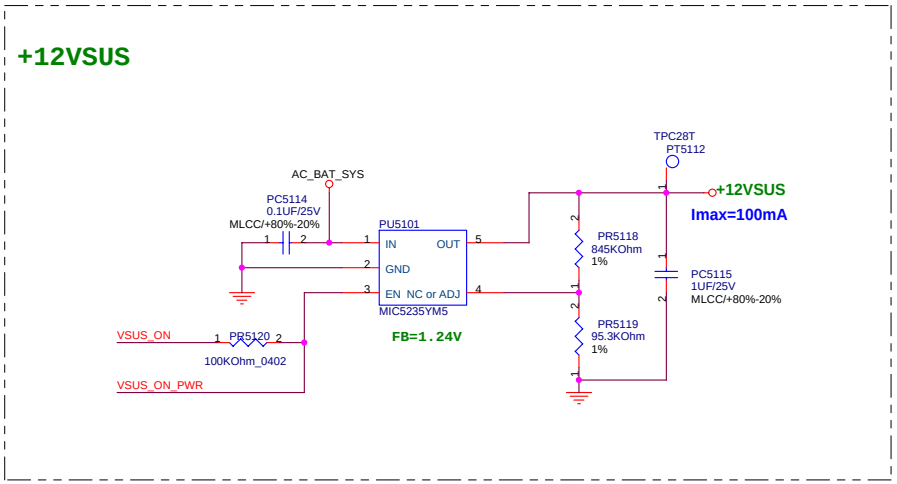
ASUSTeK COMPUTER INC Engineer:

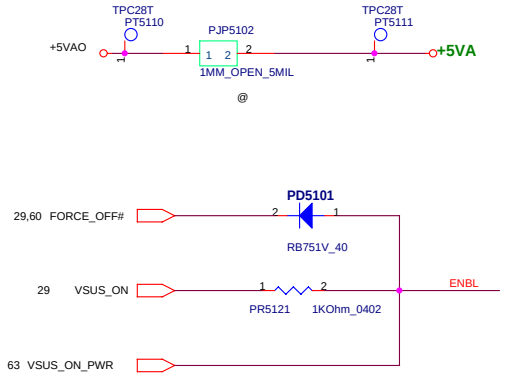
Size	Project Name	Rev
Custom	W7J	1.2

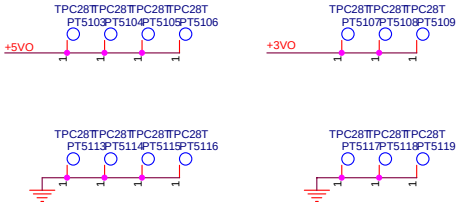
Date: Thursday, December 22, 2005 Sheet 49 of 64



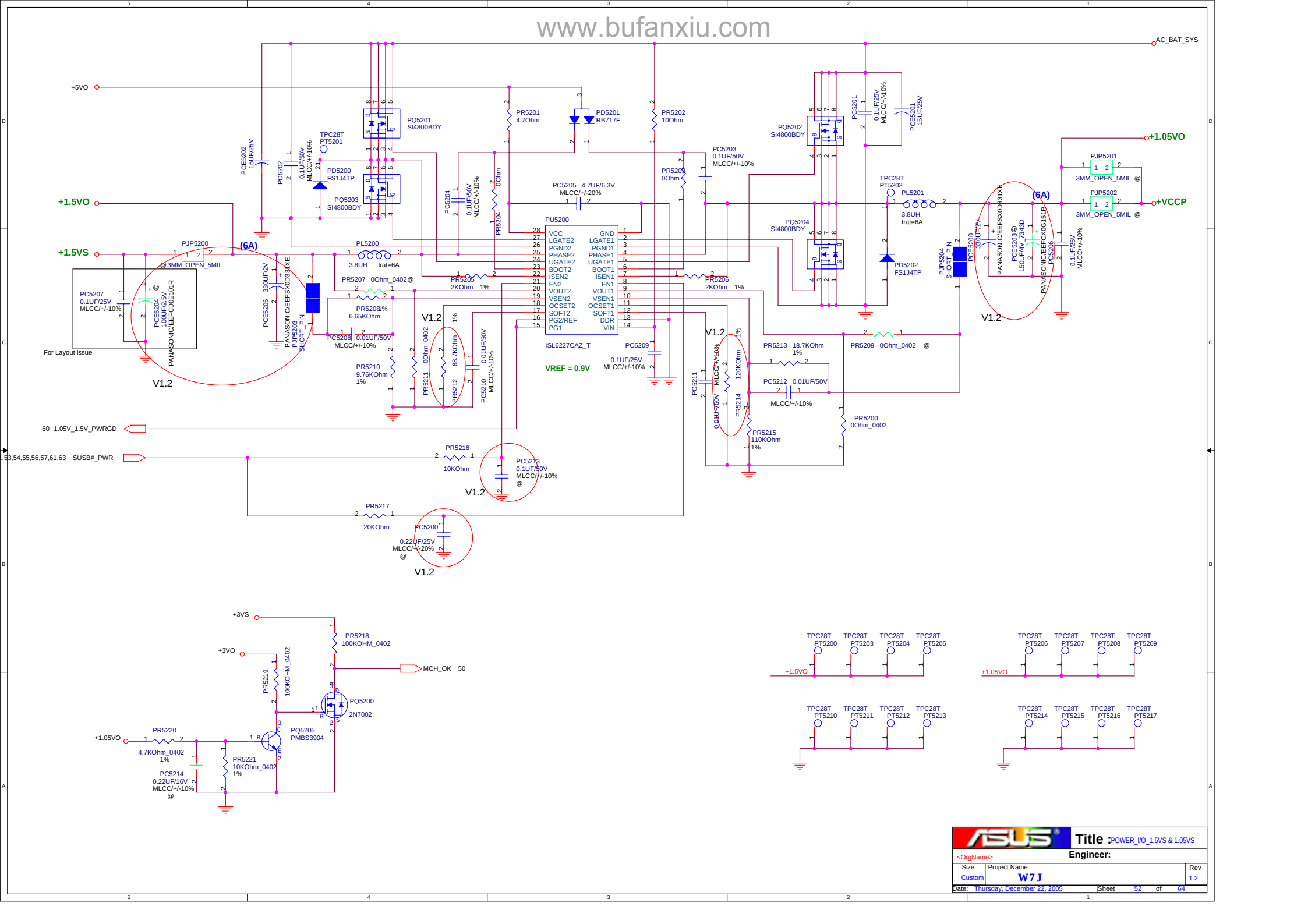




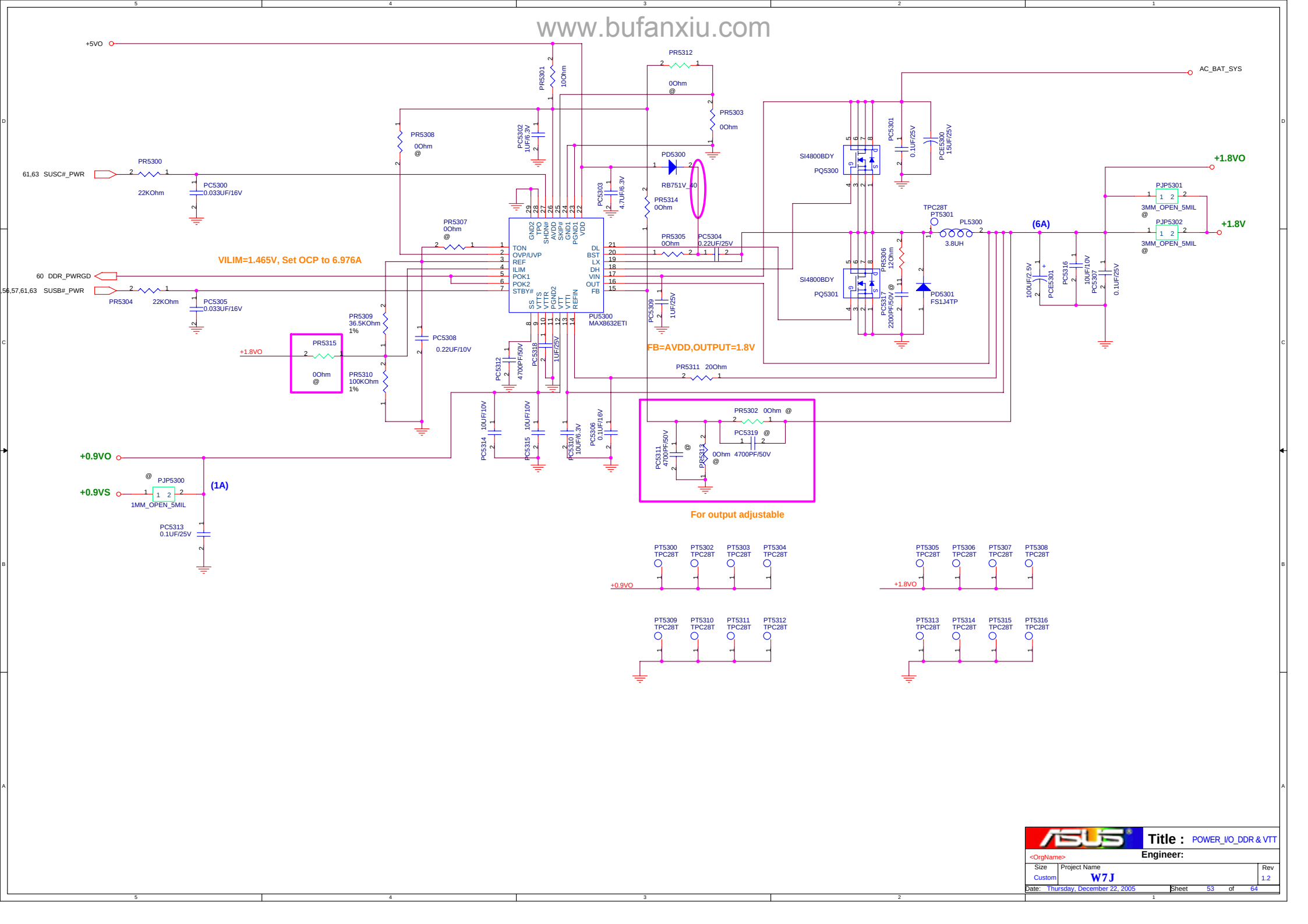




ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 51 of 64	

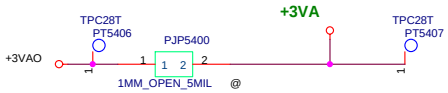


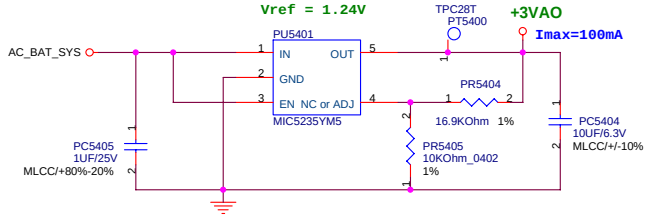
ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 52 of 64	



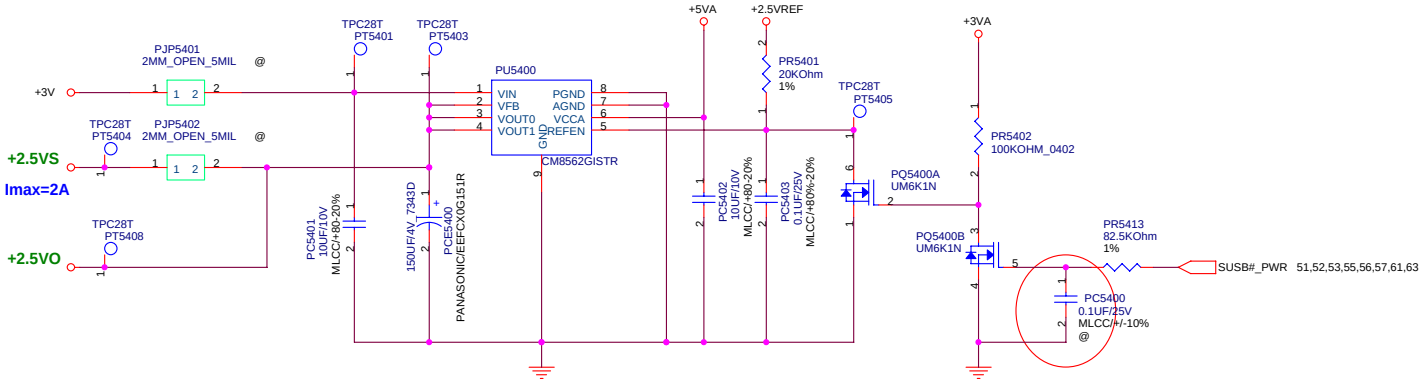
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 53 of 64	

+3VA0

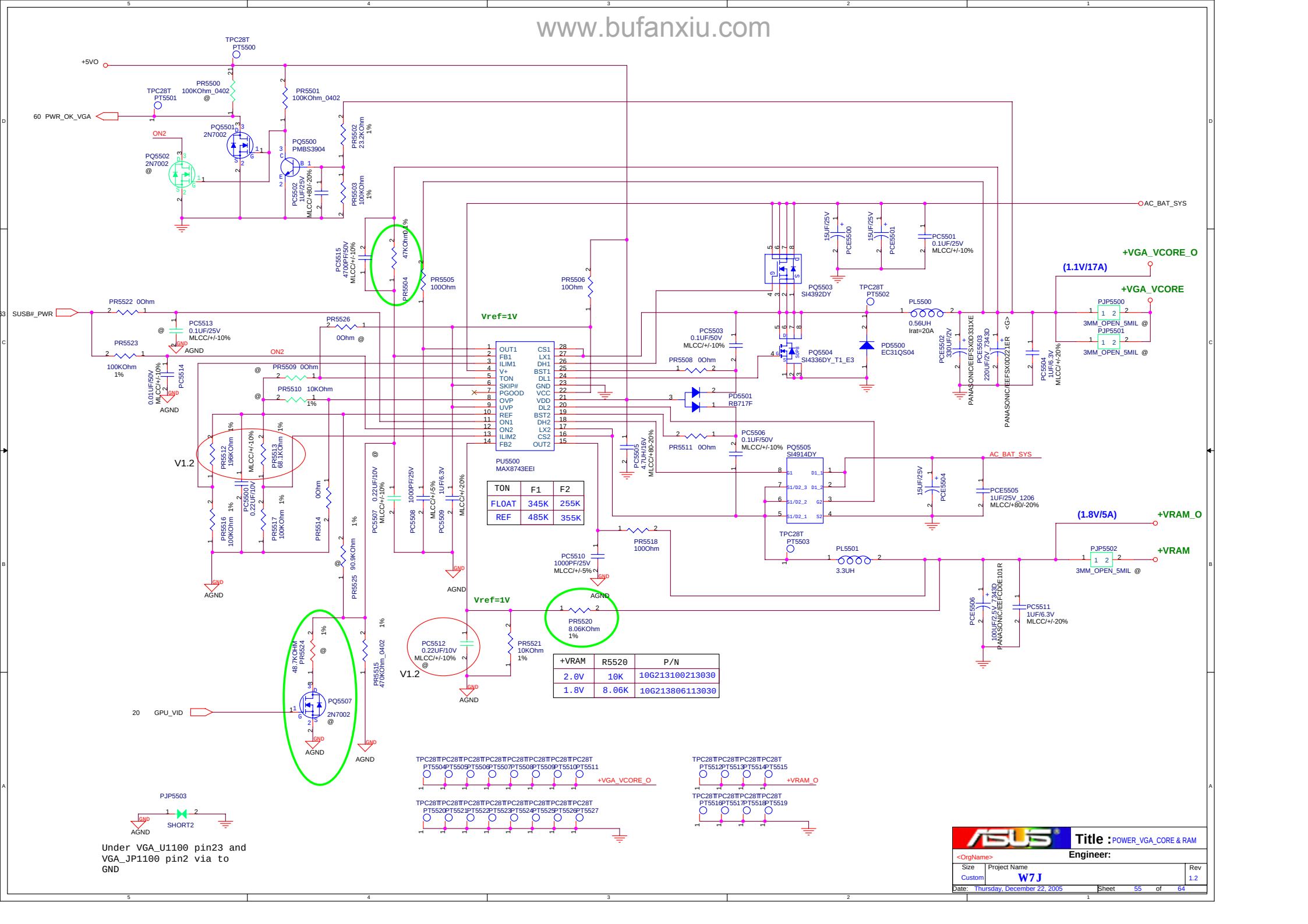




+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 54 of 64	

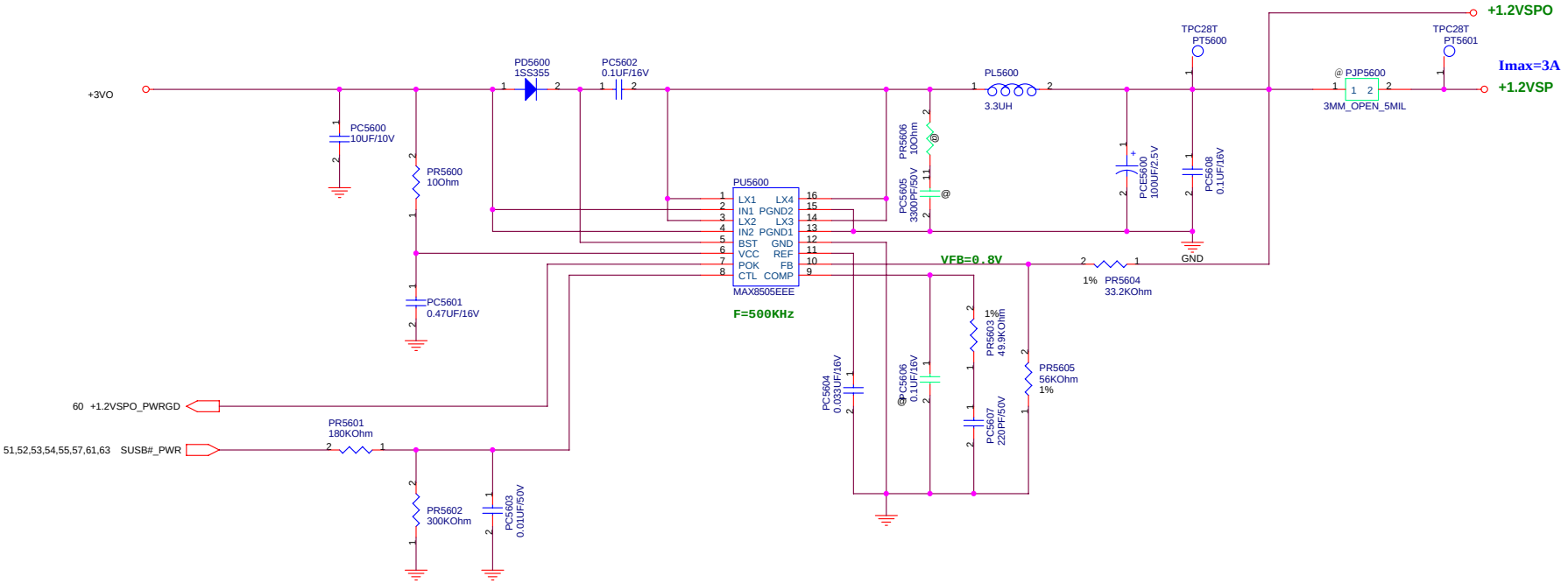


TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

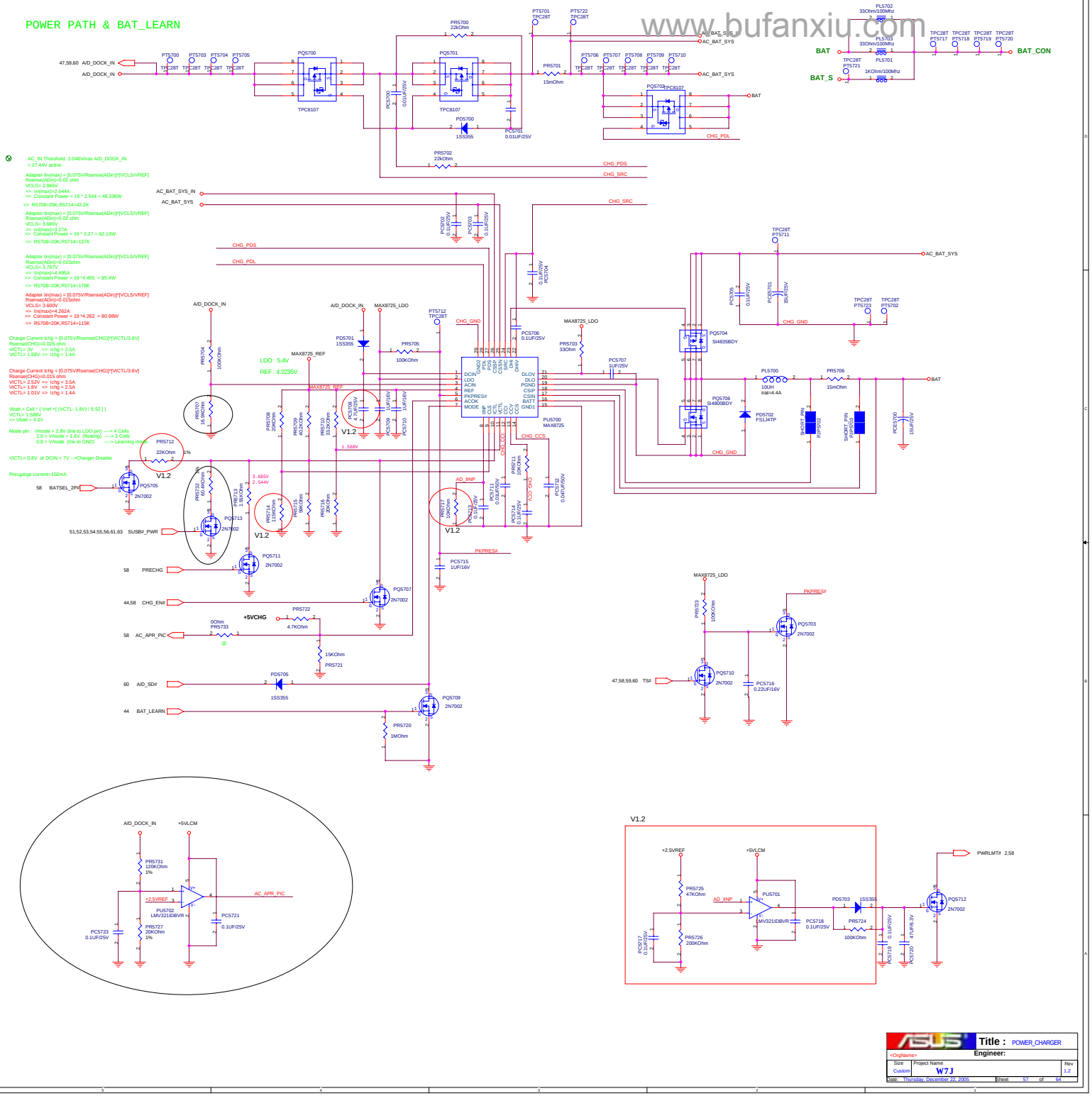
Title :	POWER_VGA_CORE & RAM
<OrgName>	Engineer:
Size: Custom	Project Name: W7J
Rev: 1.2	
Date: Thursday, December 22, 2005	Sheet 55 of 64

+1.2VSP

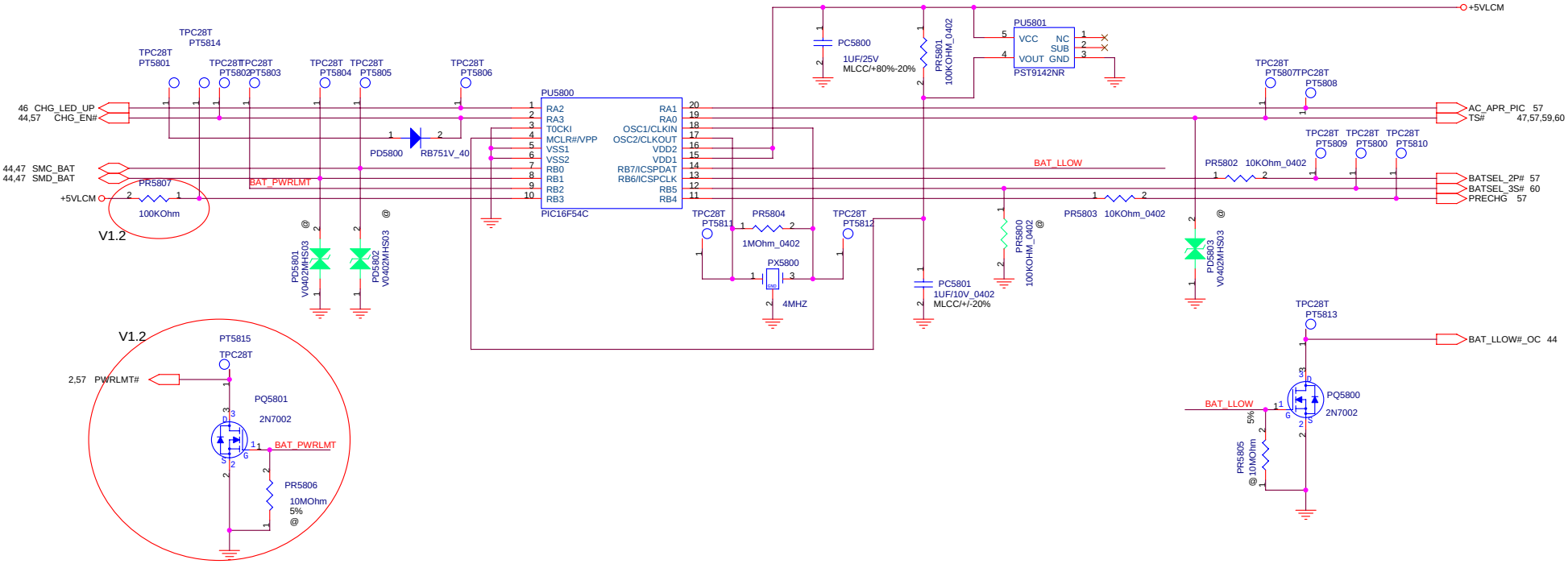


Title : POWER_VGA_+1.2VSP		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 56 of 64	

POWER PATH & BAT_LEARN



PIC16F54C



ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
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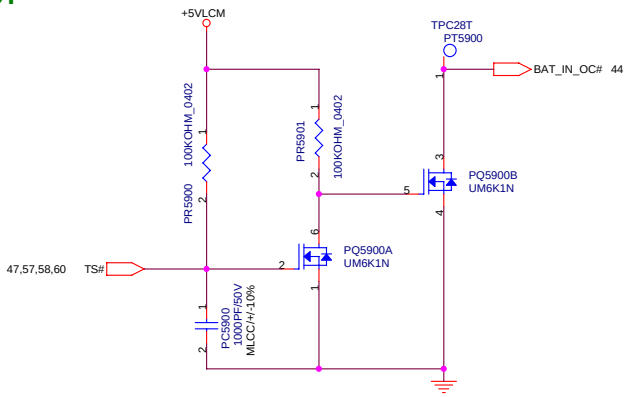
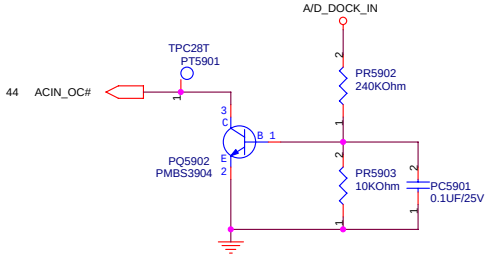
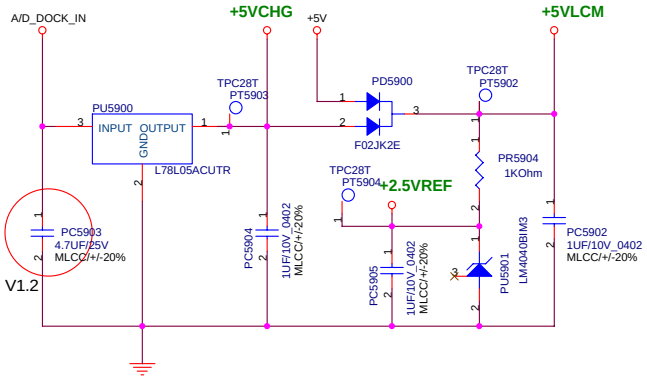
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
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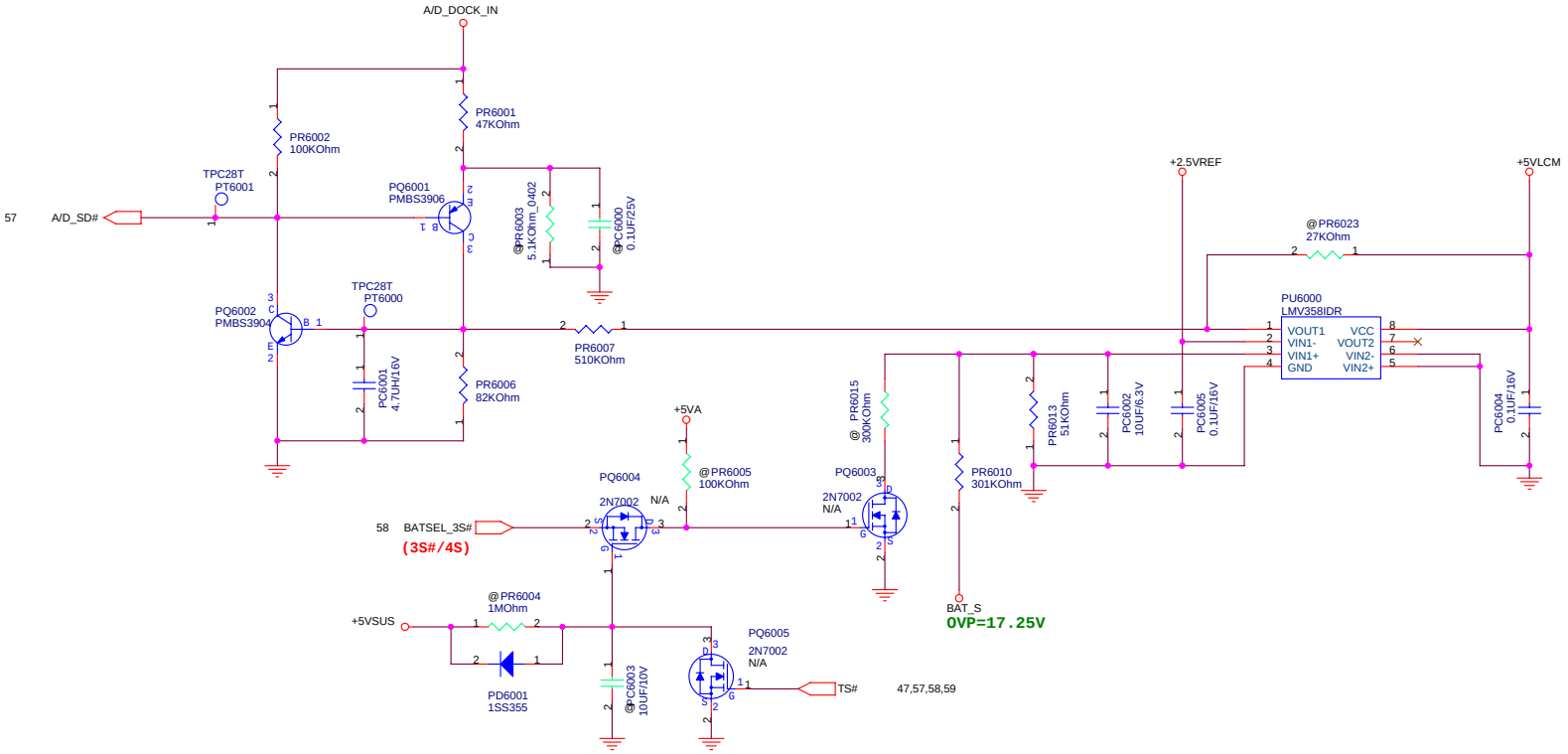
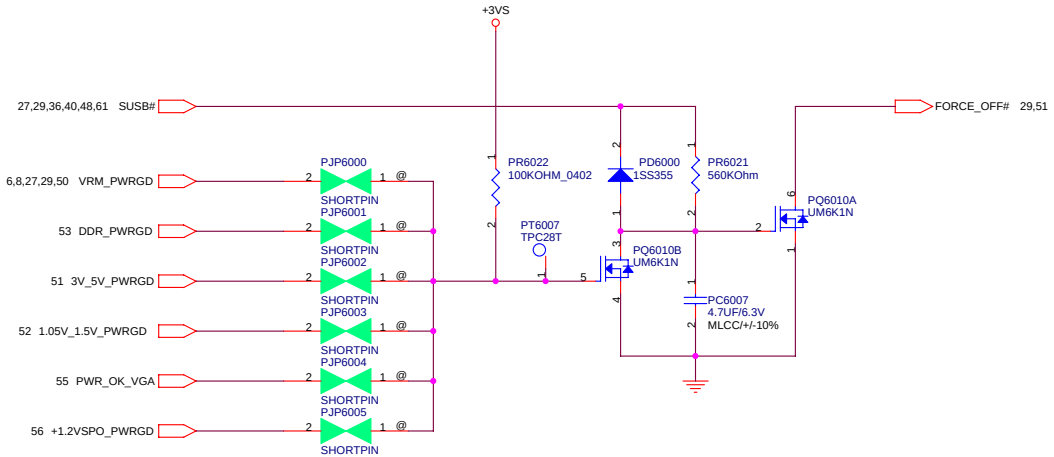
BATTERY A/D_SD# (OVP)



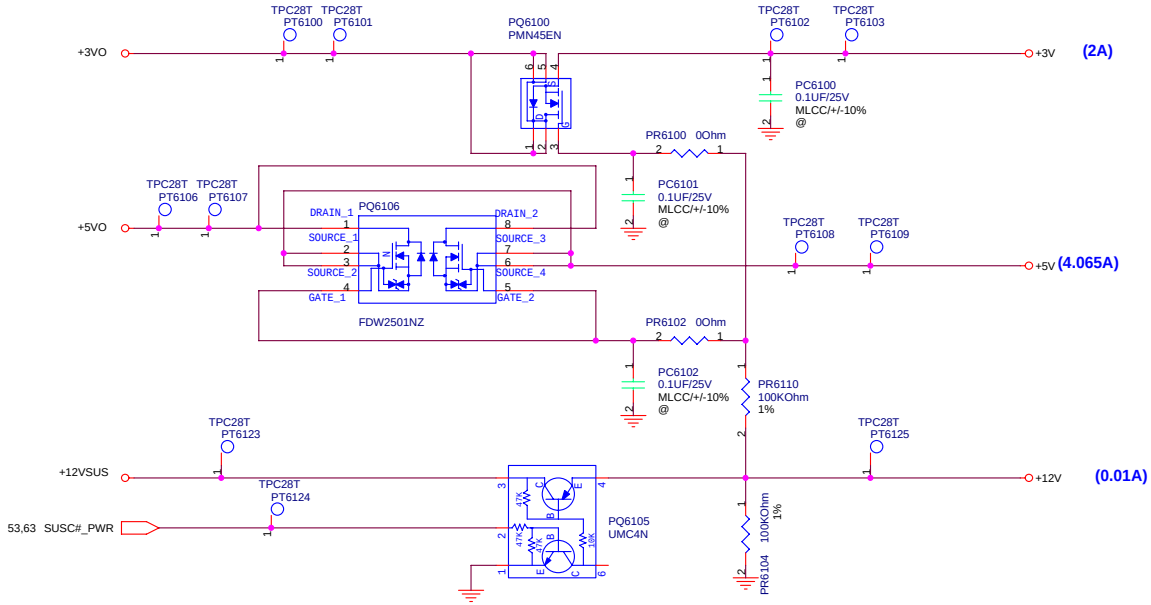
POWER GOOD DETECTER

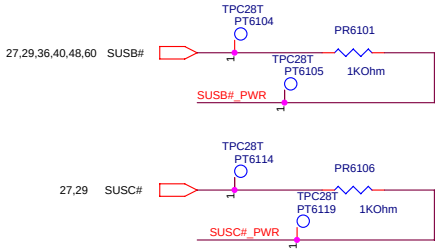


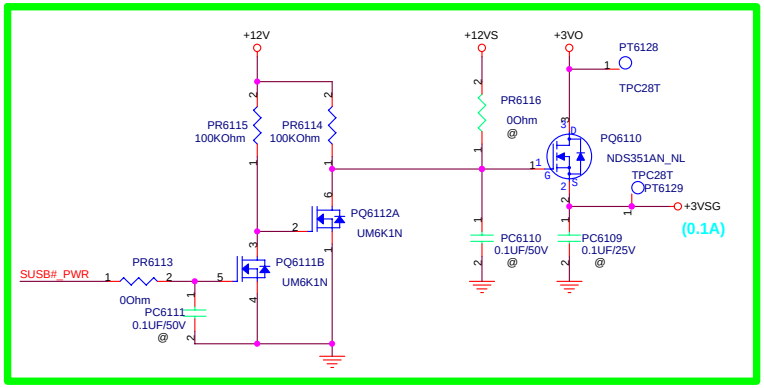
TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.5V_PWRGD

ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 60 of 64	

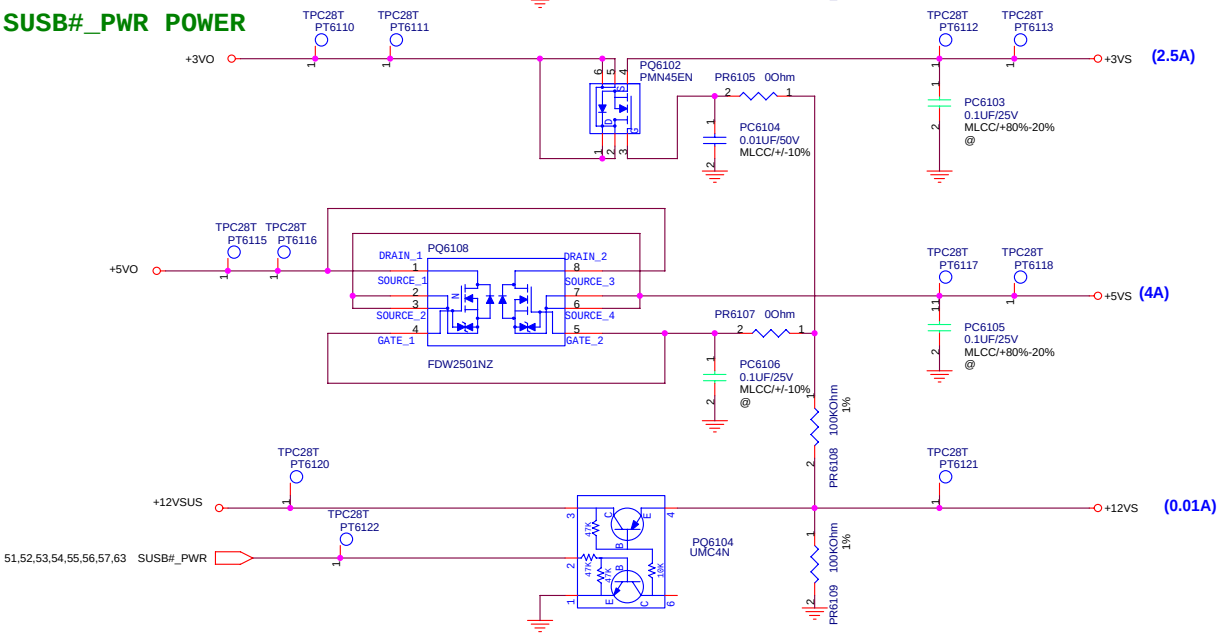
SUSC#_PWR POWER

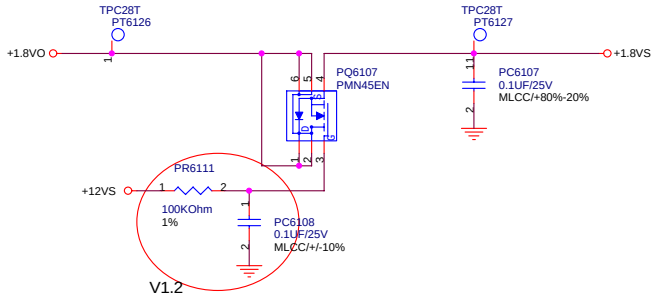




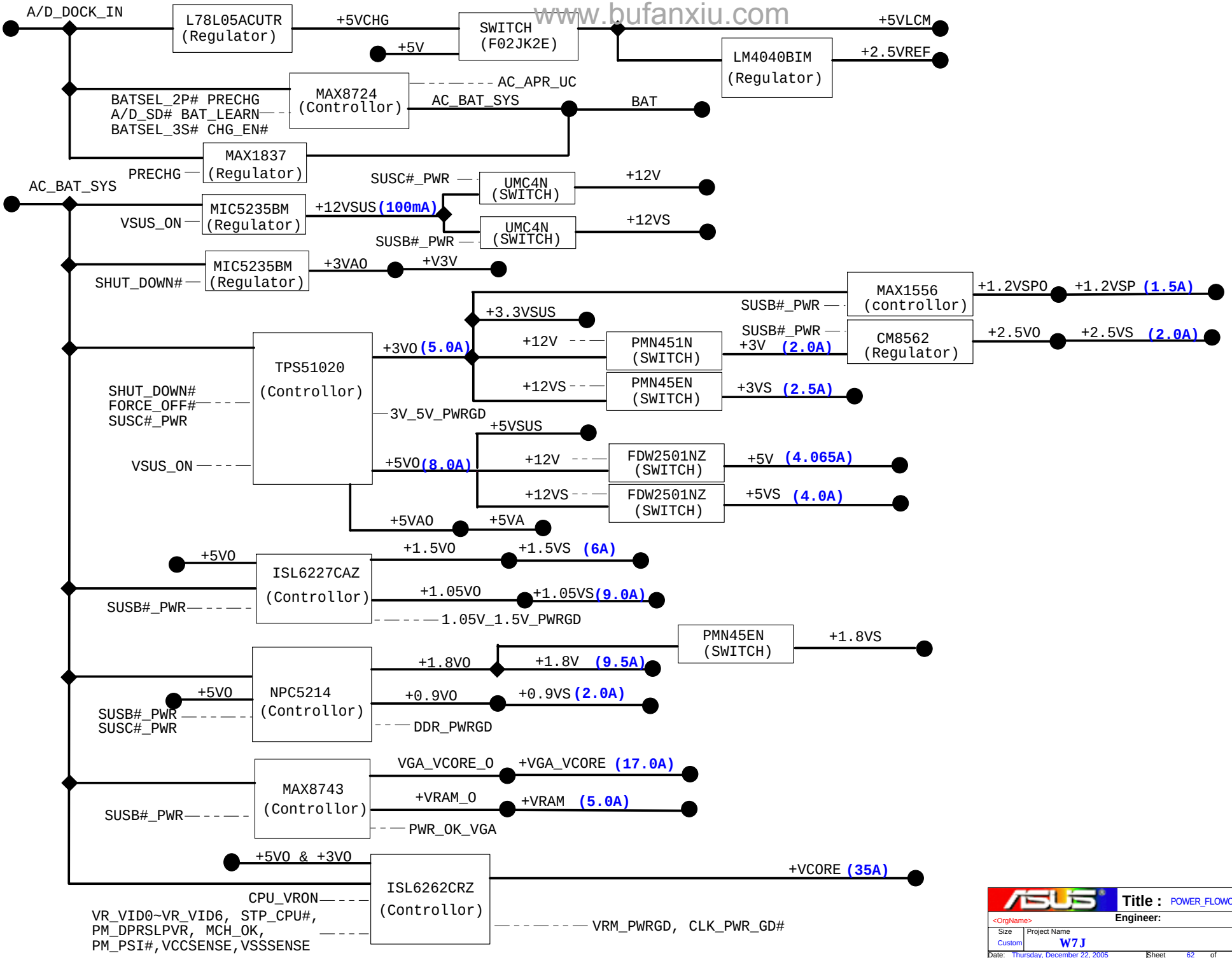


SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 61 of 64	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 62 of 64	

AC_BAT_SYS → AC_BAT_SYS 23,50,51,52,53,54,55,57

+3VA → +3VA 25,29,47,54

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3VSUS → +3VSUS 26,27,28,29,32,38,41,51

+5VSUS → +5VSUS 28,51,60

+3V → +3V 26,29,39,40,41,44,48,54,61

+3VS → +3VS 5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,48,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 27,32,33,61

+12VS → +12VS 5,24,34,46,61

+5V → +5V 16,30,32,37,44,45,46,47,48,59,61

+5VS → +5VS 5,24,28,29,30,32,33,42,43,44,46,47,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 10,20,21,48,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,12,13,14,15,16,48,53

+1.8VS → +1.8VS 20,61

+VCCP → +VCCP 2,3,4,6,7,8,10,11,12,25,28,52

+0.9VS → +0.9VS 16,53

BAT → BAT 57

+5VCHG → +5VCHG 29,57,59

+5VLCM → +5VLCM 23,44,46,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,4,5,44,50

+VGA_VCORE → +VGA_VCORE 17,55

+VRAM → +VRAM 18,19,22,55

+1.2VSP → +1.2VSP 17,18,48,56

BAT_CON → BAT_CON 47,57

FOR POWER TEST

+3VA

PJP6300 (1 2) SGL_JUMP @ → CPU_VRON_PWR 50

PJP6301 (1 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,55,56,57,61

PJP6302 (1 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 53,61

PJP6303 (1 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
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Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/29	1. Change Project name from W6J/H to W7J/F 2. Add NET: PWRLMT# to CPU pin: PROCHOT# (Page 2) 3. Add NET: DREFCLKSS,DREFCLKSS# to CLK GEN: pin17,pin18 (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# to GMCH: C40,D41 (Page 8) 5. Pull high GMCH VCCA_LVDC to +2.5VS (Page 10) 6. Add Jumper at G72M pin: B4 (Page 20) 7. Change R6811 from 200Kohm to 100Kohm (Page 23) 8. Change U57,U58 from 74LVC1G32GV to NC7SZ08M5 (Page 24) 9. Change D2 from EC31QS04 to RB751V_40 (Page 24) 10. Add Double-pi filter in VGA port (Page 24) 11. Swap ICH PCIE lans (Page 26) 12. Change GPIO7 NET from WB_AP to MUTE_POP_ICHGPIO# (Page 27) 13. Add NET: PWR_LED_1HZ to ICH: GPIO13 (Page 27) 14. Add Q6197 in net: PCIE_WAKE# (Page 27) 15. Add Q6192 in net: PWR_SW#_Q (Page 29) 16. Change R719 from 100Kohm to 1Mohm (Page 29) 17. Change R306 from 1Mohm to 10Mohm (Page 29) 18. Change C388 from 0.33uF to 1uF (Page 29) 19. Change Pull-high LID_EC# from +3VSUS to +3V (Page 29) 20. Change Audio CODEC from ADI1986 to ALC660 (Page 30) 21. Change R6614 from 0ohm to 4.7Kohm (Page 32) 22. Change R6616 from 10Kohm to 51KOhm (Page 32) 23. Change R6613 from 0ohm to 4.7Kohm (Page 32) 24. Change R6615 from 10Kohm to 51KOhm (Page 32) 25. Add NET: MUTE_POP_ICHGPIO# to MUTE_POP# circuit (Page 32) 26. Add Q6193 in net: SUSCLK (Page 34) 27. Change SLB9635TT pin16 from PLT_RST# to BUF_PLT_RST# (Page 34) 28. Delete NET PME# (Page 36) 29. Change Pull-high MDIO04 from +3V to +3VS (Page 37) 30. Change Pull-high XD_PWR_EN from +3V to +3VS (Page 37) 31. Change PCIE lans from port 1 to port 2 (Page 38) 32. Add C6625,C6626 in phone connector (Page 39) 33. Change PCIE lans from port 3 to port 1 (Page 40) 34. Add NET: EXPD# to R5538 pin20 (Page 40) 35. Add NET: C_PRESENT# to R5538 pin9,pin10 (Page 40) 36. Change PCIE lans from port 2 to port 3 (Page 41) 37. Change Pull-high 802WLAN_ON# from +3V to +3VSUS (Page 41) 38. Change FWH packaging from PLCC to TSOP (Page 43) 39. Add NET: EXPD# to M38857 P53 (Page 44) 40. Add NET: WB_AP to M38857 P67 (Page 44) 41. Add NET: C_PRESENT# to M38857 P62 (Page 44) 42. Add NET: ACZ_RST#_AUD to M38857 P61 (Page 44) 43. Change U10,U6012 pin4 from SUSC# to SUSC (Page 45) 44. Add Q6196 in net: BTPWRCL# (Page 45) 45. Add R6922 between net: WIRELESS_LAN_ON/OFF# and WB_AP (Page 47) 46. Add Q6198 in +3VS discharge (Page 48) 47. Change Power LED ON circuit (Page 48)

Rev	Date	Description
R1.2	2005/12/20	1. Change R6491 from 23.2KOhm to 51KOhm (Page 5) 2. Add Q6200 at U42 :D2+,D2- (Page 5) 3. Add NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 4. Add RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 5. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 4. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 5. Change R1001 from 1Kohm to C6631:0.1uF (Page 16) 6. Modify LCD enable circuit by U6059 (Page 23) 7. Change L89,L90,L92 to Bead 120Ohm/100MHz (Page 24) 8. Change Q60,Q61 from SI1906DL to SI1902DL (Page 24) 9. Add C6632 in Y1 (Page 25) 10. Connect H_DPRSTP# to PU5000 (Page 25) 11. Change U69 from SN74LVC1G32G to 74LVC1G32GV (Page 26) 12. Disonnect STP_CPU# to PU5000 (Page 27) 13. Add GPIO9:W_OLED# (Page 27) 14. Change R523 from 10KOhm to 100KOhm (Page 29) 15. Change R303 from 10KOhm to C6630:1uF (Page 29) 16. Add R6936 in Net:PWR_SW#_Q (Page 29) 17. Add R6633,R6634,R6635,R6636 in CN20(Page 31) 18. Add R6938 in +3.3Vaux (Page 41) 19. Change CE41,CE5705,CE25 from 100uF to 150uF (Page 45) 20. Add R6937 in BTPWRCL# (Page 45) 21. Change Q6180,Q6181 by Q6202 (Page 46) 22. Add Q6201,LED10 in WIRELESS_OLED# (Page 46) 23. Change R6686 from 0Ohm to 470Ohm (Page 47) 24. Add R6940 in Power Board +5Vs (Page 47)

<Variant Name>

Title : History

ASUSTek Computer INC. NB1 Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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