1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000813234	PRODUCTION RELEASED	2009-11-01

K84 MLB SCHEMATIC

PROD OK2FAB 11/01/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7982	1	SCHEM,MLB,K84	SCH	CRITICAL	
820-2567	1	PCBF,MLB,K84	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K84

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH:

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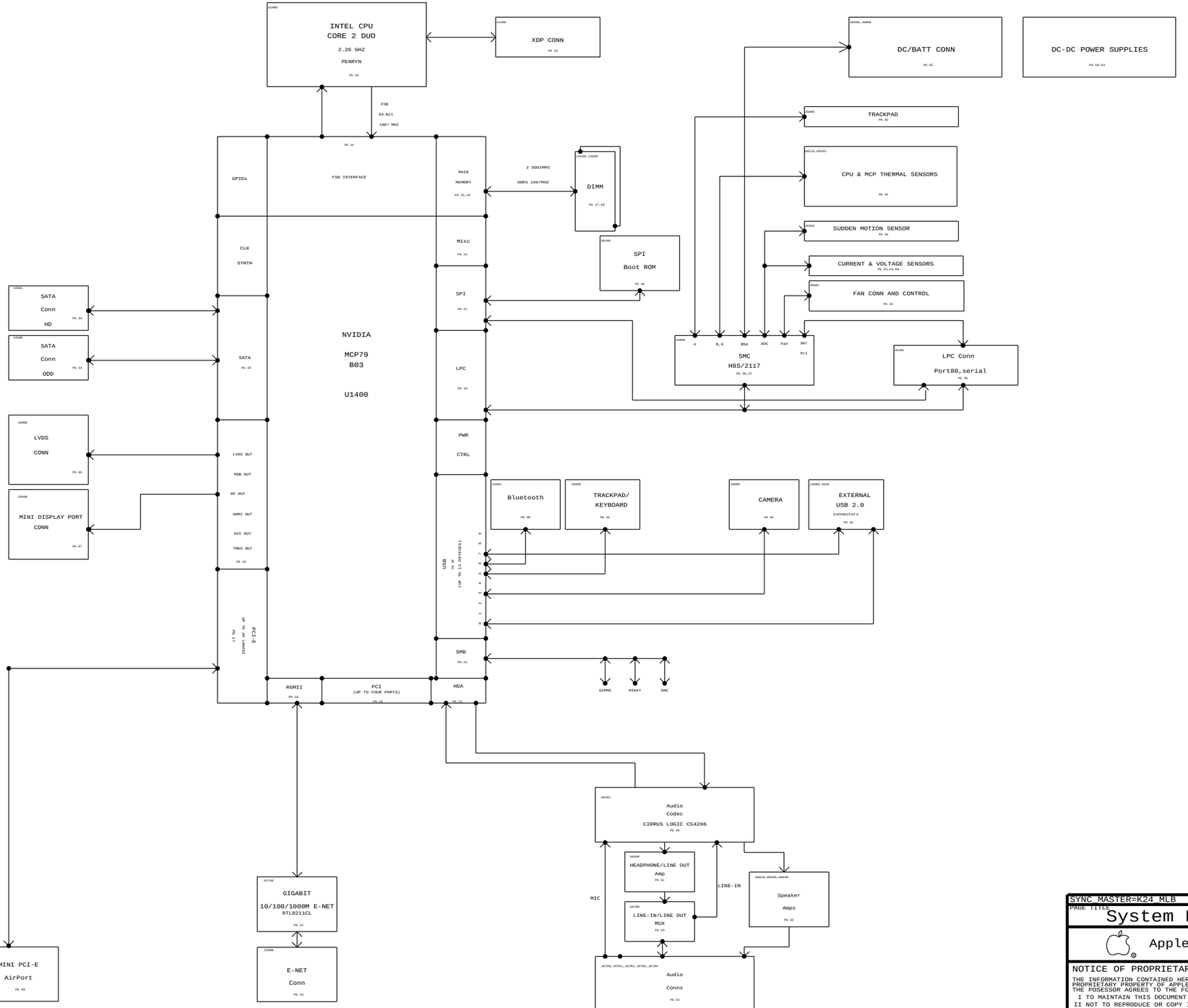

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

BRANCH

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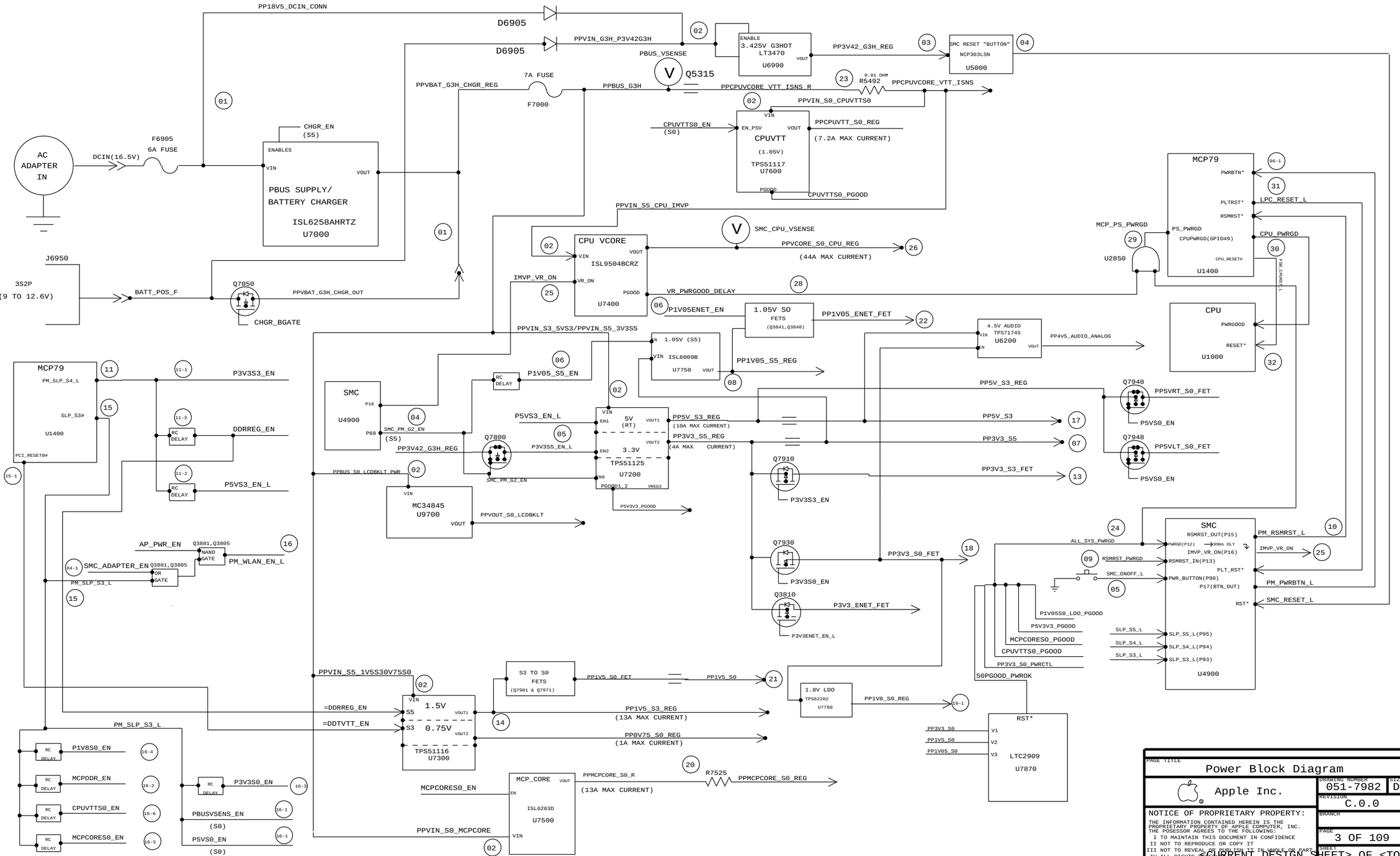
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K84 POWER SYSTEM ARCHITECTURE



PAGE TITLE	Power Block Diagram
	Apple Inc.
DRAWING NUMBER	051-7982
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0035	PCBA,MLB,FOX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,FOX_DDR_CONN,EEE_BCG
639-0254	PCBA,MLB,MLX DDR CONN,K84	K84_COMMON,CPU_2_0GHZ,MLX_DDR_CONN,EEE_A36
085-0748	K84 MLB DEVELOPMENT BOM	K84_DEVEL_ENG
639-0554	PCBA,MLB,FOX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_0GHZ,FOX_DDR_CONN,EEE_CXR
639-0555	PCBA,MLB,MLX DDR CONN,PVT K84	K84_COMMON_PVT,CPU_2_0GHZ,MLX_DDR_CONN,EEE_CY1
085-1076	K84 MLB DEVELOPMENT PVT	K84_DEVEL_PVT

BOM Groups

BOM GROUP	BOM OPTIONS
K84_COMMON	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_ENG,K84_PROGPARTS
K84_COMMON_PVT	COMMON,ALTERNATE,K84_MCP,K84_MISC,K84_DEBUG_PROD,K84_PROGPARTS
K84_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K84_MISC	ONEWIRE_PU,DP_ESD,MIKEY,LDO_NO,MEM_SENSE,1P05_HIGH_SIDE_SENSE,MCP_T_DIODE_SENSOR,MCPSMC_DIGITEMP_YES
K84_PROGPARTS	BOOTROM_PROG,SMC_PROG,WELLSPRING_PROG
K84_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K84_DEBUG_PVT	DEVEL_BOM_PVT,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K84_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K84_DEVEL_ENG	DEBUG_ADC,XDP_CONN,LPCPLUS,VREFMRGN
K84_DEVEL_PVT	XDP_CONN,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3769	1	PDC,SLGVT,2.26,25W,1066,R0,3M,BGA,P75S0	U1000	CRITICAL	CPU_2_0GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03
516S0706	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA	J3200	CRITICAL	FOX_DDR_CONN
516-0201	1	CONN,204P,SODIMM,P=0.6MM	J3100	CRITICAL	FOX_DDR_CONN
516S0790	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,NON/SC	J3200	CRITICAL	MLX_DDR_CONN
516-0213	1	CONN,204P,SODIMM,P=0.6MM,HF	J3100	CRITICAL	MLX_DDR_CONN
452-1708	4	SCR.M1.6X0.35X6.0,D4,HO.3,BLK,M97	SCREW1,SCREW2,SCREW3,SCREW4	CRITICAL	
514-0704	1	CONN,RCPT,RJ45,PLASTIC,HF,K83/K84	J3900	CRITICAL	
514-0705	2	CONN,RCPT,USB,4P,PLASTIC,HF,K83/K84	J4600,J4610	CRITICAL	
514-0706	1	CONN,RCPT,MDP,20P,PLASTIC,HF,K83/K84	J9400	CRITICAL	
514-0718	1	CONN,RCPT,S/PDIF,TX,HF,CFR,K83/K84	J6700	CRITICAL	
353S2718	1	IC,ISL88042,4X V MONTR,2.78/2.86V,TDFN8	U7870	CRITICAL	
870-1885	4	POGO PIN,MED,NOISE-IMPROVED,K84	ZS0900,ZS0901,ZS0902,ZS0903	CRITICAL	
870-1885	3	POGO PIN,MED,NOISE-IMPROVED,K84	ZS0908,ZS0909,ZS0911	CRITICAL	
870-1886	5	POGO PIN,TALL,NOISE-IMPROVED,K84	ZS0904,ZS0905,ZS0906,ZS0907,ZS0910	CRITICAL	
870-1886	5	POGO PIN,TALL,NOISE-IMPROVED,K84	ZS0912,ZS0913,ZS0914,ZS0915,ZS0919	CRITICAL	
870-1887	3	POGO PIN,THIN,NOISE-IMPROVED,K84	ZS0917,ZS0918,ZS0916	CRITICAL	
104S0033	4	RES,MF,1/4W,6.80HM,5%,0805,SMD	R6612,R6617,R6630,R6633	CRITICAL	
518S0774	1	CONN,RCPT,60P,P=0.4,STK HT 1.0	J1300	CRITICAL	XDP_CONN

353S2718 IS NEW INTERSIL PART FOR FIXING B4 DONGLE ISSUE
514-0704 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0692 PART FOR RJ45 CONNECTOR
514-0705 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0689 PART FOR USB CONNECTORS
514-0706 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0691 PART FOR MINI DP CONNECTOR
514-0718 IS CLOUD GREY 4/LB3 PLASTIC W/PDNI PLATING VERSION OF 514-0694 PART FOR AUDIO CONNECTOR

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0748	1	K84 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
085-1076	1	K84 MLB DEVELOPMENT PVT	DEVEL_PVT	CRITICAL	DEVEL_BOM_PVT

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2485	1	IC,SMC,K84	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2487	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K84	U6100	CRITICAL	BOOTROM_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2491	1	IC,WELLSPRING CONTROLLER,K84	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2488

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	DALE/VISHAY, MAGLAYERS AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
138S0603	138S0602		ALL	MURATA AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:BCG]	CRITICAL	EEE_BCG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:A36]	CRITICAL	EEE_A36
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:CXR]	CRITICAL	EEE_CXR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:CY1]	CRITICAL	EEE_CY1

K84 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 4 OF 109

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1/12/2009: INITIAL RELEASE 0.0.1-
- REPLACED K34 REFERENCE WITH K04
- UPDATED SCHEMATIC AND PCB PART NUMBER INFO

1/21/2009: RELEASE 0.0.2-
- DELETED PAGES 41,42,43,48,97,98,105 [FIREWIRE, IR CONTROLLER, BACKLIGHT CKT]
- UPDATED BOM CONFIGURATIONS
- DELETED IR SPECIFIC NETS ON SATA CONNECTOR

1/21/2009: RELEASE 0.0.3
- CORRECTED BOM CONFIG TABLES

1/21/2009: RELEASE 0.0.4-
- CORRECTED BOM CONFIG TABLE (ADDED BACK BKLT ENG)
- ADDED BACK PAGES 97-98 (LCD BACKLIGHT DRIVER AND SUPPORT CKT)
- DELETED BKLT BACKLIGHT DRIVER/DETECTION CKT

1/23/2009: RELEASE 0.0.5-
- UPDATED PAGES 72,73 5V/3.3V & DDR3 POWER SUPPLIES AS PER FLO'S RECOMMENDATIONS
- SET SOURCE SYNC OF AUDIO PAGES (62-63, 65-68) FROM LENG'S AUDIO PAGES

1/27/2009: TMLB FIRST RELEASE 0.0.1-
- NAME CHANGED TO TMLB SO CALLING IT RELEASE 0.0.1
- UPDATED SCHEM AND PCBF PART NUMBER INFO
- UPDATED BOM OPTION TABLE TO REFLECT K04_DEBUG_PROD AND BLANK PROGRAMMED PARTS. ALSO, DELETED BMON_ENG BOM OPTION
- PAGE 34: REMOVED BMON_ATMEL CIRCUIT
- REMOVED ALL SPECIFIC NETS (PAGE 34 & 52)

2/5/2009: RELEASE 0.0.2
- COPIED TMLB OVER TO PLB AS K84 WILL BE PENRYN SKU WHILE K83 WILL BE ATOM SKU
- UPDATED THE SCHEMATICS, PCBF AND CC#s PART NUMBERS INFO
- REPLACED TEXT TMLB WITH PLB THROUGHOUT SCHEMATICS
- PAGE 4: UPDATED BOM OPTION TABLE TO REFLECT K84_DEBUG_ENG FOR K84_COMMON BOM GROUP
- PAGE 4: UPDATED EEE NUMBER - BCG
- PAGE 4: ADDED 005_DEVELOPMENT BOM_VARIANT & K84_DEVEL_ENG, K84_DEVEL_PVT BOM_GROUPS
- PAGE 8: DELETED IR_RX_OUT, PPSV_S3_IR & ADDED ANDED, SMC_KBDLED_PRESENT_L
- PAGE 8: DELETED FIREWIRE, IR AND BMON SPECIFIC NETS
- PAGE 8: DELETED R8959 PCIE_FW_PRSNT_L 'S PD_RESISTOR
- PAGE 9: ADDED UNUSED FIREWIRE, IR, ANE NETS AS TEST POINTS
- PAGE 11: CHANGED ALIAS OF FW_PWE_L TO FP_FW_PWE_L
- PAGE 52: ADDED SMC_KBDLED_R_ALIAS
- PAGE 59: REPLACED CPUTHERM, THERMAL SENSORS U5515 ANDB U5535 WITH THE CHEAPER VERSION APNB 353S2573
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7280 & C7240 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS
- PAGE 72: REPLACE Q7220 WITH SI4770DDT
- PAGE 73: REPLACE 16V INPUT SIDE CAPS C7331 WITH 39UF APN 128S0248 AS PER DAYU'S RECOMMENDATIONS

2/6/2009: MAJOR RELEASE 0.1.0
- NO CHANGES SINCE LAST MINOR RELEASE 0.0.2

2/6/2009: WEEKLY RFA MOM RELEASE 0.1.0
- NO CHANGES SINCE LAST RELEASE 0.1.0

2/15/2009: RELEASE 2.0.0 (WEEKLY RFA)
- PAGE 4: ADDED TWO ALIASES OF PPBUS (PPBUSA G3H & PPBUSB G3H). PPBUSA G3H FEEDS CORE REGULATORS: CPUVTT, MCP VCORE, CPU VCORE & DDR, ALSO, ADDED SENSE RESISTOR ON PPBUS
- PAGE 8: ADDED TWO ALIASES OF PPBUS (PPBUSA G3H & PPBUSB G3H). PPBUSA G3H FEEDS CORE REGULATORS: CPUVTT, MCP VCORE, CPU VCORE & DDR, WHILE PPBUSB FEEDS 5V/3.3 V SUPPLY, LCD BKLT & PPBUS VOLTAGE SENS
- PAGES 33: REPLACED ATPBRT CONNECTOR WITH THE CHEAPER VERSION APN 922S0019 AND UPDATED CONNECTIONS ACCORDINGLY
- PAGE 34: REPLACED ATPBRT CONNECTOR WITH PN 922S0019 AND UPDATED CONNECTIONS ACCORDINGLY
- PAGE 35: REPLACED SATA HDD CONNECTOR WITH APN# PN 616S0349
- PAGE 49: REPLACED ODD CONNECTOR WITH APN 515S0511 FOR SIO
- PAGE 49: REPLACED ESD DIODES WITH CHEAPER PN 377S0059
- PAGE 50: ADDED PP5V_S0_DEBUG_SENSE - TO PD'S U6800/CPU VCORE_HIGH SIDE CURRENT SENSE AND MCP MEM VDD CURRENT SENSE CIRCUITS FOR DEVELOPMENT BOM
- PAGE 4: ADDED DEBUG_SENSE BOM OPTION TO THE K84_DEVEL_ENG BOM GROUP
- PAGE 60: RENAMED PP1V5_S3 TO PP1V5_S3_LDO_R, PP3V3_S3 LDO_R, PP3V3_S3_LDO_R, PP3V3_S3_IPD_R AND PP3V3_S3_IPD_RESPECTIVELY TO MATCH WITH NEW ADDED PAGE 60 NET NAMES.
- ADDED PAGE 65 AND COPIED OVER ZEPHYR2 SCHEMATICS PAGE FROM M97 TPD_FLEX_WILDSPRING. DELETED THE TPD_BOARD CONNECTOR. CALLING IT WELLSPRING `3
- REPLACED THE CHEAPER VERSION APN 922S0019 OF THE BIL CONNECTORS ACCORDINGLY WITH PN 519S0540 AND BIL CONNECTOR WITH PN 519S0538
- POWERALIAS OVERHAUL - PPBUS INTO TWO BRANCHES - "PPBUSA & PPBUSB". ADDED SENSE RESISTOR R7888 (2 MOHMS) ON PPBUSA. ALSO ADDED INA210 AMPLIFIER CKT ACROSS SENSE LINES. ADDED PP3V42_G3H_PPBUSAISNS (IN210
- PAGE 56: UPDATED THE CIRCUIT TO REFLECT THAT OF FREESCALE PART'S SIMILAR TO K19I
- PAGE 59: MOVED THE DECAP R5908 TO CORRECT PART U6901-5 (SIMILAR TO K24)
- PAGE 47: REMOVED BKLT_ENABLE BOM OPTION

PAGES SYNC'ED FROM LENG OOI'S AUDIO_MLB SINCE LAST RELEASE 1.0.0
1. REPLACED MIKEY CD3272 WITH CD3282
2. ADAPT JACK INSERT DETECT CIRCUIT TO CD3282 JACK INSERT DETECT FUNCTION.
3. REMOVED JACK EXTRACT CIRCUITRY, FUNCTION IS TAKEN OVER BY CD3282
4. DELETED NET FANTENNA

PAGES SYNC'ED FROM K24 SINCE LAST RELEASE 1.0.0
- PAGE 7: RCE VCORE INDUCTOR CHECK FOR DO: CHANGED L7560 TO 152S0966 AND THEN TO 152S0867. BUT NOW IT IS BACK TO 13A PART FOR NOW
2. ADDED 'DIDT TO ALL THE DATE AND PHASE NETS

2/25/09: WEEKLY RFA RELEASE (3.0.0)
- ADDED DIDT ATTRIBUTE
- PAGE 4: REMOVED SUPERCAP NO BOM OPTION. ADDED DEBUG_ADC BOM OPTION UNDER K84_DEVEL_ENG
- (THIS IS FOR NEW SENSOR PART NO)
- PAGE 4: CORRECTED APN - FOR PROGRAMMED PARTS - SMC, BOOT ROM, WELLSPRING
- PAGE 8: REMOVED LDO_YES BOM OPTION
- PAGE 8: DIVIDED PP5V_S0 FET INTO TWO BRANCHES - PP5VRT_S0_FET & PP5VLT_S0_FET (FOR ROUTING PURPOSE, PP5V_S3 IS DIVIDED INTO RT AND LT POWER SUPPLY AND WILL HAVE CORRESPONDING S0 FETS)
- PAGE 8: DIVIDED PP5V_S3 REG INTO TWO BRANCHES - PP5VRT_S3_REG & PP5VLT_S3_REG
- PAGE 8: ADDED PP5V_S3_DEBUG_SENS ALIASES FOR NEW SENSOR PAGE 60
- PAGE 8: ADDED PP3V3_S3_BT ALIAS FOR BLUETOOTH ON RIGHT CLUTCH CONNECTOR PAGE
- PAGE 8: ADDED ALIAS PP5VIN_S3_5V_S3 AND PP5V_S3
- PAGE 8: ADDED ALIAS PP5VLT_S3_VSIN UNDER PP5VRT_S3_REG
- PAGE 10: REMOVED BTC_POWER_YES AND SUPERCAP_NO BOM OPTION FROM R2820
- PAGE 34: SINCE K16 AIRPORT CARD SOLUTION IS BEING USED, PART_S3_WLAN IS DECLARED BY PP3V3_S3_WLAN
- (GOING TO 0335U) ALSO, REPLACED PP5V_WLAN WITH PP3V3_WLAN_PM PAGE 5 (FUNCTIONAL TEST POINTS)
- PAGE 34: R3453 IS MODIFIED TO 110K RESISTOR. R3454 IS NOSTUFF AND R3453 IS PULLED UP TO PP3V3_WLAN_F.
- THIS IS TO CREATE 3.3V +/-5% DELAY AND DELAY SPEC BETWEEN 3.3V POWER
- RAIL AND THE CARD BEING STABLE AND AIRPORT GETTING OUT OF RESET
- PAGE 34: DISCONNECTED PP5V_S3_WLAN_PM FROM THE CONNECTOR AND REPLACED IT WITH PP3V3_S3_BT
- (SIMILAR TO H06 CAMERA SIGNALS ARE ROUTED VIA LVDS CONNECTOR - MOVED PP5V_S3 BT CAMERA POWER CIRCUIT
- ALONG WITH THE USB CAMERA SIGNALS AS IT IS REDUNDANT
- PAGE 34: ADDED SENSE RESISTOR R3452 ON PP3V3_WLAN SIGNAL
- PAGE 34: ADDED CHOKE ON WLAN INDUCTOR SIGNAL - PLACED 0603 PART - APN 359S0367
- PAGE 39: REPLACED ETHERNET CONNECTOR WITH APN 514-0668 (SIMILAR TO K36B)
- PAGE 45: XDBNEED PART - HDD CONNECTOR - APN 518S0618
- PAGE 50: ADDED PP5V_S0_DEBUG_SENS ALIASES FOR NEW SENSOR PAGE 60
- PAGE 58: UNSTUFFED R8447 AND ADDED R8448 (SMC_KBDLED_PRESENT_L) AS PER THIS PAGE 54
- PAGE 85: DELETED 9500 CONNECTOR (CONNECTED TO HEAT-PIPE TEMPERATURE DETECTION RAILS)
- PAGE 86: REMOVED U8535 & U8538 WITH CHEAPER APN 353S2571
- PAGE 88: REMOVED WELLSPRING 3 PAGE (GOING BACK TO K24 SOLUTION) AND REPLACED IT WITH K19I DEBUG SENSOR PAGE (SCHUTIL SYNC)
- PAGE 89: REMOVED TEST SIGNALS NOT USED WITH CHANGES ON PAGE 51
- PAGE 89: ADDED BOM OPTION NOSTUFF TO R8080_FOR_NOW
- PAGE 89: DELETED TEST SIGNALS - (NOSTUFF R8080)
- PAGE 89: REPLACED BATTERY CONNECTOR J6950 WITH APN 518S0630 (M96) CONNECTOR
- PAGE 89: ADDED BYPASS 0 OHMS RESISTOR FOR PROTECTION FOR THIS CHIP WHICH WON'T REQUIRE U7060 SOLUTION
- PAGE 77: ADDED NEW PAGE FOR 005 CPU REG POWER SUPPLY - UPDATED ALL THE REF DES AS PER THE PAGE NUMBER
- PAGE 72: REPLACE 16V INPUT SIDE CAPS C7280 WITH 39UF 16V OSCON CAP (APN 128S0248) & C7240 WITH 39UF (APN 128S0248)
- PAGE 712: CHANGED C7480 TO 39UF OSCON CAP (APN 128S0248)
- PAGE 72: REPLACE Q7220 WITH SI4770DDT AND Q7240 WITH SMALLER 10A PART (APN 152S0778)
- PAGE 73: ADDED SENSE RESISTOR R7380 ON 1.5V DDR3 SUPPLY RAIL
- PAGE 77: REMOVED 1.05V S0 PLL LDO - DELETED LDO_NO BOM OPTION FROM R7745
- PAGE 75: CHANGED C7571 & C7560 TO 68UF OSCON CAPS (APN 128S0225)
- PAGE 77: ADDED PP5VRT_S3_EN (RT POWER SUPPLY ENABLE) AND ADDED R7814, C7814 S3 ENABLE CIRCUIT
- FOR GENERATING PSVLT33_EN ENABLE SIGNAL FOR LT POWER SUPPLY
- PAGE 78: ADDED PSV_LT33_PGOOD POWER GOOD SIGNAL (WIRED AND WITH OTHER S0 RAILS PGOOD) CORRESPONDING TO 5V LT
- POWER SUPPLY
- PAGE 78: ADDED 0 OHM ISOLATION RESISTORS ON POWER GOOD SIGNALS (BEFORE WIRED_AND)
- PAGE 79: ADDED 5V LT_S0 FET AND UPDATED NET NAMES FOR BOTH RT AND LT S0 FET SWITCHING ACCORDINGLY
- PAGE 80: UPDATED LVDS CONNECTOR PINOUT AND SIGNALS AS PER H06 IMPLEMENTATION - ADDED CAMERA SIGNALS
- PAGE 97: ADDED BOM OPTION - NOSTUFF - TO R9702 AS PER K19I
- PAGE 8: DELETED PP5V_S0_MCP_PLL_VLDO, PP3V3_S0_MCP_PLL_UF_R TO PP1V05_S0_MCP_PLL_VLDO
- PAGE 8: DELETED PP1V5_S0_MCP_PLL_VLDO, PP3V3_S0_MCP_PLL_UF_R TO PP1V05_S0_MCP_PLL_VLDO
- PAGE 8: RENAMED PP1V5_S3_1V5S3_R7550 TO PPVIN_S5_1V5S30V7S50
- PAGE 28: DELETED FW_RESET_L SIGNAL
- PAGE 28: DELETED FW_BKLT_ENABLE
- PAGE 60: UPDATED WLAN DIVIDER CIRCUIT WITH 3V3 POWER RAIL INSTEAD OF 5V
- PAGE 60: UPDATED WLAN SUPPLY WITH CORRECT NET NAMES REFLECTING 1.5V/0.75V INSTEAD OF 1.8V/0.9V AND
- 4N SYNC WITH PAGE 8 ALIASES
- PAGE 4: REMOVE 1525U0778 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE SINCE L7260 AS HAS BEEN REPLACED WITH THIS PART
- PAGE 4: REMOVED 104S0018 ALTERNATE PART ENTRY FROM THE ALTERNATE PARTS TABLE

PAGES SYNCED FROM K24 SINCE LAST RELEASE 2.0.0
- PG 50: SWAPPED THE PART NUMBER AND THE ALTERNATE PART NUMBER FOR VR5020. MADE ISL60002 THE ALTERNATE PART

PAGES SYNCED FROM LENG OOI'S AUDIO_MLB SINCE LAST RELEASE 2.0.0
- CHANGED SPEAKER AMPS TO LM48310, PLACEHOLDERS FOR LM48311. LM48311 IS THE CSP VERSION OF THE LM48310.
- ADDED 10 UF CAPS
- REMOVED OPTIONAL STUFFING RESISTORS AROUND THE RE-TASKING JACK ANALOG SWITCH.

2/26/2009: RELEASE 4.0.0 (RFA RELEASE):
- PAGE 4: ADDED LDO_NO BOM OPTION
- PAGE 8: RENAMED PP1V05_S0_MCP_PLL_DCK TO __PP1V05_S0_MCP_PLL_UF_R
- PAGE 8: ADDED PP3V3_S0_MCP_PLL_VLDO, PP3V3_S0_MCP_PLL_VLDO
- PAGE 34: ADDED NOTE FOR CONNECTOR WITH PART NUMBER 922S0025 CONNECTOR
- PAGE 34: ADDED NOTE WITH REGARD TO 100 MS DELAY REQUIREMENT BETWEEN 3.3 WLAN
- POWER GETTING STABLE AND AIRPORT CARD COMING OUT OF RESET
- PAGE 34: ADDED NOTE ON AMPN AND SWPN
- PAGE 57: REPLACED KEYBOARD CONNECTOR WITH APN 518S0738
- PAGE 57: REMOVED BACK_DOOR_DETECT_L SIGNAL
- PAGE 90: REFRESHED THE SYMBOL OF U9060, PART NUMBER CHANGED TO 353S2603

3/4/2009: RELEASE 5.0.0 (RFA)-
- PAGE 34: ADDED A TEXT NOTE THAT J3401 (AIRPORT CONNECTOR) COULD CHANGE TO 1.8MM_HEIGHT APN 516S0582
- PAGE 57: REPLACED KEYBOARD CONNECTOR WITH THAT OF K24 (APN 518S0637) - SYNC'ED FROM K24
- PAGE 58: REPLACED BATTERY CONNECTOR WITH THAT OF K24 (APN 518-0591)
- PAGE 60: DELETED NOTE REGARDING INDUCTOR FILTER REQUIREMENT ON BATT_POS_F (AS PER JOHN SCHEN)
- PAGE 78: CHANGED Q7050 TO 376S0761 AS PER DAYU'S K24 DESIGN
- PAGE 79: CHANGED Q7080 AND Q7001 CHEAPER TO 376S0867 (HAT112B) AS PER DAYU'S RECOMMENDATION
- PAGE 79: DISCONNECTED EN_PSV (PIN 34) FROM PSVLTS3_EN SIGNAL AND CONNECTING IT TO
- PPSVLT_S3_VSIN (SVRT PS)
- PAGE 72: L7220 CHANGED TO 152S0778 FOR COST SAVING AS PER DAYU
- PAGE 73: ADDED ONE MORE OSCON 39UF CAP ON INPUT SIDE
- PAGE 73: MOVED THE SENSE RESISTOR NEXT TO INDUCTOR
- PAGE 74: REMOVED UNUSED NETWORK ON U7400 PIN 5 AND PIN 6 AS PER DAYU [R7406, C7410, R7427, R7426]
- PAGE 74: STUFF R7413 AS PER DAYU
- PAGE 74: CHANGED Q7400 AND Q7402 TO 376S0772 AS PER DAYU
- PAGE 74: CHANGED Q7401 AND Q7403 TO 376S0771 AS PER DAYU
- PAGE 74: CHANGED R7525 TO 187S0132 FOR COST SAVING AS PER DAYU
- PAGE 75: DELETING PSVLTS3_EN AS IT IS NO LONGER NEEDED (SEE ABOVE). ALSO UPDATED ASSOCIATED TEXT NOTE
- PAGE 97: FIXED CONNECTION POINT (D01) FOR LCDBKLT VIN
- PAGE 97: ADDED OHMS SERIES RESISTOR ON LCD_BKLT_PWM FOR DEBUGGING PURPOSES
- PAGE 97: RENAMED LCD_BKLT_PWM TO LVDS_TO_BKLT_PWM
- PAGE 97: CHANGED VOVP VALUE TO 8.9V AS PER FREESCALE FEEDBACK
- PAGE 97: ADDED R9720 (22K) AND SWAPPED C9705 AND R9705 LOCATIONS FOR NOISE REDUCTION AS PER FREESCALE RECOMMENDATION
- PAGE 97: DELETED C9713 AS IT IS REDUNDANT
- PAGE 97: ADDED PLACEMENT NOTE ATTRIBUTE TO C9713 AND C9710 FOR PLACING THOSE NEAR L9710

3/20/2009: RELEASE 7.1.0 (MAJOR)-
- PAGE 31 & 32: PIN SWAPS ON THE DDR3 CONNECTOR PAGES FOR ROUTING PURPOSES (REFER TO RON'S EMAIL)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.0.0
- PG: 67, DELETED R6726
- PG: 66, CHANGED C6618/11/30/31 TO 0.015UF
- PG: 66, CHANGED C6619/12 TO LOAD COMPARATOR CKT
- PG: 66, ADDED R6873
- PG: 68, CORRECTED CODEC OUTPUT SIGNALS TABLE COMMENTS

3/24/2009: RELEASE 7.2.0 (MAJOR)-
- PAGE 4: CHANGE THE CPU_TO_NEW_APNB_337S3704
- PAGE 7: DELETED PPBUS_G3H AS NO NEED FOR TWO PPBUS_BRANCHES
- PAGE 8: COMBINED TWO SEPARATE PPBUSA7B BRANCHES INTO ONE =PPBUS_G3H
- PAGE 34: CHANGED J3401 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 45: CHANGED J4501 ROUTING CONNECTIONS AS PER NEW PIN OUT DESCRIPTION FROM DIANA
- PAGE 59: DELETED SMC_PBUSA_ISENSE ALIAS AND STUFFED R5805
- PAGE 64: DELETED U5470 INA210 CIRCUIT AS THERE IS NO NEED
- PAGE 74: REMOVED R7560 SENSE RESISTOR AND RENAMED =PPBUSA_G3H TO =PPBUS_G3H AS NO NEED TO HAVE TWO PPBUS BRANCHES
- PAGE 79: DELETED R7650 CONNECTION BETWEEN CHGR_AGATE AND CHGR_LOWCURRENT_GATE AS PER DAYU
- PAGE 79: ADDED PLACEMENT NOTE TO C7615, C6210 TO 138S0653
- PAGE 76: AS PER DAYU, ADDED
R7951 (6259_YES) CONNECTION BETWEEN CHGR_PIN26 AND CHGR_LOWCURRENT_GATE;
R7952 (6259_NO) CONNECTION BETWEEN CHGR_PIN28 AND GND_CHGR_SGND;
R7953 (6259_YES) CONNECTION BETWEEN CHGR_PIN1 AND PIN 12 (VNST);
R7954 (6259_NO) CONNECTION BETWEEN CHGR_PIN6 AND GND_CHGR_SGND
- PAGE 79: CHANGED C7615 TO 1UF, 25V, X5R, 0402 NET TO VOLTAGE=1.5V
- PAGE 97: STUFF R9716 AS PER KIRAN'S FEEDBACK

3/26/2009: RELEASE 7.4.0 (MAJOR)-
- PAGE 60: REPLACED DUAL PACKAGE OPA330 OPAMPS WITH SINGLE PACKAGE ONES - APN 353S2179
- (U0930, U0931, U0940, U0941 - ALSO, ADDED C6037 & C6041
- PAGE 97: DELETED EXTRA CLEAN UP FOR PIN ZS0912 AND SCREW HOLES Z0908, Z0909

3/26/2009: RELEASE 7.5.0 (MAJOR)-
- PAGE 73: ADDED SHORT XW7304 FROM PIN 1 OF C7300 TO POWER GND (PIN 18)
- PAGE 72: REPLACED C7282 WITH OSCON APN 128S0248 IN PARALLEL WITH C7280 AS PER DAYU

3/26/2009: RELEASE 7.6.0 (MAJOR)-
- ADDED PLACEMENT NOTES TO XW SHORTS AS PER DAYU
- ADDED DIDT=TRUE ATTRIBUTE TO BOOT/VBST SIGNALS OF ALL THE SWITCHING SUPPLIES
- PAGE 8: ADDED PP5V_S3_BT ALIAS AS THERE IS NO BIL CONNECTOR
- PAGE 8: ADDED =PP3V3_S3_BT FOR THE BIL CONNECTOR
- PAGE 8: ADDED =PP3V3_S3_AUDIO AS THERE IS NO BIL CONNECTOR
- PAGE 8: DELETED =PP3V42_G3H_PPBUSAISNS & =PPBUS_SENSE_IDROPLINE HAS BEEN REMOVED
- PAGE 8: ADDED =PP5V_S3_PWRSWSOFT ALIAS, GOING TO 5V RT S0 FET CIRCUITS GOES TO 5V LT S0 FET CIRCUIT
- PAGE 8: ADDED PLACEMENT NOTE TO 1525U0778
- PAGE 9: ADDED ONE MORE ATTRIBUTE TO THE LVDS HOLE
- PAGE 9: ADDED DUAL 12 PIN CONNECTOR, PINOUT FROM J6955, APN 516S0787
- PAGE 60: RENAMED PP1V5_S3_LDO_R TO PP1V5_S3_LDO_RT
- PAGE 60: RENAMED PP1V5_S3_LDO_R TO PP1V5_S3_LDO_LT
- PAGE 60: ADDED PLACEMENT NOTE FOR LOCATION OF 5V S0 FET CIRCUITS TO REFLECT RT AND LT (MATCHES UPDATED ALIASES ON PAGE 8)

PAGES SYNCED FROM CASEY HARDY'S AUDIO_MLB SINCE LAST RELEASE 7.5.0
- PG: 67, ADDED R6725
- PG: 67, ADDED =PP3V3_S3_AUDIO NET
- PG: 67, ADDED XW6702
- PG: 67, ADDED XW6703
- PG: 69, REMOVED PP3V3_S3_ALIAS NOTES
- PG: 69, NO STUFFED R8724

3/29/2009: RELEASE 8.0.0 (RFA)-
- PAGE 7: SCRUBBED THROUGH THE FUNCTIONAL TEST POINTS AGAINST TOM'S SPREADSHEET
- PAGE 7: RENAMED RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 7: DELETED BATT_SIGNAL CONN AND ADDED HALL EFFECT CONNECTOR TEST POINTS
- PAGE 8: DELETED PP3V3_S3_BT ALIAS
- PAGE 8: ADDED TP_ ALIASES FOR - CARDREADER_RESET, USB_CARDREADER_N/P, AND USB_IR_N/P
- PAGE 9: FIXED BAD TP_NC NETS - TP_RTL8211_CLK125, TP_PP3V3_ENET_PHY_VDDREG
- PAGE 34: DELETED 2001Z_NLE MOUNTING HOLE - NO LONGER NEEDED
- PAGE 34: RENAMED TITLE: RIGHT CLUTCH CONNECTOR TO X16 WIRELESS CONNECTOR
- PAGE 56: REPLACED R2930 WITH 1K 1% 1/16W, 0402, 84.5OHM RESISTOR) - PAGE 56: REPLACED R2930 WITH 1K 1% 1/16W, 0402, 84.5OHM RESISTOR)
- PAGE 66: FIXED UNNAMED NETS CONNECTED TO - R6633
- PAGE 74: FIXED UNNAMED NETS CONNECTED TO - XW7401, XW7402, XW7403 AND XW7404
- PAGE 78: FIXED BAD TP_NC NETS -- TP_PDRREG_PGOOD
- PAGE 78: REPLACED L7720 WITH PART NUMBER - APN 152S0518
- PAGE 69: CHANGE PIN OUTS OF J6955 AS PER CHINMAY

3/31/2009: RELEASE 9.0.0 (RFA)-
- PAGE 4,: DELETED DEBUG_SENSE BOM_OPTION AND ADDED MEM_SENSE AND
- 1V05_HIGH_SIDE_SENSE OPTIONS UNDER K84_COMMON BOM_GROUP
- PAGE 4: ADDED MCP_ISENSE_DEBUG BOM OPTIONS UNDER K84_COMMON BOM_GROUP
- PAGE 8: ADDED POPS_PWRSWSOFT_POGO PIN_870-1699_AS ALTERNATE FOR THE MEDIUM ONES
- PAGE 4: UPDATED DESCRIPTION FOR TBTLPP BOM
- PAGE 12: REPLACED C1260 WITH APN 128S0212 AS PER DAYU
- PAGE 12: REPLACED C1260 WITH APN 128S0212 AS PER DAYU
- PAGE 34: ADDED NOTE THAT NOTE FOR ST_CONNECTOR IS TO BE ADDED FOR PP5V_S0 HDD FET
- PAGE 34: ADDED NOTE WITH PIN NAMES AND NETS CONNECTED WITH PP5V_S0 HDD FET
- PAGE 34: ADDED 5 OHMS SERIES RESISTORS BETWEEN SMC_SMBUS CONNECTIONS TO MCP SMBUS 0 - PAGE 34: ADDED 5 OHMS SERIES RESISTORS BETWEEN SMC_SMBUS CONNECTIONS TO MCP SMBUS 0
- ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 34: ADDED BOM OPTION MCPSMC_DIGITEMP_NO TO SMC_ SMBUS 1 CONNECTIONS.
- AND ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0 OHMS
- PAGE 34: ADDED 5 OHMS SERIES RESISTORS BETWEEN SMC_B_SMBUS AND MCP _SMBUS_1
- CONNECTIONS. AND, ASSOCIATED BOM OPTION MCPSMC_DIGITEMP_YES WITH THESE 0
- PAGE 52: ADDED BOM OPTION MCPSMC_DIGITEMP_NO TO R5230 AND R5231
- PAGE 54: REPLACED DEBUG_SENSE BOM_OPTION WITH NEW ONES FOR MEMORY VDD
- PAGE 54: CHANGED R8447 TO 0 OHMS RESISTOR
- PAGE 58: ADDED PLACEMENT NOTE FOR THE SLEEP_HARD_SIDE_SENSE FOR CPU 1.05V AND
- MCP_VDDQ_SENSE FOR MEMORY VDD
- PAGE 59: ADDED MCP_T_DIODE_SENSOR AND STUFFED CS540
- PAGE 72: RENAMED NETS AND NOTES TO REMOVE REFERENCES TO RT POWER SUPPLY
- PAGE 72: ADDED C7260 WITH APN 152S0943 AS PER DAYU
- PAGE 72: ADDED C7282 APN 128S0218 IN PARALLEL WITH C7280 AS PER DAYU
- PAGE 73: REPLACED Q7320 AND Q7321 WITH CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 74: REPLACED C7393 AND C7452 WITH 0.001UF CAPS APN 1525U0325
- PAGE 74: REPLACED C7272 WITH 0.022UF APN 1525U0332 CAP TO INCREASE THE SLEW RATE
- PAGE 75: ADDED A NOTE OF PP3V3_S3 TO R7572
- PAGE 75: REPLACED Q7580 AND Q7565 WITH CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 76: CORRECTED MAX OUTPUT NOTE TO REFLECT 7.2A INSTEAD OF 8A
- PAGE 76: REPLACED Q7620 WITH 2 CSD58858 APN 376S0790 MOSFETS AS PER DAYU
- PAGE 77: ADDED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL VIA A 0 OHM RESISTOR TO PIN 3 (PG) OF THE LDO
- PAGE 78: DELETED PSV_LT33_PGOOD AS THERE IS NO 5V LT POWER SUPPLY ANYMORE
- PAGE 78: RENAMED =PSVRT33_EN TO =PP5V33_EN
- PAGE 78: ADDED P1V05S0_LDO_PGOOD POWER GOOD SIGNAL TO THE WIRED AND CIRCUIT

4/1/2009: RELEASE 9.1.0 (MAJOR)-
- PAGE 4: CHANGED MCP_P/N TO 338S0702 AS PER CHALLEE
- PAGE 52: FIXED SENSOR ADC SMBUS CONNECTIONS (BOTH SCL AND SDA WERE WRONGLY CONNECTED TO SMB_0_S0_DATA NETS
- PAGE 69: REFRESHED HALL EFFECT SENSOR WITH THE NEW SYMBOL
- PAGE 95: REROUTED LED_RDRV_SIGNAL (AS THE POLARITY/CHIP WAS MOVED TO TOP SIDE)
- PAGE 90: ADDED C9017 (1000PF) CAP AS PER JOHN SCHEN
- PAGE 97: FIXED THE LCDBKLT_VIN SIGNAL NAME ASSOCIATION TO THE CORRECT NET INSTEAD OF R9730_PIN
- PAGE 97: DISCONNECTED PGND (PC GREEN) FROM VR9700 AND ADDED A SEPARATE XW9701 SHORT TO ISOLATE NOISY_GND FROM THE SYSTEM GND. NAMED IT LCDBKLT_PGND AND ASSIGNED MIN_LINE_WIDTH ATTRIBUTES
- PAGE 97: RENAMED GND_LCDBKLT TO GND_LCDBKLT_PGND
- PAGE 97: DISCONNECTED PINS 2 AND 5 FROM GND AND TIED (13,19,21) AND CONNECTED SEPARATELY TO SYSTEM_GND
- PAGE 97: REPLACED D9710 WITH 40V PART- APN 371S0580 AS PER DEREK
- PAGE 97: STUFFED R9746 AND SWAPPED C9705 AND R9705 AS PER FREESCALE FOR COMPENSATION - ALSO, CHANGED R9705 TO 10K 1% VALUE - APN 1144S0315

4/2/2009: RELEASE 9.2.0 (MAJOR)-
- PAGE 4: SERVED AS THE UPDATE FROM TOM
- PAGE 49: FIXED PLACEMENT NOTE ASSOCIATED WITH C4907 (SHOULD BE: PLACE NEAR PIN E1)
- PAGE 49: FIXED PLACEMENT NOTES ASSOCIATED WITH R4899,C4928 (SHOULD BE:PLACE NEAR PIN N12) - PAGE 49: FIXED PLACEMENT NOTES ASSOCIATED WITH R4899,C4928 (SHOULD BE:PLACE NEAR PIN N12)
- PAGE 51: FIXED PLACEMENT NOTES ASSOCIATED WITH R4828 - PLACE NEAR PIN AT SMC
- PAGE 52: FIXED DUPLICATION OF RARE_BASE_TRUE ASSOCIATED WITH SMBUS_SMC_B_S0_SCL/SDA
- PAGE 97: RENAMED SINGLE PIN NET GND_LCDBKLT TO GND_LCDBKLT_PGND

Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

4/2/2009: RELEASE 9.3.0 (MAJOR):
- PAGE 4:B ADDED 5.95MM SANYO PART 128S0288 AS ALTERNATE TO 128S0271
- PAGE 4:B ADDED 5.95MM SANYO PART 128S0286 AS ALTERNATE TO 128S0248
- PAGE 4: DELETED 152S0694 ALTERNATE ENTRY FOR 152S0138 AS IT IS NOT USED
- PAGE 50: REPLACED DUAL Q5032 FET WITH TWO SINGLE Q5032 & Q5033 (APN 376S0612) N-CH FETS FOR ROUTING PURPOSES (SIL ANODE SIGNAL)
- PAGE 54:B CHANGED R5412 TO 118OHM (114S0127)
- PAGE 72: ADDED MIN_LINE/NECK_WIDTH ATTRIBUTES TO 5V_S3_DRVL, 3V3S5_VBST, 3V3S5_DRVL (FIXED THE NET NAME- ADDED UNDERSCORE)
- PAGE 75: CHANGED L7560 TO APN 152S0526 - 0.68UH, 3.5MOHM,16A - AS PER DAYU
- PAGE 75: CHANGED R7569 TO 11.3K APN 114S0319 FOR SETTING THE CORRECT OCSET AS PER DAYU
- PAGE 97: CHANGED MIN_NECK_WIDTH ASSOCIATED WITH PPVOUT_S0_LCDBKLT TO 0.24MM AS THAT'S THE PIN WIDTH
- PAGE 97: CHANGED MIN_LINE/NECK_WIDTH ASSOCIATED WITH GND_LCDBKLT_SGND TO 0.670.24MM

PAGES SYNCED FROM DAVID'S AUDIO_MLB SINCE LAST RELEASE 9.2.0
- REMOVED R6725 AND =PP3V3_S3_AUDIO CONNECTION TO MAX14504 ANALOG SWITCH

4/2/2009: RELEASE: 9.4.0 (MAJOR):
- PAGE 97: ADDED A 1000PF CAP (C9727) ON LCDBKLT_VIN NEAR PIN 1
- PAGE 97: REPLACED C9717 WITH 1000PF CAP APN 132S0147 AND ADDED PLACEMENT NOTE AS PER JOHN SCHEN

4/2/2009: RELEASE: 9.5.0 (MAJOR):
- PAGE 9: REPLACED Z0906,Z0907,Z0910 AND Z0911 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584

4/3/2009: RELEASE: 9.6.0 (MAJOR):
- PAGE 4: UNDER K84_PROGPARTS BOM GROUP, REPLACED BLANK P/N WITH PROGRAMMED P/N
- PAGE 8: ADDED GLOBAL_ DIGITAL GROUND NET WITH MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES
- PAGE 9: REPLACED Z0905 AND Z0913 MLB MOUNTING HOLES WITH 2.7 MM DIAMETER PLATED HOLES - APN 998-1584
- PAGE 9: DELETED GND MIN_LINE/NECK_WIDTH AND VOLTAGE ATTRIBUTES FROM FAN STANDOFF

PAGES SYNCED FROM LENG'S AUDIO_MLB SINCE LAST RELEASE 9.5.0*
- REMOVED OPTIONAL STUFF-AROUND RESISTORS FOR ANALOG SWITCH
- CONNECT AUDIO JACK SHIELD TO DIGITAL GROUND.

4/3/2009: RELEASE: 10.0.0 (RFA):
- PAGE 9: ADDED 7 EXTRA TALL POGO PINS FOR EMI - 4 STUFFED AT THE BOTTOM, 3 UNSTUFFED ON THE TOP
- PAGE 28: DELETED MAKE_BASE=TRUE ASSOCIATED WITH PCIE_RESET_L
- PAGE 52: FIXED DUPLICATION OF MAKE_BASE=TRUE ASSOCIATED WITH I2C_MIKEY_SCL/SDA_R
- PAGE 69: REFRESHED J6955 SYMBOL - APN 516S0787
- PAGE 78: DELETED MAKE_BASE=TRUE ASSOCIATED WITH ALL SYS_PWRGD
- PAGE 78: DELETED SYNONYMS AS THEY ARE NOT NEEDED ANYMORE (DUE TO 0 OHMS)

PAGES SYNCED FROM LENG'S AUDIO_MLB SINCE LAST RELEASE 9.6.0*
- ADDED 100PF EMC CAP ON THREE SPEAKER CONNECTORS.
- CHANGED MIN_WIDTH OF CODEC HP OUT NETS.

4/5/2009: RELEASE 10.1.0 (MAJOR):

- PAGE 4: ADDED CHGR_6258 BOM OPTION UNDER MODULE PARTS TABLE AND TO K84_MISC BOM GROUP. THIS IS TO STUFF ISL6258 PART
- PAGE 9: ADDED ONE MORE TALL POGO PIN ON BOTTOM SIDE
- PAGE 13: FIXED THE NOTE ON THE XDP PAGE- REPLACING 920-0620 ADAPTER BOARD WITH 920-0782 ADAPTER FLEX
- PAGE 34: RENAMED P5VWLAN_SS NET TO P3V3WLAN_SS
- PAGE 46: DELETED TEXT NOTE RELATED TO R4691 & R4690 AS IT IS NA TO K84
- PAGE 52: MOVED THE R5251 CONNECTION TO SENSOR ADC TO THE RIGHT SIDE TO SHOW A SEPARATE CONNECTION FOR CLARITY
- PAGE 52: DELETED TEXT NOTE ON BATTERY LED DRIVER AS IT IS NA TO K84
- PAGE 69: PUT R6961 BEFORE C6955 TO GET RC FILTER. ALSO, FOR NOW, REPLACED R6961 WITH A 0 OHM RESISTOR AND NOSTUFF'ED C6955
- PAGE 70: ADDED OMIT BOM OPTION TO U7000 AS THIS PART WILL GET STUFFED WITH EITHER ISL6258 OR ISL6259 DEPENDING UPON PAGE 4 BOM TABLE
- PAGE 70: FIXED Q7001 DRAIN-SOURCE ORIENTATION

4/6/2009 - RELEASE 10.1.1 (MINOR):

SCHEMATIC AND BOM CLEAN-UP
- PAGE 4: DELETED CHGR_6258 AND RENAMED 6259_NO TO CHGR_6259_NO. REPLACED CHGR_6258 WITH CHGR_6259_NO IN MODULE PARTS TABLE
- PAGE 4: DELETED ENTRIES IN THE ALTERNATE BOM TABLE FOR THE FOLLOWING APN: 516-0213 AND 516S0709
- PAGE 8: DELETED =PP3V3_S3_AUDIO ALIAS AS IT IS NO LONGER APPLICABLE
- PAGE 57: DELETED NO_TEST = TRUE ATTRIBUTE FROM Z2_SCLK AND Z2_MOSI AS THEY CONFLICT WITH FUNC_TEST ATTRIBUTE ON PAGE 7
- PAGE 69: RENAMED 6259_NO/YES TO CHGR_6259_NO/YES

4/6/2009 - RELEASE 11.0.0 (OK2FAB):

- NO CHANGE SINCE LAST MINOR RELEASE 10.1.1

4/7/2009 - RELEASE 12.0.0 OK2FAB (RFA):
- NO CHANGE SINCE LAST RFA RELEASE 11.0.0.
THIS IS A RESUBMIT AS PREVIOUS RFA DIDNT GO THROUGH

4/23/2009 - RELEASE 12.1.0 (MAJOR):
- PAGE 4: ADDED METAL PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES- 514-0691 ALTERNATE FOR 514-0690; 514-0689 ALTERNATE FOR 514-0688
- PAGE 13: REPLACED J1300 XDP CONNECTOR WITH MORE ROBUST CONNECTOR APN 998-2515
- PAGE 39: REPLACED J3900 ETHERNET CONNECTOR WITH POR PLASTIC CONNECTOR APN 514-0692
- PAGE 46: REPLACED J4600 & J4610 USB CONNECTORS WITH POR PLASTIC CONNECTOR APN 514-0688
- PAGE 75: CHANGE Q7560 AND Q7565 TO SIS426 APN 376S0749 PER RDAR://6812904
- PAGE 75: CHANGE R7565 TO 1OHM APN 113S0023 PER RDAR://6812904
- PAGE 76: CHANGED THE CPU VTT OVER CURRENT TRIP POINT PER RDAR://6792329 BY CHANGING R7604 FROM 8.87KN) TO 6.04KN)
- PAGE 94: REPLACED J9400 DP CONNECTOR WITH POR PLASTIC CONNECTOR APN 514-0690
- PAGE 75: CHANGED C7565 AND C7568 TO CASE_B4_SM PACKAGE FROM CASE_B2_SM DUE TO PACKAGING ERROR (SAME APN)

4/24/2009 - RELEASE 12.2.0 (MAJOR):

PAGES SYNCED FROM CASEY'S AUDIO_MLB SINCE LAST RELEASE 12.1.0*
- REPLACED J6700 WITH APN: 514-0694
- ADDED DZ 6702 AND L6706
- CONNECTED R6860 TO AUD_IP_PERPH_DET

4/27/2009 - RELEASE 12.3.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED NEW BOM ENTRY 639-0254 FOR MOLEX DDR3 CONNECTOR CONFIG. ALSO, EDITED 639-0035 BOM NAME TO REFLECT FOXCONN DDR3 CONNECTOR. ADDED TWO ENTRIES (J3200 AND J3100) FOR FOXCONN AND TWO FOR MOLEX UNDER MODULE PARTS TABLE .
- PAGE 74: CHANGED C7432 TO 0.001UF AS PER RDAR://6792327
- PAGE 74: UNSTUFFED C7434 AS PER RDAR://6792327
- PAGE 74: CHANGED C7428 TO 0.47UF AS PER RDAR://6792327
- PAGE 74: CHANGED R7415 TO 10.5K AS PER RDAR://6792327
- PAGE 97: CHANGED R9716 FROM 226K TO 243K TO CHANGE THE OVP POINT TO 35.3V AS PER KIRAN

4/28/2009: RELEASE 12.4.0 (MAJOR):

- PAGE 67: ADDED 0603 FERRITE PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER FOR EMI PURPOSES - L6707 & L6708

4/28/2009: RELEASE 12.5.0 (MAJOR):
- PAGE 67: MOVED L6707 & L6708 TO J6703 (FULL RANGE SPEAKER CONNECTOR) BETWEEN CAPS AND CONNECTOR

4/29/2009: RELEASE 12.6.0 (MAJOR & WEEKLY ECO):

- PAGE 67: ADDED 0603 FERRITE PLACEHOLDERS APN 155S0367 ON RIGHT PIEZO SPEAKER J6704 FOR EMI PURPOSES - L6709 & L6710
- PAGE 97: CHANGED L9710 TO A BIGGER 2525 PACKAGE (LOW DCR) APN 152S0585 FOR BETTER EFFICIENCY

4/29/2009: RELEASE 12.7.0 (MAJOR & WEEKLY ECO):
- PAGE 97: CHANGED L9710 BACK TO THE ORIGINAL APN 152S0826 AS 2525 PACKAGE CAN'T FIT IN

5/01/2009: RELEASE 12.8.0 (MAJOR):
- PAGE 4: ADDED A36 EEE NUMBER FOR NEW BOM CONFIGURATION 639-0254
- PAGE 60: ADDED 0 OHMS SERIES RESISTORS R6003 AND R6004 ON AVDD AND DVDD SUPPLY RAILS TO ADC CHIP
- PAGE 60: CHANGED R6001 & R6002 TO 33 OHMS RESISTORS TO FIX UNDERSHOOT ON I2C BUS

05/01/2009: RELEASE 12.9.0 (MAJOR):

- PAGE 4: UPDATED PLASTIC PART ALTERNATES FOR USB AND MINI DP CONNECTORS. ALSO ADDED CORRESPONDING NOTES- 514-0690 PLASTIC ALTERNATE FOR 514-0691 METAL; 514-0688 PLASTIC ALTERNATE FOR 514-0689 METAL

- PAGE 46: REPLACED PLASTIC USB CONNECTORS WITH METAL APN 514-0689 PARTS
- PAGE 94: REPLACED PLASTIC MINI DP CONNECTOR WITH METAL APN 514-0691 PART

05/04/2009: RELEASE 12.10.0 (MAJOR):
- PAGE 4: REMOVED SHORT POGO PIN ALTERNATE
- PAGE 4: REVERTING MCP TO EARLIER USE APN 338S0710
- PAGE 60: CHANGED U6050 INA 211 PART TO 200X GAIN INA 210 APN 353S2073

05/05/2009: RELEASE 12.11.0 (MAJOR & WEEKLY ECO):
- PAGE 4: ADDED 4 QUANTITIES OF DIMM CONNECTOR SCREWS APN 452-1708
- PAGE 46: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH POR IS PLASTIC USB CONNECTOR PART
- PAGE 94: ADDED NOTE ABOUT USING METAL PART'S SCHEMATIC AND CAD SYMBOLS THOUGH POR IS PLASTIC MINI DP CONNECTOR PART

05/08/2009: RELEASE 12.12.0 (MAJOR & WEEKLY ECO):

- PAGE 4: DELETED SANYO 6.00MM OSCON CAPS 128S0248 & 128S0271 FROM THE ALTERNATE TABLE (MAKING ALTERNATES AS PRIMARY)
- PAGE 4: TURNING ON BOM OPTION MCPSMC_DIGITEMP_YES AS POR IS TO CONNECT MIKEY TO MCP79 SMBUS 0 INSTEAD OF SMBUS 1 AND TO CONNECT SMC_B SMBUS TO MCP79 SMBUS 1
- PAGE 4: ADDED A TEXT NOTE STATING THAT ADC CAN ONLY WORK IN S0 STATE AS IT HAS I2C BUS PU TO S0 POWER RAIL
- PAGE 37: CHANGED C3714 AND C3715 TO 2.2UF APN 138S0642 TO FIX ETHERNET JITTER ISSUE
- PAGE 50: CHANGED R5030 TO 63.4 OHMS APN 114S0102 TO INCREASE THE SIL CURRENT PER RDAR://PROBLEM/6752822
- PAGE 50: CHANGED R5714 TO 0 OHM APN 116S0004 PER RDAR://PROBLEM/6752822
- PAGE 52: CHANGED R5200, R5201, R5260 & R5261 TO 2K APN 116S0073
- PAGE 72: REPLACED C7252, C7291 & C7292 WITH 5.95MM SANYO APN 128S0288
- PAGE 72: REPLACED C7240 & C7282 WITH 5.95MM SANYO APN 128S0286
- PAGE 73: REPLACED C7331 & C7345 WITH 5.95MM SANYO APN 128S0286
- PAGE 77: CHANGED C7771 TO 47UF APN 138S0659 TO FIX ETHERNET JITTER ISSUE

05/10/2009: RELEASE 12.13.0 (MAJOR & WEEKLY ECO - THRU' EMAIL):
- PAGE 60: CHANGED R6003 AND R6004 TO 10 OHMS 5% RESISTOR VALUES RDAR://PROBLEM/6834630

05/11/2009: RELEASE 12.14.0 (MAJOR & WEEKLY ECO - THRU' EMAIL):

- PAGE 57 : CHANGED R5714 TO 165 OHMS APN 114S0141 AS PER RDAR://PROBLEM/6875543
- PAGE 72 : CHANGED C7252, C7291 & C7292 BACK TO ORIGINAL APN 128S0271

05/20/2009: AGILE RELEASE PROTO 2 OK2FAB 13.0.0 (FAB):

- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

05/22/2009: AGILE RELEASE PROTO 2 OK2FAB 14.0.0 (FAB)-

RETRY
- FINAL PROTO 2 OK2FAB RELEASE
- UPDATED PAGE BORDERS TO NEW E4 DSIZE STANDARDS

06/09/2009: RELEASE 14.1.0 (MAJOR)-
- PAGE 4: REMOVING CHGR_6259_NO BOM OPTION AS ISL 6259 IS NOT POR
- PAGE 4: ADDED NEW ISL PART APN 353S2718 AS AN ALTERNATE TO FIX B4 DONGLE ISSUE
- PAGE 9: REPLACED ALL MEDIUM POGO PINS WITH APN 870-1794 (2 MM) AND ZS0916-ZS0918 WITH THINBC APN 870-1820 (2 MM) ONES
- PAGE 59: ADDED R5922 10 OHMS SERIES R ON VDD SUPPLY TO FIX SMS NOISE ISSUE
- PAGE 67: CHANGED J6704 TO A THREE PIN CONNECTOR 518S0520
- PAGE 69: REFRESHED J6955 SYMBOL (HALL EFFECT CONNECTOR)
- PAGE 70: REMOVED CHGR_6259_YES/NO BOM ATTRIBUTES AS ISL 6259 IS NOT POR
- PAGE 70: DELETED R7051 & R7053 CHGR_6259_YES BOM OPTIONS COMPONENTS
- PAGE 70: REPLACING R7052 & R7054 CHGR_6259_NO BOM OPTION COMPONENTS WITH XW SHORTS- XW7052 & XW7054
- PAGE 70: REMOVED R7050 CHGR_6259_YES COMPONENT AS IT IS NOT NEEDED WITH ISL 6258 (PM_SLP_S3_L DIRECTLY CONNECTS TO ISL 6258 PIN)
- PAGE 94: STUFFED C9485 AND CHANGED IT TO 22UF (APN 138S0654),CHANGED C9400 & C9481 TO 4.7UF (APN 138S0618) & CHANGED C9480 TO 22UF (APN 138S0654): TO FIX B4 DONGLE ISSUE

PAGES SYNCED FROM CASEY HARDY?S AUDIO_MLB SINCE LAST RELEASE 14.0.0
- ADDED R6862 PULL-UP RESISTOR TO PERPH. DETECT CKT.

06/10/2009: RELEASE 14.2.0 (MAJOR)-

- PAGE 4: ADDED APN 138S0661 LOW NOISE MURATA CAPS AS ALTERNATE FOR C9715 & C9716 TO FIX LCD BKLT AUDIBLE NOISE ISSUE
- PAGE 49: ADDED 0.1UF CAPS ON SMS_X_AXIS, SMS_Y_AXIS & SMS_Z_AXIS NETS TO FIX NOISE ISSUE
- PAGE 77: CHANGED R7780 TO 25.5K APN 114S0354 & R7781 TO 80.6K APN 114S0402 AS PER DAYU

06/11/2009: RELEASE 14.3.0 (MAJOR)-
- PAGE 77: ADDED 0 OHMS BOM OPTIONS R7782 BETWEEN PIN 4 OF U7750 (SKIP PIN) AND POWER RAIL AND R7783 BETWEEN PIN 4 AND GND. R7782 WILL BE NOSTUFF FOR NOW. THIS IS AS PER DAYU TO FIX ETHERNET JITTER ISSUE

06/11/2009: RELEASE 14.4.0 (MAJOR)-
- PAGE 49: REPLACED C4950-C4952 WITH 1UF APN 138S0640 CAPS
- PAGE 78: DISCONNECTED P1V05_S5_PGOOD FROM PIN 3 OF U7840 AND CONNECTED IT TO PIN 1 (RSMRST_PWRGD) TO FIX LEAKAGE ISSUE

06/12/2009: RELEASE 14.5.0 (MAJOR)-
- PAGE 9: ADDED ONE MORE EXTRA TALL POGO PIN AS PER EMC RECOMMENDATION : ZS0920
- PAGE 78: ADDED 0 OHM BOM OPTION R7895 BETWEEN 1V05_S5_PGOOD AND RSMRST_PWRGD FOR DEBUG PURPOSES

06/22/2009: RELEASE 14.6.0 (MAJOR)-

- PAGE 4: ADDED CPU APN 337S3769 AS ALTERNATE TO 337S3704
- PAGE 9: ADDED NOSTUFF BOM OPTION TO ZS0920
- PAGE 50: CHANGED R5030 TO 48.7 OHMS APN 114S0091 (SIL CURRENT TO 12MA)
- PAGE 57: CHANGED R5714 TO 113 OHMS APN 114S0125 (KB LED CURRENT TO 8.5MA)
- PAGE 97: ADDED CRITICAL ATTRIBUTE TO C9715 & C9716
- PAGE 97: CHANGED R9710 TO 7.68K APN 114S0304 (LCD BKLT CURRENT TO 20MA)

06/25/2009: RELEASE 14.7.0 (MAJOR)-

- PAGE 70: DELETED OMIT BOM OPTION FROM U7000 AS ISL6259 HAVE BEEN REMOVED

07/17/2009: AGILE EVT OK2FAB RELEASE 15.0.0 (FAB)-

- NO CHANGES SINCE LAST MAJOR 14.7.0. THIS IS FINAL EVT FAB RELEASE

07/21/2009: RELEASE 15.1.0 (MAJOR)-

- PAGE 4: DELETED MIKEY_LOAD_DET BOM OPTION FROM THE TABLE UNDER K84_MISC CATEGORY AS PER CASEY
- PAGE 4: UPDATED ALTERNATES FOR MINI DP AND USB CONNECTORS WITH PG2 PLASTIC CONNECTORS- APN 514-0706 (MDP) & 514-0705 (USB). AND, UPDATED NOTE BELOW THE ALTERNATES PARTS TABLE ACCORDINGLY
- PAGE 4: ADDED PG2 CONNECTOR APN 514-0704 IN THE MODULE PARTS TABLE FOR RJ45 J3900 CONNECTOR
- PAGE 4: DELETED 353S2310 PART FROM THE ALTERNATES BOM TABLE AS ALL PRODUCTION HAS NOW MOVED TO ITS ALTERNATE PART 353S2718
- PAGE 4: ADDED NEW INTERSIL PART APN 353S2718 IN THE MODULE PARTS TABLE FOR U7870 TO FIX B4 DONGLE ISSUE
- PAGE 21: DELETED NOSTUFF BOM ATTRIBUTE FROM R2143 AS MIKEY_LOAD_DET CIRCUIT HAS BEEN REMOVED. SO R2143 NEEDS TO BE STUFFED NOW
- PAGE 39: ADDED BOMOPTION ATTRIBUTE OMIT TO J3900 AS NEW PG2 CONNECTOR PART HAS BEEN ADDED ON PAGE 4 MODULE PARTS TABLE
- PAGE 78: ADDED BOMOPTION ATTRIBUTE OMIT TO U7870 AS NEW INTERSIL PART PART HAS BEEN ADDED ON PAGE 4 MODULE PARTS TABLE

07/27/2009: RELEASE 15.2.0 (MAJOR)-
- PAGE 4: DELETED LOW NOISE MURRATA CAP ENTRY FROM THE ALTERNATES TABLE
- PAGE 49: CHANGED SMS NOISE FILTERING CAPS C4950-C4952 TO 0.47UF APN 132S0178 TO FIX THE SMART TEST FAILURE
- PAGE 70: DISCONNECTED PM_SLP_S3_L FROM PIN 4 (VREF) AS IT WAS INCORRECTLY CONNECTED, THEREBY CAUSING HIGHER SLEEP/SHUTDOWN POWER
- PAGE 97: NOSTUFFED C9716 AND CHANGED C9715 TO APN 138S0661 AS POR IS TO HAVE SINGLE CAP LOW NOISE MURRATA CAP SOLUTION AS PER ACOUSTICS ENGINEER

08/05/2009: RELEASE 15.3.0 (MAJOR)-
- PAGE 4: ADDED APN 138S0606 (TAIYO-YUDEN) AS AN ALTERNATE FOR APN 138S0602
- PAGE 4: ADDED PDNI PLATED AUDIO CONNECTOR W/ CHAMFER APN 514-0718 AS AN ALTERNATE FOR J6700 APN 514-0694
- PAGE 4: ADDED GOLD PLATED AUDIO CONNECTOR W/O CHAMFER APN 998-2622 AS AN ALTERNATE FOR J6700 APN 514-0694
- PAGE 4: ADDED GOLD PLATED RJ45 CONNECTOR APN 998-2621 AS AN ALTERNATE FOR J3900 APN 514-0704
- PAGE 4: ADDED GOLD PLATED MINI DP CONNECTOR APN 998-2626 AS AN ALTERNATE FOR J9400 APN 514-0691
- PAGE 4: ADDED GOLD PLATED USB CONNECTOR APN 998-2624 AS AN ALTERNATE FOR J4600/J4610 APN 514-0689
- PAGE 4: ADDED LOW NOISE POGO PINS 870-1885 (MEDIUM), 870-1886 (TALL), AND 870-1887 (THIN) AS ALTERNATES
- PAGE 49: CHANGED C4950, C4951, C4952 TO APN:132S0131 (CAP,0402,0.033UF, 16V,10%) AS THESE WOULD BE USED TO ACHIEVE CUT-OFF FREQUENCY OF ~146HZ FOR SMS (AS PER THE VENDOR) AND FILTER THE NOISE TOO AS SEEN BY SMC CHIP. CAPS ON SMS PAGE WOULD BE UNSTUFFED
- PAGE 59: ADDED NOSTUFF BOM OPTION ATTRIBUTE TO C5923-C5925 AS STATED ABOVE. ALSO, EDITED THE NOTE ACCORDINGLY
- PAGE 70: CHANGED R7031 FROM 10 OHM TO 2.2 OHM, 5%, APN:116S0010 TO FIX SLOW CHARGING ISSUE, PER DAYU
- PAGE 70: CHANGED R7047 FROM 10 OHM TO 0 OHM, 5%, APN:116S0004 TO FIX SLOW CHARGING ISSUE, PER DAYU
- PAGE 70: CHANGED C7043 FROM 0.1UF TO 1UF, 10%, APN:138S0640 TO FIX SLOW CHARGING ISSUE, PER DAYU

08/27/2009: AGILE PDFC OK2FAB RELEASE 16.0.0 (FAB)-

- FINAL PDFC (PRE DVT) RELEASE!
- PAGE 97: REFRESHED THE SYMBOL OF C9715 4.7UF APN 138S0661

08/31/2009: RELEASE 16.1.0 (MAJOR)-

- PAGE 4: REMOVED 138S0606 FROM THE ALTERNATES TABLE AS IT DOESN'T PERTAIN TO K84
- PAGE 4: REPLACED CPU APN 337S3704 WITH 337S3769 IN MODULE PARTS TABLE AND REMOVED 337S3704 FROM THE ALTERNATE PART TABLE AS POR IS 337S3769 (P7550)
- PAGE 4: REMOVE 870-1794, 870-1698 & 870-1820 FROM THE ALTERNATES TABLE AS POR IS LOW NOISE POGO PINS
- PAGE 4: ADDED LOW NOISE POGO APNS 870-1885 (IN PLACE OF 870-1794), 870-1886 (IN PLACE OF 870-1698) & 870-1887 (IN PLACE OF 870-1820) IN MODULE PARTS TABLE
- PAGE 4: ADDED NEW INTERSIL ISL6258A (WITH IMPROVED CHARGE CURRENT ACCURACY LIMITS) APN 353S2811 AS AN ALTERNATE FOR APN 353S1832
- PAGE 4: REMOVED 998S APN FROM THE ALTERNATES TABLE PERTAINING TO I/O CONNECTORS AS THEY ARE NO LONGER POR FOR DVT
- PAGE 4: REMOVED 514-0706, 514-0705 AND 514-0718 FROM THE ALTERNATES TABLE AND ADDED TO MODULE PARTS TABLE AS THEY ARE NOW POR I/O CONNECTORS
- PAGE 9: ADDED OMIT BOM OPTION ON ALL THE POGO PINS
- PAGE 46: ADDED OMIT BOM OPTIONS TO J4600 & J4610 USB CONNECTORS
- PAGE 67: ADDED OMIT BOM OPTION TO J6700 AUDIO CONNECTOR
- PAGE 94: ADDED OMIT BOM OPTION TO J9400 MINI DP CONNECTOR
- PAGE 97: UPDATED SCHEMATIC NOTE RELATED TO TARGET AND ACTUAL ISET & OVP NUMBERS AS PER KIRAN'S EMAIL

09/16/2009: RELEASE 17.0.0 (FAB)-

- FINAL DVT OK2FAB RELEASE

09/21/2009: RELEASE A.0.0 (FAB)-

- FINAL PVT OK2FAB RELEASE
- PAGE 4: ADDED APN 104S0033 (6.8 OHMS, 1/4W) RESISTORS IN MODULE PARTS TABLE FOR R6612, R6617, R6630 & R6633 ADDED APN 518S0774 FOR XDP CONNECTOR J1300 (TO REPLACE 998-2515)
- PAGE 13: ADDED OMIT TO J1300
- PAGE 50: CHANGED R5030 SIL RESISTOR TO 80.6 OHMS APN 114S0112 AS PER ID
- PAGE 53: REPLACED APN 376S0545 WITH 376S0820 @ Q5315 - PER ECO#0000737172
- PAGE 66: ADDED BOMOPTION OMIT TO RESISTORS R6612, R6617, R6630 & R6633

10/12/2009: RELEASE B.0.0 (FAB)-

- PROD_DEBUG (POST FIRST 5K UNTIL 1 MONTH INTO PRODUCTION) OK2FAB RELEASE
- PAGE 4: ADDED 1 NEW POR BOMS 639-0554, 639-0555 AND 1 NEW DEVELOPEMENT BOM 085-1076 FOR INITIAL RAMP
- PAGE 4: UPDATED BOM GROUPS TABLE TO REFLECT AFOREMENTIONED CHANGES. NEW DEVELOPMENT BOM ONLY HAS XDP CONNECTOR AND LPCPLUS COMPONENTS
- PAGE 4: ADDED 2 NEW EEES TO ATTACH WITH AFOREMENTIONED NEW 639 BOMS
- PAGE 4: DELETED 353S2811 ENTRY FROM THE ALTERNATES TABLE
- PAGE 70: REPLACED U7000 WITH THE NEW INTERSIL SCREENED PARTS APN 353S2811

11/01/2009: RELEASE C.0.0 (FAB)-
- PROD (POST 1ST MONTH OF PRODUCTION) OK2FAB RELEASE
- PAGE 2: UPDATED SYSTEM BLOCK DIAGRAM
- PAGE 3: UPDATED POWER SYSTEM BLOCK DIAGRAM
- PAGE 4: UPDATED BOM TABLES TO NOT INCLUDE ANY 085 DEVELOPMENT BOMS. AND, K84_DEBUG_PROD BOM GROUP IS TURNED ON

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE
Revision History

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
BRANCH
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Functional Test Points

FAN CONNECTORS FUNC_TEST

P1K	TRUE	PP5VRT_S0	7 8
P1K	TRUE	FAN_RT_PWM	43
P1K	TRUE	FAN_RT_TACH	43

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

P22K	TRUE	BI_MIC_LO	53 54
P22K	TRUE	BI_MIC_HI	53 54
P22K	TRUE	BI_MIC_SHIELD	53 54

SPEAKER FUNC_TEST

P22K	TRUE	SPKRAMP_L_N_OUT	52 53
P22K	TRUE	SPKRAMP_L_P_OUT	52 53
P22K	TRUE	SPKRAMP_R_N_OUT	52 53
P22K	TRUE	SPKRAMP_R_P_OUT	52 53
P22K	TRUE	SPKRAMP_SUB_N_OUT	52 53
P22K	TRUE	SPKRAMP_SUB_P_OUT	52 53

LVDS FUNC_TEST

P60	TRUE	PP3V3_LCDVDD_SW_F	7 65 (NEED 2 TP)
P60	TRUE	PP3V3_S0_LCD_F	65
P60	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68 (NEED 2 TP)
P60	TRUE	LVDS_IG_DDC_CLK	18 65
P60	TRUE	LVDS_IG_DDC_DATA	18 65
P60	TRUE	LVDS_IG_A_DATA_N<0>	18 65 72
P60	TRUE	LVDS_IG_A_DATA_P<0>	18 65 72
P60	TRUE	LVDS_IG_A_DATA_N<1>	18 65 72
P60	TRUE	LVDS_IG_A_DATA_P<1>	18 65 72
P60	TRUE	LVDS_IG_A_DATA_N<2>	18 65 72
P60	TRUE	LVDS_IG_A_DATA_P<2>	18 65 72
P60	TRUE	LVDS_IG_A_CLK_F_N	65 72
P60	TRUE	LVDS_IG_A_CLK_F_P	65 72
P60	TRUE	LED_RETURN_1	65 68
P60	TRUE	LED_RETURN_2	65 68
P60	TRUE	LED_RETURN_3	65 68
P60	TRUE	LED_RETURN_4	65 68
P60	TRUE	LED_RETURN_5	65 68
P60	TRUE	LED_RETURN_6	65 68
P60	TRUE	PP5V_S3_CAMERA_F	7 65
J897	TRUE	USB_CAMERA_CONN_P	65 73
J894	TRUE	USB_CAMERA_CONN_N	65 73

(NEED TO ADD 5 GND TP)

SATA ODD CONN FUNC_TEST

P26	TRUE	PP5V_SW_ODD (NEED 2 TP)	7 34 47
P26	TRUE	SMC_ODD_DETECT	34 36
P26	TRUE	SATA_ODD_D2R_C_P	34 72
P26	TRUE	SATA_ODD_D2R_C_N	34 72
P26	TRUE	SATA_ODD_R2D_P	34 72
P26	TRUE	SATA_ODD_R2D_N	34 72

(NEED TO ADD 2 GND TP)

SATA HDD/SIL FUNC_TEST

P31K	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	7 34
P31K	TRUE	SATA_HDD_R2D_P	34 72
P31K	TRUE	SATA_HDD_R2D_N	34 72
P31K	TRUE	SATA_HDD_D2R_C_P	34 72
P31K	TRUE	SATA_HDD_D2R_C_N	34 72
J30K	TRUE	SYS_LED_ANODE_R	34

(NEED TO ADD 3 GND TP)

BATT POWER CONN FUNC_TEST

P32K	TRUE	SMBUS_SMC_BSA_SCL	39 75
P32K	TRUE	SMBUS_SMC_BSA_SDA	39 75
P32K	TRUE	SYS_DETECT_L	55
P32K	TRUE	BATT_POS_F (NEED 2 TP)	55 56

(NEED TO ADD 2 GND TP)

HALL EFFECT CONNECTOR FUNC_TEST

P10K	TRUE	PP3V42_G3H	7 8
P10K	TRUE	SMC_LID_R	55

X16 WIRELESS CONN FUNC_TEST

J303	TRUE	PP3V3_S3_BT_F	30
J301	TRUE	CONN_PCIE_MINI_D2R_P	30 72
J302	TRUE	CONN_PCIE_MINI_D2R_N	30 72
J306	TRUE	CONN_PCIE_MINI_R2D_P	30 72
P22K	TRUE	CONN_PCIE_MINI_R2D_N	30 72
P22K	TRUE	PCIE_CLK100M_MINI_CONN_P	30 72
P22K	TRUE	PCIE_CLK100M_MINI_CONN_N	30 72
J223	TRUE	PP3V3_WLAN (NEED 2 TP)	7 30
J288	TRUE	PCIE_WAKE_L	17 30
P22K	TRUE	CONN_USB2_BT_P	30 73
P22K	TRUE	CONN_USB2_BT_N	30 73
P26K	TRUE	MINI_CLKREQ_O_L	30
J273	TRUE	MINI_RESET_CONN_L	30
J289	TRUE		

(NEED TO ADD 2 GND TP)

IPD_FLEX_CONN FUNC_TEST

J37K	TRUE	PP3V3_S3_LDO	7 45
J37K	TRUE	PP18V5_S3	7 45
J372	TRUE	Z2_CS_L	44 45
J376	TRUE	Z2_DEBUG3	44 45
J371	TRUE	Z2_MOSI	44 45
J365	TRUE	Z2_MISO	44 45
J368	TRUE	Z2_SCLK	44 45
J361	TRUE	Z2_BOOST_EN	45
J364	TRUE	Z2_HOST_INTN	44 45
J363	TRUE	Z2_CLKIN	44 45
J383	TRUE	Z2_KEY_ACT_L	44 45
J364	TRUE	Z2_RESET	44 45
J362	TRUE	PSOC_MISO	44 45
J366	TRUE	PSOC_MOSI	44 45
J369	TRUE	PSOC_SCLK	44 45
J357	TRUE	SMBUS_SMC_A_S3_SDA	39 75
J358	TRUE	SMBUS_SMC_A_S3_SCL	39 75
J377	TRUE	PSOC_F_CS_L	44 45
J378	TRUE	PICKB_L	44 45

(NEED TO ADD 2 GND TP)

KEYBOARD CONN FUNC_TEST

J354	TRUE	PP3V3_S3	7 8
J355	TRUE	PP3V42_G3H	7 8
J344	TRUE	WS_KBD1	44
J345	TRUE	WS_KBD2	44
J346	TRUE	WS_KBD3	44
J347	TRUE	WS_KBD4	44
J349	TRUE	WS_KBD5	44
J348	TRUE	WS_KBD6	44
J360	TRUE	WS_KBD7	44
J352	TRUE	WS_KBD8	44
J351	TRUE	WS_KBD9	44
J353	TRUE	WS_KBD10	44
J327	TRUE	WS_KBD11	44
J328	TRUE	WS_KBD12	44
J329	TRUE	WS_KBD13	44
J343	TRUE	WS_KBD14	44
J342	TRUE	WS_KBD15_CAP	44
J341	TRUE	WS_KBD16_NUM	44
J339	TRUE	WS_KBD17	44
J340	TRUE	WS_KBD18	44
J338	TRUE	WS_KBD19	44
J336	TRUE	WS_KBD20	44
J337	TRUE	WS_KBD21	44
J333	TRUE	WS_KBD22	44
J335	TRUE	WS_KBD23	44
J334	TRUE	WS_KBD_ONOFF_L	44
J332	TRUE	WS_LEFT_SHIFT_KBD	44
J330	TRUE	WS_LEFT_OPTION_KBD	44
J331	TRUE	WS_CONTROL_KBD	44

(NEED TO ADD 1 GND TP)

POWER NETS FUNC_TEST

J37K	TRUE	PPVCORE_S0_CPU	8
J38K	TRUE	PPVCORE_S0_MCP	8
J39K	TRUE	PP0V75_S0	8
J39K	TRUE	PP1V05_S0	8
J39K	TRUE	PP1V5_S0	8
J39K	TRUE	PP1V8_S0	8
J39K	TRUE	PP5VLT_S0	8
J39K	TRUE	PP5VRT_S0	7 8
J39K	TRUE	PP3V3_S0	8
J39K	TRUE	PP1V5_S3	8
J39K	TRUE	PP3V3_S3	7 8
J39K	TRUE	PP5V_S3	8
J39K	TRUE	PP1V1R1V05_S5	8
J39K	TRUE	PP3V3_S5	8
J39K	TRUE	PP3V42_G3H	7 8
J39K	TRUE	PPBUS_G3H	8
J39K	TRUE	PP3V3_ENET_PHY	8
J39K	TRUE	PP1V2R1V05_ENET	8
J39K	TRUE	PP3V3_G3_RTC	21 22 25
J39K	TRUE	PP3V3_WLAN	7 30
J39K	TRUE	PP5V_SW_ODD	7 34 47
J39K	TRUE	PP5V_S0_HDD_FLT	7 34
J39K	TRUE	PP3V3_S5_AVREF_SMC	36 37
J39K	TRUE	PP18V5_S3	7 45
J39K	TRUE	PP3V3_S3_LDO	7 45
J39K	TRUE	PP3V3_LCDVDD_SW_F	7 65
J39K	TRUE	PPVOUT_S0_LCDBKLT	7 47 65 68
J39K	TRUE	PP4V5_AUDIO_ANALOG	49
J39K	TRUE	SMC_PM_G2_EN	36 57 63
J39K	TRUE	PM_SLP_S4_L	21 36 37 63
J39K	TRUE	PM_SLP_S3_L	21 32 36 63 67
J39K	TRUE	PP5V_S3_CAMERA_F	7 65

(NEED TO ADD 1 GND TP)

DC POWER CONN FUNC_TEST

P10K	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	55
P10K	TRUE	ADAPTER_SENSE	55

(NEED TO ADD 2 GND TP)

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE: FUNC TEST

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

"S0,S0M" RAILS

59 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU — 11 12
=PPVCORE_S0_CPU_VSENSE — 40

61 =PPCPUVTT_S0_REG
PP1V05_S0 — 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU — 10 11 12 13
=PP1V05_S0_MCP_FSB — 14 22 23
=PP1V05_S0_MCP_PEX_DVDD — 8 23
=PP1V05_S0_MCP_AVDD_UF — 23
=PP1V05_S0_MCP_SATA_DVDD — 8 23
=PP1V05_S0_MCP_HDMI_VDD — 18 24
=PP1V05_S0_VMON — 63
=PP1V05_S0_MCP_PLL_UF_R — 62

60 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP — 22 23
=PPVCORE_S0_MCP_VSENSE — 40

58 =PP0V75_S0_REG
PP0V75_S0 — 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP — 64
=PP0V75_S0_MEM_VTT_A — 27
=PP0V75_S0_MEM_VTT_B — 28

64 =PP1V5_S0_FET
PP1V5_S0 — 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU — 11 12
=PP1V5_S0_VMON — 63
=PP1V8R1V5_S0_MCP_MEM — 16 23
=PP1V5_S0_MEM_MCP — 28
=PP1V5_S0_MCP_PLL_VLDO — 62

62 =PP1V8_S0_REG
PP1V8_S0 — 7
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD — 18 24
=PP1V8_S0_AUDIO — 49

62 23 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

64 =PP5VRT_S0_FET
PP5VRT_S0 — 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_CPUVTTS0 — 61
=PP5V_S0_LPCPLUS — 38
=PP5V_S0_FAN_RT — 43
=PP5V_S0_CPU_IMVP — 59

64 =PP5VLT_S0_FET
PP5VLT_S0 — 7
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_DP_AUX_MUX — 66
=PP5V_S0_HDD — 34
=PP5V_S0_MCPREG — 60
=PP5V_S0_VMON — 63

64 =PP3V3_S0_FET
PP3V3_S0 — 7
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP — 13
=PP3V3_S0_MCP — 21 22 23
=PP3V3_S0_MCP_DAC_UF — 24
=PP3V3_S0_MCP_VPLL_UF — 24
=PP3V3_S0_ODD — 34
=PP3V3_S0_SMBUS_SMC_0_S0 — 39
=PP3V3_S0_SMBUS_SMC_B_S0 — 39
=PP3V3_S0_SMBUS_MCP_0 — 39
=PP3V3_S0_FAN_RT — 43
=PP3V3_S0_AUDIO — 49 53 54
=PP3V3_S0_IMVP — 59
=PP3V3_S0_LCD — 65
=PP3V3_S0_MCP_GPIO — 18 19 21
=PP3V3_S0_MCP_PLL_UF — 23
=PP3V3R1V5_S0_MCP_HDA — 21 23
=PP3V3_S0_SMC — 37
=PP3V3_S0_MCPTHMSNS — 42
=PP3V3_S0_CPUTHMSNS — 42
=PP3V3_S0_DPCONN — 67
=PPSPD_S0_MEM_A — 27
=PPSPD_S0_MEM_B — 28
=PP3V3_S0_PWRCTL — 63
=PP3V3_S0_VMON — 63
=PP3V3_S0_CPUVTTISNS — 41
=PP3V3_S0_SMBUS_MCP_1 — 39
=PP3V3_S0_P1V8S0 — 62
=PP3V3_S0_MCP_PLL_VLDO — 62
=PP3V3_S0_MCPDDRISNS — 41

"S3" RAILS

58 =PP1V5_S3_REG
PP1V5_S3 — 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_P1V5S0FET — 64
=PP1V5_S3_MEM_A — 27
=PP1V5_S3_MEM_B — 28
=PP1V5_S3_MEMRESET — 29

64 =PP3V3_S3_FET
PP3V3_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMBUS_SMC_A_S3 — 39
=PP3V3_S3_PDCISENS — 58
=PP3V3_S3_SMBUS_SMC_MGMT — 39
=PP3V3_S3_VREFMRGN — 26
=PP3V3_S3_WLAN — 30
=PP3V3_S3_MCP_GPIO — 21
=PP3V3_S3_TPAD — 44
=PP3V3_S3_SMS — 46
=PP3V3_S3_BT — 30

57 =PP5V_S3_REG
PP5V_S3 — 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB — 35
=PP5V_S3_CAMERA — 65
=PP5V_S3_AUDIO_AMP — 52
=PP5V_S3_MCPDDRFET — 64
=PP5V_S3_1V5S30V75S0 — 58
=PP5V_S3_AUDIO — 49 51 53
=PP5V_S3_P5VLTS0FET — 64
=PP5V_S3_VTTCLAMP — 64
=PP5V_S3_DEBUG_ISNS — 47
=PP5V_S3_SYSLED — 37
=PP5V_S3_TPAD — 45
=PP5V_S3_ODD — 34
=PP5V_S3_DEBUG_ADC_AVDD — 47
=PP5V_S3_DEBUG_ADC_DVDD — 47
=PP5V_S3_P5VRTS0FET — 64

58 26 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

"S5" RAILS

62 =PP1V05_S5_REG
PP1V1R1V05_S5 — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC — 22 23
=PP1V05_ENET_P1V05ENETFET — 32

57 =PP3V3_S5_REG
PP3V3_S5 — 7
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO — 18 20
=PP3V3_S5_ROM — 38 48
=PP3V3_S5_LCD — 65
=PP3V3_S5_MCP — 22 23
=PP3V3_S5_MCPPWRGD — 25
=PP3V3_S5_PWRCTL — 63
=PP3V3_S5_P1V05ENETFET — 32
=PP3V3_S5_P3V3S3FET — 64
=PP3V3_S5_P3V3S0FET — 64
=PP3V3_S5_P1V05S5 — 62
=PP3V3_S5_MEMRESET — 29
=PP3V3_S5_P3V3ENETFET — 32
=PP3V3_S5_DP_PORT_PWR — 67

"G3H" RAILS

55 =PP3V42_G3H_REG
PP3V42_G3H — 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF — 37
=PP3V42_G3H_SMBUS_SMC_BSA — 39
=PP3V42_G3H_PWRCTL — 63
=PP3V42_G3H_CHGR — 56
=PP3V42_G3H_SMCUSBMUX — 35
=PP3V42_G3H_TPAD — 44
=PP3V3_S5_SMC — 36 37
=PP3V3_S5_LPCPLUS — 38
=PP3V42_G3H_RTC_D — 25
=PP3V42_G3H_ONEWIRE — 55
=PP3V42_G3H_HALL — 55

55 =PP18V5_DCIN_CONN
PP18V5_G3H — 56
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR — 56

56 =PPBUS_G3H
PPBUS_G3H — 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_MCPCORE — 60
=PPVIN_S5_1V5S30V75S0 — 58
=PPCPUVCORE_VTT_ISNS_R — 41
(BEFORE HIGH SIDE SENSING RES.)
=PPBUS_S0_LCDBKLT — 69
=PPVIN_S5_3V3S5 — 57
=PPVIN_S3_5VS3 — 57
=PPBUS_G3HRS5 — 40

41 =PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 — 61
=PPVIN_S5_CPU_IMVP — 59

DIGITAL GROUND
GND
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=0V

"ENET" RAILS

32 =PP3V3_ENET_FET
PP3V3_ENET_PHY — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT — 18 23
=PP3V3_ENET_PHY — 31

32 =PP1V05_ENET_FET
PP1V2R1V05_ENET — 7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC — 23
=PP1V05_ENET_MCP_RMGT — 18 23
=PP1V05_ENET_PHY — 31

PEX & SATA AVDD/DVDD aliases

23 =PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
23 8 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
23 =PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
127 mA (A01)
23 8 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)

=PP1V05_S0_MCP_PEX_AVDD0 — 17
=PP1V05_S0_MCP_PEX_AVDD1 — 17
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 — 17
=PP1V05_S0_MCP_PEX_DVDD1 — 17
57 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 — 20
=PP1V05_S0_MCP_SATA_AVDD1 — 20
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 — 20
=PP1V05_S0_MCP_SATA_DVDD1 — 20
43 mA (A01)

SYNC_MASTER=K24_MLB
SYNC_DATE=02/04/2009
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Power Aliases
Apple Inc.
DRAWING NUMBER 051-7982
SIZE D
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BRANCH
PAGE 8 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.5OD.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

OMIT
Z0905
3P2R2P7

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT
Z0906
3P2R2P7

OMIT
Z0907
3P2R2P7

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT
Z0911
3P2R2P7

OMIT
Z0910
3P2R2P7

LVDS CONNECTOR HOLE

OMIT
Z0913
3P2R2P7

EMI IO MEDIUM POGO PINS (870-1794)

OMIT
ZS0900
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0901
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0902
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0903
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0908
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0909
2.0DIA-MED-EMI-MLB-K84
SM

OMIT
ZS0911
2.0DIA-MED-EMI-MLB-K84
SM

EMI TALL POGO PINS (870-1698)

OMIT
ZS0904
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0905
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0906
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0907
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0910
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0912
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0913
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0914
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0915
2.0DIA-TALL-EMI-MLB-M97-M98
SM

OMIT
ZS0919
2.0DIA-TALL-EMI-MLB-M97-M98
SM

EMI THINBC POGO PINS (870-1820)

OMIT
ZS0917
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0918
2.0DIA-MLB-THIN-BC-K84
SM

OMIT
ZS0916
2.0DIA-MLB-THIN-BC-K84
SM

NOSTUFF
ZS0920
2.0DIA-MLB-THIN-BC-K84
SM

PCI-E ALIASES

UNUSED GPU LANES

17	=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	PEG_PRSNT_L	TP_PEG_PRSNT_L	MAKE_BASE=TRUE
17	PEG_CLK100M_P	TP_PEG_CLK100M_P	MAKE_BASE=TRUE
17	PEG_CLK100M_N	TP_PEG_CLK100M_N	MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

17	PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE
17	PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_EXCARD_PRSNT_L	TP_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE
17	EXCARD_CLKREQ_L	TP_EXCARD_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_P	TP_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_EXCARD_N	TP_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE

UNUSED FIREWIRE LANE

72 17	PCIE_FW_D2R_P	TP_PCIE_FW_D2R_P	MAKE_BASE=TRUE
72 17	PCIE_FW_D2R_N	TP_PCIE_FW_D2R_N	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_P	TP_PCIE_FW_R2D_C_P	MAKE_BASE=TRUE
72 17	PCIE_FW_R2D_C_N	TP_PCIE_FW_R2D_C_N	MAKE_BASE=TRUE
17	PCIE_FW_PRSNT_L	TP_PCIE_FW_PRSNT_L	MAKE_BASE=TRUE
17	FW_CLKREQ_L	TP_FW_CLKREQ_L	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_P	TP_PCIE_CLK100M_FW_P	MAKE_BASE=TRUE
17	PCIE_CLK100M_FW_N	TP_PCIE_CLK100M_FW_N	MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

20	USB_EXTD_P	TP_USB_EXTD_P	MAKE_BASE=TRUE
20	USB_EXTD_N	TP_USB_EXTD_N	MAKE_BASE=TRUE
20	USB_EXCARD_P	TP_USB_EXCARD_P	MAKE_BASE=TRUE
20	USB_EXCARD_N	TP_USB_EXCARD_N	MAKE_BASE=TRUE
20	USB_MINI_P	TP_USB_MINI_P	MAKE_BASE=TRUE
20	USB_MINI_N	TP_USB_MINI_N	MAKE_BASE=TRUE
20	USB_EXTC_P	TP_USB_EXTC_P	MAKE_BASE=TRUE
20	USB_EXTC_N	TP_USB_EXTC_N	MAKE_BASE=TRUE
73 20	USB_CARDREADER_P	TP_USB_CARDREADER_P	MAKE_BASE=TRUE
73 20	USB_CARDREADER_N	TP_USB_CARDREADER_N	MAKE_BASE=TRUE
73 20	USB_IR_N	TP_USB_IR_N	MAKE_BASE=TRUE
73 20	USB_IR_P	TP_USB_IR_P	MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE, MAKE_BASE=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	NO_TEST=TRUE, MAKE_BASE=TRUE

LVDS ALIASES

18	LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE
18	LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE, MAKE_BASE=TRUE

MISC MCP79 ALIASES

14	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE
19	FW_PME_L	TP_FW_PME_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TCK_L	TP_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE
17	GMUX_JTAG_TDO	TP_GMUX_JTAG_TDO	MAKE_BASE=TRUE
19	GMUX_JTAG_TDI	TP_GMUX_JTAG_TDI	MAKE_BASE=TRUE
19	GMUX_JTAG_TMS	TP_GMUX_JTAG_TMS	MAKE_BASE=TRUE
21	MCP_GPIO_4	MIKEY_MIC_LOAD_DET	MAKE_BASE=TRUE
17	CARDREADER_RESET	TP_CARDREADER_RESET	MAKE_BASE=TRUE

54

LAN ALIASES

18	=MCP_MII_RXER	MCP_MII_PD	MAKE_BASE=TRUE
18	=MCP_MII_COL		
18	=MCP_MII_CRS		

R0930
47K
5%
1/16W
MF-LF
402

DP HOTPLUG PULL-DOWN

18	=DVI_HPD_GMUX_INT	HPLUG_DET2	MAKE_BASE=TRUE

R0940
20K
5%
1/16W
MF-LF
402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

27	MEM_A_A<15>	TP_MEM_A_A15	MAKE_BASE=TRUE
28	MEM_B_A<15>	TP_MEM_B_A15	MAKE_BASE=TRUE

ETHERNET ALIASES

32	=P3V3ENET_EN	PM_SLP_RMGT_L	MAKE_BASE=TRUE, 21
32	=P1V05ENET_EN		
31	=PP3V3_ENET_PHY_VDDREG	RTL8211_VDDREG	MAKE_BASE=TRUE
31	=RTL8211_REGOUT	NC_RTL8211_REGOUT	MAKE_BASE=TRUE
31	=RTL8211_ENSWREG		
31	TP_RTL8211_CLK125	RTL8211_CLK125	MAKE_BASE=TRUE

R0931
22
5%
1/10W
MF-LF
402

CPU FSB FREQUENCY STRAPS

70 18 CPU_BSEL<0:2> (IN) = =MCP_BSEL<0:2> (OUT) 14
MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

SMC ALIASES

36	SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE

CPU VCORE ALIASES

59	IMVP6_VR_TT	TP_IMVP6_VR_TT	MAKE_BASE=TRUE
59	IMVP6_NTC	TP_IMVP6_NTC	MAKE_BASE=TRUE

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

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SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
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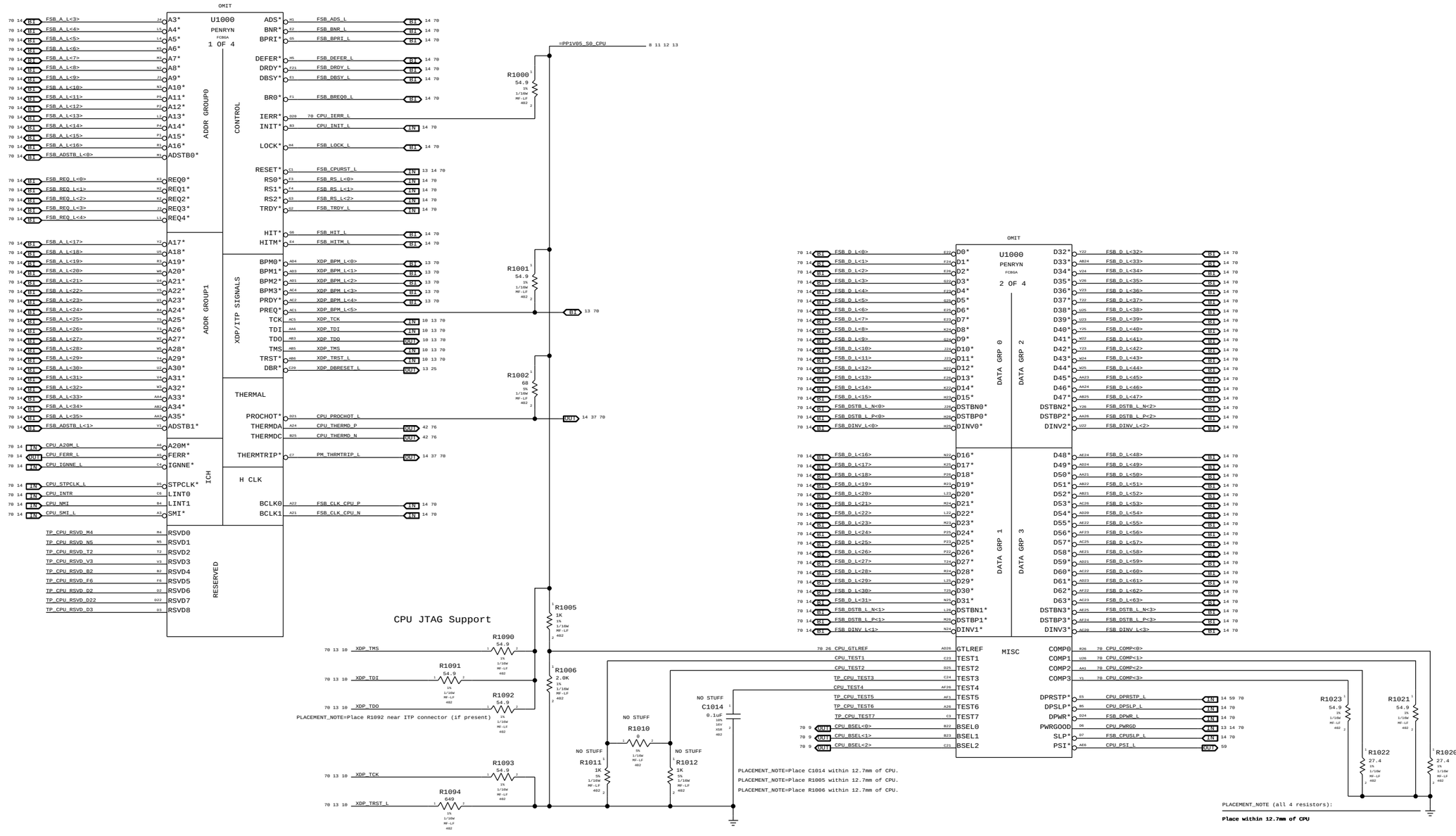
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

CPU FSB

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

BRANCH

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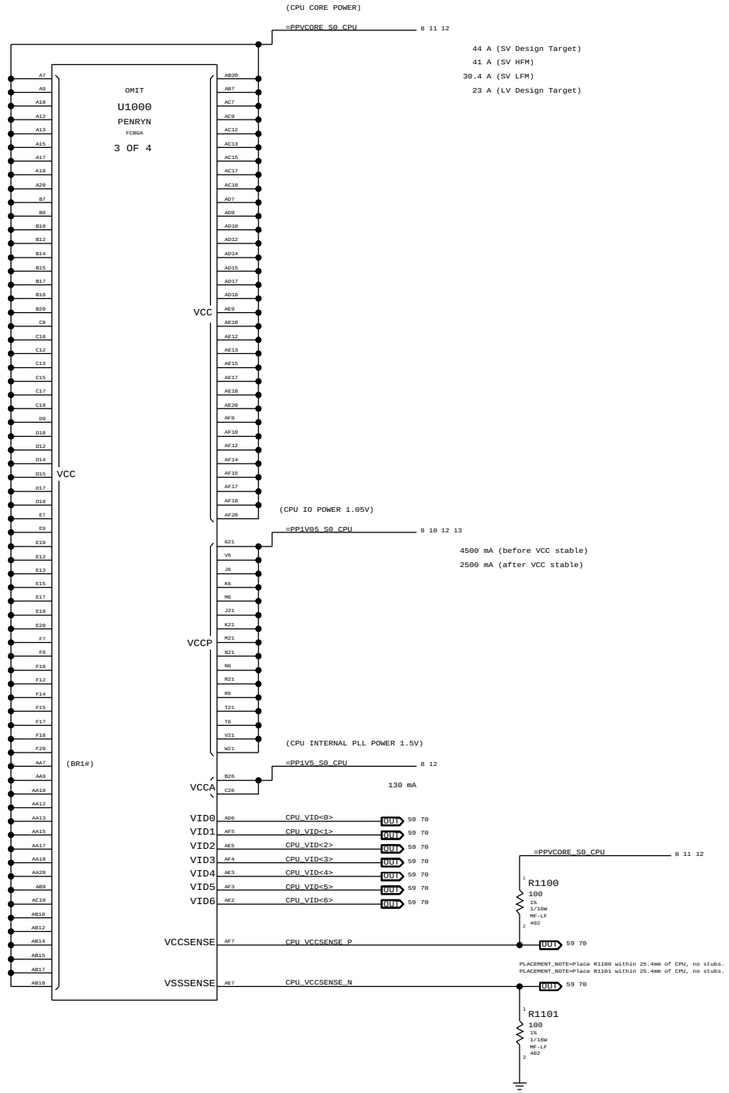
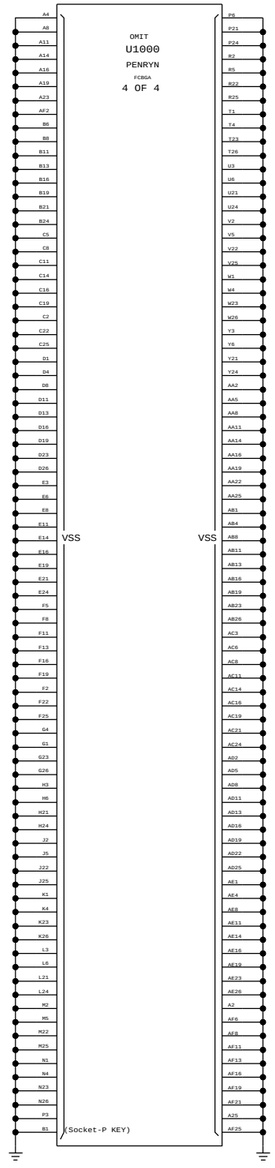
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





SYNC FROM T18

CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

SYNC MASTER=K24_MLB SYNC DATE=04/06/2009

PAGE TITLE

CPU Power & Ground

Apple Inc.

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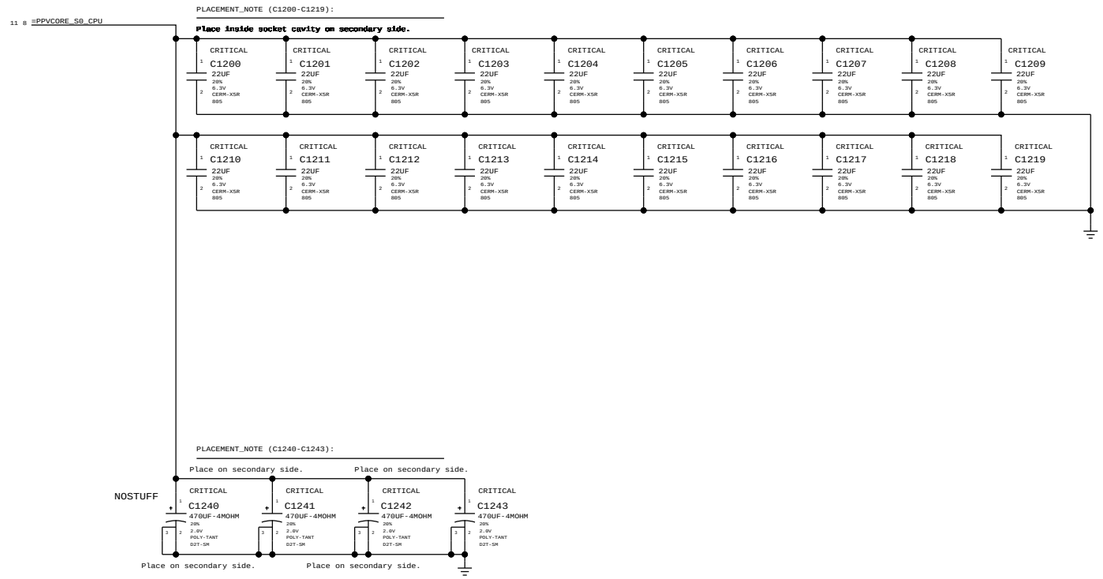
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

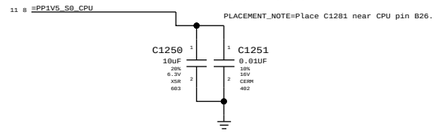
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



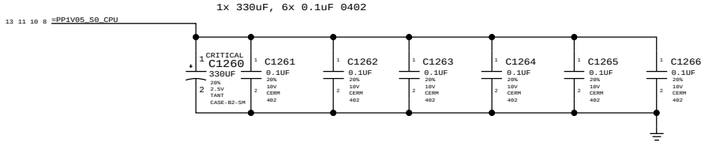
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC_MASTER=K24_MLB SYNC_DATE=03/30/2009

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

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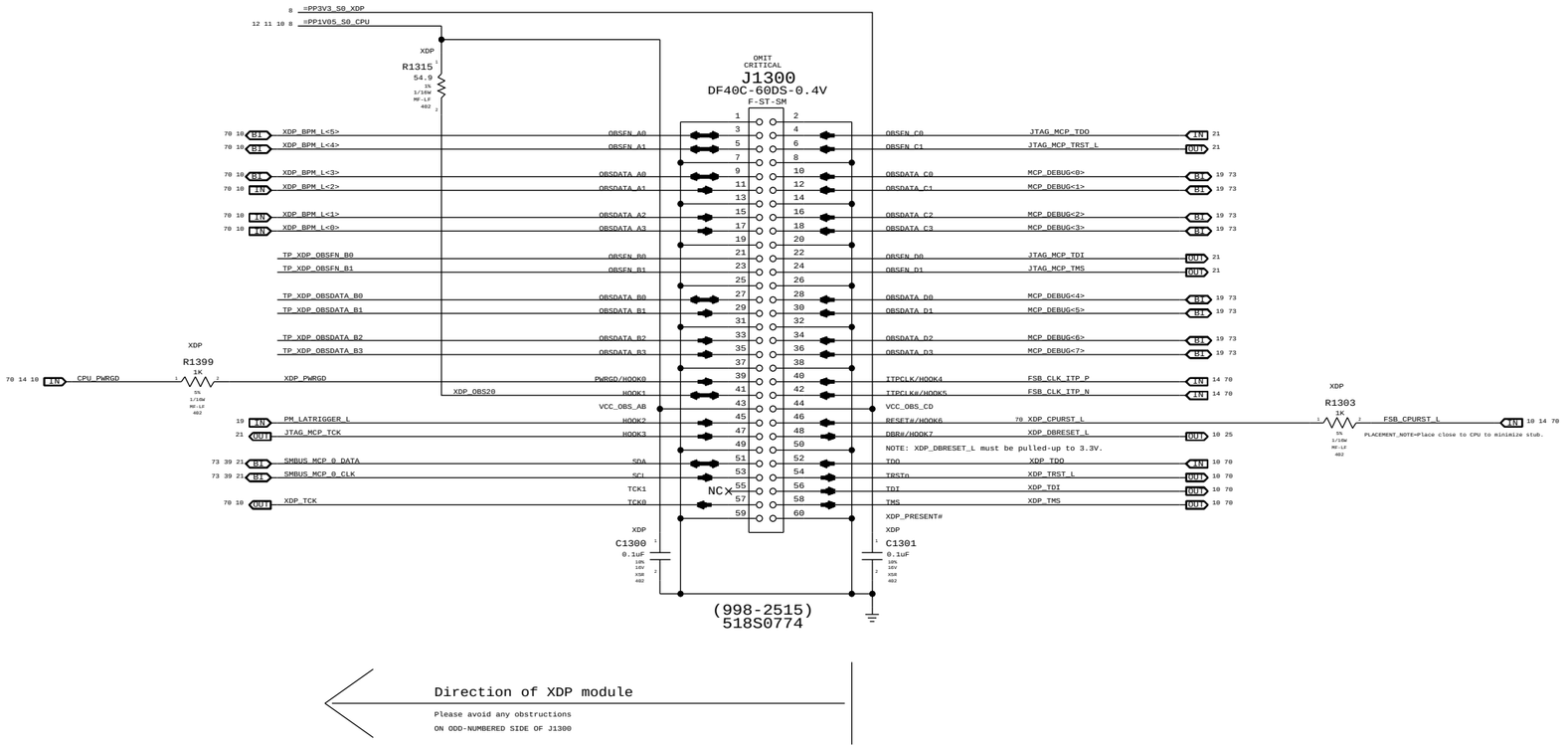
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

MCP79-specific pinout



SYNC_MASTER=K24_MLB SYNC_DATE=02/25/2009

PAGE TITLE

eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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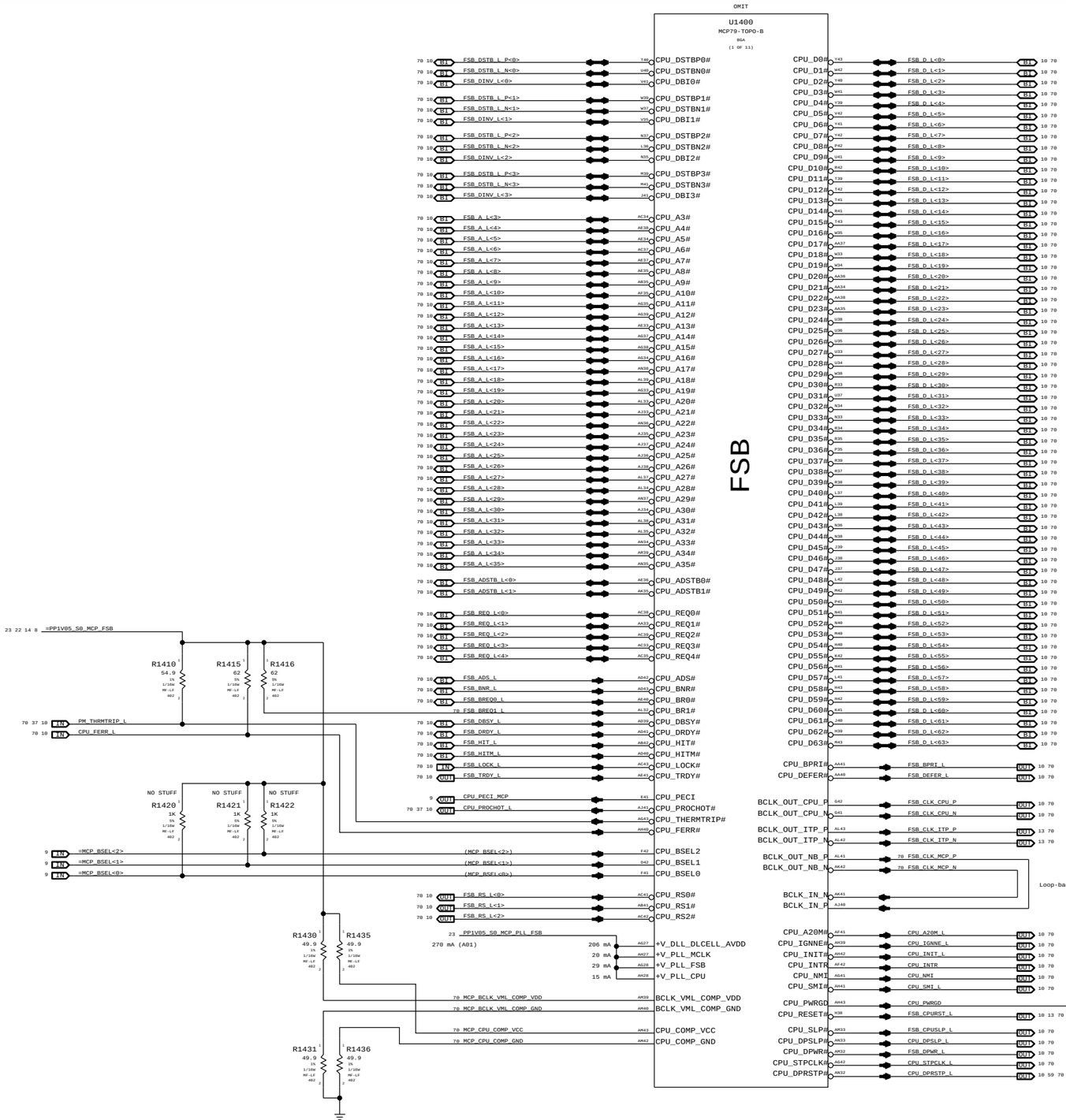

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PAGE TITLE: MCP CPU Interface

Apple Inc.

DRAWING NUMBER: 051-7982 | SIZE: D

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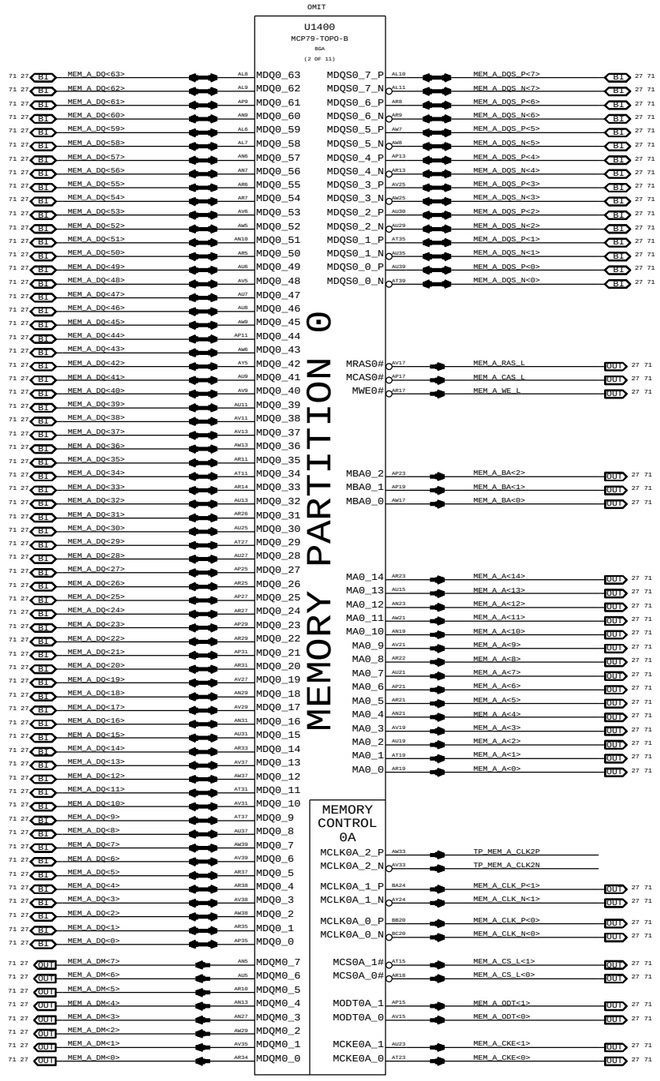
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BGA
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BGA
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SYNC_MASTER=K24_MLB
SYNC_DATE=04/06/2009
PAGE TITLE
MCP Memory Interface
Apple Inc.
DRAWING NUMBER
051-7982
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REVISION
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OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

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MCLK1B_1_N	BA23	TP_MEM_B_CLK4N
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23 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

MRESET0# AY32 — TP_MEM_RESET_L → OUT 29
TP or NC for DDR2.

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R1610 1 — 40.2 1% 1/16W MF-LF 402 — 2
R1611 1 — 40.2 1% 1/16W MF-LF 402 — 2

71 MCP_MEM_COMP_VDD → AM41 MEM_COMP_VDD
71 MCP_MEM_COMP_GND → AM41 MEM_COMP_GND

=PP1V8R1V5_S0_MCP_MEM 8 16 23
4771 mA (A01, DDR3)

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G30	GND3	+VDD_MEM3 AM21
P18	GND4	+VDD_MEM4 AM23
T16	GND5	+VDD_MEM5 AM25
T6	GND6	+VDD_MEM6 AM27
V10	GND7	+VDD_MEM7 AM29
V34	GND8	+VDD_MEM8 AN16
W5	GND9	+VDD_MEM9 BC29
AA39	GND10	+VDD_MEM10 AN20
AB22	GND11	+VDD_MEM11 AN24
AB7	GND12	+VDD_MEM12 AT17
AD22	GND13	+VDD_MEM13 AP16
AE20	GND14	+VDD_MEM14 AN22
AF24	GND15	+VDD_MEM15 AP20
AG24	GND16	+VDD_MEM16 AP24
AH35	GND17	+VDD_MEM17 AY16
AK7	GND18	+VDD_MEM18 AR16
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F28	GND24	+VDD_MEM24 AU16
BC21	GND25	+VDD_MEM25 AN18
AY9	GND26	+VDD_MEM26 AU24
BC9	GND27	+VDD_MEM27 AT21
D34	GND28	+VDD_MEM28 AY29
F24	GND29	+VDD_MEM29 AV24
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H31	GND31	+VDD_MEM31 AU22
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M6	GND35	+VDD_MEM35 AY17
M7	GND36	+VDD_MEM36 AY18
M9	GND37	+VDD_MEM37 AM15
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P7	GND45	+VDD_MEM45 AM31
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R5	GND49	
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T20	GND51	GND56 T34
AK11	GND52	GND57 T35
T24	GND53	GND58 T37
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SYNC MASTER=K24_MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Memory Misc

Apple Inc.

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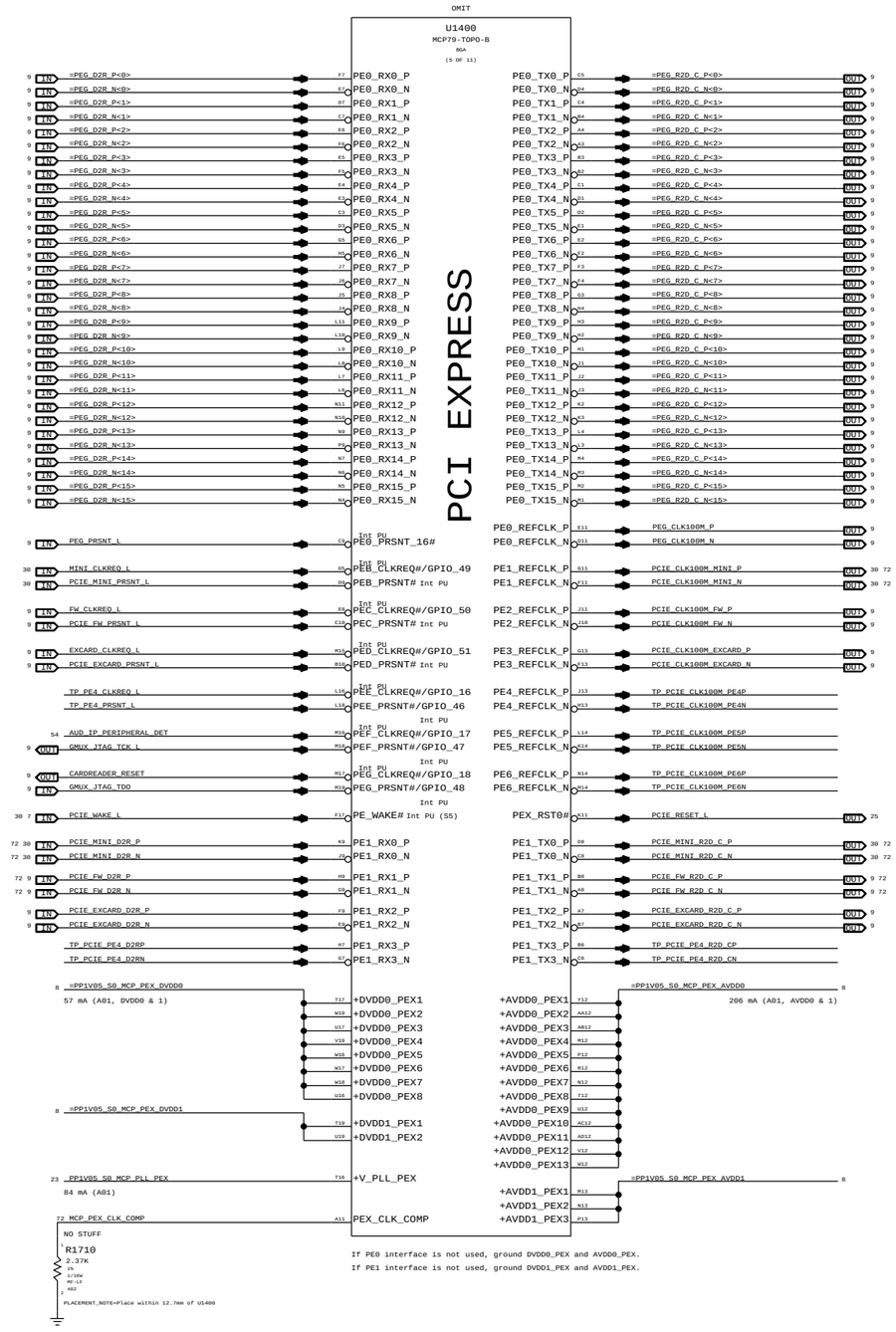

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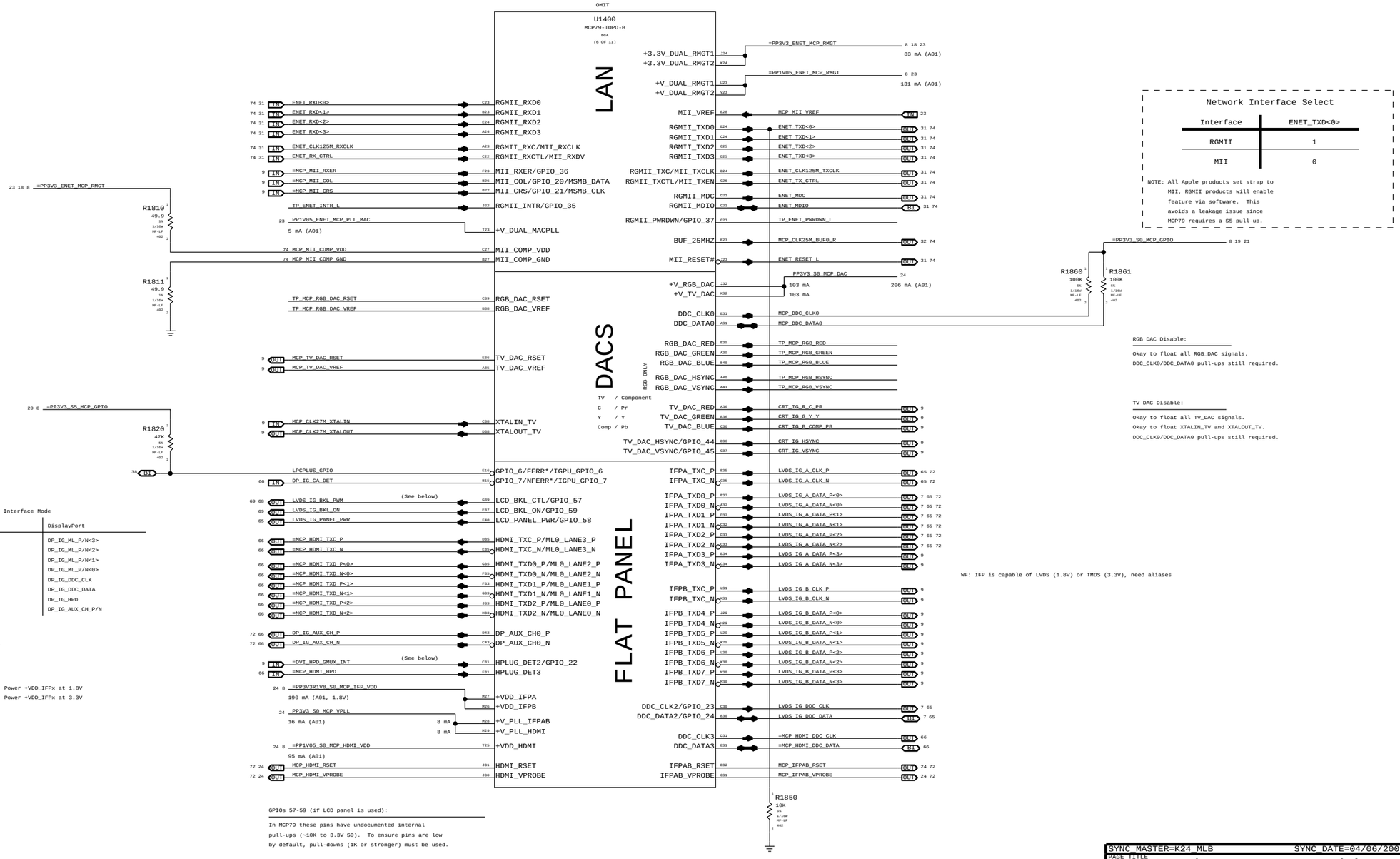

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PAGE TITLE

MCP Ethernet & Graphics

Apple Inc.

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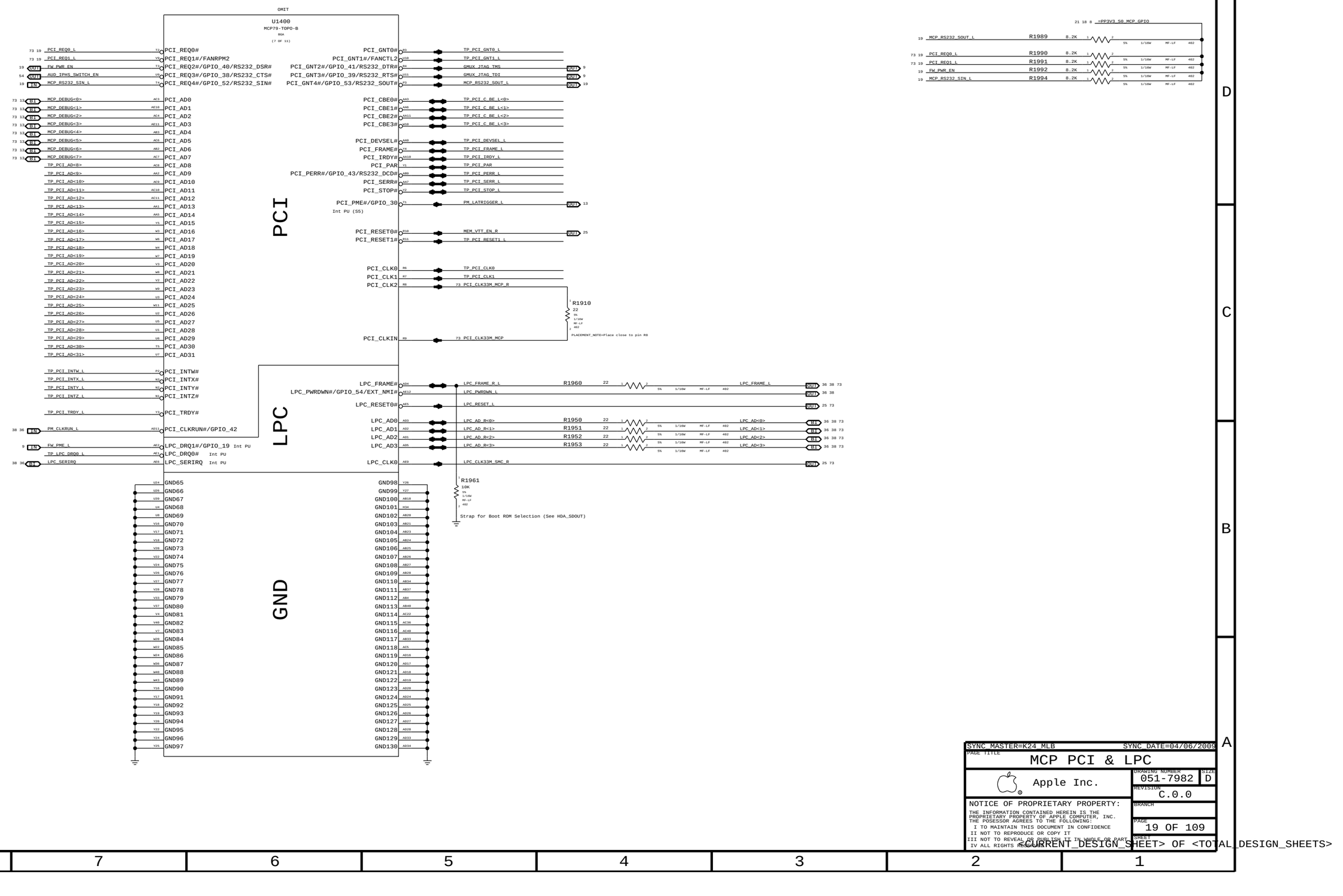
OMIT
U1400
MCP79-TOPO-B
BGA
(7 OF 11)
PCI
PCI_REQ0#
PCI_REQ1#/FANRPM2
PCI_REQ2#/GPIO_40/RS232_DSR#
PCI_REQ3#/GPIO_38/RS232_CTS#
PCI_REQ4#/GPIO_52/RS232_SIN#
PCI_GNT0#
PCI_GNT1#/FANCTL2
PCI_GNT2#/GPIO_41/RS232_DTR#
PCI_GNT3#/GPIO_39/RS232_RTS#
PCI_GNT4#/GPIO_53/RS232_SOUT#
PCI_AD0
PCI_AD1
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31
PCI_CBE0#
PCI_CBE1#
PCI_CBE2#
PCI_CBE3#
PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_PAR
PCI_PERR#/GPIO_43/RS232_DCD#
PCI_SERR#
PCI_STOP#
PCI_PME#/GPIO_30
Int PU (S5)
PCI_RESET0#
PCI_RESET1#
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLKIN
R1910
22
PLACEMENT_NOTE=Place close to pin R8
PCI_INTW#
PCI_INTX#
PCI_INTY#
PCI_INTZ#
PCI_TRDY#
PCI_CLKRUN#/GPIO_42
LPC_DRQ1#/GPIO_19 Int PU
LPC_DRQ0# Int PU
LPC_SERIRQ Int PU
LPC
LPC_FRAME#
LPC_PWRDWN#/GPIO_54/EXT_NMI#
LPC_RESET0#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_CLK0
R1960
R1950
R1951
R1952
R1953
R1961
10K
Strap for Boot ROM Selection (See HDA_SDOUT)
GND
GND65
GND66
GND67
GND68
GND69
GND70
GND71
GND72
GND73
GND74
GND75
GND76
GND77
GND78
GND79
GND80
GND81
GND82
GND83
GND84
GND85
GND86
GND87
GND88
GND89
GND90
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GND101
GND102
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GND104
GND105
GND106
GND107
GND108
GND109
GND110
GND111
GND112
GND113
GND114
GND115
GND116
GND117
GND118
GND119
GND120
GND121
GND122
GND123
GND124
GND125
GND126
GND127
GND128
GND129
GND130
=PP3V3_S0_MCP_GPIO
R1989
R1990
R1991
R1992
R1994
8.2K
SYNC_MASTER=K24_MLB
SYNC_DATE=04/06/2009
PAGE TITLE
MCP PCI & LPC
Apple Inc.
DRAWING NUMBER
051-7982
SIZE
D
REVISION
C.0.0
BRANCH
PAGE
19 OF 109
SHEET
<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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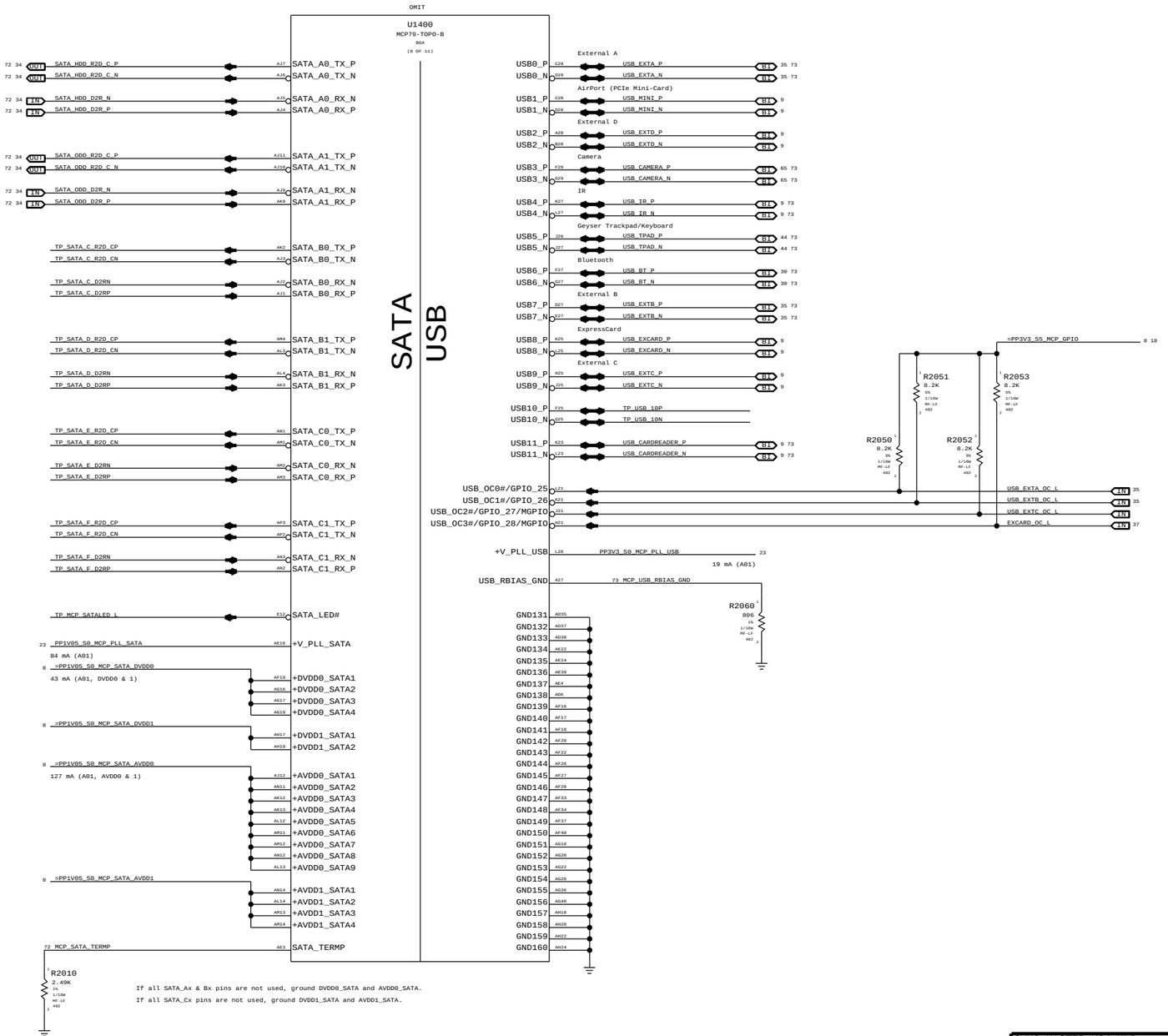

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE

MCP SATA & USB

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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PAGE 20 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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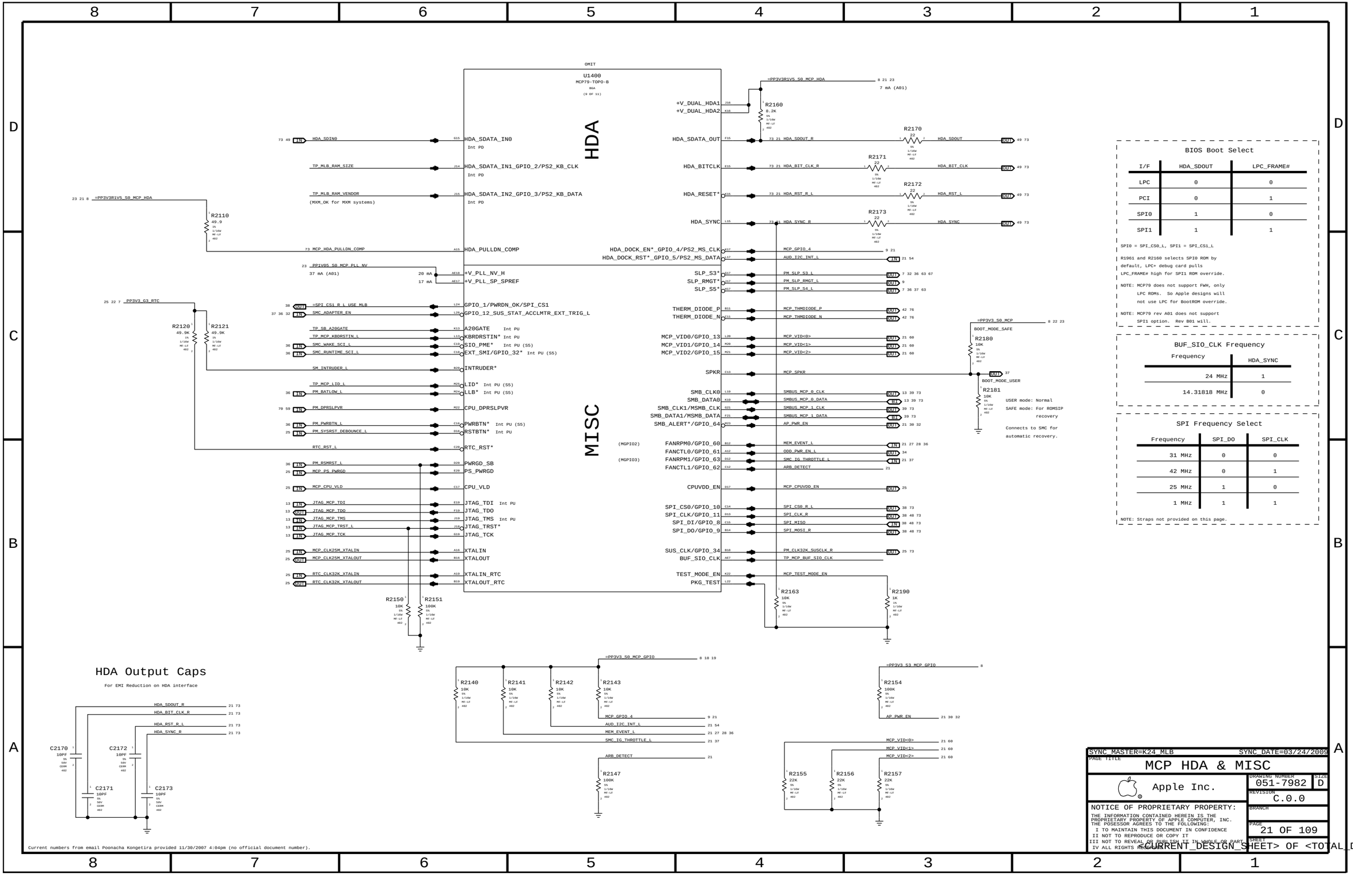
U1400
MCP79-TOPO-B
BGA
(9 OF 11)
OMIT
HDA
MISC
HDA_SDATA_IN0
HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK
HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA
HDA_PULLDN_COMP
+V_PLL_NV_H
+V_PLL_SP_SPREF
GPIO_1/PWRDN_OK/SPI_CS1
GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L
A20GATE
KBRDRSTIN*
SIO_PME*
EXT_SMI/GPIO_32*
INTRUDER*
LID*
LLB*
CPU_DPRSLPVR
PWRBTN*
RSTBTN*
RTC_RST*
PWRGD_SB
PS_PWRGD
CPU_VLD
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
JTAG_TCK
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
HDA_SDATA_OUT
HDA_BITCLK
HDA_RESET*
HDA_SYNC
HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA
SLP_S3*
SLP_RMGT*
SLP_S5*
THERM_DIODE_P
THERM_DIODE_N
MCP_VID0/GPIO_13
MCP_VID1/GPIO_14
MCP_VID2/GPIO_15
SPKR
SMB_CLK0
SMB_DATA0
SMB_CLK1/MSMB_CLK
SMB_DATA1/MSMB_DATA
SMB_ALERT*/GPIO_64
(MGPIO2)
FANRPM0/GPIO_60
FANCTL0/GPIO_61
(MGPIO3)
FANRPM1/GPIO_63
FANCTL1/GPIO_62
CPUVDD_EN
SPI_CS0/GPIO_10
SPI_CLK/GPIO_11
SPI_DI/GPIO_8
SPI_DO/GPIO_9
SUS_CLK/GPIO_34
BUF_SIO_CLK
TEST_MODE_EN
PKG_TEST
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
R2160 0.2K
R2170 22
R2171 22
R2172 22
R2173 22
HDA_SDOUT
HDA_BIT_CLK
HDA_RST_L
HDA_SYNC
R2110 49.9
MCP_HDA_PULLDN_COMP
=PP1V05_S0_MCP_PLL_NV
37 mA (A01)
20 mA
17 mA
=PP3V3_G3_RTC
R2120 49.9K
R2121 49.9K
=SPI_CS1_R_L_USE_MLB
SMC_ADAPTER_EN
TP_SB_A20GATE
TP_MCP_KBDRSTIN_L
SMC_WAKE_SCI_L
SMC_RUNTIME_SCI_L
SM_INTRUDER_L
TP_MCP_LID_L
PM_BATLOW_L
PM_DPRSLPVR
PM_PWRBTN_L
PM_SYSRST_DEBOUNCE_L
RTC_RST_L
PM_RSMRST_L
MCP_PS_PWRGD
MCP_CPU_VLD
JTAG_MCP_TDI
JTAG_MCP_TDO
JTAG_MCP_TMS
JTAG_MCP_TRST_L
JTAG_MCP_TCK
MCP_CLK25M_XTALIN
MCP_CLK25M_XTALOUT
RTC_CLK32K_XTALIN
RTC_CLK32K_XTALOUT
R2150 10K
R2151 100K
MCP_GPIO_4
AUD_I2C_INT_L
PM_SLP_S3_L
PM_SLP_RMGT_L
PM_SLP_S4_L
MCP_THMDIODE_P
MCP_THMDIODE_N
MCP_VID<0>
MCP_VID<1>
MCP_VID<2>
MCP_SPKR
SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA
SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA
AP_PWR_EN
MEM_EVENT_L
ODD_PWR_EN_L
SMC_IG_THROTTLE_L
ARB_DETECT
MCP_CPUVDD_EN
SPI_CS0_R_L
SPI_CLK_R
SPI_MISO
SPI_MOSI_R
PM_CLK32K_SUSCLK_R
TP_MCP_BUF_SIO_CLK
MCP_TEST_MODE_EN
R2163 10K
R2190 1K
=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K
BOOT_MODE_USER
R2181 10K
USER mode: Normal
SAFE mode: For ROMSIP recovery
Connects to SMC for automatic recovery.
BIOS Boot Select
I/F | HDA_SDOUT | LPC_FRAME#
LPC | 0 | 0
PCI | 0 | 1
SPI0 | 1 | 0
SPI1 | 1 | 1
SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.
BUF_SIO_CLK Frequency
Frequency | HDA_SYNC
24 MHz | 1
14.31818 MHz | 0
SPI Frequency Select
Frequency | SPI_DO | SPI_CLK
31 MHz | 0 | 0
42 MHz | 0 | 1
25 MHz | 1 | 0
1 MHz | 1 | 1
NOTE: Straps not provided on this page.
HDA Output Caps
For EMI Reduction on HDA interface
C2170 10PF
C2171 10PF
C2172 10PF
C2173 10PF
=PP3V3_S0_MCP_GPIO
R2140 10K
R2141 10K
R2142 10K
R2143 10K
R2147 100K
=PP3V3_S3_MCP_GPIO
R2154 100K
R2155 22K
R2156 22K
R2157 22K
SYNC MASTER=K24_MLB
SYNC_DATE=03/24/2009
PAGE TITLE
MCP HDA & MISC
Apple Inc.
DRAWING NUMBER 051-7982
SIZE D
REVISION C.0.0
BRANCH
PAGE 21 OF 109
SHEET
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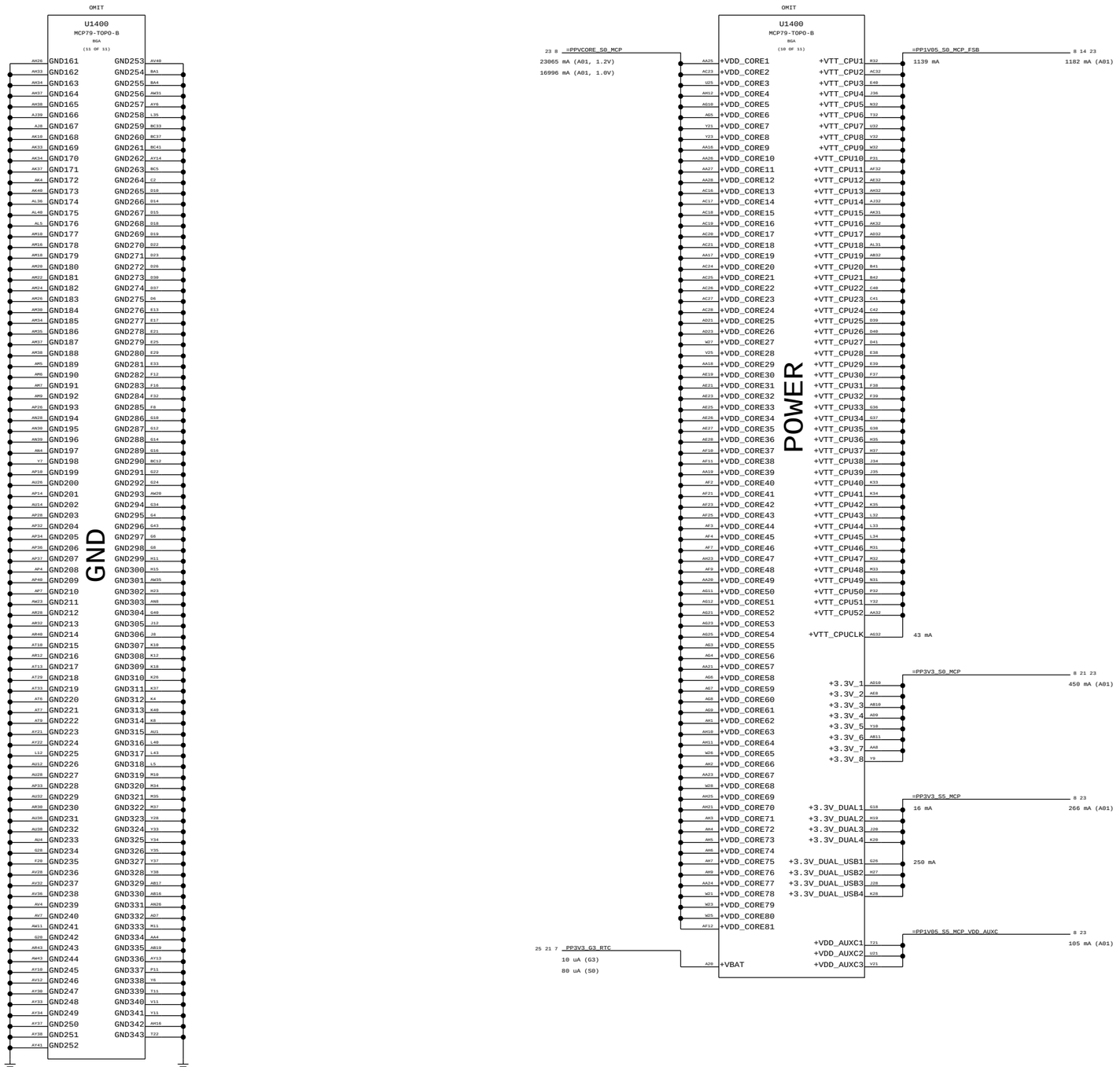


SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

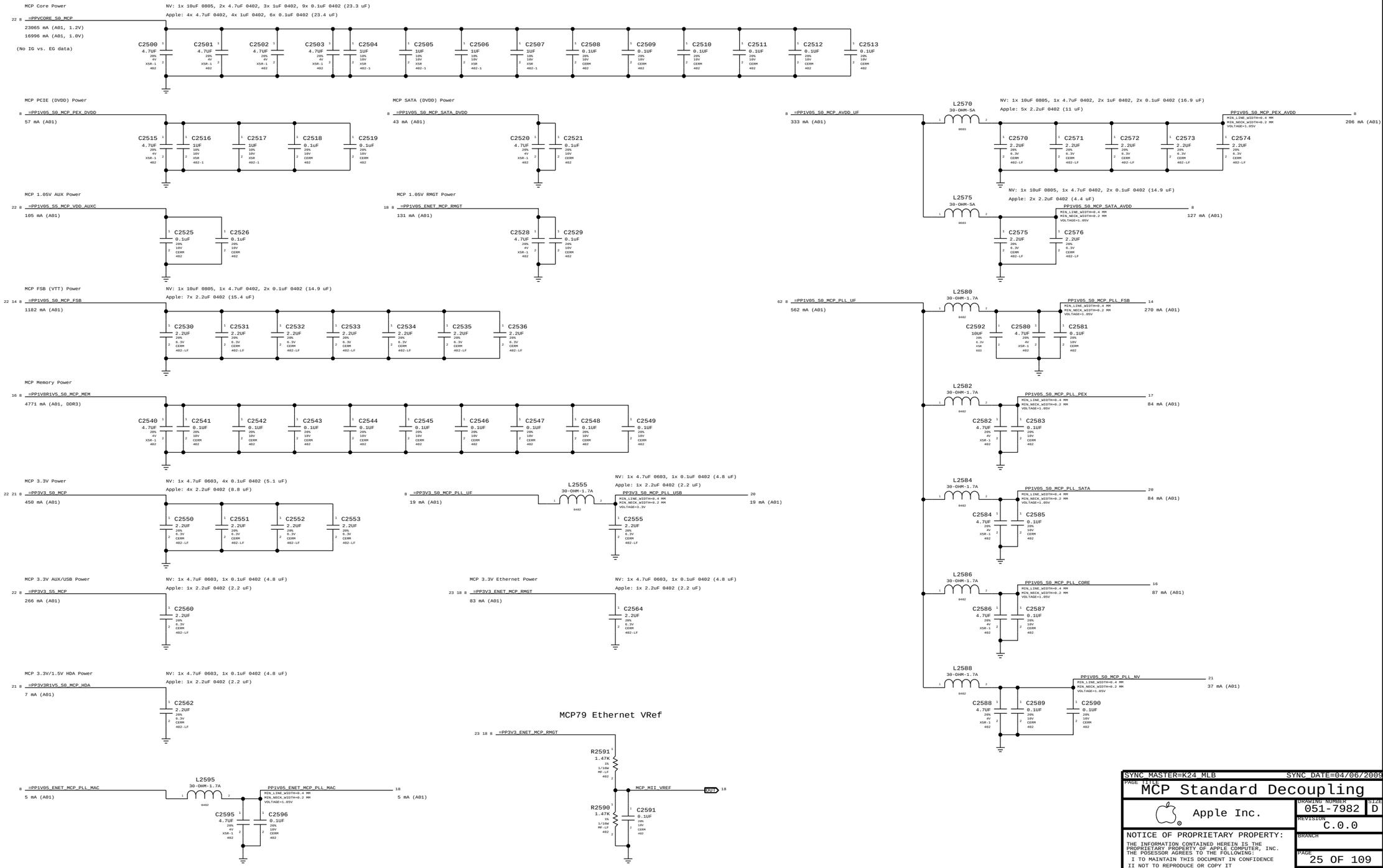
REVISION: C.0.0

BRANCH:

PAGE: 22 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



SYNC MASTER=K24_MLB SYNC DATE=04/06/2009

PAGE TITLE
MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

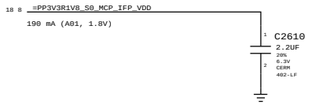
BRANCH

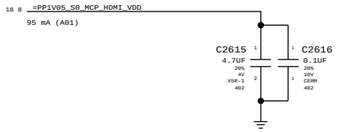
PAGE 25 OF 109

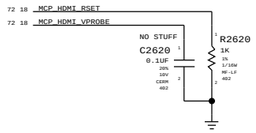
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

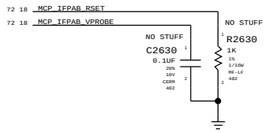
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



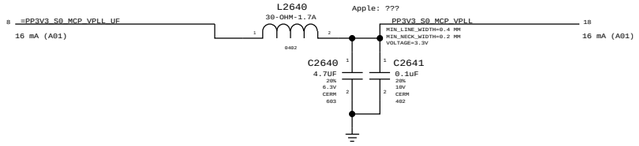




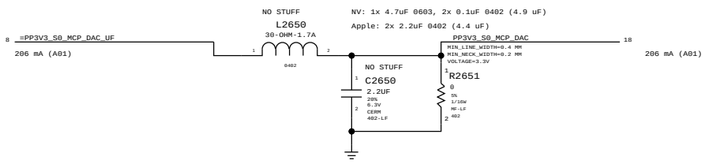


WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)



SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

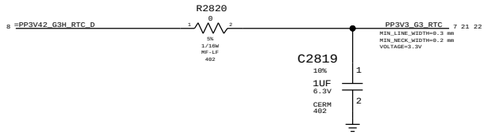
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: MCP Graphics Support

Apple Inc.

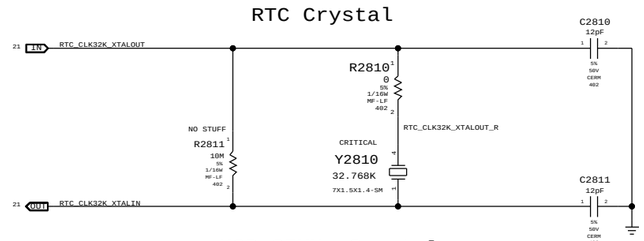
DRAWING NUMBER: 051-7982 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 26 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



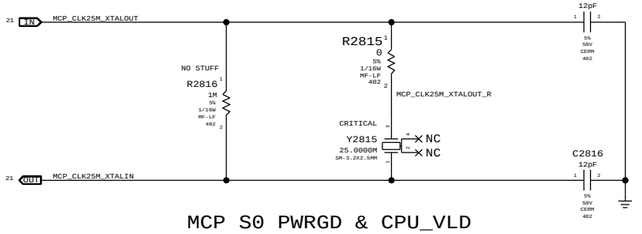
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79

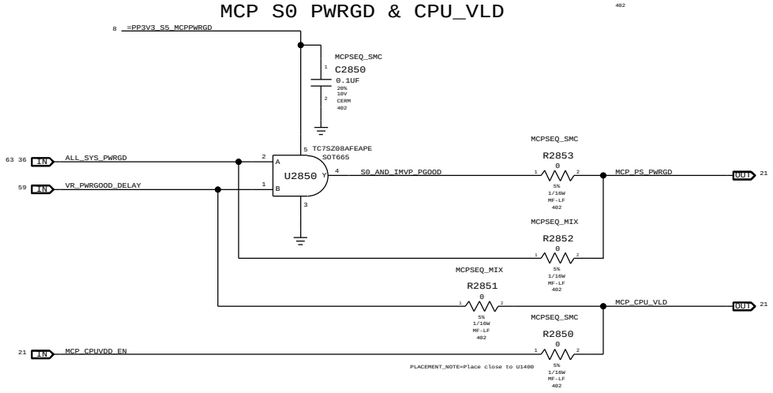
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

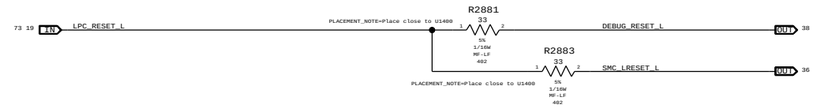
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

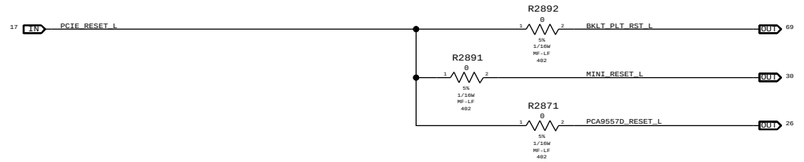
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

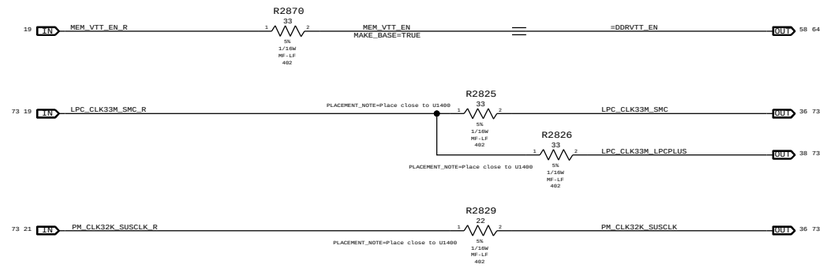
Platform Reset Connections

LPC Reset (Unbuffered)

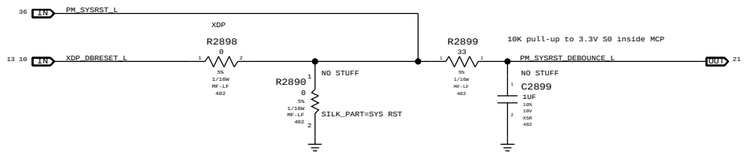


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC_MASTER=K24_MLB SYNC_DATE=02/15/2005

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 28 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

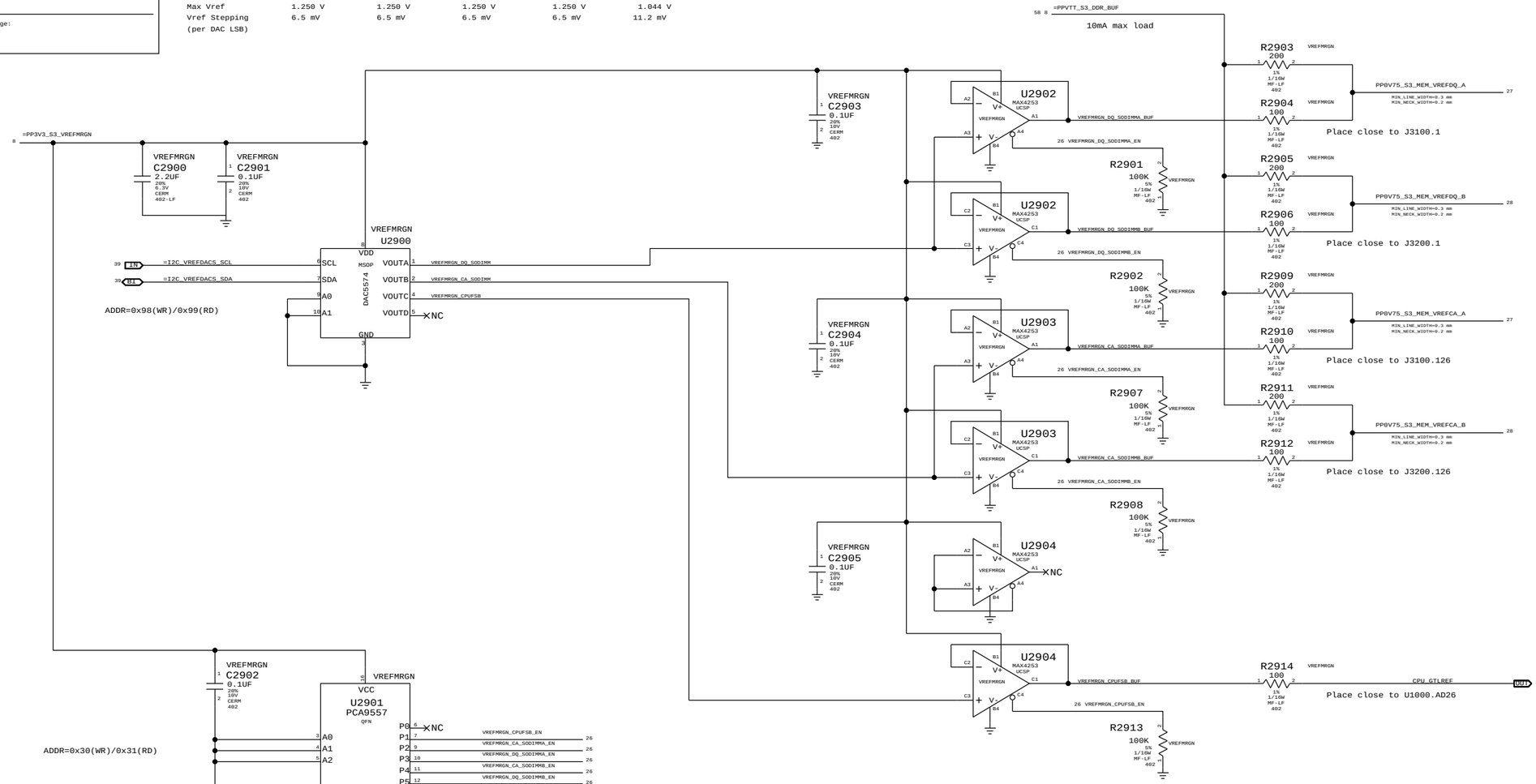
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
REVISION C.0.0
BRANCH
PAGE 29 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

		KEY					
71 15	IN	MEM_A_CKE<0>	73	CKE0	CKE1	74	MEM_A_CKE<1>	IN	15 71
			75	VDD	VDD	76			
		OMIT	77	NC	A15	78	MEM_A_A<15>	IN	9
71 15	IN	MEM_A_BA<2>	79	BA2	A14	80	MEM_A_A<14>	IN	15 71
			81	VDD	VDD	82			
71 15	IN	MEM_A_A<12>	83	A12/BC*	A11	84	MEM_A_A<11>	IN	15 71
71 15	IN	MEM_A_A<9>	85	A9	A7	86	MEM_A_A<7>	IN	15 71
			87	VDD	VDD	88			
71 15	IN	MEM_A_A<8>	89	A8	A6	90	MEM_A_A<6>	IN	15 71
71 15	IN	MEM_A_A<5>	91	A5	A4	92	MEM_A_A<4>	IN	15 71
			93	VDD	VDD	94			
71 15	IN	MEM_A_A<3>	95	A3	A2	96	MEM_A_A<2>	IN	15 71
71 15	IN	MEM_A_A<1>	97	A1	A0	98	MEM_A_A<0>	IN	15 71
			99	VDD	VDD	100			
71 15	IN	MEM_A_CLK_P<0>	101	CK0	CK1	102	MEM_A_CLK_P<1>	IN	15 71
71 15	IN	MEM_A_CLK_N<0>	103	CK0*	CK1*	104	MEM_A_CLK_N<1>	IN	15 71
			105	VDD	VDD	106			
71 15	IN	MEM_A_A<10>	107	A10/AP	BA1	108	MEM_A_BA<1>	IN	15 71
71 15	IN	MEM_A_BA<0>	109	BA0	RAS*	110	MEM_A_RAS_L	IN	15 71
			111	VDD	VDD	112			
71 15	IN	MEM_A_WE_L	113	WE*	S0*	114	MEM_A_CS_L<0>	IN	15 71
71 15	IN	MEM_A_CAS_L	115	CAS*	ODT0	116	MEM_A_ODT<0>	IN	15 71
			117	VDD	VDD	118			
71 15	IN	MEM_A_A<13>	119	A13	ODT1	120	MEM_A_ODT<1>	IN	15 71
71 15	IN	MEM_A_CS_L<1>	121	S1*	NC	122	NC		
			123	VDD	VDD	124			
NC			125	TEST	VREFCA	126			
			127	VSS	VSS	128			
71 15	BI	MEM_A_DQ<34>	129	DQ32	DQ36	130	MEM_A_DQ<37>	BI	15 71
71 15	BI	MEM_A_DQ<35>	131	DQ33	DQ37	132	MEM_A_DQ<36>	BI	15 71
			133	VSS	VSS	134			
71 15	BI	MEM_A_DQS_N<4>	135	DQS4*	DM4	136	MEM_A_DM<4>	IN	15 71
71 15	BI	MEM_A_DQS_P<4>	137	DQS4	VSS	138			
			139	VSS	DQ38	140	MEM_A_DQ<38>	BI	15 71
71 15	BI	MEM_A_DQ<32>	141	DQ34	DQ39	142	MEM_A_DQ<39>	BI	15 71
71 15	BI	MEM_A_DQ<33>	143	DQ35	VSS	144			
			145	VSS	DQ44	146	MEM_A_DQ<41>	BI	15 71
71 15	BI	MEM_A_DQ<44>	147	DQ40	DQ45	148	MEM_A_DQ<40>	BI	15 71
71 15	BI	MEM_A_DQ<45>	149	DQ41	VSS	150			
			151	VSS	DQS5*	152	MEM_A_DQS_N<5>	BI	15 71
71 15	IN	MEM_A_DM<5>	153	DM5	DQS5	154	MEM_A_DQS_P<5>	BI	15 71
			155	VSS	VSS	156			
71 15	BI	MEM_A_DQ<47>	157	DQ42	DQ46	158	MEM_A_DQ<43>	BI	15 71
71 15	BI	MEM_A_DQ<46>	159	DQ43	DQ47	160	MEM_A_DQ<42>	BI	15 71
			161	VSS	VSS	162			
71 15	BI	MEM_A_DQ<49>	163	DQ48	DQ52	164	MEM_A_DQ<53>	BI	15 71
71 15	BI	MEM_A_DQ<52>	165	DQ49	DQ53	166	MEM_A_DQ<48>	BI	15 71
			167	VSS	VSS	168			
71 15	BI	MEM_A_DQS_N<6>	169	DQS6*	DM6	170	MEM_A_DM<6>	IN	15 71
71 15	BI	MEM_A_DQS_P<6>	171	DQS6	VSS	172			
			173	VSS	DQ54	174	MEM_A_DQ<55>	BI	15 71
71 15	BI	MEM_A_DQ<54>	175	DQ50	DQ55	176	MEM_A_DQ<50>	BI	15 71
71 15	BI	MEM_A_DQ<51>	177	DQ51	VSS	178			
			179	VSS	DQ60	180	MEM_A_DQ<57>	BI	15 71
71 15	BI	MEM_A_DQ<61>	181	DQ56	DQ61	182	MEM_A_DQ<56>	BI	15 71
71 15	BI	MEM_A_DQ<60>	183	DQ57	VSS	184			
			185	VSS	DQS7*	186	MEM_A_DQS_N<7>	BI	15 71
71 15	IN	MEM_A_DM<7>	187	DM7	DQS7	188	MEM_A_DQS_P<7>	BI	15 71
			189	VSS	VSS	190			
71 15	BI	MEM_A_DQ<58>	191	DQ58	DQ62	192	MEM_A_DQ<62>	BI	15 71
71 15	BI	MEM_A_DQ<59>	193	DQ59	DQ63	194	MEM_A_DQ<63>	BI	15 71
			195	VSS	VSS	196			
		MEM_A_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT	21 28 36
			199	VDDSPD	SDA	200	=I2C_SODIMMA_SDA	BI	39
		MEM_A_SA<1>	201	SA1	SCL	202	=I2C_SODIMMA_SCL	IN	39
			203	VTT	VTT	204			

516-0201

SPD ADDR=0xA0(WR)/0xA1(RD)

8 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

8 =PP0V75_S0_MEM_VTT_A

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

26 PP0V75_S3_MEM_VREFCA_A

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)

			1	VREFDQ	VSS	2			
		OMIT	3	VSS	DQ4	4	MEM_A_DQ<4>	BI	15 71
71 15	BI	MEM_A_DQ<0>	5	DQ0	DQ5	6	MEM_A_DQ<5>	BI	15 71
71 15	BI	MEM_A_DQ<1>	7	DQ1	VSS	8			
		CRITICAL	9	VSS	DQS0*	10	MEM_A_DQS_N<0>	BI	15 71
71 15	IN	MEM_A_DM<0>	11	DM0	DQS0	12	MEM_A_DQS_P<0>	BI	15 71
			13	VSS	VSS	14			
71 15	BI	MEM_A_DQ<6>	15	DQ2	DQ6	16	MEM_A_DQ<3>	BI	15 71
71 15	BI	MEM_A_DQ<7>	17	DQ3	DQ7	18	MEM_A_DQ<2>	BI	15 71
			19	VSS	VSS	20			
71 15	BI	MEM_A_DQ<14>	21	DQ8	DQ12	22	MEM_A_DQ<9>	BI	15 71
71 15	BI	MEM_A_DQ<11>	23	DQ9	DQ13	24	MEM_A_DQ<8>	BI	15 71
			25	VSS	VSS	26			
71 15	BI	MEM_A_DQS_N<1>	27	DQS1*	DM1	28	MEM_A_DM<1>	IN	15 71
71 15	BI	MEM_A_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN	28 29
			31	VSS	VSS	32			
71 15	BI	MEM_A_DQ<13>	33	DQ10	DQ14	34	MEM_A_DQ<15>	BI	15 71
71 15	BI	MEM_A_DQ<12>	35	DQ11	DQ15	36	MEM_A_DQ<10>	BI	15 71
			37	VSS	VSS	38			
71 15	BI	MEM_A_DQ<25>	39	DQ16	DQ20	40	MEM_A_DQ<24>	BI	15 71
71 15	BI	MEM_A_DQ<29>	41	DQ17	DQ21	42	MEM_A_DQ<28>	BI	15 71
			43	VSS	VSS	44			
71 15	BI	MEM_A_DQS_N<3>	45	DQS2*	DM2	46	MEM_A_DM<3>	IN	15 71
71 15	BI	MEM_A_DQS_P<3>	47	DQS2	VSS	48			
			49	VSS	DQ22	50	MEM_A_DQ<27>	BI	15 71
71 15	BI	MEM_A_DQ<26>	51	DQ18	DQ23	52	MEM_A_DQ<31>	BI	15 71
71 15	BI	MEM_A_DQ<30>	53	DQ19	VSS	54			
			55	VSS	DQ28	56	MEM_A_DQ<18>	BI	15 71
71 15	BI	MEM_A_DQ<20>	57	DQ24	DQ29	58	MEM_A_DQ<17>	BI	15 71
71 15	BI	MEM_A_DQ<21>	59	DQ25	VSS	60			
			61	VSS	DQS3*	62	MEM_A_DQS_N<2>	BI	15 71
71 15	IN	MEM_A_DM<2>	63	DM3	DQS3	64	MEM_A_DQS_P<2>	BI	15 71
			65	VSS	VSS	66			
71 15	BI	MEM_A_DQ<23>	67	DQ26	DQ30	68	MEM_A_DQ<22>	BI	15 71
71 15	BI	MEM_A_DQ<16>	69	DQ27	DQ31	70	MEM_A_DQ<19>	BI	15 71
			71	VSS	VSS	72			

516-0201

"Factory" (top) slot

SYNC MASTER=K24 MLB	SYNC DATE=02/05/2009
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 31 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- +PP1V5_S0_MEM_B
- +PP1V5_S3_MEM_B
- +PP0V75_S0_MEM_VTT_B
- +PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402

26 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3 — OMIT

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204
205	MTG PIN	MTG PIN	206
207	MTG PIN	MTG PIN	208
209	MTG PIN	MTG PIN	210
211	MTG PIN	MTG PIN	212

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3 — OMIT CRITICAL

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

516S0706

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B 26

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

8 =PPSPD_S0_MEM_B
MEM_B_SA<0>
MEM_B_SA<1>
MTG PINS
=PP0V75_S0_MEM_VTT_B 8

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

DDR3 GROUND RETURN CAPS (MCP SIDE)

8 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402
C3224 0.1UF 20% 10V CERM 402
C3225 0.1UF 20% 10V CERM 402
C3226 0.1UF 20% 10V CERM 402
C3227 0.1UF 20% 10V CERM 402
C3228 0.1UF 20% 10V CERM 402
C3229 0.1UF 20% 10V CERM 402

"Expansion" (bottom) slot

SYNC MASTER=K24 MLB — SYNC DATE=02/05/2009

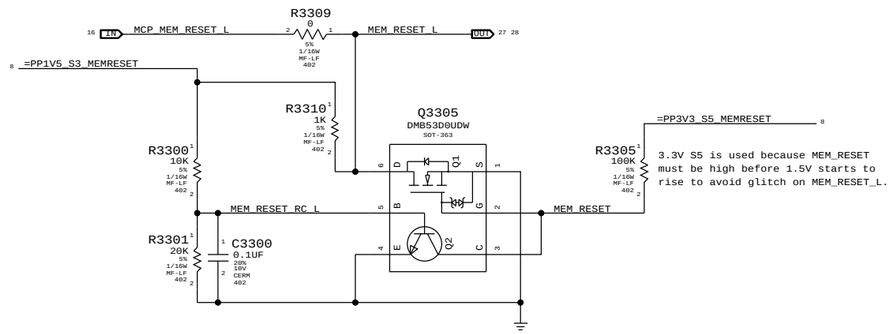
PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

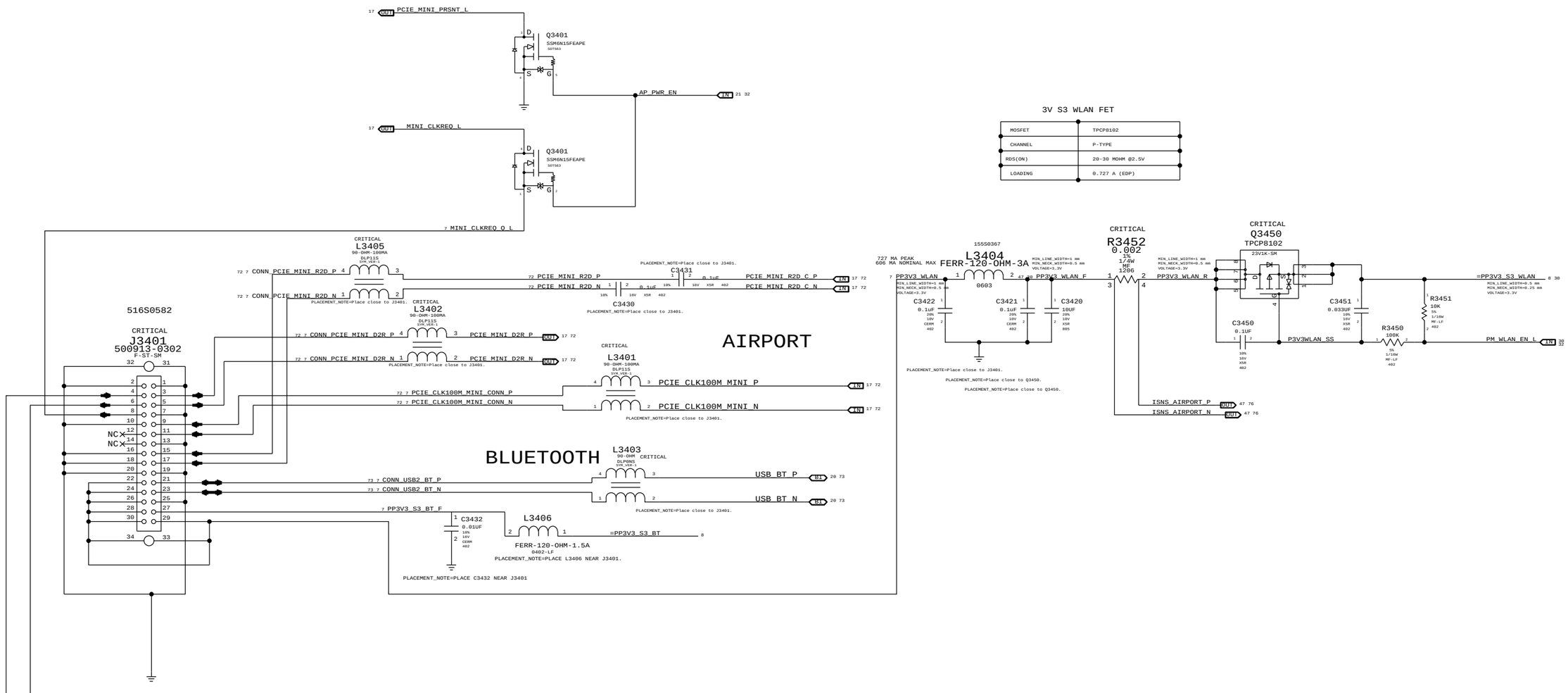
DRAWING NUMBER: 051-7982 — SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 32 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC_MASTER=K24_MLB	SYNC_DATE=04/06/2009
PAGE TITLE: DDR3 Support	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 33 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K24_MLB SYNC_DATE=01/27/2009

PAGE TITLE

X16 WIRELESS CONNECTOR

Apple Inc.

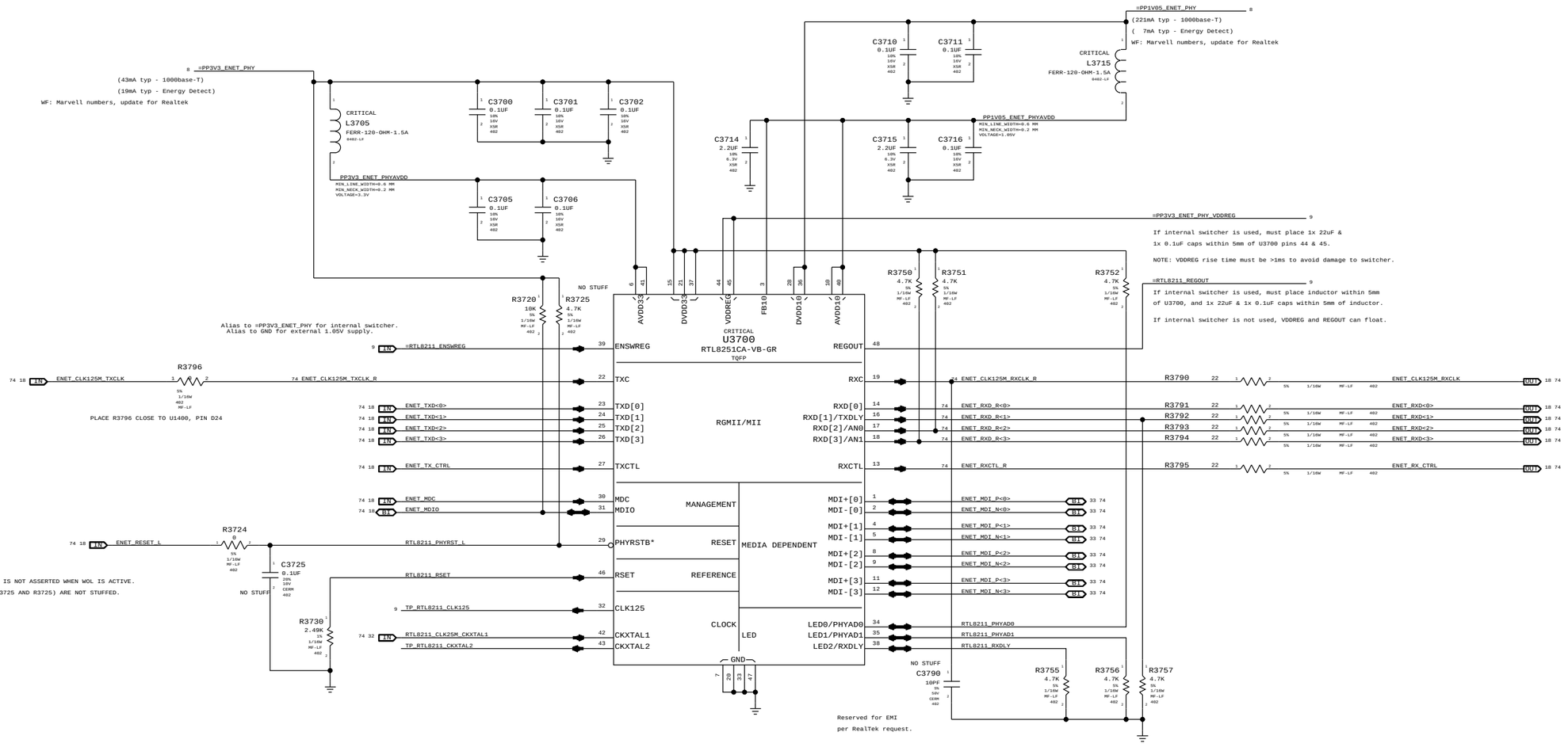
DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

BRANCH

PAGE 34 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
Ethernet PHY (RTL8211CL)

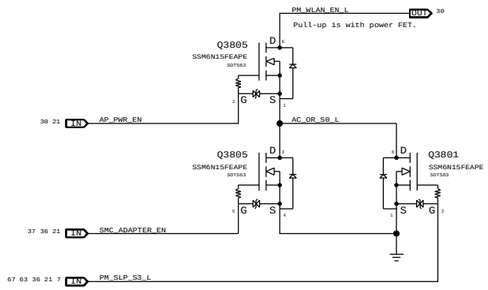
Apple Inc.

DRAWING NUMBER 051-7982
SIZE D
REVISION C.0.0
BRANCH
PAGE 37 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

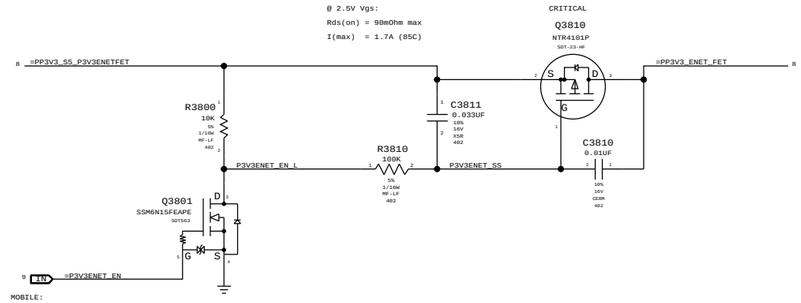
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



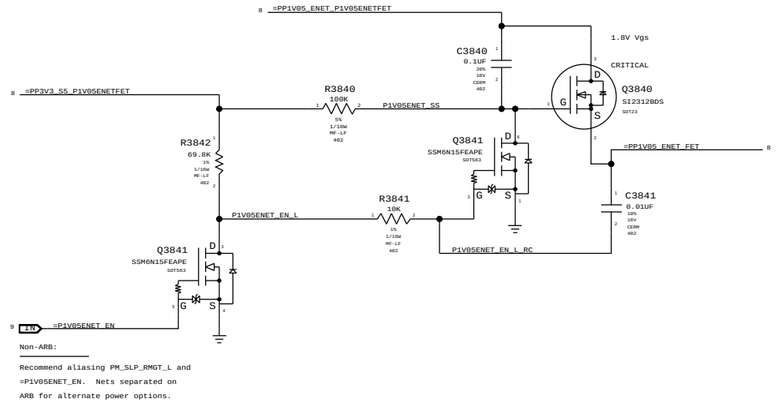
3.3V ENET FET



MOBILE:

Recommend aliasing PM_SLP_RMGT_L and
=P3V3ENET_EN. Nets separated on
ARB for alternate power options.

1.05V ENET FET

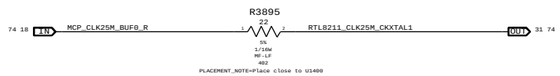


Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and
=P1V05ENET_EN. Nets separated on
ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE
Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER 051-7982
SIZE D
REVISION C.0.0
BRANCH
PAGE 38 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V XSR 402
C3901 0.1UF 10% 16V XSR 402
C3902 0.1UF 10% 16V XSR 402
C3903 0.1UF 10% 16V XSR 402

CRITICAL
T3901 SM
TX
TLA-6T213HF
RX

CRITICAL
T3902 SM
TX
TLA-6T213HF
RX

74 31 B1 ENET_MDI_P<1>
74 31 B1 ENET_MDI_N<1>
74 31 B1 ENET_MDI_P<3>
74 31 B1 ENET_MDI_N<3>
74 31 B1 ENET_MDI_N<2>
74 31 B1 ENET_MDI_P<2>
74 31 B1 ENET_MDI_N<0>
74 31 B1 ENET_MDI_P<0>

ENET_CENTER_TAP<1> R3903 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<3> R3902 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<2> R3901 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<0> R3900 75 1% 1/16W MF-LF 402

74 ENET_MDI_TRAN_P<1>
74 ENET_MDI_TRAN_N<1>
74 ENET_MDI_TRAN_P<3>
74 ENET_MDI_TRAN_N<3>
74 ENET_MDI_TRAN_N<2>
74 ENET_MDI_TRAN_P<2>
74 ENET_MDI_TRAN_N<0>
74 ENET_MDI_TRAN_P<0>

ETHERNET CONNECTOR

OMIT
CRITICAL
J3900
RJ45-10/100TX-K83
F-R-TH

ENET_MDI
1 TRAN_P0
2 TRAN_N0
3 TRAN_P1
4 TRAN_P2
5 TRAN_N2
6 TRAN_N1
7 TRAN_P3
8 TRAN_N3
9 SHIELD PINS
10
11
12

514-0692

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

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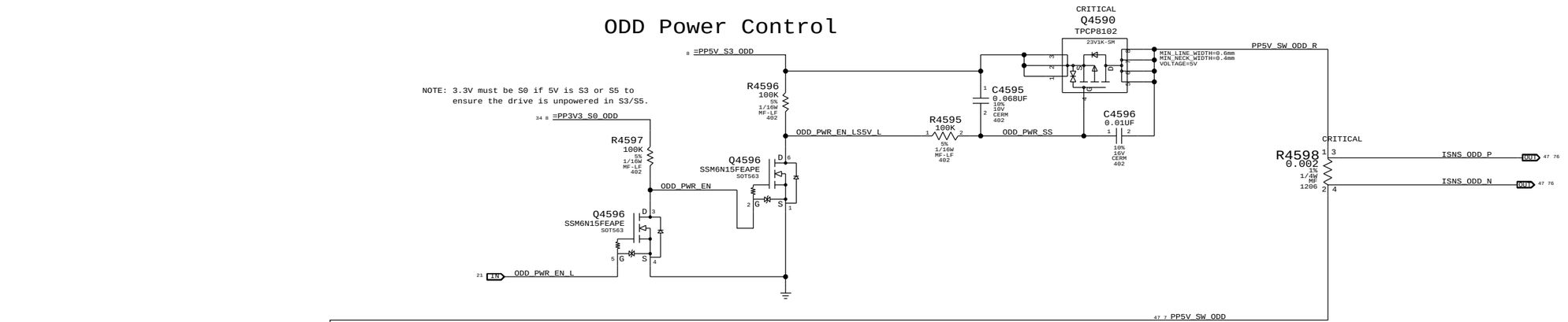
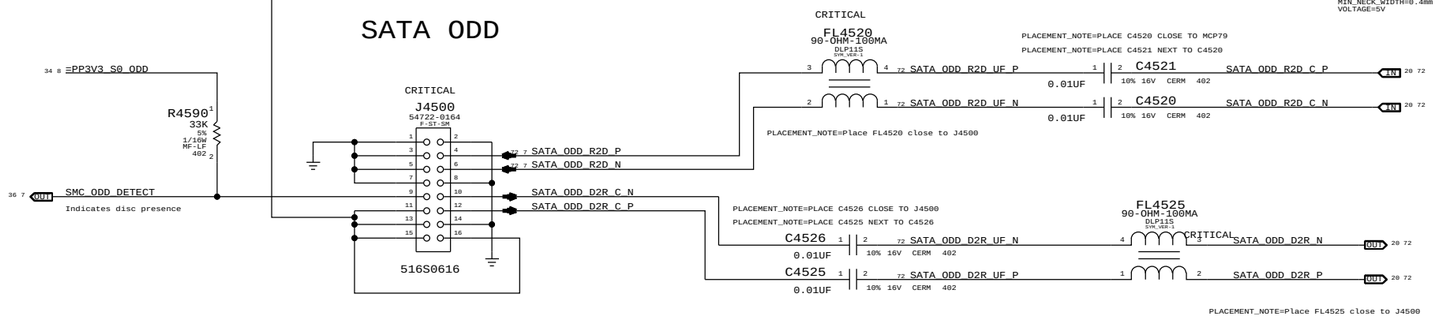
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

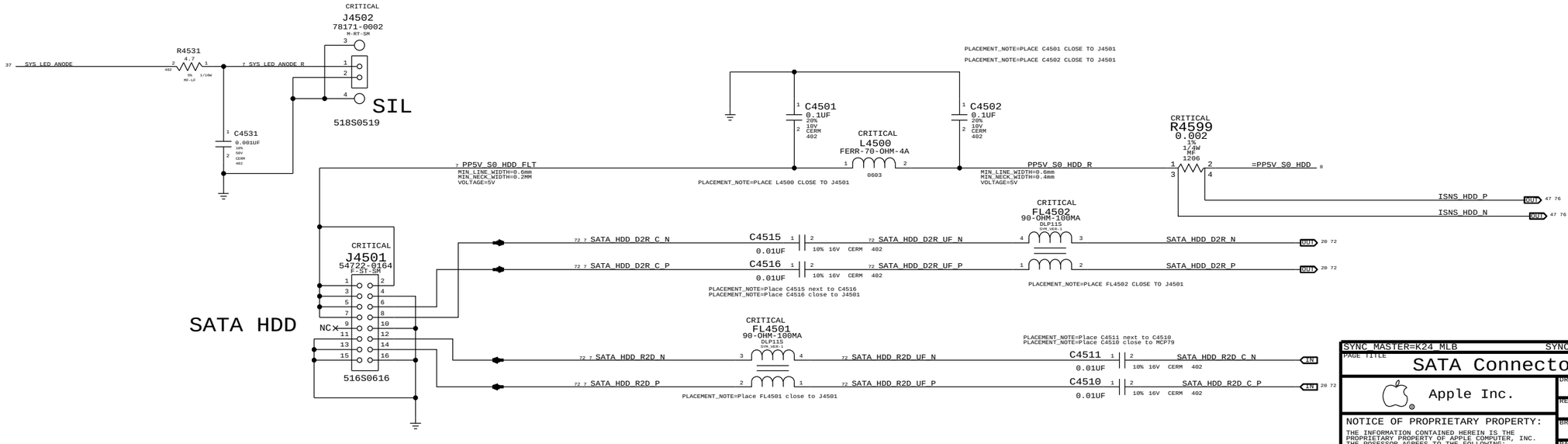
ODD Power Control



SATA ODD



SATA HDD



SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE

SATA Connectors

Apple Inc.

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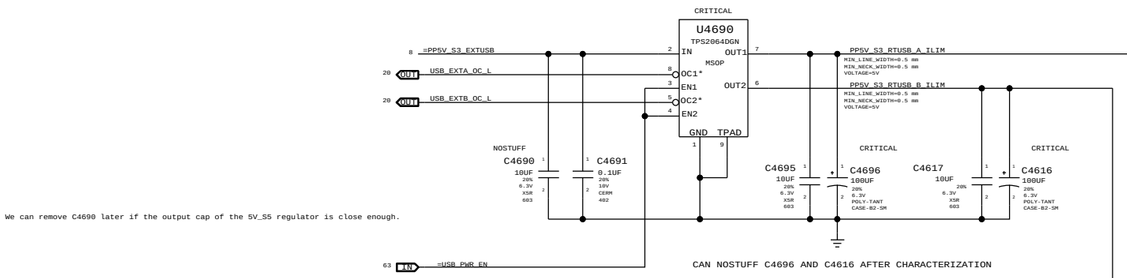
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

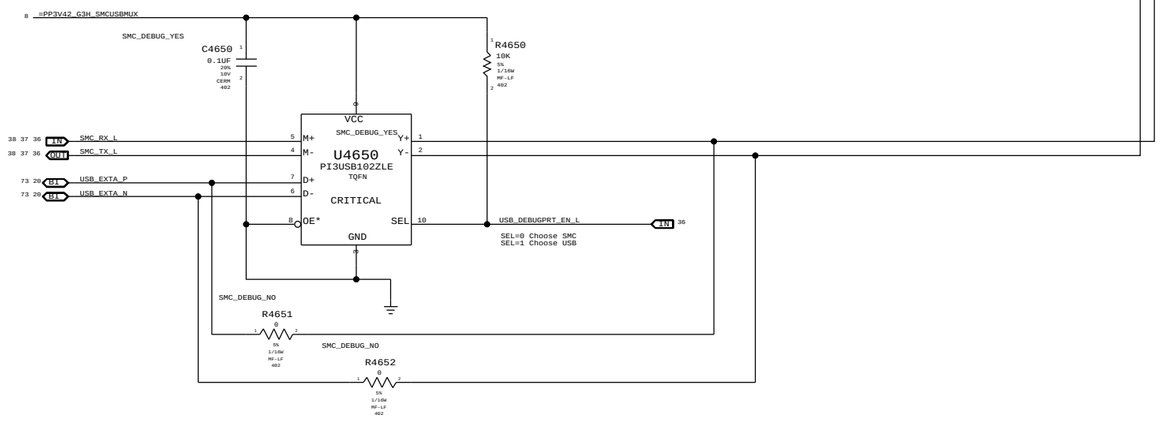
POR IS PLASTIC USB CONNECTOR PARTS BUT METAL PART'S SCHEMATIC AND CAD SYMBOLS
HAVE BEEN USED AS ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch

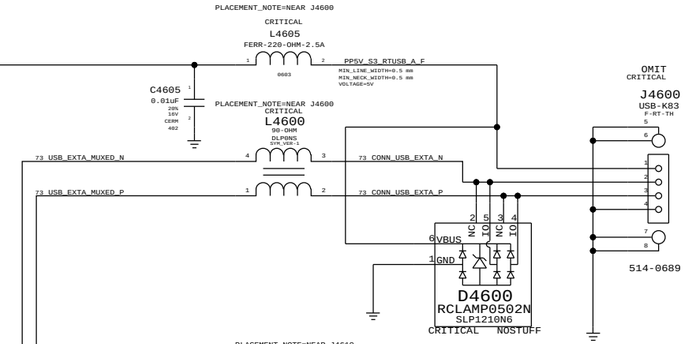


We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

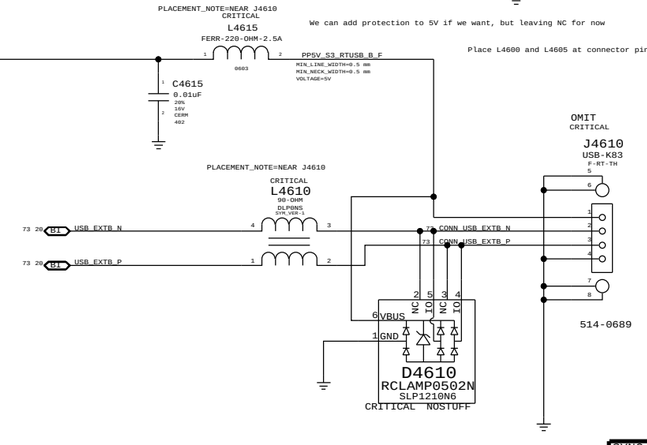
USB/SMC Debug Mux



USB PORT A (FRONT PORT)



USB PORT B (BACK PORT)



SYNC_MASTER=K24_MLB	SYNC_DATE=02/05/2009
PAGE TITLE: External USB Connectors	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
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	BRANCH:
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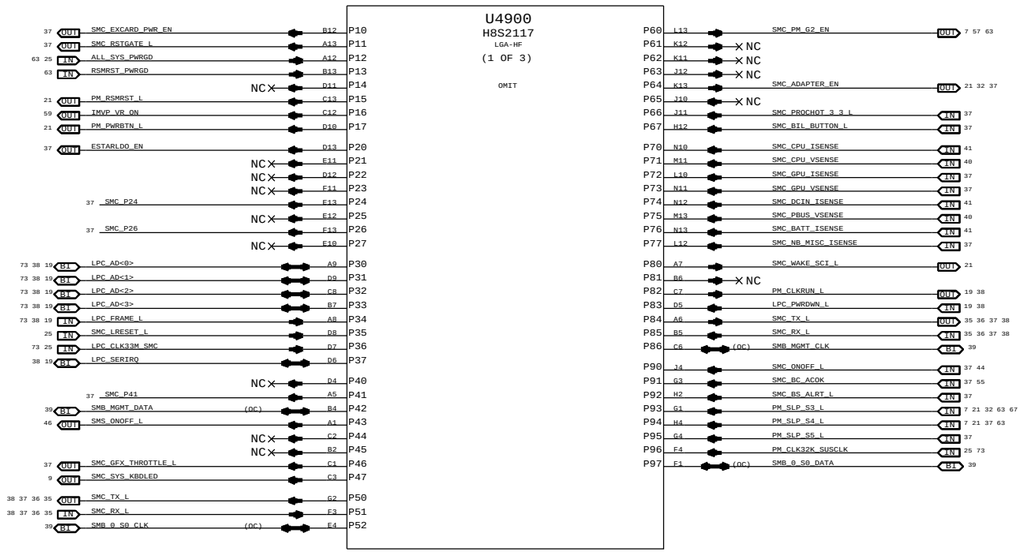
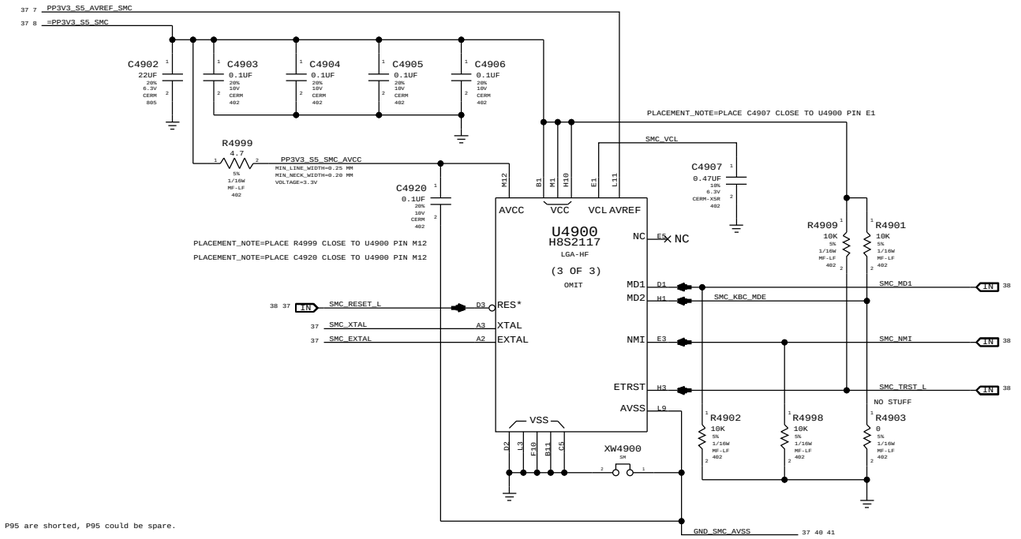
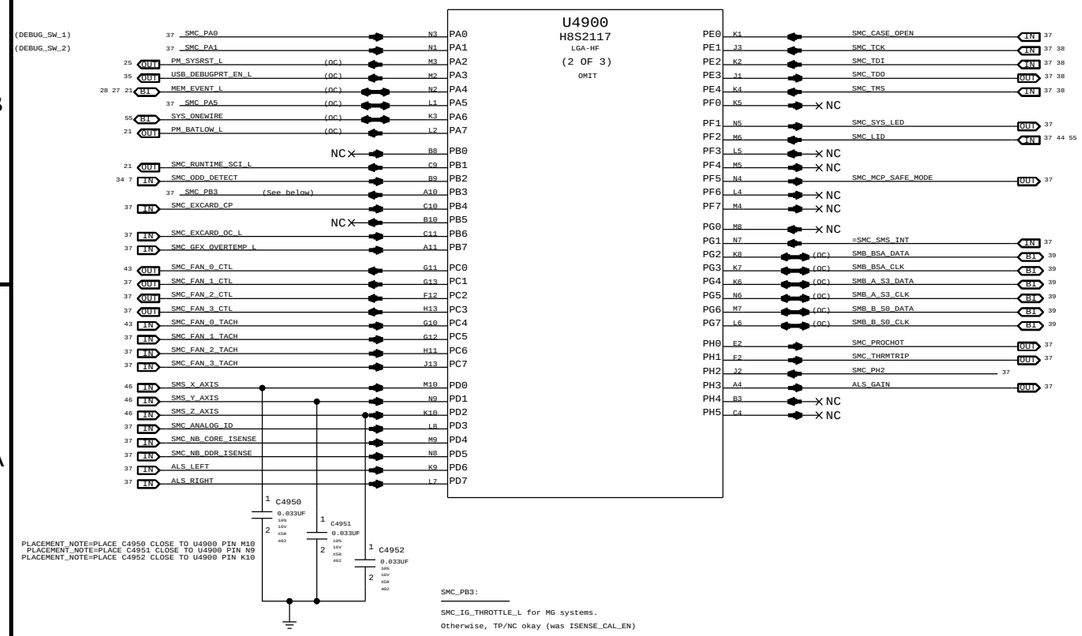
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



(DEBUG_SW_1)
(DEBUG_SW_2)

PLACEMENT_NOTE=PLACE C4950 CLOSE TO U4900 PIN M10
PLACEMENT_NOTE=PLACE C4951 CLOSE TO U4900 PIN N9
PLACEMENT_NOTE=PLACE C4952 CLOSE TO U4900 PIN K10

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K24_MLB	SYNC_DATE=04/02/2009
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
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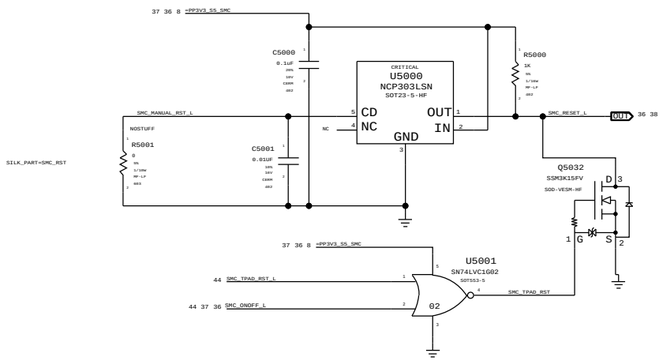
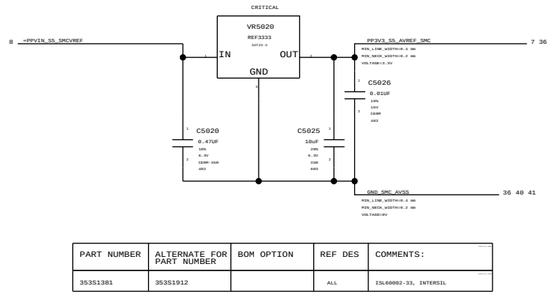
SMC Reset "Button" / Brownout Detect

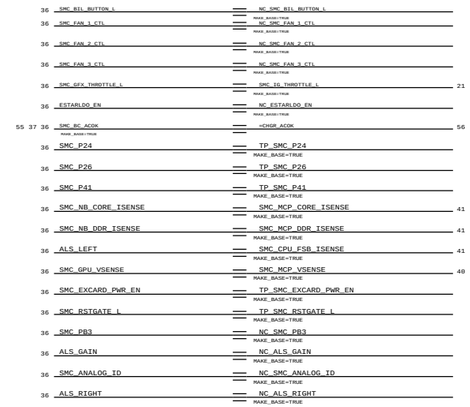


SMC AVREF Supply

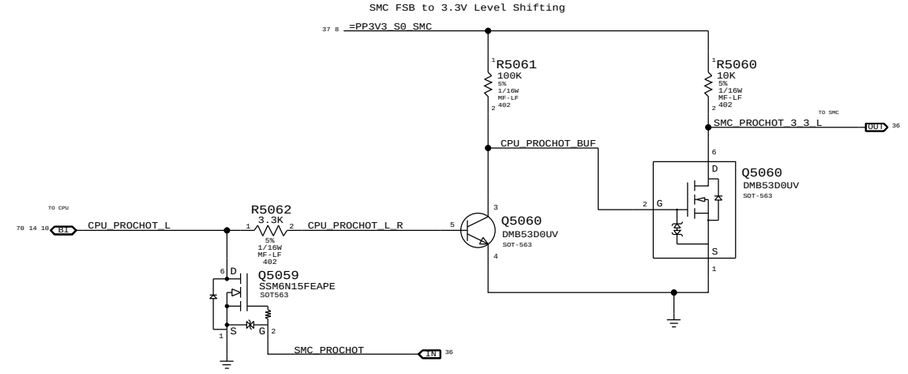


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

SMC_MCP_CORE_ISENSE

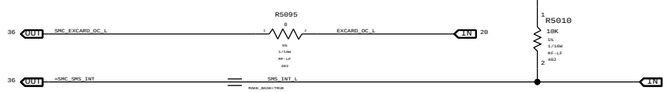


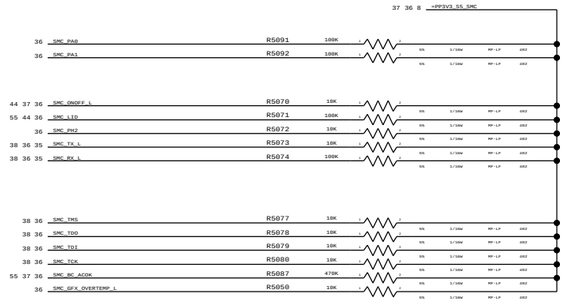
SMC FSB to 3.3V Level Shifting



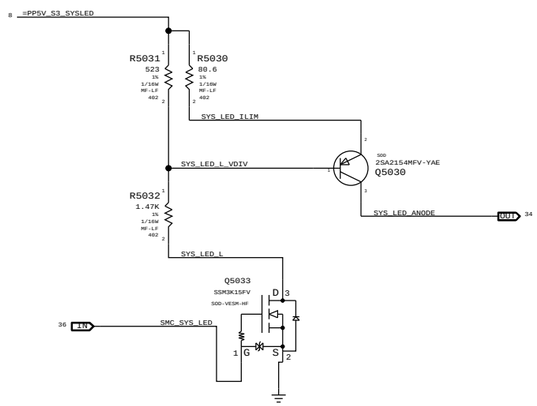
MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345

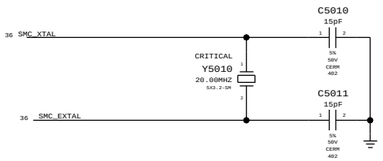




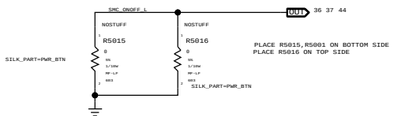
System (Sleep) LED Circuit



SMC Crystal Circuit



Debug Power "Button"



SYNC MASTER=K24_MLB	SYNC DATE=02/04/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
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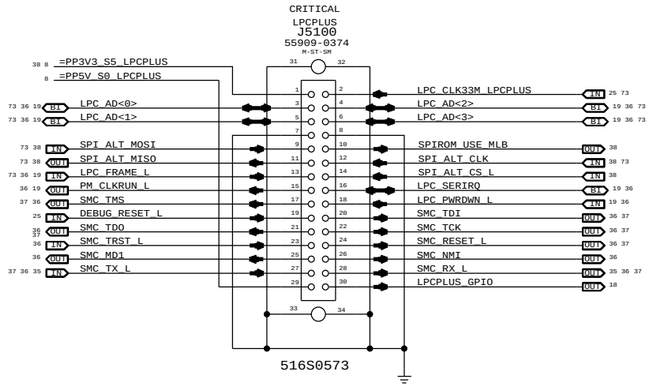
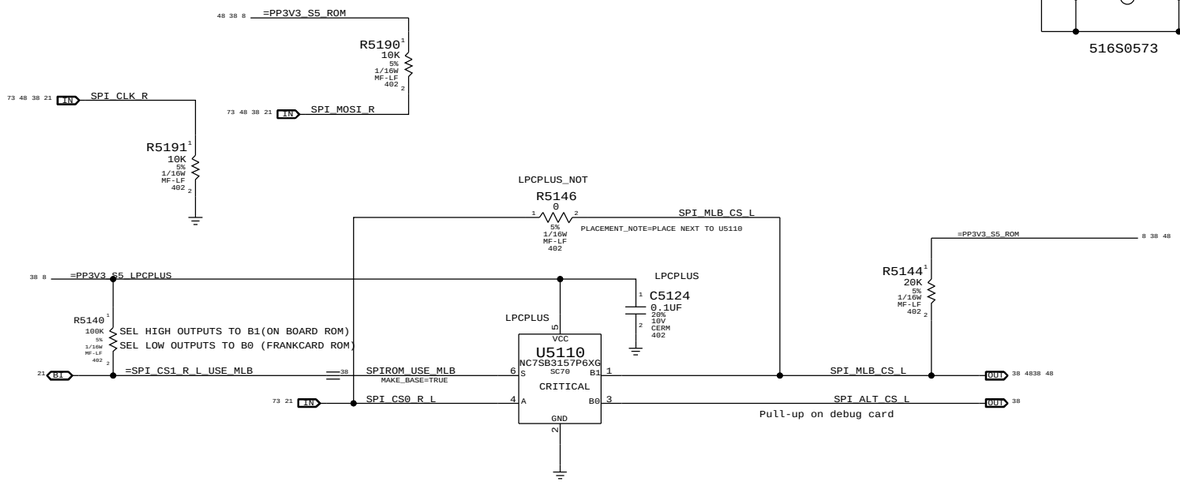
LPC+SPI Connector



Alternate SPI ROM Support



SYNC_MASTER=K24_MLB SYNC_DATE=02/15/2009

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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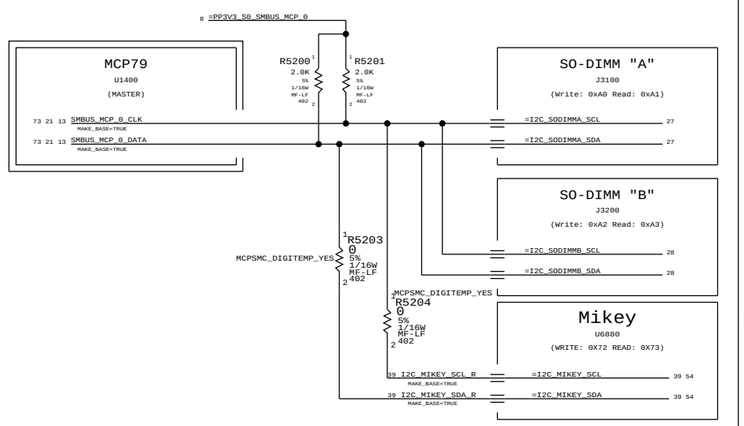
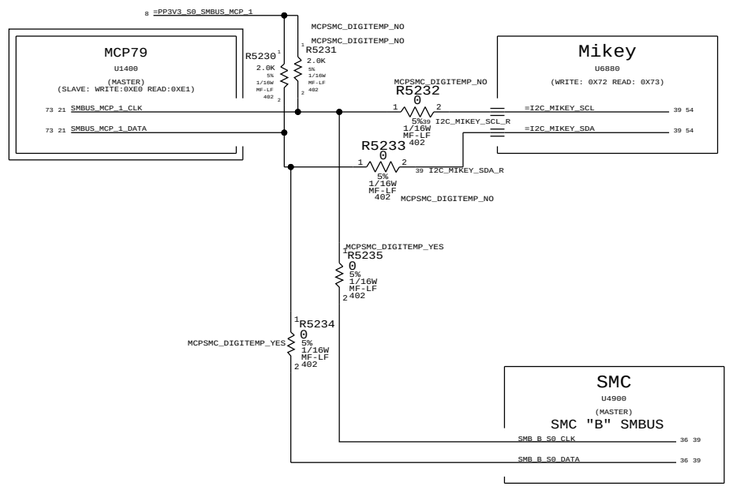
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP79 SMBUS "0" CONNECTIONS

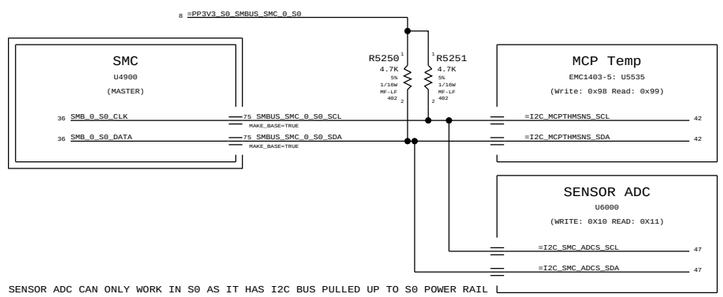


MCP79 SMBUS "1" CONNECTIONS



MCP SMBUS1 ACTS AS SLAVE DEVICE FOR MCPSMC_DIGITEMP_YES STUFFED

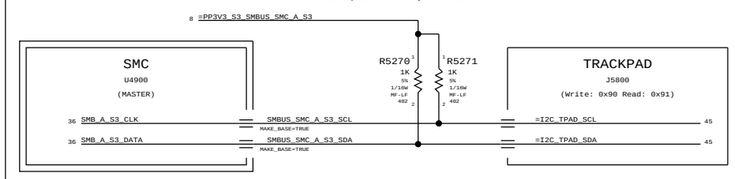
SMC "0" SMBus Connections



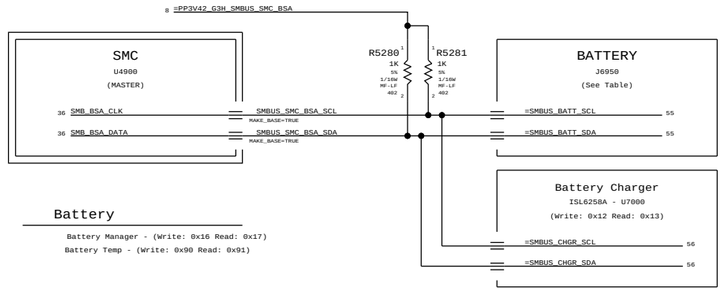
SENSOR ADC CAN ONLY WORK IN S0 AS IT HAS I2C BUS PULLED UP TO S0 POWER RAIL

SMC "A" SMBus Connections

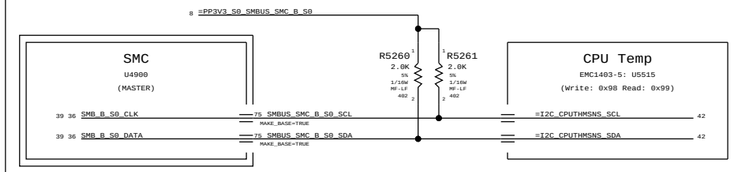
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "Battery A" SMBus Connections



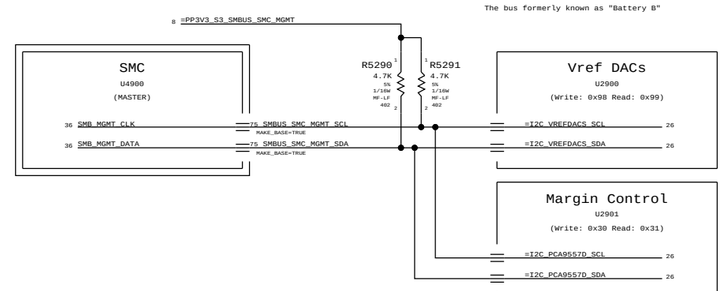
SMC "B" SMBus Connections



SMC "B" SMBUS SIGNALS ALSO GET CONNECTED TO MCP SMBUS 1 CONNECTIONS(SEE LEFT SIDE)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE
K84 SMBUS CONNECTIONS

Apple Inc.

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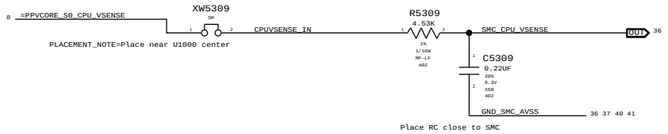
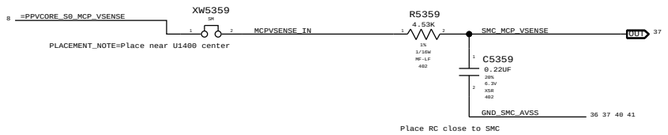
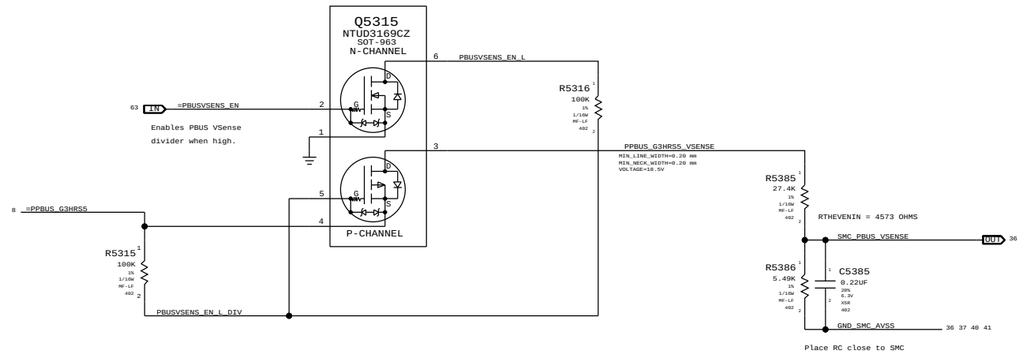
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



SYNC MASTER=K24 MLB SYNC DATE=04/06/2009

PAGE TITLE

VOLTAGE SENSING

Apple Inc.

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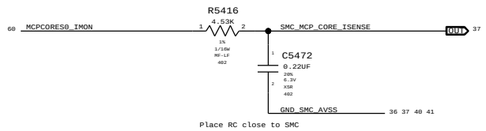
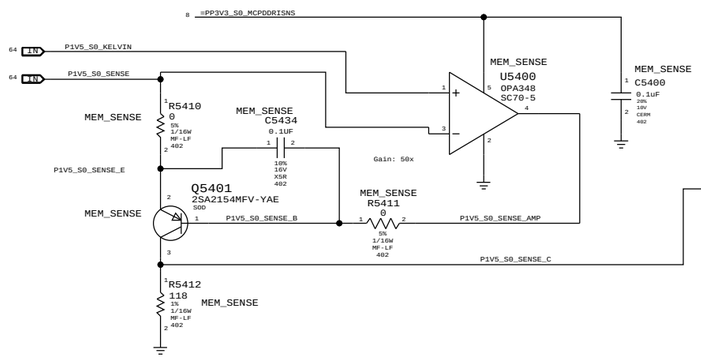
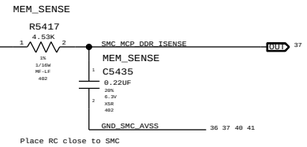
MCP VCore Current Sense Filter



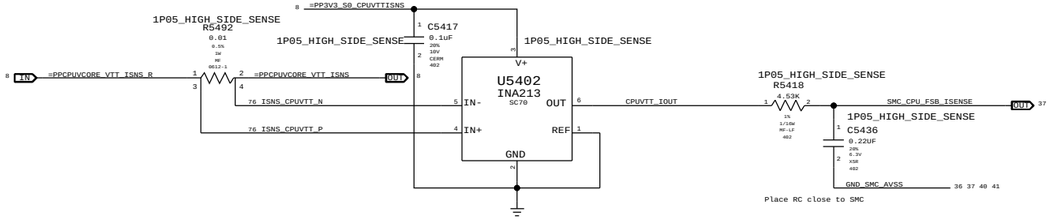
MCP MEM VDD Current Sense



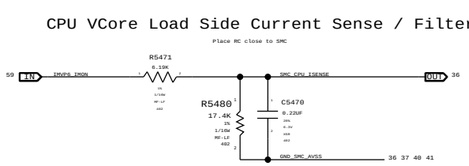
MCP MEM VDD Current Sense Filter



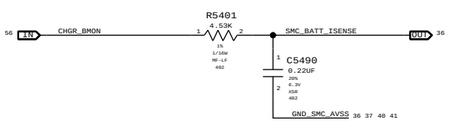
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



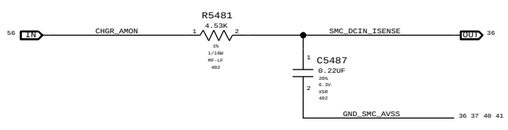
CPU VCore Load Side Current Sense / Filter



DC-IN (BMON) CURRENT SENSE



DC-IN (AMON) CURRENT SENSE



SYNC MASTER=K24_MLB SYNC DATE=01/27/2009

PAGE TITLE

Current Sensing

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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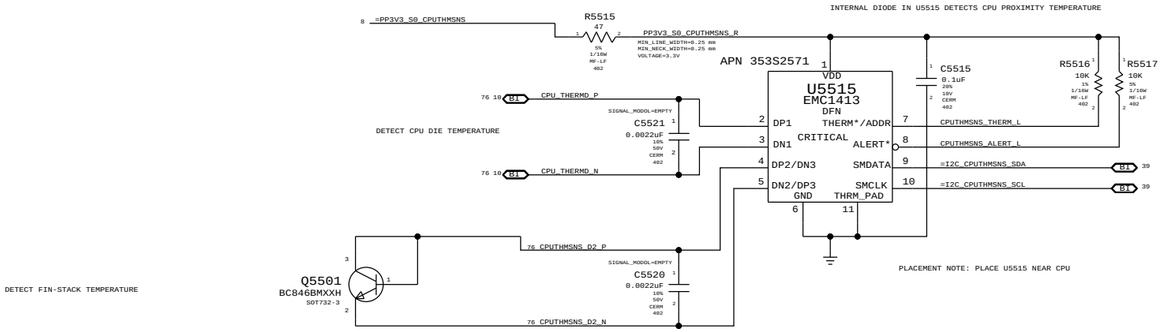
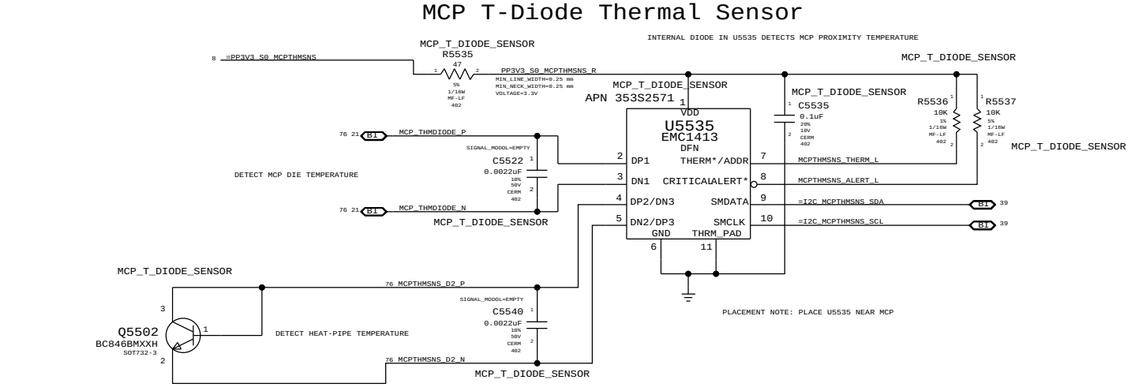
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



PLACEMENT_NOTE=PLACE CLOSE TO J4501 IN A CONVENIENT LOCATION

SYNC_MASTER=K24_MLB SYNC_DATE=02/04/2009

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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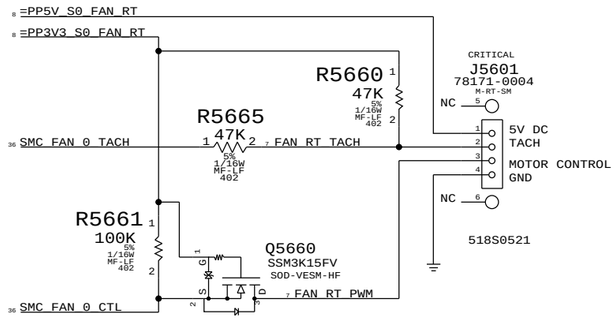
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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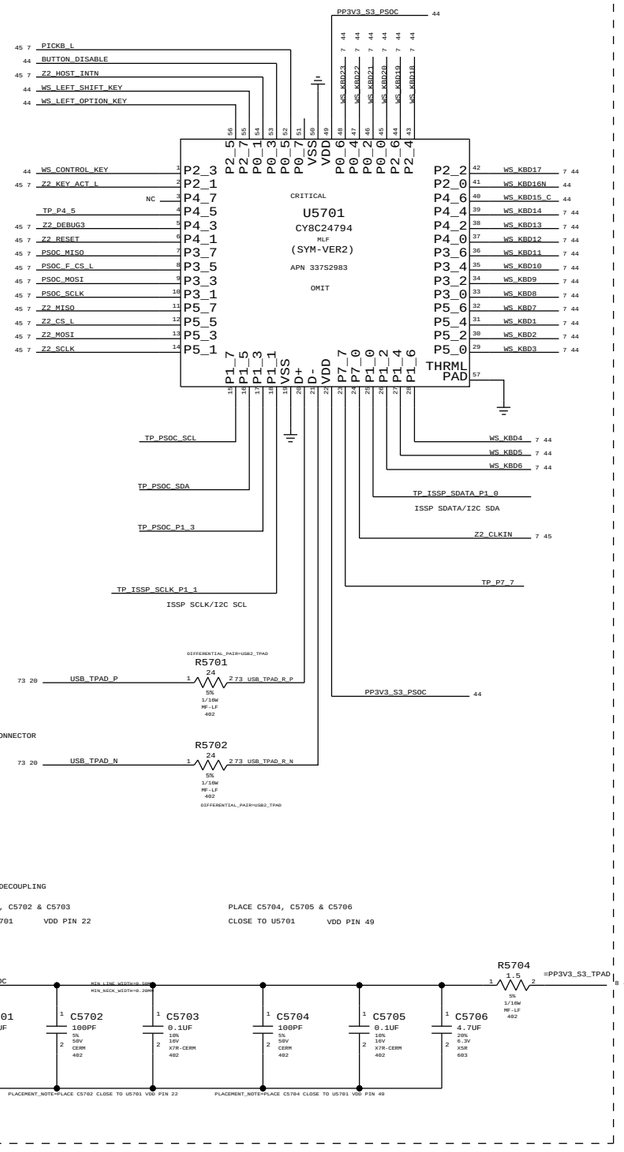
PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER



U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

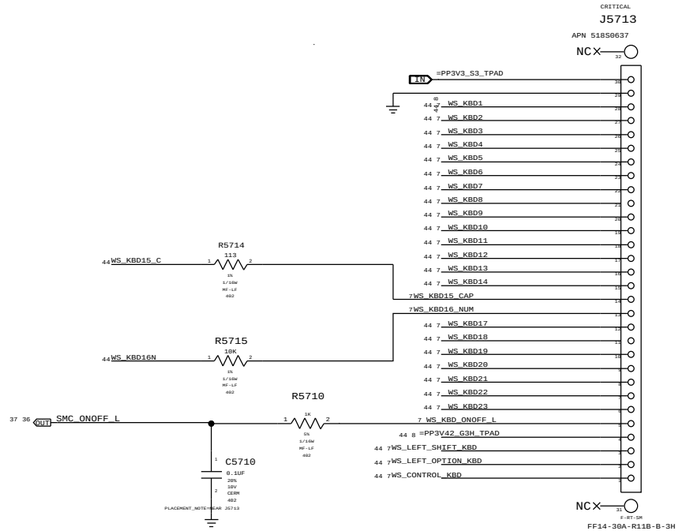
ISOLATION CIRCUIT

TPAD BUTTONS DISABLE

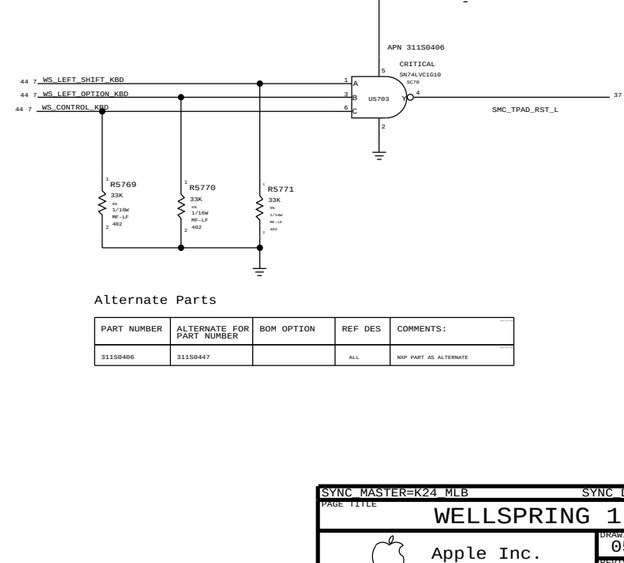
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

SYNC MASTER=K24 MLB
SYNC DATE=03/04/2009

PAGE TITLE
WELLSPRING 1

Apple Inc.

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REVISION C.0.0
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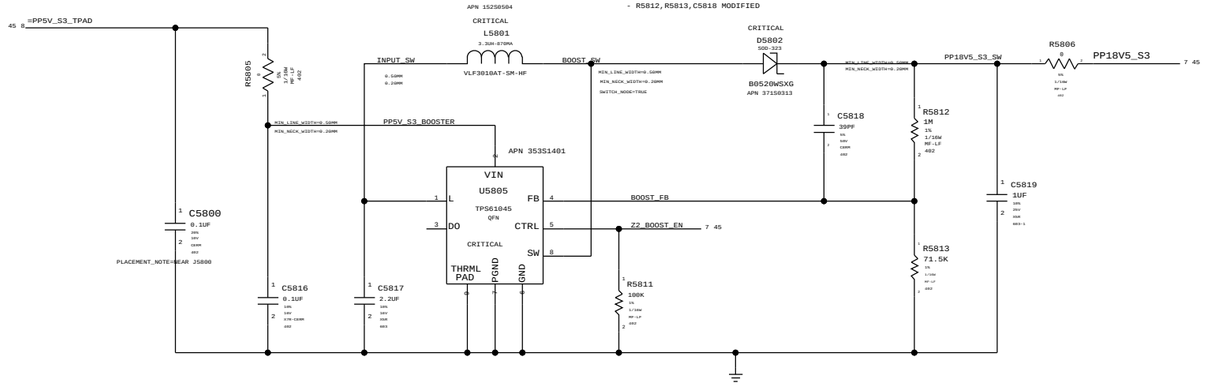
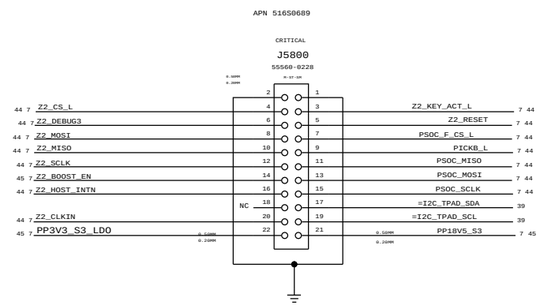
BOOSTER +18.5VDC FOR SENSORS

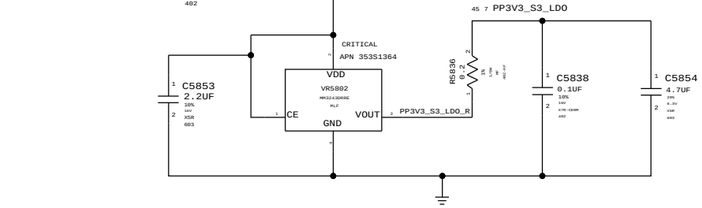
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- RS812,RS813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



SYNC MASTER=K24 MLB SYNC DATE=02/25/2009

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

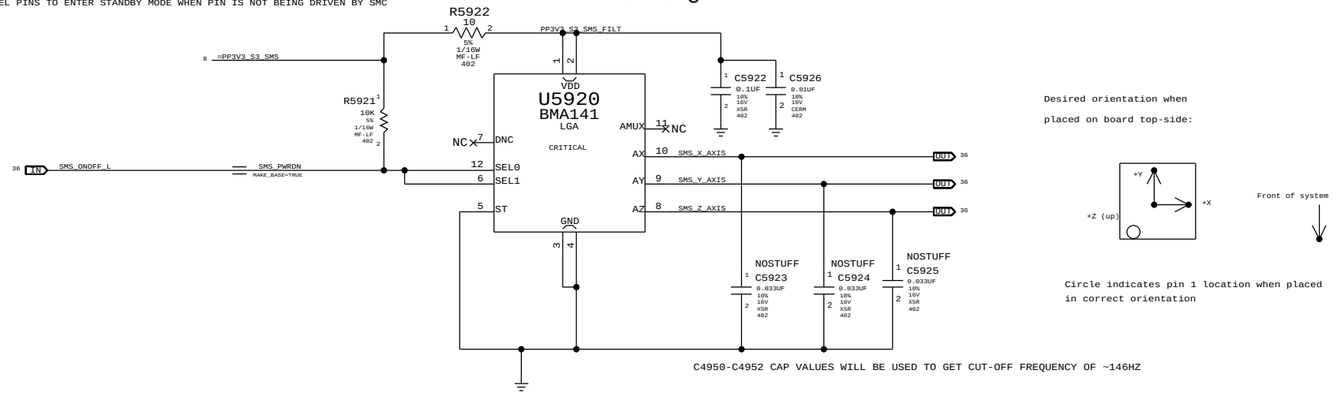
BRANCH:

PAGE: 58 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Analog SMS

R5921 PULLS UP SEL PINS TO ENTER STANDBY MODE WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:

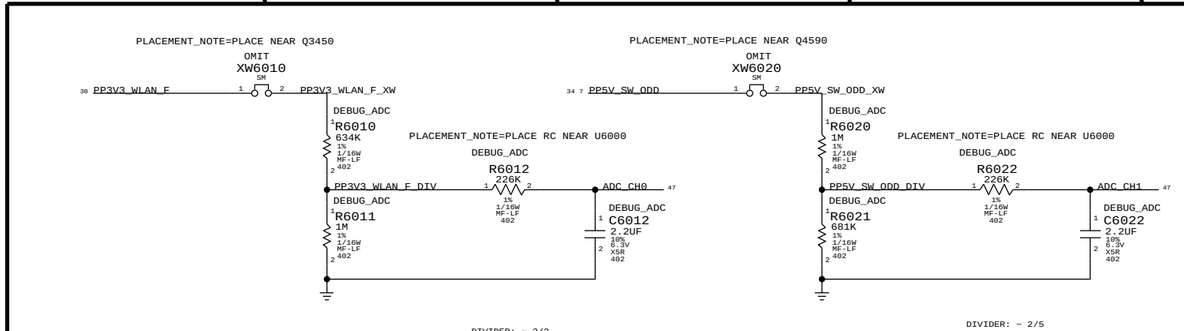
Circle indicates pin 1 location when placed in correct orientation

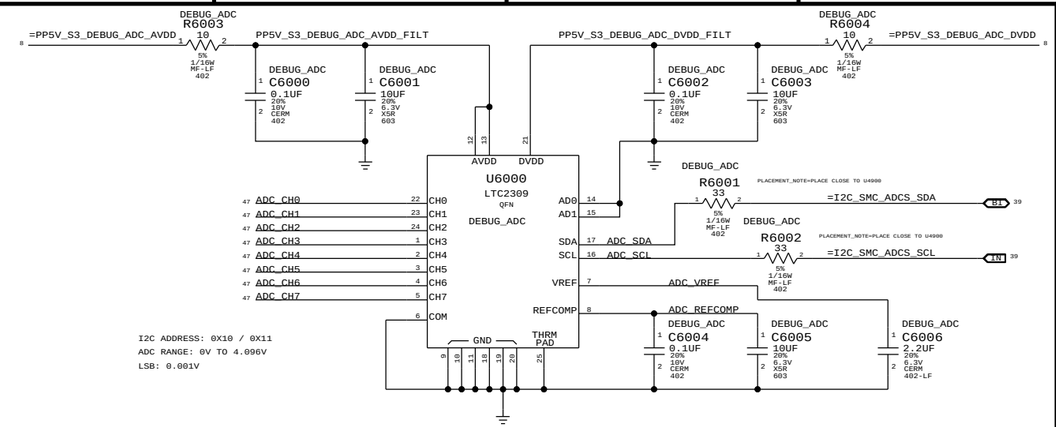
C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ

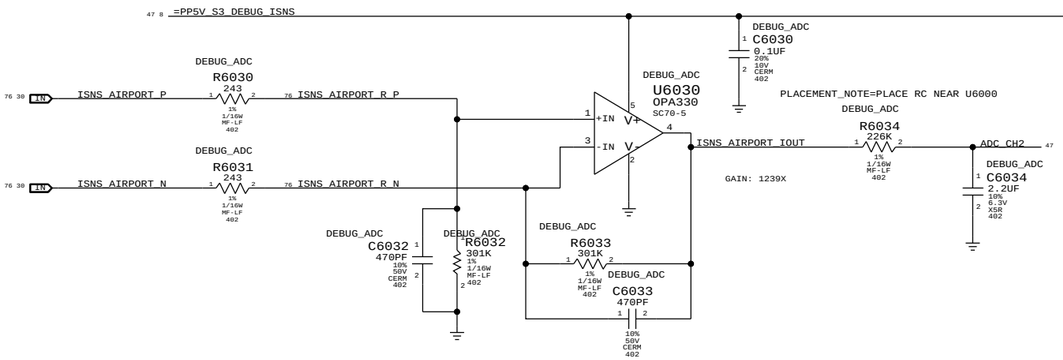
PAGE TITLE: SMS

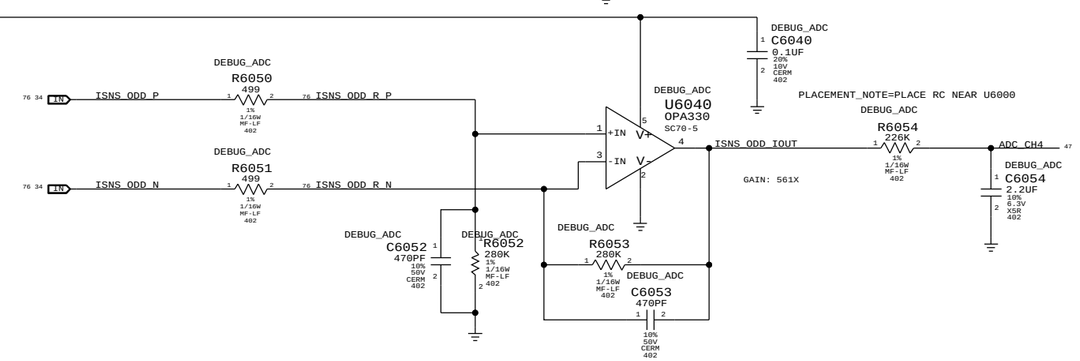
Apple Inc.

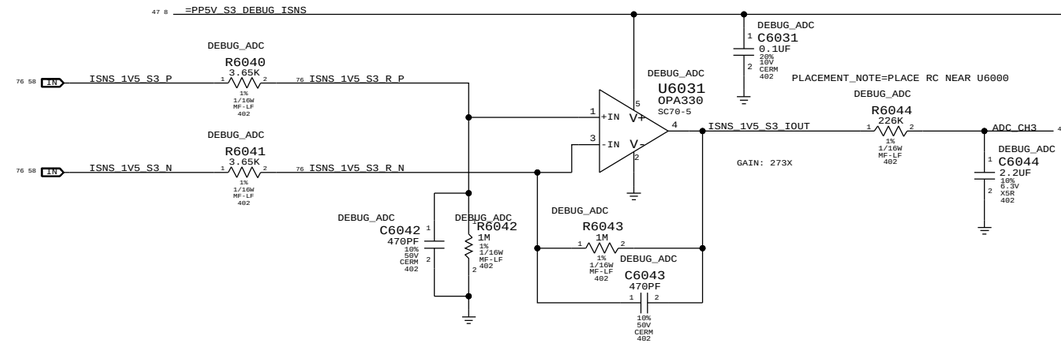
DRAWING NUMBER: 051-7982
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 59 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

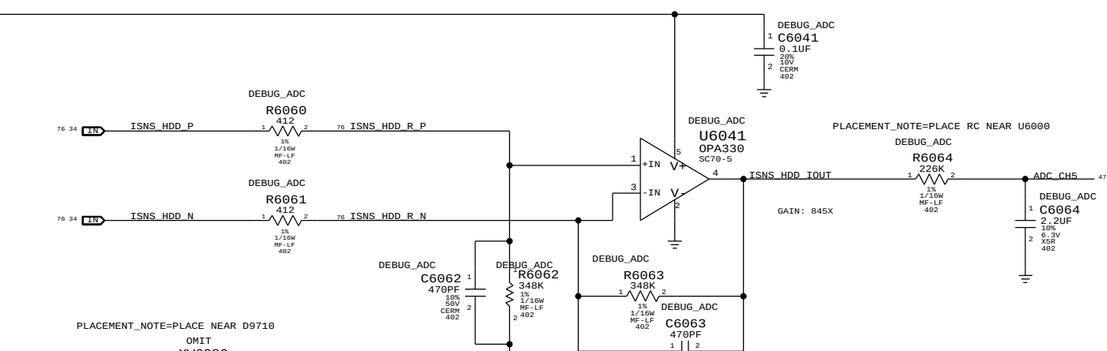


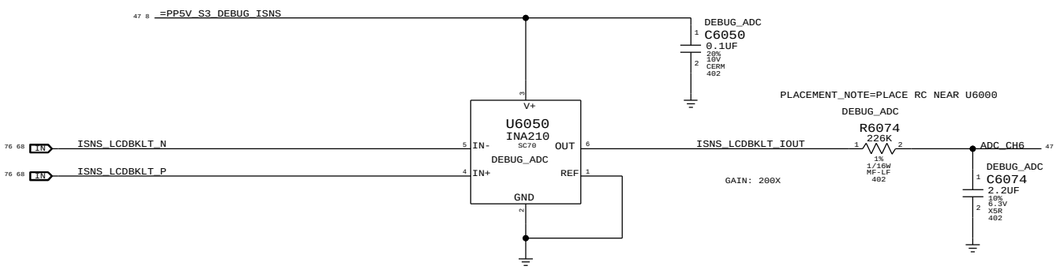


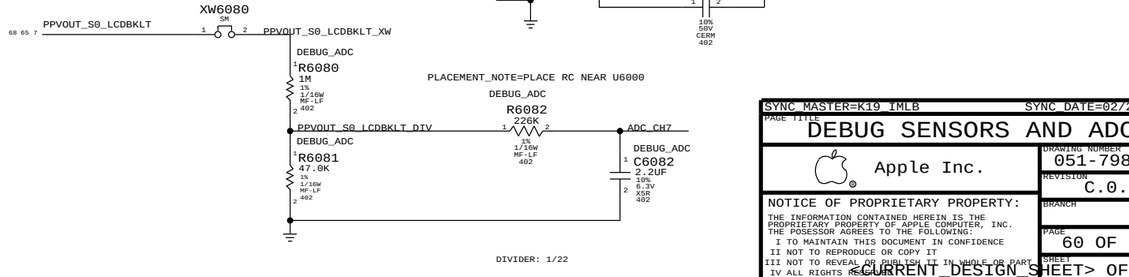












SYNC_MASTER=K19_IMLB SYNC_DATE=02/25/2009

PAGE TITLE

DEBUG SENSORS AND ADC

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

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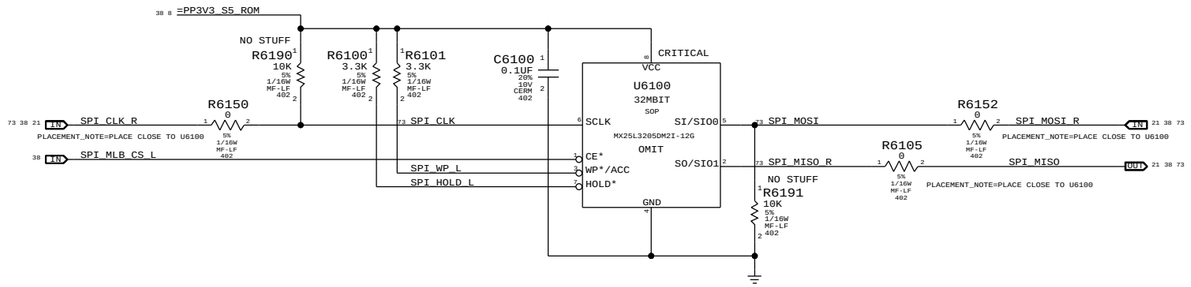
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SYNC MASTER=K24_MLB SYNC DATE=02/15/2009

PAGE TITLE

SPI ROM

Apple Inc.

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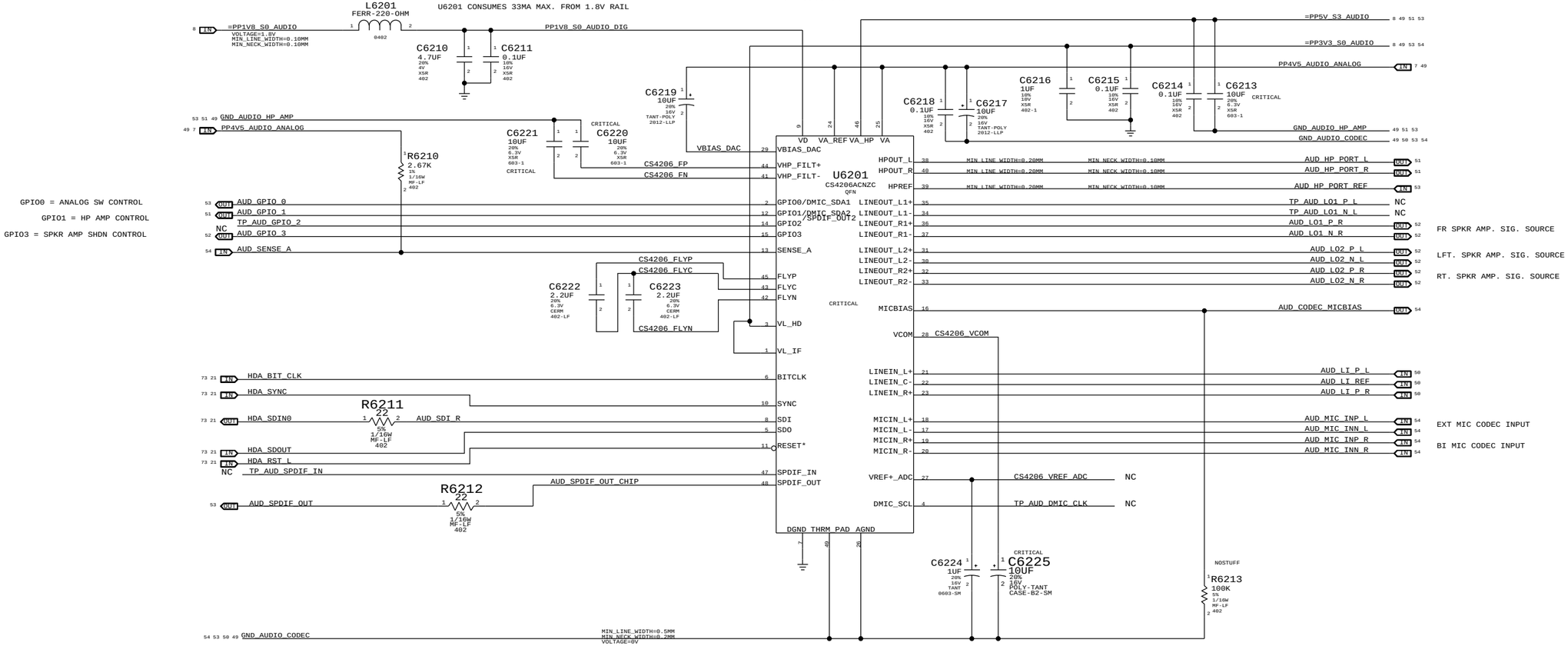
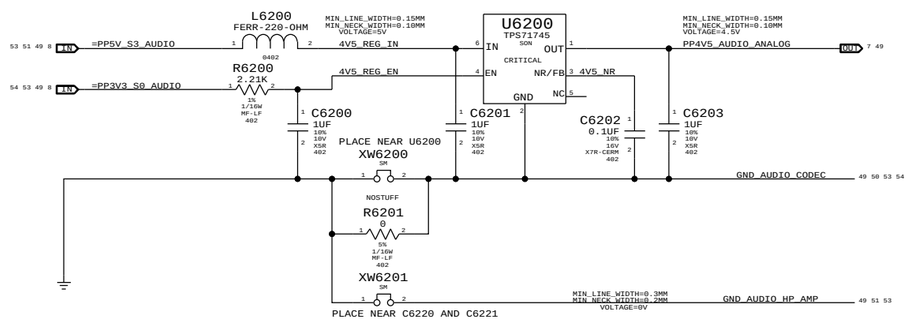
AUDIO CODEC

APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D
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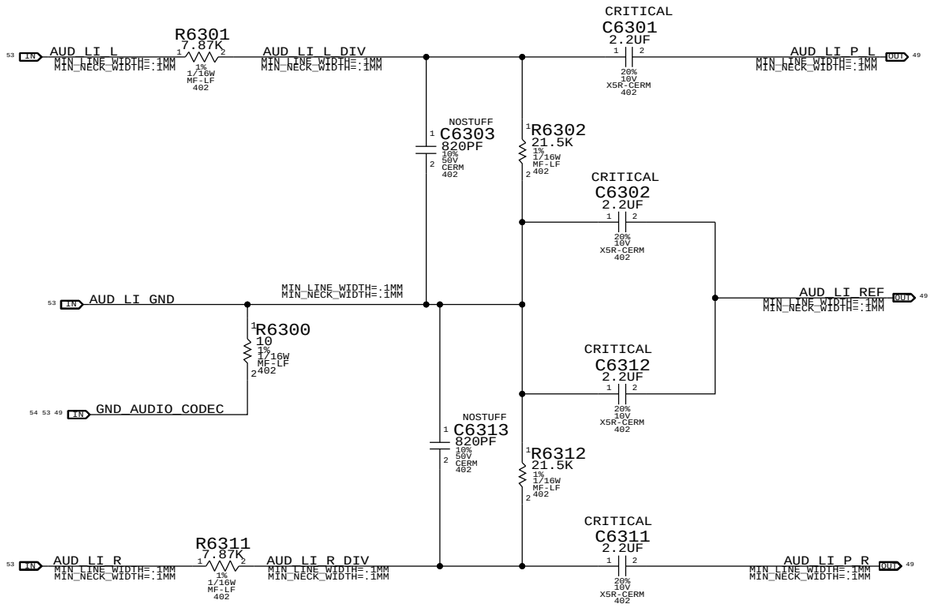
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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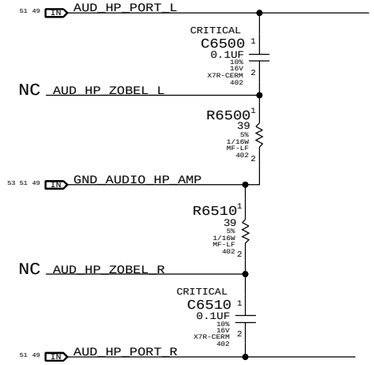
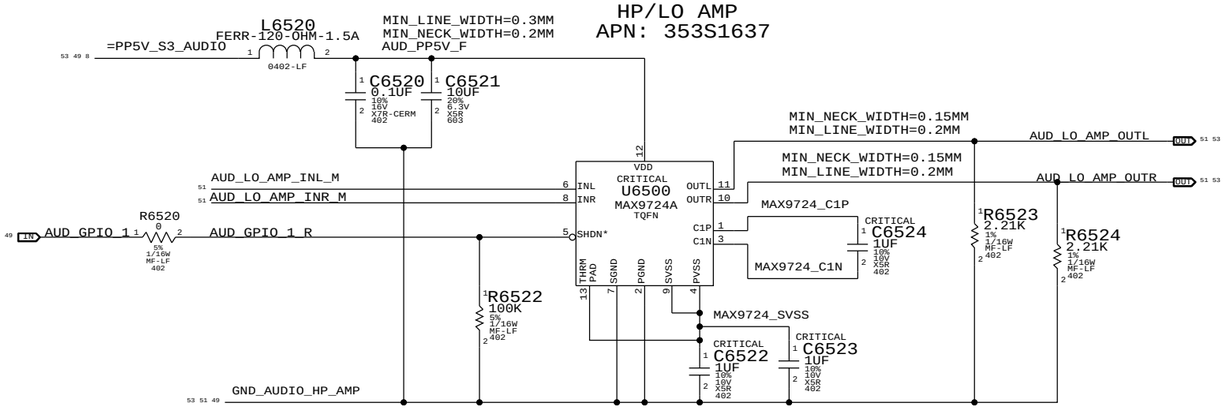
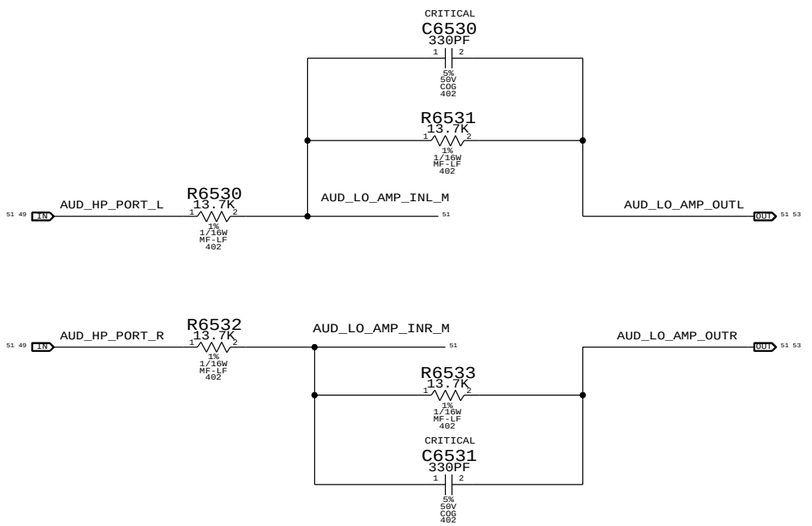
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER







SYNC MASTER=AUDIO	SYNC DATE=06/09/2009
PAGE TITLE: AUDIO: HEADPHONE FILTER	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
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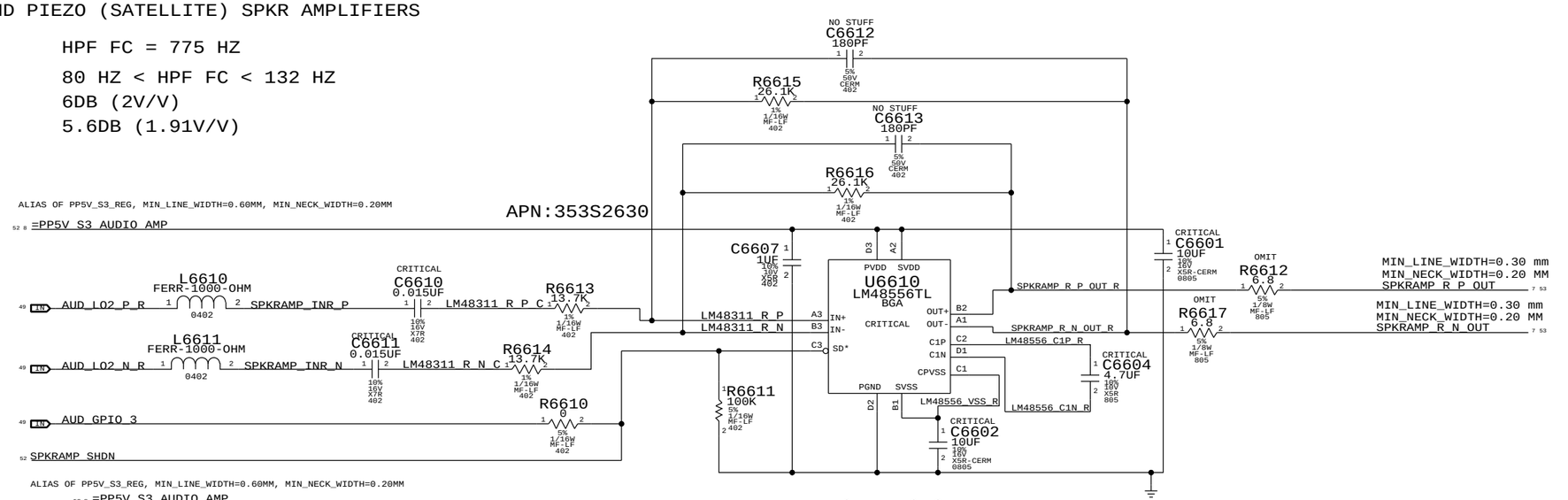
DYNAMIC (SUB) AND PIEZO (SATELLITE) SPKR AMPLIFIERS

SATELLITE	HPF FC = 775 HZ
SUB	80 HZ < HPF FC < 132 HZ
SUB GAIN	6DB (2V/V)
SAT GAIN	5.6DB (1.91V/V)



SYNC_MASTER=AUDIO SYNC_DATE=06/09/2009

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

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AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO

APN:514-0694
OMIT
J6700
AUDIO-JACK-TRANS-K83
F-RT-TH
CRITICAL

AUDIO
PHS_DETECT
GND
HP DETECT
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS

C6700 1UF 10% 6.3V CERM 402

AUD_CONNJ1_MIC
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING
AUD_IP_PERPH_DET_JACK
AUD_CONNJ1_TIPDET

AUD_SPDIF_OUT

L6701 FERR-1000-OHM 0402 — HS_MIC_HI
L6702 FERR-1000-OHM 0402 — HS_MIC_LO
CRITICAL L6703 FERR-120-OHM-1.5A 0402-LF — AUD_CONN_GND
CRITICAL L6704 FERR-220-OHM 0402 — AUD_CONN_L
CRITICAL L6705 FERR-220-OHM 0402 — AUD_CONN_R
L6706 FERR-1000-OHM 0402 — AUD_IP_PERPH_DET

R6700 10K 5% 1/10W MF-LF 402 — AUD_J1_SLEEVEDET_R
R6701 4.7 5% 1/10W MF-LF 402 — AUD_J1_TIPDET_R

CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402

C6701 100PF 5% 50V CERM 402

PLACE NEAR J6700
XW6702 SM — AUD_HP_PORT_REF
PLACE NEAR J6700
XW6700 SM — GND_AUDIO_HP_AMP
PLACE NEAR J6700
XW6701 SM — AUD_LI_GND
AUD_CONN_GND

MIC CONNECTOR

APN:518S0520

CRITICAL J6701 78171-0003 M-RT-SM

BI_MIC_LO
BI_MIC_SHIELD
BI_MIC_HI

SPEAKER CONNECTORS

APN:518S0519

CRITICAL J6702 78171-0002 M-RT-SM — LEFT PIEZO
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
C6703 100PF 5% 50V CERM 402
C6702 100PF 5% 50V CERM 402

CRITICAL J6703 78171-0002 M-RT-SM — DYN. FULL RANGE
CRITICAL L6707 FERR-120-OHM-3A 0603
SPKRAMP_SUB_P_OUT
SPKRAMP_SUB_N_OUT
C6705 100PF 5% 50V CERM 402
C6704 100PF 5% 50V CERM 402
CRITICAL L6708 FERR-120-OHM-3A 0603
SPKRAMP_SUB_P_OUT_CONN
SPKRAMP_SUB_N_OUT_CONN

CRITICAL J6704 78171-0003 M-RT-SM — RT. PIEZO
CRITICAL L6709 FERR-120-OHM-3A 0603
SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT
C6707 100PF 5% 50V CERM 402
C6706 100PF 5% 50V CERM 402
CRITICAL L6710 FERR-120-OHM-3A 0603
SPKRAMP_R_P_OUT_CONN
SPKRAMP_R_N_OUT_CONN

ANALOG AUDIO IO SWITCH

APN: 353S2536

=PP5V_S3_AUDIO
R6724 0 5% 1/16W MF-LF 402
PP_MAX14504_VCC
C6710 1UF 10% 10V X5R 402

U6700 MAX14504 WLP CRITICAL
VCC
NC1
NC2
NO1
NO2
CB
NEG
COM1
COM2
EN*
GND

AUD_LO_AMP_OUTL — R6716 0 — AUD_LO_AMP_OUTL_SWITCH
AUD_LO_AMP_OUTR — R6717 0 — AUD_LO_AMP_OUTR_SWITCH
AUD_LI_L — R6718 0 — AUD_LI_L_SWITCH
AUD_LI_R — R6719 0 — AUD_LI_R_SWITCH
AUD_GPIO_0 — R6720 0 — AUD_SWITCH_CTRL
R6721 100K 5% 1/16W MF-LF 402
AUD_CONN_GND — R6715 0 — AUD_SWITCH_GND
GND_AUDIO_CODEC — R6714 0

NOSTUFF R6727 0

SWITCH_CP
C6711 0.0033UF 10% 50V CERM 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_L
R6712 24K 5% 1/16W MF-LF 402
AUD_CONN_R
R6713 24K 5% 1/16W MF-LF 402

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

GND STUFFING OPTIONS FOR CMOS SWITCH

SYNC_MASTER=AUDIO	SYNC_DATE=06/09/2009
PAGE TITLE: AUDIO: JACK	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
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	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CODEC OUTPUT SIGNAL PATHS

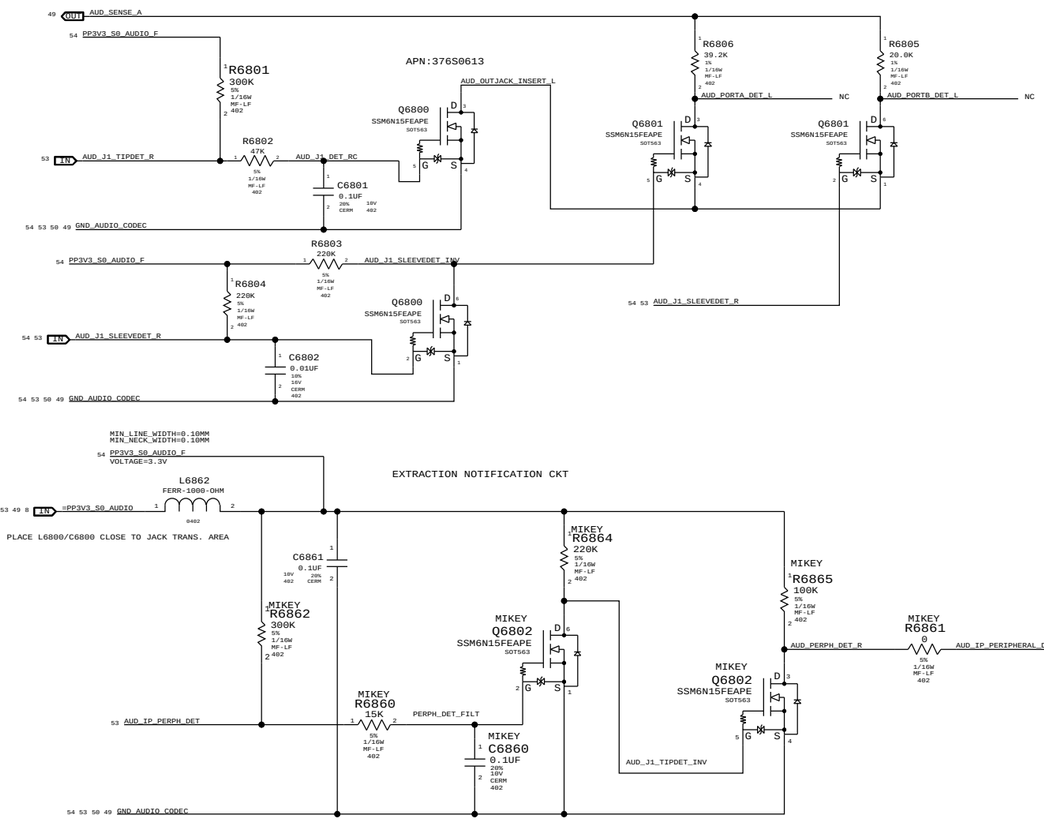
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF/ENABLE	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MCP79 GPIO_38	MCP79 GPIO_17 (PERIPH DETECT) MCP79 GPIO_4 (LOAD DETECT)

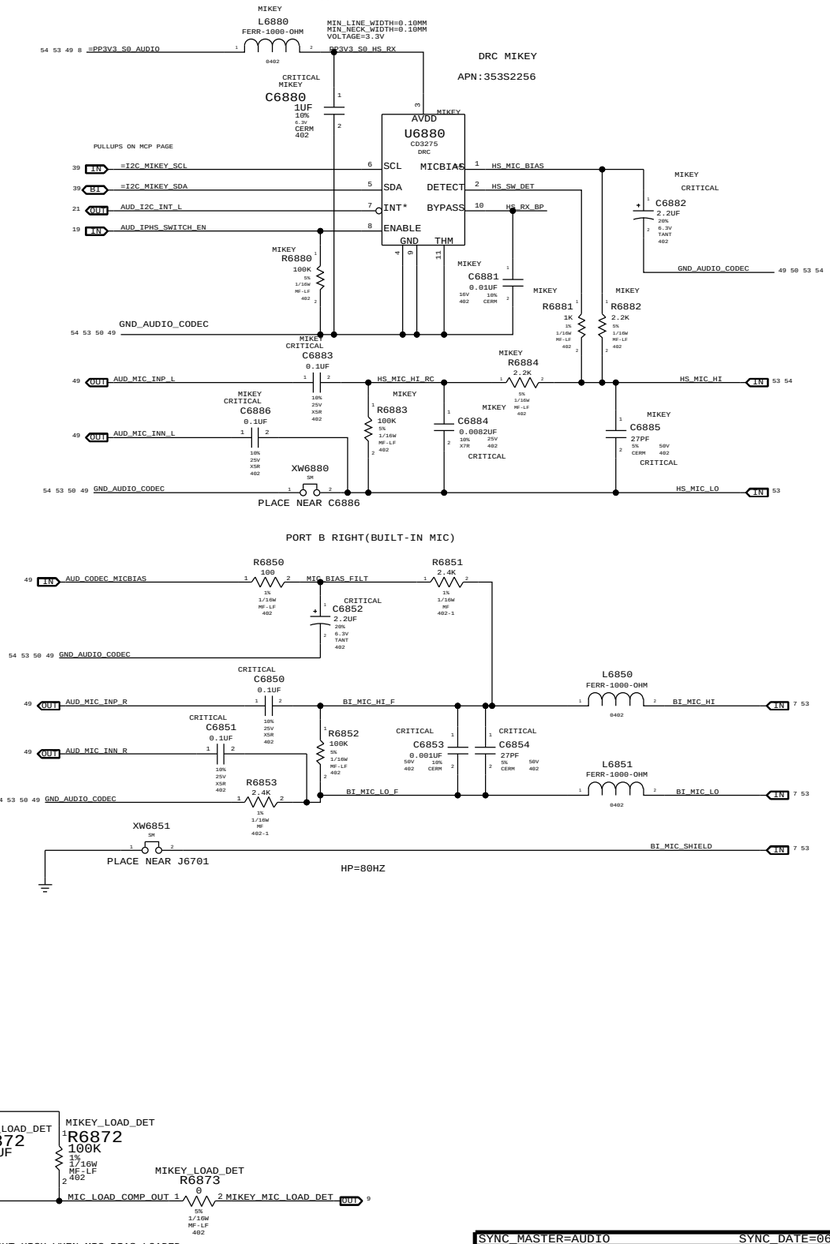
PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)



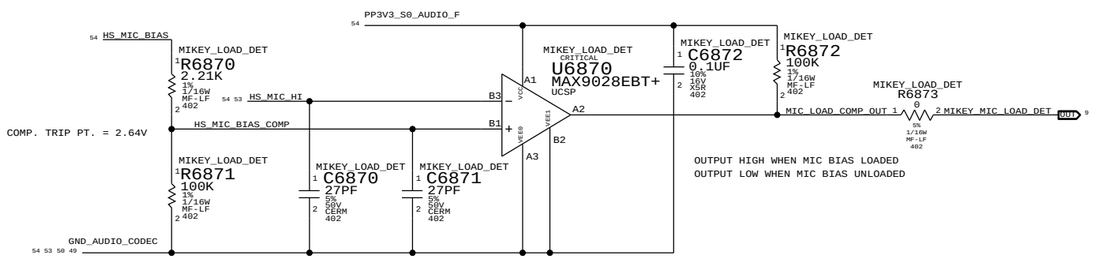
PORT B LEFT(HEADSET MIC)

HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)

MIKEY MIC LOAD DET CKT



SYNC MASTER=AUDIO SYNC DATE=06/09/2009

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

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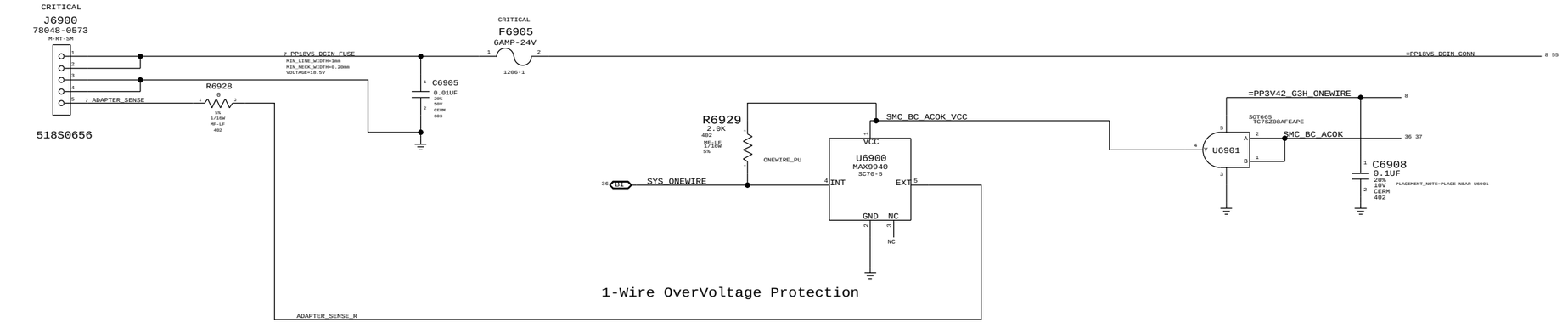
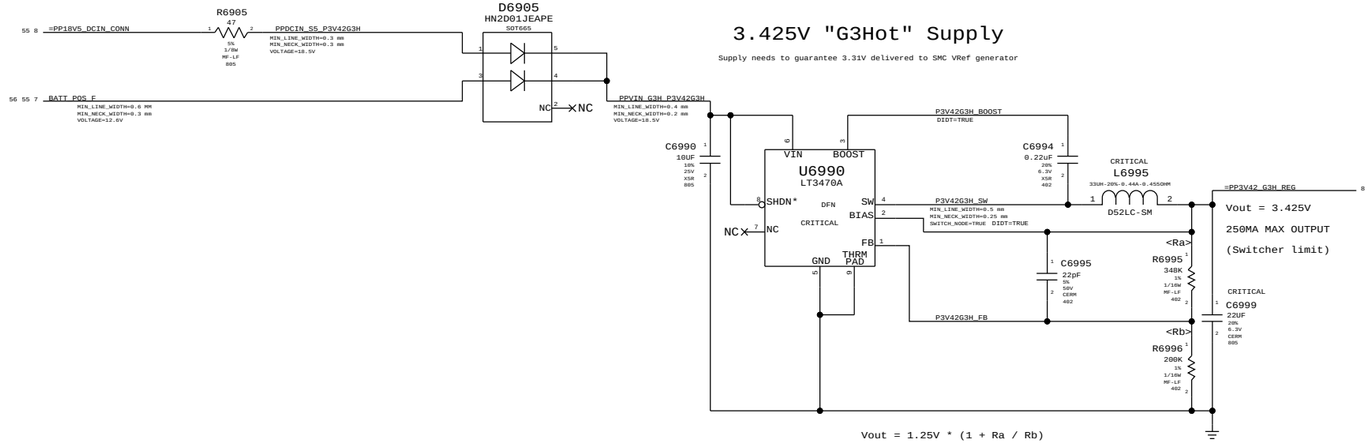
MagSafe DC Power Jack



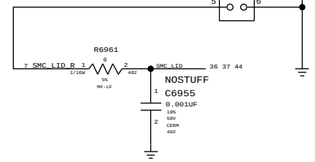
1-Wire OverVoltage Protection



3.425V "G3Hot" Supply

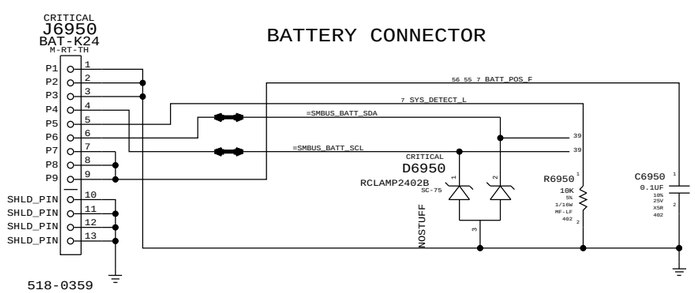
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)



HALL EFFECT CONNECTOR

BATTERY CONNECTOR



SYNC_MASTER=K24_MLB	SYNC_DATE=02/05/2009
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
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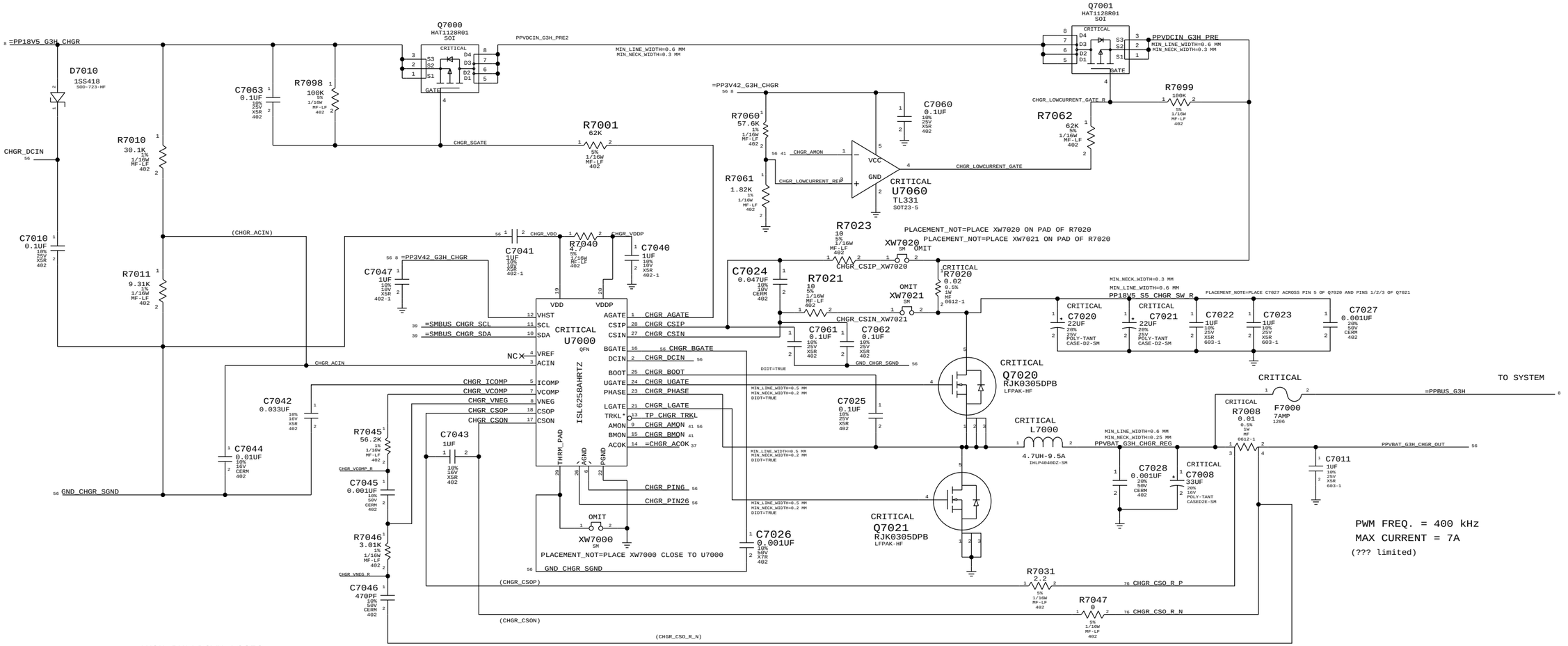
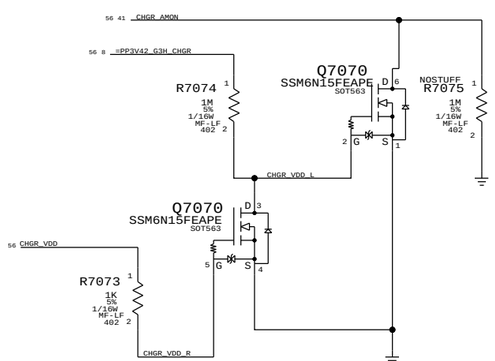
	PAGE: 69 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

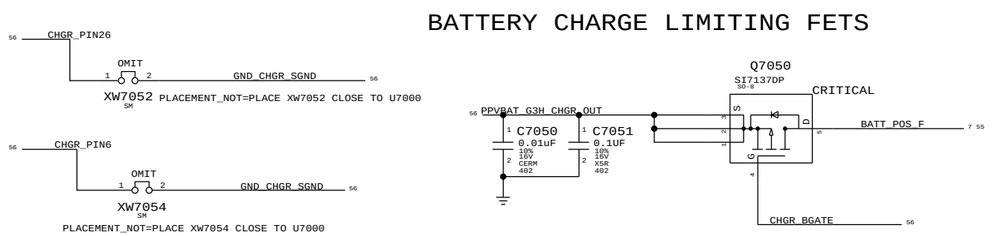
PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)

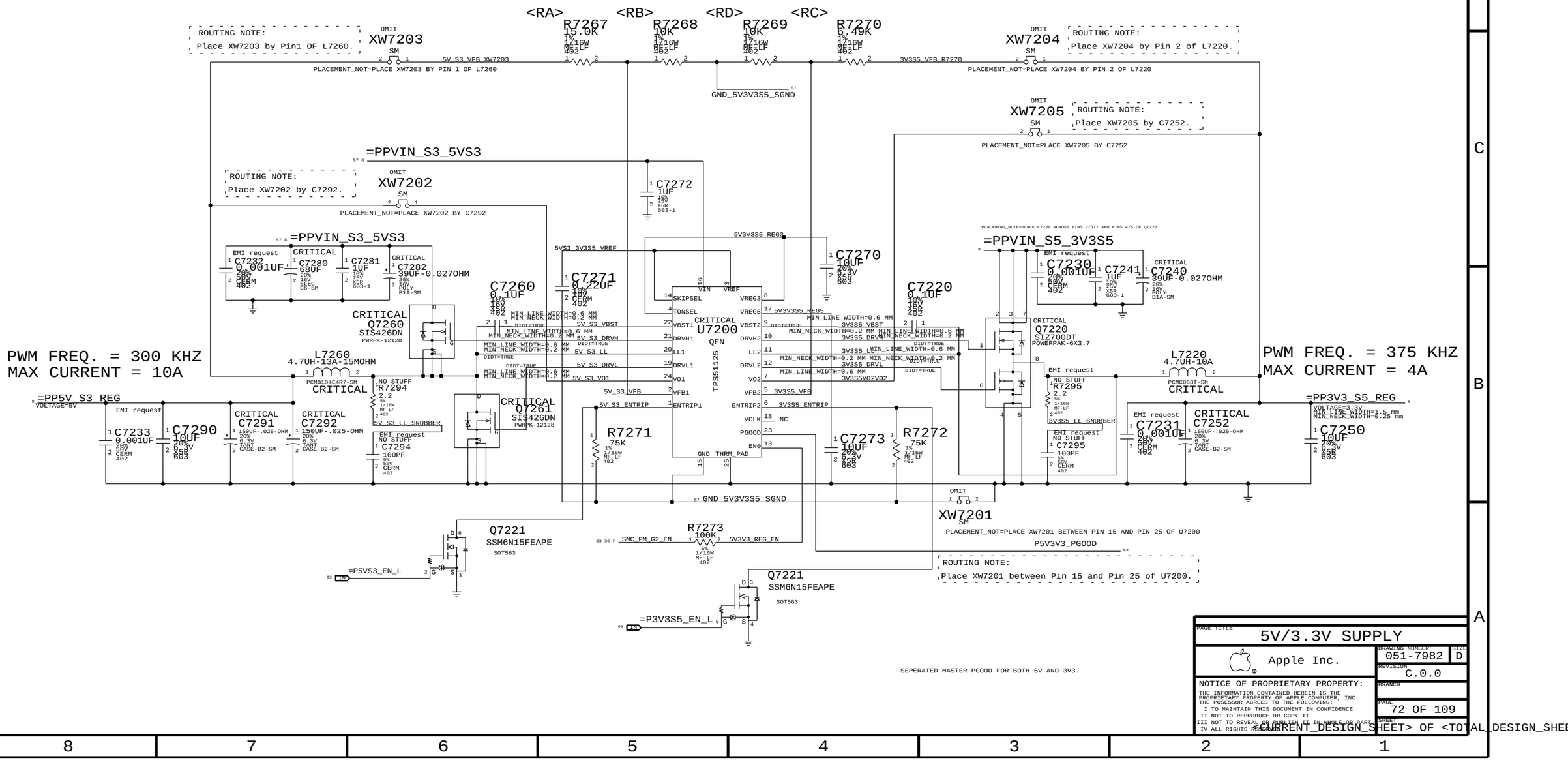
SYNC MASTER=K24 MLB	SYNC DATE=02/05/2009
PAGE TITLE	PBUS Supply/Battery Charger
Apple Inc.	DRAWING NUMBER 051-7982 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 70 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

- COPY THIS PAGE FROM K36 CSA.76

5V S3/3.3V S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

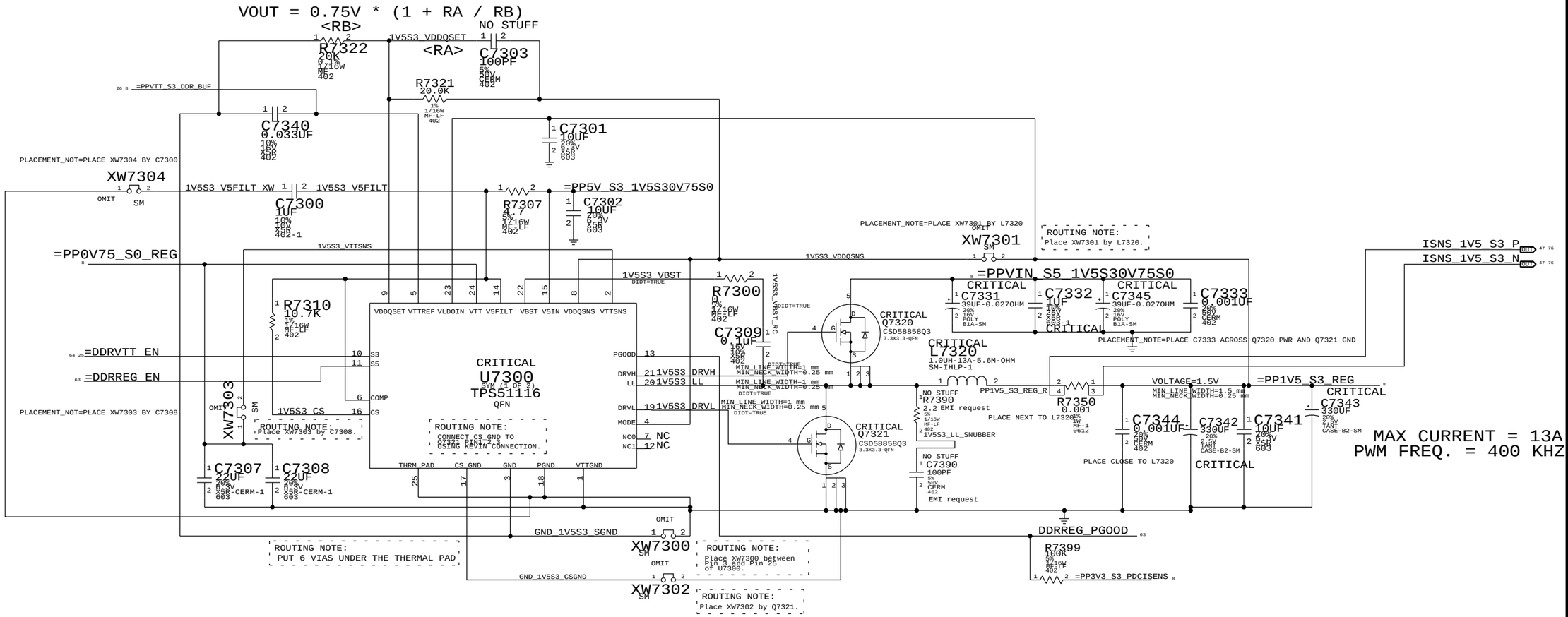
VOUT = (2 * RC / RD) + 2



PAGE TITLE	5V/3.3V SUPPLY
	Apple Inc.
DRAWING NUMBER	051-7982
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	72 OF 109
SHEET	<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5V/0.75V(DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)



PLACEMENT_NOT=PLACE XW7300 BETWEEN PIN 3 AND PIN 25 OF U7300

PLACEMENT_NOT=PLACE XW7302 BY Q7321

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

PAGE TITLE: 1.5V/0.75V DDR3 SUPPLY

Apple Inc.

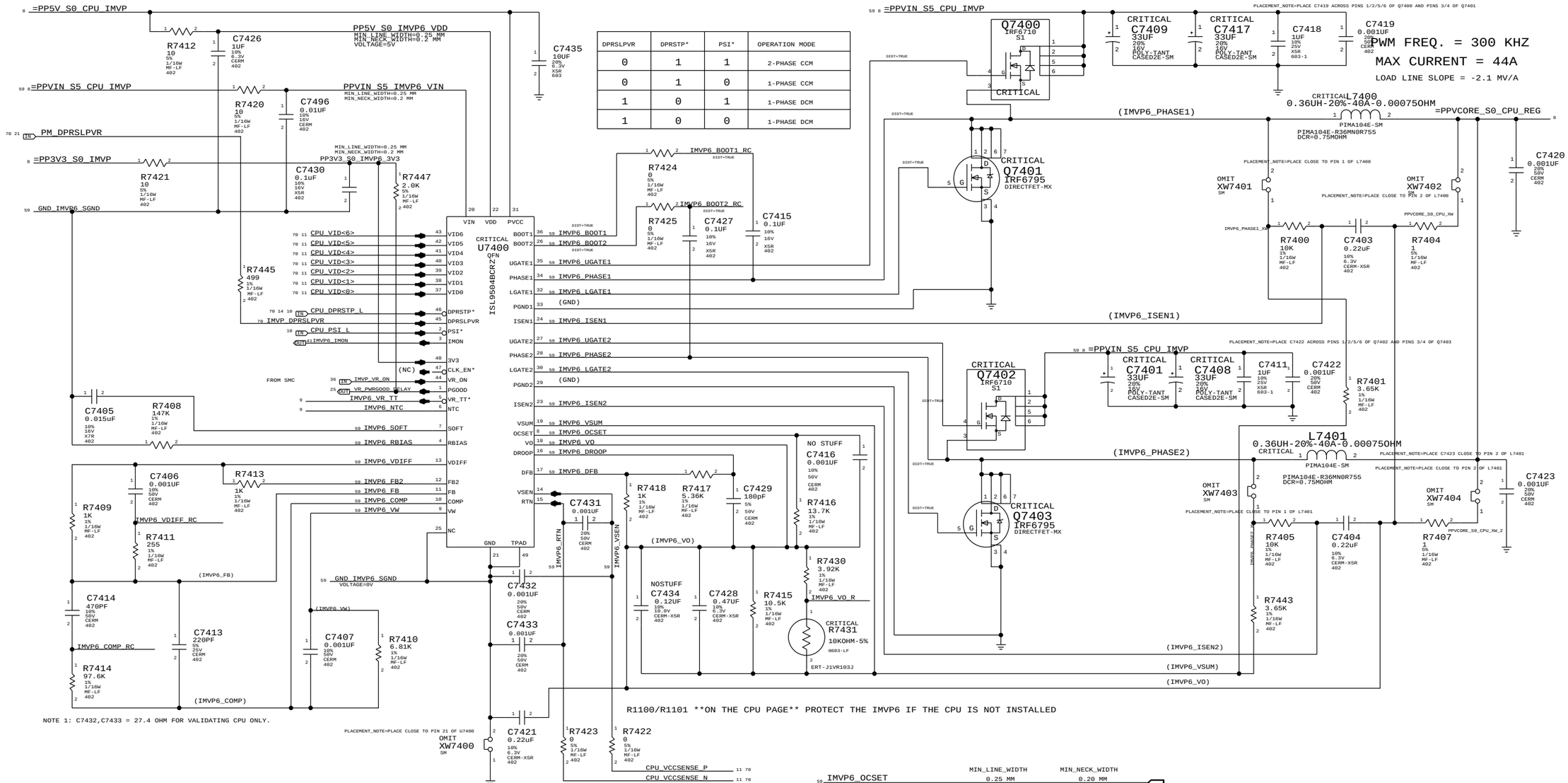
DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 73 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC_MASTER=K24_MLB SYNC_DATE=03/03/2009

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

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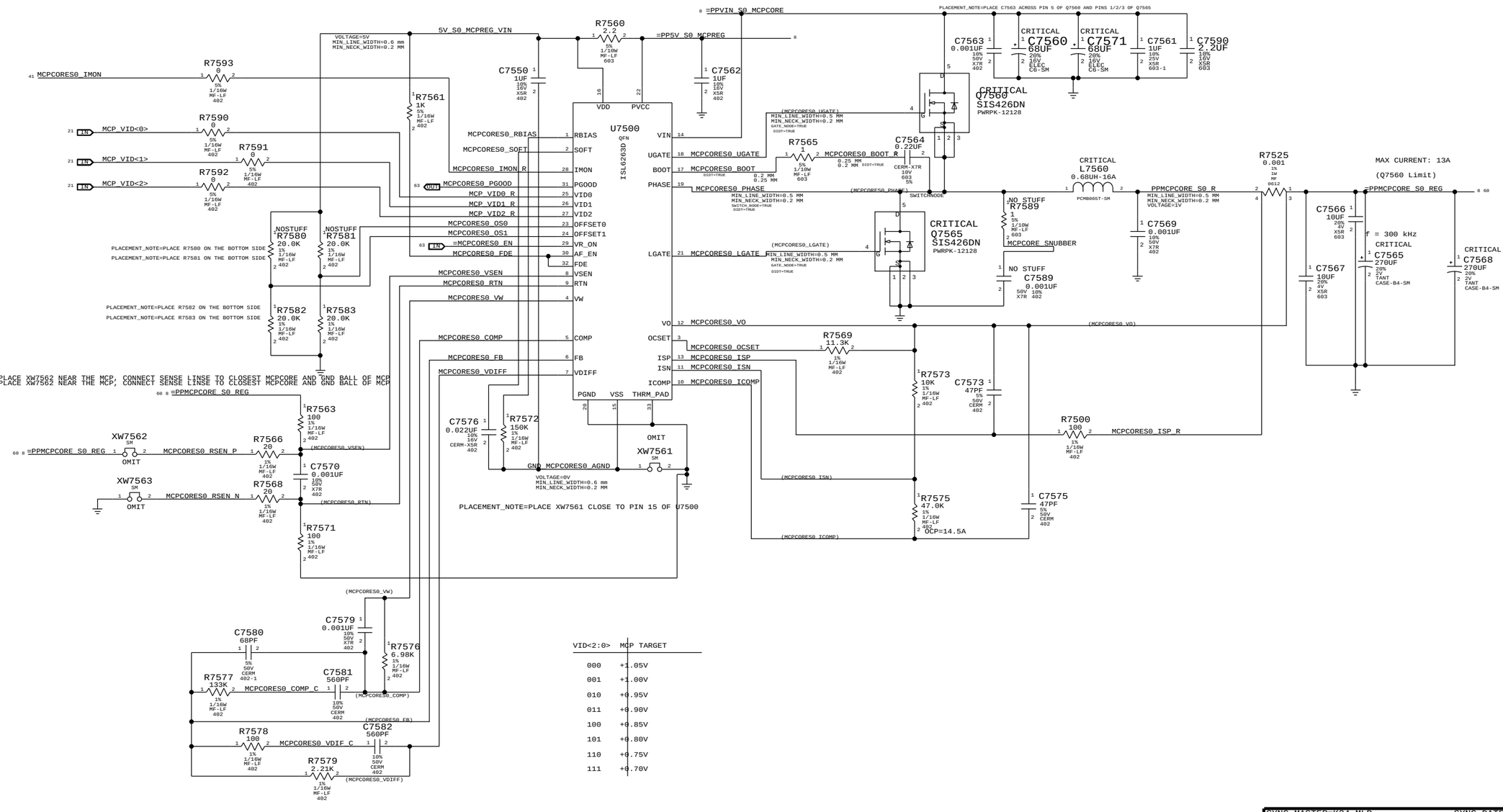
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K24 MLB SYNC DATE=02/15/2005

PAGE TITLE

MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

BRANCH

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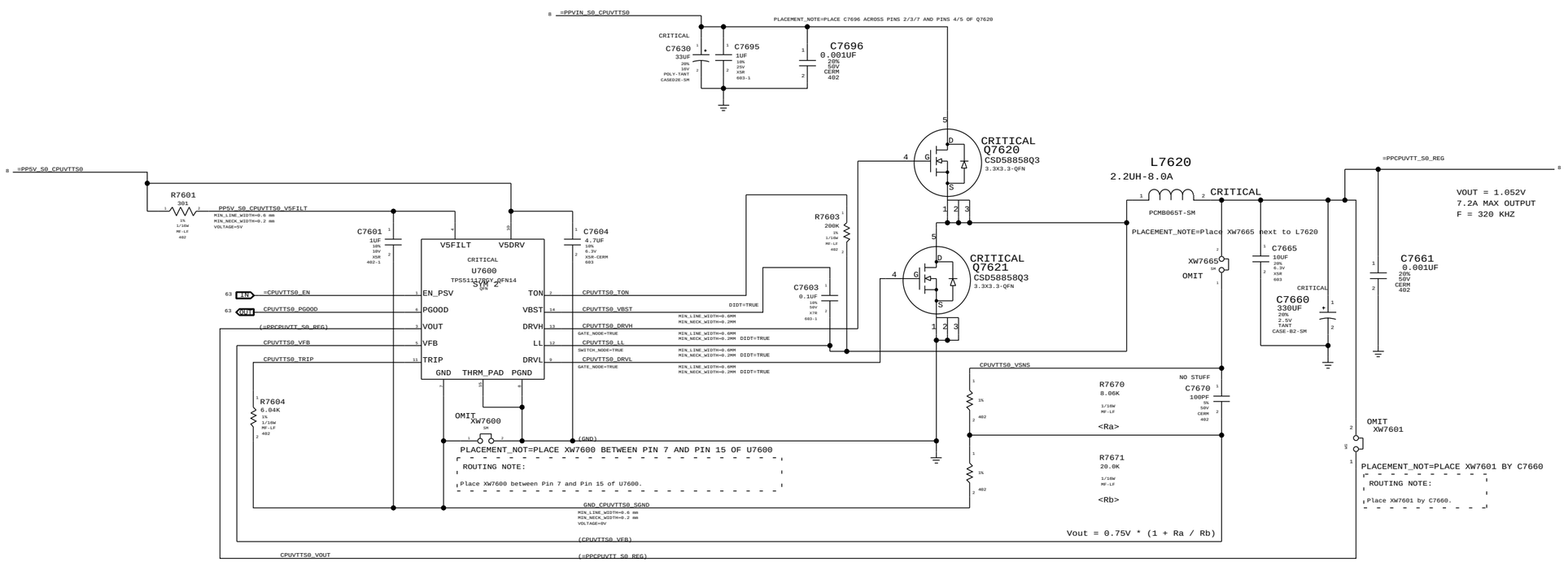
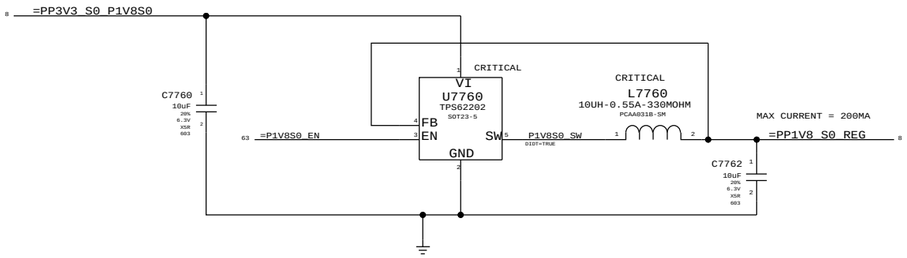
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPUVTT POWER SUPPLY

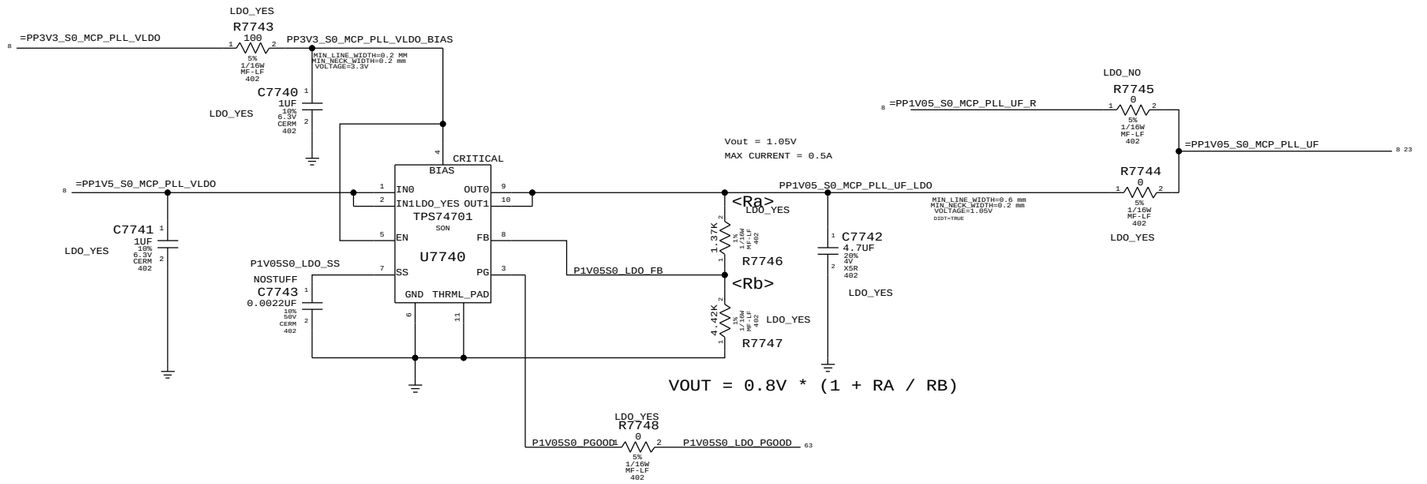


SYNC MASTER=K24_MLB	SYNC DATE=02/04/2009
PAGE TITLE: CPU VTT(1.05V) SUPPLY	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 76 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

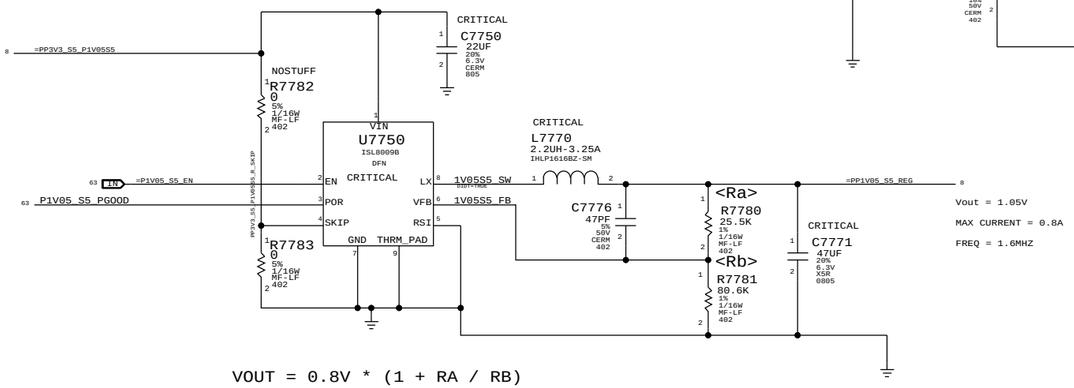
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



SYNC MASTER=K24_MLB	SYNC DATE=03/24/2009
PAGE TITLE: MISC POWER SUPPLIES	
Apple Inc.	DRAWING NUMBER: 051-7982 SIZE: D
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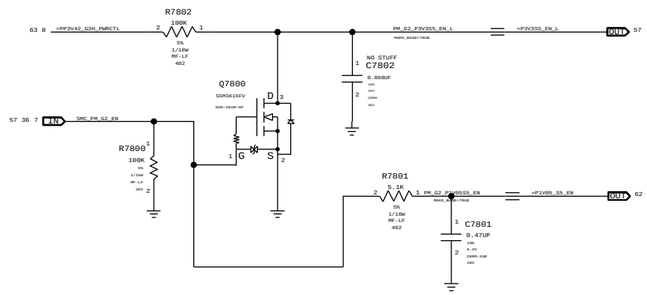
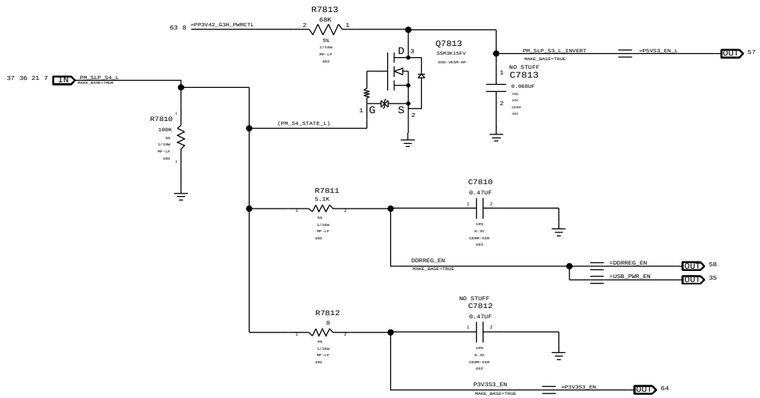
	BRANCH:
	PAGE: 77 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.3V 1.05V S5 ENABLE



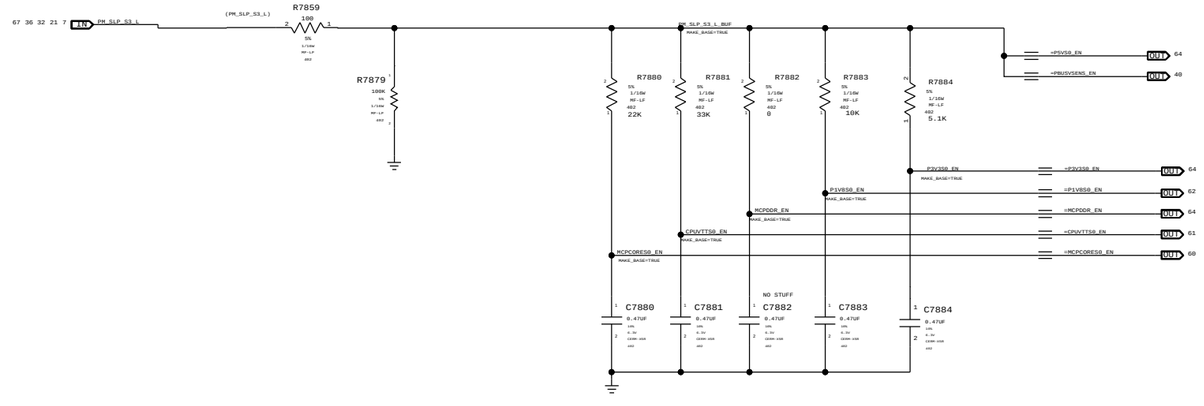
S3 ENABLE



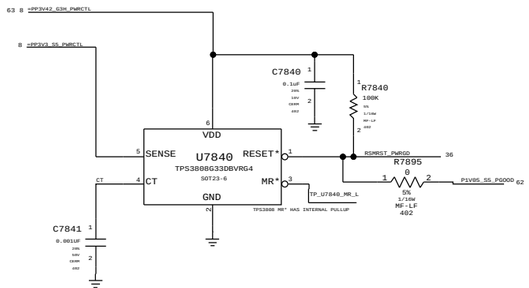
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

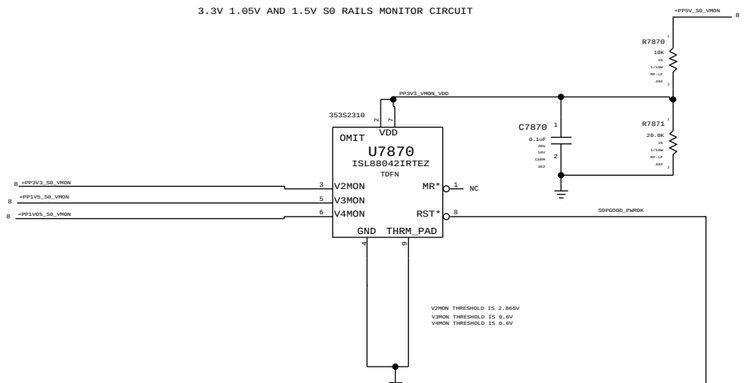
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



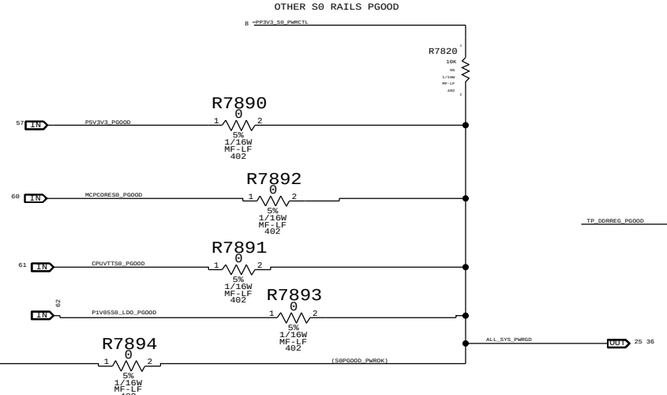
VOLTAGE MONITOR



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal

PAGE TITLE	POWER SEQUENCING
	Apple Inc.
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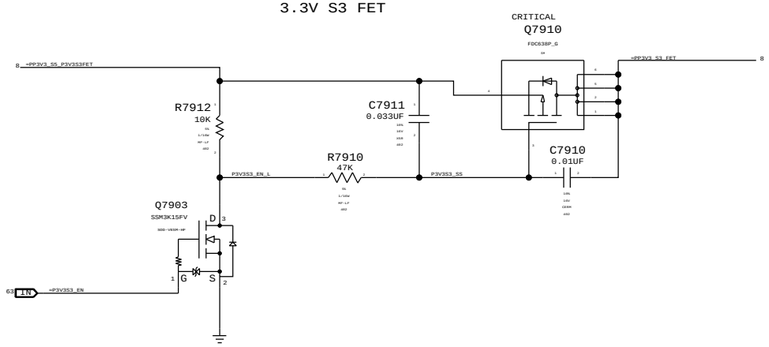
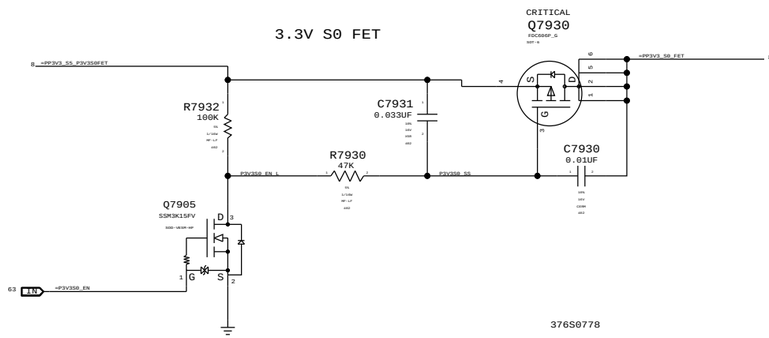
3.3V S3 FET



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

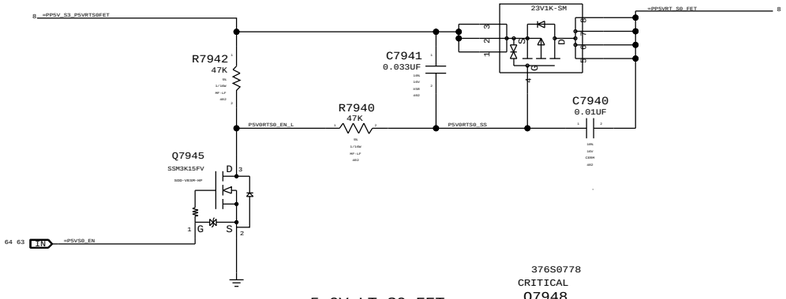
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

376S0778

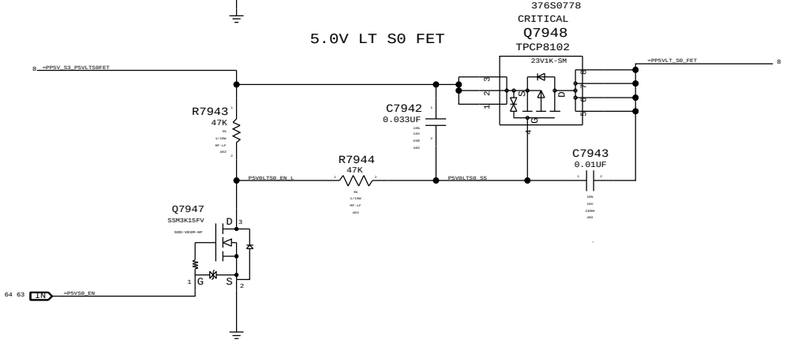
5.0V RT S0 FET



5.0V RT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	0.48 A (EDP)

376S0778

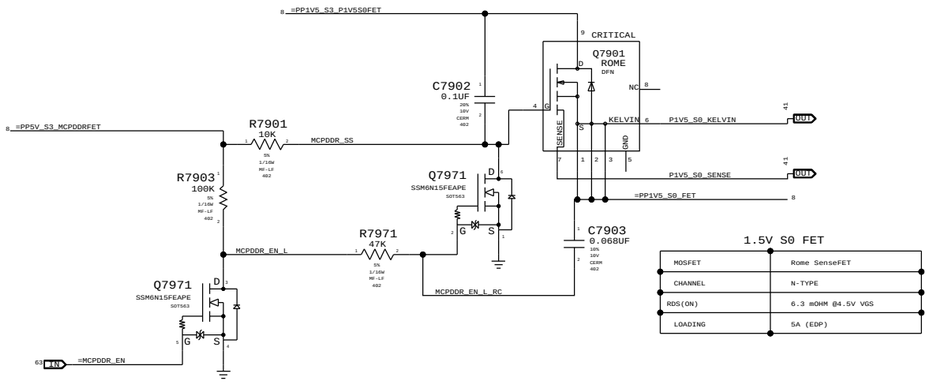
5.0V LT S0 FET



5.0V LT S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.302 A (EDP)

1.5V S0 FET

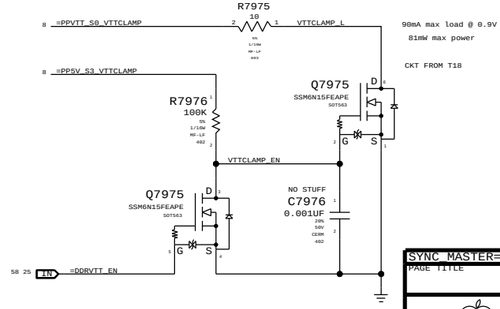
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



90mA max load @ 0.9V
81mW max power

CKT FROM T18

SYNC_MASTER=K24_MLB	SYNC_DATE=02/15/2009
PAGE TITLE	POWER FETS
Apple Inc.	DRAWING NUMBER 051-7982
	SIZE D
	REVISION C.0.0
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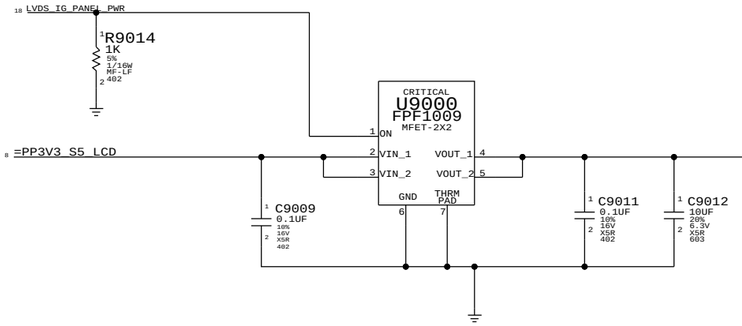
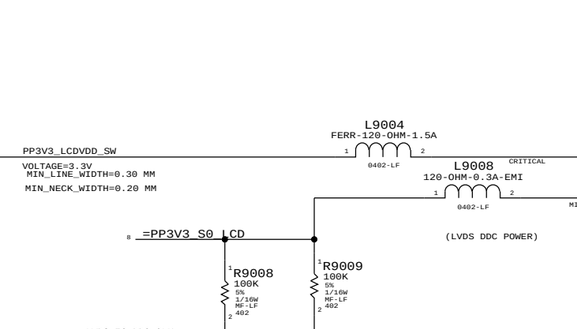
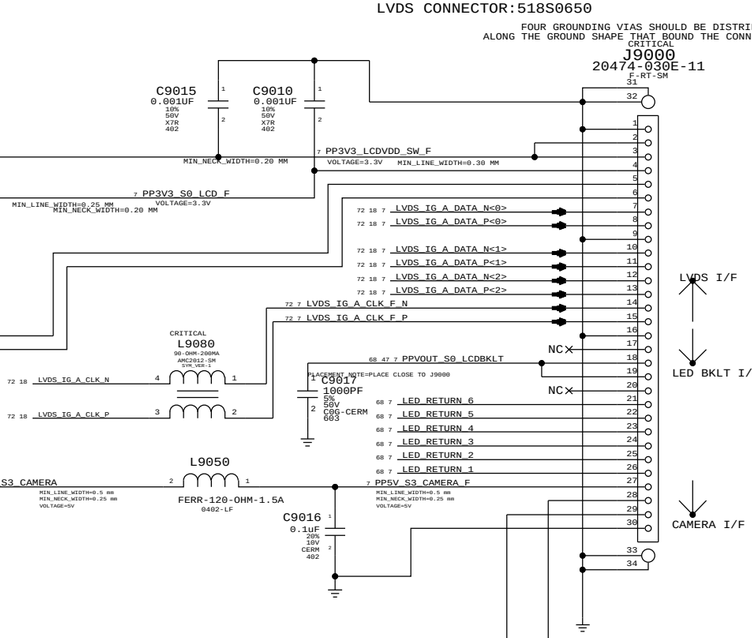
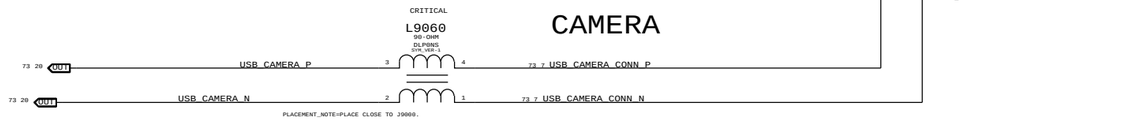
	PAGE 79 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP









SYNC_MASTER=K24_MLB SYNC_DATE=02/15/2009

PAGE TITLE: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-7982 SIZE: D

REVISION: C.0.0

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

8	7	6	5	4	3	2	1

18 =MCP_HDMI_TXC_P — DP_ML_P<3> — 67 72 MAKE_BASE=TRUE
18 =MCP_HDMI_TXC_N — DP_ML_N<3> — 67 72 MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_P<0> — DP_ML_P<2> — 67 72 MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_N<0> — DP_ML_N<2> — 67 72 MAKE_BASE=TRUE
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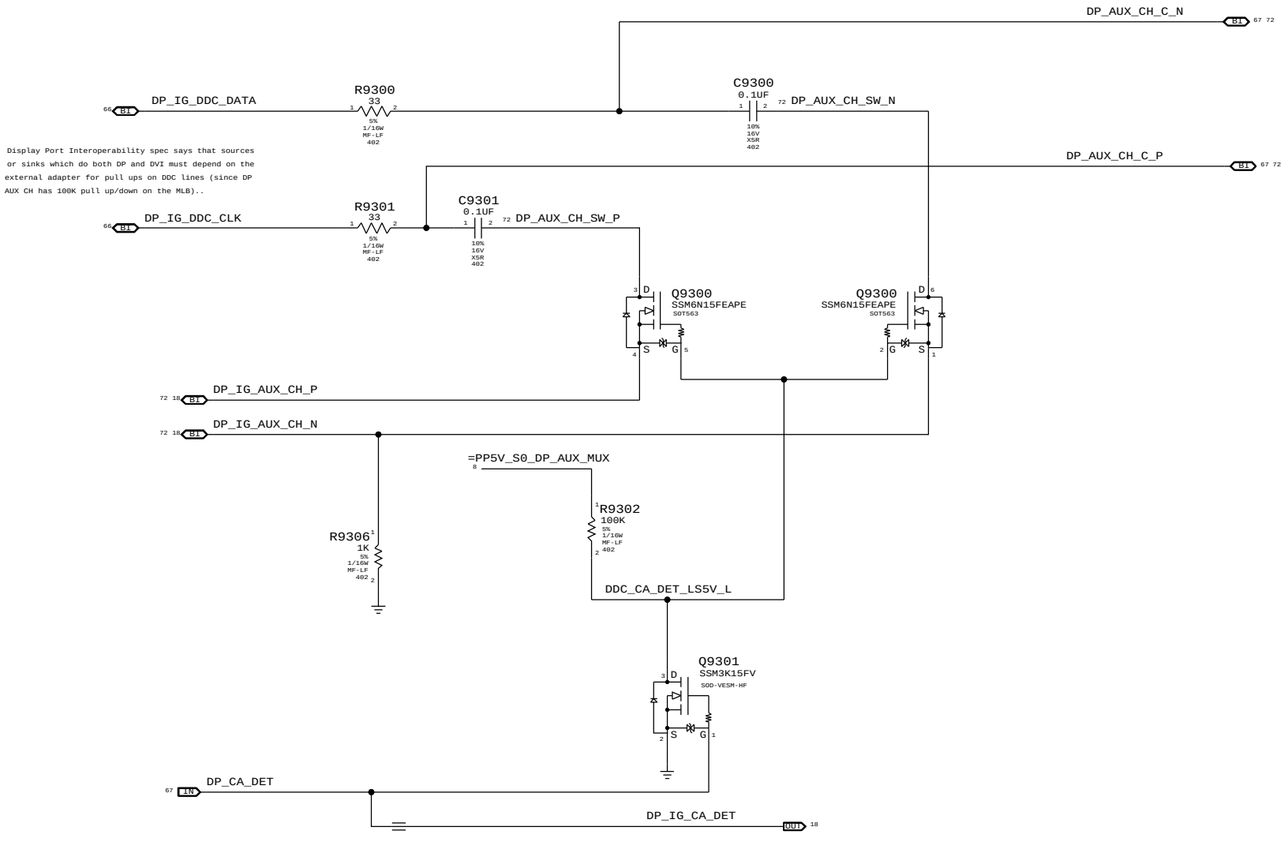
18 =MCP_HDMI_TXD_P<2> — DP_ML_P<0> — 67 72 MAKE_BASE=TRUE
18 =MCP_HDMI_TXD_N<2> — DP_ML_N<0> — 67 72 MAKE_BASE=TRUE
18 =MCP_HDMI_HPD — DP_HPD — 67 MAKE_BASE=TRUE
18 =MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — 66 MAKE_BASE=TRUE
18 =MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — 66 MAKE_BASE=TRUE



SYNC_MASTER=K24_MLB — SYNC_DATE=04/06/2009

PAGE TITLE
DISPLAYPORT SUPPORT

Apple Inc.

DRAWING NUMBER 051-7982 — SIZE D
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SHEET

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POR IS PLASTIC MINI DP CONNECTOR BUT METAL PART'S SCHEMATIC AND CAD SUMBOLS
HAVE BEEN USED BEACUSE ITS LAND PATTERN CAN ACCOMODATE BOTH TYPES

Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
L9400
FERR-120-OHM-3A
0603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C9400
4.7UF
20%
6.3V
X5R-CERM
402
C9480
22UF
20%
6.3V
X5R-CERM-1
603
C9481
4.7UF
20%
6.3V
X5R-CERM
402
C9485
22UF
20%
6.3V
X5R-CERM-1
603
CRITICAL
C9486
22UF
20%
6.3V
X5R-CERM-1
603
R9420
100K
5%
1/16W
MF-LF
402

DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
D9410
RCLAMP0524P
SLP2510P8

HDMI_CEC
R9425
1M
5%
1/16W
MF-LF
402

CRITICAL OMIT
J9400
MINIDSPLYPRT-K83
F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
	HOT_PLUG_DETECT	GND
	CONFIG1	ML_LANE0P
	CONFIG2	ML_LANE0N
	GND	GND
	ML_LANE3P	ML_LANE1P
	ML_LANE3N	ML_LANE1N
	GND	GND
	AUX_CHP	ML_LANE2P
	AUX_CHN	ML_LANE2N
	DP_PWR	RETURN

SHIELD PINS
22 21
514-0691

FL9400
12-OHM-100MA
TCM1210-4SM
SYM_VER-2
FL9401
12-OHM-100MA
TCM1210-4SM
SYM_VER-2
FL9402
12-OHM-100MA
TCM1210-4SM
SYM_VER-2
FL9403
12-OHM-100MA
TCM1210-4SM
SYM_VER-2

DP_ML_P<3> C9414 0.1uF DP_ML_C_P<3>
DP_ML_N<3> C9415 0.1uF DP_ML_C_N<3>
DP_AUX_CH_C_P
DP_AUX_CH_C_N
DP_ML_CONN_P<3>
DP_ML_CONN_N<3>
DP_ML_CONN_P<0>
DP_ML_CONN_N<0>
DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>
C9410 0.1uF DP_ML_P<0>
C9411 0.1uF DP_ML_N<0>
C9412 0.1uF DP_ML_P<1>
C9413 0.1uF DP_ML_N<1>
C9416 0.1uF DP_ML_P<2>
C9417 0.1uF DP_ML_N<2>

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
R9421 100K 5% 1/16W MF-LF 402
DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8
R9422 1M 5% 1/16W MF-LF 402
DP to DVI/HDMI
Cable Adapter
(CA) has 100k
pull-up to DP_PWR.
DP_ESD
CRITICAL
D9400
RCLAMP0504F
SC70-6-1
DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8

=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
R9446 100K 5% 1/16W MF-LF 402
MCP79 requires pull
down HPD input with
100K if DP_HPD is used.
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/16W MF-LF 402
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

SYNC MASTER=K24 MLB SYNC DATE=04/06/2009
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DisplayPort Connector
Apple Inc.
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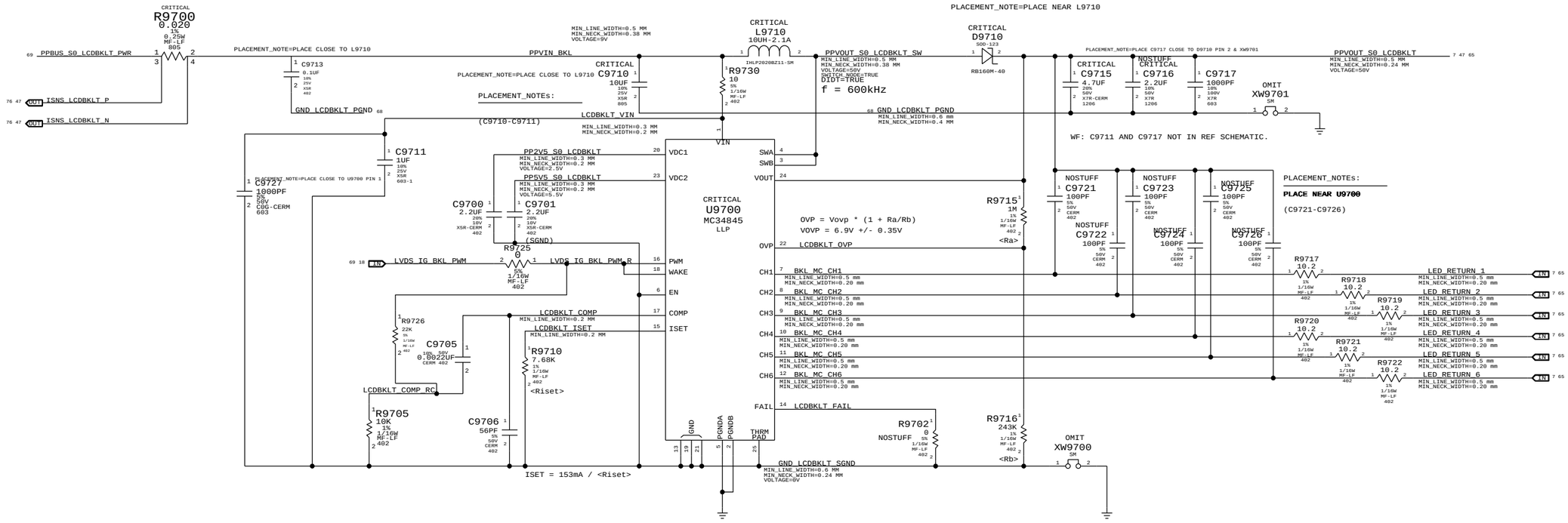
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



13.3 Inch Panel (9 LEDs per string)

TARGET: ISET = 20MA, OVP = 35V

ACTUAL: ISET = 19.9MA, OVP = 35.2V

SYNC_MASTER=VEMURI_K19I SYNC_DATE=02/09/2009

PAGE TITLE

LCD Backlight Driver (MC34845)

Apple Inc.

DRAWING NUMBER 051-7982 SIZE D

REVISION C.0.0

BRANCH

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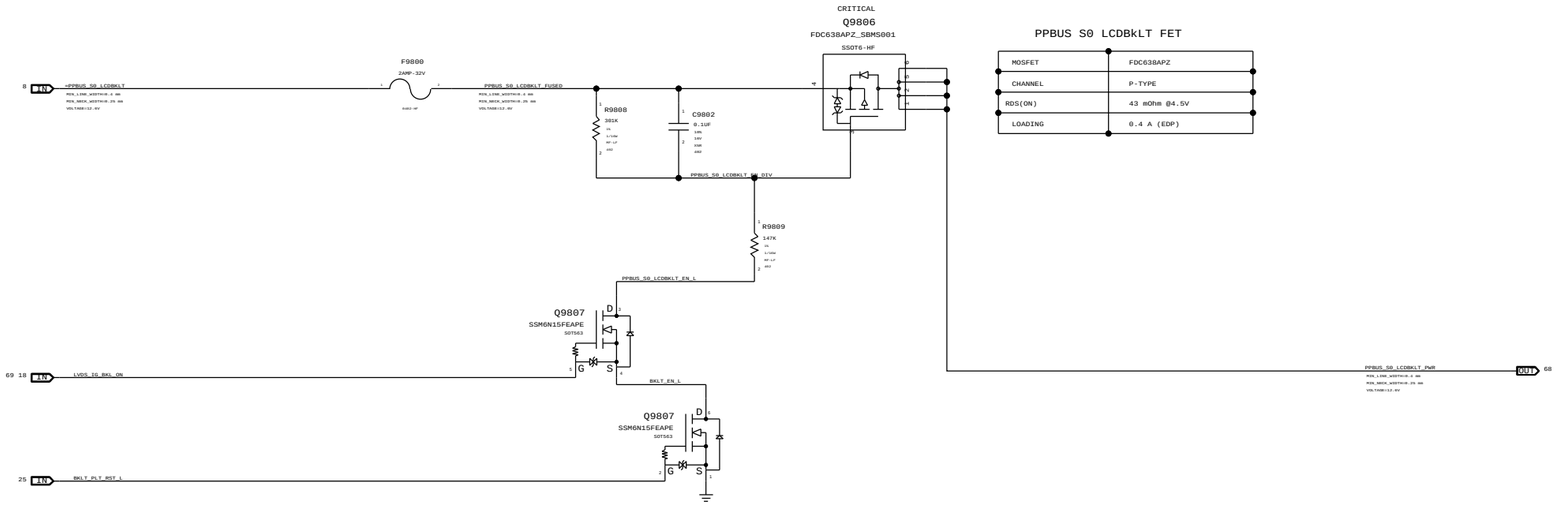

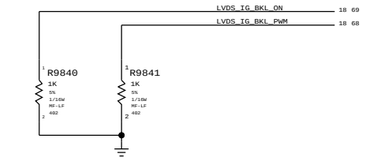

MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

SYNC MASTER=K24 MLB
SYNC DATE=04/06/2009

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-7982
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BMIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_LOCK_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_BMIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_H	CPU_50S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 37
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	10 14 37
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FBOM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	10 14 59
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 59
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	59
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 26
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_BMIL	CPU_VID<6..0>	11 59
		CPU_50S	CPU_BMIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

SYNC_MASTER=K24_MLB
SYNC_DATE=04/06/2009
PAGE TITLE: CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 27
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 27
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 27
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 28
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

SYNC_MASTER=K24_MLB SYNC_DATE=04/06/2009

PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	v	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	30
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	30
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 30
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 30
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 30
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	9 17
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	9 17
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_N	9 17
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_REF_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 30
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 30
MCP_REA_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P	7 30
	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N	7 30
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	66 67
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	67
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	66 67
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	67
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 66
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	66
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	66
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	66 67
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	66 67
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 24
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	7 65
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 65
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	7 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7 18 65
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7 18 65
J183 DP_HI	DP_100D	DISPLAYPORT	DP_HL_CONN_P<3..0>	67
J182	DP_100D	DISPLAYPORT	DP_HL_CONN_N<3..0>	67
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 24
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	20 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	7 34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	34
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	34
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	20 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	7 34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	34
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	34
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 34
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 34
	SATA_100D	SATA	SATA_ODD_R2D_P	7 34
	SATA_100D	SATA	SATA_ODD_R2D_N	7 34
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	34
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	34
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 34
	SATA_100D	SATA	SATA_ODD_D2R_N	20 34
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 34
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 34
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	34
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	34
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

SYNC MASTER=K24 MLB SYNC DATE=03/30/2009

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP_BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_5SS	PCI	MCP_DEBUG<7..0> 13 19
PCI_AD	PCI_5SS	PCI	PCI_AD<23..8>
PCI_AD24	PCI_5SS	PCI	PCI_AD<24>
PCI_AD	PCI_5SS	PCI	PCI_AD<31..25>
PCI_AD	PCI_5SS	PCI	PCI_PAR
PCI_C_BE_L	PCI_5SS	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_5SS	PCI	PCI_IRDY_L
PCI_CNTL	PCI_5SS	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_5SS	PCI	PCI_PERR_L
PCI_CNTL	PCI_5SS	PCI	PCI_SERR_L
PCI_CNTL	PCI_5SS	PCI	PCI_STOP_L
PCI_CNTL	PCI_5SS	PCI	PCI_TRDY_L
PCI_CNTL	PCI_5SS	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_5SS	PCI	PCI_REQ0_L 19
PCI_GNT0_L	PCI_5SS	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_5SS	PCI	PCI_REQ1_L 19
PCI_GNT1_L	PCI_5SS	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_5SS	PCI	PCI_INTW_L
PCI_INTX_L	PCI_5SS	PCI	PCI_INTX_L
PCI_INTY_L	PCI_5SS	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_5SS	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP 19
LPC_AD	LPC_5SS	LPC	LPC_AD<3..0> 19 36 38
LPC_FRAME_L	LPC_5SS	LPC	LPC_FRAME_L 19 36 38
LPC_RESET_L	LPC_5SS	LPC	LPC_RESET_L 19 25
MCP_LPC_CLK0	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC_R 19 25
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC 25 36
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS 25 38
USB_EXTA	USB_90D	USB	USB_EXTA_P 20 35
	USB_90D	USB	USB_EXTA_N 20 35
	USB_90D	USB	USB_EXTA_MUXED_P 35
	USB_90D	USB	USB_EXTA_MUXED_N 35
	USB_90D	USB	CONN_USB_EXTA_P 35
	USB_90D	USB	CONN_USB_EXTA_N 35
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20 65
	USB_90D	USB	USB_CAMERA_N 20 65
	USB_90D	USB	USB_CAMERA_CONN_P 7 65
	USB_90D	USB	USB_CAMERA_CONN_N 7 65
USB_BT	USB_90D	USB	USB_BT_P 20 30
	USB_90D	USB	USB_BT_N 20 30
	USB_90D	USB	CONN_USB2_BT_P 7 30
	USB_90D	USB	CONN_USB2_BT_N 7 30
USB_TPAD	USB_90D	USB	USB_TPAD_P 20 44
	USB_90D	USB	USB_TPAD_N 20 44
	USB_90D	USB	USB_TPAD_R_P 44
	USB_90D	USB	USB_TPAD_R_N 44
USB_IR	USB_90D	USB	USB_IR_P 9 20
	USB_90D	USB	USB_IR_N 9 20
USB_EXTB	USB_90D	USB	USB_EXTB_P 20 35
	USB_90D	USB	USB_EXTB_N 20 35
	USB_90D	USB	CONN_USB_EXTB_P 35
	USB_90D	USB	CONN_USB_EXTB_N 35
USB_SD	USB_90D	USB	USB_CARDREADER_P 9 20
	USB_90D	USB	USB_CARDREADER_N 9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
SMBUS_MCP_0_CLK	SMB_5SS	SMB	SMBUS_MCP_0_CLK 13 21 39
SMBUS_MCP_0_DATA	SMB_5SS	SMB	SMBUS_MCP_0_DATA 13 21 39
SMBUS_MCP_1_CLK	SMB_5SS	SMB	SMBUS_MCP_1_CLK 21 39
SMBUS_MCP_1_DATA	SMB_5SS	SMB	SMBUS_MCP_1_DATA 21 39
HDA_BIT_CLK	HDA_5SS	HDA	HDA_BIT_CLK 21 49
	HDA_5SS	HDA	HDA_BIT_CLK_R 21
HDA_SYNC	HDA_5SS	HDA	HDA_SYNC 21 49
	HDA_5SS	HDA	HDA_SYNC_R 21
HDA_RST_L	HDA_5SS	HDA	HDA_RST_R_L 21
	HDA_5SS	HDA	HDA_RST_L 21 49
HDA_SDIN0	HDA_5SS	HDA	HDA_SDIN0 21 49
	HDA_5SS	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_5SS	HDA	HDA_SDOUT 21 49
	HDA_5SS	HDA	HDA_SDOUT_R 21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
MCP_SUS_CLK	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK_R 21 25
	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK 25 36
SPI_CLK	SPI_5SS	SPI	SPI_CLK_R 21 38 48
	SPI_5SS	SPI	SPI_CLK 48
	SPI_5SS	SPI	SPI_ALT_CLK 38
SPI_MOSI	SPI_5SS	SPI	SPI_MOSI_R 21 38 48
	SPI_5SS	SPI	SPI_MOSI 48
	SPI_5SS	SPI	SPI_ALT_MOSI 38
SPI_MISO	SPI_5SS	SPI	SPI_MISO 21 38 48
	SPI_5SS	SPI	SPI_MISO_R 48
	SPI_5SS	SPI	SPI_ALT_MISO 38
SPI_CS0	SPI_5SS	SPI	SPI_CS0_R_L 21 38
	SPI_5SS	SPI	SPI_CS0_L
	SPI_5SS	SPI	SPI_CS1_R_L
	SPI_5SS	SPI	SPI_CS1_R_L_USE_MLB

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 32
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31 32
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 31
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 31
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 31
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 31
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 31
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 31
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 31
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 31
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 31
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31 33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_555	SMB	SMBUS_SMC_A_S3_SCL	7 39
SMBUS_SMC_A_S3_SDA	SMB_555	SMB	SMBUS_SMC_A_S3_SDA	7 39
SMBUS_SMC_B_S0_SCL	SMB_555	SMB	SMBUS_SMC_B_S0_SCL	39
SMBUS_SMC_B_S0_SDA	SMB_555	SMB	SMBUS_SMC_B_S0_SDA	39
SMBUS_SMC_0_S0_SCL	SMB_555	SMB	SMBUS_SMC_0_S0_SCL	39
SMBUS_SMC_0_S0_SDA	SMB_555	SMB	SMBUS_SMC_0_S0_SDA	39
SMBUS_SMC_BSA_SCL	SMB_555	SMB	SMBUS_SMC_BSA_SCL	7 39
SMBUS_SMC_BSA_SDA	SMB_555	SMB	SMBUS_SMC_BSA_SDA	7 39
SMBUS_SMC_MGMT_SCL	SMB_555	SMB	SMBUS_SMC_MGMT_SCL	39
SMBUS_SMC_MGMT_SDA	SMB_555	SMB	SMBUS_SMC_MGMT_SDA	39

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K84 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DIFFPAIR			CHGR_CSO_R_P	56
DIFFPAIR			CHGR_CSO_R_N	56
DIFFPAIR			CPUTHMSNS_D2_P	42
DIFFPAIR			CPUTHMSNS_D2_N	42
DIFFPAIR			CPU_THERMD_P	10 42
DIFFPAIR			CPU_THERMD_N	10 42
DIFFPAIR			ISNS_CPUVTT_P	41
DIFFPAIR			ISNS_CPUVTT_N	41
DIFFPAIR			ISNS_HDD_P	34 47
DIFFPAIR			ISNS_HDD_N	34 47
DIFFPAIR			ISNS_HDD_R_P	47
DIFFPAIR			ISNS_HDD_R_N	47
DIFFPAIR			MCPTHMSNS_D2_P	42
DIFFPAIR			MCPTHMSNS_D2_N	42
DIFFPAIR			MCP_THMDIODE_P	21 42
DIFFPAIR			MCP_THMDIODE_N	21 42
DIFFPAIR			ISNS_ODD_P	34 47
DIFFPAIR			ISNS_ODD_N	34 47
DIFFPAIR			ISNS_ODD_R_P	47
DIFFPAIR			ISNS_ODD_R_N	47
DIFFPAIR			ISNS_AIRPORT_P	30 47
DIFFPAIR			ISNS_AIRPORT_N	30 47
DIFFPAIR			ISNS_AIRPORT_R_P	47
DIFFPAIR			ISNS_AIRPORT_R_N	47
DIFFPAIR			ISNS_1V5_S3_P	47 58
DIFFPAIR			ISNS_1V5_S3_N	47 58
DIFFPAIR			ISNS_1V5_S3_R_P	47
DIFFPAIR			ISNS_1V5_S3_R_N	47
DIFFPAIR			ISNS_LCDBKLT_P	47 68
DIFFPAIR			ISNS_LCDBKLT_N	47 68

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K84 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=S0_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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K84 RULE DEFINITIONS

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