1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		293301	PRODUCTION RELEASED	09/11/03	?

SCHEM,MLB,PB17"

09/04/2003

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8	INTREPID MAXBUS AND BOOT STRAPS
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11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
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21	M10 ANALOG, POWER, GND

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22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
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29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
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32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
37	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6531	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 051-6531 REV. B

SHT 1 OF 44

U44 INTREPID

J18 Ethernet Connector P.28
4 DATA PAIRS
U49 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHz
J22 FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
U28 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
100MHZ

J11 OPTICAL DRIVE Connector P.25
EIDE
J13 ULTRA ATA/100 Connector P.25
UIDE

SLEEP LED P.26
LMU
J14 TUBA (SOUND) Connector P.26
I2S
I2C
I2C
U48/J2/J4 Fan Circuit P.26

J25 Battery Connector P.32
Power Supply & Charger P.32-36
J19 SUTRO (PWR) Connector P.32
SMBUS
3.3V
U39 PMU P.31
SERIAL
5V
U36 LMU P.24
I2C

J10 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U26 TI PCI1510 CardBus Controller P.18
PCI BUS
32BITS
33MHZ
3.3V

J3 (SHARE WITH BLUETOOTH)
LEFT USB P.25
USB 2.0
J12
RIGHT USB BACKUP BATTERY P.33
NOT USED
USB 2.0
J3 (SHARE WITH LEFT USB)
BlueTooth P.25
NOT USED
J9
Modem Board Connector P.26
INTRPEID
I2C

ETHERNET 10/100/1000 P.14	FIREWIRE 800 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15
USB PORT A P.15					SCCA P.15	
USB PORT B P.15					VIA/PMU P.15	
USB PORT C P.15					BOOTROM P.14	
USB PORT D P.15					PCI 32BITS 33MHZ P.13	
USB PORT E P.15						
USB PORT F P.15						
MAXBUS P.9	DDR MEMORY P.10				4X AGP P.13	

NOT USED

J5 Serial Debug Connector P.26
J15 TRACKPAD Connector | Keyboard Connector
KB LED LIGHT SENSOR P.24
U17 BOOT ROM 1M X 8 P.10
U52 USB 2.0 CONTROLLER P.27

AGP BUS
1.5V/3.3V
32BITS
66MHZ
U43 ATI M10 64MB P.18-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
J21 AIRPOPT Connector P.25

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U42 APOLLO CPU (MPC7457) P.5-6
CPU PLL Config P.7
PMU

MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14 2:1 DDR MUXES P.11
J20/J23 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.12

J8 Inverter Connector P.22

LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)
J7 LCD Panel Connector P.22
J17 S-Video Connector P.22
J16 DVI-I Connector P.22

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6531 | REV. B
SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
PG 31

INRUSH LIMITER
PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS
DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS
+3V_PMU LDO
PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

+5V_MAIN
DCDC_EN_L
AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

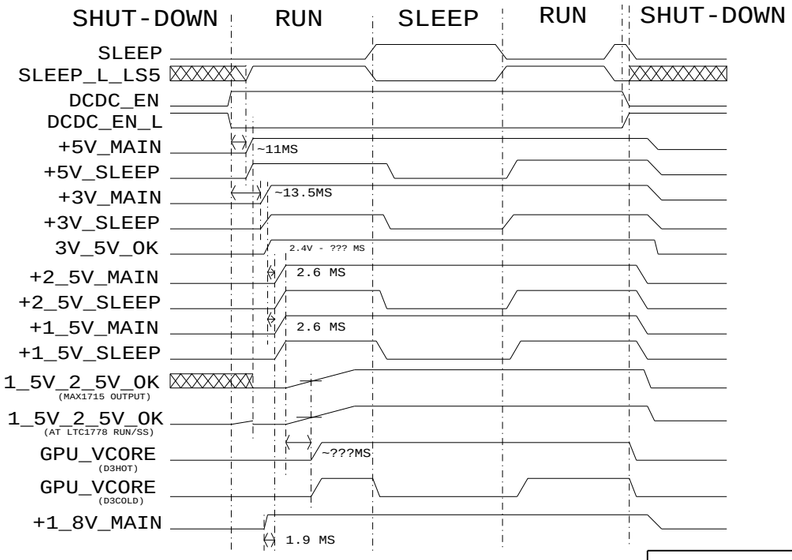
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

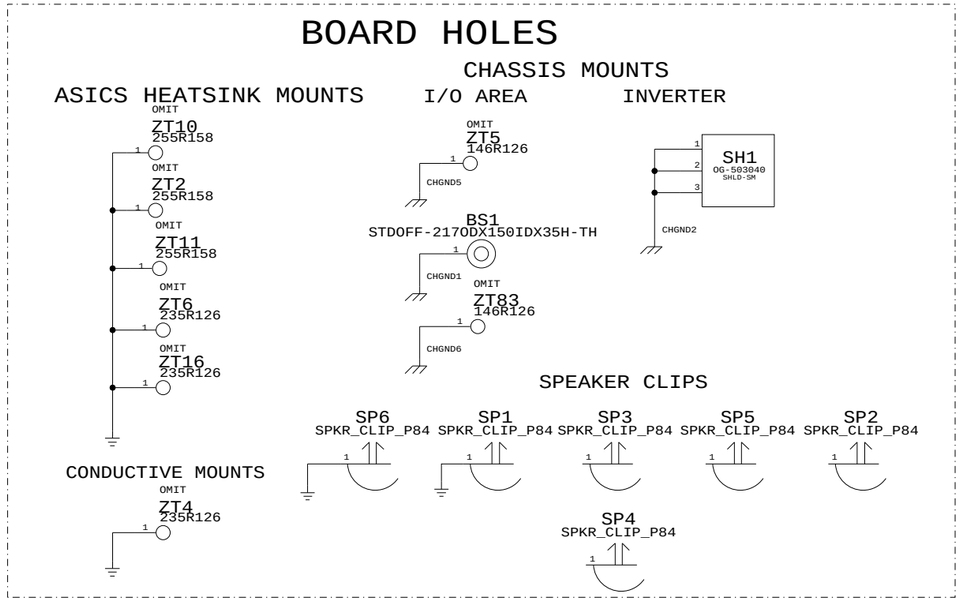
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

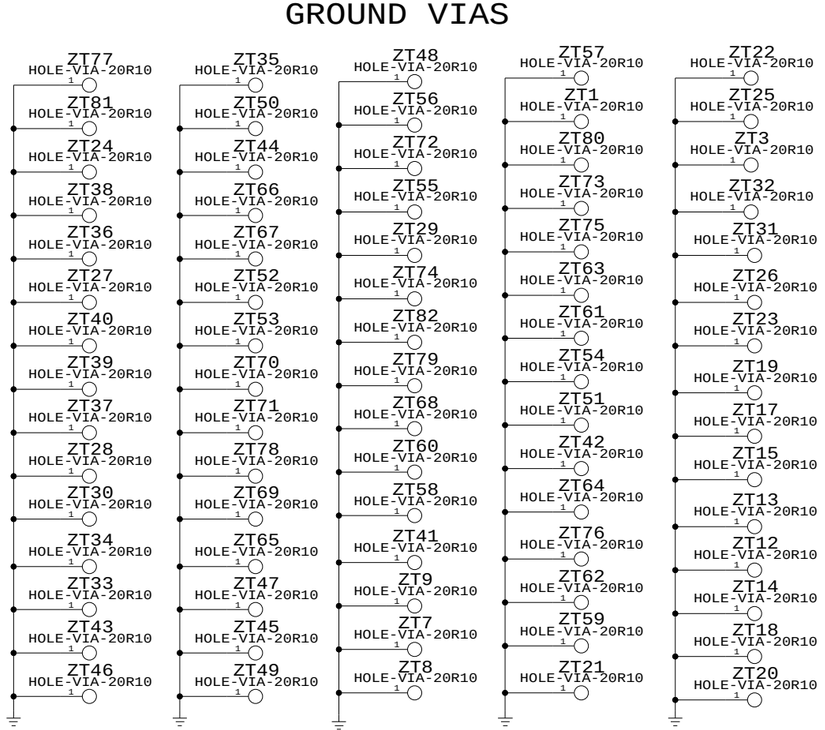
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



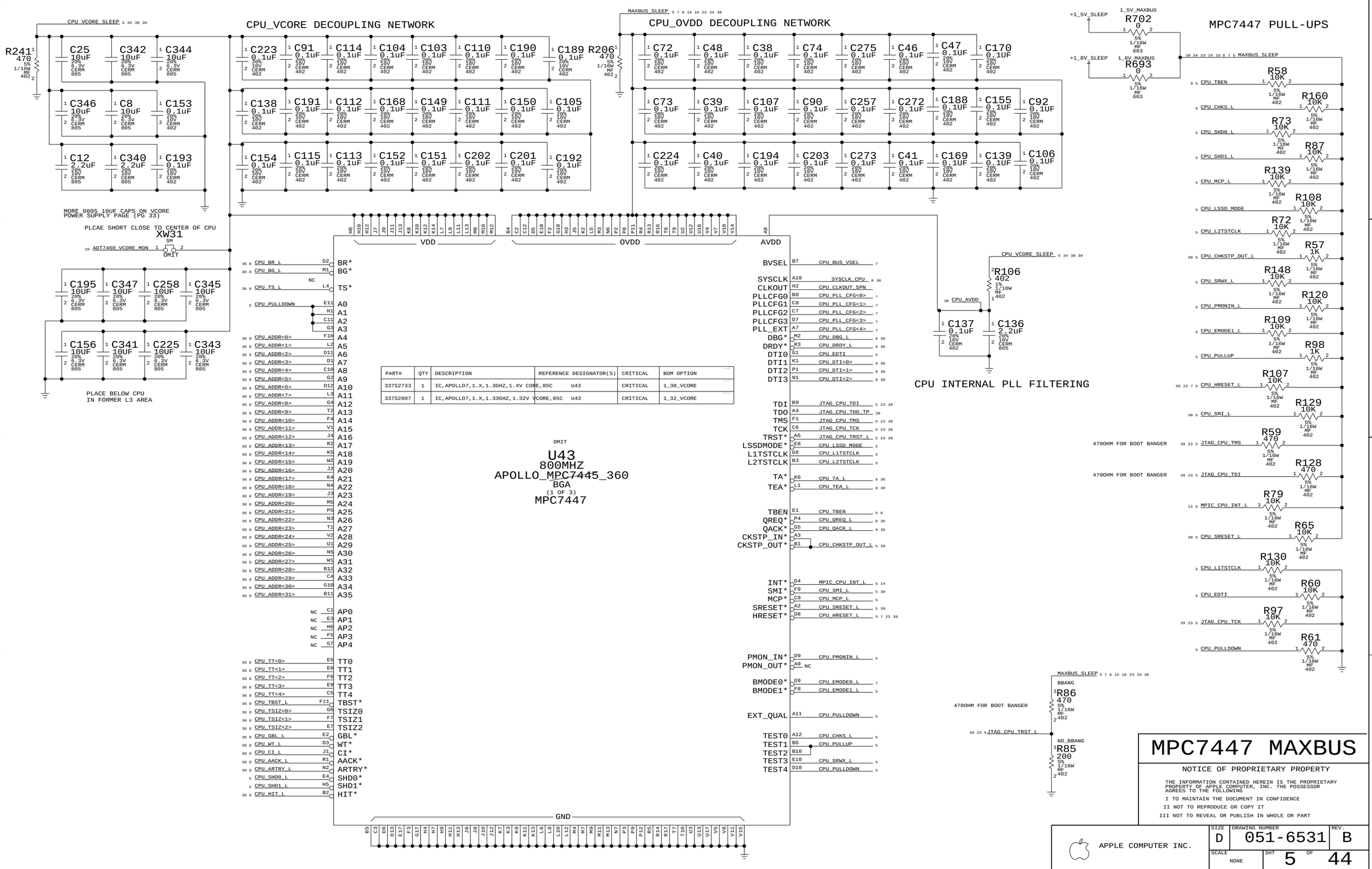
GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 4 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
337S2807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22

OMIT
U43
800MHZ
BGA
(2 OF 3)
APOLLO_MPC7445_360

36 8	CPU_DATA<0>	R15	D0
36 8	CPU_DATA<1>	W15	D1
36 8	CPU_DATA<2>	T14	D2
36 8	CPU_DATA<3>	V16	D3
36 8	CPU_DATA<4>	W16	D4
36 8	CPU_DATA<5>	T15	D5
36 8	CPU_DATA<6>	U15	D6
36 8	CPU_DATA<7>	P14	D7
36 8	CPU_DATA<8>	V13	D8
36 8	CPU_DATA<9>	W13	D9
36 8	CPU_DATA<10>	T13	D10
36 8	CPU_DATA<11>	P13	D11
36 8	CPU_DATA<12>	U14	D12
36 8	CPU_DATA<13>	W14	D13
36 8	CPU_DATA<14>	R12	D14
36 8	CPU_DATA<15>	T12	D15
36 8	CPU_DATA<16>	W12	D16
36 8	CPU_DATA<17>	V12	D17
36 8	CPU_DATA<18>	N11	D18
36 8	CPU_DATA<19>	N10	D19
36 8	CPU_DATA<20>	R11	D20
36 8	CPU_DATA<21>	U11	D21
36 8	CPU_DATA<22>	W11	D22
36 8	CPU_DATA<23>	T11	D23
36 8	CPU_DATA<24>	R10	D24
36 8	CPU_DATA<25>	N9	D25
36 8	CPU_DATA<26>	P10	D26
36 8	CPU_DATA<27>	U10	D27
36 8	CPU_DATA<28>	R9	D28
36 8	CPU_DATA<29>	W10	D29
36 8	CPU_DATA<30>	U9	D30
36 8	CPU_DATA<31>	V9	D31
36 8	CPU_DATA<32>	W5	D32
36 8	CPU_DATA<33>	U6	D33
36 8	CPU_DATA<34>	T5	D34
36 8	CPU_DATA<35>	U5	D35
36 8	CPU_DATA<36>	W7	D36
36 8	CPU_DATA<37>	R6	D37
36 8	CPU_DATA<38>	P7	D38
36 8	CPU_DATA<39>	V6	D39
36 8	CPU_DATA<40>	P17	D40
36 8	CPU_DATA<41>	R19	D41
36 8	CPU_DATA<42>	V18	D42
36 8	CPU_DATA<43>	R18	D43
36 8	CPU_DATA<44>	V19	D44
36 8	CPU_DATA<45>	T19	D45
36 8	CPU_DATA<46>	U19	D46
36 8	CPU_DATA<47>	W19	D47
36 8	CPU_DATA<48>	U18	D48
36 8	CPU_DATA<49>	W17	D49
36 8	CPU_DATA<50>	W18	D50
36 8	CPU_DATA<51>	T16	D51
36 8	CPU_DATA<52>	T18	D52
36 8	CPU_DATA<53>	T17	D53
36 8	CPU_DATA<54>	W3	D54
36 8	CPU_DATA<55>	V17	D55
36 8	CPU_DATA<56>	U4	D56
36 8	CPU_DATA<57>	U8	D57
36 8	CPU_DATA<58>	U7	D58
36 8	CPU_DATA<59>	R7	D59
36 8	CPU_DATA<60>	P6	D60
36 8	CPU_DATA<61>	R8	D61
36 8	CPU_DATA<62>	W8	D62
36 8	CPU_DATA<63>	T8	D63
NC	T3		DP0
NC	W4		DP1
NC	T4		DP2
NC	W9		DP3
NC	M6		DP4
NC	V3		DP5
NC	N8		DP6
NC	W6		DP7

OMIT
U43
800MHZ
BGA
(3 OF 3)
APOLLO_MPC7445_360

NC	F18	NC_F18
NC	F17	NC_F17
NC	F19	NC_F19
NC	H19	NC_H19
NC	H18	NC_H18
NC	H17	NC_H17
NC	H16	NC_H16
NC	E19	NC_E19
NC	D18	NC_D18
NC	F16	NC_F16
NC	G16	NC_G16
NC	D19	NC_D19
NC	F15	NC_F15
NC	G19	NC_G19
NC	E16	NC_E16
NC	D17	NC_D17
NC	D16	NC_D16
NC	P15	NC_P15
NC	L15	NC_L15
NC	N15	NC_N15
NC	P18	NC_P18
NC	N14	NC_N14
NC	M14	NC_M14
NC	M17	NC_M17
NC	N13	NC_N13
NC	N16	NC_N16
NC	M19	NC_M19
NC	M16	NC_M16
NC	P19	NC_P19
NC	N17	NC_N17
NC	M15	NC_M15
NC	L17	NC_L17
NC	L14	NC_L14
NC	K15	NC_K15
NC	J14	NC_J14
NC	J18	NC_J18
NC	J19	NC_J19
NC	J15	NC_J15
NC	K19	NC_K19
NC	J16	NC_J16
NC	H15	NC_H15
NC	L16	NC_L16
NC	P16	NC_P16
NC	M18	NC_M18
NC	L19	NC_L19
NC	L18	NC_L18
NC	K18	NC_K18
NC	J17	NC_J17
NC	K16	NC_K16
NC	C19	NC_C19
NC	D15	NC_D15
NC	G15	NC_G15
NC	C18	NC_C18
NC	A16	NC_A16
NC	B19	NC_B19
NC	A19	NC_A19
NC	D14	NC_D14
NC	E15	NC_E15
NC	B15	NC_B15
NC	B17	NC_B17
NC	C17	NC_C17
NC	C16	NC_C16
NC	G13	NC_G13
NC	E14	NC_E14
NC	H14	NC_H14
NC	G14	NC_G14
NC	C15	NC_C15
NC	A17	NC_A17
NC	G12	NC_G12
NC	F14	NC_F14
NC	F13	NC_F13
NC	E13	NC_E13
NC	B16	NC_B16
NC	A15	NC_A15
NC	C14	NC_C14
NC	A18	NC_A18
NC	A13	NC_A13
NC	F12	NC_F12
NC	A14	NC_A14
NC	G11	NC_G11
NC	C13	NC_C13
NC	N12	NC_N12
NC	N18	NC_N18
NC	K17	NC_K17
NC	N19	NC_N19
NC	B18	NC_B18
NC	E12	NC_E12
NC	B13	NC_B13
NC	B14	NC_B14
NC	A6	NC_A6

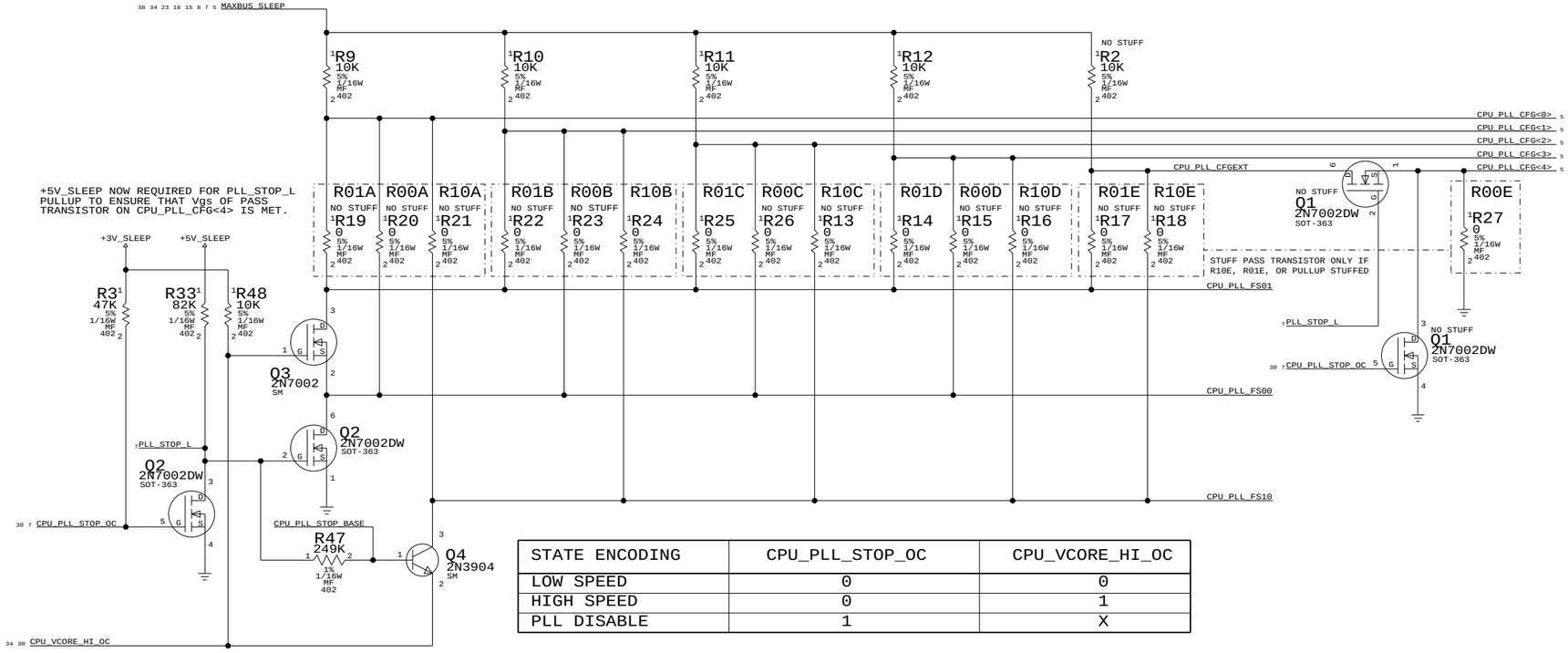
MPC7447/BBANG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B

SCALE	SHT	OF
NONE	6	44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

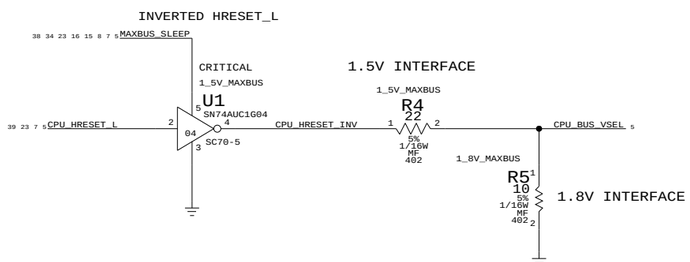
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

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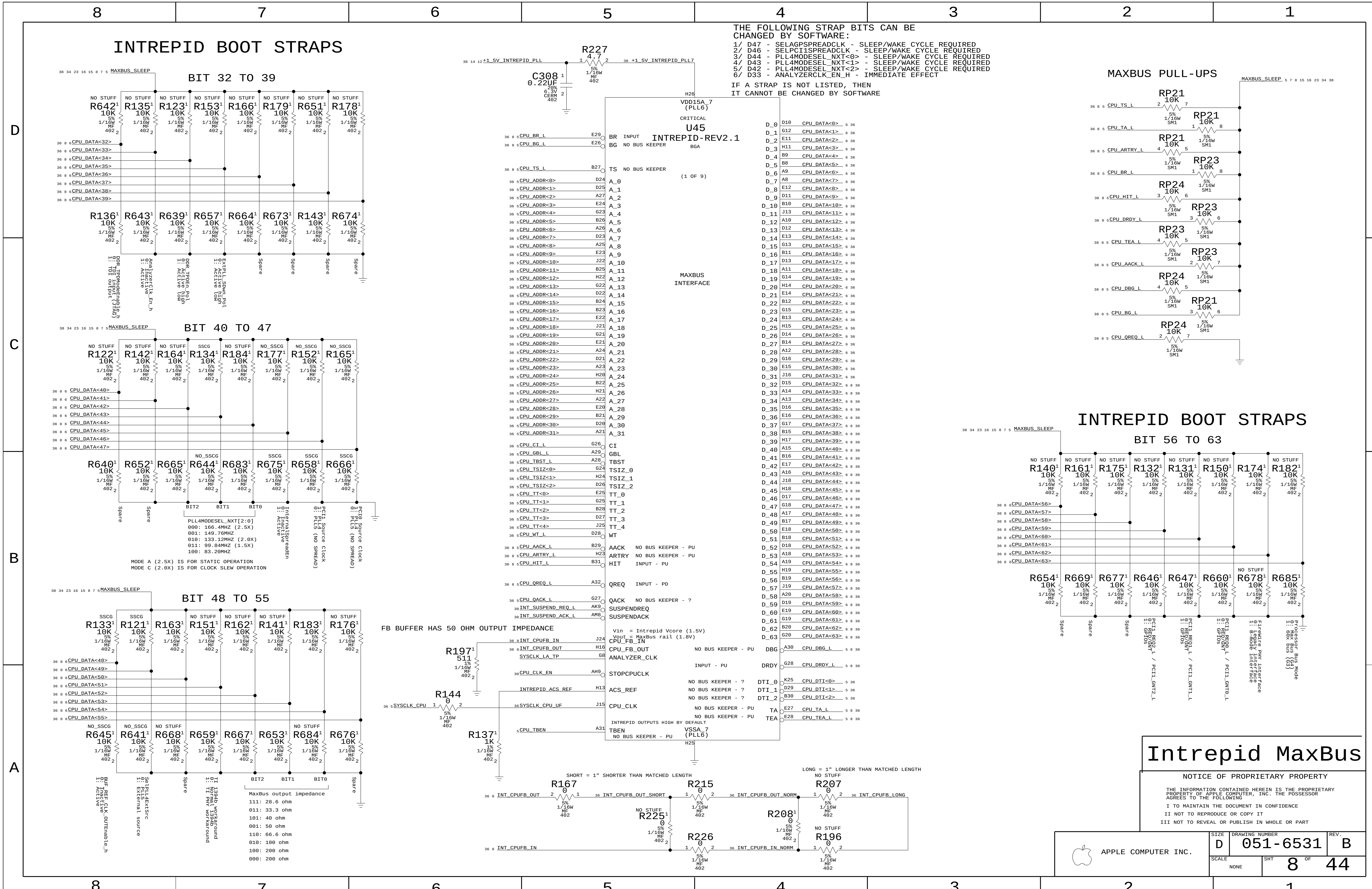

INTREPID BOOT STRAPS
BIT 32 TO 39
BIT 40 TO 47
BIT 48 TO 55
INTREPID BOOT STRAPS
BIT 56 TO 63
MAXBUS PULL-UPS
THE FOLLOWING STRAP BITS CAN BE
CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT
IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE
U45
INTREPID-REV2.1
BGA
(1 OF 9)
MAXBUS
INTERFACE
PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ
MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION
FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE
Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)
INTREPID OUTPUTS HIGH BY DEFAULT
MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm
SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH
Intrepid MaxBus
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REV. B
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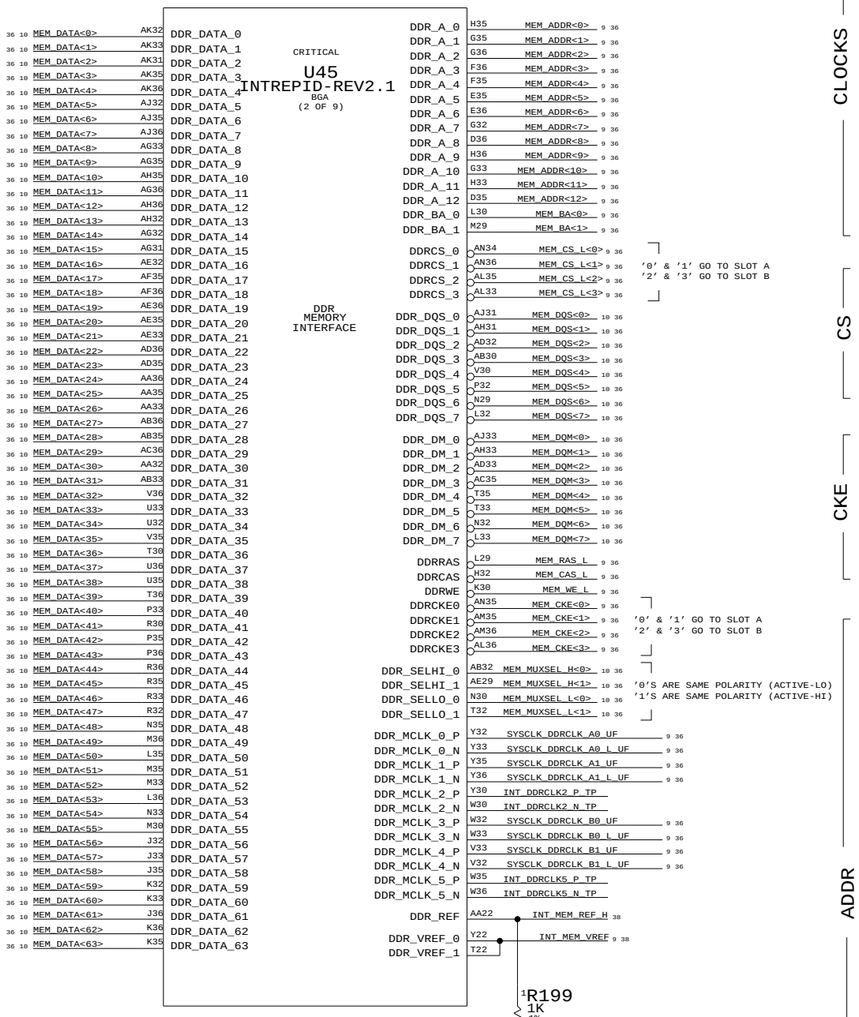
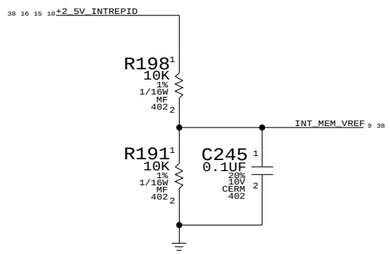
SHT 8 OF 44

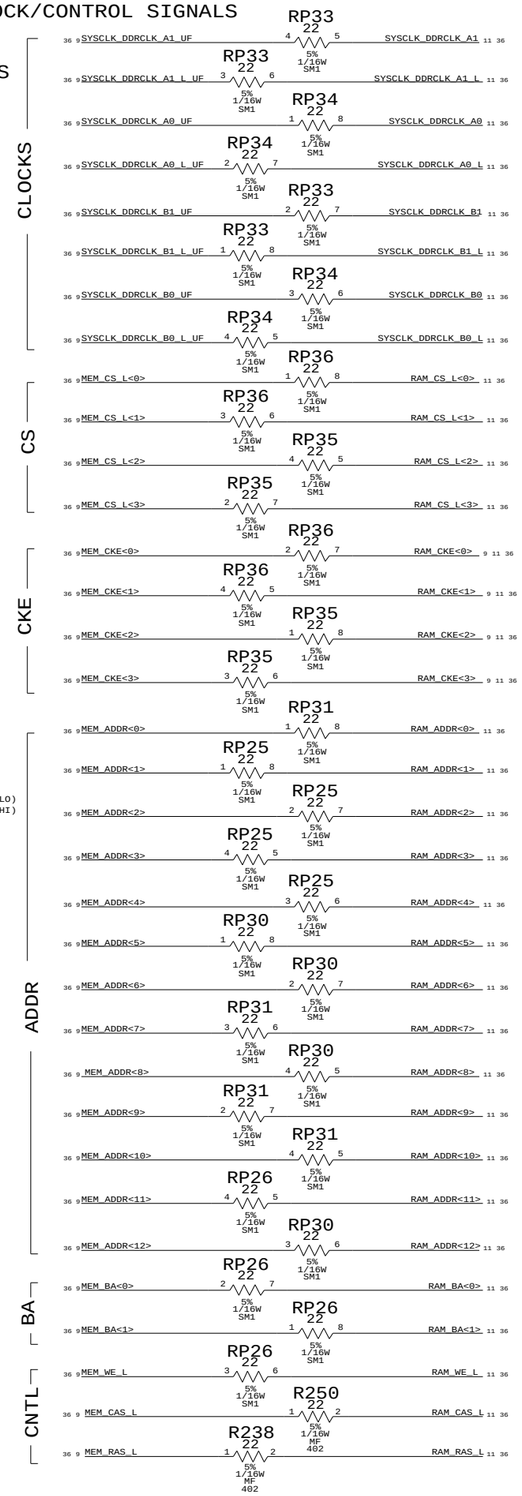
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

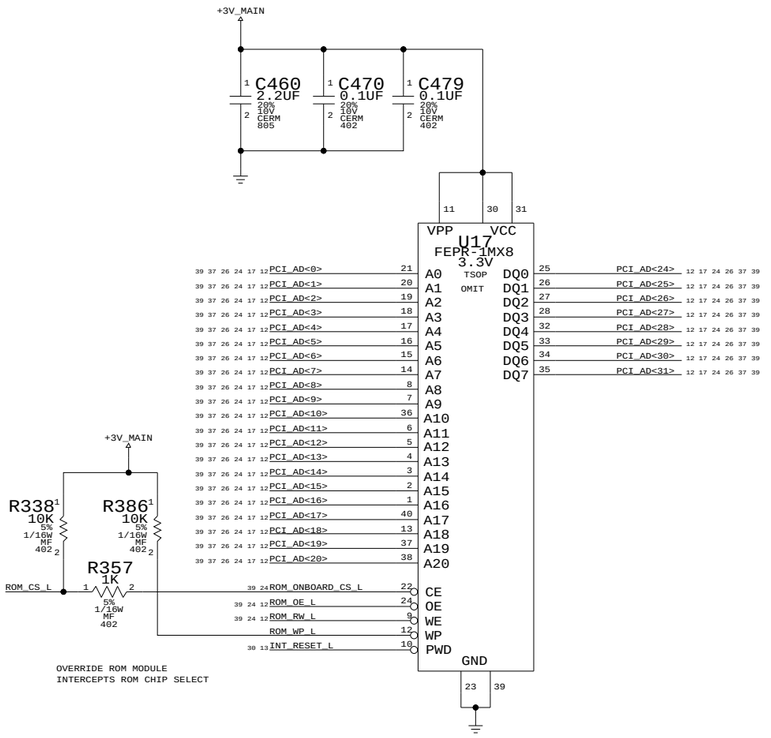


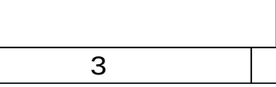
MEM_VREF





1MB BOOT ROM

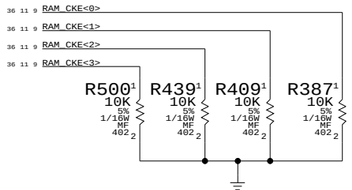




OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1336	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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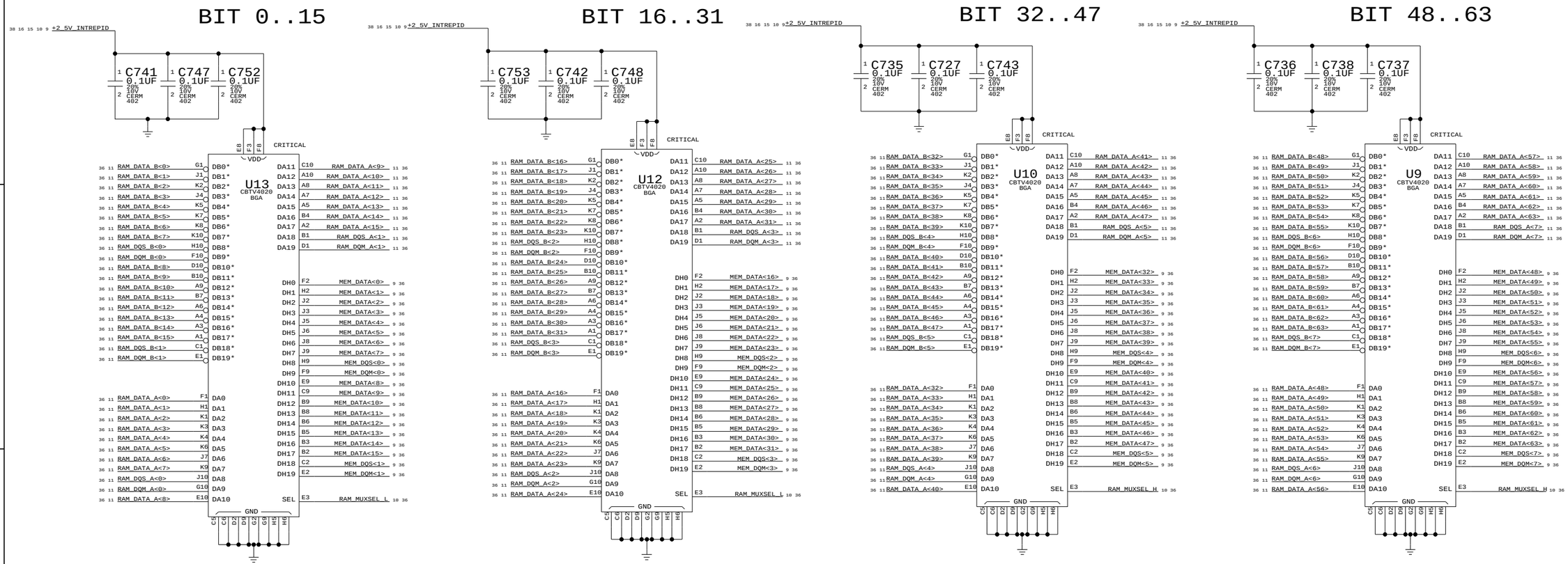

SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

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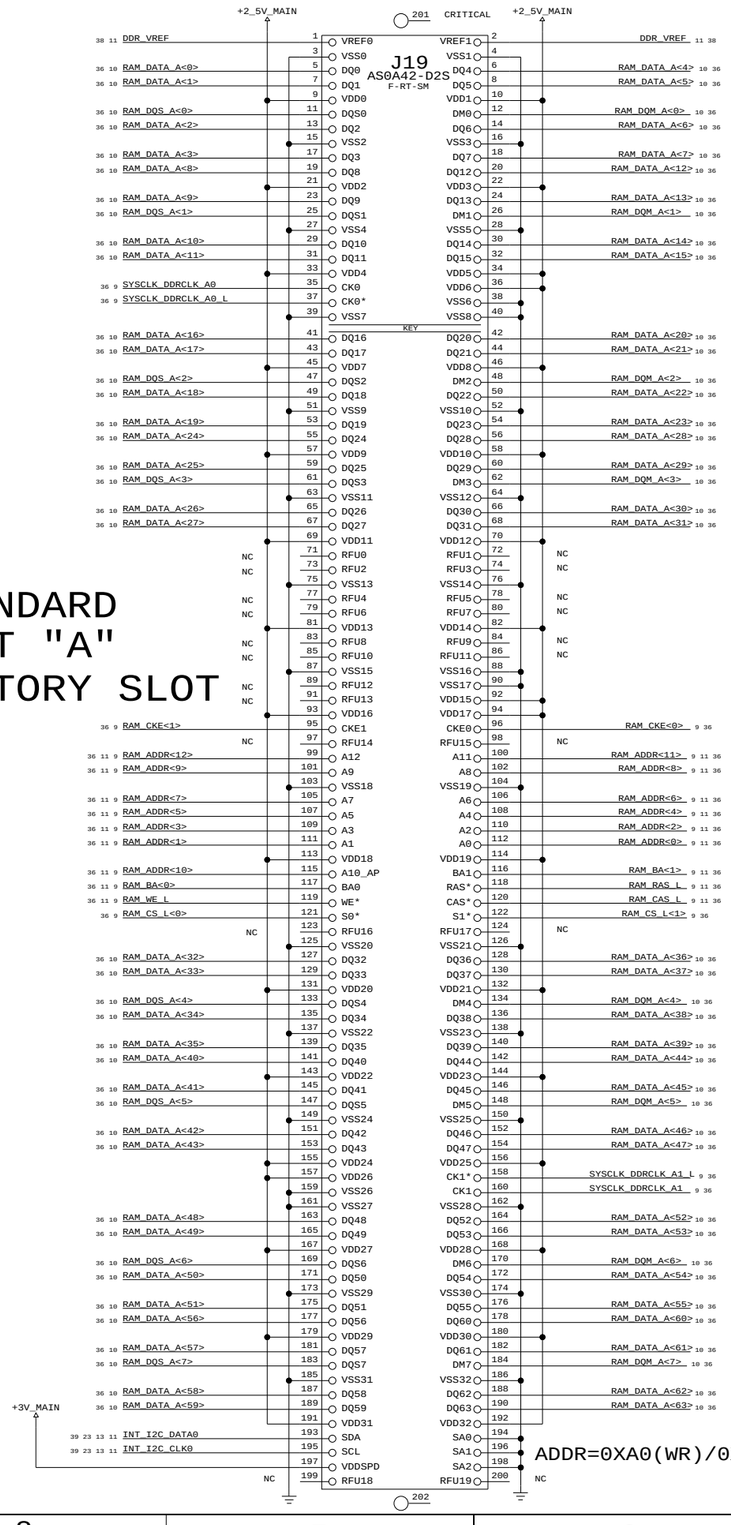
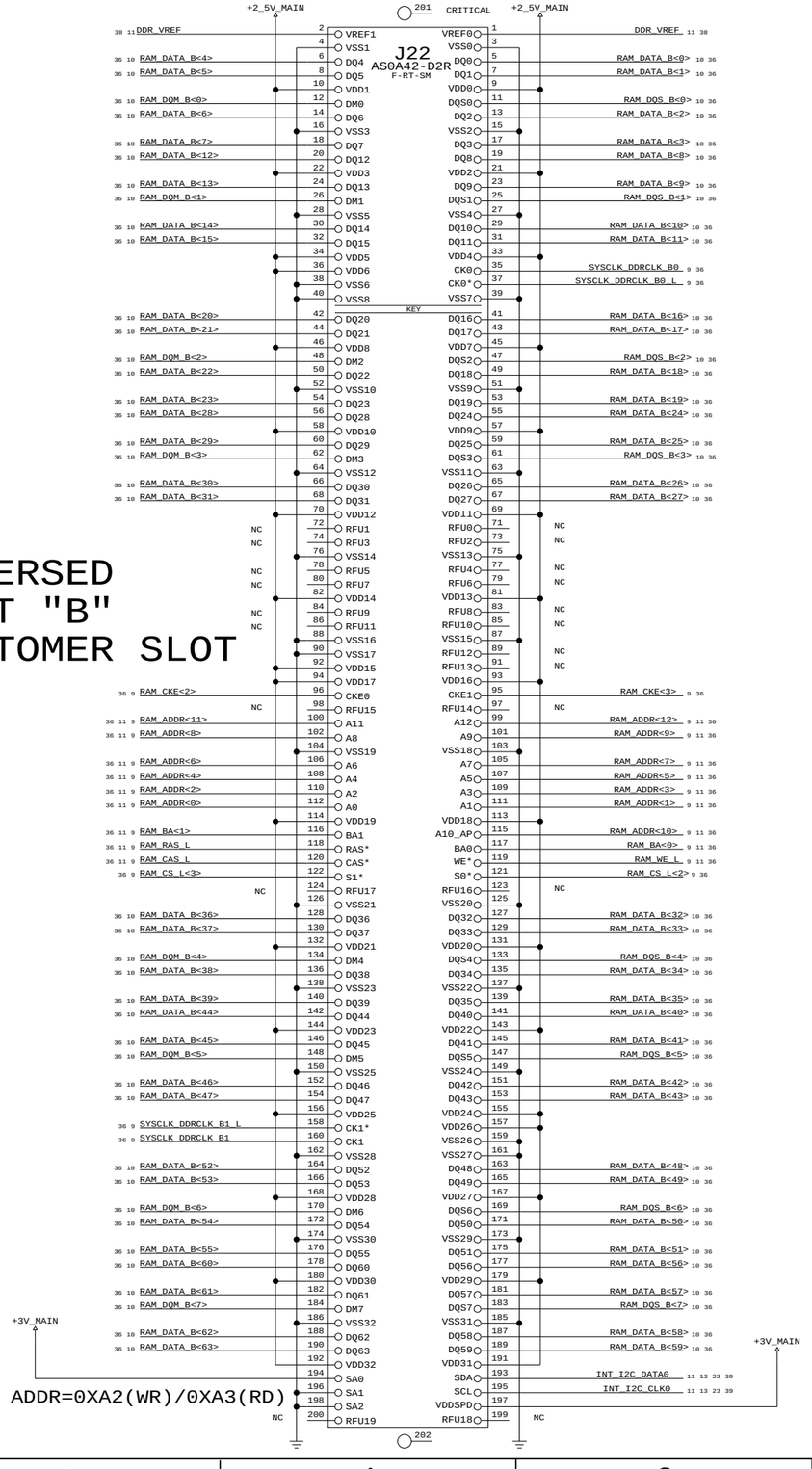
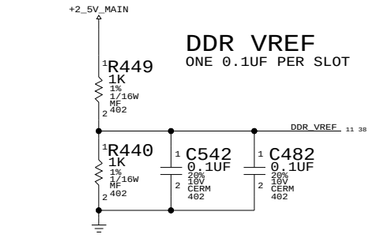
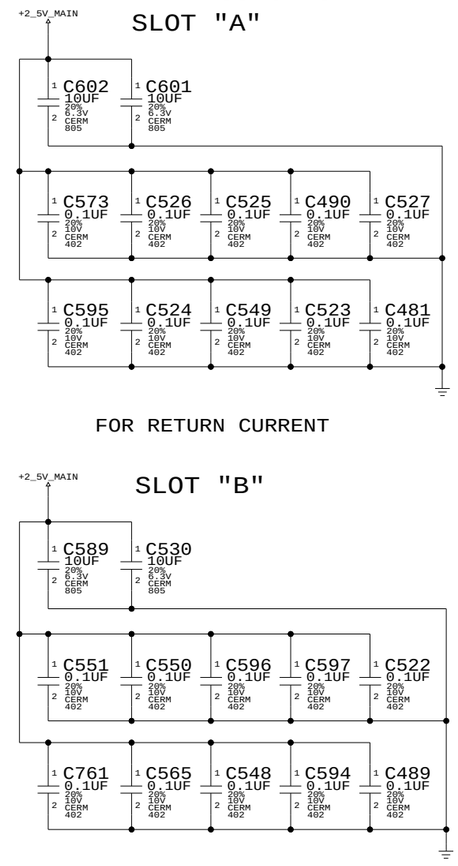
STANDARD SLOT "A" FACTORY SLOT



REVERSED SLOT "B" CUSTOMER SLOT







DDR SODIMM CONNS

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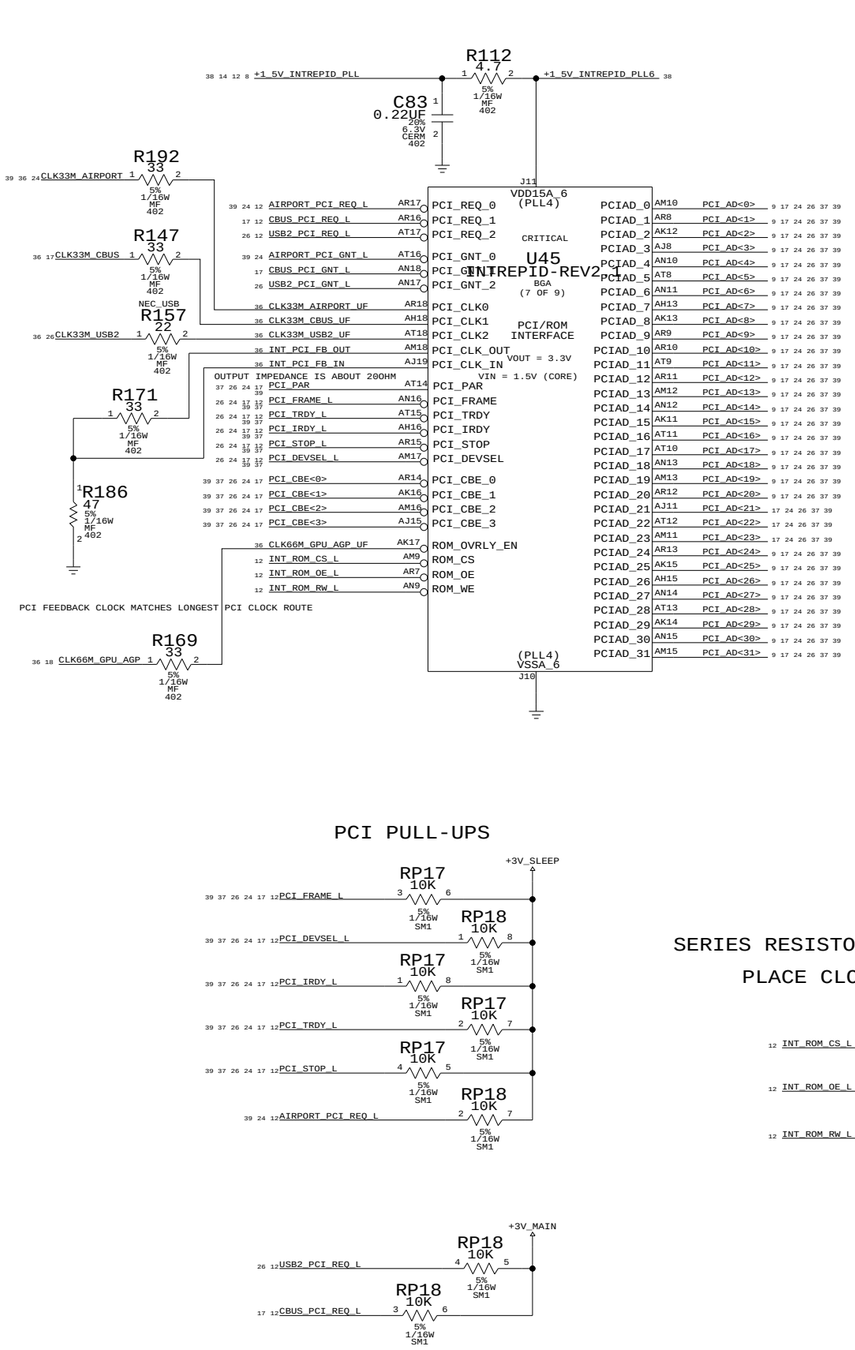
NONE	11	44

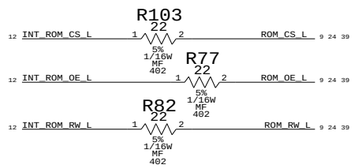


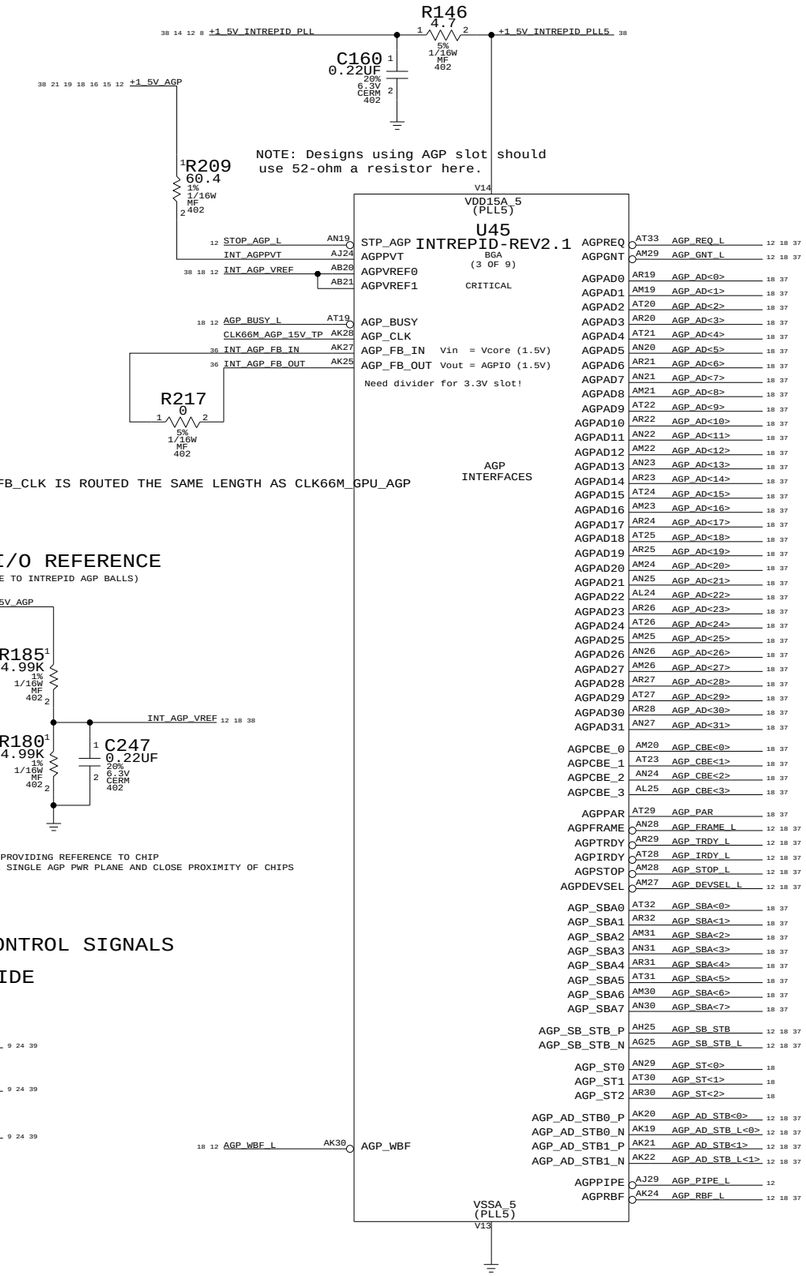
PCI PULL-UPS

USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE



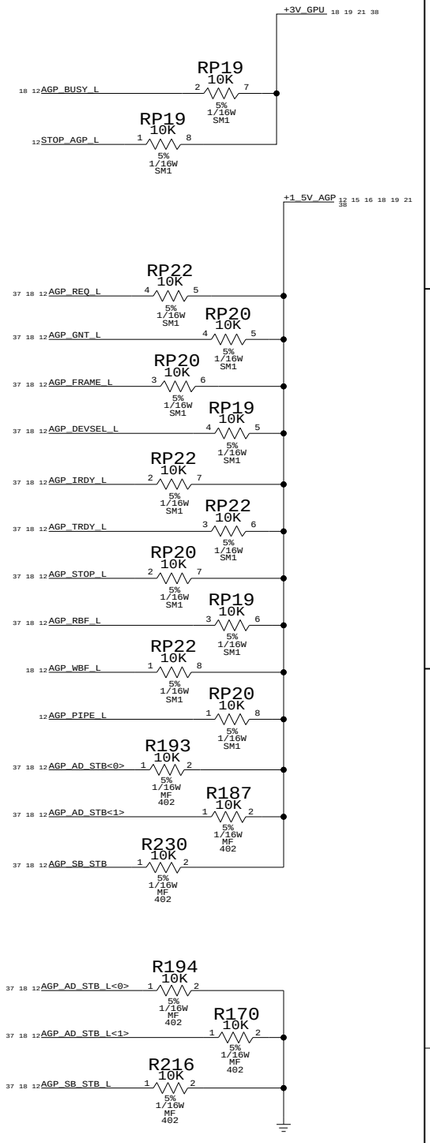


AGP I/O REFERENCE

(PLACE CLOSE TO INTREPID AGP BALLS)

SIMPLY PROVIDING REFERENCE TO CHIP BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

AGP PULL-UPS/PULL DOWNS



INTREPID AGP/PCI

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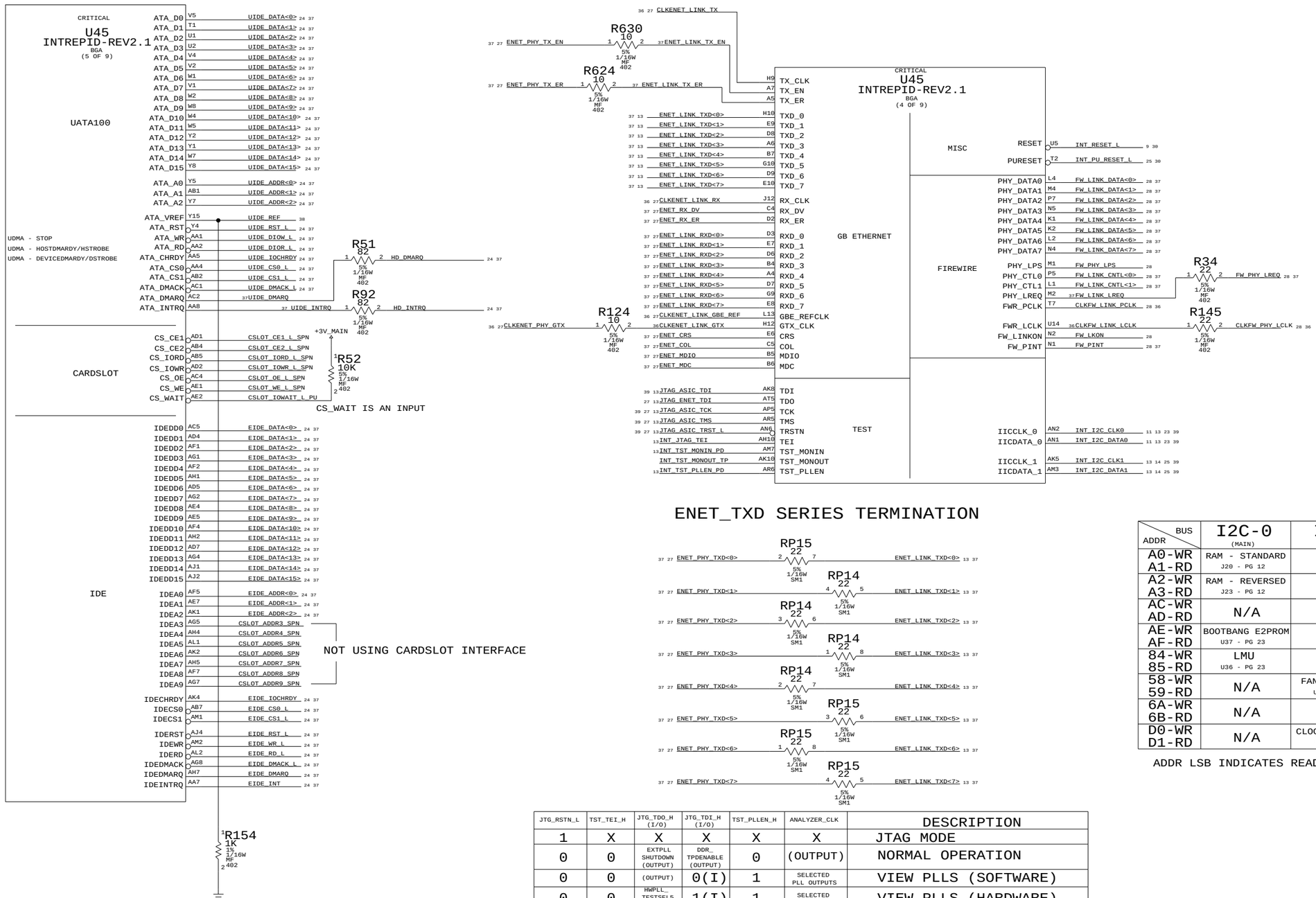
SCALE: NONE	SHT 12 OF 44	



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ (’1’) OR WRITE (’0’) MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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SIZE	DRAWING NUMBER	REV.
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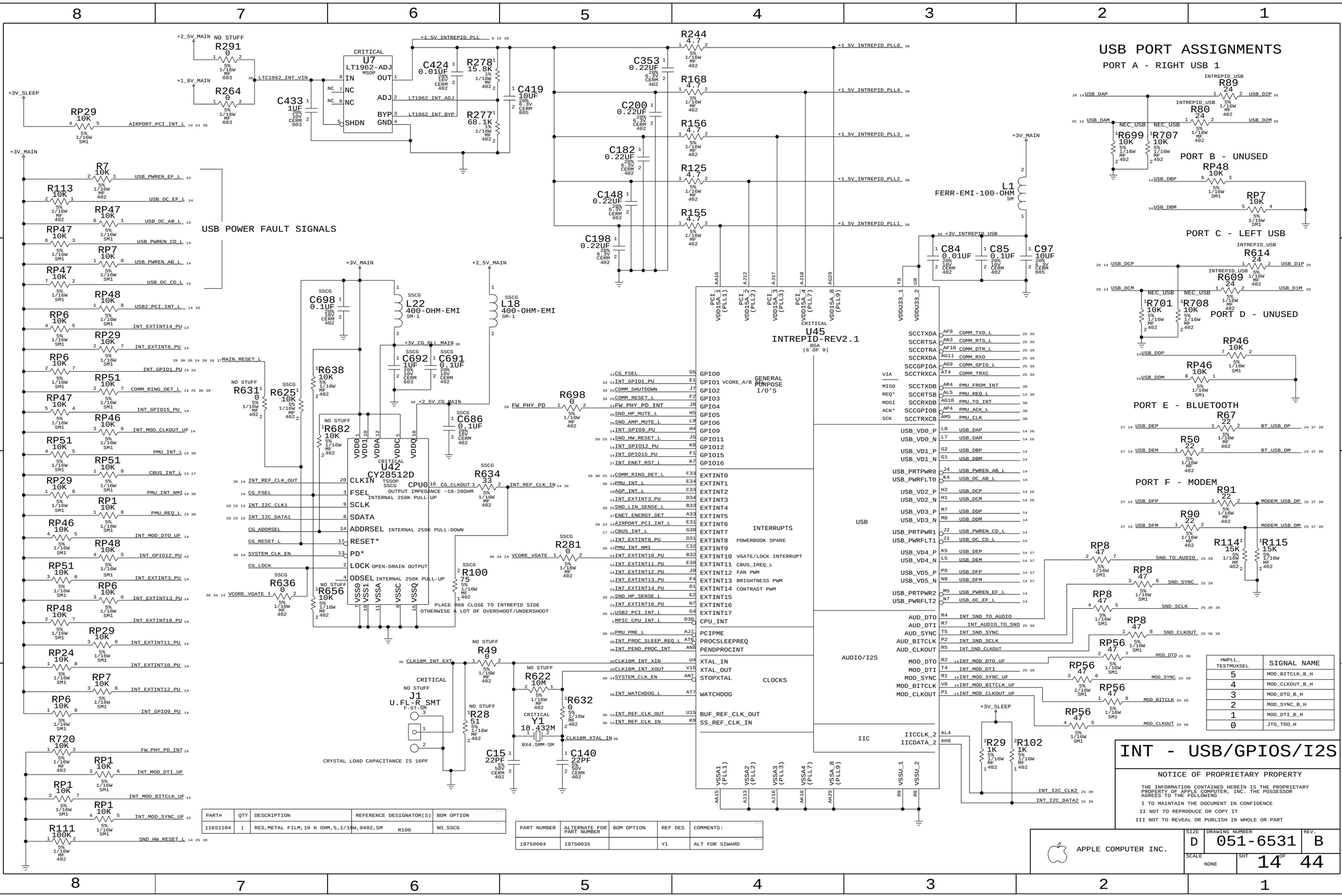
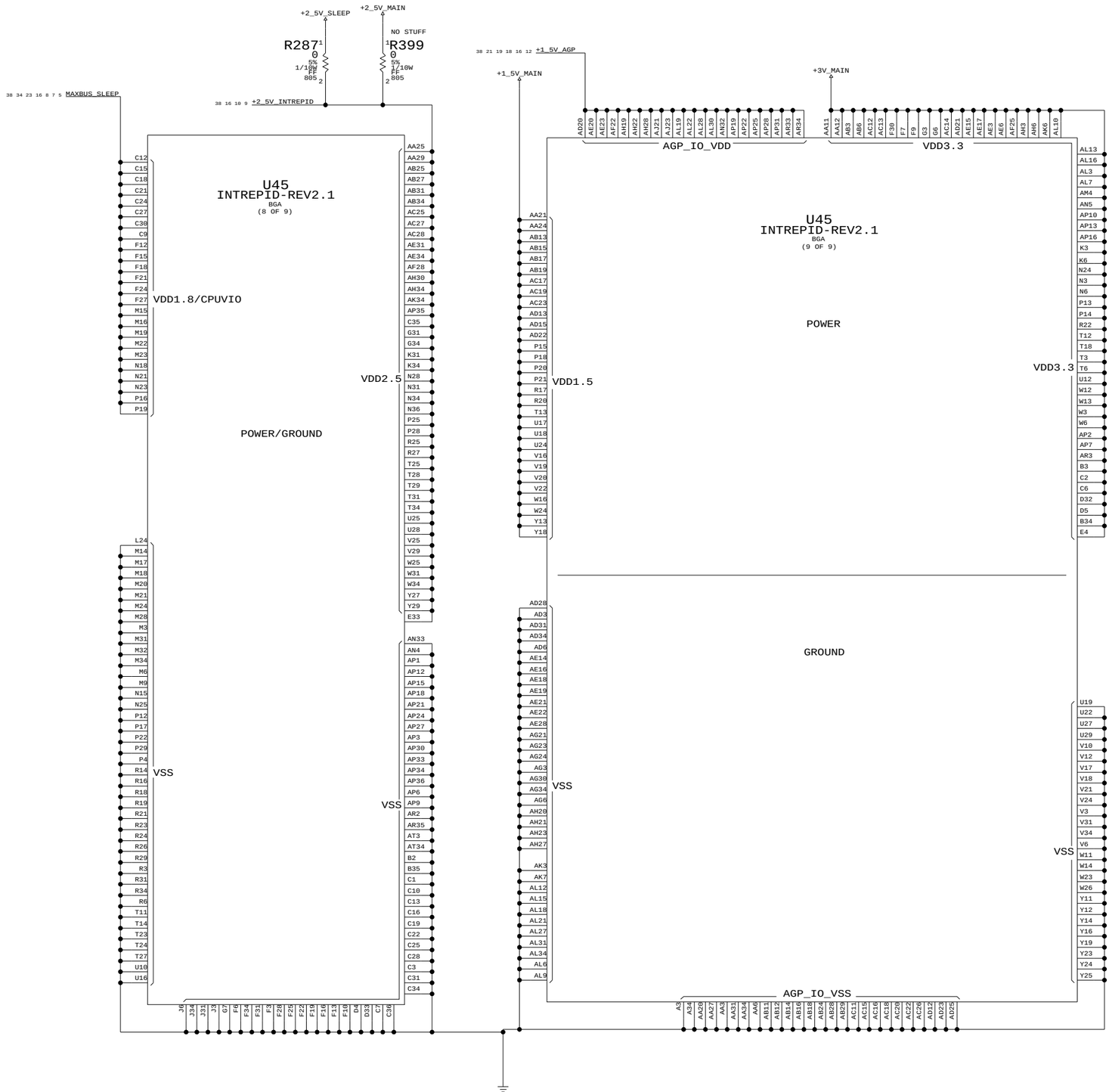
SCALE: NONE	SHT 13 OF 44	



HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD



Intrepid Power

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SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

38 34 23 15 8 7 6 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C239 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C94 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402

C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805 · C174 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C95 0.22uF 20% 6.3V CERM 402 · C117 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C314 0.22uF 20% 6.3V CERM 402

C173 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C175 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C118 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C119 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402

C205 0.22uF 20% 6.3V CERM 402 · C209 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C356 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C355 0.22uF 20% 6.3V CERM 402 · C267 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C298 0.22uF 20% 6.3V CERM 402 · C377 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402

C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805 · C228 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C265 0.22uF 20% 6.3V CERM 402 · C378 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C325 0.22uF 20% 6.3V CERM 402 · C393 0.22uF 20% 6.3V CERM 402 · C324 0.22uF 20% 6.3V CERM 402 · C323 0.22uF 20% 6.3V CERM 402

C251 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C249 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C407 0.22uF 20% 6.3V CERM 402 · C391 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C480 0.22uF 20% 6.3V CERM 402 · C390 0.22uF 20% 6.3V CERM 402 · C370 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C365 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402

C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805 · C367 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C403 0.22uF 20% 6.3V CERM 402 · C291 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C322 0.22uF 20% 6.3V CERM 402 · C392 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402 · C376 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C399 0.22uF 20% 6.3V CERM 402 · C410 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C384 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402 · C406 0.22uF 20% 6.3V CERM 402 · C405 0.22uF 20% 6.3V CERM 402

C404 0.22uF 20% 6.3V CERM 402 · C400 0.22uF 20% 6.3V CERM 402 · C386 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402 · C387 0.22uF 20% 6.3V CERM 402 · C401 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C389 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402 · C398 0.22uF 20% 6.3V CERM 402

C337 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C402 0.22uF 20% 6.3V CERM 402 · C397 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C388 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C336 0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C147 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C142 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402

C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805 · C244 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402

C144 0.22uF 20% 6.3V CERM 402 · C246 0.22uF 20% 6.3V CERM 402 · C211 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402 · C197 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C375 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C53 0.22uF 20% 6.3V CERM 402 · C42 0.22uF 20% 6.3V CERM 402 · C21 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C31 0.22uF 20% 6.3V CERM 402 · C143 0.22uF 20% 6.3V CERM 402 · C123 0.22uF 20% 6.3V CERM 402 · C121 0.22uF 20% 6.3V CERM 402

C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805 · C33 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402 · C43 0.22uF 20% 6.3V CERM 402 · C35 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C60 0.22uF 20% 6.3V CERM 402 · C52 0.22uF 20% 6.3V CERM 402 · C199 0.22uF 20% 6.3V CERM 402 · C57 0.22uF 20% 6.3V CERM 402 · C19 0.22uF 20% 6.3V CERM 402

C16 0.22uF 20% 6.3V CERM 402 · C108 0.22uF 20% 6.3V CERM 402 · C55 0.22uF 20% 6.3V CERM 402 · C32 0.22uF 20% 6.3V CERM 402 · C125 0.22uF 20% 6.3V CERM 402 · C45 0.22uF 20% 6.3V CERM 402 · C76 0.22uF 20% 6.3V CERM 402 · C277 0.22uF 20% 6.3V CERM 402 · C28 0.22uF 20% 6.3V CERM 402 · C26 0.22uF 20% 6.3V CERM 402

C34 0.22uF 20% 6.3V CERM 402 · C23 0.22uF 20% 6.3V CERM 402 · C120 0.22uF 20% 6.3V CERM 402 · C146 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C30 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C96 0.22uF 20% 6.3V CERM 402 · C54 0.22uF 20% 6.3V CERM 402 · C50 0.22uF 20% 6.3V CERM 402

C75 0.22uF 20% 6.3V CERM 402 · C122 0.22uF 20% 6.3V CERM 402 · C51 0.22uF 20% 6.3V CERM 402 · C59 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C126 0.22uF 20% 6.3V CERM 402 · C98 0.22uF 20% 6.3V CERM 402 · C109 0.22uF 20% 6.3V CERM 402 · C56 0.22uF 20% 6.3V CERM 402 · C27 0.22uF 20% 6.3V CERM 402

C296 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C210 0.22uF 20% 6.3V CERM 402 · C58 0.22uF 20% 6.3V CERM 402 · C22 0.22uF 20% 6.3V CERM 402 · C20 0.22uF 20% 6.3V CERM 402 · C61 0.22uF 20% 6.3V CERM 402 · C44 0.22uF 20% 6.3V CERM 402 · C29 0.22uF 20% 6.3V CERM 402 · C24 0.22uF 20% 6.3V CERM 402

C183 0.22uF 20% 6.3V CERM 402 · C18 0.22uF 20% 6.3V CERM 402 · C49 0.22uF 20% 6.3V CERM 402 · C36 0.22uF 20% 6.3V CERM 402 · C17 0.22uF 20% 6.3V CERM 402 · C99 0.22uF 20% 6.3V CERM 402 · C396 0.22uF 20% 6.3V CERM 402 · C124 0.22uF 20% 6.3V CERM 402 · C127 0.22uF 20% 6.3V CERM 402 · C100 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 16 OF 44	

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17

R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17

R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805

C795 0.22UF 20% 6.3V CERM 402

C798 0.22UF 20% 6.3V CERM 402

C790 0.22UF 20% 6.3V CERM 402

C796 0.22UF 20% 6.3V CERM 402

C797 0.22UF 20% 6.3V CERM 402

C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN

+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

U19
TPS2211
SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15	CRITICAL	
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

+VPP_CBUS_SW 17 38

+VCC_CBUS_SW 17 38

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

C773 0.1UF 20% 10V CERM 402

C467 0.1UF 20% 10V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TPS2211_SHDN_L_PU

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
	N8	AD0	
	M7	AD1	
	L7	AD2	
	N6	AD3	
	K4	AD4	
	M6	AD5	
	L6	AD6	
	N5	AD7	
	N4	AD8	
	M2	AD9	
	M5	AD10	
	L4	AD11	
	N3	AD12	
	K5	AD13	
	L5	AD14	
	M4	AD15	
	J4	AD16	
	H1	AD17	
	H3	AD18	
	H2	AD19	
	G2	AD20	
	G4	AD21	
	F1	AD22	
	C3	AD23	
	F3	AD24	
	E2	AD25	
	F4	AD26	
	B1	AD27	
	D2	AD28	
	E4	AD29	
	D3	AD30	
	E3	AD31	
	K6	C/BE0*	
	M3	C/BE1*	
	J2	C/BE2*	
	A1	C/BE3*	
	N1	PAR	
	K1	IRDY	
CBUS_PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
CBUS_PCI_PERR_L	K3	PERR	
	J1	FRAME	
	L1	STOP	
	J3	TRDY	
	K2	DEVSEL	
CBUS_PCI_RESET_L	G3	PRST	
CBUS_PCI_REQ_L	C2	REQ	
CBUS_PCI_GNT_L	C1	GNT	
CLK33M_CBUS	G1	PCLK	
NC	M9	SPKROUT	
NC	M8	RI_OUT/PME	
CBUS_SUSPEND_PU	N10	SUSPEND	
CBUS_INT_L	K7	MFUNC0	
CBUS_MFUNC1_PD	N9	MFUNC1	
CBUS_MFUNC2_PD	L9	MFUNC2	
CBUS_MFUNC3_PD	K10	MFUNC3	
CBUS_MFUNC4_PD	M10	MFUNC4	
CBUS_MFUNC5_PD	N12	MFUNC5	
CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	
	B11	VCCCB	
	L3	VCCP	
	N13	VCCD0*	CBUS_VCCD0_L
	L12	VCCD1*	CBUS_VCCD1_L
	K9	VPPD0	CBUS_VPPD0
	M11	VPPD1	CBUS_VPPD1
	L13	CD1*/CCD1*	CBUS_DET_1_L 17 39
	B5	CD2*/CCD2*	CBUS_DET_2_L 17 39
	F12	IORD*/CAD13	CBUS_IORD_L 17
	C11	IOWR*/CAD15	CBUS_IOWR_L 17
	G10	OE*/CAD11	CBUS_OE_L 17
	H13	CE1*/CC/BE0*	CBUS_CE1_L 17
	B2	VS1*/CVS1	CBUS_VS1 17
	A9	VS2*/CVS2	CBUS_VS2 17
	D13	WE*/CGNT*	CBUS_WE_L 17
	A6	RDY/IREQ*/CINT*	CBUS_READY 17
	D8	RESET/CRST*	CBUS_RESET_L 17
	A8	REG*/CC/BE3*	CBUS_REG_L 17
	C6	BVD1/CSTSCHG/STSCHG*/RI*	CBUS_BVD1_L 17
	D6	BVD2/SPKR*/CAUDIO	CBUS_BVD2_L 17
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*	CBUS_WP_L 17
	G13	CE2/CAD10*	CBUS_CE2_L 17
	B8	INPACK/CREQ*	CBUS_INPACK_L 17
	B6	WAIT/CSERR*	CBUS_WAIT_L 17
	C7	A0/CAD26	CBUS_ADDR<0> 17
	D7	A1/CAD25	CBUS_ADDR<1> 17
	B7	A2/CAD24	CBUS_ADDR<2> 17
	D10	A3/CAD23	CBUS_ADDR<3> 17
	B12	A4/CAD22	CBUS_ADDR<4> 17
	C8	A5/CAD21	CBUS_ADDR<5> 17
	C9	A6/CAD20	CBUS_ADDR<6> 17
	A12	A7/CAD18	CBUS_ADDR<7> 17
	E11	A8/CC/BE1*	CBUS_ADDR<8> 17
	F11	A9/CAD14	CBUS_ADDR<9> 17
	G11	A10/CAD9	CBUS_ADDR<10> 17
	G12	A11/CAD12	CBUS_ADDR<11> 17
	D9	A12/CC/BE2*	CBUS_ADDR<12> 17
	E12	A13/CPAR	CBUS_ADDR<13> 17
	D12	A14/CPERR*	CBUS_ADDR<14> 17
	C10	A15/CIRDY*	CBUS_ADDR<15> 17
	B13	A16/CCLK	CBUS_ADDR_16_UF
	F10	A17/CAD16	CBUS_ADDR<17> 17
	E13	A18/RSVD	CBUS_ADDR<18> 17
	A13	A19/CBLOCK*	CBUS_ADDR<19> 17
	E10	A20/CSTOP*	CBUS_ADDR<20> 17
	D11	A21/CDEVSEL*	CBUS_ADDR<21> 17
	C12	A22/CTRDY*	CBUS_ADDR<22> 17
	A10	A23/CFRAME*	CBUS_ADDR<23> 17
	B10	A24/CAD17	CBUS_ADDR<24> 17
	B9	A25/CAD19	CBUS_ADDR<25> 17
	A4	D0/CAD27	CBUS_DATA<0> 17
	C4	D1/CAD29	CBUS_DATA<1> 17
	A3	D2/RSVD	CBUS_DATA<2> 17
	K11	D3/CAD0	CBUS_DATA<3> 17
	K12	D4/CAD1	CBUS_DATA<4> 17
	J13	D5/CAD3	CBUS_DATA<5> 17
	J10	D6/CAD5	CBUS_DATA<6> 17
	H12	D7/CAD7	CBUS_DATA<7> 17
	C5	D8/CAD28	CBUS_DATA<8> 17
	B4	D9/CAD30	CBUS_DATA<9> 17
	B3	D10/CAD31	CBUS_DATA<10> 17
	M12	D11/CAD2	CBUS_DATA<11> 17
	J11	D12/CAD4	CBUS_DATA<12> 17
	K13	D13/CAD6	CBUS_DATA<13> 17
	J12	D14/RSVD	CBUS_DATA<14> 17
	H11	D15/CAD8	CBUS_DATA<15> 17

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

R767 22 5% 1/16W MF 402

R764 47 5% 1/16W MF 402 — NO STUFF — IO_RESET_L 30 27 26 23

R766 47 5% 1/16W MF 402 — MAIN_RESET_L 39 30 26 24 20 18 17 14

RP39 10K 5% 1/32W 25V SM

CBUS_MFUNC1_PD 17
CBUS_MFUNC2_PD 17
CBUS_MFUNC3_PD 17
CBUS_MFUNC4_PD 17
CBUS_MFUNC5_PD 17
CBUS_MFUNC6_PD 17

GND

A2 A11 D1 F13 H4 K8 M13 N2

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805

C776 2.2UF 20% 10V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

		84	81		
		2	1	CBUS_DATA<3>	17
39 17	CBUS_DET_1_L	4	3	CBUS_DATA<4>	17
17	CBUS_DATA<11>	6	5	CBUS_DATA<5>	17
17	CBUS_DATA<12>	8	7	CBUS_DATA<6>	17
17	CBUS_DATA<13>	10	9		
		12	11	CBUS_DATA<7>	17
17	CBUS_DATA<14>	14	13	CBUS_CE1_L	17
17	CBUS_DATA<15>	16	15	CBUS_ADDR<10>	17
17	CBUS_CE2_L	18	17	CBUS_OE_L	17
17	CBUS_VS1	20	19		
		22	21	CBUS_ADDR<11>	17
17	CBUS_IORD_L	24	23	CBUS_ADDR<9>	17
17	CBUS_IOWR_L	26	25	CBUS_ADDR<8>	17
17	CBUS_ADDR<17>	28	27	CBUS_ADDR<13>	17
17	CBUS_ADDR<18>	30	29		
		32	31	CBUS_ADDR<14>	17
17	CBUS_ADDR<19>	34	33	CBUS_WE_L	17
17	CBUS_ADDR<20>	36	35	CBUS_READY	17
17	CBUS_ADDR<21>	38	37	+VCC_CBUS_SW	17 38
38 17	+VCC_CBUS_SW	40	39		
		42	41	+VPP_CBUS_SW	17 38
38 17	+VPP_CBUS_SW	44	43	CBUS_ADDR<16>	17
17	CBUS_ADDR<22>	46	45	CBUS_ADDR<15>	17
17	CBUS_ADDR<23>	48	47	CBUS_ADDR<12>	17
17	CBUS_ADDR<24>	50	49		
		52	51	CBUS_ADDR<7>	17
17	CBUS_ADDR<25>	54	53	CBUS_ADDR<6>	17
17	CBUS_VS2	56	55	CBUS_ADDR<5>	17
17	CBUS_RESET_L	58	57	CBUS_ADDR<4>	17
17	CBUS_WAIT_L	60	59		
		62	61	CBUS_ADDR<3>	17
17	CBUS_INPACK_L	64	63	CBUS_ADDR<2>	17
17	CBUS_REG_L	66	65	CBUS_ADDR<1>	17
17	CBUS_BVD2_L	68	67	CBUS_ADDR<0>	17
17	CBUS_BVD1_L	70	69		
		72	71	CBUS_DATA<0>	17
17	CBUS_DATA<8>	74	73	CBUS_DATA<1>	17
17	CBUS_DATA<9>	76	75	CBUS_DATA<2>	17
17	CBUS_DATA<10>	78	77	CBUS_WP_L	17
39 17	CBUS_DET_2_L	80	79		
			83 82		

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0133	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

OMIT
CRITICAL

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(1 OF 6)

AGP_AD<31> AB30 AD31
AGP_AD<30> AB27 AD30
AGP_AD<29> AA29 AD29
AGP_AD<28> AB28 AD28
AGP_AD<27> AA30 AD27
AGP_AD<26> AA27 AD26
AGP_AD<25> Y30 AD25
AGP_AD<24> AA28 AD24
AGP_AD<23> W30 AD23
AGP_AD<22> W27 AD22
AGP_AD<21> V30 AD21
AGP_AD<20> V28 AD20
AGP_AD<19> V29 AD19
AGP_AD<18> V27 AD18
AGP_AD<17> U30 AD17
AGP_AD<16> U28 AD16
AGP_AD<15> R27 AD15
AGP_AD<14> R29 AD14
AGP_AD<13> P28 AD13
AGP_AD<12> P30 AD12
AGP_AD<11> P27 AD11
AGP_AD<10> P29 AD10
AGP_AD<9> N28 AD9
AGP_AD<8> N30 AD8
AGP_AD<7> M30 AD7
AGP_AD<6> M27 AD6
AGP_AD<5> M29 AD5
AGP_AD<4> L28 AD4
AGP_AD<3> L30 AD3
AGP_AD<2> L27 AD2
AGP_AD<1> L29 AD1
AGP_AD<0> K28 AD0

AGP_CBE<3> W28 CBEB3
AGP_CBE<2> U29 CBEB2
AGP_CBE<1> R30 CBEB1
AGP_CBE<0> N27 CBEB0

CLK66M_GPU_AGP AG30 PCICLK
AGP_FRAME_L U27 FRAMEB
AGP_IRDY_L T30 IRDYB
AGP_TRDY_L T28 TRDYB
AGP_STOP_L T27 STOPB
AGP_DEVSEL_L T29 DEVSELB
AGP_PAR R28 PAR
AGP_REQ_L AF29 REQB
AGP_GNT_L AF27 GNTB
AGP_INT_L AH29 INTAB
AGP_ATI_RESET_L AH30 RSTB
AGP_WBF_L AE27 WBF

AGP_ATI_VREFG AK3 VREFG
AGP_ATI_VREF D8 VREF

C19
P2
B18
P4
A19
R3
A18
R4
D19
P1 VSS
G29
G27
B29
C26
A16
C11

AD_STB0 N29 AGP_AD_STB<0>
AD_STB1 W29 AGP_AD_STB<1>
AD_STBB0 M28 AGP_AD_STB_L<0>
AD_STBB1 Y29 AGP_AD_STB_L<1>
AGP_BUSYB AG28 AGP_BUSY_L
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU

SUS_STAT AJ28 AGP_SUS_STAT_L_PU

ST0 AF30 AGP_ST<0>
ST1 AF28 AGP_ST<1>
ST2 AE29 AGP_ST<2>

SBA7 AC28 AGP_SBA<7>
SBA6 AB29 AGP_SBA<6>
SBA5 AC27 AGP_SBA<5>
SBA4 AC30 AGP_SBA<4>
SBA3 AD27 AGP_SBA<3>
SBA2 AD30 AGP_SBA<2>
SBA1 AE28 AGP_SBA<1>
SBA0 AD29 AGP_SBA<0>
RBFB AE30 AGP_RBF_L

STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB
SB_STBS AD28 AGP_SB_STB_L
RSTB_MSK AD24 ATI_RSTB_MSK

DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU

A10
C5
A3
G4
E2
U2
V4
AB2
AC4
VSS B23
K2
A23
K1
B22
L2
A22
L1

D+ AC10 GPU_THERM_DP
D- AC11 GPU_THERM_DM
+GPU_MEM

TEST_YCLK E8
TEST_MLCK J6 (PULL-UP to GPU_MEM_IO)
MEMTEST C8 ATI_MEMTEST
PLLTEST AC22 NC

MEMVMODE0 B7
MEMVMODE1 B6

38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1.5V_AGP
38 21 19 18 12 +1.8V_GPU

R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402

C62 0.1uF 20% 16V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)

MAIN_RESET_L IS TOGGLED FOR SLEEP
24 20 17 14 39 30 26 MAIN_RESET_L
R54 10K 5% 1/16W MF 402
R53 47 5% 1/16W MF 402

21 19 18 12 38 +3V_GPU
R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
38 21 18 +GPU_MEM
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 16V CERM 402
C37 10uF 20% 6.3V CERM 805
PLACE VERF_VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

38 21 20 19 +1.8V_GPU
ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0
ATI_MEMVMODE1
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

R118 45.3 1% 1/16W MF 402

OMIT
U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(6 OF 6)

M2
P3
A21
B19
M15
N15
P15
R15
VSS T15
T12
T13
T14
W16
V16
U16
T16
R16
R17
R18
R19

U6
AE15
VDDCI F18
P25

39 38 19 GPU_VCORE
L2
60-OHM-EMI
SM
GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(2 OF 6)

B26 A17
A26 B16
B25 A16
A25 B14
C22 A14
D21 B13
C21 A13
D20 D13
C20 C13
D22 D12
C23 C12
D23 D10
A27 C10
B27 D9

H2 C9
H1 B12
J2 A12
J1 B11
K4 A11
K3 B9
L4 A9
M3 B8
L3 VSS A8
M4 VSS C7
N2 D7
N1 C6
N4 D6
N3 C4
G30 D4
G28 C3
B30 D3
D26 A5
D16 B5
B15 A4
D11 B4
B10 A2
D5 B2
B3 A1
G3 B1
E1 E4
U1 E3
V3 F3
AB1 F4
AC3 H3
J30 H4
J29 J3
H30 J4
H29 C1
F30 C2
F29 D1
E30 D2
E29 F1
J28 F2
J27 G1
H28 G2
H27 R1
F28 R2
F27 T1
E28 T2
E27 V1
D30 V2
D29 VSS W1 VSS
C30 W2
C29 T3
A30 T4
A29 U3
A28 U4
B28 W3
D28 W4
C28 Y3
D27 Y4
C27 Y1
D25 Y2
C25 AA1
D24 AA2
C24 AC1
D18 AC2
C18 AD1
AD2
D17 AA3
C17 AA4
D15 AB3
C15 AB4
D14 AD3
C14 AD4
B17 AE3
AE4

OMIT

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4
FERR-EMI-100-OHM
SM
38 +3V_ATI_OSC_SLEEP
C77 0.1uF 20% 16V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF
R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2
27.0000M
OSC SM-1
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 5% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
R189 287 1% 1/16W MF 402
ATI_CLK27M_IN 19
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3
FERR-EMI-100-OHM
SM
38 +3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 16V CERM 402
NO STUFF
R173 0 5% 1/16W MF 402
GPU_SS
R181 0 5% 1/16W MF 402
GPU_SS 7 CRITICAL
VDD
U47
CY25811
SOI
XIN/CLKIN
XOUT
SSCLK
NC
FRSEL
S1
S0
VSS
18 ATI_CLK27M_OSC_SS
ATI_SSCLK_UF
GPU_SS
R201 33 5% 1/16W MF 402
ATI_SSCLK_IN 19
CY25811_S1
CY25811_S0
NO STUFF
R37 0 5% 1/16W MF 402
NO STUFF
R38 0 5% 1/16W MF 402

M10 AGP INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

GPU_DVOD<0>	AJ5	ZV_LCDDATA0
GPU_DVOD<1>	AK5	ZV_LCDDATA1
GPU_DVOD<2>	AG6	ZV_LCDDATA2
GPU_DVOD<3>	AH6	ZV_LCDDATA3
GPU_DVOD<4>	AJ6	ZV_LCDDATA4
GPU_DVOD<5>	AK6	ZV_LCDDATA5
GPU_DVOD<6>	AG7	ZV_LCDDATA6
GPU_DVOD<7>	AH7	ZV_LCDDATA7
GPU_DVOD<8>	AJ7	ZV_LCDDATA8
GPU_DVOD<9>	AK7	ZV_LCDDATA9
GPU_DVOD<10>	AG8	ZV_LCDDATA10
GPU_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
ZV_LCDDATA20_PU	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
GPU_DVO_VSYNC	AJ4	ZV_LCDCNTL0
GPU_DVO_HSYNC	AK4	ZV_LCDCNTL1
GPU_DVOD_DE	AH5	ZV_LCDCNTL2
GPU_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN (NO ICT TEST)	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN (NO ICT TEST)	AF3	GPIO9
ATI_GPIO10_SPN (NO ICT TEST)	AG2	GPIO10
ATI_GPIO11_SPN (NO ICT TEST)	AF2	GPIO11
ATI_GPIO12_SPN (NO ICT TEST)	AG1	GPIO12
ATI_GPIO13_SPN (NO ICT TEST)	AF1	GPIO13
HPD_PWR_SNS_EN	AE2	GPIO14
GPU_VCORE_CNTL_L	AE1	GPIO15
ATI_SSCLK_IN	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS
	A20	VSS
	B21	VSS
SSOUT	AJ25	NC

EXT_TMDS R228 10K 5% 1/16W MF 402 — +1.8V_GPU
INT_TMDS R234 10K 5% 1/16W MF 402 — +3V_GPU

R221 1K 5% 1/16W MF 402 — R223 10K 5% 1/16W MF 402 (NO STUFF) — +3V_GPU

R229 1K 5% 1/16W MF 402 — ATI_TESTEN

ROMCSB — NC
R — GPU_R
G — GPU_G
B — GPU_B
VSYNC — ATI_VSYNC
V2SYNC — NC
HSYNC — ATI_HSYNC
H2SYNC — NC
RSET — ATI_RSET
R2SET — ATI_R2SET
Y_G — GPU_Y
C_R — GPU_C
COMP_B — GPU_COMP
DIGON — FP_PWR_EN
BLON — INV_ON_PWM
HPD1 — GPU_HPD
AUXWIN — GPU_AUXWIN
DDC1DATA — GPU_DVI_DDC_DATA
DDC1CLK — GPU_DVI_DDC_CLK
DDC2DATA — LVDS_DDC_DATA
DDC2CLK — LVDS_DDC_CLK
DDC3DATA — SI_DDC_DATA
DDC3CLK — SI_DDC_CLK
TXOUT_U0N — LVDS_U0N
TXOUT_U0P — LVDS_U0P
TXOUT_U1N — LVDS_U1N
TXOUT_U1P — LVDS_U1P
TXOUT_U2N — LVDS_U2N
TXOUT_U2P — LVDS_U2P
TXOUT_U3N — LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P — LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN — CLKLVDS_UN
TXCLK_UP — CLKLVDS_UP
TXOUT_L0N — LVDS_L0N
TXOUT_L0P — LVDS_L0P
TXOUT_L1N — LVDS_L1N
TXOUT_L1P — LVDS_L1P
TXOUT_L2N — LVDS_L2N
TXOUT_L2P — LVDS_L2P
TXOUT_L3N — LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P — LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN — CLKLVDS_LN
TXCLK_LP — CLKLVDS_LP

R240 75 1% 1/16W MF 402 — R246 75 1% 1/16W MF 402 — R249 75 1% 1/16W MF 402

R256 715 1% 1/16W MF 402 — R257 499 1% 1/16W MF 402

R245 75 1% 1/16W MF 402 — R248 75 1% 1/16W MF 402 — R254 75 1% 1/16W MF 402

R711 10K 5% 1/16W MF 402 — +3V_GPU

R247 10K 5% 1/16W MF 402 — R253 10K 5% 1/16W MF 402

Q77 SI3446DV TSOP

L24 FERR-220-OHM 0805 (500mA)

GPU_CORE_OK — C166 1000pF 10% 25V X7R 402

+1.5V_GPU_VDD15 — C222 C256 C299 C305 C328 0.01uF 20% 16V CERM 402 — C328 10uF 20% 6.3V CERM 805

+GPU_VDD15_UF — C232 C269 C300 C306 0.01uF 20% 16V CERM 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

GPU_VCORE — C167 10uF 20% 6.3V CERM 805; C219 10uF 20% 6.3V CERM 805; C252 C270 C301 C307 C329 C332 0.22uF 20% 6.3V CERM 402

C186 C220 C253 C271 C302 C311 C330 C333 0.22uF 20% 6.3V CERM 402

C187 C221 C254 C282 C303 C326 C331 C338 0.22uF 20% 6.3V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

	F12	
	L6	
	T6	
	AB6	
VDD15	F17	
	G25	
	R25	
	AB25	
	AJ3	
OMIT	AF25	
	AG4	
	AH4	
	AF5	
	F6	
	G6	
	H6	
	P6	
	AD26	
	V6	
	W6	
	AC6	
	AD6	
	AE6	
	F7	
	F10	
	AE10	
	F11	
	AE11	
VDDC	F13	
	F14	
	AE14	
	AF14	
	W26	
	AF15	
	AE17	
	AC25	
	AE18	
	F23	
	F24	
	AE24	
	F25	
	M25	
	N25	
	W25	
	V25	
VSS	G7	
	G8	
	G9	
	G10	
	G11	
	G12	
	G13	
	G14	
	G15	
	G16	
	G17	
	G18	
	G19	
	G20	
	G21	
	G22	
	G23	
	G24	
	H7	
	H8	
	H23	
	H24	
	J7	
	J24	
	K7	
	K24	
	L7	
	L24	
	M7	
	M24	
	N7	
	N24	
	P7	
	P24	
	R7	
	R24	
	T7	
	T24	
	U7	
	U24	
	V7	
	V24	
	W7	
	W24	
	Y7	
	Y24	
	AA7	
	AA24	
	AB7	
	AB24	
	AC7	
	AC8	
	AC23	
	AC24	
	AD7	
	AD8	
	AD9	
	AD10	
	AD11	
	AD12	
	AD13	
	AD14	
	AD15	
	AD16	
	AD17	
	AD18	
	AD19	
	AD20	
	AD21	
	AD22	
	AD23	

M10 Power Shut down Sequencing

XW21 SM — DP6 BAS16TW SOT-363 — XW24 SM — +2_5V_SLEEP
+1.8V_ATI_PVDD — +2_5V_SLEEP_NECK
+1.8V_PVDD_NECK

XW20 SM — DP6 BAS16TW SOT-363 — +1.5V_AGP_NECK — XW23 SM — +1.5V_AGP
GPU_VCORE_NECK

XW22 SM — DP6 BAS16TW SOT-363
+GPU_VDD15_UF — +GPU_VDD15_NECK

R258 R260 R262 R265 R269 R271 R273 10K 5% 1/16W MF 402 — +3V_GPU — NO STUFF

R259 R261 R263 R266 R270 R272 R274 10K 5% 1/16W MF 402 — NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

+PBUS

R389 1M 5% 1/16W MF 402 — 1778_VCC
R430 1 5% 1/16W MF 603 — 1778_VIN
R339 576K 1% 1/16W MF 402

C762 C766 4.7UF 20% 25V CERM 1206

Q51 SI7860DP SO-8-PWRPK CRITICAL — GPU_VCORE_SW

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

L30 2.1UH-11A SM — CRITICAL

D24 SMB B340LB

Q48 SI7892DP SO-8-PWRPK — CRITICAL

R352 4.99K 1% 1/16W MF 402 — 1778_VFB
R451 18.2K 1% 1/16W MF 402 — GPU_PWRMSR
R351 20K 1% 1/16W MF 402 — HIGH_VCORE_DIV
R804 1.82K 1% 1/16W MF 402 — HIGH_VCORE
R307 100K 5% 1/16W MF 402 — GPU_VCORE_CNTL
R410 10K 5% 1/16W MF 402 — GPU_VCORE_CNTL_L — VCORE_CNTL_RC
R515 0.1UF 20% 10V CERM 402 — GPU_PWRMSR

C708 22uF 20% 10V CERM 1210
C721 C720 330UF 20% 6.3V POLY SMD
C719 330UF 20% 6.3V POLY SMD
C902 0.1UF 20% 10V CERM 402

Q80 2N7002DW SOT-363 — Q80 2N7002DW SOT-363

NO STUFF: R388 0 5% 1/16W MF 402; R341 63.4K 1% 1/16W MF 402; C473 4.7UF 20% 10V CERM 1206 1778_GND

C494 0.1UF 20% 25V CERM 603

R236 100K 5% 1/16W MF 402

U16 LTC1778 SSOP CRITICAL
RUN/SS, ITH, VRNG, FCB, PGOOD, SGND, PGND, EXT, INTVCC, VIN, BOOST, TG, SW, BG, VFB, ION

C514 0.1UF 20% 25V CERM 603 — 1778_BST_RC

D5 MBR0540 SM — R416 2.2 5% 1/16W MF 603 — 1778_BST_RC

NO STUFF: C882 0.0022UF 10% 50V CERM 402

OMIT: XW2 SM

R340 20K 1% 1/16W MF 402 — 1778_ITH_RC
C448 470PF 10% 50V CERM 402
C451 220PF 5% 25V CERM 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C483 0.1UF 20% 10V CERM 402

R390 0 5% 1/16W MF 402 — DCDC_EN

R306 100K 5% 1/16W MF 402 — R316 100K 5% 1/16W MF 402 — DP1 BAS16TW SOT-363 — 1778_SHDN_L_D3COLD

R294 10K 5% 1/16W MF 402 — +1.5V_AGP — GPU_VCORE_PWR_SEQ
GPU_VCORE_SEQ_L — Q6 2N3904 SM
GPU_VCORE_SEQ — Q5 2N3904 SM
R203 33K 5% 1/16W MF 402

DP1 BAS16TW SOT-363 — SLEEP_L_LS5
DP1 BAS16TW SOT-363
DP1 BAS16TW SOT-363

+5V_MAIN

M10 CORE PWR/LVDS/TMDS

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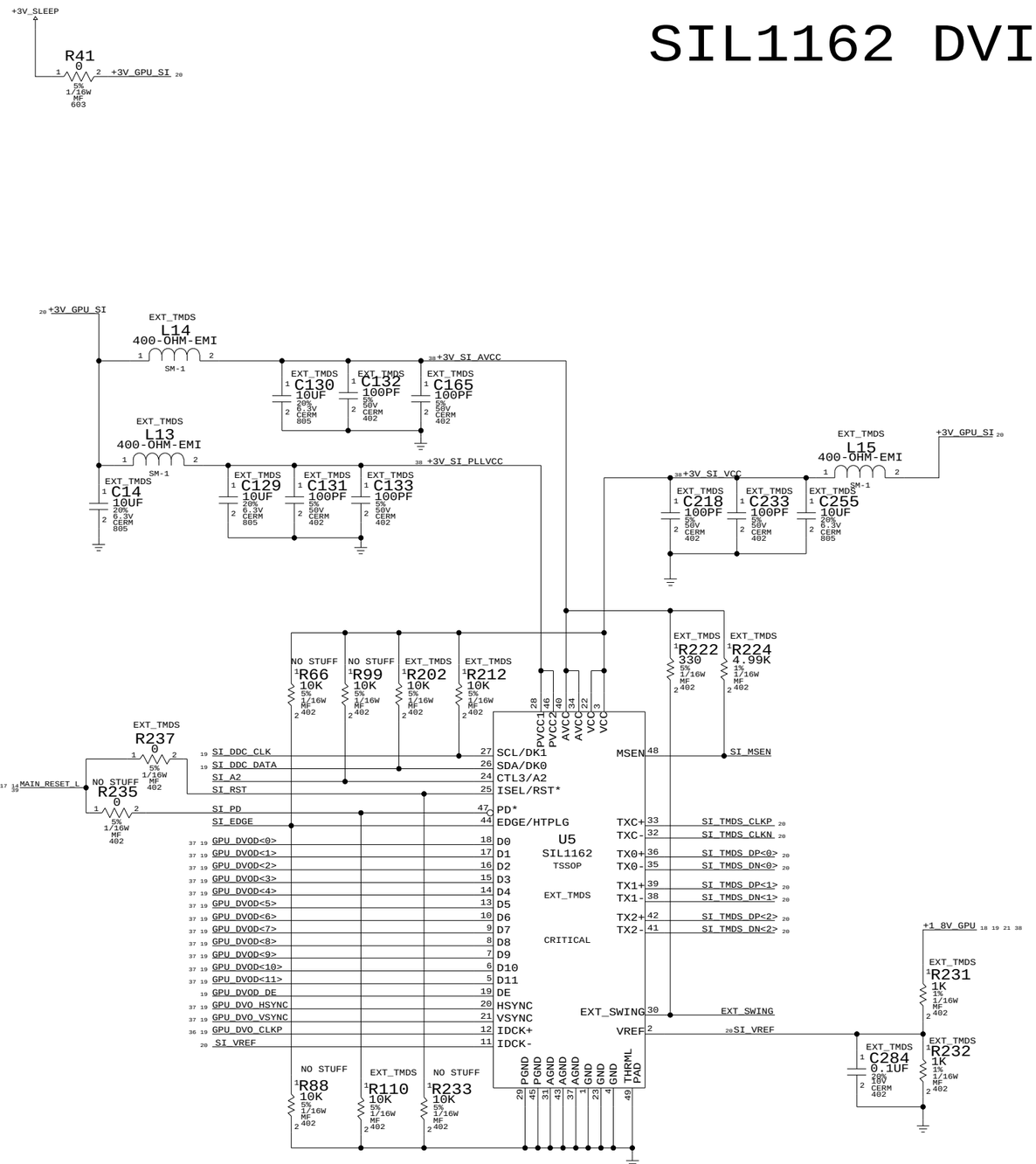
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B

SCALE	SHT
NONE	20 OF 44

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

GPU PLL - 1.8V

U55 MM1571J (100mA MAX) SOT-25A CRITICAL
(Total PVDD = 66mA)
+2_5V_GPU → VIN; +1_8V_ATI_PVDD ← VOUT
GPU_CORE_OK → CONT; ATI_PVDD_BYP ← NOISE; GND
C889 1UF 10% 6.3V CERM 603
C379 0.01uF 20% 16V CERM 402
C380 10uF 20% 6.3V CERM 805

L65 FERR-220-OHM 0402: +1_8V_ATI_PVDD → +1_8V_GPU_PLL
C438 10uF 20% 6.3V CERM 805
C865 0.1uF 20% 10V CERM 402
C716 0.01uF 20% 16V CERM 402 (21mA)

L58 FERR-220-OHM 0402: +2_5V_GPU → +2_5V_GPU_A2VDD (140mA)
C360 10uF 20% 6.3V CERM 805
C364 0.01uF 20% 16V CERM 402
C374 0.01uF 20% 16V CERM 402

L66 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_AVDD
C415 10uF 20% 6.3V CERM 805
C437 0.01uF 20% 16V CERM 402
C870 0.01uF 20% 16V CERM 402
(AVDD+VDDDI=75mA)

L55 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_AVDDQ (2mA)
C339 10uF 20% 6.3V CERM 805
C363 0.01uF 20% 16V CERM 402

L56 FERR-220-OHM 0402: +1_8V_GPU → +1_8V_GPU_VDDDI (AVDD+VDDDI=75mA)
C358 10uF 20% 6.3V CERM 805
C361 0.01uF 20% 16V CERM 402
C372 0.01uF 20% 16V CERM 402

L57 FERR-220-OHM 0402: +GPU_MEM → +GPU_MCLK
C359 10uF 20% 6.3V CERM 805
C362 0.01uF 20% 16V CERM 402
C373 0.01uF 20% 16V CERM 402

+1_5V_SLEEP → R722 0 5% 1/10W FF 805 → +1_5V_AGP
1.5V

+1_8V_SLEEP → R284 0 5% 1/10W FF 805 → +1_8V_GPU
1.8V

+1_8V_SLEEP, +2_5V_SLEEP → ATI_MEMIO_LO R729 0 5% 1/4W FF 1210; ATI_MEMIO_HI R728 0 5% 1/4W FF 1210 → +GPU_MEM
1.8V 2.5V

+2_5V_SLEEP → R721 0 5% 1/10W FF 805 → +2_5V_GPU
2.5V

+3V_SLEEP → R299 0 5% 1/10W FF 805 → +3V_GPU
3.3V

AGP 4X I/O - 1.5V

+1_5V_AGP
L59 FERR-10-OHM-500MA SM: +1_5V_AGP_GPU (20mA)
C381 0.1uF 20% 10V CERM 402
C420 0.1uF 20% 10V CERM 402
C446 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C871 10uF 20% 6.3V CERM 805
C382 0.01uF 20% 16V CERM 402
C421 0.01uF 20% 16V CERM 402
C447 0.01uF 20% 16V CERM 402
C671 0.01uF 20% 16V CERM 402

MEMORY CORE - 2.5V

+GPU_MEM
L63 FERR-220-OHM 0805: +GPU_MEMCORE (1800mA)
C383 0.1uF 20% 10V CERM 402
C425 0.1uF 20% 10V CERM 402
C866 0.1uF 20% 10V CERM 402
C672 0.1uF 20% 10V CERM 402
C715 10uF 20% 6.3V CERM 805
C408 0.01uF 20% 16V CERM 402
C426 0.01uF 20% 16V CERM 402
C450 0.01uF 20% 16V CERM 402
C701 0.01uF 20% 16V CERM 402

LVDS PLL - 1.8V

+1_8V_ATI_PVDD
L61 FERR-220-OHM 0402: +1_8V_GPU_PNLPLL (40mA)
C409 10uF 20% 6.3V CERM 805
C428 0.01uF 20% 16V CERM 402
C867 0.01uF 20% 16V CERM 402
EXT_TMDS R279 0 5% 1/16W MF 603 → +1_8V_GPU_TP_PLL
C877 10uF 20% 6.3V CERM 805
C878 0.01uF 20% 16V CERM 402

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD
L62 FERR-220-OHM 0402: +1_8V_GPU_MEMPLL
C411 10uF 20% 6.3V CERM 805
C429 0.01uF 20% 16V CERM 402

LVDS - 2.5V

+2_5V_GPU
L64 FERR-10-OHM-500MA SM: +2_5V_GPU_PNLTO (350mA)
C412 10uF 20% 6.3V CERM 805
C434 0.01uF 20% 16V CERM 402
C868 0.01uF 20% 16V CERM 402

LVDS/TMDS - 1.8V

+1_8V_GPU
L60 FERR-220-OHM 0402: +1_8V_GPU_PNLTO (180mA)
C413 10uF 20% 6.3V CERM 805
C435 0.1uF 20% 10V CERM 402
C864 0.1uF 20% 10V CERM 402
C704 0.1uF 20% 10V CERM 402
C414 0.1uF 20% 10V CERM 402
C436 0.01uF 20% 16V CERM 402
C869 0.01uF 20% 16V CERM 402

GPU I/O

AK29 PVDD; AF23 AVDD0; AF24 AVDD1
AE21 A2VDD0; AF21 A2VDD1; AJ23 A2VDDQ
AH23 VDD1DI; AF20 VDD2DI
F19 VDDRH0; N6 VDDRH1
K25, L25, T25, Y28, K27, AA25, K26, L26, M26, N26, P26, R26, T26, U26, V26, Y26, AA26, AB26, AC26 VDDP
ES, E6, E12, E13, E18 VDDM, E19, E20, E26, F26
E7, H26, E9, E10, E11, E14, E15, E16 VDDR1, E17, E21, E22, E23, E24, E25
AK21 LPVDD; AK11 TPVDD; A7 MPVDD
AE16 LVDDR_18; AF16 LVDDR_18; AG16 LVDDR_25; AF17 LVDDR_25
AG12 TXVDDR0; AG13 TXVDDR1; AG14 TXVDDR2; AG15 TXVDDR3

OMIT
U44 RAGE_MOBILITY M10-CSP64 64MB BGA (4 OF 6)

PVSS AK30; AVSSQ AF22; A2VSSQ AJ22; AVSSN0 AE22; AVSSN1 AE23; A2VSSN0 AE19; A2VSSN1 AE20; VSS1DI AG23; VSS2DI AF19; VSSRH0 F20; VSSRH1 M6
F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5, W5, Y5, AA5, AB5, AC5, AD5, G26, K6, R6, Y6, AA6, F8, F9, F15, F16, F21, F22, H25, J25, J26 VDDR1
AF6, AE7, AF7, AE8, AF8, AE9, AF9, AF10, AD25, AE25, AE26, AF26 VDDR3
LPVSS AJ21; TPVSS AJ11; MPVSS A6
LVSSR0 AH16; LVSSR1 AG17; LVSSR2 AH17; LVSSR3 AF18
DVOVMODE AH12; TXVSSR1 AH13; TXVSSR2 AH14; TXVSSR3 AH15

MEMORY I/O

U54 INT_TMDS CRITICAL MM1571J SOT-25A
+2_5V_GPU → VIN; +1_8V_ATI_TPVDD ← VOUT
INT_TMDS GPU_CORE_OK → CONT; ATI_TPVDD_BYP ← NOISE; GND
C879 1UF 10% 6.3V CERM 603
C880 0.01uF 10% 16V CERM 402
L69 FERR-220-OHM 0402: +1_8V_GPU_TP_PLL
C881 10UF 20% 6.3V CERM 805

+GPU_MEM
L67 FERR-220-OHM 0805
(1200mA) GPU_MEM_IO_FLT
C872 10uF 20% 6.3V CERM 805
C875 0.1uF 20% 10V CERM 402
C850 0.1uF 20% 10V CERM 402
C855 0.1uF 20% 10V CERM 402
C860 0.1uF 20% 10V CERM 402
C873 0.1uF 20% 10V CERM 402
C876 0.1uF 20% 10V CERM 402
C851 0.1uF 20% 10V CERM 402
C856 0.1uF 20% 10V CERM 402
C861 0.1uF 20% 10V CERM 402
C874 0.1uF 20% 10V CERM 402
C847 0.1uF 20% 10V CERM 402
C852 0.1uF 20% 10V CERM 402
C857 0.1uF 20% 10V CERM 402
C862 0.01uF 20% 16V CERM 402

EXT_TMDS L16 FERR-10-OHM-500MA SM: +1_8V_GPU → +1_8V_DVO_F
C304 10uF 20% 6.3V CERM 805
C327 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402
INT_TMDS R268 0 5% 1/16W MF 603

L68 FERR-10-OHM-500MA SM: +3V_GPU → +3V_GPU_FLT
C722 10uF 20% 6.3V CERM 805
C848 0.1uF 20% 10V CERM 402
C853 0.1uF 20% 10V CERM 402
C858 0.1uF 20% 10V CERM 402
C863 0.1uF 20% 10V CERM 402
C725 0.1uF 20% 10V CERM 402
C849 0.1uF 20% 10V CERM 402
C854 0.1uF 20% 10V CERM 402
C859 0.1uF 20% 10V CERM 402

EXT_TMDS R255 0 5% 1/16W MF 402 → +1_8V_GPU
ATI_DVODMODE → INT_TMDS R251 0 5% 1/16W MF 402

3.3V IO SUPPLY

(Max Current varies, depends on usage)

M10 SHUT DOWN POWER SEQUENCING

+2_5V_SLEEP → OMIT XW27 SM → +2_5V_SLEEP_NECK2 → DP7 BAS16TW SOT-363 → +3V_SLEEP_NECK → OMIT XW30 SM → +3V_SLEEP
+1_8V_SLEEP → OMIT XW28 SM → +1_8V_SLEEP_NECK → DP7 BAS16TW SOT-363
+1_5V_SLEEP → OMIT XW29 SM → +1_5V_SLEEP_NECK → DP7 BAS16TW SOT-363

M10 POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 74AHC1G32 SM — ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
U57 74AHC1G32 SM — ATI_VSYNC → R714 33 5% 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 MBR0530 SM — DDC_CLK_ISO

J14 QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DN<1>	9	2	TMDS_CONN_DP<2>
TMDS_CONN_DP<0>	18	10	TMDS_CONN_DP<1>
	19	3	
(TMDS_DN<5>)	NC 20	4 NC	(TMDS_DN<4>)
	NC 12	NC (TMDS_DN<3>)	
(TMDS_DP<5>)	NC 21	5 NC	(TMDS_DP<4>)
	NC 13	NC (TMDS_DP<3>)	
	22	6	DVI_DDC_CLK_UF
	14	7	(+5V_DDC_SLEEP)
TMDS_CONN_CLKP	23	8	DVI_DDC_DATA_UF
TMDS_CONN_CLKN	24	16	VGA_VSYNC
		C1	DVI_HPD_UF
VGA_B	C3	C1	VGA_R
VGA_HSYNC	C4	C2	VGA_G
	34	32	
		35	

R661 4.7K 5% 1/16W MF 402 — R655 4.7K 5% 1/16W MF 402
R670 100 5% 1/16W MF 402 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD → GPU_HPD
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100pF 5% 50V CERM 402
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND1 CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, +5V_sw will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC clk. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF → DVI_TURN_ON → DVI_TRUN_ON_ILIM
R690 680 5% 1/16W MF 402
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q42 2N3904 SM — SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
+5V_DDC_SLEEP

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF
U46 LMC7211 SM CRITICAL — HPD_PWR_SW
R663 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402
+PBUS
Q45 TP0610 SM
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_ENABLE
COMP_DISABLE
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM — HPD_ON_RC
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
Q41 2N7002DW SOT-363
R213 100K 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 90-OHM-200MA SM — TMDS_DN<0> → TMDS_CONN_DN<0>; TMDS_DP<0> → TMDS_CONN_DP<0>
L21 165-OHM SM — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L73 90-OHM-200MA SM — TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
L74 90-OHM-200MA SM — TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402 — LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402 — LVDS_DDC_DATA
C449 0.001uF 20% 50V CERM 402 — NO STUFF
C452 0.001uF 20% 50V CERM 402
C416 0.001uF 20% 50V CERM 402
CHGND4

J6 G-501973 F-RT-SM — +3V_LCD (LVDS DDC POWER)

LVDS_L0N	8	7	LVDS_L0P
LVDS_L1N	11	10	LVDS_L1P
LVDS_L2N	14	13	LVDS_L2P
CLKLVDS_LN	17	16	CLKLVDS_LP
LVDS_U0N	20	19	LVDS_U0P
LVDS_U1N	23	22	LVDS_U1P
LVDS_U2N	26	25	LVDS_U2P
CLKLVDS_UN	29	28	CLKLVDS_UP

C500 0.001uF 20% 50V CERM 402

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_DIGON_L, LCD_PWREN_L
Q11 SI3443DV TSOP
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM — FP_PWR_EN

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
L32 400-OHM-EMI SM-1 — +5V_INV_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN_1
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
Q7 FDG6324L SC70-6 — FP_PWR_EN
C749 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C739 0.001UF 20% 50V CERM 402
+3V_PMU
C552 0.1UF 20% 10V CERM 402
74LVC32 TSSOP
U24 32 — INV_ON_PWM → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND2
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01UF 20% 50V CERM 603

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → TV_GND1
L26 FERR-10-OHM-500MA SM
C712 0.01UF 20% 50V CERM 603

GPU_Y	L25 3.3UH 0603	C702 560PF 10% 50V CERM 402	C707 560PF 10% 50V CERM 402
GPU_C	L29 3.3UH 0603	C718 560PF 10% 50V CERM 402	C724 560PF 10% 50V CERM 402
GPU_COMP	L27 3.3UH 0603	C714 560PF 10% 50V CERM 402	C713 560PF 10% 50V CERM 402

CRITICAL J15 MINIDIN RT-TH MH1177 — TV_C, TV_Y, TV_COMP
CHGND1

XW13 SM — GPU_TV_GND2 → TV_GND2
L28 FERR-10-OHM-500MA SM
C717 0.01UF 20% 50V CERM 603

Place GND shorts at graphics controller

VIDEO CONNECTORS

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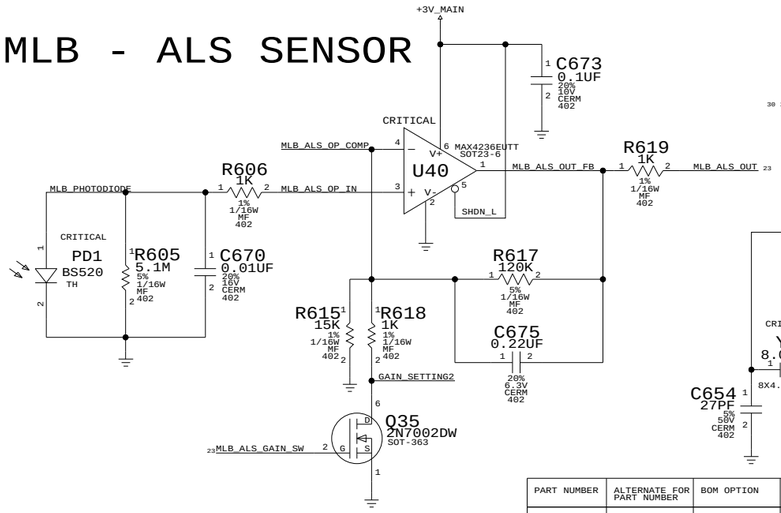
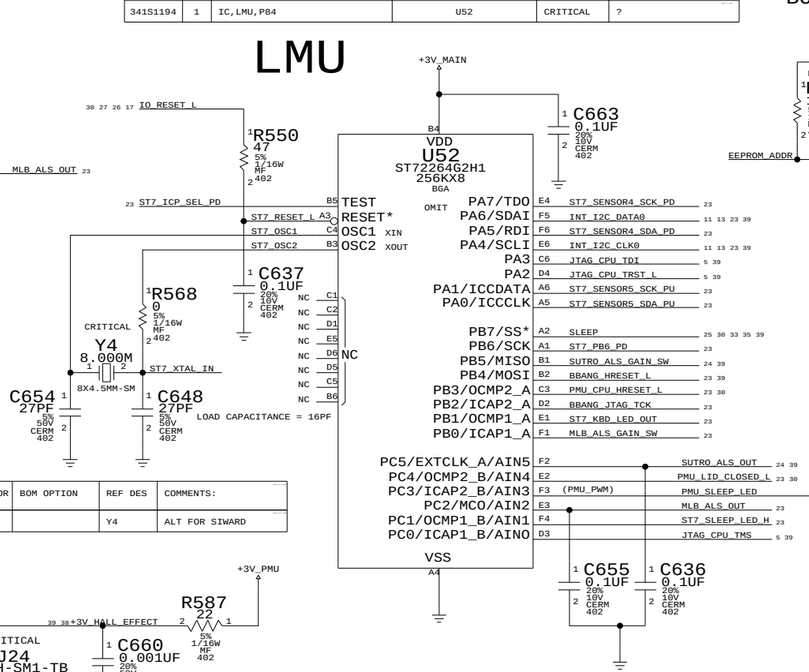
APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6531 | REV. B
SCALE NONE | SHT 22 OF 44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR

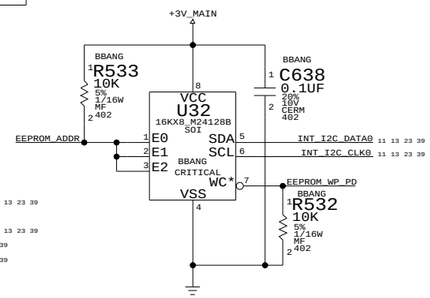


LMU

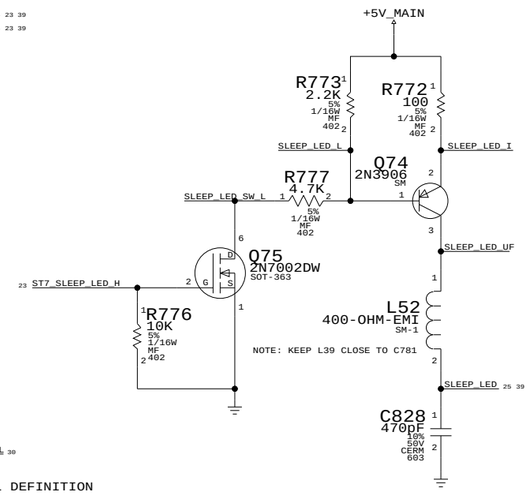


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

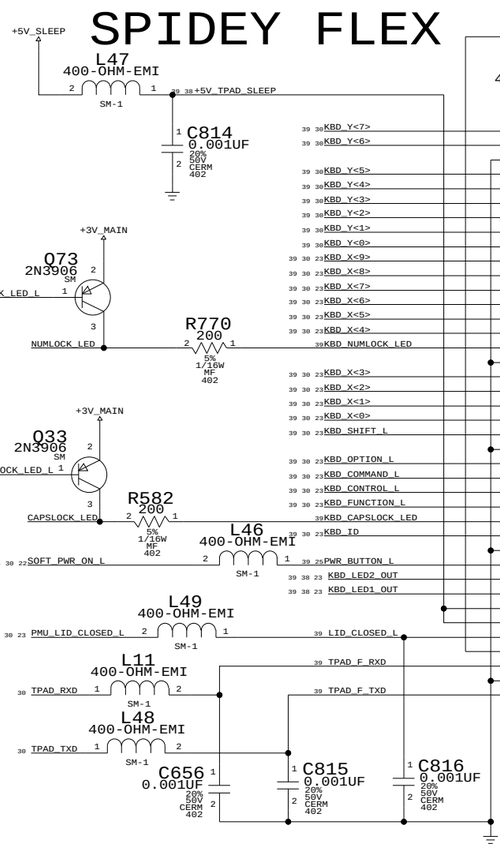
BOOT BANGER E2PROM



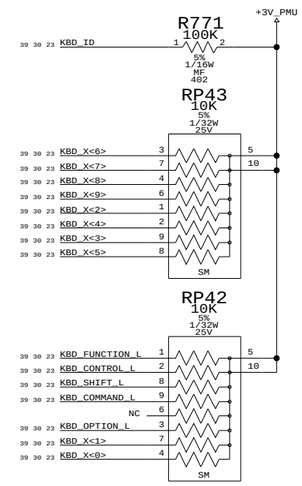
SLEEP LED



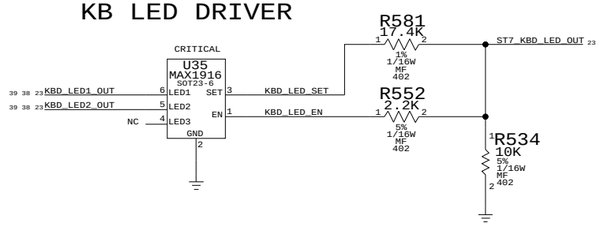
SPIDEY FLEX

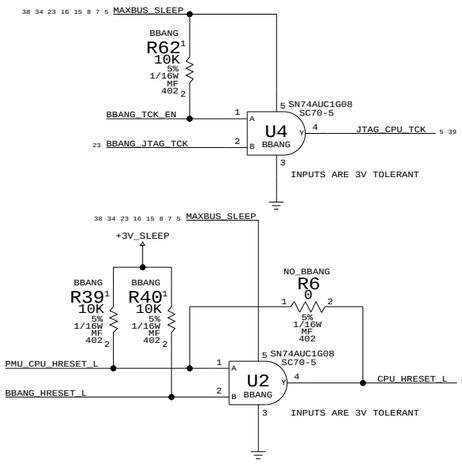


KEYBOARD PULLUPS



KB LED DRIVER

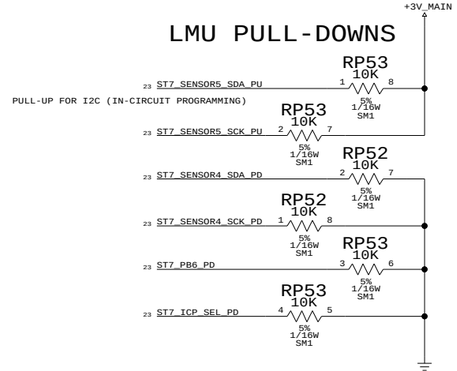




BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

APPLE COMPUTER INC.

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D	051-6531	B
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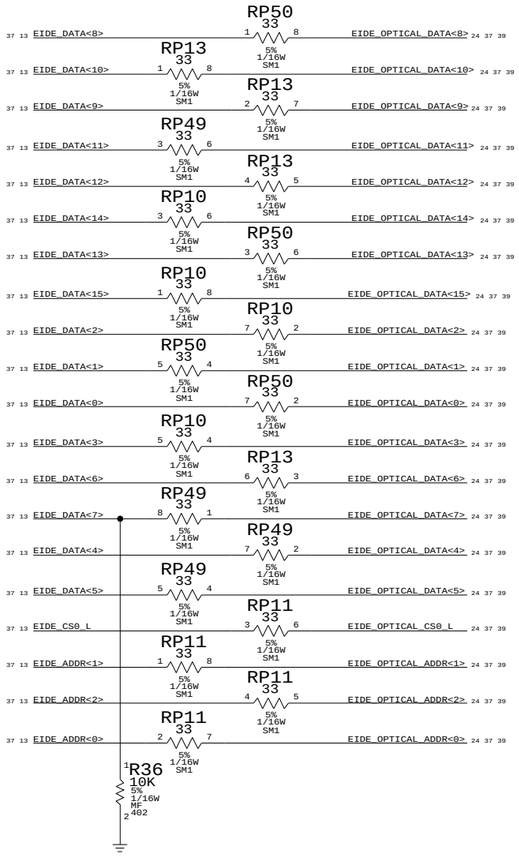
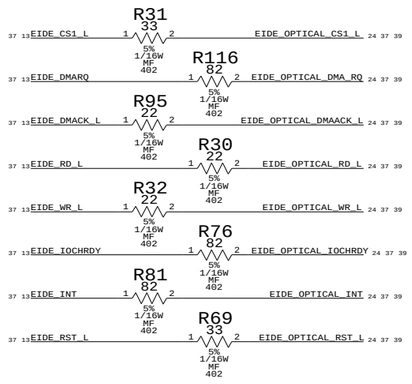
HARD DRIVE INTERFACE (UATA100)

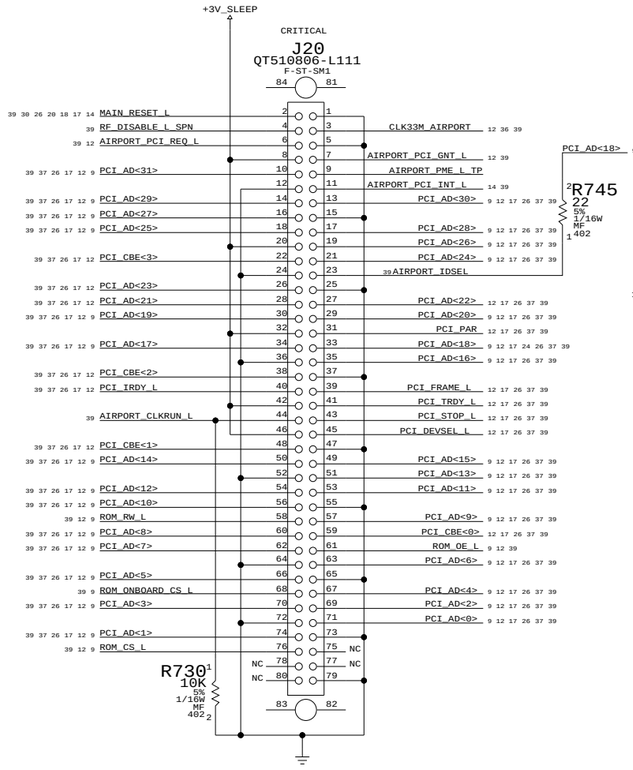
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

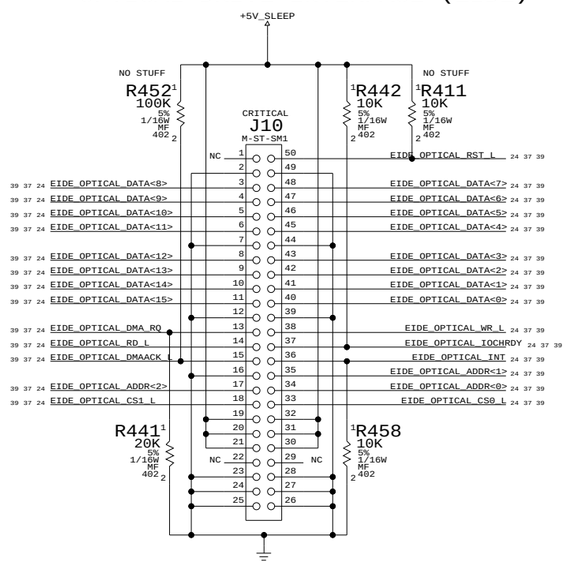




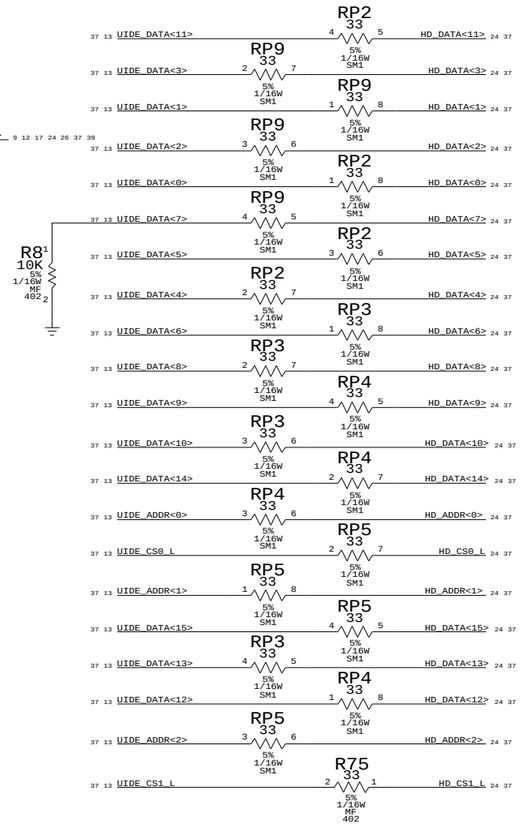
WIRELESS INTERFACE



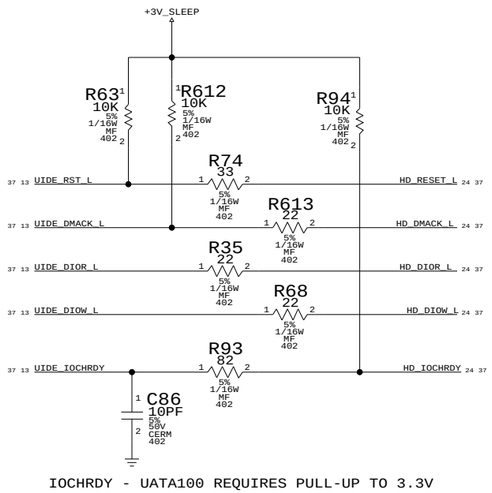
OPTICAL DRIVE INTERFACE (EIDE)



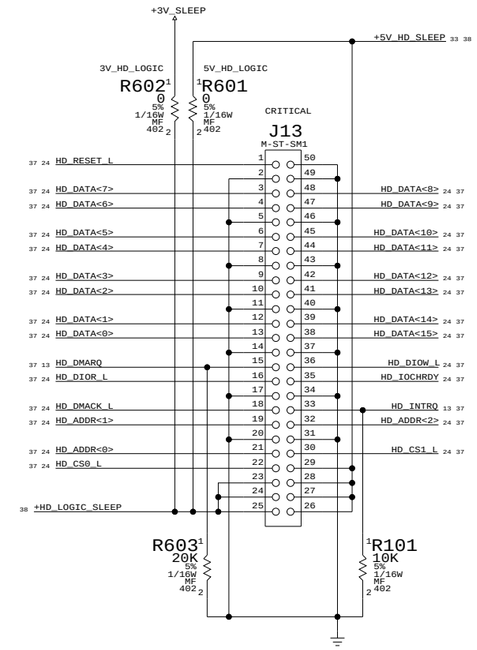
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

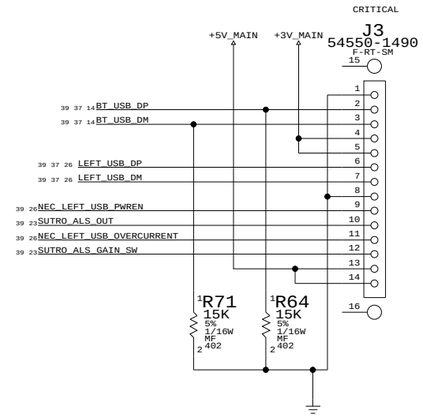


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402 — SND_SYNC → SND_SYNC_F
L80 FERR-220-OHM 0402 — SND_CLKOUT → SND_CLKOUT_F
L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
L82 FERR-220-OHM 0402 — SND_TO_AUDIO → SND_TO_AUDIO_F
L76 FERR-220-OHM 0402 — SND_AMP_MUTE → SND_AMP_MUTE_F
L78 FERR-220-OHM 0402 — SND_HW_RESET_L → SND_HW_RESET_L_F
L79 FERR-220-OHM 0402 — SND_SCLK → SND_SCLK_F

C895 NO STUFF 0.01UF 20% 16V CERM 402
C899 NO STUFF 0.01UF 20% 16V CERM 402
C896 NO STUFF 0.01UF 20% 16V CERM 402
C897 NO STUFF 0.01UF 20% 16V CERM 402
C898 NO STUFF 0.01UF 20% 16V CERM 402
C900 NO STUFF 0.01UF 20% 16V CERM 402
C901 NO STUFF 0.01UF 20% 16V CERM 402

+3V_MAIN
+5V_MAIN

J12 CRITICAL
QT510306-L111
F-ST-SM1

INT_AUDIO_TO_SND_F → SND_TO_AUDIO_F
SND_HP_SENSE_L
INT_I2C_CLK2 → SND_LIN_SENSE_L
SND_SCLK_F → SND_AMP_MUTE_F
SND_CLKOUT_F → SLEEP
SND_SYNC_F
INT_I2C_DATA2 → SND_HW_RESET_L_F
SLEEP_LED → SND_HP_MUTE_INV

XW9 SM — SND_AGND

RP44 100K 5% 1/16W SM1 — SND_AMP_MUTE → SND_AMP_MUTE_L
Q26 2N7002DW SOT-363 — AMP_CONTROL
RP44 100K 5% 1/16W SM1 — INT_PU_RESET_L
Q26 2N7002DW SOT-363

RP44 100K 5% 1/16W SM1 — SND_HP_MUTE_INV
R689 100K 5% 1/16W MF 402
Q31 2N7002DW SOT-363 — SND_HP_MUTE
Q31 2N7002DW SOT-363 — SND_HP_MUTE_L
RP44 100K 5% 1/16W SM1 — AMP_CONTROL

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

C767 10UF 20% 6.3V CERM 805
C513 NO STUFF 0.1UF 20% 16V CERM 402
R405 10K 5% 1/16W MF 402
C478 NO STUFF 0.1UF 20% 16V CERM 402
C469 10UF 20% 6.3V CERM 805

J8 CRITICAL
QT510166-L010
F-ST-SM1

MOD_DTO → MOD_SYNC
MOD_CLKOUT → INT_MOD_DTI
MOD_BITCLK
COMM_RESET_L
COMM_SHUTDOWN → MODEM_USB_DM
INT_I2C_CLK2 → MODEM_USB_DP
INT_I2C_DATA2 → COMM_RING_DET_L

SERIAL DEBUG INTERFACE

J16 SERIAL_DEBUG CRITICAL
M-ST-5087
SM

COMM_TXD_L → COMM_DTR_L
COMM_TRXC → COMM_RTS_L
COMM_GPIO_L → COMM_RXD

DEBUG POWER BUTTON

R527 NO STUFF 0 5% 1/16W MF 603 — PWR_BUTTON_L

FAN CONTROLLER

R814 10 5% 1/16W MF 402 — ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402

U3 ADT7460 QSOP
VCC, +2.5V/SMBALERT#, SDA, SCL, D1+, D1-, D2+, D2-, GND
PWM1/XTO, TACH1, PWM2/SMBALERT#, TACH2, PWM3/ADR ENABLE#, TACH3, TACH4/ADR SELECT/THERM#

ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM

R42 10K 5% 1/16W MF 402 — ADT7460_FAN1_PWM
R692 10K 5% 1/16W MF 402 — FANL_TACH
R695 10K 5% 1/16W MF 402 — ADT7460_FAN2_PWM
FANR_TACH
ADT7460_ADR_EN_L
NC
ADT7460_THERM

Q78 2N7002DW SOT-363 — FANL_PWM
Q78 2N7002DW SOT-363 — FANR_PWM

C688 NO STUFF 0.001UF 20% 50V CERM 402
C690 NO STUFF 0.001UF 20% 50V CERM 402
C846 NO STUFF 0.001UF 20% 50V CERM 402
C905 NO STUFF 0.001UF 20% 50V CERM 402

DEBUG JUMPERS

R293 10K 5% 1/16W MF 402 — FANL_PWM
R295 10K 5% 1/16W MF 402 — FANR_PWM

R537 NO STUFF 0 5% 1/16W MF 603 — PMU_NMI_BUTTON_L
R553 NO STUFF 0 5% 1/16W MF 603 — PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

R623 10K 5% 1/16W MF 402

J2 CRITICAL
SM-2MT

FANR_GND
FANR_TACH
FANR_PWM

Q36 SI3446DV TSOP

C135 4.7UF 20% 10V CERM 1206 — PLACE CLOSE TO CONNECTOR

LEFT FAN (CPU)

R679 10K 1/16W 5% MF 402

J4 CRITICAL
SM-2MT

FANL_TACH
FANL_GND
FANL_PWM

Q37 SI3446DV TSOP

C134 4.7UF 20% 10V CERM 1206 — PLACE CLOSE TO CONNECTOR

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
C681 0.001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DP
SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DP
CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
C678 NO STUFF 0.001UF 20% 50V CERM 402
Q47 2N3904 SM
THERM1_A_DP
THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
C651 NO STUFF 0.001UF 20% 50V CERM 402
Q62 2N3904 SM
THERM2_A_DP
THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP → THERM1_DP
R725 0 5% 1/16W MF 402 — CPU_M_DM → THERM1_DM
R713 0 5% 1/16W MF 402 — SUPPLY_M_DP → THERM2_DP
R716 0 5% 1/16W MF 402 — SUPPLY_M_DM → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R723 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DP → THERM1_DP
R726 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DM → THERM1_DM
R710 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DP → THERM2_DP
R717 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DM → THERM2_DM

THERM ISOLATION

R811 100K 5% 1/16W MF 402 — +3V_MAIN
R812 100K 5% 1/16W MF 402 — +3V_PMU_AVCC
THERM_L_OC
THERM_INV
ADT7460_THERM
R813 100K 5% 1/16W MF 402
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to
facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB 2.0

APPLE COMPUTER INC.

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Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/10W MF 402

3405_MODE

R319 0 5% 1/10W MF 402

U14 LTC3405 SOT23-6 CRITICAL
VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L5 3.3uH SM1

+1_0V_MARVELL

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

C486 10uF 20% 6.3V CERM 805

3405_VFB

R362 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — CLKENET_LINK_TX — CLKENET_PHY_TX

R353 0 5% 1/16W MF 402 — CLKENET_LINK_RX — CLKENET_PHY_RX

R344 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF — CLKENET_PHY_GBE_REF

U49 88E1111 BCC CRITICAL

TX_CLK, RX_CLK, 125CLK, CTRL10

TXD0, TXD1, TXD2, TXD3, TXD4, TXD5, TXD6, TXD7

TX_EN, TX_ER, GTX_CLK

RXD0, RXD1, RXD2, RXD3, RXD4, RXD5, RXD6, RXD7

RX_DV, RX_ER, CRS, COL, MDC, MDIO

INT-/INT+, RESET, COMA

S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-

XTAL1, XTAL2, VSSC

DVDD, VDDO, VDDOH, VDDOX, AVDD

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

CONFIG0, CONFIG1, CONFIG2, CONFIG3, CONFIG4, CONFIG5, CONFIG6

TDI, TDO, TCK, TMS, TRST, RSET, SEL_OSC, SEL_2.5V, GND

C492 C511 C517 C502 C465 C475 0.1UF/0.01UF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C464 C472 C453 C503 C501 C496 0.1UF/0.01UF/10uF

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C497 C504 C487 C476 C754 0.1UF/0.01UF/10uF

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MARVELL

+2_5V_MARVELL_AVDD

L34 FERR-EMI-600-OHM SM

+2_5V_MAIN

R465 0 5% 1/16W MF 603

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W FF 805 — CHGND1

C488 C466 C506 C520 0.1UF 20% 10V CERM 402

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

CRITICAL J17 RJ45 RT-TH

RJ45_DP<0>, RJ45_C0_PD, RJ45_DN<0>, RJ45_DP<1>, RJ45_C1_PD, RJ45_DN<1>, RJ45_DP<2>, RJ45_C2_PD, RJ45_DN<2>, RJ45_DP<3>, RJ45_C3_PD, RJ45_DN<3>

Short shielded RJ-45

CHGND1

SM XFR-ENET-1000BT T1 CRITICAL

MDI_P<0>, MDI_M<0>, MDI_P<1>, MDI_M<1>, MDI_P<2>, MDI_M<2>, MDI_P<3>, MDI_M<3>

R346 R372 R404 R413 49.9 1% 1/16W MF 402

R355 R381 R406 R428 49.9 1% 1/16W MF 402

MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C454 C477 C493 C505 0.01UF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

R735 R733 R382 R347 75 5% 1/16W MF 402

ENET_CTAP_CHGND

C457 100pF 10% 3KV CERM 1808 — CHGND1

SEE CONFIG TABLES (BELOW)

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

+2_5V_MARVELL

R371 10K 5% 1/10W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 5% 1/16W MF 402

R343 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D1 1N914 SOT23 — IO_RESET_L — ENET_RST_L

ENET_ENERGY_DET

Q15 2N7002DW SOT-363 — AC_IN

Q15 2N7002DW SOT-363 — SLEEP_L_LS5

C755 2.2uF 20% 10V CERM 805

ENET_COMA

ENET_HSDACP, ENET_HSDACM

ENET_VSSC

CLK25M_ENET_XIN, CLK25M_ENET_XOUT

NO STUFF R435 20K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM — CLK25M_XTAL_IN

C555 C491 33pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0052	197S0011	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

SPEC SAID TO USE 10K

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

1MA(MAX) BUS HOLDER EACH

FIREWIRE

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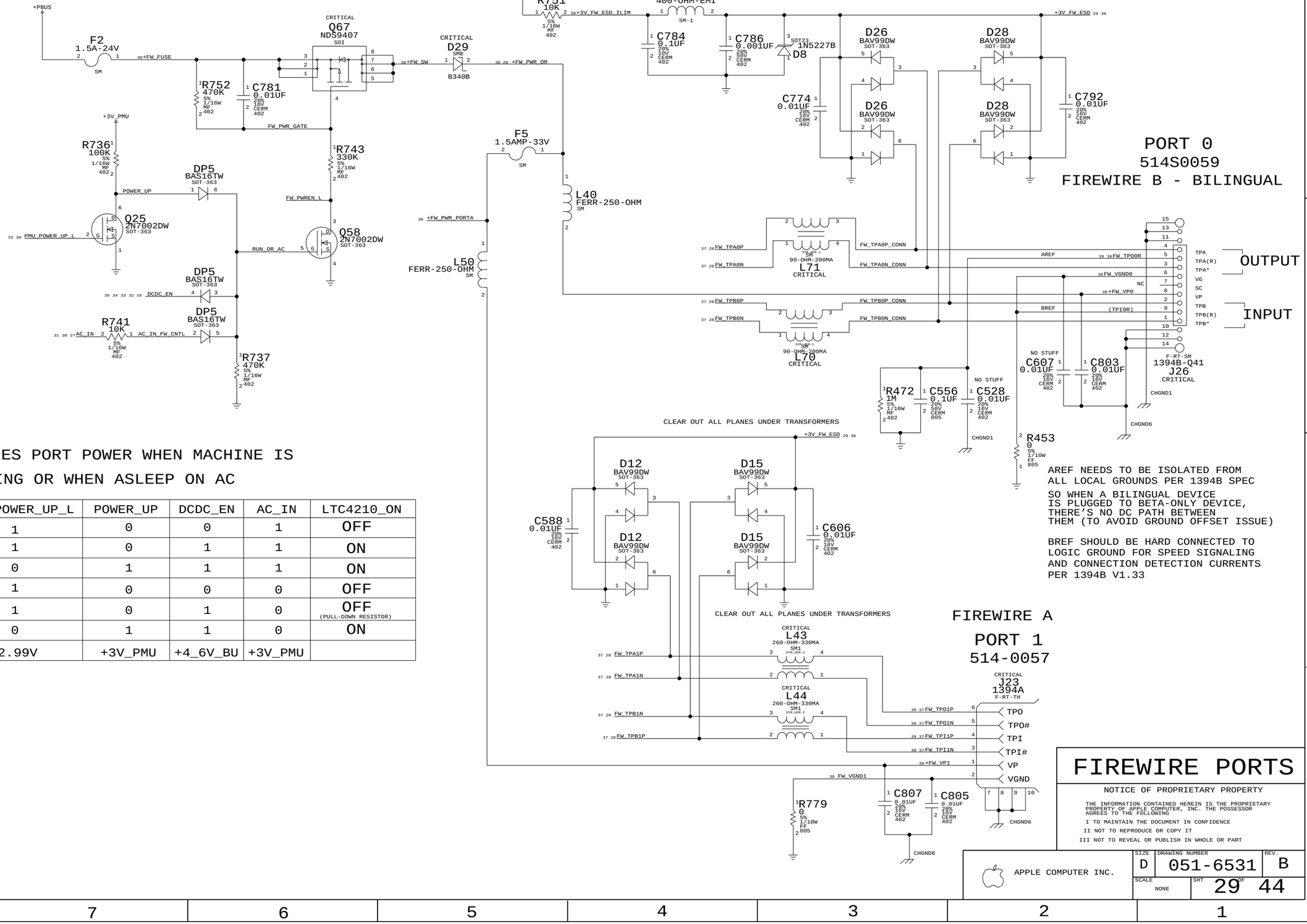
PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS
RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

APPLE COMPUTER INC.

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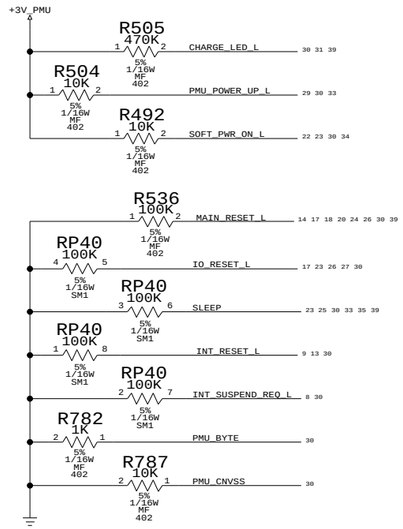
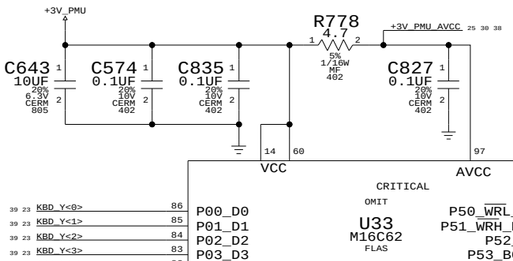




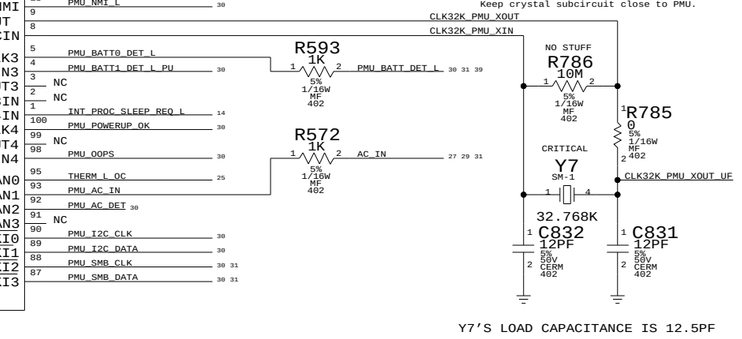
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

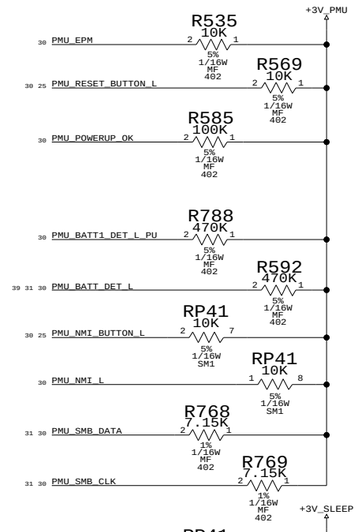
(PMU_AP)

44	CPU_VCORE_HI_OC	7 34
43	INT_RESET_L	9 13 30
42	MAIN_RESET_L	14 17 18 20 24 26 30 39
41	NC	
40	PMU_INT_NMI	14
39	PMU_EPM	30
38	INT_PU_RESET_L	13 25 30
37	PMU_CPU_HRESET_L	23
36	PMU_ACK_L	14
35	PMU_CLK	14
34	PMU_FROM_INT	14
33	PMU_TO_INT	14
32	PMU_REQ_L	14
31	PMU_LID_CLOSED_L	23 30
30	PMU_RESET_BUTTON_L	25 30
29	PMU_NMI_BUTTON_L	25 30
28	TPAD_RXD	23 30
27	TPAD_TXD	23 30
26	SYSTEM_CLK_EN	14
25	CPU_CLK_EN	8
24	PMU_CHARGE_V	31
23	PMU_CHRG_BATT_0	31
22	NC (CHARGE_I)	
21	NC	
20	PMU_SLEEP_LED_L	23
19	CPU_SMI_L	5
18	POWER_VALID	30
17	PMU_PME_L	14 26 30
16	INT_PEND_PROC_INT	14
15	PMU_NMI_L	30
9		
8	CLK32K_PMU_XOUT	
5	PMU_BATT0_DET_L	
4	PMU_BATT1_DET_L_PU	30
3	NC	
2	NC	
1	INT_PROC_SLEEP_REQ_L	14
100	PMU_POWERUP_OK	30
99	NC	
98	PMU_OOPS	30
95	THERM_L_OC	25
93	PMU_AC_IN	
92	PMU_AC_DET	30
91	NC	
90	PMU_I2C_CLK	30
89	PMU_I2C_DATA	30
88	PMU_SMB_CLK	30 31
87	PMU_SMB_DATA	30 31

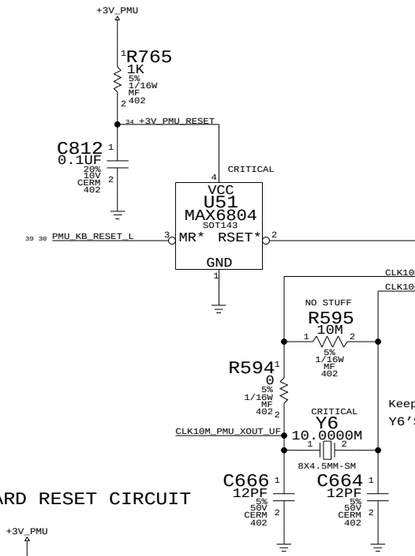
Keep crystal subcircuit close to PMU.



Y7'S LOAD CAPACITANCE IS 12.5PF

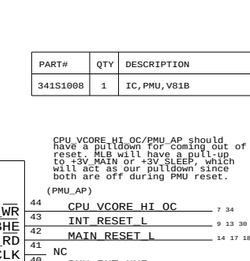


UNDERVOLTAGE RESET CIRCUIT

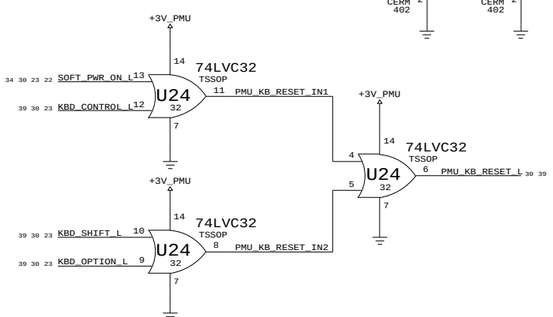


Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD



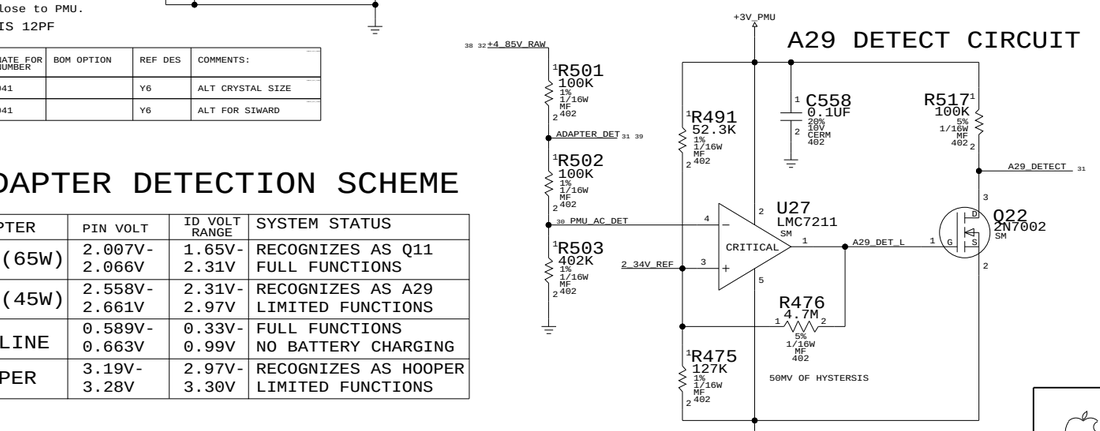
PMU KEYBOARD RESET CIRCUIT



Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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SCALE: NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

Q013 SI4435DY SOI
Q016 SI4435DY SOI

+ADAPTER_SW
+ADAPTER_SENSE

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805
R474 47K 5% 1/16W MF 402
R374 470K 5% 1/16W MF 402
AC_ENABLE_GATE
AC_ENABLE_L
BCKFD_PROT_GATE
C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q021 2N7002DW SOT-363

+3V_PMU
R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
1V20_REF
U15 LMC7211 SM CRITICAL
AC_IN
AC_DIV
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
R394 1M 5% 1/16W MF 402
AC_IN_L
Q010 2N7002DW SOT-363
R383 470K 5% 1/16W MF 402
Q010 2N7002DW SOT-363

GREATER THAN 13.5V DETECT

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP CRITICAL
RS+ RS- PG NC1 NC2 OUT GND NC NC MAX4172_OUT

+24V_PBUS
R454 2.21K 0.1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1

R460 0.025 1% 1W MF 2512
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
C578 0.47UF 20% 50V CERM 1206
C579 0.47UF 20% 50V CERM 1206

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_GND

U31 MAX1772 QSOP CRITICAL
CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CLS CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND

REF = 4.096V

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

C652 1UF 20% 10V CERM 603
C526 1K 1% 1/16W MF 402
C622 0.01UF 20% 10V CERM 402
C616 0.01UF 20% 10V CERM 402
1772_CCV_RC
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
1772_REF
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

R542 1K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R561 100K 5% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
Q027 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q027 2N7002DW SOT-363
PMU_CHARGE_V
Q029 2N7002DW SOT-363
BATT_LOW_L
Q029 2N7002DW SOT-363

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+3V_PMU
R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q030 2N7002DW SOT-363
Q030 2N7002DW SOT-363
PMU_CHRG_BATT_0

+3V_PMU
C615 0.1UF 20% 10V CERM 402
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
U38 LMC7211 SM CRITICAL
BATT_LOW
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q065 2N7002DW SOT-363
A29_DETECT

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
IAC_RC_COMP
C771 0.1UF 20% 10V CERM 402

+3V_PMU
R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5 CRITICAL
IAC_FB
R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ
Q020 2N7002DW SOT-363
A29_DETECT

+3V_PMU
R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
OVER_18V_ADJ
R748 100K 5% 1/16W MF 402
Q020 2N7002DW SOT-363
AC_GTR_18V
C775 1UF 20% 10V CERM 603
Q065 2N7002DW SOT-363
1772_ACOK_L

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
1772_LDO

+24V_PBUS
C608 0.1UF 20% 50V CERM 805

Q63 IRF7805 SM CRITICAL
Q64 IRF7811W SO-8 CRITICAL

C547 2.2UF 20% 6.3V CERM 1812
C562 2.2UF 20% 6.3V CERM 1812
C563 2.2UF 20% 6.3V CERM 1812
C557 2.2UF 20% 6.3V CERM 1812
C564 2.2UF 20% 6.3V CERM 1812

L42 10uH SM1 CRITICAL
D30 MBRS140T3 SM
+BATT_RSNS
R763 0.05 1% 1W MF 2512
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206
+BATT_24V_FUSE
C824 33UF 20% 25V ELEC SM1

NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

Q024 SI4435DY SOI CRITICAL
Q076 SUD45P03 TO-252 CRITICAL

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
BATT_24PBUS_EN
BATT_14PBUS_EN
DP4 BAS16TW SOT-363
Q021 2N7002DW SOT-363

AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_VSNS
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
L8 FERR-EMI-100-OHM SM
L12 FERR-50-OHM SM
PMU_SMB_CLK
PMU_SMB_DATA

BATTERY CHARGER

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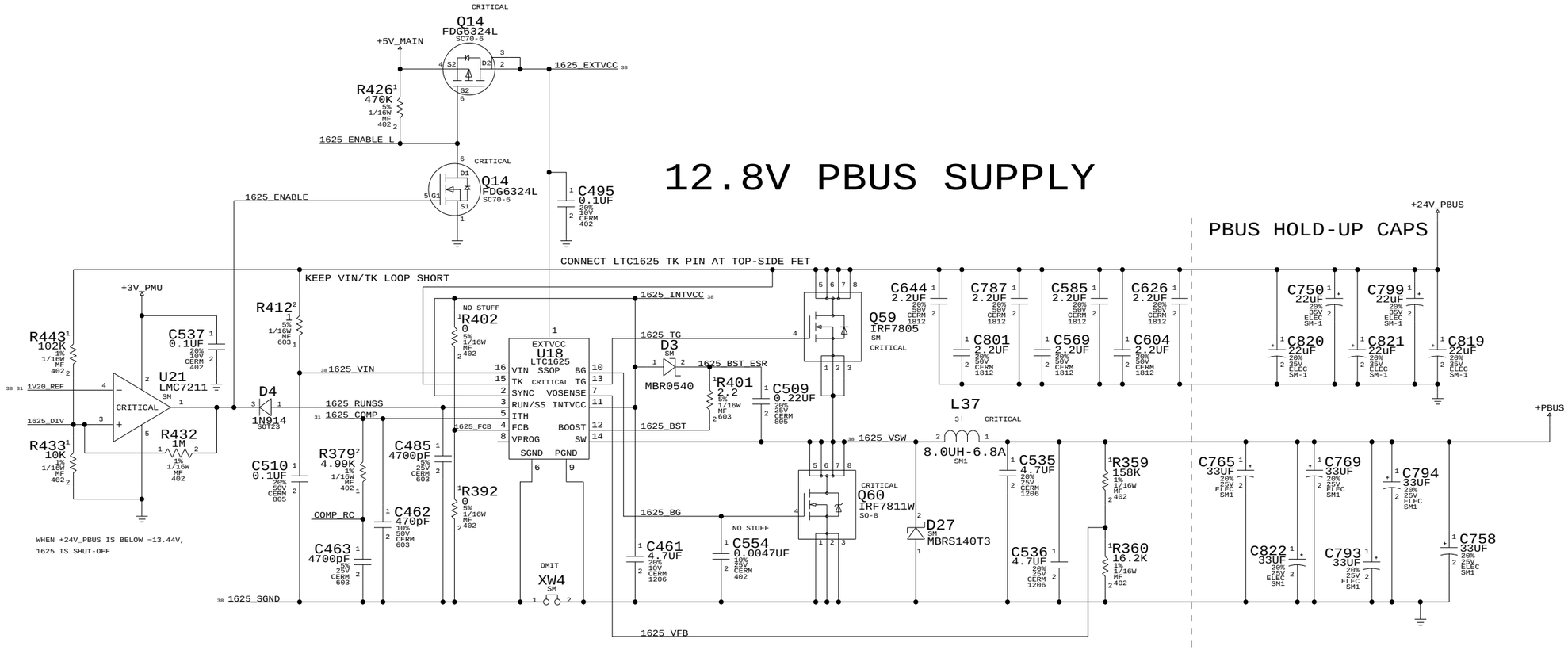
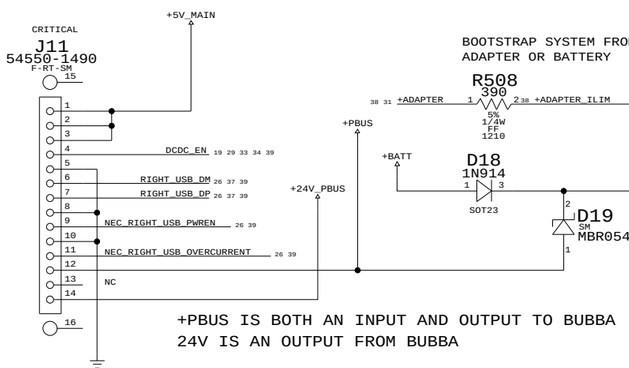
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 31 OF 44	

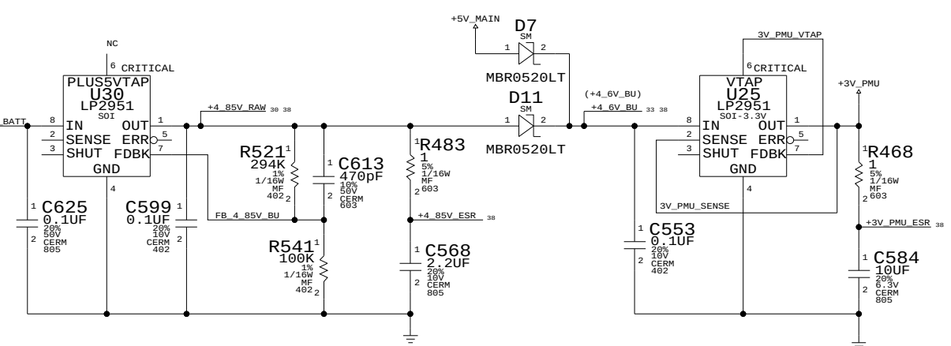
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

APPLE COMPUTER INC.

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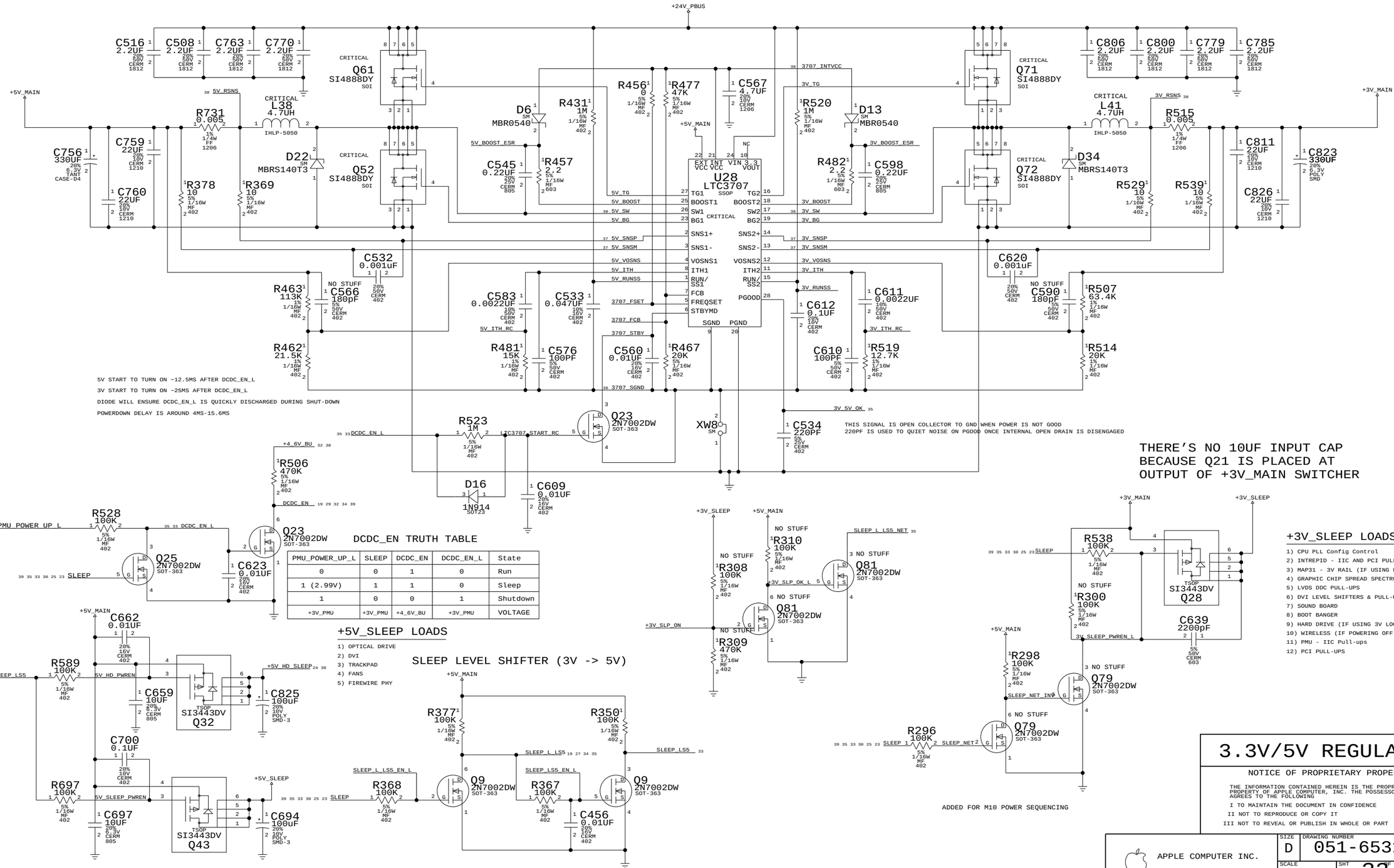
3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

+5V_MAIN

MAXBUS_SLEEP

CPU_VCORE_PWR_SEQ

CPU_VCORE_SEQ_L

CPU_VCORE_SEQ

SLEEP_L_LS5

DCDC_EN

CPU_VCORE_HI_OC

INT_GPIO1_PU

VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>

VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>

VCORE_MUX_SEL
VCORE_MUX_EN

U11 PI3B3257 QSOP (STR_VER=2)
VCC, A1, B1, A2, B2, A3, B3, A4, B4, SEL, OE, GND, Y1, Y2, Y3, Y4
CRITICAL

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

+PBUS

CRITICAL C427 8.2UF 20% 16V TANT CASE-D
CRITICAL C431 8.2UF 20% 16V TANT CASE-D
CRITICAL C443 8.2UF 20% 16V TANT CASE-D
CRITICAL C430 8.2UF 20% 16V TANT CASE-D
CRITICAL C432 8.2UF 20% 16V TANT CASE-D
CRITICAL C441 8.2UF 20% 16V TANT CASE-D
CRITICAL C444 8.2UF 20% 16V TANT CASE-D
CRITICAL C445 8.2UF 20% 16V TANT CASE-D

CPU_VCORE_SLEEP

C2 10UF 20% 6.3V CERM 805
C689 10UF 20% 6.3V CERM 805
C5 10UF 20% 6.3V CERM 805
C699 10UF 20% 6.3V CERM 805
C234 10UF 20% 6.3V CERM 805
C682 10UF 20% 6.3V CERM 805
C674 10UF 20% 6.3V CERM 805
C274 10UF 20% 6.3V CERM 805
C7 10UF 20% 6.3V CERM 805
C680 10UF 20% 6.3V CERM 805
C693 10UF 20% 6.3V CERM 805
C13 10UF 20% 6.3V CERM 805
C116 10UF 20% 6.3V CERM 805
C6 10UF 20% 6.3V CERM 805
C695 10UF 20% 6.3V CERM 805
C679 10UF 20% 6.3V CERM 805
C285 10UF 20% 6.3V CERM 805
C4 10UF 20% 6.3V CERM 805
C3 10UF 20% 6.3V CERM 805
C687 10UF 20% 6.3V CERM 805

+5V_MAIN

VCORE_VCC

PLACE C423 CLOSE TO PINS 15 & 13!

D2 SM MBR0530

VCORE_BOOST

VCC U20 MAX1717 QSOP VDD

SKP/SDN, FBS, ILIM, GNDS, A/B, REF, TON, CC, D0, D1, D2, D3, D4, V+, BST, DH, LX, DL, GND, FB, TIME, VGATE

VCORE_VPLUS
VCORE_BST
VCORE_DH
VCORE_LX
VCORE_DL
VCORE_GND
VCORE_FB
VCORE_TIME
VCORE_VGATE

CRITICAL Q50 SI7860DP SO-8-PWRPK
CRITICAL Q49 SI7860DP SO-8-PWRPK
CRITICAL Q54 IRF7832 SO-8
CRITICAL Q55 IRF7832 SO-8
CRITICAL Q53 IRF7832 SO-8

Keep trace fat and short!!

CRITICAL L36 1.2UH-18.3A SM1

CPU_VCORE_SLEEP_F

CRITICAL R331 0.001 1% 1W MF 2512

CRITICAL C728 220UF 20% 2V TANT 7343
CRITICAL C734 220UF 20% 2V TANT 7343
CRITICAL C733 220UF 20% 2V TANT 7343
CRITICAL C732 220UF 20% 2V TANT 7343
CRITICAL C885 220UF 20% 2V TANT 7343
CRITICAL C731 220UF 20% 2V TANT 7343
CRITICAL C730 220UF 20% 2V TANT 7343
CRITICAL C729 220UF 20% 2V TANT 7343
CRITICAL C884 220UF 20% 2V TANT 7343

CRITICAL D25 B540C SM
R732 2.2 5% 1/4W MF 1210
NO STUFF
CPU_VCORE_SNUB

C455 0.0047UF 10% 25V CERM 402
C518 0.1UF 20% 25V CERM 603
C768 0.0047uF 10% 25V CERM 402
C764 0.0022uF 10% 50V CERM 603
NO STUFF

XW5 SM
XW7 SM
R415 100 5% 1/16W MF 402

R297 470K
R314 470K NO STUFF
R328 0 NO STUFF
R324 0 NO STUFF
R304 470K
R329 0
R325 0
R322 10K NO STUFF
R303 0 NO STUFF
R313 470K NO STUFF
R327 470K NO STUFF
R323 470K NO STUFF
R301 470K NO STUFF
R305 0 NO STUFF
R330 470K NO STUFF
R326 0 NO STUFF
R302 1K
<D4> <D3> <D2> <D1> <D4> <D3> <D2> <D1>

R408 100K
R398 100K
R356 100K
DP2 BAS16TW SOT-363
R267 10K
Q12 2N3904 SM
Q017 2N3904 SM
R318 0

R288 0 NO_4XVCORE
R289 0 NO_4XVCORE
R290 0 NO_4XVCORE
R292 0 NO_4XVCORE

R384 0 NO STUFF
R366 0
R337 470K NO STUFF
<D0>

R397 27.4K
R407 0
C507 1UF 20% 10V CERM 603
R349 20
C498 1UF 20% 10V CERM 603
R429 2.2

R336 470K
C529 0.01UF 20% 16V CERM 402
R448 66.5K
R385 12.7K
C459 1UF 20% 10V CERM 603
C512 220PF 5% 25V CERM 402
R434 390K
C521 0.001UF 20% 50V CERM 402

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU
XW3 SM

VCORE_GNDSNS
VCORE_SNS

+5V_MAIN
R805 100K
VCORE_SEL_OFF_PU
R809 1.5K 1%
VCORE_SEL_ON
R806 0 NO STUFF
R807 0
AB_SEL_LOW
MAX1717_AB_SEL
Q086 2N7002DW SOT-363
R808 100K NO STUFF

VCORE_OFFSET
R376 162K 1% R2
VCORE_GNDDIV
OMIT
R321 3.01K 1% R1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

FMAX CONNECTOR

NO STUFF
R315 2.05K 1%
R312 100 1%
CRITICAL
NO STUFF
J5 M-ST-SM-52465-1217

VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)
VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

VCORE SUPPLY

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D	051-6531	B
SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		27
	CLK25M_ENET_XOUT						10 MIL SPACING		27
	NEC_XT1						10 MIL SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 25 39
	SND_CLKOUT					200.0000	10 MIL SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		28
	FW_OSC					200.0000	10 MIL SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 24
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	208				13 24
	UIDE_DATA<6..0>				200			100 MHZ	13 24
	UIDE_ADDR<2..0>				200			100 MHZ	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	24
	HD_ADDR<2..0>		5		208			100 MHZ	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS					31
	1772_CSSP	1772_CSS					31
	1772_CSIN	1772_CSI					31
	1772_CSIP	1772_CSI					31
	3V_SNSM	3V_SNS					33
	3V_SNSP	3V_SNS					33
	5V_SNSM	5V_SNS					33
	5V_SNSP	5V_SNS					33
THERMOSTAT	THERM1_DM	THERM1					25
	THERM1_DP	THERM1					25
	THERM2_DM	THERM2					25
	THERM2_DP	THERM2					25
	THERM1_M_DM	THERM1_MAIN					
	THERM1_M_DP	THERM1_MAIN					
	THERM2_M_DM	THERM2_MAIN					
	THERM2_M_DP	THERM2_MAIN					
	THERM1_A_DM	THERM1_ALT					25
	THERM1_A_DP	THERM1_ALT					25
	THERM2_A_DM	THERM2_ALT					25
	THERM2_A_DP	THERM2_ALT					25

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM INTREPID PLLS	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS ATI M10	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1538	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1539	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1536	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1540	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1535	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1536	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1537	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1538	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1541	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1540	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1539	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1542	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1543	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1547	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1544	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1545	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1546	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1548	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1551	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1549	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1550	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1552	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0 INTREPID SSCG	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

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D	051-6531	B
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FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
T290 FUNC_TEST=YES CHGND4 38
T290 FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
T291 FUNC_TEST=YES SND_AMP_MUTE 25
T292 FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
T289 FUNC_TEST=YES SRCLK_TP 26
T288 FUNC_TEST=YES SRMOD_TP 26
T290 FUNC_TEST=YES TEB_TP 26
T290 FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
T271 FUNC_TEST=YES FANR_PWM 25
T272 FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPO0R 29 38
T281 FUNC_TEST=YES VCORE_VID0
T282 FUNC_TEST=YES VCORE_VID1
T283 FUNC_TEST=YES VCORE_VID2
T284 FUNC_TEST=YES VCORE_VID3
T285 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
T273 FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
T276 FUNC_TEST=YES MOD_CLKOUT 14 25
T277 FUNC_TEST=YES MOD_DTO 14 25
T279 FUNC_TEST=YES MOD_SYNC 14 25
T276 FUNC_TEST=YES SLEEP 23 25 30 33 35
T280 FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6531 | REV. B

SCALE NONE | SHT 39 OF 44

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE FOR CONSTRAINT BACK ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)

*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)

*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)

*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV

*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)

*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)

*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVODMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constriants for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022 (124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)

*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS

*** RELEASED FOR PRODUCTION 7/28/03 ***

8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SIL1162 TMDS TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT

9/4/03
228) ADDED 197S0052 AS ALTERNATE FOR G1 (98 MHZ FW OSCILLATOR)
229) CHANGED C728-C734,C884,C885 TO 128S0022 TO REMOVE DUPLICATE PART NUMBER
230) CHANGED C883 TO 132S0100 TO CORRECT FOR USE OF OEM PART NUMBER

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6531 | REV. B

SCALE NONE | SHT 40 OF 44

8 7 6 5 4 3 2 1

D C B A

*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL 27D2< 38B3>
+1_5V_AGP 12C5< 12D1< 12D4< 15D6< 16C8<
18C6< 18D6< 19A8< 19B4<> 19D5<>
21B8< 21D6< 38C3>
+1_5V_AGP_GPU 21C5< 38C3>
+1_5V_AGP_NECK 19B4<> 38B3>
+1_5V_GPU_VDD15 19D3< 38C3>
+1_5V_INTREPID_PLL 8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1 14C3< 38D3>
+1_5V_INTREPID_PLL2 14D3< 38D3>
+1_5V_INTREPID_PLL3 14D3< 38D3>
+1_5V_INTREPID_PLL4 14D3< 38D3>
+1_5V_INTREPID_PLL5 12D3< 38D3>
+1_5V_INTREPID_PLL6 12D6< 38D3>
+1_5V_INTREPID_PLL7 8D5< 38D3>
+1_5V_INTREPID_PLL8 14D3< 38D3>
+1_5V_LDO 35D8< 38D6>
+1_5V_MAIN 38D6>
+1_5V_SLEEP 38D6>
+1_5V_SLEEP_NECK 21A3<> 38B3>
+1_5V_SLEEP_VIN 35D8<> 38D6>
+1_8V_ATI_PVDD 19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD 21D2<>
+1_8V_DVO_F 21B2<
+1_8V_GPU 18A7< 19D8< 20A5< 21A2< 21A6<
21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD 21D5< 38C3>
+1_8V_GPU_AVDDQ 21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL 21B5< 38C3>
+1_8V_GPU_PLL 21D5< 38C3>
+1_8V_GPU_PNLIO 21A5< 38C3>
+1_8V_GPU_PNLPLL 21B5< 38C3>
+1_8V_GPU_TP_PLL 21B4< 21D1<
+1_8V_GPU_VDDDI 21C7< 21D4< 38C3>
+1_8V_MAIN 38D6> 39A2>
+1_8V_MAIN_LX_F 35A4<>
+1_8V_PVDD_NECK 19B5<> 38B3>
+1_8V_SLEEP 38D6>
+1_8V_SLEEP_NECK 21A3<> 38B3>
+1_95V_FW_DVDD 28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1 28D6< 38A3>
+1_95V_FW_DVDD_RX0 28C5< 38A3>
+1_95V_FW_DVDD_TX0 28C5< 38A3>
+1_95V_FW_PLL400VDD 28D5< 38A3>
+1_95V_FW_PLL500VDD 28D5< 38A3>
+1_95V_FW_PLLVDD 28D5< 28D7<> 38A3>
+2_5V_CG_MAIN 14C6< 38A3>
+2_5V_GPU 21A7< 21B6< 21D3< 21D7< 21D8<
38B3>
+2_5V_GPU_A2VDD 21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO 21A5< 38C3>
+2_5V_INTREPID 9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
16B8< 38D3>
+2_5V_MAIN 38D6>
+2_5V_MARVELL 27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD 27C4< 38B3>
+2_5V_SLEEP 38D6>
+2_5V_SLEEP_NECK1 19C4<> 38B3>
+2_5V_SLEEP_NECK2 21A3<> 38B3>
+3V_ATI_OSC_SLEEP 18D2< 38C3>
+3V_ATI_SS 18B2< 38C3>
+3V_CG_PLL_MAIN 14C6< 38A3>
+3V_FW 28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD 28C6< 38A3>
+3V_FW_AVDD_PORT0 28C6< 38A3>
+3V_FW_AVDD_PORT1 28C6< 38A3>
+3V_FW_AVDD_PORT2 28D6< 38A3>
+3V_FW_ESD 29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM 29D4< 38B3>
+3V_FW_UF 28D7<> 38A3>
+3V_GPU 12D1< 18B8< 18C5< 18C7< 18D6<
19C4< 19C5< 19C7< 19D7< 21A6< 21B1<
38C3>
+3V_GPU_FLT 21B2< 38C3>
+3V_GPU_SI 20C4< 20C8< 20D8<
+3V_HALL_EFFECT 23C6<> 38B6> 39C4>
+3V_INTREPID_USB 14C3< 38D3>
+3V_LCD 22B4<> 38B6>
+3V_LCD_SW 22A4<> 38B6>
+3V_MAIN 38D6>
+3V_NEC_VDD 26D7< 26D7< 38A3>
+3V_PMU 38D6> 39A2>
+3V_PMU_AVCC 25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR 32A2< 38C6>
+3V_PMU_RESET 30B7< 34A3<>
+3V_SI_AVCC 20C7< 38B3>
+3V_SI_PLLVCC 20C7< 38B3>
+3V_SI_VCC 20C6< 38B3>
+3V_SLEEP 38D6>
+3V_SLEEP_NECK 21A3<> 38B3>
+3V_SLP_OK_L 33B4<>
+3V_SLP_ON 33A5<>
+4_6V_BU 32A3<> 33B6< 38C6>
+4_85V_ESR 32A4< 38C6>
+4_85V_RAW 30B4< 32A4<> 38C6>
+5V_DDC_SLEEP 22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF 22D6< 38B6>
+5V_HD_SLEEP 24D1<> 33A7<> 38C6>
+5V_INV_SW 22B2<> 38B6> 39D1>
+5V_INV_UF_SW 22B2<> 38B6>
+5V_MAIN 38D6>
+5V_SLEEP 38D6>
+5V_SOUND_SLEEP 38B6>
+5V_TPAD_SLEEP 23C7<> 38B6> 39C4>
+12_8V_INV 22B1<> 38B6> 39A2>
+24V_PBUS 38D6> 39B2>
+ADAPTER 31D8<> 32B7<> 38D6>
+ADAPTER_ILIM 32B6<> 38C6>
+ADAPTER_OR_BATT 32A5<> 38C6>
+ADAPTER_SENSE 31D5<> 38C6>
+ADAPTER_SW 31D6<> 38C6>
+BATT 38D6>
+BATT_14V_FUSE 31D1<> 38C6>
+BATT_24V_FUSE 31B1< 31D2<> 38C6>
+BATT_POS 31A4<> 38C6> 39C3>
+BATT_RSNS 31B2< 38C6>
+BATT_VSNS 31A4< 38C6>
+FW_FUSE 29D7<> 38A3>
+FW_PWR_OR 28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA 29C5< 38A3>
+FW_SW 29D5<> 38A3>
+FW_VP0 29C2<> 38A3>
+FW_VP1 29A3<> 38A3>
+GPU_MCLK 21C7< 21D4< 38C3>
+GPU_MEM 18A6<> 18B8< 21B4< 21B7< 21C6<
21C8< 21D2< 38C3>
+GPU_MEMCORE 21C5< 38C3>
+GPU_VDD15_NECK 19B5<> 38B3>
+GPU_VDD15_UF 19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP 24C2<> 38C6>
+PBUS 38D6> 39B2>
+VCC_CBUS_SW 17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW 17B1<> 17B2<> 17D2<> 38C3>
1V20_REF 31C7< 32C8< 38D1>
1V65_REF 31A5<
1_5V_2_5V_OK 35C5> 38B1>
1_5V_BOOST 35C6<> 38C1>
1_5V_BST 35C5<> 38C1>
1_5V_DH 35C5<> 38C1>
1_5V_DL 35B5<> 38C1>
1_5V_FB 35B5< 35B7< 38C1>
1_5V_ILIM 35C5<> 38C1>
1_5V_LX 35B5<> 38C1>
1_5V_SLEEP_EN_L 35C7<> 35D7<>
1_8V_SLEEP_PWREN_L 35A3<>
1_8V_SW 35A5<> 38A1>
1_8V_VFB 38A1>
2_5V_BOOST 35C4<> 38D1>
2_5V_BST 35C4<> 38D1>
2_5V_DH 35C4<> 38D1>
2_5V_DL 35B4<> 38D1>
2_5V_ILIM 35C5<> 38C1>
2_5V_LX 35B4<> 38D1>
2_5V_SLEEP_PWREN_L 35C2<>
2_34V_REF 30A4<
3V_5V_OK 33B4<> 35A8<> 35D6<
3V_5V_OK_INV 35A8<>
3V_BG 33C4<>
3V_BOOST 33C4<>
3V_BOOST_ESR 33D3<>
3V_ITH 33C4<>
3V_ITH_RC 33C3<
3V_PMU_VTAP 32B3<
3V_RSNS 33D2< 38D1>
3V_RUNSS 33C4<
3V_SLEEP_PWREN_L 33A3<>

3V_SNSM 33C4< 37A2>
3V_SNSP 33C4< 37A2>
3V_SW 33C4<> 38D1>
3V_TG 33D4<>
3V_VOSNS 33C4<>
5V_BG 33C5<>
5V_BOOST 33C5<>
5V_BOOST_ESR 33D6<>
5V_HD_PWREN 33A8<>
5V_ITH 33C5<>
5V_ITH_RC 33C6<
5V_RSNS 33D7< 38D1>
5V_RUNSS 33C5<
5V_SLEEP_PWREN 33A8<>
5V_SNSM 33C5< 37A2>
5V_SNSP 33C5< 37A2>
5V_SW 33C5<> 38D1>
5V_TG 33C5<>
5V_VOSNS 33C5<>
1625_BG 32C5<>
1625_BST 32C5<
1625_BST_ESR 32C5<>
1625_COMP 31D2< 32C6<
1625_DIV 32C8<
1625_ENABLE 32D7<>
1625_ENABLE_L 32D6<>
1625_EXTVCC 32D5<> 38D1>
1625_FCB 32C6<
1625_INTVCC 32C5<> 38D1>
1625_RUNSS 32C6<
1625_SGND 32B7<> 38D1>
1625_TG 32C5<>
1625_VFB 32B5<>
1625_VIN 32C6< 38D1>
1625_VSW 32C4<> 38D1>
1772_ACIN 31B5<
1772_ACOK_L 31B5<> 31C4<>
1772_BST 31B4<>
1772_BST_ESR 31C3<
1772_CCI 31B5<>
1772_CCS 31B5<
1772_CCV 31B5<>
1772_CCV_RC 31B5<
1772_CELLS 31B4<
1772_CLS 31A4<
1772_CSIN 31B4<> 37A2>
1772_CSIP 31B4<> 37A2>
1772_CSSN 31C5< 37A2>
1772_CSSP 31C5< 37A2>
1772_DCIN 31B5< 38C6>
1772_DHI 31B4<>
1772_DLO 31B4<>
1772_DLOV 31B4<> 38C6>
1772_GND 31A5<> 38C6>
1772_ICHG 31B5<>
1772_ICTL 31B5<>
1772_IINP 31B5<
1772_LDO 31C4<> 38C6>
1772_LX 31B4<> 38C6>
1772_REF 31B5<>
1772_VCTL 31B5<
1778_BG 19A5<> 38B1>
1778_BST 19A5<> 38B1>
1778_BST_RC 19A4<> 38B1>
1778_FCB 19A5< 38B1>
1778_GND 19A5< 19A7<> 38B1>
1778_ION 19A5< 38B1>
1778_ITH 19A5<> 38B1>
1778_ITH_RC 19A7< 38B1>
1778_SHDN_L 19A6<
1778_SHDN_L_D3COLD 19A7<>
1778_TG 19A5<> 38B1>
1778_VCC 19A5<> 38B1>
1778_VFB 19A2< 19A5< 38B1> 39A1>
1778_VIN 19A5< 38B1>
1778_VRNG 19A5< 38B1>
3405_MODE 27D5<
3405_VFB 27D4<>
3707_FCB 33C5<
3707_FSET 33C5<
3707_INTVCC 33D4<> 38D1>
3707_SGND 33B5<> 38D1>
3707_STBY 33C5<>
A29_CLS_ADJ 31A5<>
A29_CURRENT_ADJ 31C4<>
A29_DETECT 30A2< 31A5<> 31C4<>
A29_DET_L 30A3<
AB_SEL_LOW 34A6<>
AC_DIV 31C8<
AC_ENABLE_GATE 31D6<>
AC_ENABLE_L 31C6<>
AC_GTR_18V 31C4<>
AC_IN 27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL 29C7<>
AC_IN_L 31C2<> 31C6<>
AC_IN_L_RC 31C2<>
ADAPTER_DET 30A4< 31D8<> 39C2>
ADAPTER_I_REG 31D3<>
ADT7460_ADR_EN_L 25B3<>
ADT7460_FAN1_PWM 25B3<>
ADT7460_FAN2_PWM 25B3<>
ADT7460_THERM 25A5<> 25B3<>
ADT7460_VCC 25C4<
ADT7460_VCORE_MON 5C8<> 25B4<>
AGP8X_DET_PU 18C6<>
AGP_AD<0> 12D2<> 18C7<>
AGP_AD<15..0> 37D5>
AGP_AD<1> 12C2<> 18C7<>
AGP_AD<2> 12C2<> 18C7<>
AGP_AD<3> 12C2<> 18C7<>
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COMM_RTS_L 14C2> 25D1<> 39B2>
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CSLOT_ADDR8_SPN 13B7>
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DVI_HPD_UF 22C3< 22C5<> 39C7>
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HD_DMARQ 13C6< 24C2<> 37B5>
HD_INTRQ 13C6< 24C1<> 37B5>
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KBD_LED2_OUT 23A5<> 23A7<> 38B6> 39C2>
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LTC3411_ITH_RC 38A1>
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RAM_DATA_B<4>   10C8<> 11D5<>
RAM_DATA_B<5>   10C8<> 11D5<>
RAM_DATA_B<6>   10C8<> 11D5<>
RAM_DATA_B<7>   10C8<> 11D5<>
RAM_DATA_B<8>   10C8<> 11D3<>
RAM_DATA_B<15..8>  36C5>
RAM_DATA_B<9>   10C9<> 11D3<>
RAM_DATA_B<10>  10C8<> 11D3<>
RAM_DATA_B<11>  10C8<> 11D3<>
RAM_DATA_B<12>  10C8<> 11D5<>
RAM_DATA_B<13>  10C8<> 11D5<>
RAM_DATA_B<14>  10C8<> 11D5<>
RAM_DATA_B<15>  10C8<> 11D5<>
RAM_DATA_B<16>  10C6<> 11D3<>
RAM_DATA_B<31..16>  36B5>
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RAM_DATA_B<18>  10C6<> 11C3<>
RAM_DATA_B<19>  10C6<> 11C3<>
RAM_DATA_B<20>  10C6<> 11D5<>
RAM_DATA_B<21>  10C6<> 11C5<>
RAM_DATA_B<22>  10C6<> 11C5<>
RAM_DATA_B<23>  10C6<> 11C5<>
RAM_DATA_B<24>  10C6<> 11C3<>
RAM_DATA_B<25>  10C6<> 11C3<>
RAM_DATA_B<26>  10C6<> 11C3<>
RAM_DATA_B<27>  10C6<> 11C3<>
RAM_DATA_B<28>  10C6<> 11C5<>
RAM_DATA_B<29>  10C6<> 11C5<>
RAM_DATA_B<30>  10C6<> 11C5<>
RAM_DATA_B<31>  10C6<> 11C5<>
RAM_DATA_B<32>  10D4<> 11B3<>
RAM_DATA_B<47..32>  36B5>
RAM_DATA_B<33>  10C4<> 11B3<>
RAM_DATA_B<34>  10C4<> 11B3<>
RAM_DATA_B<35>  10C4<> 11B3<>
RAM_DATA_B<36>  10C4<> 11B5<>
RAM_DATA_B<37>  10C4<> 11B5<>
RAM_DATA_B<38>  10C4<> 11B5<>
RAM_DATA_B<39>  10C4<> 11B5<>
RAM_DATA_B<40>  10C4<> 11B3<>
RAM_DATA_B<41>  10C4<> 11B3<>
RAM_DATA_B<42>  10C4<> 11A3<>
RAM_DATA_B<43>  10C4<> 11A3<>
RAM_DATA_B<44>  10C4<> 11B5<>
RAM_DATA_B<45>  10C4<> 11B5<>
RAM_DATA_B<46>  10C4<> 11A5<>
RAM_DATA_B<47>  10C4<> 11A5<>
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RAM_DATA_B<55..48>  36B5>
RAM_DATA_B<49>  10C2<> 11A3<>
RAM_DATA_B<50>  10C2<> 11A3<>
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RAM_DATA_B<53>  10C2<> 11A5<>
RAM_DATA_B<54>  10C2<> 11A5<>
RAM_DATA_B<55>  10C2<> 11A5<>
RAM_DATA_B<56>  10C2<> 11A3<>
RAM_DATA_B<63..56>  36A5>
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RAM_DATA_B<58>  10C1<> 11A3<>
RAM_DATA_B<59>  10C2<> 11A3<>
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RAM_DATA_B<61>  10C2<> 11A5<>
RAM_DATA_B<62>  10C2<> 11A5<>
RAM_DATA_B<63>  10C2<> 11A5<>
RAM_DQM_A<0>    10B8<> 11C5<> 36C5>
RAM_DQM_A<1>    10C7<> 11D6<> 36C5>
RAM_DQM_A<2>    10B6<> 11C6<>
RAM_DQM_A<3..2>  36B5>
RAM_DQM_A<3>    10C5<> 11C6<>
RAM_DQM_A<4>    10B4<> 11B6<>
RAM_DQM_A<5..4>  36B5>
RAM_DQM_A<5>    10C3<> 11A6<>
RAM_DQM_A<6>    10B2<> 11A6<> 36B5>
RAM_DQM_A<7>    10C1<> 11A6<> 36A5>
RAM_DQM_B<0>    10C8<> 11D5<> 36C5>
RAM_DQM_B<1>    10C8<> 11D5<> 36C5>
RAM_DQM_B<2>    10C6<> 11C5<>
RAM_DQM_B<3..2>  36B5>
RAM_DQM_B<3>    10C6<> 11C5<>
RAM_DQM_B<4>    10C4<> 11B5<>
RAM_DQM_B<5..4>  36B5>
RAM_DQM_B<5>    10C4<> 11B5<>
RAM_DQM_B<6>    10C2<> 11A5<> 36B5>
RAM_DQM_B<7>    10C2<> 11A5<> 36A5>
RAM_DQS_A<0>    10B8<> 11D8<> 36C5>
RAM_DQS_A<1>    10C7<> 11D8<> 36C5>
RAM_DQS_A<2>    10B6<> 11C8<>
RAM_DQS_A<3..2>  36B5>
RAM_DQS_A<3>    10C5<> 11C8<>
RAM_DQS_A<4>    10B4<> 11B8<>
RAM_DQS_A<5..4>  36B5>
RAM_DQS_A<5>    10C3<> 11A8<>
RAM_DQS_A<6>    10B2<> 11A8<> 36B5>
RAM_DQS_A<7>    10C1<> 11A8<> 36A5>
RAM_DQS_B<0>    10C8<> 11D3<> 36C5>
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RAM_DQS_B<2>    10C6<> 11C3<>
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RAM_DQS_B<3>    10C6<> 11C3<>
RAM_DQS_B<4>    10C4<> 11B3<>
RAM_DQS_B<5..4>  36B5>
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RAM_DQS_B<6>    10C2<> 11A3<> 36B5>
RAM_DQS_B<7>    10C2<> 11A3<> 36A5>
RAM_RAS_L       9A4< 11B5<> 11B6<> 36A5>
RAM_WE_L        9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN  24D6<> 39C1>
RIGHT_USB_DM    26A3< 32A7<> 37A2> 39D1>
RIGHT_USB_DP    26A3< 32A7<> 37A2> 39D1>
RJ45_CD_PD      27B2<>
RJ45_C1_PD      27B2<>
RJ45_C2_PD      27B2<>
RJ45_C3_PD      27B2<>
RJ45_DN<0>      27B2<> 37D2> 39B3>
RJ45_DN<1>      27B2<> 37D2> 39B3>
RJ45_DN<2>      27B2<> 37D2> 39A3>
RJ45_DN<3>      27B2<> 37D2> 39A3>
RJ45_DP<0>      27B2<> 37D2> 39B3>
RJ45_DP<1>      27B2<> 37D2> 39B3>
RJ45_DP<2>      27B2<> 37D2> 39A3>
RJ45_DP<3>      27B2<> 37D2> 39A3>
ROM_CS_L        9B3< 12A5< 24B6<> 39B1>
ROM_OE_L        9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
ROM_RW_L        9B3< 12A5< 24C6<> 39B1>
ROM_WP_L        9B3<
RSDM3_TP        26C5>
RSDM4_TP        26C5>
RSDM5_TP        26C5>
RSDP3_TP        26C5>
RSDP4_TP        26C5>
RSDP5_TP        26C5>
RUN_OR_AC       29C6<>
SI_A2           20B7<
SI_DDC_CLK      19C5<> 20B7<
SI_DDC_DATA     19C5<> 20B7<
SI_EDGE         20B7<
SI_MSEN         20B5<>
SI_PD           20B7<
SI_RST          20B7<
SI_TMDS_CLKN    20B5<> 20C4<
SI_TMDS_CLKP    20B5<> 20C4<
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SI_TMDS_DP<1>   20B5<> 20C4<
SI_TMDS_DP<2>   20A5<> 20B4<
SI_VREF         20A5< 20A7<
SLEEP           23C4<> 25C6<> 30B6<> 30D7< 33A4<
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SLEEP_LED       23C1< 25C7<> 39B6>
SLEEP_LED_I     23D1<
SLEEP_LED_L     23D2<
SLEEP_LED_SW_L  23C2<>
SLEEP_LED_UF    23C1<
SLEEP_LS5       33A5<> 33A8<
SLEEP_LS5_EN_L  33A5<>
SLEEP_L_LS5     19A7<> 27A8<> 33A5<> 34C8<> 35C8<
SLEEP_L_LS5_EN_L  33A6<>
SLEEP_L_LS5_INV  35A3< 35C2< 35C8<>
SLEEP_L_LS5_NET  33B3<> 35C8<>
SLEEP_NET       33A3<>
SLEEP_NET_INV   33A3<>
SMC_TP          26B5<
SND_AGND        25C7<> 38B6>
SND_AMP_MUTE    25C8< 25D6<> 39A4>
SND_AMP_MUTE_F  25C7< 25D6<>
SND_AMP_MUTE_L  14C5<> 25D5<>
SND_CLKOUT      14B1< 25D8< 36B1> 39D6>
SND_CLKOUT_F    25C7<> 25D7<
SND_HP_MUTE     25C5<>
SND_HP_MUTE_INV  25C5<> 25C6<> 39A4>
SND_HP_MUTE_L   14C5<> 25C4<>
SND_HP_SENSE_L  14B5<> 25D6<> 39C6>
SND_HW_RESET_L  14A7< 14B5<> 25C8< 39C6>
SND_HW_RESET_L_F  25C6<> 25C7<
SND_LIN_SENSE_L  14B5<> 25D6<> 39C6>
SND_SCLK        14B1< 25C8< 36B1> 39C6>
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SND_SCLK_F      25C7< 25D7<>
SND_SYNC        14B1< 25D8< 39D6>
SND_SYNC_F      25C7<> 25D7<
SND_TO_AUDIO    14B1< 25D8< 39D6>
SND_TO_AUDIO_F  25D6<> 25D7<
SOFT_PWR_ON_L   22D1< 23A8< 30A8< 30C6<> 30D7<
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SRCLK_TP        26A5> 39A4>
SRMOD_TP        26A5< 39A4>
ST7_ICP_SEL_PD  23A2< 23D6<
ST7_KBD_LED_OUT  23A4< 23C4<>
ST7_OSC1        23D5<
ST7_OSC2        23D5<>
ST7_PB6_PD      23B2< 23C4<>
ST7_RESET_L     23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23B4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN     23C5<
STOP_AGP_L      12D2< 12D4<>
SUPPLY_M_DM     25B6< 25B8<
SUPPLY_M_MP     25B6< 25B8<
SUTRO_ALS_GAIN_SW  23C4<> 24B2<> 39C2>
SUTRO_ALS_OUT   23C4<> 24B2<> 39C2>
SYSCLK_CPU      5C3< 8A6< 36D1>
SYSCLK_CPU_UF   8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 36D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
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SYSTEM_CLK_EN   14A5< 14B7< 30C4<>
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TEST_TP         26A5< 39A4>
THERM1_A_DM     25A6< 25A8< 37A2>
THERM1_A_DP     25A6< 25A8< 37A2>
THERM1_DM       25A5< 25B5< 25B5<> 37A2>
THERM1_DP       25A5< 25B5< 25B5<> 37A2>
THERM1_M_DM     37A2>
THERM1_M_DP     37A2>
THERM2_A_DM     25A6< 25A8< 37A2>
THERM2_A_DP     25A6< 25A8< 37A2>
THERM2_DM       25A5< 25B5< 25B5<> 37A2>
THERM2_DP       25A5< 25B5< 25B5<> 37A2>
THERM2_M_DM     37A2>
THERM2_M_DP     37A2>
THERM_INV       25A5<>
THERM_L_OC      25A4<> 30B4<>
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TMDS_CLKP       20B3< 20C2< 20C3< 22C7<> 37B2>
TMDS_CLK_CMF    20C1<
TMDS_CONN_CLKN  22B6<> 22C7<> 37B2> 39A8>
TMDS_CONN_CLKP  22C6<> 22C7<> 37B2> 39D7>
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TMDS_CONN_DN<2>  22B6<> 22D5<>
TMDS_CONN_DP<0>  22B7<> 22D6<>
TMDS_CONN_DP<1>  22B7<> 22D5<>
TMDS_CONN_DP<2>  22B6<> 22D5<>
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TMDS_D1_CMF     20B1<
TMDS_D2_CMF     20A1<
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                39A8>
TMDS_DN<2>      20A1< 20A3< 20B3< 22B7<> 37B2>
                39A8>
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TMDS_DP<1>      20A3< 20B2< 20C3< 22B8<> 37B2>
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TMDS_DP<2>      20A2< 20A3< 20B3< 22B7<> 37B2>
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TPAD_F_TXD      23A7<> 39C4>
TPAD_RXD        23A8< 30C2< 30C4<>
TPAD_TXD        23A8< 30B2< 30C4<>
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TV_COMP         22A6<> 39D6>
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TV_GND2         22A6<> 38B6> 39A7>
TV_Y            22A6<> 39D6>
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UIDE_DATA<7>    13D7<> 24C4< 37C5>
UIDE_DATA<8>    13D7<> 24C4<
UIDE_DATA<15..8>  37C5>
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UIDE_DATA<10>   13D7<> 24C4<
UIDE_DATA<11>   13D7<> 24D4<
UIDE_DATA<12>   13D7<> 24B4<
UIDE_DATA<13>   13D7<> 24B4<
UIDE_DATA<14>   13D7<> 24C4<
UIDE_DATA<15>   13D7<> 24B4<
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UIDE_DIOW_L     13C7<> 24A4< 37C5>
UIDE_DMACK_L    13C7<> 24A4< 37C5>
UIDE_DMARQ      13C7<> 37C5>
UIDE_INTRQ      13C7< 37C5>
UIDE_IOCHRDY    13C7< 24A4< 37C5>
UIDE_REF        13C7<> 38D3>
UIDE_RST_L      13C7<> 24A4< 37C5>
USB2_PCI_GNT_L  12C7<> 26B7<
USB2_PCI_INT_L  14B5<> 14C7< 26A8<
USB2_PCI_REQ_L  12A7< 12D7<> 26B7>
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USB_D1P         14C1< 26A4< 26A5>
USB_D2M         14D1< 26A4< 26A5>
USB_D2P         14D1< 26A4< 26A5>
USB_DAM         14B2<> 14D2< 26A5>
USB_DAP         14B2<> 14D2< 26A5>
USB_DBM         14B2<> 14D2<
USB_DBP         14B2<> 14D2<
USB_DCM         14B2<> 14C2< 26A5>
USB_DCP         14B2<> 14C2< 26A5>
USB_DDM         14B2<> 14C2<
USB_DDP         14B2<> 14C2<
USB_DEM         14B2< 14B2<> 37B2>
USB_DEP         14B2<> 14C2< 37B2>
USB_DFM         14B2< 14B2<> 37B2>
USB_DFP         14B2< 14B2<> 37B2>
USB_OC_AB_L     14B2< 14C7<
USB_OC_CD_L     14B2< 14C7<
USB_OC_EF_L     14B2< 14D7<
USB_PWREN_AB_L  14B2<> 14C7<
USB_PWREN_CD_L  14B2<> 14C7<
USB_PWREN_EF_L  14B2<> 14D7<
VCORE_BOOST     34C4<> 38C1>
VCORE_BST       34C5<> 38C1>
VCORE_CC        34B6<> 38B1>
VCORE_CNTL_RC   19A3<>
VCORE_DH        34B5<> 38C1>
VCORE_DL        34B5<> 38C1>
VCORE_FAST<1>   34D3< 34D5<
VCORE_FAST<2>   34D3< 34D5<
VCORE_FAST<3>   34D3< 34D5<
VCORE_FAST<4>   34D3< 34D5<
VCORE_FB        34B5< 38B1> 39A2>
VCORE_GND       34B5<> 38B1>
VCORE_GNDA      34B6<>
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VCORE_GNDDIV    34A4< 34B5< 38B1>
VCORE_GNDDIV_TEST  34A3<>
VCORE_GNDGNS    34A2<> 34A4< 38B1>
VCORE_GNDSNS_TEST  34A3<>
VCORE_ILIM      34C6<> 38C1>
VCORE_LX        34B5<> 38C1>
VCORE_MUX_EN    34D5<> 39A2>
VCORE_MUX_SEL   34D5<>
VCORE_REF       34B6<> 38C1>
VCORE_SEL_OFF_PU  34B6<>
VCORE_SEL_ON    34B6<>
VCORE_SHDN_L    34C6<>
VCORE_SLOW<1>   34D6<
VCORE_SLOW<2>   34D6<
VCORE_SLOW<3>   34D6<
VCORE_SLOW<4>   34D6<
VCORE_SNS       34A1<> 38B1>
VCORE_TIME      34B4<> 38B1>
VCORE_TON       34B6< 38C1>
VCORE_VCC       34C6< 38C1>
VCORE_VGATE     14B5< 14B7< 34B4> 38B1>
VCORE_VID0      39A3>
VCORE_VID1      39A3>
VCORE_VID2      39A3>
VCORE_VID3      39A3>
VCORE_VID4      39A3>
VCORE_VID<0>    34A2<> 34B8<
VCORE_VID<1>    34A2<> 34B8< 34D4<>
VCORE_VID<2>    34A2<> 34B8< 34D4<>
VCORE_VID<3>    34A2<> 34B8< 34D4<>
VCORE_VID<4>    34A2<> 34B8< 34D4<>
VGA_B           22C6<> 22D7< 39D7>
VGA_G           22C5<> 22D7< 39D7>
VGA_HSYNC       22C6<> 22C7< 39D7>
VGA_HSYNC_BUF   22C8<>
VGA_R           22C5<> 22D7< 39D7>
VGA_VSYNC       22C5<> 22C7< 39D7>
VGA_VSYNC_BUF   22C8<>
ZV_LCDDATA20_PU  19C7<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

BS1 PCB_STANDOFF 4
C1 CAP 22
C2 CAP 34
C3 CAP 34
C4 CAP 34
C5 CAP 34
C6 CAP 34
C7 CAP 34
C8 CAP 5
C9 CAP 16
C10 CAP 16
C11 CAP 18
C12 CAP 5
C13 CAP 34
C14 CAP 20
C15 CAP 14
C16 CAP 16
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