

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# M42C MLB

11/27/2006 POST RAMP WITH LOCKED BOOTROM

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
C		474680	PRODUCTION RELEASED	11/27/06	?

Page	(.csa)	Contents	DRI	Sync	Date
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4	4	CONFIGURATION OPTIONS	RX	SMC	07/18/2005
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9	9	CPU DECAPS & VID<>	MK	SMC	08/19/2005
10	10	CPU MISC1-TEMP SENSOR	ES	ENET	08/19/2005
11	11	CPU ITP700FLEX DEBUG	RX	MASTER	5/23/05
12	12	NB CPU Interface	MK	NB	07/25/2005
13	13	NB PEG / Video Interfaces	DK	NB	07/25/2005
14	14	NB Misc Interfaces	RX	NB	08/15/2005
15	15	NB DDR2 Interfaces	LT	NB	07/25/2005
16	16	NB Power 1	DK	NB	07/25/2005
17	17	NB Power 2	DK	NB	07/25/2005
18	18	NB Grounds	DK	NB	07/25/2005
19	19	NB (GM) Decoupling	DK	NB	06/22/2005
20	20	NB Config Straps	DK	NB	06/28/2005
21	21		RX	SB	08/05/2005
22	22		RX	ENET	11/16/2005
23	23		RX	ENET	11/28/2005
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26	26	SB Misc	RX	NB	07/26/2005
27	27	M42 SMBUS CONNECTIONS	ES	ENET	08/30/2005
28	28	DDR2 SO-DIMM Connector A	LT	MEMORY	06/20/2005
29	29	DDR2 SO-DIMM Connector B	LT	MEMORY	06/20/2005
30	30	Memory Active Termination	LT	MEMORY	06/20/2005
31	31	Memory Vtt Supply	LT	(MASTER)	(MASTER)
32	32	CLOCKS	DK	CLOCK	06/03/2005
33	33	CLOCK TERMINATION	DK	CLOCK	06/06/2005
34	34	PATA CONNECTOR	ES	ENET	11/01/2005
35	35	SATA CONNECTOR	ES	ENET	11/14/2005
36	36	ETHERNET CONTROLLER	ES	ENET	12/06/2005
37	37	ETHERNET CONNECTOR	ES	ENET	11/14/2005
38	38	FIREWIRE CONTROLLER	ES	ENET	08/30/2005
39	39	FIREWIRE PORT	ES	ENET	11/16/2005
40	40	CONNECTOR MISC	ES	ENET	11/16/2005
41	41	IR CONTROLLER	ES	ENET	11/09/2005
42	42		ES	ENET	11/01/2005
43	43		ES	ENET	08/19/2005
44	44	BLUETOOTH INTERFACE	MK	ENET	08/29/2005
45	45	SMC	MK	SMC	08/18/2005
46	46	SMC SUPPORT	LD	SMC	08/23/2005
47	47	LPC+ Debug Connector	MK	NB	06/30/2005
48	48	CPU Current & Voltage Sense	ES	ENET	08/30/2005

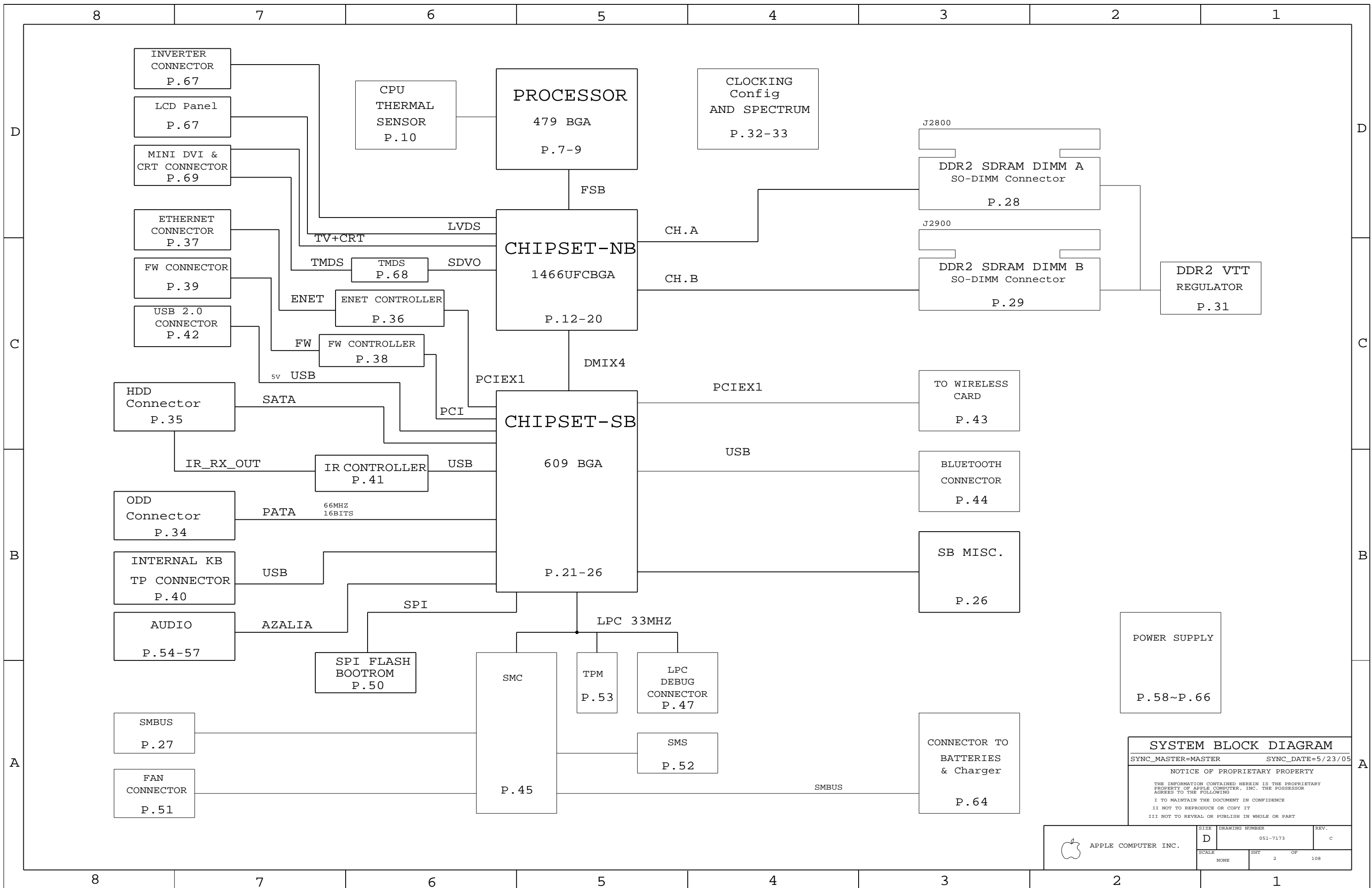
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50	50	SPI BOOTROM	ES	MASTER	5/23/05
51	51	Fan	MK	ENET	11/10/2005
52	52	SMS	RX	SMC	08/23/2005
53	53	TPM	DK	SMC	07/18/2005
54	54	AUDIO: CODEC	DK	M42AUDIO	08/05/2006
55	55	AUDIO: SPEAKER AMP	DK	M42AUDIO	08/05/2006
56	56	AUDIO: JACK	DK	M42AUDIO	08/05/2006
57	57	AUDIO: JACK TRANSLATORS	MK	M42AUDIO	08/05/2006
58	58	IMVP6 CPU VCore Regulator	MK	POWER	07/13/2005
59	59	5V / 3.3V Power Supply	MK	POWER	07/13/2005
60	60	2.5V/1.2V Regulator	MK	ENET	12/06/2005
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65	65	DC-In & Battery Connectors	MK	POWER	07/13/2005
66	66	PBUS Supply/Battery Charger	ES	SMC	08/19/2005
67	67	INVERTER, LVDS, TMDS	DK	GRAPHIC	06/06/2005
68	68	EXTERNAL TMDS	DK	GRAPHIC	06/06/2005
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70	70	Cross Reference Page			
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EE DRIS:  
 RX-RAYMOND XU  
 DK-DINESH KUMAR  
 RC-RAY CHANG  
 MK-MARC KLINGELHOFER  
 LT-LAWRENCE TAN  
 ES-ERIC SMITH  
 LD-LINDA DUNN

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7173	1	SCHEM, MACBOOK, MLB	SCH	
820-1889	1	PCBF, MACBOOK, MLB	PCB	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7173	REV. C
					SHT 1 OF 108



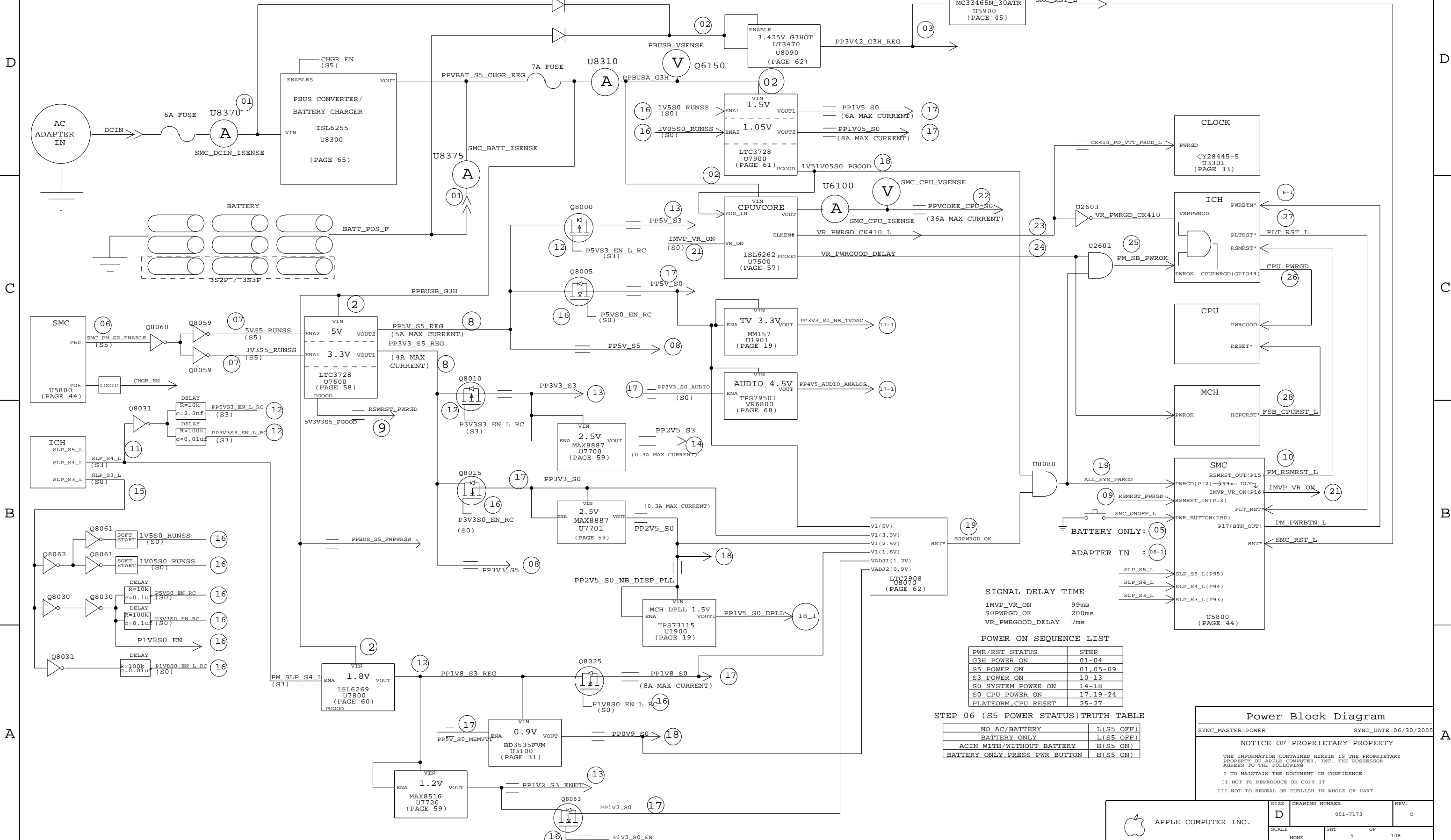
**SYSTEM BLOCK DIAGRAM**

SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	2	108	

# M42A POWER SYSTEM ARCHITECTURE



**SIGNAL DELAY TIME**

IMVP_VR_ON	99ms
SOPWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

**POWER ON SEQUENCE LIST**

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

**STEP 06 (S5 POWER STATUS) TRUTH TABLE**

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

**Power Block Diagram**

SYNC\_MASTER=POWER SYNC\_DATE=06/30/2005

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SIZE	DRAWING NUMBER	REV.
D	051-7173	c
SCALE	SHT	OF
NONE	3	108

Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	v	v	v	v	v	v
5V3V3S3_CONT						
5V3V3S3_SKIP	v	v	v	v	v	v
ACCEL_KIONIX			v	v	v	
ACCEL_ST	v	v				v
INVERTER_BUF	v	v	v	v	v	v
INVERTER_UNBUF						
ITP						
LEMENU	v	v	v	v	v	v
MEMVIT_EN_PU	v	v	v	v	v	v
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	v	v	v	v	v	v
USB_D_OC_PU	v	v	v	v	v	v
USB_E_OC_PU	v	v	v	v	v	v
GOOD	v			v		
BETTER		v			v	
BEST			v			v
M42A_PGM	v	v	v	v	v	v
ONEWIRE_PULLUP	v	v	v	v	v	v
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	v	v	v	v	v	v
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	v	v	v	v	v	v
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	v	v	v	v	v	v
3V3_IND_3MM						
NORMAL	v	v		v	v	
FANCY			v			v
STANDOFF	v	v	v	v	v	v
FET_FDN6296	v	v	v	v	v	v
FET_STL8NH3LL						
GOOD-ST	v					
BETTER-ST		v				
BEST-KIONIX			v			
GOOD-KIONIX				v		
BETTER-KIONIX					v	
BEST-ST						v
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	v	v	v	v	v	v
M42						
M42A	v	v	v	v	v	v

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

MLB STACKUP		
LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT		
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3387	1	IC, MEMOM, CPU B2 DC 1.83GHZ, 479 PGA	U0700	GOOD
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BETTER
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC, FW32306, 1394A LINK, BGA, 129P	U4400	LEMENU
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	LEMENU
359S0109	1	IC, SLOBLP436, CLOCK GEN, 68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1942	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, 802CE	U6301	M42A_PGM
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, 808	U4102	M42A_PGM
341S1946	1	IC, SMC, 176P BGA, MS8/2116	U5800	M42A_PGM
341S1890	1	IC, PSOC-W/USB, 56P, MLP, CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WES	CRITICAL	GOOD-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WET	CRITICAL	BETTER-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEW	CRITICAL	BEST-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEV	CRITICAL	GOOD-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:W6V	CRITICAL	BETTER-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEU	CRITICAL	BEST-ST

CONFIGURATION OPTIONS

SYNC\_MASTER=SMC SYNC\_DATE=07/18/2005

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	D	051-7173	C
	SCALE	SHT	OF
	NONE	4	108

# Functional Test Points

## Power Supply NO\_TESTS

NO_TEST	TEST	VALUE
	IMVP6_RBIAS	58
	IMVP6_COMP	58
	5VS5_RUNSS	59 63
	1V5S0_RUNSS	52 63
	1V8S3_COMP	61
	1V8S3_FSET	61
	TRUE 3V3S5_COMP	
	TRUE 3V3S5_FSET	
	TRUE 1V05S0_COMP	
	TRUE 1V05S0_FSET	
	TRUE P3V42G3H_FB	63

## CLOCK NO\_TESTS

NO_TEST	TEST	VALUE
	TRUE CK410_CPU0_N	32 33
	TRUE CK410_CPU0_P	32 33
	TRUE CK410_CPU1_N	32 33
	TRUE CK410_CPU1_P	32 33
	TRUE CK410_CPU2_ITP_SRC10_N	32 33
	TRUE CK410_CPU2_ITP_SRC10_P	32 33
	TRUE CK410_DOT96_27M_N	32 33
	TRUE CK410_DOT96_27M_P	32 33
	TRUE CK410_LVDS_N	32 33
	TRUE CK410_LVDS_P	32 33
	TRUE CK410_PCI4_CLK_SPN	
	TRUE CK410_PCF1_CLK	32 33
	TRUE CK410_SRC1_N_SPN	6
	TRUE CK410_SRC1_P_SPN	6
	TRUE CK410_SRC2_N	32 33
	TRUE CK410_SRC2_P	32 33
	TRUE CK410_SRC3_N_SPN	6
	TRUE CK410_SRC3_P_SPN	6
	TRUE CK410_SRC4_N	32 33
	TRUE CK410_SRC4_P	32 33
	TRUE CK410_SRC5_N	32 33
	TRUE CK410_SRC5_P	32 33
	TRUE CK410_SRC6_N	32 33
	TRUE CK410_SRC6_P	32 33
	TRUE CK410_SRC7_N_SPN	6
	TRUE CK410_SRC7_P_SPN	6
	TRUE CK410_SRC8_N	32 33
	TRUE CK410_SRC8_P	32 33
	TRUE CK410_SRC_CLKREQ01_L_SPN	6
	TRUE CK410_SRC_CLKREQ03_L_SPN	6
	TRUE CK410_SRC_CLKREQ08_L	32 33

## FIREWARE NO\_TESTS

NO_TEST	TEST	VALUE
	TRUE FW_B_TPA_N_SPN	6
	TRUE FW_B_TPA_P_SPN	6
	TRUE FW_B_TPBIAS_SPN	6
	TRUE FW_B_TPB_N_SPN	6
	TRUE FW_B_TPB_P_SPN	6
	TRUE FW_C_TPA_N_SPN	6
	TRUE FW_C_TPA_P_SPN	6
	TRUE FW_C_TPBIAS_SPN	6
	TRUE FW_C_TPB_N_SPN	6
	TRUE FW_C_TPB_P_SPN	6

## LVDS NO\_TESTS

NO_TEST	TEST	VALUE
	TRUE LVDS_B_CLK_N_SPN	6
	TRUE LVDS_B_CLK_P_SPN	6
	TRUE LVDS_B_DATA_N0_SPN	6
	TRUE LVDS_B_DATA_N1_SPN	6
	TRUE LVDS_B_DATA_N2_SPN	6
	TRUE LVDS_B_DATA_P1_SPN	6
	TRUE LVDS_B_DATA_P2_SPN	6

## ETHERNET NO\_TESTS

NO_TEST	TEST	VALUE
	TRUE ENET_MDI_TRAN_P<2>	37
	TRUE ENET_MDI_TRAN_N<2>	37
	TRUE ENET_MDI_TRAN_P<3>	37

NO_TEST	TEST	VALUE
	TRUE SMC_FAN_3_TACH	45 46
	TRUE ALS_LEFT	45 46

## Fan Connectors

FUNC_TEST	TEST	VALUE
	TRUE =PP5V_S0_FAN_RT	51 64
	TRUE FAN_RT_PWM	51
	TRUE FAN_RT_TACH	51
	TRUE =PP3V3_S0_FAN_RT	51 64
	TRUE SMC_FAN_1_CTL	45 51
	TRUE SMC_FAN_1_TACH	45 51

## LPC+ Debug Connector

FUNC_TEST	TEST	VALUE
	TRUE =PP3V42_G3H_LPCPLUS	47 64
	TRUE =PP5V_S0_LPCPLUS	47 64
	TRUE LPC_AD<0>	21 45 47 53
	TRUE LPC_AD<1>	21 45 47 53
	TRUE LPC_FRAME_L	21 45 47 53
	TRUE PM_CLKRUN_L	23 38 45 47 53
	TRUE BOOT_LPC_SPI_L	22 45 47
	TRUE SMC_TMS	45 46 47
	TRUE DEBUG_RST_L	26 47
	TRUE SMC_TRST_L	45 47
	TRUE SMC_TDO	45 46 47
	TRUE SMC_MD1	45 47
	TRUE SMC_TX_L	45 46 47
	TRUE FWH_INIT_L	5 21 47
	TRUE PCI_CLK_PORT80_LPC	33 47
	TRUE LPC_AD<2>	21 45 47 53
	TRUE LPC_AD<3>	21 45 47 53
	TRUE INT_SERIRO	23 45 47 53
	TRUE PM_SUS_STAT_L	23 45 46 47 53
	TRUE SMC_TDI	45 46 47
	TRUE SMC_TCK	45 46 47
	TRUE SMC_RST_L	45 46 47
	TRUE SMC_NMI	45 47
	TRUE SMC_RX_L	45 46 47
	TRUE SV_SET_UP	23 47

## Other Func Test Points

FUNC_TEST	TEST	VALUE
	TRUE =PP1V05_S0_REG	52 64
	SMBus FUNC_TEST	
	TRUE SMBUS_SMC_MLB_SCL	27
	TRUE SMBUS_SMC_MLB_SDA	27
	FIREWIRE FUNC_TEST	
	TRUE PPFW_SWITCH	39
	SLEEP_LED_FUNC_TEST	
	TRUE SYS_LED_ANODE	35 46
	SMC FUNC_TEST	
	TRUE SMC_LID	40 45 46 65
	TRUE SMC_MANUAL_RST_L	46
	TRUE SMC_CPU_VSENSE	45 48
	Power Supply FUNC_TEST	
	TRUE ALL_SYS_PWRGD	26 45 63
	TRUE PPVCORE_CPU_S0	64
	TRUE PP1V05_S0	44
	TRUE PP1V5_S0	44
	TRUE PP1V8_S0	44
	TRUE PP2V5_S0	44
	TRUE PP3V3_S0	44
	TRUE PP5V_S0	44
	TRUE PP1V2_S3	44
	TRUE PP1V8_S3	44
	TRUE PP2V5_S3	44
	TRUE PP3V3_S3	44
	TRUE PP5V_S3	44
	TRUE PP3V3_S5	44
	TRUE PP5V_S5	44
	TRUE PP3V42_G3H	44
	TRUE PPBUSA_G3H	
	TRUE PPBUSB_G3H	44
	TRUE PP18V5_G3H	44
	TRUE PP0V9_S0	44

## Battery Digital Connector

FUNC_TEST	TEST	VALUE
	TRUE SMC_BS_ALRT_L	45 46 65
	TRUE SMBUS_BATT_SCL_F	65
	TRUE SMBUS_BATT_SDA_F	65
	TRUE BATT_IN	
	TRUE BATT_POS	65
	TRUE BATT_NEG	65

## Audio FUNC\_TEST

FUNC_TEST	TEST	VALUE
	TRUE PP5V_S0_AUDIO_PWR	
	TRUE PP5V_S0_AUDIO	
	TRUE GND_AUDIO_PWR	64
	TRUE GND_AUDIO_CODECS	64
	TRUE ACZ_SDATAIN<0>	21 64
	TRUE ACZ_SDATAOUT	21 64
	TRUE ACZ_BITCLK	21 64
	TRUE ACZ_RST_L	21 54 57
	TRUE ACZ_SYNC	21 64

## Battery FUNC\_TEST

FUNC_TEST	TEST	VALUE
	TRUE SMC_BATT_ISET	45 66
	TRUE SMC_BATT_CHG_EN	45 46 66
	TRUE SMC_BC_ACOK	45 46 65 66
	TRUE SMC_PS_ON	39 45 46 65
	TRUE SMC_BATT_TRICKLE_EN_L	45 46 66
	TRUE SYS_ONEWIRE	45 46 65

## USB FUNC\_TEST

FUNC_TEST	TEST	VALUE
	TRUE TP_USBP_E	6
	TRUE TP_USBN_E	6
	TRUE TP_USBP_F	
	TRUE TP_USBN_F	

## DC-JACK FUNC\_TEST

FUNC_TEST	TEST	VALUE
	TRUE ACIN_ENABLE_GATE	65

## Battery charger FUNC\_TEST

FUNC_TEST	TEST	VALUE
	TRUE PPVBAT_G3H_CHGR_OUT	66

## INVERTER CONNECTOR FUNC\_TEST

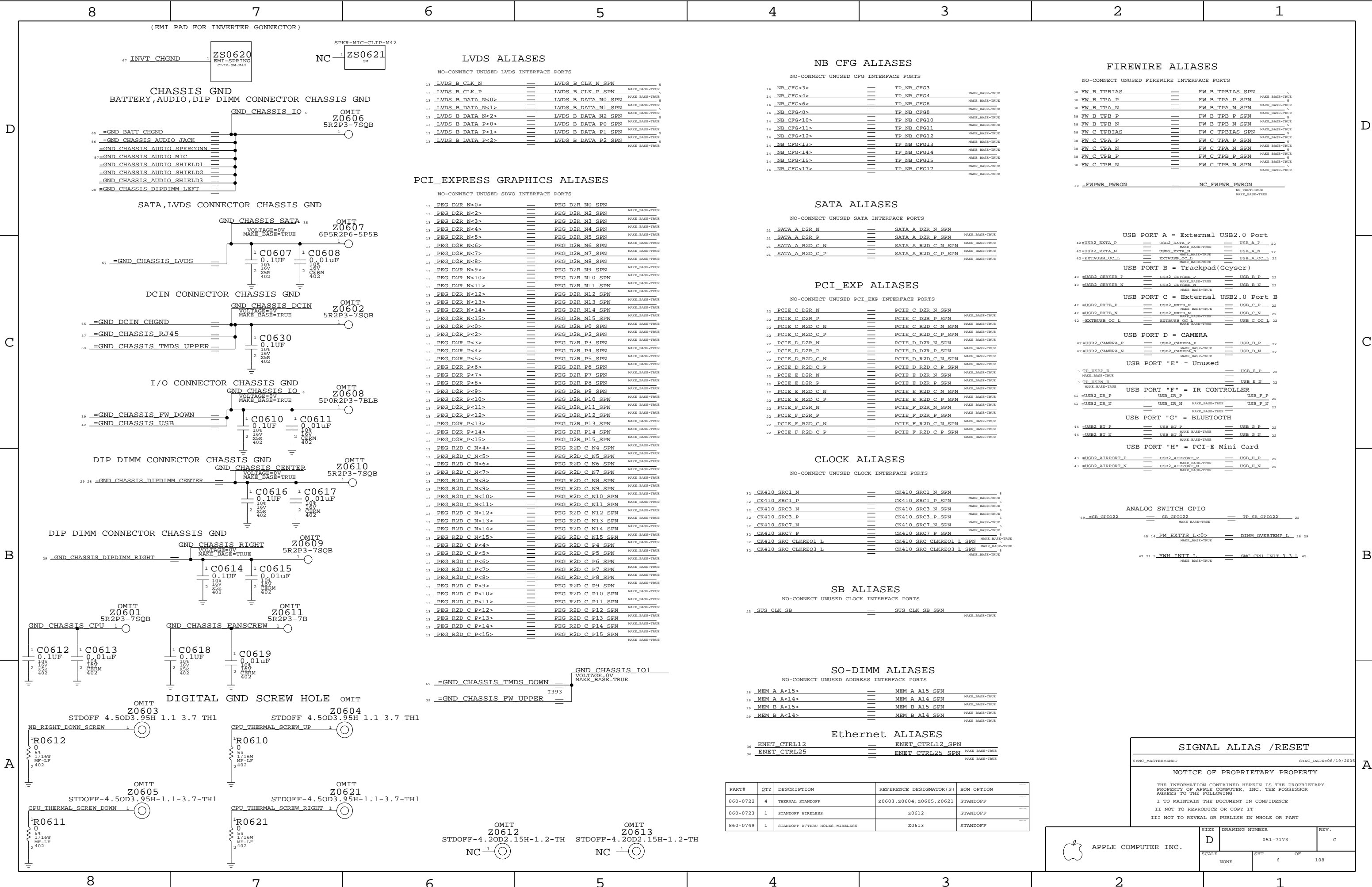
FUNC_TEST	TEST	VALUE
	TRUE PPBUS_ALL_INV_CONN	67
	TRUE INV_GND	67
	TRUE PP5V_INV_F	67
	TRUE INV_BKLIGHT_PWM_L	67

FUNC TEST 1 OF 2

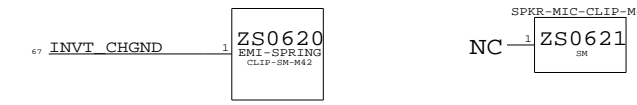
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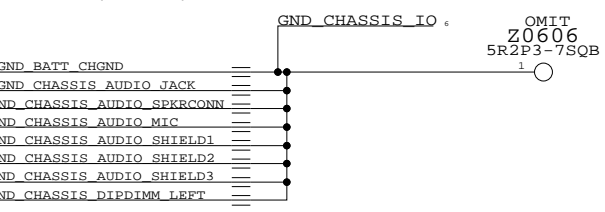
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	5		



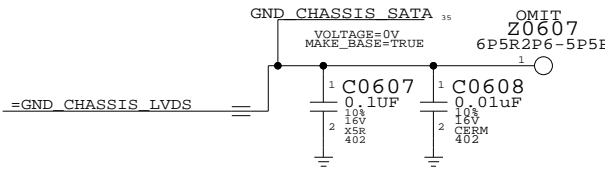
(EMI PAD FOR INVERTER CONNECTOR)



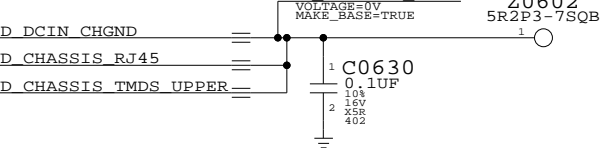
CHASSIS GND  
BATTERY, AUDIO, DIP DIMM CONNECTOR CHASSIS GND



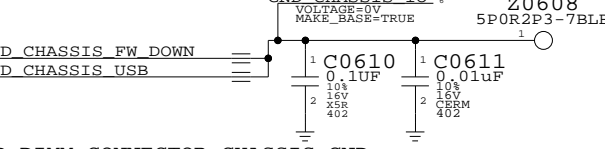
SATA, LVDS CONNECTOR CHASSIS GND



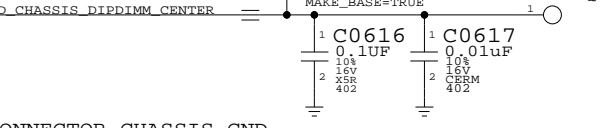
DCIN CONNECTOR CHASSIS GND



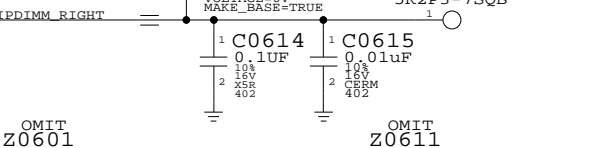
I/O CONNECTOR CHASSIS GND



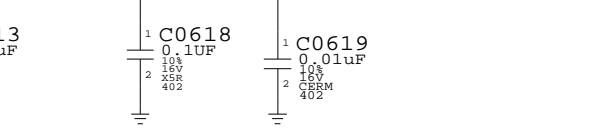
DIP DIMM CONNECTOR CHASSIS GND



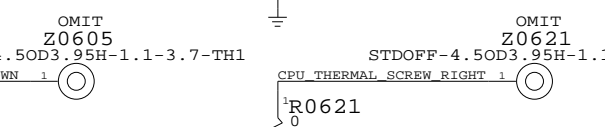
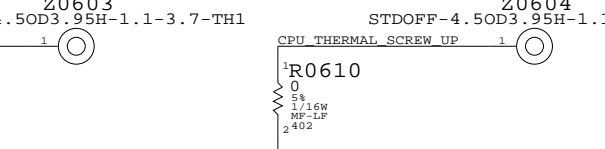
DIP DIMM CONNECTOR CHASSIS GND



DIP DIMM CONNECTOR CHASSIS GND



DIGITAL GND SCREW HOLE



LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

LVDS B CLK N	LVDS B CLK N SPN
LVDS B CLK P	LVDS B CLK P SPN
LVDS B DATA N<0>	LVDS B DATA N0 SPN
LVDS B DATA N<1>	LVDS B DATA N1 SPN
LVDS B DATA N<2>	LVDS B DATA N2 SPN
LVDS B DATA P<0>	LVDS B DATA P0 SPN
LVDS B DATA P<1>	LVDS B DATA P1 SPN
LVDS B DATA P<2>	LVDS B DATA P2 SPN

PCI EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

PEG_D2R N<0>	PEG_D2R N0 SPN
PEG_D2R N<2>	PEG_D2R N2 SPN
PEG_D2R N<3>	PEG_D2R N3 SPN
PEG_D2R N<4>	PEG_D2R N4 SPN
PEG_D2R N<5>	PEG_D2R N5 SPN
PEG_D2R N<6>	PEG_D2R N6 SPN
PEG_D2R N<7>	PEG_D2R N7 SPN
PEG_D2R N<8>	PEG_D2R N8 SPN
PEG_D2R N<9>	PEG_D2R N9 SPN
PEG_D2R N<10>	PEG_D2R N10 SPN
PEG_D2R N<11>	PEG_D2R N11 SPN
PEG_D2R N<12>	PEG_D2R N12 SPN
PEG_D2R N<13>	PEG_D2R N13 SPN
PEG_D2R N<14>	PEG_D2R N14 SPN
PEG_D2R N<15>	PEG_D2R N15 SPN
PEG_D2R P<0>	PEG_D2R P0 SPN
PEG_D2R P<2>	PEG_D2R P2 SPN
PEG_D2R P<3>	PEG_D2R P3 SPN
PEG_D2R P<4>	PEG_D2R P4 SPN
PEG_D2R P<5>	PEG_D2R P5 SPN
PEG_D2R P<6>	PEG_D2R P6 SPN
PEG_D2R P<7>	PEG_D2R P7 SPN
PEG_D2R P<8>	PEG_D2R P8 SPN
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PEG_D2R P<13>	PEG_D2R P13 SPN
PEG_D2R P<14>	PEG_D2R P14 SPN
PEG_D2R P<15>	PEG_D2R P15 SPN
PEG_R2D C N<4>	PEG_R2D C N4 SPN
PEG_R2D C N<5>	PEG_R2D C N5 SPN
PEG_R2D C N<6>	PEG_R2D C N6 SPN
PEG_R2D C N<7>	PEG_R2D C N7 SPN
PEG_R2D C N<8>	PEG_R2D C N8 SPN
PEG_R2D C N<9>	PEG_R2D C N9 SPN
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PEG_R2D C P<12>	PEG_R2D C P12 SPN
PEG_R2D C P<13>	PEG_R2D C P13 SPN
PEG_R2D C P<14>	PEG_R2D C P14 SPN
PEG_R2D C P<15>	PEG_R2D C P15 SPN

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

NB_CFG<3>	TP_NB_CFG3
NB_CFG<4>	TP_NB_CFG4
NB_CFG<6>	TP_NB_CFG6
NB_CFG<8>	TP_NB_CFG8
NB_CFG<10>	TP_NB_CFG10
NB_CFG<11>	TP_NB_CFG11
NB_CFG<12>	TP_NB_CFG12
NB_CFG<13>	TP_NB_CFG13
NB_CFG<14>	TP_NB_CFG14
NB_CFG<15>	TP_NB_CFG15
NB_CFG<17>	TP_NB_CFG17

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

SATA A D2R N	SATA A D2R N SPN
SATA A D2R P	SATA A D2R P SPN
SATA A R2D C N	SATA A R2D C N SPN
SATA A R2D C P	SATA A R2D C P SPN

PCI\_EXP ALIASES

NO-CONNECT UNUSED PCI\_EXP INTERFACE PORTS

PCIE C D2R N	PCIE C D2R N SPN
PCIE C D2R P	PCIE C D2R P SPN
PCIE C R2D C N	PCIE C R2D C N SPN
PCIE C R2D C P	PCIE C R2D C P SPN
PCIE D D2R N	PCIE D D2R N SPN
PCIE D D2R P	PCIE D D2R P SPN
PCIE D R2D C N	PCIE D R2D C N SPN
PCIE D R2D C P	PCIE D R2D C P SPN
PCIE E D2R N	PCIE E D2R N SPN
PCIE E D2R P	PCIE E D2R P SPN
PCIE E R2D C N	PCIE E R2D C N SPN
PCIE E R2D C P	PCIE E R2D C P SPN
PCIE F D2R N	PCIE F D2R N SPN
PCIE F D2R P	PCIE F D2R P SPN
PCIE F R2D C N	PCIE F R2D C N SPN
PCIE F R2D C P	PCIE F R2D C P SPN

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

CK410 SRC1 N	CK410 SRC1 N SPN
CK410 SRC1 P	CK410 SRC1 P SPN
CK410 SRC3 N	CK410 SRC3 N SPN
CK410 SRC3 P	CK410 SRC3 P SPN
CK410 SRC7 N	CK410 SRC7 N SPN
CK410 SRC7 P	CK410 SRC7 P SPN
CK410 SRC_CLKREQ1 L	CK410 SRC_CLKREQ1 L SPN
CK410 SRC_CLKREQ3 L	CK410 SRC_CLKREQ3 L SPN

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

SUS_CLK_SB	SUS_CLK_SB SPN
------------	----------------

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

MEM A A<15>	MEM A A15 SPN
MEM A A<14>	MEM A A14 SPN
MEM B A<15>	MEM B A15 SPN
MEM B A<14>	MEM B A14 SPN

Ethernet ALIASES

ENET_CTRL12	ENET_CTRL12 SPN
ENET_CTRL25	ENET_CTRL25 SPN

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

FW_B TPBIAS	FW_B TPBIAS SPN
FW_B TPA P	FW_B TPA P SPN
FW_B TPA N	FW_B TPA N SPN
FW_B TPB P	FW_B TPB P SPN
FW_B TPB N	FW_B TPB N SPN
FW_C TPBIAS	FW_C TPBIAS SPN
FW_C TPA P	FW_C TPA P SPN
FW_C TPA N	FW_C TPA N SPN
FW_C TPB P	FW_C TPB P SPN
FW_C TPB N	FW_C TPB N SPN
FWPW_PWRON	NC_FWPWR_PWRON

USB PORT A = External USB2.0 Port

USB2_EXTA_P	USB2_EXTA_P	USB_A_P
USB2_EXTA_N	USB2_EXTA_N	USB_A_N
EXTAUSB_OC_L	EXTAUSB_OC_L	USB_A_OC_L

USB PORT B = Trackpad (Geyser)

USB2_GEYSER_P	USB2_GEYSER_P	USB_B_P
USB2_GEYSER_N	USB2_GEYSER_N	USB_B_N

USB PORT C = External USB2.0 Port B

USB2_EXTB_P	USB2_EXTB_P	USB_C_P
USB2_EXTB_N	USB2_EXTB_N	USB_C_N
EXTUSB_OC_L	EXTUSB_OC_L	USB_C_OC_L

USB PORT D = CAMERA

USB2_CAMERA_P	USB2_CAMERA_P	USB_D_P
USB2_CAMERA_N	USB2_CAMERA_N	USB_D_N

USB PORT "E" = Unused

USB2_E_P	USB2_E_P	USB_E_P
USB2_E_N	USB2_E_N	USB_E_N

USB PORT "F" = IR CONTROLLER

USB2_IR_P	USB2_IR_P	USB_F_P
USB2_IR_N	USB2_IR_N	USB_F_N

USB PORT "G" = BLUETOOTH

USB2_BT_P	USB2_BT_P	USB_G_P
USB2_BT_N	USB2_BT_N	USB_G_N

USB PORT "H" = PCI-E Mini Card

USB2_AIRPORT_P	USB2_AIRPORT_P	USB_H_P
USB2_AIRPORT_N	USB2_AIRPORT_N	USB_H_N

ANALOG SWITCH GPIO

SB_GPIO22	SB_GPIO22	TP_SB_GPIO22
-----------	-----------	--------------

PM_EXITS_L<0>	DIMM_OVRTEMP_L
FWH_INIT_L	SMC_CPU_INIT_3_3_L

SIGNAL ALIAS /RESET

SYNC\_MASTER=ENET SYNC\_DATE=08/19/2005

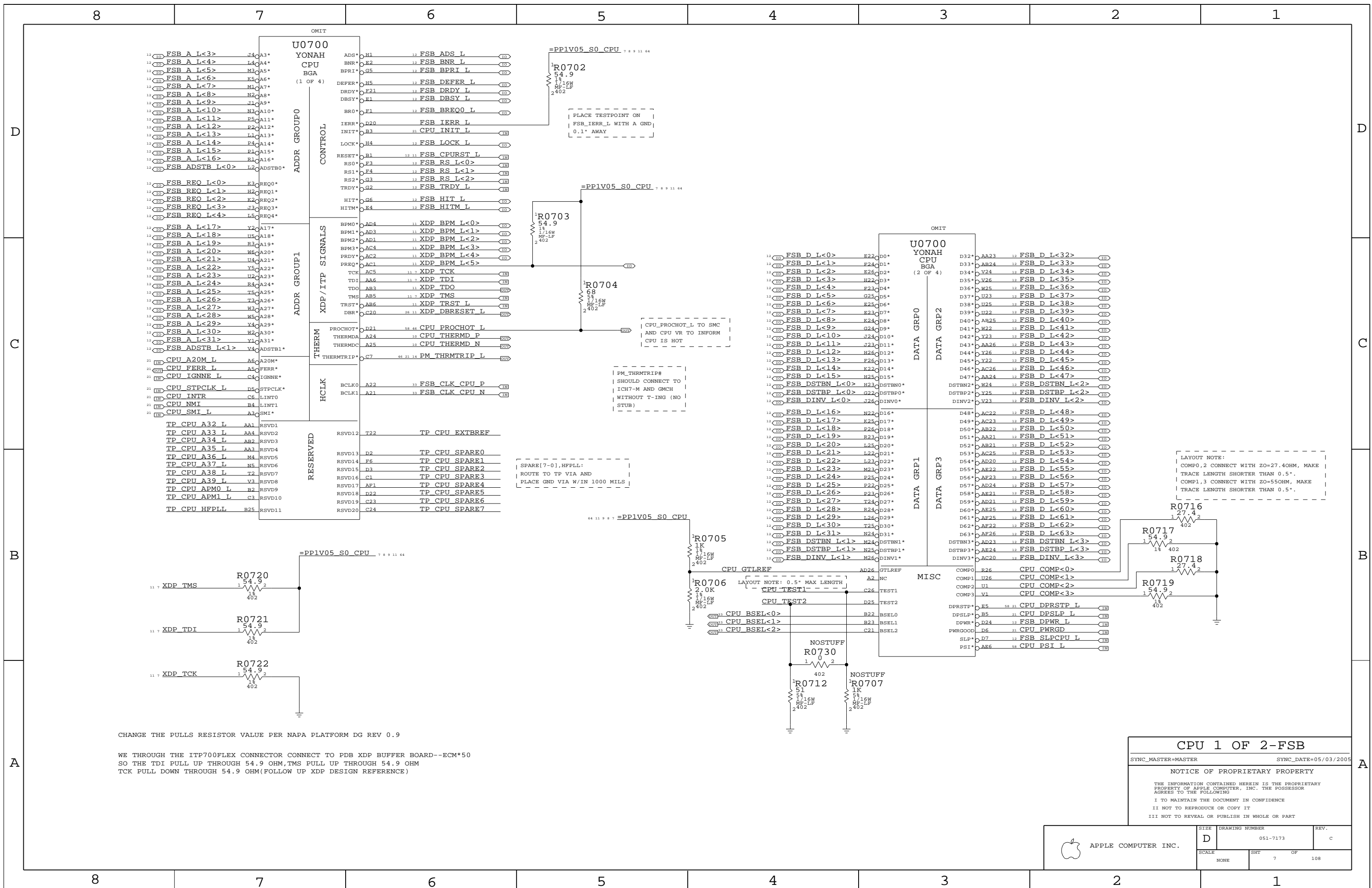
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603, Z0604, Z0605, Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/TWO HOLES, WIRELESS	Z0613	STANDOFF

APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7173	REV.	C
SCALE	NONE	SHT	6	OF	108

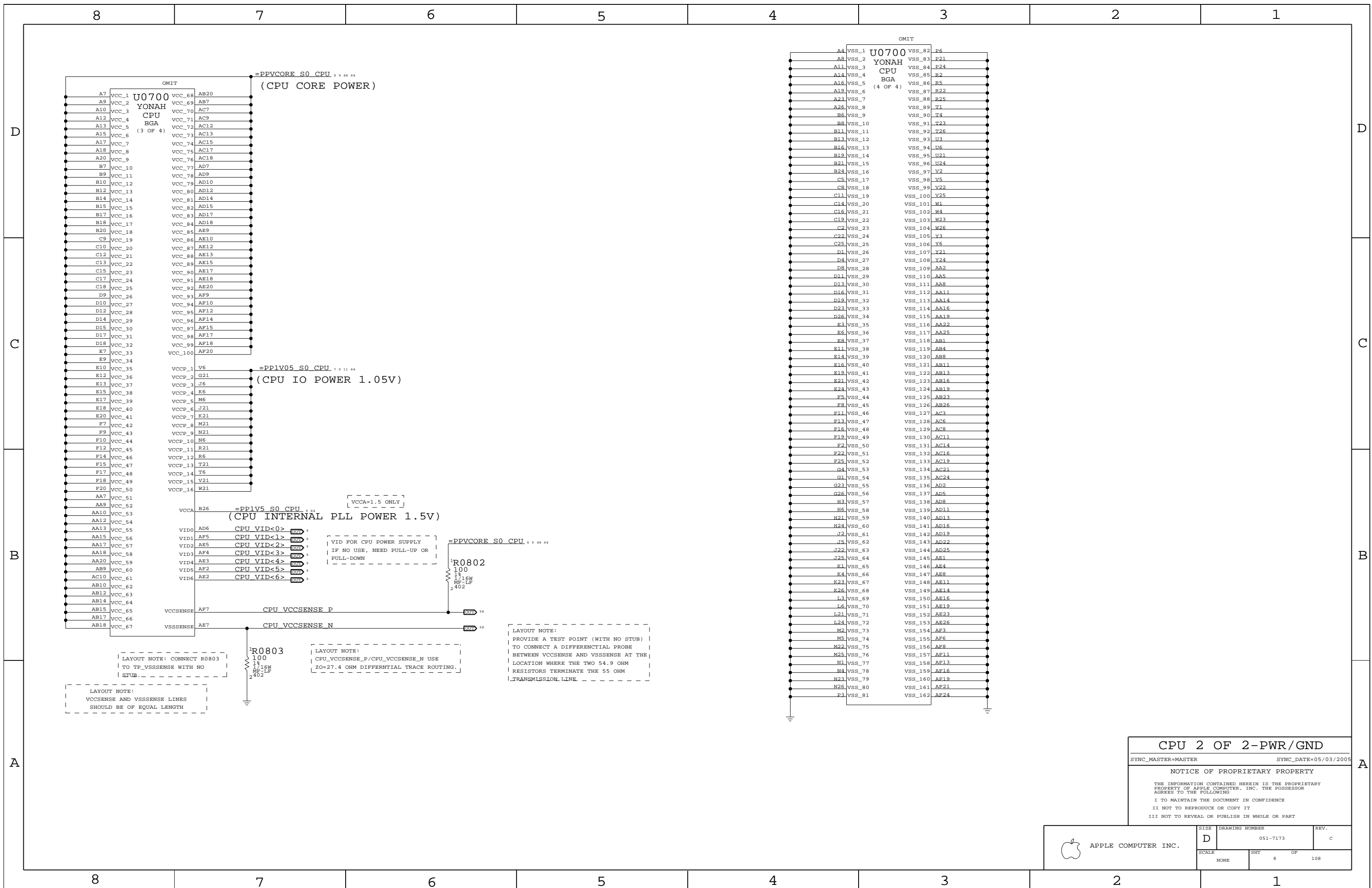


CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM\*50 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

**CPU 1 OF 2-FSB**  
 SYNC\_MASTER=MASTER SYNC\_DATE=05/03/2005  
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	D	051-7173	C
SCALE	SHT	OF	108
NONE	7		



**CPU 2 OF 2-PWR/GND**

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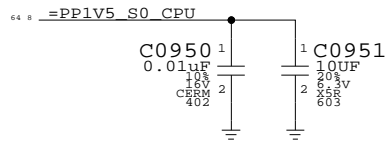
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	SHT	OF	108
NONE	8		

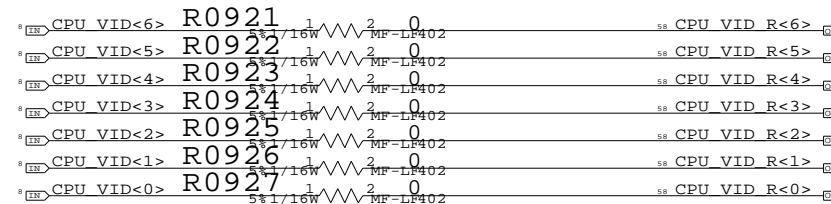


### VCCA DECOUPLING (CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

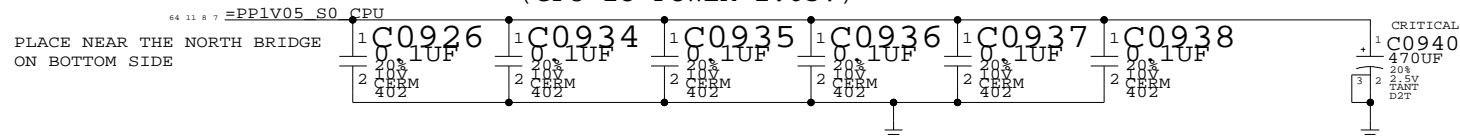
### CPU CORE VID<> SETTINGS



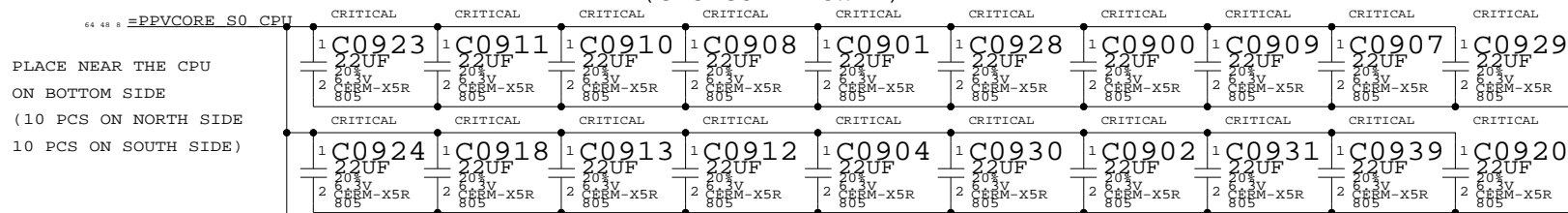
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

### VCCP CORE DECOUPLING (CPU IO POWER 1.05V)

THIS 470UF FOR CPU, GMCH FSB BUS 1.05V



### VCC CORE DECOUPLING (CPU CORE POWER)



IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP

	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM	TBD	TBD
SINGLE CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM	TBD	TBD
DUAL CORE LV CPU	VCCHFM	1.0	1.1625
	VCCLFM	TBD	TBD
ULV CPU	VCCHFM	TBD	TBD
	VCCLFM	TBD	TBD

UNIT: V

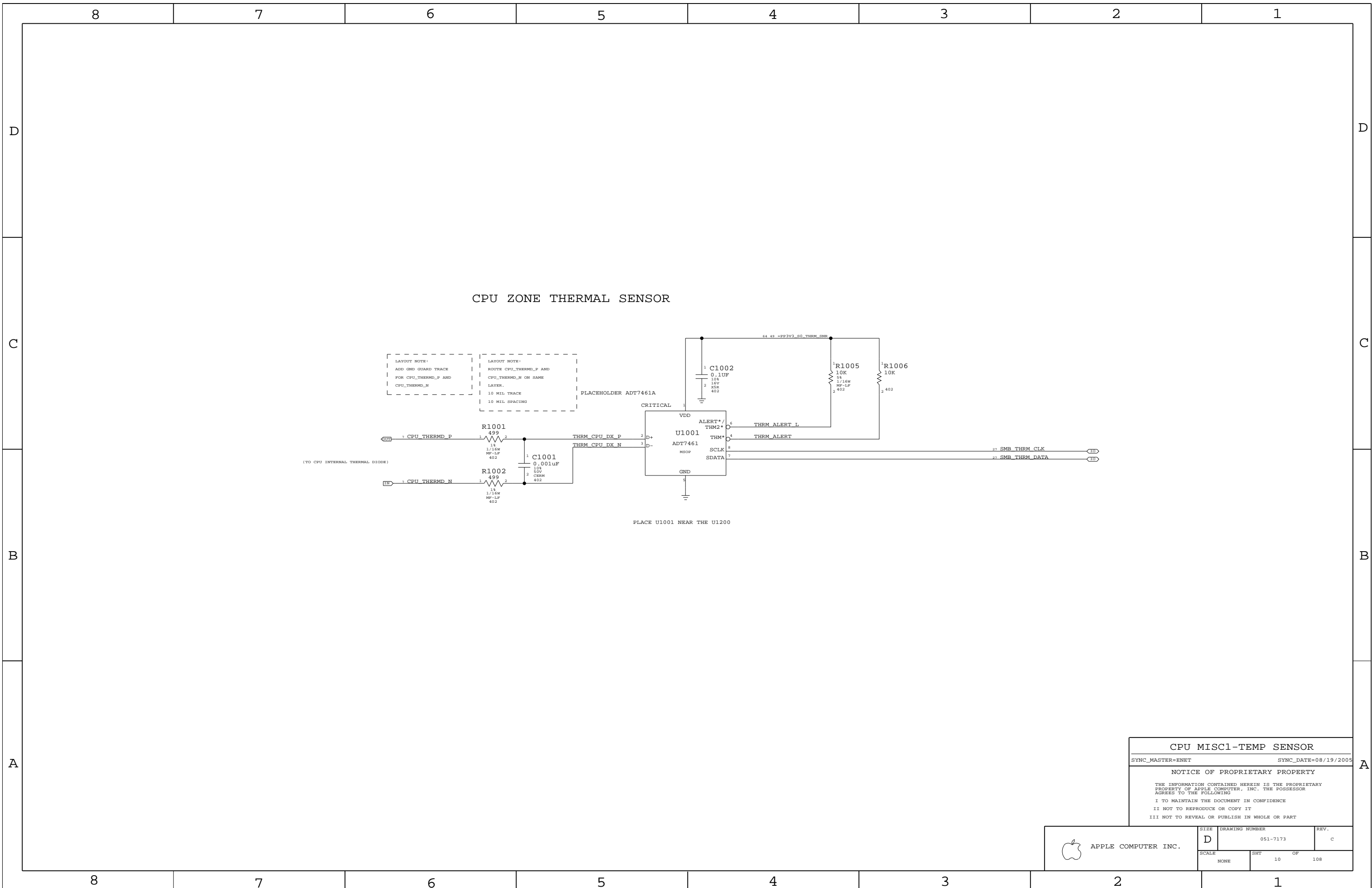
- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
- # TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE (VCORE VOLTAGE)!
- # REFER TO YONAH PROCESSOR EMTS REV 1.0
- # VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
- # VCCLFM: VCORE AT LOWEST FREQUENCY MODE

#### CPU DECAPS & VID<>

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	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	9	108	



**CPU MISC1-TEMP SENSOR**

SYNC\_MASTER=ENET SYNC\_DATE=08/19/2005

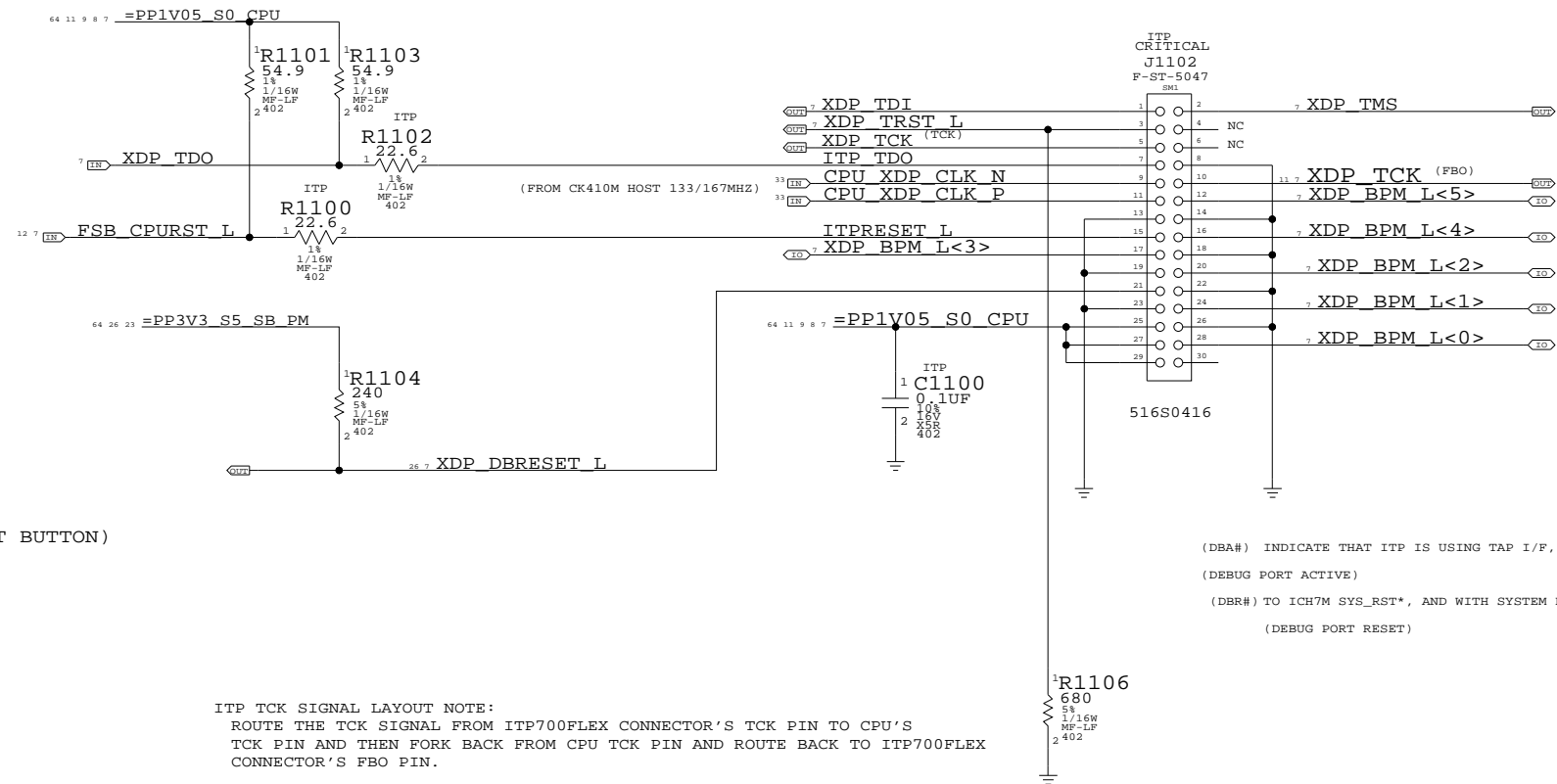
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	D	051-7173	c
SCALE	SHT	OF	108
NONE	10		

### CPU ITP700FLEX DEBUG SUPPORT



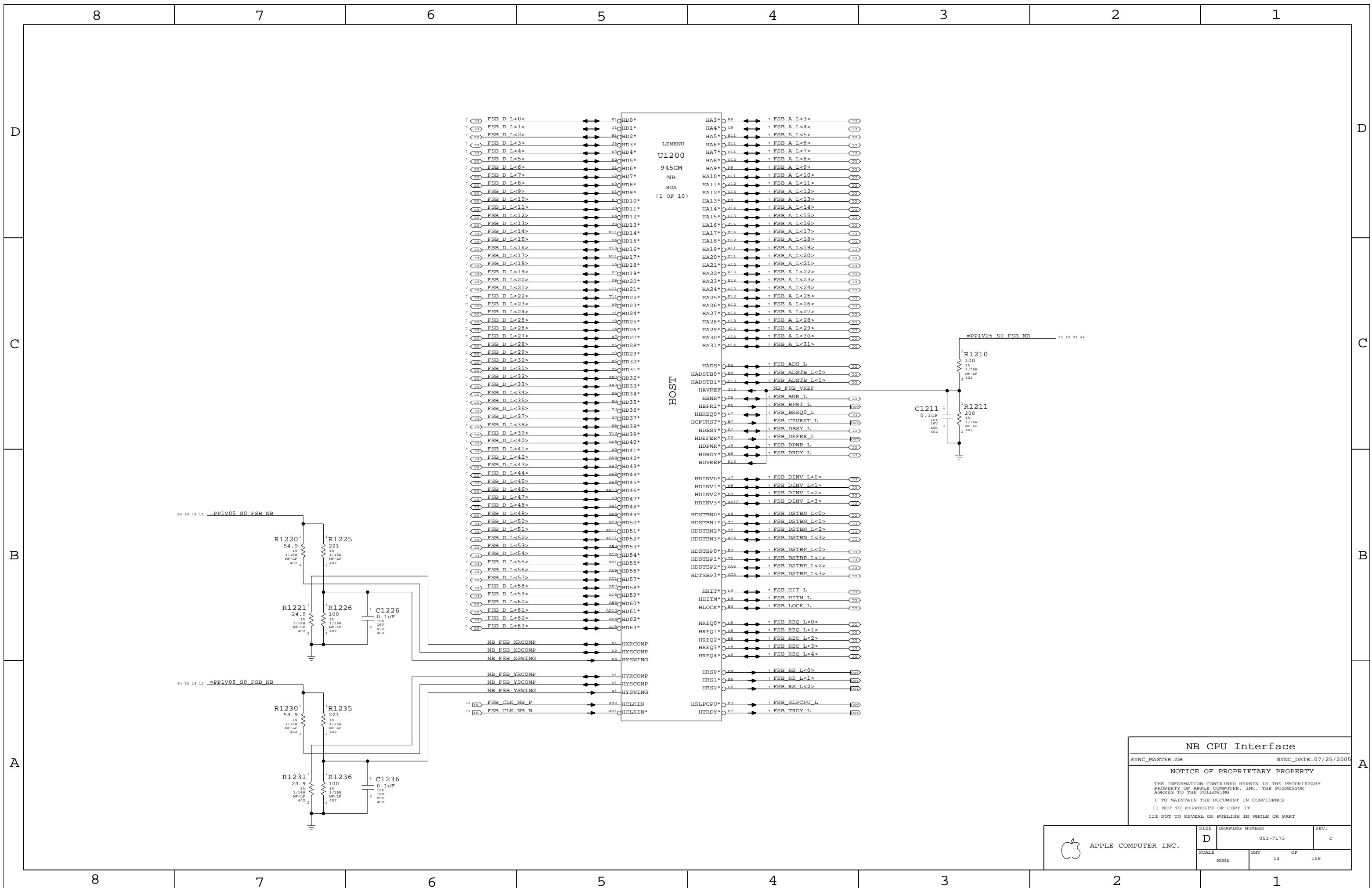
(AND WITH RESET BUTTON)

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.  
 (DEBUG PORT ACTIVE)  
 (DBR#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:  
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
 CONNECTOR'S FBO PIN.

<b>CPU ITP700FLEX DEBUG</b>		
SYNC_MASTER=MASTER	SYNC_DATE=5/23/05	
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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	11	108	



**NB CPU Interface**

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 12	OF 108

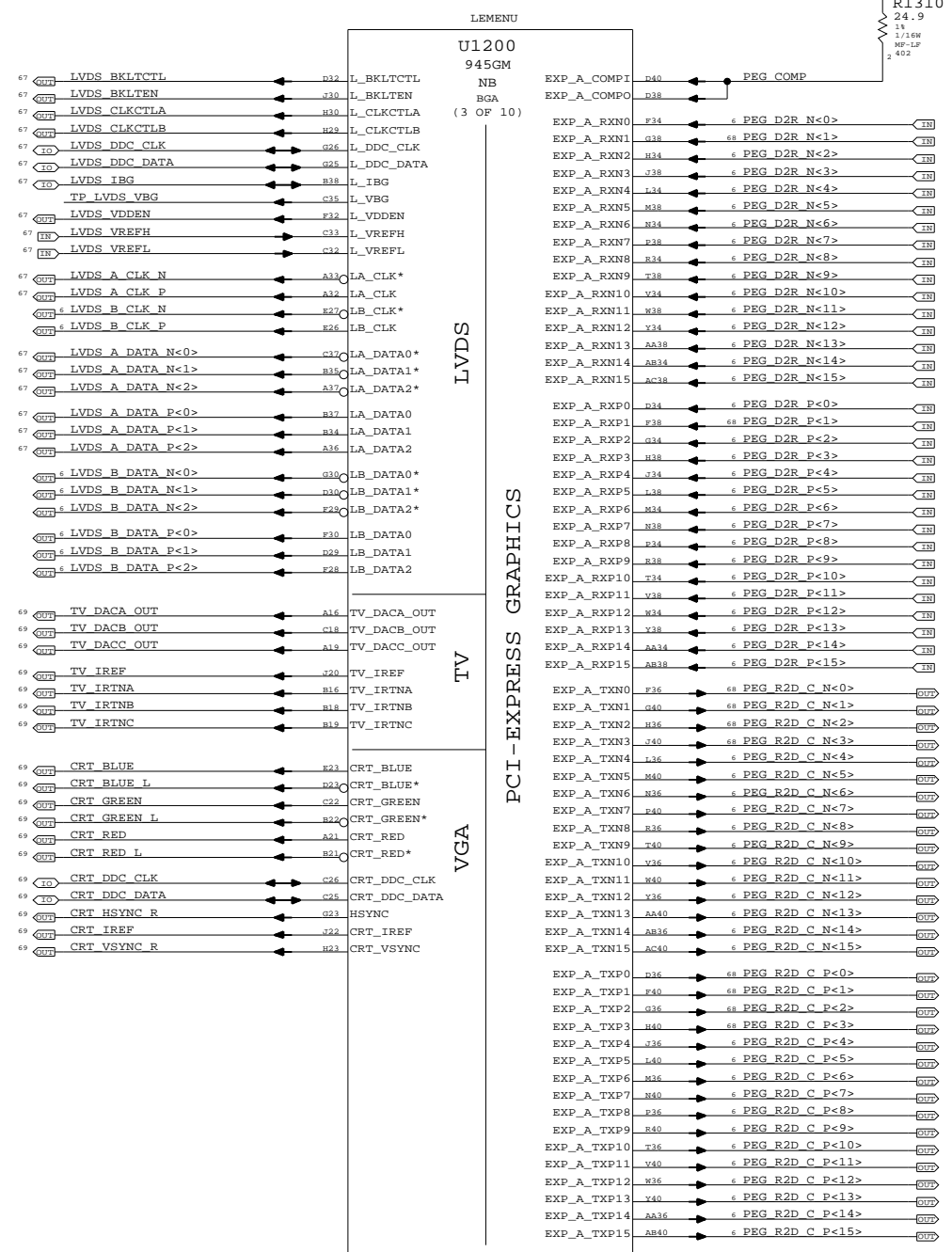
**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

**TV-Out Disable**  
 Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**  
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



SDVO Alternate Function

SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

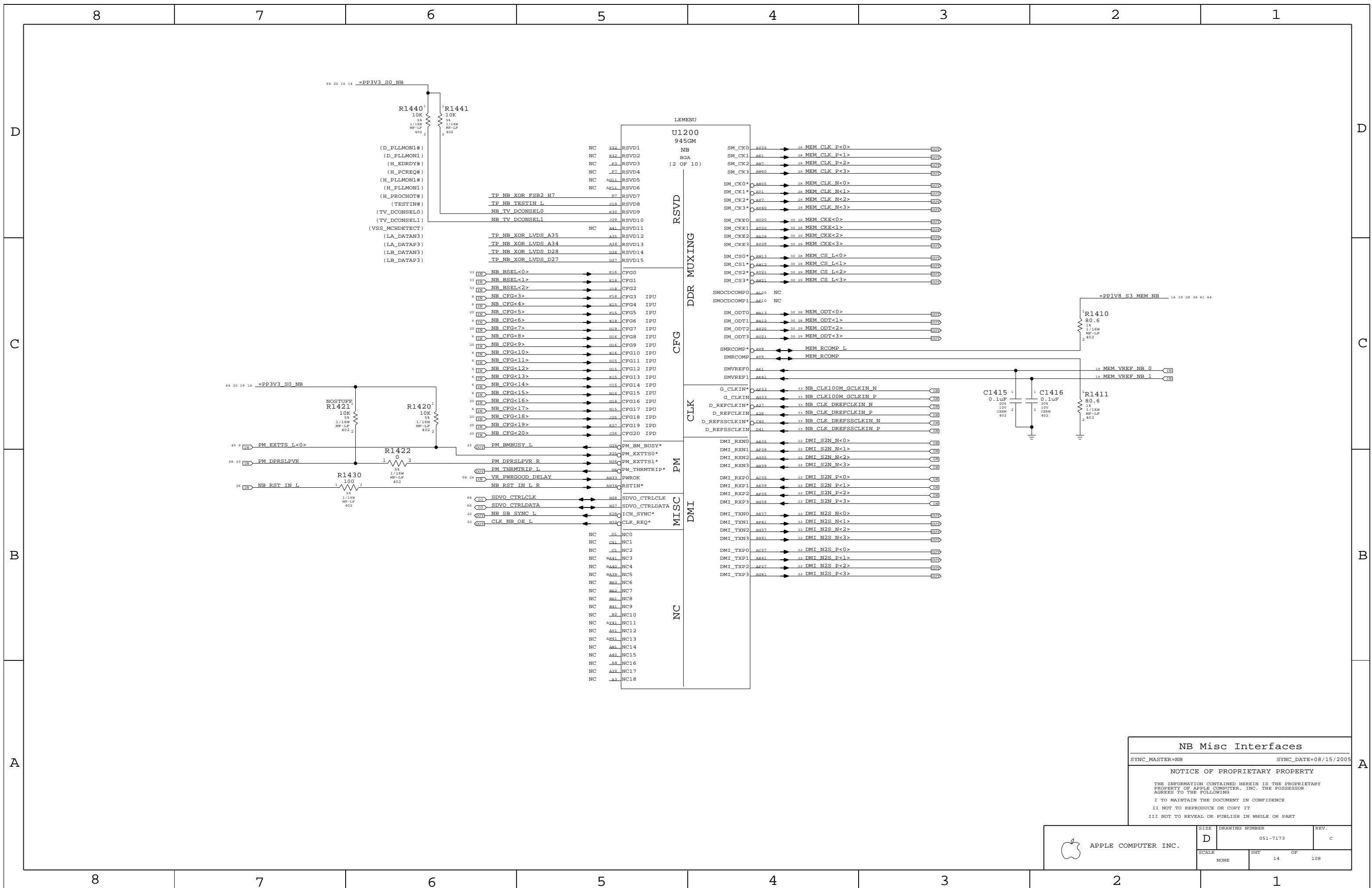
SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

**NB PEG / Video Interfaces**

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	13	108	



**NB Misc Interfaces**

SYNC\_MASTER=NB SYNC\_DATE=08/15/2005

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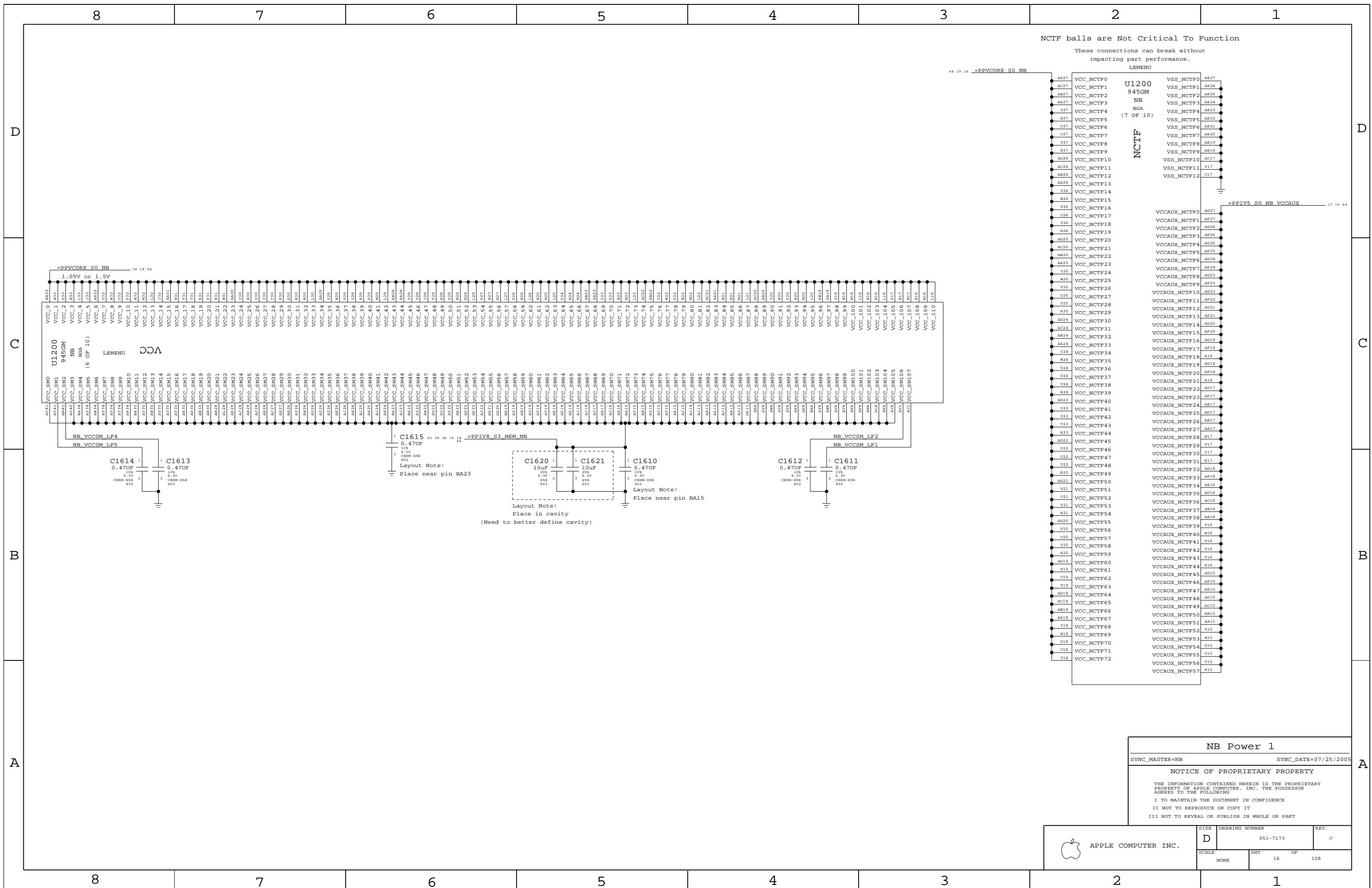
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEETS 14	OF 108





NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

U1200  
 945GM  
 NB  
 BGA  
 (7 OF 10)  
 NCTF

VCC

VCCAUX

C1615

C1620

C1621

C1610

C1612

C1611

NB Power 1

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

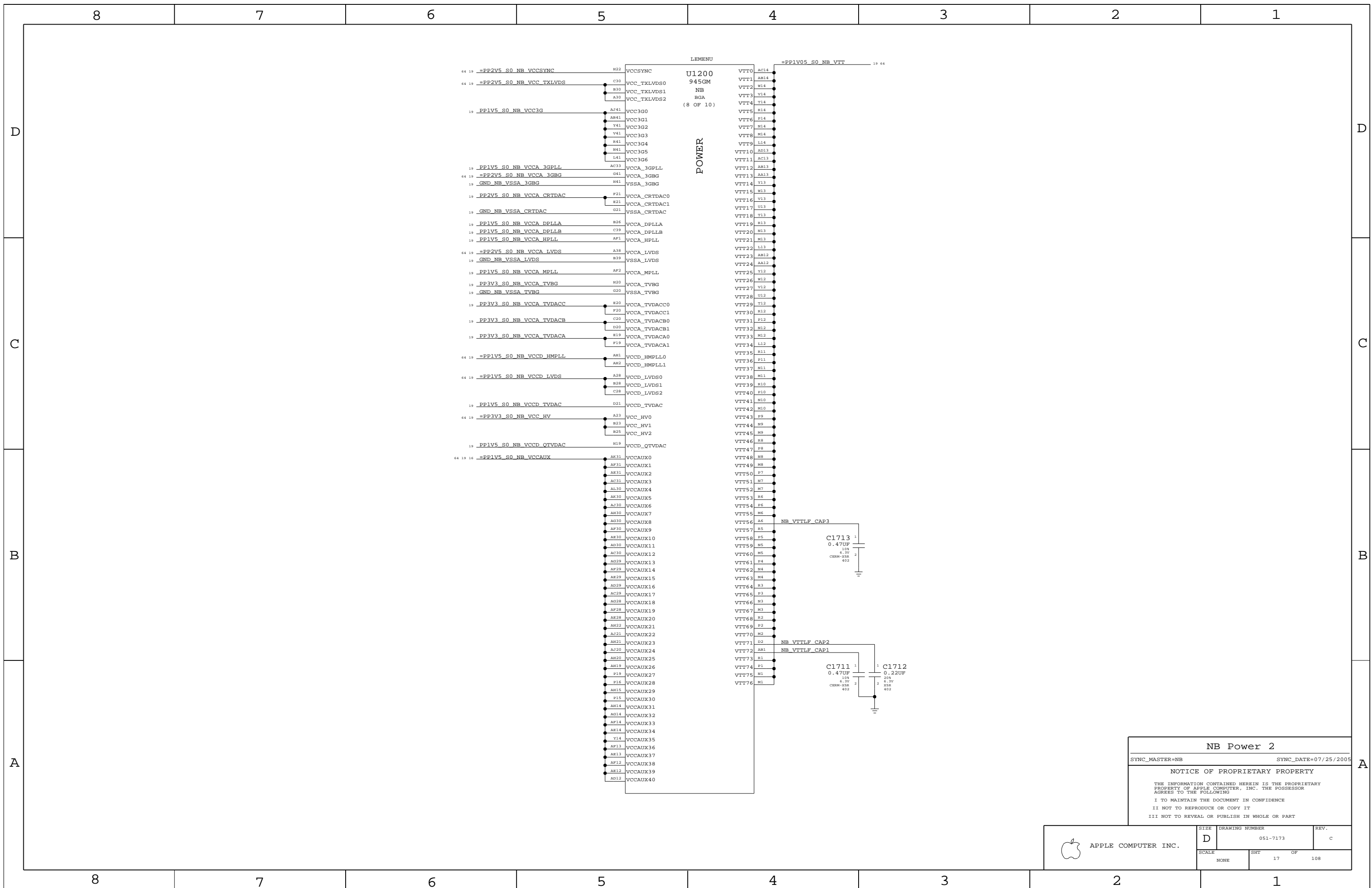
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	16		





**NB Power 2**

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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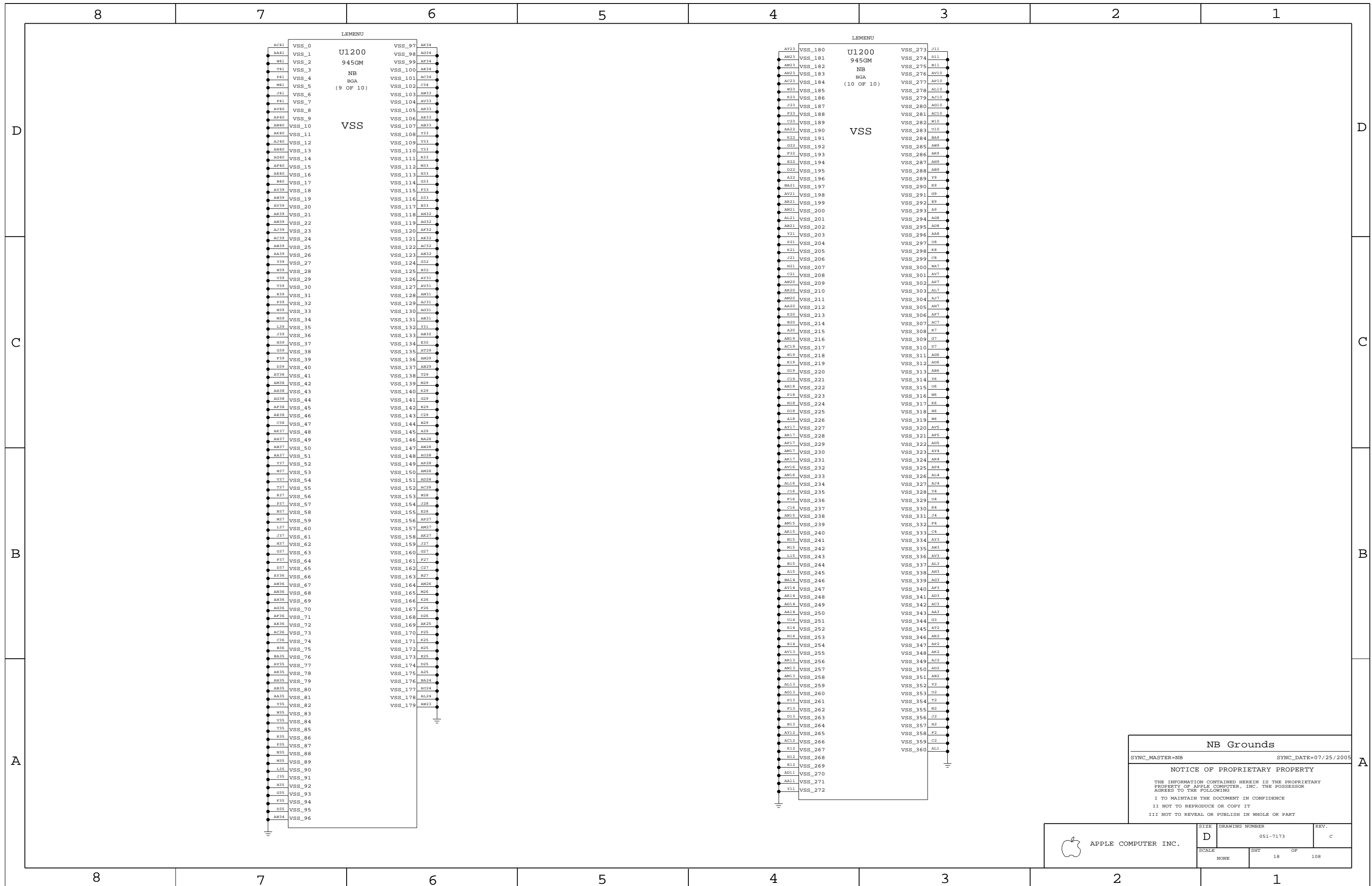
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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	17	108	



**NB Grounds**

SYNC\_MASTER=NB      SYNC\_DATE=07/25/2005

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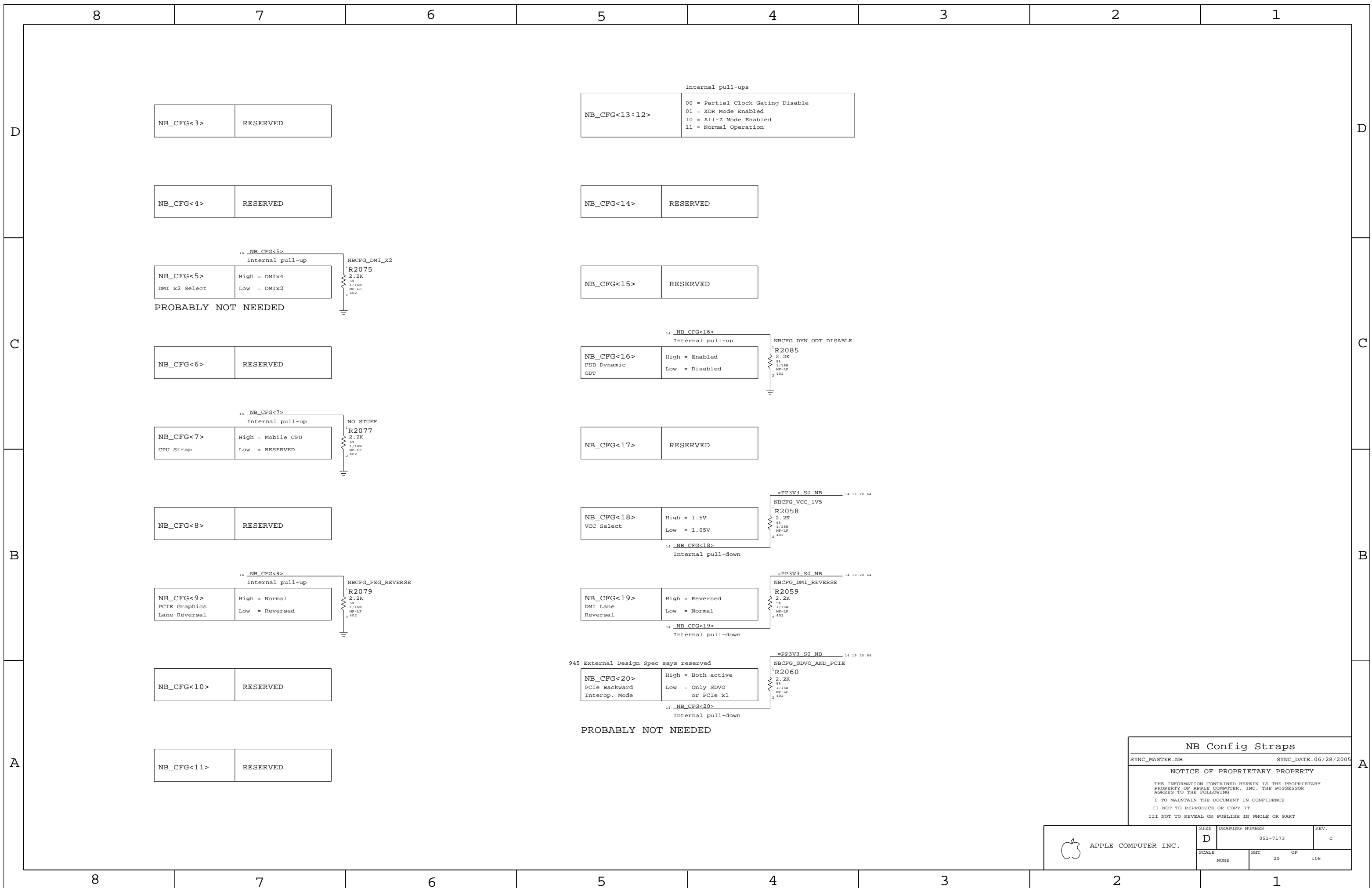
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHEET 18	OF 108





NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	---

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2

PROBABLY NOT NEEDED

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1

NB_CFG<11>	RESERVED
------------	----------

**NB Config Straps**

SYNC\_MASTER=NB SYNC\_DATE=06/28/2005

**NOTICE OF PROPRIETARY PROPERTY**

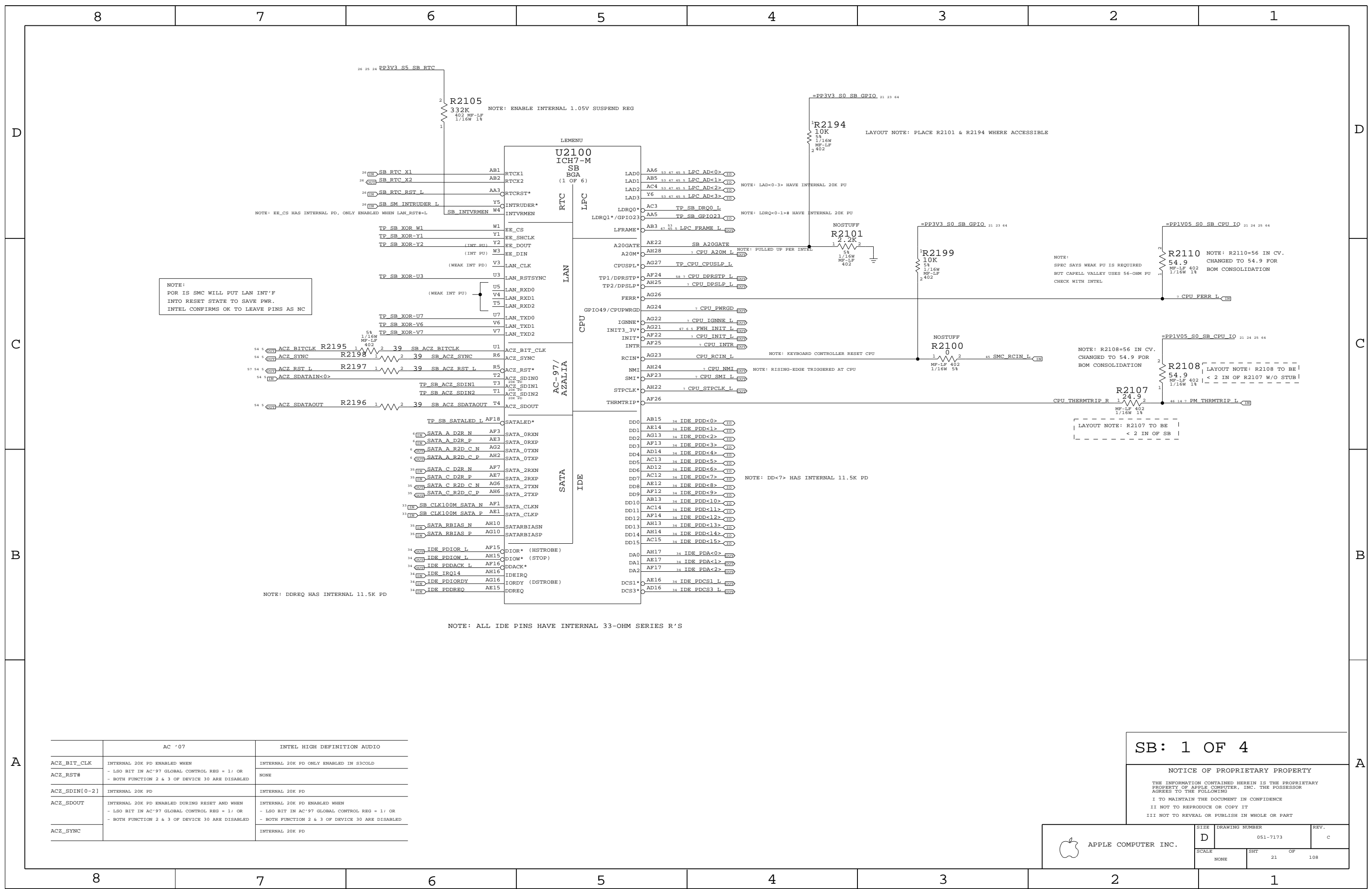
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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	20	108	



NOTE:  
POR IS SMC WILL PUT LAN INTI'F  
INTO RESET STATE TO SAVE PWR.  
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: ER\_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN\_RST#L

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: PULLED UP PER INTEL

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE:  
SPEC SAYS WEAK PU IS REQUIRED  
BUT CAPELL VALLEY USES 56-OHM PU  
CHECK WITH INTEL

NOTE: R2108=56 IN CV.  
CHANGED TO 54.9 FOR  
BOM CONSOLIDATION

LAYOUT NOTE: R2107 TO BE  
< 2 IN OF SB

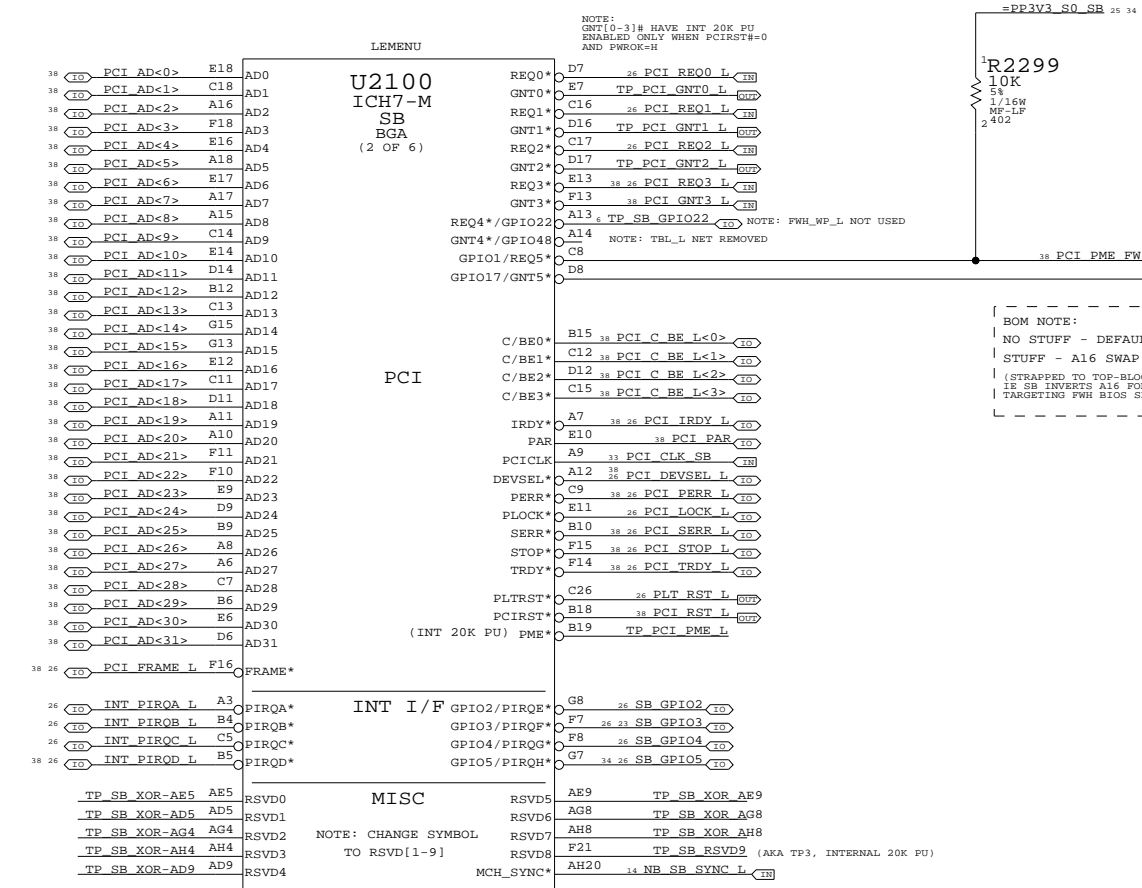
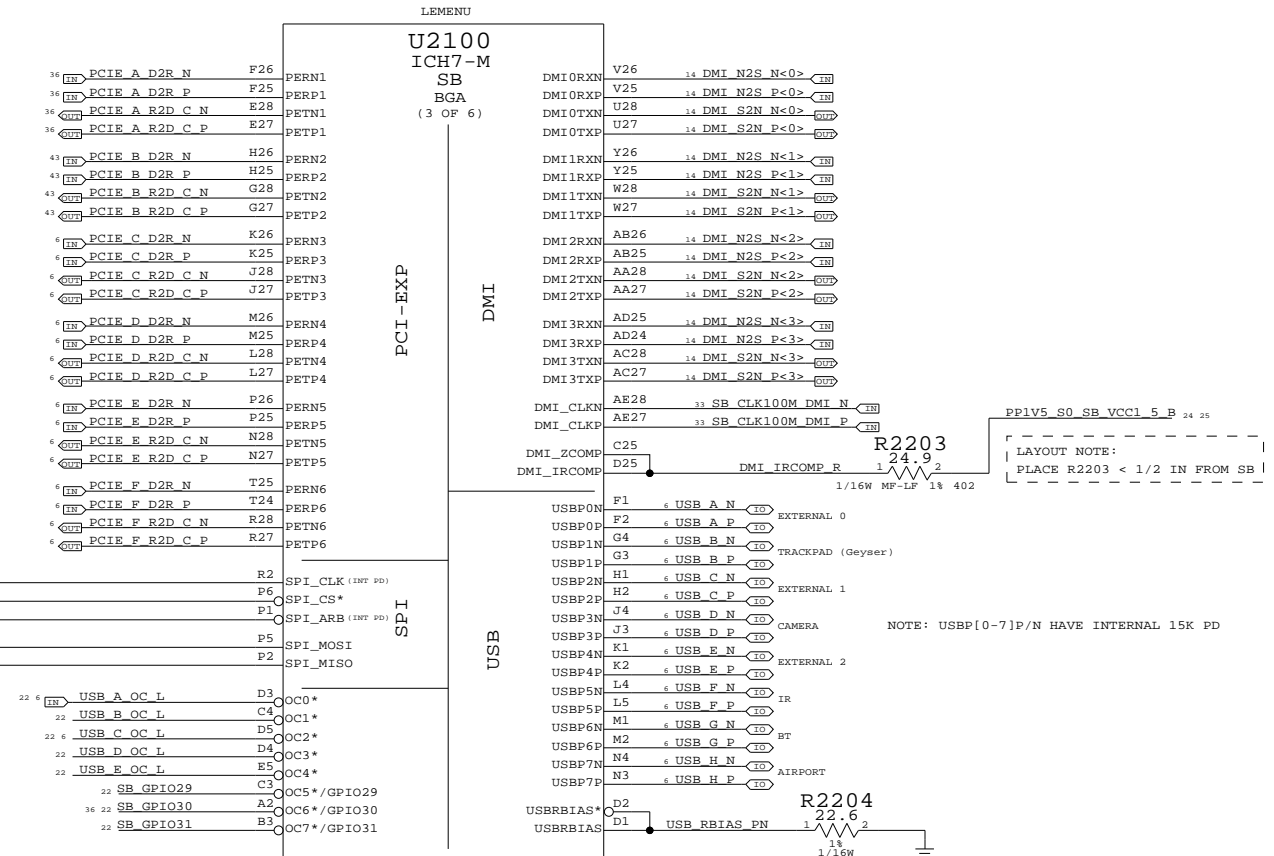
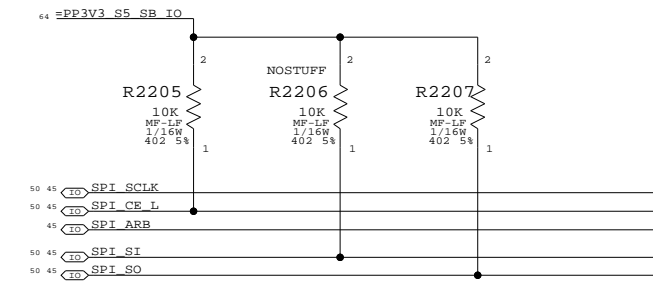
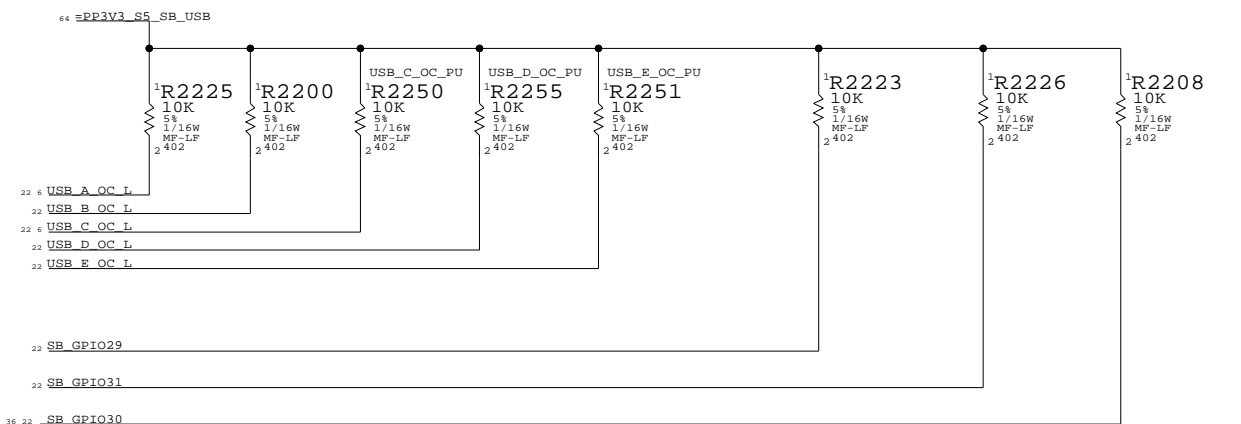
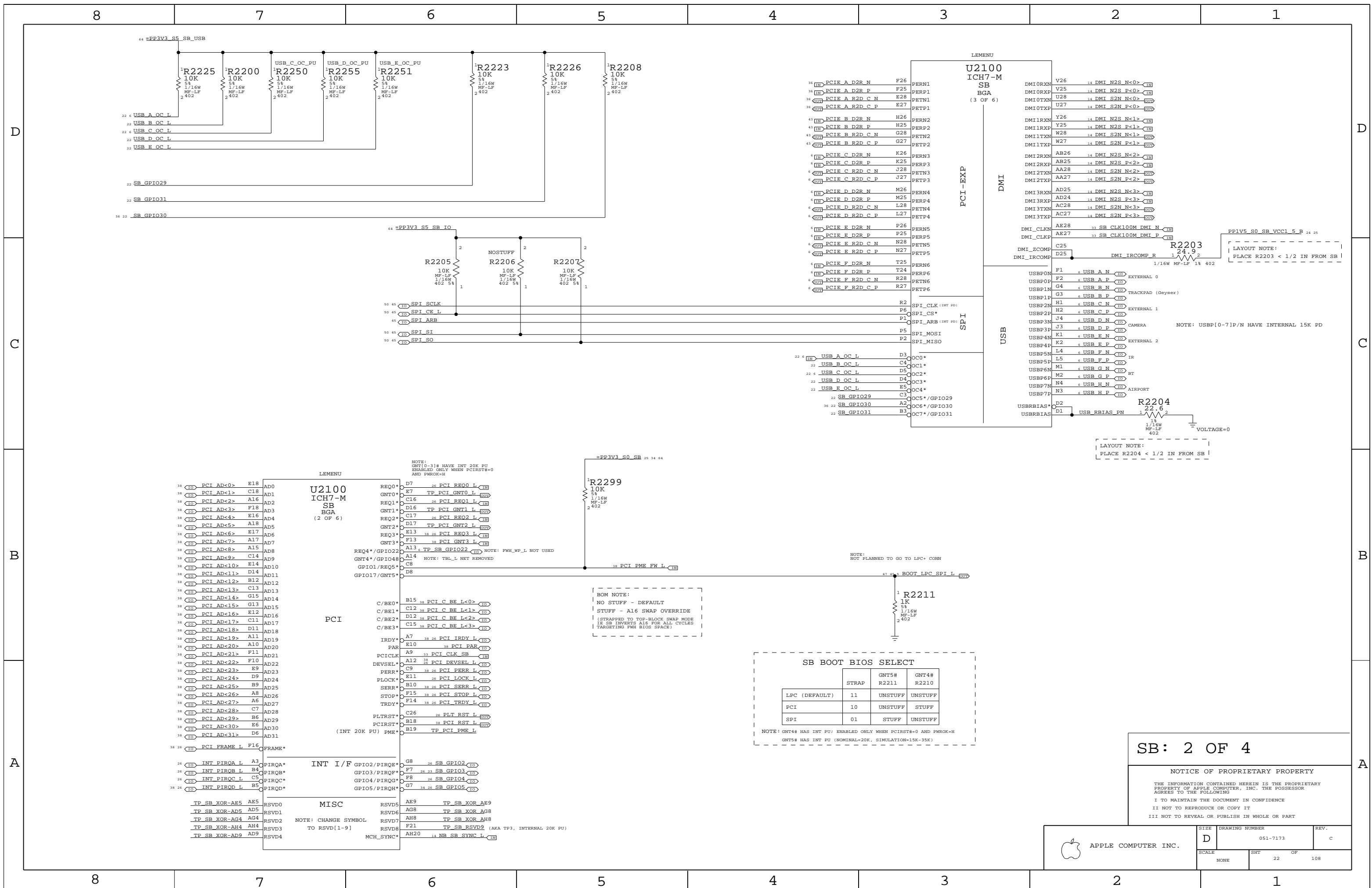
NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD	INTERNAL 20K PD

SB: 1 OF 4

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	NONE	SHT	21 OF 108



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST#0 AND PWROK#H

GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB: 2 OF 4

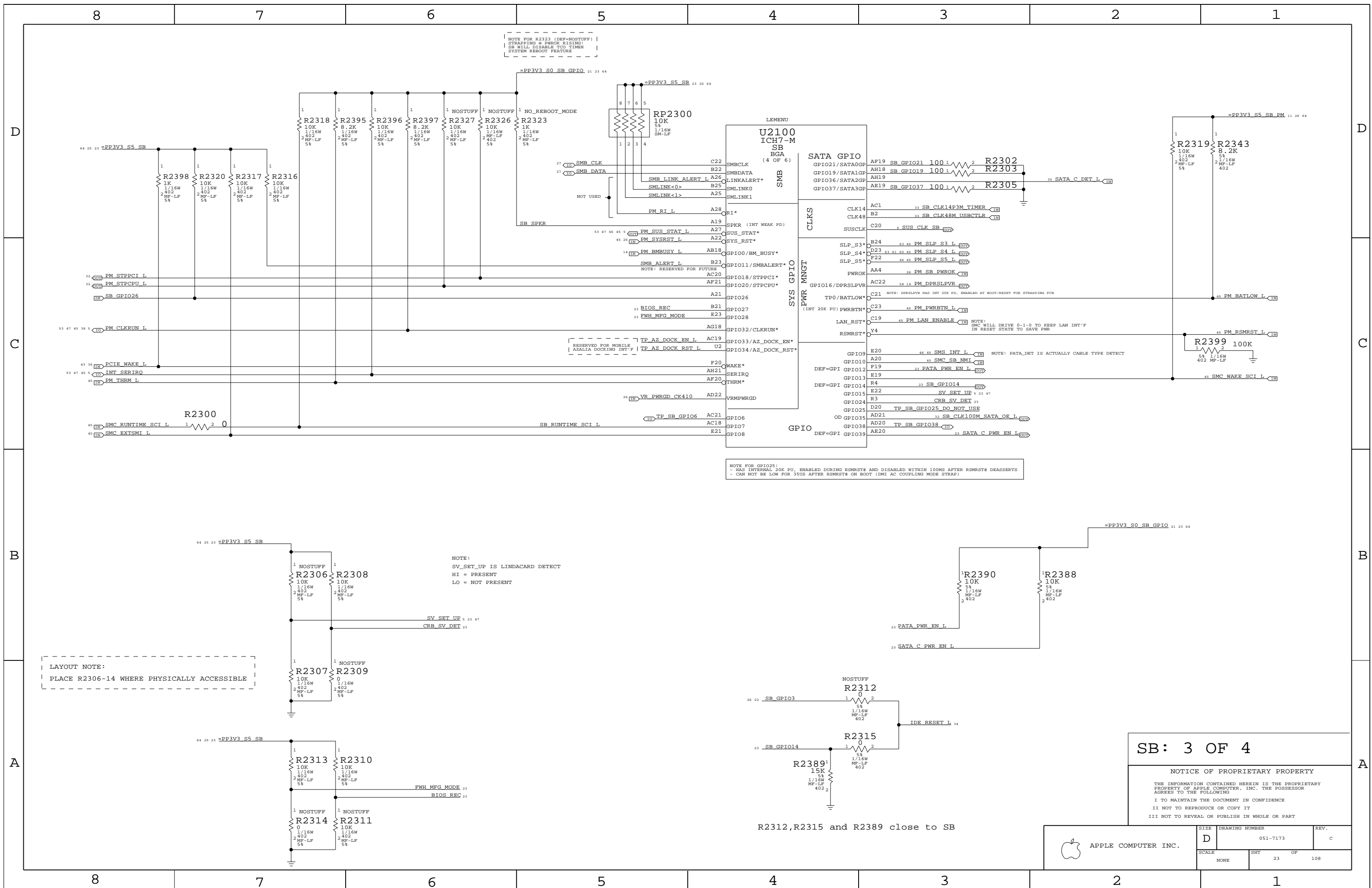
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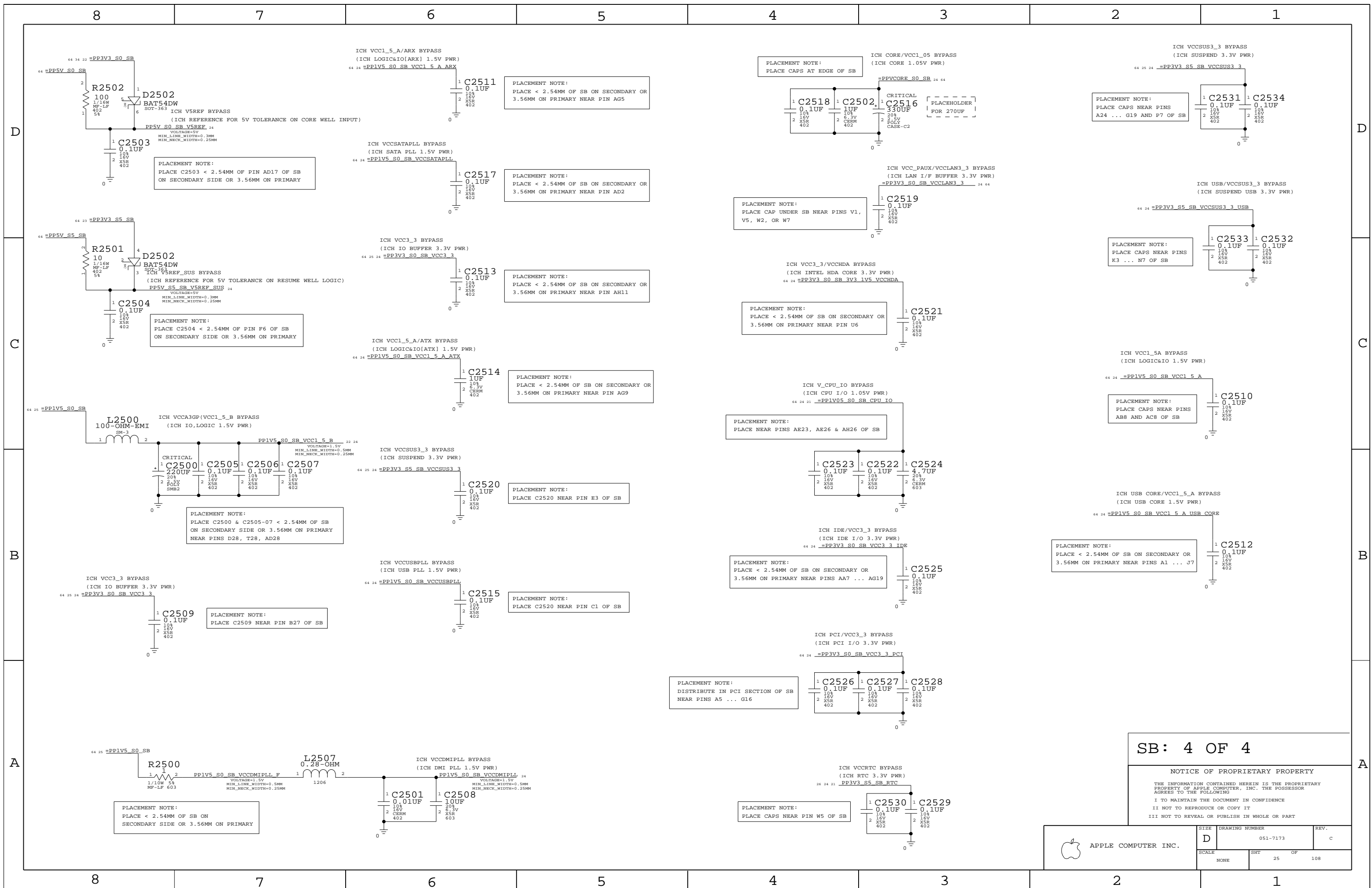
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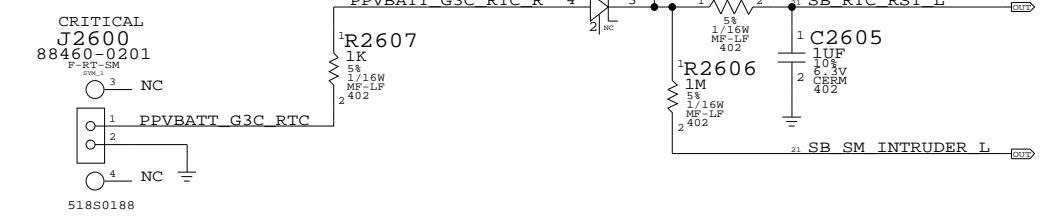
SB: 4 OF 4

NOTICE OF PROPRIETARY PROPERTY

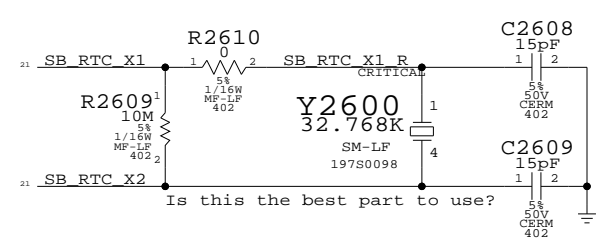
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 25	OF 108

### RTC Battery Connector

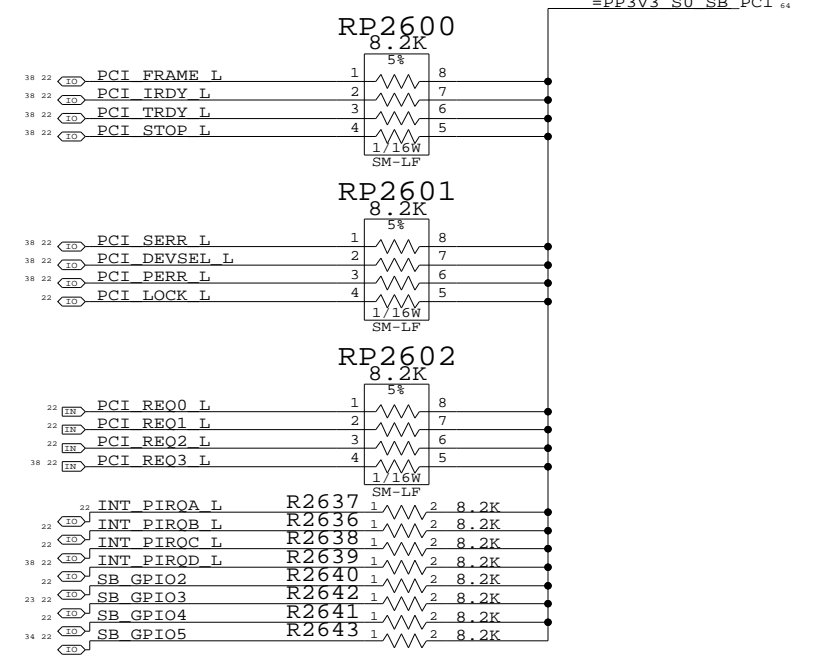
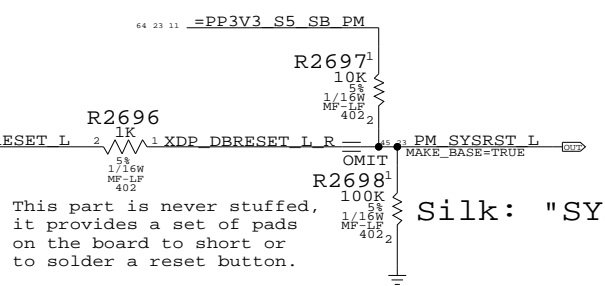


### SB RTC Crystal Circuit



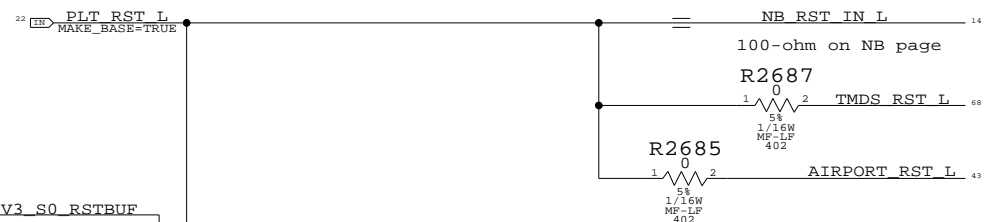
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

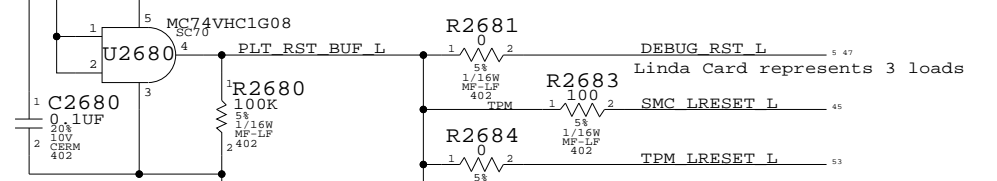


### Platform Reset Connections

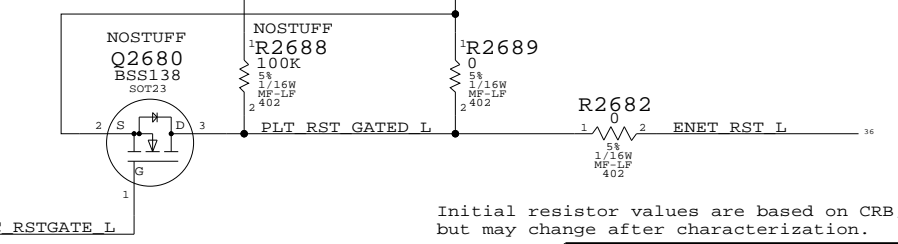
#### Unbuffered



#### Buffered



#### Gated



Initial resistor values are based on CRB, but may change after characterization.

SB Misc		
SYNC_MASTER=NB	SYNC_DATE=07/26/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	26		

8

7

6

5

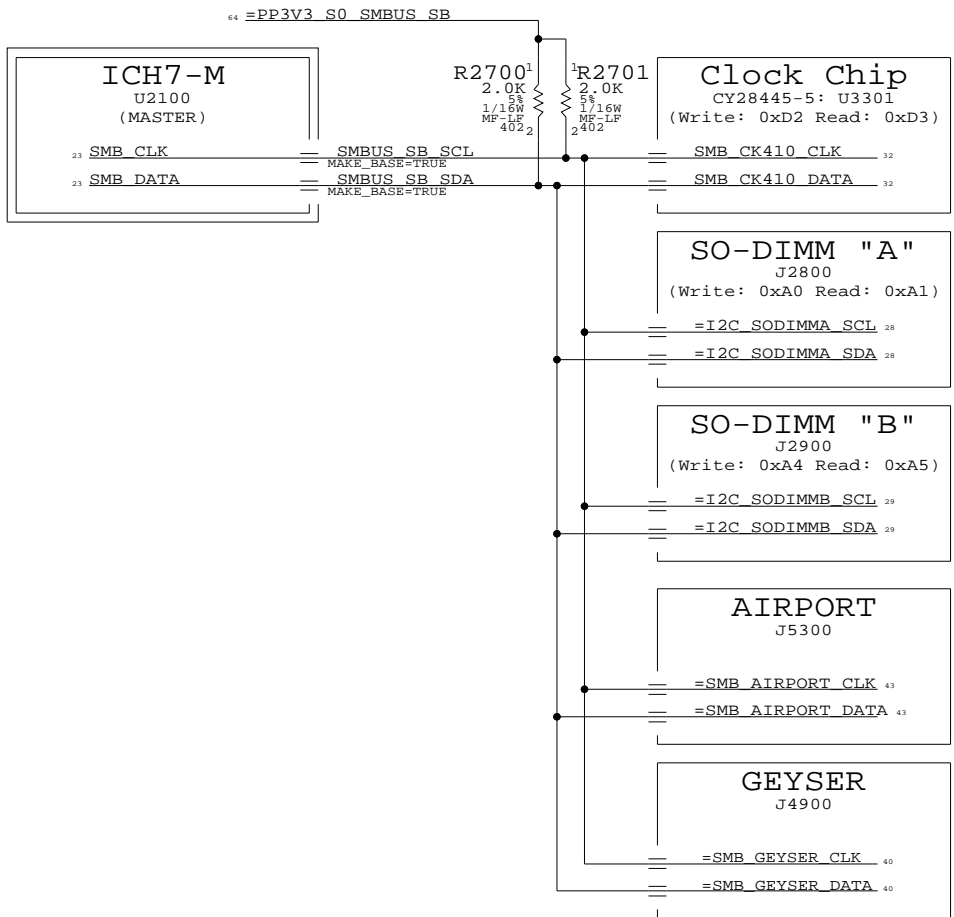
4

3

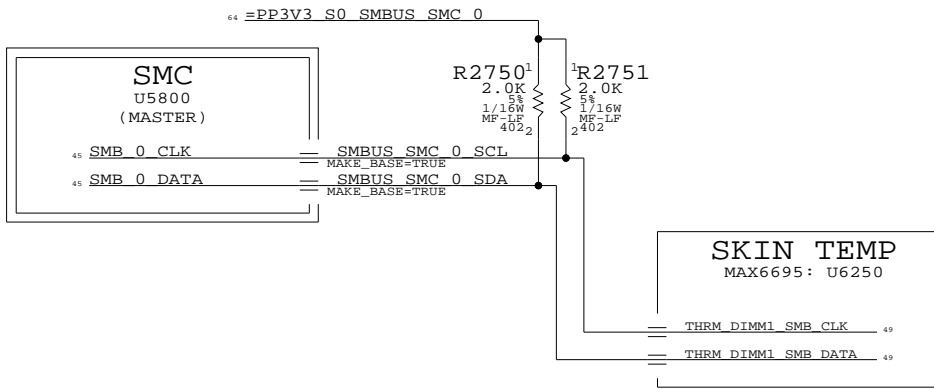
2

1

### ICH7-M SMBus Connections

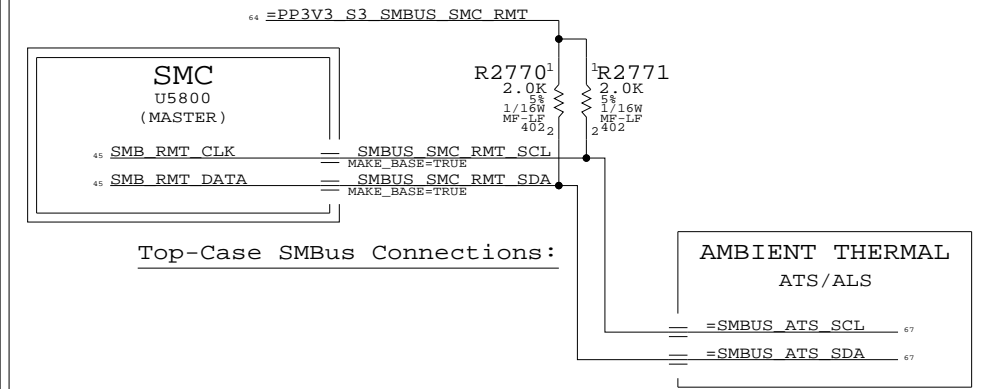


### SMC "0" SMBus Connections

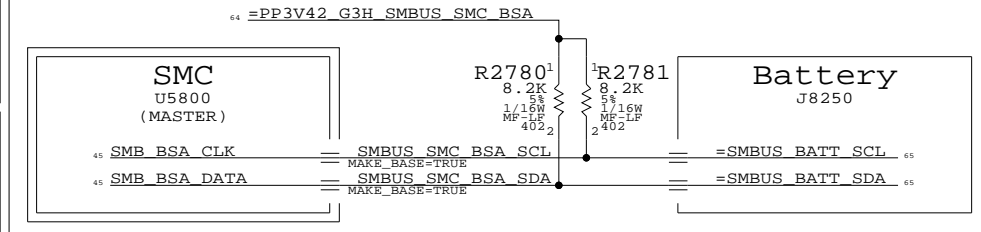


### SMC "RMT" SMBus Connections

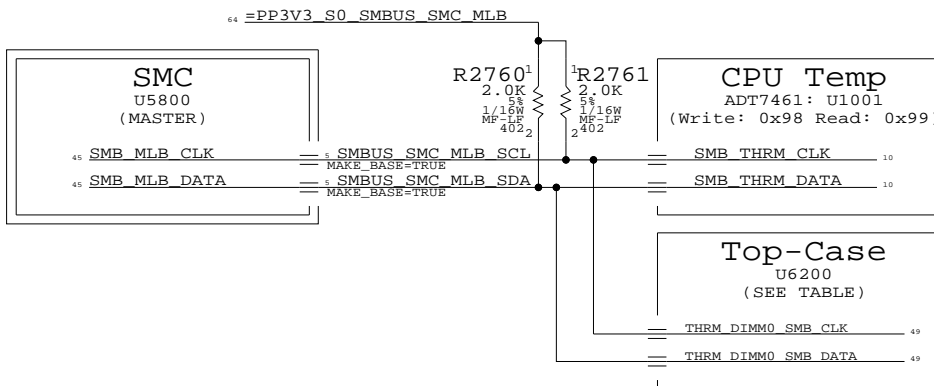
NOTE: SMC RMT bus remains powered and may be active in S3 state



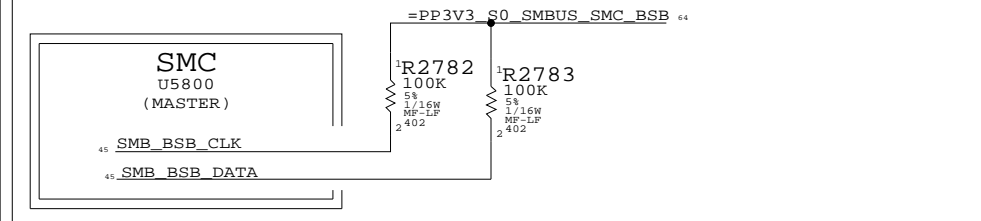
### SMC "Battery A" SMBus Connections



### SMC "MLB" SMBus Connections



### SMC "Battery B" SMBus Connections



### M42 SMBUS CONNECTIONS

SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	27	108	

8

7

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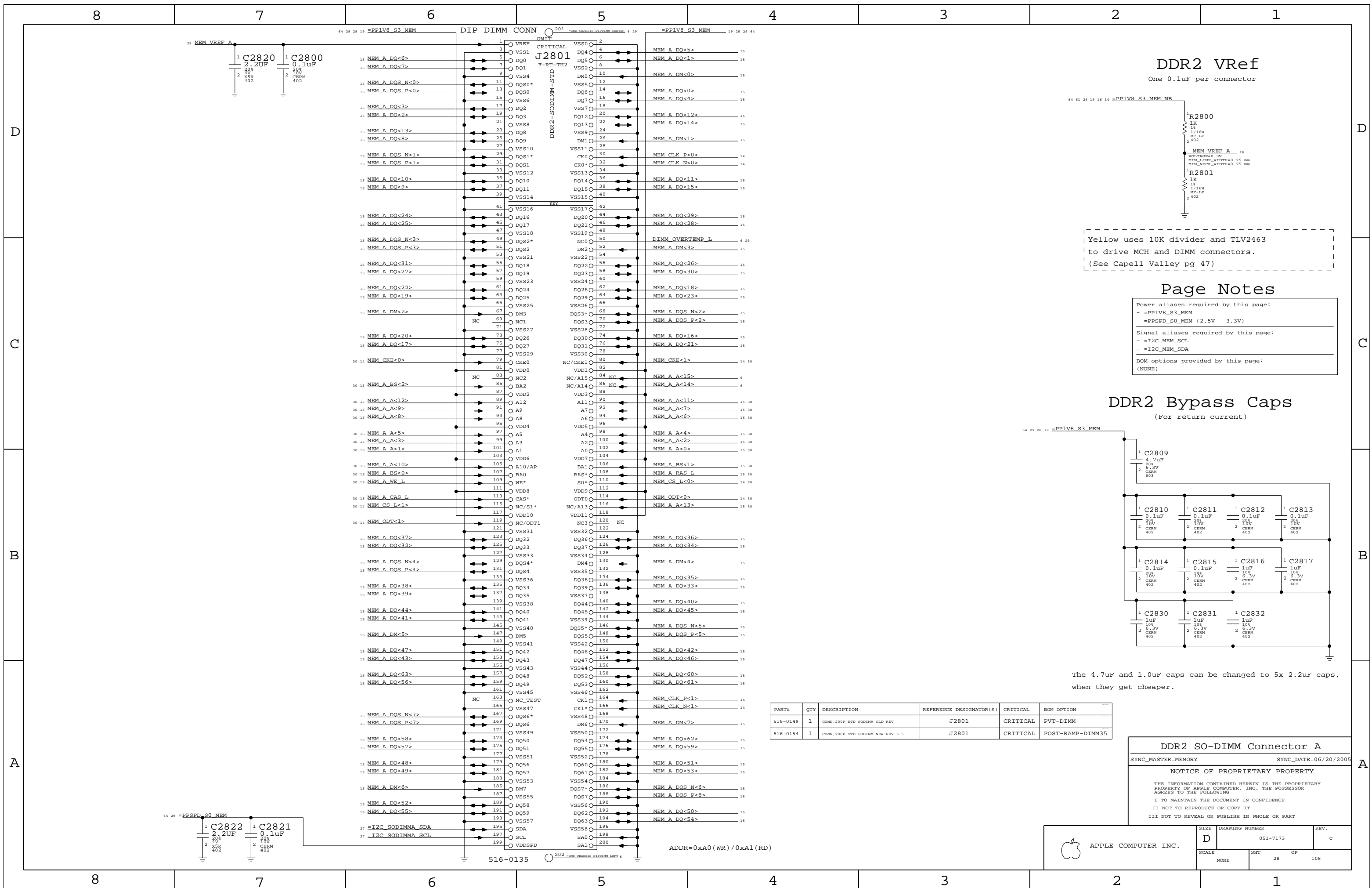
5

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3

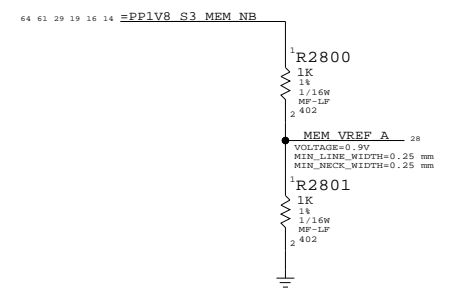
2

1



### DDR2 VRef

One 0.1uF per connector



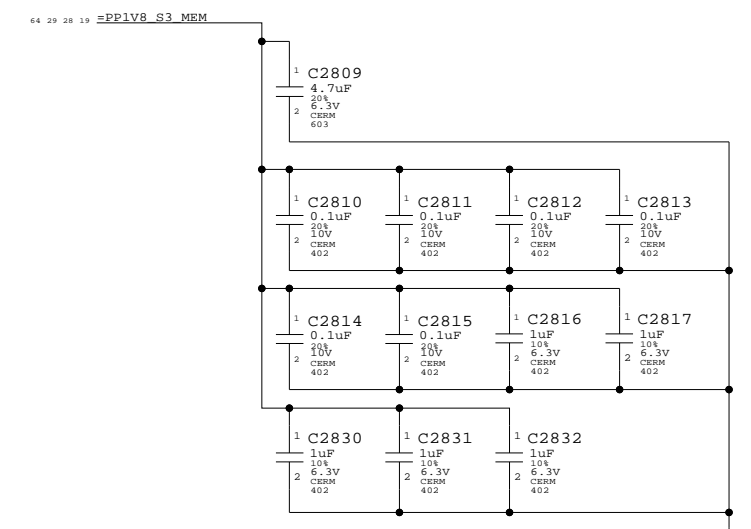
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

### Page Notes

- Power aliases required by this page:
  - =PP1V8\_S3\_MEM
  - =PPSPD\_S0\_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
  - =I2C\_MEM\_SCL
  - =I2C\_MEM\_SDA
- BOM options provided by this page:
  - (NONE)

### DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

**DDR2 SO-DIMM Connector A**

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

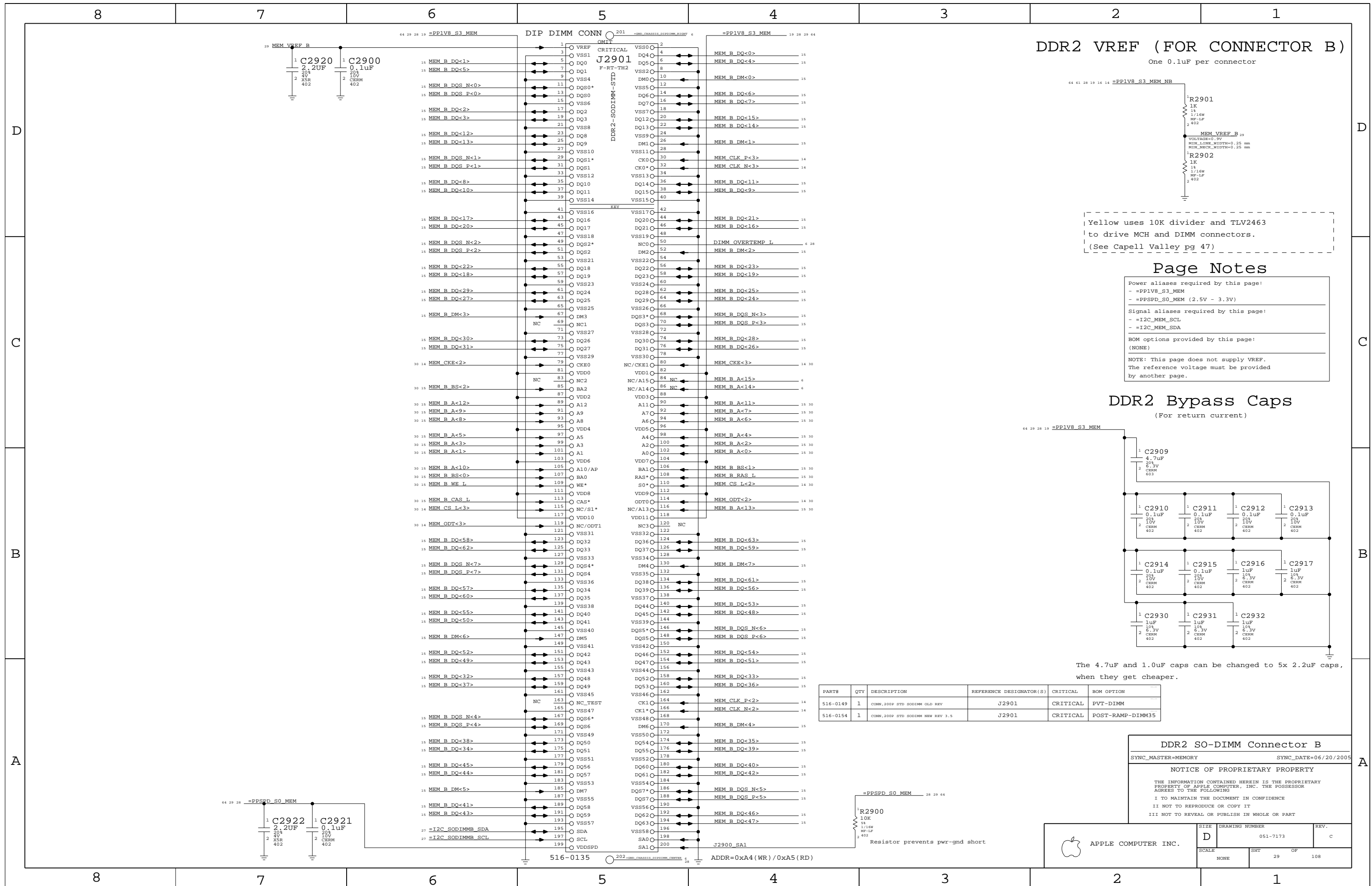
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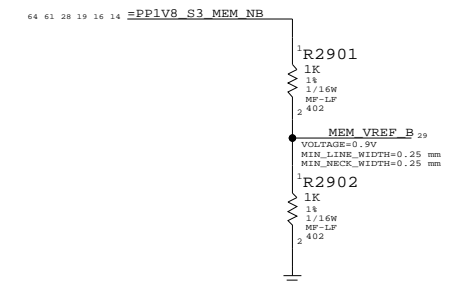
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	
NONE	28	108	

ADDR=0xA0 (WR) / 0xA1 (RD)



### DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



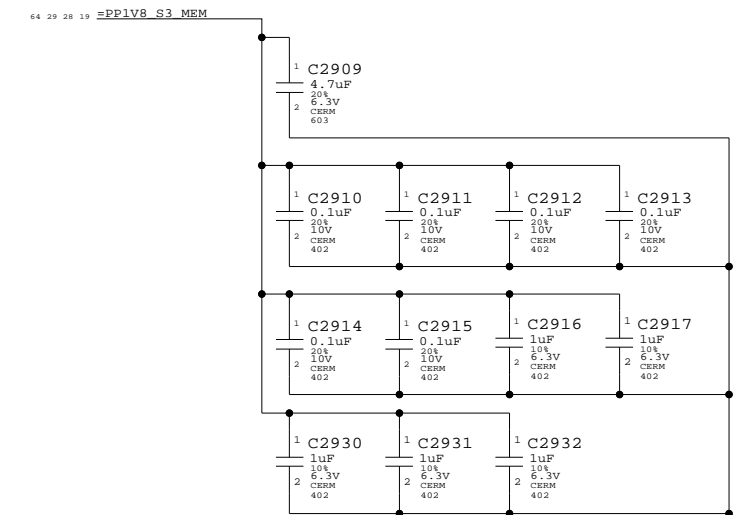
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

### Page Notes

- Power aliases required by this page:
    - =PP1V8\_S3\_MEM
    - =PPSPD\_SO\_MEM (2.5V - 3.3V)
  - Signal aliases required by this page:
    - =I2C\_MEM\_SCL
    - =I2C\_MEM\_SDA
  - BOM options provided by this page:
    - (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

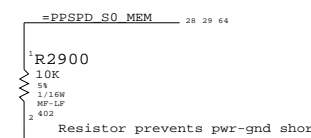
### DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 1.5	J2901	CRITICAL	POST-RAMP-DIMM35



### DDR2 SO-DIMM Connector B

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	
NONE	29	108	

8

7

6

5

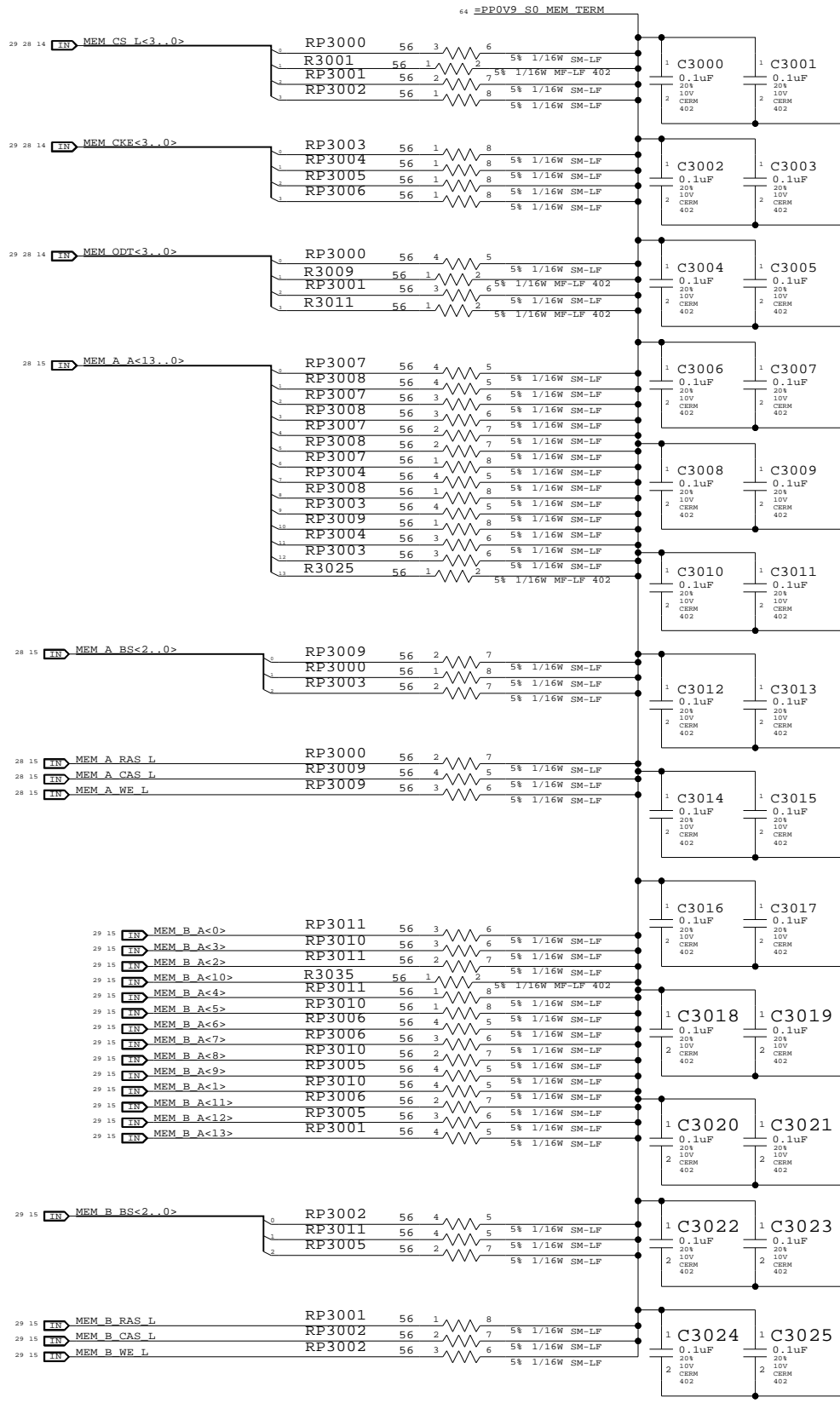
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9\_S0\_MEM\_TERM

Memory Active Termination

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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	30	108	

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

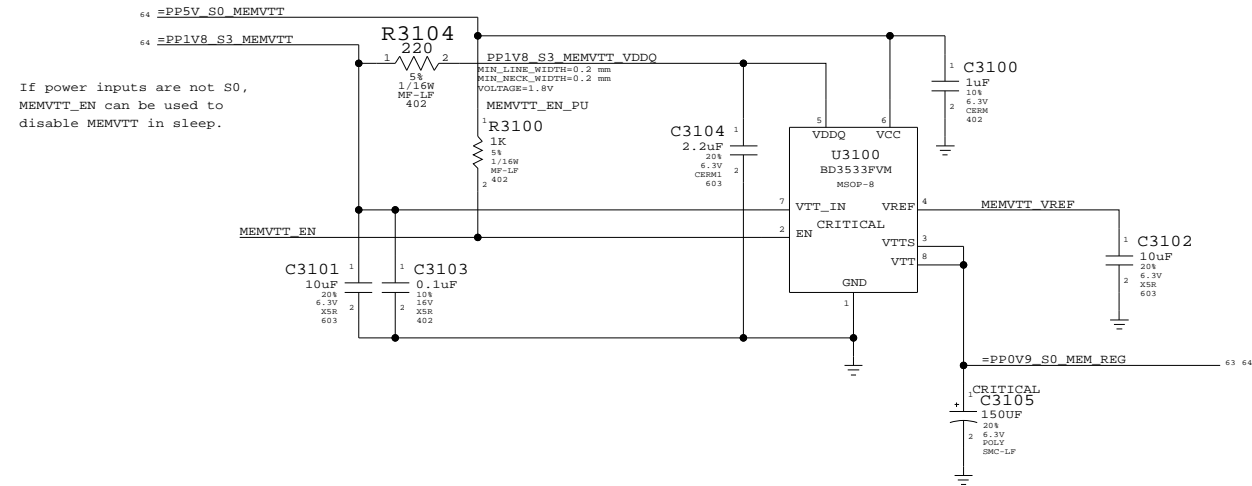
---

Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

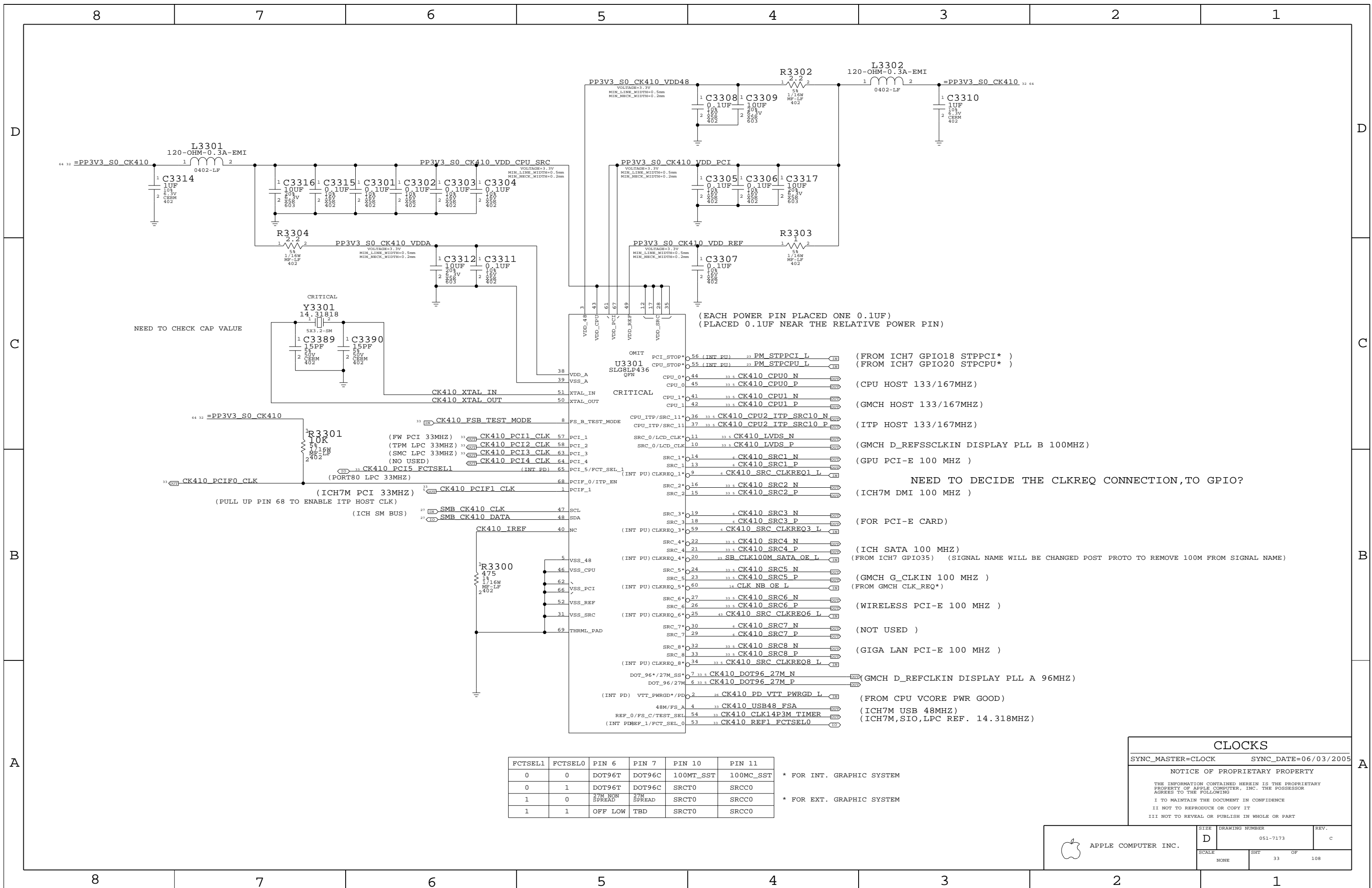
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	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	31	108	



NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI\* )  
(FROM ICH7 GPIO20 STPCPU\* )

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ )

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ )

(FOR PCI-E CARD)

(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G\_CLKIN 100 MHZ )

(FROM GMCH CLK\_REQ\*)

(WIRELESS PCI-E 100 MHZ )

(NOT USED )

(GIGA LAN PCI-E 100 MHZ )

(GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=CLOCK      SYNC\_DATE=06/03/2005

NOTICE OF PROPRIETARY PROPERTY

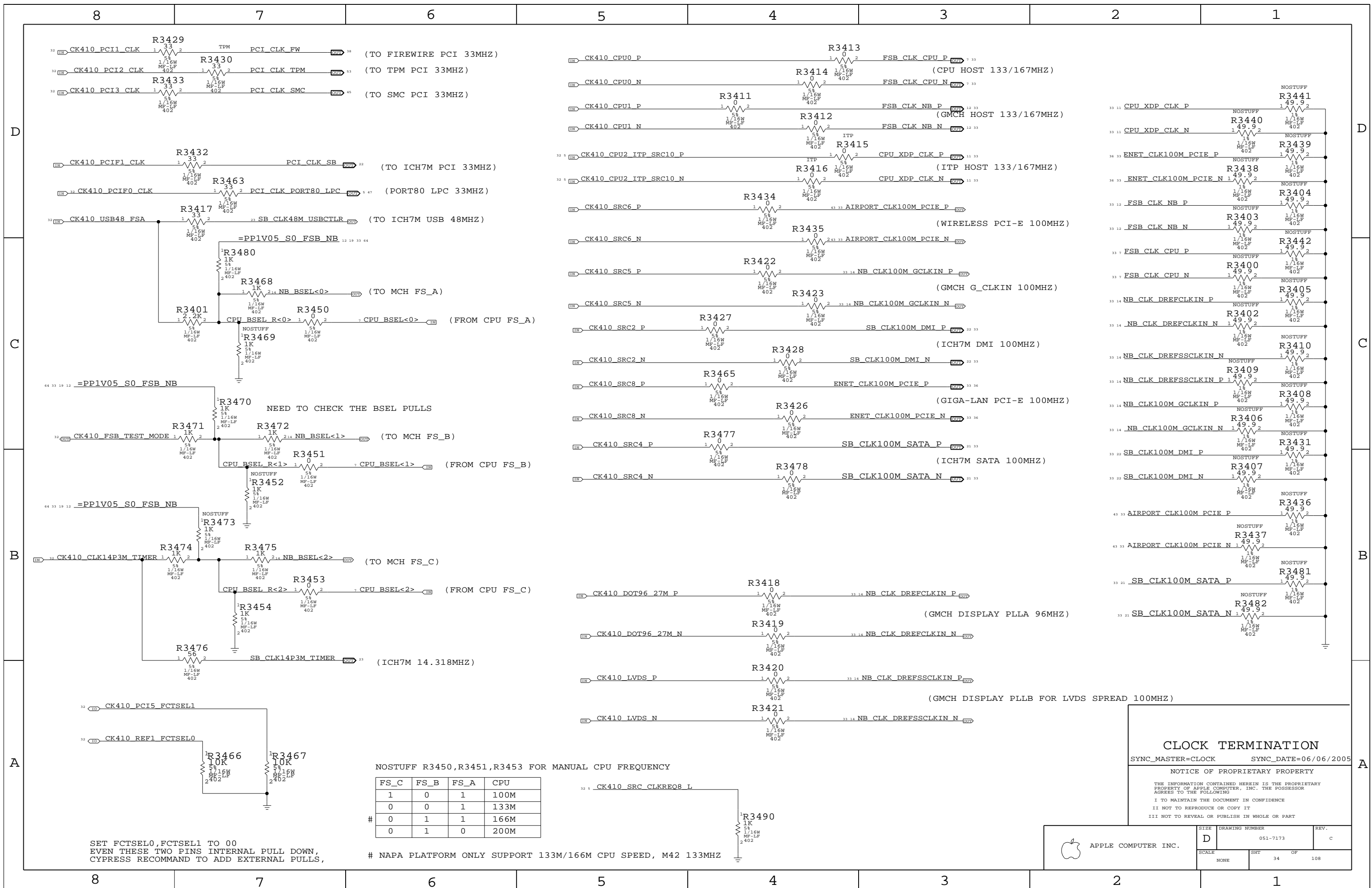
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE	SHT	OF
NONE	33	108





NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M

# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ

SET FCTSEL0, FCTSEL1 TO 00  
EVEN THESE TWO PINS INTERNAL PULL DOWN,  
CYPRESS RECOMMAND TO ADD EXTERNAL PULLS,

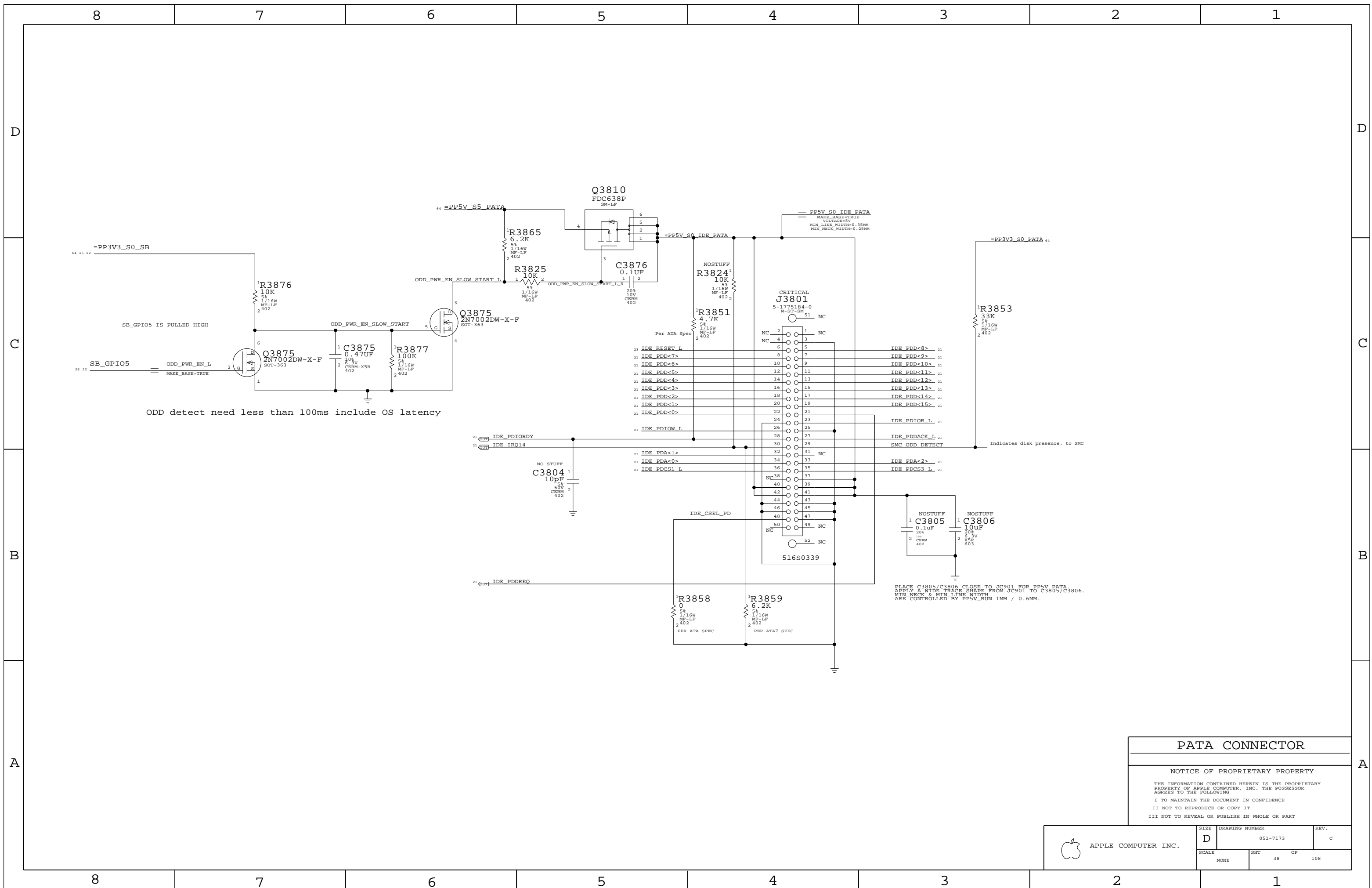
### CLOCK TERMINATION

SYNC\_MASTER=CLOCK SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	34		



**PATA CONNECTOR**

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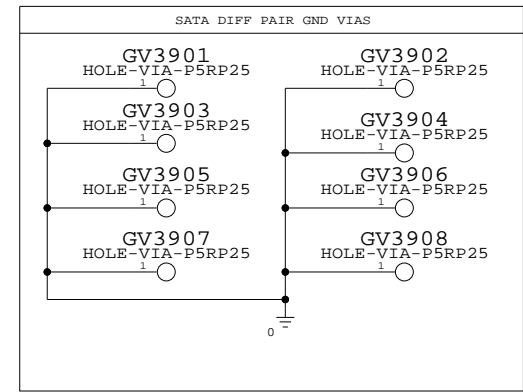
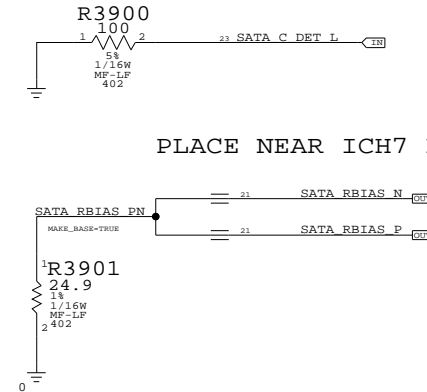
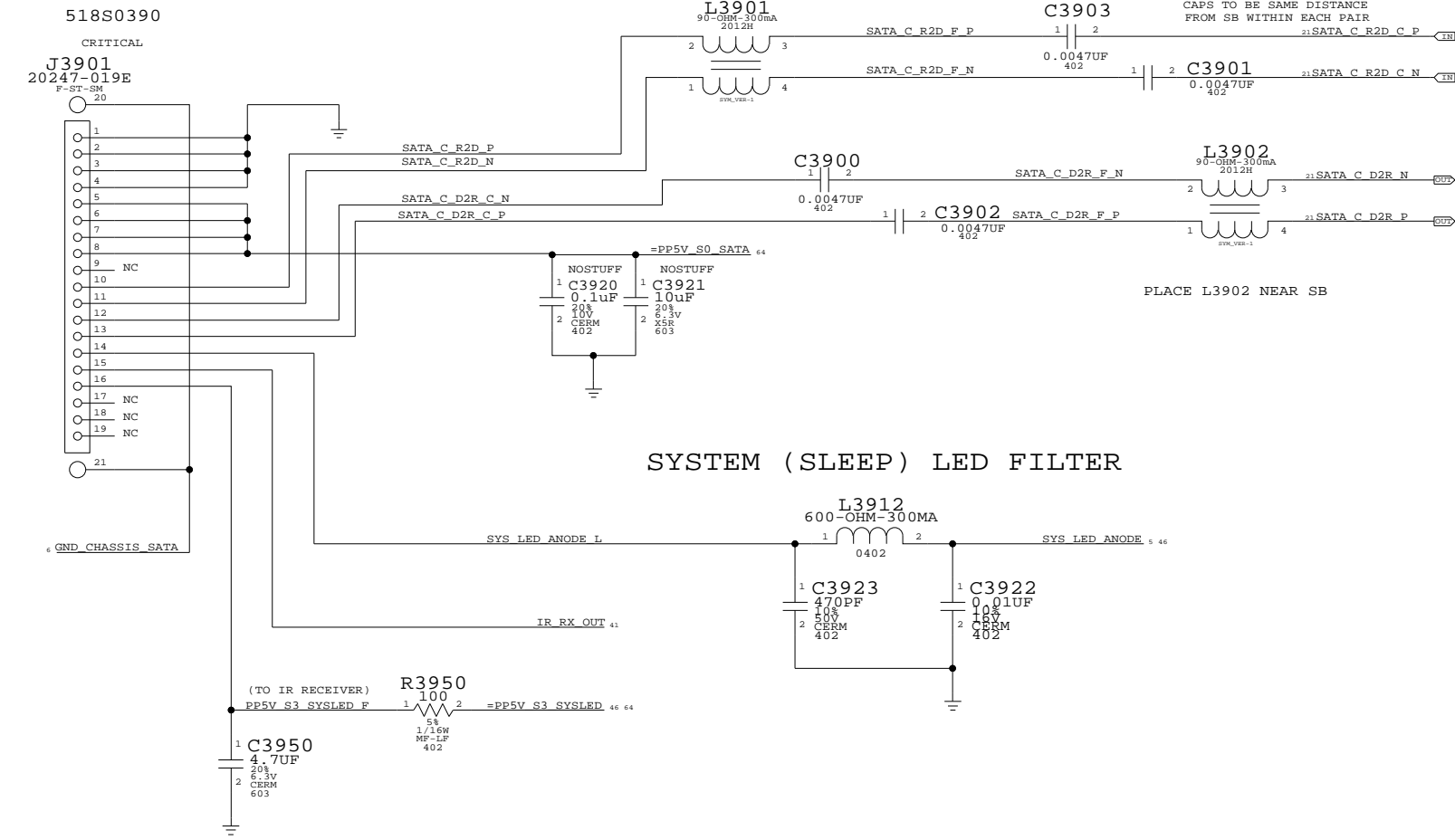
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 38	OF 108

SATA CONNECTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901, L3902	KEEP MAG. LAYER IN BOM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901, L3902	KEEP MAG. LAYER IN BOM

**SATA CONNECTOR**

NOTICE OF PROPRIETARY PROPERTY

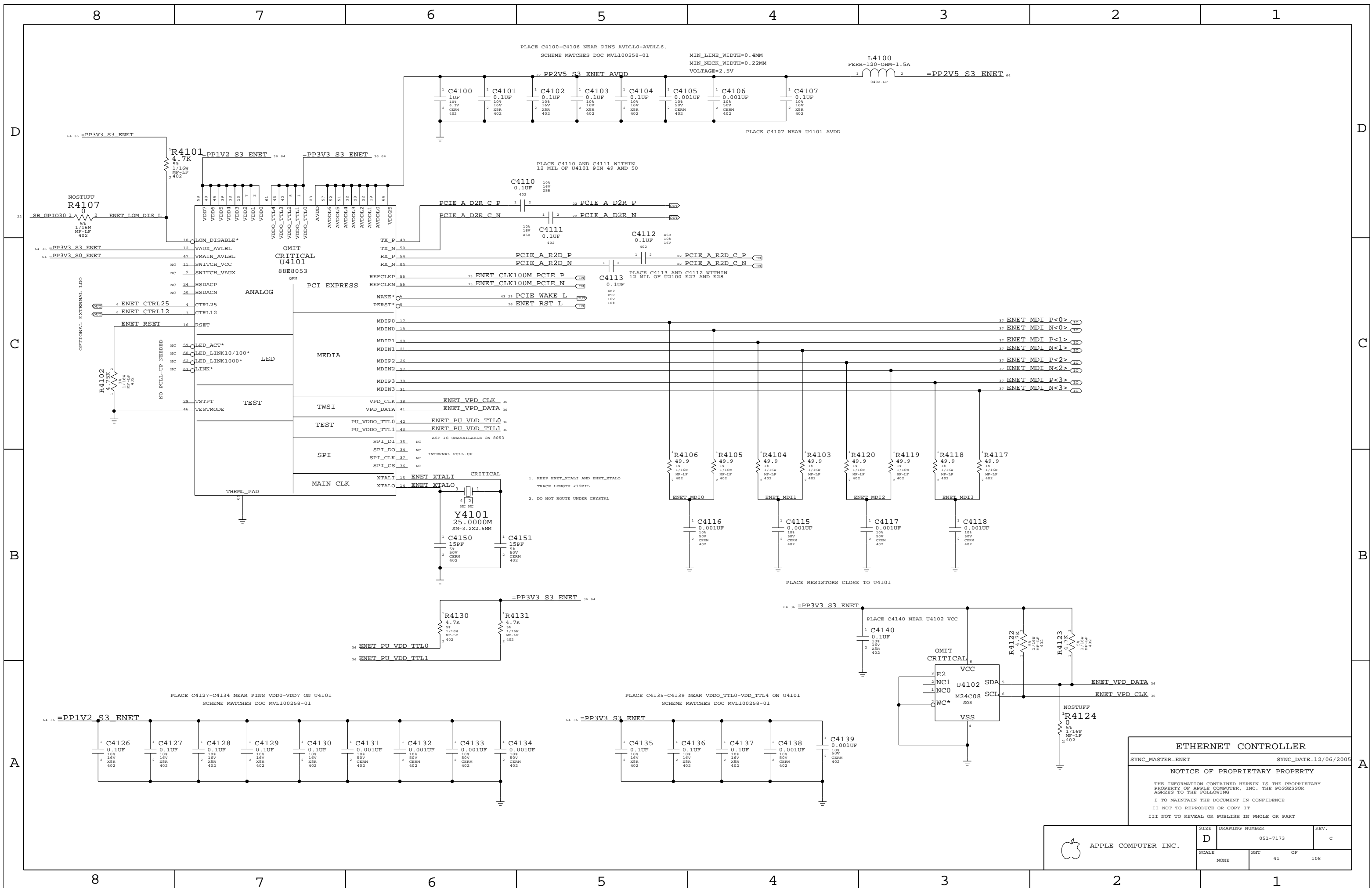
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	SHT	OF	108
NONE	39		

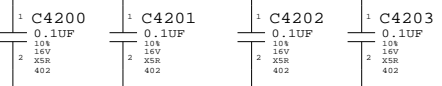


8 7 6 5 4 3 2 1

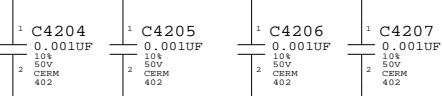
D  
C  
B  
A

L4250  
120-OHM-0.3A-EMI  
PP2V5\_S3\_ENET\_AVDD 1 0402-LF PP2V5\_S3\_ENET\_AVDD\_F

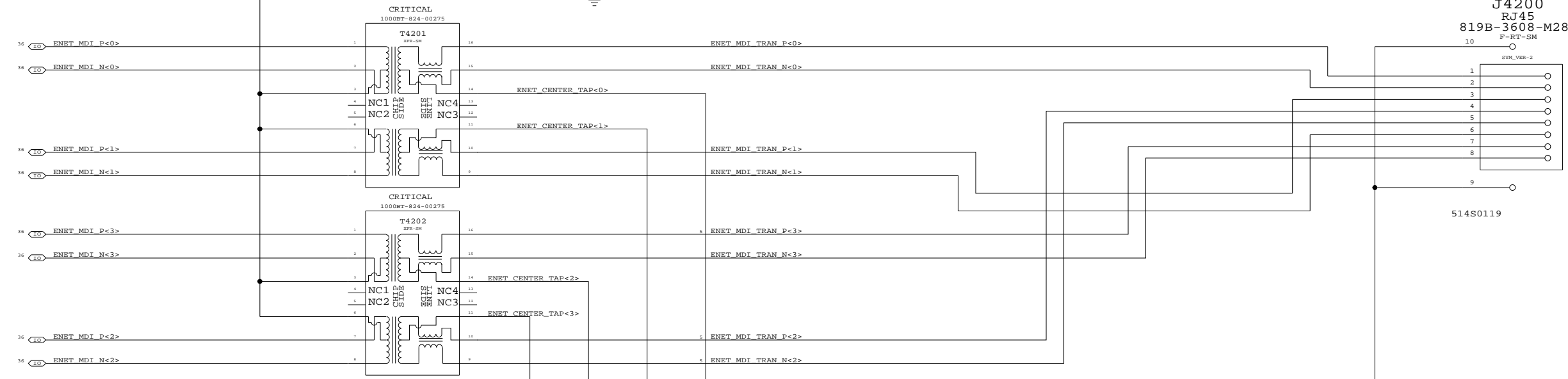
PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS



PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS



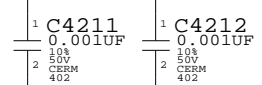
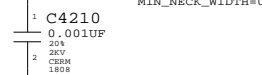
CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
157S0037	157S0011	?	R4201, T4202	SEE AND DELTA TRANSFORMER

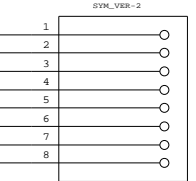


ENET\_BOB\_SMITH\_CAP  
MIN\_LINE\_WIDTH=0.6MM  
MIN\_NECK\_WIDTH=0.25MM



PLACE C4211 AND C4212 ON EACH SIDE OF J4200

OMIT  
CRITICAL  
J4200  
RJ45  
819B-3608-M280  
F-RT-SM



514S0119

ETHERNET CONNECTOR  
SYNC\_MASTER=ENET SYNC\_DATE=11/14/2005

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, SP RJ-45 JACK, MIDDLEPLANE, M33, LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN, SP RJ-45 JACK, MIDDLEPLANE, BLACK, LF	J4200	CRITICAL	FANCY

APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7173	REV. C
SCALE NONE	SHT 42	OF 108

8 7 6 5 4 3 2 1

PAGE NOTES

INPUT
=PP3V3\_S0\_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3\_S0\_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI\_GNT3\_L - PCI GRANT FROM SB
PCI\_CLK\_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI\_RST\_L - PCI RESET FROM SB
FW\_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI\_AD<0..31>, PCI\_C\_BE\_L<0..3>, PCI\_FRAME\_L, PCI\_IRDY\_L, PCI\_TRDY\_L,
PCI\_DEVSEL\_L, PCI\_STOP\_L, PCI\_PAR, PCI\_PERR\_L, PCI\_SERR\_L
FW\_A\_TPA\_P/N, FW\_A\_TPB\_P/N, FW\_A\_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW\_B\_TPA\_P/N, FW\_B\_TPB\_P/N, FW\_B\_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW\_C\_TPA\_P/N, FW\_C\_TPB\_P/N, FW\_C\_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

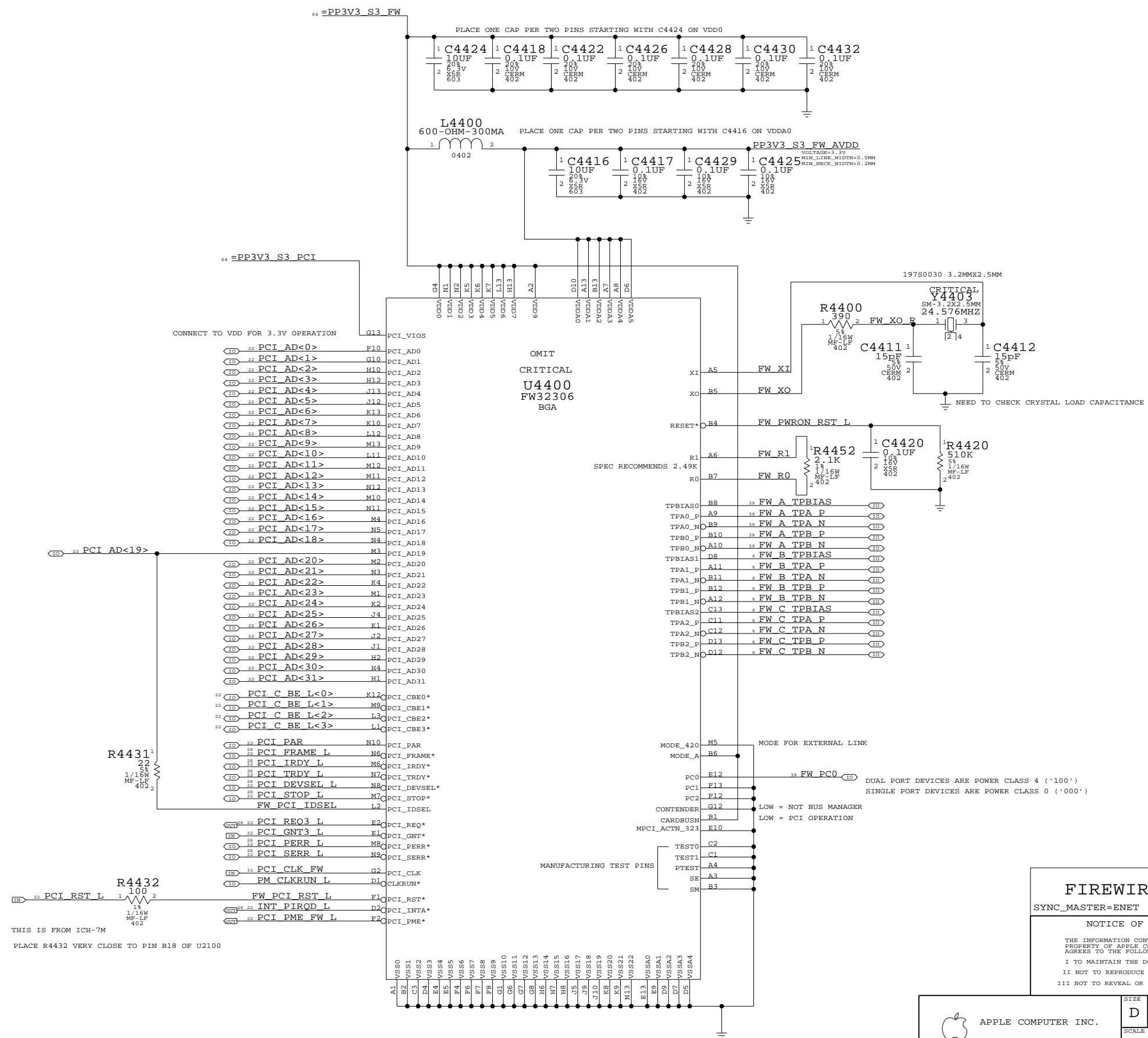
OUTPUT

PCI\_REQ3\_L - PCI REQUEST TO SB
PM\_CLKRUN\_L - CLOCK-RUN PCI PROTOCOL
INT\_PIRQD\_L - INTERRUPT TO SB
PCI\_PME\_FW\_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT\* TO INT\_PIRQD (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI\_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ3/GNT TO REQ3/GNT1 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST\* AND REMOVED CONNECTION TO PLT\_RST\_L
6/22/2005 - CHANGED CLK\_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - CHANGED CLK\_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP



THIS IS FROM ICH-7M
PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

FIREWIRE CONTROLLER
SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

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Table with columns for SCALE, SHEET, OF, and REV. Values: SCALE NONE, SHEET 44, OF 108, REV. C. Includes Apple Computer Inc. logo.

**Page Notes**

INPUT:  
 =PPBUS\_S5\_FWPWRSM - PORT POWER  
 =PP3V3\_S5\_FW - DIGITAL POWER  
 =GND\_CHASSIS\_FW\_PORT0 - CHASSIS GROUND  
 =FWPWR\_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:  
 FW\_TP0\_P/N,FW\_TP0\_P/N,FW\_TPBAS0 - FIREWIRE DIFF PAIRS

OUTPUT:  
 FW\_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

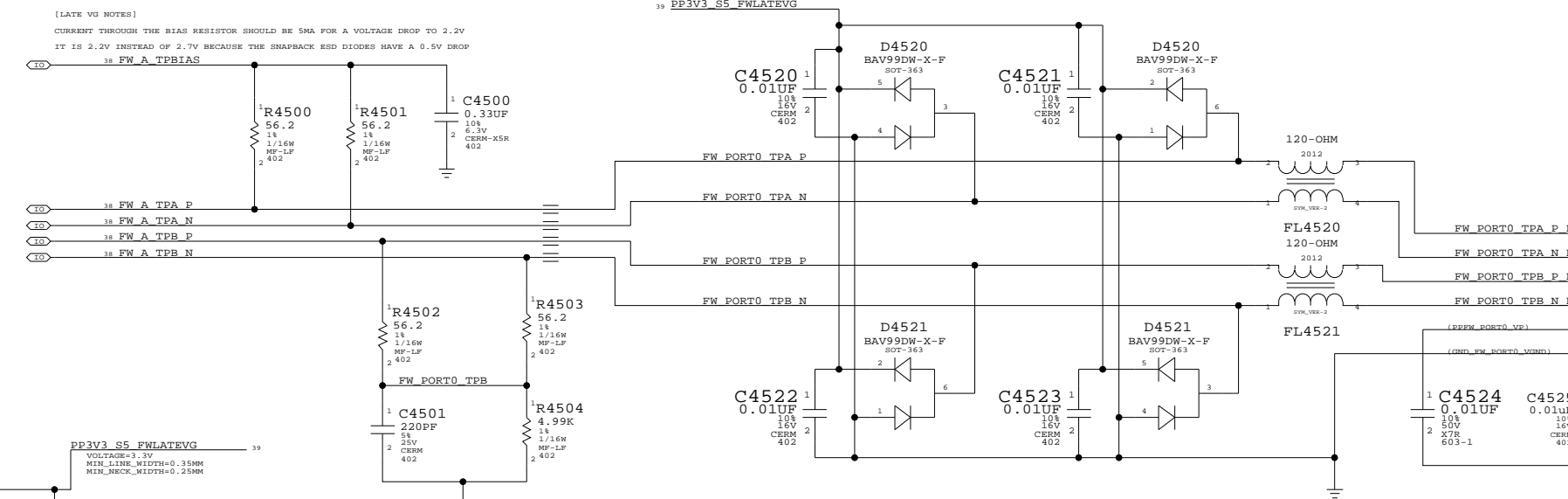
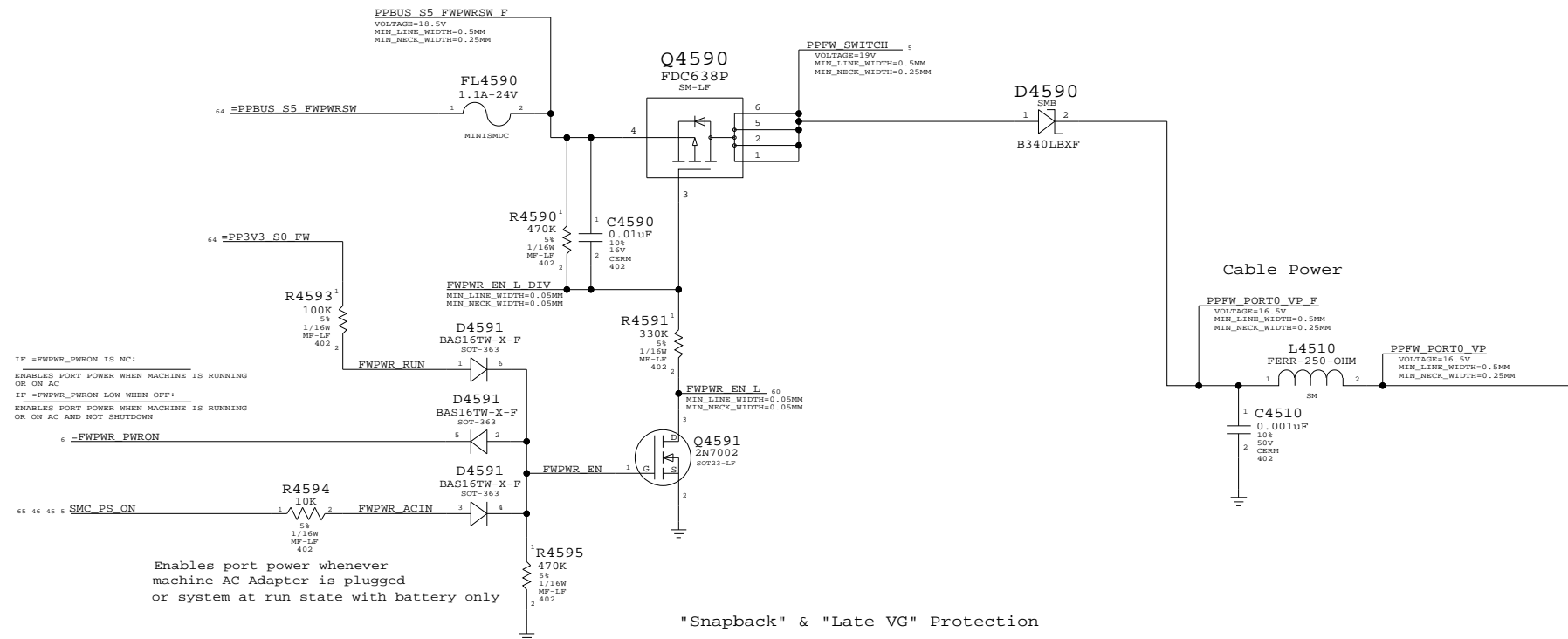
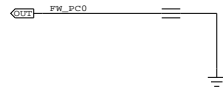
**PAGE HISTORY**

5/19/05 - INITIAL REVISION  
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE  
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER  
 6/22/05 - CONNECTED FW\_PCO FOR SINGLE PORT  
 7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1  
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0  
 7/26/05 - SWITCHED TO 514-0124 FOR FIREWIRE CONNECTOR  
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS  
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION  
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT  
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

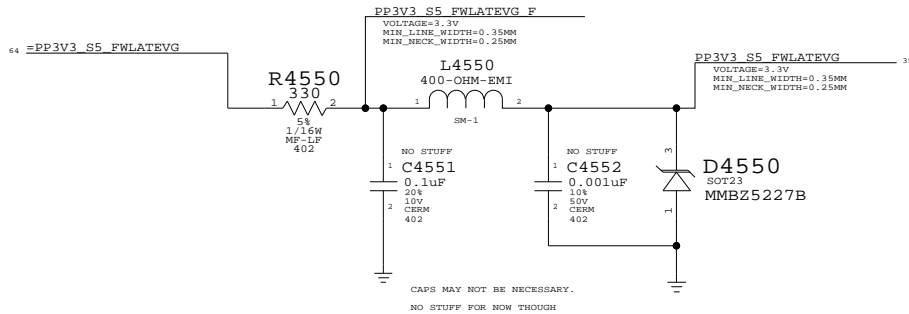
1394b implementation based on Apple  
 FireWire Design Guide (FWDG 0.6, 5/14/03)

**PORT POWER CLASS**

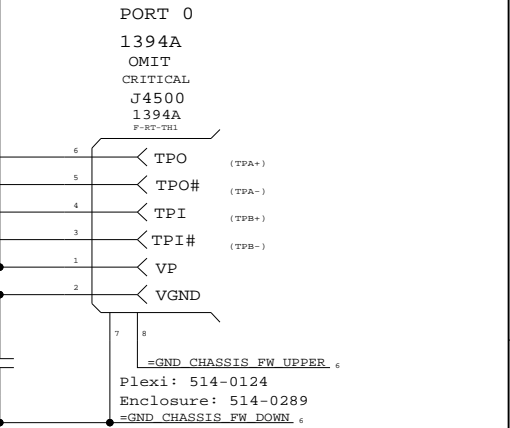
0 FOR SINGLE PORT  
 1 FOR DUAL PORT



**LATE-VG PROTECTION POWER**



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MQ3_LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK_LF	J4500	CRITICAL	FANCY



**FIREWIRE PORT**

SYNC\_MASTER=ENET SYNC\_DATE=11/16/2005

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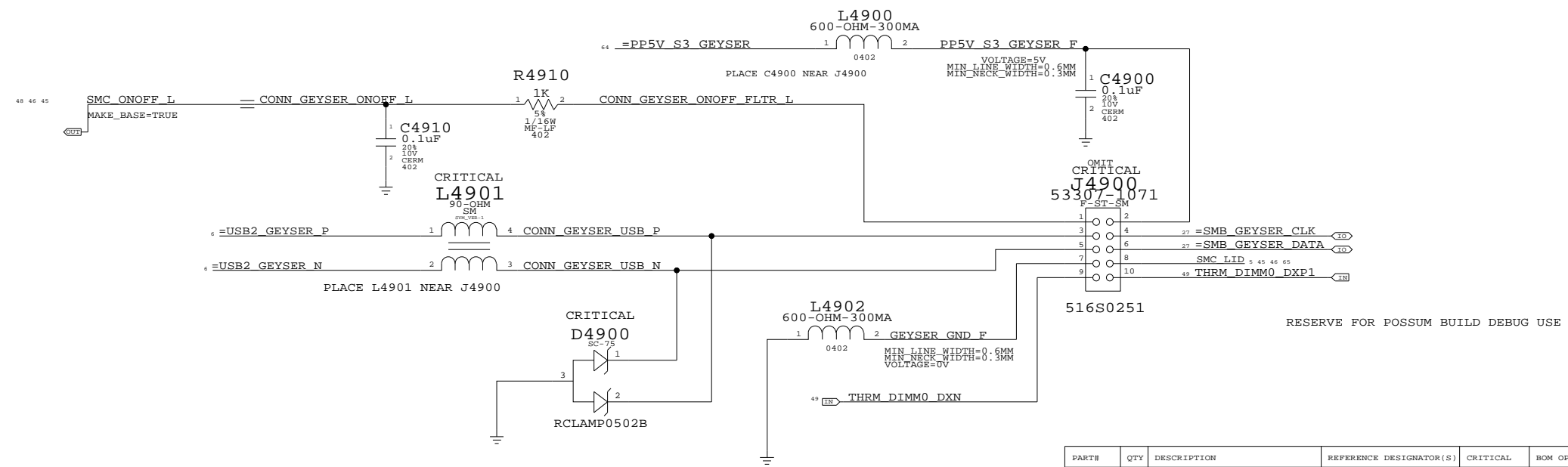
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APPLE COMPUTER INC.

SIZE: D DRAWING NUMBER: 051-7173 REV: C

SCALE: NONE SHEET: 45 OF 108

# GEYSER AND DIMMO REMOTE TEMP SENSORS



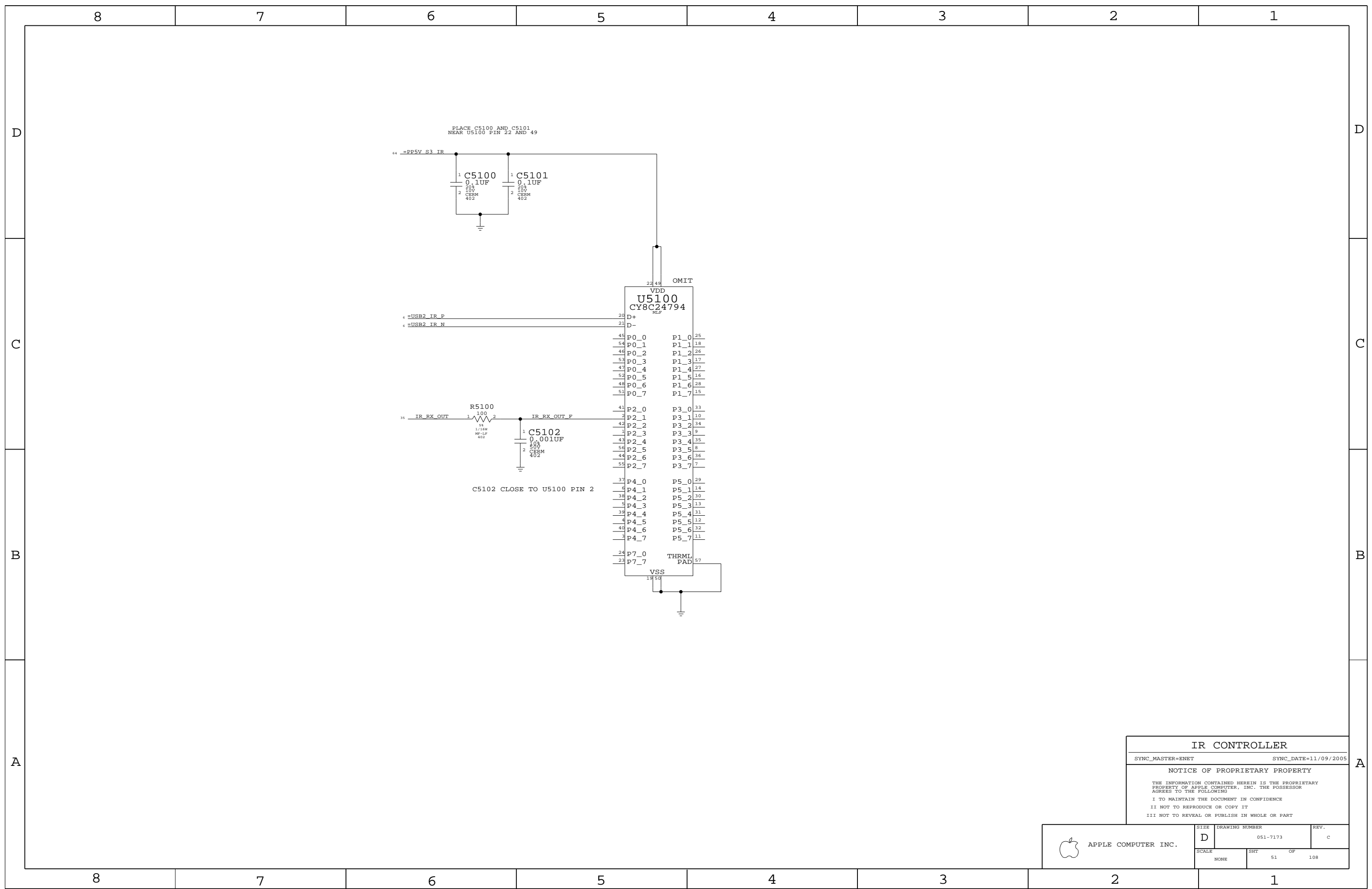
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

**CONNECTOR MISC**  
 SYNC\_MASTER=ENET      SYNC\_DATE=11/16/2005

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHEET 49	OF 108





**IR CONTROLLER**

SYNC\_MASTER=ENET SYNC\_DATE=11/09/2005

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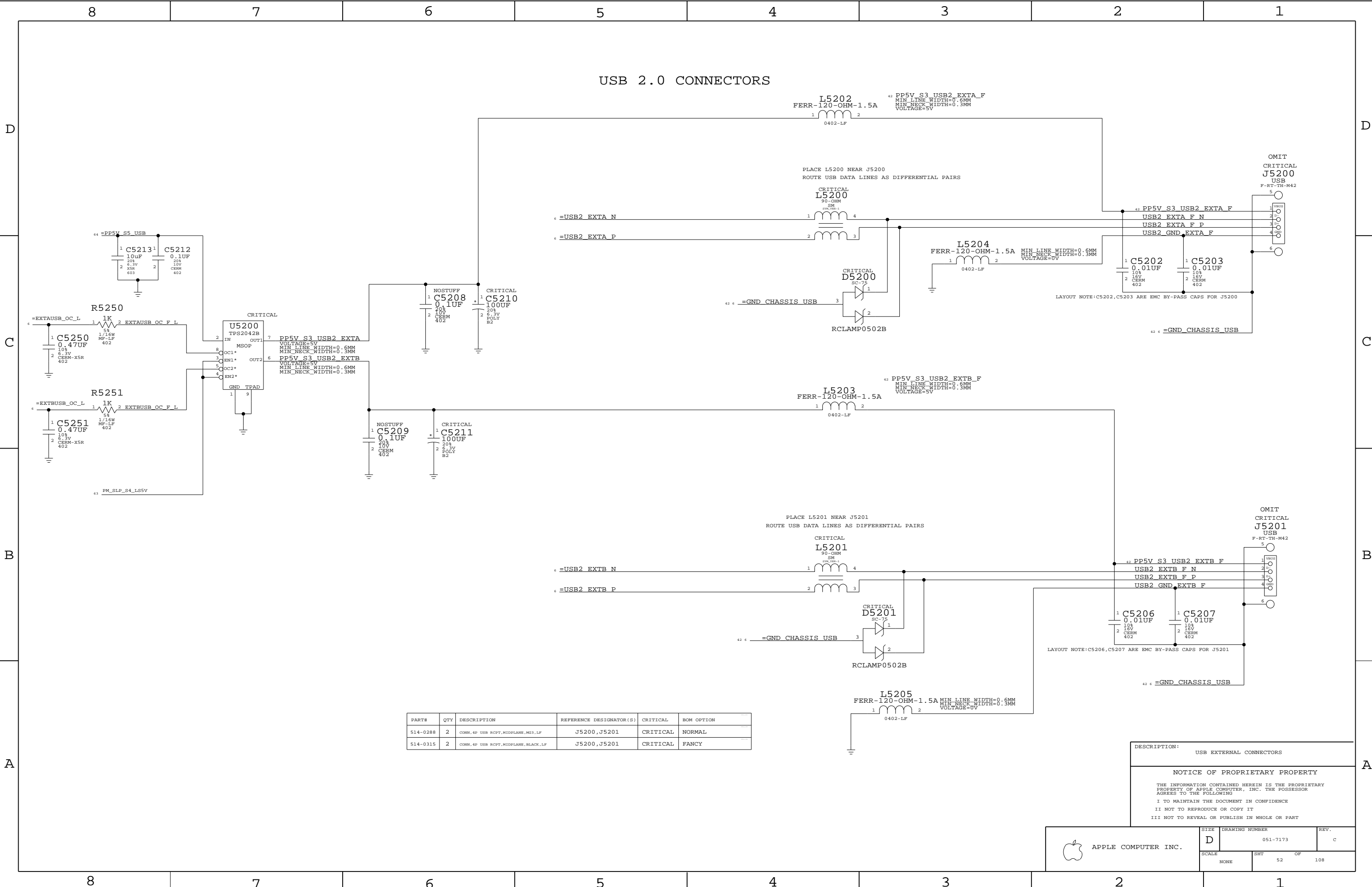
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHEET 51	OF 108

# USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN, 4P USB RCPT, MIDPLANE, W3, LF	J5200, J5201	CRITICAL	NORMAL
514-0315	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J5200, J5201	CRITICAL	FANCY

DESCRIPTION: USB EXTERNAL CONNECTORS

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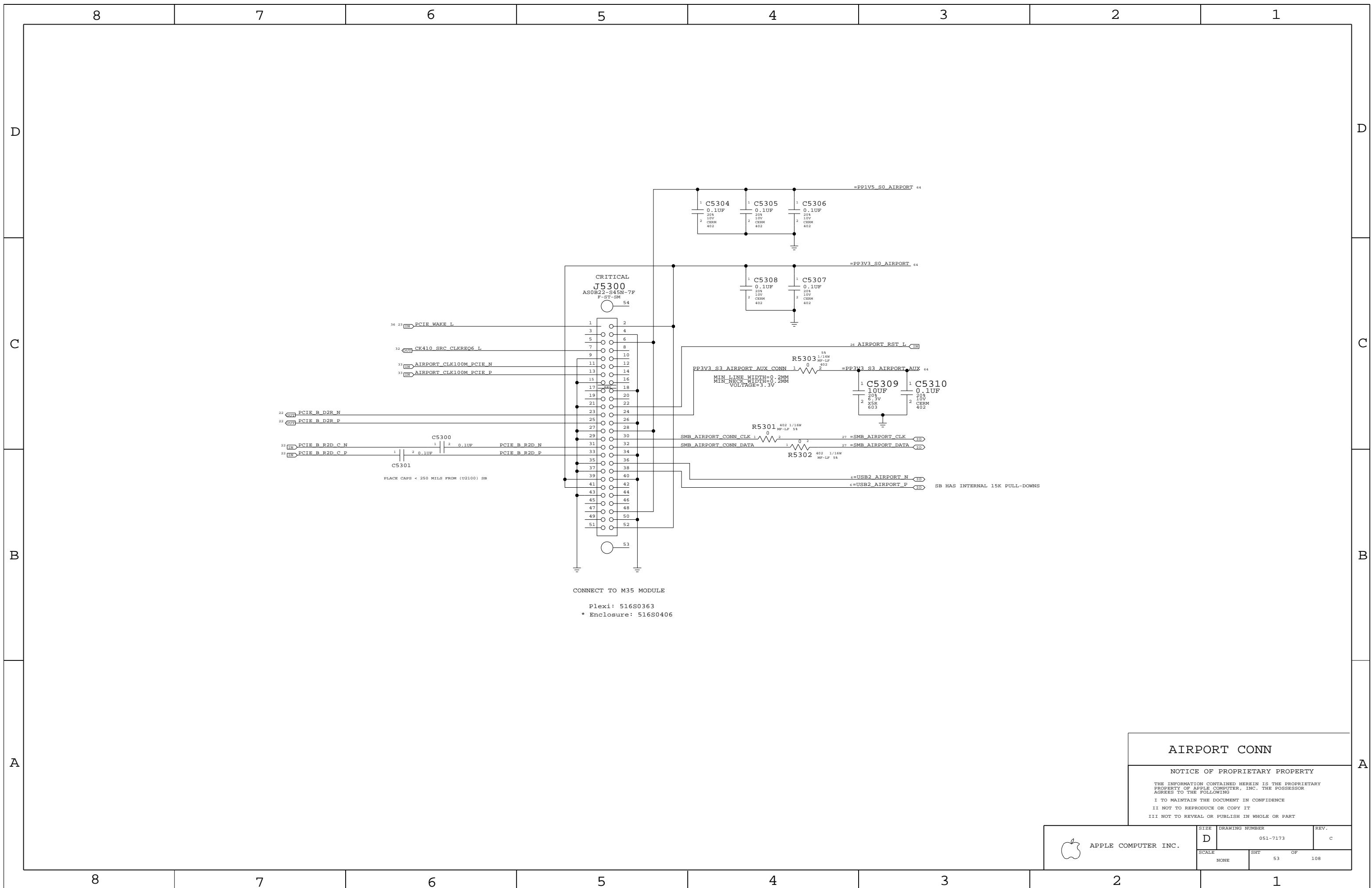
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	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	52	108	




CONNECT TO M35 MODULE

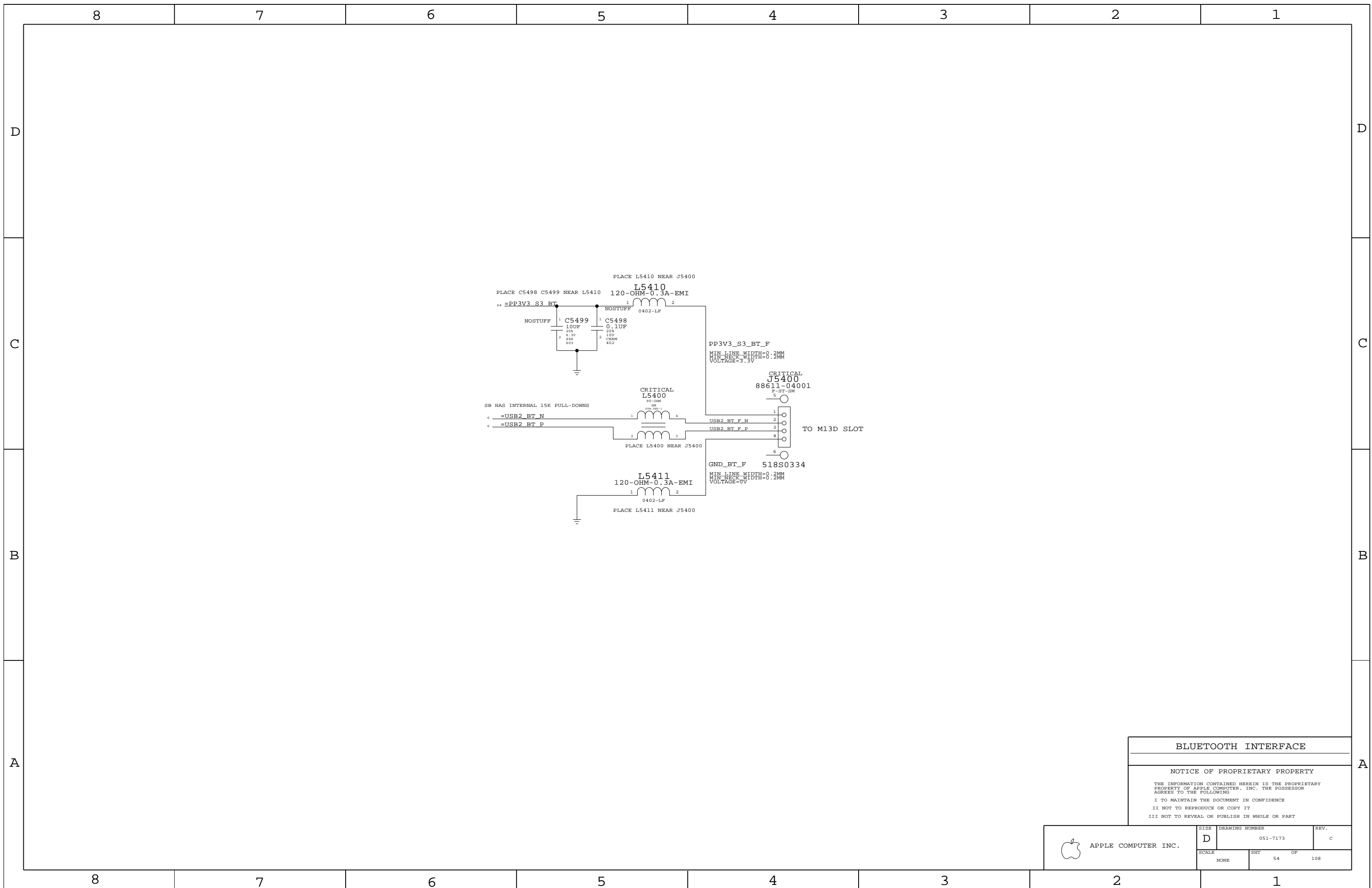
Plexi: 516S0363  
 \* Enclosure: 516S0406

### AIRPORT CONN

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	D	051-7173	C
SCALE	SHT	OF	
NONE	53	108	



**BLUETOOTH INTERFACE**

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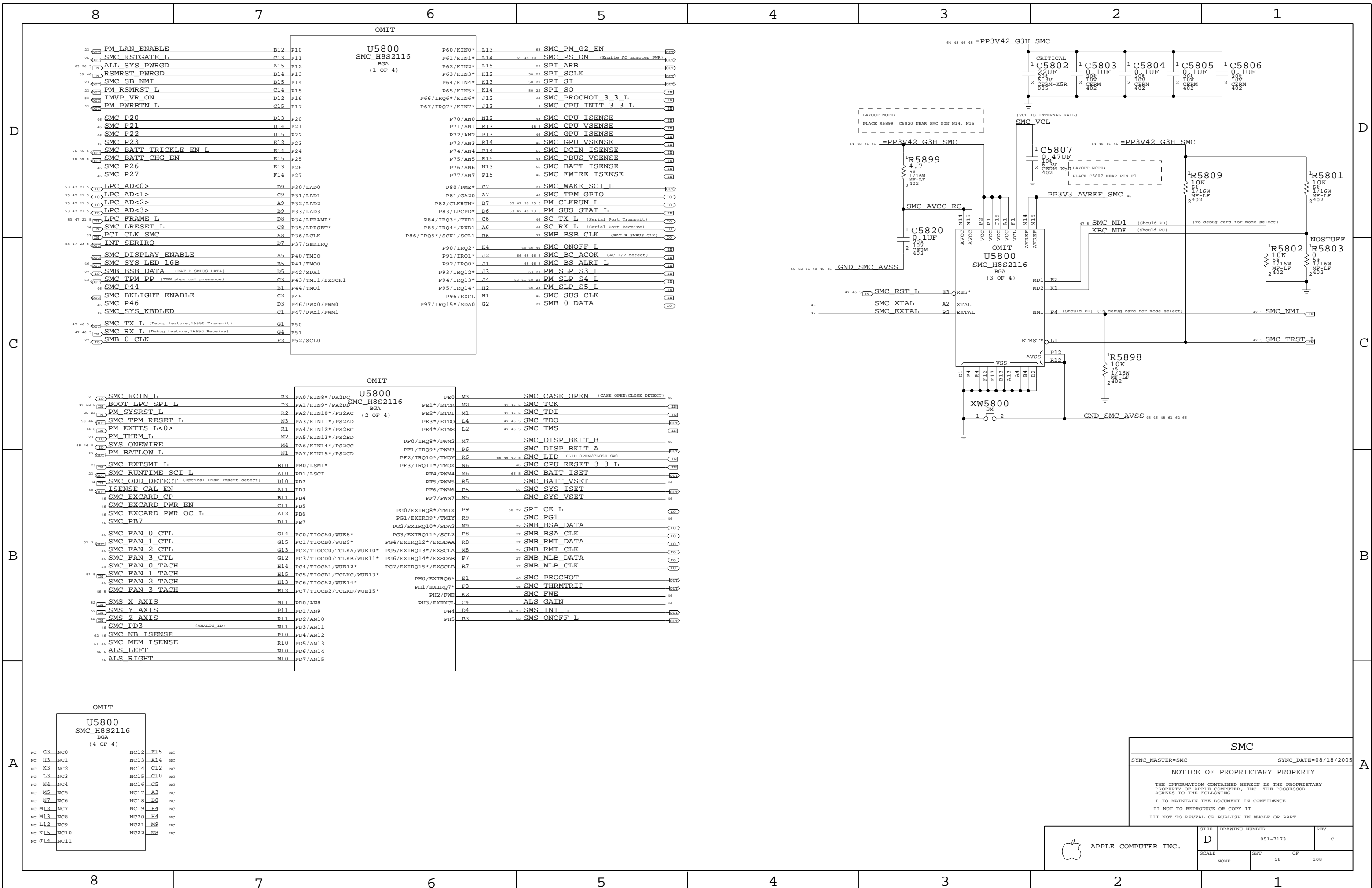
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	SCALE NONE	SHT 54	OF 108



**SMC**

SYNC\_MASTER=SMC SYNC\_DATE=08/18/2005

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	D	051-7173	C
SCALE	SHT	OF	108
NONE	58		

NC G3 NC0

NC12	E15	NC
NC13	A14	NC
NC14	C12	NC
NC15	C10	NC
NC16	C5	NC
NC17	A3	NC
NC18	B8	NC
NC19	E4	NC
NC20	H4	NC
NC21	M9	NC
NC22	N8	NC

NC H3 NC1

NC K3 NC2

NC L3 NC3

NC M4 NC4

NC N5 NC5

NC N7 NC6

NC M12 NC7

NC M13 NC8

NC L12 NC9

NC K15 NC10

NC J14 NC11

OMIT

**U5800**  
SMC\_H8S2116  
BGA  
(4 OF 4)

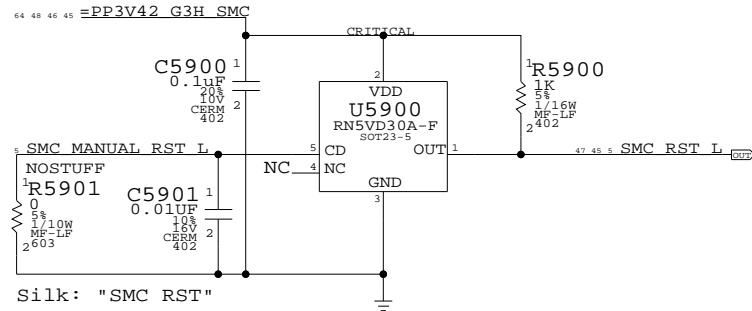
21	SMC RCIN L	R3	PA0/KIN8*/PA2DC	PE0	M3	SMC CASE OPEN (CASE OPEN/CLOSE DETECT)	46
47 22	BOOT LPC SPI L	R3	PA1/KIN9*/PA2DC	PE1*/ETCK	M2	SMC TCK	46
23	PM SYSRST L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	SMC TDI	46
56 46	SMC TPM RESET L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	SMC TDO	46
14	PM EXTTTS L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	SMC TMS	46
23	PM THRM L	N2	PA5/KIN13*/PS2BD				
65 46 5	SYS ONEWIRE	M4	PA6/KIN14*/PS2CC	PF0/IRQ8*/PWM2	M7	SMC DISP BKLT B	46
23	PM BATLOW L	N1	PA7/KIN15*/PS2CD	PF1/IRQ9*/PWM3	P6	SMC DISP BKLT A	46
23	SMC EXTSMI L	B10	PB0/LSMI*	PF2/IRQ10*/TMOY	R6	SMC LID (LID OPEN/CLOSE SW)	46
23	SMC RUNTIME SCI L	A10	PB1/LSCI	PF3/IRQ11*/TMOX	N6	SMC CPU RESET 3 3 L	46
34	SMC_ODD_DETECT (Optical Disk Insert detect)	D10	PB2	PF4/PWM4	M6	SMC BATT ISET	46
48	ISENSE CAL EN	A11	PB3	PF5/PWM5	R5	SMC BATT VSET	46
46	SMC_EXCARD_CP	B11	PB4	PF6/PWM6	E5	SMC SYS ISET	46
46	SMC_EXCARD_PWR_EN	C11	PB5	PF7/PWM7	N5	SMC SYS VSET	46
46	SMC_EXCARD_PWR_OC L	A12	PB6				
46	SMC_PB7	D11	PB7	PG0/EXIRQ8*/TMIX	P9	SMC SPI CE L	46
46	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG1/EXIRQ9*/TMIY	R9	SMC_PG1	46
51 5	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG2/EXIRQ10*/SDA2	N9	SMC_SMB_BSA_DATA	46
46	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG3/EXIRQ11*/SCL2	E8	SMC_SMB_BSA_CLK	46
46	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG4/EXIRQ12*/EXSDAA	RR	SMC_SMB_RMT_DATA	46
46	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG5/EXIRQ13*/EXSCLA	M8	SMC_SMB_RMT_CLK	46
51 5	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PG6/EXIRQ14*/EXSDAB	E7	SMC_SMB_MLB_DATA	46
46	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PG7/EXIRQ15*/EXSCLB	R7	SMC_SMB_MLB_CLK	46
46 5	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*				
52	SMS_X_AXIS	M11	PD0/AN8	PH0/EXIRQ6*	E1	SMC_PROCHOT	46
52	SMS_Y_AXIS	P11	PD1/AN9	PH1/EXIRQ7*	F3	SMC_THRMTRIP	46
52	SMS_Z_AXIS	R11	PD2/AN10	PH2/FWE	K2	SMC_FWE	46
46	SMC_PD3 (ANALOG_ID)	N11	PD3/AN11	PH3/EXEXCL	C4	SMC_ALS_GAIN	46
62	SMC_NB_ISENSE	P10	PD4/AN12				
61	SMC_MEM_ISENSE	R10	PD5/AN13				
46 5	ALS_LEFT	N10	PD6/AN14				
46	ALS_RIGHT	M10	PD7/AN15				

23	PM LAN ENABLE	B12	P10	OMIT			
26	SMC_RSTGATE L	C13	P11	<b>U5800</b> SMC_H8S2116 BGA (1 OF 4)	P60/KIN0*	L13	SMC_PM_G2_EN
63 26 5	ALL_SYS_PWRGD	A15	P12		P61/KIN1*	L14	SMC_PS_ON (Enable AC adapter PWR)
59 46	RSMRST_PWRGD	B14	P13		P62/KIN2*	L15	SPI_ARB
27	SMC_SB_NMI	B15	P14		P63/KIN3*	K12	SPI_SCLK
27	PM_RSMRST L	C14	P15		P64/KIN4*	K13	SPI_SI
50	IMVP_VR_ON	D12	P16		P65/KIN5*	K14	SPI_SO
27	PM_PWRBTN L	C15	P17		P66/IRQ6*/KIN6*	J12	SMC_PROCHOT 3 3 L
46	SMC_P20	D13	P20		P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT 3 3 L
46	SMC_P21	D14	P21				
46	SMC_P22	D15	P22		P70/AN0	N12	SMC_CPU_ISENSE
46	SMC_P23	E12	P23		P71/AN1	R13	SMC_CPU_VSENSE
66 46 5	SMC_BATT_TRICKLE_EN L	E14	P24		P72/AN2	P13	SMC_GPU_ISENSE
66 46 5	SMC_BATT_CHG_EN	E15	P25		P73/AN3	R14	SMC_GPU_VSENSE
46	SMC_P26	E13	P26		P74/AN4	P14	SMC_DCIN_ISENSE
46	SMC_P27	F14	P27		P75/AN5	R15	SMC_PBUS_VSENSE
53 47 21 5	LPC_AD<0>	D9	P30/LAD0		P76/AN6	N13	SMC_BATT_ISENSE
53 47 21 5	LPC_AD<1>	C9	P31/LAD1		P77/AN7	P15	SMC_FWIRE_ISENSE
53 47 21 5	LPC_AD<2>	A9	P32/LAD2				
53 47 21 5	LPC_AD<3>	B9	P33/LAD3		P80/PME*	C7	SMC_WAKE_SCI L
53 47 21 5	LPC_FRAME L	D8	P34/LFRAME*		P81/GA20	A7	SMC_TPM_GPIO
26	SMC_LRESET L	C8	P35/LRESET*		P82/CLKRUN*	B7	PM_CLKRUN L
33	PCI_CLK_SMC	A8	P36/LCLK		P83/LPCPD*	D6	PM_SUS_STAT L
53 47 21 5	INT_SERIRQ	D7	P37/SERIRQ		P84/IRQ3*/TXD1	C6	SC_TX L (Serial Port Transmit)
46	SMC_DISPLAY_ENABLE	A5	P40/TMIO		P85/IRQ4*/RXD1	A6	SC_RX L (Serial Port Receive)
46	SMC_SYS_LED_16B	B5	P41/TMO0		P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK (BAT B SMBUS CLK)
27	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1				
53 47 21 5	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1		P90/IRQ2*	K4	SMC_ONOFF L
46	SMC_P44	B1	P44/TMO1		P91/IRQ1*	J2	SMC_BC_ACOK
46	SMC_BKLIGHT_ENABLE	C2	P45		P92/IRQ0*	J1	SMC_BS_ALRT L
46	SMC_P46	D3	P46/PWX0/PWM0		P93/IRQ12*	J3	PM_SLP_S3 L
46	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1		P94/IRQ13*	J4	PM_SLP_S4 L
47 46 5	SMC_TX L (Debug feature,16550 Transmit)	G1	P50		P95/IRQ14*	H2	PM_SLP_S5 L
47 46 5	SMC_RX L (Debug feature,16550 Receive)	G4	P51		P96/EXCL	H1	SMC_SUS_CLK
27	SMB_0_CLK	E2	P52/SCL0		P97/IRQ15*/SDA0	G2	SMB_0_DATA

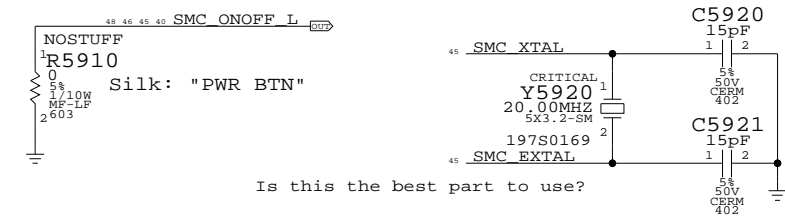
23	PM LAN ENABLE	B12	P10	OMIT			
26	SMC_RSTGATE L	C13	P11	<b>U5800</b> SMC_H8S2116 BGA (1 OF 4)	P60/KIN0*	L13	SMC_PM_G2_EN
63 26 5	ALL_SYS_PWRGD	A15	P12		P61/KIN1*	L14	SMC_PS_ON (Enable AC adapter PWR)
59 46	RSMRST_PWRGD	B14	P13		P62/KIN2*	L15	SPI_ARB
27	SMC_SB_NMI	B15	P14		P63/KIN3*	K12	SPI_SCLK
27	PM_RSMRST L	C14	P15		P64/KIN4*	K13	SPI_SI
50	IMVP_VR_ON	D12	P16		P65/KIN5*	K14	SPI_SO
27	PM_PWRBTN L	C15	P17		P66/IRQ6*/KIN6*	J12	SMC_PROCHOT 3 3 L
46	SMC_P20	D13	P20		P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT 3 3 L
46	SMC_P21	D14	P21				
46	SMC_P22	D15	P22		P70/AN0	N12	SMC_CPU_ISENSE
46	SMC_P23	E12	P23		P71/AN1	R13	SMC_CPU_VSENSE
66 46 5	SMC_BATT_TRICKLE_EN L	E14	P24		P72/AN2	P13	SMC_GPU_ISENSE
66 46 5	SMC_BATT_CHG_EN	E15	P25		P73/AN3	R14	SMC_GPU_VSENSE
46	SMC_P26	E13	P26		P74/AN4	P14	SMC_DCIN_ISENSE
46	SMC_P27	F14	P27		P75/AN5	R15	SMC_PBUS_VSENSE
53 47 21 5	LPC_AD<0>	D9	P30/LAD0		P76/AN6	N13	SMC_BATT_ISENSE
53 47 21 5	LPC_AD<1>	C9	P31/LAD1		P77/AN7	P15	SMC_FWIRE_ISENSE
53 47 21 5	LPC_AD<2>	A9	P32/LAD2				
53 47 21 5	LPC_AD<3>	B9	P33/LAD3		P80/PME*	C7	SMC_WAKE_SCI L
53 47 21 5	LPC_FRAME L	D8	P34/LFRAME*		P81/GA20	A7	SMC_TPM_GPIO
26	SMC_LRESET L	C8	P35/LRESET*		P82/CLKRUN*	B7	PM_CLKRUN L
33	PCI_CLK_SMC	A8	P36/LCLK		P83/LPCPD*	D6	PM_SUS_STAT L
53 47 21 5	INT_SERIRQ	D7	P37/SERIRQ		P84/IRQ3*/TXD1	C6	SC_TX L (Serial Port Transmit)
46	SMC_DISPLAY_ENABLE	A5	P40/TMIO		P85/IRQ4*/RXD1	A6	SC_RX L (Serial Port Receive)
46	SMC_SYS_LED_16B	B5	P41/TMO0		P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK (BAT B SMBUS CLK)
27	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1				
53 47 21 5	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1		P90/IRQ2*	K4	SMC_ONOFF L
46	SMC_P44	B1	P44/TMO1		P91/IRQ1*	J2	SMC_BC_ACOK
46	SMC_BKLIGHT_ENABLE	C2	P45		P92/IRQ0*	J1	SMC_BS_ALRT L
46	SMC_P46	D3	P46/PWX0/PWM0		P93/IRQ12*	J3	PM_SLP_S3 L
46	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1		P94/IRQ13*	J4	PM_SLP_S4 L
47 46 5	SMC_TX L (Debug feature,16550 Transmit)	G1	P50		P95/IRQ14*	H2	PM_SLP_S5 L
47 46 5	SMC_RX L (Debug feature,16550 Receive)	G4	P51		P96/EXCL	H1	SMC_SUS_CLK
27	SMB_0_CLK	E2	P52/SCL0		P97/IRQ15*/SDA0	G2	SMB_0_DATA

23	PM LAN ENABLE	B12	P10	OMIT			
26	SMC_RSTGATE L	C13	P11	<b>U5800</b> SMC_H8S2116 BGA (1 OF 4)	P60/KIN0*	L13	SMC_PM_G2_EN
63 26 5	ALL_SYS_PWRGD	A15	P12		P61/KIN1*	L14	SMC_PS_ON (Enable AC adapter PWR)
59 46	RSMRST_PWRGD	B14	P13		P62/KIN2*	L15	SPI_ARB
27	SMC_SB_NMI	B15	P14		P63/KIN3*	K12	SPI_SCLK
27	PM_RSMRST L	C14	P15		P64/KIN4*	K13	SPI_SI
50	IMVP_VR_ON	D12	P16		P65/KIN5*	K14	SPI_SO
27	PM_PWRBTN L	C15	P17		P66/IRQ6*/KIN6*	J12	SMC_PROCHOT 3 3 L
46	SMC_P20	D13	P20		P67/IRQ7*/KIN7*	J13	SMC_CPU_INIT 3 3 L
46	SMC_P21	D14	P21				
46	SMC_P22	D15	P22		P70/AN0	N12	SMC_CPU_ISENSE
46	SMC_P23	E12	P23		P71/AN1	R13	SMC_CPU_VSENSE
66 46 5	SMC_BATT_TRICKLE_EN L	E14	P24		P72/AN2	P13	SMC_GPU_ISENSE
66 46 5	SMC_BATT_CHG_EN	E15	P25		P73/AN3	R14	SMC_GPU_VSENSE
46	SMC_P26	E13	P26		P74/AN4	P14	SMC_DCIN_ISENSE
46	SMC_P27	F14	P27		P75/AN5	R15	SMC_PBUS_VSENSE
53 47 21 5	LPC_AD<0>	D9	P30/LAD0		P76/AN6	N13	SMC_BATT_ISENSE
53 47 21 5	LPC_AD<1>	C9	P31/LAD1		P77/AN7	P15	SMC_FWIRE_ISENSE
53 47 21 5	LPC_AD<2>	A9	P32/LAD2				
53 47 21 5	LPC_AD<3>	B9	P33/LAD3		P80/PME*	C7	SMC_WAKE_SCI L
53 47 21 5	LPC_FRAME L	D8	P34/LFRAME*		P81/GA20	A7	SMC_TPM_GPIO
26	SMC_LRESET L	C8	P35/LRESET*		P82/CLKRUN*	B7	PM_CLKRUN L
33	PCI_CLK_SMC	A8	P36/LCLK		P83/LPCPD*	D6	PM_SUS_STAT L
53 47 21 5	INT_SERIRQ	D7	P37/SERIRQ		P84/IRQ3*/TXD1	C6	SC_TX L (Serial Port Transmit)
46	SMC_DISPLAY_ENABLE	A5	P40/TMIO		P85/IRQ4*/RXD1	A6	SC_RX L (Serial Port Receive)
46	SMC_SYS_LED_16B	B5	P41/TMO0		P86/IRQ5*/SCK1/SCL1	B6	SMB_BSB_CLK (BAT B SMBUS CLK)
27	SMB_BSB_DATA (BAT B SMBUS DATA)	D5	P42/SDA1				
53 47 21 5	SMC_TPM_PP (TPM physical presence)	C3	P43/TMI1/EXSCK1		P90/IRQ2*	K4	SMC_ONOFF L
46	SMC_P44	B1	P44/TMO1		P91/IRQ1*	J2	SMC_BC_ACOK
46	SMC_BKLIGHT_ENABLE	C2	P45		P92/IRQ0*	J1	SMC_BS_ALRT L
46	SMC_P46	D3	P46/PWX0/PWM0		P93/IRQ12*	J3	PM_SLP_S3 L
46	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1</				

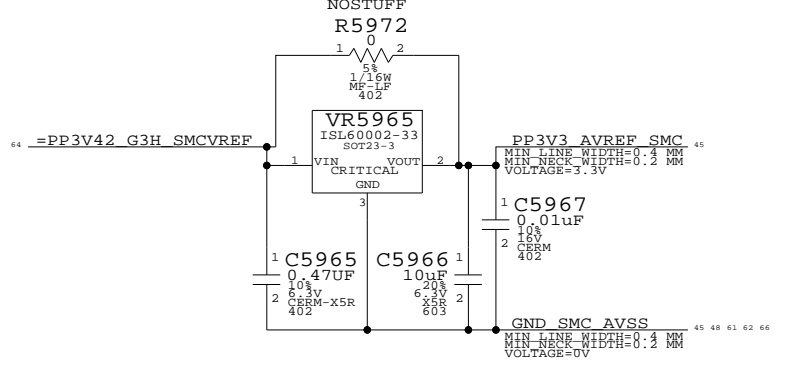
SMC Reset Button / Brownout Detect



Debug Power Button SMC Crystal Circuit

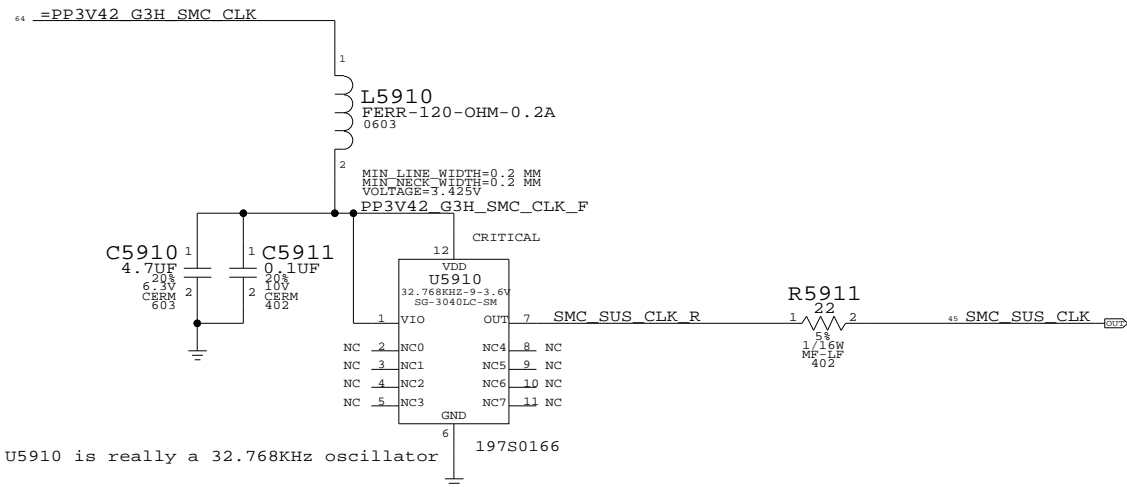


SMC AVREF Supply



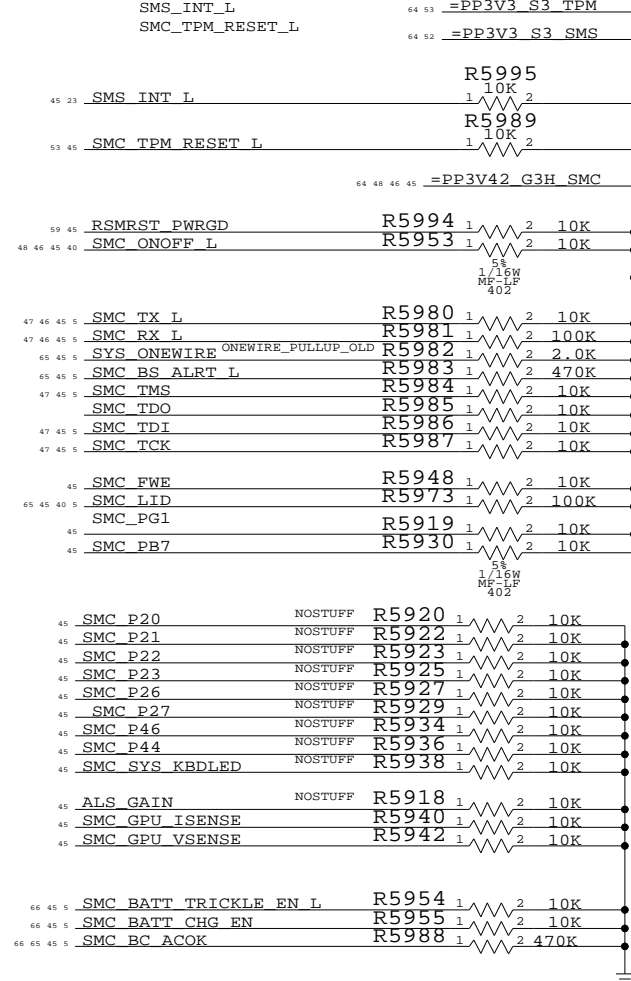
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

SMC G3HOT OSCILLATOR

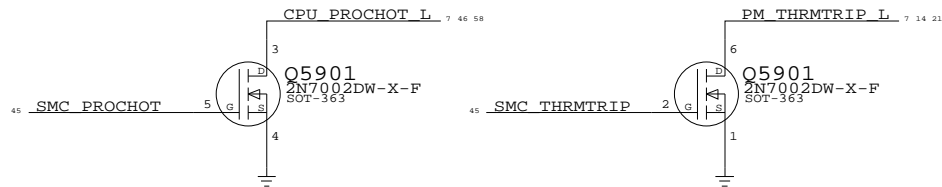


U5910 is really a 32.768KHz oscillator 197S0166

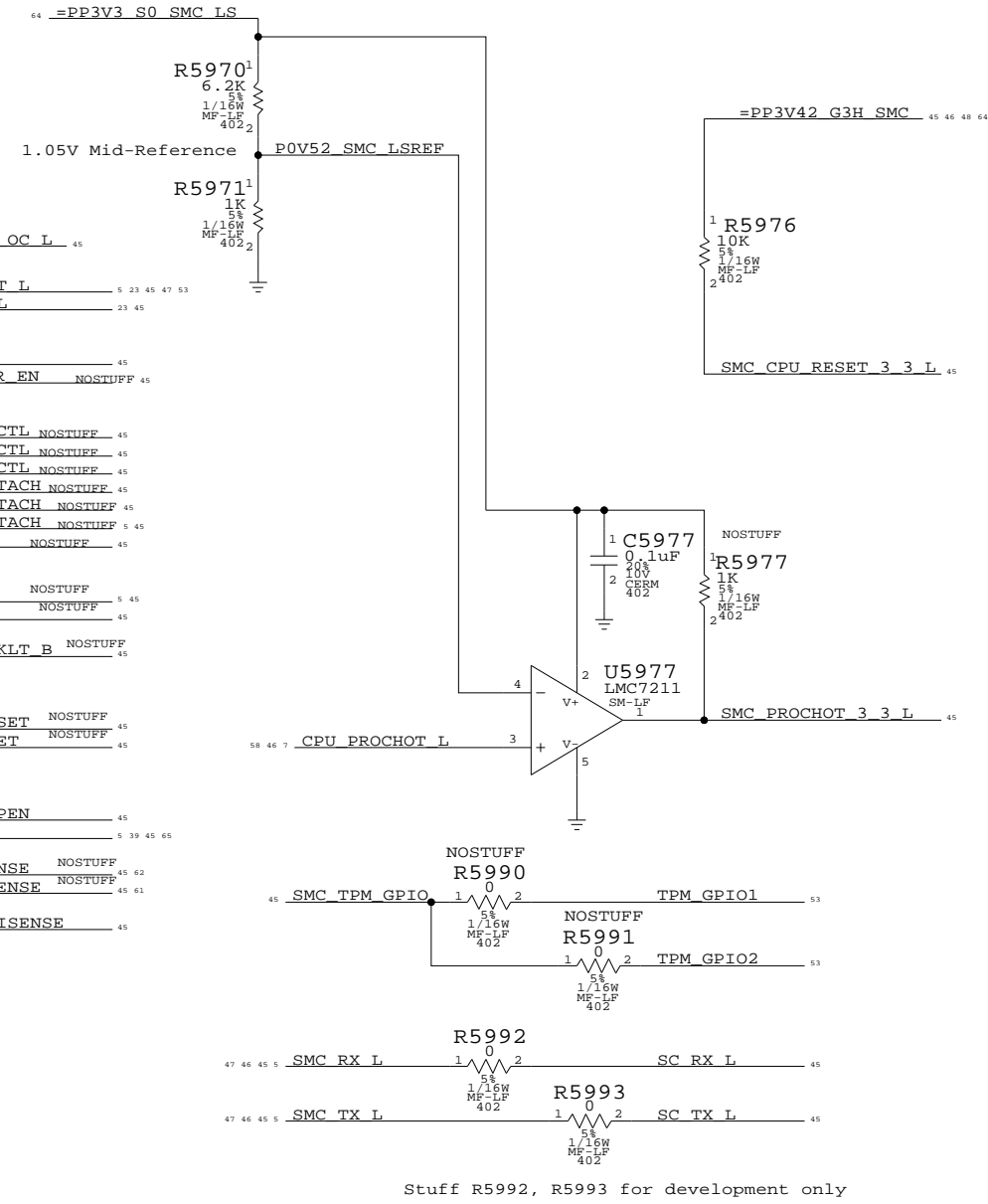
THESE NEED TO BE PULLED TO THE PROPER RAIL:



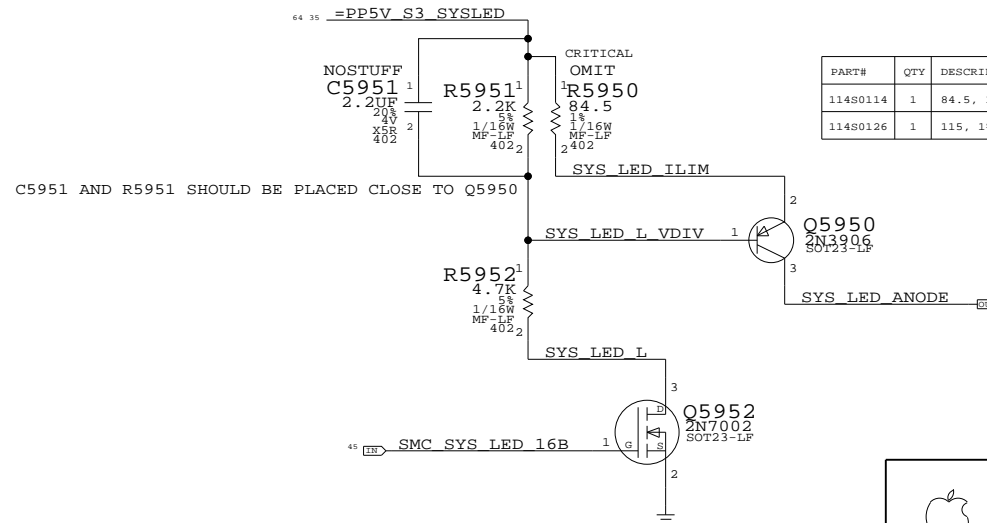
SMC 3.3V to 1.05V Level Shifting



SMC 1.05V to 3.3V Level Shifting



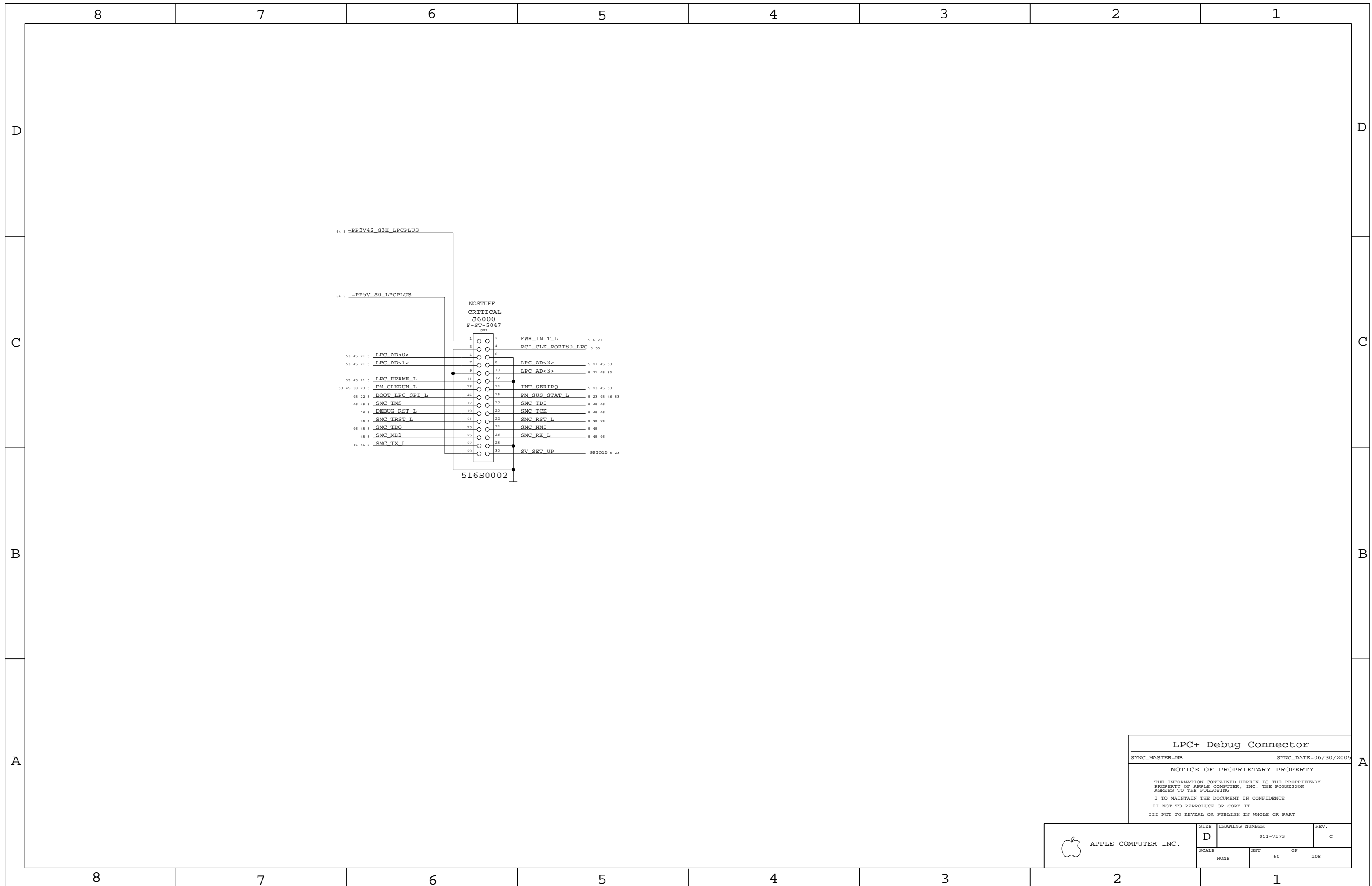
System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
11480126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

**SMC SUPPORT**  
 SYNC\_MASTER=SMC SYNC\_DATE=08/23/2005  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	59		



**LPC+ Debug Connector**

SYNC\_MASTER=NB SYNC\_DATE=06/30/2005

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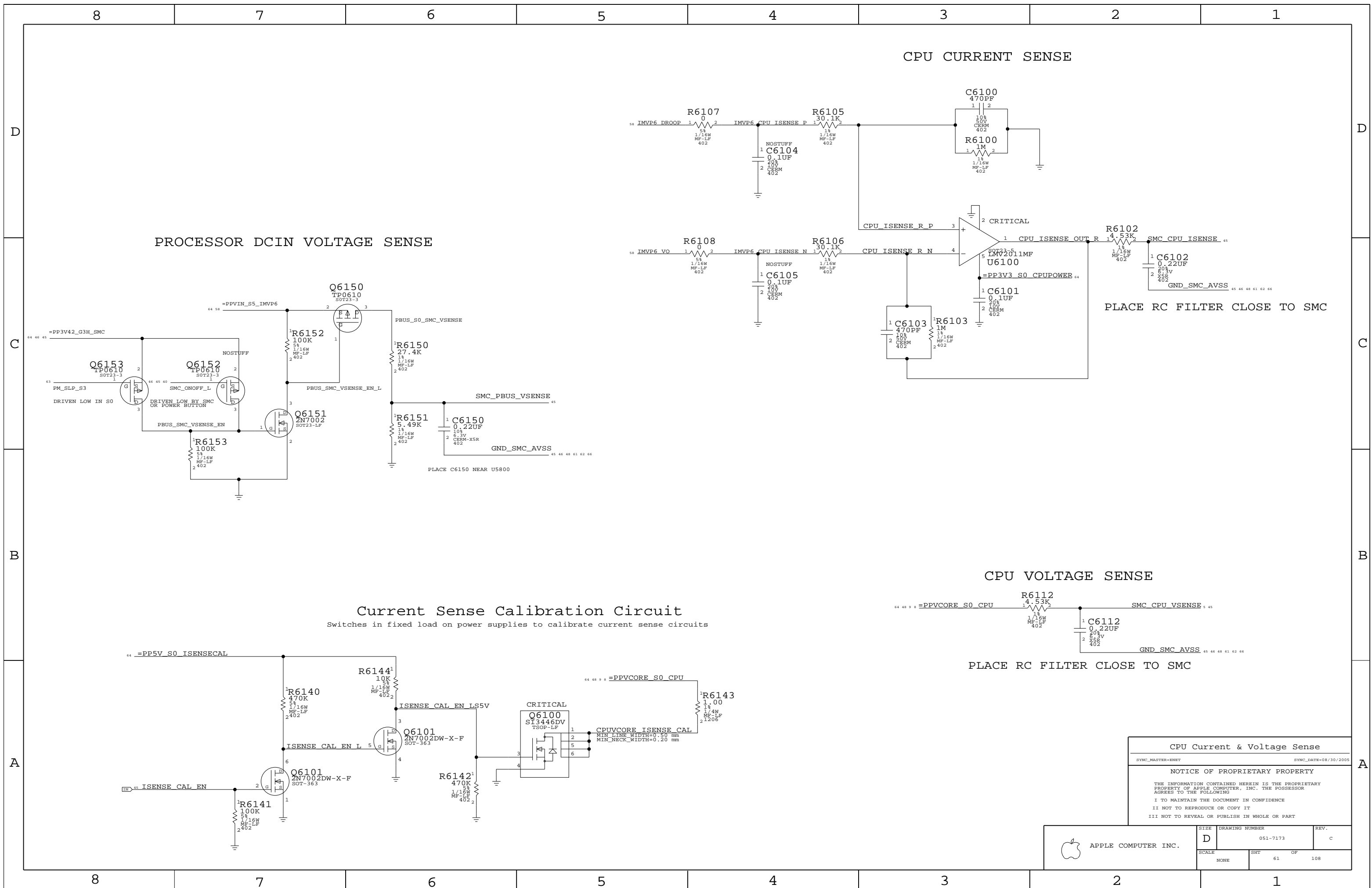
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	SCALE NONE	SHEETS 60	OF 108



PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

CPU VOLTAGE SENSE

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

PLACE RC FILTER CLOSE TO SMC

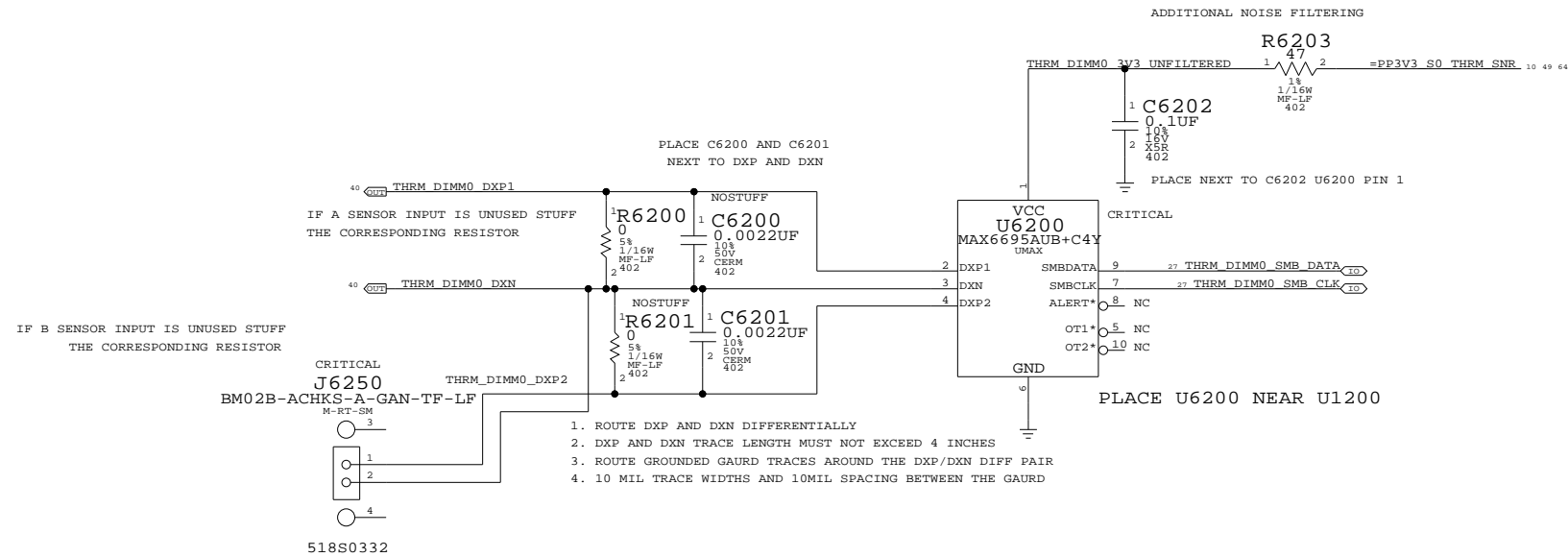
PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense  
 SYNC\_MASTER=EMBT SYNC\_DATE=08/30/2005  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	61		

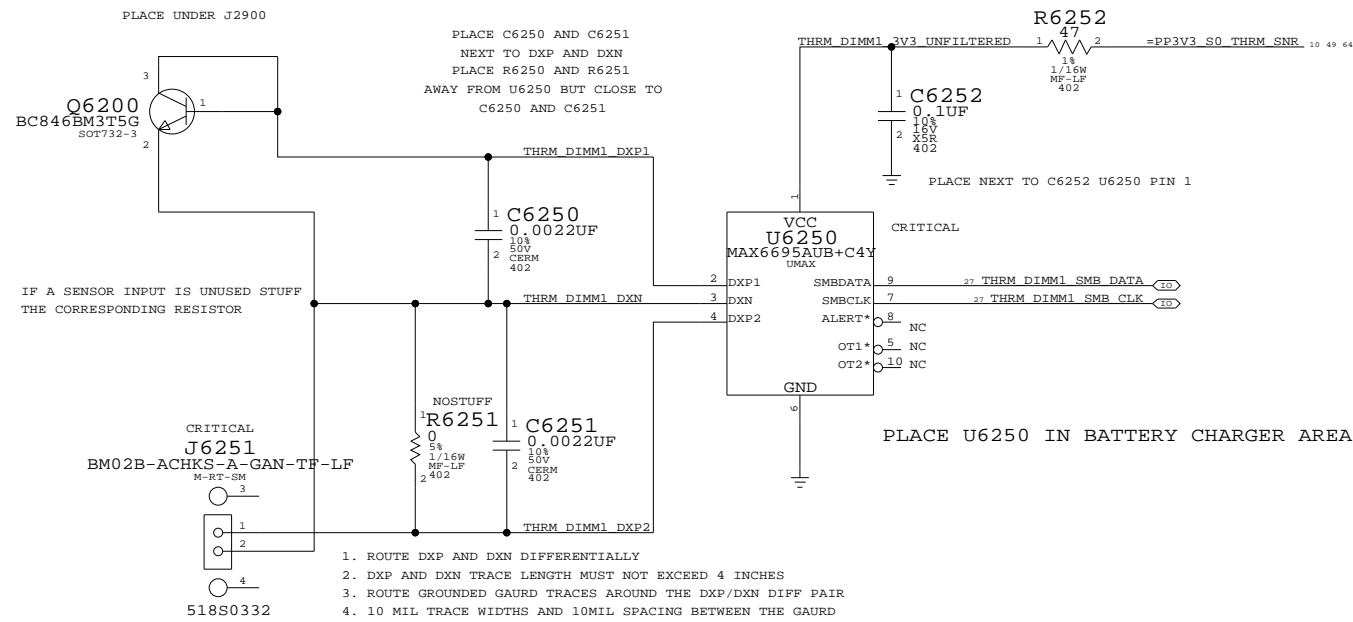


### DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452  
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

### DIMM1 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452  
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

#### TEMPERATURE SENSE

SYNC\_MASTER=ENET SYNC\_DATE=11/09/2005

#### NOTICE OF PROPRIETARY PROPERTY

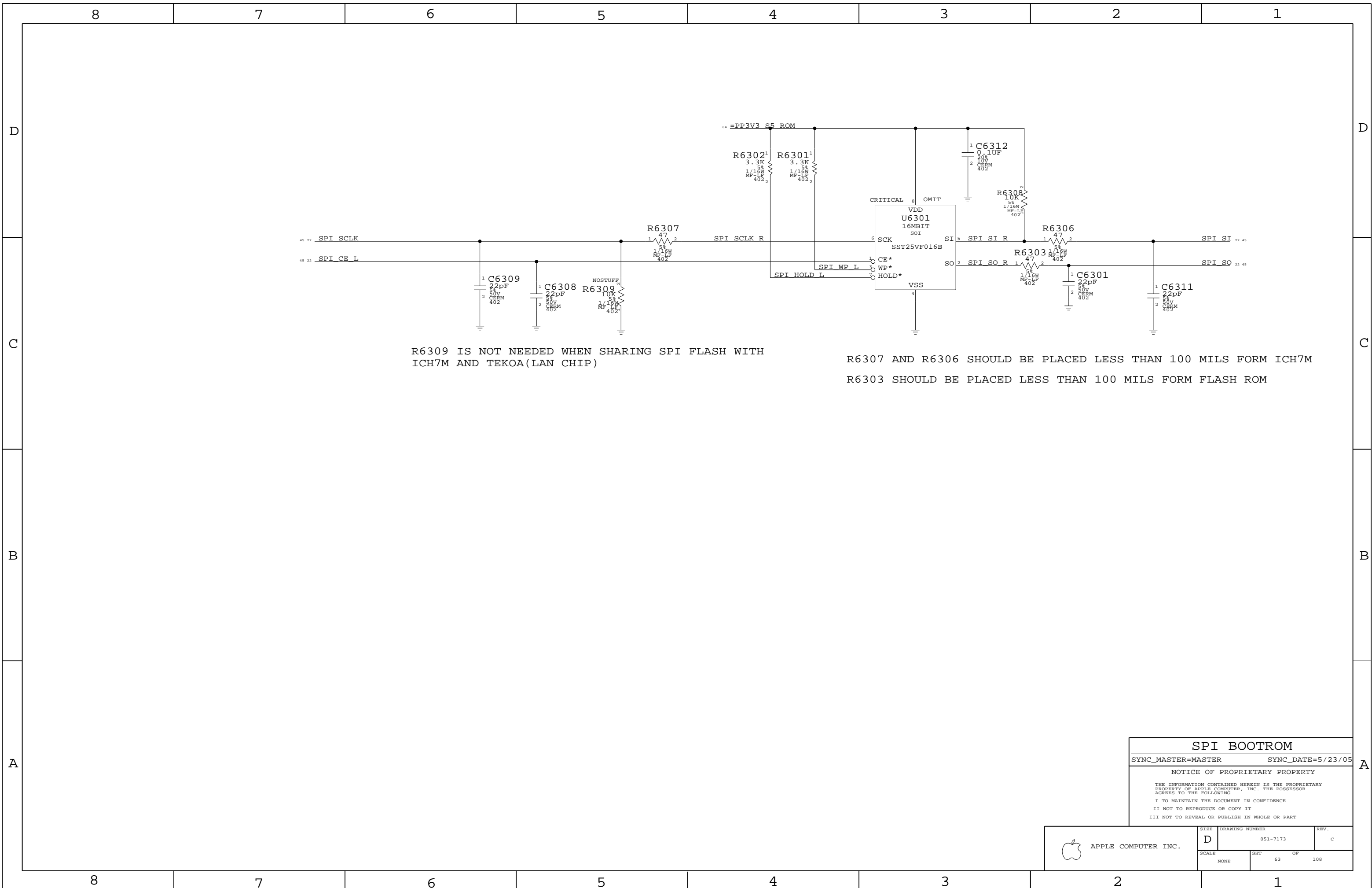
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	62	108	



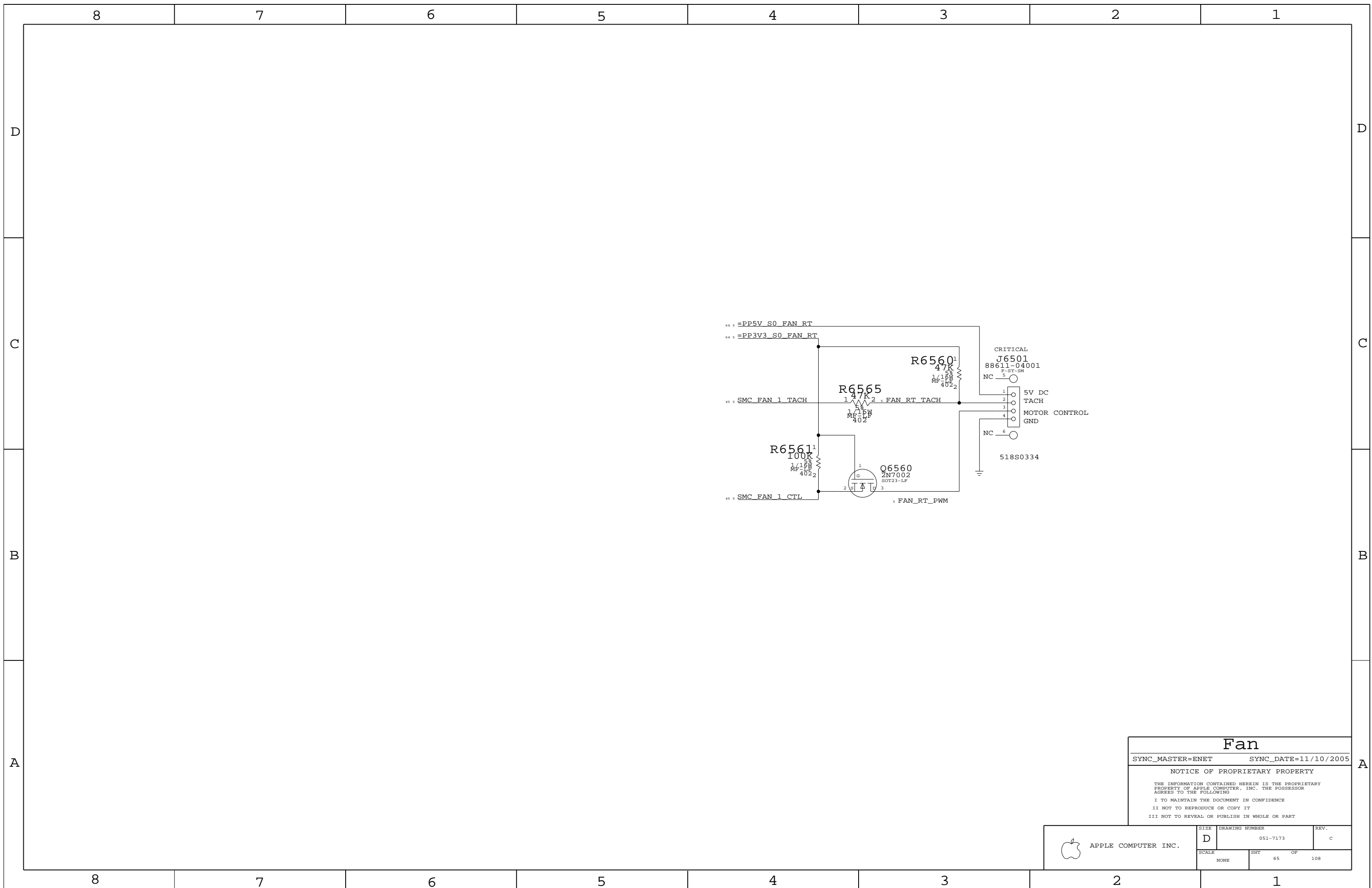
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M  
 R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

**SPI BOOTROM**

SYNC\_MASTER=MASTER      SYNC\_DATE=5/23/05  
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHIT 63	OF 108



**Fan**

SYNC\_MASTER=ENET      SYNC\_DATE=11/10/2005

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHIT 65	OF 108

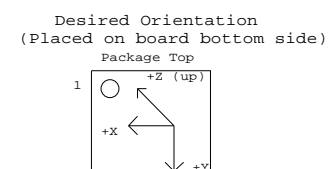
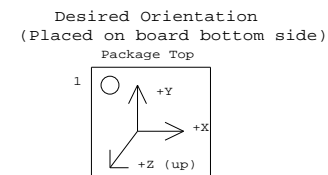
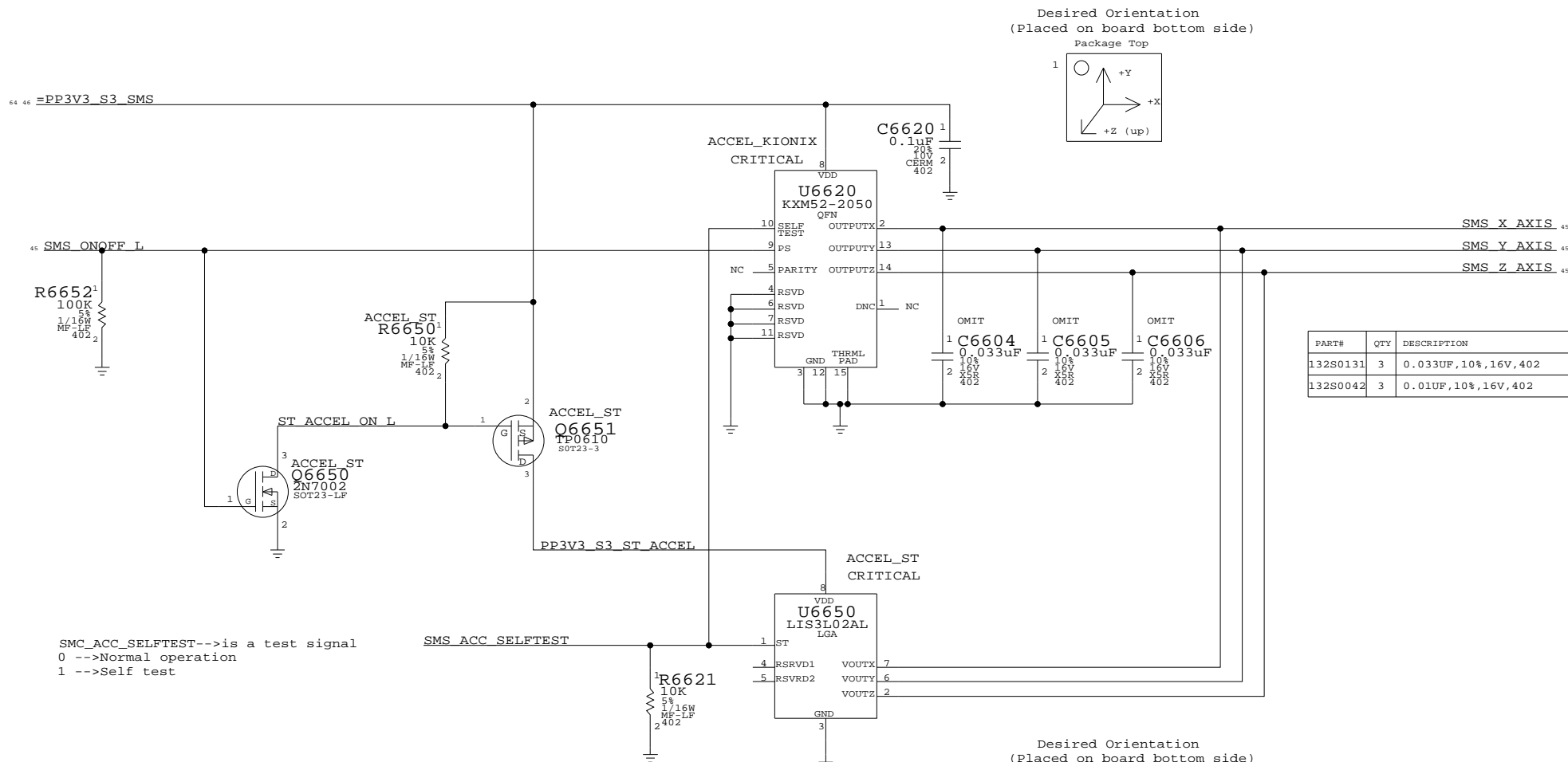
PAGE NOTES

INPUT  
 =PP3V3\_S3\_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)  
 SMS\_ONOFF\_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT  
 SMS\_ACC\_\*\_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE  
 7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050  
 7/26/2005 - CONNECTED PD PIN TO SMC'S SMS\_ONOFF\_L  
 7/26/2005 -



R6652  
 100K  
 5%  
 1/16W  
 MF-LF  
 402

ACCEL\_ST  
 R6650  
 10K  
 5%  
 1/16W  
 MF-LF  
 402

ACCEL\_ST  
 Q6650  
 2N7002  
 SOT23-LF

R6621  
 10K  
 5%  
 1/16W  
 MF-LF  
 402

C6620  
 0.1uF  
 10%  
 CERM  
 402

C6604  
 0.033uF  
 10%  
 16V  
 X5R  
 402

C6605  
 0.033uF  
 10%  
 16V  
 X5R  
 402

C6606  
 0.033uF  
 10%  
 16V  
 X5R  
 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMC\_ACC\_SELFTEST-->is a test signal  
 0 -->Normal operation  
 1 -->Self test

**SMS**

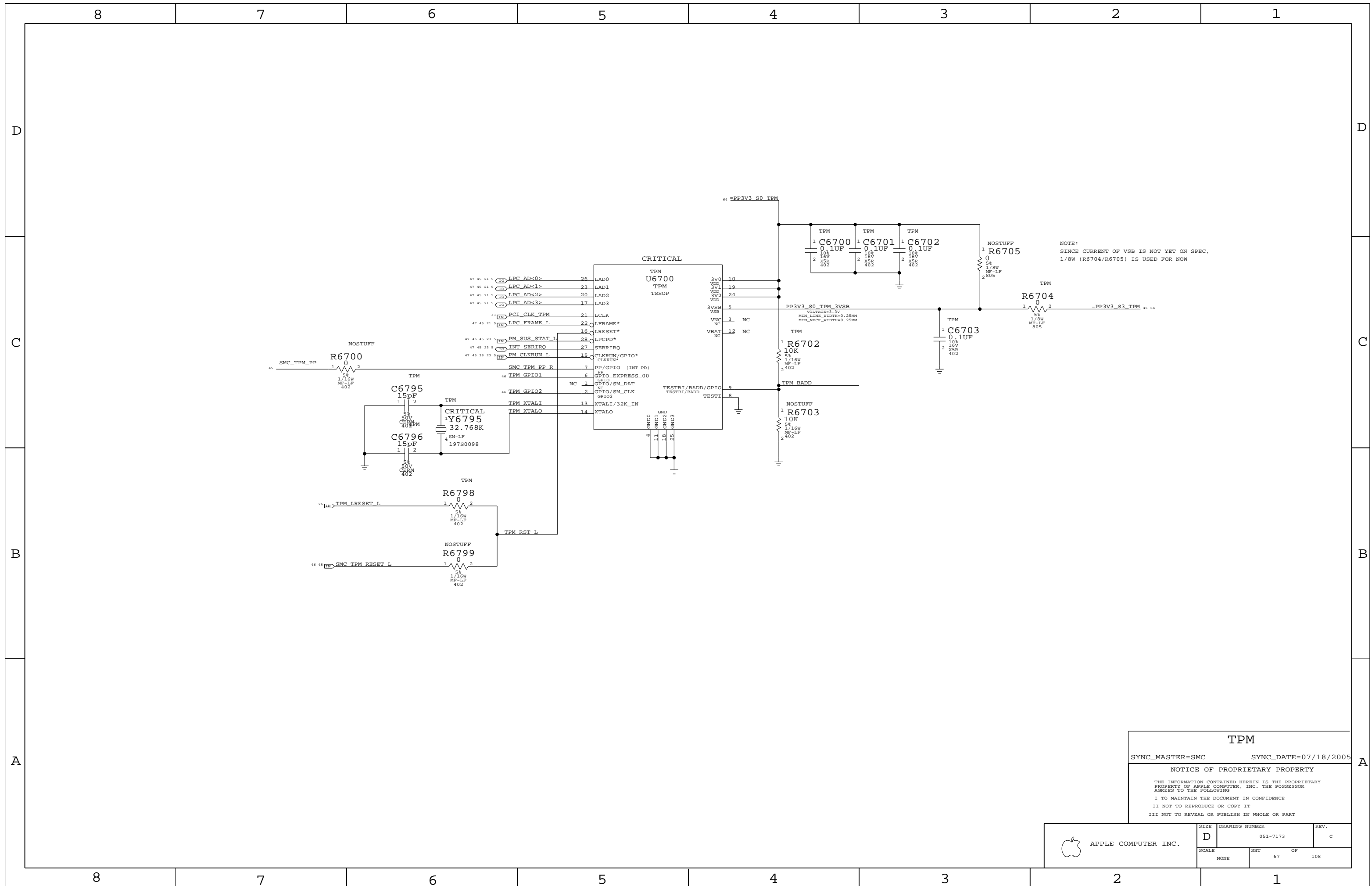
SYNC\_MASTER=SMC      SYNC\_DATE=08/23/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	SHT	OF	REV.
NONE	66	108	



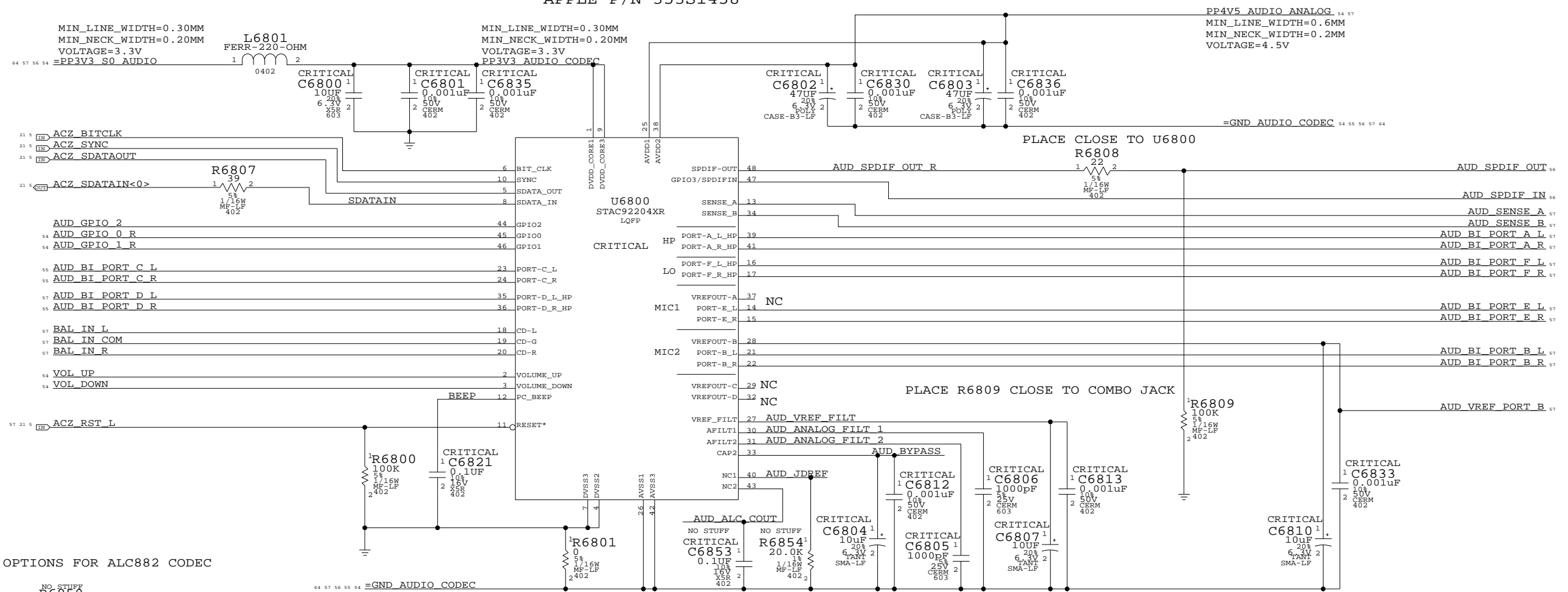
**TPM**  
 SYNC\_MASTER=SMC                      SYNC\_DATE=07/18/2005

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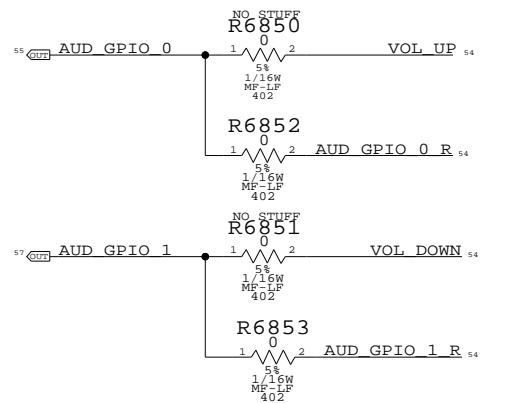
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. c
	SCALE NONE	SHEET 67	OF 108

# AUDIO CODEC

## APPLE P/N 353S1458

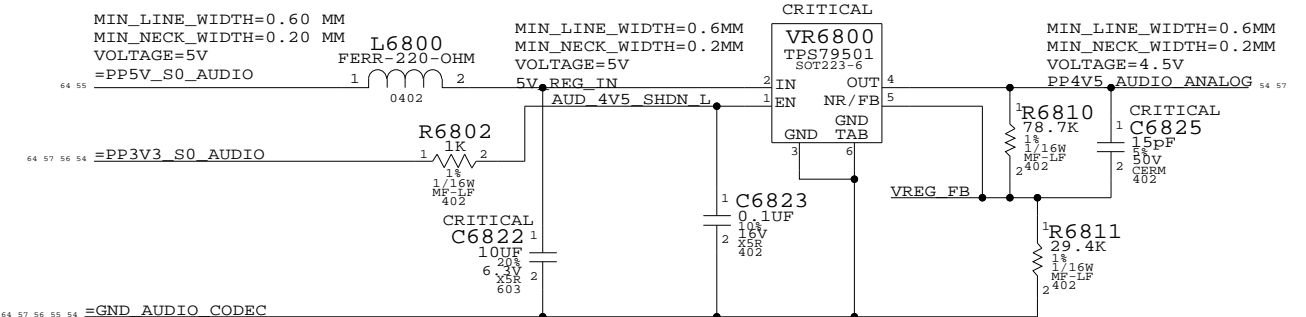


### STUFFING OPTIONS FOR ALC882 CODEC



### USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS



### 4.5V POWER SUPPLY FOR CODEC

### AUDIO: CODEC

SYNC\_MASTER=M42AUDIO    SYNC\_DATE=08/05/2006

NOTICE OF PROPRIETARY PROPERTY

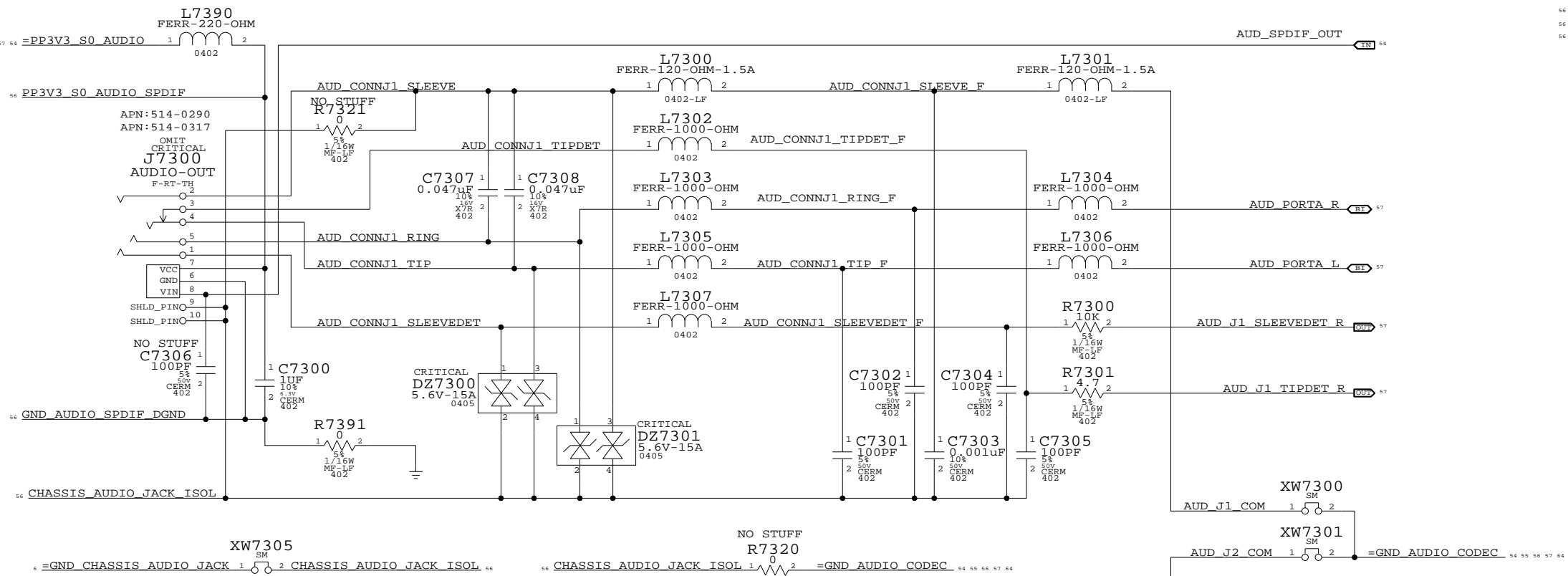
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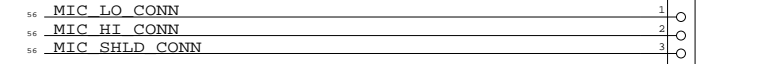
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 68	OF 108



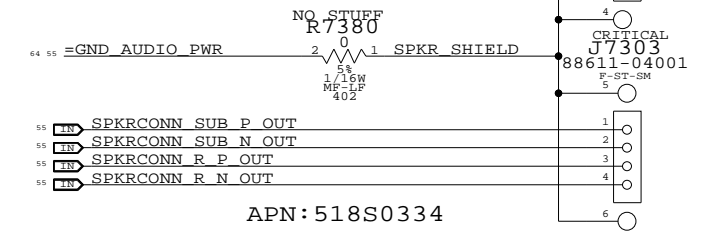
AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX



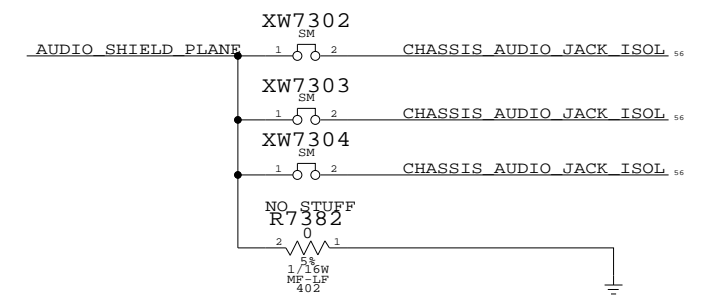
MIC CONNECTOR  
APN:514S0392



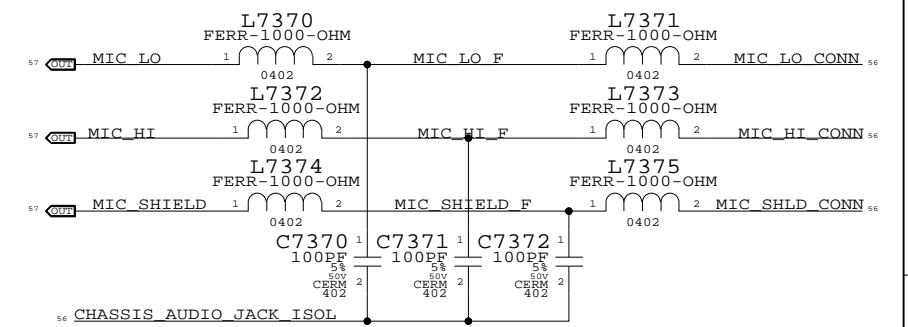
SPEAKER CONNECTOR  
APN:518S0332



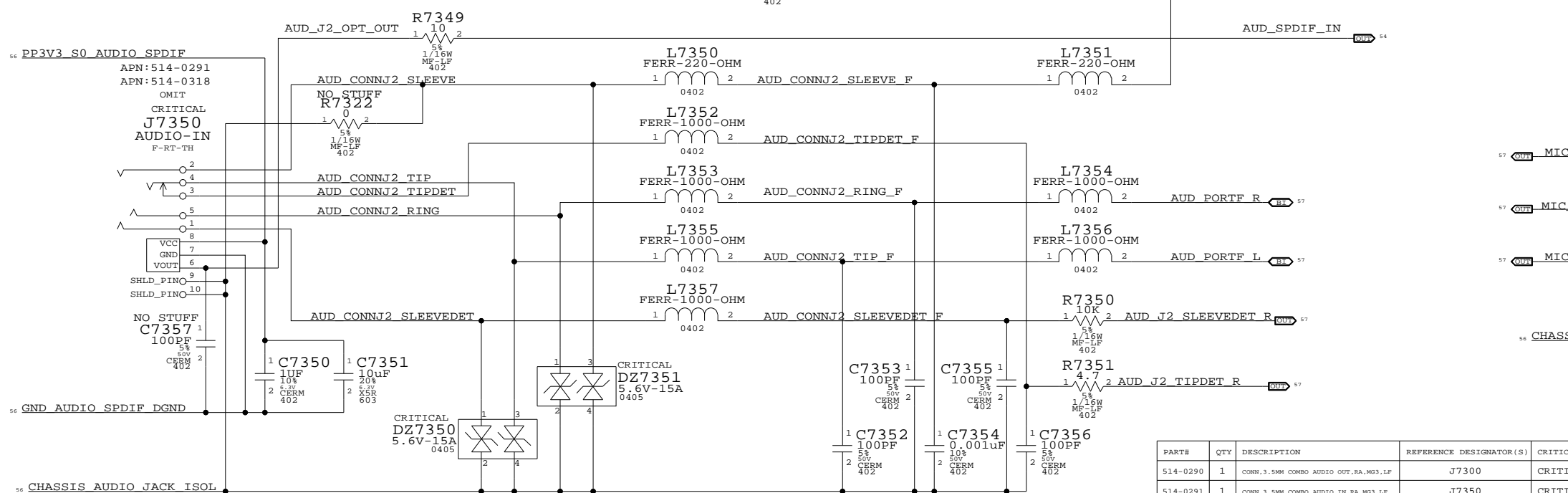
AUDIO SHIELD FILL



MIC EMI FILTER



AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

AUDIO: JACK

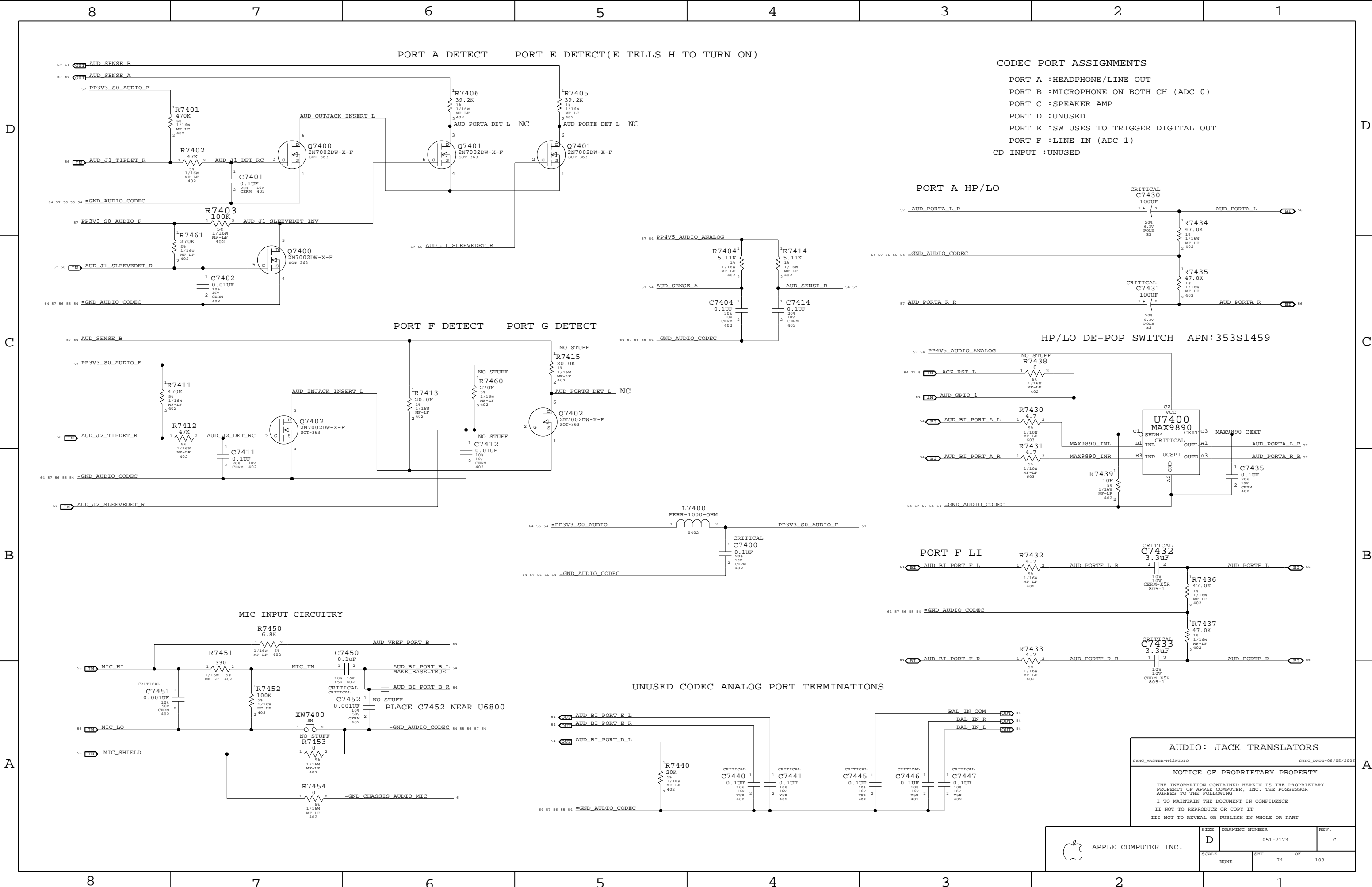
SYNC\_MASTER=M42AUDIO SYNC\_DATE=08/05/2006

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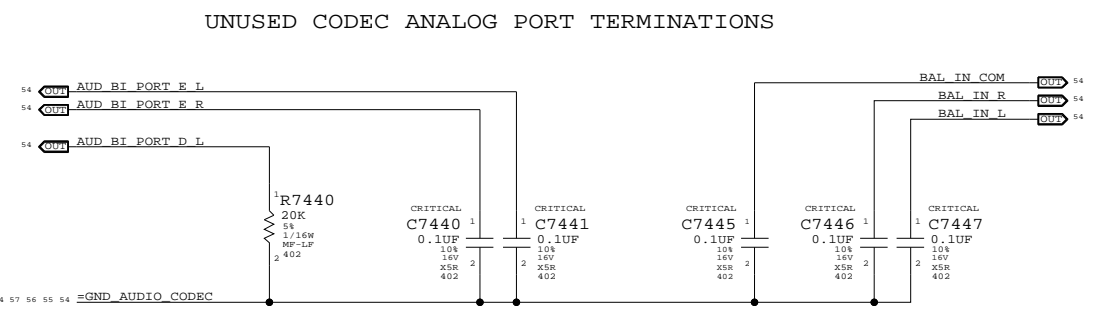
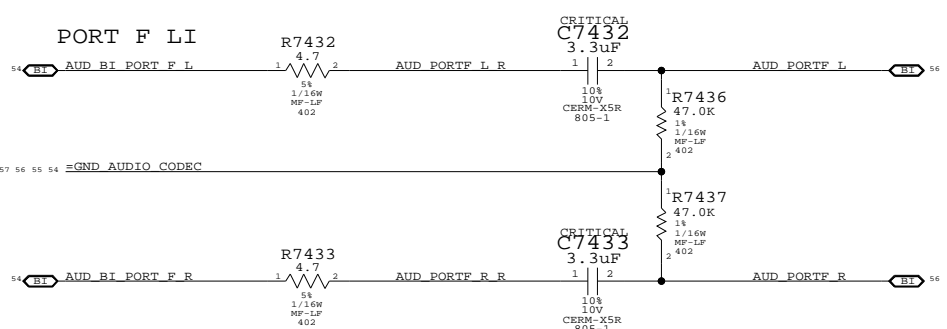
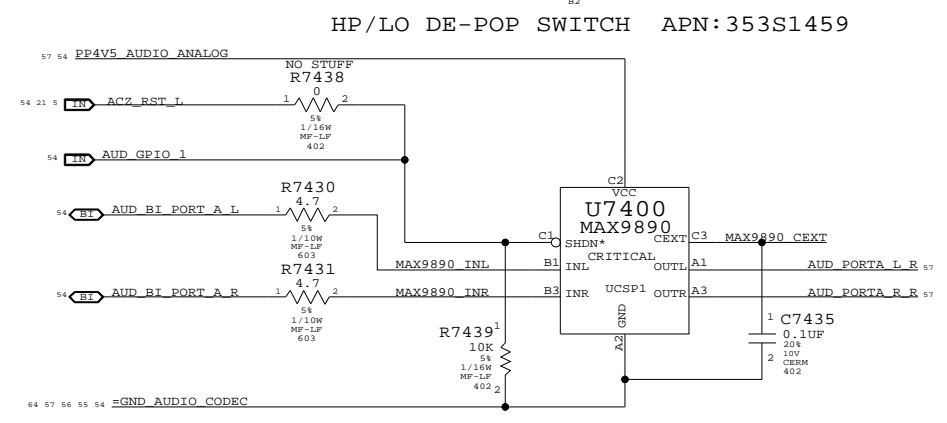
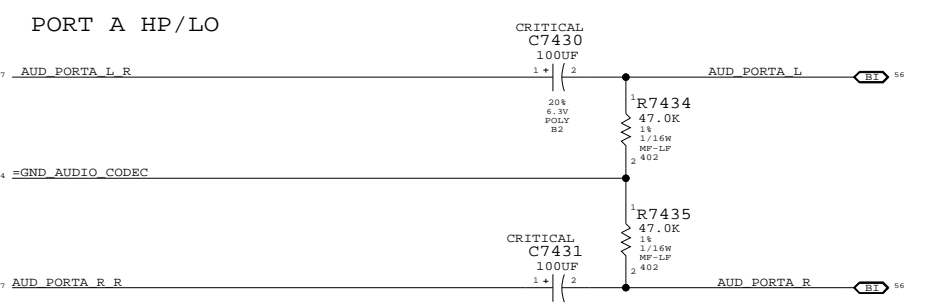
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	
NONE	73	108	





CODEC PORT ASSIGNMENTS

- PORT A : HEADPHONE/LINE OUT
- PORT B : MICROPHONE ON BOTH CH (ADC 0)
- PORT C : SPEAKER AMP
- PORT D : UNUSED
- PORT E : SW USES TO TRIGGER DIGITAL OUT
- PORT F : LINE IN (ADC 1)
- CD INPUT : UNUSED



**AUDIO: JACK TRANSLATORS**

SYNC\_MASTER=M42AUDIO SYNC\_DATE=08/05/2006

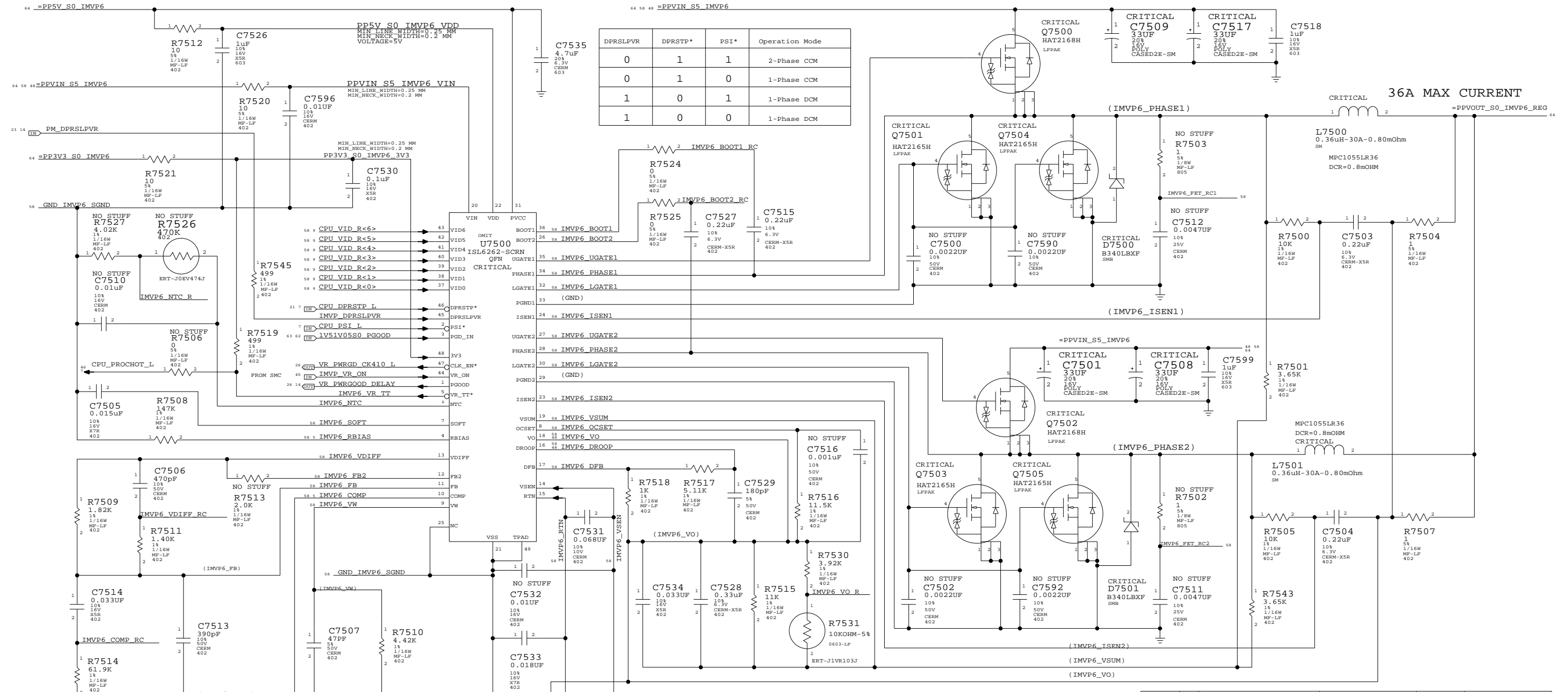
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	74	108	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7501_C7508	RENET T520V3300016AT0457650
128S0093	128S0092	?	C7509_C7517	RENET T520V3300016AT0457650



Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 \*\*on the CPU page\*\* protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

## IMVP6 CPU VCore Regulator

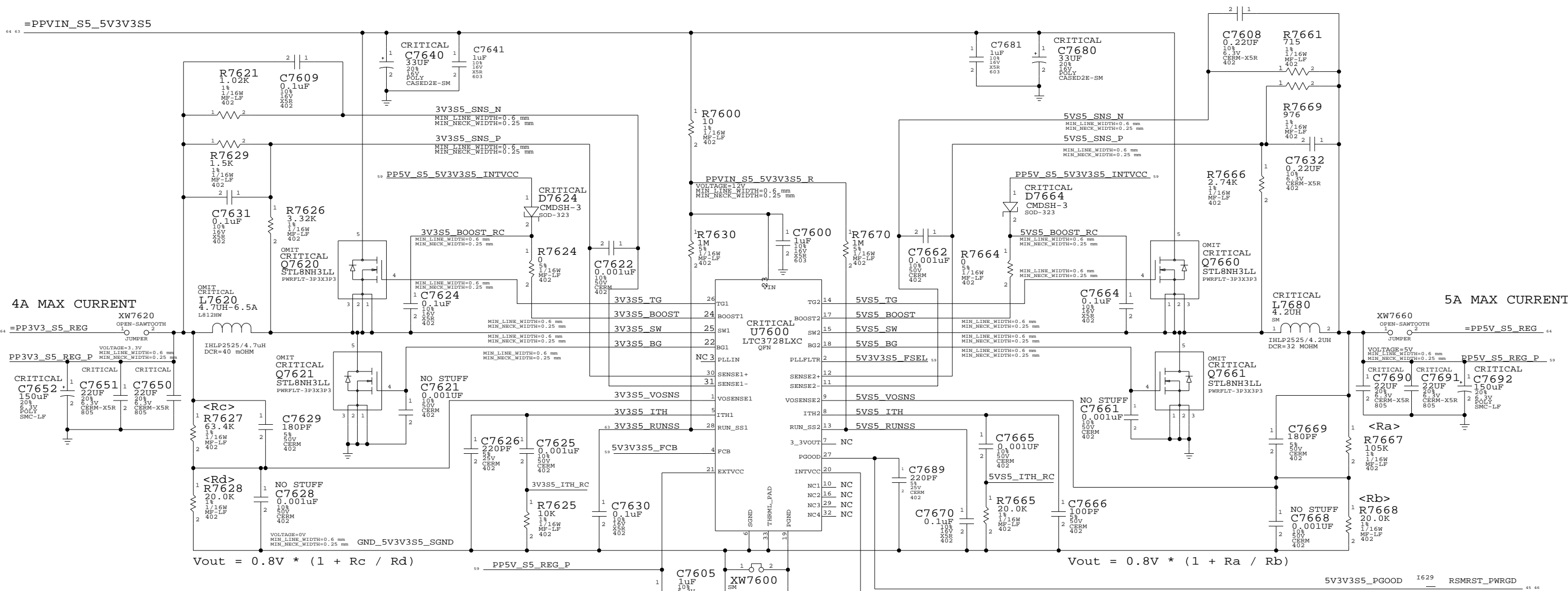
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	75		

# 5V / 3.3V POWER SUPPLY



4A MAX CURRENT

5A MAX CURRENT

$$V_{out} = 0.8V * (1 + R_c / R_d)$$

$$V_{out} = 0.8V * (1 + R_a / R_b)$$

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
15280133	1	4.7UH, +/-20%, 40mOHM, 3mm	L7620	3V3_IND_3MM
15280365	1	4.7UH, +/-20%, 40mOHM, 2.8mm	L7620	3V3_IND_2MM8
37680445	4	FAIRCHILD FDM6296	Q7620, Q7621, Q7660, Q7661	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12880093	12880092	?	C7680, C7640	RENET VS20V330M16ATE0487650
37680448	37680445	?	Q7620, Q7621	VISHAY SI7806ADN
37680448	37680445	?	Q7660, Q7661	VISHAY SI7806ADN

## 5V / 3.3V Power Supply

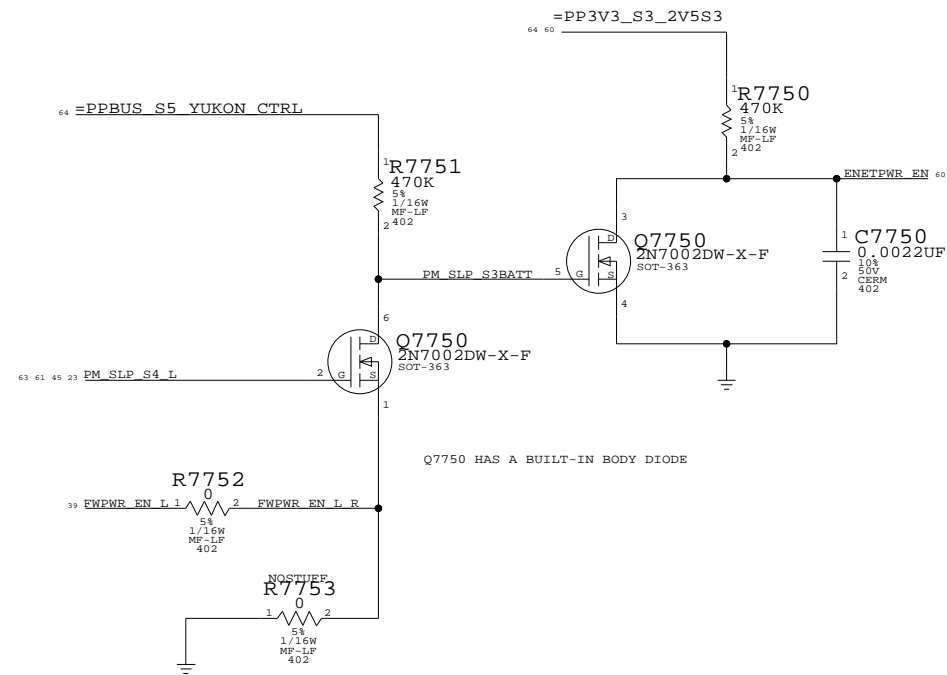
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	76		

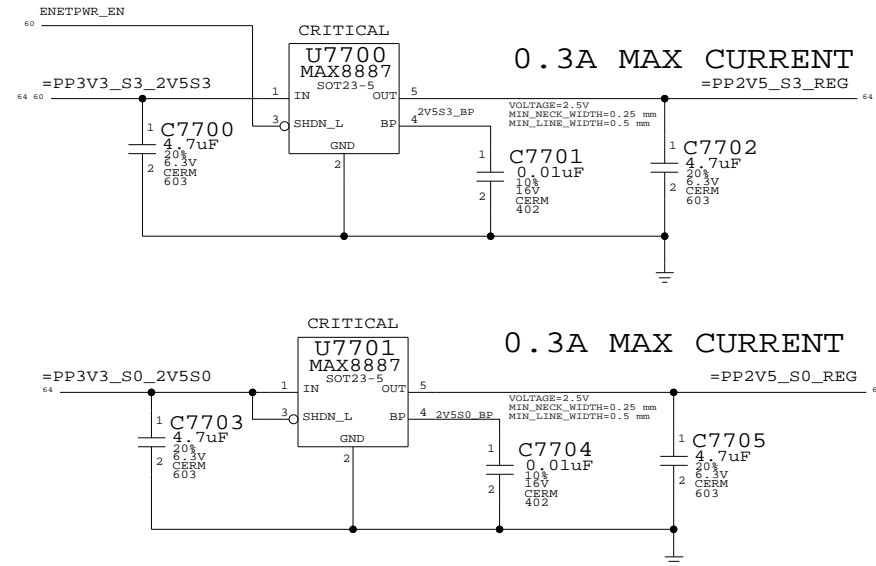
# YUKON POWER CONTROL



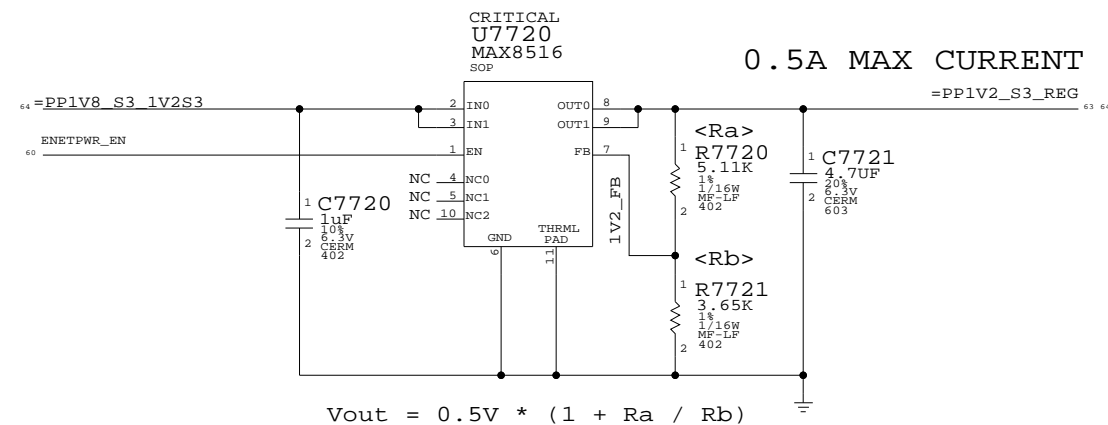
NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3   S0	~S0   ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR\_EN IS BUFFERED PM\_SLP\_S4\_L

# 2.5V REGULATORS



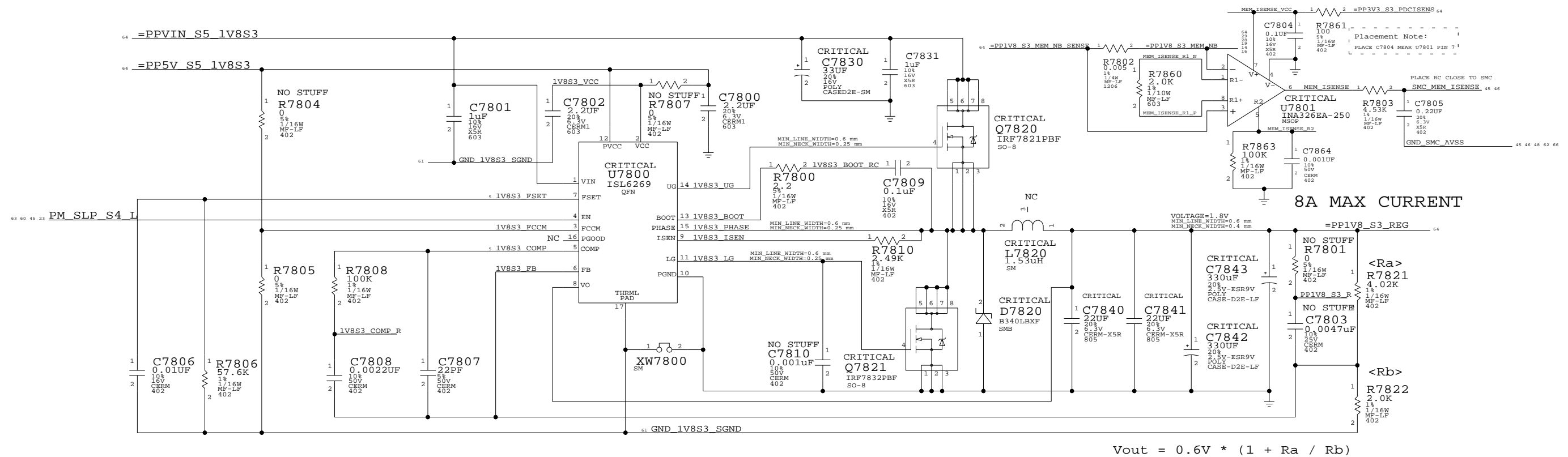
# 1.2V REGULATOR



**2.5V/1.2V Regulator**  
 SYNC\_MASTER=ENET SYNC\_DATE=12/06/2005  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	c
SCALE	SHT	OF	108
NONE	77		

# 1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	ERRY 7520V330M16AT00457450

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842, C7843	PANASONIC KEPSX0D331ER
128S0095	128S0060	?	C7842, C7843	PANASONIC KEPSX0D331EK

**1.8V Supply**

SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

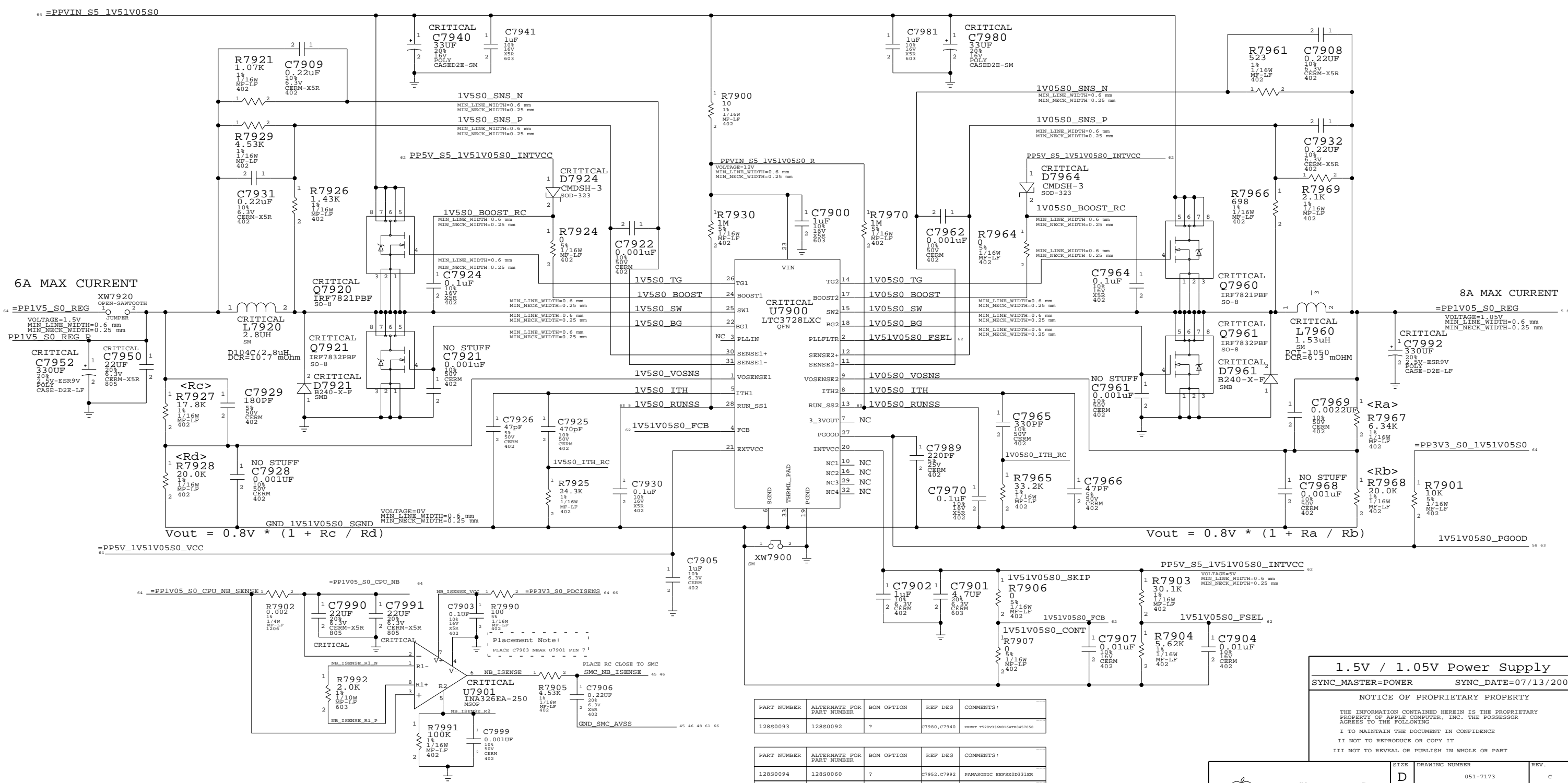
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	78		

# 1.5V/1.05V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980, C7940	EXHIBIT 7520V33H001A480457450
128S0094	128S0060	?	C7952, C7992	PANASONIC EEP5X003311E
128S0095	128S0060	?	C7952, C7992	PANASONIC EEP5X003311E

**1.5V / 1.05V Power Supply**  
 SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.

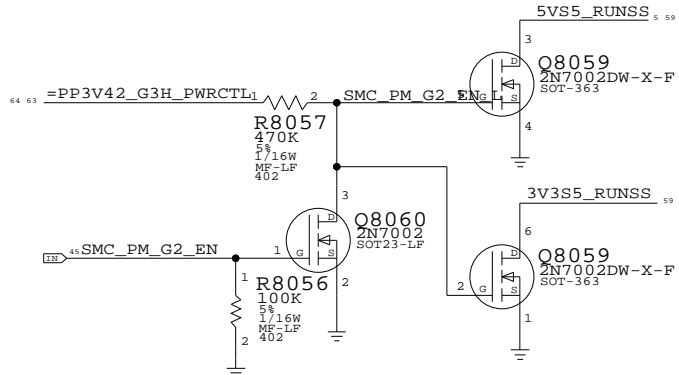
SIZE	DRAWING NUMBER	REV.
D	051-7173	C
SCALE	SHT	OF
NONE	79	108

### POWER CONTROL SIGNALS

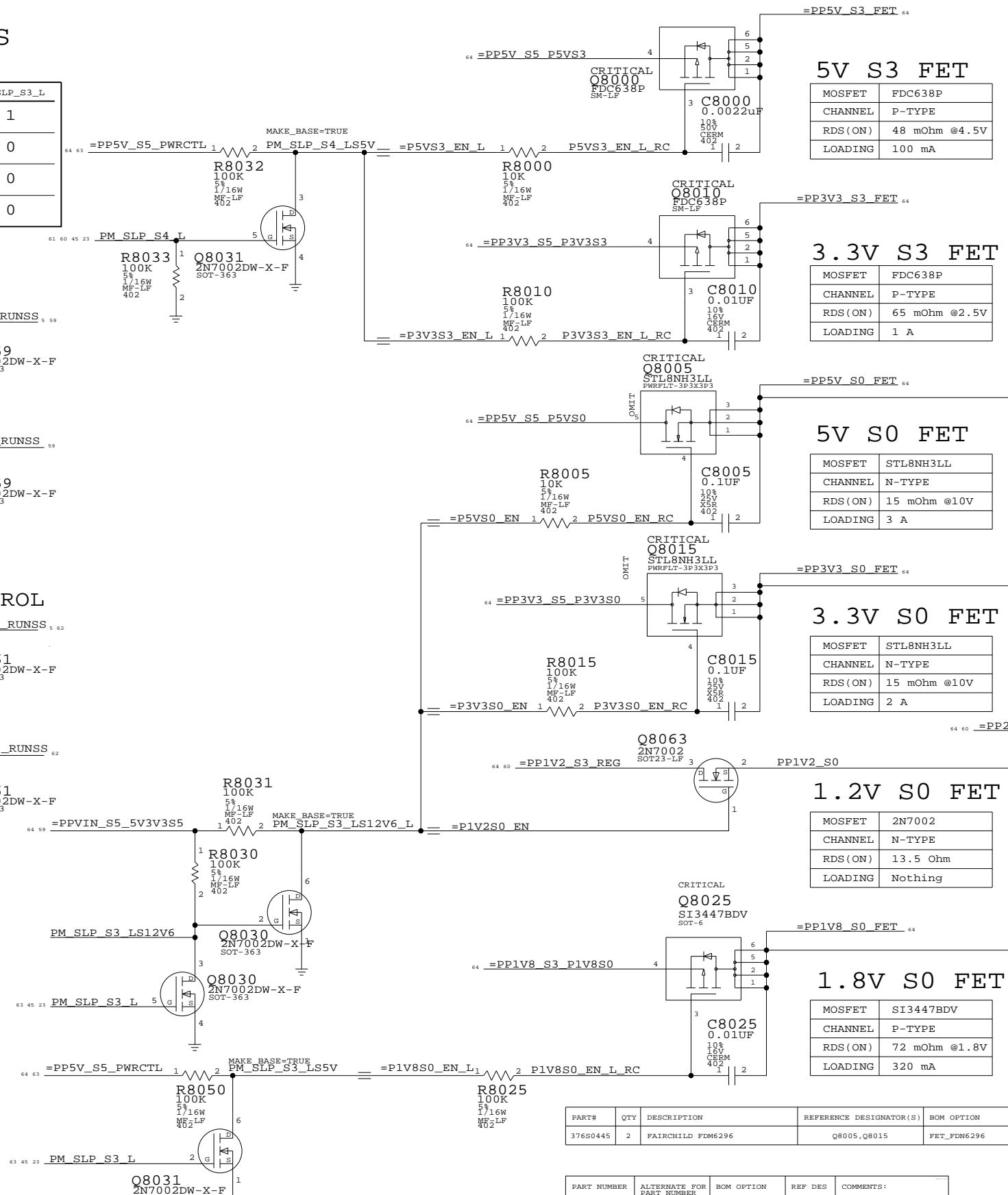
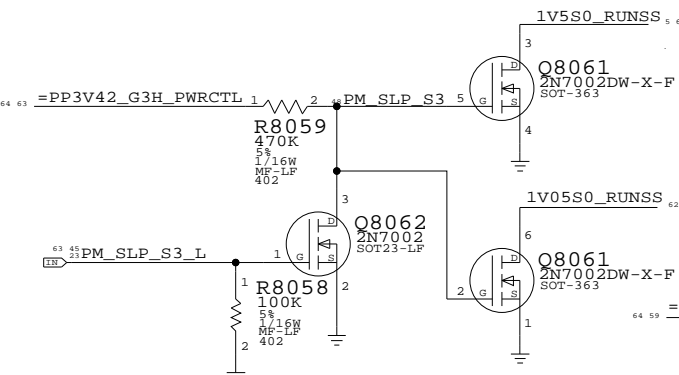
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

### 5V/3.3V S5 RUN/SS CONTROL



### 1.5V/1.05V S0 RUN/SS CONTROL

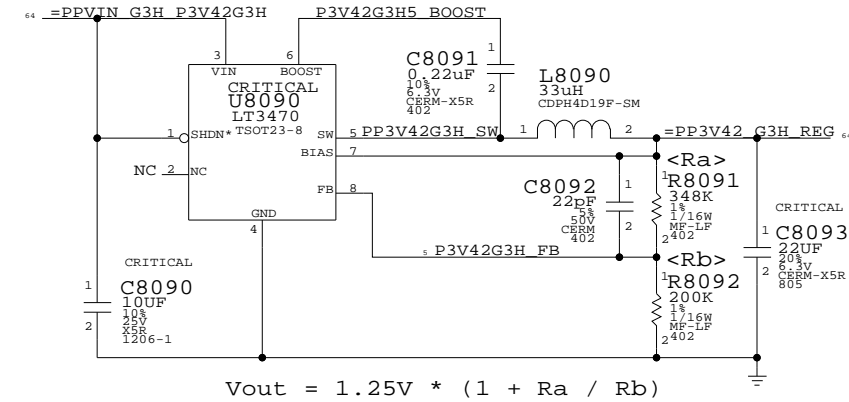


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005, Q8015	FET_FDM6296

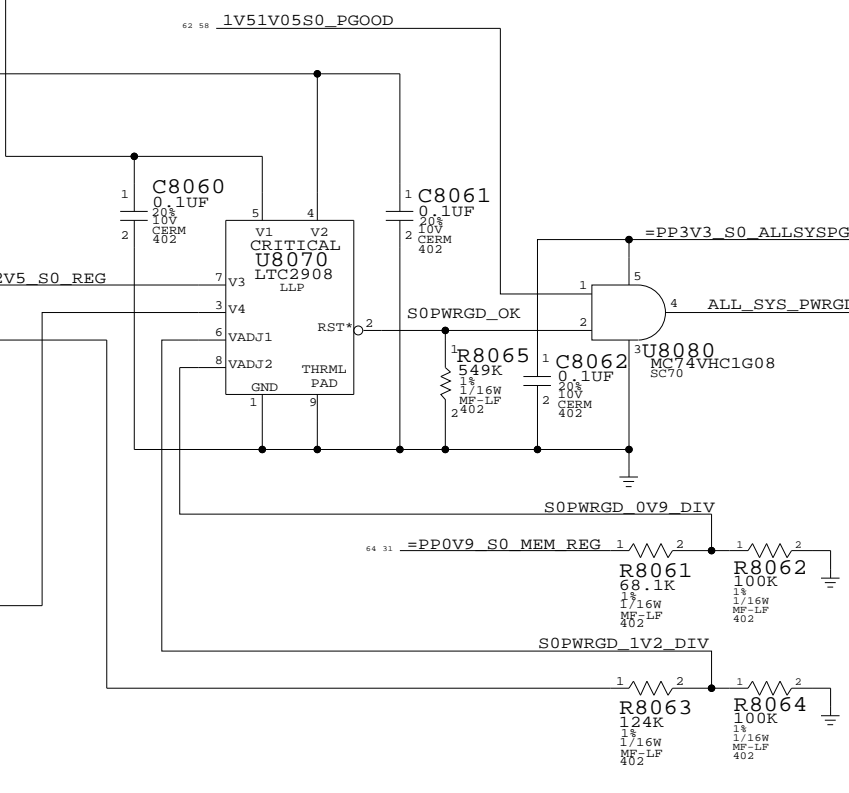
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	D8005, Q8015	VISHAY SI7806ADN

### 3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



### ALL SYSTEM PWRGD CIRCUIT



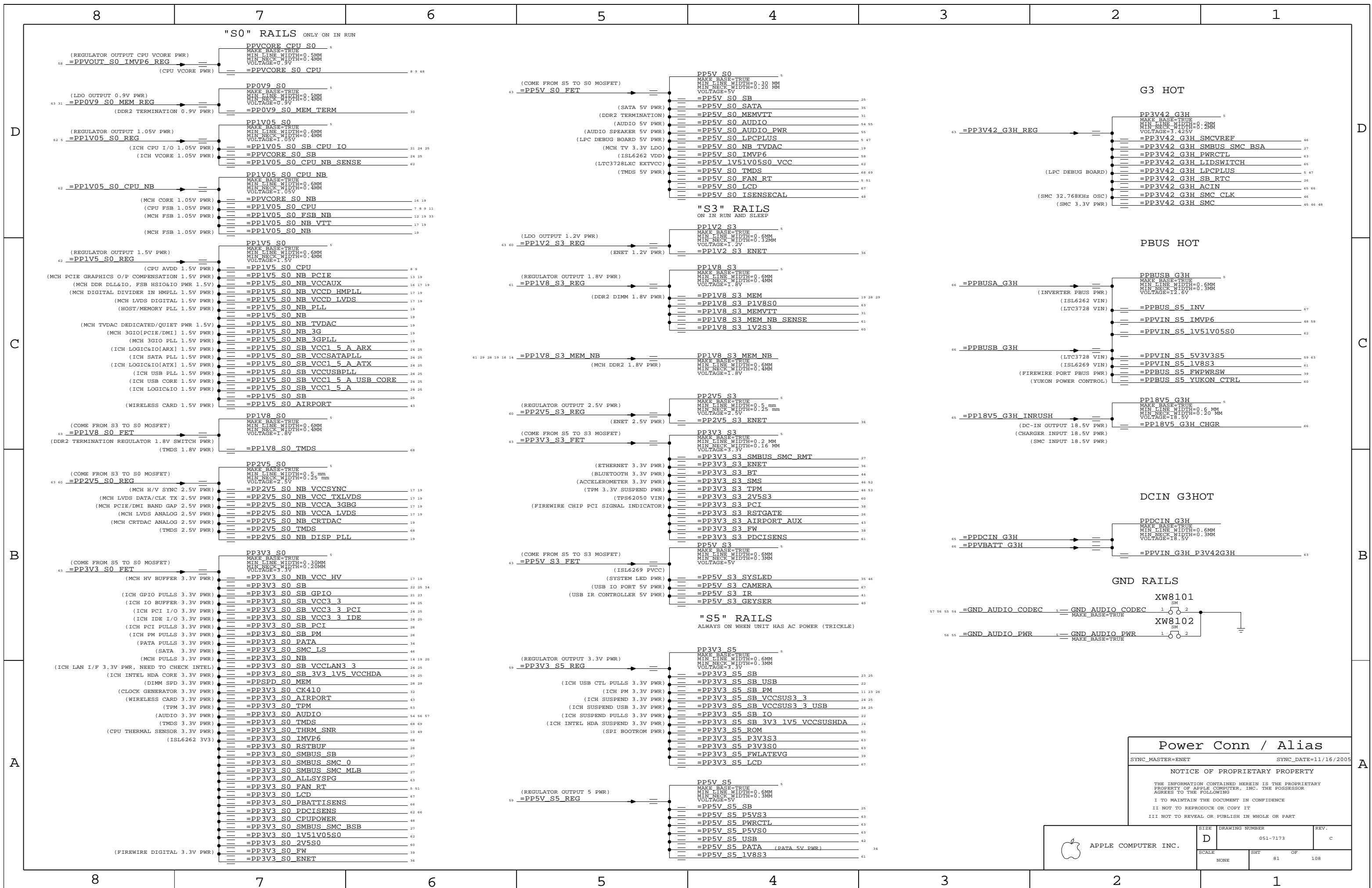
### S3/S0 FETS, G3H SUPPLY

SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	80		



**Power Conn / Alias**

SYNC\_MASTER=ENET SYNC\_DATE=11/16/2005

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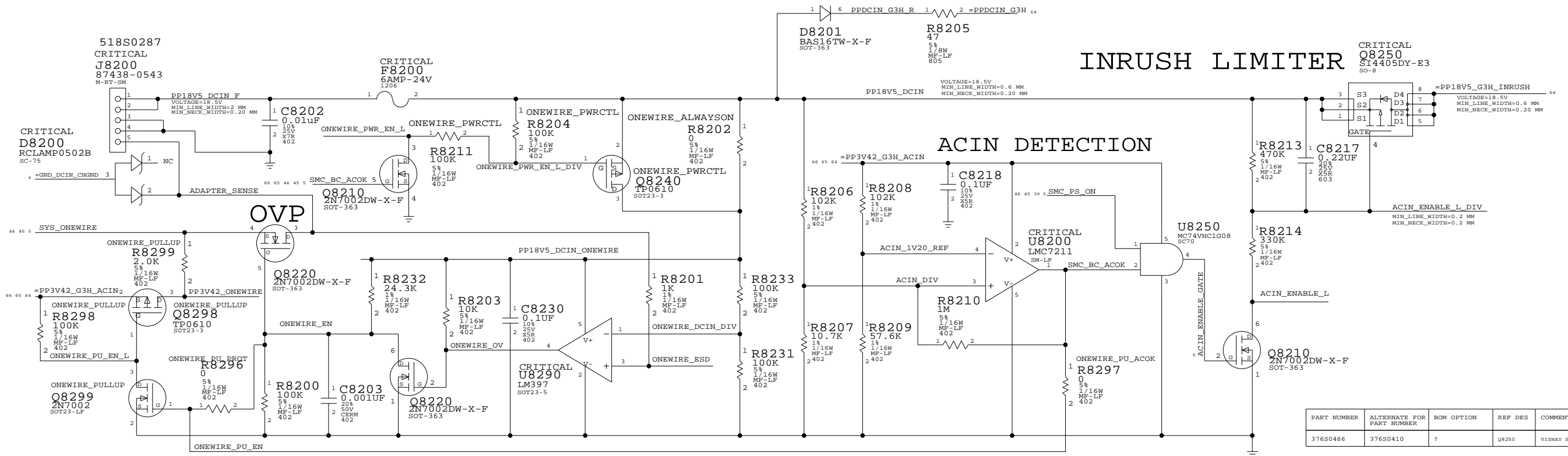
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 81	OF 108



# DC-JACK INTERFACE

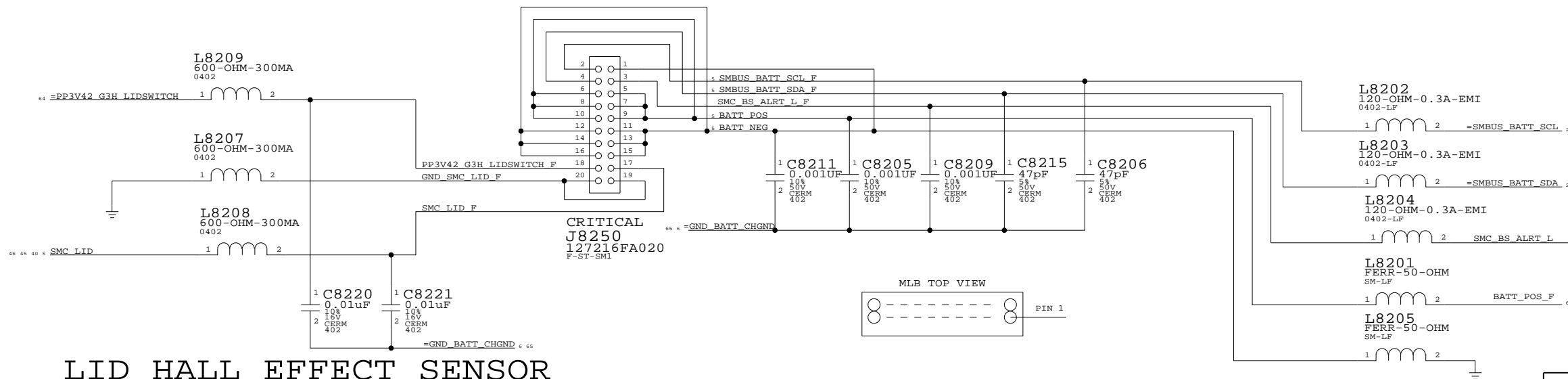
8 7 6 5 4 3 2 1



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

# BATTERY INTERFACE

B B



## LID HALL EFFECT SENSOR

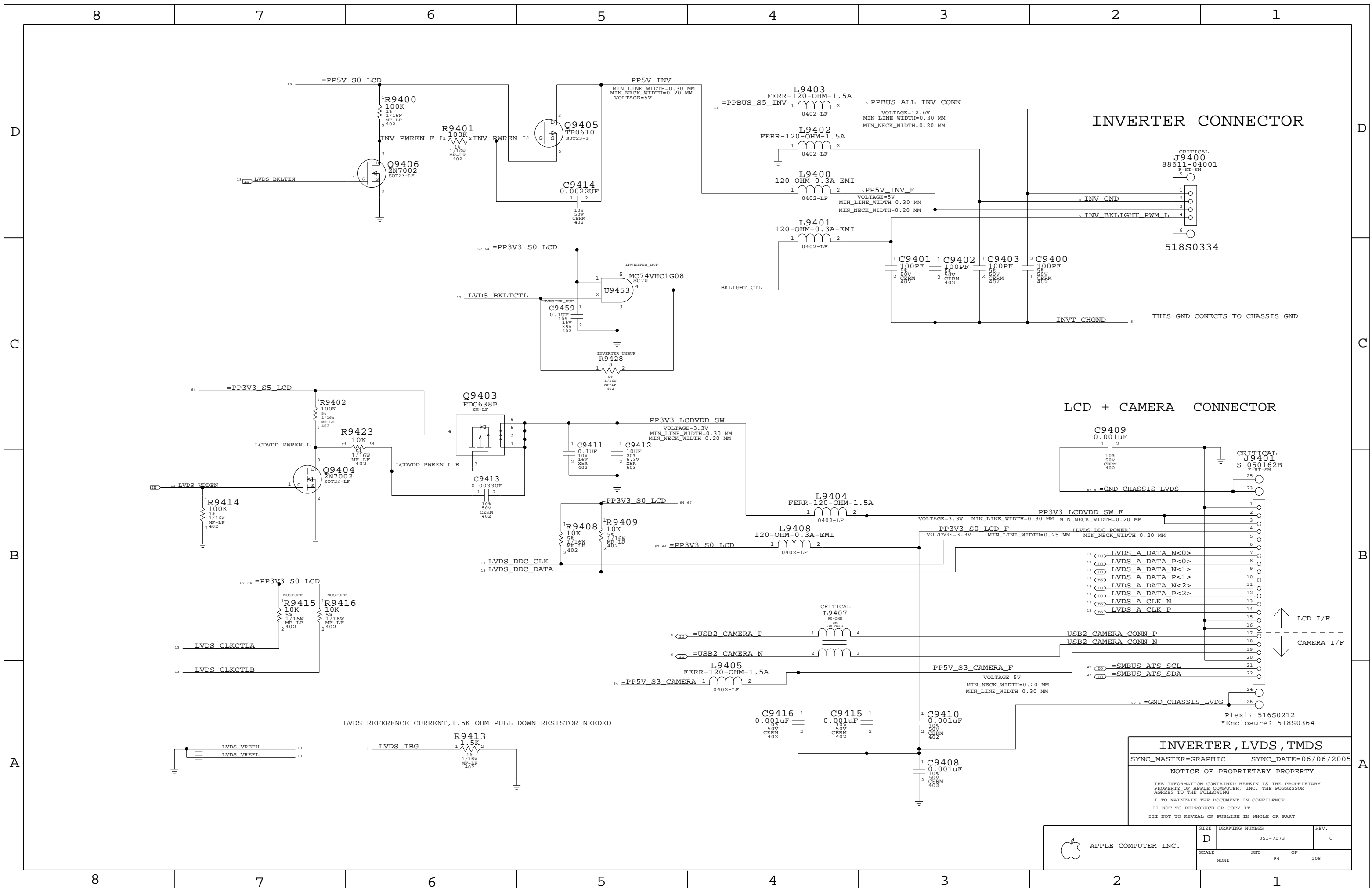
DC-In & Battery Connectors  
 SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	REV.
NONE	82	108	

8 7 6 5 4 3 2 1





INVERTER CONNECTOR

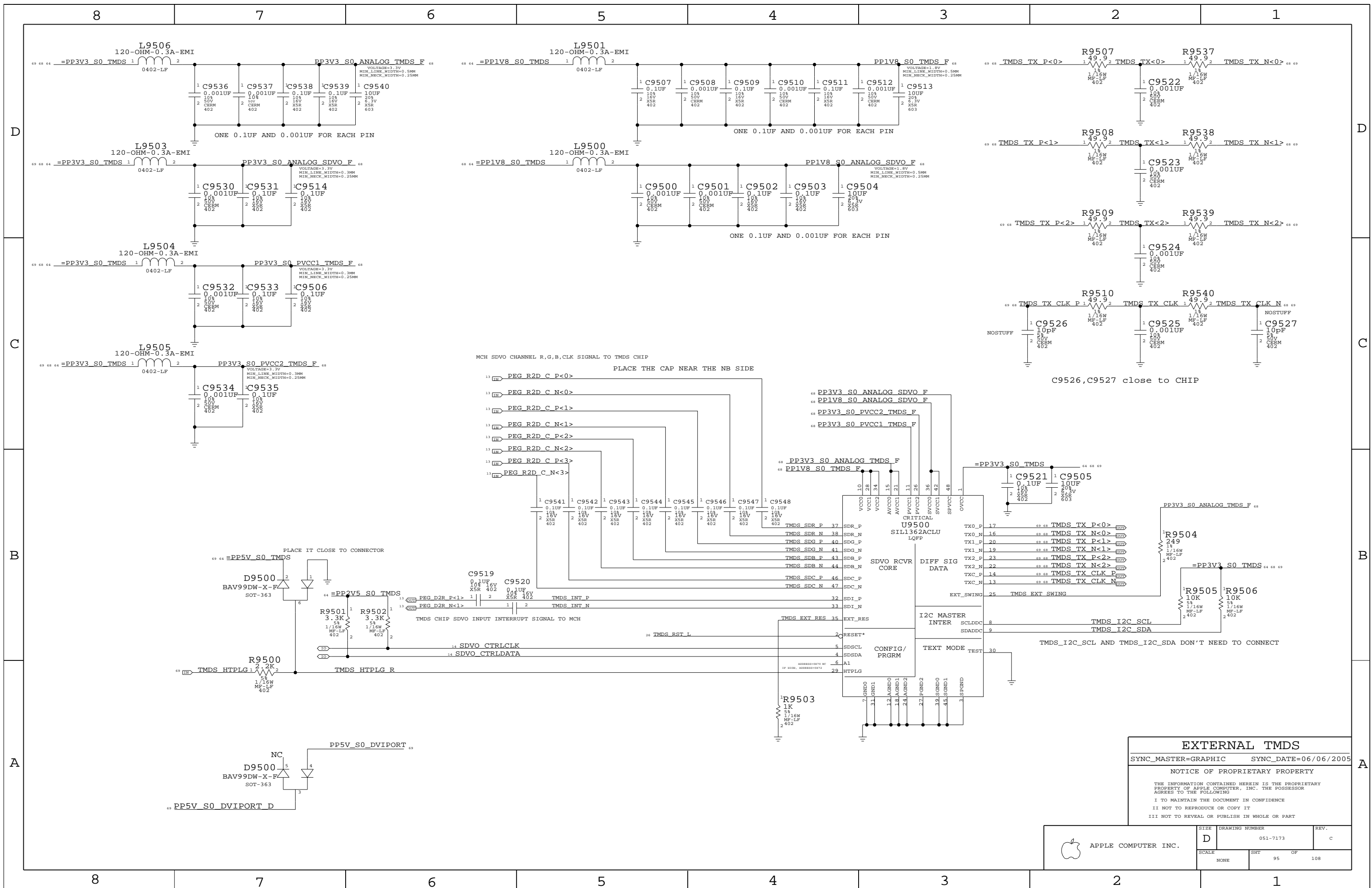
LCD + CAMERA CONNECTOR

INVERTER, LVDS, TMDs

SYNC\_MASTER=GRAPHIC SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	C
SCALE	SHT	OF	108
NONE	94		



**EXTERNAL TMDs**

SYNC\_MASTER=GRAPHIC    SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. C
	SCALE NONE	SHEET 95	OF 108

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
15580227	15580164	?	REF: 15580164	KEEP MAG LAYER IN BOX

## Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

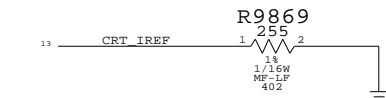
TMDS(MINI DVI) INTERFACE

Isolation required for DVI power switch

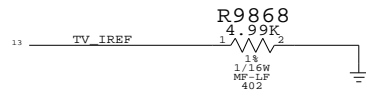
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

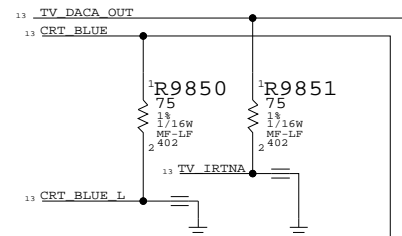
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT\_IREF AND GROUND



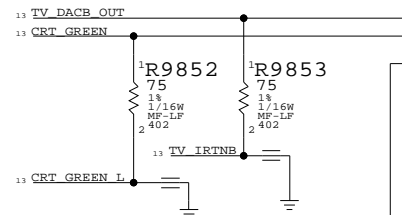
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



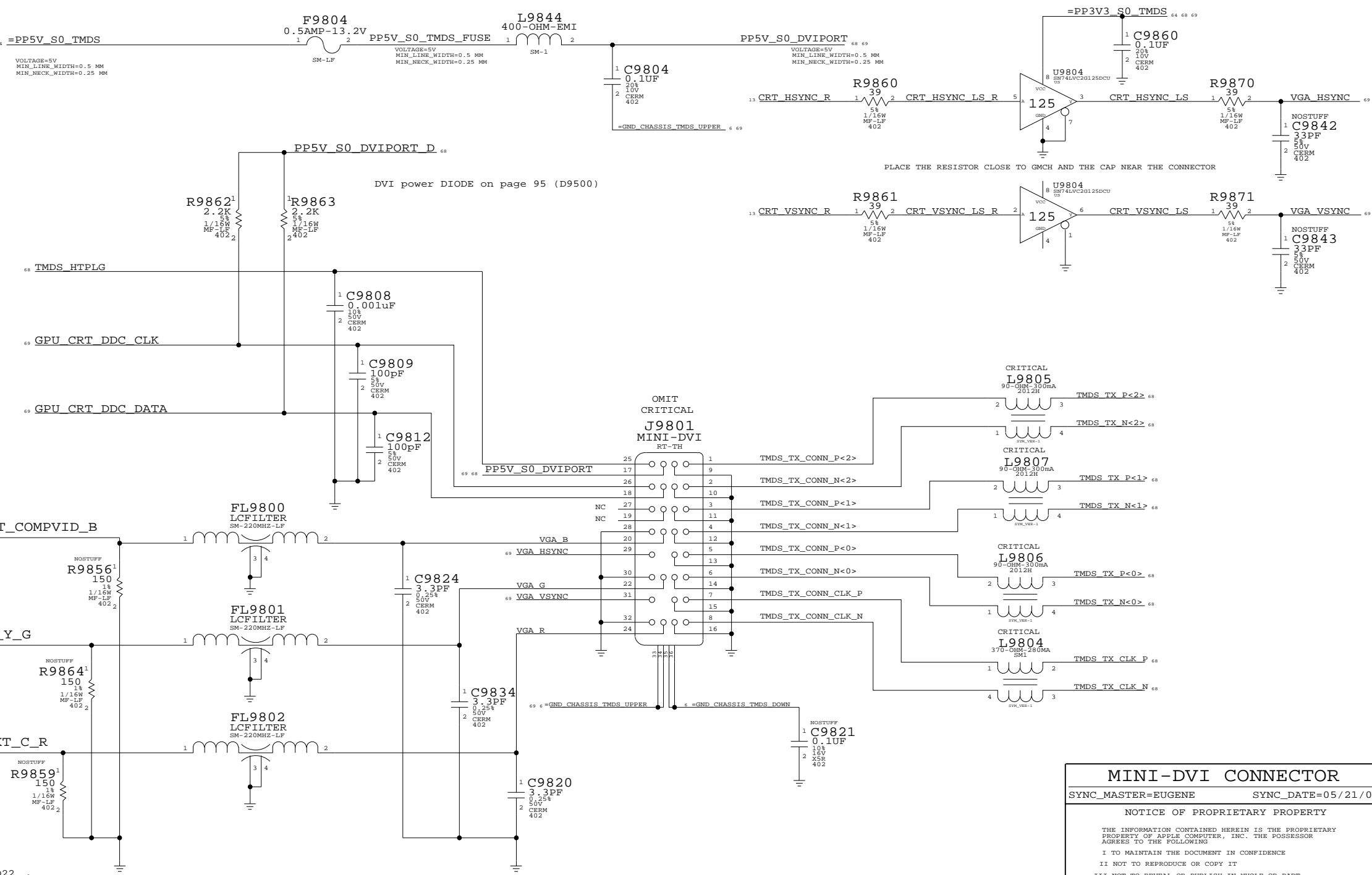
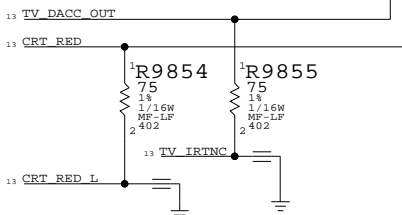
PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI BCDF, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI BCDF, RA, BLACK, LF	J9801	CRITICAL	FANCY

### MINI-DVI CONNECTOR

SYNC\_MASTER=EUGENE SYNC\_DATE=05/21/05

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	8	7	6	5	4	3	2	1	
	FWPWR_EN	FWPWR_EN - @m42a_1ib.M42A	39C5	IMVP6_PHASE2	IMVP6_PHASE2 - @m42a_1ib.M42A	58A6 58C6	MEM_DQ<17>	MEM_DQ<17> - @m42a_1ib.M42A	15C4 29C6
	FWPWR_EN_L	FWPWR_EN_L - @m42a_1ib.M42A	39C4 60C8	IMVP6_RBIAS	IMVP6_RBIAS - @m42a_1ib.M42A	5D7 58A4 58B7	MEM_DQ<18>	MEM_DQ<18> - @m42a_1ib.M42A	15C4 29C6
	FWPWR_EN_L_DIV	FWPWR_EN_L_DIV - @m42a_1ib.M42A	39C5	IMVP6_RTN	IMVP6_RTN - @m42a_1ib.M42A	58A4 58B6	MEM_DQ<19>	MEM_DQ<19> - @m42a_1ib.M42A	15C4 29C4
	FWPWR_EN_L_R	FWPWR_EN_L_R - @m42a_1ib.M42A	60C7	IMVP6_SOFT	IMVP6_SOFT - @m42a_1ib.M42A	58A4 58C7	MEM_DQ<20>	MEM_DQ<20> - @m42a_1ib.M42A	15C4 29C6
	FWPWR_RUN	FWPWR_RUN - @m42a_1ib.M42A	39C6	IMVP6_UGATE1	IMVP6_UGATE1 - @m42a_1ib.M42A	58A8 58C6	MEM_DQ<21>	MEM_DQ<21> - @m42a_1ib.M42A	15C4 29C4
	FW_A_TPA_N	FW_A_TPA_N - @m42a_1ib.M42A	38B3 39B6	IMVP6_UGATE2	IMVP6_UGATE2 - @m42a_1ib.M42A	58A6 58C6	MEM_DQ<22>	MEM_DQ<22> - @m42a_1ib.M42A	15C4 29C6
	FW_PORT0_TPA_N	FW_PORT0_TPA_N - @m42a_1ib.M42A	39B5	IMVP6_VDIFF	IMVP6_VDIFF - @m42a_1ib.M42A	58A4 58B7	MEM_DQ<23>	MEM_DQ<23> - @m42a_1ib.M42A	15C4 29C6
	FW_A_TPA_P	FW_A_TPA_P - @m42a_1ib.M42A	38B3 39B6	IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m42a_1ib.M42A	58B7	MEM_DQ<24>	MEM_DQ<24> - @m42a_1ib.M42A	15C4 29C4
	FW_PORT0_TPA_P	FW_PORT0_TPA_P - @m42a_1ib.M42A	39B5	IMVP6_VO	IMVP6_VO - @m42a_1ib.M42A	58A5 58A4 58B6	MEM_DQ<25>	MEM_DQ<25> - @m42a_1ib.M42A	15C4 29C4
	FW_A_TPB_IAS	FW_A_TPB_IAS - @m42a_1ib.M42A	38B3 39B6	IMVP6_VO_R	IMVP6_VO_R - @m42a_1ib.M42A	58B4	MEM_DQ<26>	MEM_DQ<26> - @m42a_1ib.M42A	15C4 29C4
	FW_A_TPB_N	FW_A_TPB_N - @m42a_1ib.M42A	38B3 39B6	IMVP6_VO_R1	IMVP6_VO_R1 - @m42a_1ib.M42A	58A8	MEM_DQ<27>	MEM_DQ<27> - @m42a_1ib.M42A	15C4 29C6
	FW_PORT0_TPB_N	FW_PORT0_TPB_N - @m42a_1ib.M42A	39B5	IMVP6_VO_R2	IMVP6_VO_R2 - @m42a_1ib.M42A	58A6	MEM_DQ<28>	MEM_DQ<28> - @m42a_1ib.M42A	15C4 29C4
	FW_A_TPB_P	FW_A_TPB_P - @m42a_1ib.M42A	38B3 39B6	IMVP6_VR_TT	IMVP6_VR_TT - @m42a_1ib.M42A	58C7	MEM_DQ<29>	MEM_DQ<29> - @m42a_1ib.M42A	15C4 29C6
	FW_PORT0_TPB_P	FW_PORT0_TPB_P - @m42a_1ib.M42A	39B5	IMVP6_VSEN	IMVP6_VSEN - @m42a_1ib.M42A	58A4 58B5	MEM_DQ<30>	MEM_DQ<30> - @m42a_1ib.M42A	15C4 29C6
	FW_B_TPA_N	FW_B_TPA_N - @m42a_1ib.M42A	6D2 38B3	IMVP6_VSUM	IMVP6_VSUM - @m42a_1ib.M42A	58A4 58C6	MEM_DQ<31>	MEM_DQ<31> - @m42a_1ib.M42A	15C4 29C6
	FW_B_TPA_N_SPN	FW_B_TPA_N_SPN - @m42a_1ib.M42A	5B7 6D1	IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m42a_1ib.M42A	58A8	MEM_DQ<32>	MEM_DQ<32> - @m42a_1ib.M42A	15C4 29A6
	FW_B_TPA_P	FW_B_TPA_P - @m42a_1ib.M42A	6D2 38B3	IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m42a_1ib.M42A	58A6	MEM_DQ<33>	MEM_DQ<33> - @m42a_1ib.M42A	15C4 29A4
	FW_B_TPB_IAS	FW_B_TPB_IAS - @m42a_1ib.M42A	5B7 6D1	IMVP_VP	IMVP_VP - @m42a_1ib.M42A	58A4 58B7	MEM_DQ<34>	MEM_DQ<34> - @m42a_1ib.M42A	15B4 29A4
	FW_B_TPB_N	FW_B_TPB_N - @m42a_1ib.M42A	5B7 6D1	IMVP_DFRSLPVR	IMVP_DFRSLPVR - @m42a_1ib.M42A	58C7	MEM_DQ<35>	MEM_DQ<35> - @m42a_1ib.M42A	15B4 29A4
	FW_B_TPB_P	FW_B_TPB_P - @m42a_1ib.M42A	5B7 6D1	IMVP_VR_ON	IMVP_VR_ON - @m42a_1ib.M42A	45D8 58C7	MEM_DQ<36>	MEM_DQ<36> - @m42a_1ib.M42A	15B4 29A4
	FW_C_TPA_N	FW_C_TPA_N - @m42a_1ib.M42A	6D2 38B3	INT_PIROA_L	INT_PIROA_L - @m42a_1ib.M42A	22A7 26C3	MEM_DQ<37>	MEM_DQ<37> - @m42a_1ib.M42A	15B4 29A6
	FW_C_TPA_P	FW_C_TPA_P - @m42a_1ib.M42A	6D2 38B3	INT_PIROB_L	INT_PIROB_L - @m42a_1ib.M42A	22A7 26C3	MEM_DQ<38>	MEM_DQ<38> - @m42a_1ib.M42A	15B4 29A4
	FW_D_TPB_IAS	FW_D_TPB_IAS - @m42a_1ib.M42A	5B7 6D1	INT_PIROC_L	INT_PIROC_L - @m42a_1ib.M42A	22A7 26C3	MEM_DQ<39>	MEM_DQ<39> - @m42a_1ib.M42A	15B4 29A4
	FW_D_TPB_N	FW_D_TPB_N - @m42a_1ib.M42A	5B7 6D1	INT_PIROQ_L	INT_PIROQ_L - @m42a_1ib.M42A	22A7 26C3 38A5	MEM_DQ<40>	MEM_DQ<40> - @m42a_1ib.M42A	15B4 29A6
	FW_D_TPB_P	FW_D_TPB_P - @m42a_1ib.M42A	5B7 6D1	INT_SERIRQ	INT_SERIRQ - @m42a_1ib.M42A	5C2 23C8 45C8 47C5 53C6	MEM_DQ<41>	MEM_DQ<41> - @m42a_1ib.M42A	15B4 29A6
	FW_E_TPB_IAS	FW_E_TPB_IAS - @m42a_1ib.M42A	5B7 6D1	INTV_CHGND	INTV_CHGND - @m42a_1ib.M42A	6D8 67C2	MEM_DQ<42>	MEM_DQ<42> - @m42a_1ib.M42A	15B4 29A4
	FW_E_TPB_N	FW_E_TPB_N - @m42a_1ib.M42A	5B7 6D1	INTV_BKLIGHT_PWM_L	INTV_BKLIGHT_PWM_L - @m42a_1ib.M42A	5B1 67D2	MEM_DQ<43>	MEM_DQ<43> - @m42a_1ib.M42A	15B4 29A6
	FW_E_TPB_P	FW_E_TPB_P - @m42a_1ib.M42A	5B7 6D1	INTV_GND	INTV_GND - @m42a_1ib.M42A	5B1 67D2	MEM_DQ<44>	MEM_DQ<44> - @m42a_1ib.M42A	15B4 29A6
	FW_F_TPB_IAS	FW_F_TPB_IAS - @m42a_1ib.M42A	6D2 38B3	INV_PWREN_F_L	INV_PWREN_F_L - @m42a_1ib.M42A	67D6	MEM_DQ<45>	MEM_DQ<45> - @m42a_1ib.M42A	15B4 29A6
	FW_F_TPB_N	FW_F_TPB_N - @m42a_1ib.M42A	5B7 6D1	INV_PWREN_L	INV_PWREN_L - @m42a_1ib.M42A	67D6	MEM_DQ<46>	MEM_DQ<46> - @m42a_1ib.M42A	15B4 29A4
	FW_F_TPB_P	FW_F_TPB_P - @m42a_1ib.M42A	5B7 6D1	IR_RX_OUT	IR_RX_OUT - @m42a_1ib.M42A	35C6 41C6	MEM_DQ<47>	MEM_DQ<47> - @m42a_1ib.M42A	15B4 29A4
	FW_G_TPB_IAS	FW_G_TPB_IAS - @m42a_1ib.M42A	6D2 38B3	IR_RX_OUT_F	IR_RX_OUT_F - @m42a_1ib.M42A	41C5	MEM_DQ<48>	MEM_DQ<48> - @m42a_1ib.M42A	15B4 29A4
	FW_G_TPB_N	FW_G_TPB_N - @m42a_1ib.M42A	6D2 38B3	ISENSE_CAL_EN	ISENSE_CAL_EN - @m42a_1ib.M42A	45B8 48A8	MEM_DQ<49>	MEM_DQ<49> - @m42a_1ib.M42A	15B4 29A6
	FW_G_TPB_P	FW_G_TPB_P - @m42a_1ib.M42A	5B7 6D1	ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m42a_1ib.M42A	48A7	MEM_DQ<50>	MEM_DQ<50> - @m42a_1ib.M42A	15B4 29B6
	FW_HCI_IDSEL	FW_HCI_IDSEL - @m42a_1ib.M42A	38A5	ISENSE_CAL_EN_LS5V	ISENSE_CAL_EN_LS5V - @m42a_1ib.M42A	48A6	MEM_DQ<51>	MEM_DQ<51> - @m42a_1ib.M42A	15B4 29A4
	FW_PCI_RST_L	FW_PCI_RST_L - @m42a_1ib.M42A	38A5	ITPFRSET_L	ITPFRSET_L - @m42a_1ib.M42A	11B3	MEM_DQ<52>	MEM_DQ<52> - @m42a_1ib.M42A	15B4 29A6
	FW_PORT0_TPA_N_FL	FW_PORT0_TPA_N_FL - @m42a_1ib.M42A	39A2	ITP_TDO	ITP_TDO - @m42a_1ib.M42A	11B3	MEM_DQ<53>	MEM_DQ<53> - @m42a_1ib.M42A	15B4 29A4
	FW_PORT0_TPA_P_FL	FW_PORT0_TPA_P_FL - @m42a_1ib.M42A	39A2	J2900_SAI	J2900_SAI - @m42a_1ib.M42A	29A4	MEM_DQ<54>	MEM_DQ<54> - @m42a_1ib.M42A	15B4 29A4
	FW_PORT0_TPB	FW_PORT0_TPB - @m42a_1ib.M42A	39A5	KBC_MDE	KBC_MDE - @m42a_1ib.M42A	45C2	MEM_DQ<55>	MEM_DQ<55> - @m42a_1ib.M42A	15B4 29B6
	FW_PORT0_TPB_N_FL	FW_PORT0_TPB_N_FL - @m42a_1ib.M42A	39A2	LCDVDV_PWREN_L	LCDVDV_PWREN_L - @m42a_1ib.M42A	67B7	MEM_DQ<56>	MEM_DQ<56> - @m42a_1ib.M42A	15B4 29A4
	FW_PORT0_TPB_P_FL	FW_PORT0_TPB_P_FL - @m42a_1ib.M42A	39A2	LCDVDV_PWREN_L_R	LCDVDV_PWREN_L_R - @m42a_1ib.M42A	67B6	MEM_DQ<57>	MEM_DQ<57> - @m42a_1ib.M42A	15B4 29B6
	FW_PWRON_RST_L	FW_PWRON_RST_L - @m42a_1ib.M42A	38C3	LPC_AD<0>	LPC_AD<0> - @m42a_1ib.M42A	5D2 21D4 45D8 47C6 53C6	MEM_DQ<58>	MEM_DQ<58> - @m42a_1ib.M42A	15B4 29B6
	FW_R0	FW_R0 - @m42a_1ib.M42A	38B3	LPC_AD<1>	LPC_AD<1> - @m42a_1ib.M42A	5D2 21D4 45D8 47C6 53C6	MEM_DQ<59>	MEM_DQ<59> - @m42a_1ib.M42A	15B4 29B4
	FW_R1	FW_R1 - @m42a_1ib.M42A	38C3	LPC_AD<2>	LPC_AD<2> - @m42a_1ib.M42A	5C2 21D4 45D8 47C5 53C6	MEM_DQ<60>	MEM_DQ<60> - @m42a_1ib.M42A	15A4 29B6
	FW_XI	FW_XI - @m42a_1ib.M42A	38C3	LPC_AD<3>	LPC_AD<3> - @m42a_1ib.M42A	5C2 21D4 45D8 47C5 53C6	MEM_DQ<61>	MEM_DQ<61> - @m42a_1ib.M42A	15A4 29B4
	FW_XO	FW_XO - @m42a_1ib.M42A	38C3	LPC_FRAME_L	LPC_FRAME_L - @m42a_1ib.M42A	5C2 21C5 45C8 47C6 53C6	MEM_DQ<62>	MEM_DQ<62> - @m42a_1ib.M42A	15A4 29B6
	FW_Y0	FW_Y0 - @m42a_1ib.M42A	38C3	LVDS_A_CLK_N	LVDS_A_CLK_N - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<63>	MEM_DQ<63> - @m42a_1ib.M42A	15C2 29B6
	FW_Y1	FW_Y1 - @m42a_1ib.M42A	38C3	LVDS_A_CLK_P	LVDS_A_CLK_P - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<64>	MEM_DQ<64> - @m42a_1ib.M42A	15C2 29B6
	FW_Y2	FW_Y2 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<65>	MEM_DQ<65> - @m42a_1ib.M42A	15C2 29B6
	FW_Y3	FW_Y3 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<66>	MEM_DQ<66> - @m42a_1ib.M42A	15C2 29B6
	FW_Y4	FW_Y4 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<67>	MEM_DQ<67> - @m42a_1ib.M42A	15C2 29A6
	FW_Y5	FW_Y5 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<68>	MEM_DQ<68> - @m42a_1ib.M42A	15C2 29A6
	FW_Y6	FW_Y6 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<69>	MEM_DQ<69> - @m42a_1ib.M42A	15C2 29A4
	FW_Y7	FW_Y7 - @m42a_1ib.M42A	38C3	LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m42a_1ib.M42A	13C5 67B2	MEM_DQ<70>	MEM_DQ<70> - @m42a_1ib.M42A	15C2 29B4
	FW_Y8	FW_Y8 - @m42a_1ib.M42A	38C3	LVDS_BKLTCTL	LVDS_BKLTCTL - @m42a_1ib.M42A	13C5 67C6	MEM_DQ<71>	MEM_DQ<71> - @m42a_1ib.M42A	15C2 29B6
	FW_Y9	FW_Y9 - @m42a_1ib.M42A	38C3	LVDS_BKLTCTL	LVDS_BKLTCTL - @m42a_1ib.M42A	13D5 67D7	MEM_DQ<72>	MEM_DQ<72> - @m42a_1ib.M42A	15C2 29B6
	FW_Y10	FW_Y10 - @m42a_1ib.M42A	38C3	LVDS_B_CLK_N	LVDS_B_CLK_N - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<73>	MEM_DQ<73> - @m42a_1ib.M42A	15C2 29B6
	FW_Y11	FW_Y11 - @m42a_1ib.M42A	38C3	LVDS_B_CLK_N_SPN	LVDS_B_CLK_N_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<74>	MEM_DQ<74> - @m42a_1ib.M42A	15C2 29C6
	FW_Y12	FW_Y12 - @m42a_1ib.M42A	38C3	LVDS_B_CLK_P	LVDS_B_CLK_P - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<75>	MEM_DQ<75> - @m42a_1ib.M42A	15C2 29C4
	FW_Y13	FW_Y13 - @m42a_1ib.M42A	38C3	LVDS_B_CLK_P_SPN	LVDS_B_CLK_P_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<76>	MEM_DQ<76> - @m42a_1ib.M42A	15C2 29A6
	FW_Y14	FW_Y14 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<77>	MEM_DQ<77> - @m42a_1ib.M42A	15C2 29A4
	FW_Y15	FW_Y15 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<78>	MEM_DQ<78> - @m42a_1ib.M42A	15C2 29A6
	FW_Y16	FW_Y16 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<79>	MEM_DQ<79> - @m42a_1ib.M42A	15C2 29A4
	FW_Y17	FW_Y17 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N0_SPN	LVDS_B_DATA_N0_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<80>	MEM_DQ<80> - @m42a_1ib.M42A	15C2 29A4
	FW_Y18	FW_Y18 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<81>	MEM_DQ<81> - @m42a_1ib.M42A	15C2 29B6
	FW_Y19	FW_Y19 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N1_SPN	LVDS_B_DATA_N1_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<82>	MEM_DQ<82> - @m42a_1ib.M42A	15C2 29B6
	FW_Y20	FW_Y20 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<83>	MEM_DQ<83> - @m42a_1ib.M42A	15C2 29B6
	FW_Y21	FW_Y21 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_N2_SPN	LVDS_B_DATA_N2_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<84>	MEM_DQ<84> - @m42a_1ib.M42A	15C2 29B6
	FW_Y22	FW_Y22 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<85>	MEM_DQ<85> - @m42a_1ib.M42A	15C2 29B6
	FW_Y23	FW_Y23 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<86>	MEM_DQ<86> - @m42a_1ib.M42A	15C2 29B6
	FW_Y24	FW_Y24 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m42a_1ib.M42A	6D6 13C5	MEM_DQ<87>	MEM_DQ<87> - @m42a_1ib.M42A	15C2 29B6
	FW_Y25	FW_Y25 - @m42a_1ib.M42A	38C3	LVDS_B_DATA_P2_SPN	LVDS_B_DATA_P2_SPN - @m42a_1ib.M42A	5A7 6D5	MEM_DQ<88>	MEM_DQ<88> - @m42a_1ib.M42A	15C2 29B6
	FW_Y26	FW_Y26 - @m42a_1ib.M42A	38C3	LVDS_CLKCTLA	LVDS_CLKCTLA - @m42a_1ib.M42A	13D5 67A7	MEM_DQ<89>	MEM_DQ<89> - @m42a_1ib.M42A	15C2 29B6
	FW_Y27	FW_Y27 - @m42a_1ib.M42A	38C3	LVDS_CLKCTLB	LVDS_CLKCTLB - @m42a_1ib.M42A				



	8	7	6	5	4	3	2	1
	<p>NB_CFG&lt;10&gt; NB_CFG&lt;10&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG10 - @m42a_lib.M42A 6D3            NB_CFG&lt;11&gt; NB_CFG&lt;11&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG11 - @m42a_lib.M42A 6D3            NB_CFG&lt;12&gt; NB_CFG&lt;12&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG12 - @m42a_lib.M42A 6D3            NB_CFG&lt;13&gt; NB_CFG&lt;13&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG13 - @m42a_lib.M42A 6D3            NB_CFG&lt;14&gt; NB_CFG&lt;14&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG14 - @m42a_lib.M42A 6D3            NB_CFG&lt;15&gt; NB_CFG&lt;15&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG15 - @m42a_lib.M42A 6D3            NB_CFG&lt;16&gt; NB_CFG&lt;16&gt; - @m42a_lib.M42A 14C6 20C5            NB_CFG&lt;17&gt; NB_CFG&lt;17&gt; - @m42a_lib.M42A 6D4 14C6            TP_NB_CFG17 - @m42a_lib.M42A 6D3            NB_CFG&lt;18&gt; NB_CFG&lt;18&gt; - @m42a_lib.M42A 14C6 20B5            NB_CFG&lt;19&gt; NB_CFG&lt;19&gt; - @m42a_lib.M42A 14C6 20B5            NB_CFG&lt;20&gt; NB_CFG&lt;20&gt; - @m42a_lib.M42A 1486 20A5            NB_CLK100M_GCLKIN_N NB_CLK100M_GCLKIN_N - @m42a_lib.M42A 14C4 33B2 33C4            NB_CLK100M_GCLKIN_P NB_CLK100M_GCLKIN_P - @m42a_lib.M42A 14C4 33C2 33C4            NB_CLK_DREFCLKIN_N NB_CLK_DREFCLKIN_N - @m42a_lib.M42A 14C4 33B3 33C2            NB_CLK_DREFCLKIN_P NB_CLK_DREFCLKIN_P - @m42a_lib.M42A 14C4 33B3 33C2            NB_CLK_DREFSSCLKIN_N NB_CLK_DREFSSCLKIN_N - @m42a_lib.M42A 14C4 33A4 33C2            NB_CLK_DREFSSCLKIN_P NB_CLK_DREFSSCLKIN_P - @m42a_lib.M42A 1484 33A3 33C2            NB_FSB_VREF NB_FSB_VREF - @m42a_lib.M42A 12C4            NB_FSB_XRCOMP NB_FSB_XRCOMP - @m42a_lib.M42A 12A6            NB_FSB_XSCOMP NB_FSB_XSCOMP - @m42a_lib.M42A 12A6            NB_FSB_XSWING NB_FSB_XSWING - @m42a_lib.M42A 12A6            NB_FSB_YRCOMP NB_FSB_YRCOMP - @m42a_lib.M42A 12A6            NB_FSB_YSCOMP NB_FSB_YSCOMP - @m42a_lib.M42A 12A6            NB_FSB_YSWING NB_FSB_YSWING - @m42a_lib.M42A 12A6            NB_ISENSE_R1_N NB_ISENSE_R1_N - @m42a_lib.M42A 62A6            NB_ISENSE_R1_P NB_ISENSE_R1_P - @m42a_lib.M42A 62A7            NB_ISENSE_R2_N NB_ISENSE_R2_N - @m42a_lib.M42A 62A6            NB_ISENSE_R2_P NB_ISENSE_R2_P - @m42a_lib.M42A 62A7            NB_ISENSE_VCC NB_ISENSE_VCC - @m42a_lib.M42A 62A6            NB_RIGHT_DOWN_SCREW NB_RIGHT_DOWN_SCREW - @m42a_lib.M42A 6A8            NB_RST_IN_L_R NB_RST_IN_L_R - @m42a_lib.M42A 1486            NB_SB_SYNC_L NB_SB_SYNC_L - @m42a_lib.M42A 1486 22A6            NB_TV_DCONSEL0 NB_TV_DCONSEL0 - @m42a_lib.M42A 14C6            NB_TV_DCONSEL1 NB_TV_DCONSEL1 - @m42a_lib.M42A 1684            NB_VCCSM_LF1 NB_VCCSM_LF1 - @m42a_lib.M42A 1684            NB_VCCSM_LF2 NB_VCCSM_LF2 - @m42a_lib.M42A 1688            NB_VCCSM_LF3 NB_VCCSM_LF3 - @m42a_lib.M42A 1688            NB_VCCSM_LF4 NB_VCCSM_LF4 - @m42a_lib.M42A 1688            NB_VCCSM_LF5 NB_VCCSM_LF5 - @m42a_lib.M42A 1688            NB_VTTFL_CAP1 NB_VTTFL_CAP1 - @m42a_lib.M42A 17A4            NB_VTTFL_CAP2 NB_VTTFL_CAP2 - @m42a_lib.M42A 17A4            NB_VTTFL_CAP3 NB_VTTFL_CAP3 - @m42a_lib.M42A 17B4            ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_STAR - @m42a_lib.M42A 34C7            T ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_STAR_L - @m42a_lib.M42A 34C6            T_L_R ODD_PWR_EN_SLOW_STAR ODD_PWR_EN_SLOW_STAR_L_R - @m42a_lib.M42A 34C5            ONEWIRE_DCIN_DIV ONEWIRE_DCIN_DIV - @m42a_lib.M42A 65C5            ONEWIRE_EN ONEWIRE_EN - @m42a_lib.M42A 65C7            ONEWIRE_ESD ONEWIRE_ESD - @m42a_lib.M42A 65C5            ONEWIRE_OV ONEWIRE_OV - @m42a_lib.M42A 65C6            ONEWIRE_PU_EN ONEWIRE_PU_EN - @m42a_lib.M42A 65B7            ONEWIRE_PWR_EN_L ONEWIRE_PWR_EN_L - @m42a_lib.M42A 65C8            ONEWIRE_PWR_EN_R ONEWIRE_PWR_EN_R - @m42a_lib.M42A 65C7            ONEWIRE_PWR_EN_L_DIV ONEWIRE_PWR_EN_L_DIV - @m42a_lib.M42A 65C6            P0V52_SMC_LSREF P0V52_SMC_LSREF - @m42a_lib.M42A 46D3            P1V8S0_EN_L_RC P1V8S0_EN_L_RC - @m42a_lib.M42A 63A5            P3V3S0_EN_RC P3V3S0_EN_RC - @m42a_lib.M42A 63B5            P3V3S3_EN_L_RC P3V3S3_EN_L_RC - @m42a_lib.M42A 63C5            P3V42G3H5_BOOST P3V42G3H5_BOOST - @m42a_lib.M42A 63D2            P3V42G3H_FB P3V42G3H_FB - @m42a_lib.M42A 5D7 63D2            P5V0_EN_RC P5V0_EN_RC - @m42a_lib.M42A 63C5            P5V0_EN_L_RC P5V0_EN_L_RC - @m42a_lib.M42A 63D5            PATA_PWR_EN_L PATA_PWR_EN_L - @m42a_lib.M42A 23B3 23C3            PBUS_S0_SMC_VSENSE PBUS_S0_SMC_VSENSE - @m42a_lib.M42A 48C6            PBUS_SMC_VSENSE_EN PBUS_SMC_VSENSE_EN - @m42a_lib.M42A 48C8            PBUS_SMC_VSENSE_EN_L PBUS_SMC_VSENSE_EN_L - @m42a_lib.M42A 48C7            PCIE_A_D2R_C_N PCIE_A_D2R_C_N - @m42a_lib.M42A 36D6            PCIE_A_D2R_C_P PCIE_A_D2R_C_P - @m42a_lib.M42A 36D6            PCIE_A_D2R_N PCIE_A_D2R_N - @m42a_lib.M42A 22D4 36D5            PCIE_A_D2R_P PCIE_A_D2R_P - @m42a_lib.M42A 22D4 36D5            PCIE_A_R2D_C_N PCIE_A_R2D_C_N - @m42a_lib.M42A 22D4 36C5            PCIE_A_R2D_C_P PCIE_A_R2D_C_P - @m42a_lib.M42A 22D4 36C5            PCIE_A_R2D_N PCIE_A_R2D_N - @m42a_lib.M42A 36C6            PCIE_A_R2D_P PCIE_A_R2D_P - @m42a_lib.M42A 36C6            PCIE_B_D2R_N PCIE_B_D2R_N - @m42a_lib.M42A 22D4 43C7            PCIE_B_D2R_P PCIE_B_D2R_P - @m42a_lib.M42A 22D4 43C7            PCIE_B_R2D_C_N PCIE_B_R2D_C_N - @m42a_lib.M42A 22D4 43B7            PCIE_B_R2D_C_P PCIE_B_R2D_C_P - @m42a_lib.M42A 22D4 43B7            PCIE_B_R2D_N PCIE_B_R2D_N - @m42a_lib.M42A 43B6            PCIE_B_R2D_P PCIE_B_R2D_P - @m42a_lib.M42A 43B6            PCIE_C_D2R_N PCIE_C_D2R_N - @m42a_lib.M42A 6C3 22D4            PCIE_C_D2R_P PCIE_C_D2R_P - @m42a_lib.M42A 6C3            PCIE_C_D2R_N PCIE_C_D2R_N - @m42a_lib.M42A 6C4 22D4            PCIE_C_D2R_P PCIE_C_D2R_P - @m42a_lib.M42A 6C3            PCIE_C_R2D_C_N PCIE_C_R2D_C_N - @m42a_lib.M42A 6C4 22D4            PCIE_C_R2D_C_P PCIE_C_R2D_C_P - @m42a_lib.M42A 6C4            PCIE_C_R2D_N PCIE_C_R2D_N - @m42a_lib.M42A 6C4 22D4            PCIE_C_R2D_P PCIE_C_R2D_P - @m42a_lib.M42A 6C3            PCIE_D_D2R_N PCIE_D_D2R_N - @m42a_lib.M42A 6C4 22D4            PCIE_D_D2R_P PCIE_D_D2R_P - @m42a_lib.M42A 6C3            PCIE_D_D2R_N PCIE_D_D2R_N - @m42a_lib.M42A 6C4 22D4            PCIE_D_D2R_P PCIE_D_D2R_P - @m42a_lib.M42A 6C3            PCIE_D_R2D_C_N PCIE_D_R2D_C_N - @m42a_lib.M42A 6C4 22D4            PCIE_D_R2D_C_P PCIE_D_R2D_C_P - @m42a_lib.M42A 6C3            PCIE_D_R2D_N PCIE_D_R2D_N - @m42a_lib.M42A 6C4 22C4            PCIE_D_R2D_P PCIE_D_R2D_P - @m42a_lib.M42A 6C3            PCIE_E_D2R_N PCIE_E_D2R_N - @m42a_lib.M42A 6C3            PCIE_E_D2R_P PCIE_E_D2R_P - @m42a_lib.M42A 6C4 22C4            PCIE_F_R2D_C_N PCIE_F_R2D_C_N - @m42a_lib.M42A 6C4 22C4</p>	<p>PCIE_F_R2D_C_P PCIE_F_R2D_C_P - @m42a_lib.M42A 6B4 22C4            PCIE_WAKE_L PCIE_WAKE_L - @m42a_lib.M42A 23C8 36C6 43C6            PCI_AD&lt;0&gt; PCI_AD&lt;0&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;1&gt; PCI_AD&lt;1&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;2&gt; PCI_AD&lt;2&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;3&gt; PCI_AD&lt;3&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;4&gt; PCI_AD&lt;4&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;5&gt; PCI_AD&lt;5&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;6&gt; PCI_AD&lt;6&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;7&gt; PCI_AD&lt;7&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;8&gt; PCI_AD&lt;8&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;9&gt; PCI_AD&lt;9&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;10&gt; PCI_AD&lt;10&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;11&gt; PCI_AD&lt;11&gt; - @m42a_lib.M42A 22B7 38C5            PCI_AD&lt;12&gt; PCI_AD&lt;12&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;13&gt; PCI_AD&lt;13&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;14&gt; PCI_AD&lt;14&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;15&gt; PCI_AD&lt;15&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;16&gt; PCI_AD&lt;16&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;17&gt; PCI_AD&lt;17&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;18&gt; PCI_AD&lt;18&gt; - @m42a_lib.M42A 22B7 38B5            PCI_AD&lt;19&gt; PCI_AD&lt;19&gt; - @m42a_lib.M42A 22A7 38B6            PCI_AD&lt;20&gt; PCI_AD&lt;20&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;21&gt; PCI_AD&lt;21&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;22&gt; PCI_AD&lt;22&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;23&gt; PCI_AD&lt;23&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;24&gt; PCI_AD&lt;24&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;25&gt; PCI_AD&lt;25&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;26&gt; PCI_AD&lt;26&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;27&gt; PCI_AD&lt;27&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;28&gt; PCI_AD&lt;28&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;29&gt; PCI_AD&lt;29&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;30&gt; PCI_AD&lt;30&gt; - @m42a_lib.M42A 22A7 38B5            PCI_AD&lt;31&gt; PCI_AD&lt;31&gt; - @m42a_lib.M42A 22A7 38B5            PCI_CLK_PM PCI_CLK_PM - @m42a_lib.M42A 33D6 33A5            PCI_CLK_PORT80_LPC PCI_CLK_PORT80_LPC - @m42a_lib.M42A 22A6 33D6 47C5            PCI_CLK_SMB PCI_CLK_SMB - @m42a_lib.M42A 33D6 45C8            PCI_CLK_TPM PCI_CLK_TPM - @m42a_lib.M42A 53C6 53C6            PCI_C_BE_L&lt;0&gt; PCI_C_BE_L&lt;0&gt; - @m42a_lib.M42A 22B6 38B5            PCI_C_BE_L&lt;1&gt; PCI_C_BE_L&lt;1&gt; - @m42a_lib.M42A 22B6 38B5            PCI_C_BE_L&lt;2&gt; PCI_C_BE_L&lt;2&gt; - @m42a_lib.M42A 22B6 38B5            PCI_C_BE_L&lt;3&gt; PCI_C_BE_L&lt;3&gt; - @m42a_lib.M42A 22B6 38B5            PCI_DEVSEL_L PCI_DEVSEL_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_FRAHBE_L PCI_FRAHBE_L - @m42a_lib.M42A 22B6 26C3 38A5            PCI_GNT3_L PCI_GNT3_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_IRDY_L PCI_IRDY_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_LOCK_L PCI_LOCK_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_PAR PCI_PAR - @m42a_lib.M42A 22A6 26D3 38A5            PCI_PERR_L PCI_PERR_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_PME_FW_L PCI_PME_FW_L - @m42a_lib.M42A 22B5 38A5            PCI_REQ0_L PCI_REQ0_L - @m42a_lib.M42A 22B6 26C3            PCI_REQ1_L PCI_REQ1_L - @m42a_lib.M42A 22B6 26C3            PCI_REQ2_L PCI_REQ2_L - @m42a_lib.M42A 22B6 26C3 38A5            PCI_RST_L PCI_RST_L - @m42a_lib.M42A 22A6 26C3 38A5            PCI_RST_L PCI_RST_L - @m42a_lib.M42A 22A6 26C3 38A5            PCI_SERR_L PCI_SERR_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_STOP_L PCI_STOP_L - @m42a_lib.M42A 22A6 26D3 38A5            PCI_TRDY_L PCI_TRDY_L - @m42a_lib.M42A 22A6 26D3 38A5            PEG_COMP PEG_COMP - @m42a_lib.M42A 13D3            PEG_D2R_N&lt;0&gt; PEG_D2R_N&lt;0&gt; - @m42a_lib.M42A 6D6 13D3            PEG_D2R_N0_SPN PEG_D2R_N0_SPN - @m42a_lib.M42A 13D3            PEG_D2R_N&lt;1&gt; PEG_D2R_N&lt;1&gt; - @m42a_lib.M42A 6D5 63B6            PEG_D2R_N&lt;2&gt; PEG_D2R_N&lt;2&gt; - @m42a_lib.M42A 6D6 13D3            PEG_D2R_N&lt;3&gt; PEG_D2R_N&lt;3&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;4&gt; PEG_D2R_N&lt;4&gt; - @m42a_lib.M42A 6C5            PEG_D2R_N&lt;5&gt; PEG_D2R_N&lt;5&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;6&gt; PEG_D2R_N&lt;6&gt; - @m42a_lib.M42A 6C5            PEG_D2R_N&lt;7&gt; PEG_D2R_N&lt;7&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;8&gt; PEG_D2R_N&lt;8&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;9&gt; PEG_D2R_N&lt;9&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;10&gt; PEG_D2R_N&lt;10&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_N&lt;11&gt; PEG_D2R_N&lt;11&gt; - @m42a_lib.M42A 6C5            PEG_D2R_N&lt;12&gt; PEG_D2R_N&lt;12&gt; - @m42a_lib.M42A 6C5 13C3            PEG_D2R_N&lt;13&gt; PEG_D2R_N&lt;13&gt; - @m42a_lib.M42A 6C6 13D3            PEG_D2R_N&lt;14&gt; PEG_D2R_N&lt;14&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_N&lt;15&gt; PEG_D2R_N&lt;15&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;0&gt; PEG_D2R_P&lt;0&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;1&gt; PEG_D2R_P&lt;1&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;2&gt; PEG_D2R_P&lt;2&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;3&gt; PEG_D2R_P&lt;3&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;4&gt; PEG_D2R_P&lt;4&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;5&gt; PEG_D2R_P&lt;5&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;6&gt; PEG_D2R_P&lt;6&gt; - @m42a_lib.M42A 6C5 13C3            PEG_D2R_P&lt;7&gt; PEG_D2R_P&lt;7&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;8&gt; PEG_D2R_P&lt;8&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;9&gt; PEG_D2R_P&lt;9&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;10&gt; PEG_D2R_P&lt;10&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;11&gt; PEG_D2R_P&lt;11&gt; - @m42a_lib.M42A 6C5 13C3            PEG_D2R_P&lt;12&gt; PEG_D2R_P&lt;12&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;13&gt; PEG_D2R_P&lt;13&gt; - @m42a_lib.M42A 6C6 13C3            PEG_D2R_P&lt;14&gt; PEG_D2R_P&lt;14&gt; - @m42a_lib.M42A 6B5 6B5            PEG_D2R_P&lt;15&gt; PEG_D2R_P&lt;15&gt; - @m42a_lib.M42A 6B5 6B5</p>	<p>PEG_R2D_C_N&lt;0&gt; PEG_R2D_C_N&lt;0&gt; - @m42a_lib.M42A 13C3 68C6            PEG_R2D_C_N&lt;1&gt; PEG_R2D_C_N&lt;1&gt; - @m42a_lib.M42A 13C3 68C6            PEG_R2D_C_N&lt;2&gt; PEG_R2D_C_N&lt;2&gt; - @m42a_lib.M42A 13C3 68B6            PEG_R2D_C_N&lt;3&gt; PEG_R2D_C_N&lt;3&gt; - @m42a_lib.M42A 13B3 68B6            PEG_R2D_C_N&lt;4&gt; PEG_R2D_C_N&lt;4&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_N4_SPN PEG_R2D_C_N4_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_N&lt;5&gt; PEG_R2D_C_N&lt;5&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_N&lt;6&gt; PEG_R2D_C_N&lt;6&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_N&lt;7&gt; PEG_R2D_C_N&lt;7&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_N&lt;8&gt; PEG_R2D_C_N&lt;8&gt; - @m42a_lib.M42A 6B5            PEG_R2D_C_N&lt;9&gt; PEG_R2D_C_N&lt;9&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_N&lt;10&gt; PEG_R2D_C_N&lt;10&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_N&lt;11&gt; PEG_R2D_C_N&lt;11&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_N&lt;12&gt; PEG_R2D_C_N&lt;12&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_N&lt;13&gt; PEG_R2D_C_N&lt;13&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_N&lt;14&gt; PEG_R2D_C_N&lt;14&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_N&lt;15&gt; PEG_R2D_C_N&lt;15&gt; - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_P&lt;0&gt; PEG_R2D_C_P&lt;0&gt; - @m42a_lib.M42A 13B3 68C6            PEG_R2D_C_P&lt;1&gt; PEG_R2D_C_P&lt;1&gt; - @m42a_lib.M42A 13B3 68C6            PEG_R2D_C_P&lt;2&gt; PEG_R2D_C_P&lt;2&gt; - @m42a_lib.M42A 13B3 68B6            PEG_R2D_C_P&lt;3&gt; PEG_R2D_C_P&lt;3&gt; - @m42a_lib.M42A 13B3 68B6            PEG_R2D_C_P&lt;4&gt; PEG_R2D_C_P&lt;4&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P4_SPN PEG_R2D_C_P4_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;5&gt; PEG_R2D_C_P&lt;5&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P5_SPN PEG_R2D_C_P5_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P6_SPN PEG_R2D_C_P6_SPN - @m42a_lib.M42A 6B5 13B3            PEG_R2D_C_P&lt;7&gt; PEG_R2D_C_P&lt;7&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P7_SPN PEG_R2D_C_P7_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;8&gt; PEG_R2D_C_P&lt;8&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P8_SPN PEG_R2D_C_P8_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;9&gt; PEG_R2D_C_P&lt;9&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P9_SPN PEG_R2D_C_P9_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;10&gt; PEG_R2D_C_P&lt;10&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P10_SPN PEG_R2D_C_P10_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;11&gt; PEG_R2D_C_P&lt;11&gt; - @m42a_lib.M42A 6B6 13B3            PEG_R2D_C_P&lt;12&gt; PEG_R2D_C_P&lt;12&gt; - @m42a_lib.M42A 6B5 13A3            PEG_R2D_C_P12_SPN PEG_R2D_C_P12_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;13&gt; PEG_R2D_C_P&lt;13&gt; - @m42a_lib.M42A 6B6 13A3            PEG_R2D_C_P13_SPN PEG_R2D_C_P13_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;14&gt; PEG_R2D_C_P&lt;14&gt; - @m42a_lib.M42A 6B6 13A3            PEG_R2D_C_P14_SPN PEG_R2D_C_P14_SPN - @m42a_lib.M42A 6B5            PEG_R2D_C_P&lt;15&gt; PEG_R2D_C_P&lt;15&gt; - @m42a_lib.M42A 6B6 13A3            FLT_RST_BUF_L FLT_RST_BUF_L - @m42a_lib.M42A 26B3            FLT_RST_GATED_L FLT_RST_GATED_L - @m42a_lib.M42A 26A3            FLT_RST_L FLT_RST_L - @m42a_lib.M42A 22A6 26C3            NB_RST_IN_L NB_RST_IN_L - @m42a_lib.M42A 1487 26C1            PM_BATLOW_L PM_BATLOW_L - @m42a_lib.M42A 23C1 45B8            PM_BBUSY_L PM_BBUSY_L - @m42a_lib.M42A 1486 23C5            PM_CLKRUN_L PM_CLKRUN_L - @m42a_lib.M42A 5C2 23C8 38A5 45D5 47C6 53C6            PM_DPRSFPVR_P PM_DPRSFPVR_P - @m42a_lib.M42A 1487 23C3 58D8            PM_EXTTX_L&lt;0&gt; PM_EXTTX_L&lt;0&gt; - @m42a_lib.M42A 5B2 1487 45B8            DIMM_OVERTEMP_L DIMM_OVERTEMP_L - @m42a_lib.M42A 6B1 28C4 29C4            PM_LAN_ENABLE PM_LAN_ENABLE - @m42a_lib.M42A 23C3 45D8            PM_PWRBTN_L PM_PWRBTN_L - @m42a_lib.M42A 23C4 45B8            PM_RI_L PM_RI_L - @m42a_lib.M42A 23D5            PM_RSMRST_L PM_RSMRST_L - @m42a_lib.M42A 23C1 45D8            PM_SB_PWROK PM_SB_PWROK - @m42a_lib.M42A 23C3 26A6            PM_SLP_S3 PM_SLP_S3 - @m42a_lib.M42A 48C8 63B7            PM_SLP_S3BATT PM_SLP_S3BATT - @m42a_lib.M42A 60C7            PM_SLP_S3_L PM_SLP_S3_L - @m42a_lib.M42A 23C3 45C5 63A7 63A7 63B8            PM_SLP_S3_L1V26 PM_SLP_S3_L1V26 - @m42a_lib.M42A 63B7            PM_SLP_S4_L PM_SLP_S4_L - @m42a_lib.M42A 23C3 45C5 60C8 61B8 63D6            PM_SLP_S5_L PM_SLP_S5_L - @m42a_lib.M42A 23C3 45C5 46D3            PM_STPCPU_L PM_STPCPU_L - @m42a_lib.M42A 23C8 32C4            PM_STPPCI_L PM_STPPCI_L - @m42a_lib.M42A 23C8 32C4            PM_SUS_STAT_L PM_SUS_STAT_L - @m42a_lib.M42A 5C2 23C5 45D5 46D3 47C5 53C6            PM_SYSTRIP_L PM_SYSTRIP_L - @m42a_lib.M42A 23C5 26C5 45C8            XDP_DBRSTRT_L XDP_DBRSTRT_L - @m42a_lib.M42A 26C6            FM_THRMTRIP_L FM_THRMTRIP_L - @m42a_lib.M42A 70C 1486 21C2 46B3            FM_THRM_L FM_THRM_L - @m42a_lib.M42A 23C8 45B8            PPOV9_S0 PPOV9_S0 - @m42a_lib.M42A 5A2 64D7            =PPOV9_S0_MEM_TERM - @m42a_lib.M42A 30D4 64D6            =PPOV9_S0_MEM_REG - @m42a_lib.M42A 31B3 63B2 64D8            =PPOV9_S0_MEM_TERM - @m42a_lib.M42A 30D4 64D6            =PPOV9_S0_MEM_REG - @m42a_lib.M42A 31B3 63B2 64D8            PPIV2_S0 PPIV2_S0 - @m42a_lib.M42A 63B4            PPIV2_S3 PPIV2_S3 - @m42a_lib.M42A 5A2 64C4            =PPIV2_S3_REG - @m42a_lib.M42A 60B2 63B5 64C5            =PPIV2_S3_ENET - @m42a_lib.M42A 36A8 36D7 64C3            =PPIV2_S3_REG - @m42a_lib.M42A 60B2 63B5 64C5            =PPIV2_S3_ENET - @m42a_lib.M42A 36A8 36D7 64C3            PPIV5_S0_DPLL PPIV5_S0_DPLL - @m42a_lib.M42A 19A4            PPIV5_S0_NB_3GPLL_F PPIV5_S0_NB_3GPLL_F - @m42a_lib.M42A 19A4            PPIV5_S0_NB_QTVDAC PPIV5_S0_NB_QTVDAC - @m42a_lib.M42A 19A7            PPIV5_S0_NB_VCC3G PPIV5_S0_NB_VCC3G - @m42a_lib.M42A 17D6 19B2            PPIV5_S0_NB_VCCA_3GP PPIV5_S0_NB_VCCA_3GP - @m42a_lib.M42A 17D6 19A2            PPIV5_S0_NB_VCCA_DPL PPIV5_S0_NB_VCCA_DPL - @m42a_lib.M42A 17C6 19D4            PPIV5_S0_NB_VCCA_DPLB PPIV5_S0_NB_VCCA_DPLB - @m42a_lib.M42A 17C6 19D4            PPIV5_S0_NB_VCCA_HPL PPIV5_S0_NB_VCCA_HPL - @m42a_lib.M42A 17C6 19C4            PPIV5_S0_NB_VCCA_MPL PPIV5_S0_NB_VCCA_MPL - @m42a_lib.M42A 17C6 19C4            PPIV5_S0_NB_VCCD_QTV PPIV5_S0_NB_VCCD_QTV - @m42a_lib.M42A 17B6 19A5            PPIV5_S0_NB_VCCD_TVD PPIV5_S0_NB_VCCD_TVD - @m42a_lib.M42A 17C6 19A5            PPIV5_S0_NB_VCCA_DPLB PPIV5_S0_NB_VCCA_DPLB - @m42a_lib.M42A 17C6 19D4            PPIV5_S0_REG_P PPIV5_S0_REG_P - @m42a_lib.M42A 62B8            PPIV5_S0_SB_VCC1_5_B PPIV5_S0_SB_VCC1_5_B - @m42a_lib.M42A 22C1 24D5 25B6            PPIV5_S0_SB_VCCMIFLL_P PPIV5_S0_SB_VCCMIFLL_P - @m42a_lib.M42A 24B5 25A5            PPIV5_S0_SB_VCCMIFLL_L PPIV5_S0_SB_VCCMIFLL_L - @m42a_lib.M42A 25A7</p>	<p>PP1V8_S0 PP1V8_S0 - @m42a_lib.M42A 5B2 64C7            =PP1V8_S0_TMSD - @m42a_lib.M42A 64B6 68D6 68D6            =PP1V8_S0_FET - @m42a_lib.M42A 63B3 64B8            =PP1V8_S0_TMSD - @m42a_lib.M42A 64B6 68D6 68D6            =PP1V8_S0_FET - @m42a_lib.M42A 63B3 64B8            =PP1V8_S0_TMSD - @m42a_lib.M42A 64B6 68D6 68D6            =PP1V8_S0_FET - @m42a_lib.M42A 63B3 64B8            PP1V8_S0_ANALOG_SDVO PP1V8_S0_ANALOG_SDVO - @m42a_lib.M42A 68C4 68D3            _F PP1V8_S0_TMSD_F PP1V8_S0_TMSD_F - @m42a_lib.M42A 68B4 68D3            PP1V8_S3 PP1V8_S3 - @m42a_lib.M42A 5B2 64C4            =PP1V8_S3_IV2S3 - @m42a_lib.M42A 60B5 64C3            =PP1V8_S3_MEM_NB_SENSE - @m42a_lib.M42A 61C4 64C3            =PP1V8_S3_MEM_NB_SENSE - @m42a_lib.M42A 61C4 64C3            =PP1</p>				



	8	7	6	5	4	3	2	1
	TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m42a_lib.M42A	14C6					
	TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m42a_lib.M42A	14C6					
	TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m42a_lib.M42A	22B6					
	TP_PCI_GNT1_L	TP_PCI_GNT1_L - @m42a_lib.M42A	22B6					
	TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m42a_lib.M42A	22B6					
	TP_PCI_PME_L	TP_PCI_PME_L - @m42a_lib.M42A	22A6					
	TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m42a_lib.M42A	21C6					
	TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m42a_lib.M42A	21C6					
	TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m42a_lib.M42A	21D4					
	TP_SB_GPI06	TP_SB_GPI06 - @m42a_lib.M42A	23C5					
	TP_SB_GPI022	TP_SB_GPI022 - @m42a_lib.M42A	6B1 22B6					
		=SB_GPI022 - @m42a_lib.M42A	6B2 69A6					
		SB_GPI022 - @m42a_lib.M42A	6B2					
		=SB_GPI022 - @m42a_lib.M42A	6B2 69A6					
	TP_SB_GPI023	TP_SB_GPI023 - @m42a_lib.M42A	21D5					
	TP_SB_GPI025_DO_NOT_USE	TP_SB_GPI025_DO_NOT_USE - @m42a_lib.M42A	23C3					
	TP_SB_GPI038	TP_SB_GPI038 - @m42a_lib.M42A	23C3					
	TP_SB_RCVENIN_L	TP_SB_RCVENIN_L - @m42a_lib.M42A	15B2					
	TP_SB_RSVD9	TP_SB_RSVD9 - @m42a_lib.M42A	22A6					
	TP_SB_SATALED_L	TP_SB_SATALED_L - @m42a_lib.M42A	21C6					
	TP_SB_XOR-AD5	TP_SB_XOR-AD5 - @m42a_lib.M42A	22A7					
	TP_SB_XOR-AD9	TP_SB_XOR-AD9 - @m42a_lib.M42A	22A7					
	TP_SB_XOR-AE5	TP_SB_XOR-AE5 - @m42a_lib.M42A	22A7					
	TP_SB_XOR-AG4	TP_SB_XOR-AG4 - @m42a_lib.M42A	22A7					
	TP_SB_XOR-AH4	TP_SB_XOR-AH4 - @m42a_lib.M42A	22A7					
	TP_SB_XOR-U3	TP_SB_XOR-U3 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-U7	TP_SB_XOR-U7 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-V6	TP_SB_XOR-V6 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-V7	TP_SB_XOR-V7 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-Y1	TP_SB_XOR-Y1 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-Y2	TP_SB_XOR-Y2 - @m42a_lib.M42A	21C6					
	TP_SB_XOR-AE9	TP_SB_XOR-AE9 - @m42a_lib.M42A	22A6					
	TP_SB_XOR-AG8	TP_SB_XOR-AG8 - @m42a_lib.M42A	22A6					
	TP_SB_XOR-AH8	TP_SB_XOR-AH8 - @m42a_lib.M42A	22A6					
	TP_SB_XOR-W1	TP_SB_XOR-W1 - @m42a_lib.M42A	21C6					
	TP_USBN_F	TP_USBN_F - @m42a_lib.M42A	5C1					
	TP_USBP_F	TP_USBP_F - @m42a_lib.M42A	5C1					
	TV_DACA_OUT	TV_DACA_OUT - @m42a_lib.M42A	13C5 69B8					
	TV_DACB_OUT	TV_DACB_OUT - @m42a_lib.M42A	13C5 69A8					
	TV_DACC_OUT	TV_DACC_OUT - @m42a_lib.M42A	13C5 69A8					
	TV_IREF	TV_IREF - @m42a_lib.M42A	13C5 69C8					
	USB2_BT_F_N	USB2_BT_F_N - @m42a_lib.M42A	44C4					
	USB2_BT_F_P	USB2_BT_F_P - @m42a_lib.M42A	44B4					
	USB2_CAMERA_CONN_N	USB2_CAMERA_CONN_N - @m42a_lib.M42A	67A2					
	USB2_CAMERA_CONN_P	USB2_CAMERA_CONN_P - @m42a_lib.M42A	67B2					
	USB2_EXTA_F_N	USB2_EXTA_F_N - @m42a_lib.M42A	42C2					
	USB2_EXTA_F_P	USB2_EXTA_F_P - @m42a_lib.M42A	42C2					
	USB2_EXTB_F_N	USB2_EXTB_F_N - @m42a_lib.M42A	42B2					
	USB2_EXTB_F_P	USB2_EXTB_F_P - @m42a_lib.M42A	42B2					
	USB2_GND_EXTA_F	USB2_GND_EXTA_F - @m42a_lib.M42A	42C2					
	USB2_GND_EXTB_F	USB2_GND_EXTB_F - @m42a_lib.M42A	42B2					
	USB_A_N	USB_A_N - @m42a_lib.M42A	6C1 22C2					
		=USB2_EXTA_N - @m42a_lib.M42A	6C2 42C5					
		USB2_EXTA_N - @m42a_lib.M42A	6C2					
		=USB2_EXTA_N - @m42a_lib.M42A	6C2 42C5					
	USB_A_OC_L	USB_A_OC_L - @m42a_lib.M42A	6C1 22C4 22D8					
		=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8					
		EXTAUSB_OC_L - @m42a_lib.M42A	6C2					
		=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8					
	USB_A_P	USB_A_P - @m42a_lib.M42A	6C1 22C2					
		=USB2_EXTA_P - @m42a_lib.M42A	6C2 42C5					
		USB2_EXTA_P - @m42a_lib.M42A	6C2					
		=USB2_EXTA_P - @m42a_lib.M42A	6C2 42C5					
	USB_B_N	USB_B_N - @m42a_lib.M42A	6C1 22C2					
		=USB2_GEVSEER_N - @m42a_lib.M42A	6C2 40C7					
		USB2_GEVSEER_N - @m42a_lib.M42A	6C2					
		=USB2_GEVSEER_N - @m42a_lib.M42A	6C2 40C7					
	USB_B_OC_L	USB_B_OC_L - @m42a_lib.M42A	22C4 22D8					
	USB_B_P	USB_B_P - @m42a_lib.M42A	6C1 22C2					
		=USB2_GEVSEER_P - @m42a_lib.M42A	6C2 40C7					
		USB2_GEVSEER_P - @m42a_lib.M42A	6C2					
		=USB2_GEVSEER_P - @m42a_lib.M42A	6C2 40C7					
	USB_C_N	USB_C_N - @m42a_lib.M42A	6C1 22C2					
		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5					
		USB2_EXTB_N - @m42a_lib.M42A	6C2					
		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5					
	USB_C_P	USB_C_P - @m42a_lib.M42A	6C1 22C2					
		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5					
		USB2_EXTB_P - @m42a_lib.M42A	6C2					
		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5					
	USB_D_OC_L	USB_D_OC_L - @m42a_lib.M42A	22C4 22D8					
	USB_E_N	USB_E_N - @m42a_lib.M42A	6C1 22C2					
		TP_USBN_E - @m42a_lib.M42A	5C1 6C2					
		USB_E_OC_L - @m42a_lib.M42A	22C4 22D8					
		USB_E_P - @m42a_lib.M42A	6C1 22C2					
		TP_USBP_E - @m42a_lib.M42A	5C1 6C2					
	USB_F_N	USB_F_N - @m42a_lib.M42A	6C1 22C2					
		=USB2_IR_N - @m42a_lib.M42A	6C2 41C6					
		USB_IR_N - @m42a_lib.M42A	6C2					
		=USB2_IR_N - @m42a_lib.M42A	6C2 41C6					
	USB_F_P	USB_F_P - @m42a_lib.M42A	6C1 22C2					
		=USB2_IR_P - @m42a_lib.M42A	6C2 41C6					
		USB_IR_P - @m42a_lib.M42A	6C2					
		=USB2_IR_P - @m42a_lib.M42A	6C2 41C6					
	USB_G_N	USB_G_N - @m42a_lib.M42A	6B1 22C2					
		=USB2_BT_N - @m42a_lib.M42A	6B2 44C6					
		USB_BT_N - @m42a_lib.M42A	6B2					
		=USB2_BT_N - @m42a_lib.M42A	6B2 44C6					
	USB_G_P	USB_G_P - @m42a_lib.M42A	6B1 22C2					
		=USB2_BT_P - @m42a_lib.M42A	6C2 44C6					
		USB_BT_P - @m42a_lib.M42A	6C2					
		=USB2_BT_P - @m42a_lib.M42A	6C2 44C6					
	USB_RBIA5_PN	USB_RBIA5_PN - @m42a_lib.M42A	22C2					
	VGA_B	VGA_B - @m42a_lib.M42A	69B4					
	VGA_G	VGA_G - @m42a_lib.M42A	69B4					
	VGA_HSYNC	VGA_HSYNC - @m42a_lib.M42A	69B4 69C1					
	VGA_R	VGA_R - @m42a_lib.M42A	69A4					
	VGA_VSYNC	VGA_VSYNC - @m42a_lib.M42A	69B4 69C1					
	VOL_DOWN	VOL_DOWN - @m42a_lib.M42A	54B7 54C7					
	VOL_UP	VOL_UP - @m42a_lib.M42A	54B7 54C7					
	VREG_FB	VREG_FB - @m42a_lib.M42A	54A4					
	VR_PWRGD_CK410	VR_PWRGD_CK410 - @m42a_lib.M42A	23C5 26A8					
	VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m42a_lib.M42A	14B6 26B5 58C7					
	XDP_BPM_L<0>	XDP_BPM_L<0> - @m42a_lib.M42A	7C6 11B2					
	XDP_BPM_L<1>	XDP_BPM_L<1> - @m42a_lib.M42A	7C6 11B2					
	XDP_BPM_L<2>	XDP_BPM_L<2> - @m42a_lib.M42A	7C6 11B2					
	XDP_BPM_L<3>	XDP_BPM_L<3> - @m42a_lib.M42A	7C6 11B3					
	XDP_BPM_L<4>	XDP_BPM_L<4> - @m42a_lib.M42A	7C6 11B2					
	XDP_BPM_L<5>	XDP_BPM_L<5> - @m42a_lib.M42A	7C6 11B2					
	XDP_DBRESET_L	XDP_DBRESET_L - @m42a_lib.M42A	7C6 11B4 26C6					
	XDP_TCK	XDP_TCK - @m42a_lib.M42A	7A8 7C6 11B2 11B3					
	XDP_TDI	XDP_TDI - @m42a_lib.M42A	7B8 7C6 11B3					
	XDP_TDO	XDP_TDO - @m42a_lib.M42A	7C6 11B5					
	XDP_TMS	XDP_TMS - @m42a_lib.M42A	7B8 7C6 11B2					
	XDP_TRST_L	XDP_TRST_L - @m42a_lib.M42A	7C6 11B3					

8			7			6			5			4			3			2			1		
Title: Cref Part Report			C2500 CAP_P_SMB2			m42a[25B8]			C3804 CAP_402			m42a[34B5]			C5921 CAP_402			m42a[46C6]					
Design: m42a			C2501 CAP_402			m42a[25A6]			C3805 CAP_402			m42a[34B3]			C5951 CAP_402			m42a[46A4]					
Date: Aug 5 16:01:17 2006			C2502 CAP_402			m42a[25D4]			C3806 CAP_603			m42a[34B3]			C5965 CAP_402			m42a[46B8]					
C0607 CAP_402			m42a[6C7]			C2503 CAP_402			m42a[25D8]			C3875 CAP_402			m42a[34C7]			C5966 CAP_603			m42a[46B7]		
C0608 CAP_402			m42a[6C7]			C2504 CAP_402			m42a[25C8]			C3876 CAP_402			m42a[34C5]			C5967 CAP_402			m42a[46B7]		
C0610 CAP_402			m42a[6C7]			C2505 CAP_402			m42a[25B7]			C3900 CAP_402			m42a[35D6]			C5977 CAP_402			m42a[46C2]		
C0611 CAP_402			m42a[6A8]			C2506 CAP_402			m42a[25B7]			C3901 CAP_402			m42a[35D5]			C6100 CAP_402			m42a[48D3]		
C0612 CAP_402			m42a[6A8]			C2507 CAP_402			m42a[25B7]			C3902 CAP_402			m42a[35C6]			C6101 CAP_402			m42a[48C3]		
C0613 CAP_402			m42a[6A8]			C2508 CAP_603			m42a[25A6]			C3903 CAP_402			m42a[35D5]			C6102 CAP_402			m42a[48C2]		
C0614 CAP_402			m42a[6A8]			C2509 CAP_402			m42a[25B8]			C3920 CAP_402			m42a[35C7]			C6103 CAP_402			m42a[48C3]		
C0615 CAP_402			m42a[6A8]			C2510 CAP_402			m42a[25C1]			C3921 CAP_603			m42a[35C6]			C6104 CAP_402			m42a[48D4]		
C0616 CAP_402			m42a[6B7]			C2511 CAP_402			m42a[25D6]			C3922 CAP_402			m42a[35C5]			C6105 CAP_402			m42a[48C4]		
C0617 CAP_402			m42a[6B7]			C2512 CAP_402			m42a[25B1]			C3923 CAP_402			m42a[35C6]			C6112 CAP_402			m42a[48B2]		
C0618 CAP_402			m42a[6A8]			C2513 CAP_402			m42a[25C6]			C3950 CAP_603			m42a[35B8]			C6150 CAP_402			m42a[48C6]		
C0619 CAP_402			m42a[6A7]			C2514 CAP_402			m42a[25C6]			C4100 CAP_402			m42a[36D6]			C6200 CAP_402			m42a[49C5]		
C0630 CAP_402			m42a[6C7]			C2515 CAP_402			m42a[25B6]			C4101 CAP_402			m42a[36D6]			C6201 CAP_402			m42a[49C5]		
C0900 CAP_805			m42a[9B5]			C2516 CAP_P_CASE-C2			m42a[25D3]			C4102 CAP_402			m42a[36D5]			C6202 CAP_402			m42a[49D4]		
C0901 CAP_805			m42a[9B6]			C2517 CAP_402			m42a[25D6]			C4103 CAP_402			m42a[36D5]			C6250 CAP_402			m42a[49A5]		
C0902 CAP_805			m42a[9A5]			C2518 CAP_402			m42a[25D4]			C4104 CAP_402			m42a[36D5]			C6251 CAP_402			m42a[49A5]		
C0904 CAP_805			m42a[9A6]			C2519 CAP_402			m42a[25D3]			C4105 CAP_402			m42a[36D5]			C6252 CAP_402			m42a[49B4]		
C0907 CAP_805			m42a[9B4]			C2520 CAP_402			m42a[25B6]			C4106 CAP_402			m42a[36D4]			C6301 CAP_402			m42a[50C2]		
C0908 CAP_805			m42a[9B6]			C2521 CAP_402			m42a[25C3]			C4107 CAP_402			m42a[36D4]			C6308 CAP_402			m42a[50C5]		
C0909 CAP_805			m42a[9B5]			C2522 CAP_402			m42a[25B3]			C4110 CAP_402			m42a[36D5]			C6309 CAP_402			m42a[50C6]		
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C0913 CAP_805			m42a[9A7]			C2526 CAP_402			m42a[25A4]			C4115 CAP_402			m42a[36B4]			C6605 CAP_402			m42a[52B4]		
C0918 CAP_805			m42a[9A7]			C2527 CAP_402			m42a[25A3]			C4116 CAP_402			m42a[36A4]			C6606 CAP_402			m42a[52B4]		
C0920 CAP_805			m42a[9A4]			C2528 CAP_402			m42a[25A3]			C4117 CAP_402			m42a[36B3]			C6620 CAP_402			m42a[52C4]		
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C0926 CAP_402			m42a[9A7]			C2531 CAP_402			m42a[25D1]			C4127 CAP_402			m42a[36A8]			C6702 CAP_402			m42a[53C3]		
C0928 CAP_805			m42a[9B5]			C2532 CAP_402			m42a[25C1]			C4128 CAP_402			m42a[36A7]			C6703 CAP_402			m42a[53C3]		
C0929 CAP_805			m42a[9B4]			C2533 CAP_402			m42a[25C1]			C4129 CAP_402			m42a[36A7]			C6795 CAP_402			m42a[53C6]		
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C0936 CAP_402			m42a[9B6]			C2609 CAP_402			m42a[26C7]			C4134 CAP_402			m42a[36A6]			C6803 CAP_P_CASE-B3-LF			m42a[54D3]		
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C0938 CAP_402			m42a[9B5]			C2611 CAP_402			m42a[26B8]			C4136 CAP_402			m42a[36A5]			C6805 CAP_603			m42a[54B4]		
C0939 CAP_805			m42a[9A4]			C2680 CAP_402			m42a[26B3]			C4137 CAP_402			m42a[36A4]			C6806 CAP_603			m42a[54B3]		
C0940 CAP_P_3P_D2T			m42a[9B5]			C2800 CAP_402			m42a[28D7]			C4138 CAP_402			m42a[36A4]			C6807 CAP_P_SMA-LF			m42a[54B3]		
C0941 CAP_P_3P_D2T			m42a[9A7]			C2809 CAP_603			m42a[28B2]			C4139 CAP_402			m42a[36A4]			C6810 CAP_P_SMA-LF			m42a[54B2]		
C0942 CAP_P_3P_D2T			m42a[9A7]			C2810 CAP_402			m42a[28B2]			C4140 CAP_402			m42a[36B3]			C6812 CAP_402			m42a[54B4]		
C0943 CAP_P_3P_D2T			m42a[9A6]			C2811 CAP_402			m42a[28B2]			C4150 CAP_402			m42a[36B6]			C6813 CAP_402			m42a[54B3]		
C0944 CAP_P_3P_D2T			m42a[9A6]			C2812 CAP_402			m42a[28A7]			C4151 CAP_402			m42a[36B6]			C6821 CAP_402			m42a[54D5]		
C0946 CAP_P_3P_D2T			m42a[9A5]			C2813 CAP_402			m42a[28B1]			C4200 CAP_402			m42a[37C7]			C6822 CAP_603			m42a[54A5]		
C0950 CAP_402			m42a[9D7]			C2814 CAP_402			m42a[28B2]			C4201 CAP_402			m42a[37C6]			C6823 CAP_402			m42a[54A5]		
C0951 CAP_603			m42a[9D7]			C2815 CAP_402			m42a[28B2]			C4202 CAP_402			m42a[37C6]			C6825 CAP_402			m42a[54A4]		
C1001 CAP_402			m42a[10B5]			C2816 CAP_402			m42a[28B1]			C4203 CAP_402			m42a[37C6]			C6830 CAP_402			m42a[54D4]		
C1002 CAP_402			m42a[10C4]			C2817 CAP_402			m42a[28B1]			C4204 CAP_402			m42a[37C7]			C6833 CAP_402			m42a[54B2]		
C1100 CAP_402			m42a[11B3]			C2820 CAP_402			m42a[28D7]			C4205 CAP_402			m42a[37C6]			C6835 CAP_402			m42a[54D6]		
C1111 CAP_402			m42a[12C3]			C2821 CAP_402			m42a[28A7]			C4206 CAP_402			m42a[37C6]			C6836 CAP_402			m42a[54D3]		
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C1236 CAP_402			m42a[12A6]			C2830 CAP_402			m42a[28B2]			C4210 CAP_1808			m42a[37A6]			C7200 CAP_P_SMC-LF			m42a[55D6]		
C1415 CAP_402			m42a[14C3]			C2831 CAP_402			m42a[28B2]			C4211 CAP_402			m42a[37A6]			C7201 CAP_P_CASE-B3-LF			m42a[55C4]		
C1416 CAP_402			m42a[14C2]			C2832 CAP_402			m42a[28B1]			C4212 CAP_402			m42a[37A5]			C7202 CAP_603			m42a[55C4]		
C1610 CAP_402			m42a[16B5]			C2900 CAP_402			m42a[29D7]			C4211 CAP_402			m42a[38C2]			C7203 CAP_P_CASE-B3-LF			m42a[55B4]		
C1611 CAP_402			m42a[16B4]			C2909 CAP_603			m42a[29B2]			C4412 CAP_402			m42a[38C2]			C7204 CAP_603			m42a[55B4]		
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C1613 CAP_402			m42a[16B8]			C2911 CAP_402			m42a[29B2]			C4417 CAP_402			m42a[38D4]			C7206 CAP_603			m42a[55B4]		
C1614 CAP_402			m42a[16B8]			C2912 CAP_402			m42a[29B1]			C4418 CAP_402			m42a[38D4]			C7207 CAP_402			m42a[55C5]		
C1615 CAP_402			m42a[16B6]			C2913 CAP_402			m42a[29B1]			C4420 CAP_402			m42a[38C3]			C7208 CAP_402			m42a[55B5]		
C1620 CAP_603			m42a[16B5]			C2914 CAP_402			m42a[29B2]			C4422 CAP_402			m42a[38D4]			C7209 CAP_402			m42a[55A5]		
C1621 CAP_603			m42a[16B5]			C2915 CAP_402			m42a[29B2]			C4424 CAP_603			m42a[38D5]			C7210 CAP_402			m42a[55C6]		
C1711 CAP_402			m42a[17A3]			C2916 CAP_603			m42a[29B1]			C4425 CAP_402			m42a[38D3]			C7211 CAP_402			m42a[55C5]		
C1712 CAP_402			m42a[17A3]			C2917 CAP_402			m42a[29B1]			C4426 CAP_402			m42a[38D4]			C7220 CAP_402			m42a[55B6]		
C1713 CAP_402			m42a[17B3]			C2920 CAP_402			m42a[29D7]			C4428 CAP_402			m42a[38D3]			C7221 CAP_402			m42a[55B5]		
C1900 CAP_P_3P_D2T			m42a[19B8]			C2921 CAP_402			m42a[29A7]			C4429 CAP_402			m42a[38D3]			C7230 CAP_402			m42a[55A6]		
C1902 CAP_603			m42a[19B7]			C2922 CAP_402			m42a[29A7]			C4430 CAP_402			m42a[38D3]			C7231 CAP_402			m42a[55A5]		
C1903 CAP_603			m42a[19B7]			C2930 CAP_402			m42a[29B2]			C4432 CAP_402			m42a[38D3]			C7260 CAP_402			m42a[55D2]		
C1904 CAP_402			m42a[19B6]			C2931 CAP_402			m42a[29B2]			C4500 CAP_402			m42a[39B5]			C7261 CAP_402			m42a[55C2]		
C1906 CAP_402			m42a[19B6]			C2932 CAP_402			m42a[29B1]			C4501 CAP_402			m42a[39A5]			C7270 CAP_402			m42a[55C2]		
C1907 CAP_402			m42a[19B5]			C3000 CAP_402			m42a[30D4]			C4510 CAP_402			m42a[39C3]			C7271 CAP_402			m42a[55B2]		
C1910 CAP_603			m42a[19B8]			C3001 CAP_402			m42a[30D3]			C4520 CAP_402			m42a[39A4]			C7280 CAP_402			m42a[55B2]		
C1911 CAP_402			m42a[19B7]			C3002 CAP_402			m42a[30D4]			C4521 CAP_402			m42a[39B3]			C7281 CAP_402			m42a[55B2]		
C1912 CAP_603			m42a[19B8]			C3003 CAP_402			m42a[30D3]			C4522 CAP_402			m42a[39A4]			C7300 CAP_402			m42a[56C7]		
C1913 CAP_402			m42a[19B7]			C3004 CAP_402			m42a[30D4]			C4523 CAP_402			m42a[39A3]			C7301 CAP_402			m42a[56C5]		
C1914 CAP_603			m42a[19B6]			C3005 CAP_402			m42a[30D3														

	8	7	6	5	4	3	2	1				
D	C7507	CAP_402	m42a[58B7]	C7981	CAP_603	m42a[62C4]	C9820	CAP_402	m42a[69A4]	L1922	IND_0603	m42a[19A7]
	C7508	CAP_P_CASED2E-SM	m42a[58C3]	C7989	CAP_402	m42a[62B4]	C9821	CAP_402	m42a[69A3]	L1934	IND_0603	m42a[19C5]
	C7509	CAP_P_CASED2E-SM	m42a[58D3]	C7990	CAP_805	m42a[62A7]	C9824	CAP_402	m42a[69B5]	L1936	IND_0603	m42a[19C5]
	C7510	CAP_402	m42a[58C8]	C7991	CAP_805	m42a[62A7]	C9834	CAP_402	m42a[69A4]	L1970	IND_1210	m42a[19B4]
	C7511	CAP_402	m42a[58B3]	C7992	CAP_P_CASE-D2E-LF	m42a[62B1]	C9839	CAP_402	m42a[69B7]	L1975	IND_0805	m42a[19A4]
	C7512	CAP_402	m42a[58C3]	C7999	CAP_402	m42a[62A6]	C9842	CAP_402	m42a[69C1]	L1985	IND_0603	m42a[19D3]
	C7513	CAP_402	m42a[58B7]	C8000	CAP_402	m42a[63D4]	C9843	CAP_402	m42a[69C1]	L1990	IND_0603	m42a[19C3]
	C7514	CAP_402	m42a[58B8]	C8005	CAP_402	m42a[63C4]	C9860	CAP_402	m42a[69C2]	L2500	IND_SM-3	m42a[25B8]
	C7515	CAP_402	m42a[58C5]	C8010	CAP_402	m42a[63C4]	D1986	DIODE_SCHOT_6PB_SOT-363	m42a[19C2 19D2]	L2507	IND_1206	m42a[25A7]
	C7516	CAP_402	m42a[58B4]	C8015	CAP_402	m42a[63B4]	D2502	DIODE_SCHOT_6PB_SOT-363	m42a[25C8 25D8]	L3301	IND_0402-LF	m42a[32D7]
	C7517	CAP_P_CASED2E-SM	m42a[58D3]	C8025	CAP_402	m42a[63A4]	D2600	DIODE_SCHOT_6PB_SOT-363	m42a[26D5 26E5]	L3302	IND_0402-LF	m42a[32D3]
	C7518	CAP_603	m42a[58D2]	C8060	CAP_402	m42a[63B3]	D4520	DIODE_DUAL_6P_SOT-36	m42a[39B4 39B3]	L3901	FILTER_4P_2012H	m42a[35D6]
	C7521	CAP_402	m42a[58A6]	C8061	CAP_402	m42a[63B2]	D4521	DIODE_DUAL_6P_SOT-36	m42a[39A4 39A3]	L3902	FILTER_4P_2012H	m42a[35D5]
	C7526	CAP_603	m42a[58D7]	C8062	CAP_402	m42a[63B2]	D4550	DIODE_DUAL_6P_SOT-36	m42a[39A4 39A3]	L3912	IND_0402	m42a[35C6]
	C7527	CAP_402	m42a[58C5]	C8090	CAP_1206-1	m42a[63C3]	D5200	DIODE_SCHOT_3P_A_SC-75	m42a[42C3]	L4100	IND_0402-LF	m42a[36D3]
	C7528	CAP_402	m42a[58B5]	C8091	CAP_402	m42a[63D2]	D5201	DIODE_SCHOT_3P_A_SC-75	m42a[42A3]	L4250	IND_0402-LF	m42a[37D7]
	C7529	CAP_402	m42a[58B5]	C8092	CAP_402	m42a[63D1]	D7500	DIODE_SCHOT_SMB	m42a[58C3]	L4400	IND_0402	m42a[38D4]
	C7530	CAP_402	m42a[58C7]	C8093	CAP_805	m42a[63D1]	D7501	DIODE_SCHOT_SMB	m42a[58B3]	L4510	IND_SM	m42a[39C3]
	C7531	CAP_402	m42a[58B5]	C8202	CAP_402	m42a[65D7]	D4550	ZENER_SOT23	m42a[39A6]	L4550	IND_SM-1	m42a[39A7]
	C7532	CAP_402	m42a[58B6]	C8203	CAP_402	m42a[65C7]	D4590	DIODE_SCHOT_SMB	m42a[39D4]	L4900	IND_0402	m42a[40D5]
	C7533	CAP_402	m42a[58B6]	C8205	CAP_402	m42a[65A5]	D4591	DPAK3P_SOT-363	m42a[39C5 39C5]	L4901	FILTER_4P_SM	m42a[40C6]
	C7534	CAP_402	m42a[58B5]	C8206	CAP_402	m42a[65A4]	D4900	DIODE_SCHOT_3P_A_SC-75	m42a[40C6]	L4902	IND_0402	m42a[40C5]
	C7535	CAP_603	m42a[58D6]	C8209	CAP_402	m42a[65A5]	D5200	DIODE_SCHOT_3P_A_SC-75	m42a[42C3]	L5200	FILTER_4P_SM	m42a[42C4]
	C7590	CAP_402	m42a[58C3]	C8211	CAP_402	m42a[65A5]	D5201	DIODE_SCHOT_3P_A_SC-75	m42a[42A3]	L5201	FILTER_4P_SM	m42a[42B4]
	C7592	CAP_402	m42a[58B3]	C8215	CAP_402	m42a[65A4]	D7500	DIODE_SCHOT_SMB	m42a[58C3]	L5202	IND_0402-LF	m42a[42D4]
C7596	CAP_402	m42a[58D7]	C8217	CAP_603	m42a[65C2]	D7501	DIODE_SCHOT_SMB	m42a[58B3]	L5203	IND_0402-LF	m42a[42C4]	
C7599	CAP_603	m42a[58C2]	C8218	CAP_402	m42a[65C4]	D7624	DIODE_SCHOT_SOD-323	m42a[59C6]	L5204	IND_0402-LF	m42a[42C3]	
C7600	CAP_603	m42a[59C4]	C8219	CAP_402	m42a[65A7]	D7624	DIODE_SCHOT_SOD-323	m42a[59C6]	L5205	IND_0402-LF	m42a[42C3]	
C7601	CAP_603	m42a[59A4]	C8221	CAP_402	m42a[65A7]	D7664	DIODE_SCHOT_SOD-323	m42a[59C3]	L5400	FILTER_4P_SM	m42a[44B5]	
C7602	CAP_402	m42a[59A4]	C8230	CAP_402	m42a[65C6]	D7820	DIODE_SCHOT_SOD-323	m42a[61B4]	L5410	IND_0402-LF	m42a[44C5]	
C7604	CAP_402	m42a[59A2]	C8300	CAP_402	m42a[66C7]	D7921	DIODE_SMB	m42a[62B7]	L5411	IND_0402-LF	m42a[44B5]	
C7605	CAP_402	m42a[59A5]	C8301	CAP_402	m42a[66C7]	D7924	DIODE_SCHOT_SOD-323	m42a[62C6]	L5910	IND_0603	m42a[46A7]	
C7607	CAP_402	m42a[59A3]	C8302	CAP_402	m42a[66C7]	D7961	DIODE_SMB	m42a[62B2]	L6800	IND_0402	m42a[54A5]	
C7608	CAP_402	m42a[59D2]	C8303	CAP_402	m42a[66C4]	D7961	DIODE_SMB	m42a[62B2]	L6801	IND_0402	m42a[54D6]	
C7609	CAP_402	m42a[59D7]	C8304	CAP_402	m42a[66C5]	D7964	DIODE_SCHOT_SOD-323	m42a[62C3]	L7200	IND_0402	m42a[55C7]	
C7621	CAP_402	m42a[59B6]	C8305	CAP_1206-1	m42a[66C4]	D8200	DIODE_SCHOT_3P_A_SC-75	m42a[65C7]	L7210	IND_0402	m42a[55A7]	
C7622	CAP_402	m42a[59C5]	C8306	CAP_1206-1	m42a[66C3]	D8201	DPAK3P_SOT-363	m42a[65D4]	L7220	IND_0402	m42a[55B7]	
C7624	CAP_402	m42a[59C6]	C8307	CAP_1206-1	m42a[66C3]	D8300	DIODE_SCHOT_SOD-123	m42a[66C5]	L7230	IND_0402	m42a[55A7]	
C7625	CAP_402	m42a[59B6]	C8308	CAP_P_CASED2E-SM	m42a[66B4]	D8322	DPAK3P_SOT-363	m42a[66C8 66A5 66A6]	L7300	IND_0402-LF	m42a[56D6]	
C7626	CAP_402	m42a[59B6]	C8309	CAP_P_6_3X5_5SM1	m42a[66B3]	D9500	DIODE_DUAL_6P_SOT-36	m42a[68A7 68B7]	L7301	IND_0402-LF	m42a[56D4]	
C7628	CAP_402	m42a[59B7]	C8310	CAP_P_CASED2E-SM	m42a[66C7]	D27300	SUPPR_TRANSIENT_4P1_0405	m42a[56C6]	L7302	IND_0402	m42a[56D6]	
C7629	CAP_402	m42a[59B7]	C8311	CAP_402	m42a[66C7]	D27301	SUPPR_TRANSIENT_4P1_0405	m42a[56C6]	L7303	IND_0402	m42a[56C6]	
C7630	CAP_402	m42a[59B5]	C8312	CAP_402	m42a[66C5]	D27350	SUPPR_TRANSIENT_4P1_0405	m42a[56A6]	L7304	IND_0402	m42a[56C4]	
C7631	CAP_402	m42a[59C7]	C8313	CAP_402	m42a[66C6]	D27351	SUPPR_TRANSIENT_4P1_0405	m42a[56A6]	L7355	IND_0402	m42a[56B6]	
C7632	CAP_402	m42a[59C2]	C8316	CAP_402	m42a[66B4]	F8200	FUSE_1206	m42a[65D6]	L7356	IND_0402	m42a[56B4]	
C7640	CAP_P_CASED2E-SM	m42a[59D6]	C8317	CAP_402	m42a[66B5]	F8300	FUSE_1206	m42a[66C3]	L7355	IND_0402	m42a[56B6]	
C7641	CAP_603	m42a[59B6]	C8318	CAP_402	m42a[66B4]	F9804	FUSE_SM-LF	m42a[69C5]	L7357	IND_0402	m42a[56A6]	
C7650	CAP_805	m42a[59B7]	C8320	CAP_402	m42a[66B5]	FL4520	FILTER_4P_2012	m42a[39B3]	L7370	IND_0402	m42a[56B2]	
C7651	CAP_805	m42a[59B8]	C8321	CAP_402	m42a[66B5]	FL4521	FILTER_4P_2012	m42a[39B3]	L7371	IND_0402	m42a[56B1]	
C7652	CAP_P_SMC-LF	m42a[59B8]	C8322	CAP_402	m42a[66B4]	FL4590	FUSE_MINISMD	m42a[39D5]	L7372	IND_0402	m42a[56B2]	
C7661	CAP_402	m42a[59B3]	C8323	CAP_402	m42a[66A5]	FL9800	FILTER_IC_SM-220MHZ-LF	m42a[69B5]	L7373	IND_0402	m42a[56B1]	
C7662	CAP_402	m42a[59C4]	C8324	CAP_402	m42a[66A4]	FL9801	FILTER_IC_SM-220MHZ-LF	m42a[69A5]	L7374	IND_0402	m42a[56B2]	
C7664	CAP_402	m42a[59C3]	C8325	CAP_402	m42a[66C7]	FL9802	FILTER_IC_SM-220MHZ-LF	m42a[69A5]	L7390	IND_0402	m42a[56D8]	
C7665	CAP_402	m42a[59B4]	C8326	CAP_402	m42a[66C7]	GV3901	HOLE_VIA	m42a[35C2]	L7400	IND_0402	m42a[57B4]	
C7666	CAP_402	m42a[59B3]	C8327	CAP_402	m42a[66D7]	GV3902	HOLE_VIA	m42a[35C2]	L7500	IND_SM	m42a[58D2]	
C7668	CAP_402	m42a[59B2]	C8328	CAP_402	m42a[66B6]	GV3903	HOLE_VIA	m42a[35C2]	L7501	IND_SM	m42a[58B2]	
C7669	CAP_402	m42a[59B2]	C8340	CAP_402	m42a[66C7]	GV3904	HOLE_VIA	m42a[35C2]	L7620	IND_0402-LF	m42a[59B7]	
C7670	CAP_402	m42a[59B4]	C8341	CAP_402	m42a[66B8]	GV3905	HOLE_VIA	m42a[35B2]	L7820	IND_3P_SM	m42a[61B3]	
C7680	CAP_P_CASED2E-SM	m42a[59D3]	C8370	CAP_402	m42a[66C3]	GV3906	HOLE_VIA	m42a[35B2]	L7920	IND_SM	m42a[62B7]	
C7681	CAP_603	m42a[59D4]	C8371	CAP_402	m42a[66C2]	GV3907	HOLE_VIA	m42a[35B2]	L7960	IND_3P_SM	m42a[62B2]	
C7689	CAP_402	m42a[59B4]	C8372	CAP_402	m42a[66B1]	GV3907	HOLE_VIA	m42a[35B2]	L8090	IND_CDPH4D19F-SM	m42a[63D1]	
C7690	CAP_805	m42a[59B2]	C8375	CAP_402	m42a[66B3]	GV3908	HOLE_VIA	m42a[35B2]	L8201	IND_SM-LF	m42a[65A3]	
C7691	CAP_805	m42a[59B1]	C8381	CAP_603	m42a[66B3]	J1102	CON_F30STSM_5047_SML	m42a[11B2]	L8202	IND_0402-LF	m42a[65A3]	
C7692	CAP_P_SMC-LF	m42a[59B1]	C8381	CAP_603	m42a[66B3]	J2600	CON_F2RT_S2MT_SM_F-R	m42a[26D6]	L8203	IND_0402-LF	m42a[65A3]	
C7700	CAP_603	m42a[60C4]	C9400	CAP_402	m42a[67C3]	J2801	CON_F200RT_DDR2DIMM	m42a[28D6]	L8204	IND_0402-LF	m42a[65A3]	
C7701	CAP_402	m42a[60C3]	C9401	CAP_402	m42a[67C3]	J2801	CON_F200RT_DDR2DIMM	m42a[28D6]	L8205	IND_SM-LF	m42a[65A3]	
C7702	CAP_603	m42a[60C3]	C9403	CAP_402	m42a[67C3]	J2901	CON_F200RT_DDR2DIMM	m42a[29D5]	L8207	IND_0402	m42a[65A7]	
C7703	CAP_603	m42a[60C4]	C9408	CAP_402	m42a[67A3]	J3801	CON_M50ST_D2MT_SM_M-	m42a[34C4]	L8208	IND_0402	m42a[65A7]	
C7704	CAP_402	m42a[60C3]	C9409	CAP_402	m42a[67B2]	J3901	CON_F19ST_S2MT_SM_F-	m42a[35D8]	L8300	IND_3P_SM	m42a[66C4]	
C7705	CAP_603	m42a[60C3]	C9410	CAP_402	m42a[67A3]	J4200	CON_R345_8RT_S2MT_SM	m42a[37C2]	L9400	IND_0402-LF	m42a[67D4]	
C7720	CAP_402	m42a[60B4]	C9411	CAP_402	m42a[67B5]	J4500	CON_F4RT_S2MT_TH_F-R	m42a[39B2]	L9401	IND_0402-LF	m42a[67C4]	
C7721	CAP_603	m42a[60B3]	C9412	CAP_603	m42a[67B5]	J4900	CON_F10ST_D_SMA_F-ST	m42a[40C4]	L9402	IND_0402-LF	m42a[67D4]	
C7750	CAP_402	m42a[60C6]	C9413	CAP_402	m42a[67B6]	J5200	CON_F4RT_USB_S2MT_TH	m42a[42D1]	L9500	IND_0402-LF	m42a[68D5]	
C7800	CAP_603	m42a[61C5]	C9414	CAP_402	m42a[67D5]	J5201	CON_F4RT_USB_S2MT_TH	m42a[42B1]	L9503	IND_0402-LF	m42a[68D8]	
C7801	CAP_603	m42a[61C6]	C9415	CAP_402	m42a[67A3]	J5300	CON_F52RT_D2MT_SM_F-	m42a[43C5]	L9504	IND_0402-LF	m42a[68C8]	
C7802	CAP_603	m42a[61C5]	C9416	CAP_402	m42a[67A4]	J5400	CON_F4ST_S2MT_SM_F-S	m42a[44C4]	L9506	IND_0402-LF	m42a[68D8]	
C7803	CAP_402	m42a[61B2]	C9459	CAP_402	m42a[67C5]	J6000	CON_F30STSM_5047_SML	m42a[47C6]	L9804	FILTER_4P_2012H	m42a[69A2]	
C7804	CAP_402	m42a[61C2]	C9500	CAP_402	m42a[68D5]	J6250	CON_F2ST_S2MT_SM_F-S	m42a[49C6]	L9806	FILTER_4P_2012H	m42a[69B2]	
C7805	CAP_402	m42a[61C2]	C9501	CAP_402	m42a[68D4]	J6251	CON_F2ST_S2MT_SM_F-S	m42a[49A6]	L9807	FILTER_4P_2012H	m42a[69B2]	
C7806	CAP_402	m42a[61B7]	C9502	CAP_402	m42a[68D4]	J6501	CON_F4ST_S2MT_SM_F-S	m42a[51C3				

	8		7		6		5		4		3		2		1	
D	Q7502	TRA_HAT2168H_LFFPAK	m42a[58C3]	R2079	RES_402	m42a[20B7]	R3404	RES_402	m42a[33D1]	R5905	RES_402	m42a[46D4]				
	Q7503	TRA_HAT2165H_LFFPAK	m42a[58B4]	R2085	RES_402	m42a[20C4]	R3405	RES_402	m42a[33C1]	R5906	RES_402	m42a[46D4]				
	Q7504	TRA_HAT2165H_LFFPAK	m42a[58D3]	R2100	RES_402	m42a[21C3]	R3406	RES_402	m42a[33B1]	R5910	RES_603	m42a[46C8]				
	Q7505	TRA_HAT2165H_LFFPAK	m42a[58B3]	R2101	RES_402	m42a[21C4]	R3407	RES_402	m42a[33B1]	R5911	RES_402	m42a[46A6]				
	Q7620	TRA_STL8NH31L_COMBO	m42a[59C7]	R2105	RES_402	m42a[21D6]	R3408	RES_402	m42a[33C1]	R5918	RES_402	m42a[46C5]				
	Q7621	TRA_STL8NH31L_COMBO	m42a[59B7]	R2107	RES_402	m42a[21C2]	R3409	RES_402	m42a[33C1]	R5919	RES_402	m42a[46C5]				
	Q7660	TRA_STL8NH31L_COMBO	m42a[59C3]	R2108	RES_402	m42a[21C2]	R3410	RES_402	m42a[33C1]	R5920	RES_402	m42a[46C5]				
	Q7661	TRA_STL8NH31L_COMBO	m42a[59B3]	R2110	RES_402	m42a[21C2]	R3411	RES_402	m42a[33D4]	R5922	RES_402	m42a[46C5]				
	Q7750	TRA_2N7002DW_SOT-363	m42a[60C6 60C7]	R21194	RES_402	m42a[21D4]	R3412	RES_402	m42a[33D4]	R5923	RES_402	m42a[46C5]				
	Q7820	TRA_IRF7821_SO-8	m42a[61C4]	R2195	RES_402	m42a[21C6]	R3413	RES_402	m42a[33D4]	R5924	RES_402	m42a[46C4]				
	Q7821	TRA_IRF7821_SO-8	m42a[61B4]	R2196	RES_402	m42a[21C6]	R3414	RES_402	m42a[33D4]	R5925	RES_402	m42a[46C5]				
	Q7920	TRA_IRF7821_SO-8	m42a[62C6]	R2197	RES_402	m42a[21C6]	R3415	RES_402	m42a[33D4]	R5926	RES_402	m42a[46C4]				
	Q7921	TRA_IRF7821_SO-8	m42a[62B6]	R2198	RES_402	m42a[21C6]	R3416	RES_402	m42a[33D4]	R5927	RES_402	m42a[46C5]				
	Q7960	TRA_IRF7821_SO-8	m42a[62C3]	R2199	RES_402	m42a[21C3]	R3417	RES_402	m42a[33C7]	R5928	RES_402	m42a[46D4]				
	Q7961	TRA_IRF7821_SO-8	m42a[62B3]	R2200	RES_402	m42a[22D7]	R3418	RES_402	m42a[33B4]	R5929	RES_402	m42a[46C5]				
	Q8000	TRA_FDC638P_SM-LF	m42a[63D4]	R2203	RES_402	m42a[22C2]	R3419	RES_402	m42a[33B4]	R5930	RES_402	m42a[46C5]				
	Q8005	TRA_STL8NH31L_COMBO	m42a[63C4]	R2204	RES_402	m42a[22C2]	R3420	RES_402	m42a[33A4]	R5931	RES_402	m42a[46C4]				
	Q8010	TRA_FDC638P_SM-LF	m42a[63D4]	R2205	RES_402	m42a[22C6]	R3421	RES_402	m42a[33A4]	R5932	RES_402	m42a[46C4]				
	Q8015	TRA_STL8NH31L_COMBO	m42a[63C4]	R2206	RES_402	m42a[22C5]	R3422	RES_402	m42a[33C4]	R5933	RES_402	m42a[46C4]				
	Q8020	TRA_S13447BDV_SOT-6	m42a[63A4]	R2207	RES_402	m42a[22C5]	R3423	RES_402	m42a[33C4]	R5934	RES_402	m42a[46C5]				
	Q8030	TRA_2N7002DW_SOT-363	m42a[63A6 63B6]	R2208	RES_402	m42a[22D5]	R3426	RES_402	m42a[33C4]	R5935	RES_402	m42a[46C4]				
	Q8031	TRA_2N7002DW_SOT-363	m42a[63D6 63A6]	R2211	RES_402	m42a[22B3]	R3427	RES_402	m42a[33C4]	R5936	RES_402	m42a[46C5]				
	Q8059	TRA_2N7002DW_SOT-363	m42a[63C7 63C7]	R2223	RES_402	m42a[22D6]	R3428	RES_402	m42a[33C4]	R5937	RES_402	m42a[46C4]				
	Q8060	TRA_2N7002_SOT23-LF	m42a[63C8]	R2225	RES_402	m42a[22D7]	R3429	RES_402	m42a[33D8]	R5938	RES_402	m42a[46C5]				
	Q8061	TRA_2N7002DW_SOT-363	m42a[63B7 63B7]	R2226	RES_402	m42a[22D5]	R3430	RES_402	m42a[33D7]	R5939	RES_402	m42a[46C4]				
Q8062	TRA_2N7002_SOT23-LF	m42a[63B8]	R2250	RES_402	m42a[22D7]	R3431	RES_402	m42a[33B1]	R5940	RES_402	m42a[46C5]					
Q8063	TRA_2N7002_SOT23-LF	m42a[63B4]	R2251	RES_402	m42a[22D6]	R3432	RES_402	m42a[33D7]	R5941	RES_402	m42a[46C4]					
Q8210	TRA_2N7002DW_SOT-363	m42a[65C6 65C3]	R2255	RES_402	m42a[22D7]	R3433	RES_402	m42a[33B8]	R5942	RES_402	m42a[46C3]					
Q8220	TRA_2N7002DW_SOT-363	m42a[65C7 65C6]	R2299	RES_402	m42a[22B5]	R3434	RES_402	m42a[33D4]	R5943	RES_402	m42a[46B4]					
Q8240	TRA_TP0610_SOT23-3	m42a[65C5]	R2300	RES_402	m42a[23C7]	R3435	RES_402	m42a[33C4]	R5944	RES_402	m42a[46B4]					
Q8250	TRA_S14405DY_SO-8	m42a[66D5]	R2302	RES_402	m42a[23D3]	R3436	RES_402	m42a[33B1]	R5945	RES_402	m42a[46C4]					
Q8301	TRA_HAT2168H_LFFPAK	m42a[66C4]	R2303	RES_402	m42a[23D3]	R3437	RES_402	m42a[33B1]	R5946	RES_402	m42a[46C4]					
Q8302	TRA_HAT2165H_LFFPAK	m42a[66B4]	R2305	RES_402	m42a[23D3]	R3438	RES_402	m42a[33D1]	R5947	RES_402	m42a[46B4]					
Q8320	TRA_S14405DY_SO-8	m42a[66B3]	R2306	RES_402	m42a[23B7]	R3439	RES_402	m42a[33D1]	R5948	RES_402	m42a[46C5]					
Q8321	TRA_S14405DY_SO-8	m42a[66B3]	R2307	RES_402	m42a[23A7]	R3440	RES_402	m42a[33D1]	R5949	RES_402	m42a[46C4]					
Q8322	TRA_2N7002DW_SOT-363	m42a[66A4 66A4]	R2308	RES_402	m42a[23B7]	R3441	RES_402	m42a[33D1]	R5950	RES_402	m42a[46A3]					
Q8324	TRA_2N7002DW_SOT-363	m42a[66A3 66A4]	R2309	RES_402	m42a[23A7]	R3442	RES_402	m42a[33C1]	R5951	RES_402	m42a[46B3]					
Q8340	TRA_REL65203_SM	m42a[66C9]	R2310	RES_402	m42a[23A7]	R3443	RES_402	m42a[33C7]	R5952	RES_402	m42a[46A3]					
Q8350	TRA_2N7002_SOT23-LF	m42a[66A6]	R2311	RES_402	m42a[23A7]	R3451	RES_402	m42a[33B7]	R5953	RES_402	m42a[46D5]					
Q9403	TRA_FDC638P_SM-LF	m42a[67B6]	R2312	RES_402	m42a[23A3]	R3452	RES_402	m42a[33B7]	R5954	RES_402	m42a[46B5]					
Q9404	TRA_2N7002_SOT23-LF	m42a[67B7]	R2313	RES_402	m42a[23A7]	R3453	RES_402	m42a[33B7]	R5955	RES_402	m42a[46B5]					
Q9405	TRA_TP0610_SOT23-3	m42a[67D5]	R2314	RES_402	m42a[23A7]	R3454	RES_402	m42a[33B7]	R5970	RES_402	m42a[46D3]					
Q9406	TRA_2N7002_SOT23-LF	m42a[67D6]	R2315	RES_402	m42a[23A3]	R3463	RES_402	m42a[33D7]	R5971	RES_402	m42a[46D3]					
Q9801	TRA_2N7002DW_SOT-363	m42a[69D6 69D6]	R2316	RES_402	m42a[23D7]	R3465	RES_402	m42a[33C4]	R5972	RES_402	m42a[46C7]					
R0610	RES_402	m42a[6A7]	R2317	RES_402	m42a[23D7]	R3466	RES_402	m42a[33A7]	R5973	RES_402	m42a[46C5]					
R0611	RES_402	m42a[6A8]	R2318	RES_402	m42a[23D7]	R3467	RES_402	m42a[33A7]	R5976	RES_402	m42a[46D1]					
R0612	RES_402	m42a[6A8]	R2319	RES_402	m42a[23D2]	R3468	RES_402	m42a[33C7]	R5977	RES_402	m42a[46C1]					
R0621	RES_402	m42a[6A7]	R2320	RES_402	m42a[23D7]	R3469	RES_402	m42a[33C7]	R5980	RES_402	m42a[46D5]					
R0702	RES_402	m42a[7D5]	R2323	RES_402	m42a[23D5]	R3470	RES_402	m42a[33C7]	R5981	RES_402	m42a[46D5]					
R0703	RES_402	m42a[7C5]	R2326	RES_402	m42a[23D6]	R3471	RES_402	m42a[33B7]	R5982	RES_402	m42a[46D5]					
R0704	RES_402	m42a[7C5]	R2327	RES_402	m42a[23D6]	R3472	RES_402	m42a[33B7]	R5983	RES_402	m42a[46C5]					
R0705	RES_402	m42a[7B4]	R2343	RES_402	m42a[23D1]	R3473	RES_402	m42a[33B7]	R5984	RES_402	m42a[46C5]					
R0706	RES_402	m42a[7B4]	R2388	RES_402	m42a[23B2]	R3474	RES_402	m42a[33B8]	R5985	RES_402	m42a[46C5]					
R0707	RES_402	m42a[7A4]	R2389	RES_402	m42a[23A4]	R3475	RES_402	m42a[33B7]	R5986	RES_402	m42a[46C5]					
R0712	RES_402	m42a[7A4]	R2390	RES_402	m42a[23B3]	R3476	RES_402	m42a[33A7]	R5987	RES_402	m42a[46C5]					
R0716	RES_402	m42a[7B2]	R2395	RES_402	m42a[23D7]	R3477	RES_402	m42a[33B4]	R5988	RES_402	m42a[46B5]					
R0717	RES_402	m42a[7B2]	R2396	RES_402	m42a[23D6]	R3478	RES_402	m42a[33B4]	R5989	RES_402	m42a[46D5]					
R0718	RES_402	m42a[7B2]	R2397	RES_402	m42a[23D6]	R3480	RES_402	m42a[33C7]	R5990	RES_402	m42a[46B2]					
R0719	RES_402	m42a[7B2]	R2398	RES_402	m42a[23D8]	R3481	RES_402	m42a[33B1]	R5991	RES_402	m42a[46B2]					
R0720	RES_402	m42a[7B7]	R2399	RES_402	m42a[23C1]	R3482	RES_402	m42a[33B1]	R5992	RES_402	m42a[46B2]					
R0721	RES_402	m42a[7B7]	R2500	RES_603	m42a[25A8]	R3490	RES_402	m42a[33A4]	R5993	RES_402	m42a[46B2]					
R0722	RES_402	m42a[7A7]	R2501	RES_402	m42a[25C8]	R3824	RES_402	m42a[34C4]	R5994	RES_402	m42a[46D5]					
R0730	RES_402	m42a[7A4]	R2502	RES_402	m42a[25D8]	R3825	RES_402	m42a[34C5]	R5995	RES_402	m42a[46D5]					
R0802	RES_402	m42a[8B6]	R2600	RES_402	m42a[26D4]	R3851	RES_402	m42a[34C4]	R5996	RES_402	m42a[46B4]					
R0803	RES_402	m42a[8A7]	R2606	RES_402	m42a[26D5]	R3853	RES_402	m42a[34C3]	R5997	RES_402	m42a[46B4]					
R0921	RES_402	m42a[9D2]	R2607	RES_402	m42a[26D5]	R3858	RES_402	m42a[34B5]	R5998	RES_402	m42a[46C4]					
R0922	RES_402	m42a[9D2]	R2609	RES_402	m42a[26C7]	R3859	RES_402	m42a[34B4]	R5999	RES_402	m42a[46C4]					
R0923	RES_402	m42a[9C2]	R2610	RES_402	m42a[26C7]	R3865	RES_402	m42a[34C6]	R6100	RES_402	m42a[48D3]					
R0924	RES_402	m42a[9C2]	R2611	RES_402	m42a[26B5]	R3876	RES_402	m42a[34C7]	R6102	RES_402	m42a[48C2]					
R0925	RES_402	m42a[9C2]	R2612	RES_402	m42a[26A5]	R3877	RES_402	m42a[34C6]	R6103	RES_402	m42a[48C3]					
R0926	RES_402	m42a[9C2]	R2622	RES_402	m42a[26A5]	R3900	RES_402	m42a[35D3]	R6105	RES_402	m42a[48D4]					

	8	7	6	5	4	3	2	1				
D	R7210	RES_402	m42a[55A7]	R7903	RES_402	m42a[62A3]	R9509	RES_402	m42a[68C2]	XW7300	SHORT_SM	m42a[56C4]
	R7260	RES_402	m42a[55D2]	R7904	RES_402	m42a[62A3]	R9510	RES_402	m42a[68C2]	XW7301	SHORT_SM	m42a[56B4]
	R7261	RES_402	m42a[55C2]	R7905	RES_402	m42a[62A6]	R9537	RES_402	m42a[68D1]	XW7302	SHORT_SM	m42a[56C2]
	R7270	RES_402	m42a[55C2]	R7906	RES_402	m42a[62A3]	R9538	RES_402	m42a[68D1]	XW7303	SHORT_SM	m42a[56C2]
	R7271	RES_402	m42a[55C2]	R7907	RES_402	m42a[62A3]	R9539	RES_402	m42a[68C1]	XW7304	SHORT_SM	m42a[56B2]
	R7280	RES_402	m42a[55B2]	R7921	RES_402	m42a[62C7]	R9540	RES_402	m42a[68C1]	XW7305	SHORT_SM	m42a[56B7]
	R7281	RES_402	m42a[55B2]	R7924	RES_402	m42a[62C6]	R9821	RES_402	m42a[69D7]	XW7400	SHORT_SM	m42a[57A7]
	R7300	RES_402	m42a[56C4]	R7925	RES_402	m42a[62B6]	R9822	RES_402	m42a[69D6]	XW7500	SHORT_SM	m42a[58A6]
	R7301	RES_402	m42a[56C4]	R7926	RES_402	m42a[62C7]	R9850	RES_402	m42a[69B8]	XW7600	SHORT_SM	m42a[59A5]
	R7320	RES_402	m42a[56B5]	R7927	RES_402	m42a[62B8]	R9851	RES_402	m42a[69B8]	XW7620	JUMPER_OPEN-SAWTOOTH	m42a[59B8]
R7321	RES_402	m42a[56D7]	R7928	RES_402	m42a[62B8]	R9852	RES_402	m42a[69A8]	XW7660	JUMPER_OPEN-SAWTOOTH	m42a[59B1]	
R7322	RES_402	m42a[56B7]	R7929	RES_402	m42a[62C7]	R9853	RES_402	m42a[69A8]	XW7800	SHORT_SM	m42a[61B5]	
R7349	RES_402	m42a[56B7]	R7930	RES_402	m42a[62C5]	R9854	RES_402	m42a[69A8]	XW7900	SHORT_SM	m42a[62A5]	
R7350	RES_402	m42a[56A4]	R7961	RES_402	m42a[62C2]	R9855	RES_402	m42a[69A8]	XW7920	JUMPER_OPEN-SAWTOOTH	m42a[62B8]	
R7351	RES_402	m42a[56A4]	R7964	RES_402	m42a[62C3]	R9856	RES_402	m42a[69B6]	XW8101	SHORT_SM	m42a[64B2]	
R7380	RES_402	m42a[56C2]	R7965	RES_402	m42a[62B3]	R9859	RES_402	m42a[69A6]	XW8102	SHORT_SM	m42a[64B2]	
R7382	RES_402	m42a[56B2]	R7966	RES_402	m42a[62C2]	R9860	RES_402	m42a[69C3]	XW8300	SHORT_SM	m42a[66B4]	
R7391	RES_402	m42a[56C7]	R7967	RES_402	m42a[62B2]	R9861	RES_402	m42a[69C3]	Y2600	CRYSTAL_4PIN_SM-LF	m42a[26C7]	
R7401	RES_402	m42a[57D8]	R7968	RES_402	m42a[62D8]	R9862	RES_402	m42a[69C5]	Y3301	CRYSTAL_5X3.2-SM	m42a[32C7]	
R7402	RES_402	m42a[57D7]	R7969	RES_402	m42a[62C2]	R9863	RES_402	m42a[69C5]	Y4101	CRYSTAL_4PIN_SM-3.2X	m42a[36B6]	
R7403	RES_402	m42a[57C7]	R7970	RES_402	m42a[62C4]	R9864	RES_402	m42a[69A6]	2.5MM			
R7404	RES_402	m42a[57C4]	R7970	RES_402	m42a[62A6]	R9868	RES_402	m42a[69C8]	Y4403	CRYSTAL_4PIN_SM-3.2X	m42a[38C2]	
R7405	RES_402	m42a[57D5]	R7991	RES_402	m42a[62A6]	R9869	RES_402	m42a[69C8]	2.5MM			
R7406	RES_402	m42a[57D6]	R7992	RES_603	m42a[62A7]	R9870	RES_402	m42a[69C1]	Y5920	CRYSTAL_5X3.2-SM	m42a[46C7]	
R7411	RES_402	m42a[57C8]	R8000	RES_402	m42a[63D5]	R9871	RES_402	m42a[69C1]	Y6795	CRYSTAL_4PIN_SM-LF	m42a[53B6]	
R7412	RES_402	m42a[57B7]	R8005	RES_402	m42a[63C5]	RP2300	RPAK4P_SM-LF	m42a[23D5]	Z0601	MTGHOLE	m42a[68B]	
R7413	RES_402	m42a[57C6]	R8010	RES_402	m42a[63C5]	RP2600	RPAK4P_SM-LF	m42a[26D2]	Z0602	MTGHOLE	m42a[68B]	
R7414	RES_402	m42a[57C4]	R8015	RES_402	m42a[63A5]	RP2601	RPAK4P_SM-LF	m42a[26D2]	Z0603	PCB_STANDOFF	m42a[68B]	
R7415	RES_402	m42a[57C5]	R8025	RES_402	m42a[63A5]	RP2602	RPAK4P_SM-LF	m42a[26C2]	Z0604	PCB_STANDOFF	m42a[68B]	
R7430	RES_603	m42a[57C3]	R8030	RES_402	m42a[63B6]	RP3000	RPAK4P_SM-LF	m42a[30B4 30C4 30D4 30D4]	Z0605	PCB_STANDOFF	m42a[68B]	
R7431	RES_603	m42a[57B3]	R8031	RES_402	m42a[63B6]	RP3001	RPAK4P_SM-LF	m42a[30C4 30A4 30A4 30D4]	Z0606	MTGHOLE	m42a[68B]	
R7432	RES_402	m42a[57B3]	R8032	RES_402	m42a[63D6]	RP3002	RPAK4P_SM-LF	m42a[30A4 30A4 30A4 30D4]	Z0607	MTGHOLE	m42a[68B]	
R7433	RES_402	m42a[57A3]	R8033	RES_402	m42a[63D6]	RP3003	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30D4]	Z0608	MTGHOLE	m42a[68B]	
R7434	RES_402	m42a[57C2]	R8050	RES_402	m42a[63A6]	RP3004	RPAK4P_SM-LF	m42a[30C4 30C4 30D4]	Z0609	MTGHOLE	m42a[68B]	
R7435	RES_402	m42a[57C2]	R8056	RES_402	m42a[63C8]	RP3005	RPAK4P_SM-LF	m42a[30B4 30A4 30A4 30D4]	Z0610	MTGHOLE	m42a[68B]	
R7436	RES_402	m42a[57B2]	R8057	RES_402	m42a[63C8]	RP3006	RPAK4P_SM-LF	m42a[30B4 30B4 30B4 30D4]	Z0611	MTGHOLE	m42a[68B]	
R7437	RES_402	m42a[57B2]	R8058	RES_402	m42a[63B8]	RP3007	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30C4]	Z0612	PCB_STANDOFF	m42a[68B]	
R7438	RES_402	m42a[57C2]	R8059	RES_402	m42a[63B8]	RP3008	RPAK4P_SM-LF	m42a[30C4 30C4 30C4 30C4]	Z0613	PCB_STANDOFF	m42a[68B]	
R7439	RES_402	m42a[57B2]	R8061	RES_402	m42a[63B1]	RP3009	RPAK4P_SM-LF	m42a[30B4 30B4 30C4 30C4]	Z0621	PCB_STANDOFF	m42a[68B]	
R7440	RES_402	m42a[57A5]	R8062	RES_402	m42a[63B1]	RP3010	RPAK4P_SM-LF	m42a[30B4 30B4 30B4 30B4]	ZS0620	SPRING_CLIP_LP_RMI_C	m42a[6D7]	
R7450	RES_402	m42a[57A7]	R8063	RES_402	m42a[63A1]	RP3011	RPAK4P_SM-LF	m42a[30B4 30A4 30B4 30B4]	LIP-SM-M42			
R7451	RES_402	m42a[57A7]	R8064	RES_402	m42a[63A1]	T4201	XFR_1000BT_82400275_	m42a[37C6]	ZS0621	CLIP_SM	m42a[6D6]	
R7452	RES_402	m42a[57A7]	R8065	RES_402	m42a[63B2]	XFR-SM						
R7453	RES_402	m42a[57A7]	R8091	RES_402	m42a[63D1]	T4202	XFR_1000BT_82400275_	m42a[37B6]				
R7454	RES_402	m42a[57A7]	R8092	RES_402	m42a[63C1]	XFR-SM						
R7460	RES_402	m42a[57C6]	R8200	RES_402	m42a[65B7]	U0700	CPU_YONAH_BGA	m42a[7C3 7D7]				
R7461	RES_402	m42a[57C7]	R8201	RES_402	m42a[65C5]	U0700	CPU_YONAH_BGA	m42a[8D8 8D4]				
R7500	RES_402	m42a[58C2]	R8202	RES_402	m42a[65C2]	U1001	ACT7461_MSOP	m42a[10C5]				
R7501	RES_402	m42a[58C2]	R8203	RES_402	m42a[65C6]	U1200	NB_945GM_BGA	m42a[12D5]				
R7502	RES_805	m42a[58B3]	R8204	RES_402	m42a[65C6]	U1200	NB_945GM_BGA	m42a[13D4]				
R7503	RES_805	m42a[58D3]	R8205	RES_805	m42a[65D4]	U1200	NB_945GM_BGA	m42a[14D5]				
R7504	RES_402	m42a[58C1]	R8206	RES_402	m42a[65C4]	U1200	NB_945GM_BGA	m42a[15D3 15D7]				
R7505	RES_402	m42a[58B2]	R8207	RES_402	m42a[65C4]	U1200	NB_945GM_BGA	m42a[16D2 16C8]				
R7506	RES_402	m42a[58C7]	R8208	RES_402	m42a[65C4]	U1200	NB_945GM_BGA	m42a[17D5]				
R7507	RES_402	m42a[58B1]	R8209	RES_402	m42a[65C4]	U1200	NB_945GM_BGA	m42a[18D4 18D7]				
R7508	RES_402	m42a[58B8]	R8210	RES_402	m42a[65C4]	U1900	LREG_TPS73115_SOT23-5	m42a[19D6]				
R7509	RES_402	m42a[58B8]	R8211	RES_402	m42a[65C6]	U1901	MM157_SOT23-5-LF	m42a[19C4]				
R7510	RES_402	m42a[58B6]	R8213	RES_402	m42a[65C2]	U2100	SB_ICH7M_BGA	m42a[21D6]				
R7511	RES_402	m42a[58B8]	R8214	RES_402	m42a[65C2]	U2100	SB_ICH7M_BGA	m42a[22B7 22D3]				
R7512	RES_402	m42a[58D7]	R8231	RES_402	m42a[65C5]	U2100	SB_ICH7M_BGA	m42a[23D4]				
R7513	RES_402	m42a[58B7]	R8232	RES_402	m42a[65C6]	U2100	SB_ICH7M_BGA	m42a[24D4 24D7]				
R7514	RES_402	m42a[58B8]	R8233	RES_402	m42a[65C5]	U2601	MC74VHC1G08_SC70	m42a[26A5]				
R7515	RES_402	m42a[58B5]	R8296	RES_402	m42a[65B7]	U2603	MC74VHC1G08_SC70-5	m42a[26A7]				
R7516	RES_402	m42a[58B4]	R8297	RES_402	m42a[65C3]	U2680	MC74VHC1G08_SC70	m42a[26B3]				
R7517	RES_402	m42a[58B5]	R8298	RES_402	m42a[65C8]	U3100	LREG_BD3533FVM_MSOP-8	m42a[31C4]				
R7518	RES_402	m42a[58B5]	R8299	RES_402	m42a[65C7]	U3301	CLK_SVN_SLG8B1P436_QP	m42a[32C5]				
R7519	RES_402	m42a[58C7]	R8300	RES_402	m42a[66C6]	U4101	88E8053_QFN	m42a[36D6]				
R7520	RES_402	m42a[58D7]	R8301	RES_402	m42a[66C7]	U4102	EEPROM_M24C08_S08	m42a[36A3]				
R7521	RES_402	m42a[58D8]	R8302	RES_402	m42a[66C5]	U4400	FW32306_BGA_BGA	m42a[38C5]				
R7522	RES_402	m42a[58A5]	R8303	RES_402	m42a[66C5]	U5100	CY8C24794_MLF	m42a[41C5]				
R7523	RES_402	m42a[58A6]	R8304	RES_805	m42a[66B2]	U5200	SMI_TPS2042B_MSOP	m42a[42C7]				
R7524	RES_402	m42a[58D5]	R8305	RES_402	m42a[66C5]	U5800	SMC_HBS2116_BGA	m42a[45A8 45C3 45C7 45D7]				
R7525	RES_402	m42a[58C5]	R8306	RES_402	m42a[66C7]	U5900	VDET_RNSVD_SOT23-5	m42a[46D7]				
R7526	THERMISTER_402	m42a[58C7]	R8308	RES_0612	m42a[66C3]	U5910	OBC_CLIP_SG-3040LC-SM	m42a[46A7]				
R7527	RES_402	m42a[58C8]	R8309	RES_402	m42a[66B6]	U5977	COMPPARATOR_LMC7211_S	m42a[46C2]				
R7530	RES_402	m42a[58B4]	R8310	RES_402	m42a[66C5]	M-LF						
R7531	THERMISTER_0603-LF	m42a[58B4]	R8311	RES_402	m42a[66B7]	U6100	OPAMP_LMV2011_SOT23-5	m42a[48C3]				
R7543	RES_402	m42a[58B2]	R8312	RES_402	m42a[66C7]	U6200	MAX6695_UMAX	m42a[49D4]				
R7545	RES_402	m42a[58C7]	R8320	RES_2525	m42a[66B3]	U6250	MAX6695_UMAX	m42a[49B4]				
R7600	RES_402	m42a[59C5]	R8322	RES_402	m42a[66A3]	U6301	FLASH_SST25VF016B_SO	m42a[50D3]				
R7603	RES_402	m42a[59A3]	R8323	RES_402	m42a[66A3]	I_SOI						
R7604	RES_402	m42a[59A3]	R8324	RES_402	m42a[66A4]	U6620	K3MS2_QFN	m42a[52C5]				
R7606	RES_402	m42a[59A3]	R8325	RES_402	m42a[66A5]	U6650	L193L02AL_LGA	m42a[52B5]				
R7607	RES_402	m42a[59A3]	R8330	RES_402	m42a[66B4]	U6700	TPM_TSSOP	m42a[53C5]				
R7621	RES_402	m42a[59C7]	R8331	RES_402	m42a[66A4]	U6800	AUDIO_STAC92204XR_LQ	m42a[54D5]				
R7624	RES_402	m42a[59C5]	R8340	RES_402	m42a[66C8]	FP						
R7625	RES_402	m42a[59B6]	R8341	RES_402	m42a[66B8]	U7210	MAX9705_TDFN1	m42a[55C5]			</	