1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
A		0000713283	K24 MLB PVT RELEASE	5/6/09	?

K24 MLB SCHEMATIC

PVT RELEASE

5/6/2009

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

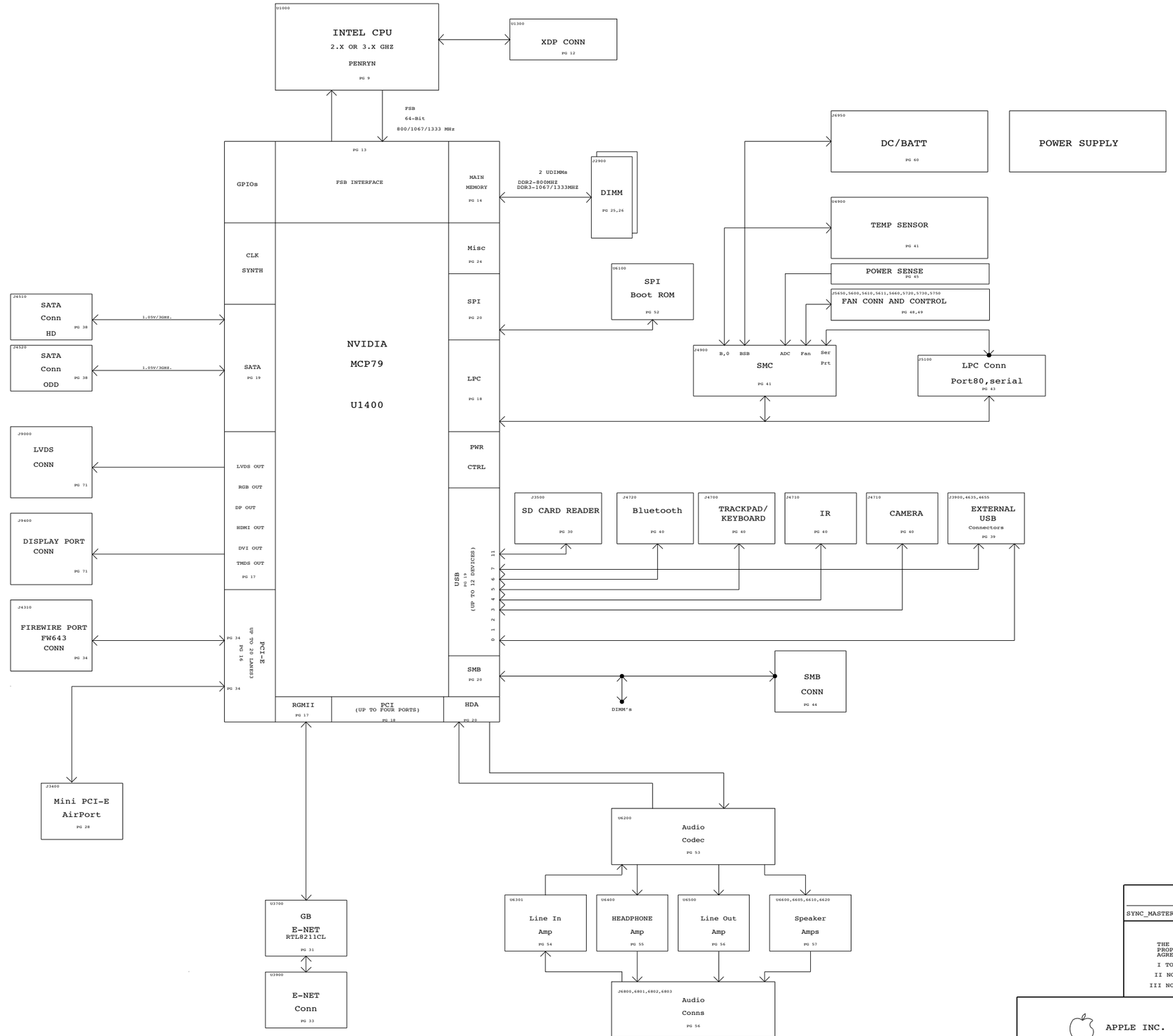
SIZE D

APPLE INC.

TITLE: SCHEM,MLB,K24

DRAWING NUMBER 051-7898 REV. A

SHT 1 OF 81



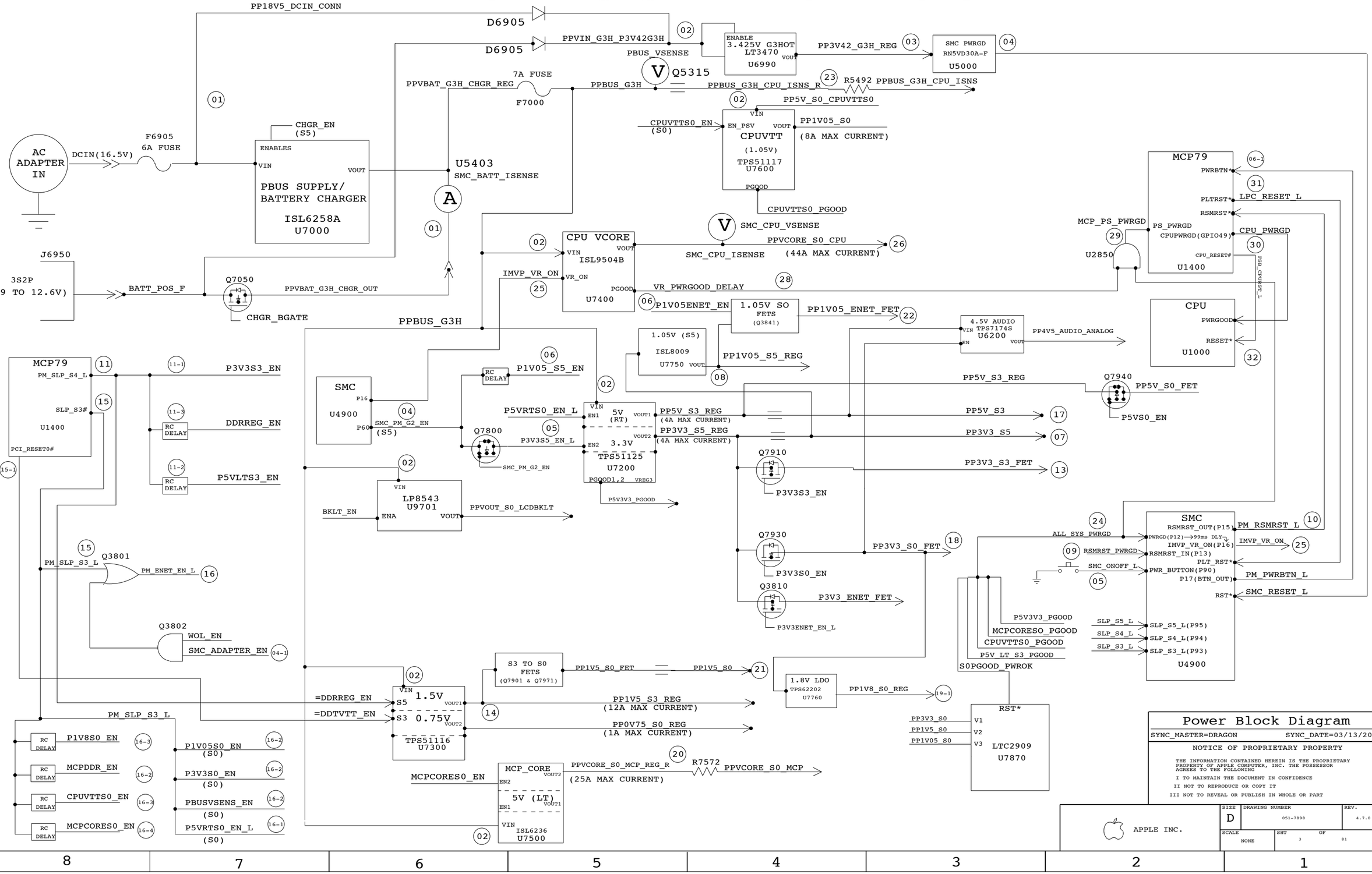
System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 2 OF 81	

K24 POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=DRAGON SYNC_DATE=03/13/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 3 OF 81	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL
085-0741	K24 MLB DEVELOPMENT BOM	K24_DEVEL_PVT

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PVT,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SLG8E,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SLGE2,PRQ,2.26,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SLGFG,PRQ,2.53,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SLGLA,PRQ,2.66,25W,1066,E0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,GMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGRM,EFI BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGRM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
516-0213	516-0201		ALL	MOLEX AS ALTERNATE
51680709	51680706		ALL	MOLEX AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

K24 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

BOM Configuration

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 4 OF 81	

Revision History

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

Revision History

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 5 OF 81	

Functional Test Points

Fan Connectors

E14	TRUE	PP5V_S0	(NEED 3 TP) 6D3 7D5
E15	TRUE	FAN_RT_PWM	47B4
E16	TRUE	FAN_RT_TACH	47C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

E20	TRUE	BI_MIC_LO	56C2 57B1
E21	TRUE	BI_MIC_HI	56C2 57B1
E22	TRUE	BI_MIC_SHIELD	56C2 57B1

SPEAKER FUNC_TEST

E29	TRUE	SPKRAMP_L_N_OUT	55A2 56B2
E27	TRUE	SPKRAMP_L_P_OUT	55B2 56B2
E28	TRUE	SPKRAMP_R_N_OUT	55C2 56A2
E23	TRUE	SPKRAMP_R_P_OUT	55C2 56B2
E24	TRUE	SPKRAMP_SUB_N_OUT	55B2 56B2
E25	TRUE	SPKRAMP_SUB_P_OUT	55C2 56B2

THERMAL FUNC_TEST

E26	TRUE	MCPTHMSNS_D2_P	46B5 80D3
E26	TRUE	MCPTHMSNS_D2_N	46B5 80D3

LVDS FUNC_TEST

E250	TRUE	PP3V3_LCDVDD_SW_F	6C3 68C2
E250	TRUE	PP3V3_S0_LCD_F	68C3
E260	TRUE	PPVOUT_S0_LCDBKLT	6C3 68B2 71C1
E240	TRUE	LVDS_IG_DDC_CLK	17B3 68C5
E260	TRUE	LVDS_IG_DDC_DATA	17A3 68C5
E260	TRUE	LVDS_IG_A_DATA_N<0>	17B3 68C2 75B3
E260	TRUE	LVDS_IG_A_DATA_P<0>	17B3 68C2 75B3
E250	TRUE	LVDS_IG_A_DATA_N<1>	17B3 68C2 75B3
E255	TRUE	LVDS_IG_A_DATA_P<1>	17B3 68C2 75B3
E250	TRUE	LVDS_IG_A_DATA_N<2>	17B3 68C2 75B3
E250	TRUE	LVDS_IG_A_DATA_P<2>	17B3 68C2 75B3
E250	TRUE	LVDS_IG_A_CLK_F_N	68C2 75B3
E250	TRUE	LVDS_IG_A_CLK_F_P	68C2 75B3
E260	TRUE	LED_RETURN_1	68B3 71B1
E310	TRUE	LED_RETURN_2	68B3 71B1
E240	TRUE	LED_RETURN_3	68B3 71B1
E240	TRUE	LED_RETURN_4	68B3 71B1
E240	TRUE	LED_RETURN_5	68B3 71B1
E240	TRUE	LED_RETURN_6	68B3 71A1
E305	TRUE	TP_BKL_SYNC	68C2

(NEED TO ADD 5 GND TP)

SATA ODD CONN

E260	TRUE	PP5V_SW_ODD	(NEED 4 TP) 6C3 37D3
E260	TRUE	SMC_ODD_DETECT	37C7 40B8
E260	TRUE	SATA_ODD_D2R_C_P	37C6 75A3
E260	TRUE	SATA_ODD_D2R_C_N	37C6 75A3
E260	TRUE	SATA_ODD_R2D_P	37C6 75A3
E260	TRUE	SATA_ODD_R2D_N	6A7 37C6 75A3

(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

E310	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 6C3 37B6
E310	TRUE	SATA_HDD_R2D_P	37A5 75A3
E315	TRUE	SATA_HDD_R2D_N	37A5 75A3
E310	TRUE	SATA_HDD_D2R_C_P	37B5 75A3
E310	TRUE	SATA_HDD_D2R_C_N	37B5 75A3
E107	TRUE	SYS_LED_ANODE_R	37A7
E100	TRUE	IR_RX_OUT	37A7 39D4
E314	TRUE	PP5V_S3_IR_R	37A7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

E322	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
E324	TRUE	SMBUS_SMC_BSA_SDA	43C5 79D3
E320	TRUE	SYS_DETECT_L	58A8
E105	TRUE	BATT_POS_F	(NEED 3 TP) 58A7 58B8 59A3

(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

E324	TRUE	PP3V42_G3H	(NEED 3 TP) 6B5 6D3 7D1
E322	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
E324	TRUE	SMBUS_SMC_BSA_SCL	6A7 43C5 79D3
E325	TRUE	SMC_BIL_BUTTON_L	40C5 58C4
E100	TRUE	SMC_LID_R	58C2

(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

E300	TRUE	PP5V_S3_BTCAMERA_F	29C7
E301	TRUE	PCIE_MINI_D2R_P	16B6 29C7 75D3
E302	TRUE	PCIE_MINI_D2R_N	16B6 29C7 75D3
E303	TRUE	PCIE_MINI_R2D_P	29C7 75D3
E299	TRUE	PCIE_MINI_R2D_N	29C7 75D3
E298	TRUE	PCIE_CLK100M_MINI_CONN_P	29C7 75D3
E298	TRUE	PCIE_CLK100M_MINI_CONN_N	29C7 75D3
E297	TRUE	USB_CAMERA_CONN_P	29B7 76C3
E296	TRUE	USB_CAMERA_CONN_N	29B7 76C3
E288	TRUE	PP5V_WLAN	(NEED 2 TP) 6C3 29C5
E292	TRUE	PCIE_WAKE_L	16B6 29C7
E294	TRUE	SMBUS_SMC_A_S3_SCL	6C5 43D2 79D3
E295	TRUE	SMBUS_SMC_A_S3_SDA	6C5 43D2 79D3
E291	TRUE	CONN_USB2_BT_P	29B7 76C3
E290	TRUE	CONN_USB2_BT_N	29B7 76B3
E274	TRUE	MINI_CLKREQ_O_L	29C7
E288	TRUE	MINI_RESET_CONN_L	29A7

(NEED TO ADD 6 GND TP)

IPD_FLEX_CONN

E390	TRUE	PP3V3_S3_LDO	6C3 49B4 49C3
E390	TRUE	PP18V5_S3	6C3 49C1 49D3
E372	TRUE	Z2_CS_L	48C8 49C3
E370	TRUE	Z2_DEBUG3	48C8 49C3
E374	TRUE	Z2_MOSI	48C8 49C3
E374	TRUE	Z2_MISO	48C8 49C3
E360	TRUE	Z2_SCLK	48C8 49C3
E360	TRUE	Z2_BOOST_EN	49C3 49C5
E362	TRUE	Z2_HOST_INTN	48D8 49C3
E362	TRUE	Z2_CLKIN	48C6 49C3
E360	TRUE	Z2_KEY_ACT_L	48C8 49C1
E362	TRUE	Z2_RESET	48C8 49C1
E364	TRUE	PSOC_MISO	48C8 49C1
E362	TRUE	PSOC_MOSI	48C8 49C1
E360	TRUE	PSOC_SCLK	48C8 49C1
E350	TRUE	SMBUS_SMC_A_S3_SDA	6D5 43D2 79D3
E350	TRUE	SMBUS_SMC_A_S3_SCL	6D5 43D2 79D3
E370	TRUE	PSOC_F_CS_L	48C8 49C1
E370	TRUE	PICKB_L	48D8 49C1

KEYBOARD CONN

E354	TRUE	PP3V3_S3	6D3 7D3
E355	TRUE	PP3V42_G3H	6A7 6D3 7D1
E344	TRUE	WS_KBD1	48C6 48D2
E345	TRUE	WS_KBD2	48C6 48D2
E346	TRUE	WS_KBD3	48C6 48D2
E347	TRUE	WS_KBD4	48C6 48D2
E348	TRUE	WS_KBD5	48C6 48D2
E349	TRUE	WS_KBD6	48C6 48D2
E350	TRUE	WS_KBD7	48C6 48D2
E350	TRUE	WS_KBD8	48C6 48D2
E351	TRUE	WS_KBD9	48C6 48D2
E352	TRUE	WS_KBD10	48C6 48D2
E328	TRUE	WS_KBD11	48C6 48D2
E329	TRUE	WS_KBD12	48C6 48D2
E329	TRUE	WS_KBD13	48C6 48D2
E329	TRUE	WS_KBD14	48C2 48C6
E343	TRUE	WS_KBD15_CAP	48C2
E343	TRUE	WS_KBD16_NUM	48C2
E343	TRUE	WS_KBD17	48C2
E339	TRUE	WS_KBD18	48C2 48D6
E340	TRUE	WS_KBD19	48C2 48D7
E338	TRUE	WS_KBD20	48C2 48D7
E338	TRUE	WS_KBD21	48C2 48D7
E337	TRUE	WS_KBD22	48C2 48D7
E337	TRUE	WS_KBD23	48C2 48D7
E335	TRUE	WS_KBD_ONOFF_L	48C2
E334	TRUE	WS_LEFT_SHIFT_KBD	48B3 48B5 48C2
E337	TRUE	WS_LEFT_OPTION_KBD	48B3 48B5 48C2
E330	TRUE	WS_CONTROL_KBD	48B3 48B0 48C2
E331			

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

E356	TRUE	KBDLED_ANODE	(NEED 2 TP) 49A4
E396	TRUE	SMC_KDBLED_PRESENT_L	49A4 49A6

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

E210	TRUE	PPVCORE_S0_CPU	7D7
E210	TRUE	PPVCORE_S0_MCP	7C7
E210	TRUE	PP0V75_S0	7C7
E200	TRUE	PP1V05_S0	7D7
E201	TRUE	PP1V5_S0	7C6
E202	TRUE	PP1V8_S0	7B6
E230	TRUE	PP5V_S0	6D7 7D5
E240	TRUE	PP3V3_S0	7D5
E220	TRUE	PP1V5_S3	7D3
E220	TRUE	PP3V3_S3	6B5 7D3
E220	TRUE	PP5V_S3	7C3
E270	TRUE	PP1V1R1V05_S5	7B3
E230	TRUE	PP3V3_S5	7B3
E272	TRUE	PP3V42_G3H	6A7 6B5 7D1
E272	TRUE	PPBUS_G3H	7C1
E240	TRUE	PP3V3_ENET_PHY	7B5
E270	TRUE	PP1V2R1V05_ENET	7B5
E272	TRUE	PP3V3_G3_RTC	20C8 21A5 24D4
E392	TRUE	PP5V_WLAN	6D5 29C5
E392	TRUE	PP5V_SW_ODD	6B7 37D3
E392	TRUE	PP5V_S0_HDD_FLT	6B7 37B6
E390	TRUE	PP3V3_S5_AVREF_SMC	40D4 41C6
E390	TRUE	PP18V5_S3	6C5 49C1 49D3
E390	TRUE	PP3V3_S3_LDO	6C5 49B4 49C3
E390	TRUE	PP3V3_LCDVDD_SW_F	6C7 68C2
E380	TRUE	PPVOUT_S0_LCDBKLT	6C7 68B2 71C1
E380	TRUE	PP4V5_AUDIO_ANALOG	52A5 52D2 52D7
E382	TRUE	SMC_PM_G2_EN	40D5 60C5 66D8
E381	TRUE	PM_SLP_S4_L	20C3 40C5 41A2 66C8
E380	TRUE	PM_SLP_S3_L	20C3 32B7 35A5 40C5 66D5 70D8

(NEED TO ADD 4 GND TP)

DC POWER CONN

E390	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 58D6
E396	TRUE	ADAPTER_SENSE	58D7

(NEED TO ADD 4 GND TP)

FUNC TEST

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 6 OF 81	

"S0,S0M" RAILS

62D1 =PPVCORE_S0_CPU_REG
(CPU VCORE PWR)
PPVCORE_S0_CPU 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 10B5 10D6 11D6
=PPVCORE_S0_CPU_VSENSE 44D8

64C7 =PPCPUVTT_S0_REG
PP1V05_S0 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 9D5 10C6 11B6 12D6
=PP1V05_S0_MCP_FSB 13A2 13B7 21D3 22C8
=PP1V05_S0_SMC_LS
=PP1V05_S0_MCP_PEX_DVDD 7A8 22D8
=PP1V05_S0_MCP_AVDD_UF 22D4
=PP1V05_S0_MCP_SATA_DVDD 7A8 22D6
=PP1V05_S0_MCP_HDMI_VDD 17A6 23D7
=PP1V05_S0_VMON 66A8
=PP1V05_S0_MCP_PLL_UF_R 65B3
=PP1V05_FW_P1V05FWFET 35C6
=PP1V05_FWPWRCTL 35B4

63C7 63C1 63B8 =PPMCPCORE_S0_REG
(MCP VCORE AFTER SENSE RES)
PPVCORE_S0_MCP 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 21D5 22D8
=PPVCORE_S0_MCP_VSENSE 44D8

61C8 =PP0V75_S0_REG
PP0V75_S0 6D3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP 67B3
=PP0V75_S0_MEM_VTT_A 26A4
=PP0V75_S0_MEM_VTT_B 27A4

67D1 =PP1V5_S0_FET
PP1V5_S0 6D3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 10B6 11B6
=PP1V5_S0_VMON 66A8
=PP1V8R1V5_S0_MCP_MEM 15C3 15C7 22C8
=PP1V5_S0_MEM_MCP 27B3
=PP1V5_S0_MCP_PLL_VLDO 65B6

65C5 =PP1V8_S0_REG
PP1V8_S0 6D3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 17B6 23D7
=PP1V8_S0_AUDIO 52D7

65B1 22C4 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

67B6 =PP5V_S0_FET
PP5V_S0 6D3 6D7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_HDD 37B3
=PP5V_S0_LPCPLUS 42D5
=PP5V_S0_FAN_RT 47C5
=PP5V_S0_CPU_IMVP 62D8
=PP5V_S0_KBDLED 49A5
=PP5V_S0_DP_AUX_MUX 69B6
=PP5V_S0_CPUVTTS0 64C8
=PP5V_S0_BKL 71D4
=PP5V_S0_MCPREG 63D4
=PP5V_S0_VMON 66B5

67C6 =PP3V3_S0_FET
PP3V3_S0 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 12D6
=PP3V3_S0_MCP 20C2 21B3 22B8
=PP3V3_S0_MCP_DAC_UF 23D4
=PP3V3_S0_MCP_VPLL_UF 23C7
=PP3V3_S0_ODD 37C7 37D6
=PP3V3_S0_SMBUS_SMC_0_S0 43D5
=PP3V3_S0_SMBUS_SMC_B_S0 43C3
=PP3V3_S0_SMBUS_MCP_0 43D8
=PP3V3_S0_FAN_RT 47C5
=PP3V3_S0_AUDIO 52A8 52D2 56D8 57B8 57D3
=PP3V3_S0_IMVP 62D8
=PP3V3_S0_LCD 68C5
=PP3V3_S0_MCP_GPIO 17C1 18D1 20A4
=PP3V3_S0_MCP_PLL_UF 22B6
=PP3V3R1V5_S0_MCP_HDA 20D3 20D8 22A8
=PP3V3_S0_SMC 41A1 41D3
=PP3V3_S0_MCPTHMSNS 46B6
=PP3V3_S0_CPUTHMSNS 46D6
=PP3V3_S0_DPCONN 70B8 70C8
=PPSPD_S0_MEM_A 26A8
=PPSPD_S0_MEM_B 27A8
=PP3V3_S0_PWRCTL 66A5
=PP3V3_S0_VMON 66A8
=PP3V3_S0_CPUVTTISNS 45C7
=PP3V3_S0_TPAD 49A6
=PP3V3_S0_SMBUS_MCP_1 43C8
=PP3V3_S0_P1V8S0 65D8
=PP3V3_S0_BKL_VDDIO 71C7
=PP3V3_S0_MCPDDRISNS 45D8
=PP3V3_S0_MCP_PLL_VLDO 65C6
=PP3V3_S0_P3V3FWFET 35D6
=PP3V3_S0_FWPWRCTL 35B1 35D2

"ENET" RAILS

32D2 =PP3V3_ENET_FET
PP3V3_ENET_PHY 6C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 17D3 17D7 22A5 22B6
=PP3V3_ENET_PHY 31D7

32B2 =PP1V05_ENET_FET
PP1V2R1V05_ENET 6C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_PLL_MAC 22A8
=PP1V05_ENET_MCP_RMGT 17D3 22D6
=PP1V05_ENET_PHY 31D2

PEX & SATA AVDD/DVDD aliases

22D1 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
22D8 7D7 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)
22D2 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
127 mA (A01)
22D6 7D7 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)

=PP1V05_S0_MCP_PEX_AVDD0 16B3
=PP1V05_S0_MCP_PEX_AVDD1 16A3
206 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 16B6
=PP1V05_S0_MCP_PEX_DVDD1 16A6
57 mA (A01)
=PP1V05_S0_MCP_SATA_AVDD0 19B6
=PP1V05_S0_MCP_SATA_AVDD1 19B6
127 mA (A01)
=PP1V05_S0_MCP_SATA_DVDD0 19B6
=PP1V05_S0_MCP_SATA_DVDD1 19B6
43 mA (A01)

"S3" RAILS

61C1 =PP1V5_S3_REG
PP1V5_S3 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3_P1V5S0FET 67D3
=PP1V5_S3_MEM_A 26D7
=PP1V5_S3_MEM_B 27D7
=PP1V5_S3_MEMRESET 28C6
=PP1V5_S3_HDD 37B8

67D6 =PP3V3_S3_FET
PP3V3_S3 6B5 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 43D3
=PP3V3_S3_PDCISENS 61B3
=PP3V3_S3_SMBUS_SMC_MGMT 43B5
=PP3V3_S3_VREFMRGN 25D8
=PP3V3_S3_WLAN 29A6
=PP3V3_S3_MCP_GPIO 20A3
=PP3V3_S3_TPAD 48A6 48B5 48C5 48D2
=PP3V3_S3_SMS 50B7
=PP3V3_S3_CARDREADER 30D7

60B8 =PP5V_S3_REG
PP5V_S3 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_EXTUSB 38C7
=PP5V_S3_IR 37A8 39D7
=PP5V_S3_BTCAMERA 29C3
=PP5V_S3_VTTCLAMP 67A3
=PP5V_S3_MCPDDRFET 67D4
=PP5V_S3_SYSLED 41B8
=PP5V_S3_TPAD 49B6 49D7
=PP5V_S3_WLAN 29C1
=PP5V_S3_1V5S30V75S0 61C5
=PP5V_S3_AUDIO 52A8 52D2 54D5 56B6
=PP5V_S3_AUDIO_AMP 55B7 55C7 55D7
=PP5V_S3_P5VS0FET 67B8
=PP5V_S3_ODD 37D5

61D8 25D3 =PPVTT_S3_DDR_BUF
PPVTT_S3_DDR_BUF
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

"S5" RAILS

65A5 =PP1V05_S5_REG
PP1V1R1V05_S5 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC 21A3 22D8
=PP1V05_ENET_P1V05ENETFET 32C4

60B1 =PP3V3_S5_REG
PP3V3_S5 6D3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 17C7 19C1
=PP3V3_S5_ROM 42B5 42C7 51C6
=PP3V3_S5_LCD 68C8
=PP3V3_S5_MCP 21B3 22B8
=PP3V3_S5_MCPPWRGD 24B8
=PP3V3_S5_PWRCTL 66B3
=PP3V3_S5_P1V05ENETFET 32C5
=PP3V3_S5_P3V3S3FET 67D8
=PP3V3_S5_P3V3S0FET 67C8
=PP3V3_S5_P1V05S5 65B8
=PP3V3_S5_MEMRESET 28C4
=PP3V3_S5_P3V3ENETFET 32D5
=PP3V3_S5_DP_PORT_PWR 70D8
=PP3V3_FW_LATEVG 36A7
=PP3V3_FW_LATEVG_ACTIVE 35A8
=PP3V3_S5_P1V05FWFET 35C7

"G3H" RAILS

58B4 =PP3V42_G3H_REG
PP3V42_G3H 6A7 6B5 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 41C8
=PP3V42_G3H_SMBUS_SMC_BSA 43C5
=PP3V42_G3H_PWRCTL 66B3 66C8 66D8
=PP3V42_G3H_CHGR 59A8 59C6 59D5
=PP3V42_G3H_SMCUSBMUX 38B8
=PP3V42_G3H_TPAD 48B5 48C2 48C3 48C5
=PP3V42_G3H_BATT 58C2 58C4
=PP3V3_S5_SMC 40D4 41C1 41C3 41C7 41D8
=PP3V3_S5_LPCPLUS 42C7 42C8 42D5
=PP3V42_G3H_RTC_D 24D8
=PP3V42_G3H_BMON_ISNS 45B8
=PP3V42_G3H_ONEWIRE 58D2
=PP3V42_G3H_AUDIO 56B6

58D1 58C8 =PP18V5_DCIN_CONN
PP18V5_G3H 6D3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PP18V5_G3H_CHGR 59D8

59C1 =PPBUS_G3H
PPBUS_G3H 6C3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT 72D8
=PPVIN_S0_MCPCORE 63D5
=PPVIN_S5_1V5S30V75S0 61C2
=PPVIN_S5_3V3S5 60C3
=PPVIN_S3_5VS3 60C6 60C7
=PPBUS_G3HRS5 44B8
=PPBUS_S5_FWPWRSW 35B7
=PPCPUVCORE_VTT_ISNS_R 45B8
(BEFORE HIGH SIDE SENSING RES.)

45B7 =PPCPUVCORE_VTT_ISNS
(AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
PPBUS_G3H_CPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 64C6
=PPVIN_S5_CPU_IMVP 62C3 62D4 62D8

"FIREWIRE" RAILS

35D4 =PP3V3_FW_FET
PP3V3_FW 36D5
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_FWPHY 36B6 35B8 34D8 34D2
=PP3V3_S0_P1V05FWFET 35C7

35B1 =PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVP_FW_PORT1 36C3
=PPVP_FW_PHY_CPS_FET 36C6

35C5 =PP1V0_FW_FET
PP1V05_FW 34D8
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V0_FW_FWPHY 34D8 35D3

Power Aliases

SYNC_MASTER=BEN

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HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

Z0901
STDOFF-4.5OD.98H-1.1-3.48-TH
ABOVE CPU

Z0903
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW MCP

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

FAN STANDOFF

Z0905
STDOFF-4.5OD.98H-1.1-3.48-TH
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5
OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5
OMIT Z0909 3R2P5
OMIT Z0910 3R2P5
OMIT Z0911 3R2P5
OMIT Z0912 3R2P5

PCI-E ALIASES

UNUSED GPU LANES

16D6 16C6 =PEG_D2R_N<15:0> — NC_PEG_D2R_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
16D6 16C6 =PEG_D2R_P<15:0> — NC_PEG_D2R_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
16D3 16C3 =PEG_R2D_C_N<15:0> — NC_PEG_R2D_C_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
16D3 16C3 =PEG_R2D_C_P<15:0> — NC_PEG_R2D_C_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
16C6 PEG_PRSNT_L — TP_PEG_PRSNT_L MAKE_BASE=TRUE
16C3 PEG_CLK100M_P — TP_PEG_CLK100M_P MAKE_BASE=TRUE
16C3 PEG_CLK100M_N — TP_PEG_CLK100M_N MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

16B6 PCIE_EXCARD_D2R_P — TP_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE
16B6 PCIE_EXCARD_D2R_N — TP_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE
16B3 PCIE_EXCARD_R2D_C_P — TP_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE
16B3 PCIE_EXCARD_R2D_C_N — TP_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE
16C6 PCIE_EXCARD_PRSNT_L — TP_PCIE_EXCARD_PRSNT_L MAKE_BASE=TRUE
16C6 EXCARD_CLKREQ_L — TP_EXCARD_CLKREQ_L MAKE_BASE=TRUE
16C3 PCIE_CLK100M_EXCARD_P — TP_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE
16C3 PCIE_CLK100M_EXCARD_N — TP_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE

FIREWIRE PRESENT SIGNALS

35D3 16C6 PCIE_FW_PRSNT_L — R0950 0 5% 1/16W MF-LF 402 NOSTUFF

USB ALIASES

UNUSED USB PORTS

19C3 USB_EXTC_P — TP_USB_EXTC_P MAKE_BASE=TRUE
19C3 USB_EXTC_N — TP_USB_EXTC_N MAKE_BASE=TRUE
19D3 USB_EXTD_P — TP_USB_EXTD_P MAKE_BASE=TRUE
19D3 USB_EXTD_N — TP_USB_EXTD_N MAKE_BASE=TRUE
19C3 USB_EXCARD_P — TP_USB_EXCARD_P MAKE_BASE=TRUE
19C3 USB_EXCARD_N — TP_USB_EXCARD_N MAKE_BASE=TRUE
19D3 USB_MINI_P — TP_USB_MINI_P MAKE_BASE=TRUE
19D3 USB_MINI_N — TP_USB_MINI_N MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

17C6 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET NO_TEST=TRUE MAKE_BASE=TRUE
17C6 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF NO_TEST=TRUE MAKE_BASE=TRUE
17C6 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN NO_TEST=TRUE MAKE_BASE=TRUE
17C6 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT NO_TEST=TRUE MAKE_BASE=TRUE
17C3 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR NO_TEST=TRUE MAKE_BASE=TRUE
17C3 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y NO_TEST=TRUE MAKE_BASE=TRUE
17C3 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB NO_TEST=TRUE MAKE_BASE=TRUE
17C3 CRT_IG_HSYNC — NC_CRT_IG_HSYNC NO_TEST=TRUE MAKE_BASE=TRUE
17C3 CRT_IG_VSYNC — NC_CRT_IG_VSYNC NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

17B3 LVDS_IG_A_DATA_P<3> — NC_LVDS_IG_A_DATA_P3 NO_TEST=TRUE MAKE_BASE=TRUE
17B3 LVDS_IG_A_DATA_N<3> — NC_LVDS_IG_A_DATA_N3 NO_TEST=TRUE MAKE_BASE=TRUE
17B3 LVDS_IG_B_CLK_P — NC_LVDS_IG_B_CLK_P NO_TEST=TRUE MAKE_BASE=TRUE
17B3 LVDS_IG_B_CLK_N — NC_LVDS_IG_B_CLK_N NO_TEST=TRUE MAKE_BASE=TRUE
17B3 LVDS_IG_B_DATA_P<3:0> — NC_LVDS_IG_B_DATA_P<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
17B3 LVDS_IG_B_DATA_N<3:0> — NC_LVDS_IG_B_DATA_N<3:0> NO_TEST=TRUE MAKE_BASE=TRUE

MISC MCP79 ALIASES

13B6 CPU_PECI_MCP — TP_CPU_PECI_MCP MAKE_BASE=TRUE
16B6 GMUX_JTAG_TCK_L — TP_GMUX_JTAG_TCK_L MAKE_BASE=TRUE
16B6 GMUX_JTAG_TDO — TP_GMUX_JTAG_TDO MAKE_BASE=TRUE
18D4 GMUX_JTAG_TDI — TP_GMUX_JTAG_TDI MAKE_BASE=TRUE
18D4 GMUX_JTAG_TMS — TP_GMUX_JTAG_TMS MAKE_BASE=TRUE

LAN ALIASES

17D6 =MCP_MII_RXER — MCP_MII_PD MAKE_BASE=TRUE
17D6 =MCP_MII_COL —
17D6 =MCP_MII_CRS —
R0930 47K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

17B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 MAKE_BASE=TRUE
R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

26D5 MEM_A_A<15> — TP_MEM_A_A15 MAKE_BASE=TRUE
27D5 MEM_B_A<15> — TP_MEM_B_A15 MAKE_BASE=TRUE

ETHERNET ALIASES

32C5 =P3V3ENET_EN — PM_SLP_RMGT_L 20C3 MAKE_BASE=TRUE
32B5 =P1V05ENET_EN —
31C2 =PP3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
31C2 =RTL8211_REGOUT — NC_RTL8211_REGOUT MAKE_BASE=TRUE
31C6 =RTL8211_ENSWREG — MAKE_BASE=TRUE
31B6 TP_RTL8211_CLK125 —
R0931 22 5% 1/16W MF-LF 402

FW ALIASES

18B7 FW_PME_L — FW_PLUG_DET_L 35B1 35D7 MAKE_BASE=TRUE
35C8 34B2 =FW_PME_L — FW643_WAKE_L MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

73C3 9B4 CPU_BSEL<0:2> IN — =MCP_BSEL<0:2> OUT 13A7 MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0908 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT
ZS0909 1.4DIA-SHORT-EMI-MLB-M97-M98 SM OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN,SHORT,EMI,MLB,K19/K24	ZS0900,ZS0901,ZS0902,ZS0903,ZS0908,ZS0909	CRITICAL	

EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM
ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

SIGNAL ALIAS

SYNC_MASTER=M97_MLB

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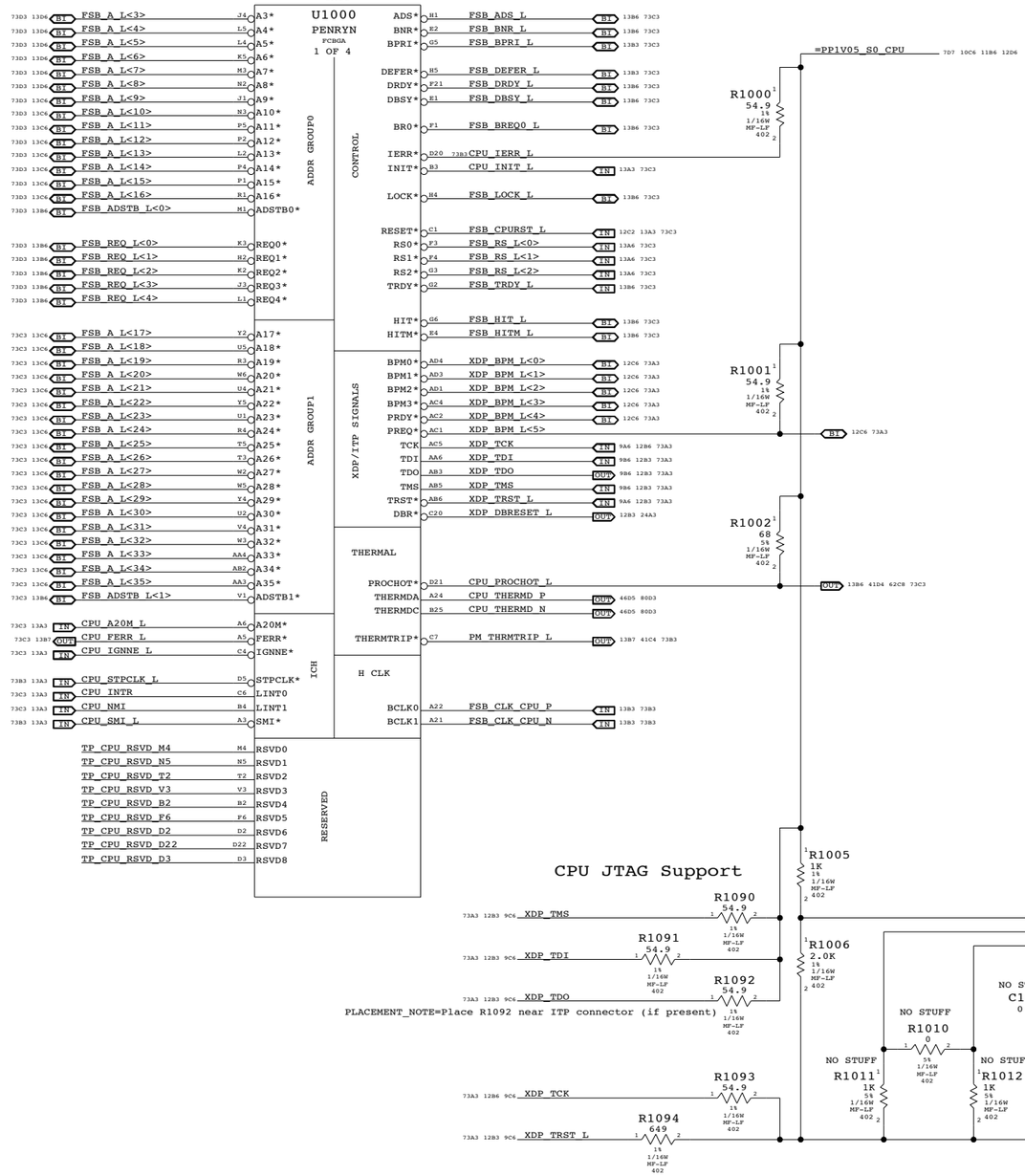

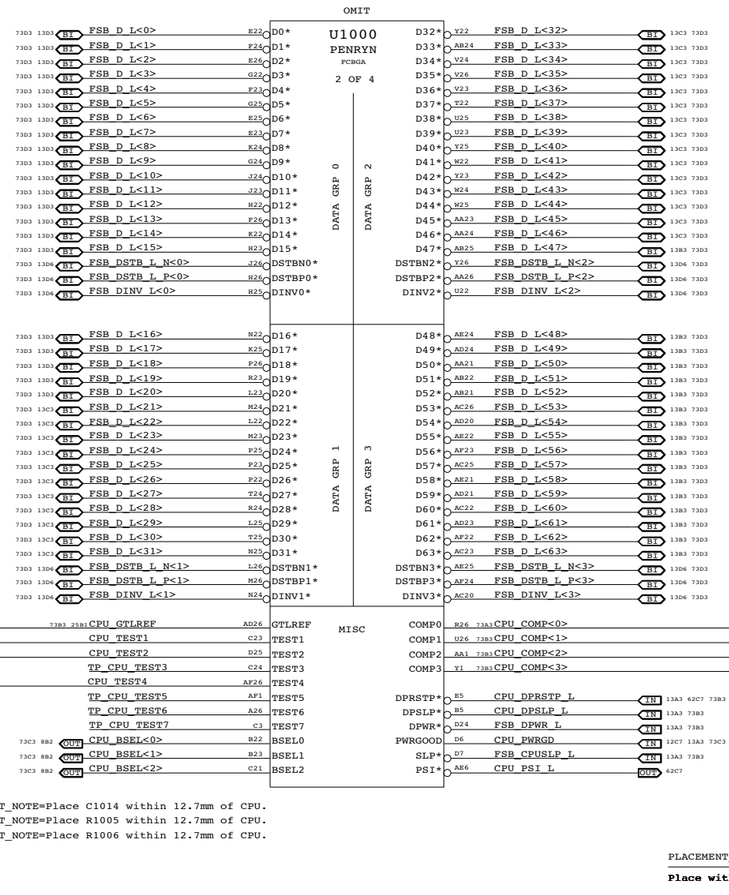

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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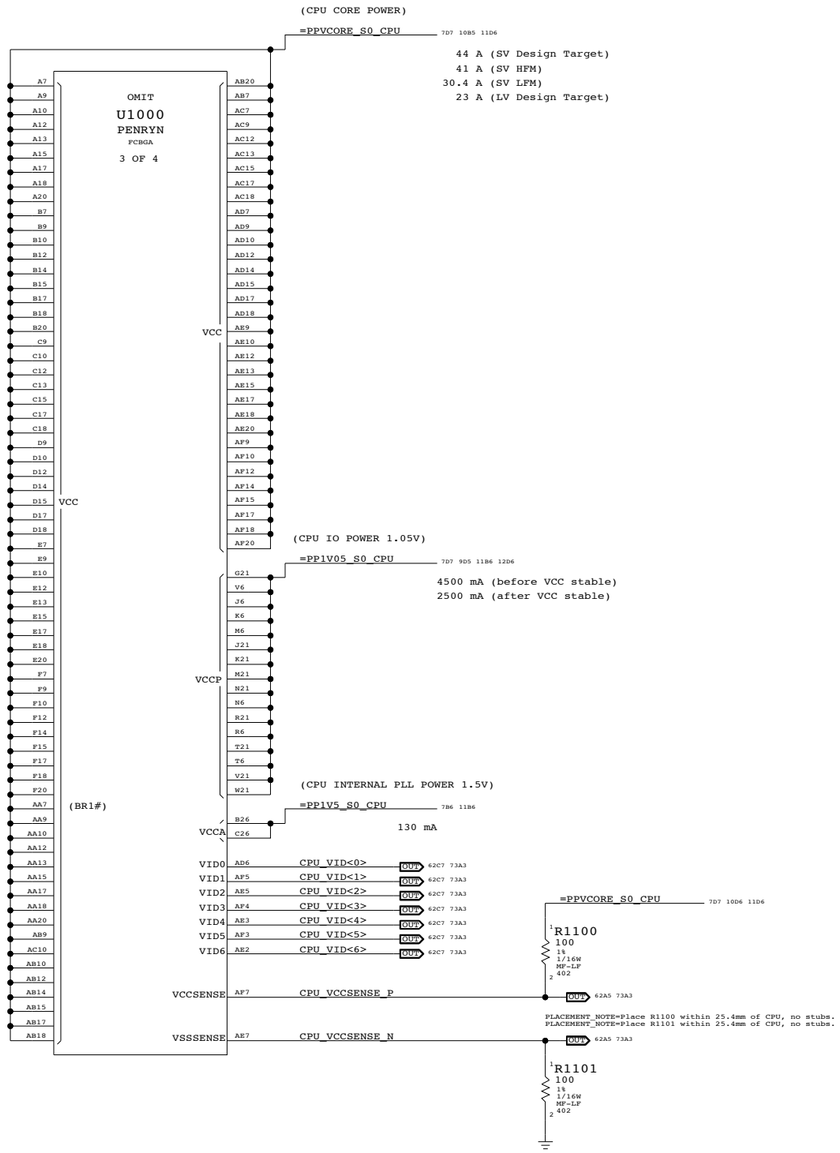
SCALE: NONE	SHT 9 OF 81	



SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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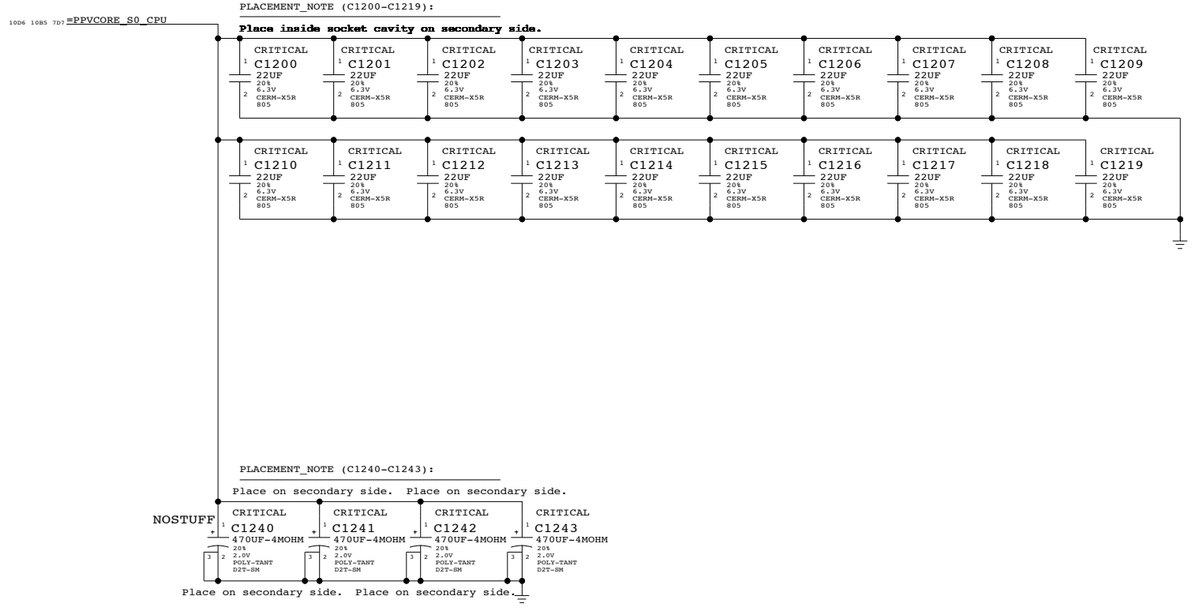
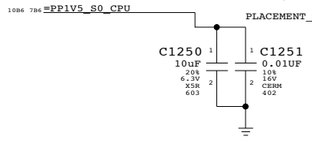
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



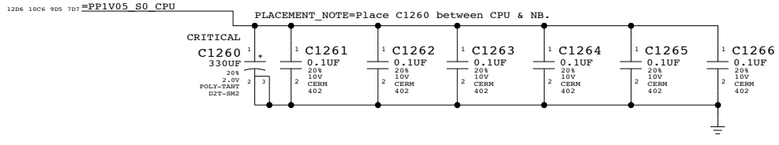
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

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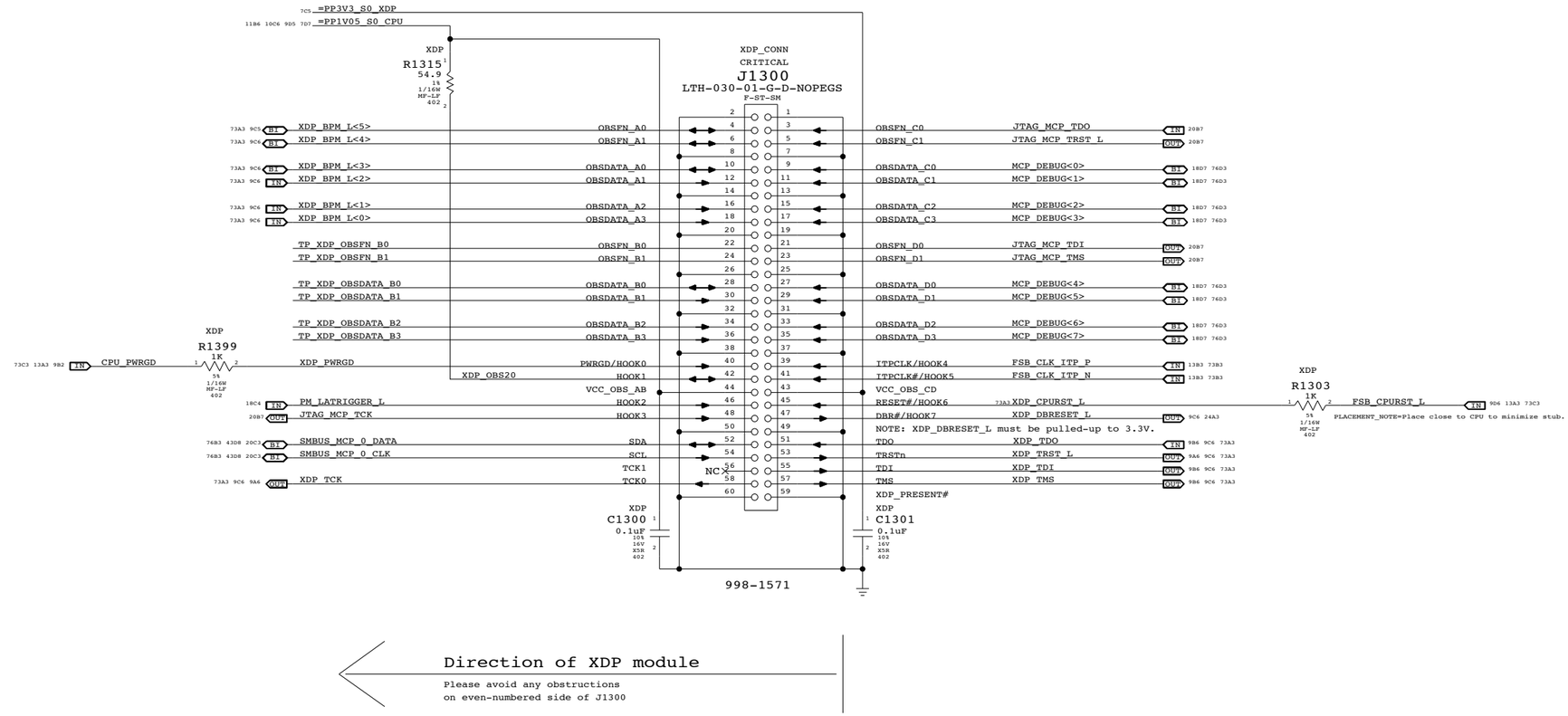
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port(MiniXDP)

SYNC_MASTER=K19_MLB SYNC_DATE=11/07/2008

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SCALE: NONE	SHT 12 OF 81	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

73D3 9C4	BI	FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#			
73D3 9C4	BI	FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#			
73D3 9C4	BI	FSB_DINV_L<0>	V41	CPU_DBI0#			
73D3 9B4	BI	FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#			
73D3 9B4	BI	FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#			
73D3 9B4	BI	FSB_DINV_L<1>	V35	CPU_DBI1#			
73D3 9C2	BI	FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#			
73D3 9C2	BI	FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#			
73D3 9C2	BI	FSB_DINV_L<2>	N35	CPU_DBI2#			
73D3 9B2	BI	FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#			
73D3 9B2	BI	FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#			
73D3 9B2	BI	FSB_DINV_L<3>	J41	CPU_DBI3#			
73D3 9D8	BI	FSB_A_L<3>	AC34	CPU_A3#			
73D3 9D8	BI	FSB_A_L<4>	AE38	CPU_A4#			
73D3 9D8	BI	FSB_A_L<5>	AE34	CPU_A5#			
73D3 9D8	BI	FSB_A_L<6>	AC37	CPU_A6#			
73D3 9D8	BI	FSB_A_L<7>	AE37	CPU_A7#			
73D3 9D8	BI	FSB_A_L<8>	AE35	CPU_A8#			
73D3 9D8	BI	FSB_A_L<9>	AB35	CPU_A9#			
73D3 9D8	BI	FSB_A_L<10>	AF35	CPU_A10#			
73D3 9D8	BI	FSB_A_L<11>	AG35	CPU_A11#			
73D3 9D8	BI	FSB_A_L<12>	AG39	CPU_A12#			
73D3 9D8	BI	FSB_A_L<13>	AE33	CPU_A13#			
73D3 9D8	BI	FSB_A_L<14>	AG37	CPU_A14#			
73D3 9D8	BI	FSB_A_L<15>	AG38	CPU_A15#			
73D3 9D8	BI	FSB_A_L<16>	AG34	CPU_A16#			
73C3 9C8	BI	FSB_A_L<17>	AH38	CPU_A17#			
73C3 9C8	BI	FSB_A_L<18>	AL39	CPU_A18#			
73C3 9C8	BI	FSB_A_L<19>	AG33	CPU_A19#			
73C3 9C8	BI	FSB_A_L<20>	AL33	CPU_A20#			
73C3 9C8	BI	FSB_A_L<21>	AJ33	CPU_A21#			
73C3 9C8	BI	FSB_A_L<22>	AN36	CPU_A22#			
73C3 9C8	BI	FSB_A_L<23>	AJ35	CPU_A23#			
73C3 9C8	BI	FSB_A_L<24>	AJ37	CPU_A24#			
73C3 9C8	BI	FSB_A_L<25>	AJ36	CPU_A25#			
73C3 9C8	BI	FSB_A_L<26>	AJ38	CPU_A26#			
73C3 9C8	BI	FSB_A_L<27>	AL37	CPU_A27#			
73C3 9C8	BI	FSB_A_L<28>	AL34	CPU_A28#			
73C3 9C8	BI	FSB_A_L<29>	AN37	CPU_A29#			
73C3 9C8	BI	FSB_A_L<30>	AJ34	CPU_A30#			
73C3 9C8	BI	FSB_A_L<31>	AL38	CPU_A31#			
73C3 9C8	BI	FSB_A_L<32>	AL35	CPU_A32#			
73C3 9C8	BI	FSB_A_L<33>	AN34	CPU_A33#			
73C3 9C8	BI	FSB_A_L<34>	AR39	CPU_A34#			
73C3 9C8	BI	FSB_A_L<35>	AN35	CPU_A35#			
73D3 9D8	BI	FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#			
73C3 9C8	BI	FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#			
73D3 9D8	BI	FSB_REQ_L<0>	AC38	CPU_REQ0#			
73D3 9D8	BI	FSB_REQ_L<1>	AA33	CPU_REQ1#			
73D3 9D8	BI	FSB_REQ_L<2>	AC39	CPU_REQ2#			
73D3 9D8	BI	FSB_REQ_L<3>	AC33	CPU_REQ3#			
73D3 9D8	BI	FSB_REQ_L<4>	AC35	CPU_REQ4#			
73C3 9D6	BI	FSB_ADS_L	AD42	CPU_ADS#			
73C3 9D6	BI	FSB_BNR_L	AD43	CPU_BNR#			
73C3 9D6	BI	FSB_BREQ0_L	AE40	CPU_BR0#			
73C3		FSB_BREQ1_L	AL32	CPU_BR1#			
73C3 9D6	BI	FSB_DBSY_L	AD39	CPU_DBSY#			
73C3 9D6	BI	FSB_DRDY_L	AD41	CPU_DRDY#			
73C3 9D6	BI	FSB_HIT_L	AB42	CPU_HIT#			
73C3 9D6	BI	FSB_HITM_L	AD40	CPU_HITM#			
73C3 9D6	IN	FSB_LOCK_L	AC43	CPU_LOCK#			
73C3 9D6	OUT	FSB_TRDY_L	AE41	CPU_TRDY#			
8C4	OUT	CPU_PECI_MCP	E41	CPU_PECI			
73C3 62C8 41D4 9C5	OUT	CPU_PROCHOT_L	AJ41	CPU_PROCHOT#			
			AG43	CPU_THERMTRIP#			
			AH40	CPU_FERR#			
8B1	IN	=MCP_BSEL<2>	(MCP_BSEL<2>)	F42	CPU_BSEL2		
8B1	IN	=MCP_BSEL<1>	(MCP_BSEL<1>)	D42	CPU_BSEL1		
8B1	IN	=MCP_BSEL<0>	(MCP_BSEL<0>)	F41	CPU_BSEL0		
73C3 9D6	OUT	FSB_RS_L<0>	AC41	CPU_RS0#			
73C3 9D6	OUT	FSB_RS_L<1>	AB41	CPU_RS1#			
73C3 9D6	OUT	FSB_RS_L<2>	AC42	CPU_RS2#			

CPU_D0#	Y43	FSB_D_L<0>	BI	9C4 73D3
CPU_D1#	W42	FSB_D_L<1>	BI	9C4 73D3
CPU_D2#	Y40	FSB_D_L<2>	BI	9C4 73D3
CPU_D3#	W41	FSB_D_L<3>	BI	9C4 73D3
CPU_D4#	Y39	FSB_D_L<4>	BI	9C4 73D3
CPU_D5#	V42	FSB_D_L<5>	BI	9C4 73D3
CPU_D6#	Y41	FSB_D_L<6>	BI	9C4 73D3
CPU_D7#	Y42	FSB_D_L<7>	BI	9C4 73D3
CPU_D8#	P42	FSB_D_L<8>	BI	9C4 73D3
CPU_D9#	V41	FSB_D_L<9>	BI	9C4 73D3
CPU_D10#	R42	FSB_D_L<10>	BI	9C4 73D3
CPU_D11#	T39	FSB_D_L<11>	BI	9C4 73D3
CPU_D12#	T42	FSB_D_L<12>	BI	9C4 73D3
CPU_D13#	T41	FSB_D_L<13>	BI	9C4 73D3
CPU_D14#	R41	FSB_D_L<14>	BI	9C4 73D3
CPU_D15#	T43	FSB_D_L<15>	BI	9C4 73D3
CPU_D16#	W35	FSB_D_L<16>	BI	9C4 73D3
CPU_D17#	AA37	FSB_D_L<17>	BI	9C4 73D3
CPU_D18#	W33	FSB_D_L<18>	BI	9C4 73D3
CPU_D19#	W34	FSB_D_L<19>	BI	9C4 73D3
CPU_D20#	AA36	FSB_D_L<20>	BI	9B4 73D3
CPU_D21#	AA34	FSB_D_L<21>	BI	9B4 73D3
CPU_D22#	AA38	FSB_D_L<22>	BI	9B4 73D3
CPU_D23#	AA35	FSB_D_L<23>	BI	9B4 73D3
CPU_D24#	U38	FSB_D_L<24>	BI	9B4 73D3
CPU_D25#	U36	FSB_D_L<25>	BI	9B4 73D3
CPU_D26#	U35	FSB_D_L<26>	BI	9B4 73D3
CPU_D27#	U33	FSB_D_L<27>	BI	9B4 73D3
CPU_D28#	U34	FSB_D_L<28>	BI	9B4 73D3
CPU_D29#	M38	FSB_D_L<29>	BI	9B4 73D3
CPU_D30#	R33	FSB_D_L<30>	BI	9B4 73D3
CPU_D31#	U37	FSB_D_L<31>	BI	9B4 73D3
CPU_D32#	N34	FSB_D_L<32>	BI	9C2 73D3
CPU_D33#	N33	FSB_D_L<33>	BI	9C2 73D3
CPU_D34#	R34	FSB_D_L<34>	BI	9C2 73D3
CPU_D35#	R35	FSB_D_L<35>	BI	9C2 73D3
CPU_D36#	P35	FSB_D_L<36>	BI	9C2 73D3
CPU_D37#	R39	FSB_D_L<37>	BI	9C2 73D3
CPU_D38#	R37	FSB_D_L<38>	BI	9C2 73D3
CPU_D39#	R38	FSB_D_L<39>	BI	9C2 73D3
CPU_D40#	L37	FSB_D_L<40>	BI	9C2 73D3
CPU_D41#	L39	FSB_D_L<41>	BI	9C2 73D3
CPU_D42#	L38	FSB_D_L<42>	BI	9C2 73D3
CPU_D43#	N36	FSB_D_L<43>	BI	9C2 73D3
CPU_D44#	N38	FSB_D_L<44>	BI	9C2 73D3
CPU_D45#	J39	FSB_D_L<45>	BI	9C2 73D3
CPU_D46#	J38	FSB_D_L<46>	BI	9C2 73D3
CPU_D47#	J37	FSB_D_L<47>	BI	9C2 73D3
CPU_D48#	L42	FSB_D_L<48>	BI	9C2 73D3
CPU_D49#	M42	FSB_D_L<49>	BI	9C2 73D3
CPU_D50#	P41	FSB_D_L<50>	BI	9C2 73D3
CPU_D51#	N41	FSB_D_L<51>	BI	9C2 73D3
CPU_D52#	N40	FSB_D_L<52>	BI	9C2 73D3
CPU_D53#	M40	FSB_D_L<53>	BI	9B2 73D3
CPU_D54#	H40	FSB_D_L<54>	BI	9B2 73D3
CPU_D55#	K42	FSB_D_L<55>	BI	9B2 73D3
CPU_D56#	H41	FSB_D_L<56>	BI	9B2 73D3
CPU_D57#	L41	FSB_D_L<57>	BI	9B2 73D3
CPU_D58#	H43	FSB_D_L<58>	BI	9B2 73D3
CPU_D59#	H42	FSB_D_L<59>	BI	9B2 73D3
CPU_D60#	K41	FSB_D_L<60>	BI	9B2 73D3
CPU_D61#	J40	FSB_D_L<61>	BI	9B2 73D3
CPU_D62#	H39	FSB_D_L<62>	BI	9B2 73D3
CPU_D63#	M43	FSB_D_L<63>	BI	9B2 73D3
CPU_BPRI#	AA41	FSB_BPRI_L	OUT	9D6 73C3
CPU_DEFER#	AA40	FSB_DEFER_L	OUT	9D6 73C3
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	OUT	9B6 73B3
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	OUT	9B6 73B3
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	OUT	12C3 73B3
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	OUT	12C3 73B3
BCLK_OUT_NB_P	AL41	73B3 FSB_CLK_MCP_P		
BCLK_OUT_NB_N	AK42	73B3 FSB_CLK_MCP_N		
BCLK_IN_N	AK41			
BCLK_IN_P	AJ40			
CPU_A20M#	AF41	CPU_A20M_L	OUT	9C8 73C3
CPU_IGNNE#	AH39	CPU_IGNNE_L	OUT	9C8 73C3
CPU_INIT#	AH42	CPU_INIT_L	OUT	9D6 73C3
CPU_INTR	AF42	CPU_INTR	OUT	9C8 73C3
CPU_NMI	AG41	CPU_NMI	OUT	9B8 73C3
CPU_SMI#	AH41	CPU_SMI_L	OUT	9B8 73B3
CPU_PWRGD	AH43	CPU_PWRGD		
CPU_RESET#	H38	FSB_CPURST_L	OUT	9D6 12C2 73C3
CPU_SLP#	AM33	FSB_CPUSLP_L	OUT	9B2 73B3
CPU_DPSLP#	AN33	CPU_DPSLP_L	OUT	9B2 73B3
CPU_DPWR#	AM32	FSB_DPWR_L	OUT	9B2 73B3
CPU_STPCLK#	AG42	CPU_STPCLK_L	OUT	9C8 73B3
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	OUT	9B2 62C7 73B3

Loop-back clock for delay matching.

22C8 21D3 13A2 7D7 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

73B3 41C4 9C6 IN PM_THRMTRIP_L
73C3 9C8 IN CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
NO STUFF
R1421 1K 5% 1/16W MF-LF 402
NO STUFF
R1422 1K 5% 1/16W MF-LF 402

22C2 PP1V05_S0_MCP_PLL_FSB
270 mA (A01)

206 mA	AG27	+V_DLL_DLCELL_AVDD
20 mA	AH27	+V_PLL_MCLK
29 mA	AG28	+V_PLL_FSB
15 mA	AH28	+V_PLL_CPU

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

73B3 MCP_BCLK_VML_COMP_VDD AM39 BCLK_VML_COMP_VDD
73B3 MCP_BCLK_VML_COMP_GND AM40 BCLK_VML_COMP_GND
73B3 MCP_CPU_COMP_VCC AM43 CPU_COMP_VCC
73B3 MCP_CPU_COMP_GND AM42 CPU_COMP_GND

=PP1V05_S0_MCP_FSB 7D7 13B7 21D3 22C8
NO STUFF
R1440 150 5% 1/16W MF-LF 402
OUT 9B2 12C7 73C3

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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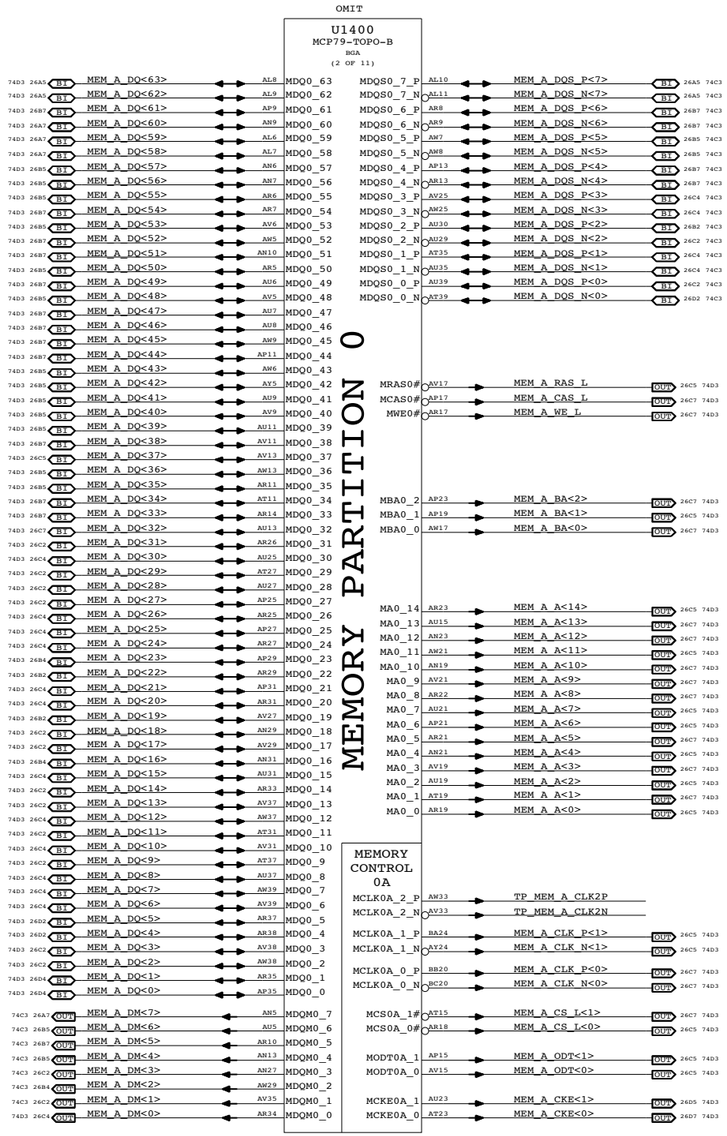
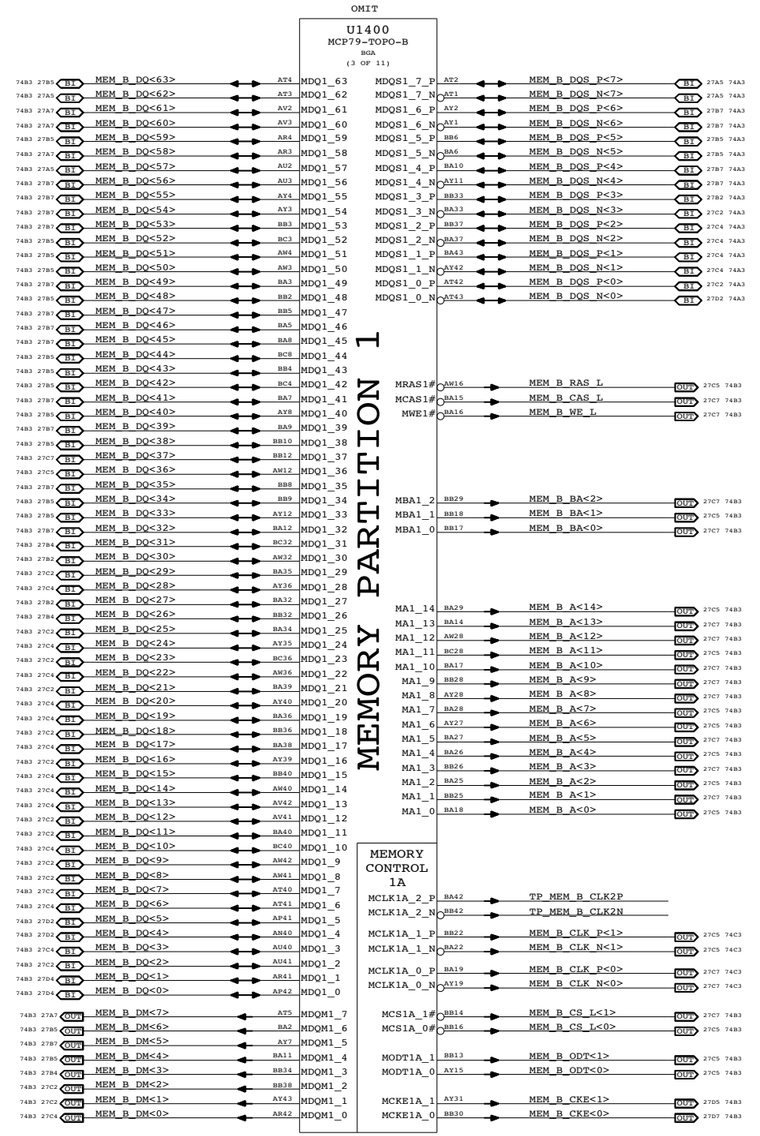
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 13 OF 81	





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE	SHT	OF
NONE	14	81

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MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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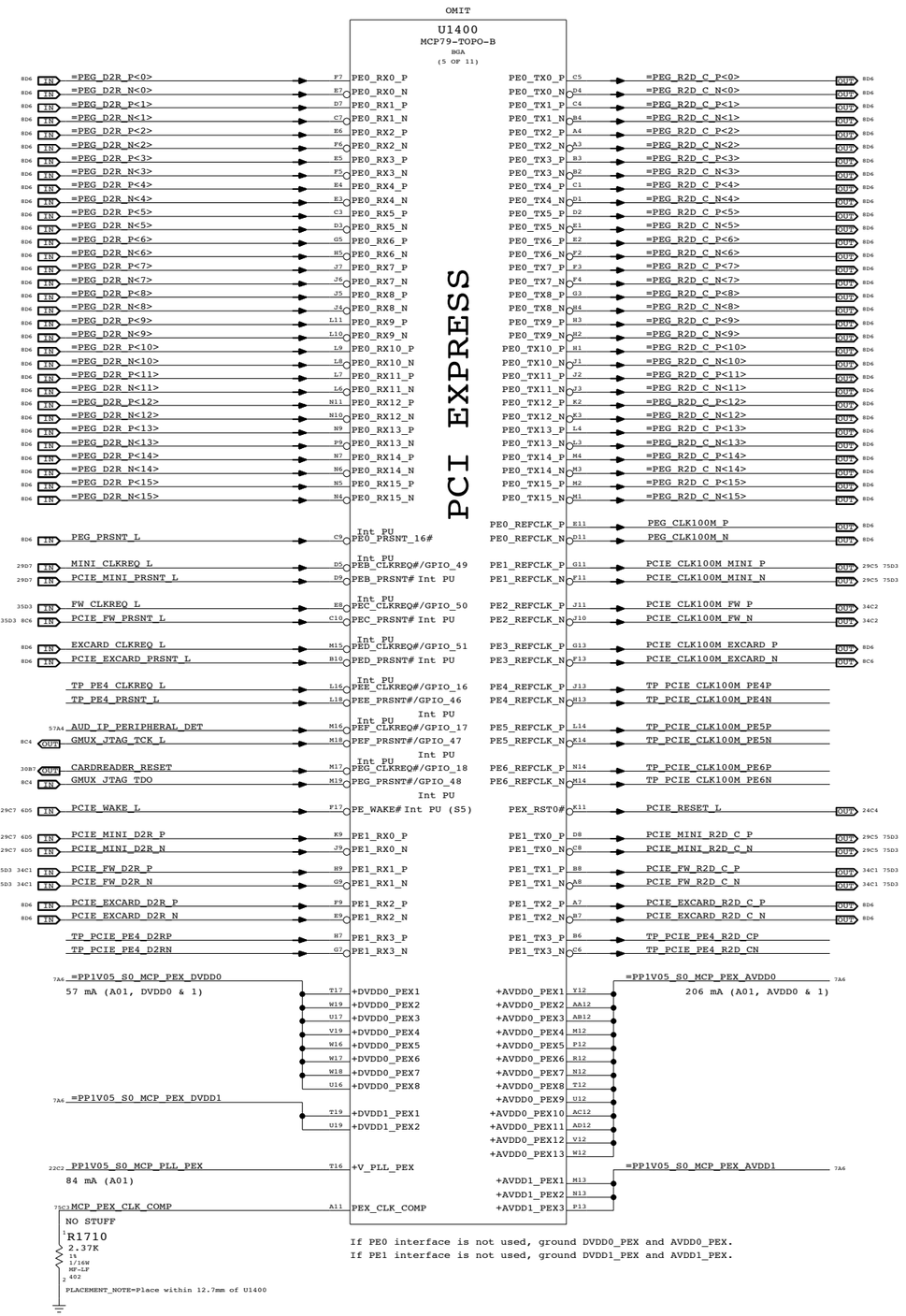
SCALE: NONE	SHT 15 OF 81	



MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 16 OF 81	

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OMIT

U1400
MCP79-TOPO-B
BGA
(6 OF 11)

LAN

DACS

FLAT PANEL

=PP3V3_ENET_MCP_RMGT — 7B5 17D7 22A5 22B6 — 83 mA (A01)
+3.3V_DUAL_RMGT1 J24
+3.3V_DUAL_RMGT2 K24

=PP1V05_ENET_MCP_RMGT — 7A5 22D6 — 131 mA (A01)
+V_DUAL_RMGT1 U23
+V_DUAL_RMGT2 V23

77D3 31C1 IN ENET_RXD<0> — C23 RGMII_RXD0
77D3 31C1 IN ENET_RXD<1> — B23 RGMII_RXD1
77D3 31C1 IN ENET_RXD<2> — E24 RGMII_RXD2
77D3 31C1 IN ENET_RXD<3> — A24 RGMII_RXD3
77D3 31C1 IN ENET_CLK125M_RXCLK — A23 RGMII_RXC/MII_RXCLK
77D3 31B1 IN ENET_RX_CTRL — C22 RGMII_RXCTL/MII_RXDV
8C4 IN =MCP_MII_RXER — F23 MII_RXER/GPIO_36
8C4 IN =MCP_MII_COL — B26 MII_COL/GPIO_20/MSMB_DATA
8C4 IN =MCP_MII_CRS — B22 MII_CRS/GPIO_21/MSMB_CLK
TP_ENET_INTR_L — J22 RGMII_INTR/GPIO_35
22A6 PP1V05_ENET_MCP_PLL_MAC — 5 mA (A01) — T23 +V_DUAL_MACPLL

MII_VREF B28 — MCP_MII_VREF — IN 22A4
RGMII_TXD0 B24 — ENET_TXD<0> — OUT 31C6 77D3
RGMII_TXD1 C24 — ENET_TXD<1> — OUT 31C6 77D3
RGMII_TXD2 C25 — ENET_TXD<2> — OUT 31C6 77D3
RGMII_TXD3 D25 — ENET_TXD<3> — OUT 31C6 77D3
RGMII_TXC/MII_TXCLK D24 — ENET_CLK125M_TXCLK — OUT 31C8 77D3
RGMII_TXCTL/MII_TXEN C26 — ENET_TX_CTRL — OUT 31B6 77C3
RGMII_MDC D21 — ENET_MDC — OUT 31B6 77D3
RGMII_MDIO C21 — ENET_MDIO — B1 31B6 77D3
RGMII_PWRDWN/GPIO_37 G23 — TP_ENET_PWRDWN_L

77D3 MCP_MII_COMP_VDD — C27 MII_COMP_VDD
77D3 MCP_MII_COMP_GND — B27 MII_COMP_GND

BUF_25MHZ E23 — MCP_CLK25M_BUF0_R — OUT 32A5 77D3
MII_RESET# J23 — ENET_RESET_L — OUT 31B7 77C3

PP3V3_S0_MCP_DAC — 23D2
+V_RGB_DAC J32 — 103 mA
+V_TV_DAC K32 — 103 mA
206 mA (A01)

TP_MCP_RGB_DAC_RSET — C39 RGB_DAC_RSET
TP_MCP_RGB_DAC_VREF — B38 RGB_DAC_VREF

DDC_CLK0 B31 — MCP_DDC_CLK0
DDC_DATA0 A31 — MCP_DDC_DATA0

RGB_DAC_RED B39 — TP_MCP_RGB_RED
RGB_DAC_GREEN A39 — TP_MCP_RGB_GREEN
RGB_DAC_BLUE B40 — TP_MCP_RGB_BLUE
RGB_DAC_HSYNC A40 — TP_MCP_RGB_HSYNC
RGB_DAC_VSYNC A41 — TP_MCP_RGB_VSYNC
RGB ONLY

8D4 OUT MCP_TV_DAC_RSET — E36 TV_DAC_RSET
8D4 OUT MCP_TV_DAC_VREF — A35 TV_DAC_VREF

TV / Component
C / Pr
Y / Y
Comp / Pb
TV_DAC_RED A36 — CRT_IG_R_C_PR — OUT 8D4
TV_DAC_GREEN B36 — CRT_IG_G_Y_Y — OUT 8D4
TV_DAC_BLUE C36 — CRT_IG_B_COMP_PB — OUT 8D4
TV_DAC_HSYNC/GPIO_44 D36 — CRT_IG_HSYNC — OUT 8D4
TV_DAC_VSYNC/GPIO_45 C37 — CRT_IG_VSYNC — OUT 8D4

8D4 IN MCP_CLK27M_XTALIN — C38 XTALIN_TV
8D4 OUT MCP_CLK27M_XTALOUT — D38 XTALOUT_TV

19C1 7A3 =PP3V3_S5_MCP_GPIO
42C3 BI LPCPLUS_GPIO — E16 GPIO_6/FERR*/IGPU_GPIO_6
69A5 IN DP_IG_CA_DET — B15 GPIO_7/NFERR*/IGPU_GPIO_7

IFPA_TXC_P B35 — LVDS_IG_A_CLK_P — OUT 68B3 75B3
IFPA_TXC_N C35 — LVDS_IG_A_CLK_N — OUT 68B3 75B3
IFPA_TXD0_P B32 — LVDS_IG_A_DATA_P<0> — OUT 6C7 68C2 75B3
IFPA_TXD0_N A32 — LVDS_IG_A_DATA_N<0> — OUT 6C7 68C2 75B3
IFPA_TXD1_P D32 — LVDS_IG_A_DATA_P<1> — OUT 6C7 68C2 75B3
IFPA_TXD1_N C32 — LVDS_IG_A_DATA_N<1> — OUT 6C7 68C2 75B3
IFPA_TXD2_P D33 — LVDS_IG_A_DATA_P<2> — OUT 6C7 68C2 75B3
IFPA_TXD2_N C33 — LVDS_IG_A_DATA_N<2> — OUT 6C7 68C2 75B3
IFPA_TXD3_P B34 — LVDS_IG_A_DATA_P<3> — OUT 8D4
IFPA_TXD3_N C34 — LVDS_IG_A_DATA_N<3> — OUT 8D4

IFPB_TXC_P L31 — LVDS_IG_B_CLK_P — OUT 8D4
IFPB_TXC_N K31 — LVDS_IG_B_CLK_N — OUT 8D4
IFPB_TXD4_P J29 — LVDS_IG_B_DATA_P<0> — OUT 8C4
IFPB_TXD4_N H29 — LVDS_IG_B_DATA_N<0> — OUT 8C4
IFPB_TXD5_P L29 — LVDS_IG_B_DATA_P<1> — OUT 8C4
IFPB_TXD5_N K29 — LVDS_IG_B_DATA_N<1> — OUT 8C4
IFPB_TXD6_P L30 — LVDS_IG_B_DATA_P<2> — OUT 8C4
IFPB_TXD6_N K30 — LVDS_IG_B_DATA_N<2> — OUT 8C4
IFPB_TXD7_P N30 — LVDS_IG_B_DATA_N<3> — OUT 8C4
IFPB_TXD7_N M30 — OUT 8C4

DDC_CLK2/GPIO_23 C30 — LVDS_IG_DDC_CLK — OUT 6C7 68C5
DDC_DATA2/GPIO_24 B30 — LVDS_IG_DDC_DATA — B1 6C7 68C5

DDC_CLK3 D31 — =MCP_HDMI_DDC_CLK — OUT 69D3
DDC_DATA3 E31 — =MCP_HDMI_DDC_DATA — B1 69D3

IFPAB_RSET E32 — MCP_IFPAB_RSET — OUT 23C6 75B3
IFPAB_VPROBE G31 — MCP_IFPAB_VPROBE — OUT 23C6 75B3

R1850 10K 5% 1/16W MF-LF 402

LVDS_IG_BKL_PWM — (See below) — G39 LCD_BKL_CTL/GPIO_57
72D7 71A7 OUT LVDS_IG_BKL_ON — E37 LCD_BKL_ON/GPIO_59
72C8 72B7 OUT LVDS_IG_PANEL_PWR — F40 LCD_PANEL_PWR/GPIO_58

69D3 OUT =MCP_HDMI_TXC_P — D35 HDMI_TXC_P/ML0_LANE3_P
69D3 OUT =MCP_HDMI_TXC_N — E35 HDMI_TXC_N/ML0_LANE3_N
69D3 OUT =MCP_HDMI_TXD_P<0> — G35 HDMI_TXD0_P/ML0_LANE2_P
69D3 OUT =MCP_HDMI_TXD_N<0> — F35 HDMI_TXD0_N/ML0_LANE2_N
69D3 OUT =MCP_HDMI_TXD_P<1> — F33 HDMI_TXD1_P/ML0_LANE1_P
69D3 OUT =MCP_HDMI_TXD_N<1> — G33 HDMI_TXD1_N/ML0_LANE1_N
69D3 OUT =MCP_HDMI_TXD_P<2> — J33 HDMI_TXD2_P/ML0_LANE0_P
69D3 OUT =MCP_HDMI_TXD_N<2> — H33 HDMI_TXD2_N/ML0_LANE0_N

75B3 69C7 OUT DP_IG_AUX_CH_P — D43 DP_AUX_CH0_P
75B3 69C7 OUT DP_IG_AUX_CH_N — C43 DP_AUX_CH0_N

8B4 IN =DVI_HPD_GMUX_INT — (See below) — C31 HPLUG_DET2/GPIO_22
69D3 IN =MCP_HDMI_HPD — F31 HPLUG_DET3

23D7 7B6 =PP3V3R1V8_S0_MCP_IFP_VDD — 190 mA (A01, 1.8V) — M27 +VDD_IFPA, M26 +VDD_IFPB
23C5 PP3V3_S0_MCP_VPLL — 16 mA (A01) — 8 mA M28 +V_PLL_IFPAB, 8 mA M29 +V_PLL_HDMI
23D7 7D7 =PP1V05_S0_MCP_HDMI_VDD — 95 mA (A01) — T25 +VDD_HDMI

75B3 23C7 OUT MCP_HDMI_RSET — J31 HDMI_RSET
75B3 23C7 OUT MCP_HDMI_VPROBE — J30 HDMI_VPROBE

=PP3V3_S0_MCP_GPIO — 7C5 18D1 20A4
R1860 100K 5% 1/16W MF-LF 402
R1861 100K 5% 1/16W MF-LF 402

R1810 49.9 1% 1/16W MF-LF 402
R1811 49.9 1% 1/16W MF-LF 402
R1820 47K 5% 1/16W MF-LF 402

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 17 OF 81	

OMIT

U1400
MCP79-TOPO-B
BGA
(7 OF 11)

PCI_REQ0_L
PCI_REQ1_L
FW_PWR_EN
AUD_IPHS_SWITCH_EN
MCP_RS232_SIN_L

MCP_DEBUG<0>
MCP_DEBUG<1>
MCP_DEBUG<2>
MCP_DEBUG<3>
MCP_DEBUG<4>
MCP_DEBUG<5>
MCP_DEBUG<6>
MCP_DEBUG<7>

TP_PCI_AD<8>
TP_PCI_AD<9>
TP_PCI_AD<10>
TP_PCI_AD<11>
TP_PCI_AD<12>
TP_PCI_AD<13>
TP_PCI_AD<14>
TP_PCI_AD<15>
TP_PCI_AD<16>
TP_PCI_AD<17>
TP_PCI_AD<18>
TP_PCI_AD<19>
TP_PCI_AD<20>
TP_PCI_AD<21>
TP_PCI_AD<22>
TP_PCI_AD<23>
TP_PCI_AD<24>
TP_PCI_AD<25>
TP_PCI_AD<26>
TP_PCI_AD<27>
TP_PCI_AD<28>
TP_PCI_AD<29>
TP_PCI_AD<30>
TP_PCI_AD<31>

TP_PCI_INTW_L
TP_PCI_INTX_L
TP_PCI_INTY_L
TP_PCI_INTZ_L

TP_PCI_TRDY_L

PM_CLKRUN_L
FW_PME_L
TP_LPC_DRQ0_L
LPC_SERIRQ

PCI_REQ0#
PCI_REQ1#/FANRPM2
PCI_REQ2#/GPIO_40/RS232_DSR#
PCI_REQ3#/GPIO_38/RS232_CTS#
PCI_REQ4#/GPIO_52/RS232_SIN#

PCI_AD0
PCI_AD1
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD28
PCI_AD29
PCI_AD30
PCI_AD31

PCI_INTW#
PCI_INTX#
PCI_INTY#
PCI_INTZ#

PCI_TRDY#

PCI_CLKRUN#/GPIO_42
PCI_DRQ1#/GPIO_19 Int PU
LPC_DRQ0# Int PU
LPC_SERIRQ Int PU

PCI

PCI_GNT0#
PCI_GNT1#/FANCTL2
PCI_GNT2#/GPIO_41/RS232_DTR#
PCI_GNT3#/GPIO_39/RS232_RTS#
PCI_GNT4#/GPIO_53/RS232_SOUT#

TP_PCI_GNT0_L
TP_PCI_GNT1_L
GMUX_JTAG_TMS
GMUX_JTAG_TDI
MCP_RS232_SOUT_L

PCI_CBE0#
PCI_CBE1#
PCI_CBE2#
PCI_CBE3#

TP_PCI_C_BE_L<0>
TP_PCI_C_BE_L<1>
TP_PCI_C_BE_L<2>
TP_PCI_C_BE_L<3>

PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_PAR
PCI_PERR#/GPIO_43/RS232_DCD#
PCI_SERR#
PCI_STOP#

TP_PCI_DEVSEL_L
TP_PCI_FRAME_L
TP_PCI_IRDY_L
TP_PCI_PAR
TP_PCI_PERR_L
TP_PCI_SERR_L
TP_PCI_STOP_L

PCI_PME#/GPIO_30
Int PU (S5)

PM_LATRIGGER_L

PCI_RESET0#
PCI_RESET1#

MEM_VTT_EN_R
TP_PCI_RESET1_L

PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLKIN

TP_PCI_CLK0
TP_PCI_CLK1
PCI_CLK33M_MCP_R

R1910
22
5%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place close to pin R8

PCI_CLK33M_MCP

LPC

LPC_FRAME#
LPC_PWRDWN#/GPIO_54/EXT_NMI#
LPC_RESET0#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_CLK0

LPC_FRAME_R_L
LPC_PWRDWN_L
LPC_RESET_L
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_CLK33M_SMC_R

R1960 22 5% 1/16W MF-LF 402 LPC_FRAME_L
R1950 22 5% 1/16W MF-LF 402 LPC_AD<0>
R1951 22 5% 1/16W MF-LF 402 LPC_AD<1>
R1952 22 5% 1/16W MF-LF 402 LPC_AD<2>
R1953 22 5% 1/16W MF-LF 402 LPC_AD<3>

R1961
10K
5%
1/16W
MF-LF
402
Strap for Boot ROM Selection (See HDA_SDOUT)

GND

GND65 GND66 GND67 GND68 GND69 GND70 GND71 GND72 GND73 GND74 GND75 GND76 GND77 GND78 GND79 GND80 GND81 GND82 GND83 GND84 GND85 GND86 GND87 GND88 GND89 GND90 GND91 GND92 GND93 GND94 GND95 GND96 GND97

GND98 GND99 GND100 GND101 GND102 GND103 GND104 GND105 GND106 GND107 GND108 GND109 GND110 GND111 GND112 GND113 GND114 GND115 GND116 GND117 GND118 GND119 GND120 GND121 GND122 GND123 GND124 GND125 GND126 GND127 GND128 GND129 GND130

=PP3V3_S0_MCP_GPIO

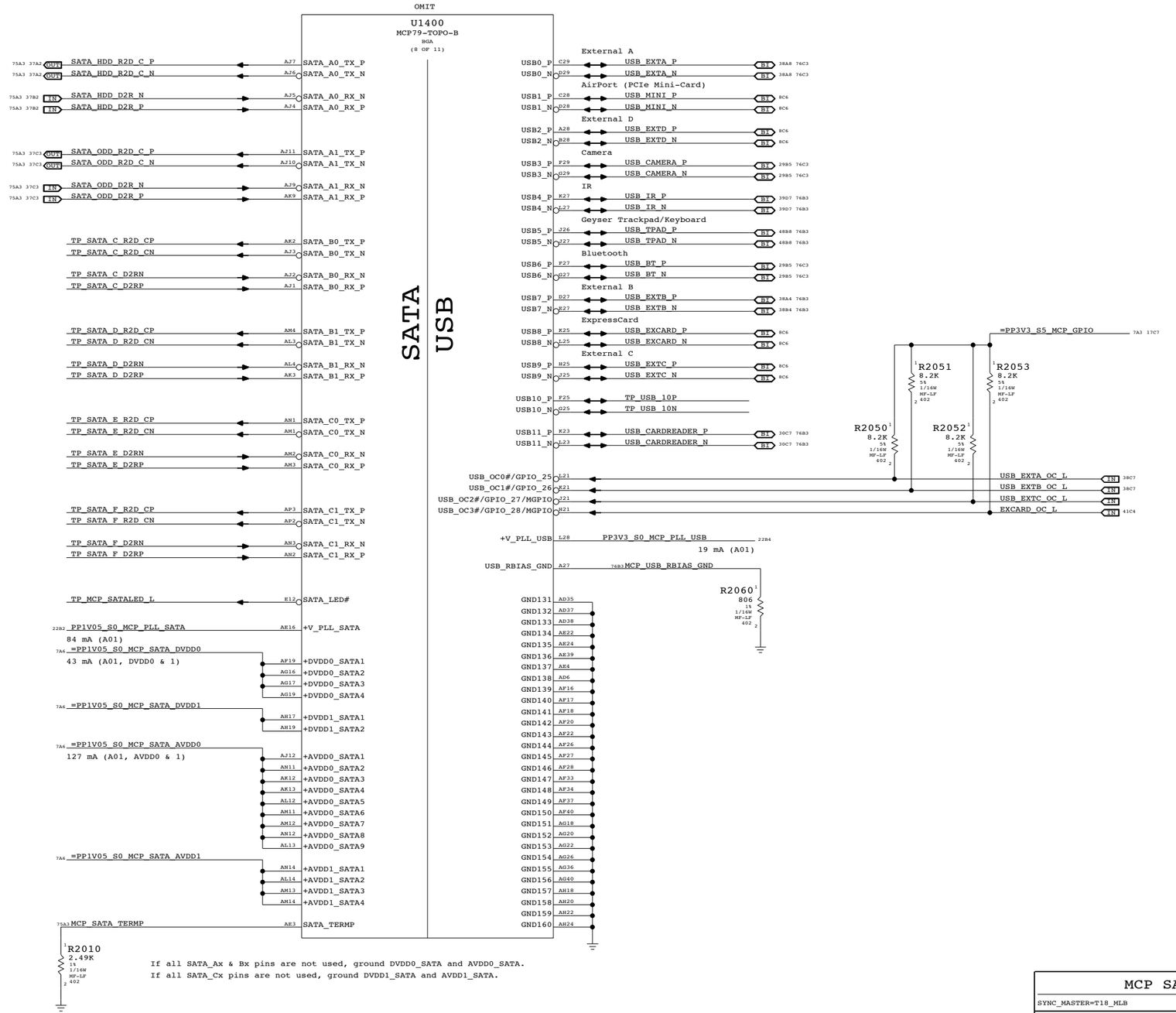
MCP_RS232_SOUT_L R1989 8.2K
PCI_REQ0_L R1990 8.2K
PCI_REQ1_L R1991 8.2K
FW_PWR_EN R1992 8.2K
MCP_RS232_SIN_L R1994 8.2K
5% 1/16W MF-LF 402

MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 18 OF 81	



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 19 OF 81	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

HDA_SDIN0 → HDA_SDATA_IN0 (G15) Int PD
TP_MLB_RAM_SIZE → HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK (J14) Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems) → HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA (J15) Int PD
MCP_HDA_PULLDN_COMP → HDA_PULLDN_COMP (A15)
PP1V05_S0_MCP_PLL_NV (37 mA (A01)) → +V_PLL_NV_H (AE18) 20 mA; +V_PLL_SP_SPREF (AE17) 17 mA

HDA_SDATA_OUT (F15) → HDA_SDOUT_R → R2170 22 5% 1/16W MF-LF 402 → HDA_SDOUT
HDA_BITCLK (E15) → HDA_BIT_CLK_R → R2171 22 5% 1/16W MF-LF 402 → HDA_BIT_CLK
HDA_RESET* (K15) → HDA_RST_R_L → R2172 22 5% 1/16W MF-LF 402 → HDA_RST_L
HDA_SYNC (L15) → HDA_SYNC_R → R2173 22 5% 1/16W MF-LF 402 → HDA_SYNC

=PP3V3R1V5_S0_MCP_HDA (7C5 20D8 22A8) 7 mA (A01)
+V_DUAL_HDA1 (J16), +V_DUAL_HDA2 (K16) ← R2160 8.2K 5% 1/16W MF-LF 402

=PP3V3R1V5_S0_MCP_HDA (22A8 20D3 7C5) → R2110 49.9 1% 1/16W MF-LF 402

PP3V3_G3_RTC (24D4 21A5 6C3) → R2120 49.9K 1% 1/16W MF-LF 402; R2121 49.9K 1% 1/16W MF-LF 402

MISC

=SPI_CS1_R_L_USE_MLB (42B8 OUT) → GPIO_1/PWRDN_OK/SPI_CS1 (L24)
SMC_ADAPTER_EN (41B2 40D5 35B5 32B7 IN) → GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L (L26)
TP_SB_A20GATE → A20GATE (K13) Int PU
TP_MCP_KBDRSTIN_L → KBRDRSTIN* (L13) Int PU
SMC_WAKE_SCI_L (40C5 IN) → SIO_PME* (C19) Int PU (S5)
SMC_RUNTIME_SCI_L (40B8 IN) → EXT_SMI/GPIO_32* (C18) Int PU (S5)
SM_INTRUDER_L → INTRUDER* (B20)
TP_MCP_LID_L → LID* (M25) Int PU (S5)
PM_BATLOW_L (40B8 IN) → LLB* (M24) Int PU (S5)
PM_DPRSLPVR (73B3 62D8 IN) → CPU_DPRSLPVR (M22)
PM_PWRBTN_L (40C8 IN) → PWRBTN* (C16) Int PU (S5)
PM_SYSRST_DEBOUNCE_L (24A1 IN) → RSTBTN* (D16) Int PU
RTC_RST_L → RTC_RST* (C20)
PM_RSMRST_L (40D8 IN) → PWRGD_SB (D20)
MCP_PS_PWRGD (24A5 IN) → PS_PWRGD (E20)
MCP_CPU_VLD (24A5 IN) → CPU_VLD (C17)
JTAG_MCP_TDI (12C3 IN) → JTAG_TDI (E19) Int PU
JTAG_MCP_TDO (12C3 OUT) → JTAG_TDO (F19)
JTAG_MCP_TMS (12C3 IN) → JTAG_TMS (J19) Int PU
JTAG_MCP_TRST_L (12C3 IN) → JTAG_TRST* (J18)
JTAG_MCP_TCK (12B6 IN) → JTAG_TCK (G19)
MCP_CLK25M_XTALIN (24B8 IN) → XTALIN (A16)
MCP_CLK25M_XTALOUT (24C8 OUT) → XTALOUT (B16)
RTC_CLK32K_XTALIN (24C8 IN) → XTALIN_RTC (A19)
RTC_CLK32K_XTALOUT (24C8 OUT) → XTALOUT_RTC (B19)

R2150 10K 5% 1/16W MF-LF 402; R2151 100K 5% 1/16W MF-LF 402

HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK (K17) → MCP_GPIO_4 (20A4)
HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA (L17) → AUD_I2C_INT_L (IN 20A4 57D3)
SLP_S3* (G17) → PM_SLP_S3_L (OUT 6C3 32B7 35A5 40C5 66D5 70D8)
SLP_RMGT* (J17) → PM_SLP_RMGT_L (OUT 8D1)
SLP_S5* (H17) → PM_SLP_S4_L (OUT 6C3 40C5 41A2 66C8)
THERM_DIODE_P (B11) → MCP_THMDIODE_P (OUT 46B5 80D3)
THERM_DIODE_N (C11) → MCP_THMDIODE_N (OUT 46B5 80D3)
MCP_VID0/GPIO_13 (L20) → MCP_VID<0> (OUT 20A3 63D8)
MCP_VID1/GPIO_14 (M20) → MCP_VID<1> (OUT 20A3 63C8)
MCP_VID2/GPIO_15 (M21) → MCP_VID<2> (OUT 20A3 63C8)
SPKR (C13) → MCP_SPKR (OUT 41C5)
SMB_CLK0 (L19) → SMBUS_MCP_0_CLK (OUT 12B6 43D8 76B3)
SMB_DATA0 (K19) → SMBUS_MCP_0_DATA (BI 12B6 43D8 76B3)
SMB_CLK1/MSMB_CLK (G21) → SMBUS_MCP_1_CLK (OUT 43B8 76B3)
SMB_DATA1/MSMB_DATA (F21) → SMBUS_MCP_1_DATA (BI 43B8 76B3)
SMB_ALERT*/GPIO_64 (M23) → AP_PWR_EN (OUT 20A3 29D5 32C7)
(MGPIO2) FANRPM0/GPIO_60 (B12) → MEM_EVENT_L (IN 20A4 26A5 27A5 40B8)
FANCTL0/GPIO_61 (A12) → ODD_PWR_EN_L (OUT 37D6)
(MGPIO3) FANRPM1/GPIO_63 (D12) → SMC_IG_THROTTLE_L (IN 20A4 41D4)
FANCTL1/GPIO_62 (C12) → ARB_DETECT (20A4)
CPUVDD_EN (D17) → MCP_CPUVDD_EN (OUT 24A8)
SPI_CS0/GPIO_10 (C14) → SPI_CS0_R_L (OUT 42B7 76A3)
SPI_CLK/GPIO_11 (D13) → SPI_CLK_R (OUT 42A5 42C8 76A3)
SPI_DI/GPIO_8 (C15) → SPI_MISO (IN 42A5 42B7 76A3)
SPI_DO/GPIO_9 (B14) → SPI_MOSI_R (OUT 42A5 42C7 76A3)
SUS_CLK/GPIO_34 (B18) → PM_CLK32K_SUSCLK_R (OUT 24B4 76A3)
BUF_SIO_CLK (AE7) → TP_MCP_BUF_SIO_CLK
TEST_MODE_EN (K22) → MCP_TEST_MODE_EN
PKG_TEST (L22)

R2163 10K 5% 1/16W MF-LF 402; R2190 1K 1% 1/16W MF-LF 402

=PP3V3_S0_MCP (7C5 21B3 22B8)
BOOT_MODE_SAFE → R2180 10K 5% 1/16W MF-LF 402
BOOT_MODE_USER → R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

=PP3V3_S0_MCP_GPIO (7C5 17C1 18D1)
R2140 10K; R2141 10K; R2142 10K; R2143 10K (5% 1/16W MF-LF 402)
MCP_GPIO_4 (20C3)
AUD_I2C_INT_L (20C3 57D3)
MEM_EVENT_L (20B3 26A5 27A5 40B8)
SMC_IG_THROTTLE_L (20B3 41D4)
ARB_DETECT (20B3)
R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO (7D3)
R2154 100K 5% 1/16W MF-LF 402
AP_PWR_EN (20C3 29D5 32C7)

MCP_VID<0> (20C3 63D8)
MCP_VID<1> (20C3 63C8)
MCP_VID<2> (20C3 63C8)
R2155 22K; R2156 22K; R2157 22K (5% 1/16W MF-LF 402)

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R (20D4 76A3)
HDA_BIT_CLK_R (20D4 76B3)
HDA_RST_R_L (20D4 76A3)
HDA_SYNC_R (20D4 76B3)

C2170 10PF 5% 50V CERM 402; C2172 10PF 5% 50V CERM 402; C2171 10PF 5% 50V CERM 402; C2173 10PF 5% 50V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

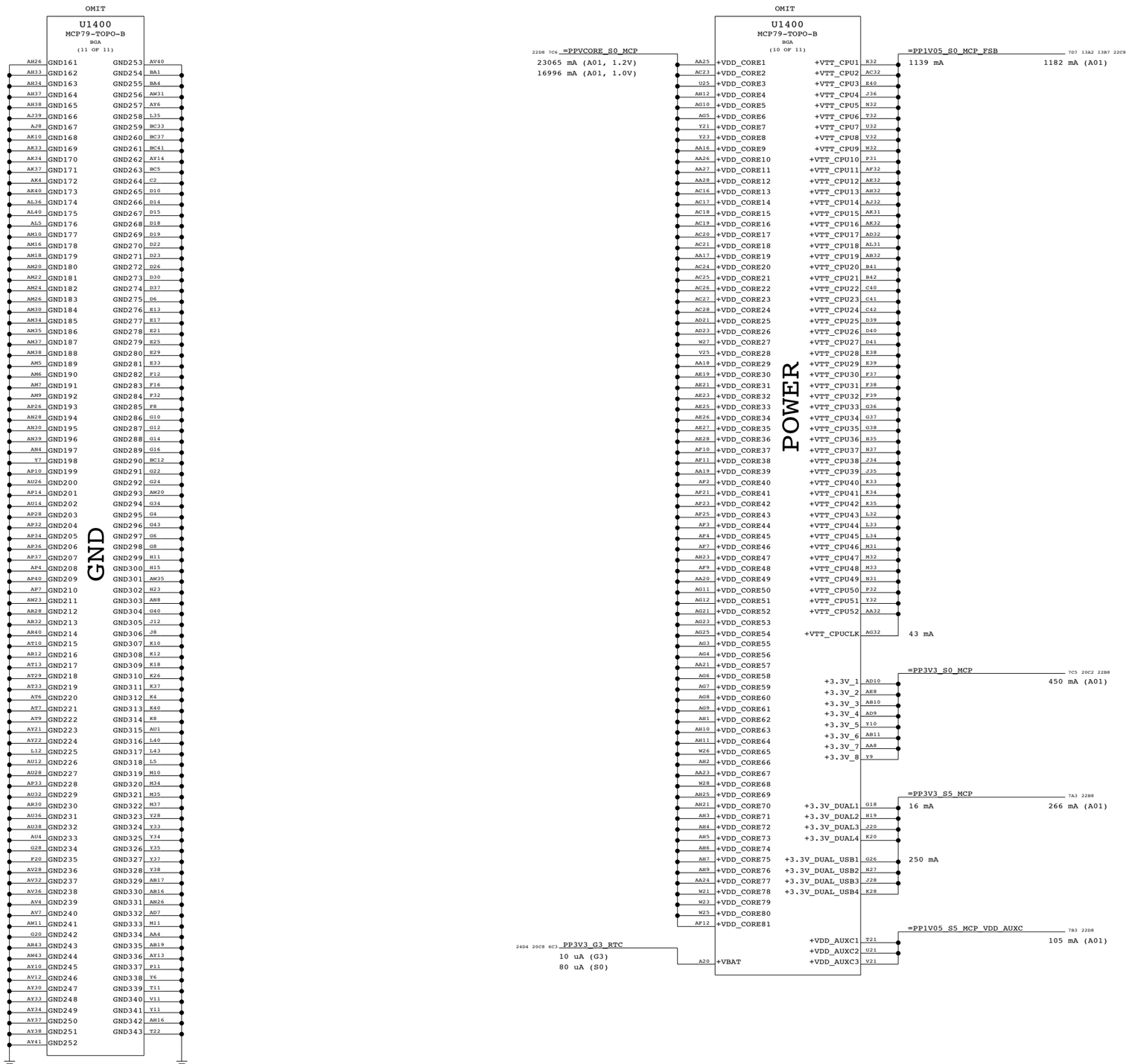
MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE: NONE SHT 20 OF 81



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 21 OF 81	

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

21D5 7C6 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R-1 402
C2501 4.7UF 20% 4V X5R-1 402
C2502 4.7UF 20% 4V X5R-1 402
C2503 4.7UF 20% 4V X5R-1 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

7D7 7A8 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R-1 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1uF 20% 10V CERM 402
C2519 0.1uF 20% 10V CERM 402

MCP SATA (DVDD) Power

7D7 7A8 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R-1 402
C2521 0.1uF 20% 10V CERM 402

7D7 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_PEX_AVDD 7A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

MCP 1.05V AUX Power

21A3 7B3 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1uF 20% 10V CERM 402
C2526 0.1uF 20% 10V CERM 402

MCP 1.05V RMGT Power

17D3 7A5 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1uF 20% 10V CERM 402

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

PP1V05_S0_MCP_SATA_AVDD 7A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

21D3 13B7 13A2 7D7 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

65B1 7B8 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

C2592 10UF 20% 6.3V X5R 603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_FSB 13A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

MCP Memory Power

15C7 15C3 7B4 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R-1 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

C2582 4.7UF 20% 4V X5R-1 402
C2583 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_PEX 16A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

21B3 20C2 7C5 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

7C5 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

C2555 2.2UF 20% 6.3V CERM 402-LF

PP3V3_S0_MCP_PLL_USB 19C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

L2584 30-OHM-1.7A 0402

C2584 4.7UF 20% 4V X5R-1 402
C2585 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_SATA 19B6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21B3 7A3 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22A5 17D7 17D3 7B5 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

L2586 30-OHM-1.7A 0402

C2586 4.7UF 20% 4V X5R-1 402
C2587 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_CORE 15C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

20D8 20D3 7C5 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

L2588 30-OHM-1.7A 0402

C2588 4.7UF 20% 4V X5R-1 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

PP1V05_S0_MCP_PLL_NV 20C7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

MCP79 Ethernet VRef

22B6 17D7 17D3 7B5 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF OUT 17D3
C2591 0.1UF 20% 10V CERM 402

7B5 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

C2595 4.7UF 20% 4V X5R-1 402
C2596 0.1UF 20% 10V CERM 402

PP1V05_ENET_MCP_PLL_MAC 17C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 22 OF 81	

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

17B6 7B6 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610
2.2UF
20%
6.3V
CERM
402-LF

17A6 7D7 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615
4.7UF
20%
4V
X5R-1
402

C2616
0.1UF
20%
10V
CERM
402

75B3 17A6 MCP_HDMI_RSET
75B3 17A6 MCP_HDMI_VPROBE

NO STUFF
C2620
0.1UF
20%
10V
CERM
402

R2620
1K
1%
1/16W
MF-LF
402

75B3 17A3 MCP_IFPAB_RSET
75B3 17A3 MCP_IFPAB_VPROBE

NO STUFF
C2630
0.1UF
20%
10V
CERM
402

NO STUFF
R2630
1K
1%
1/16W
MF-LF
402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

7C5 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640
30-OHM-1.7A
0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

17B6
16 mA (A01)

C2640
4.7UF
20%
6.3V
CERM
603

C2641
0.1uF
20%
10V
CERM
402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

7C5 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

NO STUFF
L2650
30-OHM-1.7A
0402

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

17C3
206 mA (A01)

NO STUFF
C2650
2.2UF
20%
6.3V
CERM
402-LF

R2651
0
5%
1/16W
MF-LF
402

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

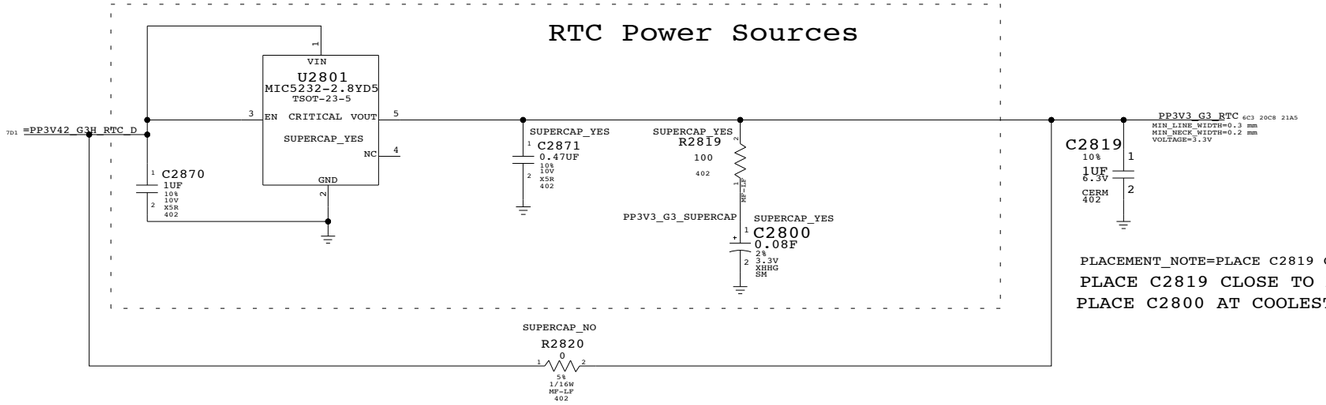
MCP Graphics Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 23 OF 81	

RTC Power Sources



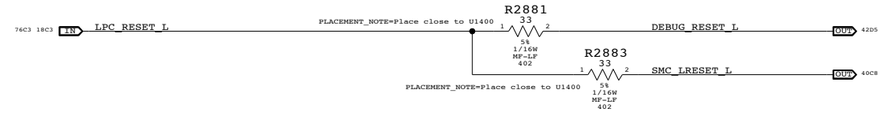
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79

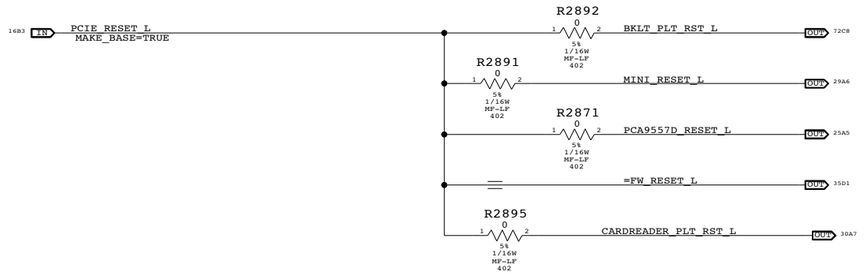
PLACE C2800 AT COOLEST SPOT ON MLB

Platform Reset Connections

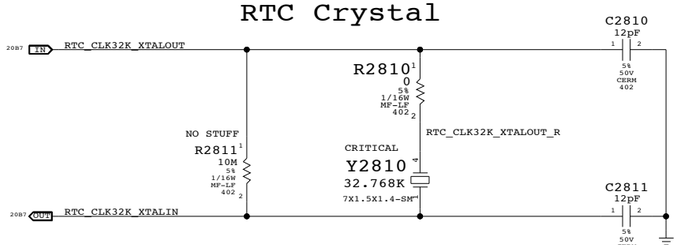
LPC Reset (Unbuffered)



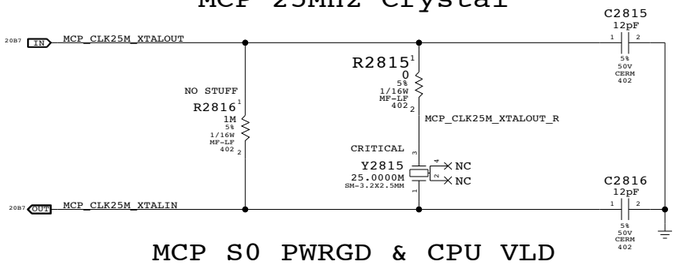
PCIE Reset (Unbuffered)



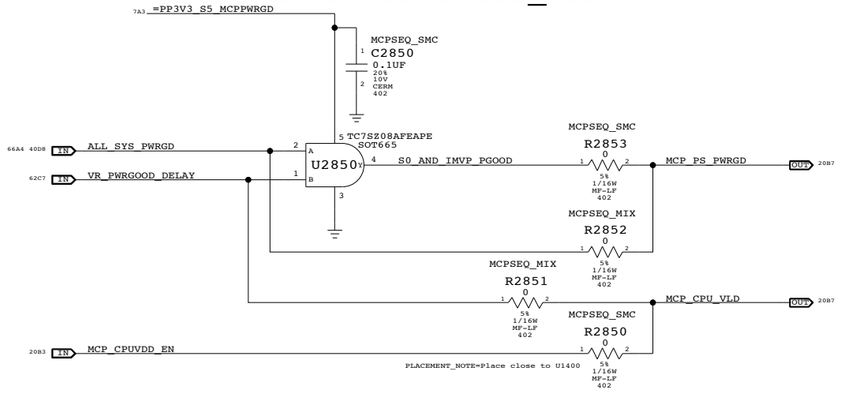
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD

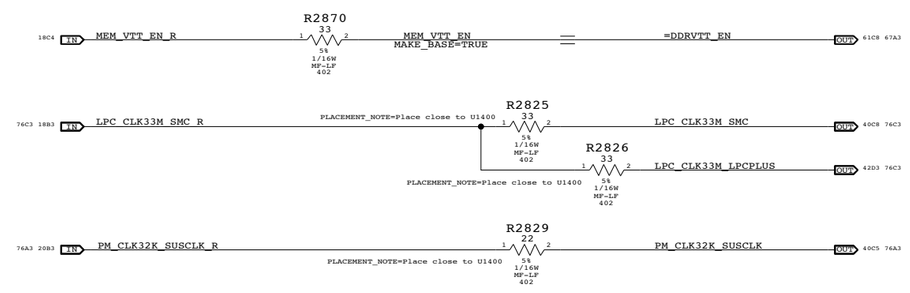


MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

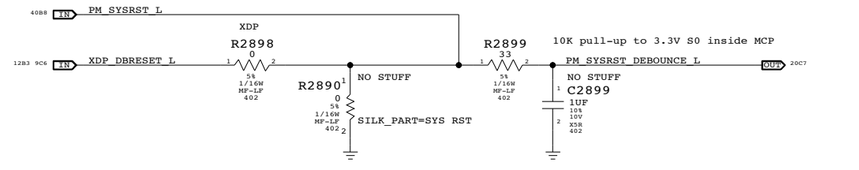
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.



Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc

SYNC_MASTER=RAYMOND SYNC_DATE=04/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 24 OF 81	

Page Notes

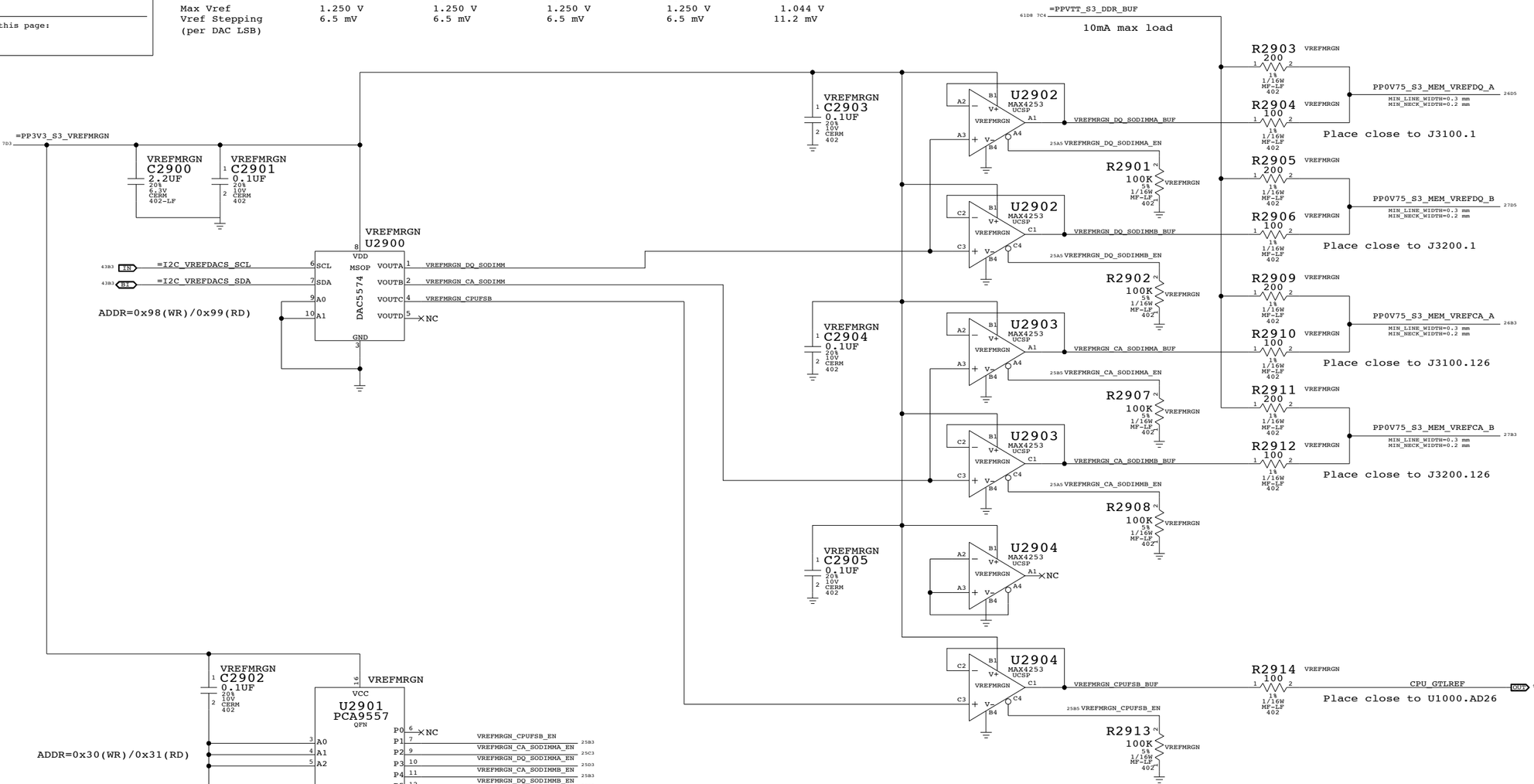
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 25 OF 81	

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

7D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3111 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3112 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3113 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3114 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3115 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3116 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3117 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)

74D3 14A5	IN	MEM_A_CKE<0>	73 CKE0	CKE1 74	MEM_A_CKE<1> IN 14A5 74D3
			75 VDD	VDD 76	
NC			77 NC	A15 78	MEM_A_A<15> IN 8D2
74D3 14C5	IN	MEM_A_BA<2>	79 BA2	A14 80	MEM_A_A<14> IN 14C5 74D3
			81 VDD	VDD 82	
74D3 14C5	IN	MEM_A_A<12>	83 A12/BC*	A11 84	MEM_A_A<11> IN 14C5 74D3
74D3 14C5	IN	MEM_A_A<9>	85 A9	A7 86	MEM_A_A<7> IN 14C5 74D3
			87 VDD	VDD 88	
74D3 14C5	IN	MEM_A_A<8>	89 A8	A6 90	MEM_A_A<6> IN 14B5 74D3
74D3 14B5	IN	MEM_A_A<5>	91 A5	A4 92	MEM_A_A<4> IN 14B5 74D3
			93 VDD	VDD 94	
74D3 14B5	IN	MEM_A_A<3>	95 A3	A2 96	MEM_A_A<2> IN 14B5 74D3
74D3 14B5	IN	MEM_A_A<1>	97 A1	A0 98	MEM_A_A<0> IN 14B5 74D3
			99 VDD	VDD 100	
74D3 14B5	IN	MEM_A_CLK_P<0>	101 CK0	CK1 102	MEM_A_CLK_P<1> IN 14B5 74D3
74D3 14B5	IN	MEM_A_CLK_N<0>	103 CK0*	CK1* 104	MEM_A_CLK_N<1> IN 14B5 74D3
			105 VDD	VDD 106	
74D3 14C5	IN	MEM_A_A<10>	107 A10/AP	BA1 108	MEM_A_BA<1> IN 14C5 74D3
74D3 14C5	IN	MEM_A_BA<0>	109 BA0	RAS* 110	MEM_A_RAS_L IN 14C5 74D3
			111 VDD	VDD 112	
74D3 14C5	IN	MEM_A_WE_L	113 WE*	S0* 114	MEM_A_CS_L<0> IN 14B5 74D3
74D3 14C5	IN	MEM_A_CAS_L	115 CAS*	ODT0 116	MEM_A_ODT<0> IN 14B5 74D3
			117 VDD	VDD 118	
74D3 14C5	IN	MEM_A_A<13>	119 A13	ODT1 120	MEM_A_ODT<1> IN 14B5 74D3
74D3 14B5	IN	MEM_A_CS_L<1>	121 S1*	NC 122	NC
			123 VDD	VDD 124	
NC			125 TEST	VREFCA 126	
			127 VSS	VSS 128	
74D3 14C7	BI	MEM_A_DQ<32>	129 DQ32	DQ36 130	MEM_A_DQ<37> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<33>	131 DQ33	DQ37 132	MEM_A_DQ<36> BI 14C7 74D3
			133 VSS	VSS 134	
74C3 14D5	BI	MEM_A_DQS_N<4>	135 DQS4*	DM4 136	MEM_A_DM<4> IN 14B7 74C3
74C3 14D5	BI	MEM_A_DQS_P<4>	137 DQS4	VSS 138	
			139 VSS	DQ38 140	MEM_A_DQ<35> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<34>	141 DQ34	DQ39 142	MEM_A_DQ<39> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<38>	143 DQ35	VSS 144	
			145 VSS	DQ44 146	MEM_A_DQ<40> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<44>	147 DQ40	DQ45 148	MEM_A_DQ<41> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<45>	149 DQ41	VSS 150	
			151 VSS	DQS5* 152	MEM_A_DQS_N<5> BI 14D5 74C3
74C3 14B7	IN	MEM_A_DM<5>	153 DM5	DQS5 154	MEM_A_DQS_P<5> BI 14D5 74C3
			155 VSS	VSS 156	
74D3 14D7	BI	MEM_A_DQ<47>	157 DQ42	DQ46 158	MEM_A_DQ<43> BI 14C7 74D3
74D3 14D7	BI	MEM_A_DQ<46>	159 DQ43	DQ47 160	MEM_A_DQ<42> BI 14C7 74D3
			161 VSS	VSS 162	
74D3 14D7	BI	MEM_A_DQ<49>	163 DQ48	DQ52 164	MEM_A_DQ<53> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<52>	165 DQ49	DQ53 166	MEM_A_DQ<48> BI 14D7 74D3
			167 VSS	VSS 168	
74C3 14D5	BI	MEM_A_DQS_N<6>	169 DQS6*	DM6 170	MEM_A_DM<6> IN 14B7 74C3
74C3 14D5	BI	MEM_A_DQS_P<6>	171 DQS6	VSS 172	
			173 VSS	DQ54 174	MEM_A_DQ<55> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<54>	175 DQ50	DQ55 176	MEM_A_DQ<50> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<51>	177 DQ51	VSS 178	
			179 VSS	DQ60 180	MEM_A_DQ<57> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<61>	181 DQ56	DQ61 182	MEM_A_DQ<56> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<60>	183 DQ57	VSS 184	
			185 VSS	DQS7* 186	MEM_A_DQS_N<7> BI 14D5 74C3
74C3 14B7	IN	MEM_A_DM<7>	187 DM7	DQS7 188	MEM_A_DQS_P<7> BI 14D5 74C3
			189 VSS	VSS 190	
74D3 14D7	BI	MEM_A_DQ<58>	191 DQ58	DQ62 192	MEM_A_DQ<62> BI 14D7 74D3
74D3 14D7	BI	MEM_A_DQ<59>	193 DQ59	DQ63 194	MEM_A_DQ<63> BI 14D7 74D3
			195 VSS	VSS 196	
		MEM_A_SA<0>	197 SA0	EVENT* 198	MEM_EVENT_L OUT 20A4 20B3 27A5 40B8
			199 VDDSPD	SDA 200	=I2C_SODIMMA_SDA BI 43D6
		MEM_A_SA<1>	201 SA1	SCL 202	=I2C_SODIMMA_SCL IN 43D6
			203 VTT	VTT 204	=PP0V75_S0_MEM_VTT_A 7C7

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL

			1 VREFDQ	VSS 2	
74D3 14B7	BI	MEM_A_DQ<0>	3 VSS	DQ4 4	MEM_A_DQ<4> BI 14B7 74D3
74D3 14B7	BI	MEM_A_DQ<1>	5 DQ0	DQ5 6	MEM_A_DQ<5> BI 14B7 74D3
			7 DQ1	VSS 8	
74D3 14A7	IN	MEM_A_DM<0>	9 VSS	DQS0* 10	MEM_A_DQS_N<0> BI 14D5 74C3
			11 DM0	DQS0 12	MEM_A_DQS_P<0> BI 14D5 74C3
			13 VSS	VSS 14	
74D3 14B7	BI	MEM_A_DQ<6>	15 DQ2	DQ6 16	MEM_A_DQ<3> BI 14B7 74D3
74D3 14B7	BI	MEM_A_DQ<7>	17 DQ3	DQ7 18	MEM_A_DQ<2> BI 14B7 74D3
			19 VSS	VSS 20	
74D3 14B7	BI	MEM_A_DQ<8>	21 DQ8	DQ12 22	MEM_A_DQ<9> BI 14B7 74D3
74D3 14B7	BI	MEM_A_DQ<12>	23 DQ9	DQ13 24	MEM_A_DQ<13> BI 14B7 74D3
			25 VSS	VSS 26	
74C3 14D5	BI	MEM_A_DQS_N<1>	27 DQS1*	DM1 28	MEM_A_DM<1> IN 14A7 74C3
74C3 14D5	BI	MEM_A_DQS_P<1>	29 DQS1	RESET* 30	MEM_RESET_L IN 27C2 28C5
			31 VSS	VSS 32	
74D3 14B7	BI	MEM_A_DQ<10>	33 DQ10	DQ14 34	MEM_A_DQ<11> BI 14B7 74D3
74D3 14B7	BI	MEM_A_DQ<15>	35 DQ11	DQ15 36	MEM_A_DQ<14> BI 14B7 74D3
			37 VSS	VSS 38	
74D3 14C7	BI	MEM_A_DQ<25>	39 DQ16	DQ20 40	MEM_A_DQ<29> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<24>	41 DQ17	DQ21 42	MEM_A_DQ<28> BI 14C7 74D3
			43 VSS	VSS 44	
74C3 14D5	BI	MEM_A_DQS_N<3>	45 DQS2*	DM2 46	MEM_A_DM<3> IN 14B7 74C3
74C3 14D5	BI	MEM_A_DQS_P<3>	47 DQS2	VSS 48	
			49 VSS	DQ22 50	MEM_A_DQ<27> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<26>	51 DQ18	DQ23 52	MEM_A_DQ<31> BI 14C7 74D3
74D3 14C7	BI	MEM_A_DQ<30>	53 DQ19	VSS 54	
			55 VSS	DQ28 56	MEM_A_DQ<18> BI 14B7 74D3
74D3 14C7	BI	MEM_A_DQ<20>	57 DQ24	DQ29 58	MEM_A_DQ<17> BI 14B7 74D3
74D3 14C7	BI	MEM_A_DQ<21>	59 DQ25	VSS 60	
			61 VSS	DQS3* 62	MEM_A_DQS_N<2> BI 14D5 74C3
74C3 14B7	IN	MEM_A_DM<2>	63 DM3	DQS3 64	MEM_A_DQS_P<2> BI 14D5 74C3
			65 VSS	VSS 66	
74D3 14C7	BI	MEM_A_DQ<23>	67 DQ26	DQ30 68	MEM_A_DQ<19> BI 14B7 74D3
74D3 14B7	BI	MEM_A_DQ<16>	69 DQ27	DQ31 70	MEM_A_DQ<22> BI 14C7 74D3
			71 VSS	VSS 72	

516-0201

PP0V75_S3_MEM_VREFCA_A 25C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

7C5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 26 OF 81	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

7D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

25C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

74B3 14A1 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 14A1 74B3
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 8D2
74B3 14C1 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 14C1 74B3
		81	VDD	VDD	82		
74B3 14C1 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 14C1 74B3
74B3 14C1 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 14C1 74B3
		87	VDD	VDD	88		
74B3 14C1 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 14B1 74B3
		93	VDD	VDD	94		
74B3 14B1 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 14B1 74B3
		99	VDD	VDD	100		
74C3 14B1 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 14B1 74C3
74C3 14B1 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 14B1 74C3
		105	VDD	VDD	106		
74B3 14C1 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 14C1 74B3
74B3 14C1 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 14C1 74B3
		111	VDD	VDD	112		
74B3 14C1 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 14B1 74B3
74B3 14C1 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 14B1 74B3
		117	VDD	VDD	118		
74B3 14C1 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 14B1 74B3
74B3 14B1 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
74B3 14C2 BI	MEM_B_DQ<37>	129	DQ32	DQ36	130	MEM_B_DQ<36>	BI 14C3 74B3
74B3 14C2 BI	MEM_B_DQ<32>	131	DQ33	DQ37	132	MEM_B_DQ<33>	BI 14C3 74B3
		133	VSS	VSS	134		
74A3 14D1 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<35>	141	DQ34	DQ39	142	MEM_B_DQ<34>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<39>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<45>	147	DQ40	DQ45	148	MEM_B_DQ<44>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 14D1 74A3
		155	VSS	VSS	156		
74B3 14D3 BI	MEM_B_DQ<46>	157	DQ42	DQ46	158	MEM_B_DQ<42>	BI 14C3 74B3
74B3 14D3 BI	MEM_B_DQ<47>	159	DQ43	DQ47	160	MEM_B_DQ<43>	BI 14C3 74B3
		161	VSS	VSS	162		
74B3 14D3 BI	MEM_B_DQ<53>	163	DQ48	DQ52	164	MEM_B_DQ<52>	BI 14D3 74B3
74B3 14D3 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 14D3 74B3
		167	VSS	VSS	168		
74A3 14D1 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<51>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<55>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<63>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<59>	BI 14D3 74B3
74B3 14D2 BI	MEM_B_DQ<58>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 14D1 74A3
		189	VSS	VSS	190		
74B3 14D3 BI	MEM_B_DQ<61>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 14D3 74B3
74B3 14D3 BI	MEM_B_DQ<60>	193	DQ59	DQ63	194	MEM_B_DQ<57>	BI 14D3 74B3
		195	VSS	VSS	196		
	MEM_B_SA<0>	197	SA0	EVENT*	198	MEM_EVENT_L	OUT 20A4 20B3 26A5 40B8
7C5 =PPSPD_S0_MEM_B		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 43C6
	MEM_B_SA<1>	201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 43C6
		203	VTT	VTT	204	=PP0V75_S0_MEM_VTT_B	7C7
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

KEY
MTG PINS

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	MEM_B_DQ<4>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<1>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<0>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 14D1 74A3
74B3 14A3 IN	MEM_B_DM<0>	11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 14D1 74A3
		13	VSS	VSS	14		
74B3 14B3 BI	MEM_B_DQ<3>	15	DQ2	DQ6	16	MEM_B_DQ<7>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<6>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 14B3 74B3
		19	VSS	VSS	20		
74B3 14B3 BI	MEM_B_DQ<13>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<14>	23	DQ9	DQ13	24	MEM_B_DQ<9>	BI 14B3 74B3
		25	VSS	VSS	26		
74A3 14D1 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 14A3 74B3
74A3 14D1 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 26C2 28C5
		31	VSS	VSS	32		
74B3 14B3 BI	MEM_B_DQ<15>	33	DQ10	DQ14	34	MEM_B_DQ<8>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<10>	35	DQ11	DQ15	36	MEM_B_DQ<11>	BI 14B3 74B3
		37	VSS	VSS	38		
74B3 14C3 BI	MEM_B_DQ<20>	39	DQ16	DQ20	40	MEM_B_DQ<16>	BI 14B3 74B3
74B3 14B3 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<21>	BI 14C3 74B3
		43	VSS	VSS	44		
74A3 14D1 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46	MEM_B_DM<2>	IN 14B3 74B3
74A3 14D1 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<18>	BI 14B3 74B3
74B3 14C3 BI	MEM_B_DQ<22>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 14C3 74B3
74B3 14B3 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<29>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<25>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<28>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 14D1 74A3
74B3 14B3 IN	MEM_B_DM<3>	63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 14D1 74A3
		65	VSS	VSS	66		
74B3 14C3 BI	MEM_B_DQ<26>	67	DQ26	DQ30	68	MEM_B_DQ<30>	BI 14C3 74B3
74B3 14C3 BI	MEM_B_DQ<31>	69	DQ27	DQ31	70	MEM_B_DQ<27>	BI 14C3 74B3
		71	VSS	VSS	72		

CRITICAL
KEY
516S0706

DDR3 GROUND RETURN CAPS (MCP SIDE)

7B4 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1 CRITICAL

PP0V75_S3_MEM_VREFCA_B 25C1

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

R3240 10K 5% 1/16W MF-LF 402
C3240 2.2UF 20% 6.3V CERM 402-LF
R3241 10K 5% 1/16W MF-LF 402
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

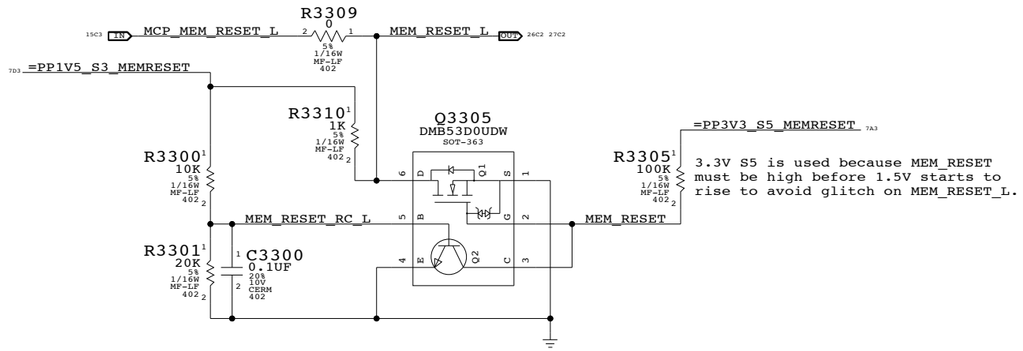
SYNC_MASTER=BEN SYNC_DATE=05/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 27 OF 81	

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.

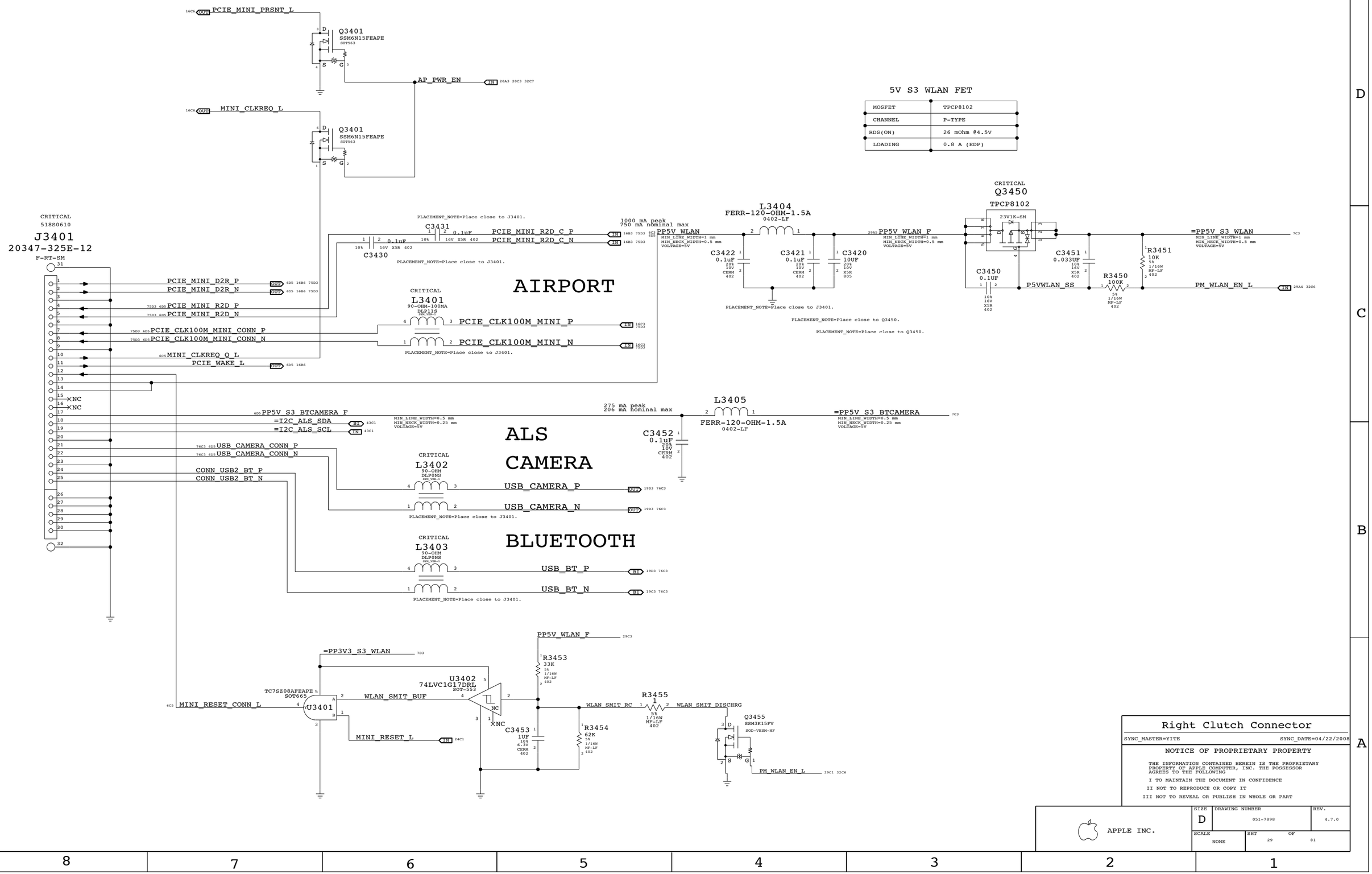


DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 28 OF 81	


PCIE_MINI_PRSNT_L
Q3401
SSM6N15FEAPE
SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401
SSM6N15FEAPE
SOT563
5V S3 WLAN FET
MOSFET TPCP8102
CHANNEL P-TYPE
RDS(ON) 26 mOhm @4.5V
LOADING 0.8 A (EDP)
CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM
PLACEMENT_NOTE=Place close to J3401.
C3431 0.1uF
C3430 0.1uF
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N
AIRPORT
CRITICAL
L3401
90-OHM-100MA
DLP11S
PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_O_L
PCIE_WAKE_L
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
1000 mA peak
750 mA nominal max
PP5V_WLAN
L3404
FERR-120-OHM-1.5A
0402-LF
C3422 0.1uF
C3421 0.1uF
C3420 10UF
PP5V_WLAN_F
CRITICAL
Q3450
TPCP8102
23V1K-SM
C3450 0.1UF
C3451 0.033UF
R3450 100K
R3451 10K
P5VWLAN_SS
=PP5V_S3_WLAN
PM_WLAN_EN_L
ALS
CAMERA
BLUETOOTH
=PP5V_S3_BTCAMERA_F
=I2C_ALS_SDA
=I2C_ALS_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N
CRITICAL
L3402
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
CRITICAL
L3403
90-OHM
DLP0NS
USB_BT_P
USB_BT_N
275 mA peak
206 mA nominal max
L3405
FERR-120-OHM-1.5A
0402-LF
C3452 0.1uF
=PP5V_S3_BTCAMERA
=PP3V3_S3_WLAN
MINI_RESET_CONN_L
U3401
TC7SZ08AFEAPE
SOT665
WLAN_SMIT_BUF
U3402
74LVC1G17DRL
SOT-553
C3453 1UF
R3453 33K
R3454 62K
R3455 1
WLAN_SMIT_RC
WLAN_SMIT_DISCHRG
Q3455
SSM3K15FV
SOD-VESM-HF
MINI_RESET_L
Right Clutch Connector
SYNC_MASTER=YITE
SYNC_DATE=04/22/2008
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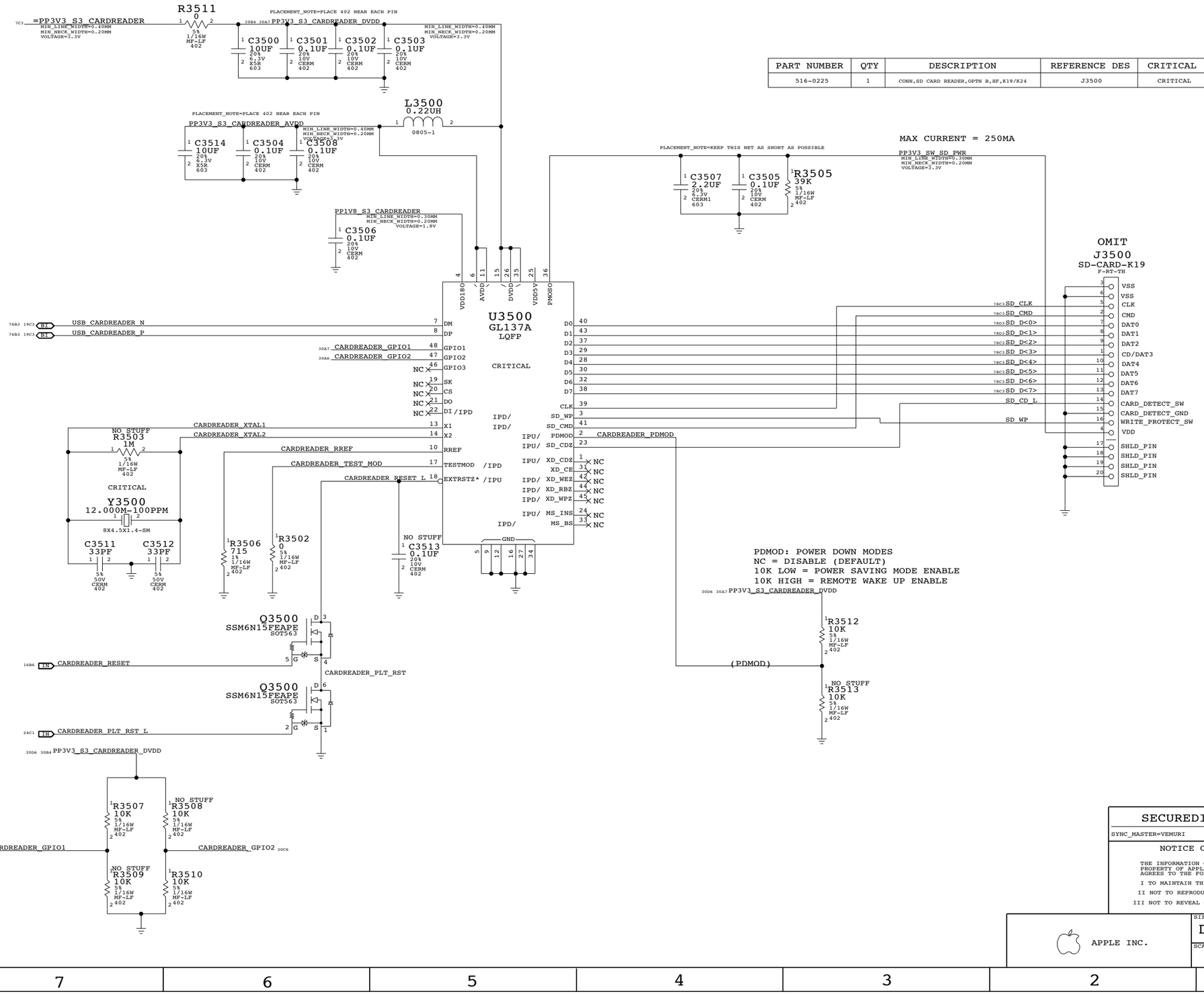
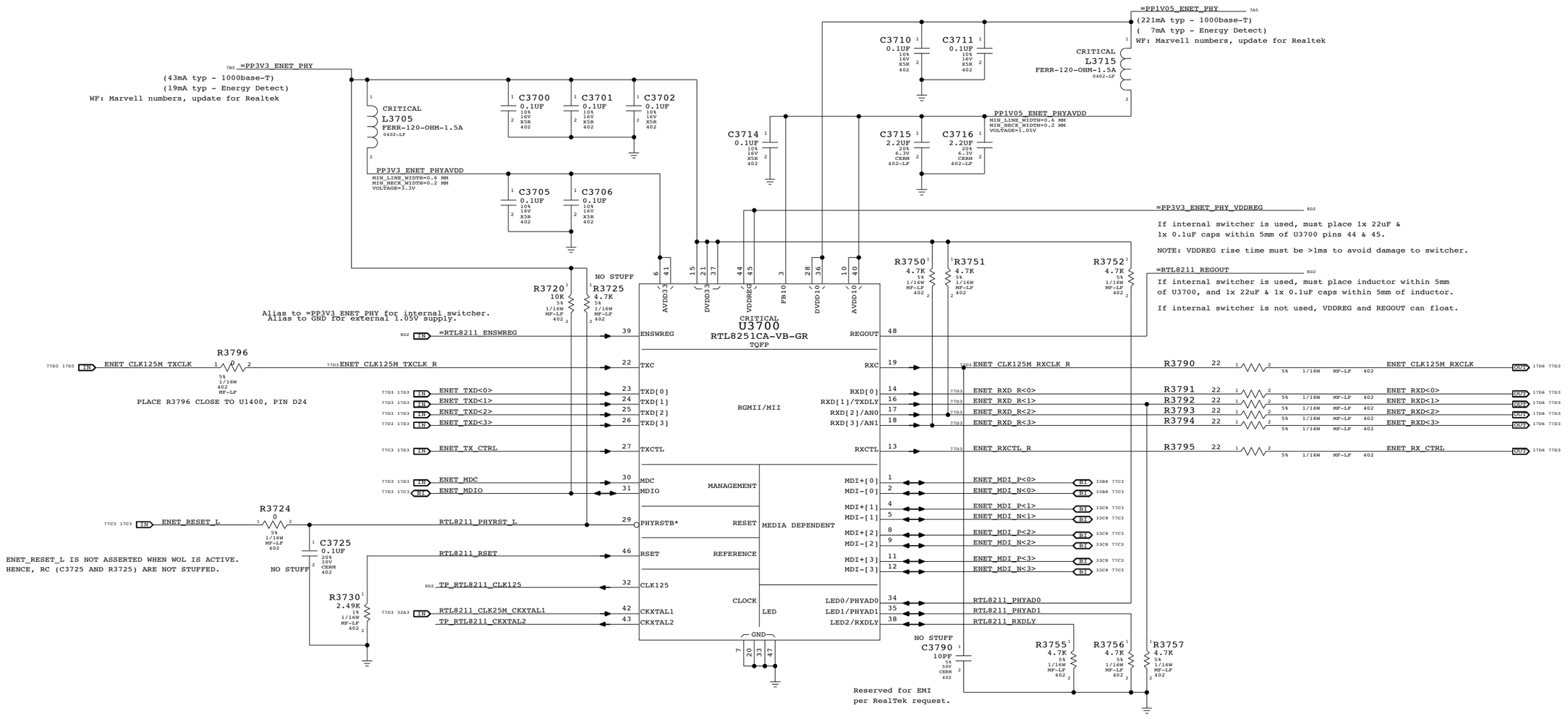
SIZE D
DRAWING NUMBER 051-7898
REV. 4.7.0
SCALE NONE
SHT 29 OF 81

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,R19/K24	J3500	CRITICAL	





Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

APPLE INC.

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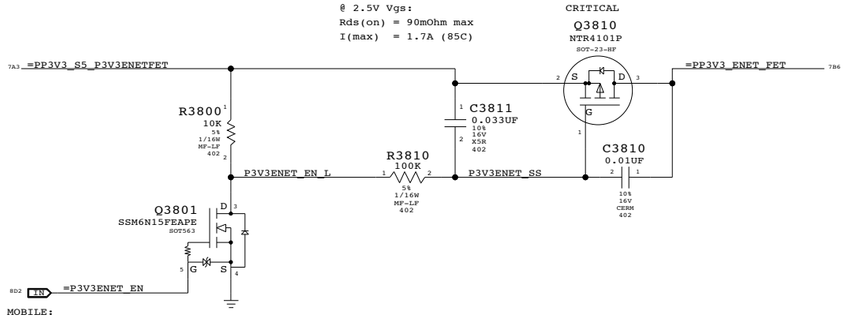
3.3V ENET FET



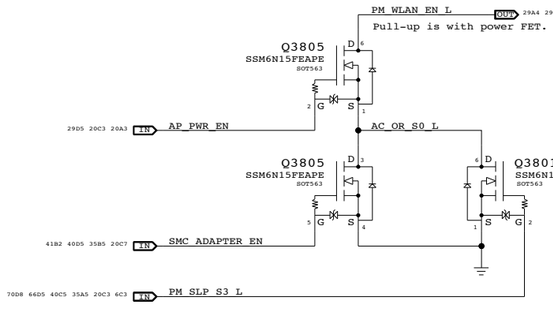
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

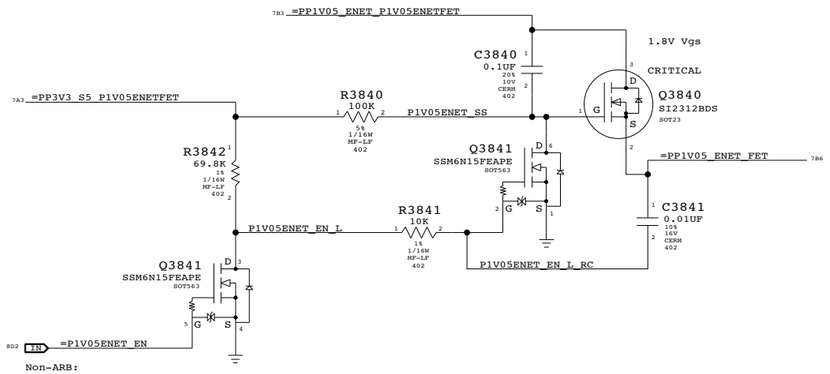
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

Ethernet & AirPort Support

SYNC_MASTER=SUMA SYNC_DATE=07/01/2008

APPLE INC.

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- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TX
RX
TLA-6T213HF

CRITICAL
T3902
SM
TX
RX
TLA-6T213HF

77C3 31B3 BI ENET_MDI_P<1>
77C3 31B3 BI ENET_MDI_N<1>
77C3 31B3 BI ENET_MDI_P<3>
77C3 31B3 BI ENET_MDI_N<3>
77C3 31B3 BI ENET_MDI_N<2>
77C3 31B3 BI ENET_MDI_P<2>
77C3 31B3 BI ENET_MDI_N<0>
77C3 31B3 BI ENET_MDI_P<0>

77C3 ENET_MDI_TRAN_P<1>
77C3 ENET_MDI_TRAN_N<1>
77C3 ENET_MDI_TRAN_P<3>
77C3 ENET_MDI_TRAN_N<3>
77C3 ENET_MDI_TRAN_N<2>
77C3 ENET_MDI_TRAN_P<2>
77C3 ENET_MDI_TRAN_N<0>
77C3 ENET_MDI_TRAN_P<0>

ENET_CENTER_TAP<1> R3903 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<3> R3902 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<2> R3901 75 1% 1/16W MF-LF 402
ENET_CENTER_TAP<0> R3900 75 1% 1/16W MF-LF 402

C3911 10PF 5% 50V CERM 402-1 CRITICAL
C3912 10PF 5% 50V CERM 402-1 CRITICAL
C3913 10PF 5% 50V CERM 402-1 CRITICAL
C3914 10PF 5% 50V CERM 402-1 CRITICAL
C3915 10PF 5% 50V CERM 402-1 CRITICAL
C3916 10PF 5% 50V CERM 402-1 CRITICAL
C3917 10PF 5% 50V CERM 402-1 CRITICAL
C3918 10PF 5% 50V CERM 402-1 CRITICAL

PLACEMENT_NOTE=PLACE C3911-C3918 ON MDI LINES WITHOUT ANY STUBS

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.65MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH

514-0636

ETHERNET CONNECTOR

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

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APPLE INC.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	

OMIT
R4100
0
5%
1/16W
MF-LF
402

=PP1V0_FW_FWPHY
135 mA
=PP1V0_FW_R

L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

=PP3V3_FW_FWPHY
138 mA
7B1 34B1 35D8 36B6 36D5

114 mA FireWire PHY
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4130
120-OHM-0.3A-EMI
0402-LF

17 mA PCIe SerDes
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
L4135
120-OHM-0.3A-EMI
0402-LF

0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

CRITICAL
U4100
FW643E
BGA

PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
C4170 0.1UF 20% 16V X5R 402 PCIE_FW_R2D_C_N (IN 16B3 75D3)
C4171 0.1UF 20% 16V X5R 402 PCIE_FW_R2D_C_P (IN 16B3 75D3)
C4175 0.1UF 20% 16V X5R 402 PCIE_FW_D2R_N (OUT 16B6 75D3)
C4176 0.1UF 20% 16V X5R 402 PCIE_FW_D2R_P (OUT 16B6 75D3)
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

NC ATBUSB
NC ATBUSH
NC ATBUSN
=FW_PHY_DS0 (IN) DS0 (IPD) NT-19
=FW_PHY_DS1 (IN) DS1 (IPD) NT-20
=FW_PHY_DS2 (IN) DS2 (IPD) NT-21

PCI EXPRESS PHY
PCIE_RXD0N 75D3 PCIE_FW_R2D_N
PCIE_RXD0P 75D3 PCIE_FW_R2D_P
PCIE_TXD0N 75D3 PCIE_FW_D2R_C_N
PCIE_TXD0P 75D3 PCIE_FW_D2R_C_P
REFCLKN PCIE_CLK100M_FW_N (IN 16C3)
REFCLKP PCIE_CLK100M_FW_P (IN 16C3)

1394 PHY
FW_P0_TPA_N TPA0N
FW_P0_TPA_P TPA0P
FW_P1_TPA_N TPA1N
FW_P1_TPA_P TPA1P
FW_P2_TPA_N TPA2N
FW_P2_TPA_P TPA2P
FW_P0_TPB_N TPB0N
FW_P0_TPB_P TPB0P
FW_P1_TPB_N TPB1N
FW_P1_TPB_P TPB1P
FW_P2_TPB_N TPB2N
FW_P2_TPB_P TPB2P
FW_P0_TPBIAS TPBIAS0
FW_P1_TPBIAS TPBIAS1
FW_P2_TPBIAS TPBIAS2
FW643_R0 R0
FW643_TPCPS TPCPS

TEST CONTROLLER
NT-4 (IPU) TCK TP_FW643_TCK
NT-3 (IPU) TDI TP_FW643_TDI
(IPU) TDO TP_FW643_TDO
NT-1 (IPU) TMS TP_FW643_TMS
NT-2 (IPU) TRST* FW643_TRST_L

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* =FW_PME_L (OUT 8C2 35C8)
REGCLT FW643_REGCTL
NT-12 (IPD) VAUX_DETECT FW643_VAUX_DETECT
NT-13 VAUX_DISABLE TP_FW643_VAUX_ENABLE
(OD) CLKREQN =FW_CLKREQ_L (OUT 35C4)

SCIF
NT-16 (IPD) SCIFCLK TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN TP_FW643_SCIFDAIN
NT-17 SCIFDOUT TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL FW643_SCL
NT-6 SDA TP_FW643_SDA

CHIP RESET
NT-5 PERST* FW_RESET_L (IN 35C1)

FW643_LDO
=PP3V3_FW_FWPHY 7B1 34D2 35D8 36B6 36D5
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

=PPVP_FW_PHY_CPS
R4160 200K 1% 1/16W MF-LF 402

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
R4150 412 1% 1/16W MF-LF 402
CRITICAL
Y4150
24.576MHZ
8M-3.2X2.5MM
NC
NC
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

FW_CLK24P576M_XO_R
FW_CLK24P576M_XI
NAND_TREE NT-OUT
REXT
XO
XI NT-9
NOTE: NT-xx notes show NAND tree order.

TP_FW643_NAND_TREE
FW643_REXT
TP_FW643_SE SE (IPD)
TP_FW643_SM SM (IPD)
TP_FW643_MODE_A MODE_A (IPD) NT-18
TP_FW643_CE CE (IPD)
TP_FW643_FW620_L FW620* (IPU)
TP_FW643_JASI_EN JASI_EN (IPD) NT-11
TP_FW643_AVREG AVREG
TP_FW643_VBUF VBUF
FW643_PU_RST_L FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL OCR_CTL_V10
OCR_CTL_V12 (Reserved)

MISCELLANEOUS

VSS VREG_VSS

FireWire LLC/PHY (FW643)

SYNC_MASTER=K19_MLB SYNC_DATE=11/02/2008

APPLE INC.

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Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

=PP3V3_S0_P3V3FWFET
R4290 10K 5% 1/16W MF-LF 402
C4290 0.033UF 10% 16V X5R 402
CRITICAL Q4291 NTR4101P SOT-23-HF
=PP3V3_FW_FET
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
P3V3FW_SS
C4291 0.01UF 10% 16V CERM 402
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN

1.05V FW FET

=PP1V05_FW_P1V05FWFET
C4296 0.1UF 20% 10V CERM 402
=PP3V3_S0_P1V05FWFET
R4297 220K 5% 1/16W MF-LF 402
CRITICAL Q4295 SI2312BDS SOT23
P1V05FW_SS
Q4293 SSM6N15FEAPE SOT563
=PP1V0_FW_FET
=PP3V3_S5_P1V05FWFET
R4295 10K 5% 1/16W MF-LF 402
C4295 0.068UF 10% 10V CERM 402
R4296 100K 5% 1/16W MF-LF 402
P1V05_FW_EN_L
P1V05_FW_EN_L_RC
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

FireWire Port Power Switch

=PP3V3_FW_FWPHY
FWPHY_WAKE_YES
R4276 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
R4277 10K 5% 1/16W MF-LF 402
FW_WAKE
CRITICAL Q4276 DMB53D0UV SOT-563
FWPHY_WAKE_YES
=FW_PME_L
CRITICAL Q4276 DMB53D0UV SOT-563
FWPHY_WAKE_YES

PCIE_FW_PRSNT_L
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

=PP3V3_S0_FWPWRCTL
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 5% 1/16W MF-LF 402
=PP1V0_FW_FWPHY
P1V0_FW_RC
C4281 1UF 10% 6.3V CERM 402
CRITICAL Q4299 DMB53D0UV SOT-563
P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
=FW_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

Late-VG Event Detection

=PP3V3_FW_LATEVG_ACTIVE
PP2V4_FW_LATEVG
R4211 10K 1% 1/16W MF-LF 402
R4212 10K 1% 1/16W MF-LF 402
C4210 0.1UF 20% 10V CERM 402
FWLATEGV_3V_REF
U4210 LMC7211 SM-HF
LATEVG_EVENT
P2V4_FWLATEVG_RC
C4211 100PF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402

FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off

NOSTUFF
R4265 10K 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
R4263 100 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
C4263 1UF 10% 10V X5R 402
NOSTUFF
CRITICAL Q4262 DMB54D0UV SOT-563

=PPBUS_S5_FWPWRSW
CRITICAL Q4260 FDC638P_G SM
R4260 300K 5% 1/16W MF-LF 402
C4260 0.1UF 10% 25V X5R 402
FWPWR_EN_L_DIV
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SH CRS08-1.5A-30V
=PPBUS_S5_FW_FET

R4261 470K 5% 1/16W MF-LF 402
FWPWR_EN_L
Q4261 2N7002DW-X-G SOT-363
SMC_ADAPTER_EN
Q4261 2N7002DW-X-G SOT-363
PM_SLP_S3_L
Enables port power when machine is running or on AC.

=PP1V05_FWPWRCTL
R4275 1K 5% 1/16W MF-LF 402
FW_PWR_EN_L
R4270 330K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
FW_DET_MIRROR
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
CRITICAL Q4270 BC847CDXV6TXG SOT563
FW_P1_TPBIAS_R
FW_DET_EMIT
R4272 1K 5% 1/16W MF-LF 402
R4273 12K 5% 1/16W MF-LF 402
=PP3V3_S0_FWPWRCTL
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
CRITICAL Q4275 DMB53D0UV SOT-563
C4270 0.1UF 10% 16V X5R 402
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

FireWire Port Power

SYNC_MASTER=YUN_K19_MLB
SYNC_DATE=12/22/2008

APPLE INC.

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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

36B6 35D8 34D2 34B1 7B1 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE — =FW_PHY_DS0 34C6

FWPHY_DS2 MAKE_BASE=TRUE — =FW_PHY_DS2 34C6

FWPHY_DS1 MAKE_BASE=TRUE — =FW_PHY_DS1 34C6

R4381 10K 1% 1/16W MF-LF 402

34B6 FW_P0_TPBIAS — NC_FW0_TPBIAS MAKE_BASE=TRUE

34B6 FW_P2_TPBIAS — NC_FW2_TPBIAS MAKE_BASE=TRUE

78D3 34C6 FW_P0_TPA_N — NC_FW0_TPAN MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPA_P — NC_FW0_TPAP MAKE_BASE=TRUE

34B6 FW_P2_TPA_N — NC_FW2_TPAN MAKE_BASE=TRUE

34B6 FW_P2_TPA_P — NC_FW2_TPAP MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPB_N — NC_FW0_TPBN MAKE_BASE=TRUE

78D3 34B6 FW_P0_TPB_P — NC_FW0_TPBP MAKE_BASE=TRUE

34B6 FW_P2_TPB_N — NC_FW2_TPBN MAKE_BASE=TRUE

34B6 FW_P2_TPB_P — NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

35A4 34B6 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 6.3V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

78D3 34B6 FW_P1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE — 36B5

78D3 34B6 FW_P1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE — 36B5

78D3 34B6 FW_P1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE — 36B5

78D3 34B6 FW_P1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE — 36B5

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 5% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

7B1 =PPVP_FW_PHY_CPS_FET

R4311 470K 5% 1/16W MF-LF 402

Q4300 BSS8402DW SOT-363 (SYM-VER1)

PPVP_FW_CPS MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=12.6V — MAKE_BASE=TRUE — =PPVP_FW_PHY_CPS 34B7

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

Q4300 BSS8402DW SOT-363 (SYM-VER1)

=PP3V3_FW_FWPHY

"Snapback" & "Late VG" Protection

36A5 35A8 PP2V4_FW_LATEVG

DP4310 BAV99DW-X-G SOT-363 CRITICAL

C4311 0.01uF 10% 50V X7R 402

DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 50V X7R 402

36B7 FW_PORT1_TPB_N

36B7 FW_PORT1_TPB_P

36B7 FW_PORT1_TPA_N

36B7 FW_PORT1_TPA_P

DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 50V X7R 402

CRITICAL DP4311 BAV99DW-X-G SOT-363

C4313 0.01uF 10% 50V X7R 402

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

7B1 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM 8M

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

TPB- TPB(R) TPB+ VP VG NC/NC TPA- TPA<R> TPA+ TPA(R) CHASSIS GND

OUTPUT

INPUT

514S0605

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

Late-VG Protection Power

7A3 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V — 35A8 36C5

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

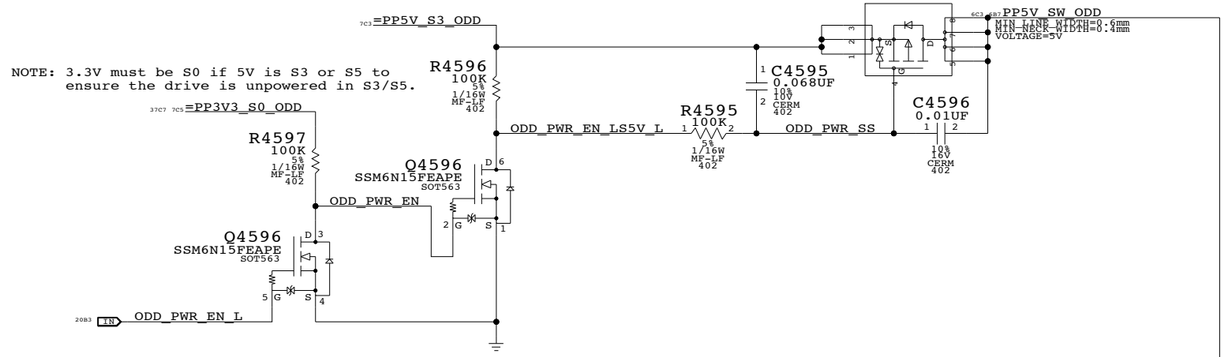
FireWire Ports

SYNC_MASTER=K19_MLB — SYNC_DATE=11/02/2008

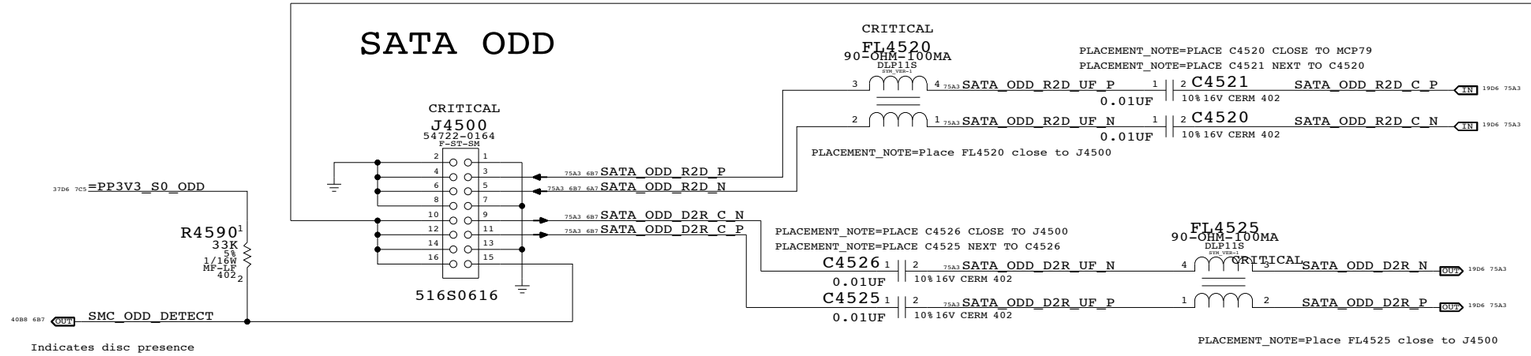
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 36 OF 81	

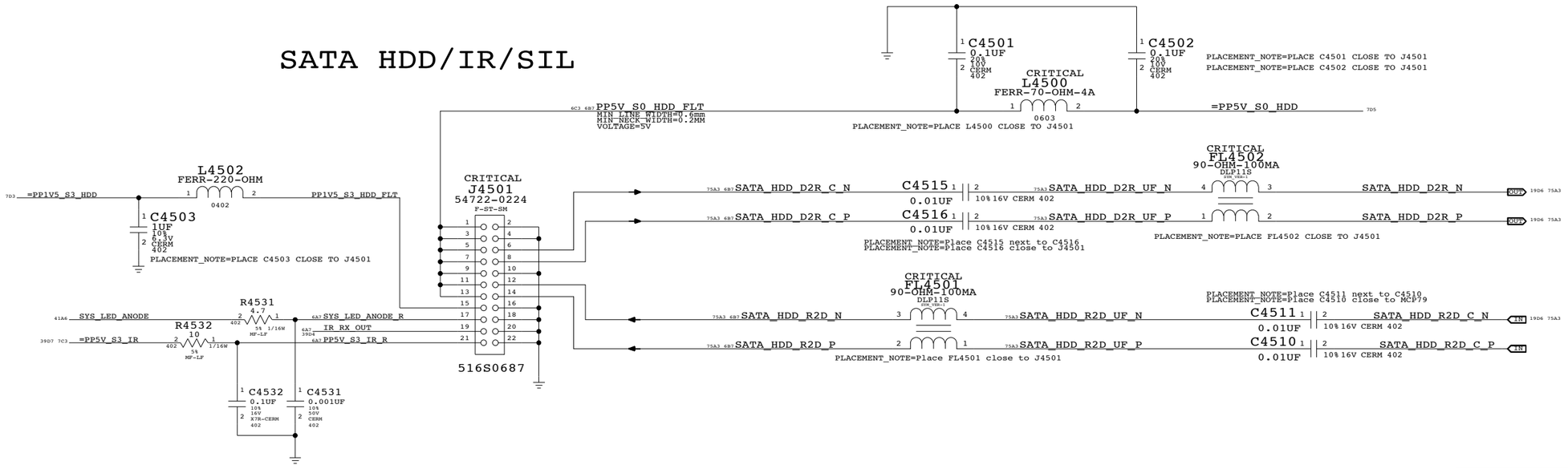
ODD Power Control



SATA ODD



SATA HDD/IR/SIL



SATA Connectors

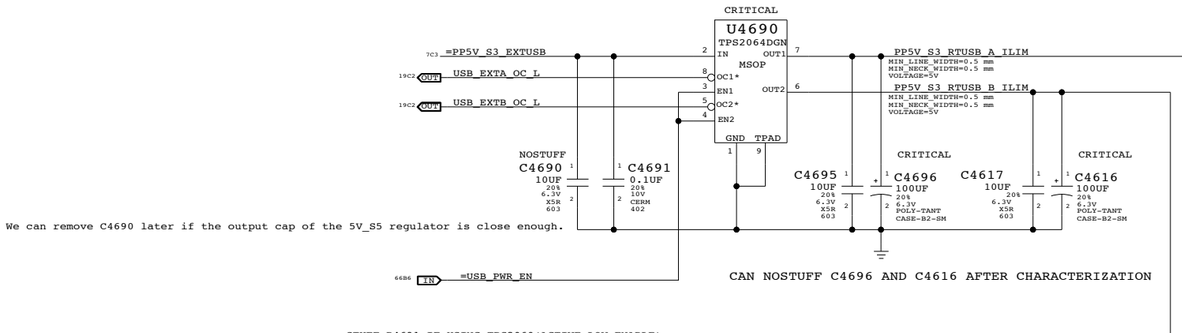
SYNC_MASTER=K19_MLB SYNC_DATE=12/04/2008

APPLE INC.

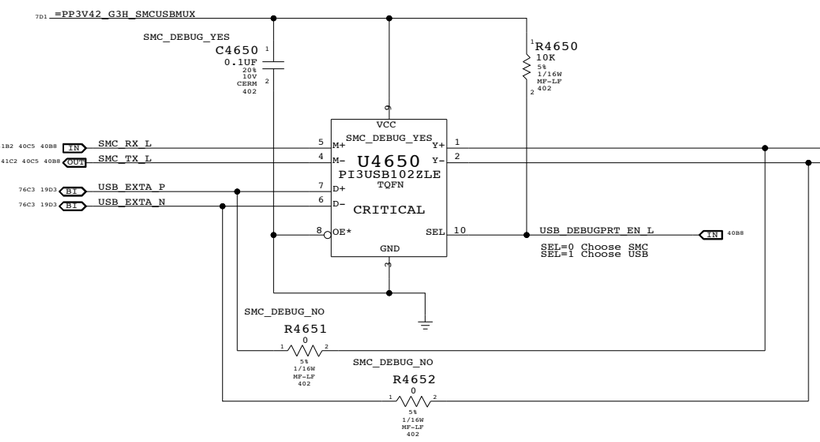
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE	SHT	OF
NONE	37	81

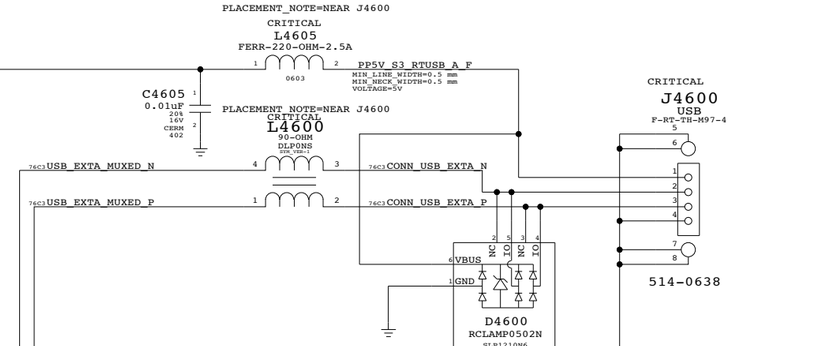
Port Power Switch



USB/SMC Debug Mux



USB PORT A (FRONT PORT)



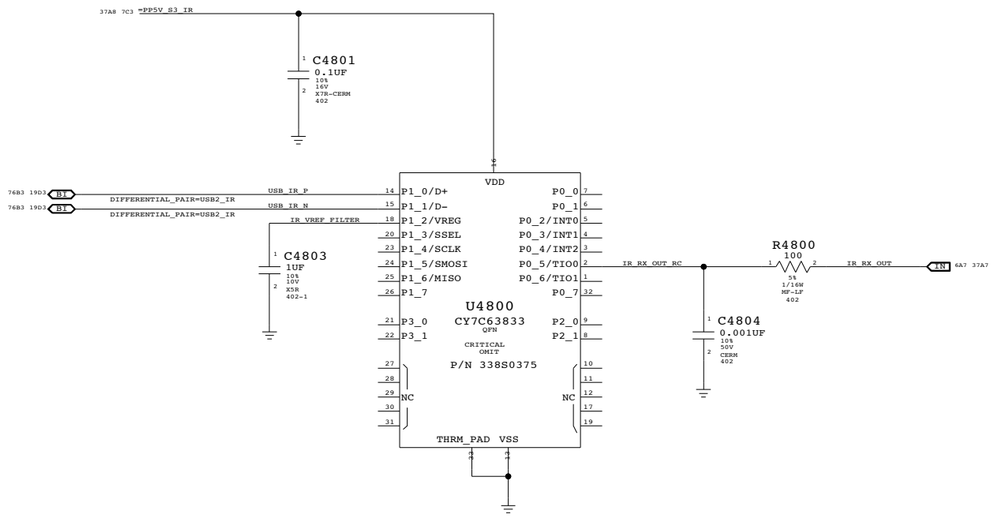
USB PORT B (BACK PORT)

External USB Connectors

SYNC_MASTER=YUAN.MA SYNC_DATE=01/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 38 OF 81	



CYPRESS 'ENCORE II' USB CONTROLLER

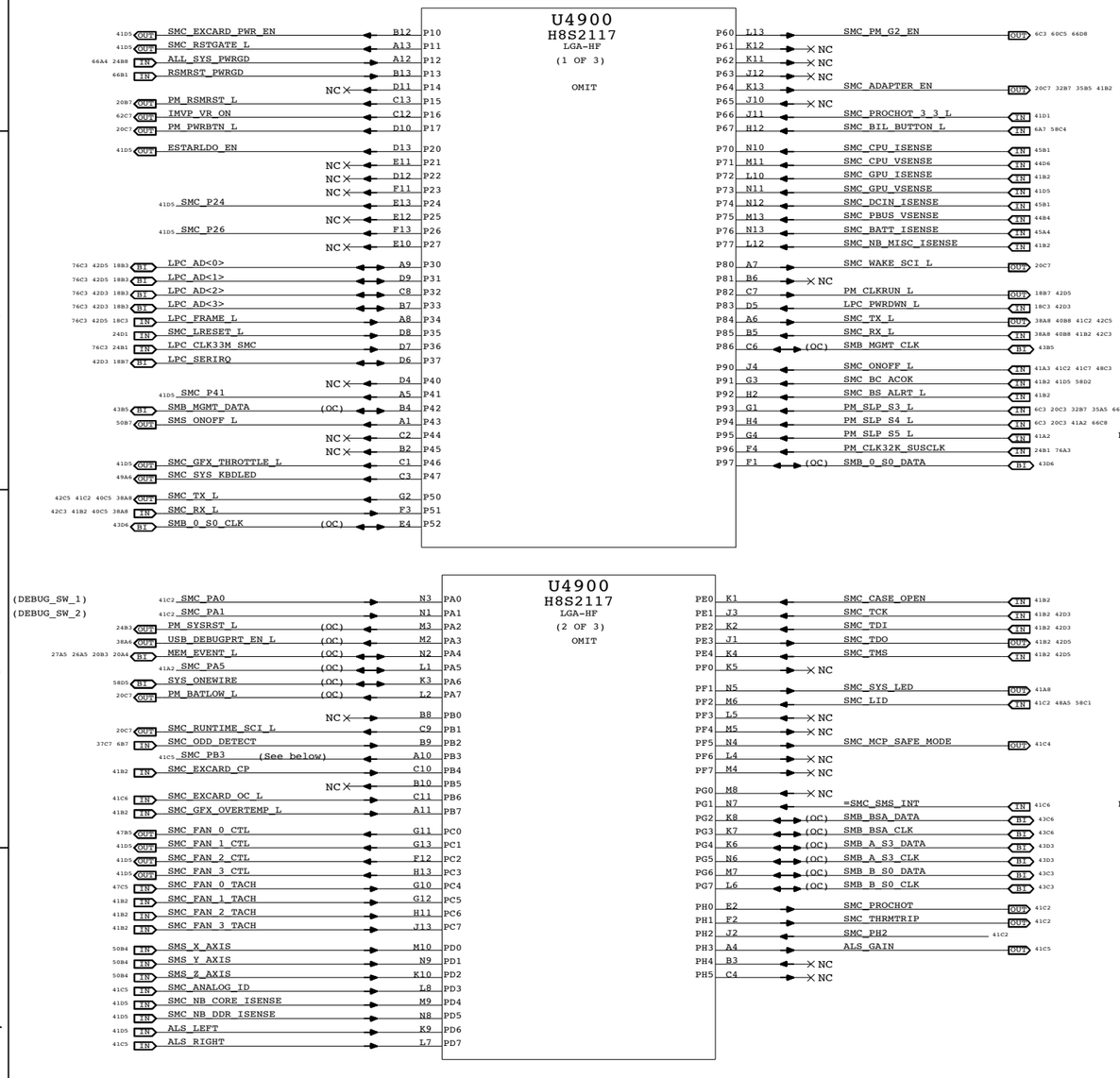
Front Flex Support

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

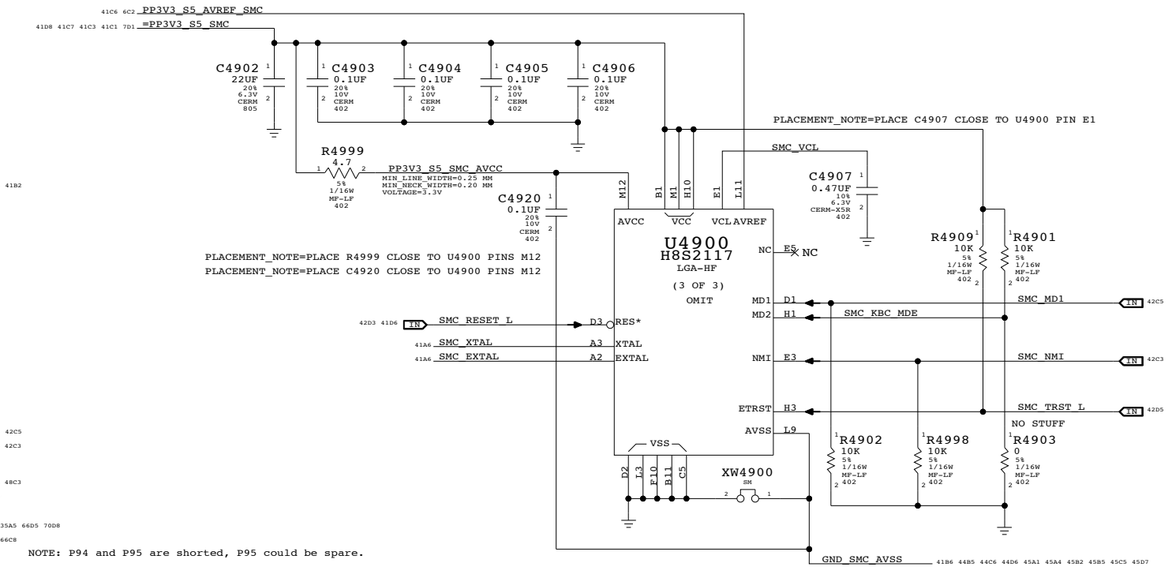
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE	SHT	OF
NONE	39	81

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

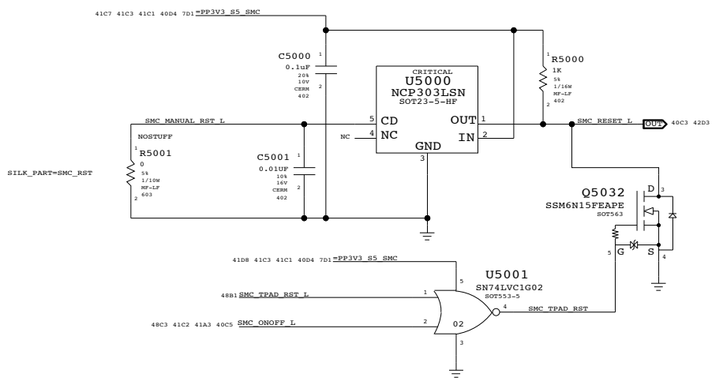
SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

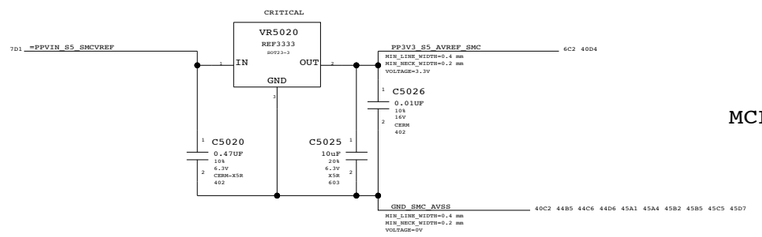
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 40 OF 81	

SMC Reset "Button" / Brownout Detect

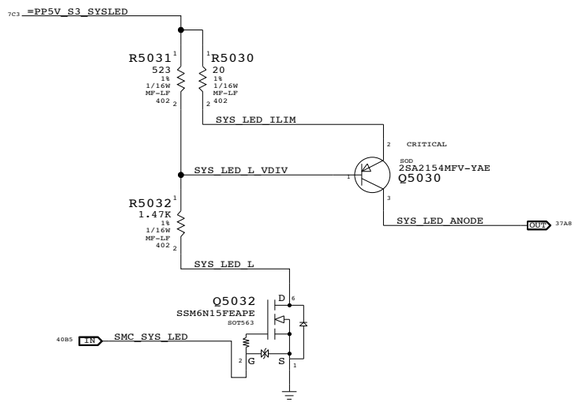


SMC AVREF Supply

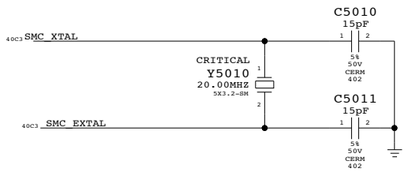


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	ISL60002-33, INTERSIL

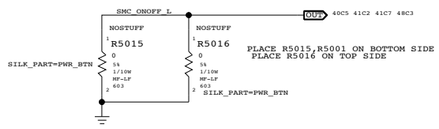
System (Sleep) LED Circuit



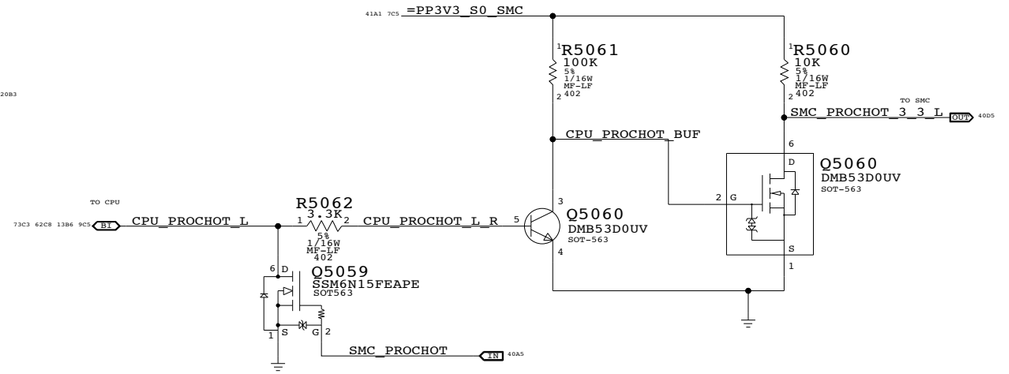
SMC Crystal Circuit

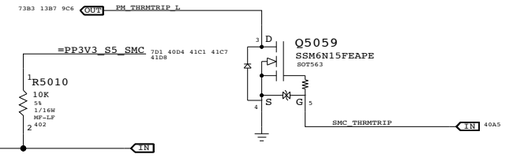


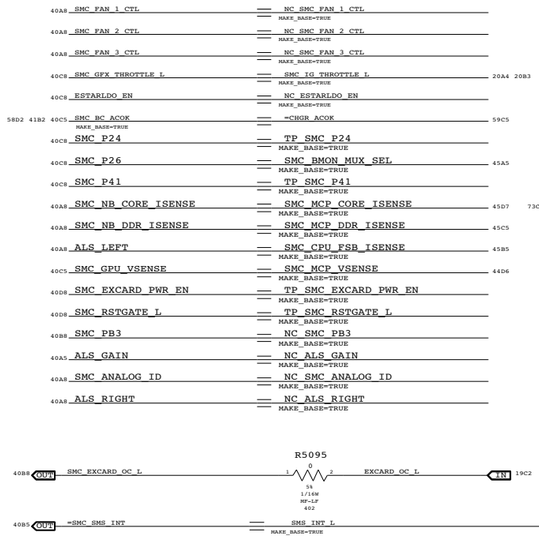
Debug Power "Button"



SMC FSB to 3.3V Level Shifting

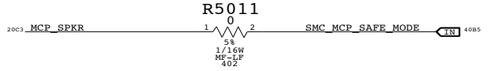


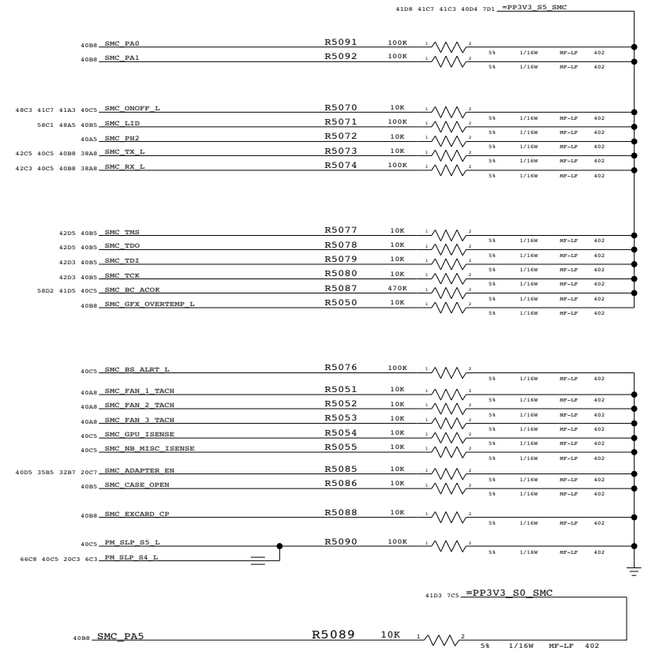




MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345



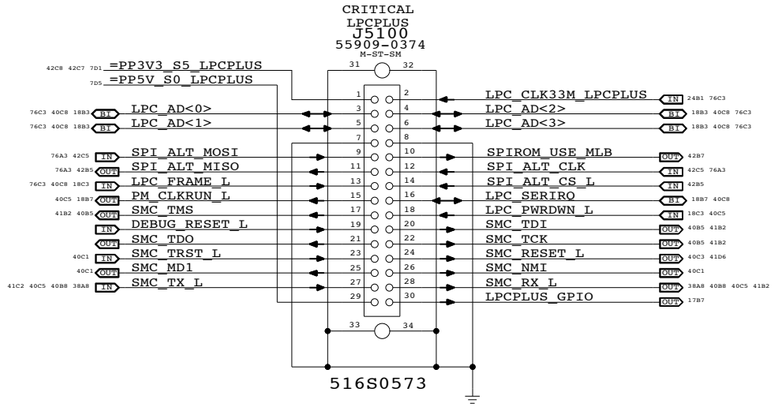


SMC Support	
SYNC_MASTER=YUAN.MA	SYNC_DATE=05/28/2008

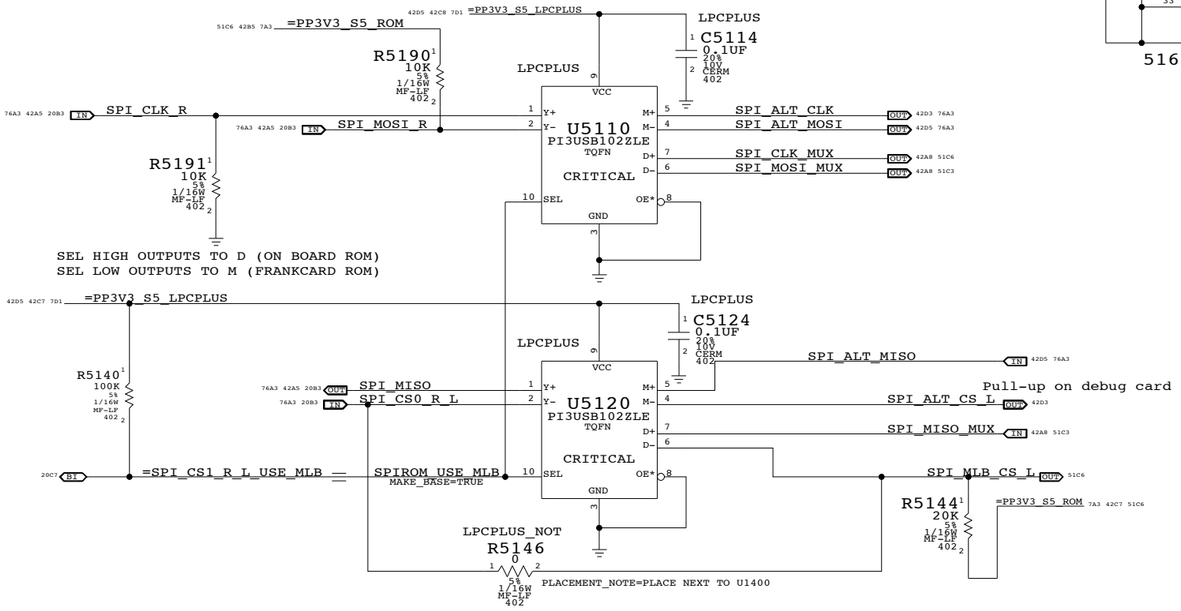
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 41 OF 81	

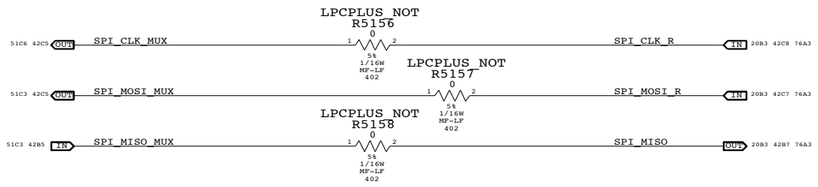
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



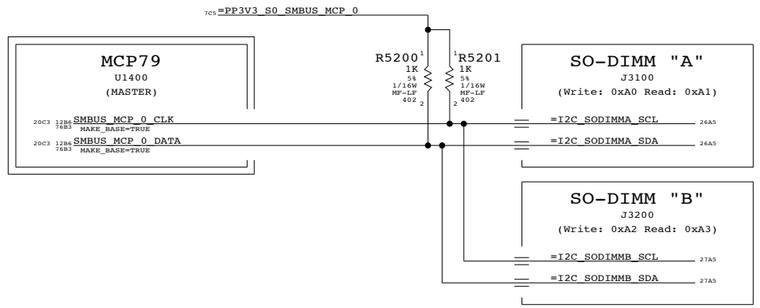
LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

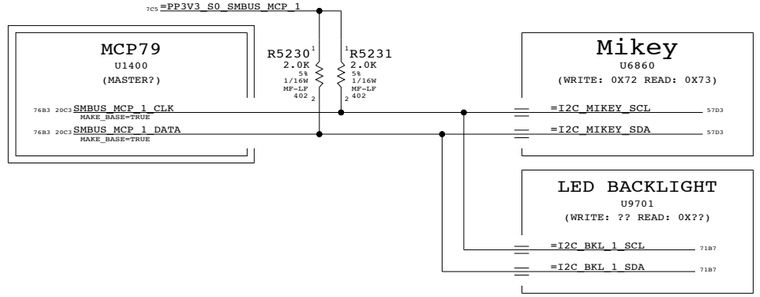
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 42 OF 81	

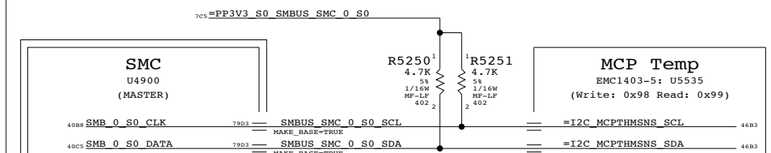
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

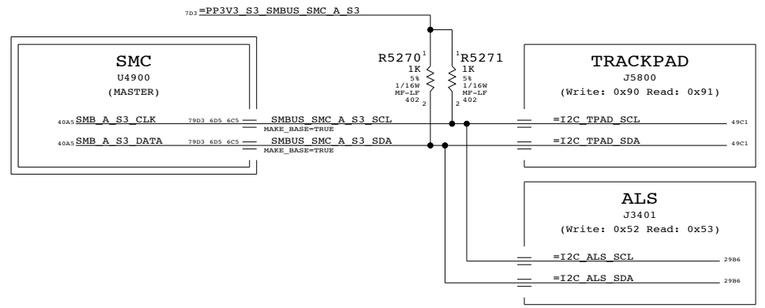


SMC "0" SMBus Connections

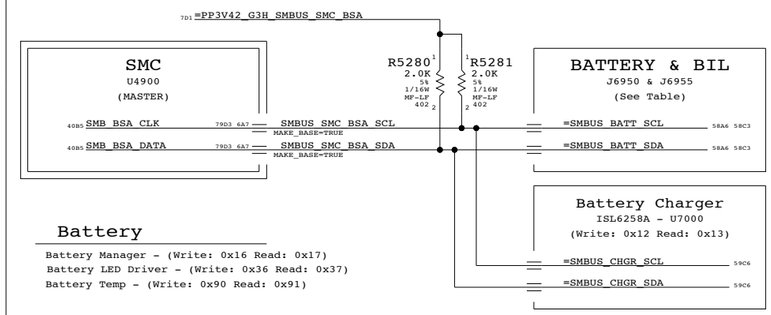


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



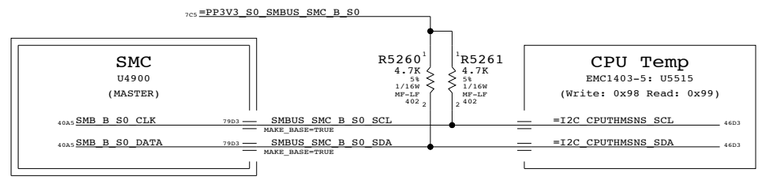
SMC "Battery A" SMBus Connections



Battery

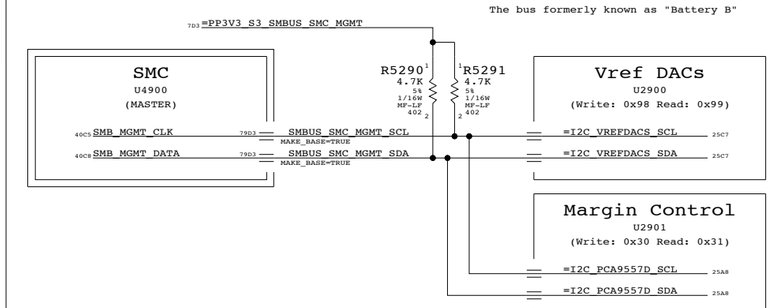
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



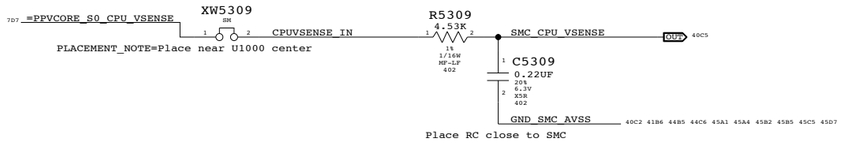
K24 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=04/21/2008

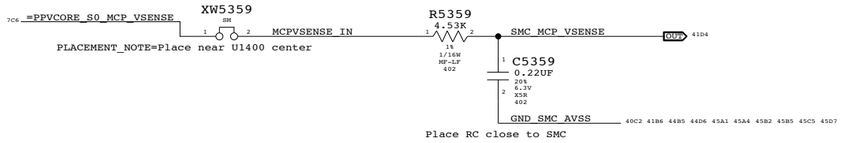
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 43 OF 81	

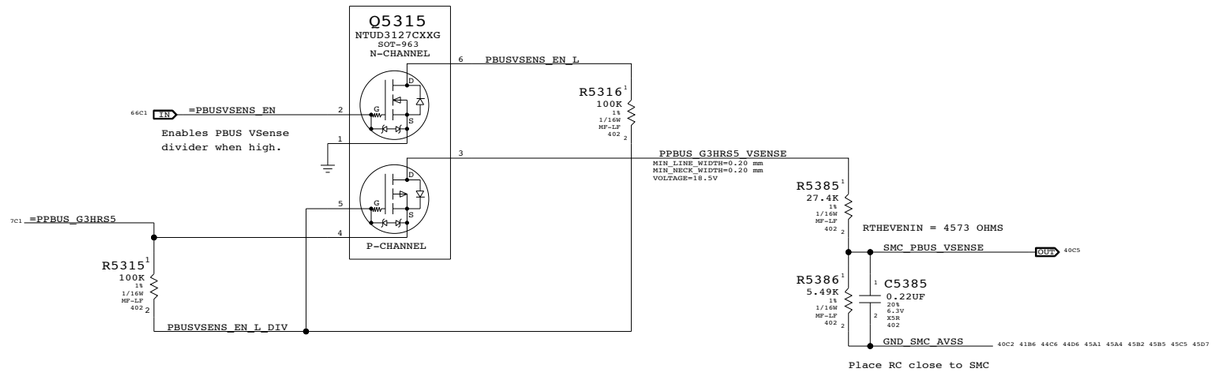
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



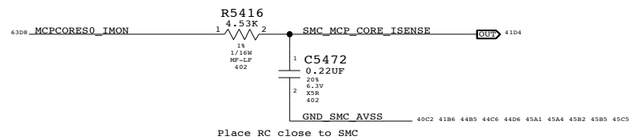
VOLTAGE SENSING

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

APPLE INC.

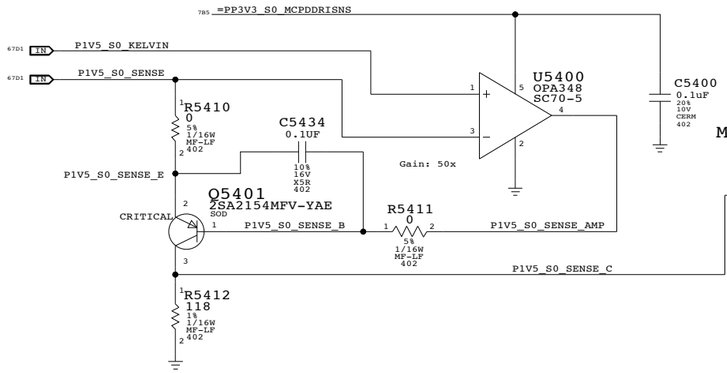
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 44 OF 81	

MCP VCore Current Sense Filter

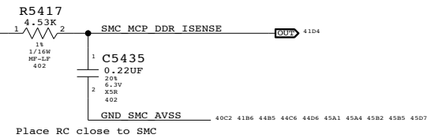


Place RC close to SMC

MCP MEM VDD Current Sense

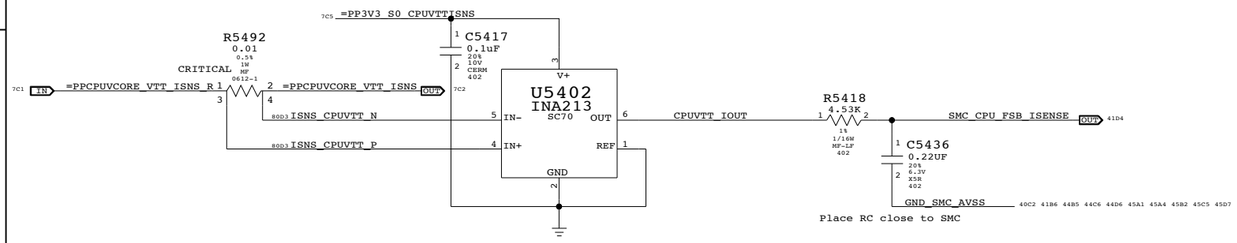


MCP MEM VDD Current Sense Filter



Place RC close to SMC

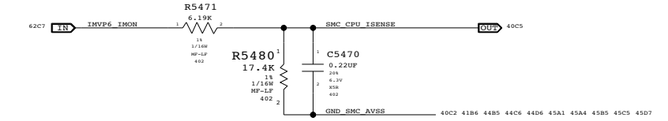
CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE



Place RC close to SMC

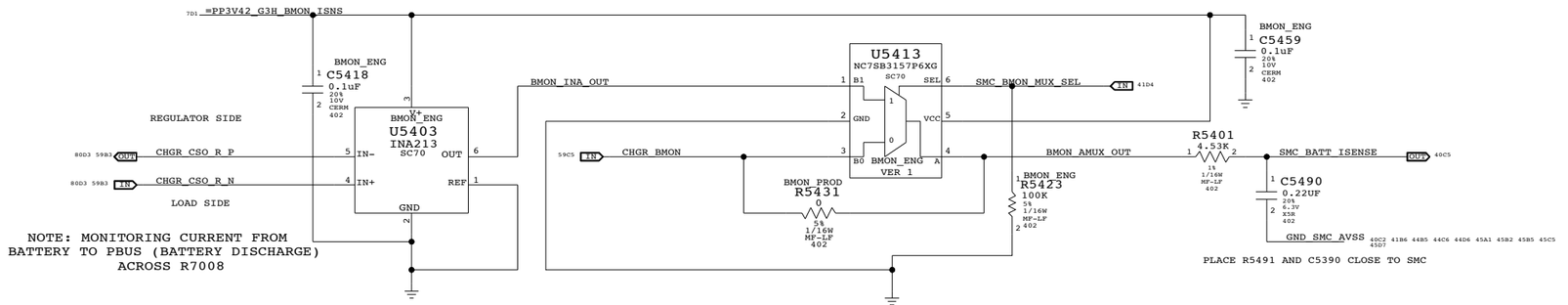
CPU VCore Load Side Current Sense / Filter

Place RC close to SMC



BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)



NOTE: MONITORING CURRENT FROM BATTERY TO PBUS (BATTERY DISCHARGE) ACROSS R7008

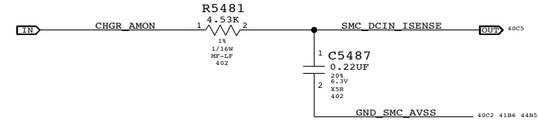
INA213 has gain of 50V/V

PLACE U5403 AND C5418 NEAR R7008

For engineering, stuff U5313 and unstuff R5330
For production, stuff R5330 and unstuff U5313

PLACE R5491 AND C5390 CLOSE TO SMC

DC-IN (AMON) CURRENT SENSE



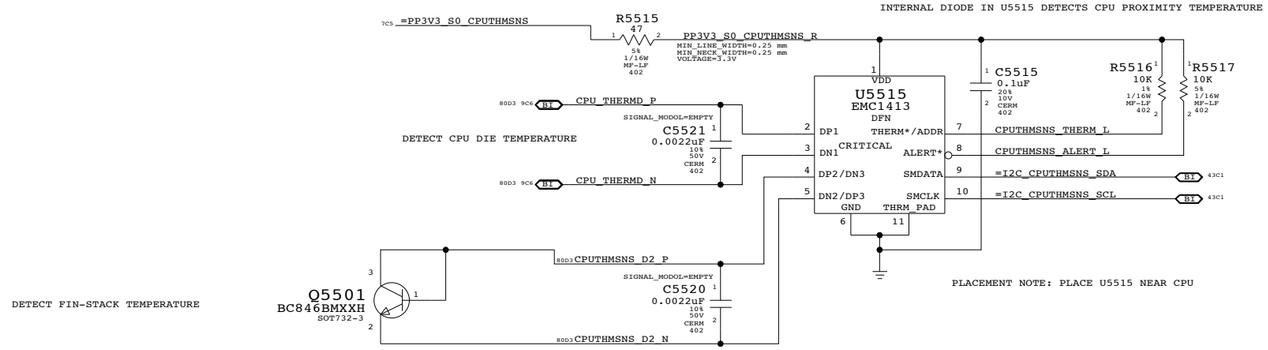
Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=12/17/2008

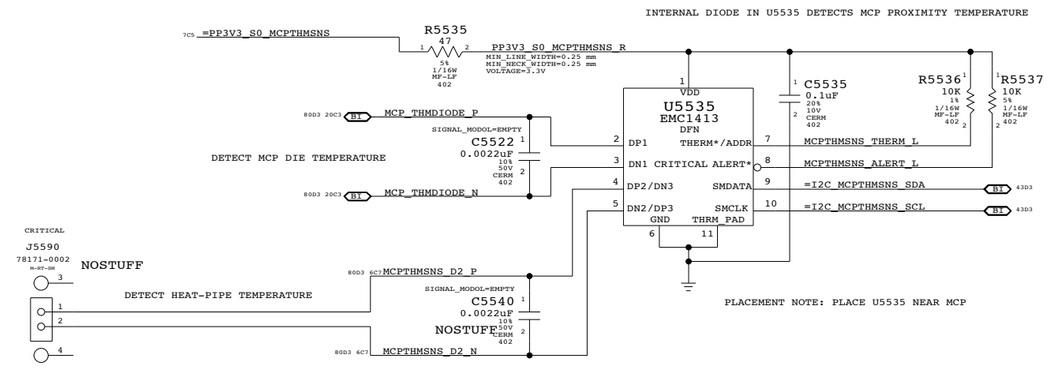
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 45 OF 81	

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



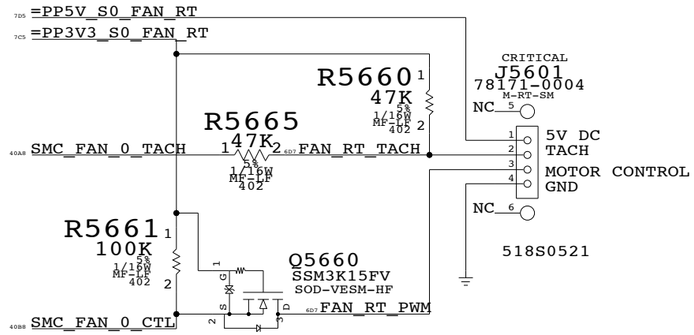
REPLACED 518S0521 WITH 518S0519

Thermal Sensors

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 46 OF 81	



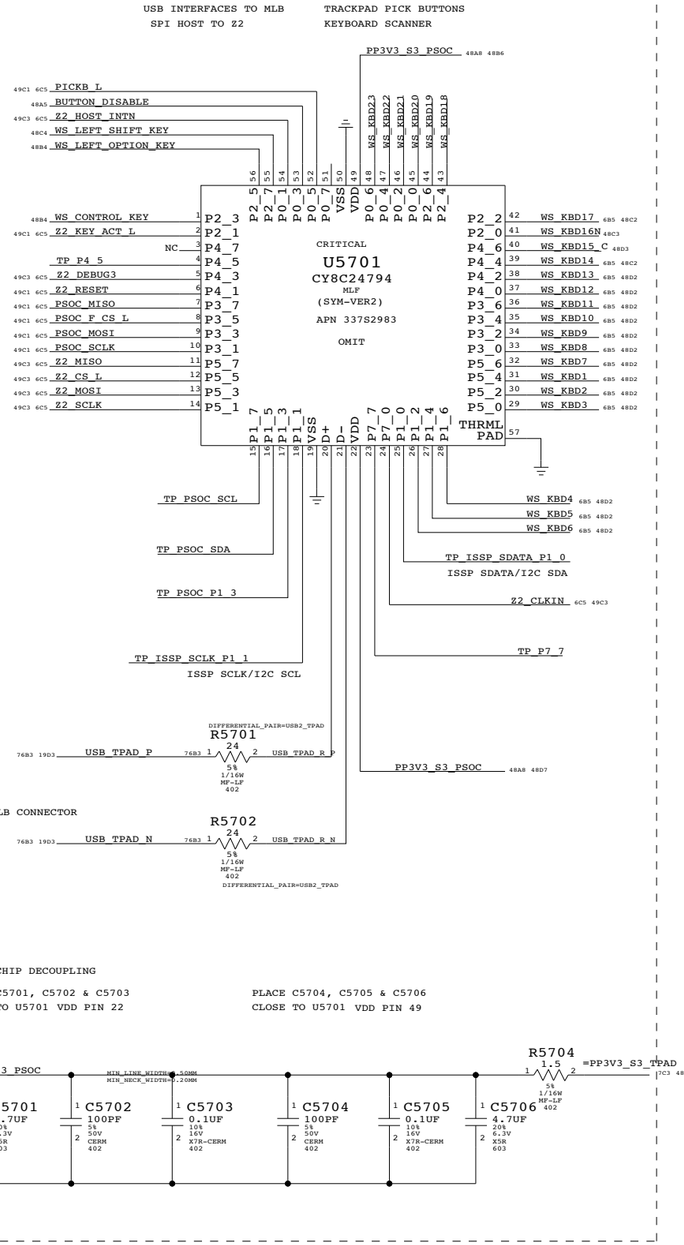
Fan

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE	SHT	OF
NONE	47	81

PSOC USB CONTROLLER



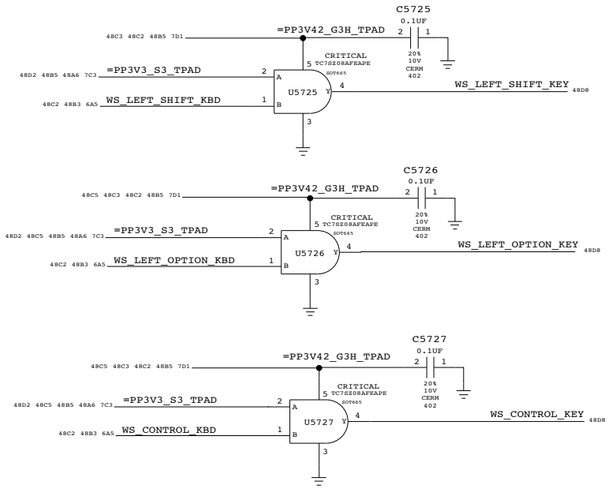
U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

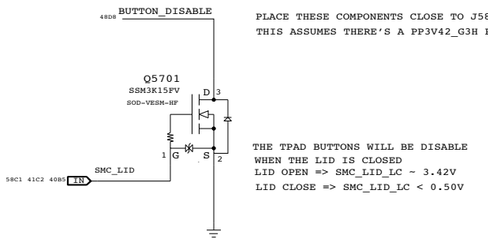
PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

ISOLATION CIRCUIT



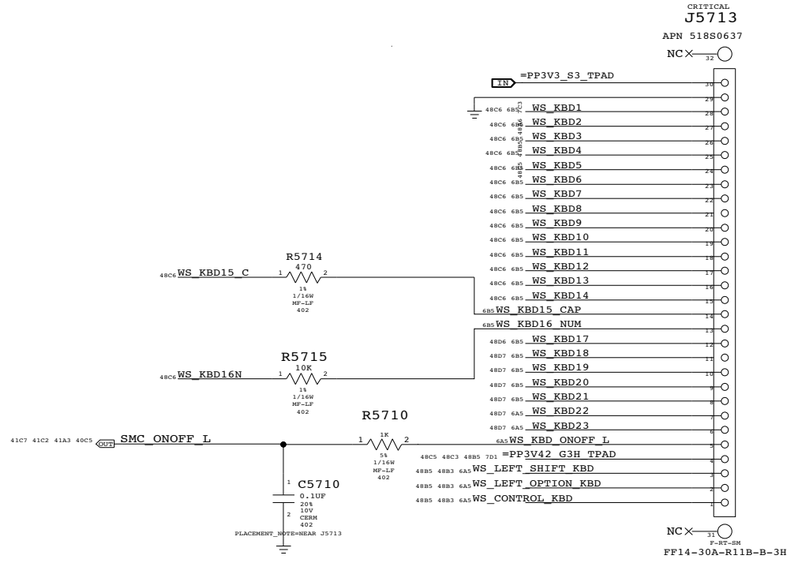
TPAD BUTTONS DISABLE



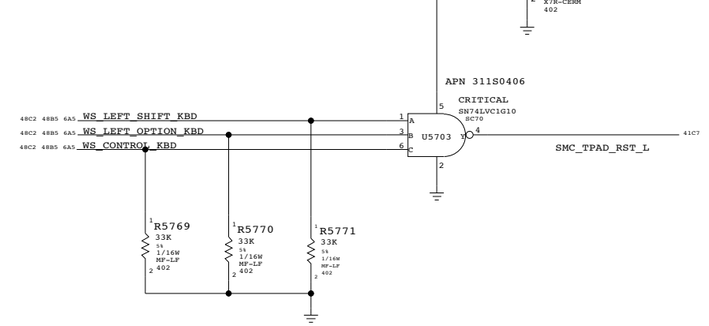
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

WELLSPRING 1

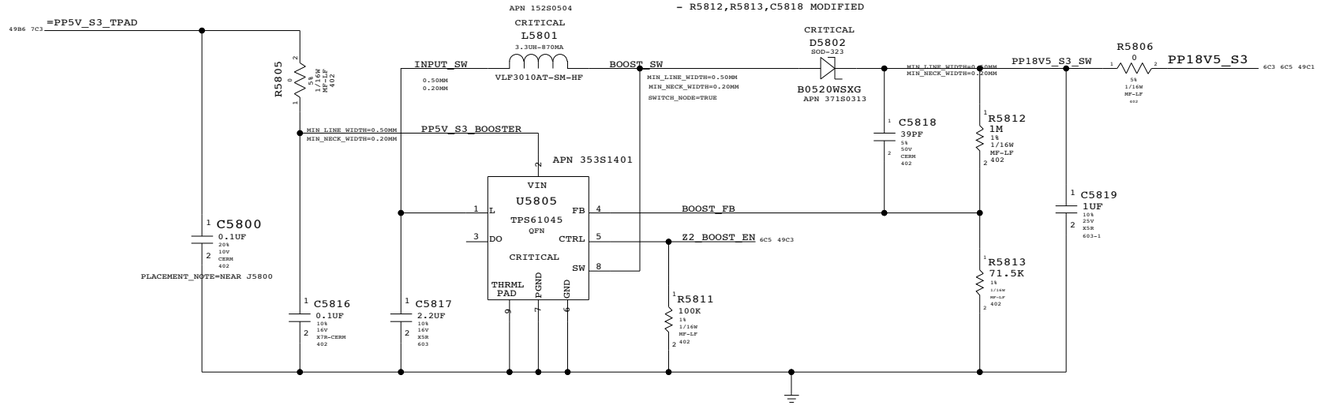
SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

APPLE INC.

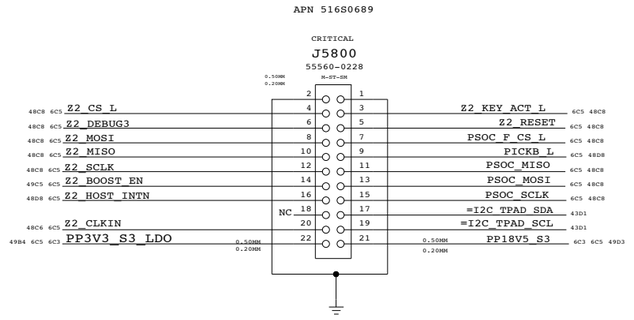
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 48 OF 81	

BOOSTER +18.5VDC FOR SENSORS

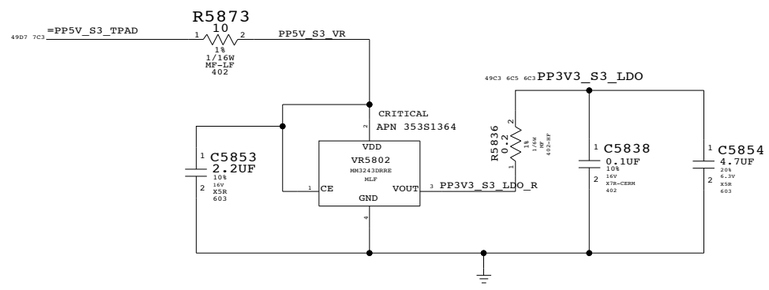
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

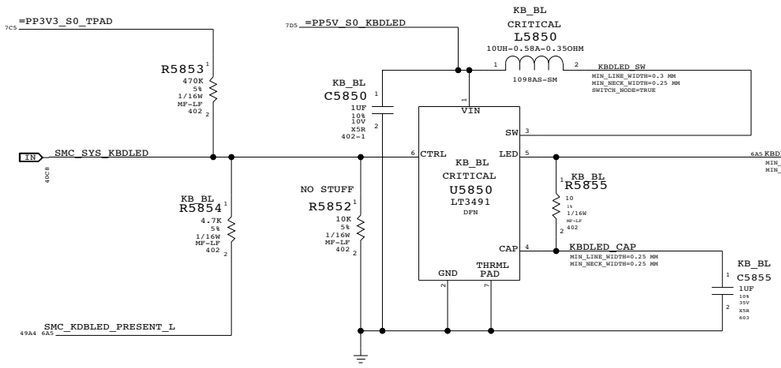
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

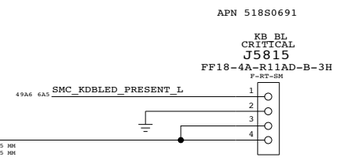
LOW = keyboard backlight present

HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT





J5815 pin 1 is grounded on keyboard backlight flex

KBD BACKLIGHT CONNECTOR

WELLSPRING 2

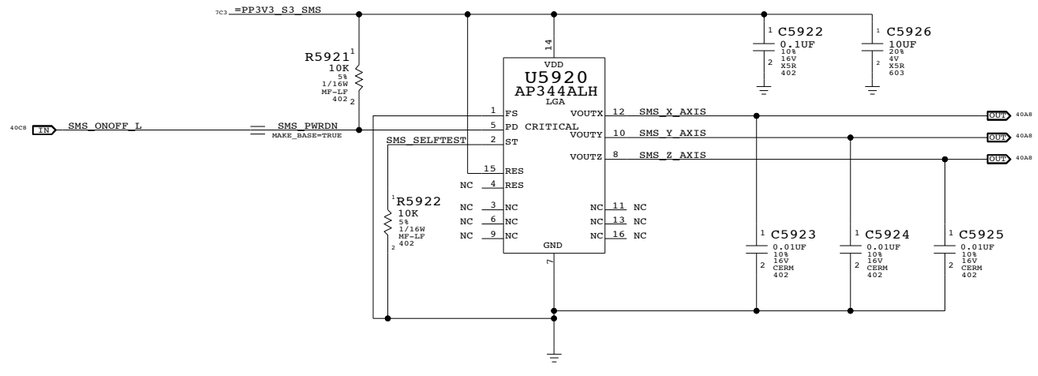
SYNC_MASTER=YUAN.MA SYNC_DATE=05/09/2008

APPLE INC.

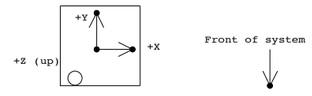
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 49 OF 81	

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when
placed on board top-side:



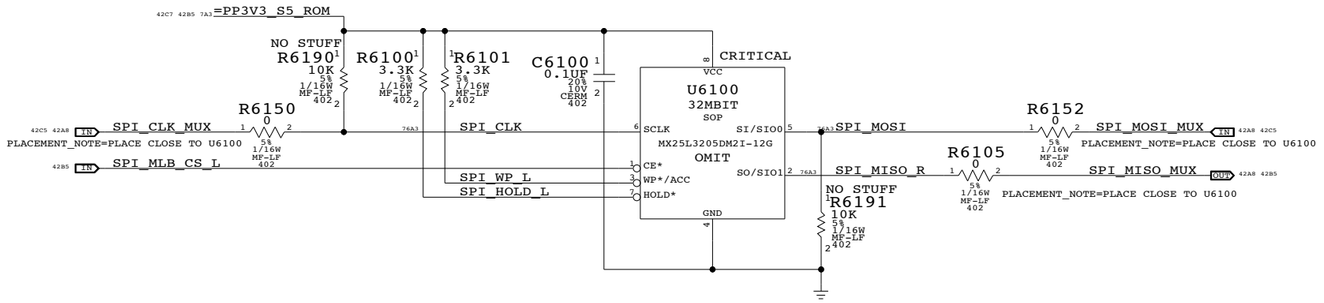
Circle indicates pin 1 location when placed
in correct orientation

SMS

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 50 OF 81	



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

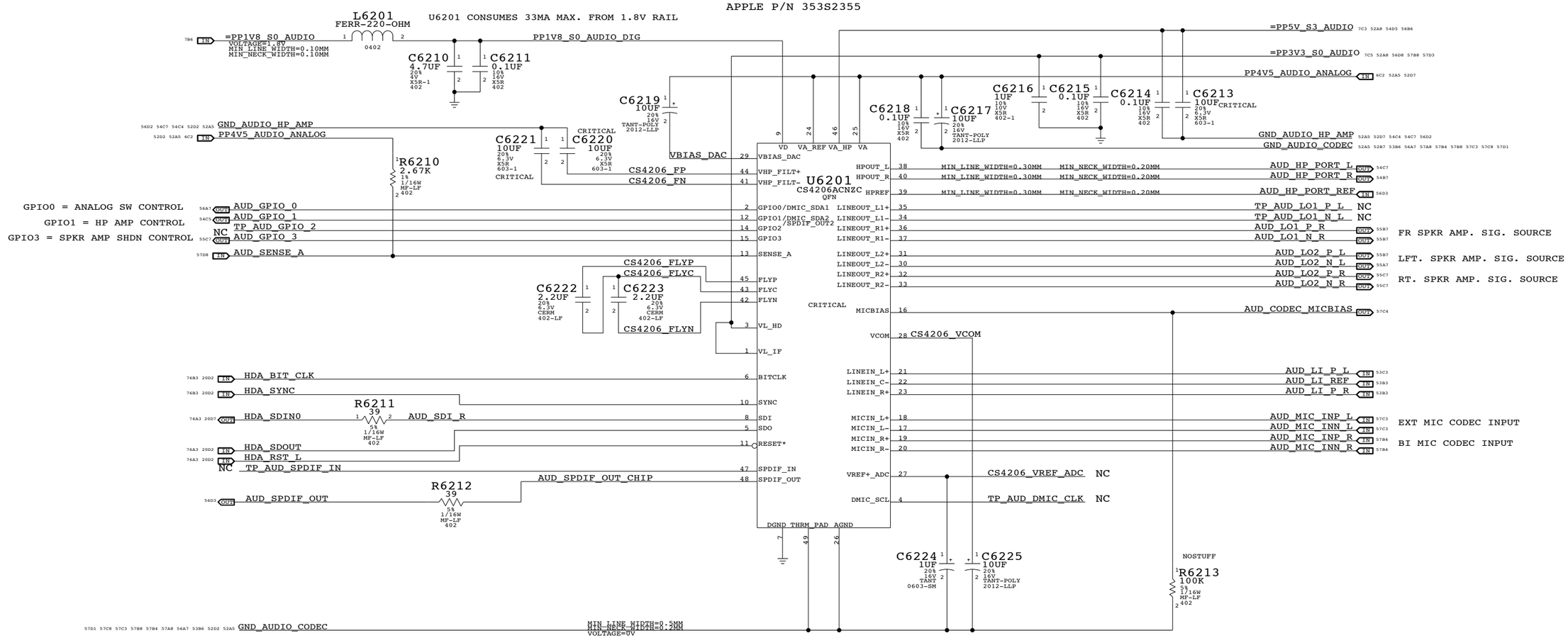
SPI ROM

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

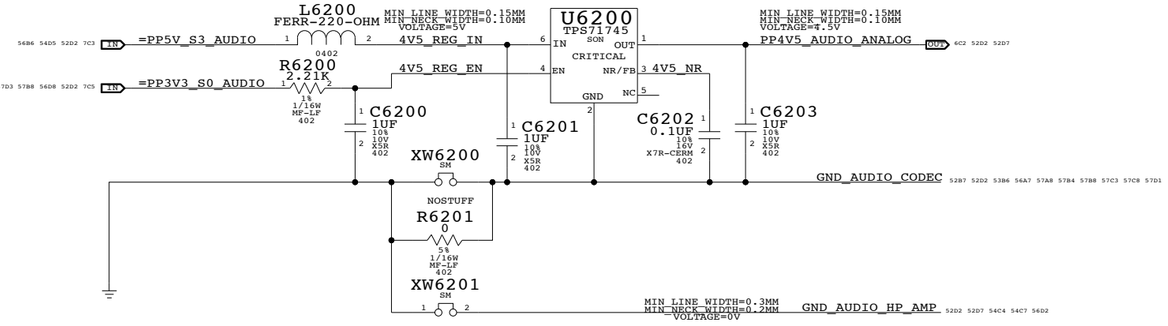
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 51 OF 81	

AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

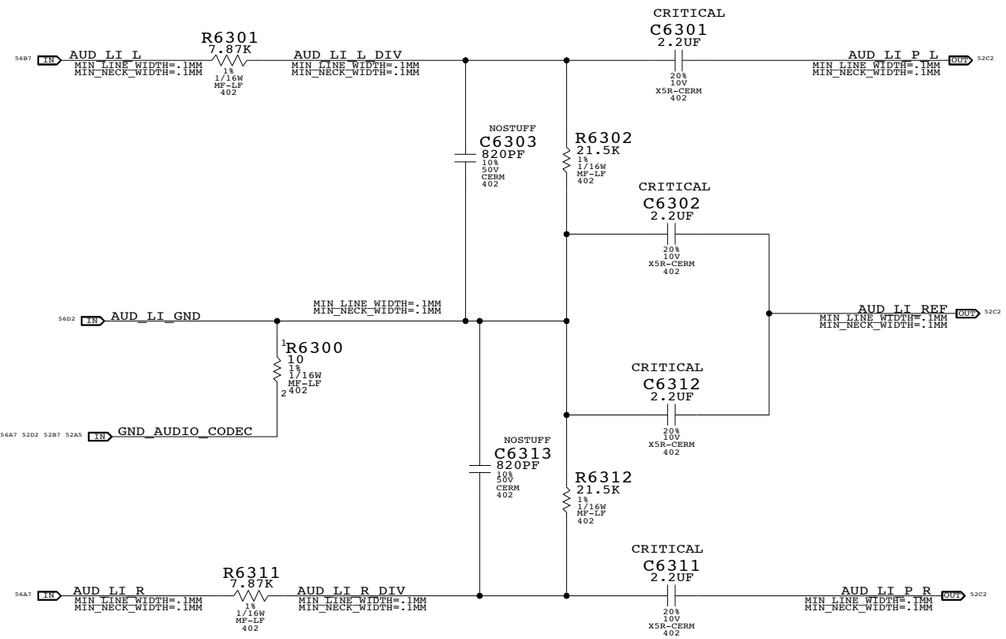
AUDIO: CODEC/REGULATOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 52 OF 81	

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



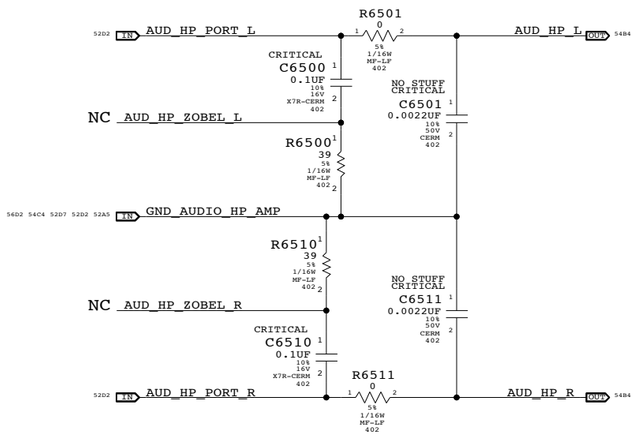
AUDIO: LINE INPUT FILTER

APPLE INC.

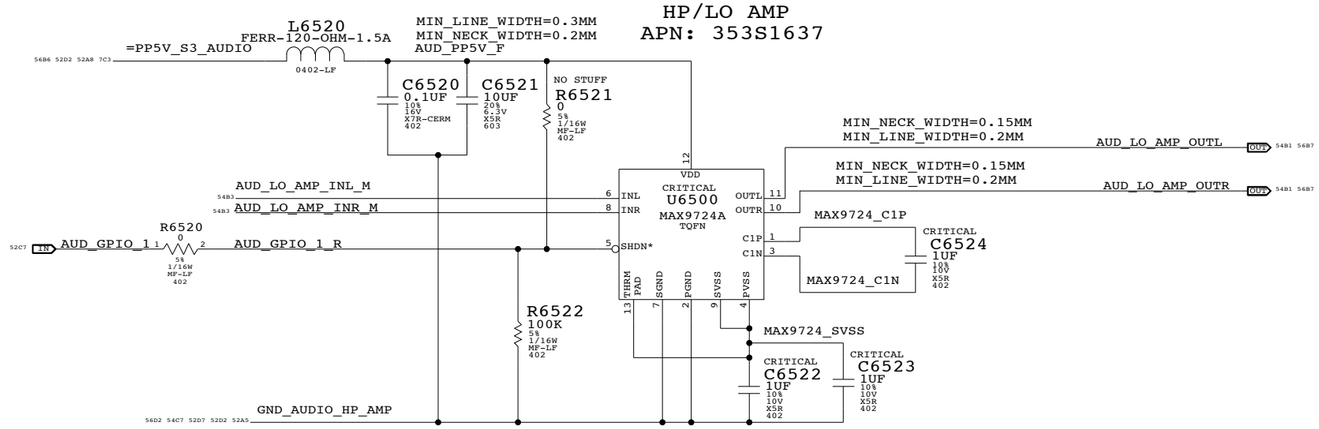
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 53 OF 81	

FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

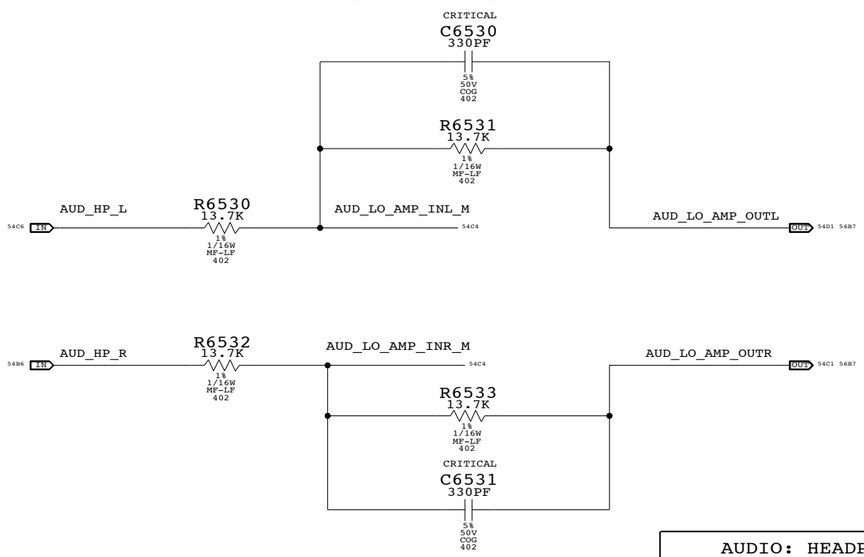
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



AUDIO: HEADPHONE FILTER

SYNC_MASTER=AUDIO SYNC_DATE=02/03/2009

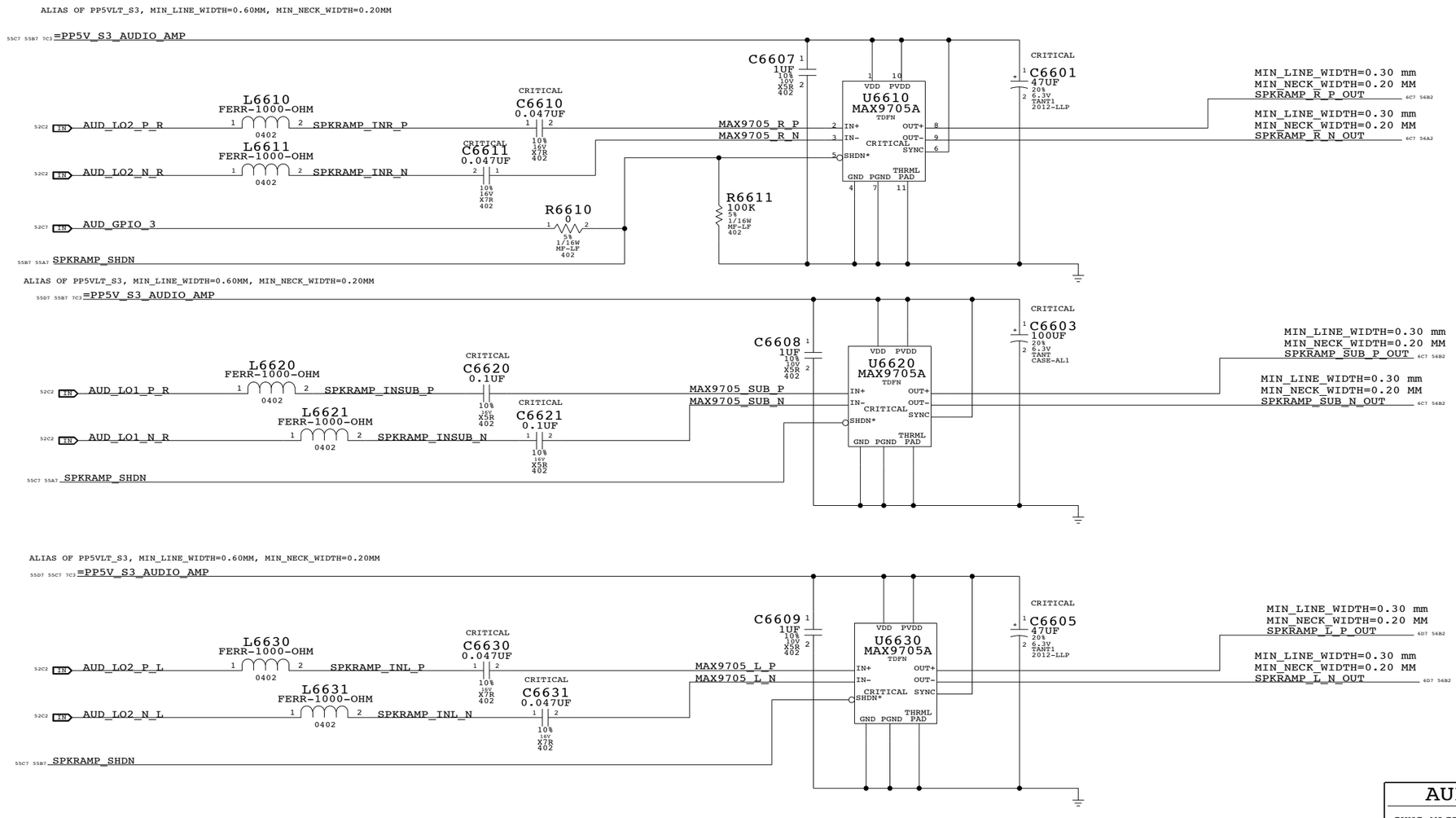
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 54 OF 81	

SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=12/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 55 OF 81	

AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO

APN:514-0671
J6700
SPDIF-TXRX-K24
F-RT-TH
CRITICAL
MIC 6
DETECT 5
SWITCH 2
LEFT 1
RIGHT 3
GND 4
AUDIO

A - VIN 7
B - VCC 8
C - GND 9
OPERATING VOLTAGE 3.3
POF

SHELL 10
11
12
SHIELD PINS 13

C6700 1UF 10% 6.3V CERM 402

AUD_CONNJ1_MIC
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIP
AUD_CONNJ1_RING

GND_CHASSIS_AUDIO_JACK

CHASSIS GND STITCHES
XW6710 SM
XW6711 SM
R6760 0 5% 1/16W MF-LF 402

GND STUFFING OPTIONS FOR CMOS SWITCH

AUD_SPDIF_OUT OUT 52B7

L6701 FERR-1000-OHM 0402 — HS_MIC_HI OUT 57C1
L6702 FERR-1000-OHM 0402 — HS_MIC_LO OUT 57C1
CRITICAL L6706 FERR-220-OHM 0402 — AUD_HP_PORT_REF OUT 52D2
CRITICAL L6703 FERR-120-OHM-1.5A 0402-LF — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, AUD_CONN_GND
CRITICAL L6704 FERR-220-OHM 0402 — AUD_CONN_L BI 56B3
CRITICAL L6705 FERR-220-OHM 0402 — AUD_CONN_R BI 56A3

XW6700 SM — GND_AUDIO_HP_AMP 52A5 52D2 52D7 54C4 54C7
XW6701 SM — AUD_LI_GND 53B6
AUD_CONN_GND 56A7 56D2 56A7 56D2

CRITICAL DZ6701 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6700 6.8V-100PF 402

C6701 100PF 5% 50V CERM 402

R6700 10K 5% 1/16W MF-LF 402 — AUD_J1_SLEEVEDET_R OUT 57C6 57C8
R6701 4.7 5% 1/16W MF-LF 402 — AUD_J1_TIPDET_R OUT 57A7 57C8

NOSTUFF R6723 0 5% 1/16W MF-LF 402
NOSTUFF R6722 0 5% 1/16W MF-LF 402
NOSTUFF R6725 0 5% 1/16W MF-LF 402
=PP3V42_G3H_AUDIO 7D1
R6724 0 5% 1/16W MF-LF 402
=PP5V_S3_AUDIO 54D5 52D2 52A8 7C3
PP_MAX14504_VCC
C6710 1UF 10% 10V X5R 402
NOSTUFF R6726 0 5% 1/16W MF-LF 402

APN: 353S2536

U6700
MAX14504
WLP
CRITICAL
A3 VCC
C4 NC1
C1 NC2
A4 NO1
A1 NO2
C2 CB
A2 NEG
COM1 B4
COM2 B1
EN* B2
GND B3 C3

AUD_LO_AMP_OUTL OUT 54D1 54B1 — R6716 0 5% 1/16W MF-LF 402 — AUD_LO_AMP_OUTL_SWITCH
AUD_LO_AMP_OUTR OUT 54C1 54B1 — R6717 0 5% 1/16W MF-LF 402 — AUD_LO_AMP_OUTR_SWITCH
AUD_LI_L IN 53C8 — R6718 0 5% 1/16W MF-LF 402 — AUD_LI_L_SWITCH
AUD_LI_R IN 53B6 — R6719 0 5% 1/16W MF-LF 402 — AUD_LI_R_SWITCH
AUD_GPIO_0 IN 52C7 — R6720 0 5% 1/16W MF-LF 402 — AUD_SWITCH_CTRL
R6721 100K 5% 1/16W MF-LF 402
AUD_CONN_GND 56D2 — R6715 0 5% 1/16W MF-LF 402 — AUD_SWITCH_GND
GND_AUDIO_CODEC 57D1 57C8 57C3 57B8 57B4 57A8 53B6 52D2 52B7 52A5 — R6714 0 5% 1/16W MF-LF 402
NOSTUFF R6727 0 5% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_L BI 56C3
R6712 24K 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
AUD_CONN_R BI 56C3
R6713 24K 5% 1/16W MF-LF 402
C6711 0.0033UF 10% 50V CERM 402

ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

MIC CONNECTOR

APN:518S0520

CRITICAL
J6701
78171-0003
M-RT-SM
4
1 BI_MIC_LO 57B1 6D7
2 BI_MIC_SHIELD 57B1 6D7
3 BI_MIC_HI 57B1 6D7
5

SPEAKER CONNECTOR

APN:518S0519

CRITICAL
J6702
78171-0002
M-RT-SM
3
SPKRAMP_L_P_OUT IN 55B2 6D7 — 1
SPKRAMP_L_N_OUT IN 55A2 6D7 — 2
4

SPKRAMP_SUB_P_OUT IN 55C2 6C7
C6760 33PF 5% 50V CERM 402
C6761 33PF 5% 50V CERM 402
SPKRAMP_SUB_N_OUT IN 55B2 6C7
SPKRAMP_R_P_OUT IN 55C2 6C7
C6762 33PF 5% 50V CERM 402
C6763 33PF 5% 50V CERM 402
SPKRAMP_R_N_OUT IN 55C2 6C7

CRITICAL
J6703
78171-0004
M-RT-SM
5
1
2
3
4
6

APN:518S0521

C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

AUDIO: JACK

SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 56 OF 81	

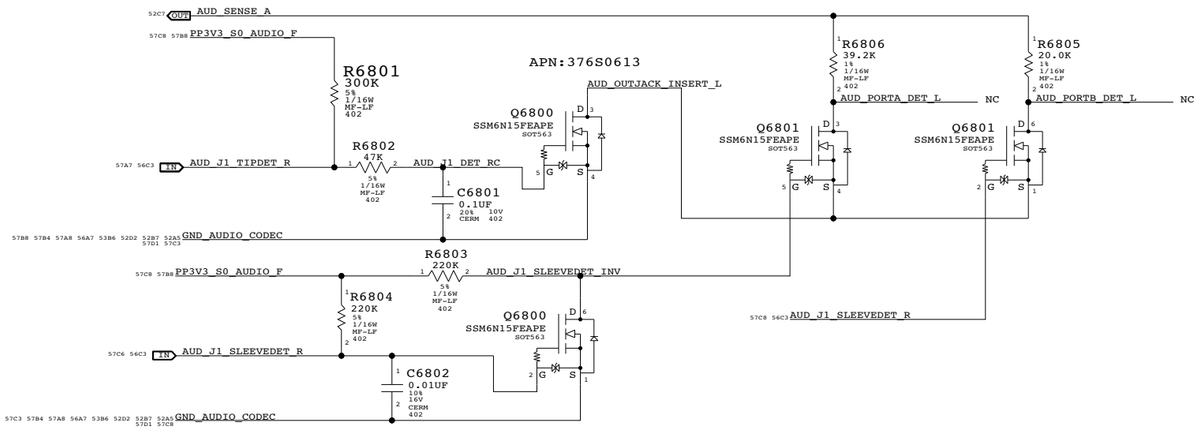
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

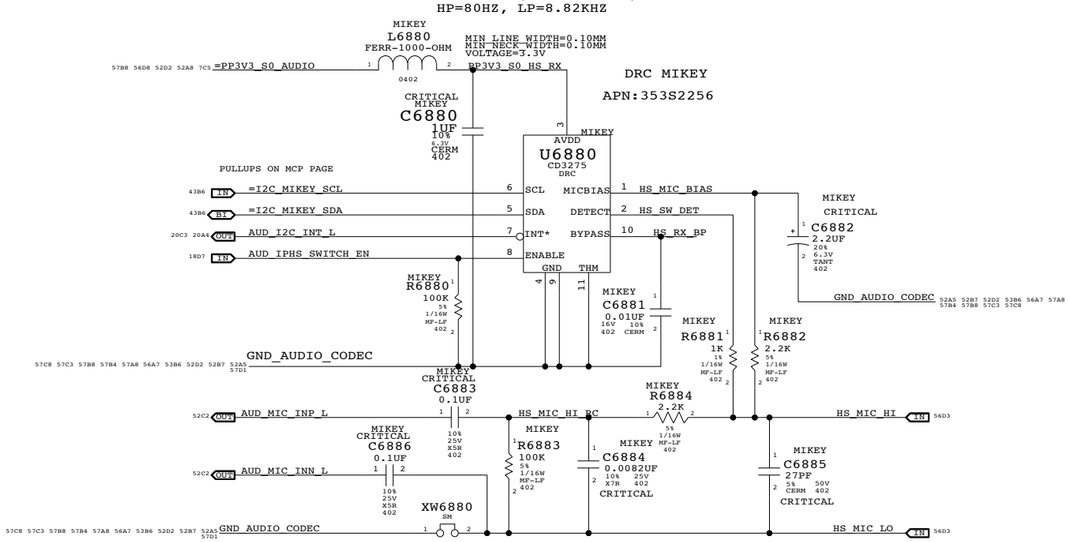
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

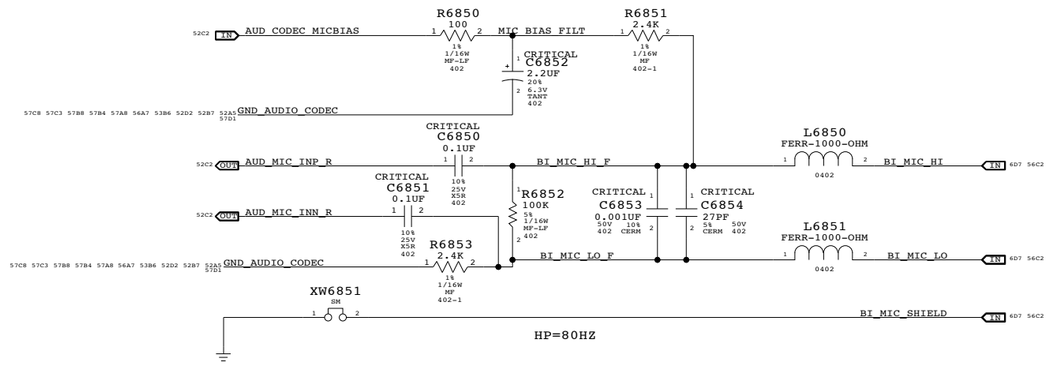
PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)



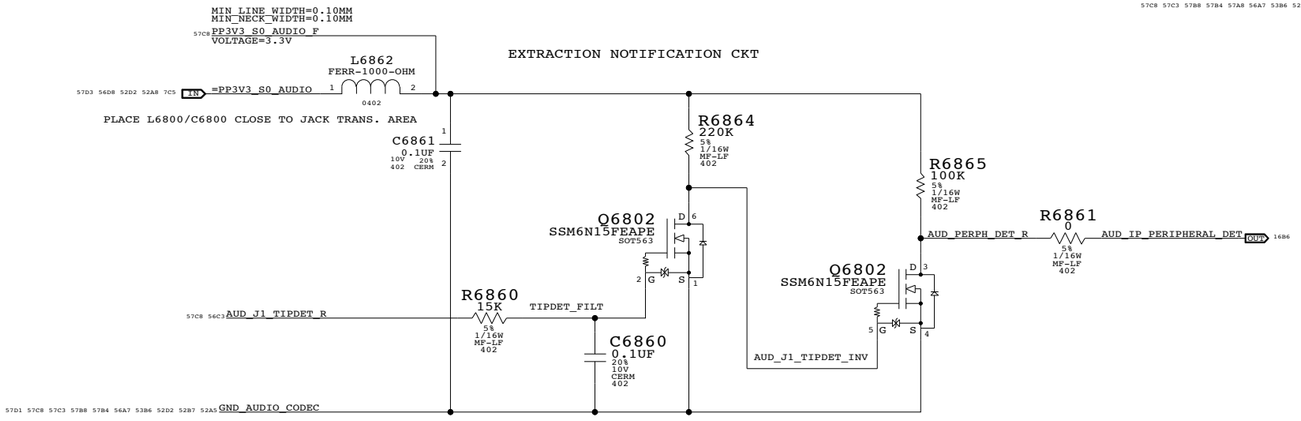
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



EXTRACTION NOTIFICATION CKT



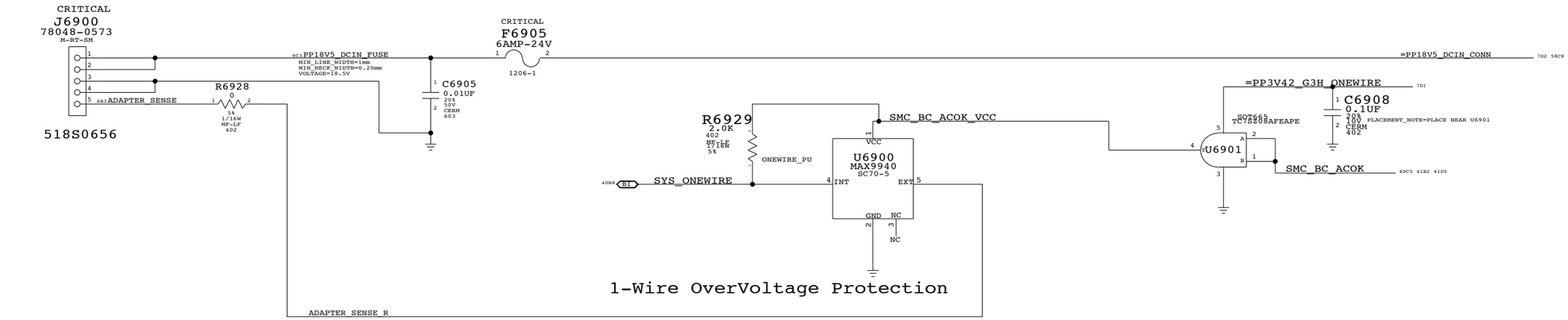
AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=03/20/2009

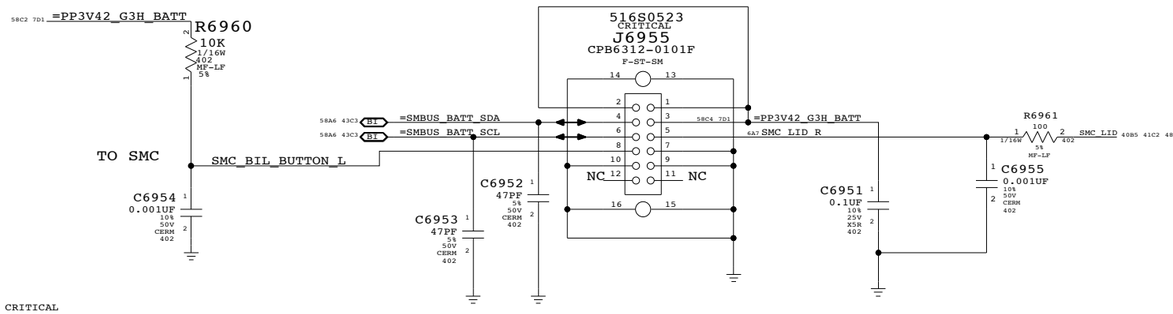
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 57 OF 81	

MagSafe DC Power Jack

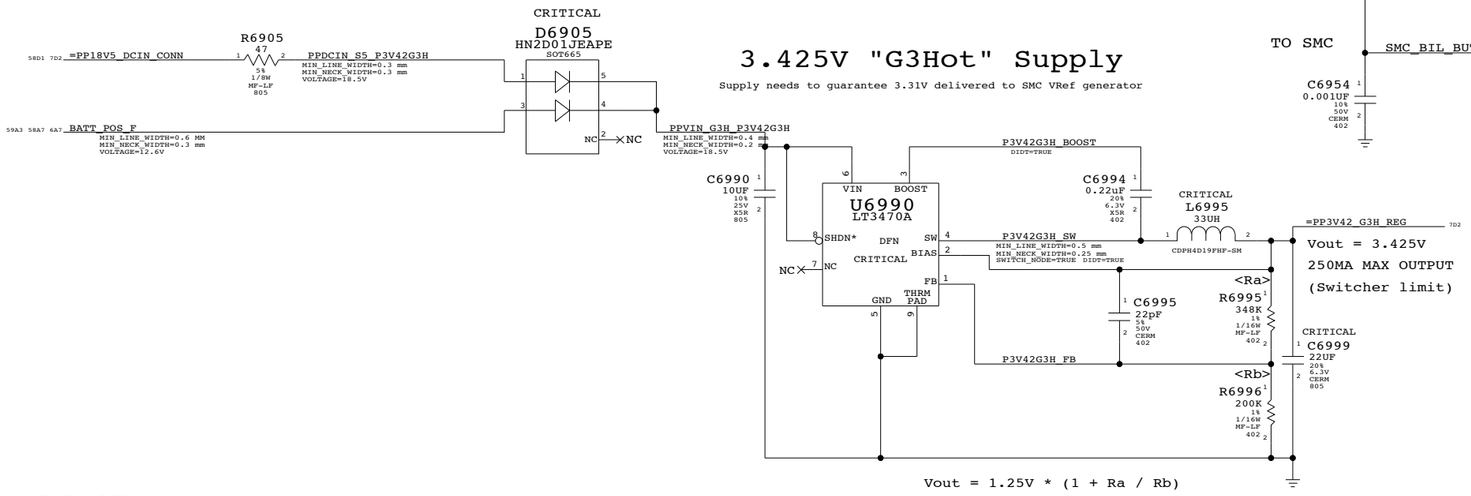


BIL CONNECTOR

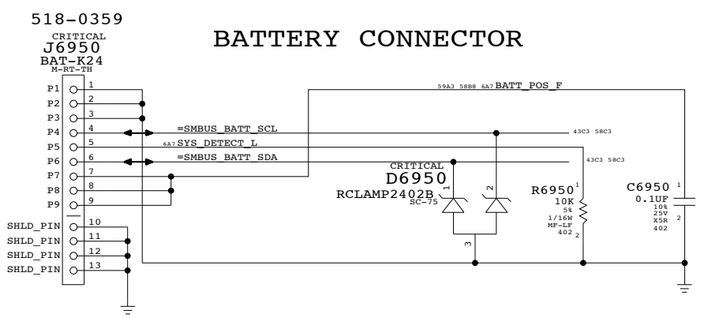


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



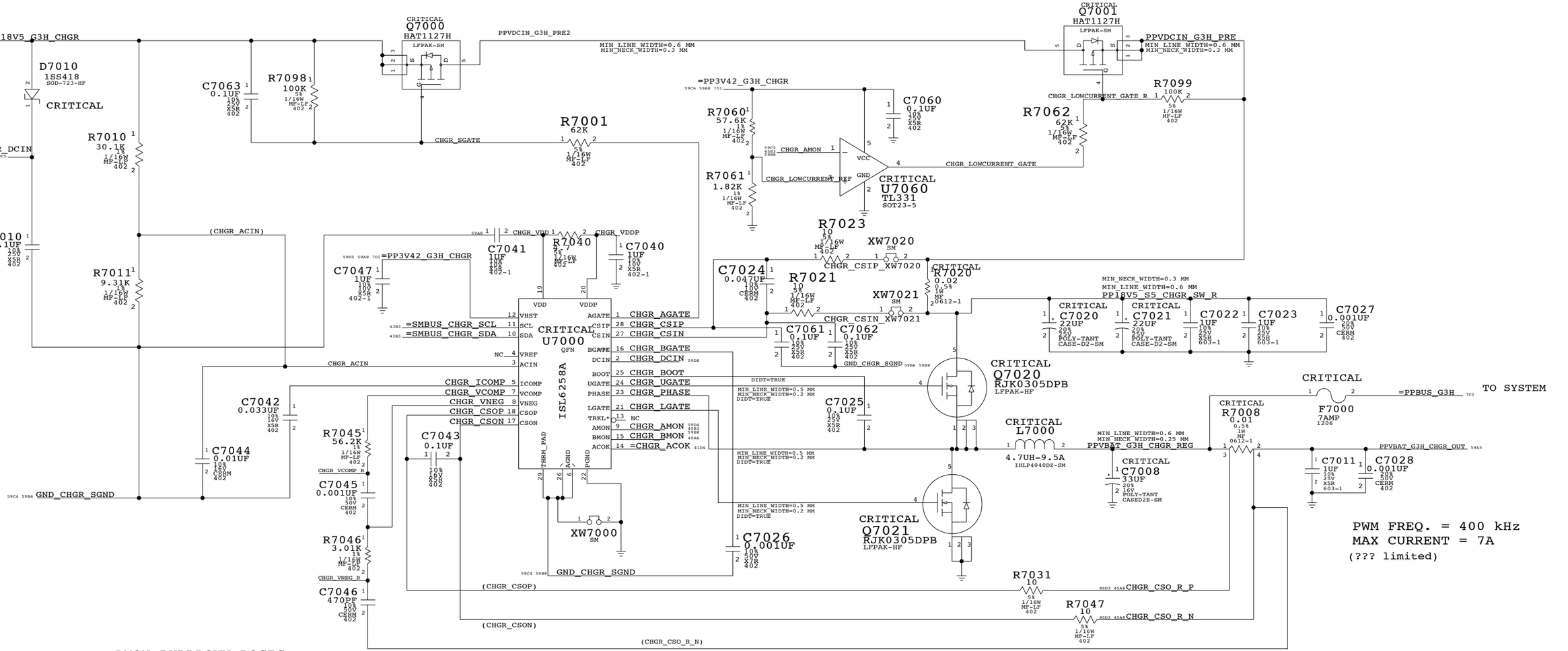
DC-In & Battery Connectors

SYNC_MASTER=YUNWU SYNC_DATE=12/11/2008

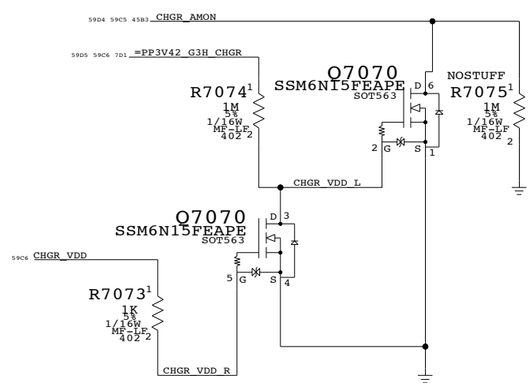
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 58 OF 81	

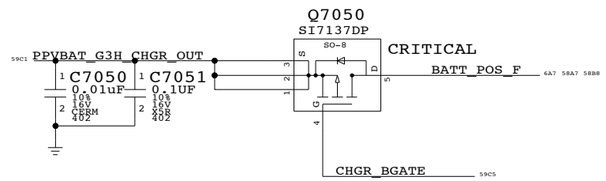
PBUS SUPPLY / BATTERY CHARGER



AMON PULLDOWN LOGIC



BATTERY CHARGE LIMITING FETS



PBUS Supply/Battery Charger

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

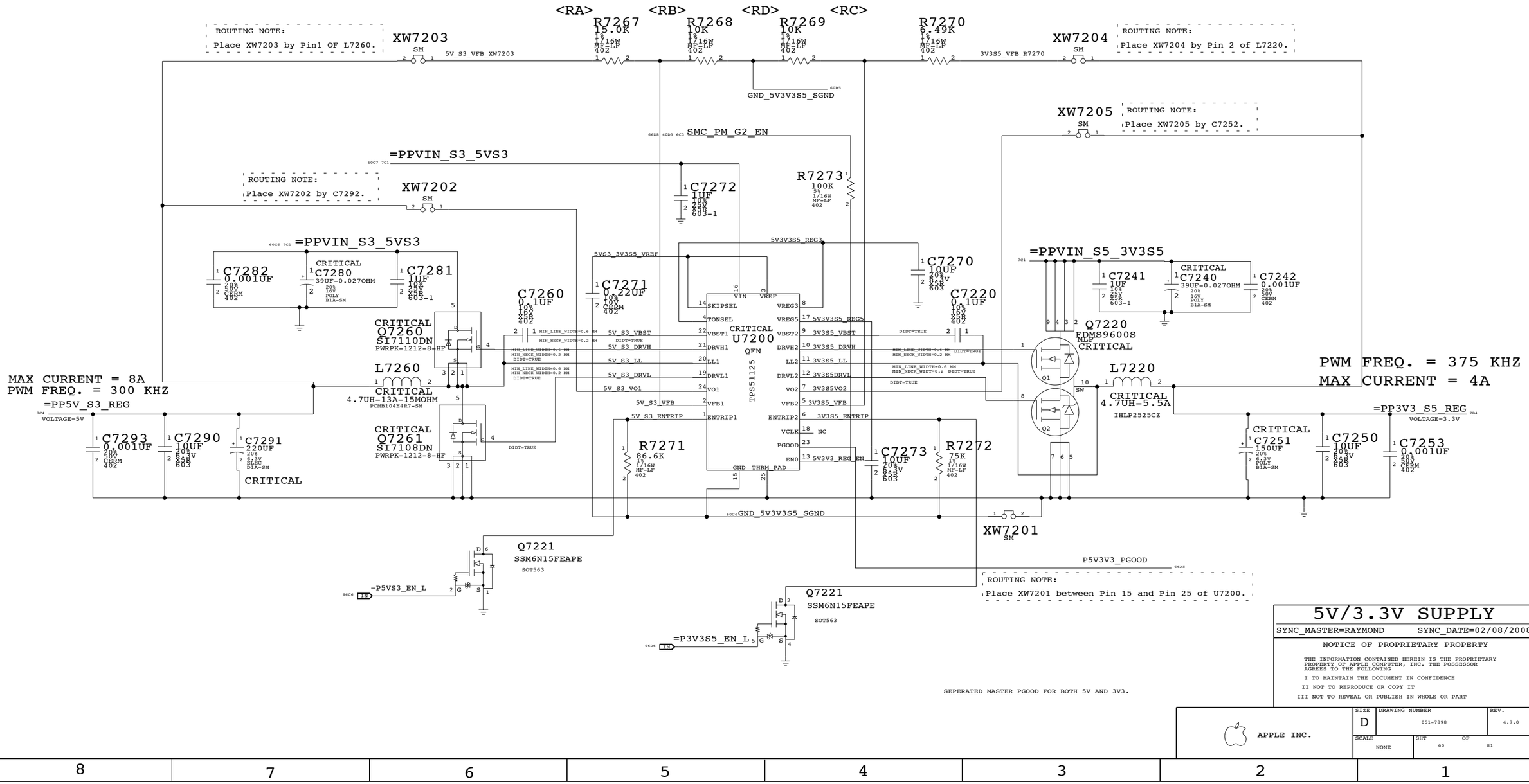
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 59 OF 81	

5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



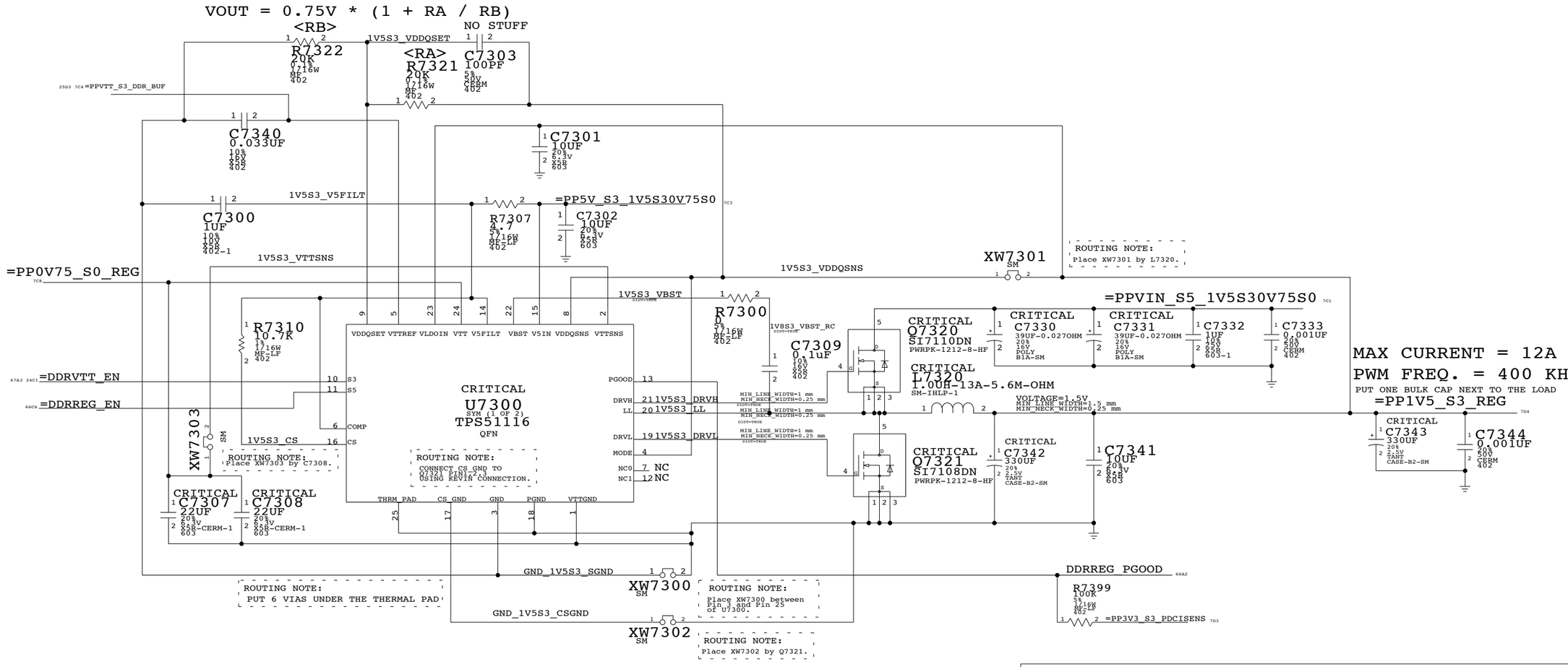
5V/3.3V SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE	SHT	OF
NONE	60	81

1.5V/0.75V(DDR3) POWER SUPPLY



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

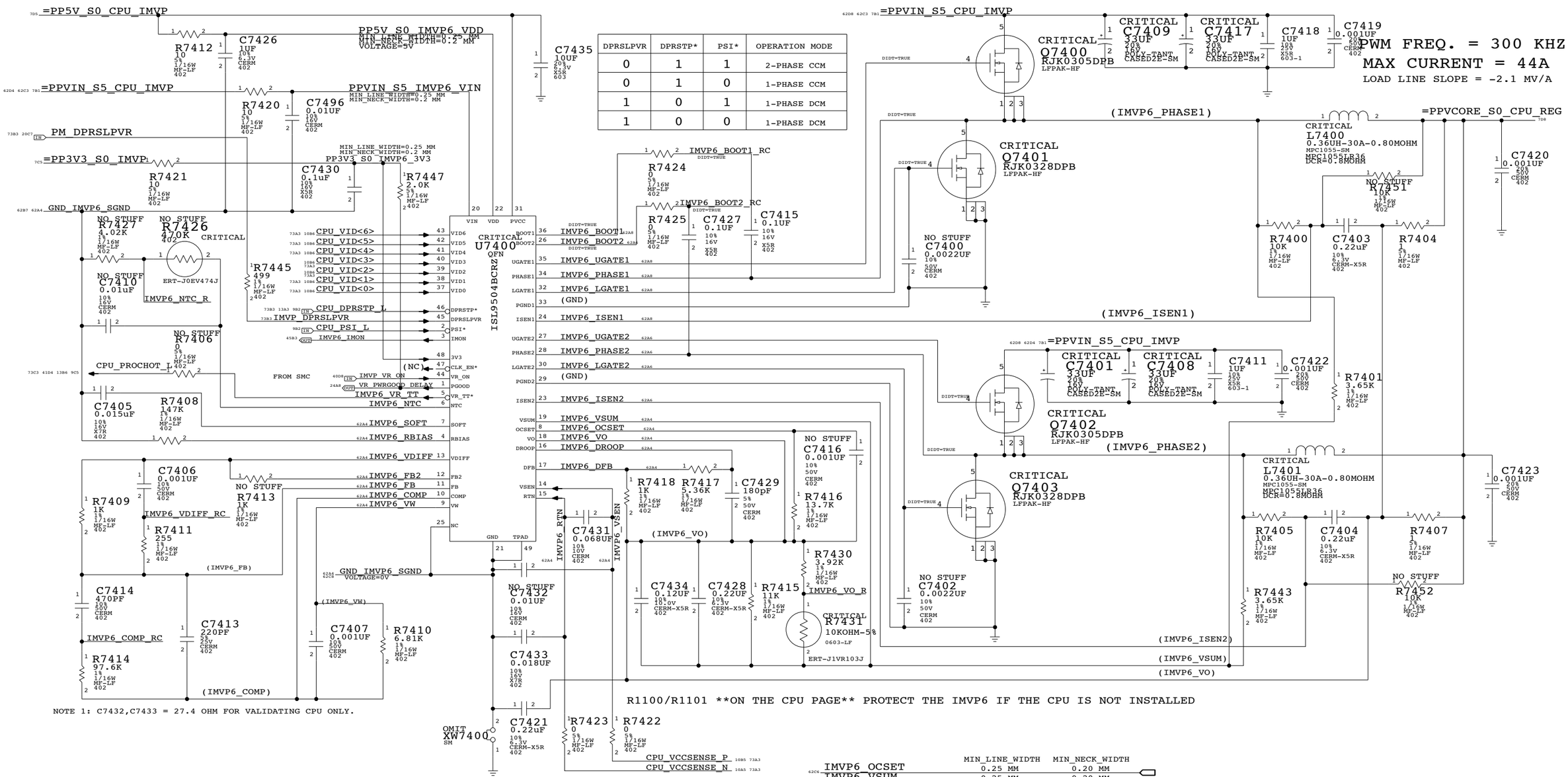
1.5V/0.75V DDR3 SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE: NONE SHT 61 OF 81



DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

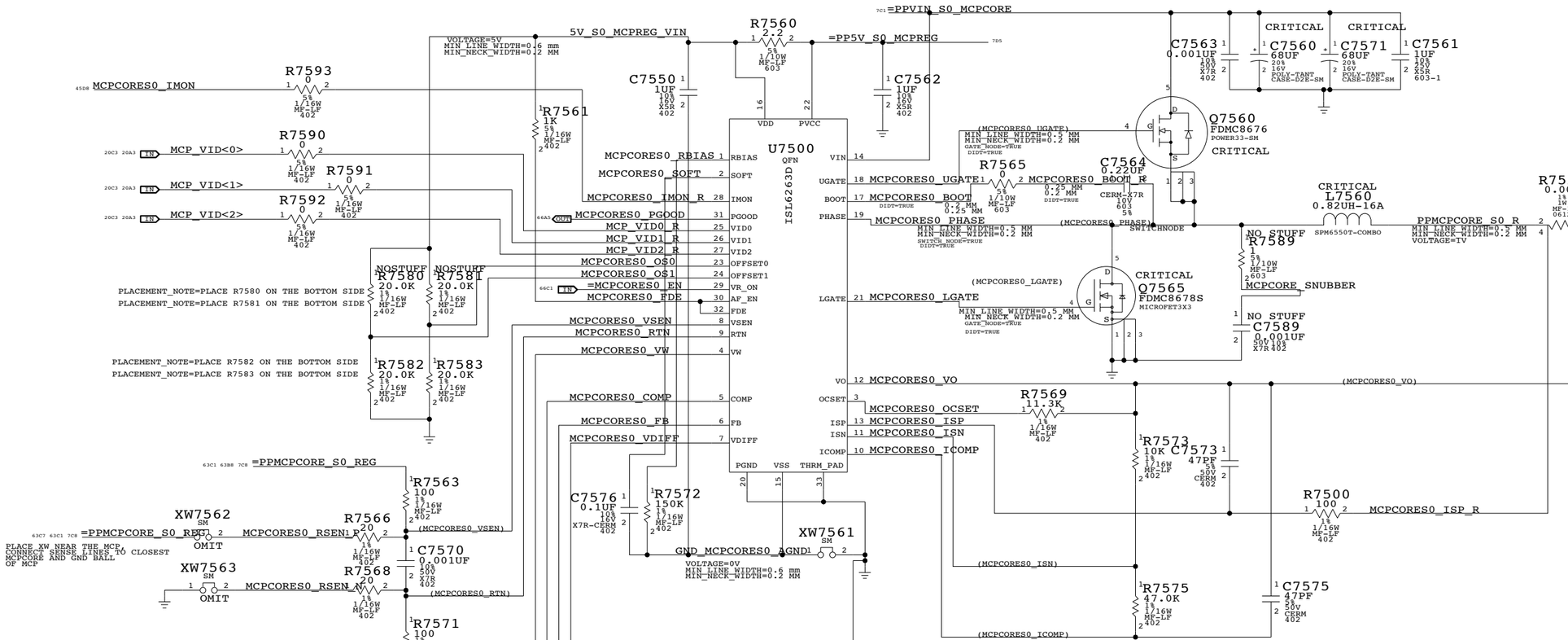
IMVP6 CPU VCore Regulator

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 62 OF 81	

MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

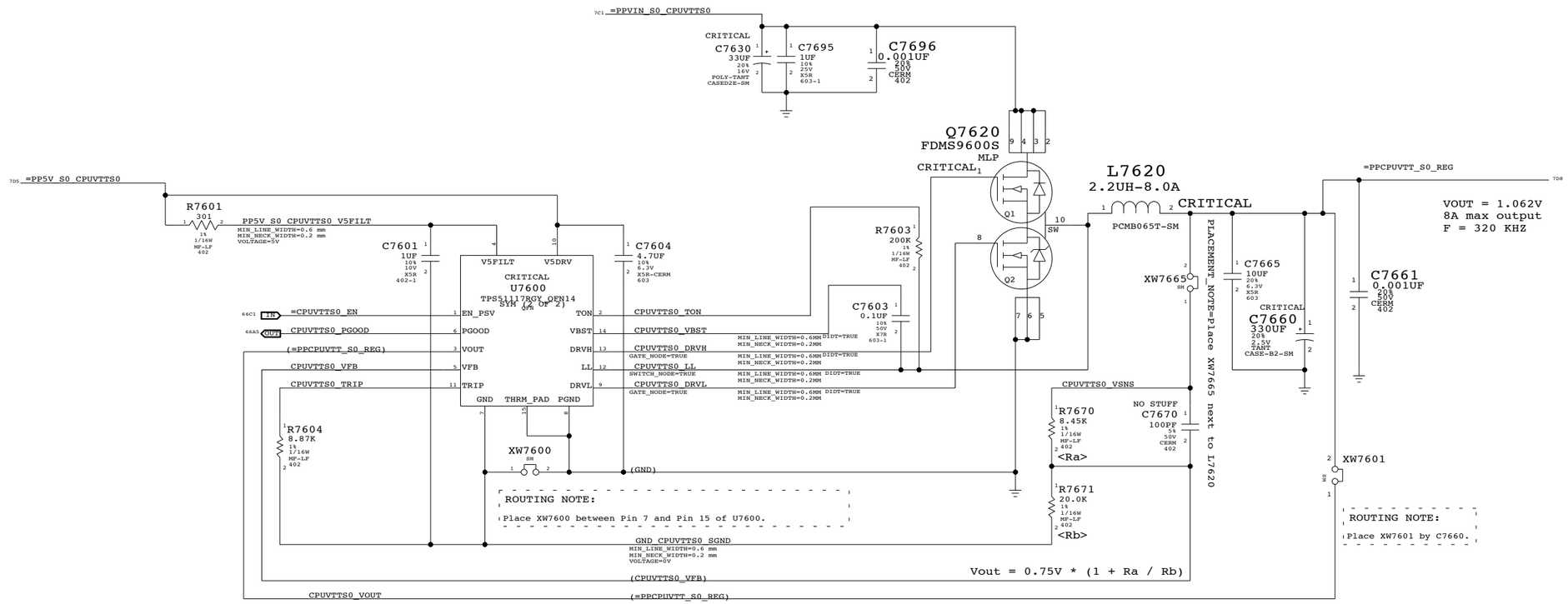
MCP CORE REGULATOR

SYNC_MASTER=K19_MLB SYNC_DATE=12/10/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 63 OF 81	

CPUVTT POWER SUPPLY



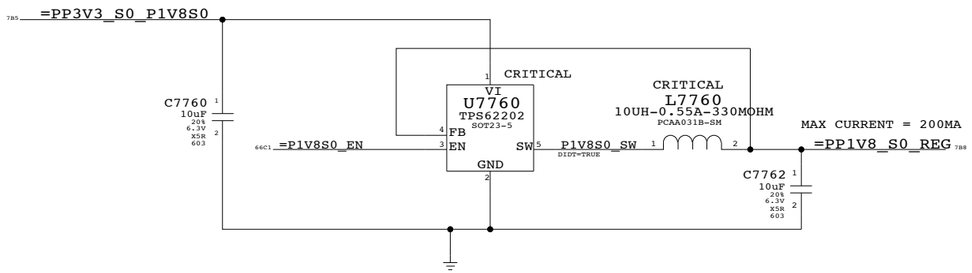
CPU VTT(1.05V) SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

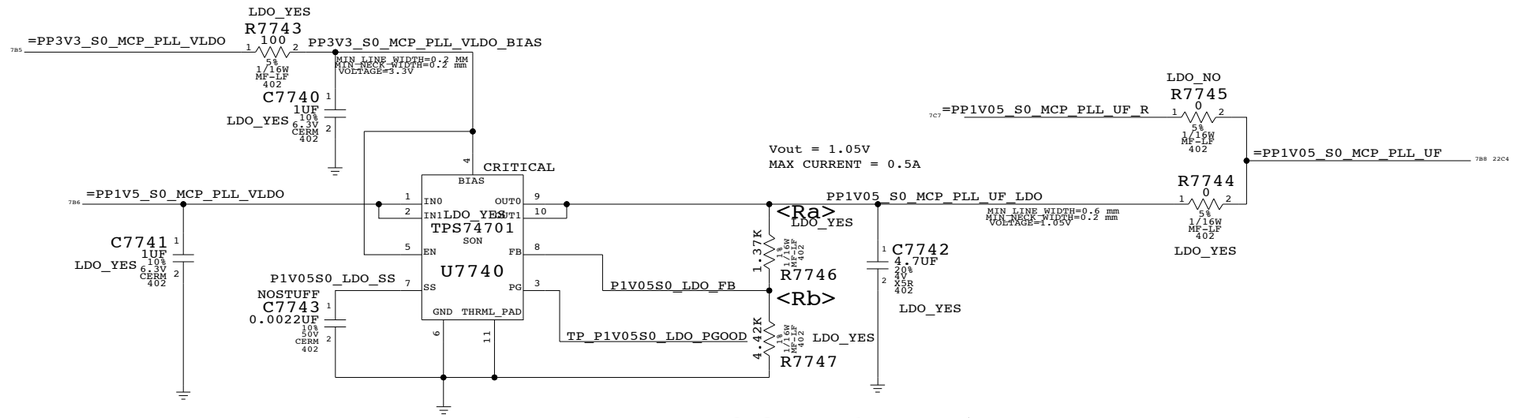
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE	SHT	OF
NONE	64	81

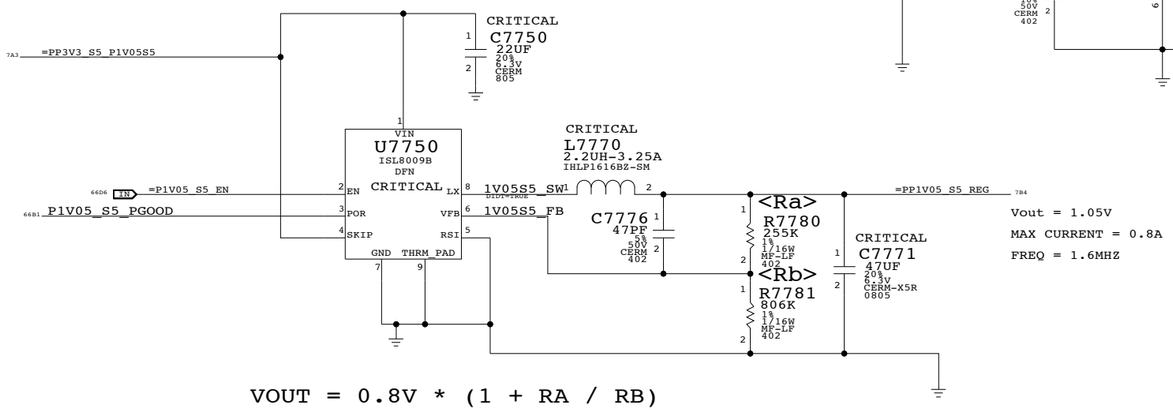
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



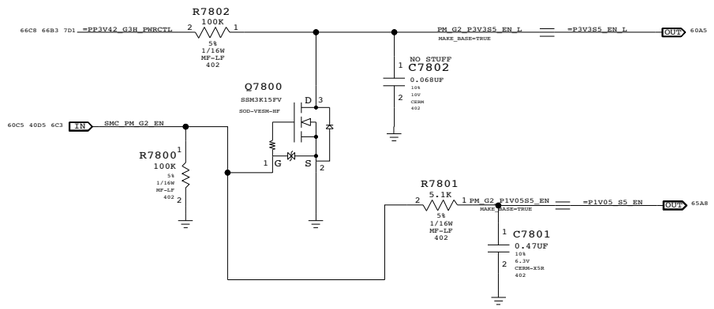
MISC POWER SUPPLIES

SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 65 OF 81	

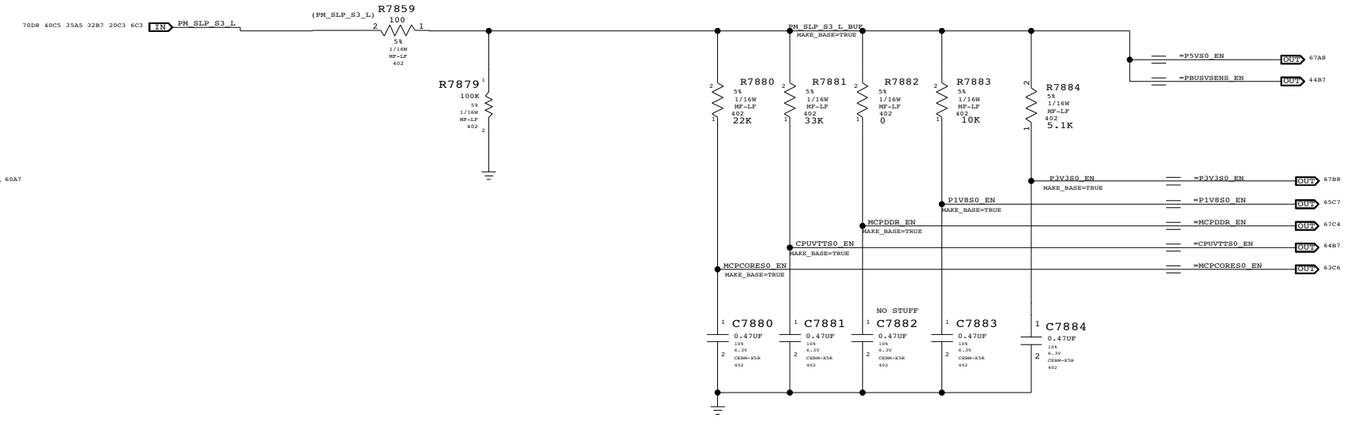
3.3V 1.05V S5 ENABLE



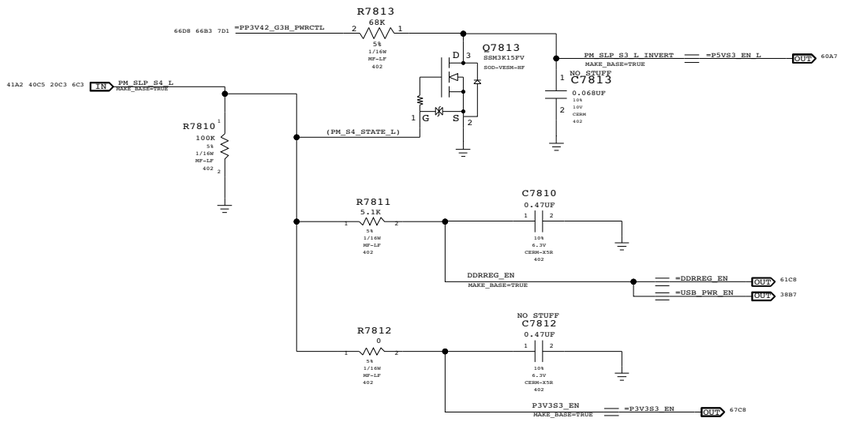
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

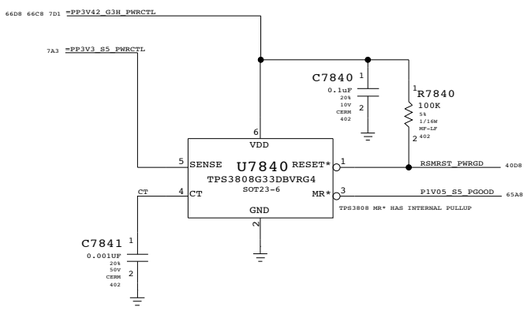
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



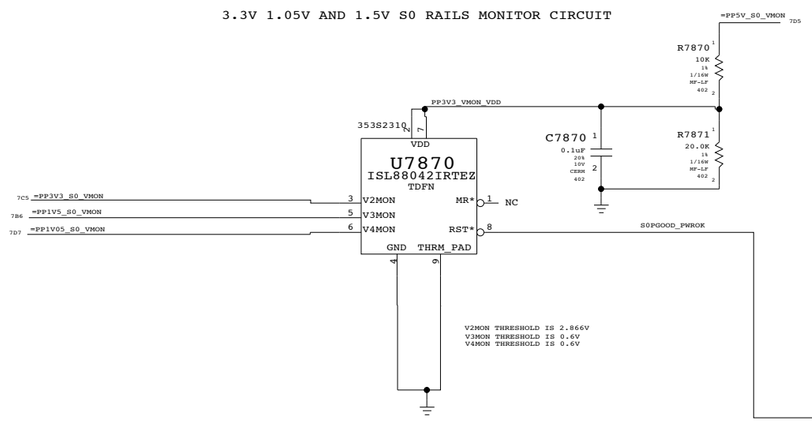
S3 ENABLE



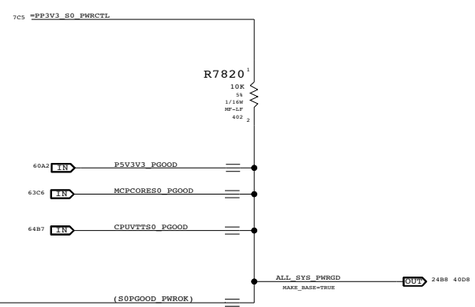
VOLTAGE MONITOR



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



Unused PGOOD signal

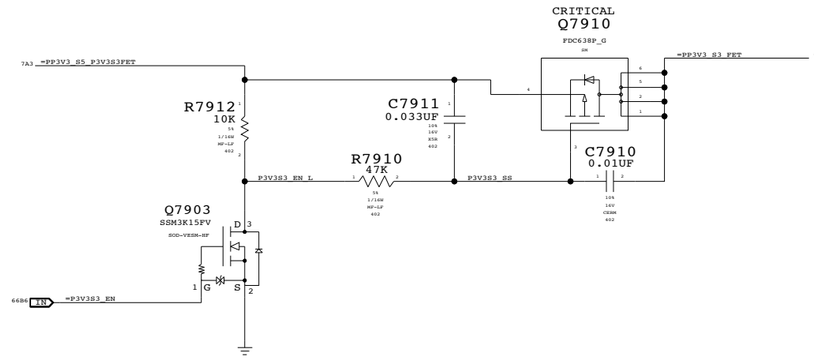
POWER SEQUENCING

SYNC_MASTER=YUAN.MA SYNC_DATE=12/11/2008

APPLE INC.

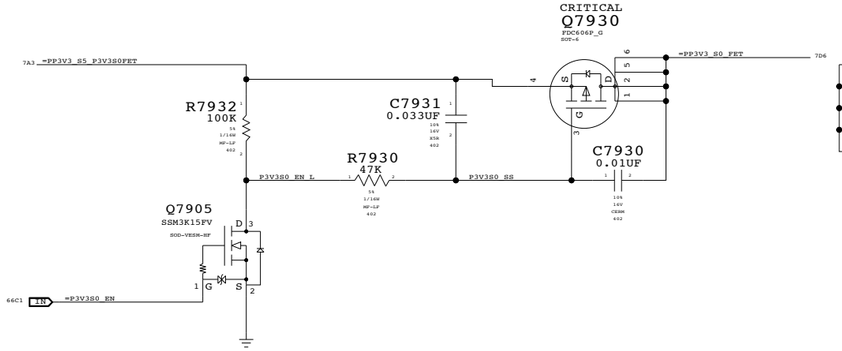
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 66 OF 81	

3.3V S3 FET



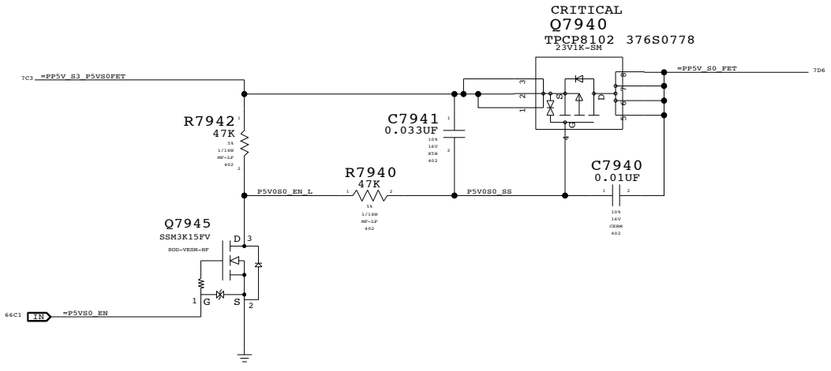
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

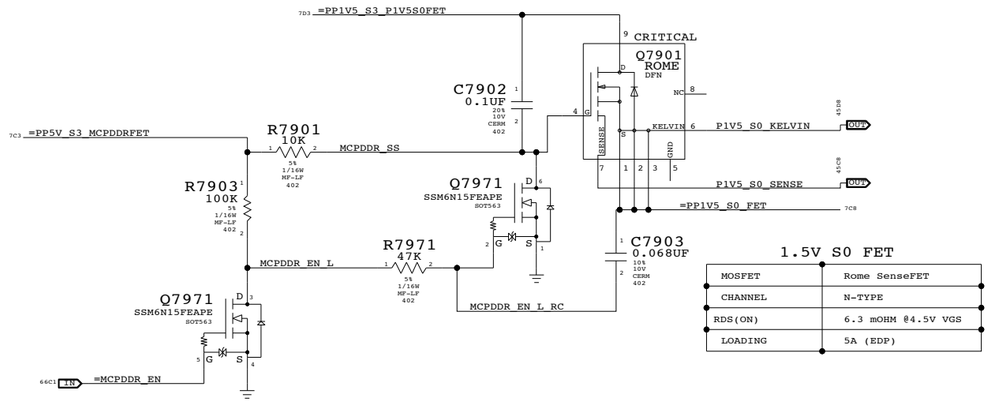
5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

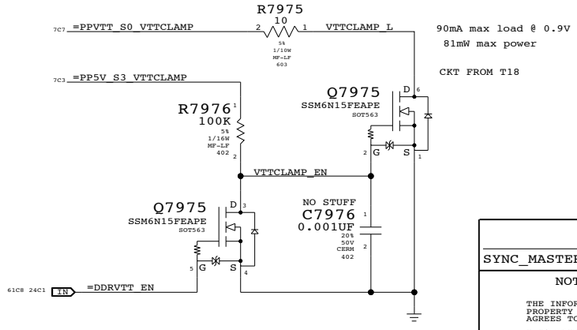
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



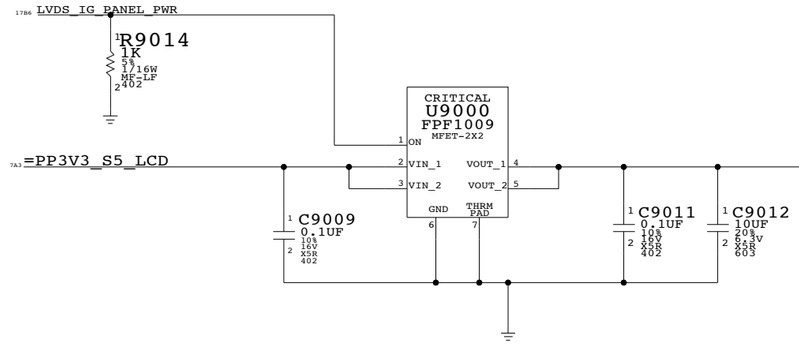
POWER FETS

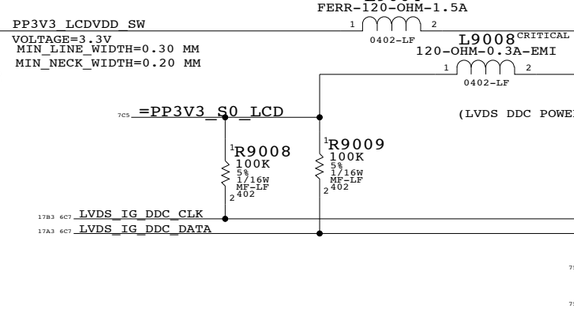
SYNC_MASTER=YUAN.MA SYNC_DATE=12/11/2008

APPLE INC.

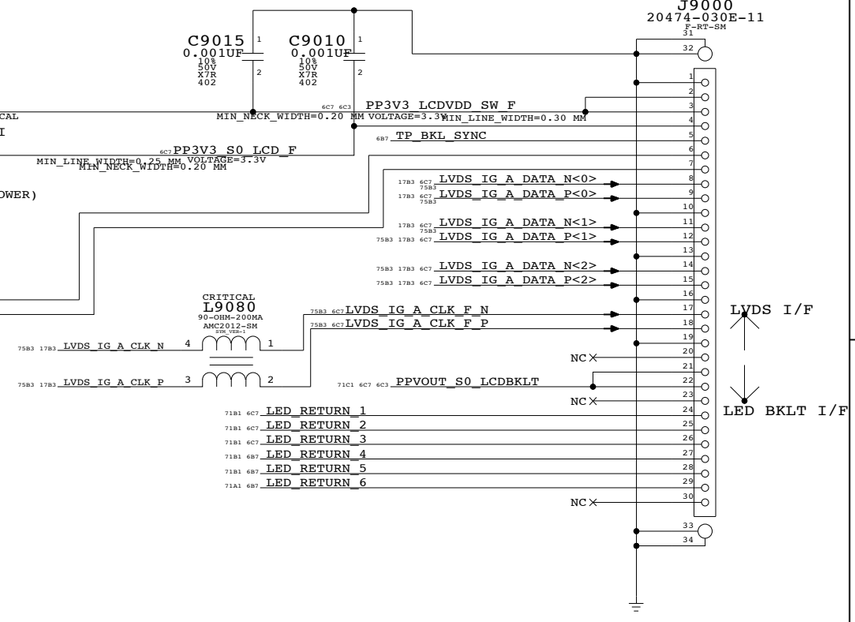
SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 67 OF 81	

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP





(LVDS DDC POWER)



LCD CONNECTOR

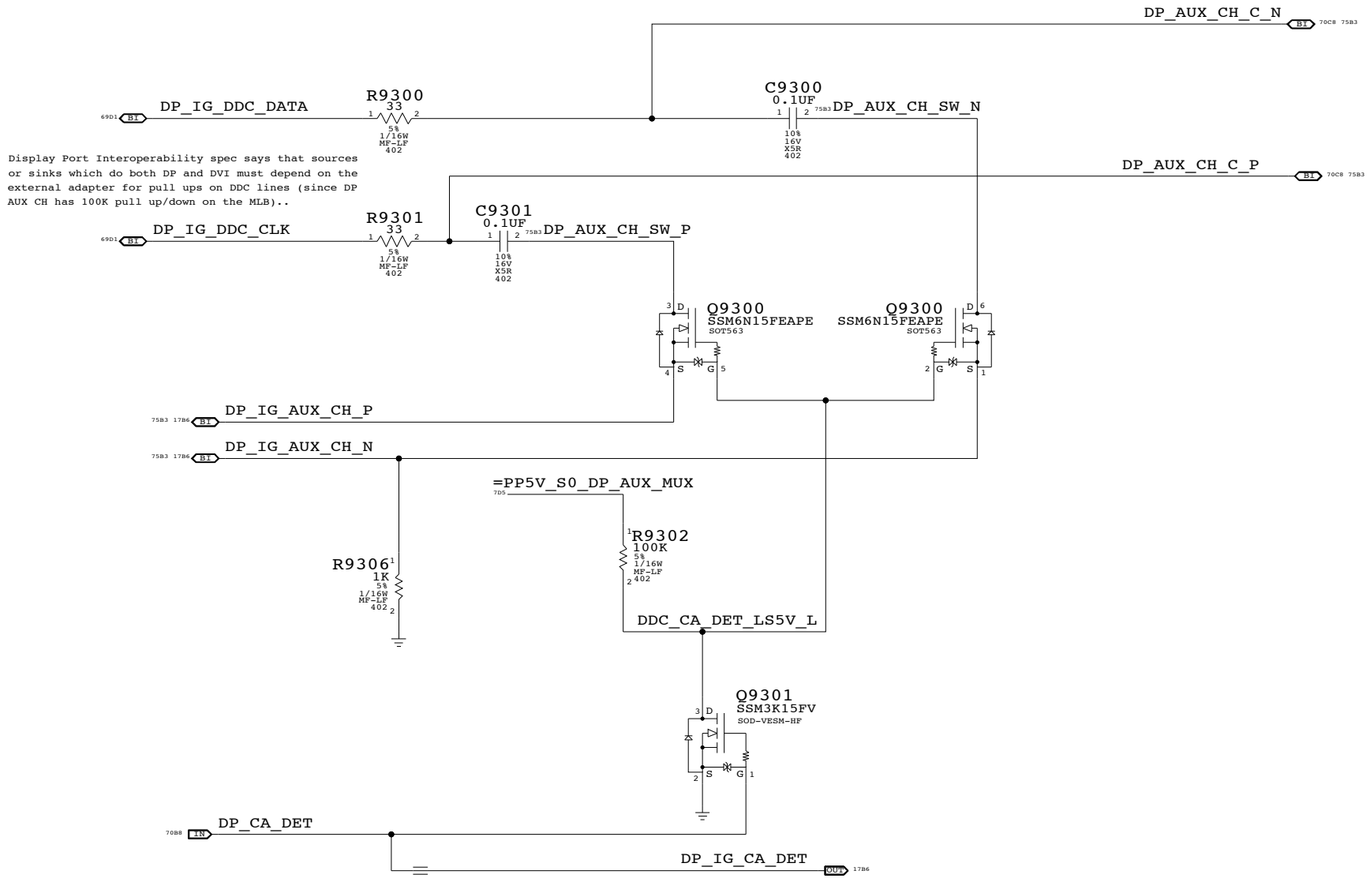
LVDS CONNECTOR:518S0650

LVDS CONNECTOR

SYNC_MASTER=NMARSYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 68 OF 81	



=MCP_HDMI_TXC_P — DP_ML_P<3> — MAKE_BASE=TRUE
=MCP_HDMI_TXC_N — DP_ML_N<3> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<0> — DP_ML_P<2> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<0> — DP_ML_N<2> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<1> — DP_ML_P<1> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<1> — DP_ML_N<1> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<2> — DP_ML_P<0> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<2> — DP_ML_N<0> — MAKE_BASE=TRUE
=MCP_HDMI_HPD — DP_HPD — MAKE_BASE=TRUE
=MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — MAKE_BASE=TRUE
=MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — MAKE_BASE=TRUE

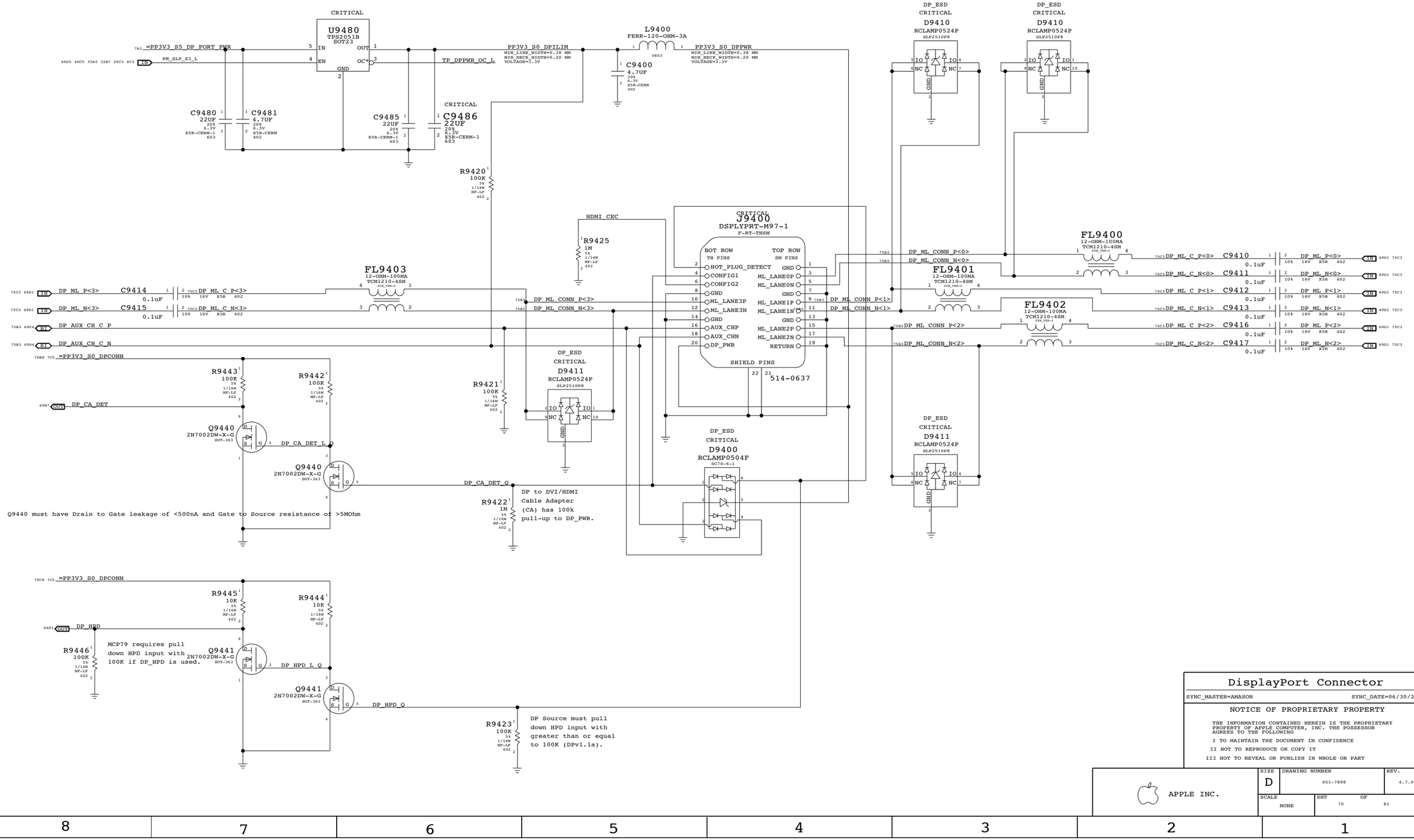
DISPLAYPORT SUPPORT

SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 69 OF 81	

Port Power Switch



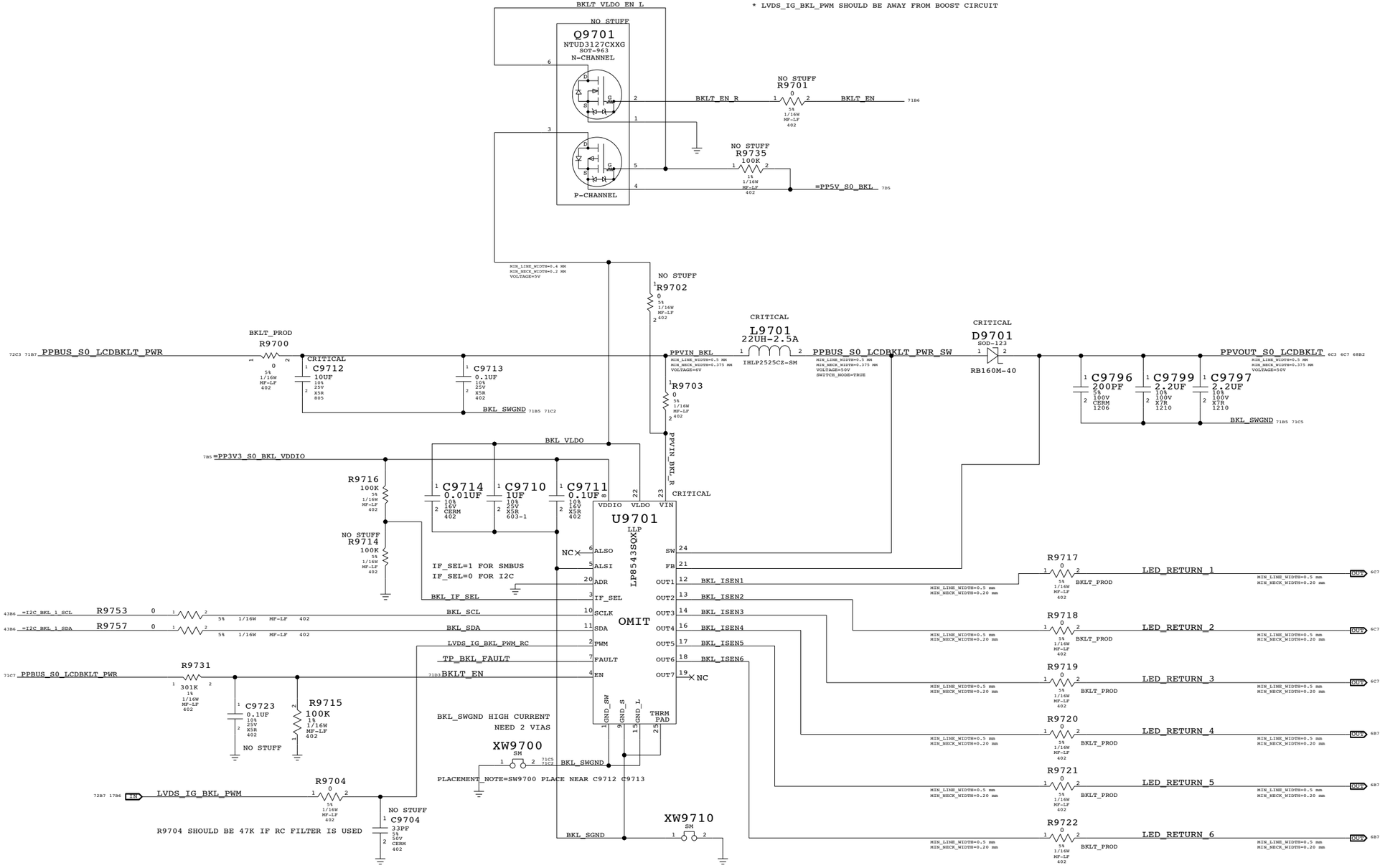
DisplayPort Connector

SYNC_MASTER=AMASON SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 70 OF 81	

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

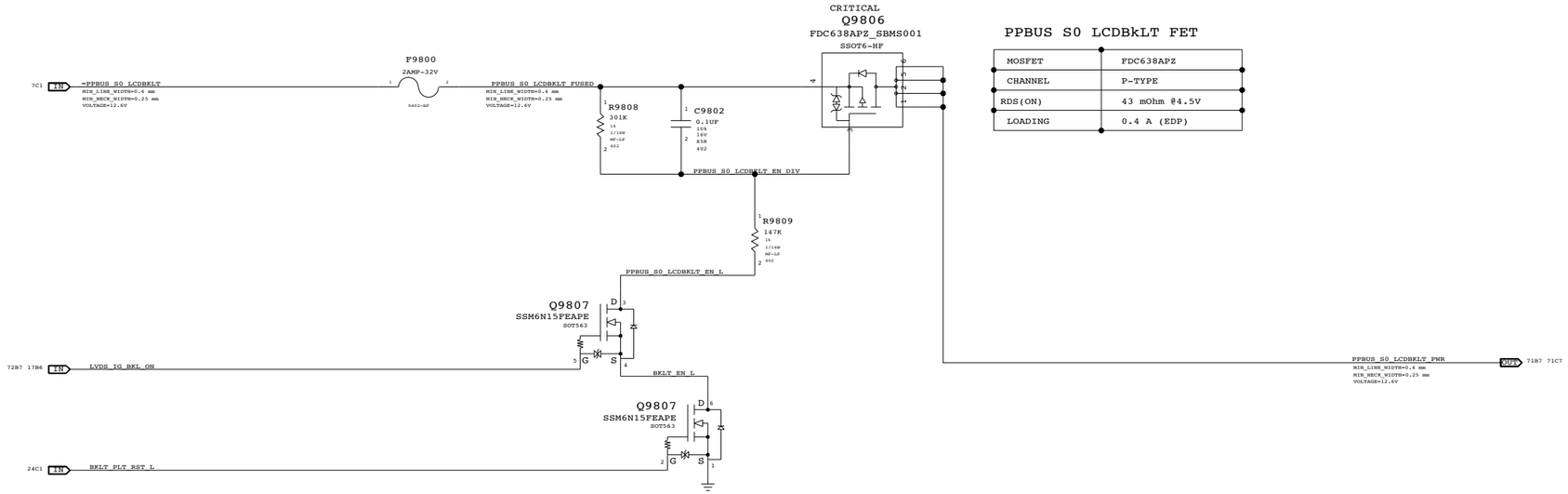
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

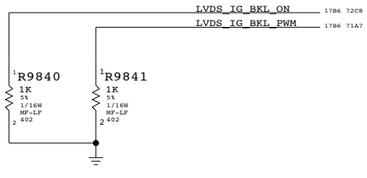
LCD BACKLIGHT DRIVER

SYNC_MASTER=KIRAN SYNC_DATE=12/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 71 OF 81	





MCP HAS INTERNAL 10K PULL-UP FOR THESE SIGNALS

LCD Backlight Support

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 72 OF 81	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9C4 13D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C3 13D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9C2 13B3 13C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C6 13D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9D8 13B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9C8 9D8 13C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9D6 13B6
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9D6 13B6
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9D6 13B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9D6 13B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9D6 13B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9D6 12C2 13A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9D6 13A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9D6 13B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9C8 13A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8B2 9B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9C8 13B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9C8 13A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9D6 13A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9C8 13A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9B8 13A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9C5 13B6 41D4 62C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9B2 12C7 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9B8 13A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9C8 13A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9C6 13B7 41C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9B2 13A3
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9B2 13A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9B2 13A3 62C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9B2 13A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 13B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	12C3 13B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	12C3 13B3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20C7 62D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	62C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9B4 25B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	9B6 9C6 12B3
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9B6 9C6 12B3
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	9B6 9C6 12B3
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	9A6 9C6 12B6
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	9A6 9C6 12B3
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	9C6 12C6
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	9C5 12C6
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	12C4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10B6 62C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10B5 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A5 62A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

CPU/FSB Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 73 OF 81	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	14B5 26C5 26C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	14A5 26D5 26D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	14B5 26C5 26C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	14B5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	14B5 14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	14C5 26C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	14C5 26C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	14C5 26C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	14C5 26C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	14B7 26C2 26C4 26D2 26D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	14B7 26C2 26C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	14B7 14C7 26B2 26B4 26C2 26C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	14C7 26C2 26C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	14C7 26B5 26B7 26C5 26C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	14C7 14D7 26B5 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	14D7 26B5 26B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	14D7 26A5 26A7 26B5 26B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	14A7 26C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	14A7 26C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	14B7 26B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	14B7 26C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	14B7 26B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	14B7 26B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	14B7 26B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	14B7 26A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	14D5 26C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	14D5 26D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	14D5 26C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	14D5 26C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	14D5 26B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	14D5 26C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	14D5 26C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	14D5 26C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	14D5 26B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	14D5 26B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	14D5 26B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	14D5 26B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	14D5 26B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	14D5 26B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	14D5 26A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	14D5 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	14B1 27C5 27C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	14A1 27D5 27D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	14B1 27C5 27C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	14B1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	14B1 14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	14C1 27C5 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	14C1 27C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	14C1 27C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	14C1 27C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	14B3 27C2 27C4 27D2 27D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	14B3 27C2 27C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	14B3 14C3 27C2 27C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	14C3 27B2 27B4 27C2 27C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	14C3 27B5 27B7 27C5 27C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	14C3 14D3 27B5 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	14D3 27B5 27B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	14D3 27A5 27A7 27B5 27B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	14A3 27C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	14A3 27C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	14B3 27C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	14B3 27B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	14B3 27B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	14B3 27B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	14B3 27B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	14B3 27A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	14D1 27C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	14D1 27D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	14D1 27C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	14D1 27C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	14D1 27C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	14D1 27B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	14D1 27C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	14D1 27B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	14D1 27B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	14D1 27B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	14D1 27B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	14D1 27B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	14D1 27B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	14D1 27A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	14D1 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15C6

Memory Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

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D	051-7898	4.7.0
SCALE: NONE	SHT 74 OF 81	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	6D5 29C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	6D5 29C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16B3 29C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16B3 29C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	6D5 16B6 29C7
	PCIE_90D	PCIE	PCIE_FW_R2D_P	34C3
	PCIE_90D	PCIE	PCIE_FW_R2D_N	34C3
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	16B3 34C1
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	16B3 34C1
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_N	16B6 34C1
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	34C3
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	34C3
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16C3 29C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	6D5 29C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	6D5 29C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	70C2 70C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	69D1 70C1 70C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	70C2 70C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17B6 69C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17B6 69C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	69C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	69C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	69C4 70C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	69D4 70C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17A6 23C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17A6 23C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6C7 68C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17B3 68B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6C7 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6C7 17B3 68C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6C7 17B3 68C2
T18 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	70C3 70C4 70C5
T18	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	70C3 70C4 70C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17A3 23C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17A3 23C6
SATA_HDD_R2D	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_P	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_C_N	19D6 37A2
	SATA_90D_HDD	SATA	SATA_HDD_R2D_P	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_N	6B7 37A5
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_P	37A4
	SATA_90D_HDD	SATA	SATA_HDD_R2D_UF_N	37A4
SATA_HDD_D2R	SATA_90D_HDD	SATA	SATA_HDD_D2R_P	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_N	19D6 37B2
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_P	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_C_N	6B7 37B5
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_P	37B4
	SATA_90D_HDD	SATA	SATA_HDD_D2R_UF_N	37B4
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_C_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_R2D_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_N	6A7 6B7 37C6
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	37C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_N	19D6 37C3
	SATA_100D	SATA	SATA_ODD_D2R_C_P	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_C_N	6B7 37C6
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	37C4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	37C4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19A6

MCP Constraints 1

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

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D	051-7898	4.7.0
SCALE: NONE	SHT 75 OF 81	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	12C3 18D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	18D2 18D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	18D2 18D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	18C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	18C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	18B3 40C8 42D3 42D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	18C3 40C8 42D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	18C3 24D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	18B3 24B4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	24B1 40C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	24B1 42D3
USB_EXTA	USB_90D	USB	USB_EXTA_P	19D3 38A8
	USB_90D	USB	USB_EXTA_N	19D3 38A8
	USB_90D	USB	USB_EXTA_MUXED_P	38C4
	USB_90D	USB	USB_EXTA_MUXED_N	38C4
	USB_90D	USB	CONN_USB_EXTA_P	38C3
	USB_90D	USB	CONN_USB_EXTA_N	38C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	19D3 29B5
	USB_90D	USB	USB_CAMERA_N	19D3 29B5
	USB_90D	USB	USB_CAMERA_CONN_P	6D5 29B7
	USB_90D	USB	USB_CAMERA_CONN_N	6D5 29B7
USB_BT	USB_90D	USB	USB_BT_P	19D3 29B5
	USB_90D	USB	USB_BT_N	19C3 29B5
	USB_90D	USB	CONN_USB2_BT_P	6D5 29B7
	USB_90D	USB	CONN_USB2_BT_N	6D5 29B7
USB_TPAD	USB_90D	USB	USB_TPAD_P	19D3 48B8
	USB_90D	USB	USB_TPAD_N	19D3 48B8
	USB_90D	USB	USB_TPAD_R_P	48B7
	USB_90D	USB	USB_TPAD_R_N	48B7
USB_IR	USB_90D	USB	USB_IR_P	19D3 39D7
	USB_90D	USB	USB_IR_N	19D3 39D7
USB_EXTB	USB_90D	USB	USB_EXTB_P	19C3 38A4
	USB_90D	USB	USB_EXTB_N	19C3 38B4
	USB_90D	USB	CONN_USB_EXTB_P	38B3
	USB_90D	USB	CONN_USB_EXTB_N	38B3
USB_SD	USB_90D	USB	USB_CARDREADER_P	19C3 30C7
	USB_90D	USB	USB_CARDREADER_N	19C3 30C7
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	19C4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	12B6 20C3 43D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	12B6 20C3 43D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	20C3 43B8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	20C3 43B8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	20D2 52C7
	HDA_55S	HDA	HDA_BIT_CLK_R	20A7 20D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	20D2 52C7
	HDA_55S	HDA	HDA_SYNC_R	20A7 20D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	20A7 20D4
	HDA_55S	HDA	HDA_RST_L	20D2 52C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	20D7 52C7
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	20D2 52C7
	HDA_55S	HDA	HDA_SDOUT_R	20A7 20D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	20C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	20B3 24B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24B1 40C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	20B3 42A5 42C8
	SPI_55S	SPI	SPI_CLK	51C5
	SPI_55S	SPI	SPI_ALT_CLK	42C5 42D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	20B3 42A5 42C7
	SPI_55S	SPI	SPI_MOSI	51C4
	SPI_55S	SPI	SPI_ALT_MOSI	42C5 42D5
SPI_MISO	SPI_55S	SPI	SPI_MISO	20B3 42A5 42B7
	SPI_55S	SPI	SPI_MISO_R	51C4
	SPI_55S	SPI	SPI_ALT_MISO	42B5 42D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	20B3 42B7
	SPI_55S	SPI	SPI_CS0_L	
	SPI_55S	SPI	SPI_CS1_R_L	
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB	

MCP Constraints 2

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE: NONE SHT 76 OF 81

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	17C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	17C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	17C3 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	31B6 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	17C3 31B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	17D3 31B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	31C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	17D6 31C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	31C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	17D6 31C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	17D6 31C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	17D6 31B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	31B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	31C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	17D3 31C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	17D3 31C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	17D3 31B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L	17C3 31B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	31B3 33B8 33C8
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	33B4 33C4 33C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	33B4 33C4 33C5

Ethernet Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 77 OF 81	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	7

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	7

FireWire Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P 34B6 36C4
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N 34C6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P 34B6 36C4
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N 34B6 36C4
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P 34B6 36B8
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N 34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P 34B6 36B8
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N 34B6 36B8
Port 2 Not Used			

SD CARD NET PROPERTIES

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I23 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0> 30C2
I24 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1> 30C2
I25 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2> 30C2
I26 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3> 30C2
I27 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4> 30C2
I28 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5> 30C2
I29 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6> 30C2
I30 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7> 30C2
I32 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK 30C2
I31 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD 30C2

FireWire Constraints

SYNC_MASTER=K19_MLB SYNC_DATE=12/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 78 OF 81	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	6C5 6D5 43D2
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	6C5 6D5 43D2
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	43C2
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	43C2
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	43D5
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	43D5
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	6A7 43C5
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	6A7 43C5
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	43B5
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	43B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 79 OF 81	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	45A8 59B3
	DIFFPAIR		CHGR_CSO_R_N	45A8 59B3
	DIFFPAIR		CPUTHMSNS_D2_P	46C5
	DIFFPAIR		CPUTHMSNS_D2_N	46C5
	DIFFPAIR		CPU_THERMD_P	9C6 46D5
	DIFFPAIR		CPU_THERMD_N	9C6 46D5
	DIFFPAIR		ISNS_CPUVTT_P	45B7
	DIFFPAIR		ISNS_CPUVTT_N	45B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	
	DIFFPAIR		ISNS_P1V5S0MCP_N	
	DIFFPAIR		ISNS_PVCORES0MCP_P	
	DIFFPAIR		ISNS_PVCORES0MCP_N	
	DIFFPAIR		MCPTHMSNS_D2_P	4C7 46B5
	DIFFPAIR		MCPTHMSNS_D2_N	4C7 46B5
	DIFFPAIR		MCP_THMDIODE_P	20C3 46B5
	DIFFPAIR		MCP_THMDIODE_N	20C3 46B5

K24 SPECIAL CONSTRAINTS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0
SCALE: NONE	SHT 80 OF 81	

K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

K24 RULE DEFINITIONS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7898	4.7.0

SCALE	SHT	OF
NONE	81	81