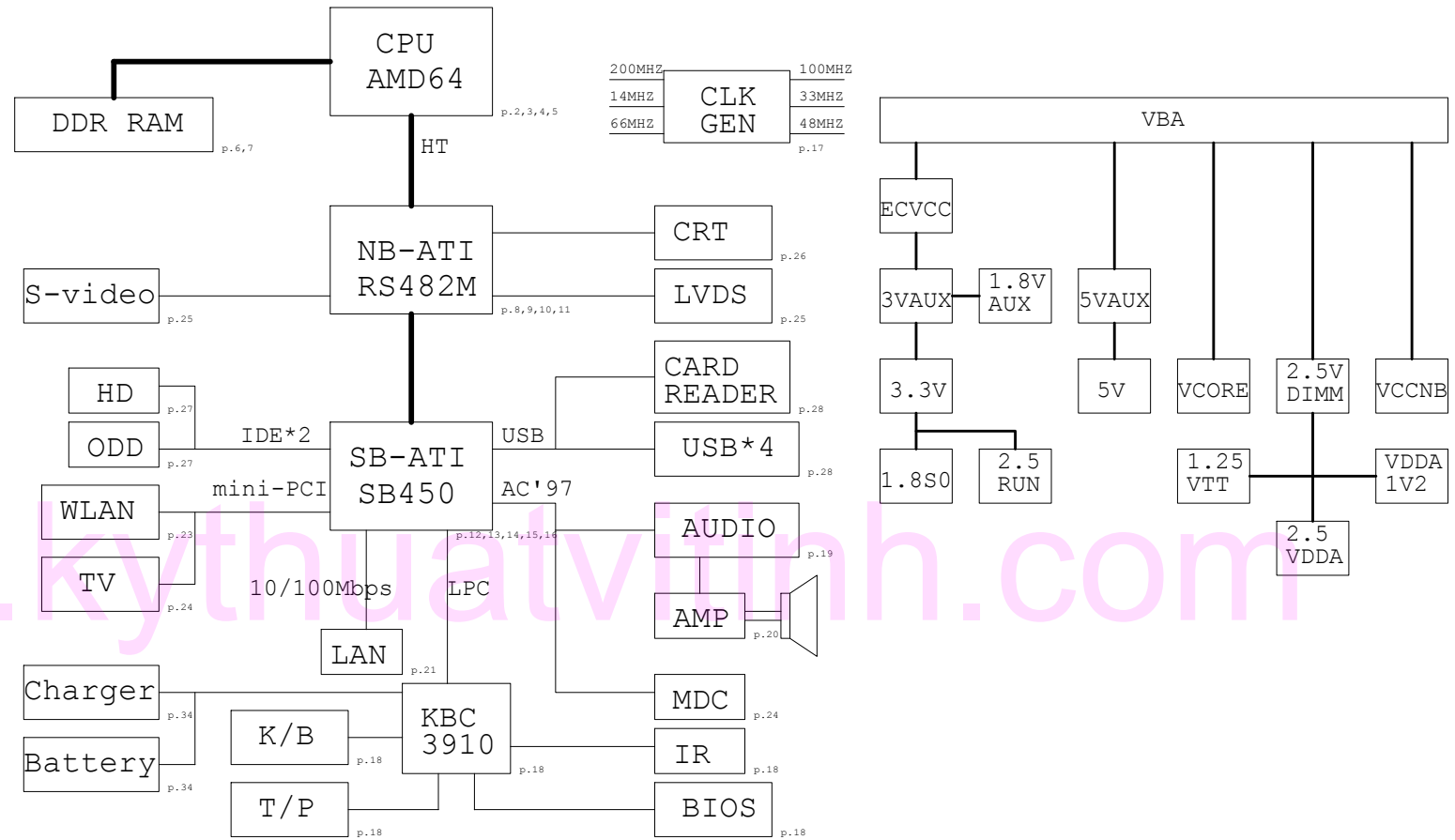
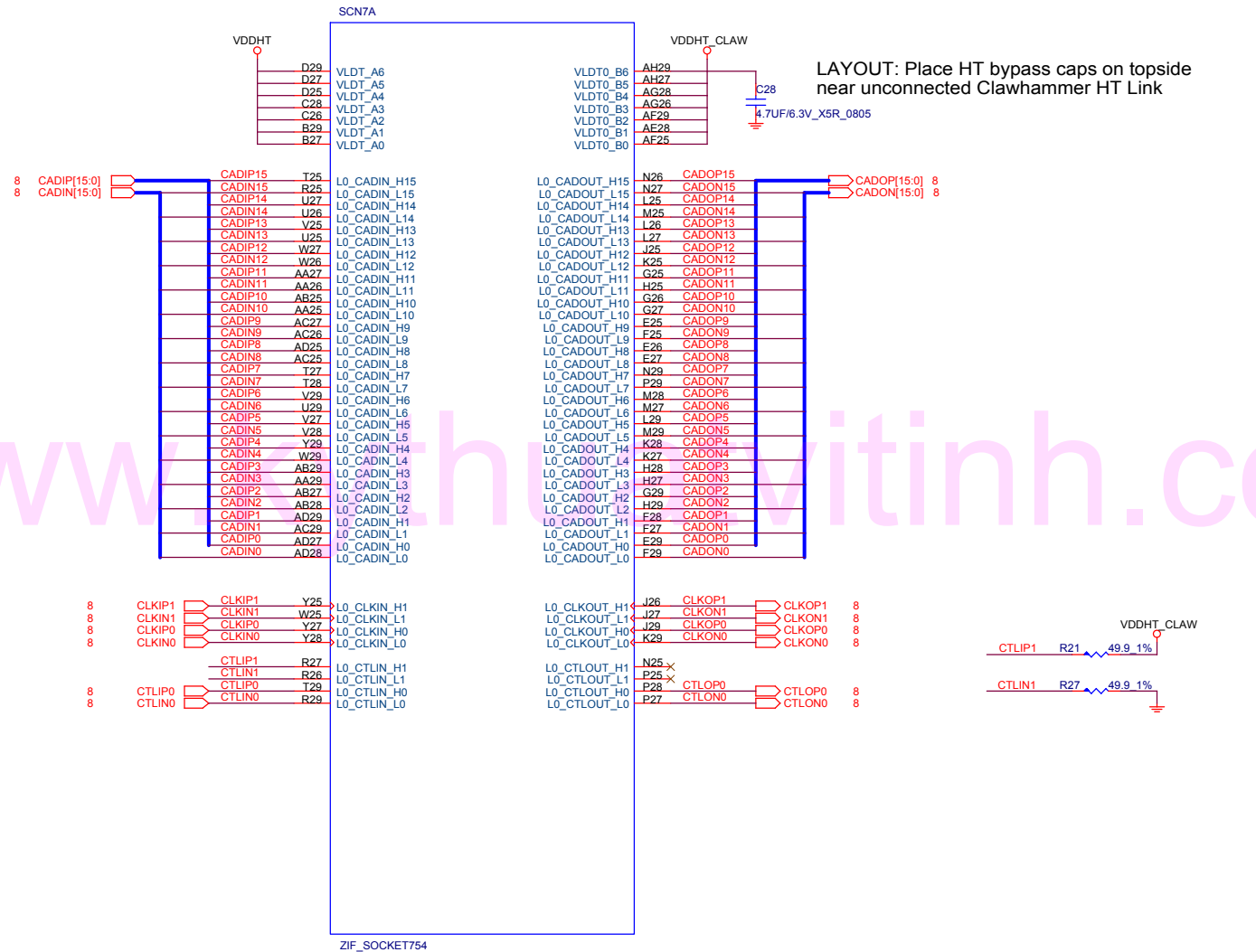


- 01 COVER PAGE
- 02_AMD K8 CPU1
- 03_AMD K8 CPU2
- 04_AMD K8 CPU3
- 05_AMD K8 CPU4
- 06_DDR SO_DIMM
- 07_DDR TERMINATION & DECOUP
- 08_RS480M-HT LINK0 I/F
- 09_RS480M-PCIE LINK I/F
- 10_RS480M-VIDEO I/F & CLKGEN
- 11_RS480M-POWER
- 12_SB400-PCI/CPU/LPC/RTC
- 13_SB400-ACPI/GPIO/AC97/USB
- 14_SB400-SATA/IDE
- 15_SB400-PWR & DECOUPLING
- 16_SB400-STRAPS
- 17_CLOCK GENERATOR
- 18_KB3910
- 19_ALC655
- 20_OPA & AUDIO JACK
- 21_RTL8100B
- 22_RJ45 & RJ11
- 23_MINI PCI CONN. (WLAN)
- 24_MINI PCI CONN. (TV) & MDC
- 25_LCD & TV CONN.
- 26_CRT CONN.
- 27_HDD & CDROM CONN.
- 28_USB PORT
- 29_LED & LID
- 30_ASIC8M
- 31_PWRGD/RESET/SYSTEM POWER
- 32_THROUGH HOLE
- 33_DCIN&SELECT
- 34_CHARGER_MB3887
- 35_SYSTEM_MAX1999
- 36_VCORE_MAX1544
- 37_VDIMM & DDRVTT_MAX1714
- 38_NB_VCORE & SB1.8V_MAX1714
- 39_REVISION HISTORY

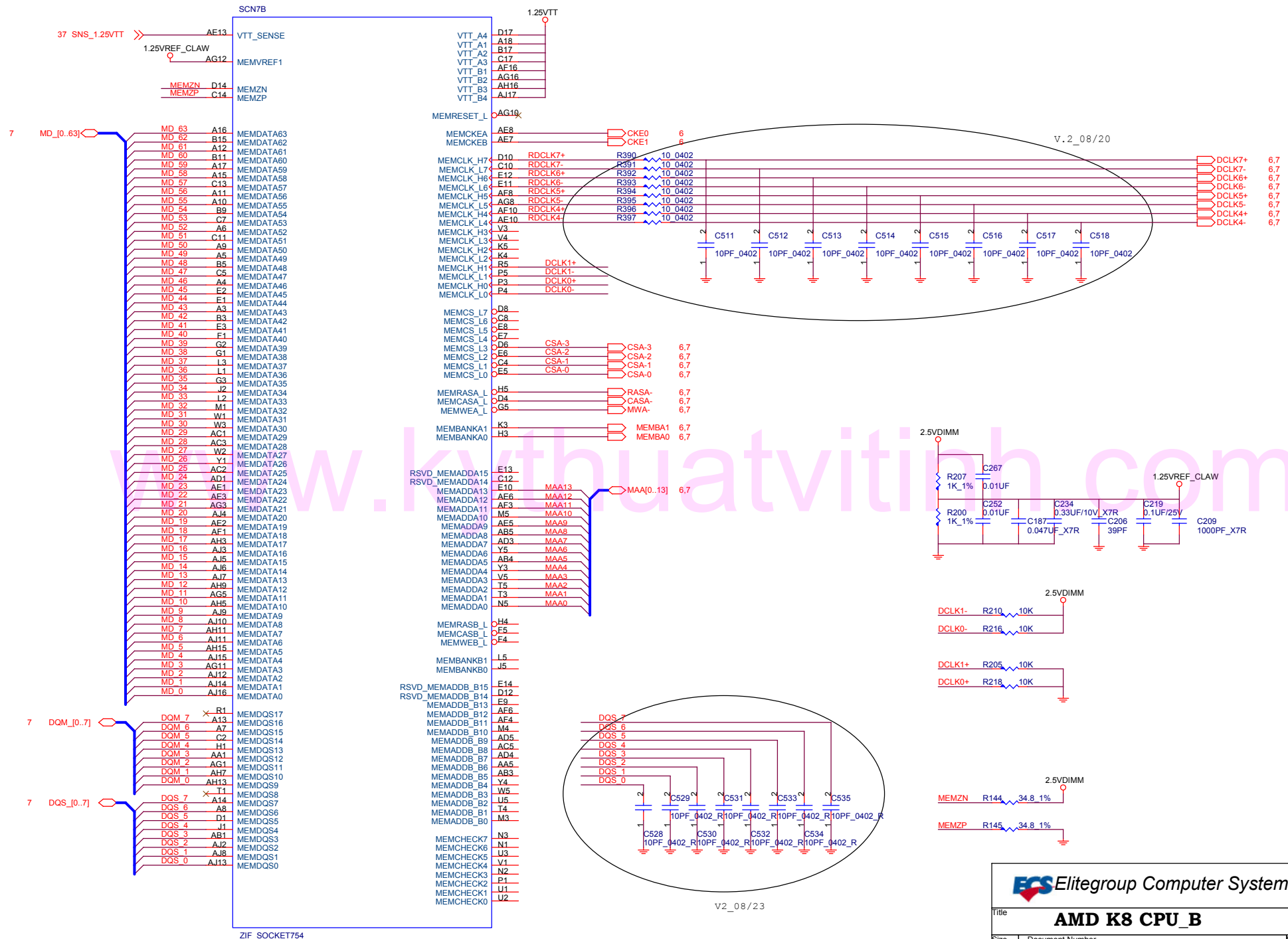


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REV	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
DATE	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20

PAGE	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
REV	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
DATE	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20	10/20



Clawhammer DDR Interface



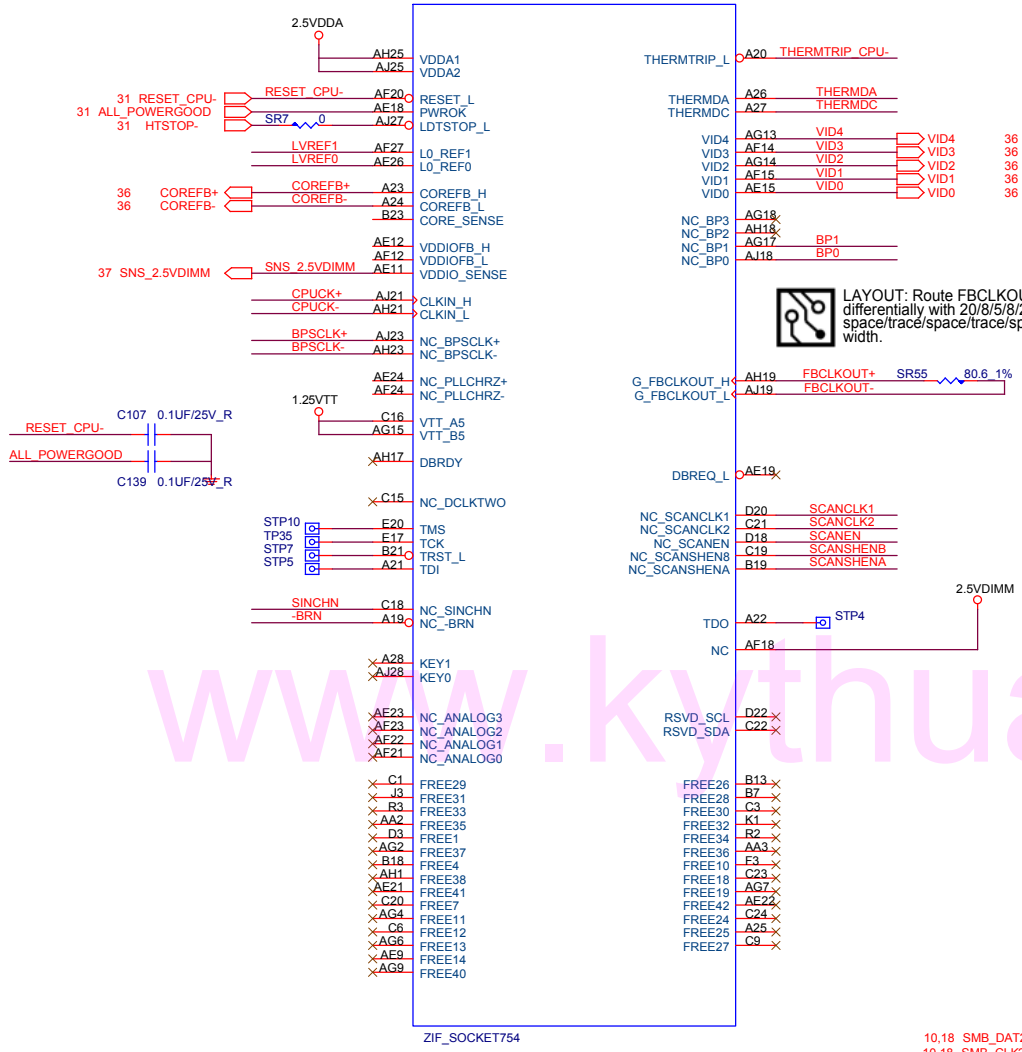
Elitegroup Computer Systems

Title: **AMD K8 CPU_B**

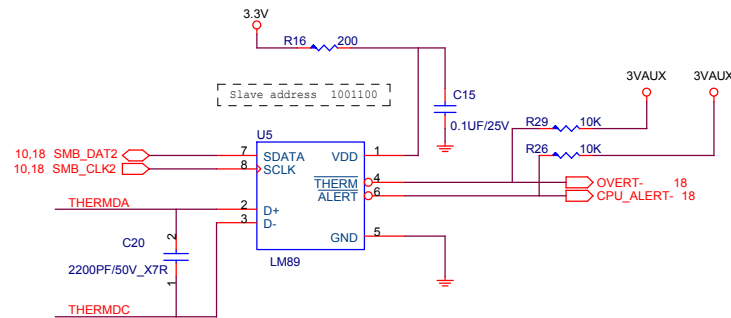
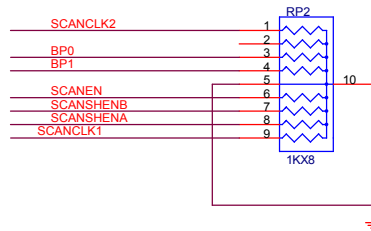
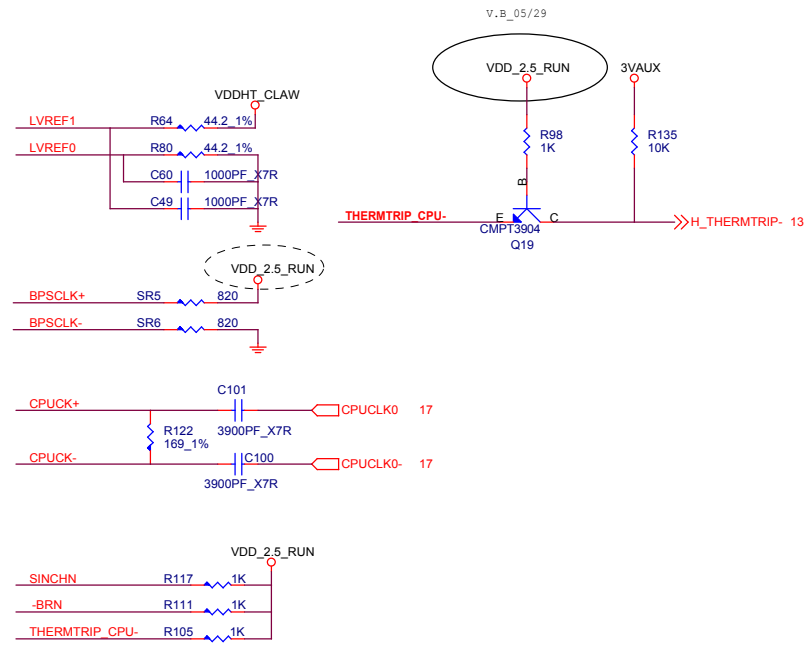
Size C Document Number **331-1-4-01** Rev 2

Date: Thursday, October 27, 2005 Sheet 3 of 39

CPU1 的 PIN AJ25 改接 +2.5VDDA 電源

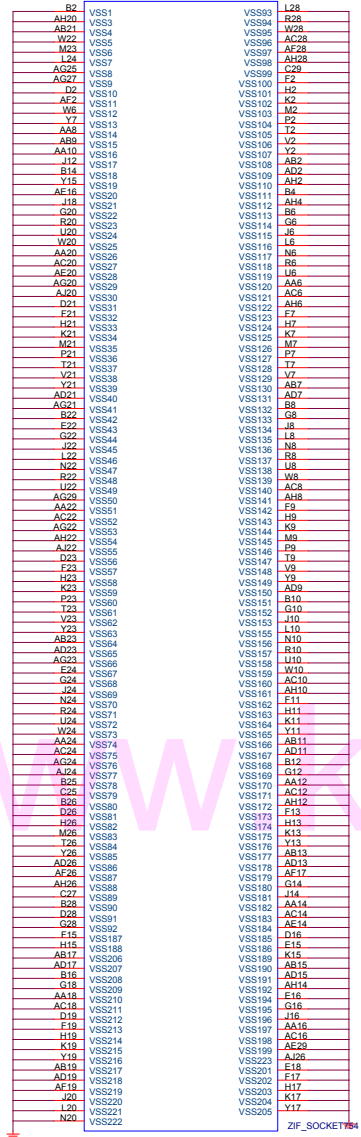
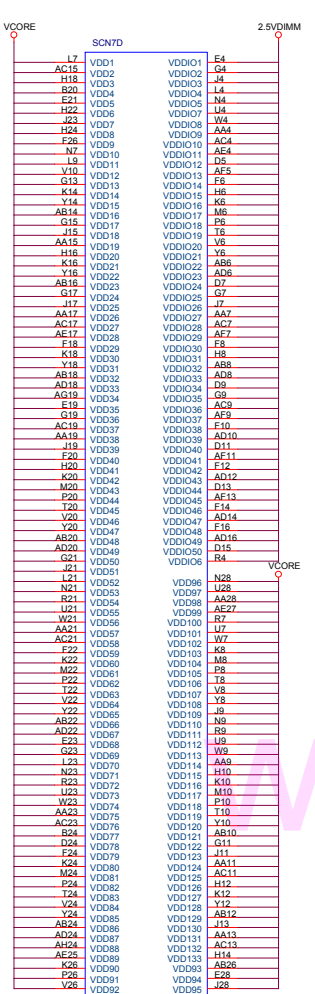


LAYOUT: Route FBCLKOUT+/- differentially with 20/8/5/8/20 space/trace/space/trace/space width.

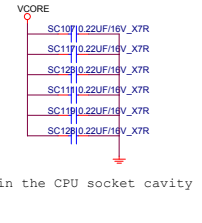
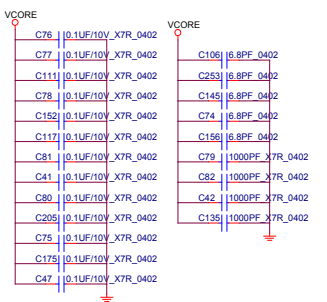


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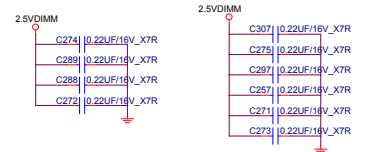
Clawhammer Power and Ground Connections



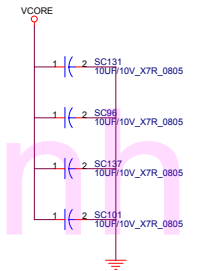
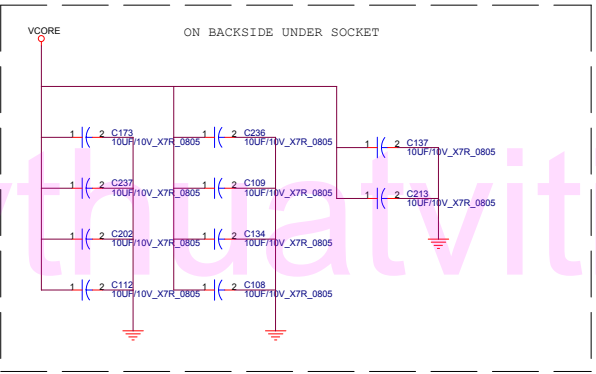
on backside under socket



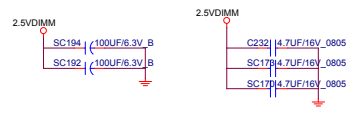
in the CPU socket cavity



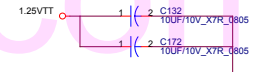
Place these capacitors near CPU socket



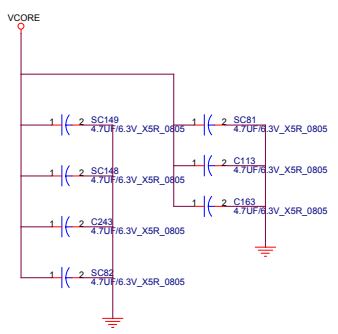
IN THE CPU SOCKET CAVITY



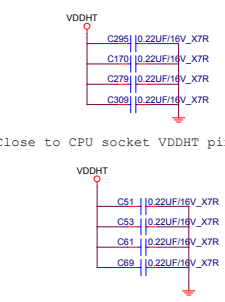
NEAR THE SO-DIMM SOCKET



On the each end of the SO-DIMM socket

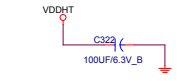


Place these capacitors close to socket

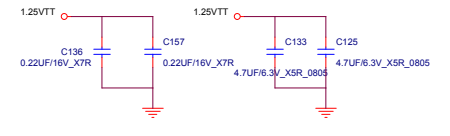


Close to CPU socket VDDHT pins within 1 inch

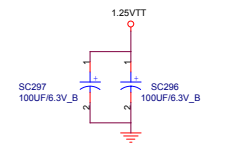
Close to NB VDDHT pins within 1 inch



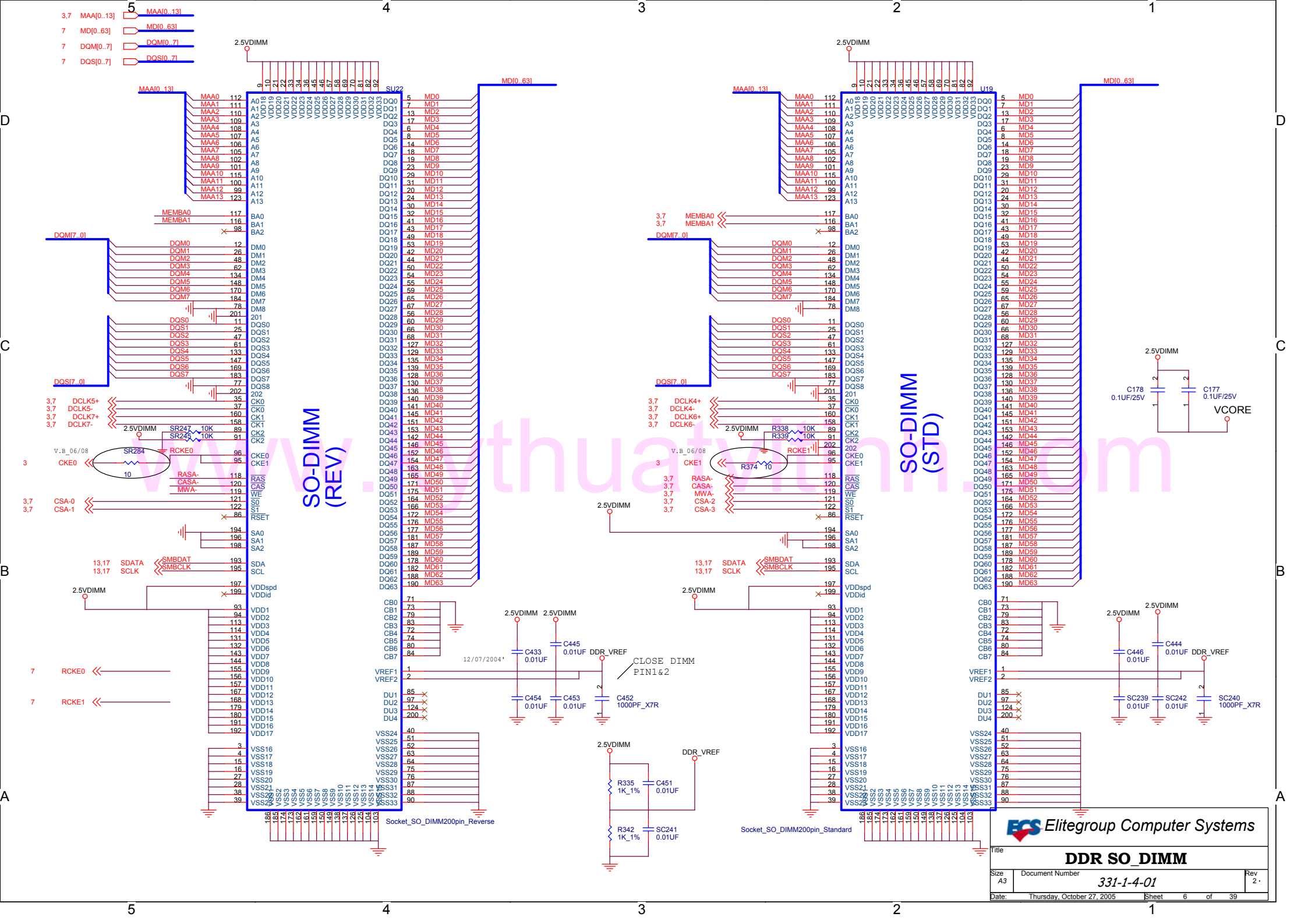
Near CPU socket on VDDHT pour



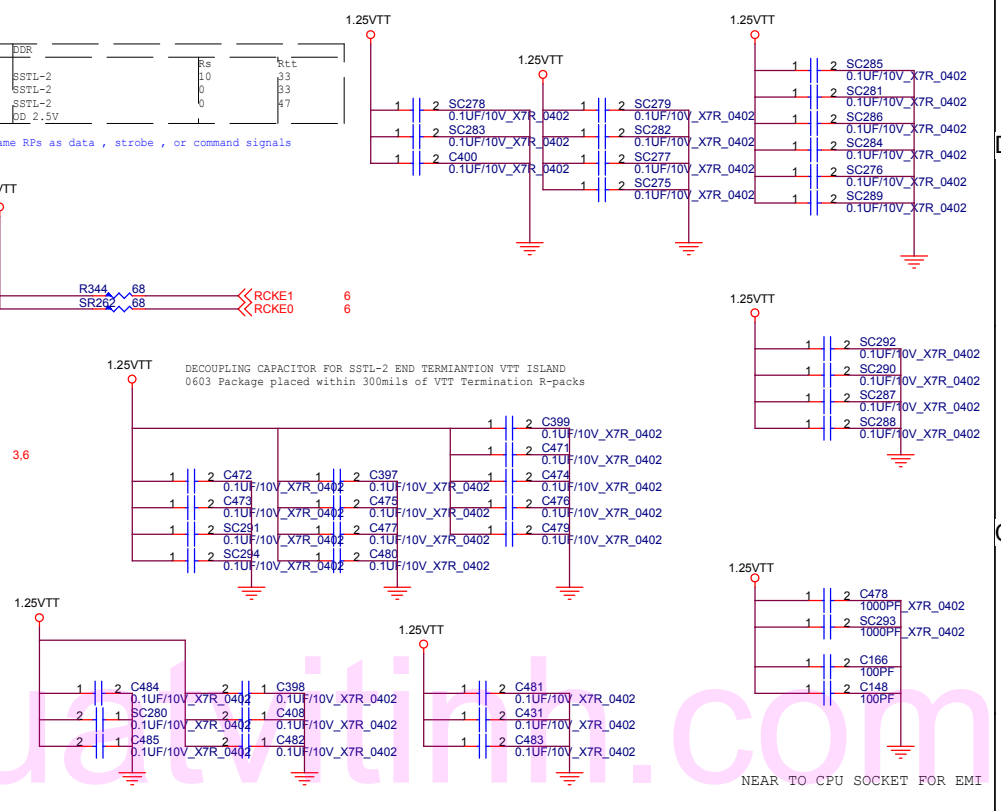
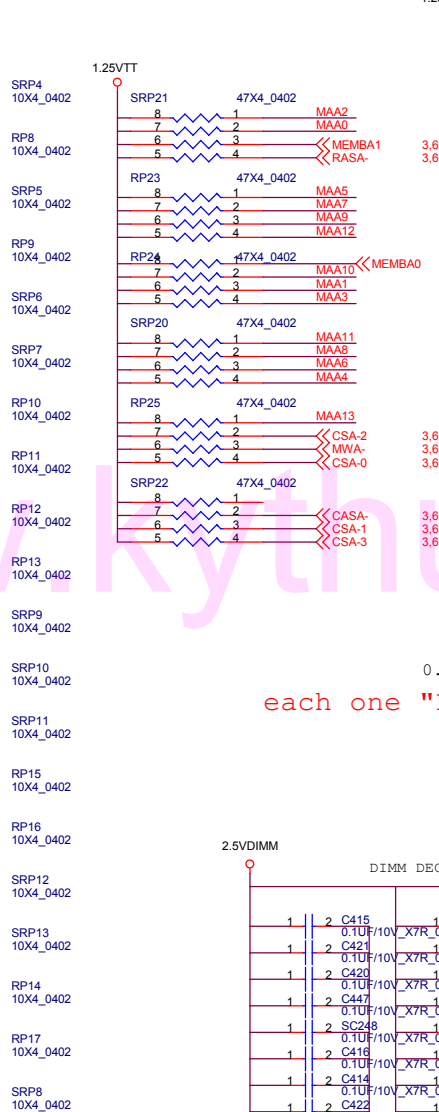
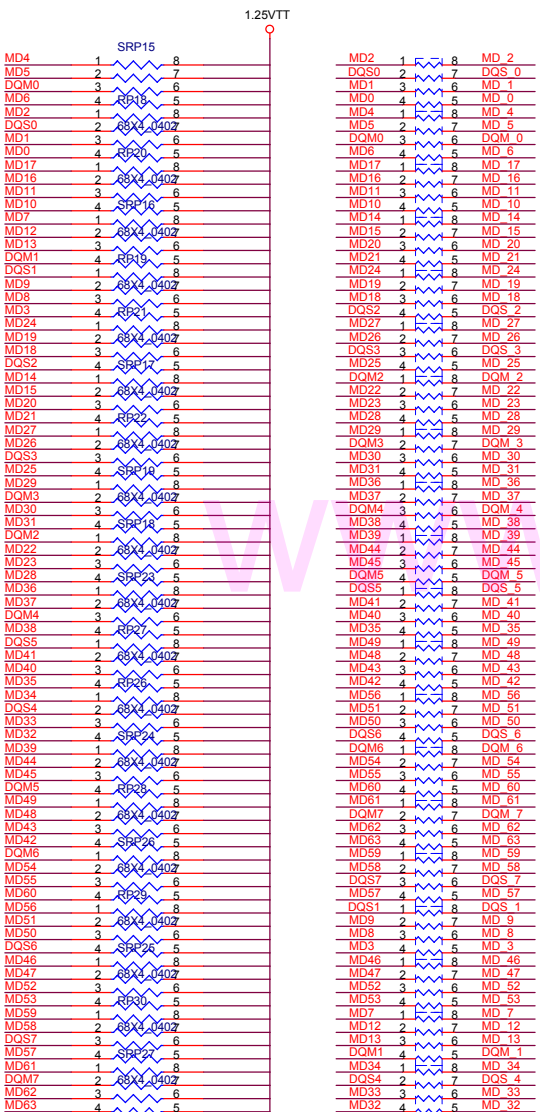
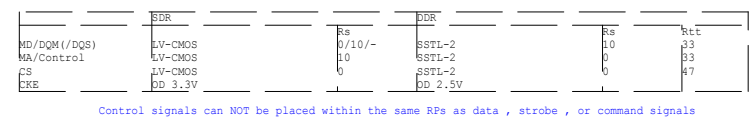
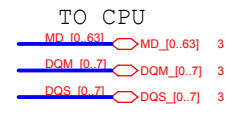
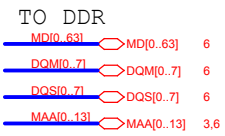
Place on the VTT fill



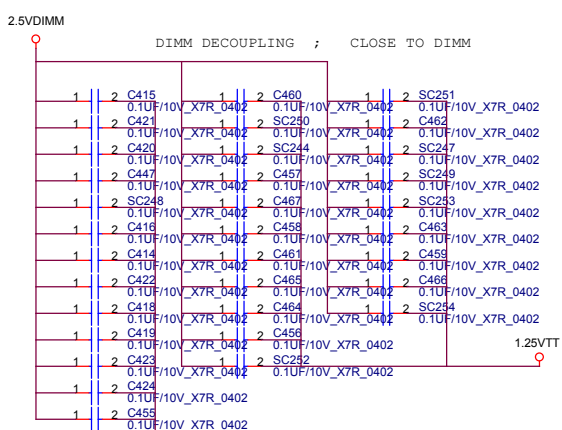
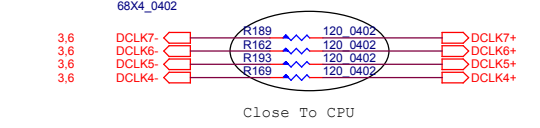
Close to CPU socket on the VTT fill



SSTL-2 Termination Resistors



each one "RPs" put two CAPS

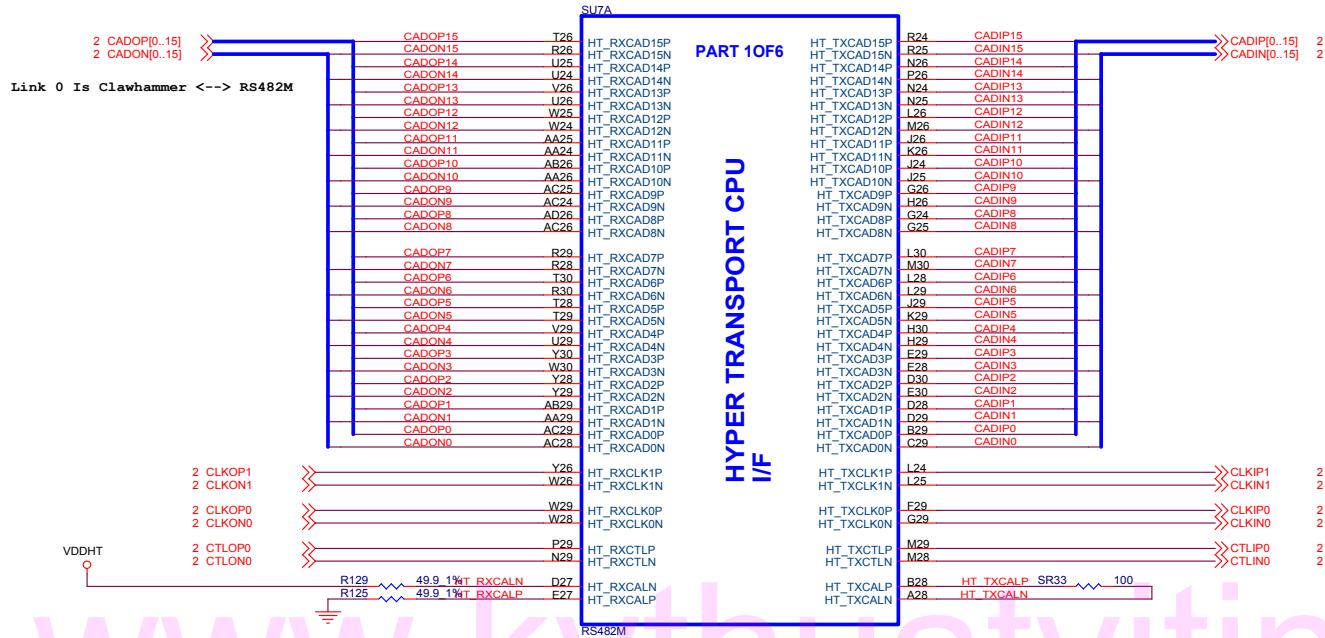


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DDR TERMINATION & DECOUP

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Date: Thursday, October 27, 2005 Sheet 7 of 39



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TP33	CADIP15	TP45	CADOP15
TP34	CADIN15	TP43	CADON15
TP46	CADIP14	TP50	CADOP14
TP49	CADIN14	TP47	CADON14
TP31	CADIP13	TP21	CADOP13
TP32	CADIN13	TP24	CADON13
TP39	CADIP12	TP52	CADOP12
TP40	CADIN12	TP53	CADON12
TP36	CADIP11	TP17	CADOP11
TP37	CADIN11	TP15	CADON11
TP29	CADIP10	TP58	CADOP10
TP30	CADIN10	TP82	CADON10
TP26	CADIP9	TP73	CADOP9
TP27	CADIN9	TP72	CADON9
TP22	CADIP8	TP76	CADOP8
TP23	CADIN8	TP74	CADON8
STP16	CADIP7	TP70	CADOP7
STP17	CADIN7	TP7	CADON7
STP13	CADIP6	TP4	CADOP6
STP15	CADIN6	TP8	CADON6
STP12	CADIP5	TP42	CADOP5
STP14	CADIN5	TP44	CADON5
TP11	CADIP4	TP1	CADOP4
TP12	CADIN4	TP3	CADON4
STP8	CADIP3	TP5	CADOP3
STP11	CADIN3	TP9	CADON3
STP6	CADIP2	TP60	CADOP2
STP9	CADIN2	TP56	CADON2
STP1	CADIP1	TP70	CADOP1
STP2	CADIN1	TP64	CADON1
TP13	CADIP0	TP71	CADOP0
TP14	CADIN0	TP65	CADON0
TP18	CTLIP0	TP48	CLKOP1
TP16	CTLIN0	TP51	CLKON1
TP28	CLKIP1	TP2	CLKOP0
TP25	CLKIN1	TP6	CLKON0
TP19	CLKIP0	TP41	CTLOP0
TP20	CTLIN0	TP38	CTLON0

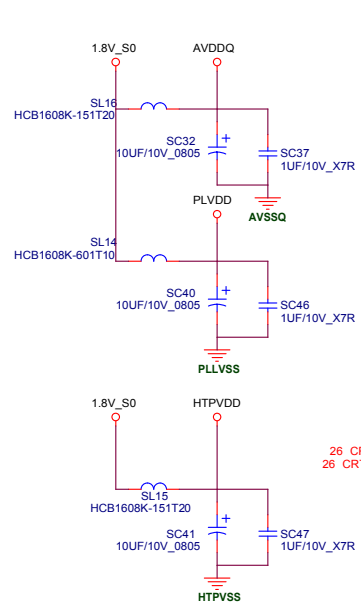


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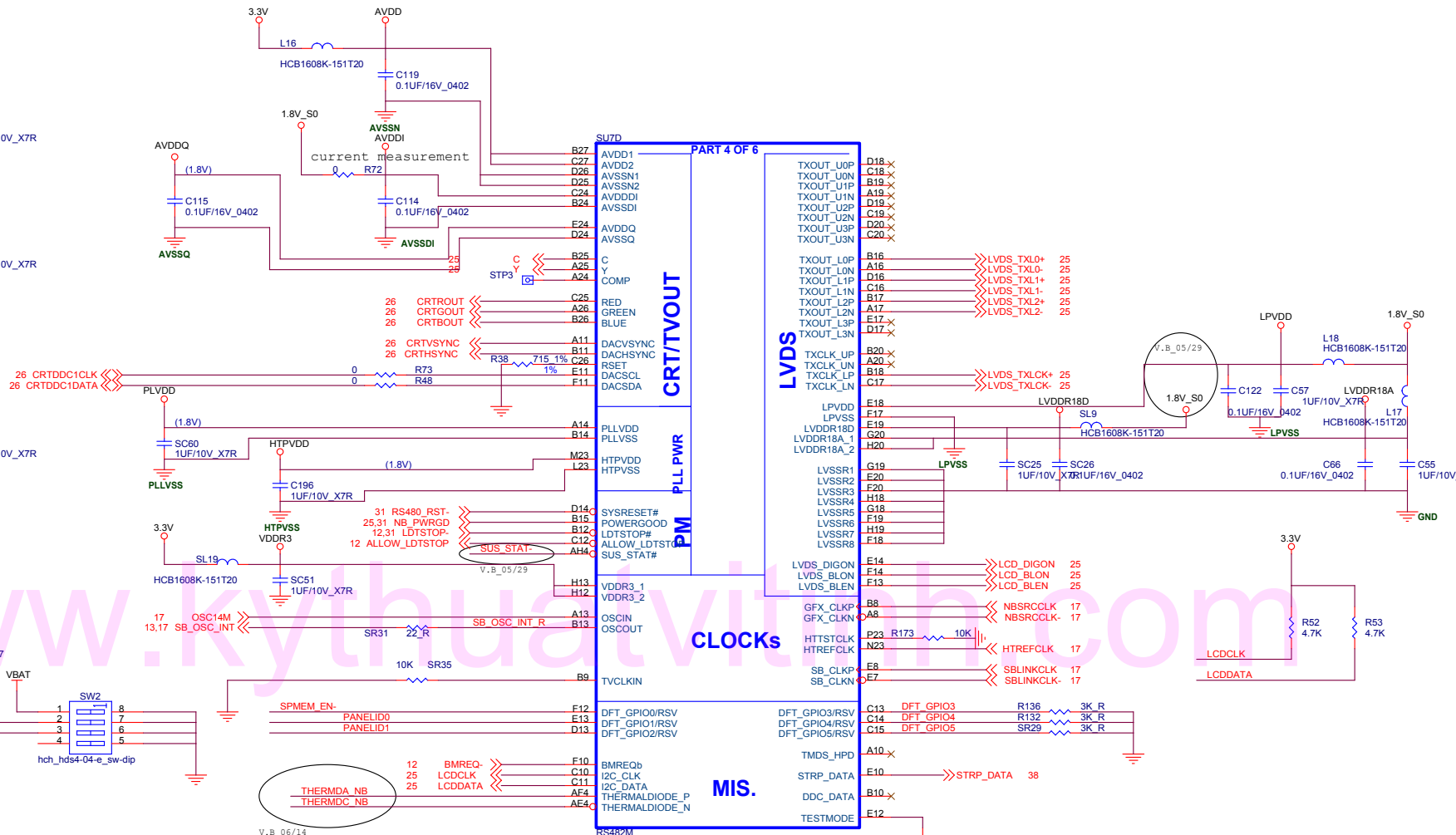
Close to NB



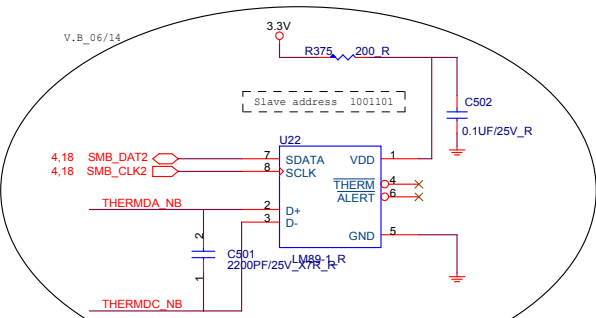
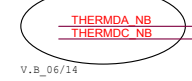
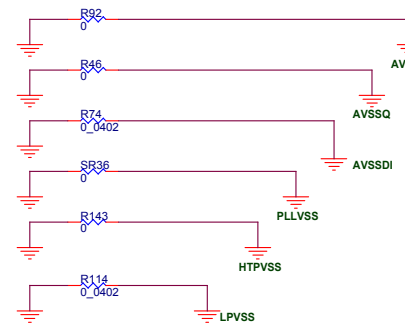
Put the TP200-287 exactly on the vias of NB



AVDD DAC VDD (3.3V)
AVDDDI DIGITAL VDD (1.8V)
AVDDQ DAC2 BANDGAP REF (1.8V)
PLLVD PLL VDD (1.8V)
HTPVDD HT PLL VDD (1.8V)



PUT AVDD, AVDDDI, AVDDQ, PLVDD, HTPVDD DECOUPLING CAPS ON THE BOTTOM, CLOSE TO BALLS

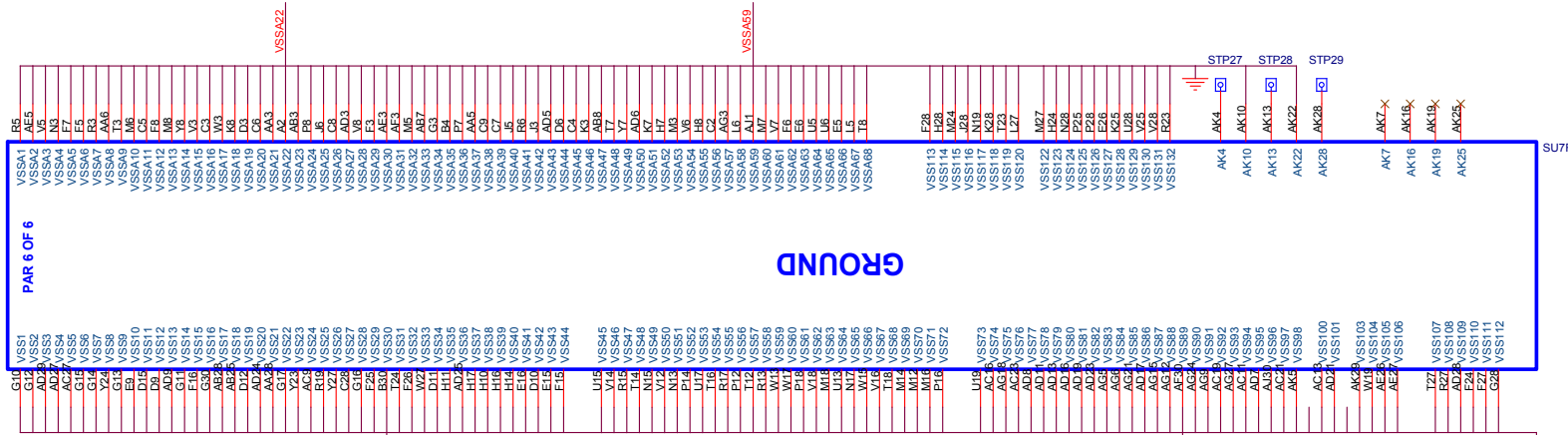


DO NOT SHARE GND VIA ON RESISTOR

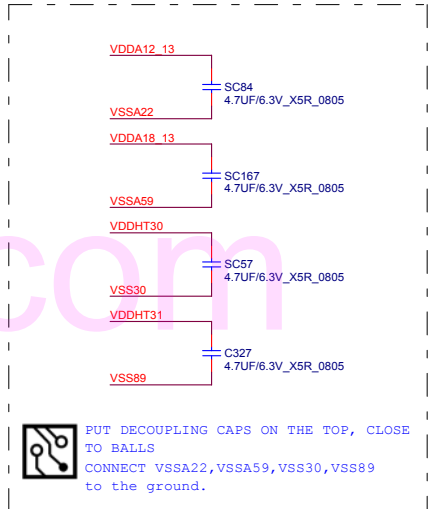
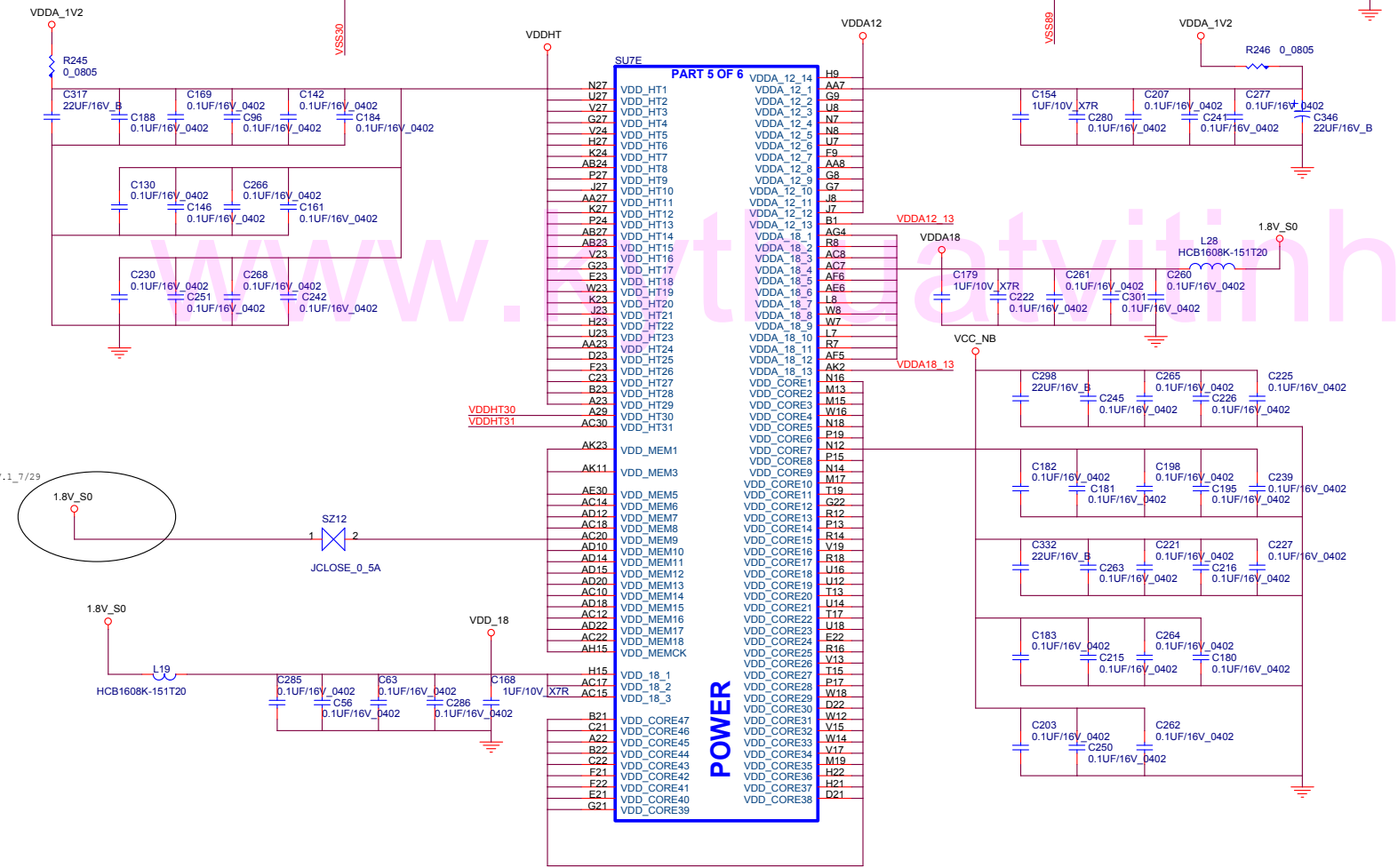
Elitegroup Computer Systems
 Title: **RS482M-VIDEO I/F & CLKGEN**
 Size: Custom Document Number: **331-1-4-01** Rev: 2
 Date: Thursday, October 27, 2005 Sheet 10 of 39

NB RS480 POWER STATES

NB RS482M POWER STATES



Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS TO GROUND.
CONNECT VSSA22, VSSA59, VSS30, VSS89 to the ground.

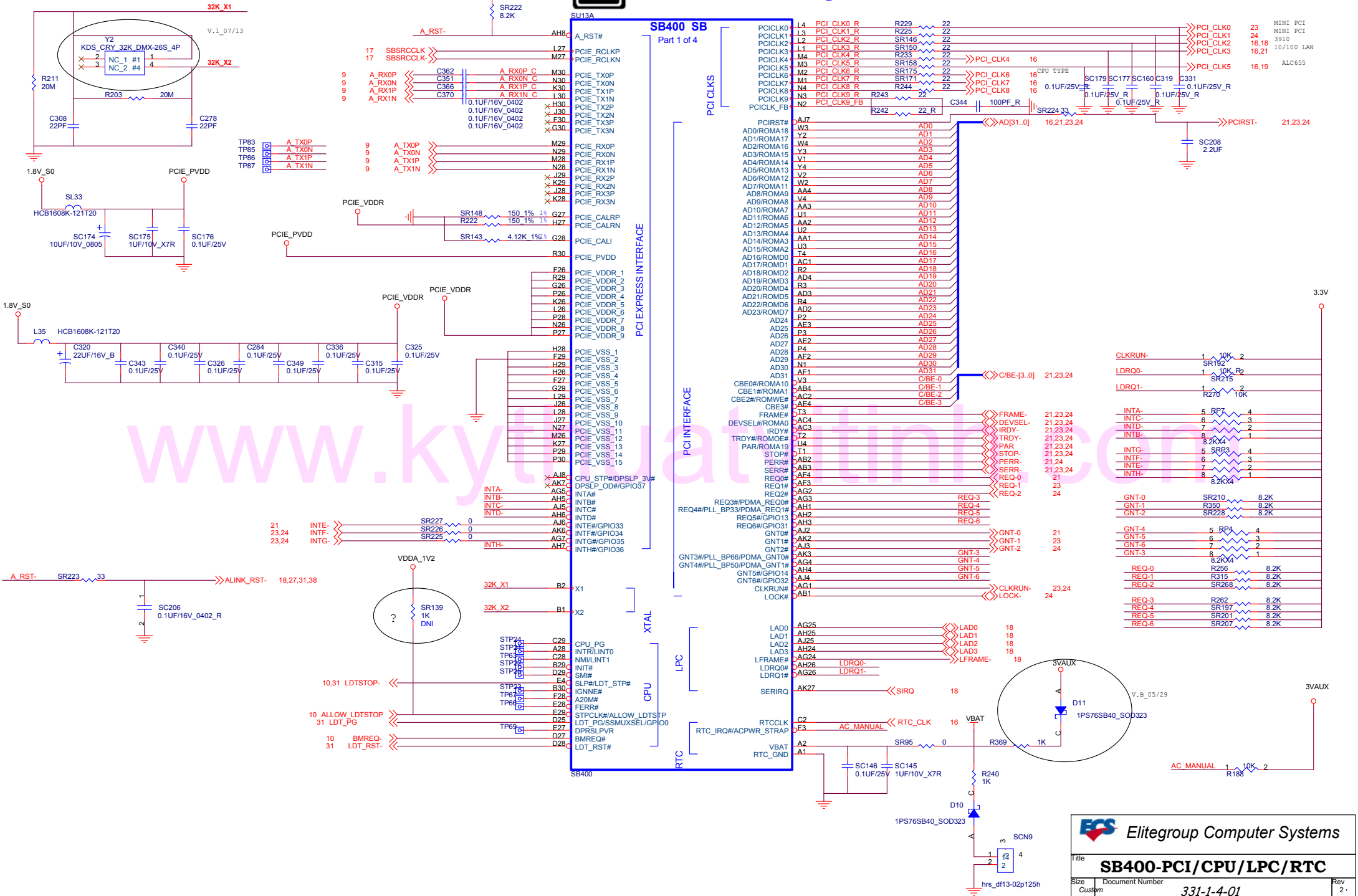
ECS Elitegroup Computer Systems

Title: **RS482M-POWER**

Size: **331-1-4-01**

Date: Thursday, October 27, 2005 Sheet 11 of 39

Note: For external RTC, remove Y600 and change R601 to 10K



LAYOUT GUIDE

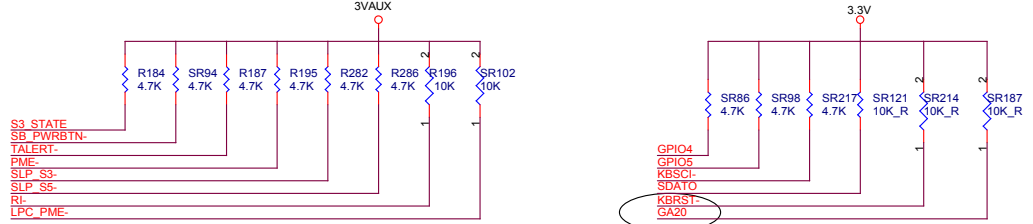
LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD MATCH THE AVERAGE OF THE OTHER SPCI_CLKS

ECS Elitegroup Computer Systems

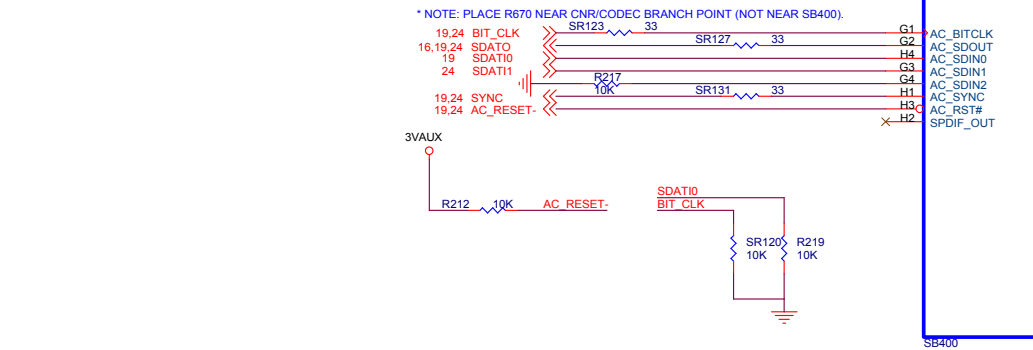
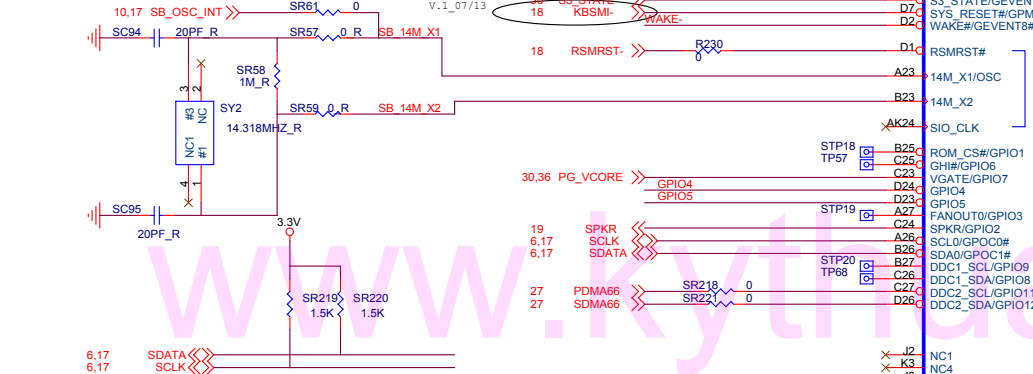
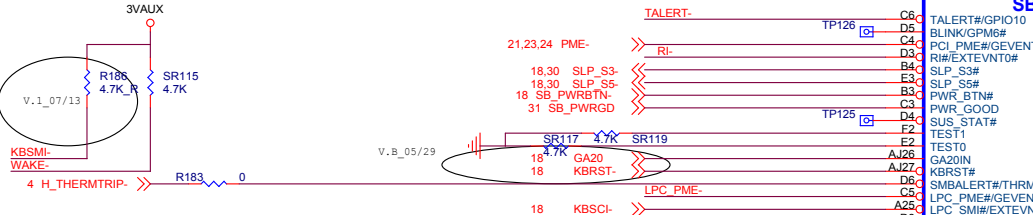
Title: **SB400-PCI/CPU/LPC/RTC**

Size: **Custbrm** | Document Number: **331-1-4-01** | Rev: **2**

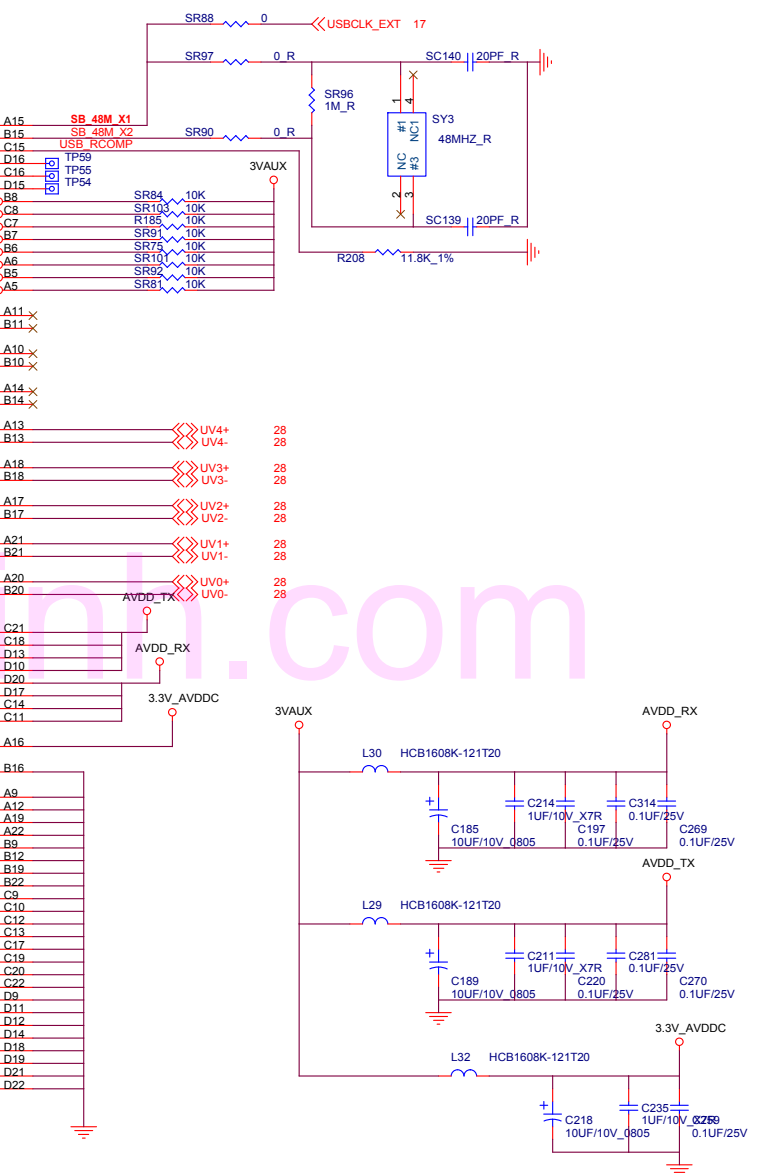
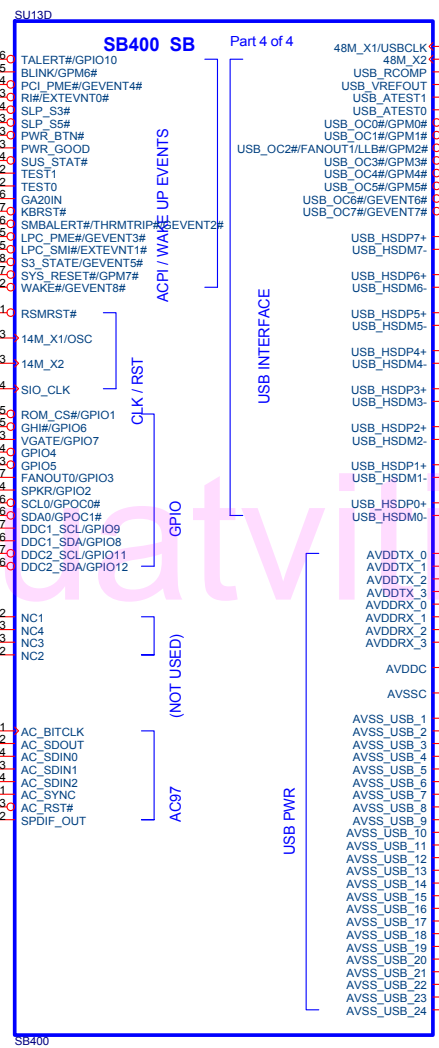
Date: Thursday, October 27, 2005 | Sheet: 12 of 39

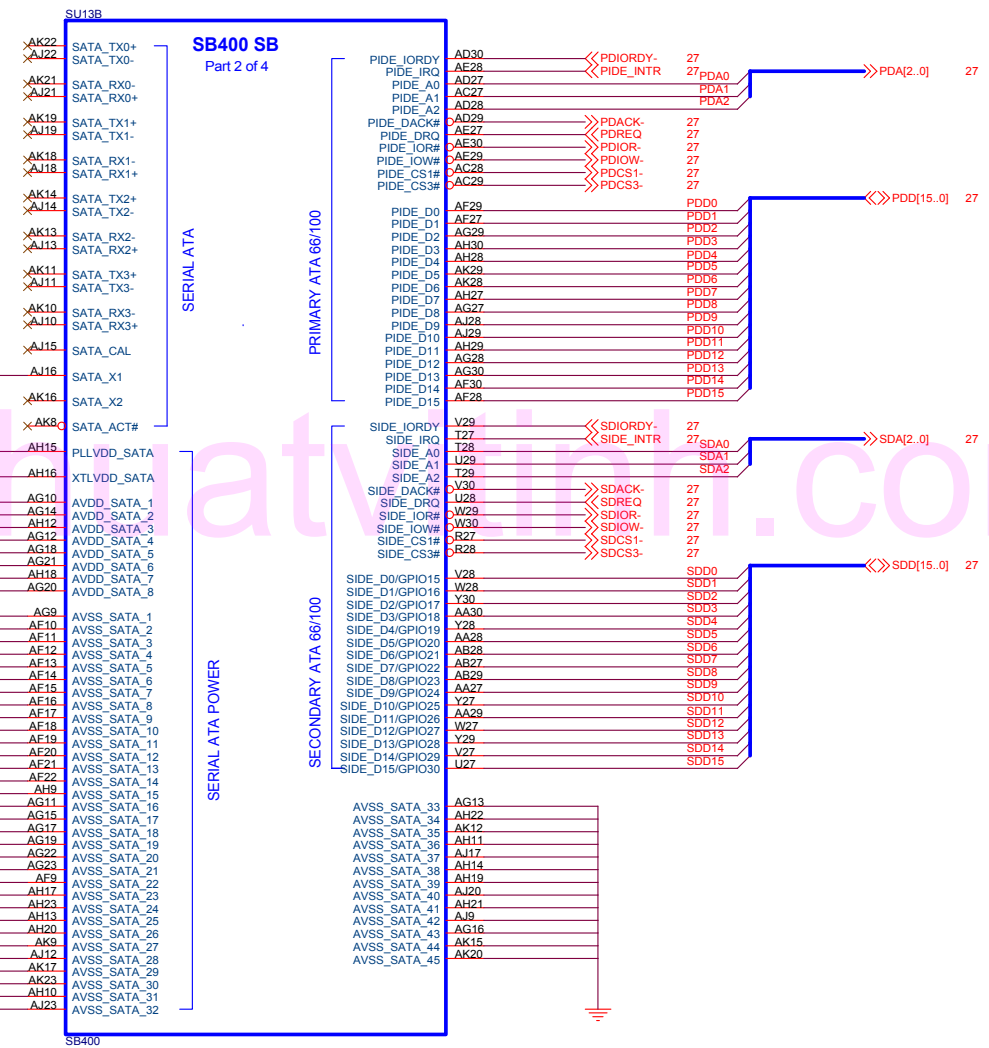


NOTE: ONLY USE FUNDAMENTAL MODE CRYSTAL



* NOTE: PLACE R670 NEAR CNR/CODEC BRANCH POINT (NOT NEAR SB400).





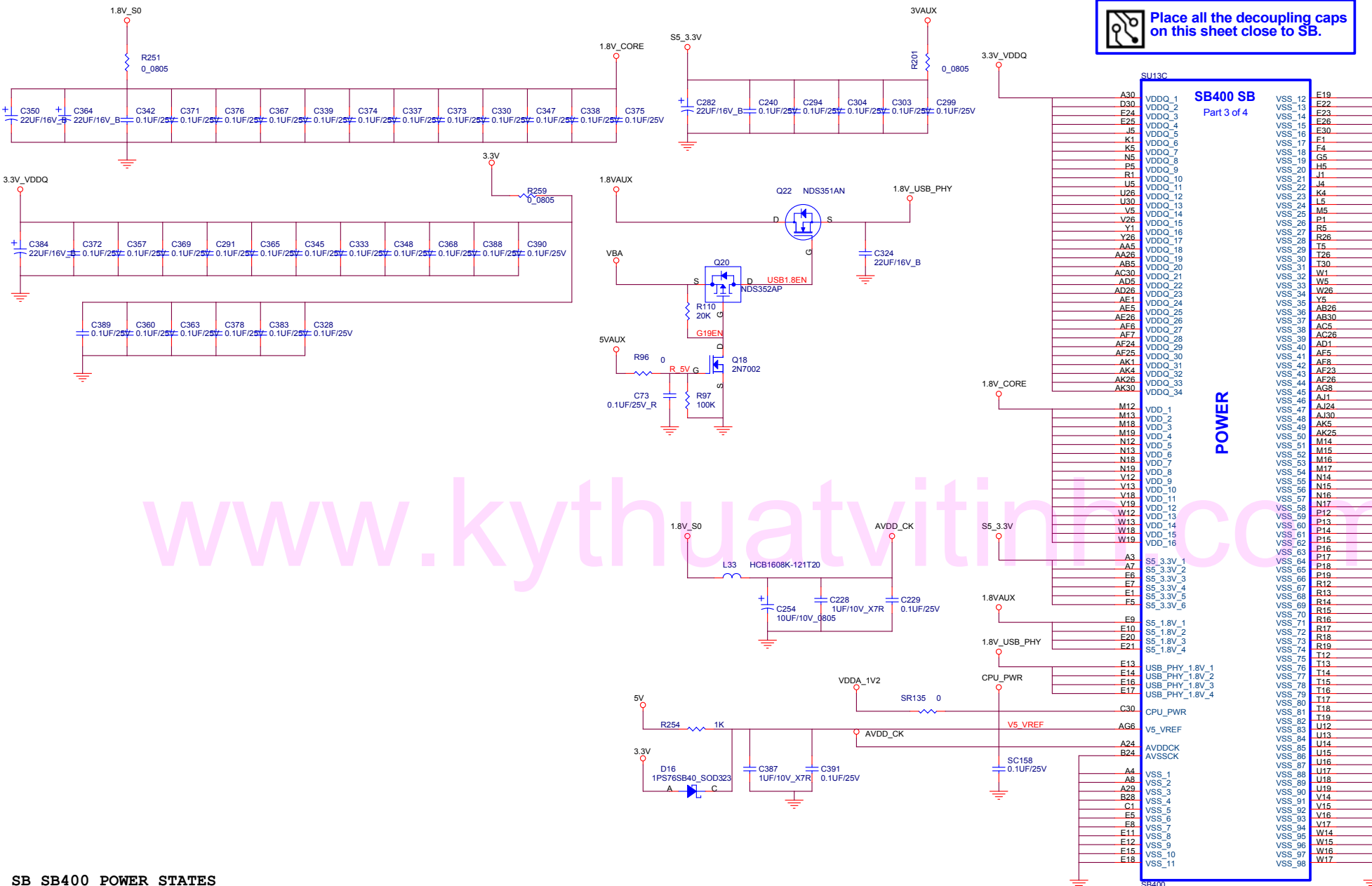
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ECS Elitegroup Computer Systems

Title: **SB400-SATA/IDE**

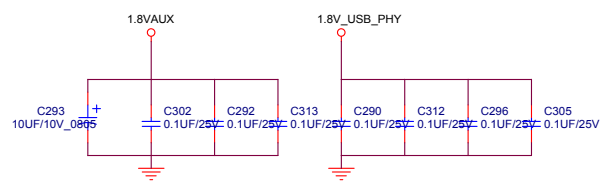
Size B	Document Number	Rev 2
	331-1-4-01	
Date:	Thursday, October 27, 2005	Sheet 14 of 39

Place all the decoupling caps on this sheet close to SB.



SB SB400 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDQ	ON	ON	OFF	OFF	OFF
VDD	ON	ON	OFF	OFF	OFF
S5_3.3V	ON	ON	ON	ON	OFF
S5_1.8V	ON	ON	ON	ON	OFF
V5_VREF	ON	ON	OFF	OFF	OFF
AVDDCK	ON	ON	OFF	OFF	OFF
CPU_PWR	ON	ON	OFF	OFF	OFF



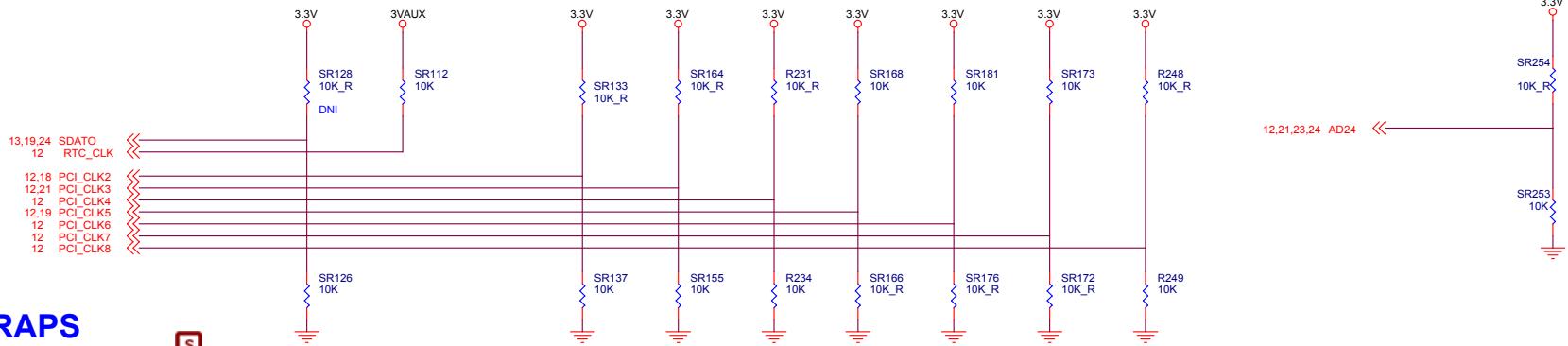
ECS Elitegroup Computer Systems

Title: **SB400-PWR & DECOUPLING**

Size: Document Number 331-1-4-01 Rev 2

Date: Thursday, October 27, 2005 Sheet 15 of 39

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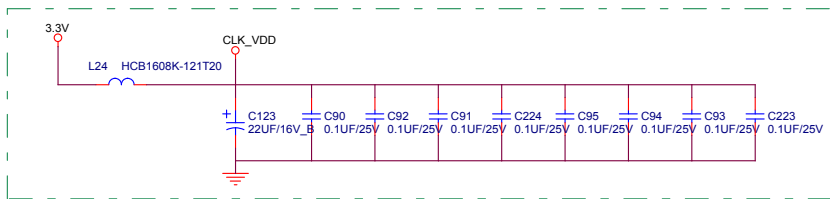


REQUIRED STRAPS

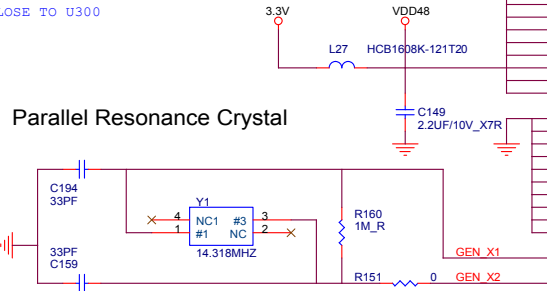
S
ACPWRON

	SDATO	RTC_CLK	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN DISABLE DEFAULT	USE INT. PLL48	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC TYPE I ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	48MHz OSC MODE	USB PHY PWRDOWN ENABLE	USE EXT. 48MHz	14MHz XTAL MODE	CPU I/F = P4	L,H = LPC TYPE II ROM L,L = FWH ROM DEFAULT	

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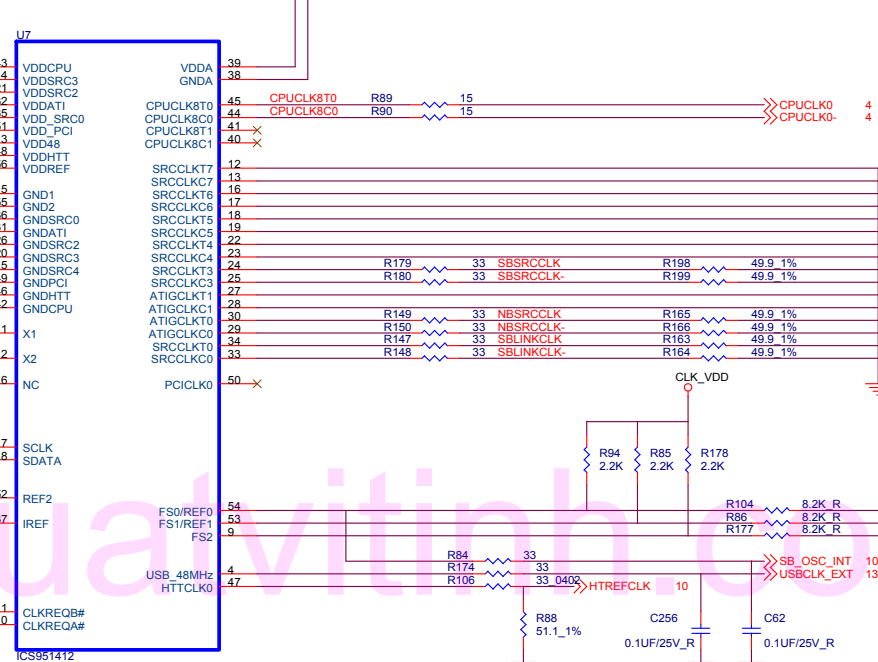
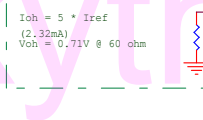


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U300 POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U300 POWER PIN



6,13 SCLK
6,13 SDATA

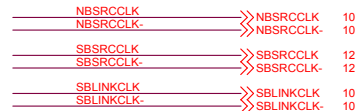
10 OSC14M



CY28RS480/ICS951412 AND ICS951416 ARE FULLY PIN COMPATIBLE AND CAN BE INTERCHANGED WITHOUT ANY HARDWARE MODIFICATION.



OVERLAP COMMON PADS FOR DUAL-OP RESISTORS



EXT CLK FREQUENCY SELECT TABLE(MHZ)

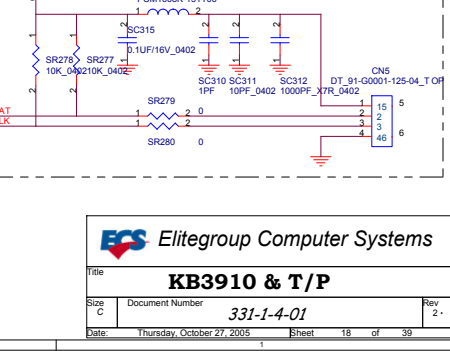
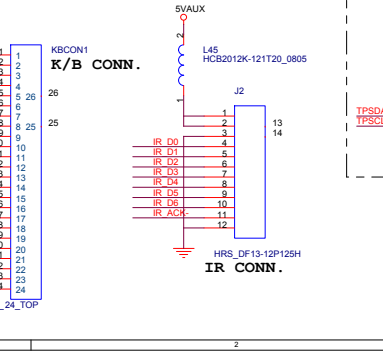
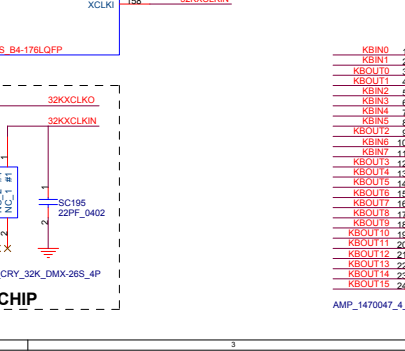
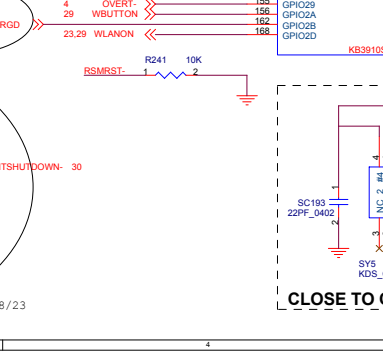
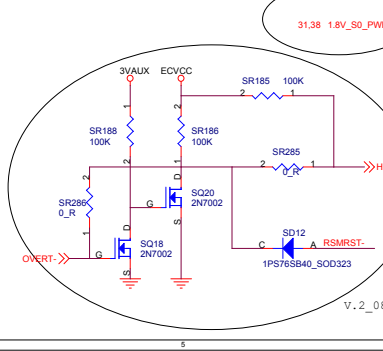
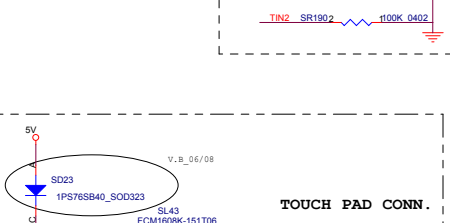
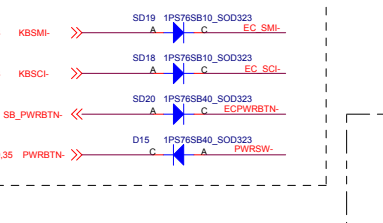
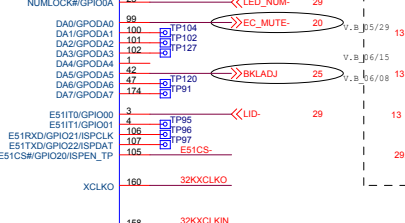
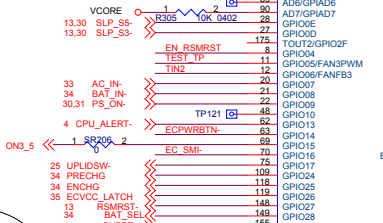
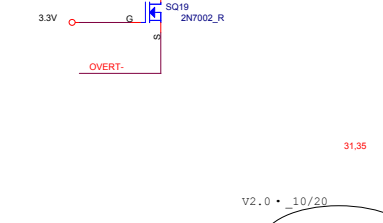
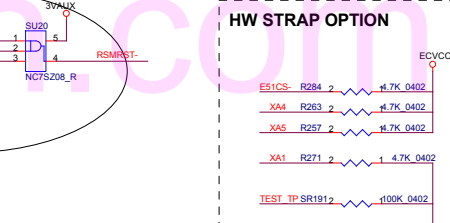
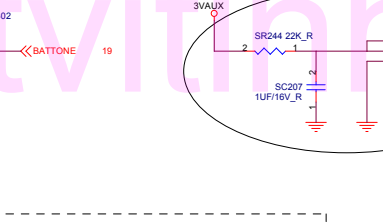
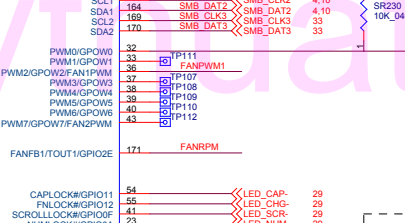
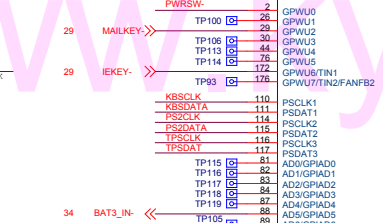
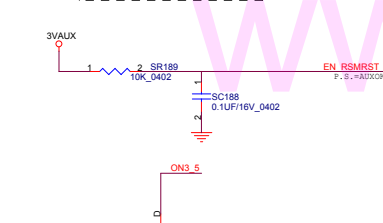
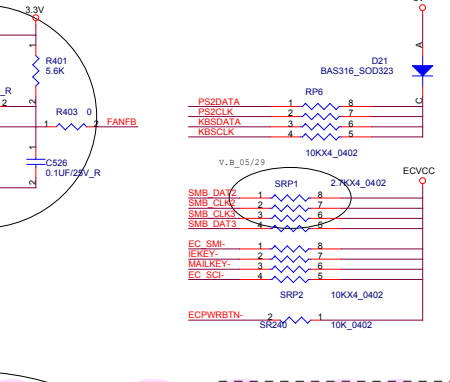
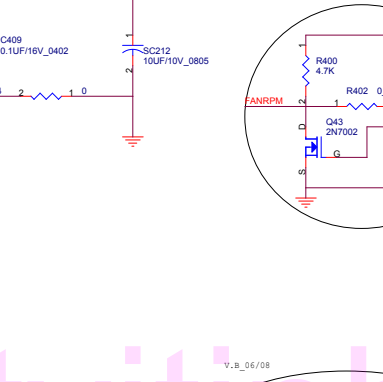
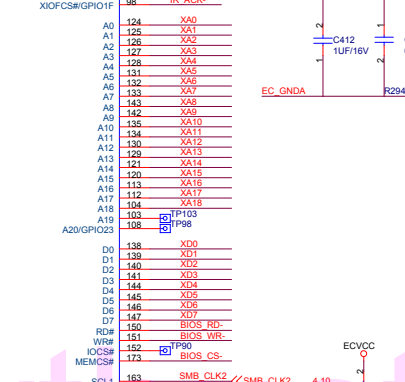
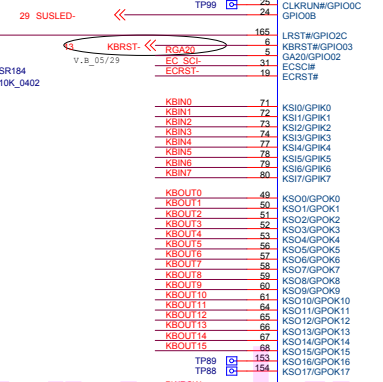
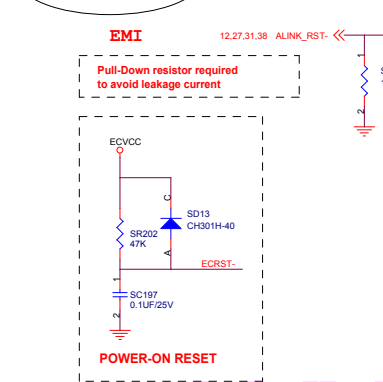
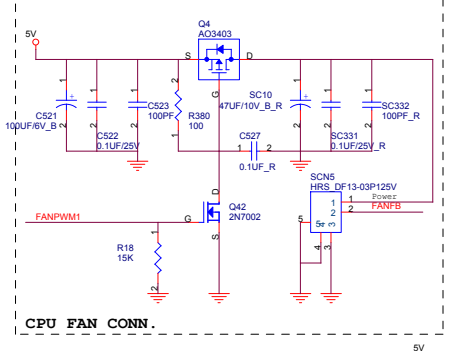
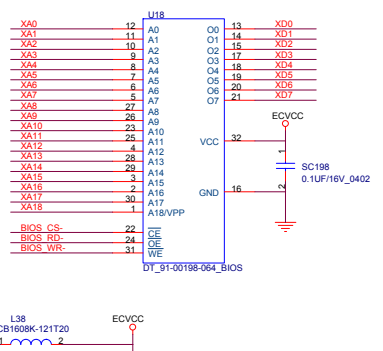
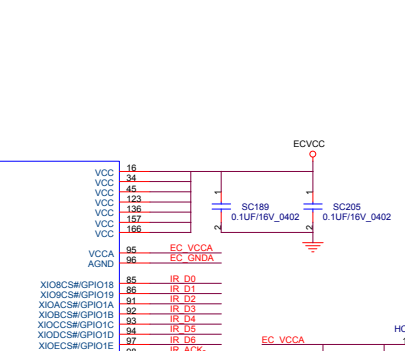
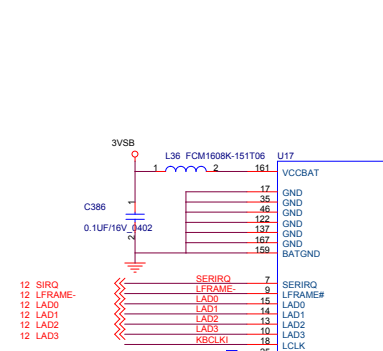
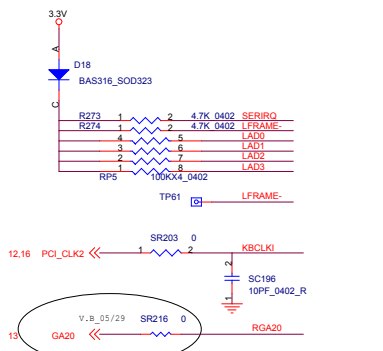
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Elitegroup Computer Systems

Title: **CLOCK GENERATOR**

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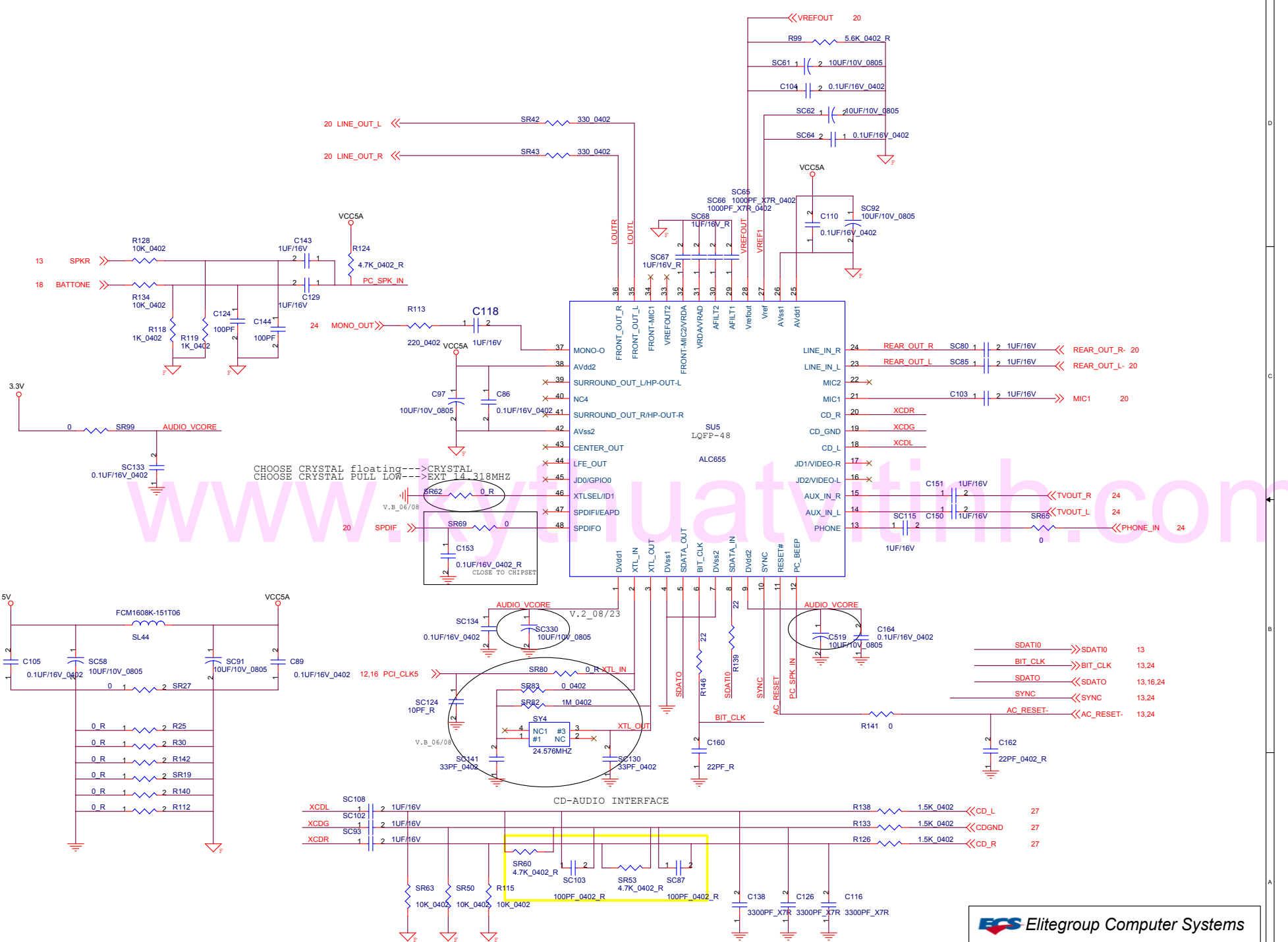
Elitegroup Computer Systems

KB3910 & T/P

File: **KB3910 & T/P**

Size: Document Number **331-1-4-01** Rev: 2

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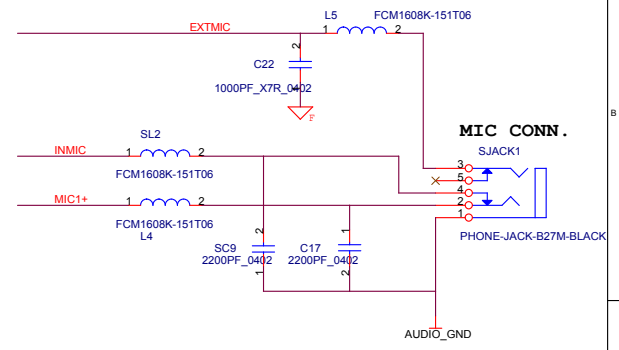
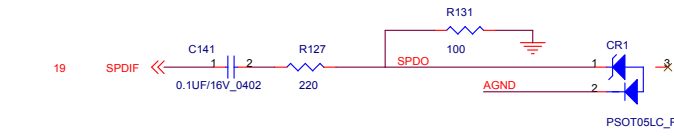
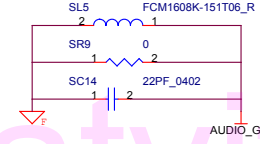
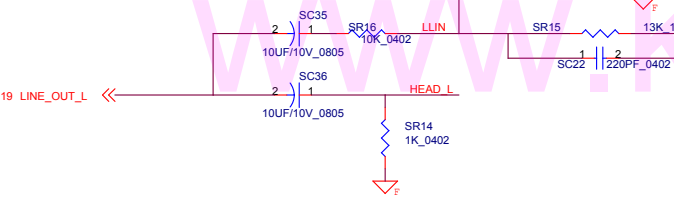
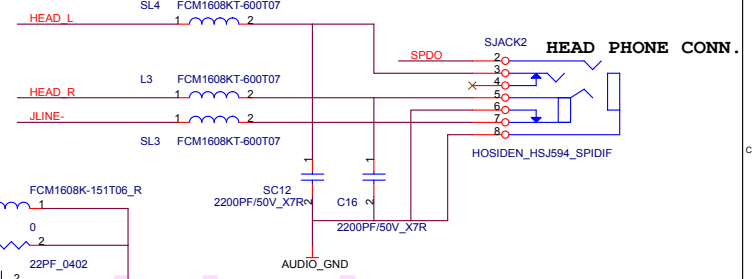
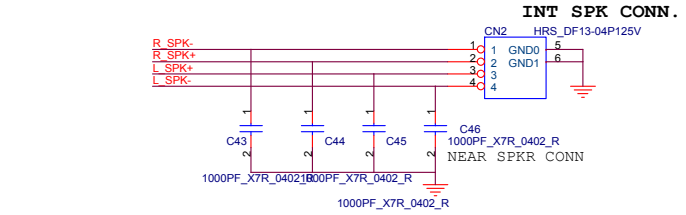
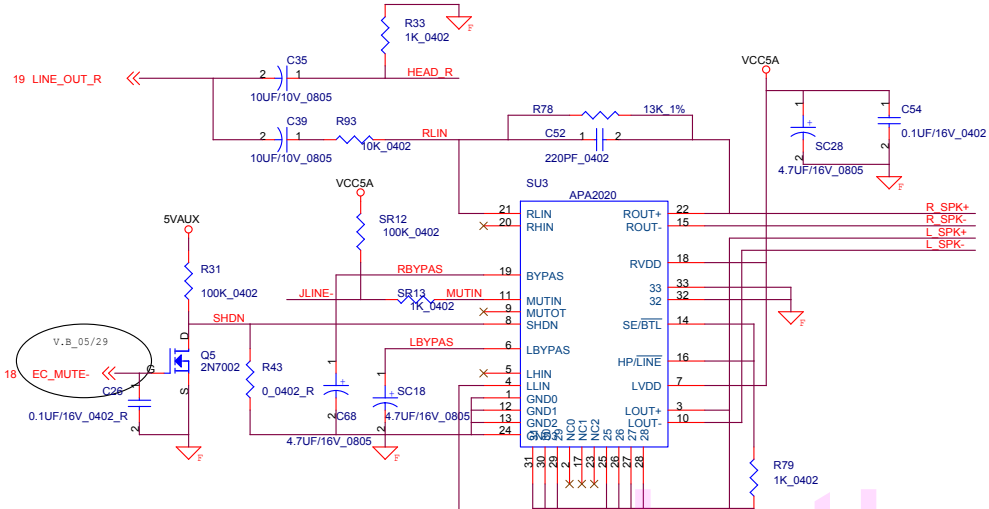
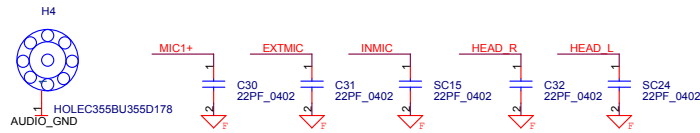
CHOOSE CRYSTAL floating---CRYSTAL
 CHOOSE CRYSTAL PULL LOW---EXT 14.318MHZ

CD-AUDIO INTERFACE

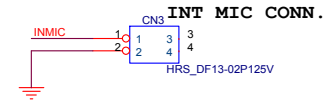
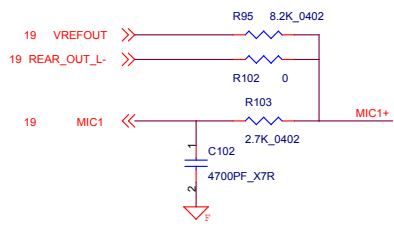
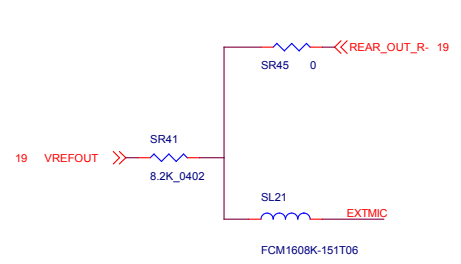
ECS Elitegroup Computer Systems

Title: **ALC655**

Size: Custom	Document Number: 331-1-4-01	Rev: 2.0
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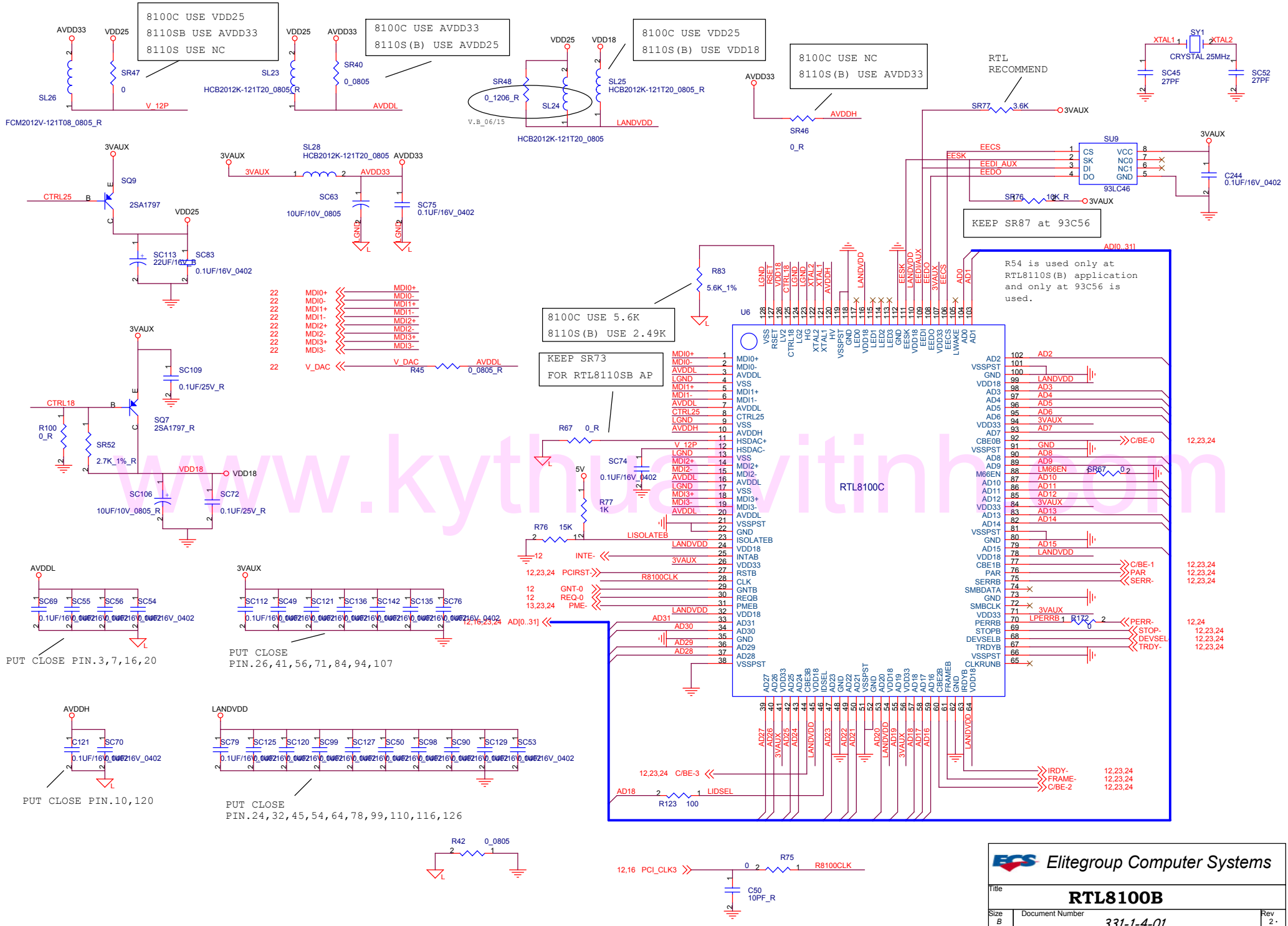
PC2001 SPEC. 12KHz--15KHz
 $F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$
VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION



ECS Elitegroup Computer Systems

Title: **OPA & AUDIO JACK**

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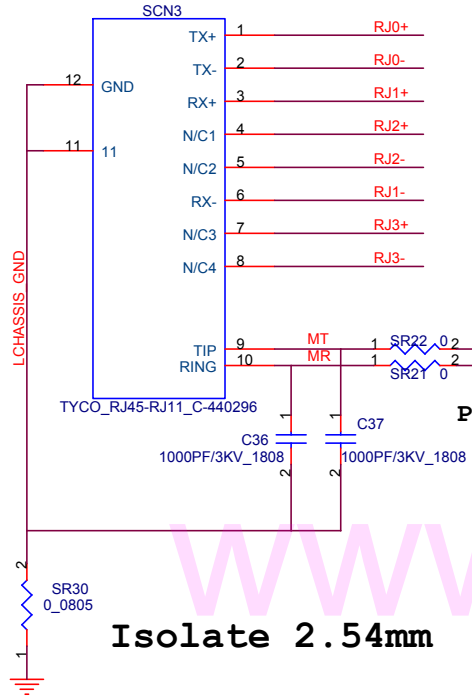
Elitegroup Computer Systems

Title: **RTL8100B**

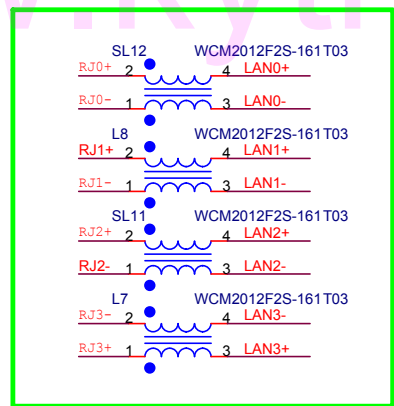
Size B Document Number: **331-1-4-01**

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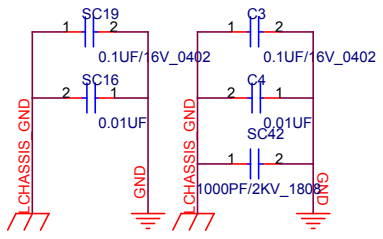
RJ-45 & RJ-11 CONN.



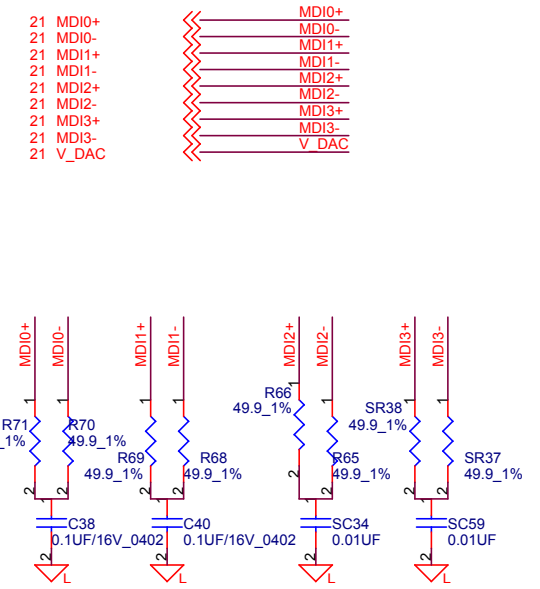
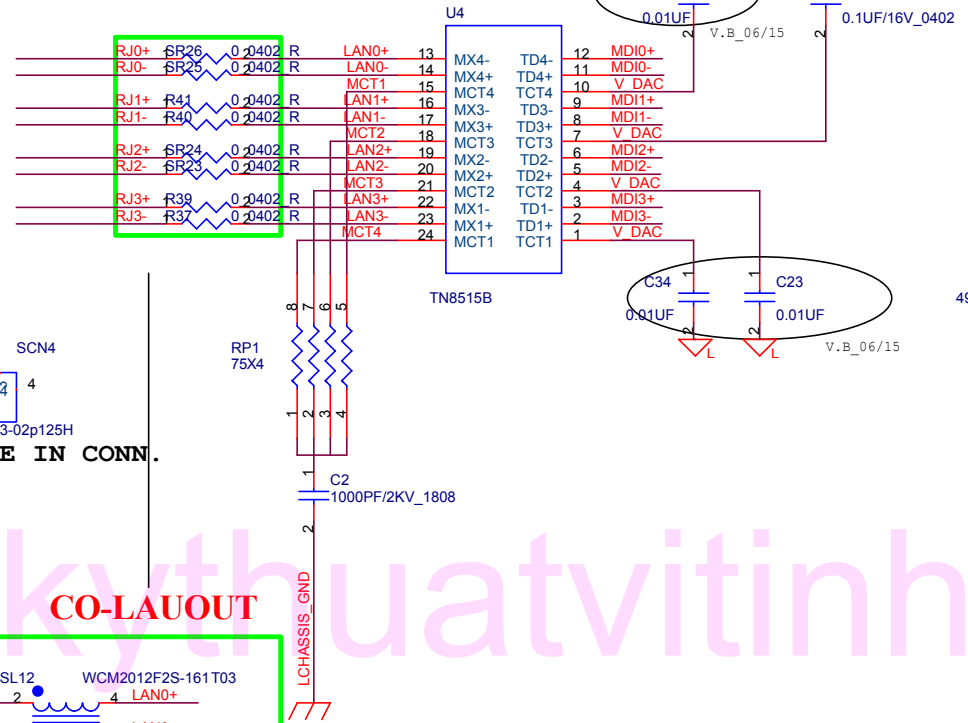
PHONE LINE IN CONN.



Isolate 2.54mm



(CONNECT TO CHASSIS GND)



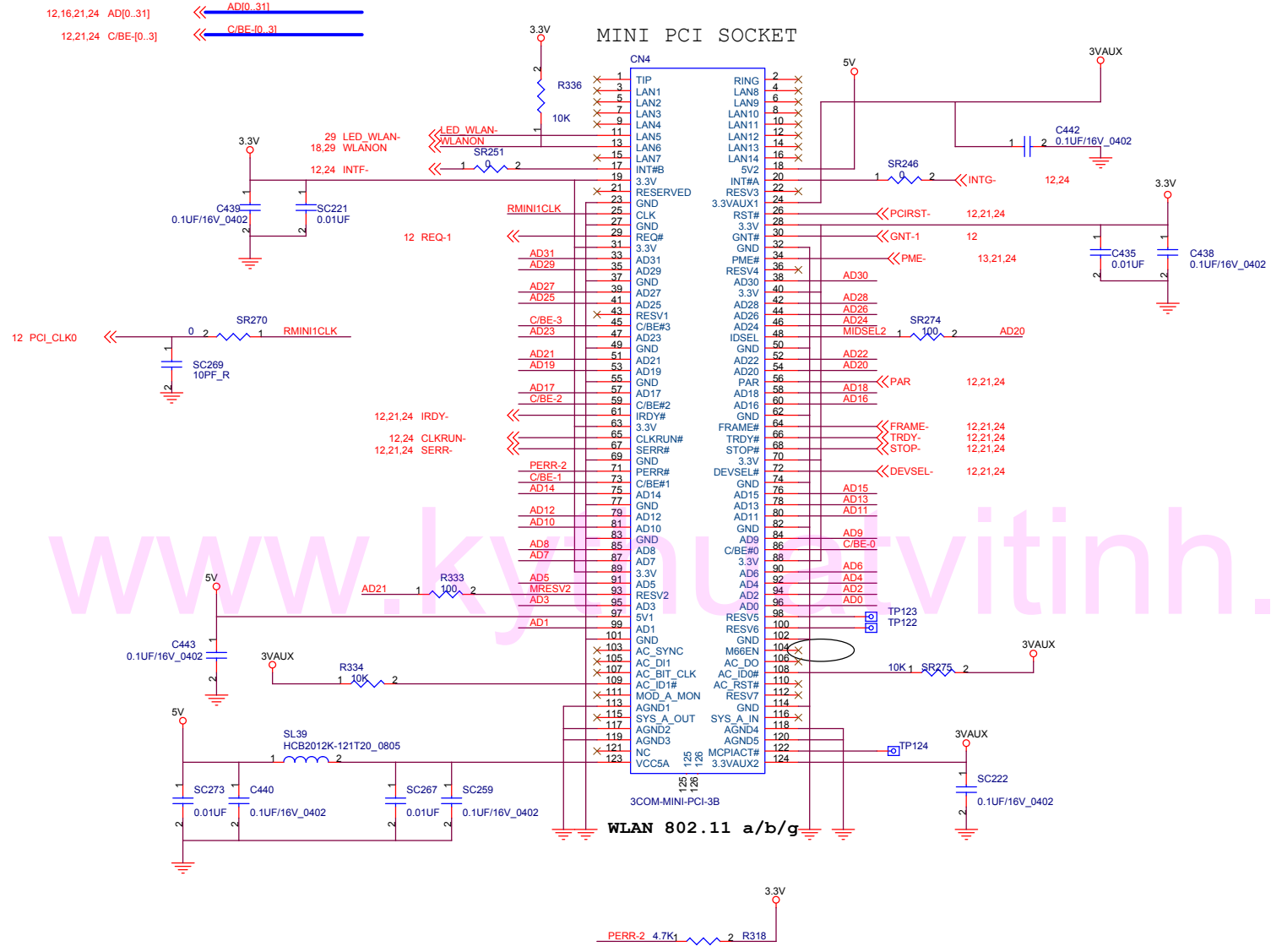
CO-LAOUT

ECS Elitegroup Computer Systems

Title: **RJ45 & RJ11**

Document Number: **331-1-4-01** Rev: 2.0

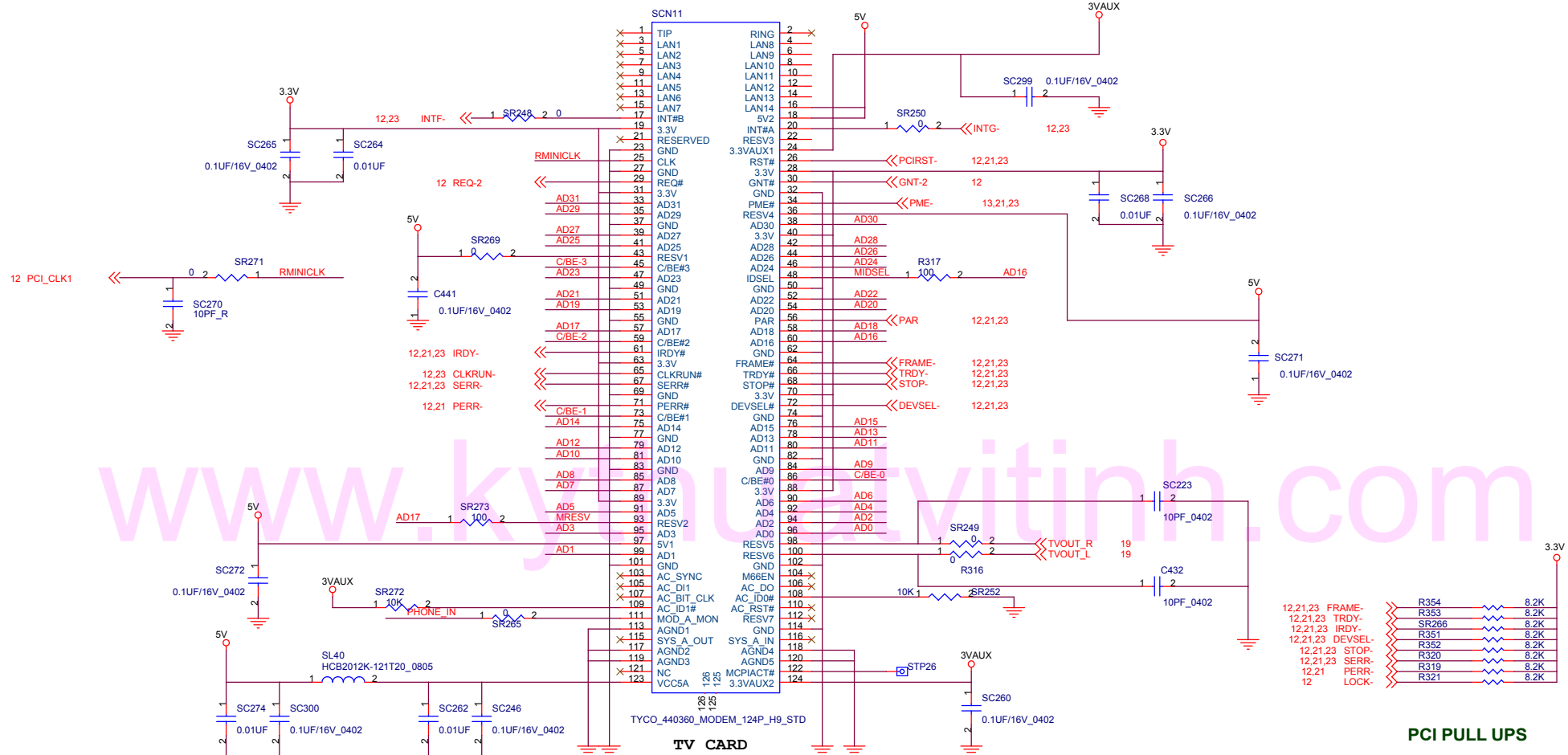
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12,16,21,23 AD[0..31] << AD[0..31]
 12,21,23 C/BE[0..3] << C/BE[0..3]

MINI PCI SOCKET

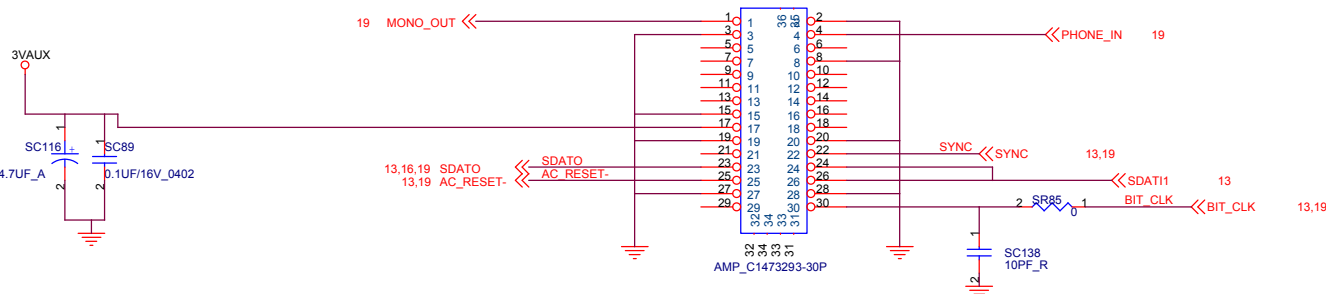


PCI PULL UPS

12,21,23	FRAME-	R354	8.2K
12,21,23	TRDY-	R353	8.2K
12,21,23	IRDY-	SR266	8.2K
12,21,23	DEVSEL-	R351	8.2K
12,21,23	STOP-	R352	8.2K
12,21,23	SERR-	R320	8.2K
12,21	PERR-	R319	8.2K
12	LOCK-	R321	8.2K

TV CARD

MDC CONN.

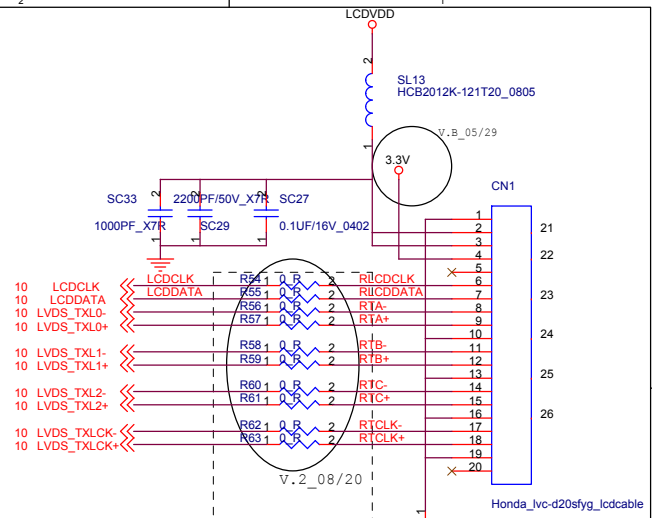
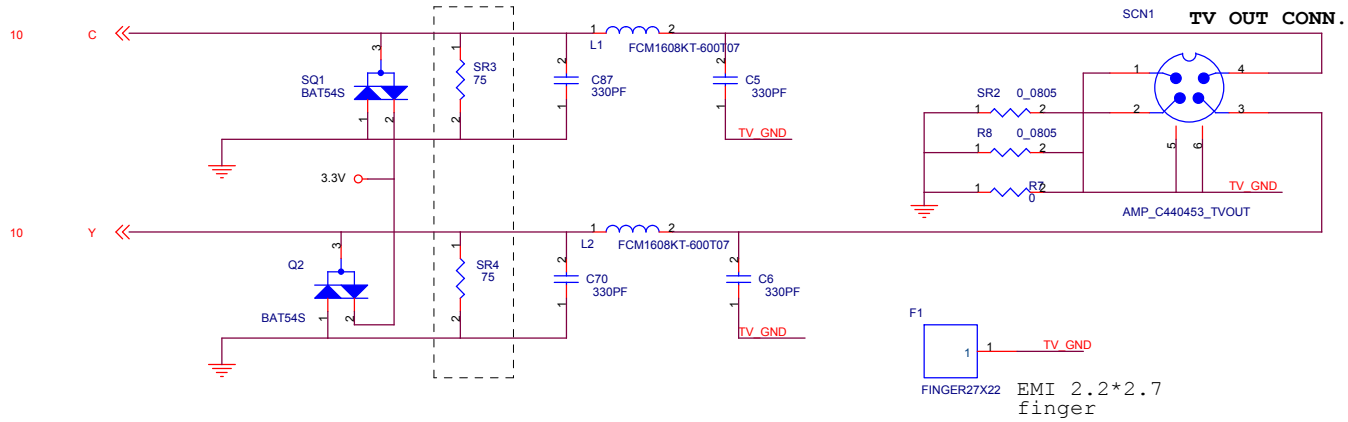


Elitegroup Computer Systems

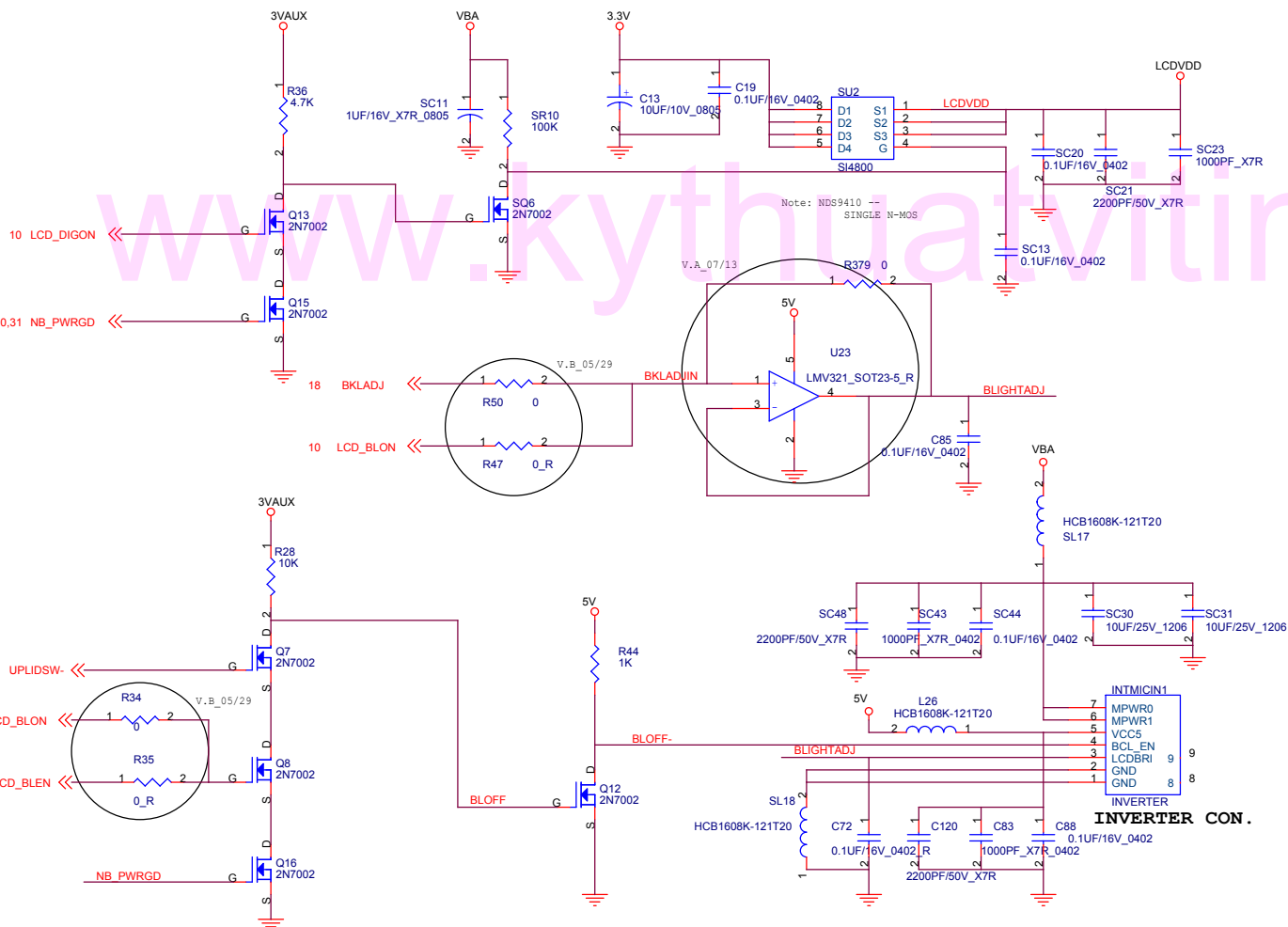
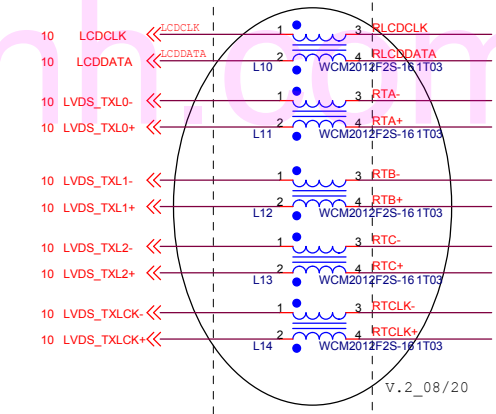
Title: **MINI PCI CONN.(TV) & MDC**

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CO-LAUOUT

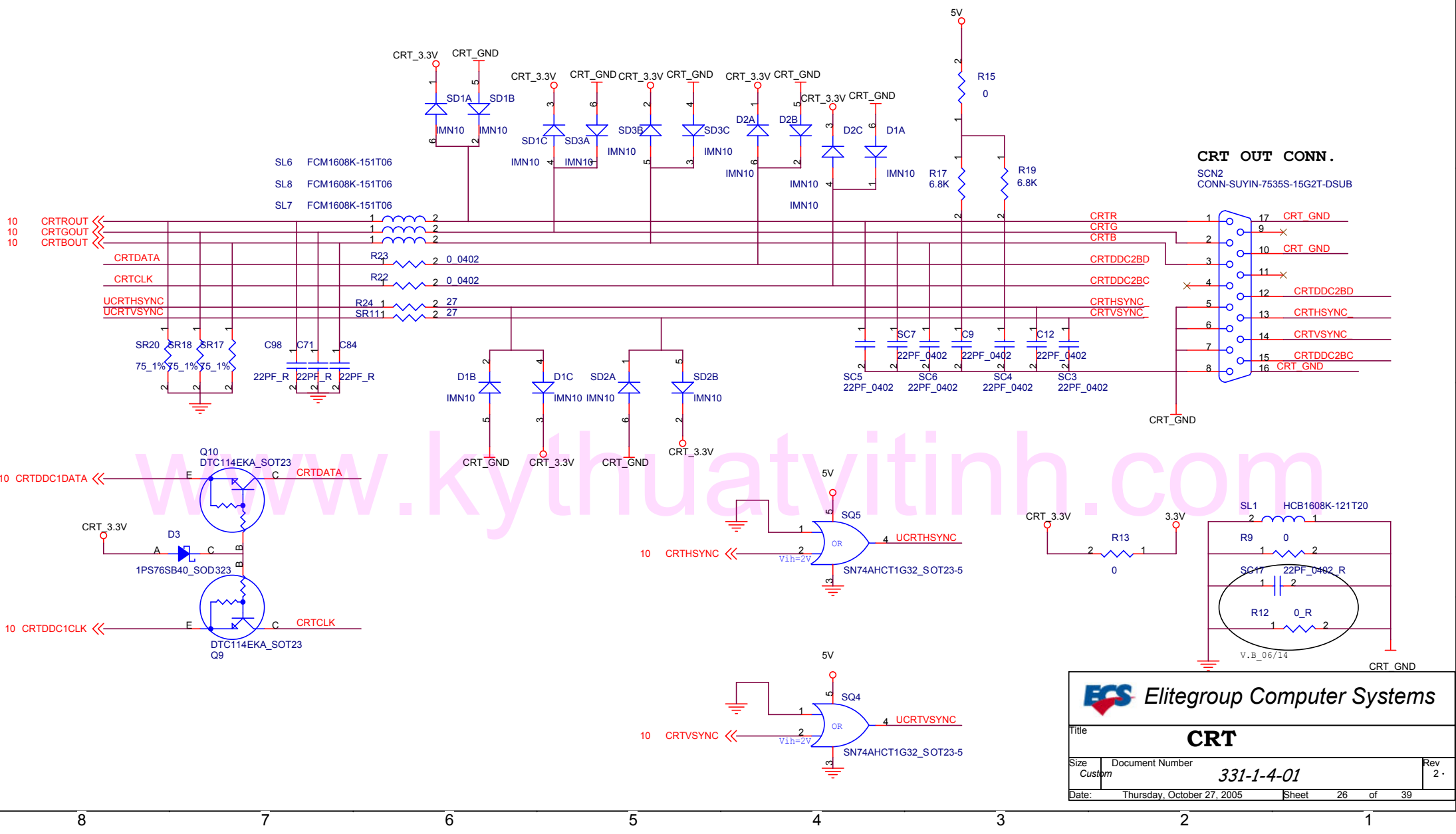


Elitegroup Computer Systems

Title: **LCD & TV CONN**

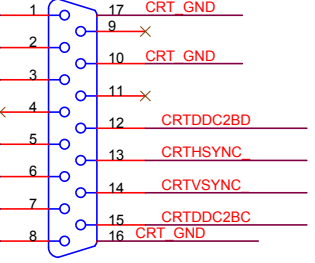
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10 CRTROUT
10 CRTGOUT
10 CRTBOUT

CRT OUT CONN.
SCN2
CONN-SUYIN-7535S-15G2T-DSUB



10 CRTDDC1DATA

10 CRTDDC1CLK

10 CRTHSYNCR

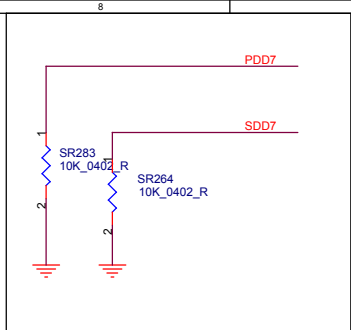
10 CRTVSYNCR

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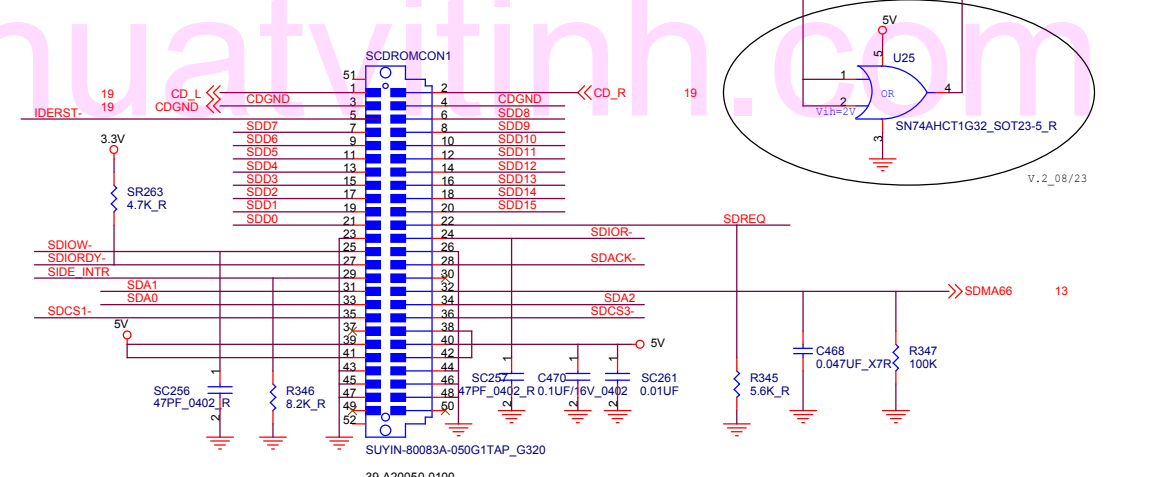
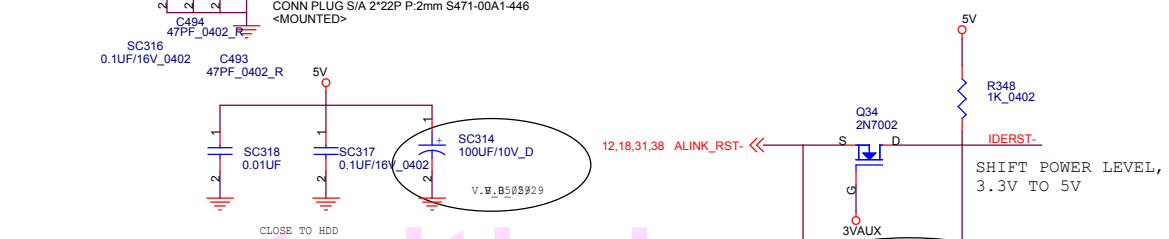
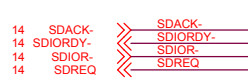
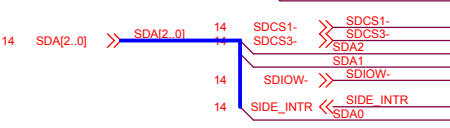
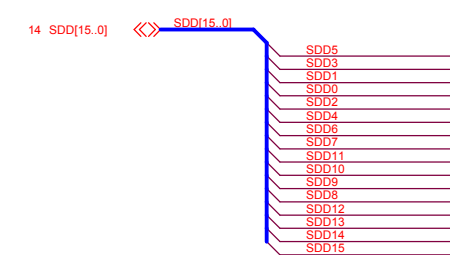
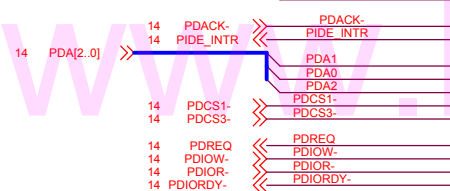
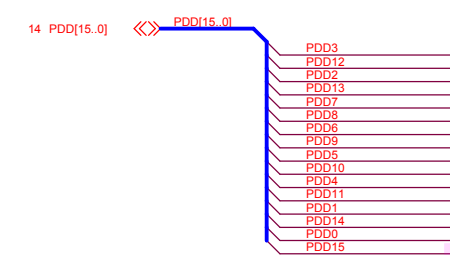
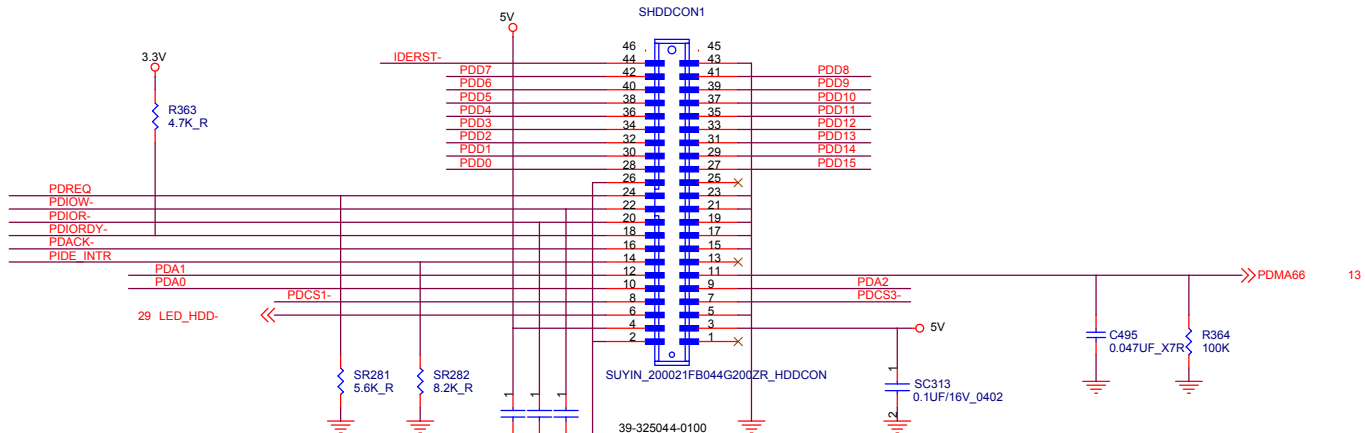
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Size: Custom | Document Number: **331-1-4-01** | Rev: 2

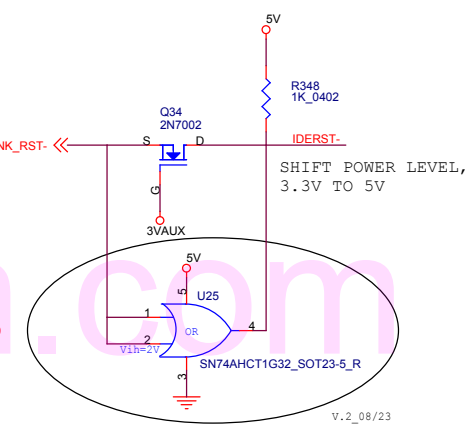
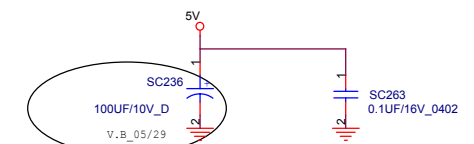
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CLOSE TO HDD CONN.



CSEL : "NC" ; "Hi" --> Master (CDROM) /Slave (DVDROM)
 CSEL : "Low" --> Slave (CDROM) /Master (DVDROM)

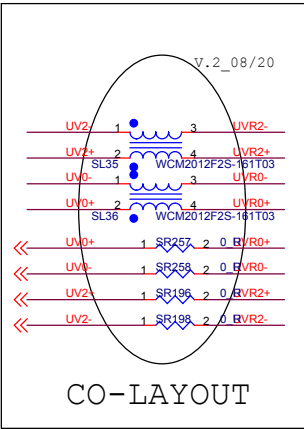


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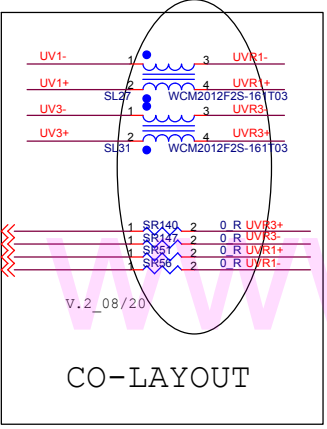
Title: **HDD & CDROM CONN.**

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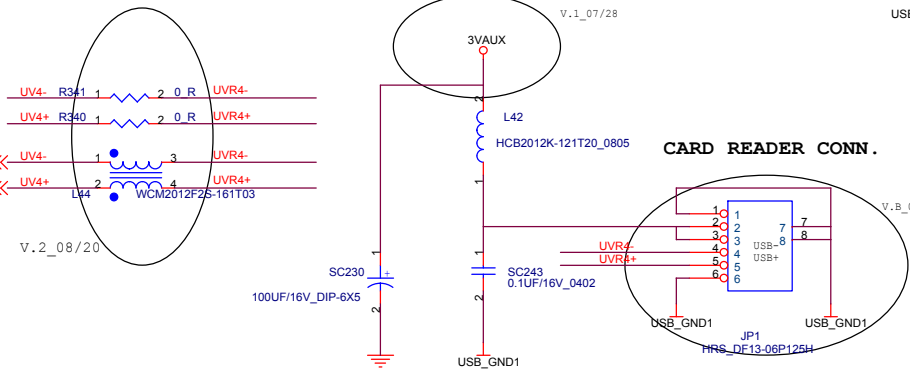
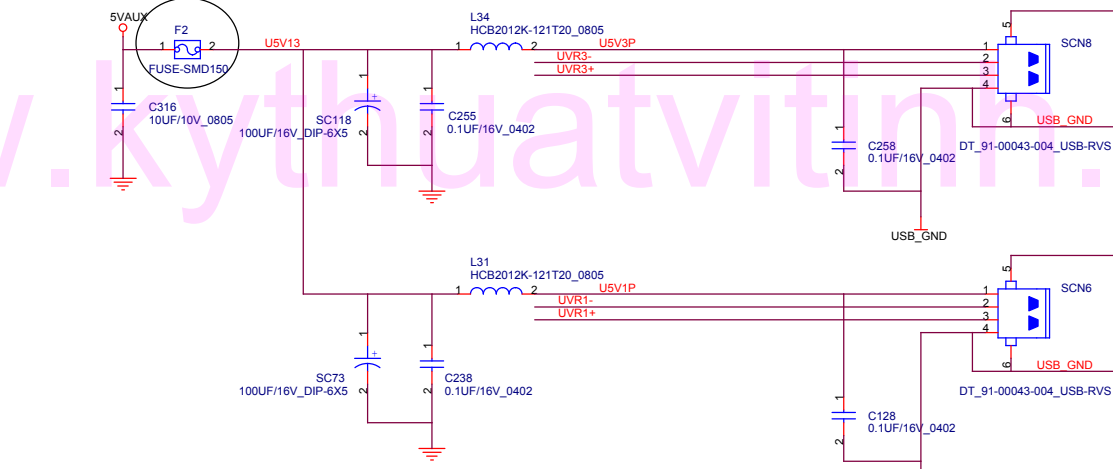
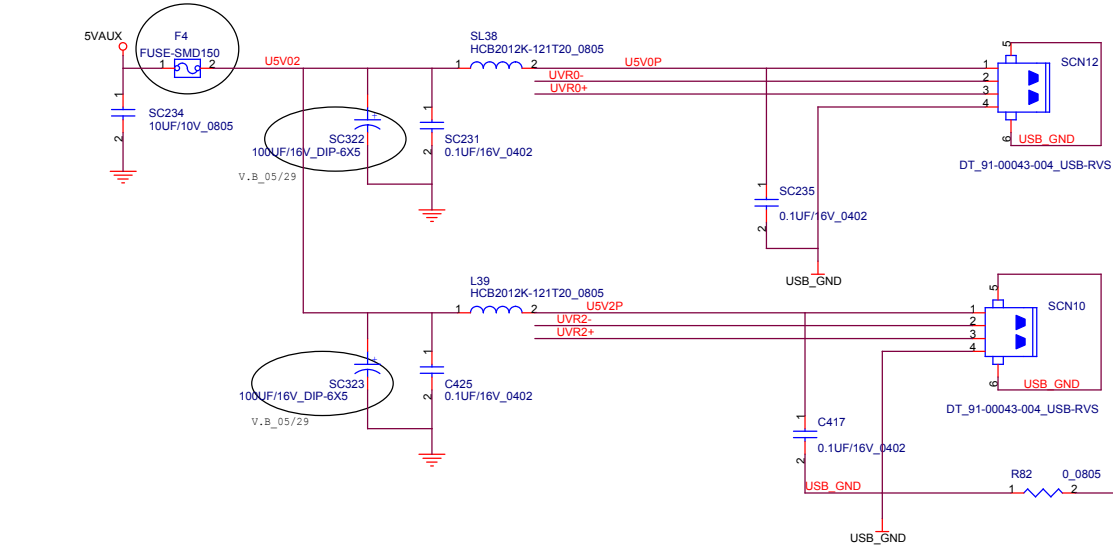
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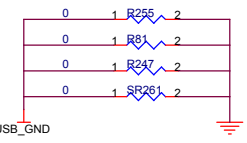
- 13 UV0+
- 13 UV0-
- 13 UV2+
- 13 UV2-



- 13 UV3+
- 13 UV3-
- 13 UV1+
- 13 UV1-



- 13 UV4-
- 13 UV4+

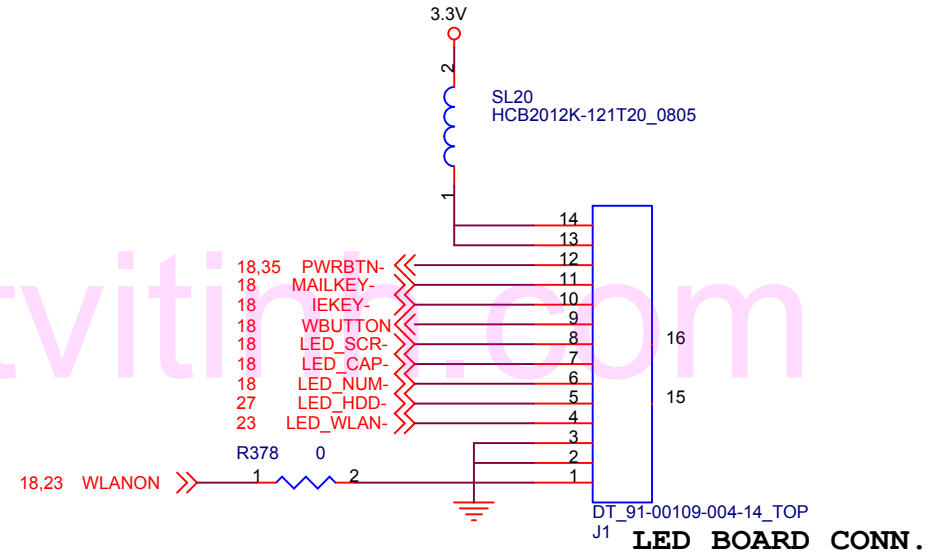
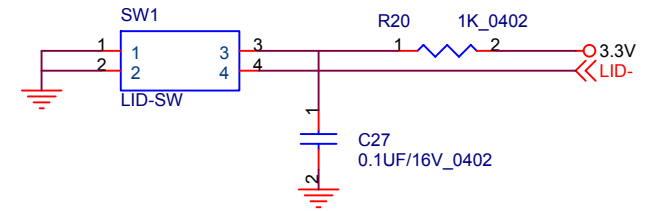
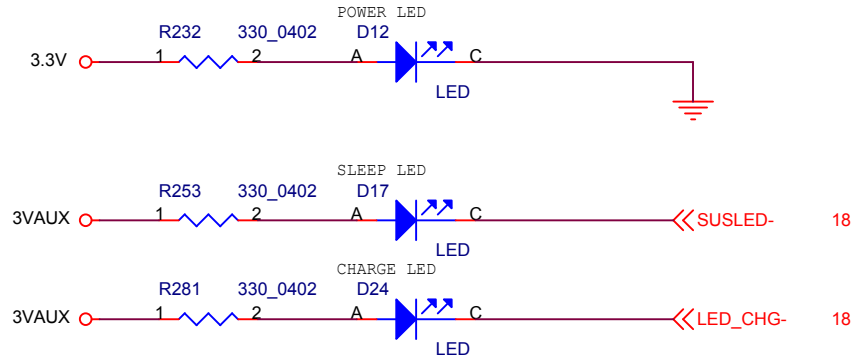


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Title: **USB PORT**

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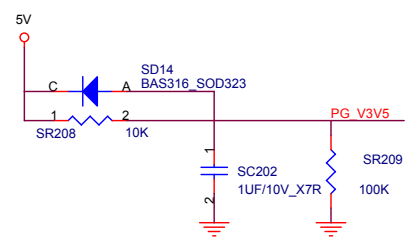
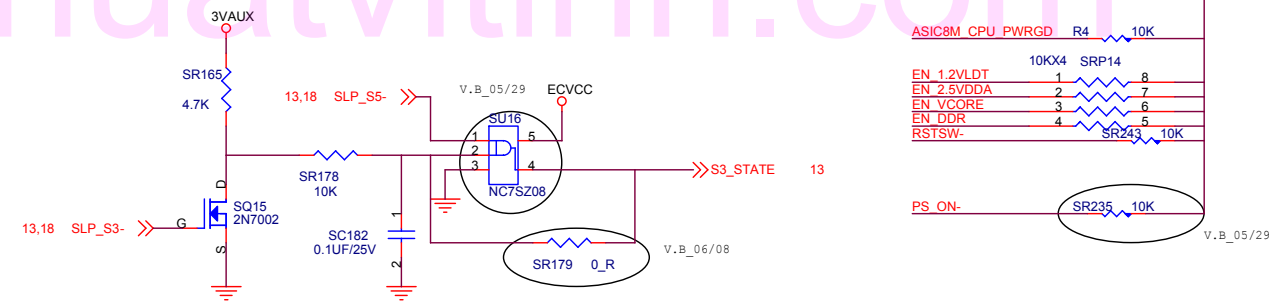
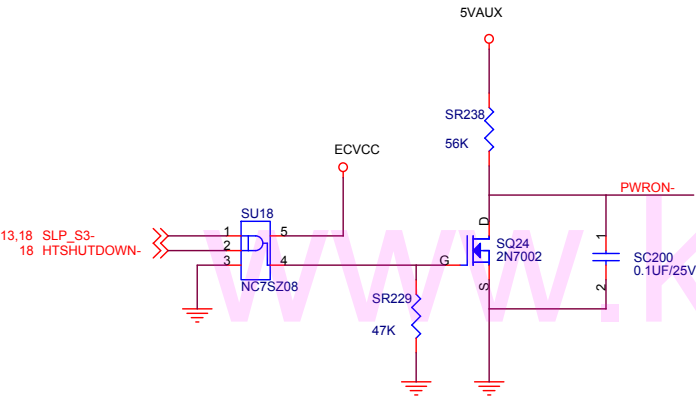
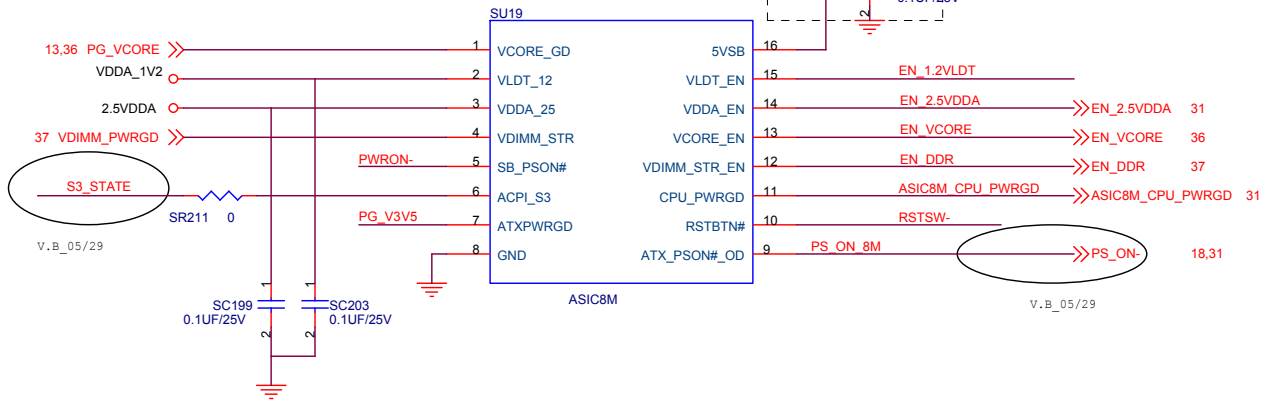
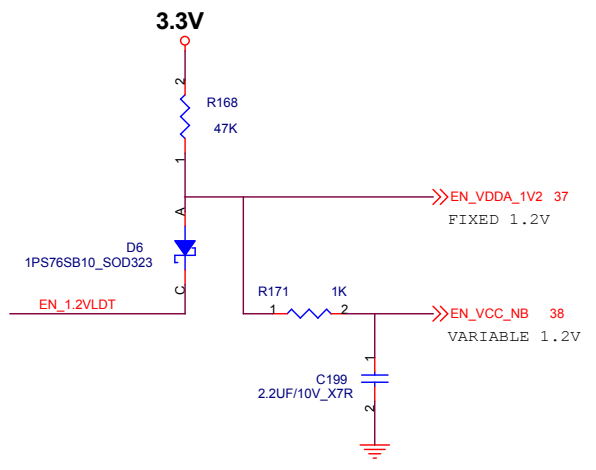
pin 1 & 4 to press



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Title		
LED & LID		
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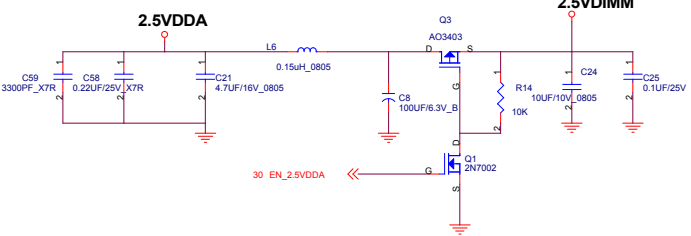
ECS Elitegroup Computer Systems

Title: **ASIC8M**

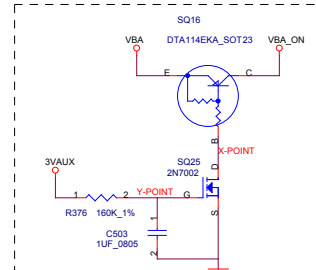
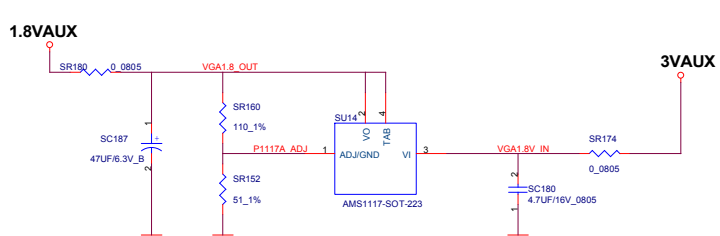
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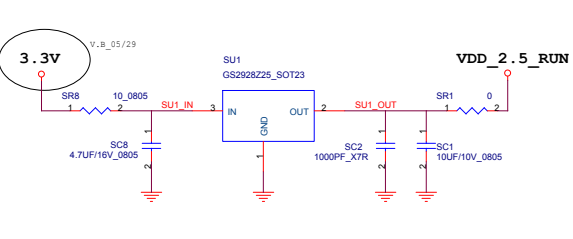
2.5VDDA SUPPLY FOR CPU



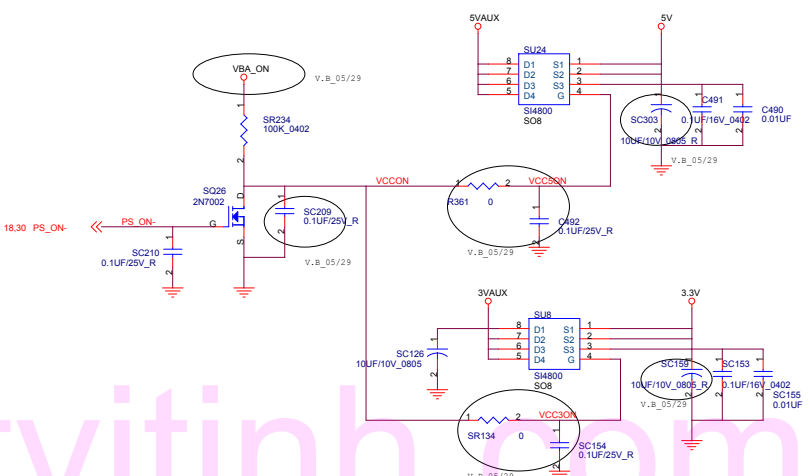
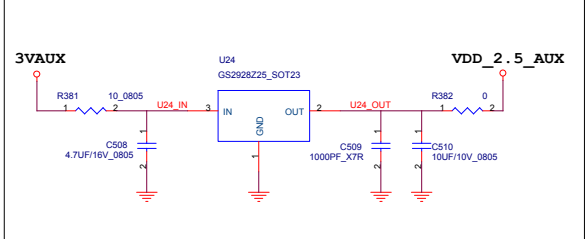
AUX 1.8V SUPPLY FOR SB



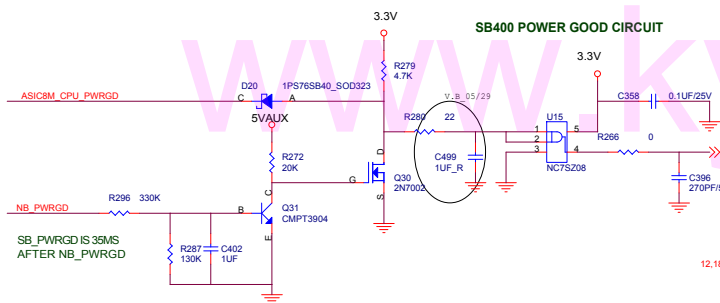
VDD_2.5_RUN/10mA



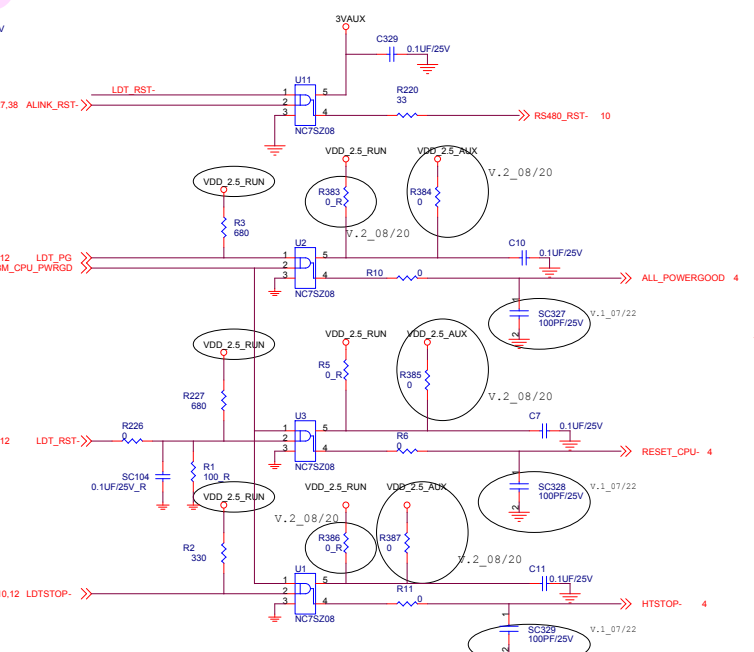
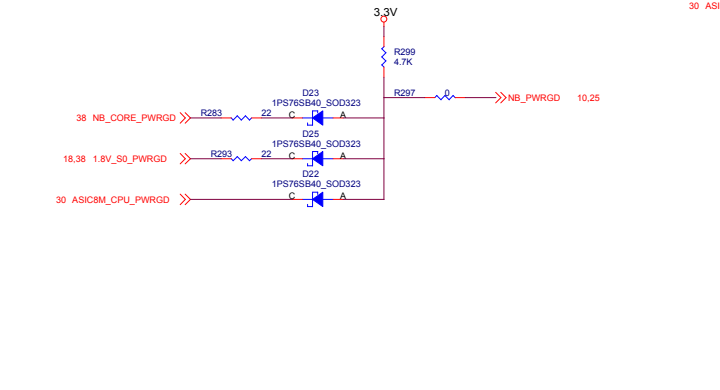
VDD_2.5_AUX/10mA



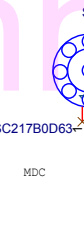
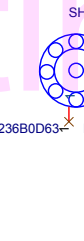
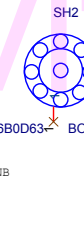
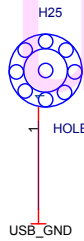
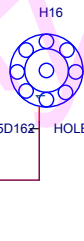
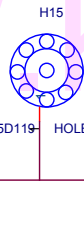
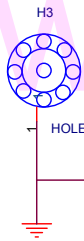
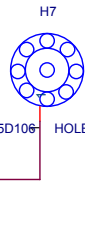
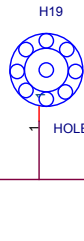
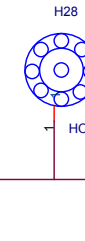
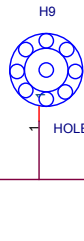
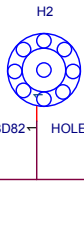
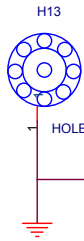
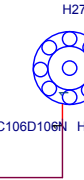
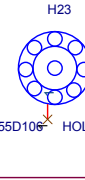
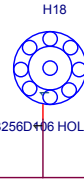
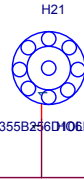
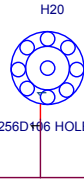
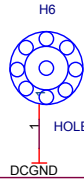
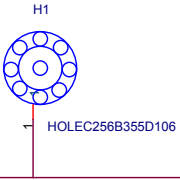
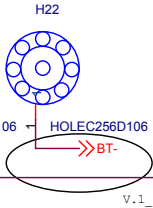
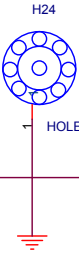
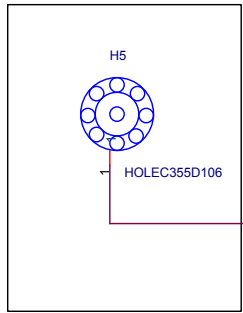
POWER GOOD & ENABLES



RS482M POWERGOOD CIRCUIT

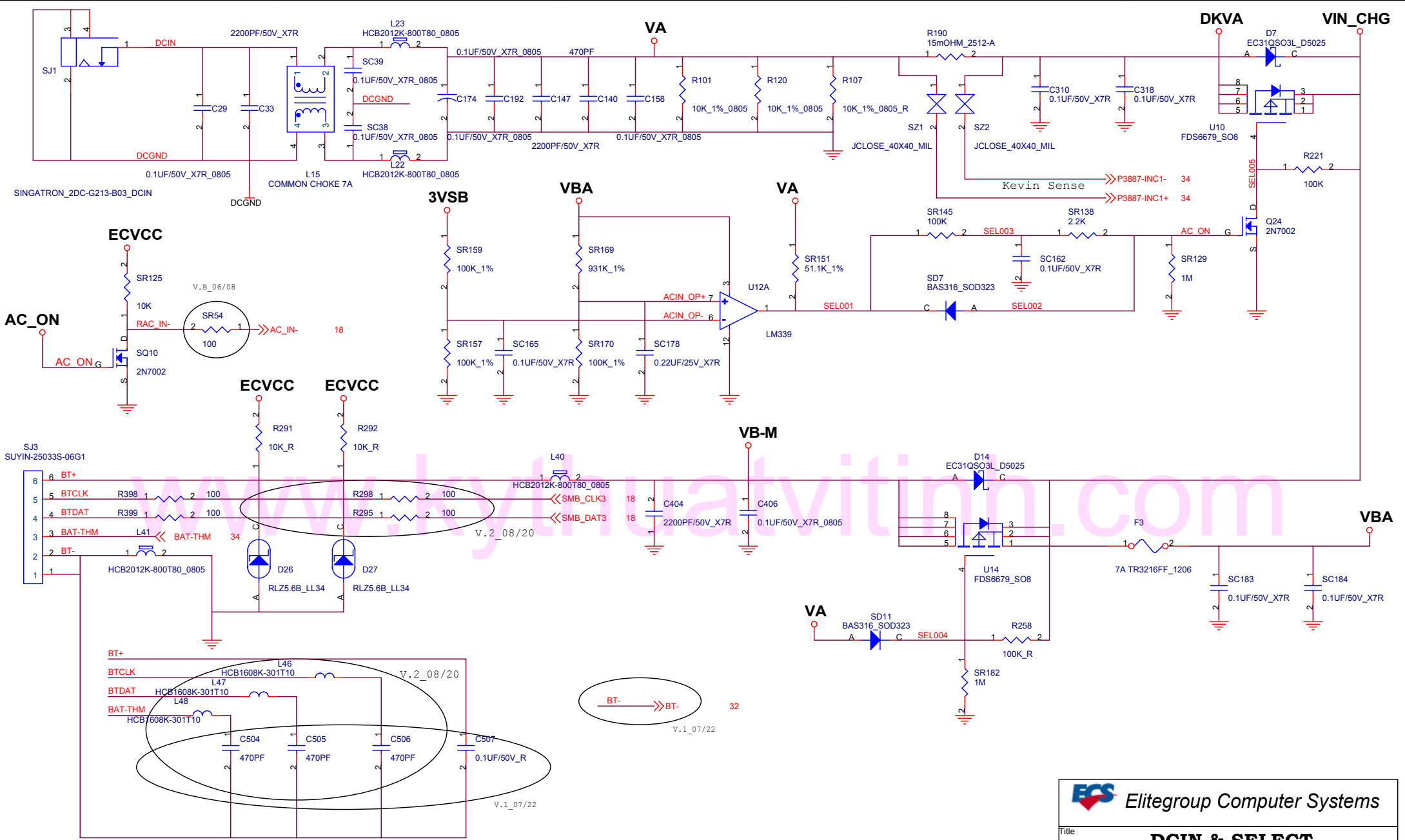


ECS Elitegroup Computer Systems			
Title	PWRGD/RESET/SYSTEM POWER		
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THROUGH HOLE		
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Elitegroup Computer Systems

Title DCIN & SELECT

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DKVA

DKVA

VB-M

Total Power set=59.63W

Pre-charge=263 mA
CHARGE 2A

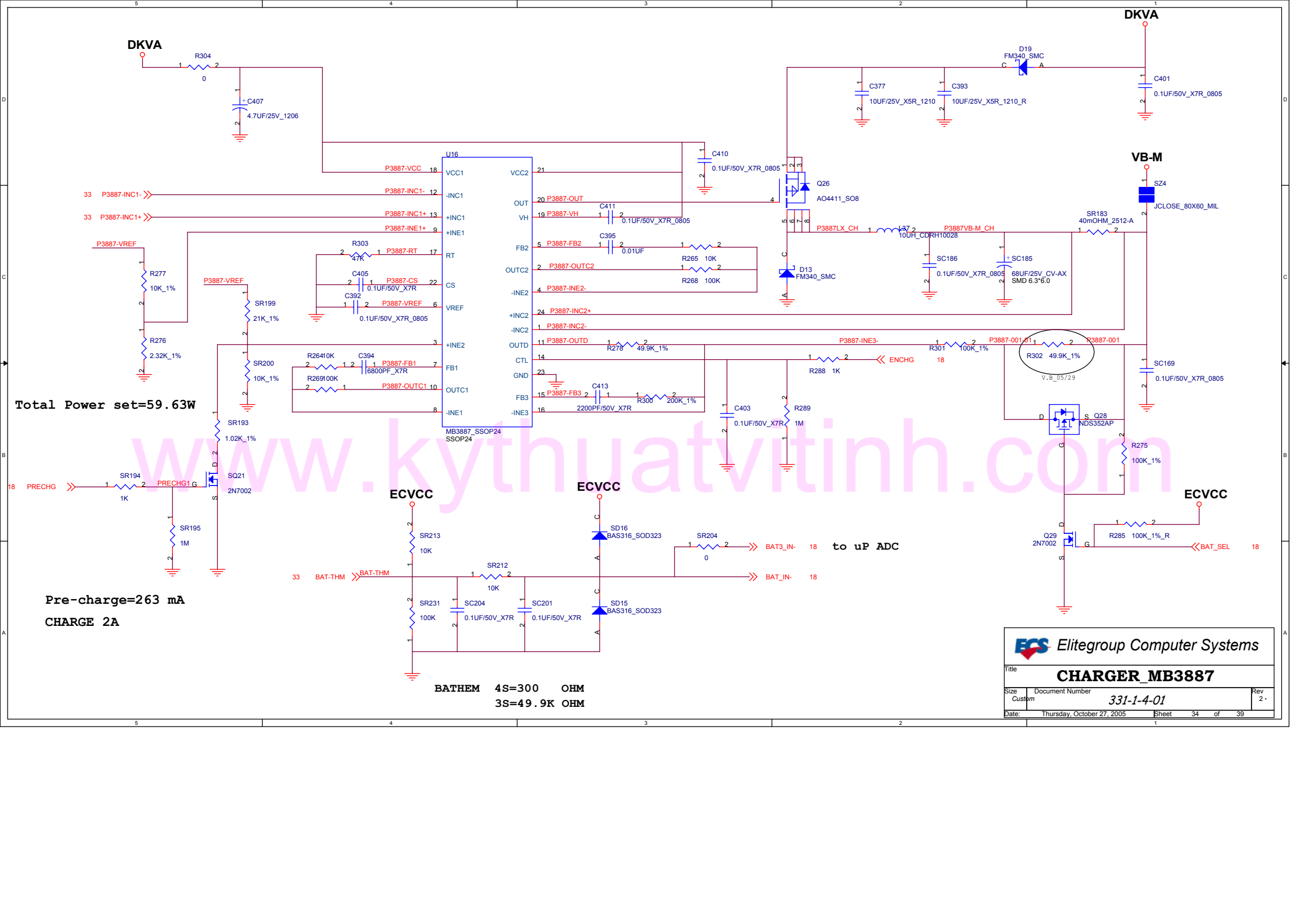
BATHEM 4S=300 OHM
3S=49.9K OHM

ECS Elitegroup Computer Systems

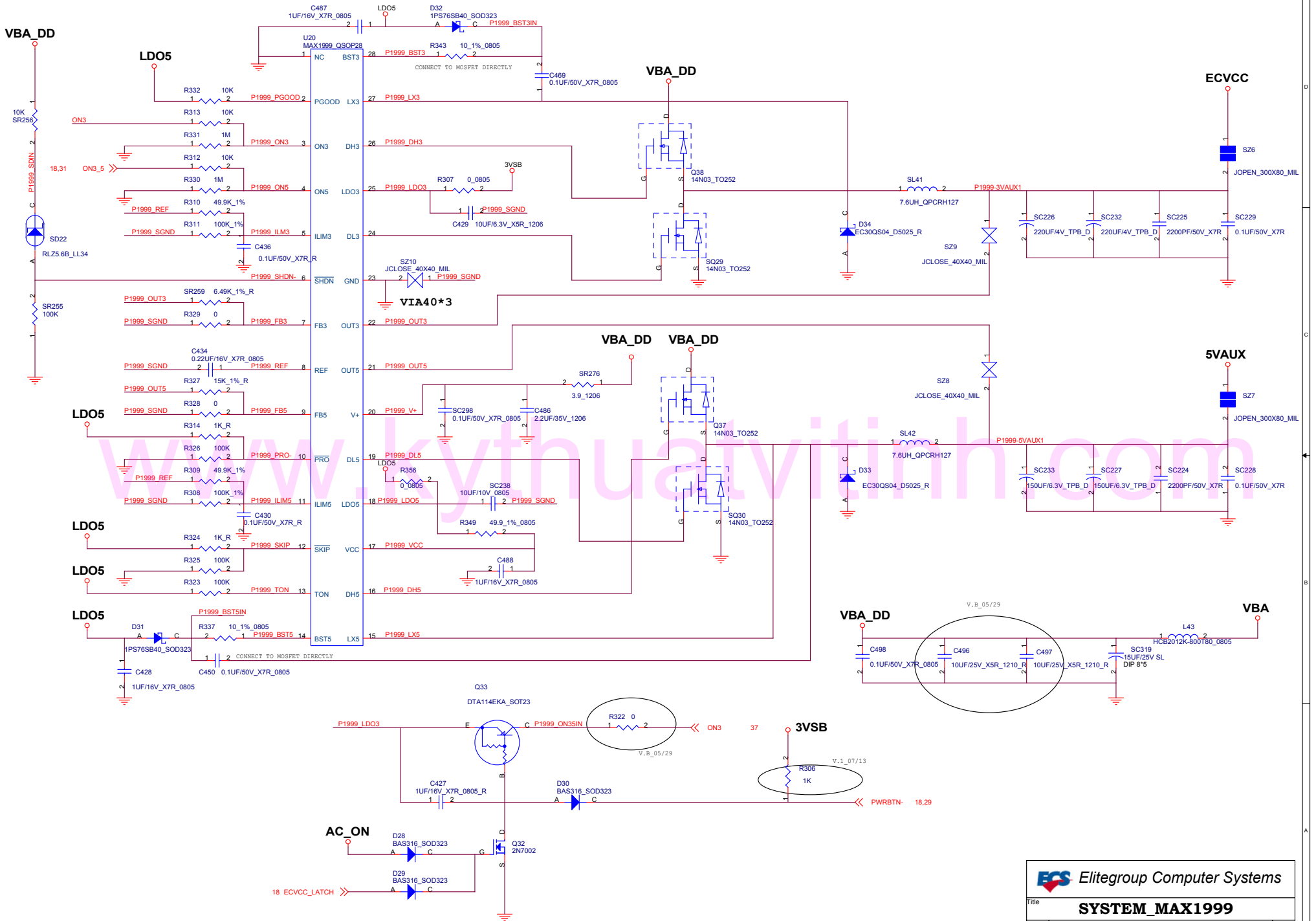
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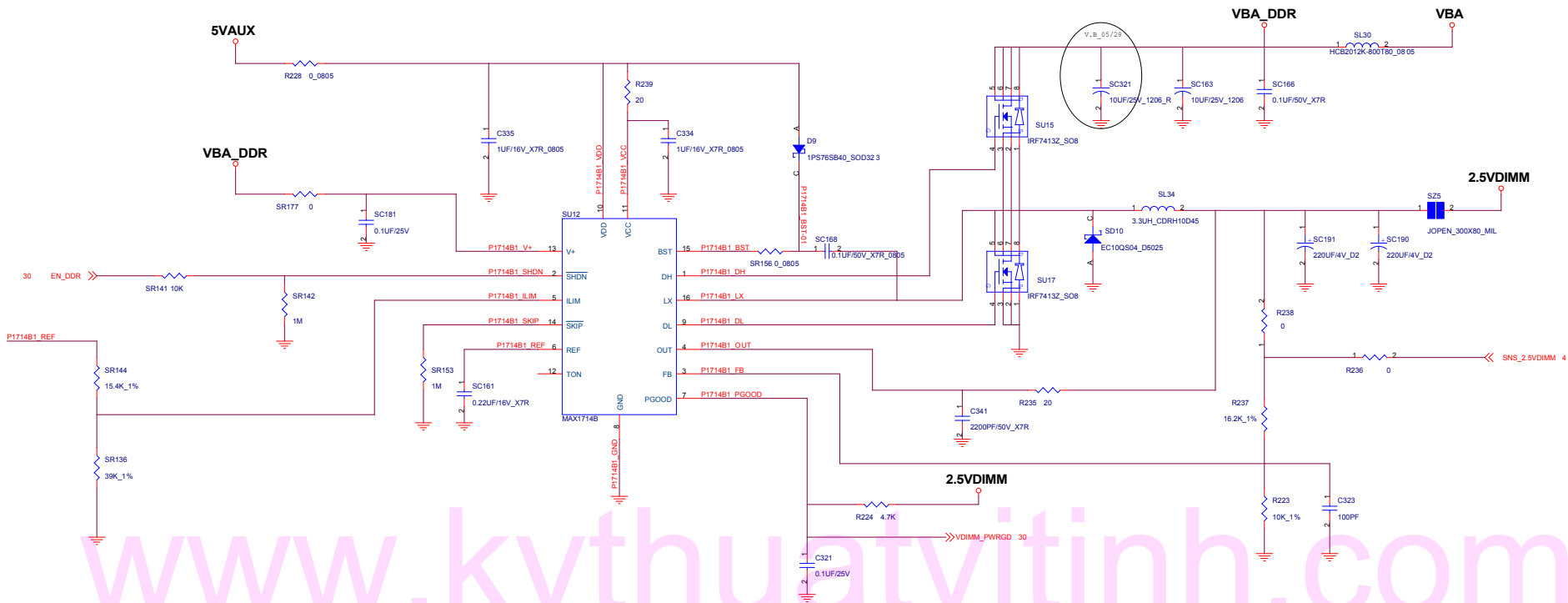
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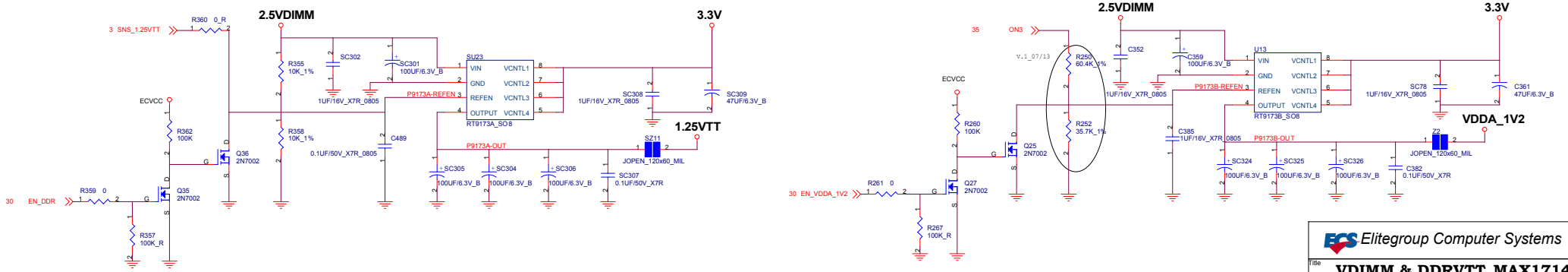


VBA_DD

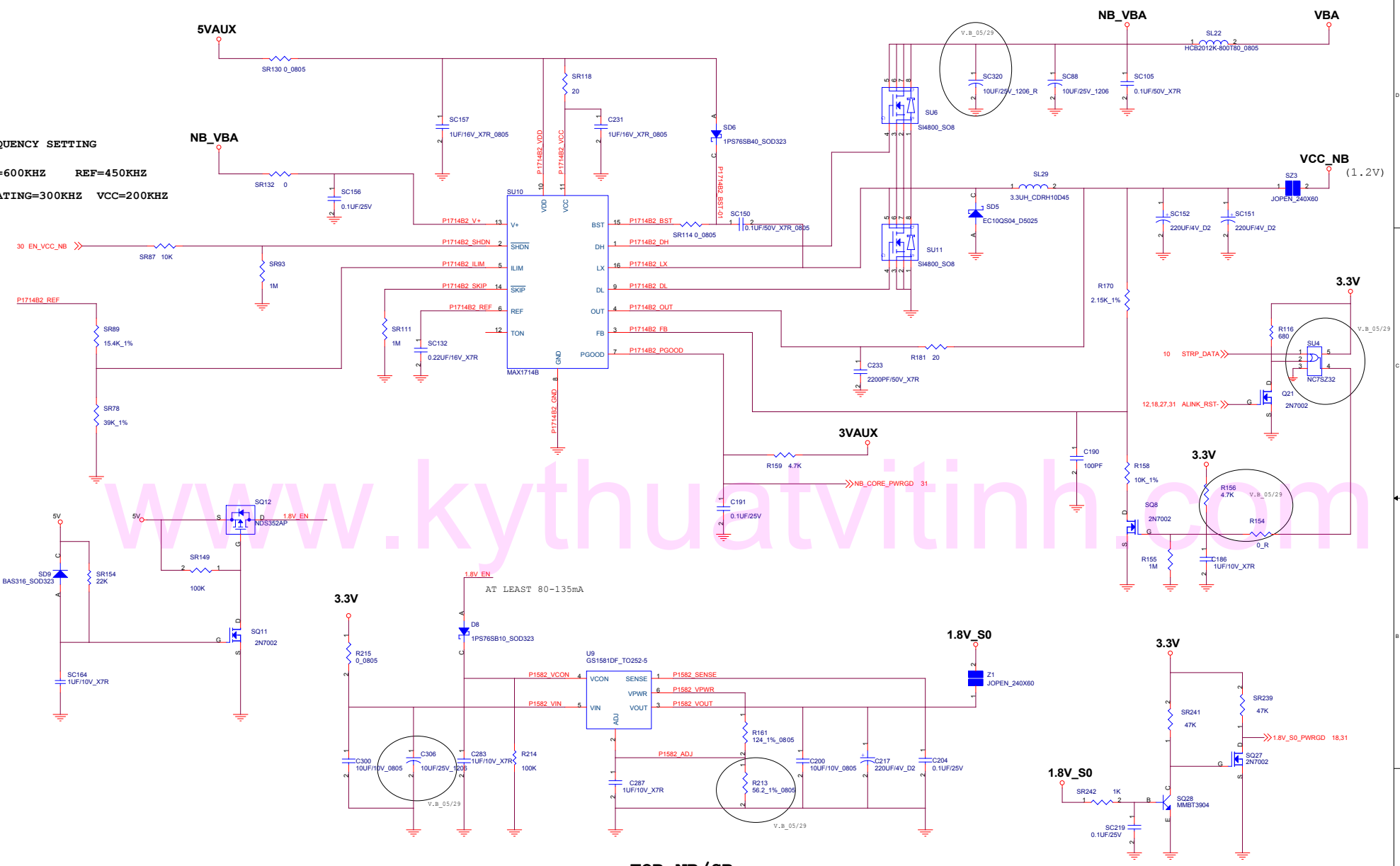




FREQUENCY SETTING
GND=600KHZ REF=450KHZ
FOLATING=300KHZ VCC=200KHZ



FREQUENCY SETTING
 GND=600KHZ REF=450KHZ
 FOLATING=300KHZ VCC=200KHZ



FOR NB/SB


331 REVISION HISTORY

V.A INITIAL

- V.B H/W
- 01.R98 VCC from 3VAUX change to VDD2.5_RUN. (page.4)
 - 02.LCD power plane SL9 used to 1.8_S0. (page.10)
 - 03.PCIRST- add SC208 2.2uF to filter noise. (page.12)
 - 04.D11 power plane chage to 3VAUX. (page.12)
 - 05.GA20 & KBRST connect to SB. (page.13)
 - 06.net PWRGD change to EC_MUTE. (page.18)
 - 07.SQ16 no function deleter it. (page.18)
 - 08.noise interference, decrease pull high resistor SRP1 10k->2.2k. (page.18)
 - 09.Backlight ON control priority shift to micro-processor R47,R35 Del, R50,R34 Add. (page.25)
 - 10.H, V sync change driving way, add Q41, Q42. (page.18)

P/W

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 Elitegroup Computer Systems		
Title REVISION HISTORY		
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