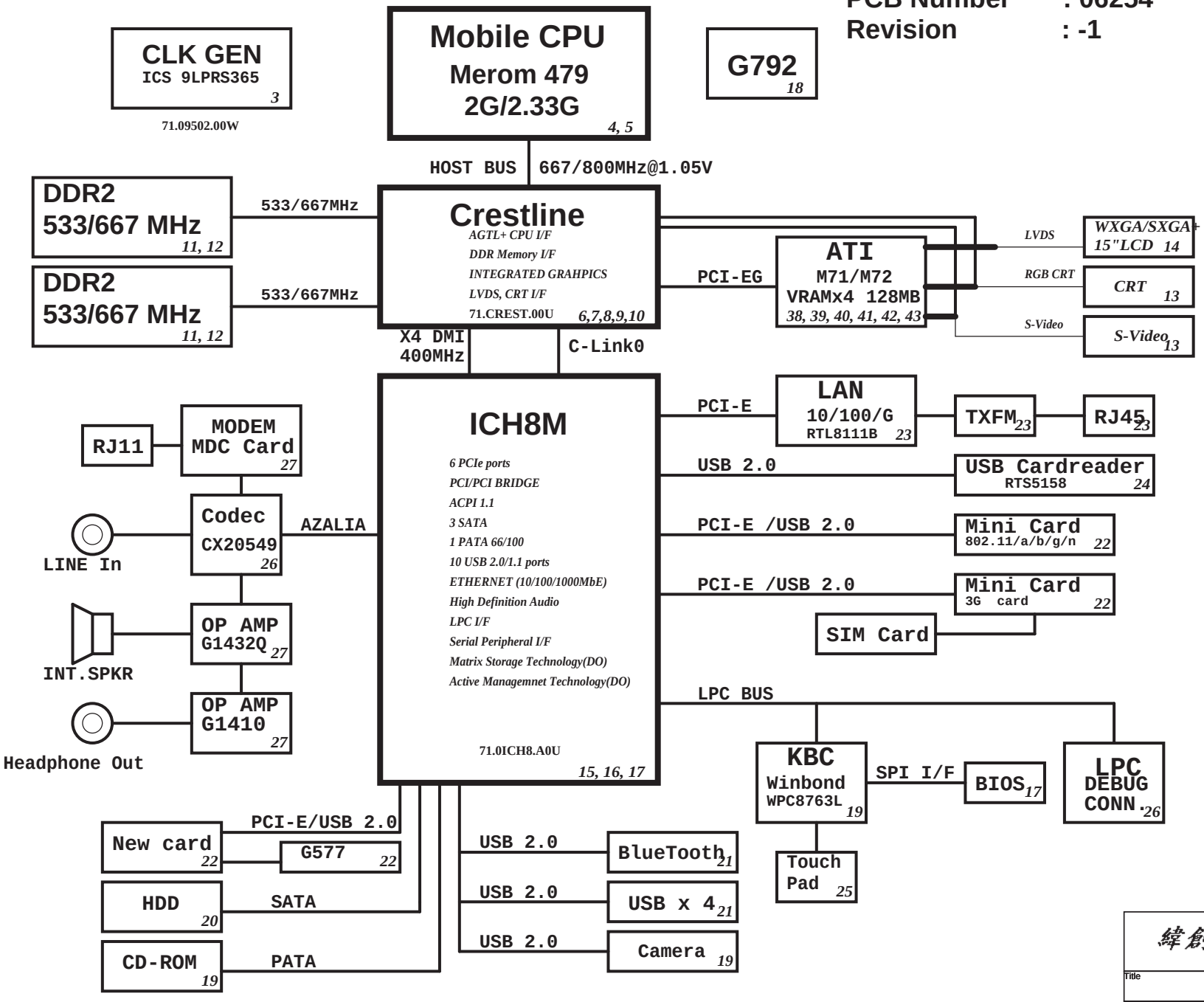
C45/C46 Block Diagram

C45 Project code: 91.4U501.001
C46 Project code: 91.4V001.001
PCB Number : 06254
Revision : -1



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC
SC411

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

SC411 TPS5110

DCBATOUT	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5913

1D8V_S3	1D5V_S0 (2A)

APL5915

3D3V_S0	2D5V_S0 (300mA)

APL5915

3D3V_S5	1D25V_S0

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

PCB STACKUP

L1: Signal 1
L2: POWER
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

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Title: BLOCK DIAGRAM
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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP TBD

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB800 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[7:6]	Reserved	
CFG8	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

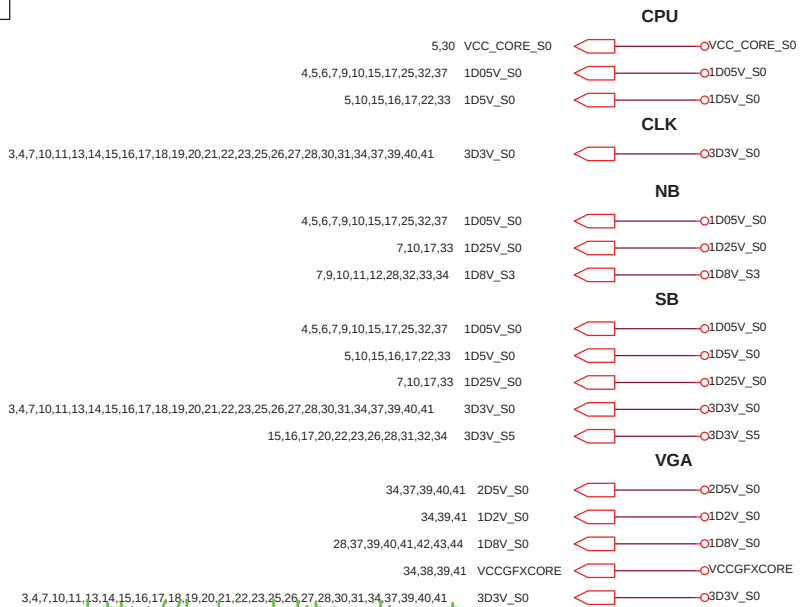
	IDSEL	INT	REQ	GNT

PCIE Routing

LANE1	LAN
LANE2	Express Card
LANE3	MiniCard WLAN
LANE4	USB Cardreader

USB Table

USB Pair	USB Device
0	USB1(ON BOARD)
1	USB2(EXT. USB)
2	USB3(EXT. USB)
3	USB4(EXT. USB)
4	MINICARD
5	USB Cardreader
6	MINICARD
7	NEW CARD
8	BLUETOOTH
9	WEBCAM



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Title: **Reference**

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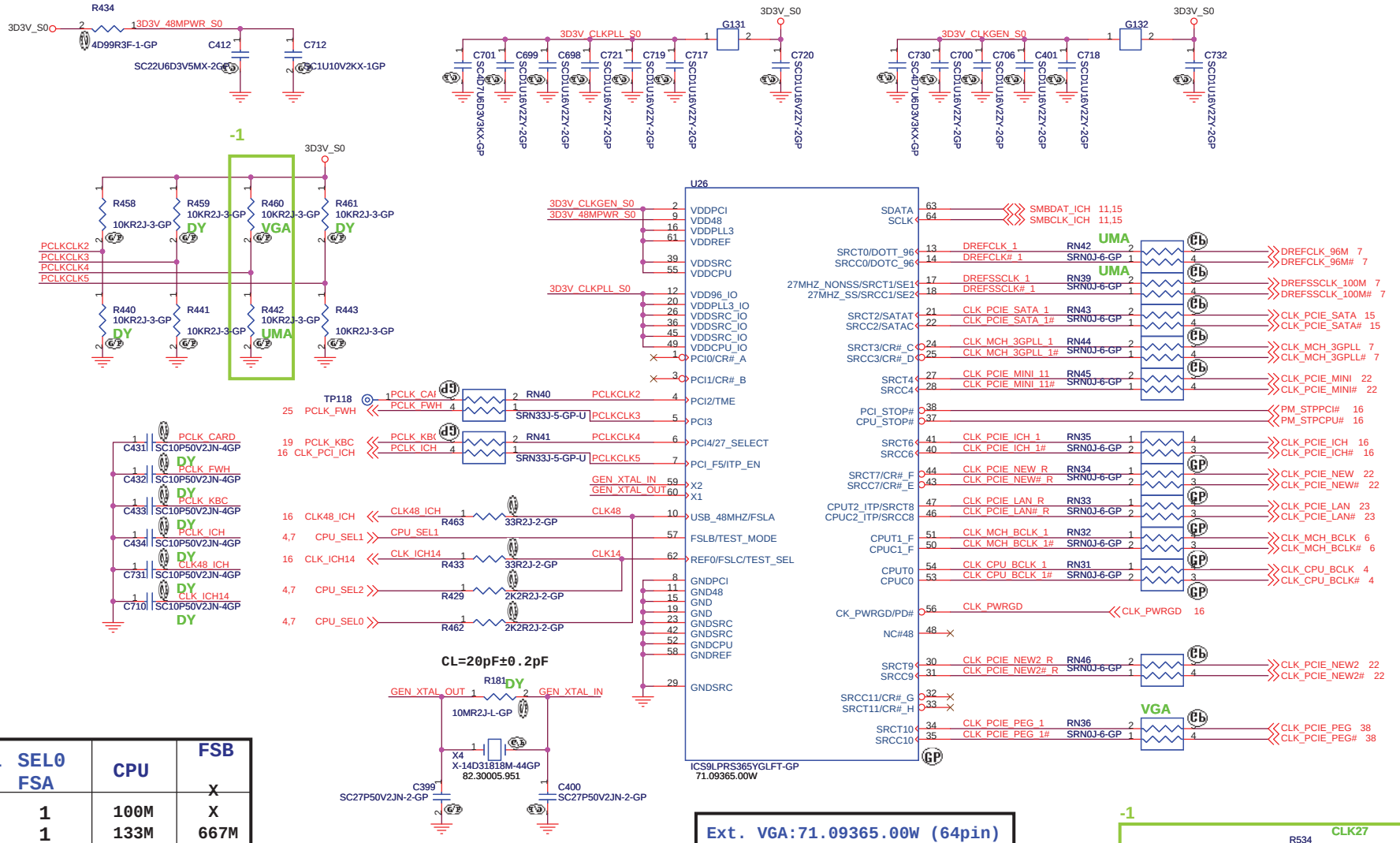
Date: Wednesday, April 25, 2007 | Sheet 2 of 45



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
				X
1	0	1	100M	X
0	0	1	133M	667M
0	1	1	166M	800M
0	1	0	200M	

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/RC-5_EN	0 = Pin37 as CPU_STOP# , pin 38 as PCI_STOP#. 1 = Pins37,38 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

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Title: Clock Generator

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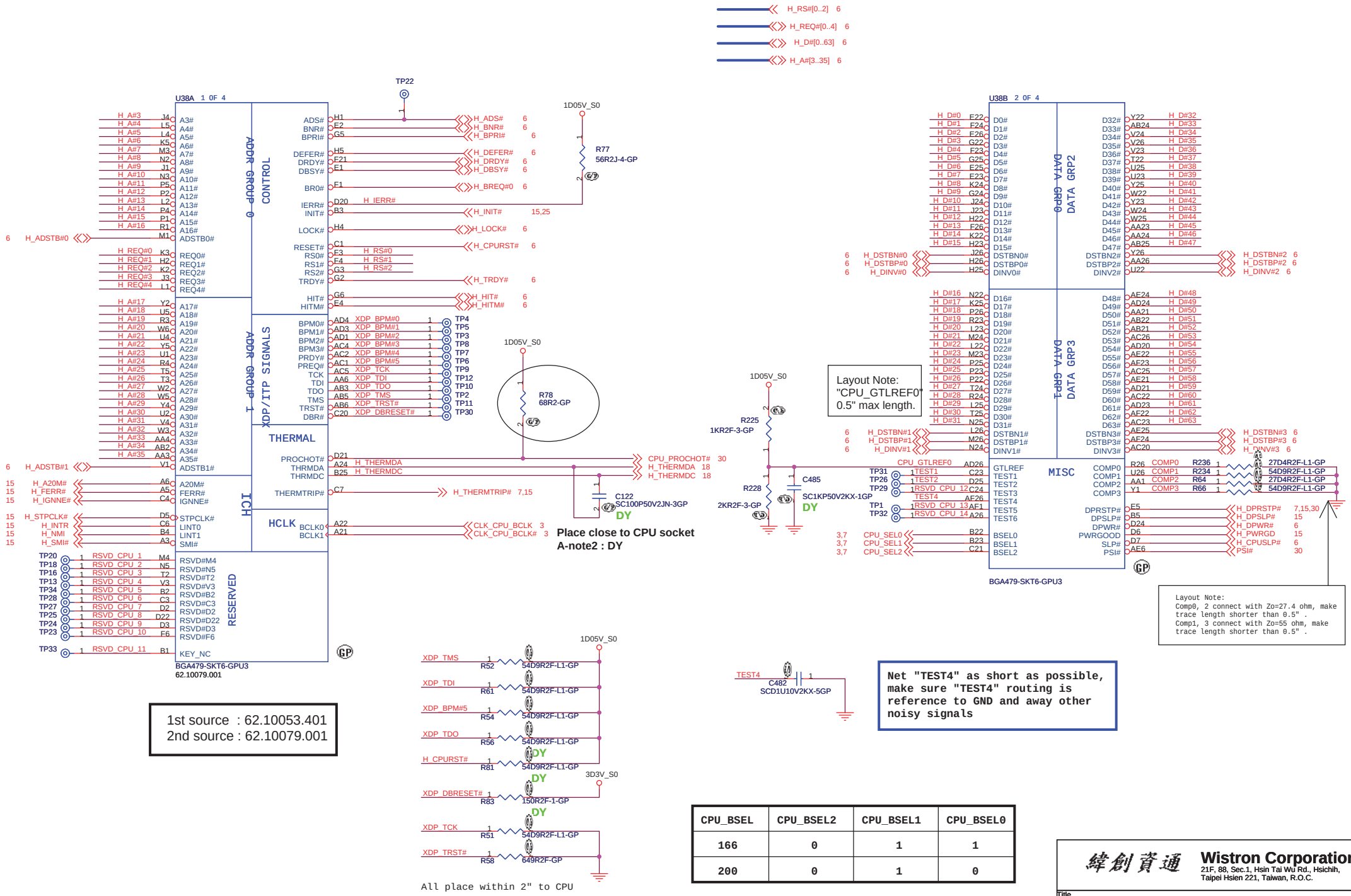
Date: Monday, May 07, 2007 | Sheet 3 of 45



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title: CPU (1 of 2) AGTL

Size: Custom | Document Number: C45/C46 | Rev: SA

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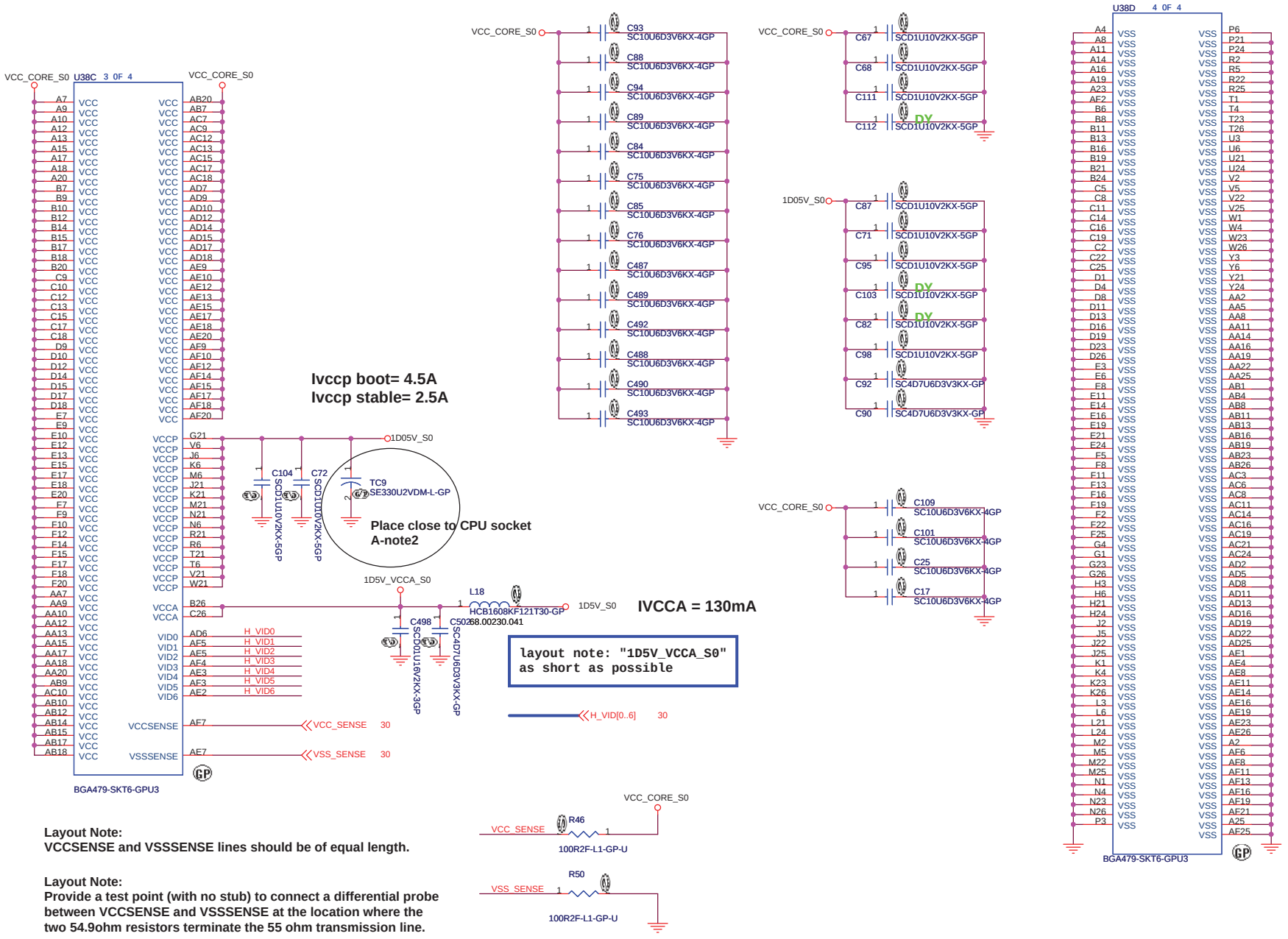

Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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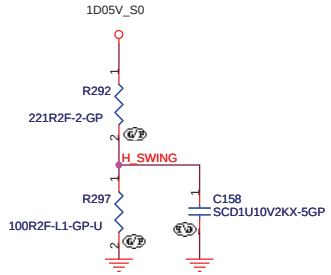
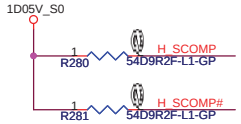
Title: CPU (2 of 2) POWER
Size: Custom | Document Number: C45/C46 | Rev: SA
Date: Wednesday, April 25, 2007 | Sheet 5 of 45

H_SWING routing Trace width and Spacing use 10 / 20 mil

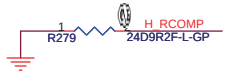
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



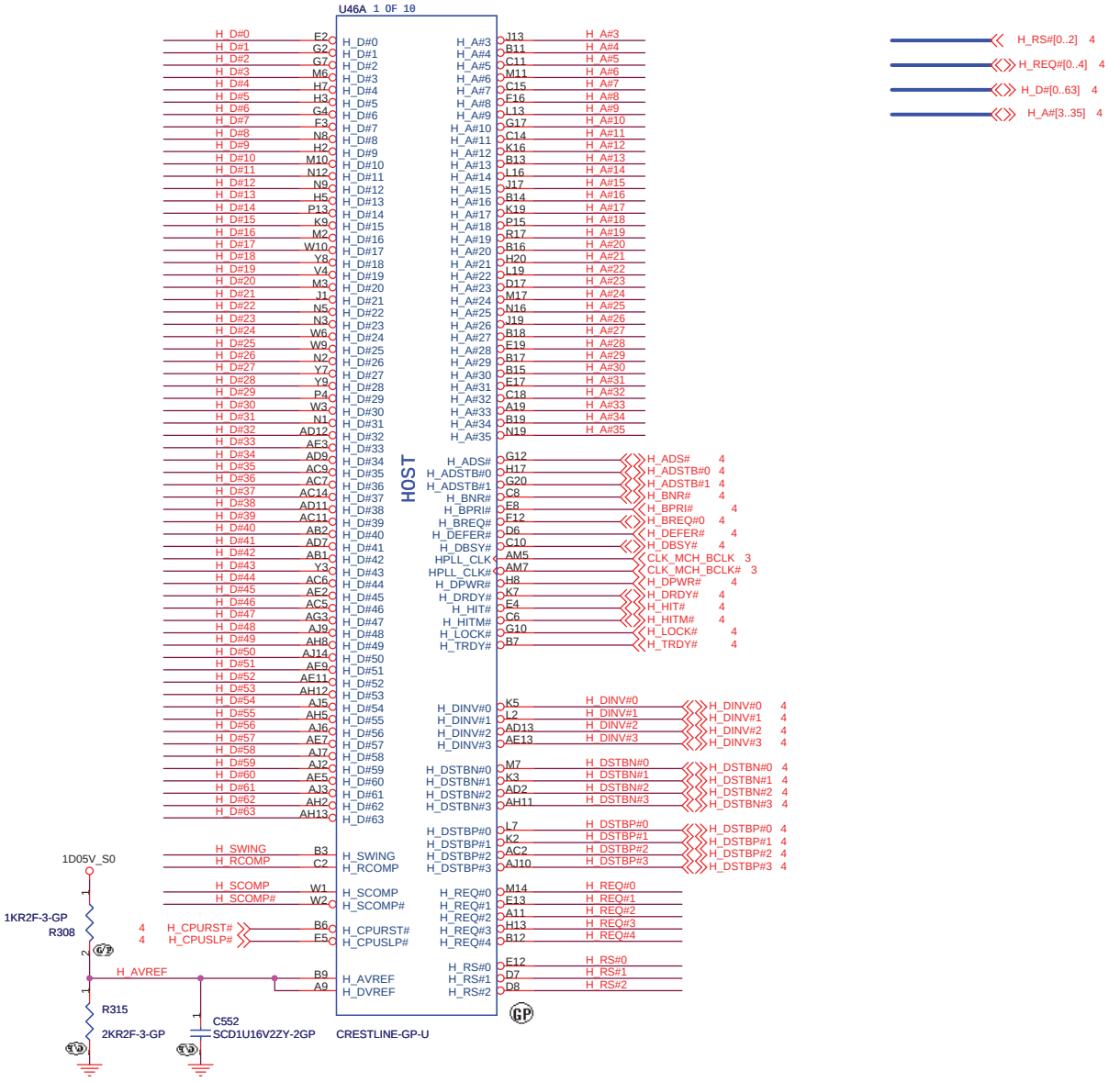
H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



H_REF Decoupling Crestline close Crestline 100 mil

965GM (71.GM965.00U)
965PM (71.PM965.00U)

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Title: *GMCH (1 of 5) AGTL*

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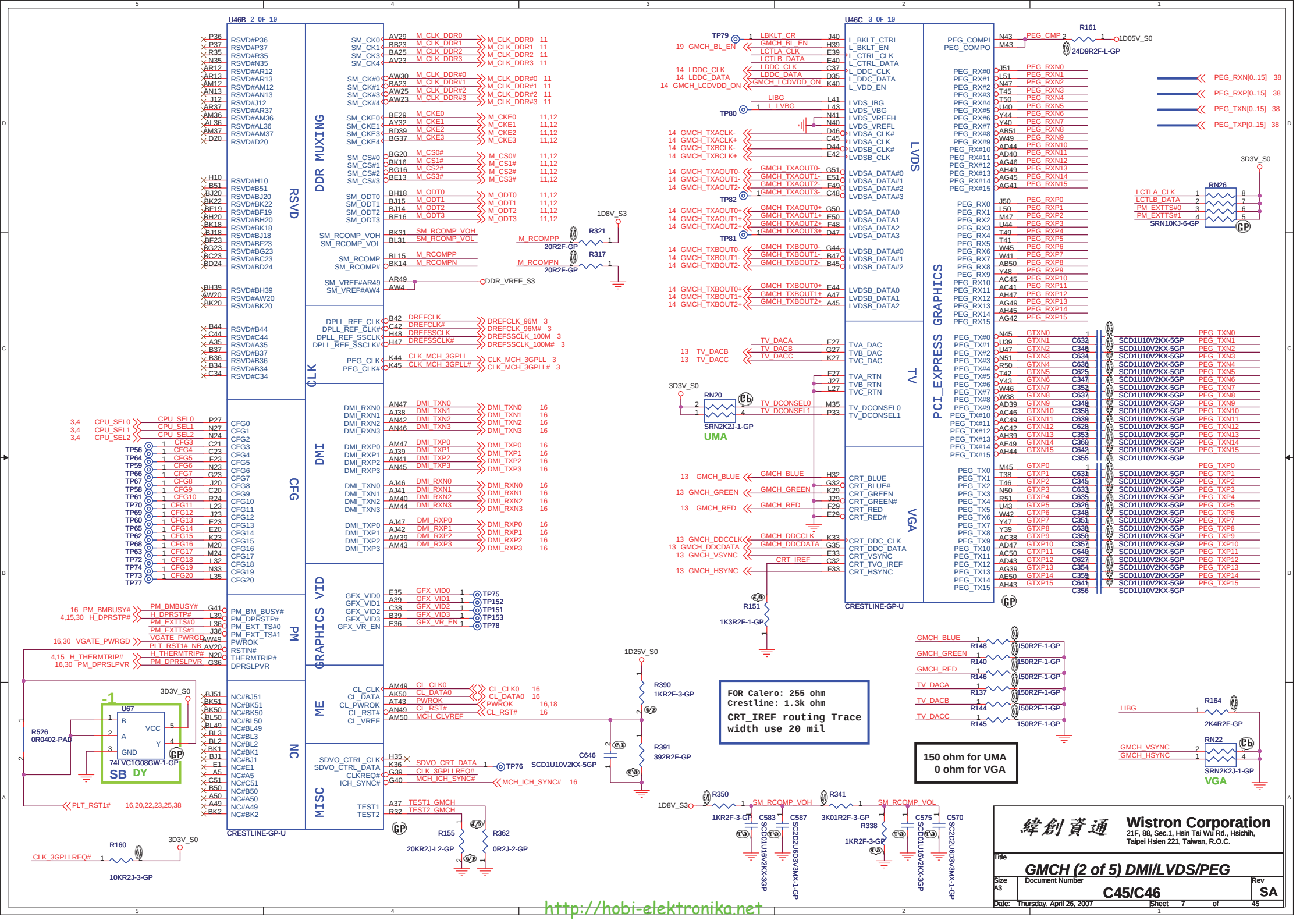
U46B 2 OF 10
RSVD
DDR MUXING
CLK
CFG
DMI
PM
GRAPHICS VID
ME
MISC
NC
CRESTLINE-GP-U
U46C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U
UMA
SB DY
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
150 ohm for UMA
0 ohm for VGA
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GMCH (2 of 5) DMI/LVDS/PEG
C45/C46
SA
Thursday, April 26, 2007
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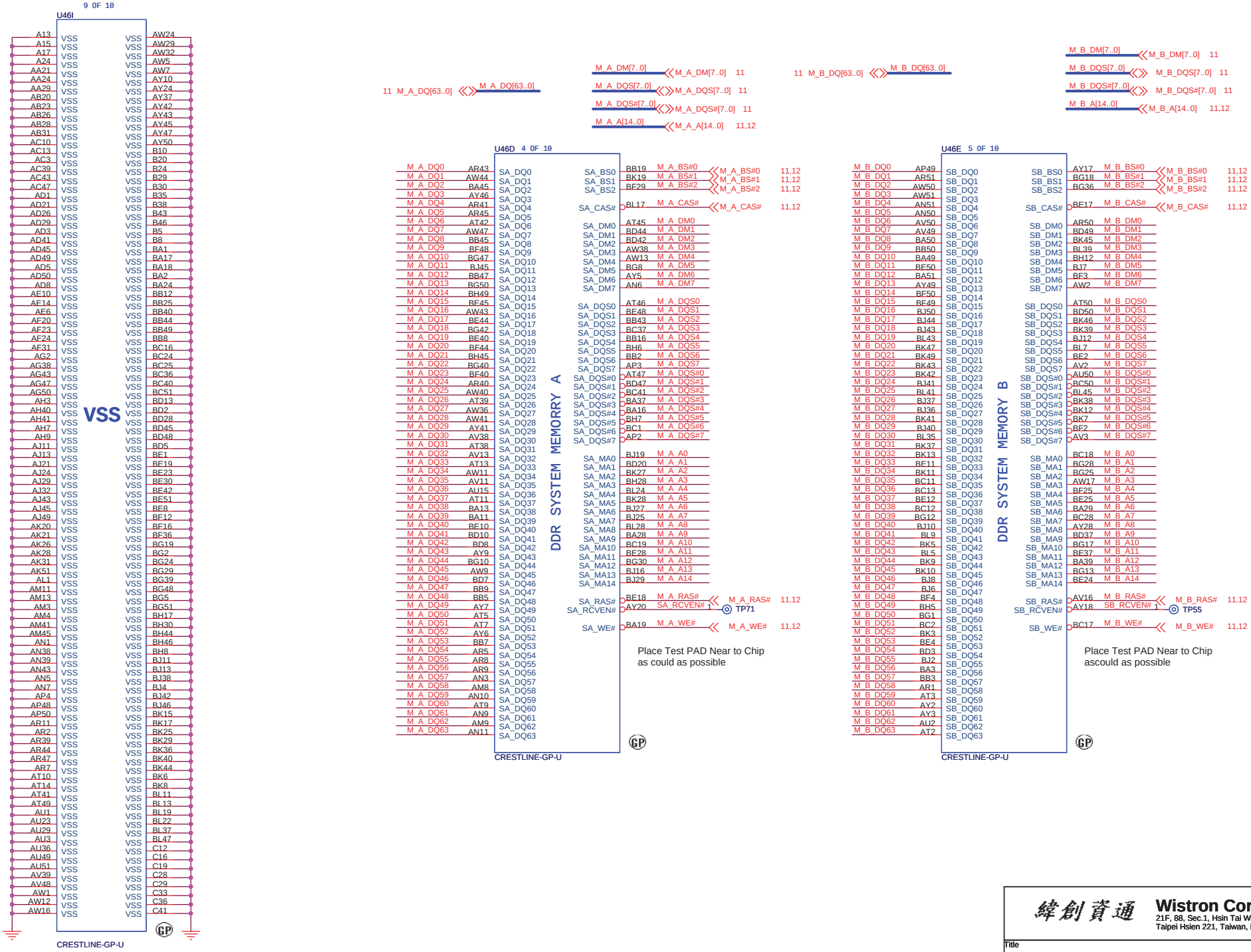

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Title: **GMCH (3 of 5) MEMORY**

Size	Document Number	Rev
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VCC_NCTF + VCC=1573mA

VCC_AXG_NCTF + VCC_AXG=7700mA

1573mA

3138mA

POWER

U46F 6 OF 10

VCC CORE

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

CRESTLINE-GP-U

FOR VCC CORE AND VCC NCTF

308 mils from the Edge
Coupling CAP

U46G 7 OF 10

VCC NCTF

VSS NCTF

VSS SCB

VSS AXM

VCC_AXM_NCTF + VCC_AXM=540mA

Place on the Edge

VSS AXM NCTF

FOR VCC SM

Place CAP where LVDS and DDR2 taps
Place on the Edge

U46J 10 OF 10

VSS

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Title	GMCH (4 of 5) POWER1
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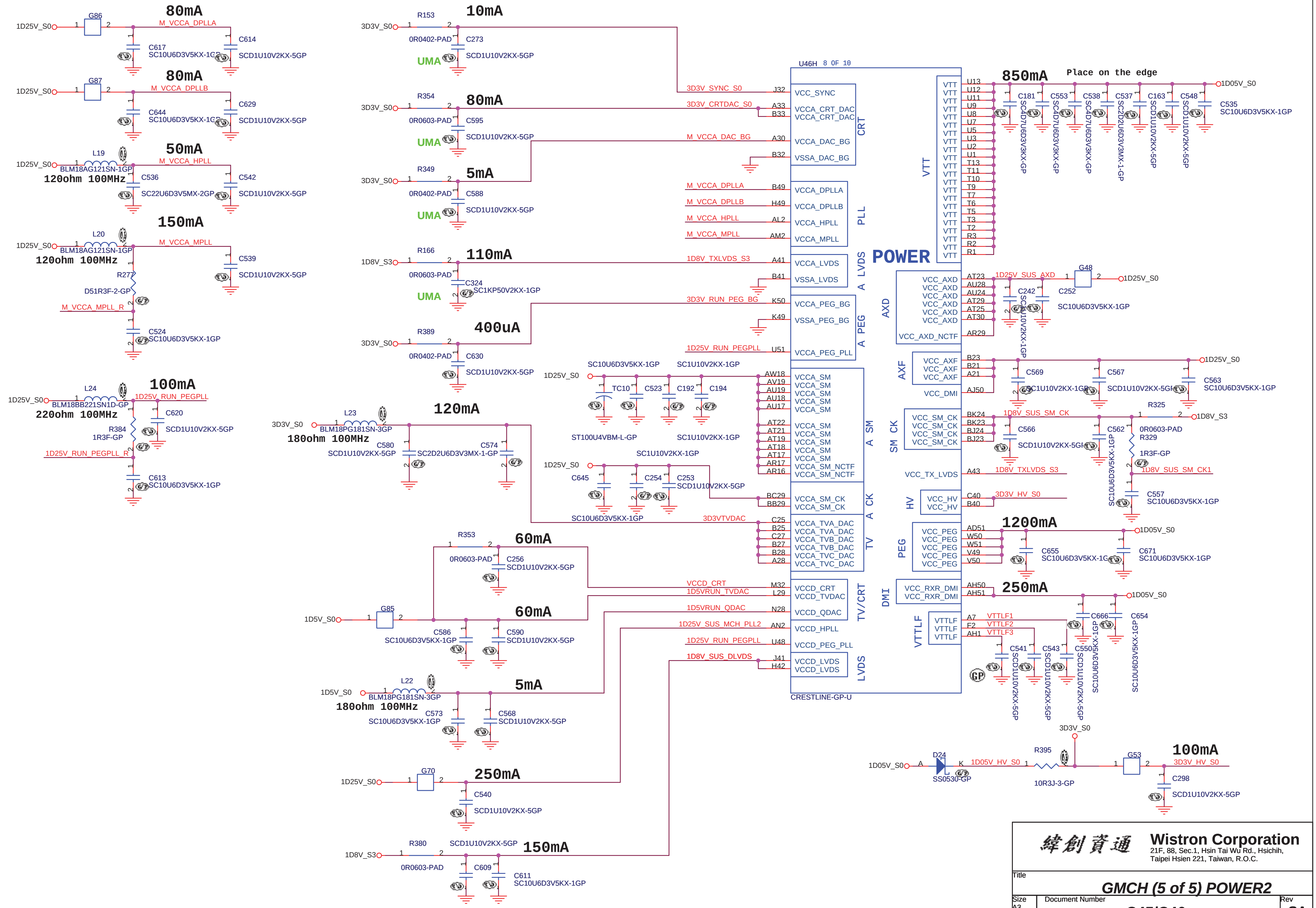

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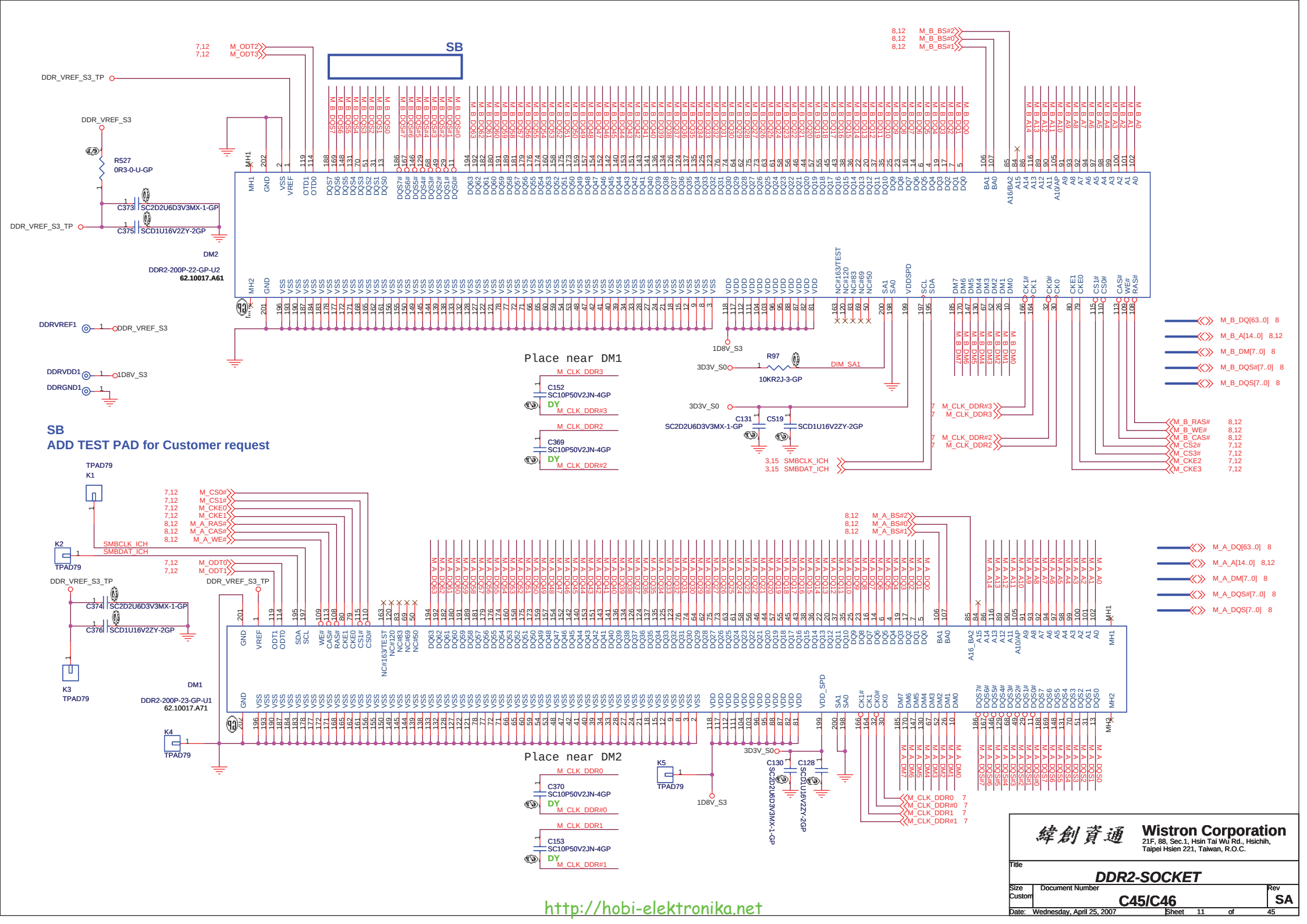
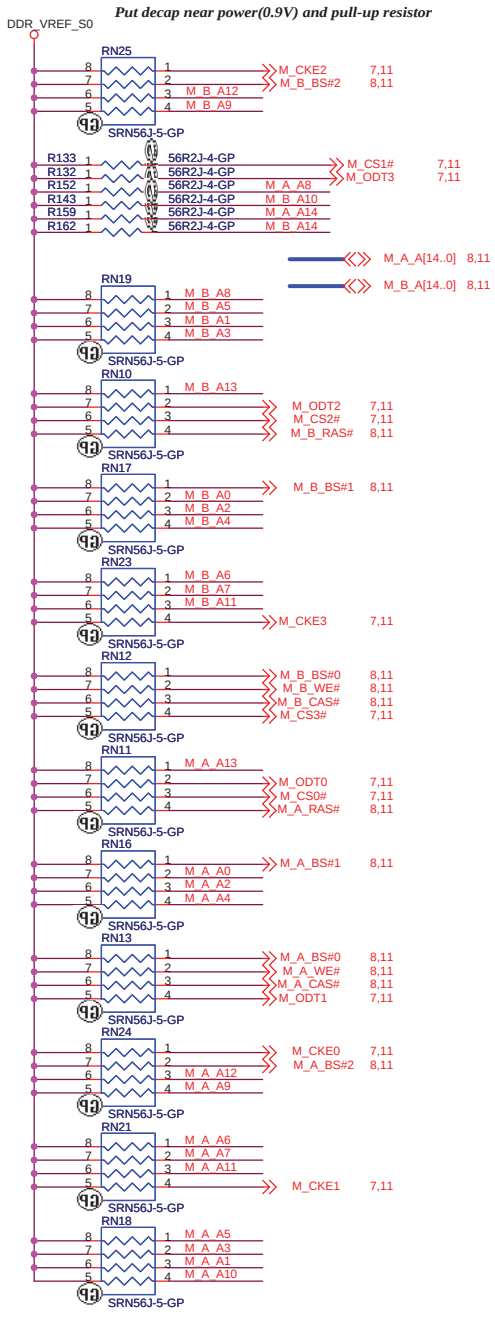
Title: **GMCH (5 of 5) POWER2**

Size	Document Number	Rev
A3	C45/C46	SA

Date: Tuesday, April 24, 2007 Sheet 10 of 45

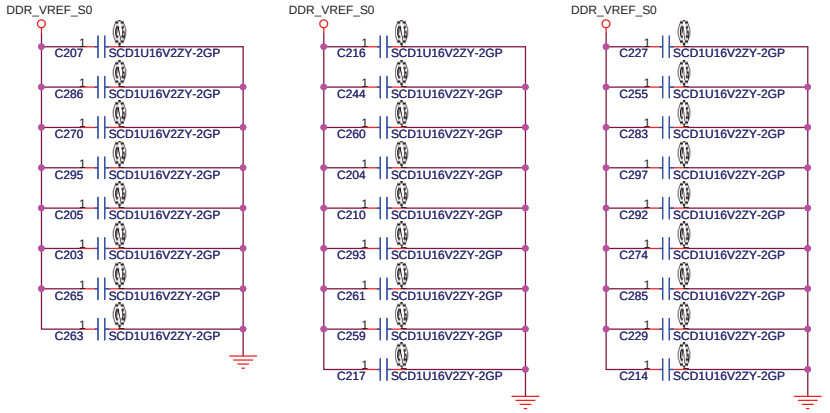


PARALLEL TERMINATION

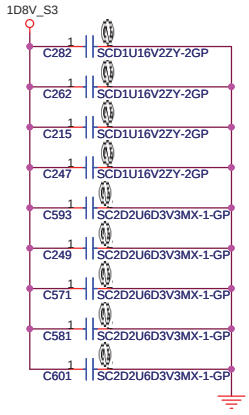


Decoupling Capacitor

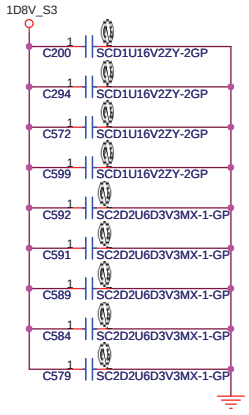
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



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Title: ***DDR2-RESISTOR&CAPACITOR***

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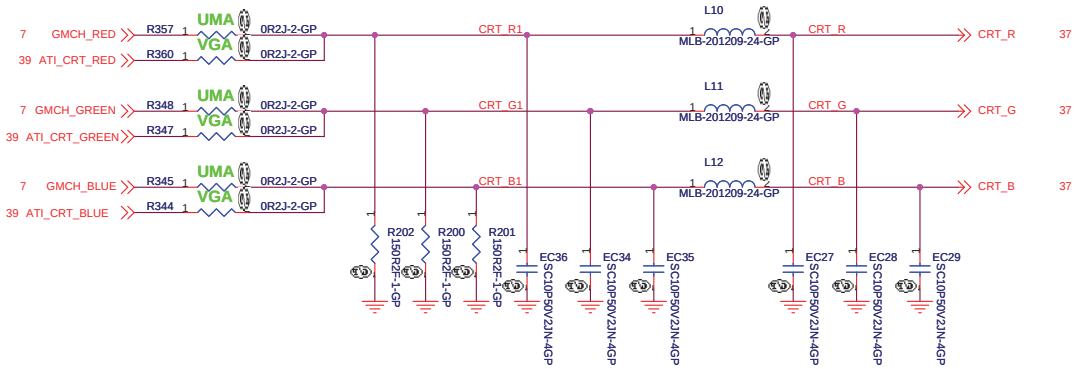
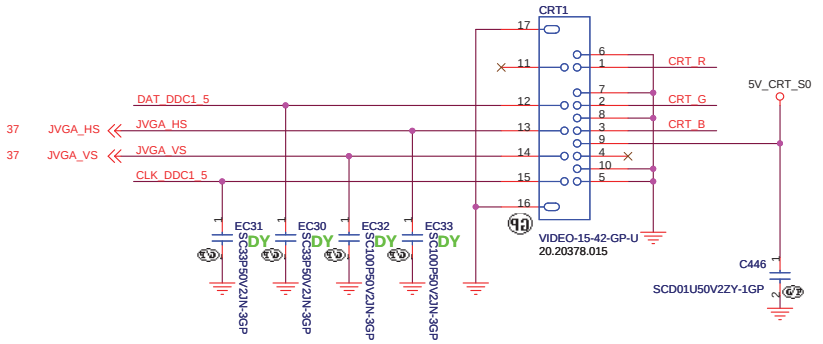
CRT CONNECTOR

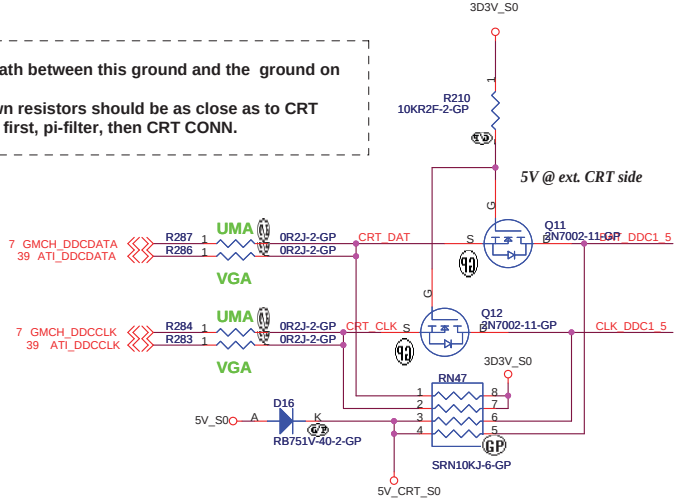
Layout Note:
Place these resistors close to the CRT-out connector

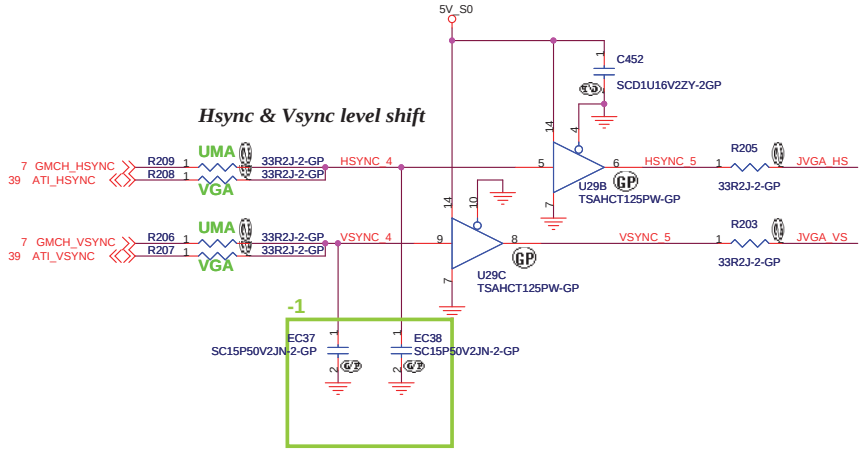
SB
Change L10, L11, L12 the same as X40



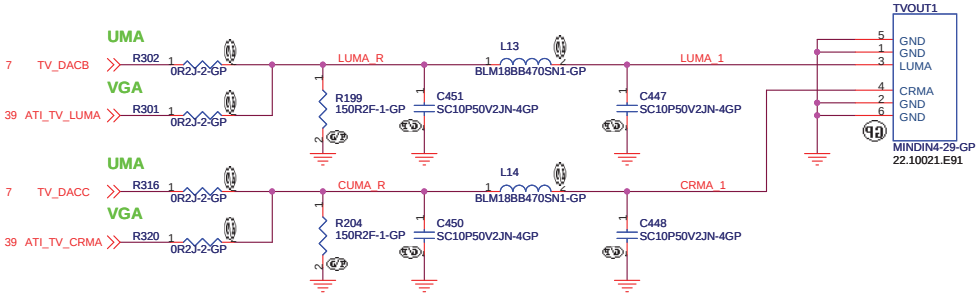


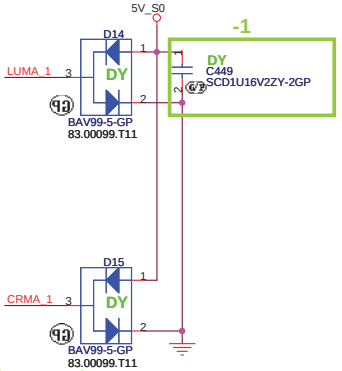
Layout Note:
*** Must be a ground return path between this ground and the ground on the VGA connector.**
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





S-VIDEO CONNECTOR





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Title	***CRT/S-Video***	
Size Custom	Document Number **C45/C46**	Rev **-1**
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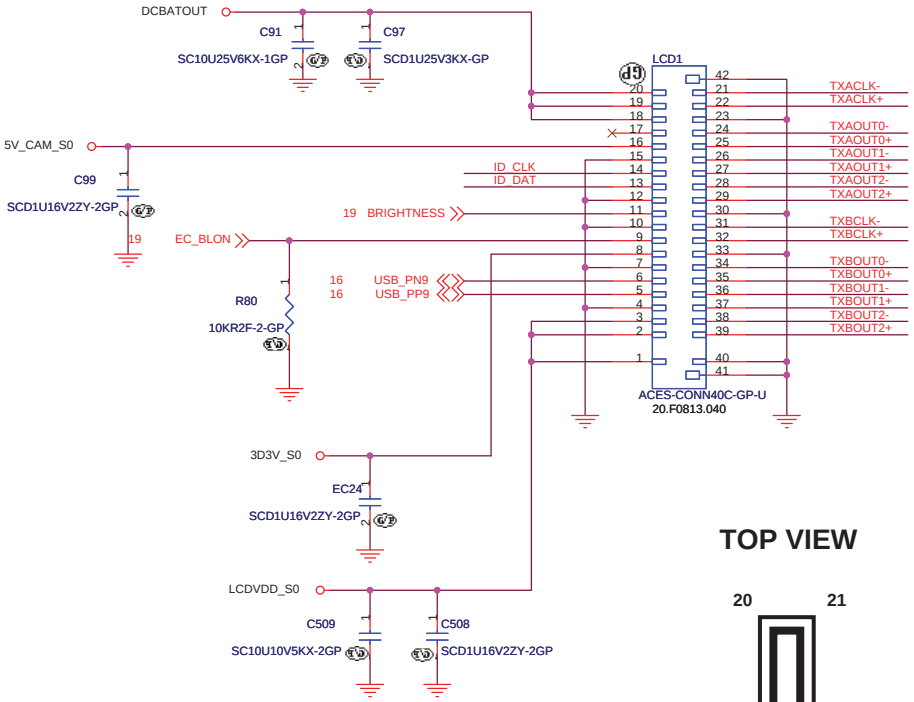
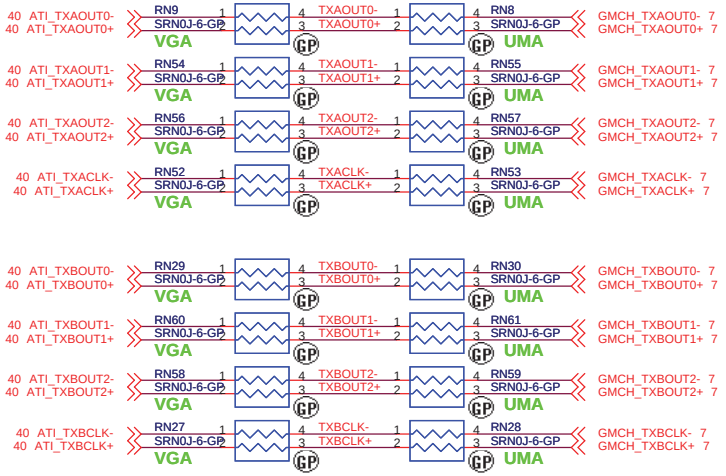
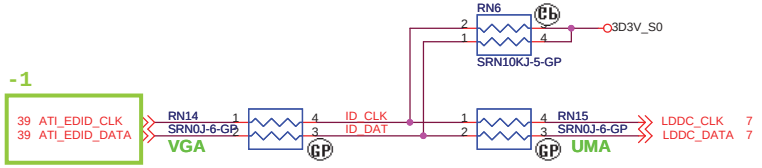
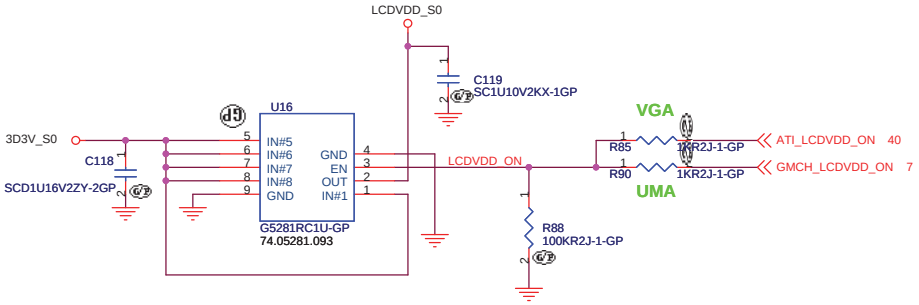
LCD CONNECTOR



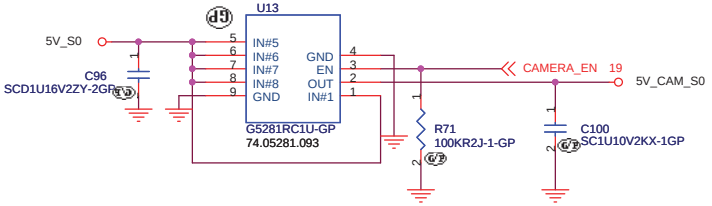
TOP VIEW







CAMERA POWER

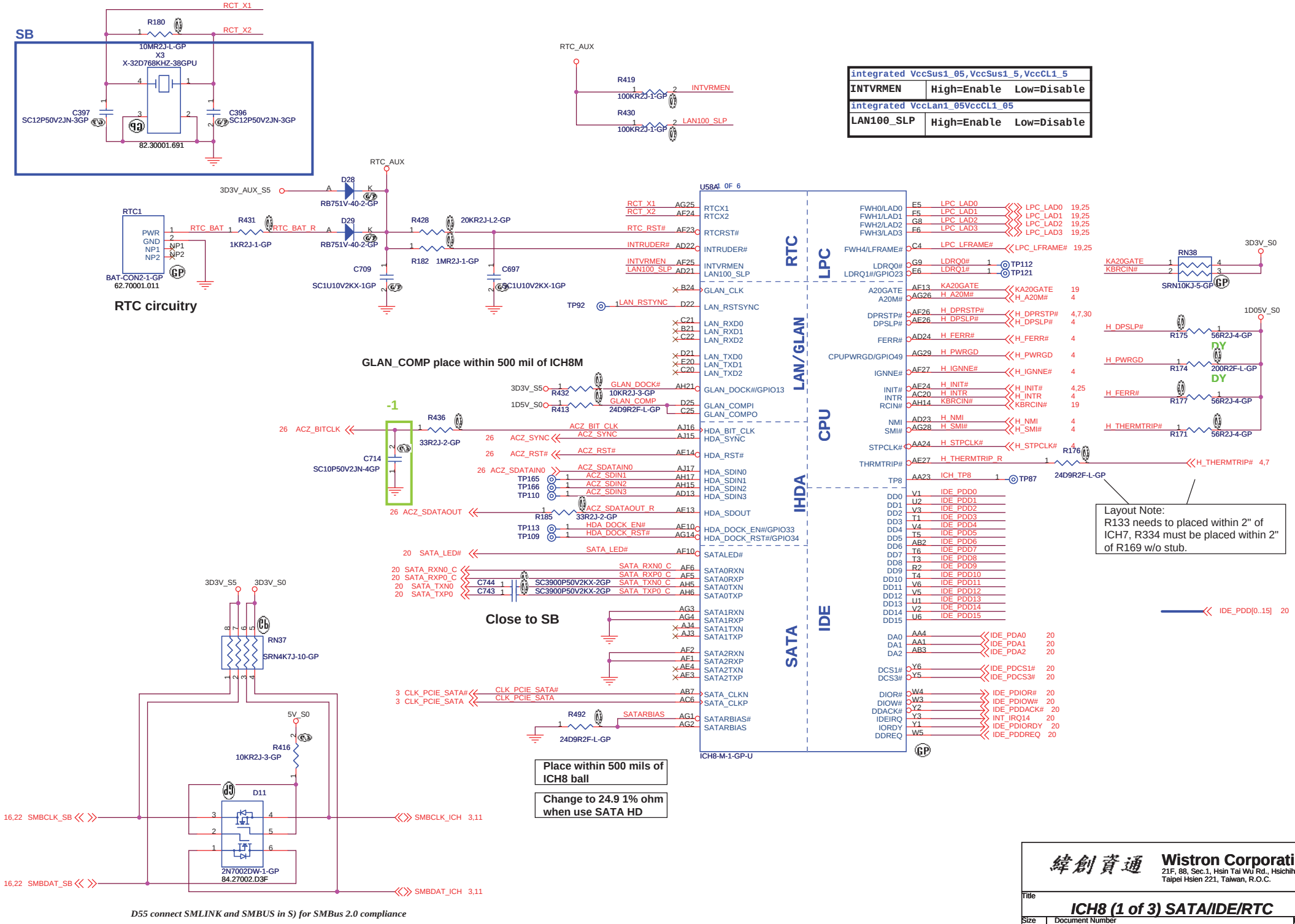


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/DVI CONN

Size: A3 | Document Number: C45/C46 | Rev: SA

Date: Thursday, April 26, 2007 | Sheet 14 of 45

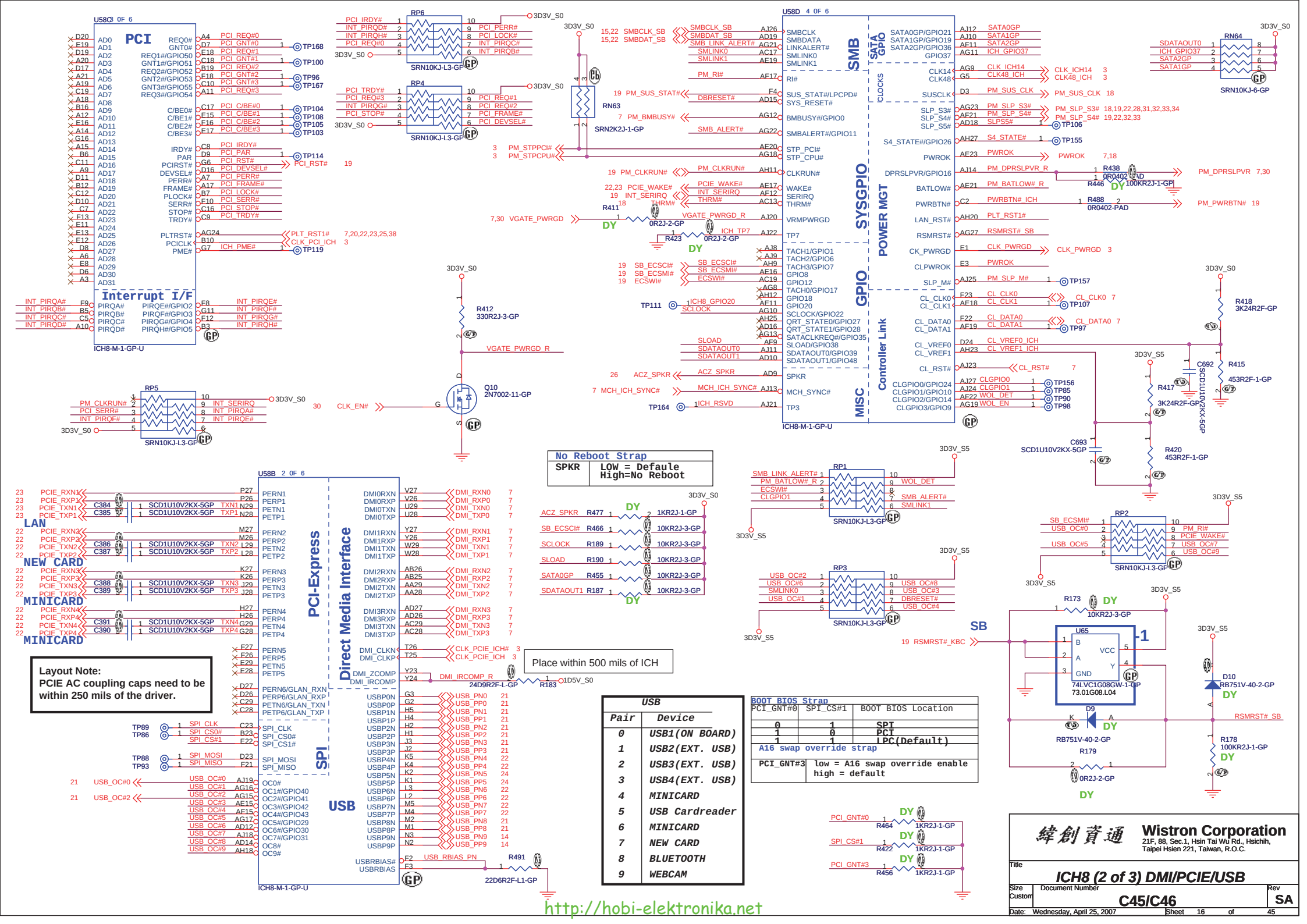


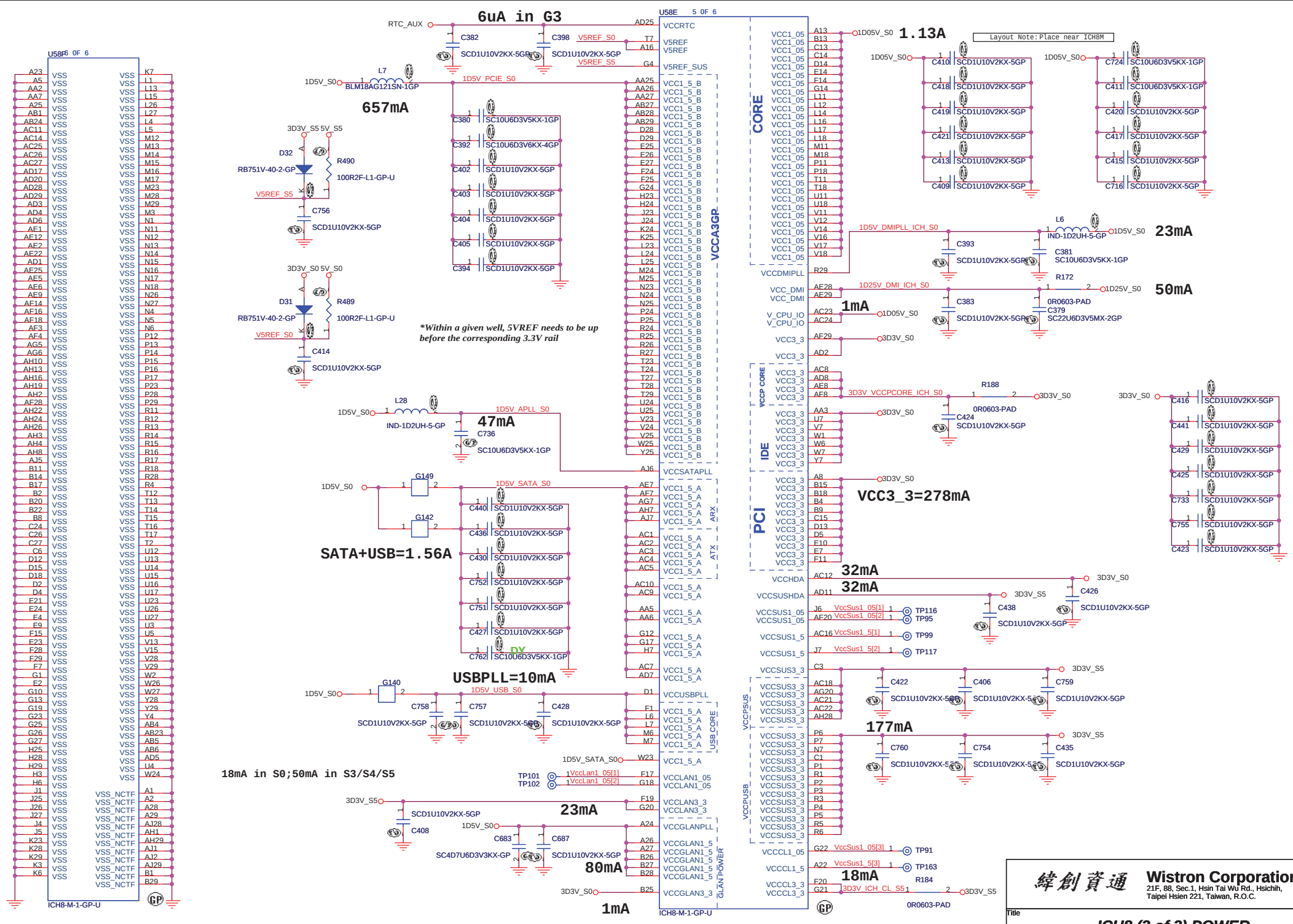
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

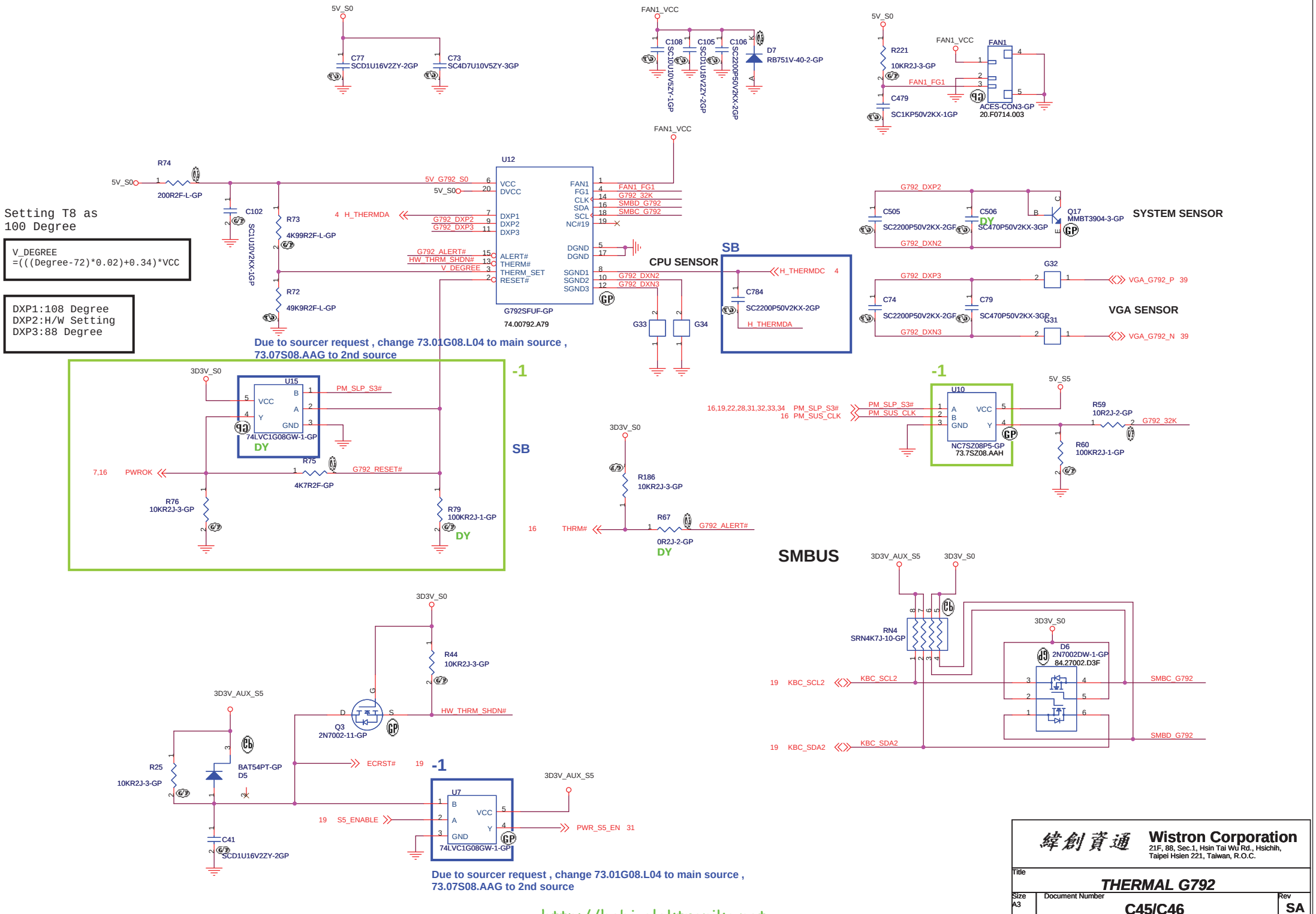
Title: ICH8 (1 of 3) SATA/IDE/RTC

Size: Custom | Document Number: C45/C46 | Rev: SA

Date: Friday, April 27, 2007 | Sheet 15 of 45


PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
PCI-Express
Direct Media Interface
SPI
USB
LAN
NEW CARD
MINICARD
MINICARD
SRN10KJ-L3-GP
SRN2K2J-1-GP
RN63
SRN10KJ-6-GP
100KR2J-1-GP
0R2J-2-GP
Q10
2N7002-11-GP
74LVC1G08GW-1-GP
73.01G08.L04
RB751V-40-2-GP
Layout Note:
PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
No Reboot Strap
SPKR | LOW = Defaule High=No Reboot
USB
Pair | Device
0 USB1(ON BOARD)
1 USB2(EXT. USB)
2 USB3(EXT. USB)
3 USB4(EXT. USB)
4 MINICARD
5 USB Cardreader
6 MINICARD
7 NEW CARD
8 BLUETOOTH
9 WEBCAM
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8 (2 of 3) DMI/PCIE/USB
Size Custom
Document Number
C45/C46
Rev SA
Date: Wednesday, April 25, 2007
Sheet 16 of 45
http://hobi-elektronika.net


6uA in G3
657mA
47mA
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
32mA
32mA
177mA
18mA
VCC3_3=278mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
ICH8-M-1-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH8 (3 of 3) POWER
C45/C46
Tuesday, April 24, 2007
http://hobi-elektronika.net

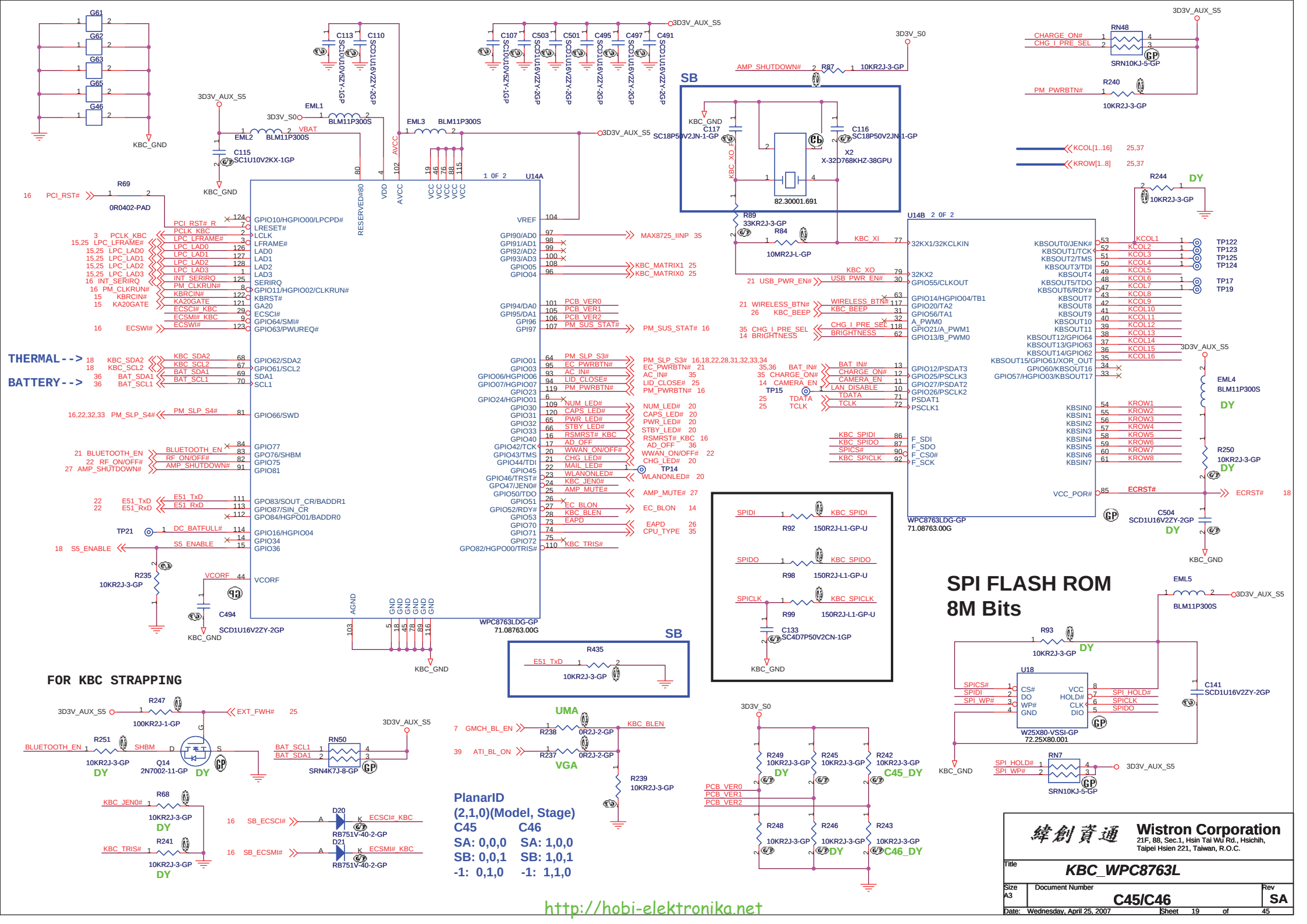


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

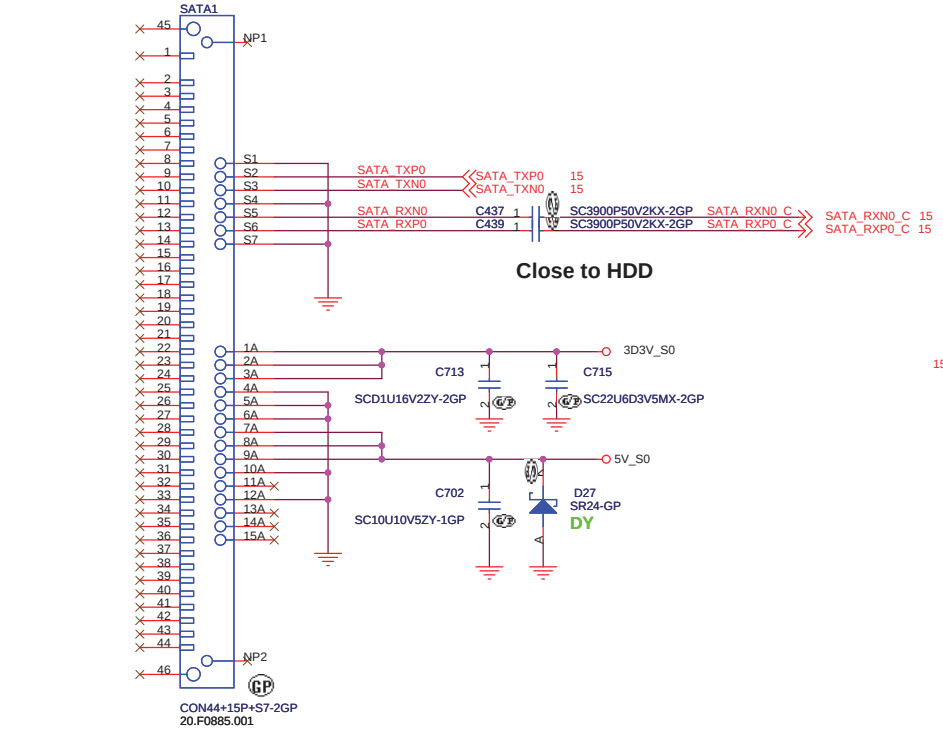
Title: ***THERMAL G792***

Size	Document Number	Rev
A3	C45/C46	SA

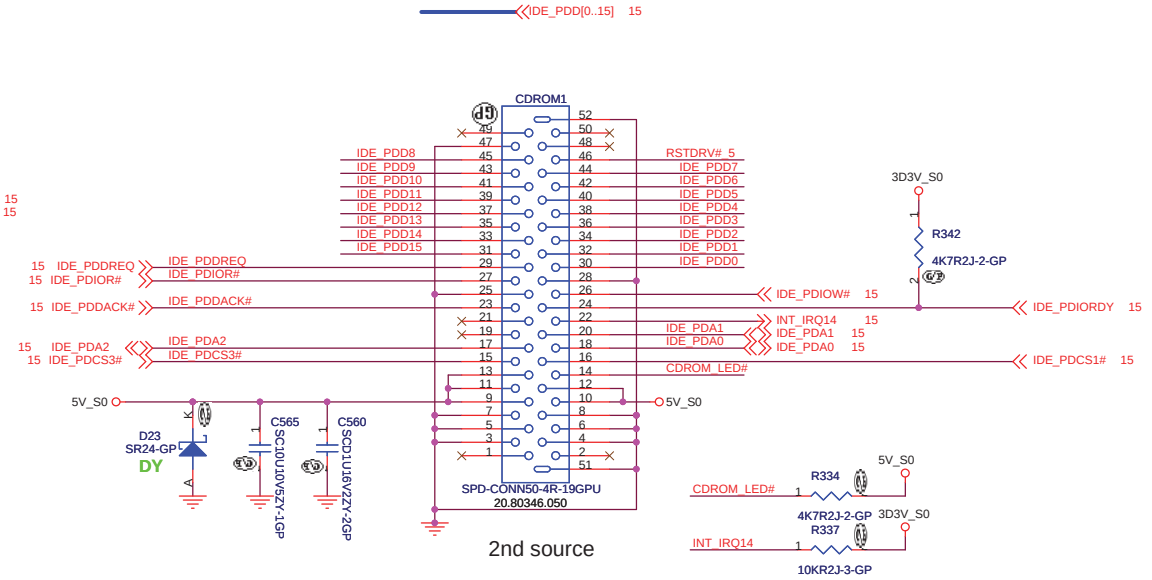
Date: Thursday, April 26, 2007 Sheet 18 of 45


THERMAL - - >
BATTERY - - >
SB
U14A
WPC8763LDG-GP
71.08763.00G
SPI FLASH ROM
8M Bits
FOR KBC STRAPPING
UMA
VGA
PlanarID
(2,1,0)(Model, Stage)
C45 C46
SA: 0,0,0 SA: 1,0,0
SB: 0,0,1 SB: 1,0,1
-1: 0,1,0 -1: 1,1,0
C45_DY
C46_DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_WPC8763L
C45/C46
SA
Wednesday, April 25, 2007
19
45
http://hobi-elektronika.net

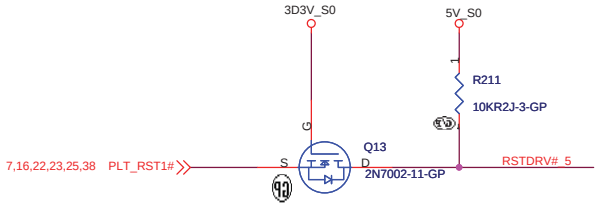
SATA HDD Connector

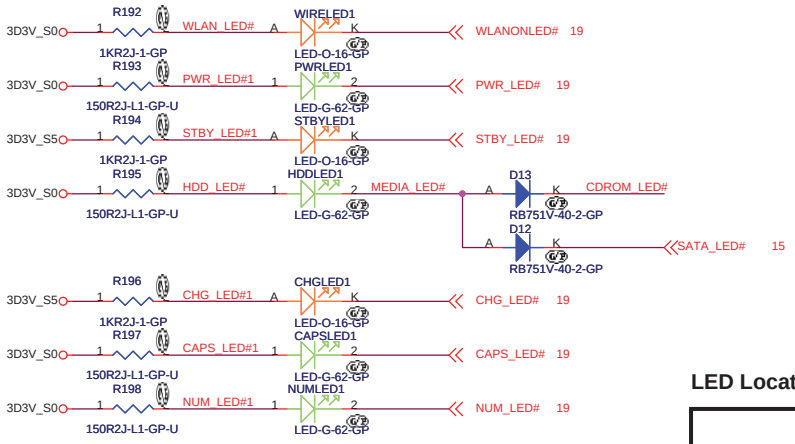


CD-ROM CONNECTOR

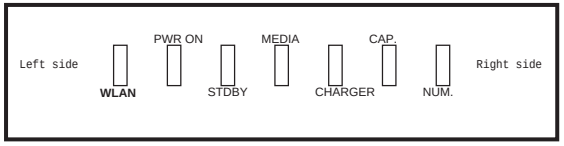


PCIRST# 3V to 5V level shift for HDD & CDROM





LED Location and Sequence (The edge of PCB,Top view)



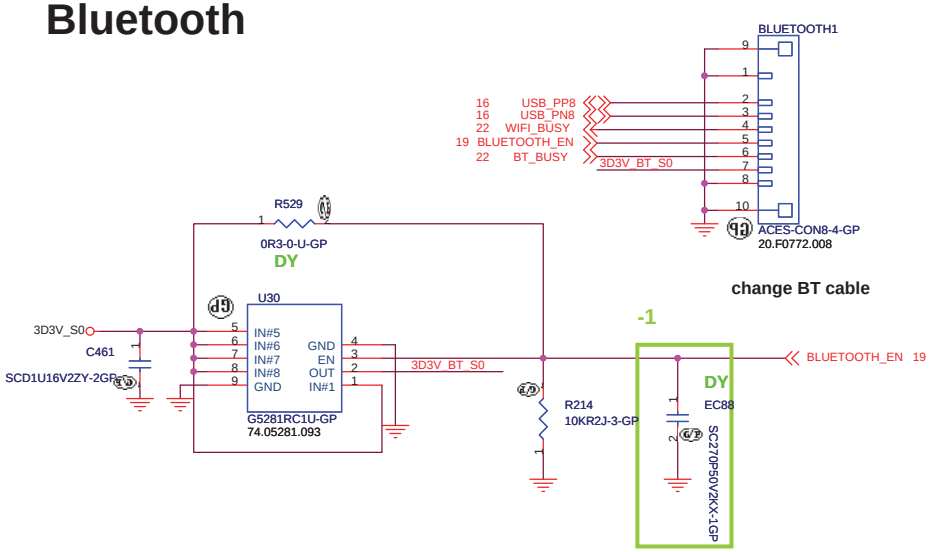
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD/CDROM/LED***

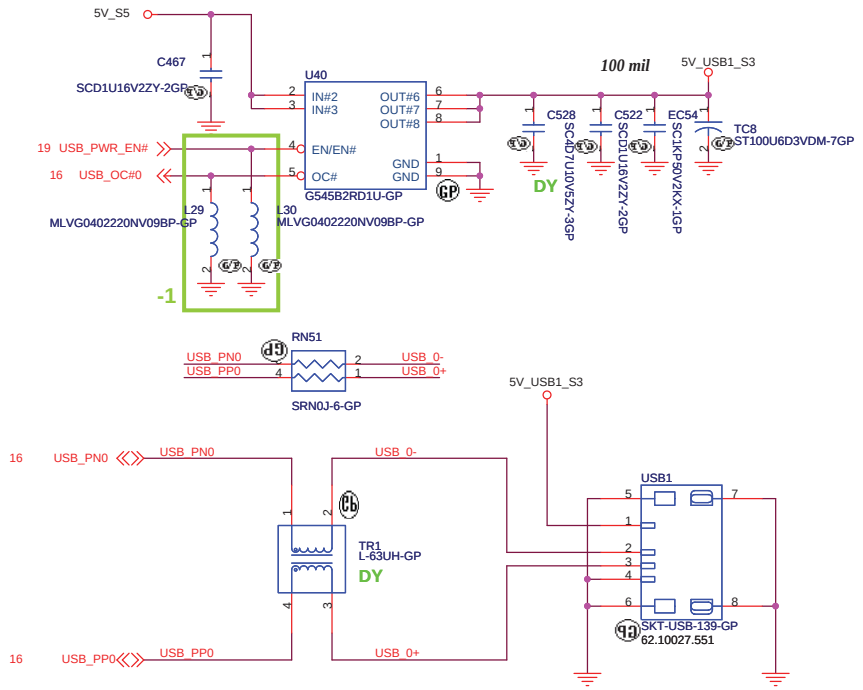
Size	Document Number	Rev
Custom	C45/C46	SA

Date: Wednesday, April 25, 2007 Sheet 20 of 45

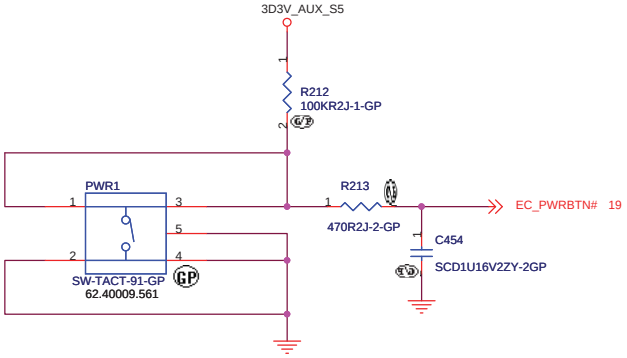
Bluetooth



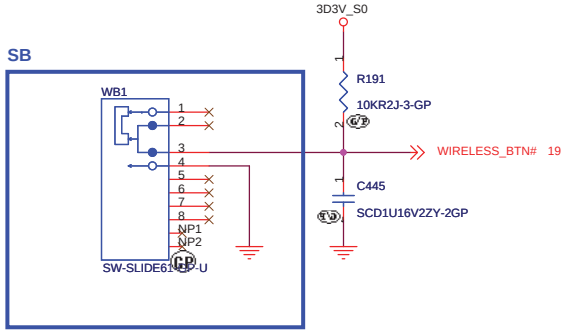
USB PORT



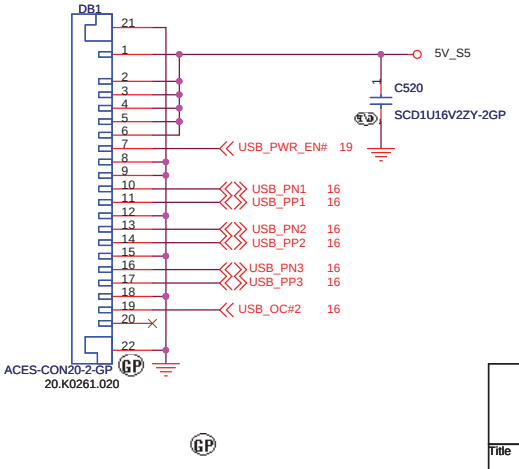
LAUNCH BOTTON



WIRELESS BOTTON



USB BOARD CONN



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB/BT/DB/LAUNCH	
Size: Custom	Document Number: C45/C46	Rev: SA
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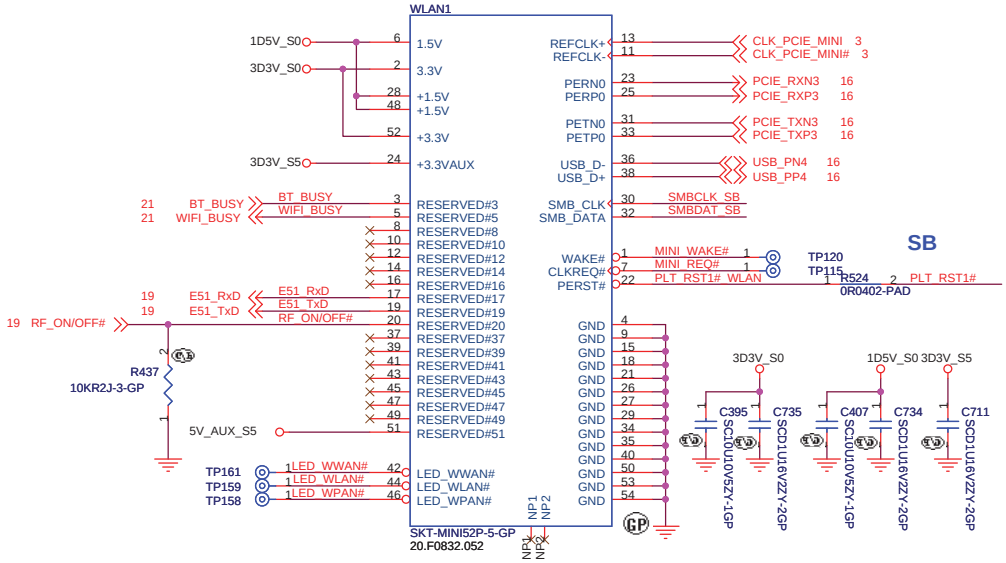
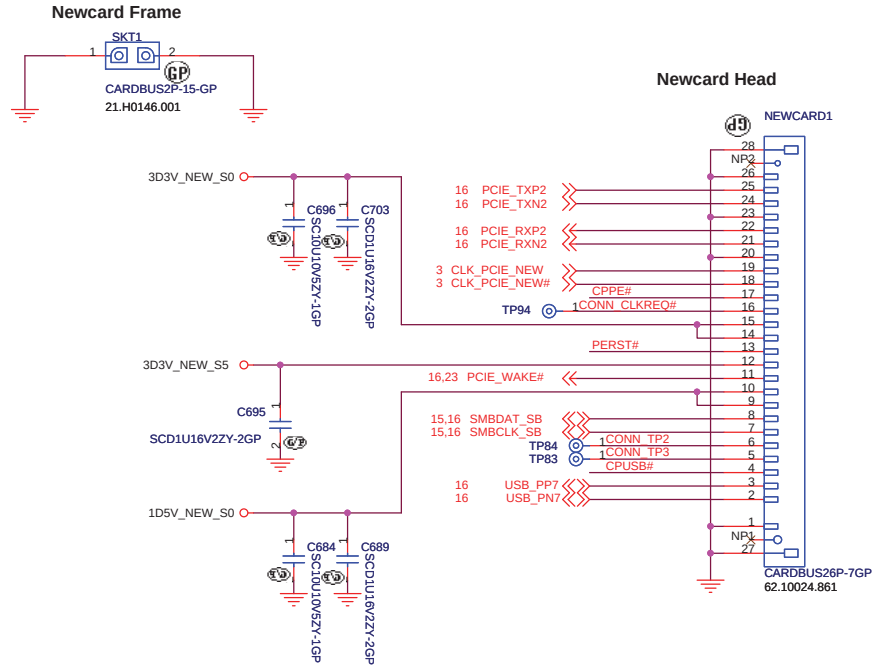
Mini Card Connector

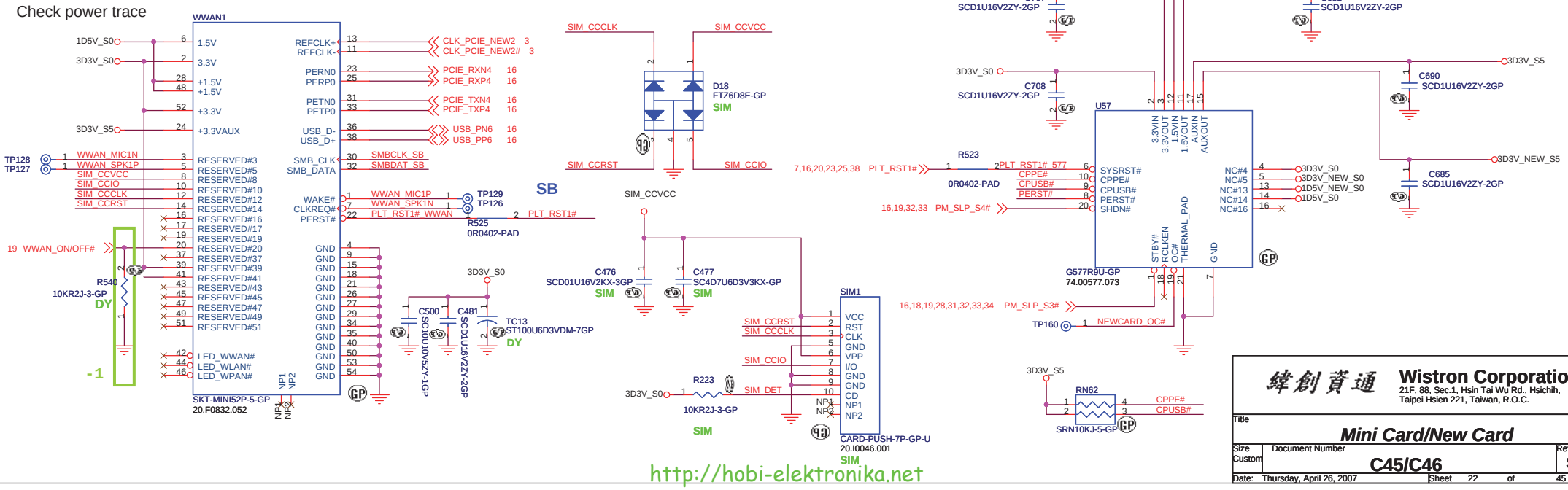


NEWCARD Connector



WWAN Connector

Check power trace



Place them Near to Chip

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Mini Card/New Card***

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Custom	C45/C46	SA

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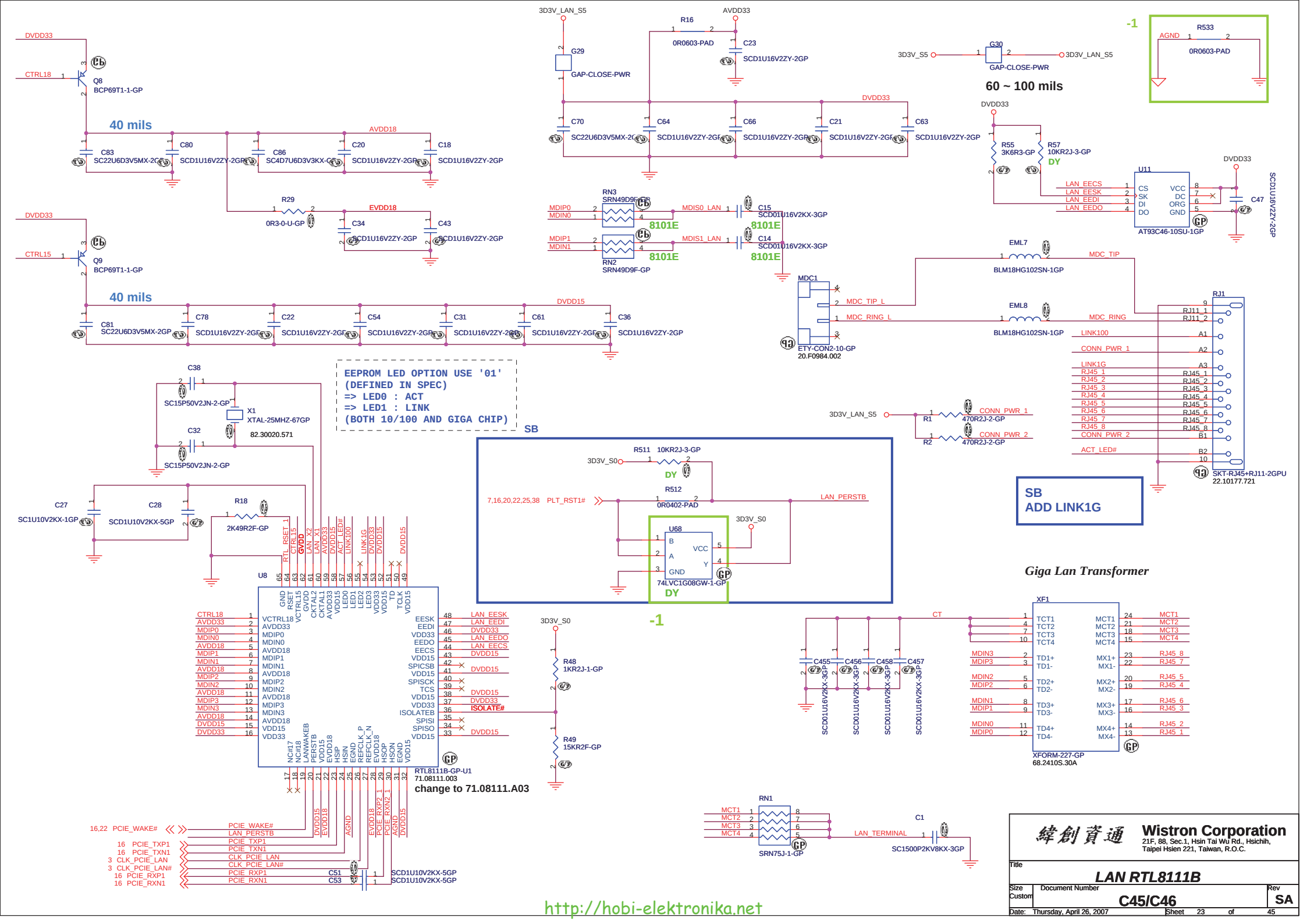
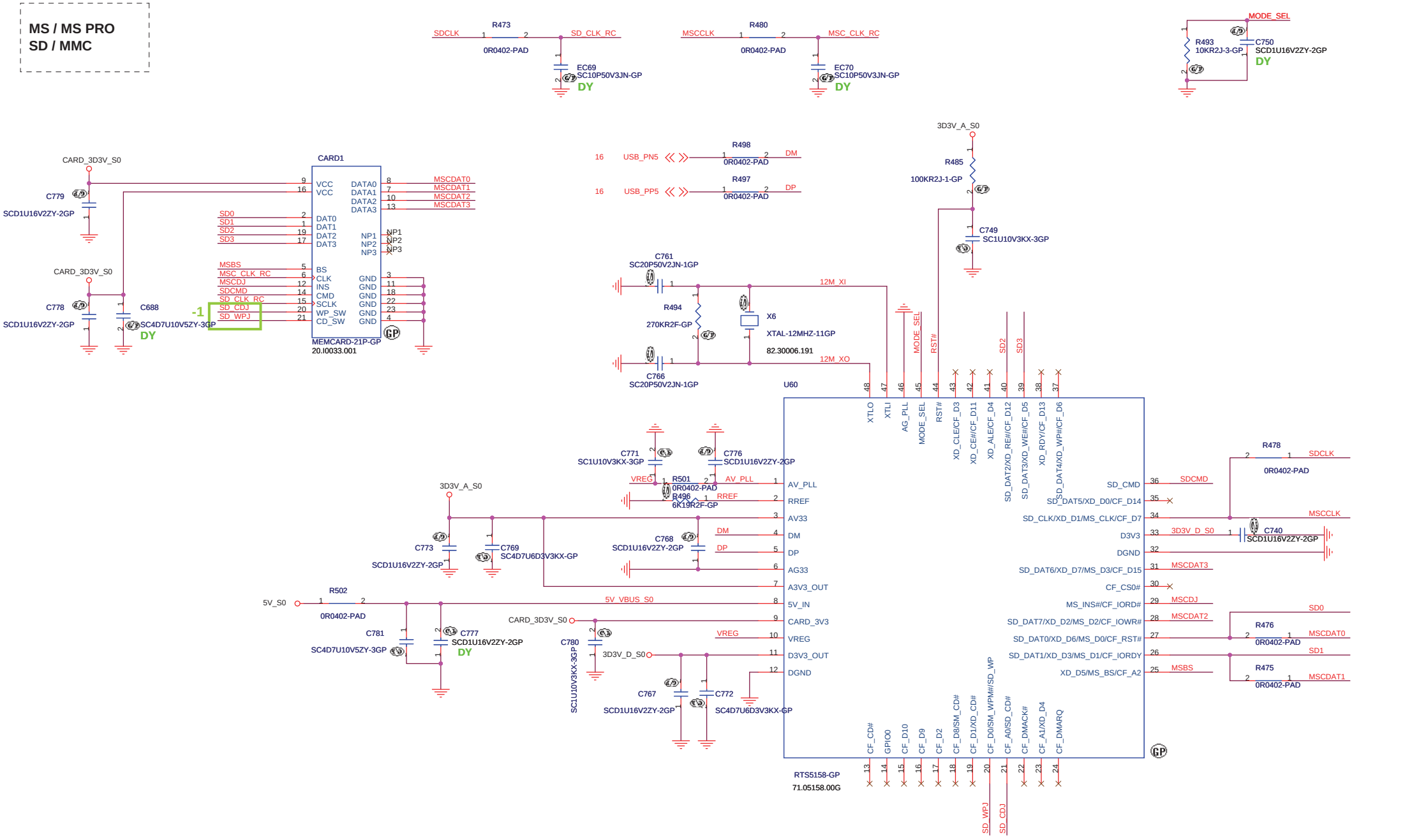

DVDD33
CTRL18
Q8
BCP69T1-1-GP
40 mils
C83
SC22U6D3V5MX-2GP
C80
SCD1U16V2ZY-2GP
C86
SC4D7U6D3V3KX-GP
AVDD18
C20
C18
R29
0R3-0-U-GP
EVDD18
C34
C43
CTRL15
Q9
C81
C78
C22
C54
C31
C61
DVDD15
C36
3D3V_LAN_S5
R16
0R0603-PAD
AVDD33
C23
G29
GAP-CLOSE-PWR
C70
C64
C66
C21
C63
3D3V_S5
G30
3D3V_LAN_S5
60 ~ 100 mils
-1
R533
AGND
R55
3K6R3-GP
R57
10KR2J-3-GP
DY
U11
LAN_EECS
LAN_EESK
LAN_EEDI
LAN_EEDO
AT93C46-10SU-1GP
C47
SCD1U16V2ZY-2GP
RN3
SRN49D9F-GP
MDIP0
MDIN0
MDIS0_LAN
C15
SCD01U16V2KX-3GP
8101E
MDIP1
MDIN1
MDIS1_LAN
C14
RN2
MDC1
MDC_TIP_L
MDC_RING_L
ETY-CON2-10-GP
20.F0984.002
EML7
BLM18HG102SN-1GP
MDC_TIP
EML8
MDC_RING
RJ1
LINK100
CONN_PWR_1
LINK1G
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
CONN_PWR_2
ACT_LED#
SKT-RJ45+RJ11-2GPU
22.10177.721
SB
ADD LINK1G
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
SB
C38
SC15P50V2JN-2-GP
X1
XTAL-25MHZ-67GP
82.30020.571
C32
C27
SC1U10V2KX-1GP
C28
SCD1U10V2KX-5GP
R18
2K49R2F-GP
R511
10KR2J-3-GP
3D3V_S0
R512
0R0402-PAD
7,16,20,22,25,38
PLT_RST1#
LAN_PERSTB
U68
74LVC1G08GW-1-GP
-1
Giga Lan Transformer
U8
CTRL18
AVDD33
MDIP0
MDIN0
AVDD18
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
DVDD15
DVDD33
LAN_EESK
LAN_EEDI
LAN_EEDO
LAN_EECS
ISOLATE#
RTL8111B-GP-U1
71.08111.003
change to 71.08111.A03
R48
1KR2J-1-GP
R49
15KR2F-GP
C455
C456
C458
C457
SCD01U16V2KX-3GP
CT
XF1
XFORM-227-GP
68.2410S.30A
16,22 PCIE_WAKE#
PCIE_WAKE#
LAN_PERSTB
16 PCIE_TXP1
16 PCIE_TXN1
PCIE_TXP1
PCIE_TXN1
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
CLK_PCIE_LAN
CLK_PCIE_LAN#
16 PCIE_RXP1
16 PCIE_RXN1
PCIE_RXP1
PCIE_RXN1
C51
C53
SCD1U10V2KX-5GP
RN1
SRN75J-1-GP
LAN_TERMINAL
C1
SC1500P2KV8KX-3GP
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN RTL8111B
Size
Custom
Document Number
C45/C46
Rev
SA
Date: Thursday, April 26, 2007
Sheet 23 of 45



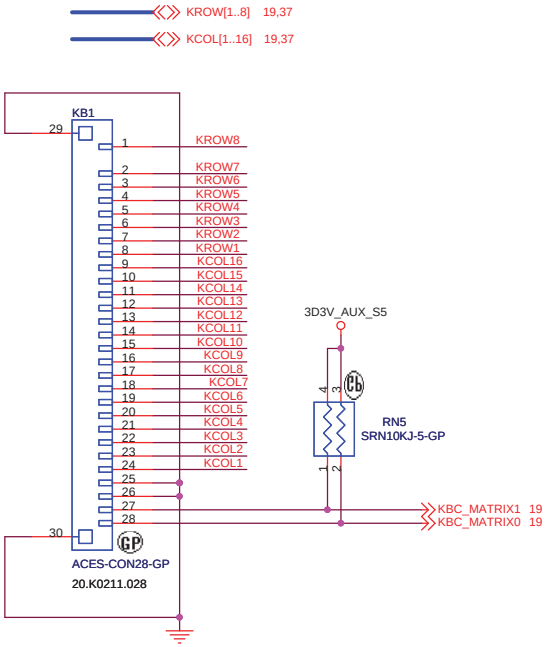
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB Card Reader Controller

Size	Document Number	Rev
Custom	C45/C46	SA

Date: Friday, April 27, 2007 Sheet 24 of 45

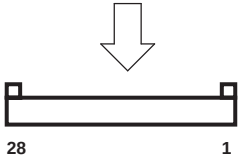
Internal KeyBoard Connector



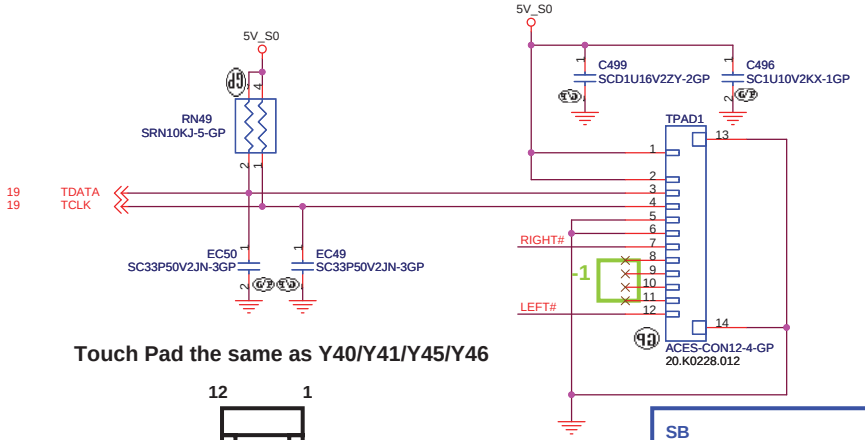
KEYBOARD MARTIX the same as Y40/Y41/Y45/Y46

Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



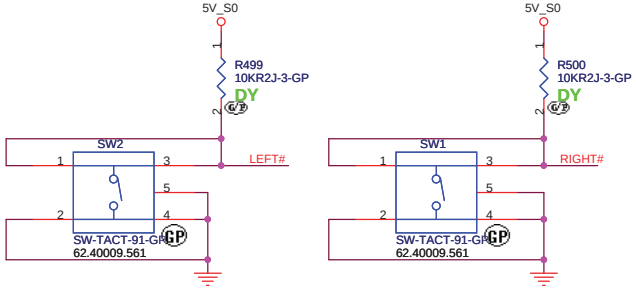
TouchPad Connector



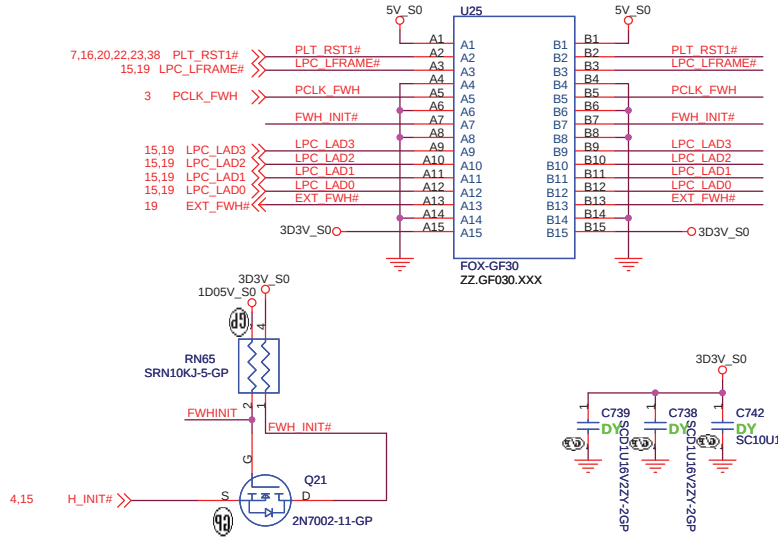
Touch Pad the same as Y40/Y41/Y45/Y46

SB
REVERSE TPAD1 PIN DEFINE

15" TOUCHPAD BUTTON SWITCH



GOLDEN FINGER FOR DEBUG BOARD

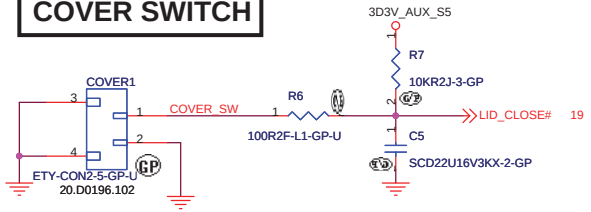


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

COVER SWITCH

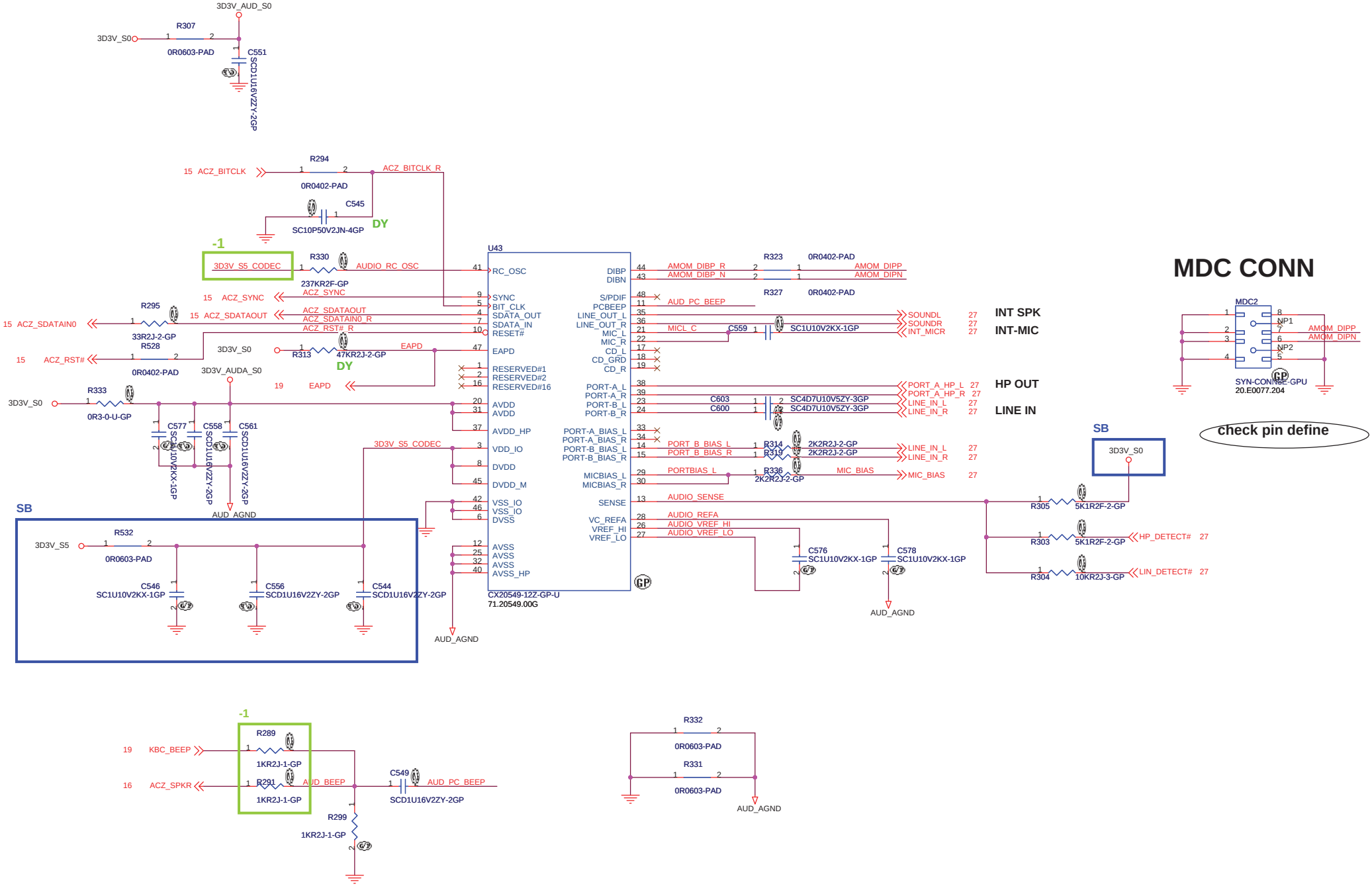


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KeyBoard/TPAD/Debug**

Size: Custom | Document Number: **C45/C46** | Rev: **SA**

Date: Thursday, April 26, 2007 | Sheet 25 of 45



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC CX20549-12Z/MDC

Size	Document Number	Rev
Custom	C45/C46	SA

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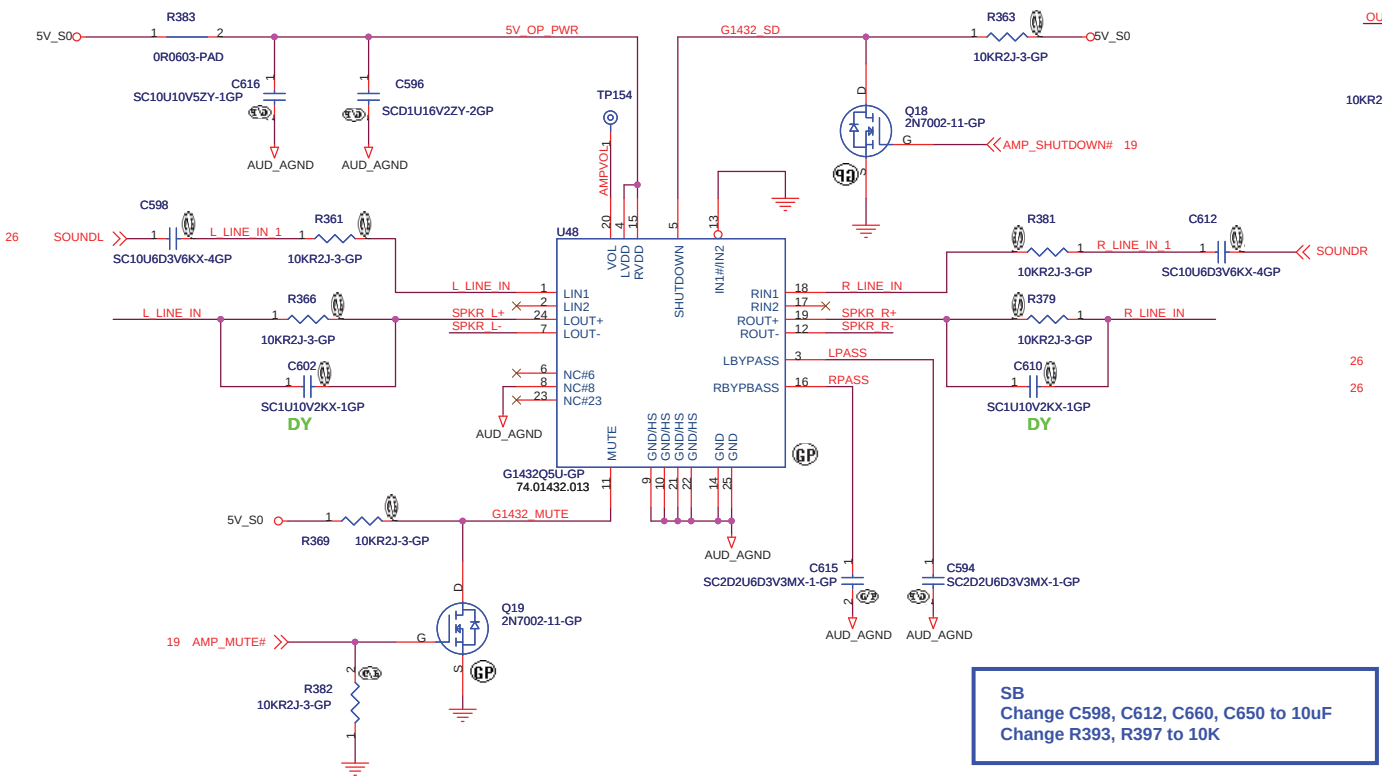
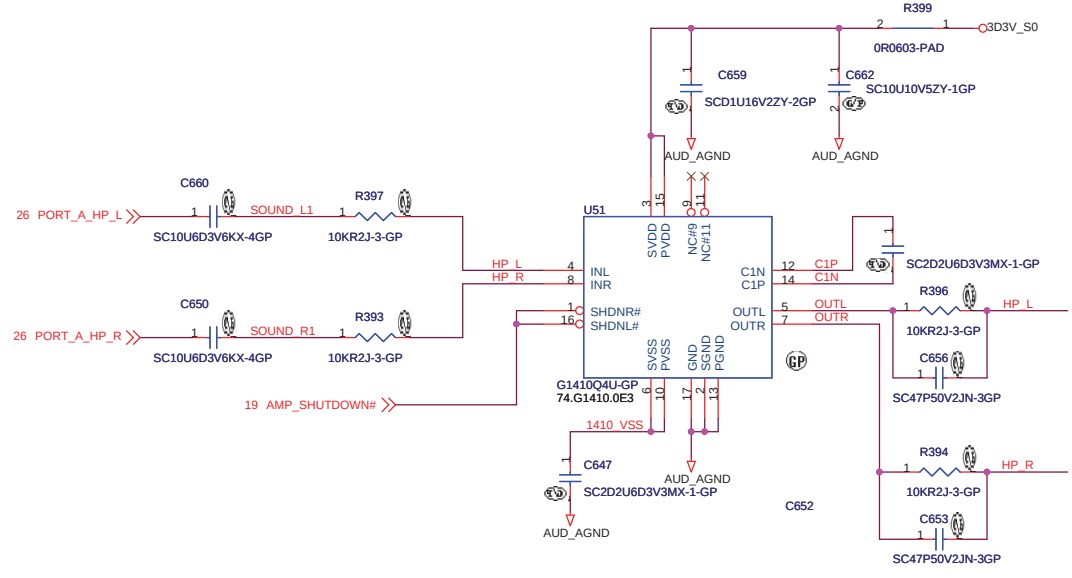
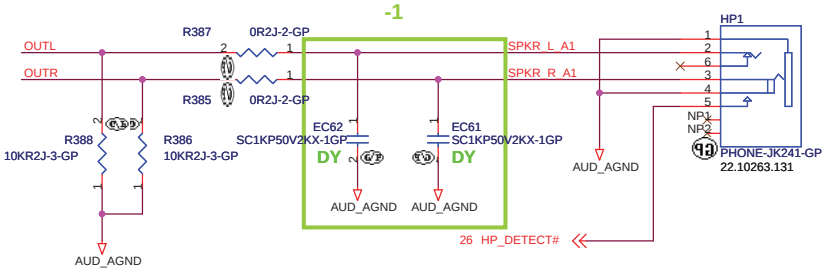
AUDIO AMPLIFIER



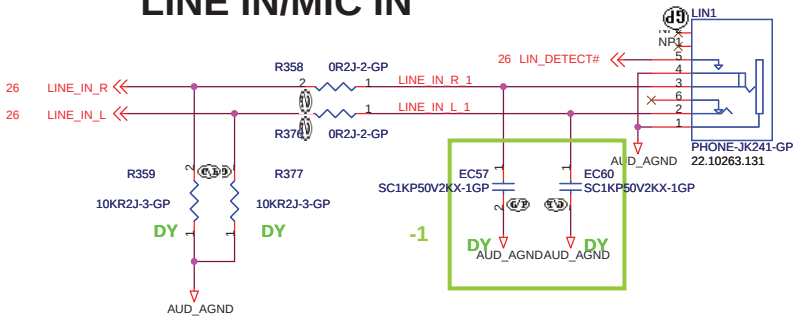
SB
Change C598, C612, C660, C650 to 10uF
Change R393, R397 to 10K



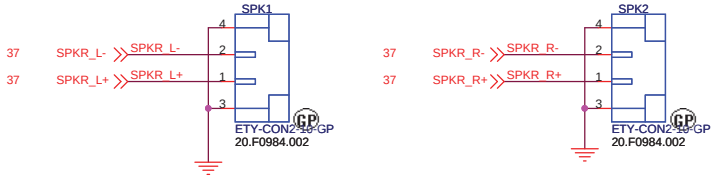
Headphone OUT



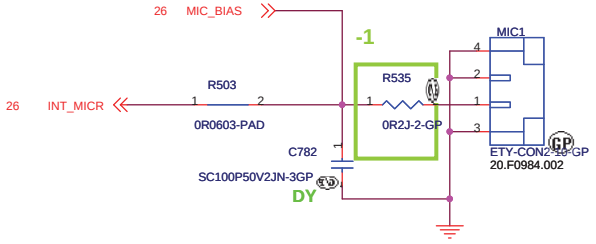
LINE IN/MIC IN



Internal Speaker



Internal MIC



緯創資通 **Wistron Corporation**
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Title: ***Audio_AMP(G1432)& JACK***

Size	Document Number	Rev
A3	C45/C46	SA

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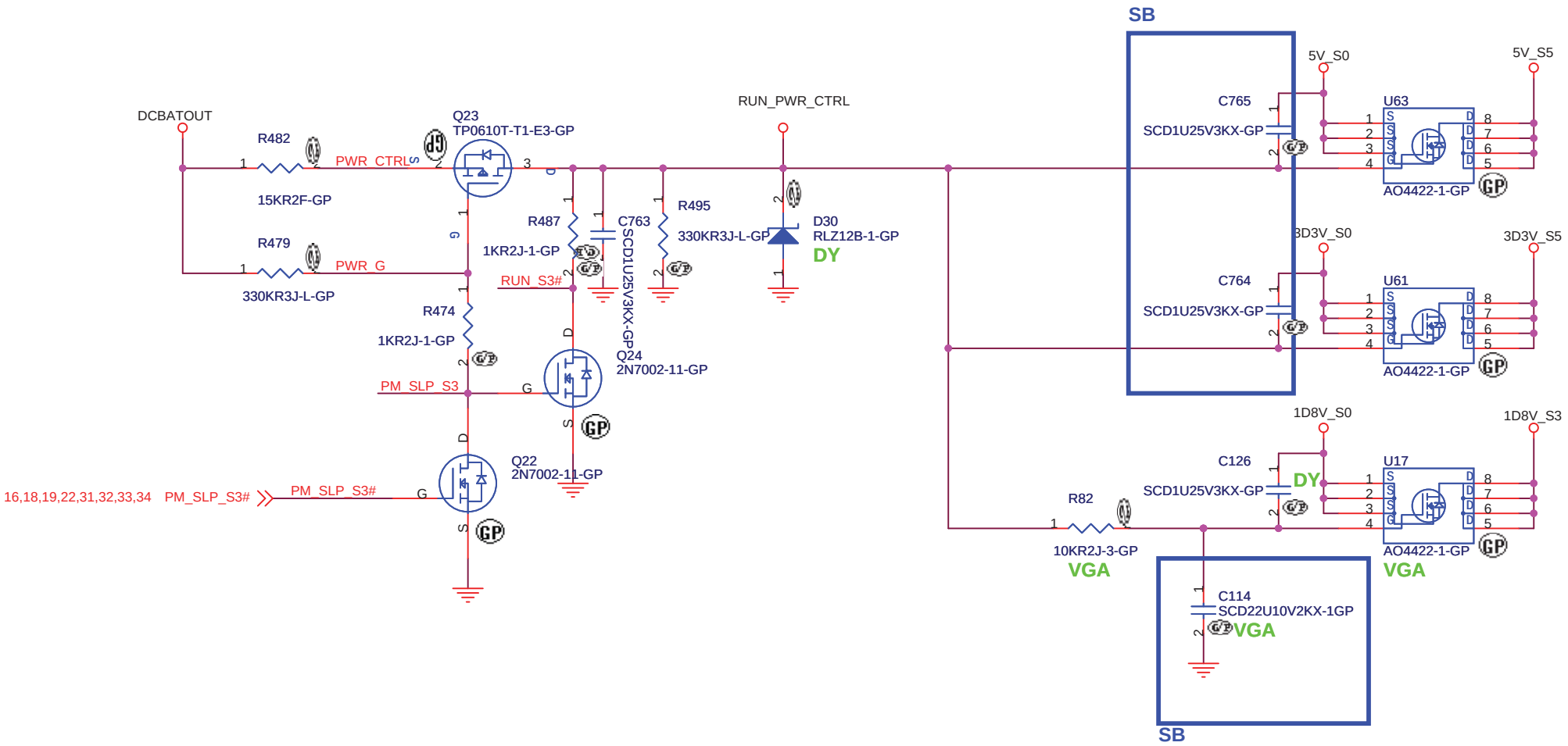
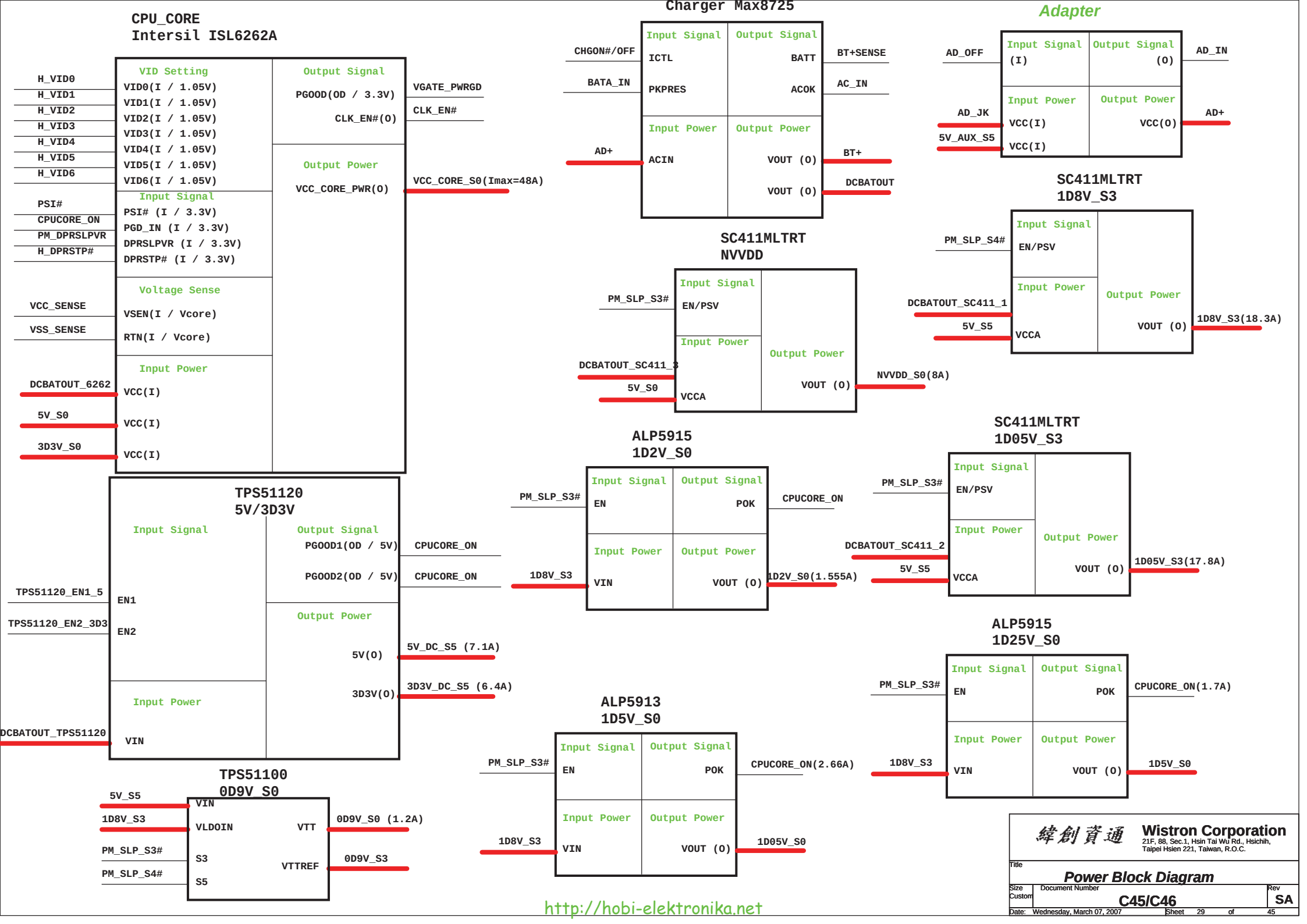
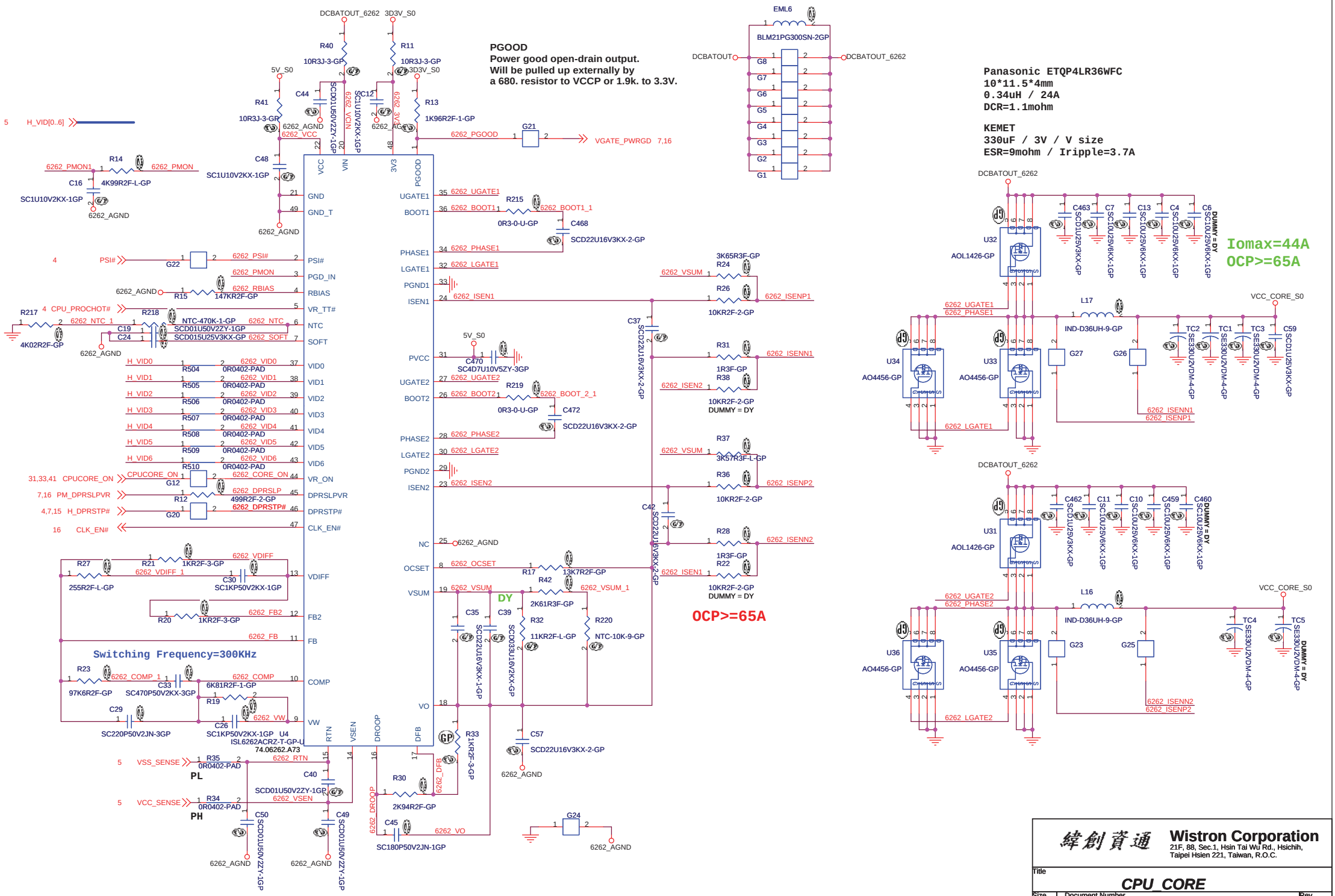
Run Power



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER / CTRL LOGIC***	
Size A4	Document Number C45/C46	Rev **SA**
Date: Wednesday, April 25, 2007	Sheet 28 of 45	


CPU_CORE
Intersil ISL6262A
VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)
Input Signal
PSI# (I / 3.3V)
PGD_IN (I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RTN(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD(OD / 3.3V)
CLK_EN#(O)
Output Power
VCC_CORE_PWR(O)
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#
VCC_SENSE
VSS_SENSE
DCBATOUT_6262
5V_S0
3D3V_S0
VGATE_PWRGD
CLK_EN#
VCC_CORE_S0(Imax=48A)
Charger Max8725
Input Signal
ICTL
PKPRES
Output Signal
BATT
ACOK
Input Power
ACIN
Output Power
VOUT (O)
VOUT (O)
CHGON#/OFF
BATA_IN
AD+
BT+SENSE
AC_IN
BT+
DCBATOUT
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
SC411MLTRT
1D8V_S3
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S4#
DCBATOUT_SC411_1
5V_S5
1D8V_S3(18.3A)
SC411MLTRT
NVVDD
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S3#
DCBATOUT_SC411_3
5V_S0
NVVDD_S0(8A)
TPS51120
5V/3D3V
Input Signal
EN1
EN2
Input Power
VIN
Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)
Output Power
5V(O)
3D3V(O)
TPS51120_EN1_5
TPS51120_EN2_3D3
DCBATOUT_TPS51120
CPUCORE_ON
CPUCORE_ON
5V_DC_S5 (7.1A)
3D3V_DC_S5 (6.4A)
ALP5915
1D2V_S0
Input Signal
EN
Input Power
VIN
Output Signal
POK
Output Power
VOUT (O)
PM_SLP_S3#
1D8V_S3
CPUCORE_ON
1D2V_S0(1.555A)
SC411MLTRT
1D05V_S3
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S3#
DCBATOUT_SC411_2
5V_S5
1D05V_S3(17.8A)
ALP5915
1D25V_S0
Input Signal
EN
Input Power
VIN
Output Signal
POK
Output Power
VOUT (O)
PM_SLP_S3#
1D8V_S3
CPUCORE_ON(1.7A)
1D5V_S0
ALP5913
1D5V_S0
Input Signal
EN
Input Power
VIN
Output Signal
POK
Output Power
VOUT (O)
PM_SLP_S3#
1D8V_S3
CPUCORE_ON(2.66A)
1D05V_S0
TPS51100
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S3#
PM_SLP_S4#
0D9V_S0 (1.2A)
0D9V_S3
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Block Diagram
Size
Custom
Document Number
C45/C46
Rev
SA
Date: Wednesday, March 07, 2007
Sheet 29 of 45


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
Panasonic ETQP4LR36WFC
10*11.5*4mm
0.34uH / 24A
DCR=1.1mohm
KEMET
330uF / 3V / V size
ESR=9mohm / Iripple=3.7A
Iomax=44A
OCP>=65A
OCP>=65A
Switching Frequency=300KHz
DCBATOUT_6262
3D3V_S0
5V_S0
EML6
BLM21PG300SN-2GP
DCBATOUT
DCBATOUT_6262
H_VID[0..6]
6262_PGOOD
VGATE_PWRGD 7,16
6262_PMON1
6262_PMON
6262_AGND
6262_VCC
VCC
VIN
3V3
PGOOD
GND
GND_T
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
NC
OCSET
VSUM
VO
PSI#
6262_PSI#
PSI#
6262_PMON
PGD_IN
6262_RBIAS
RBIAS
VR_TT#
CPU_PROCHOT#
6262_NTC_1
6262_NTC
NTC
6262_SOFT
SOFT
H_VID0
6262_VID0
VID0
H_VID1
6262_VID1
VID1
H_VID2
6262_VID2
VID2
H_VID3
6262_VID3
VID3
H_VID4
6262_VID4
VID4
H_VID5
6262_VID5
VID5
H_VID6
6262_VID6
VID6
CPUCORE_ON
6262_CORE_ON
VR_ON
PM_DPRSLPVR
6262_DPRSLP
DPRSLPVR
H_DPRSTP#
6262_DPRSTP#
DPRSTP#
CLK_EN#
6262_VDIFF
VDIFF
6262_FB2
FB2
6262_FB
FB
6262_COMP_1
6262_COMP
COMP
6262_VW
VW
RTN
VSEN
DROOP
DFB
ISL6262ACRZ-T-GP-U
74.06262.A73
VSS_SENSE
6262_RTN
PL
VCC_SENSE
6262_VSEN
PH
6262_VSUM
6262_ISEN1
6262_ISENP1
6262_ISENN1
6262_ISEN2
6262_ISENP2
6262_ISENN2
6262_VSUM_1
DY
6262_UGATE1
6262_PHASE1
6262_LGATE1
6262_UGATE2
6262_PHASE2
6262_LGATE2
U32
U33
U34
U35
U36
AOL1426-GP
AO4456-GP
IND-D36UH-9-GP
VCC_CORE_S0
6262_ISENN1
6262_ISENP1
6262_ISENN2
6262_ISENP2
http://hobi-elektronika.net
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Title
CPU_CORE
Size
Custom
Document Number
C45/C46
Rev
SA
Date: Wednesday, April 25, 2007
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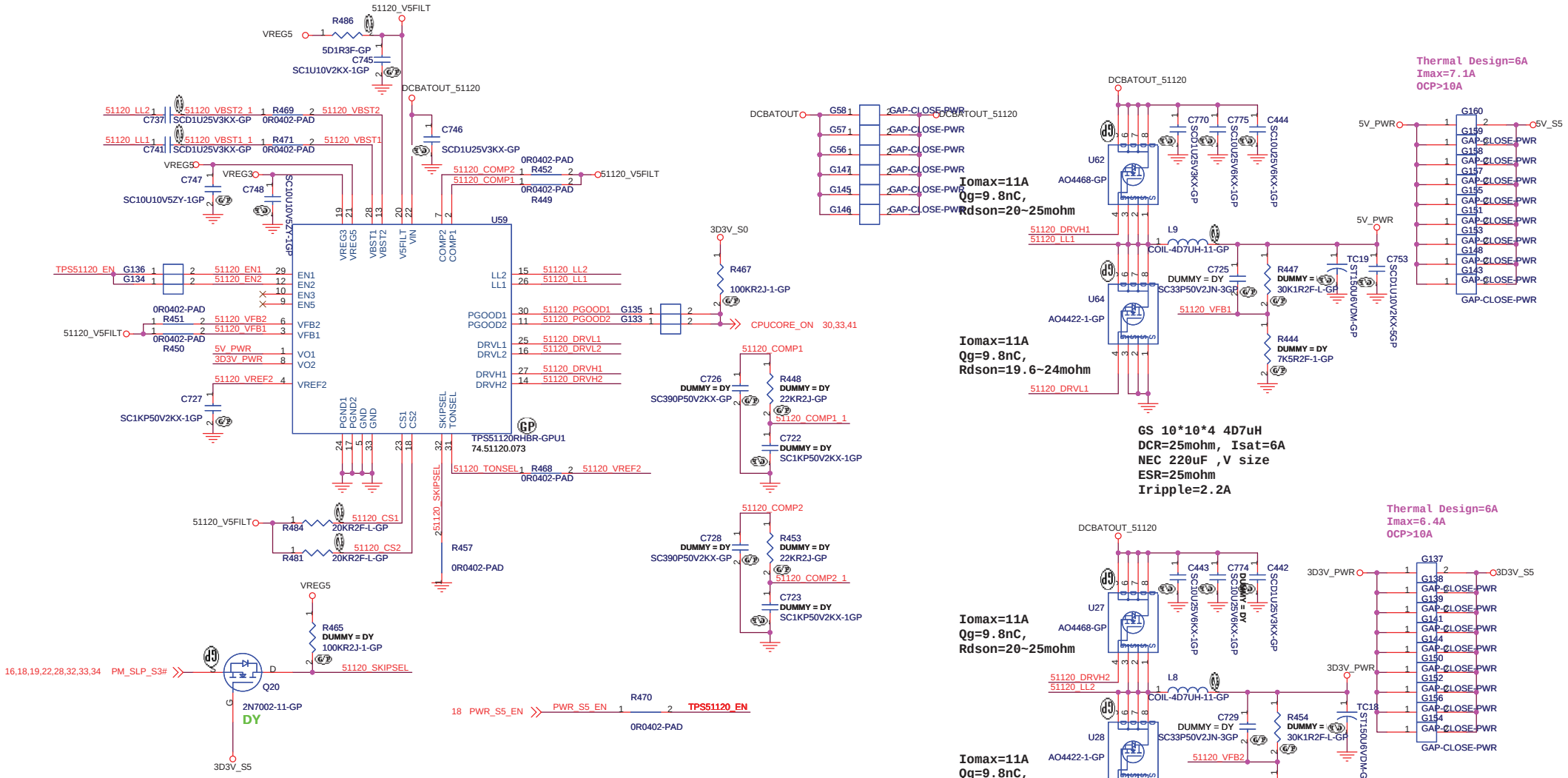

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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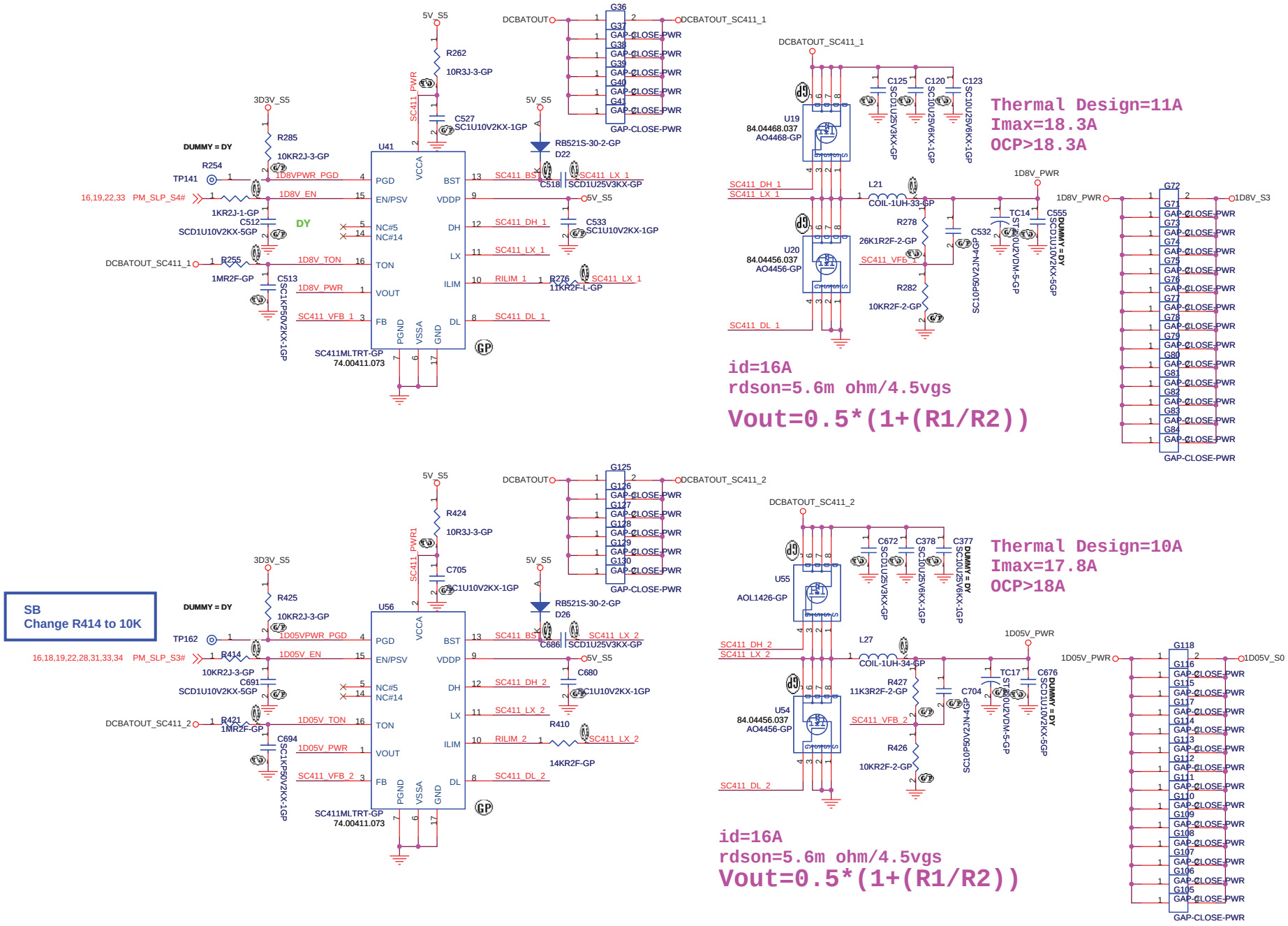
Title: ***TPS51120_3D3V_5V***

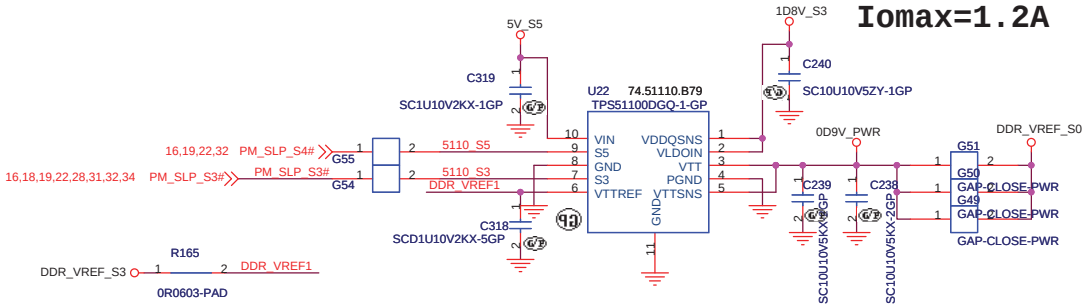
Size: Custom | Document Number: **C45/C46** | Rev: **SA**

Date: Wednesday, April 25, 2007 | Sheet 31 of 45



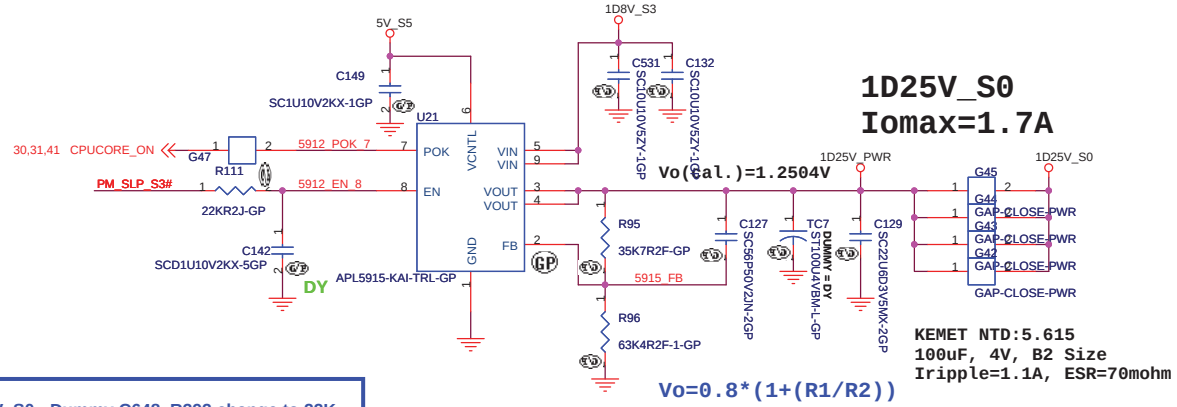
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SC411_1D05V/1D8V	
Size: Custom	Document Number: C45/C46	Rev: SA
Date: Wednesday, April 25, 2007	Sheet 32 of 45	

0D9V
Iomax=1.2A



Place near the Test point DDRVREF

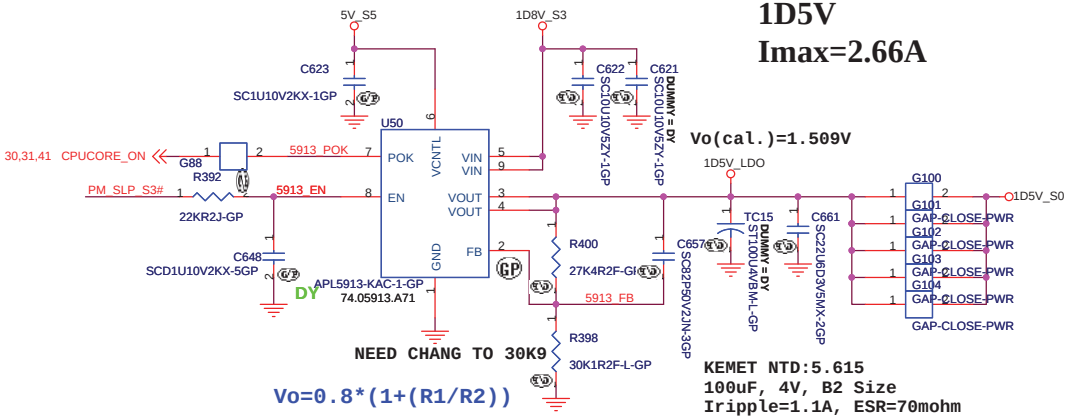
1D25V_S0
Iomax=1.7A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

SB
1D5V_S0 : Dummy C648, R392 change to 22K
1D25V_S0 : Dummy C142, R111 change to 22K

1D5V
Imax=2.66A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D5V/0D9V/1D05V
Size: A3
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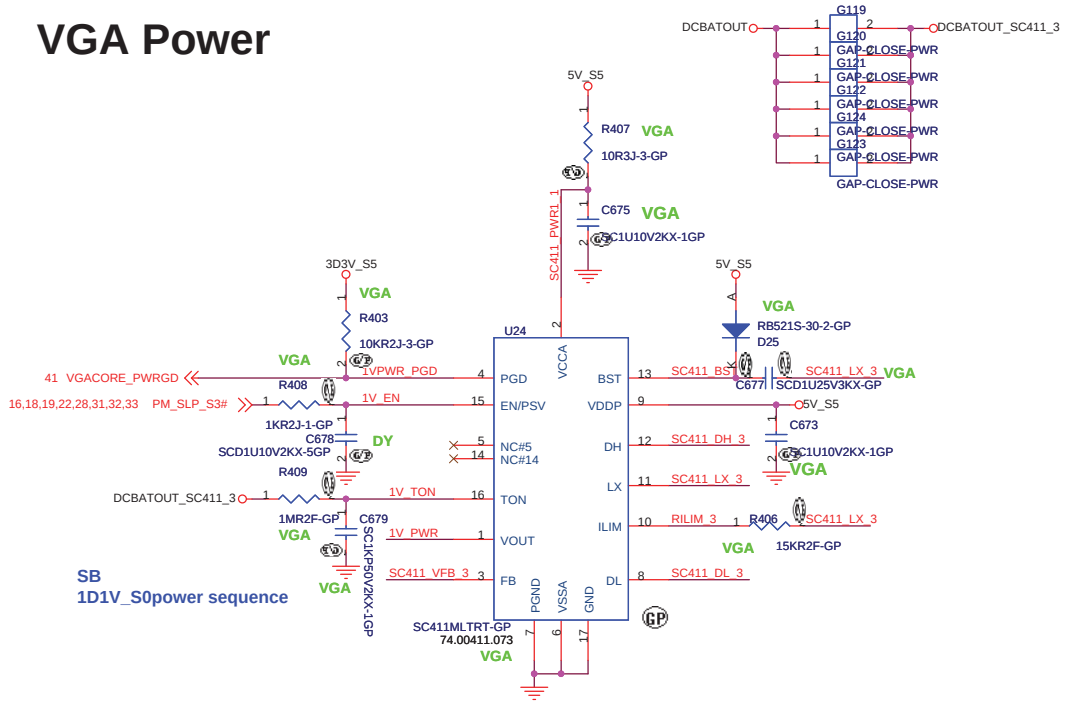
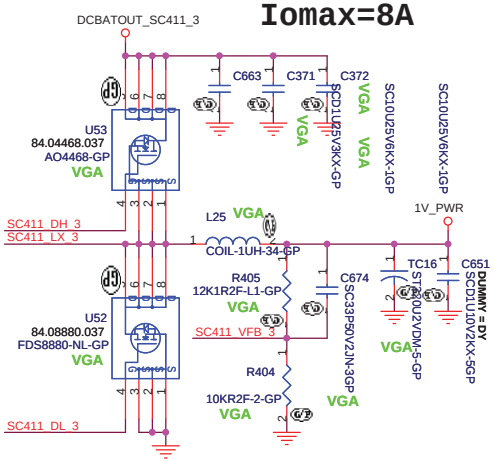
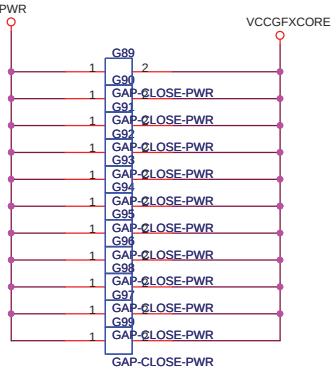
VGA Power



Thermal Design=8A
Imax=8A
OCP>14A

1V_S0
Iomax=8A



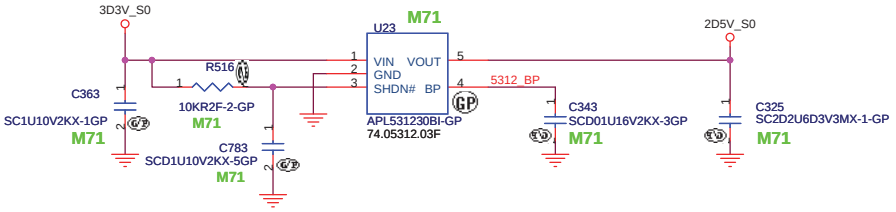


id=11.6A
rdson=12m ohm/4.5vgs

Vout=0.5*(1+(R1/R2))

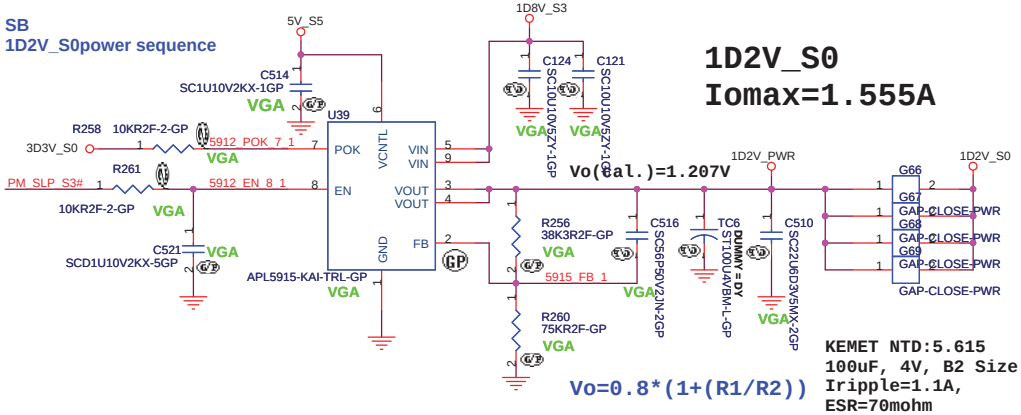
R405
FOR M71 ---> 1.2V 14K (64.14025.6DL)
FOR M72 ---> 1.1V 12.1K (64.12125.6DL)

2D5V
Iomax=300mA



SB
1D2V_S0power sequence

1D2V_S0
Iomax=1.555A



Vo=0.8*(1+(R1/R2))

KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A,
ESR=70mohm

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA POWER**

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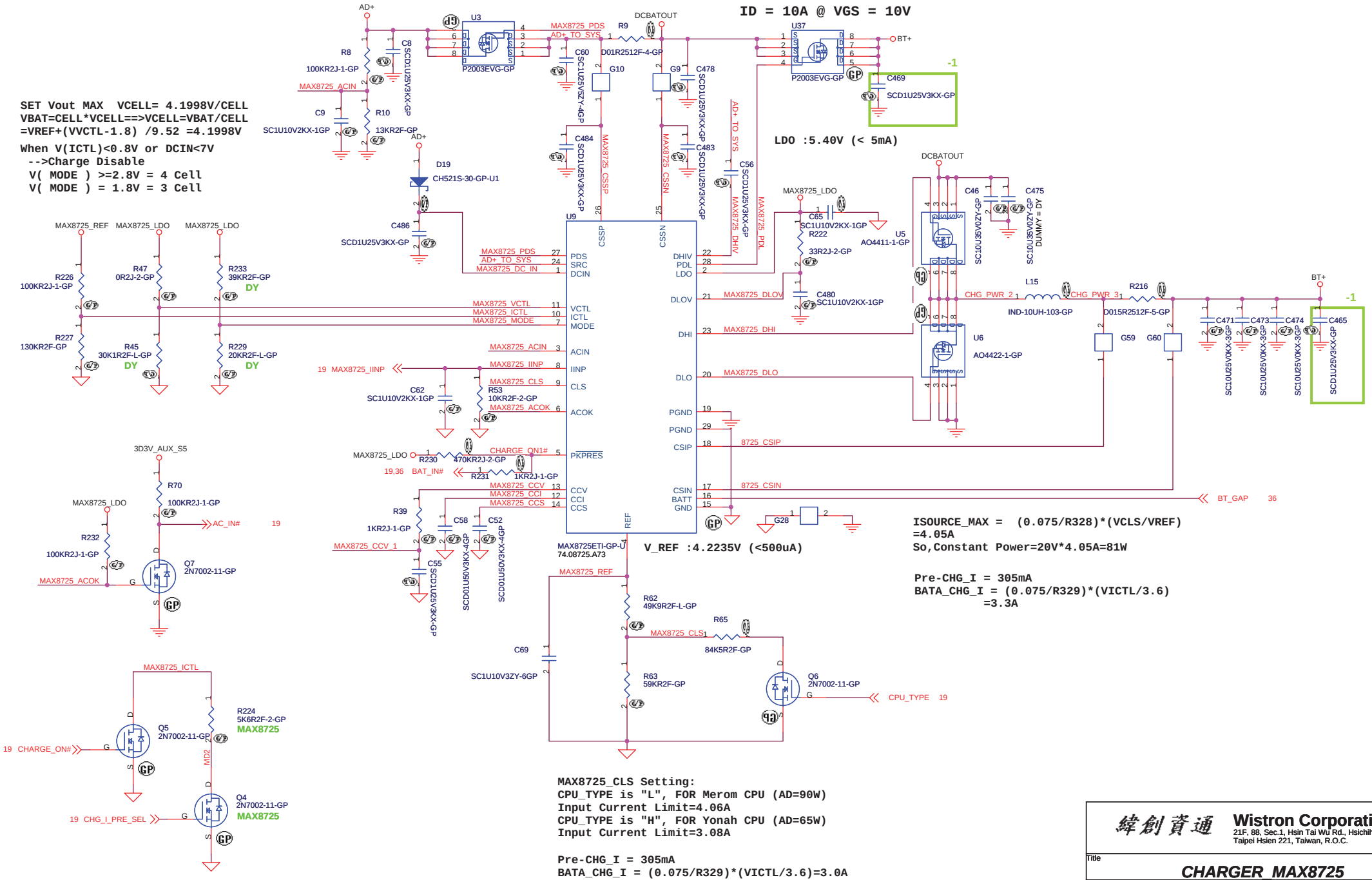

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER_MAX8725
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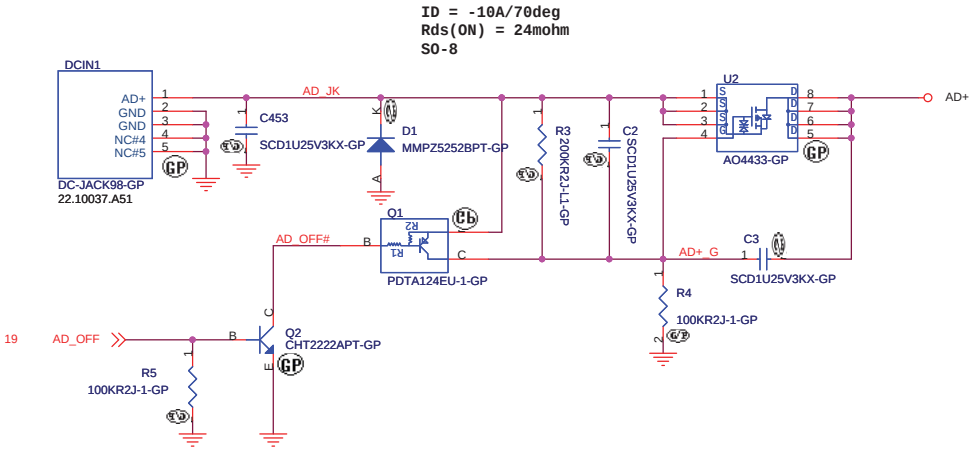
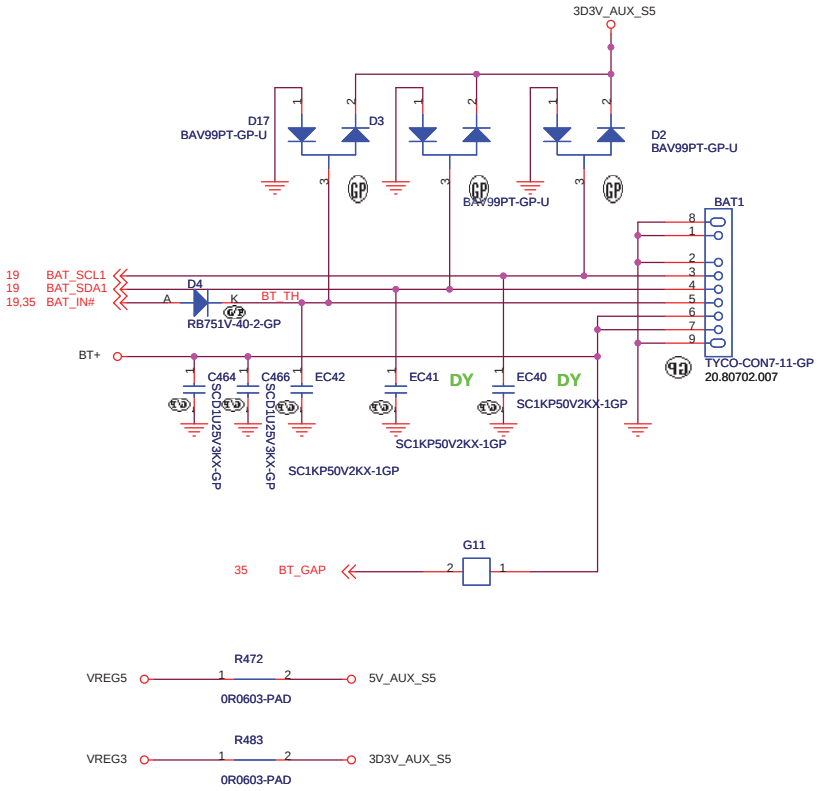
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AD_IN/BAT Conn*	
Size: Custom	Document Number: C45/C46	Rev: SA
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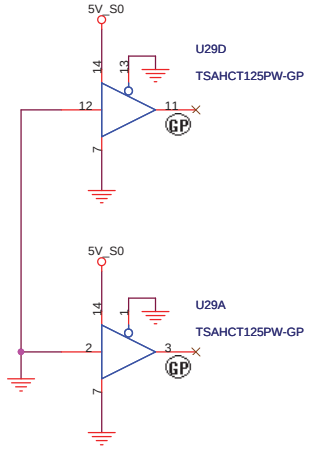
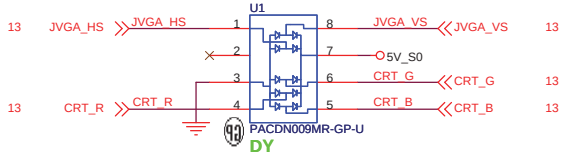
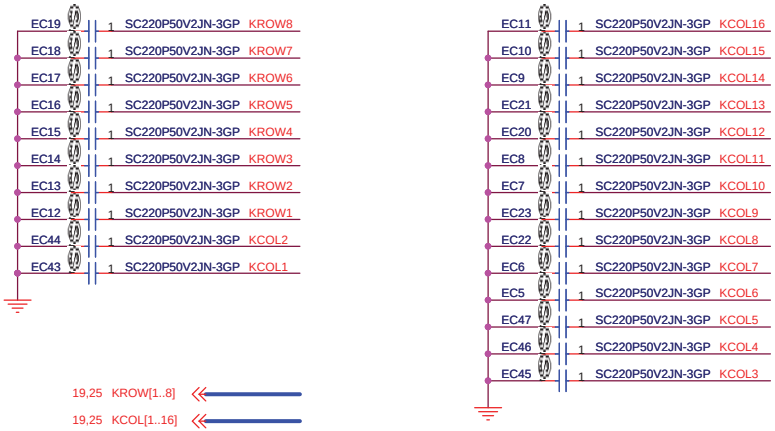
UNUSE Parts



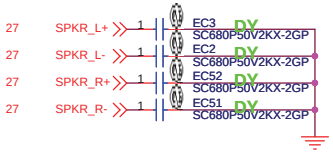
ESD Parts

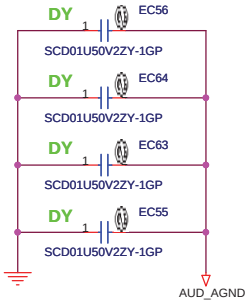


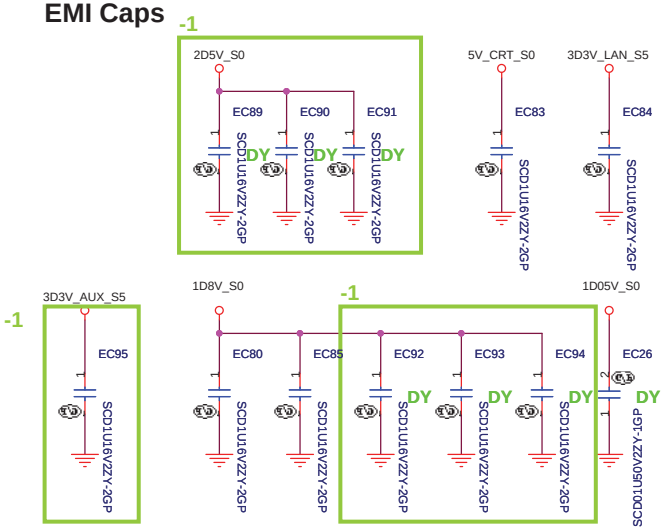
Keyboard EMI Caps

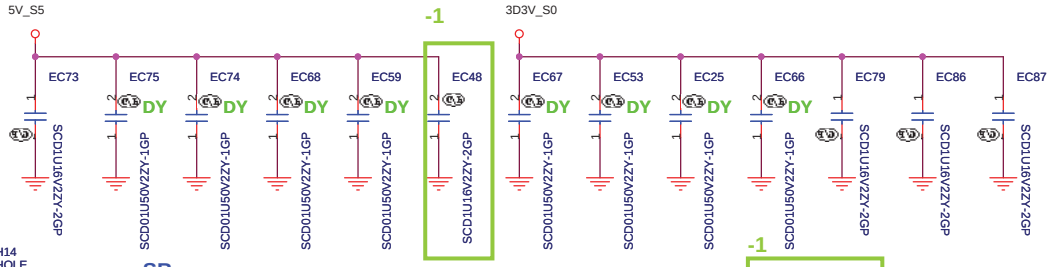


EMI Caps

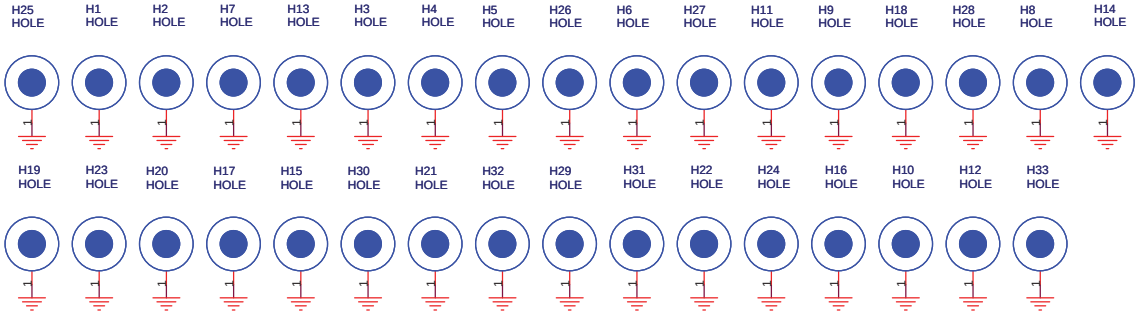


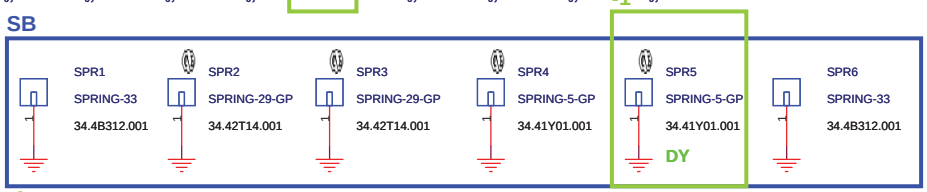


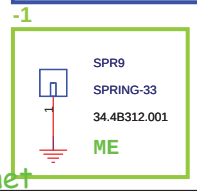




Holes







緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

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Custom	C45/C46	SA

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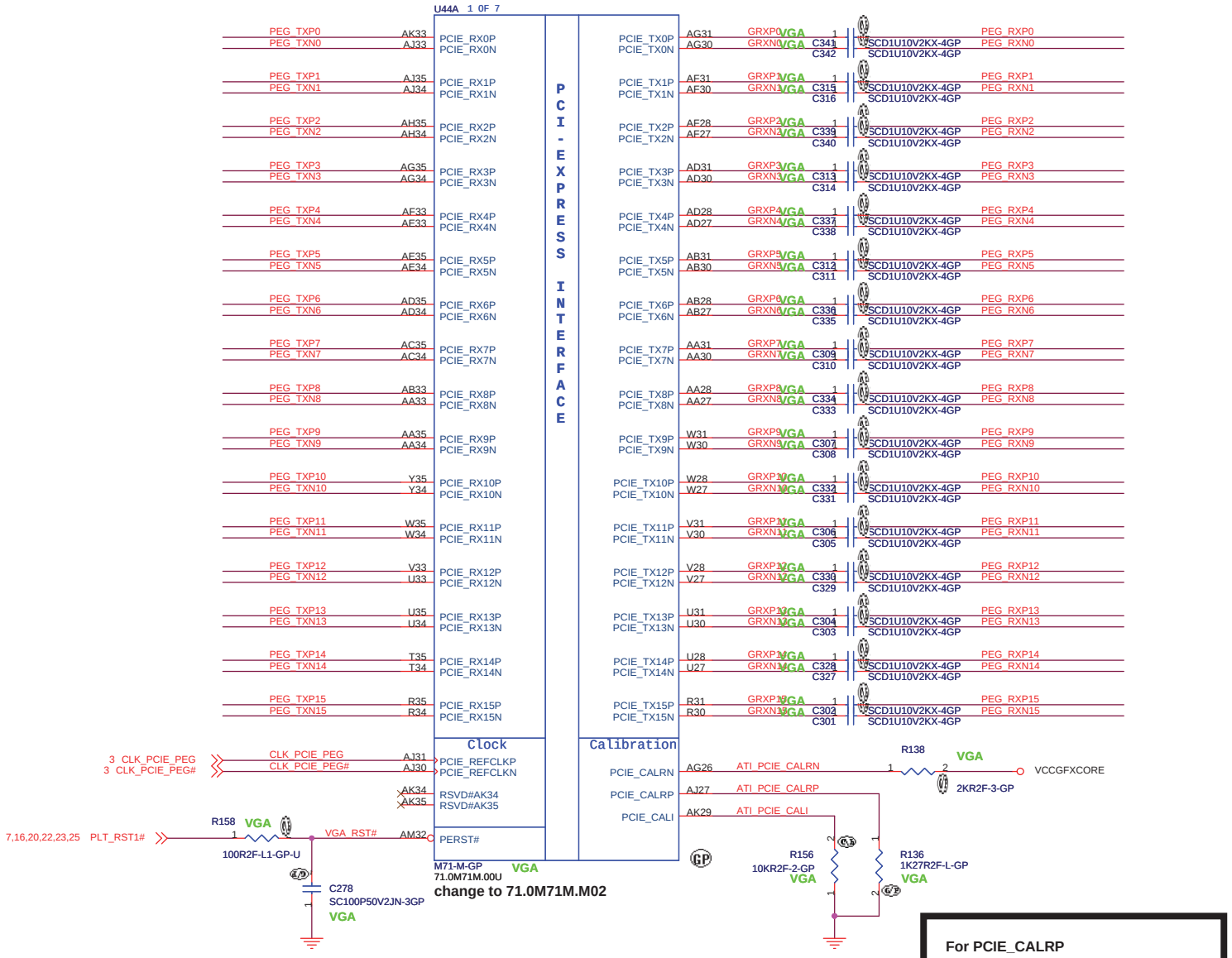

For PCIE_CALRP
1.27K to PCIE_VSS for M72M,M76M
562R to PCIE_VSS for M66M,M71M

For PCIE_CALI
10K to PCIE_VSS for M72M,M76M
1.47K to PCIE_VSS for M66M,M71M

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Title: VGA-M71/M72-M(1/5) PCIE

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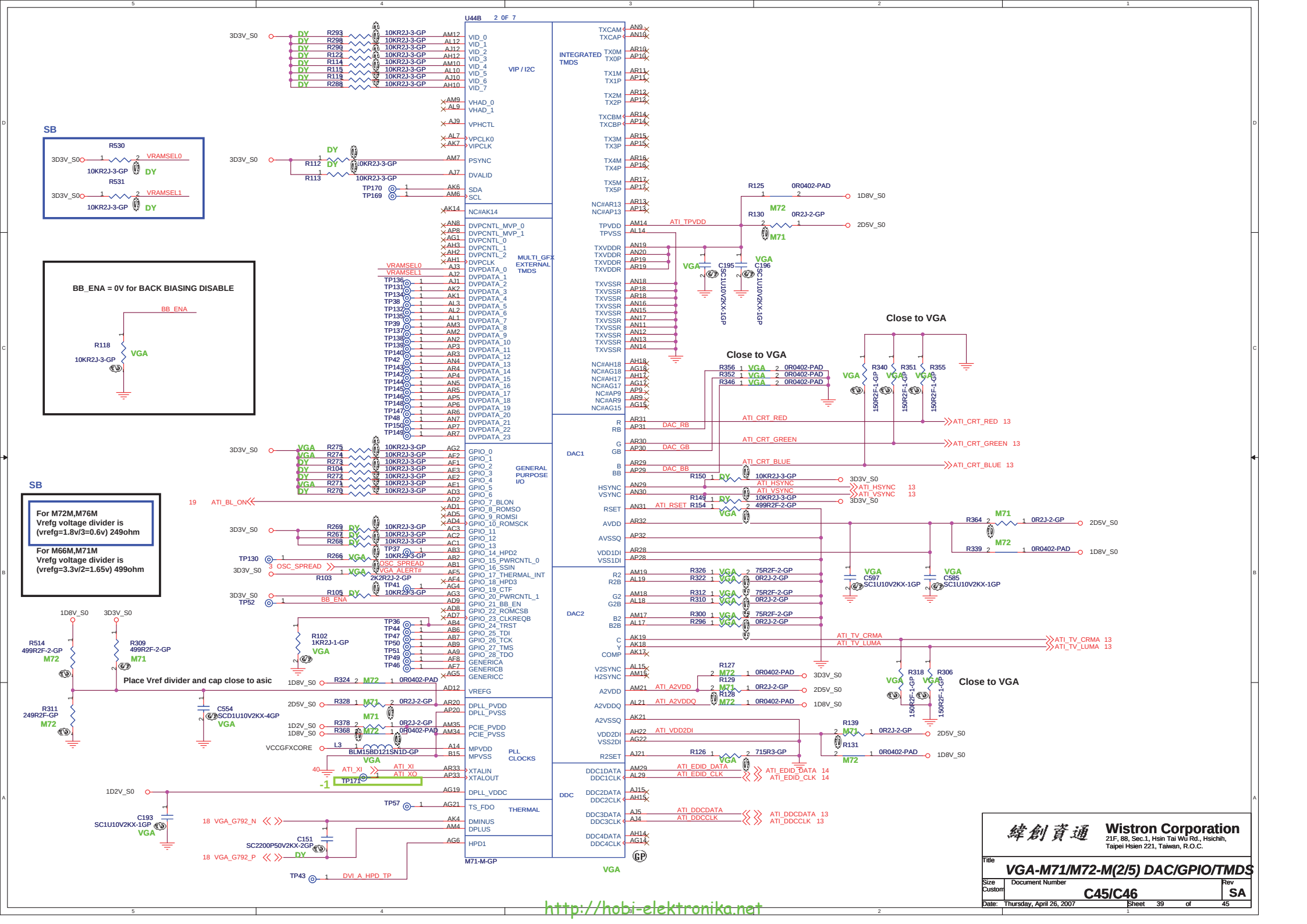
U44B 2 OF 7
VIP / I2C
INTEGRATED TMDS
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
PLL CLOCKS
THERMAL
DAC1
DAC2
DDC
M71-M-GP
VGA
SB
R530
VRAMSEL0
R531
VRAMSEL1
10KR2J-3-GP
DY
BB_ENA = 0V for BACK BIASING DISABLE
BB_ENA
R118
VGA
SB
For M72M,M76M
Vrefg voltage divider is
(vrefg=1.8v/3=0.6v) 249ohm
For M66M,M71M
Vrefg voltage divider is
(vrefg=3.3v/2=1.65v) 499ohm
Place Vref divider and cap close to asic
Close to VGA
Close to VGA
Close to VGA
ATI_CRT_RED
ATI_CRT_GREEN
ATI_CRT_BLUE
ATI_HSYNC
ATI_VSYNC
ATI_TV_CRMA
ATI_TV_LUMA
ATI_EDID_DATA
ATI_EDID_CLK
ATI_DDCDATA
ATI_DDCCLK
ATI_TPVDD
ATI_A2VDD
ATI_A2VDDQ
ATI_VDD2DI
DAC_RB
DAC_GB
DAC_BB
ATI_RSET
ATI_XI
ATI_XO
DVI_A_HPD_TP
VGA_G792_N
VGA_G792_P
ATI_BL_ON
OSC_SPREAD
VGA_ALERT#
VCCGFXCORE
1D8V_S0
2D5V_S0
3D3V_S0
1D2V_S0
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-M71/M72-M(2/5) DAC/GPIO/TMDS
Size Custom
Document Number
C45/C46
Rev SA
Date: Thursday, April 26, 2007
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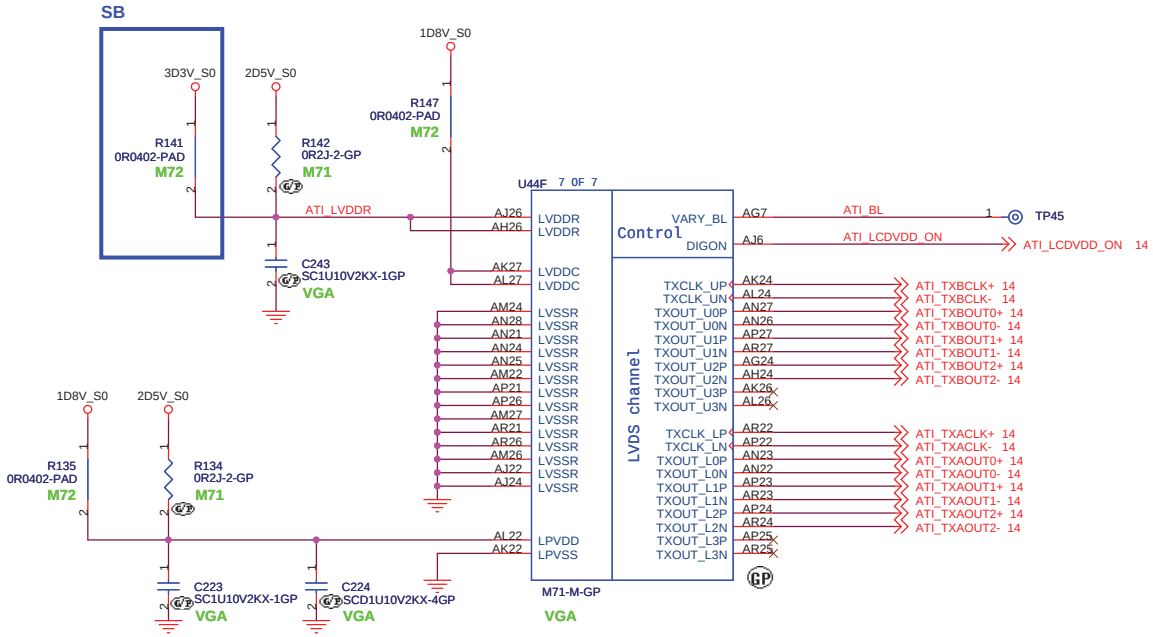
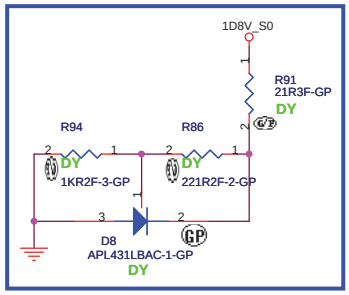
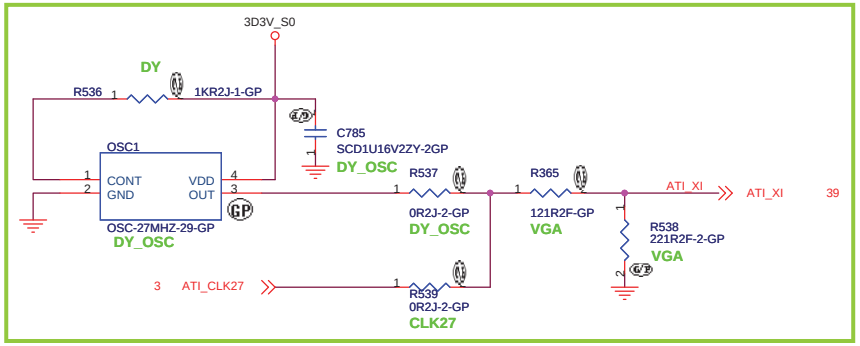
http://hobi-elektronika.net







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Title	***VGA-M71/M72-M(3/5)LVDS***	
Size A3	Document Number **C45/C46**	Rev **SA**
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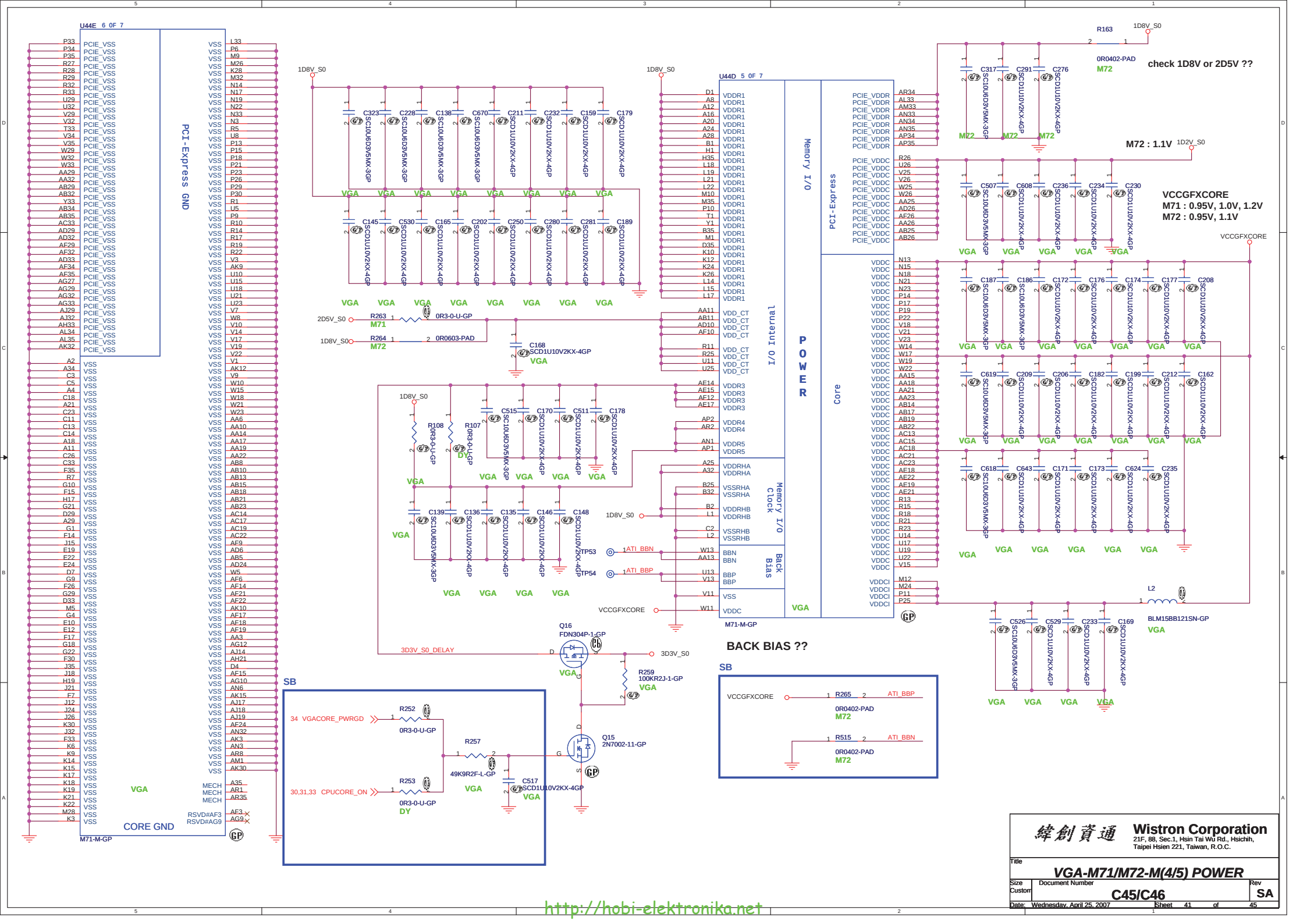

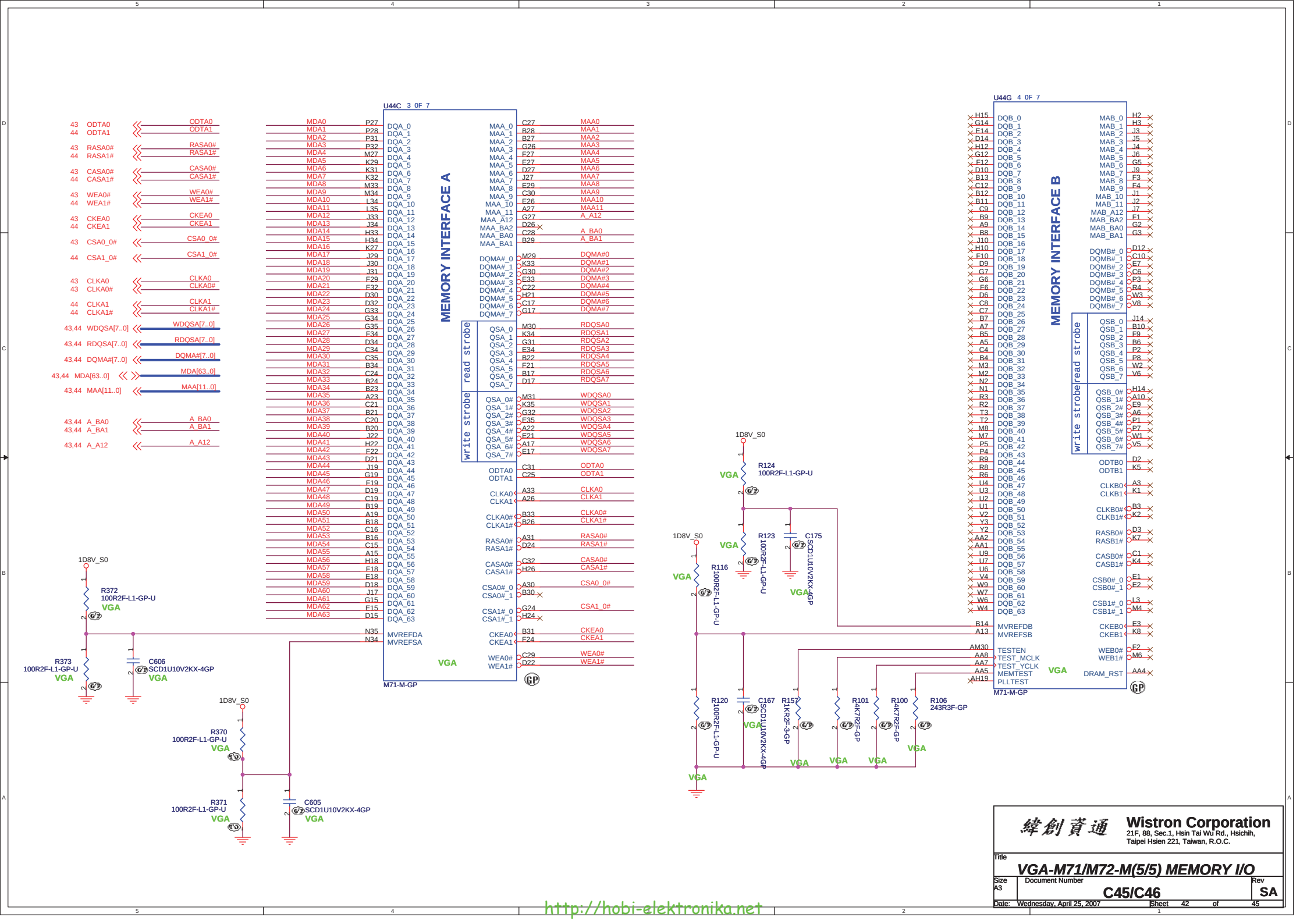

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Title	VGA-M71/M72-M(5/5) MEMORY I/O
Size A3	Document Number C45/C46
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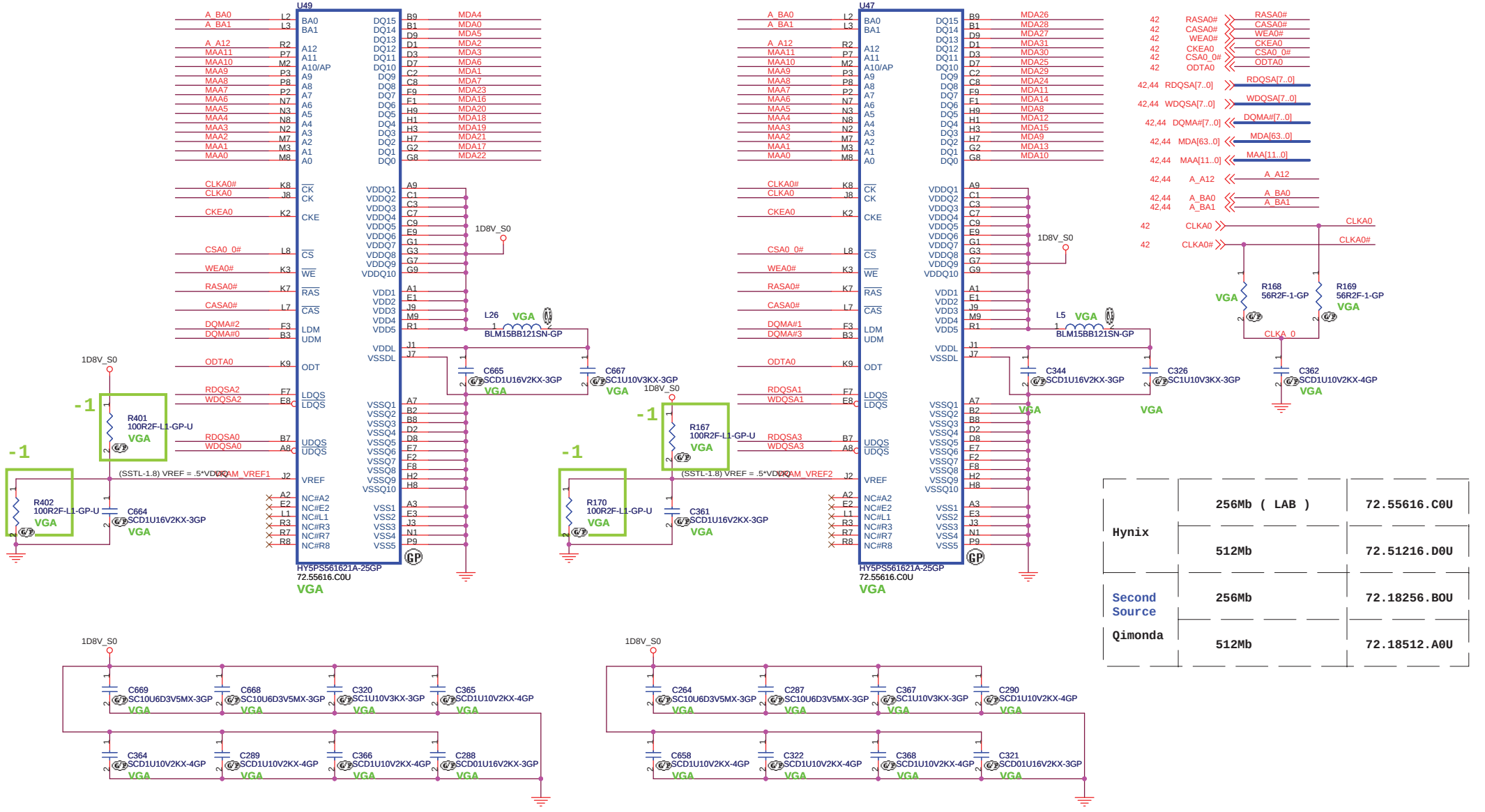
DDR2 BGA MEMORY (16M x 16)



Hynix	256Mb (LAB)	72.55616.C0U
	512Mb	72.51216.D0U
Second Source Qimonda	256Mb	72.18256.B0U
	512Mb	72.18512.A0U

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Title: VGA-VRAM(1/2)

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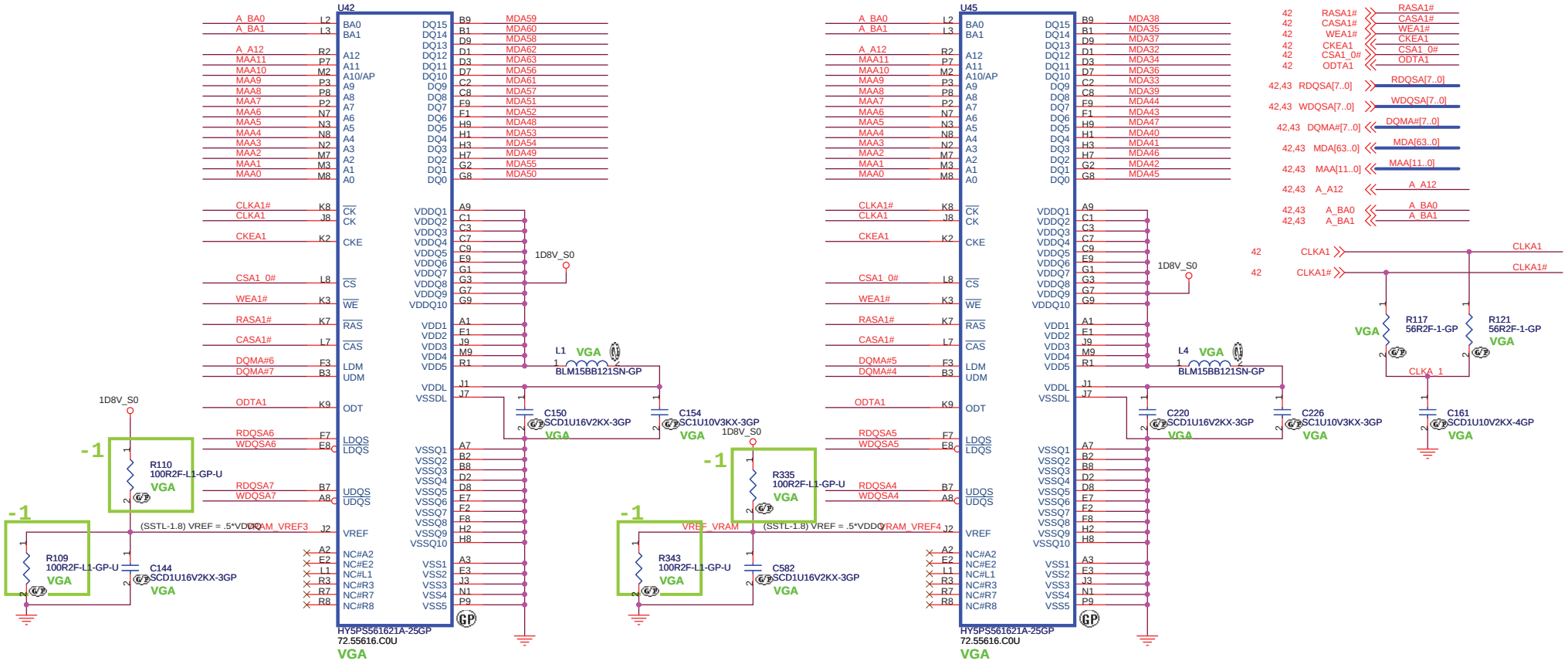
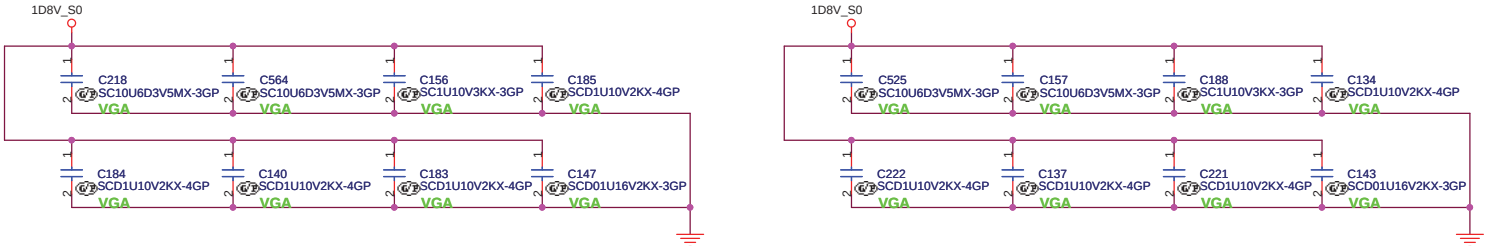
DDR2 BGA MEMORY (16M x 16)



Second Source: Qimonda 72.18256.B0U



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Title: ***VGA-VRAM(2/2)***

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History

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2006/11/17
1. Schematic drawing start..
2006/12/12
1. Change to project name to C45/C46
2007/01/08
1. LAB gerber out

BOM Change (LAB)

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2006/12/29
1. VGA Change to M72, VRAM 128MB, but verify M71 (71.0M71M.M02) and M72(71.0M72M.M01) in LAB
2. 965GM (71.GM965.00U)
3. 965PM (71.PM965.00U)
4. RTS5158 (71.08111.A03)
5. ME stand off 34.4G901.001 (H23, H25, H9, H11) for MINI Card
6. ME stand off 34.4B601.001 (H26, H27) for MODEM
7. ME stand off 87.00055.120 (H4) for LVDS
8. ICH8-M (71.ICH8M.A0U)

LAB Chipset Part Number

C45:

NB: 71.CREST.M03
SB: 71.0ICH8.M08

C46:

NB: 71.CREST.A0U
SB: 71.0ICH8.M08

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Title: HISTORY

Size: A3 | Document Number: C45/C46 | Rev: SA

Date: Wednesday, March 07, 2007 | Sheet 45 of 45