

First International Computer, Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : AMD S1 + Nvidia C51D + MCP51

Version : 0.4


Initial Date : 05/13/2006

Confidential

Manager Sign by : Avery Lee

Drawing by : Jason Lee

Total confirm by : Adam Cho

		First International Computer, Inc. SFL NO.300, Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C (886-2)8751-8751	
		Confidential	
Title PA1538/XA1526(FSC) PTB50/XTB70(FIC)			
Size C	Document Number TITLE		Rev 0.4
Date: Thursday, October 26, 2006 Sheet 1 of 57			

1. Schematic Page Description :

FIC Schematic Ver : 0.1

1. Title

2. Schematic Page Description

3. Block Diagram

4. ANNOTATIONS

5. Schematic History

6. AMD S1 HT(1/3)

7. AMD S1 DDR(2/3)

8. AMD S1 POWER(3/3)

9. CPU Thermal/Fan CNN

10. C51D_HT (1/3)

11. C51D_PCIE (2/3)

12. C51D_POWER(3/3)

13. DDRII SO-DIMM 0 RSV

14. DDRII SO-DIMM 1 STD

15. MCP51 HT(1/6)

16. MCP51 PCI(E)/LPC (2/6)

17. MCP51 SATA/PATA(3/6)

18. MCP51 AC97/USB(4/6)

19. MCP51 RGMII(5/6)

20. MCP51 POWER(6/6)
21. G7X PCI-EXPRESS

22. G7X VIDEO_1

23. G7X VIDEO_2

24. G7X MEM CHANNEL

25. VGA DDR2_A CHANNEL

26. VGA DDR2_C CHANNEL

27. DVI Port

28. LCD CNN

29. TV Port

30. 1394 VIA VT6311S

31. Cardreader AU6366

32. New Card(express card)

33. PCIE Mini Card

34. GIGA PHY 88E1116

35. GIGA TRANSFORMER

36. FirmWare Hub

37. USB CNN

38. LED / SW

39. RTC/ BLUETOOTH CNN

40. SATA HD / CD-ROM CNN
41. Azalia ALC883GR- Codec

42. AMP (G1432&G1410)/AD CN

43. SPDIF HP/MIC JACK

44. MDC / Audio CNN

45. Reset Circuit

46. KBC / GP CNN

47. DIP/LID SW; SCREW

48. PMU08A

49. Power Block Diagram

50. CPU CORE (MAX8774)

51. ACIN / DCIN

52. Battery CNN

53. Charger MB3887

54. 5VDDA / 3VDDA

55. SYSTEM POWER

56. DDRII Power

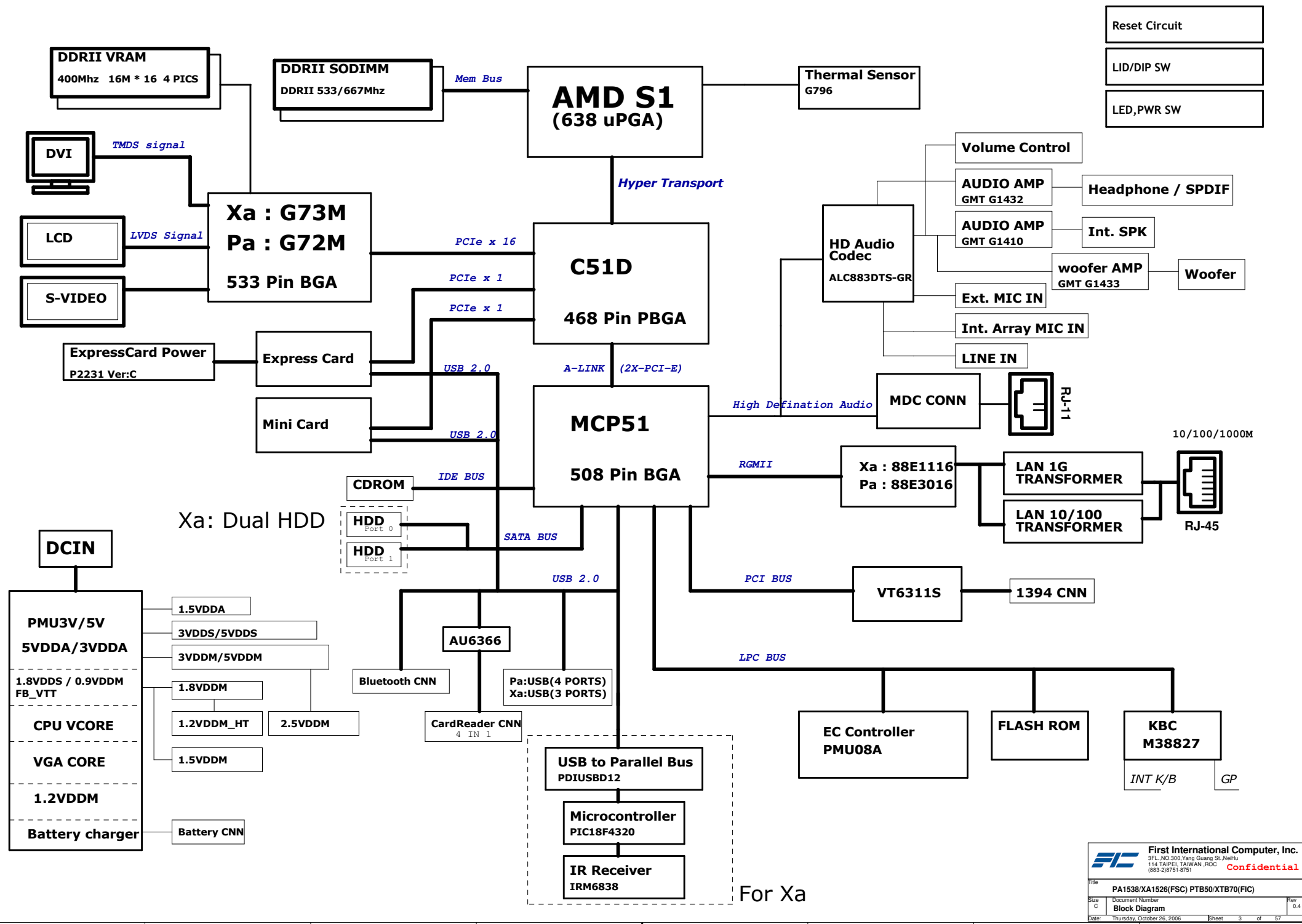
57. VGA_VDD / 1.2V / 1.5V

2. PCI BUS Description :

IDSEL	CHIP
AD22	1394 VIA VT6311S

PCIINT	CHIP
IRQA	1394 VIA VT6311S
IRQB	—
IRQC	—
IRQD	—

BUSMASTER	
REQ	CHIP
REQ0 / GNT0	—
REQ1 / GNT1	1394 VIA VT6311S
REQ2 / GNT2	—
REQ3 / GNT3	—
REQ4 / GNT4	—



4. Net name Description :

5.Board Stack up Description

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
1.5VDDA	1.5V always on power rail by DCON or PSUSC0
5VDDS	5.0V power rail
3VDDS	3.3V power rail
1.8VDDS	1.8V power rail
FB_VTT	0.9V power rail for VGA
0.9VDDM	0.9V DDR Termination Voltage
5VDDM	5.0V suspend power rail
3VDDM	3.3V suspend power rail
2.5VDDM	2.5V suspend power rail
1.5VDDM	1.5V suspend power rail
VDD_CORE	Core Voltage for VGA
VCPU_CORE	Core Voltage for CPU
1.2VDDM	VCC For CPU & NB
+1.2VHT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

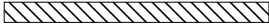

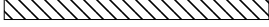


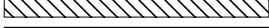

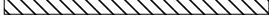
Net Name Suffix

0	=	Active Low signal
---	---	-------------------

Signal Conditioning

D	=	Damped (by a resistor)
Q	=	Isolated (by a Q-switch)
L	=	Filtered (by an inductor or bead)

PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1/Mixer
Layer 4		GND
Layer 5		VCC
Layer 6		IN2/Mixer
Layer 7		GND
Layer 8		BOTTOM

6.Schematic modify Item and History :

V0.1 --> V0.2

- 1.Modify LED circuit for Pa and Xa co-layout.
- 2.Change Card Reader from AU6333 to AU6366.
- 3.R38,R41 change to 56k ohm,C670 change to2200pF,C658 change to 1500pF,Del R385,Add C47 0.1uF(tune power sequence)
- 4.CLK_PMU08 change connect point from R451 to R592
- 5.Add D51,R589 47k ohm (Solve HTMCP_RST# Glitch)
- 6.Revise CN21 Analog connection.
- 7.Change Q11 from 06-20726-01 to 06-23930-01
- 8.Add 0.1uF between U5 pin1,pin2 ,Remove D14.
- 9.Change Headphone AMP from M441 to G1410
- 10.R236 change to NU

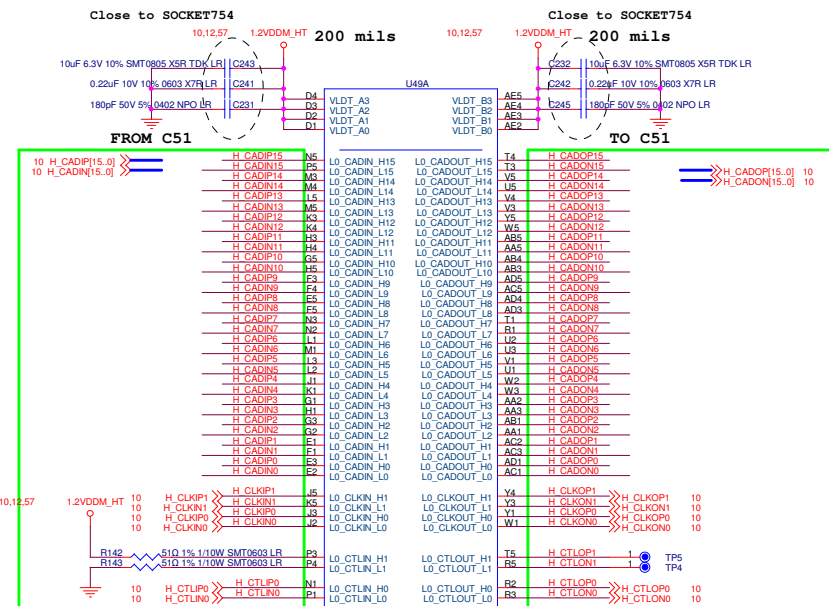
V0.2 --> V0.3

- 1.Change JP1, JP2, JP3, JP9, JP15, JP19, JP23 to 0 ohm 11-14214-00
- 2.Change C16, C17 from 10-40729-02 to 10-60092-01
- 3.Add C883 10-52810-02 on Vcpu_core plane
- 4.L77, L79 changed from 12-01986-01 to 12-01955-01
- 5.C686 changed from NU to stuff.
- 6.CPU VDDIO_FB_L change to NC (FSC recommend)
- 7.Add PCIE CLK serial 0 hm resistor R603,R604,R605,R606,R607,R608 (FSC recommend)
- 8.C647,C652 change from 18pf to 27pf, C630,C633 change from 12pf to 18pf(tune crystal timing)
- 9.D13,R201,C379,R205 change to NU,R205 stuff, Add R600 10k ohm pull down (solve KBC issue)
- 10.For EMI solution
 - Add R272,R273,R274,R275,R276,R277,R278,R279 22 ohm
 - Add C870,C871,C872,C873,C874,C875,C876,C877,C6,C5,C518,C520 5pF
 - Add C551,C548,C546,C880,C881 10pF
 - Add C878,C568,C569 100pF,C571 150pF, C480 1000pF
 - Del L41,L42, Add R238,R239,R385,R521 10ohm

V0.3 --> V0.4

- 1.Del R571, Change R572 from 910 to 1K, change D17 to one lens LED for behavior issue.
- 2.Del Q65, Change Q70 to P-MOS (06-20593-01) for behavior issue.
- 3.Del R56, R329, R189, R436, R528, R110 to short.
- 4.Add C884, C885, C886, C887 location but no stuff to prevent noise issue.
- 5.Del JP7, JP18, JP25, JP13, JP24, JP11, JP10, JP8, JP12, JP14, JP29, JP4, JP22, JP6, JP21, JP5, JP17 to short.
- 6.C45(47pF), C55(33pF) change to 150pF, R31 change from 12k to 18k.
- 7.Add R613 between R531 to GND.
- 8.C1, C2, C535, C597 from NU to stuff, add C890 on DCIN_CPU for EMI request.
- 9.Change L81, L82 to 0 ohm, add C891, C892, C893 for L1 enable function.
- 10.Add Card control power solution
- 11.Add Lan PHY power control circuit.
- 12.Modify RF LED circuit.
- 13.Modify DVI circuit.
- 14.Modify Audio Mute circuit.
- 15.For EMI solution
 - Add C494 200pF
 - Add C898,C899,C900,C901,C902,C903,C904,C905 5pF (NU)
 - Add R189 0 ohm
 - Add R258,R329,R436 0 ohm (NU)
 - Add one spring

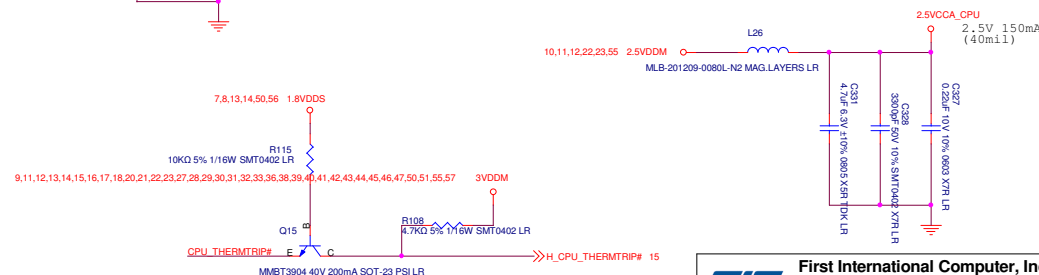
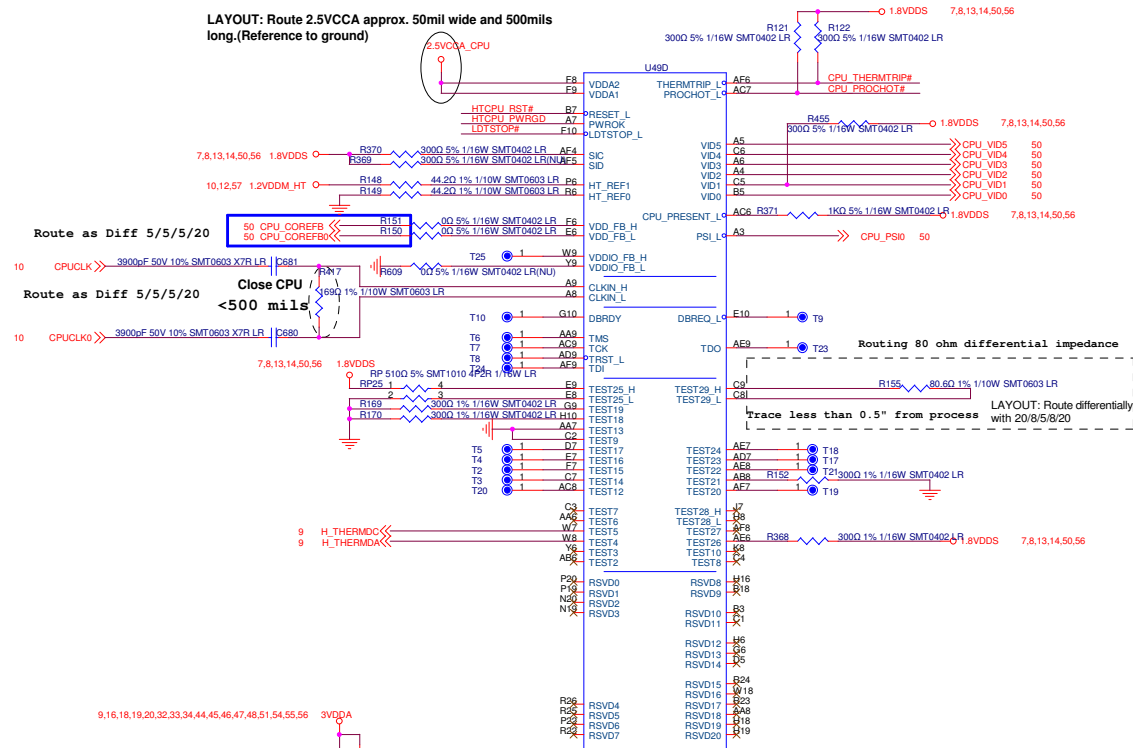
ClawHammer HT Interface



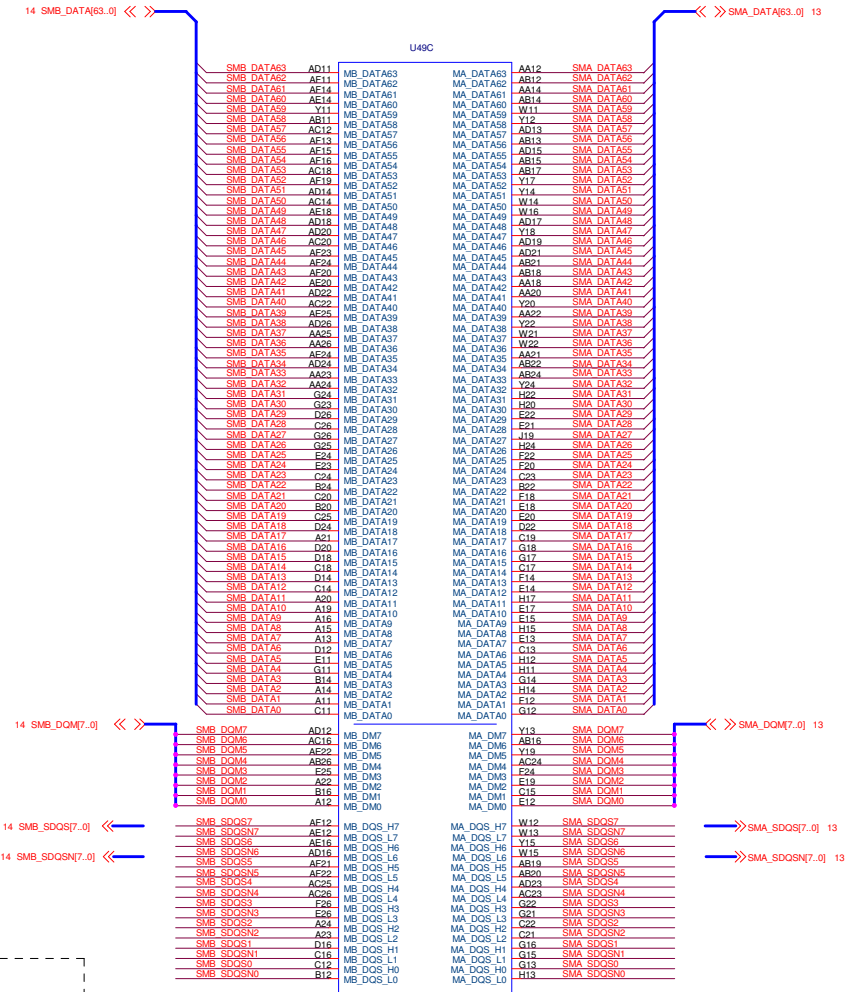
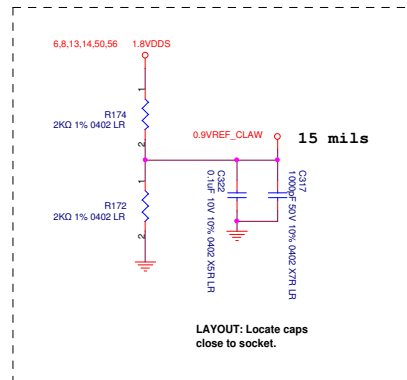
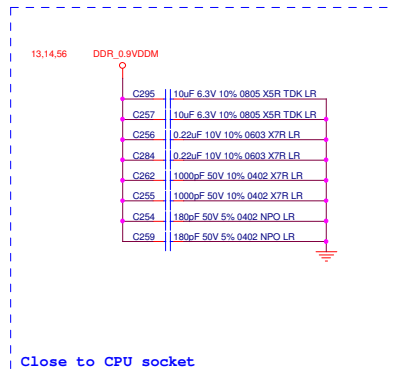
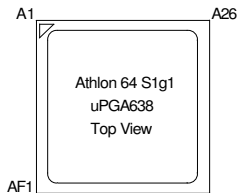
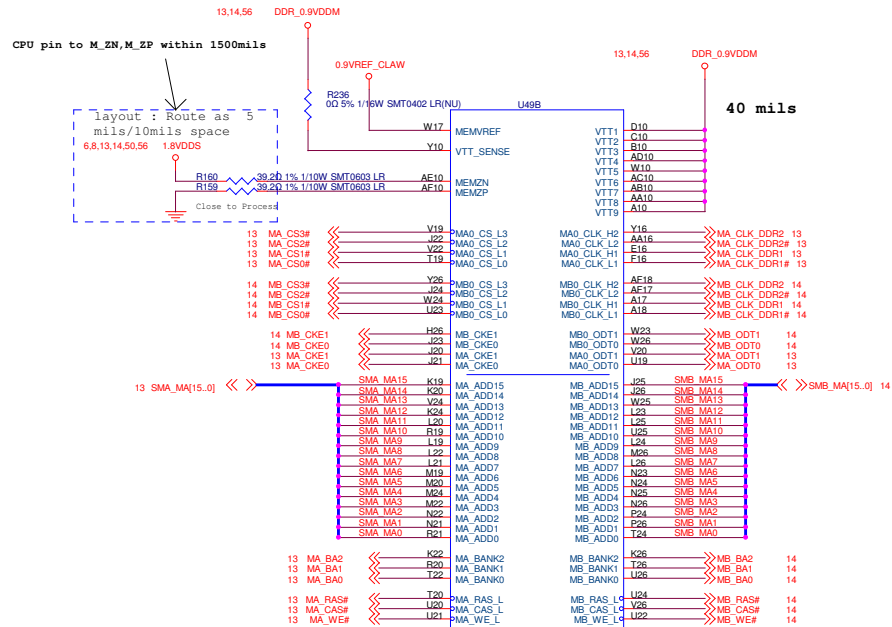
HT BUS General Routing Rules:

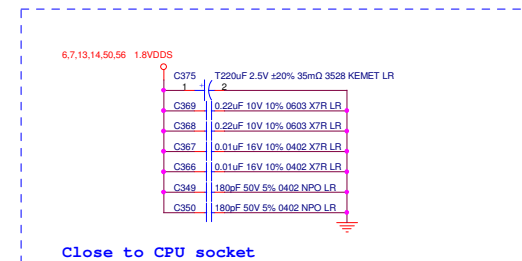
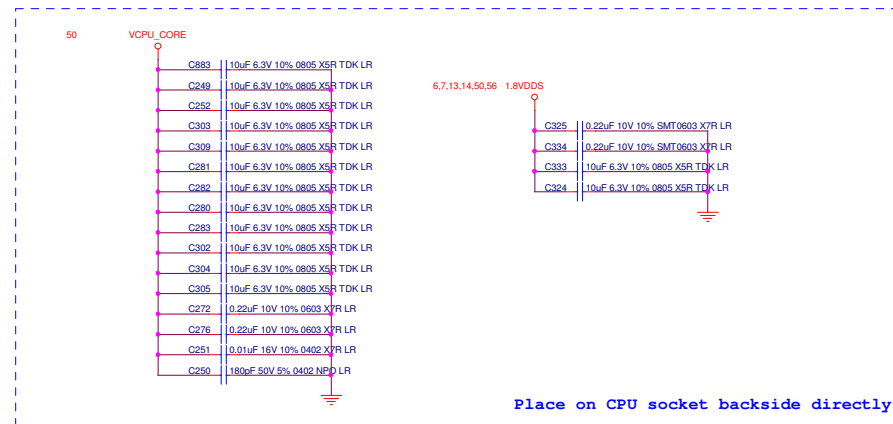
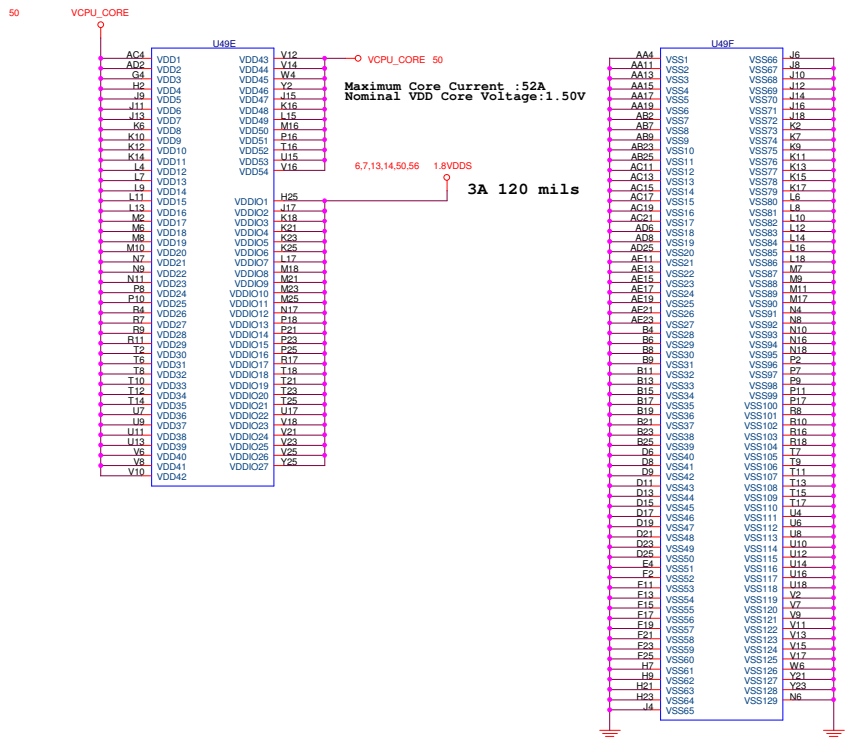
1. HT BUS is easy to route, and uses minimal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.

LAYOUT: Route 2.5VCCA approx. 50mil wide and 500mils long.(Reference to ground)

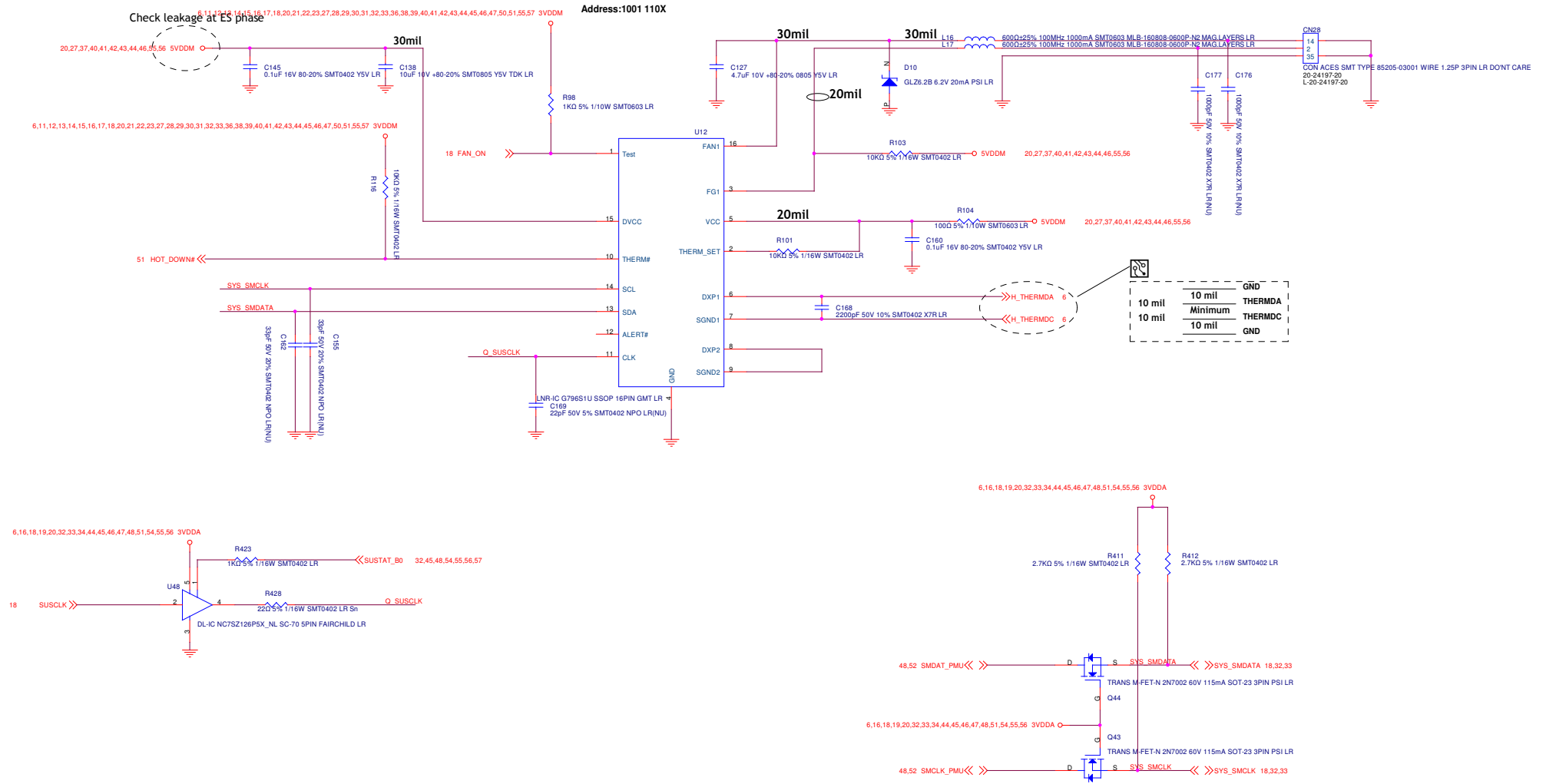


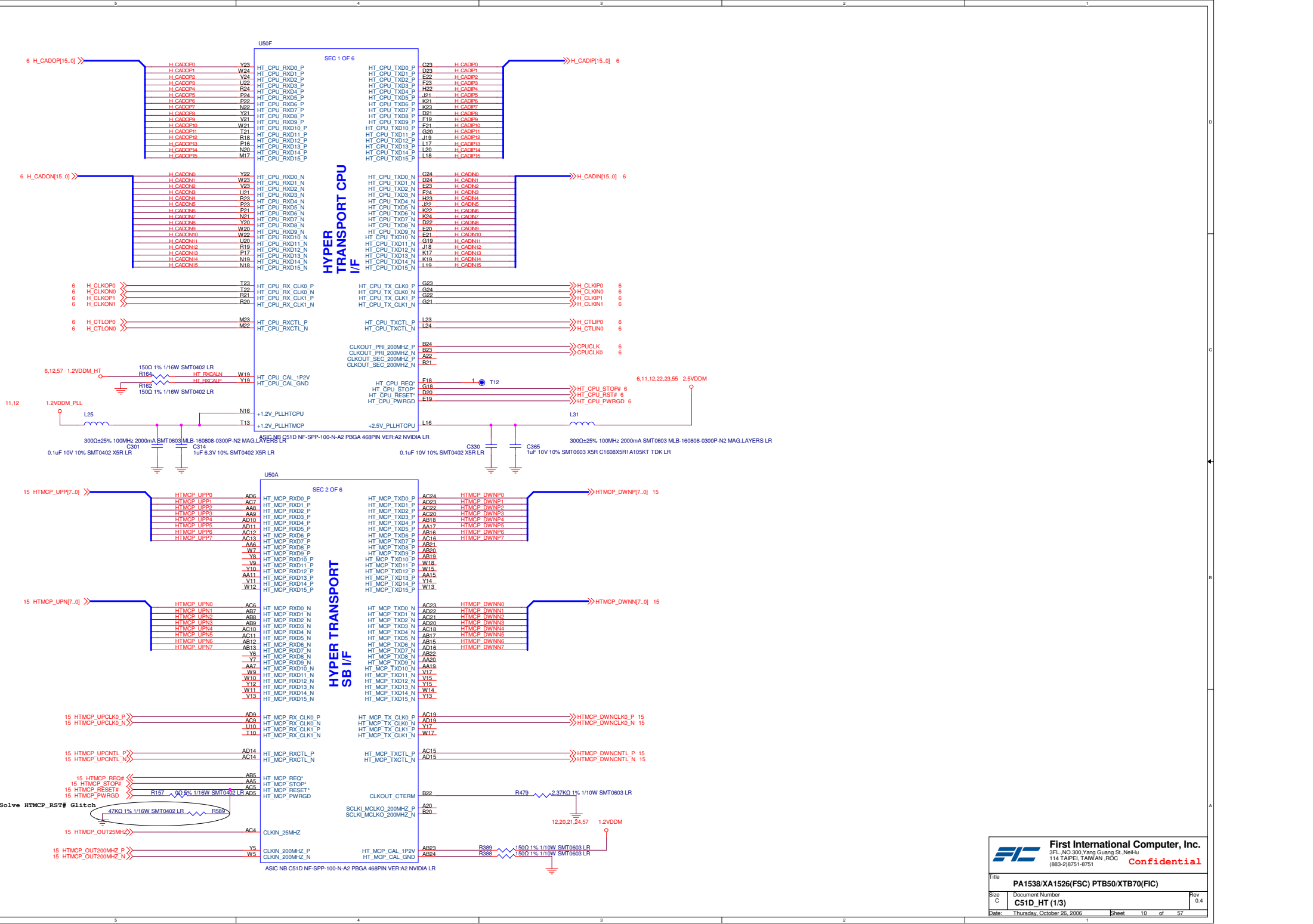
Clawhammer DDR Interface





THERMAL SENSOR



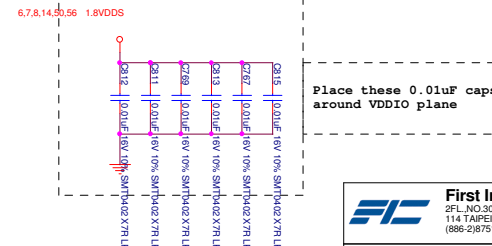
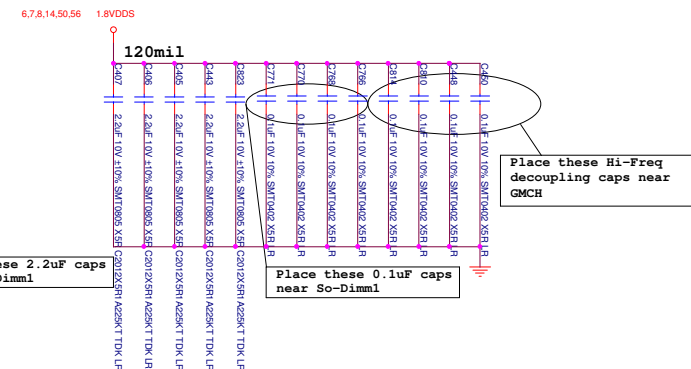
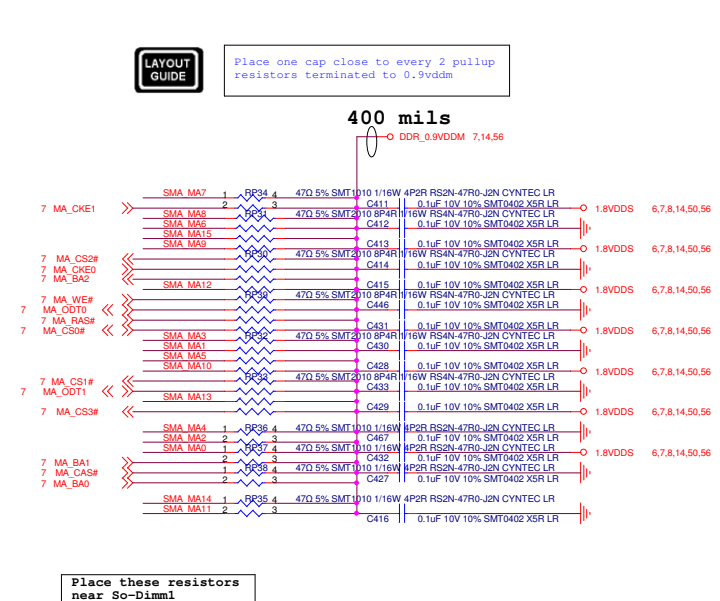


First International Computer, Inc.
3FL NO.300, Yang Guang St., Neihu,
114 TAIPEI, TAIWAN, ROC
(886-2)8751-8751

Confidential

Title			PA1538/XA1526(FSC) PTB50/XTB70(FIC)
Size	Document Number	Rev	0.4
C	C51D_HT (1/3)		
Date:	Thursday, October 26, 2006	Sheet	10 of 57

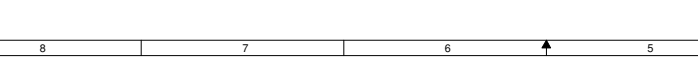
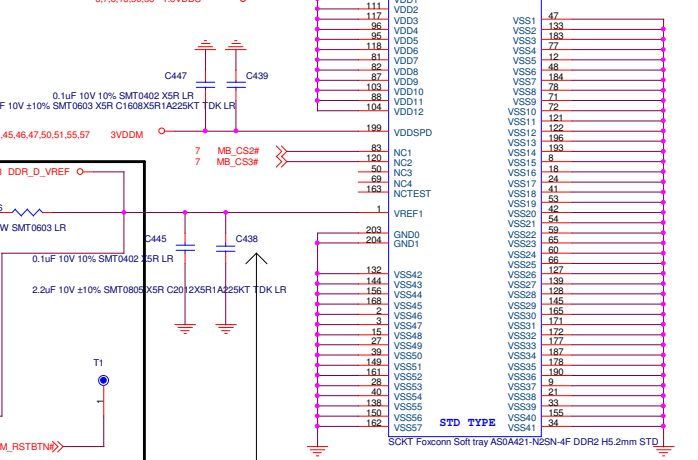
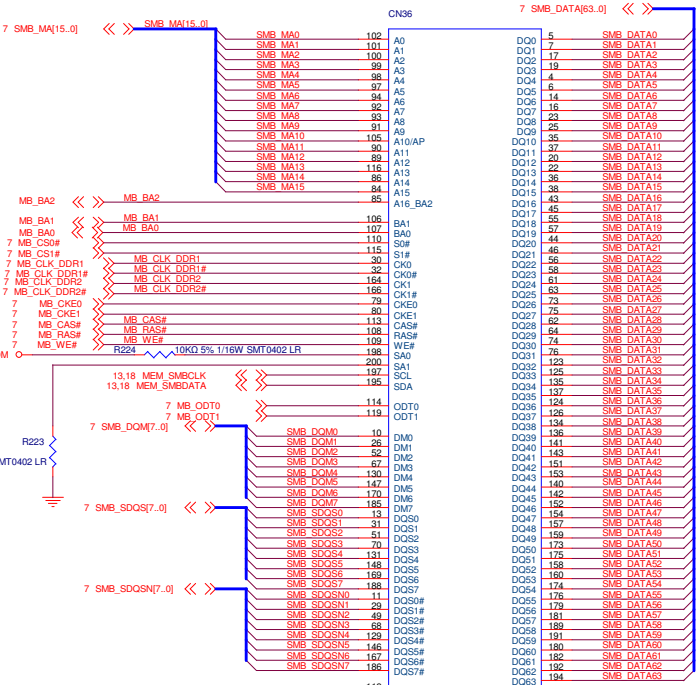
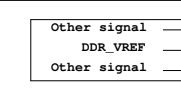
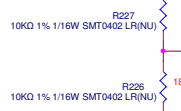
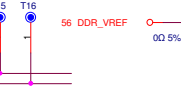
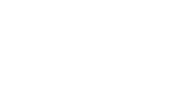
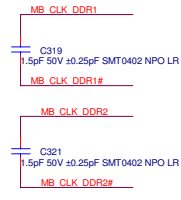


SO DIMM 0

First International Computer, Inc.
2FL, NO.300, Yang Guang St., NeiHu
114 TAIPEI, TAIWAN, ROC
(886-2)8751-8751

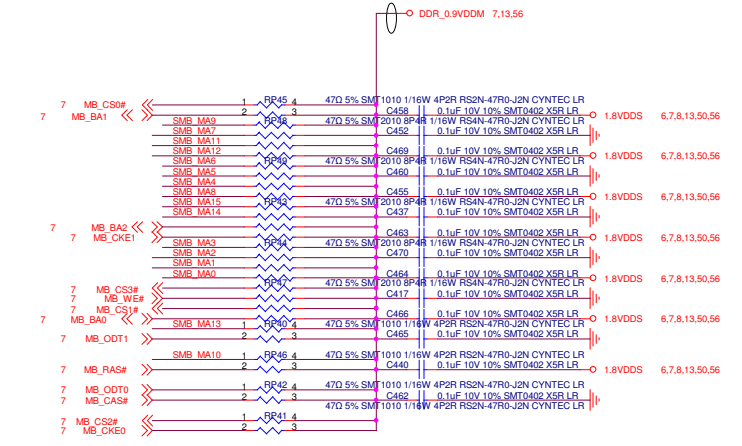
Title	PA1538/XA1526(FSC) PTB50/XTB70(FIC)		
Size	Document Number	Rev	
C	DDRII SO-DIMM 0 RSV	0.	
Date:	Thursday, October 26, 2006	Sheet	13 of 57

PLACE CLOSE TO CPU
WITHIN 1.5 INCH



Place one cap close to every 2 pullup
resistors terminated to 0.9vddm

400 mils



120mil

Place these 2.2uF caps
near So-Dimm0

Place these 0.1uF caps
near So-Dimm0

SO DIMM 1



Other signal	20mil	20mil
DDR_VREF		
Other signal	20mil	

First International Computer, Inc.
2FL NO.300, Yang Guang St. N.Hu
114 TAIPEI, TAIWAN, ROC
(886-2)8751-8751

Confidential

Title
PA1538/XA1526(FSC) PTB50/XTB70(FIC)

Size
C

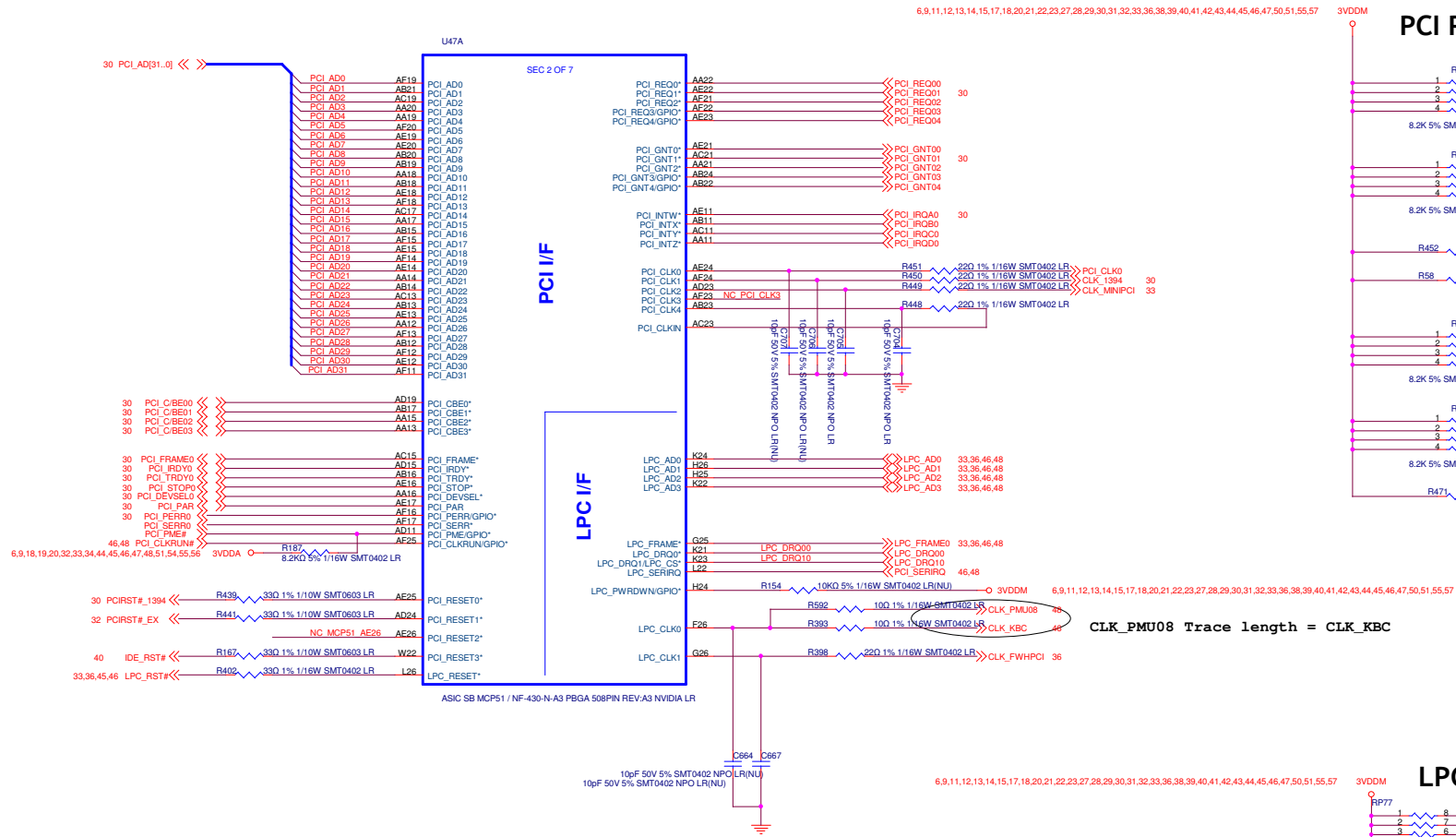
Document Number
DDRII SO-DIMM 1 STD

Date
Thursday, October 26, 2006

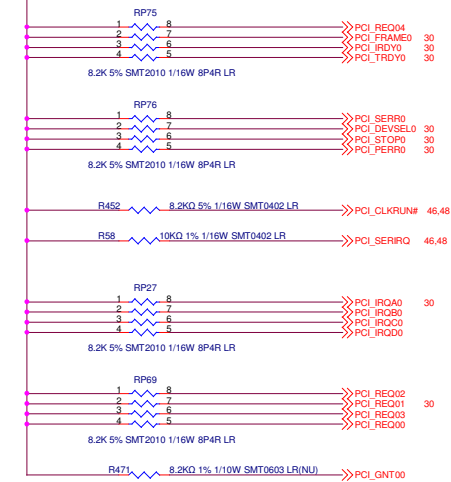
Sheet
14

of
57

Rev
0.4

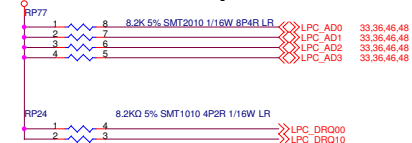


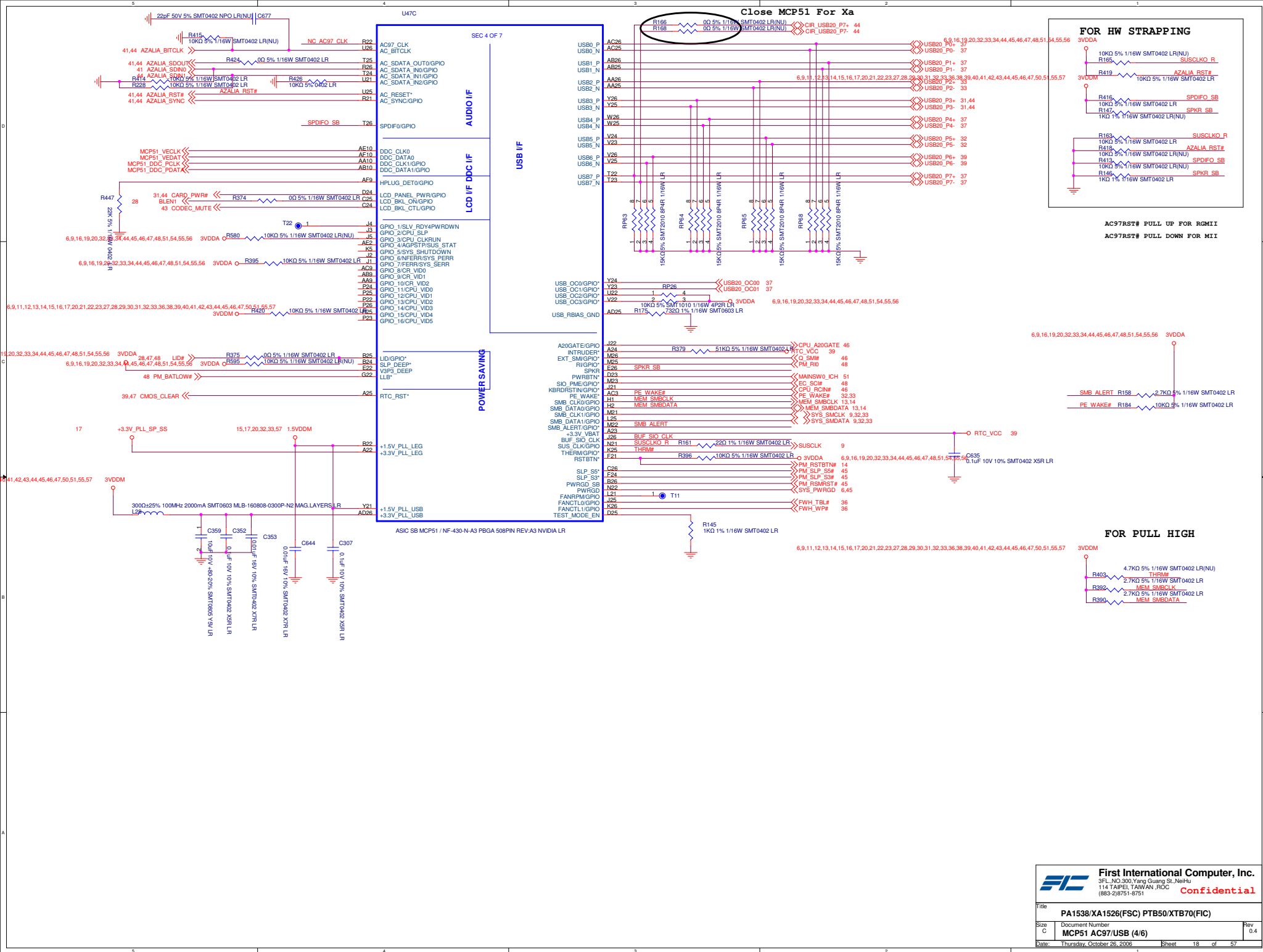
PCI Pull Up/Down

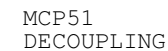


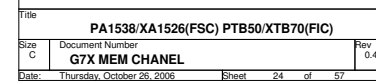
CLK_PMU08 Trace length = CLK_KBC

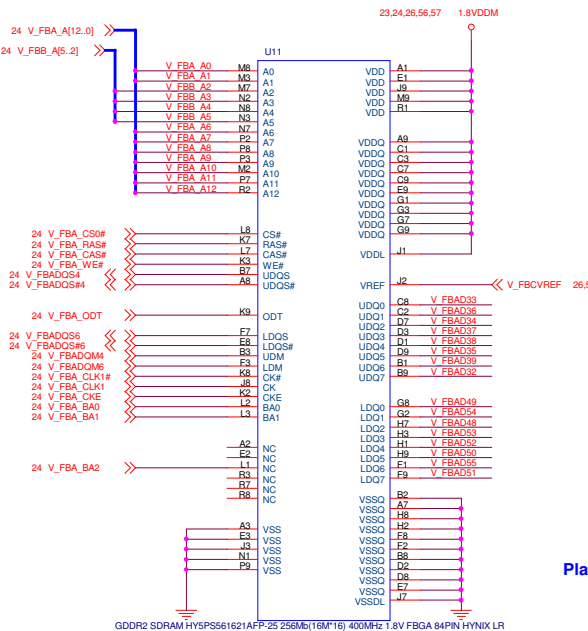
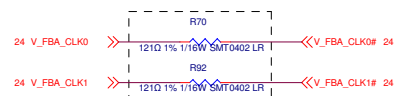
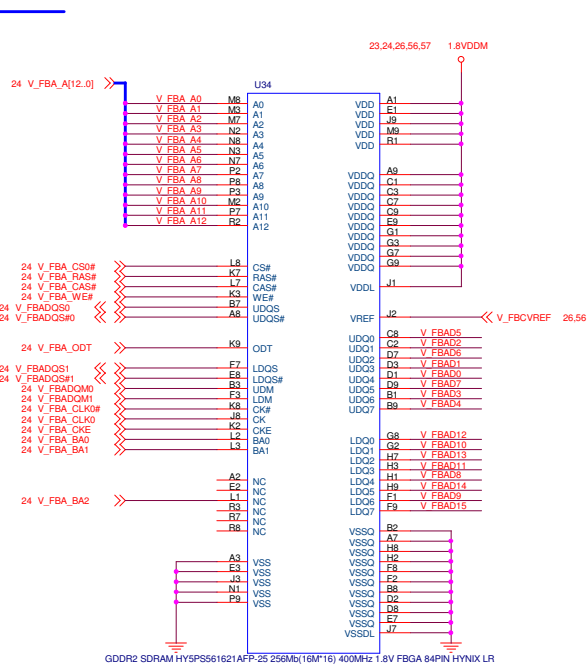
LPC Pull Up





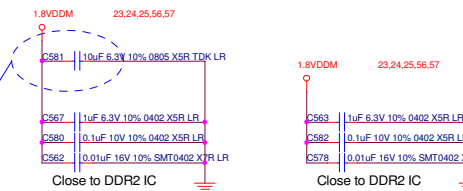
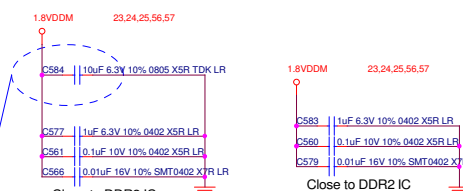
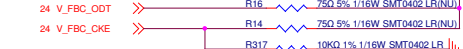
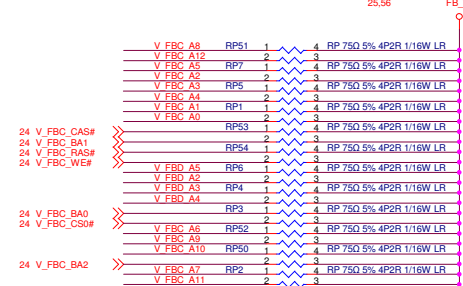
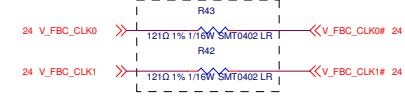






Pa: No Stuff
Xa: Stuff

G72M : 120 ohm
G73M : 470 ohm (11-13130-00)

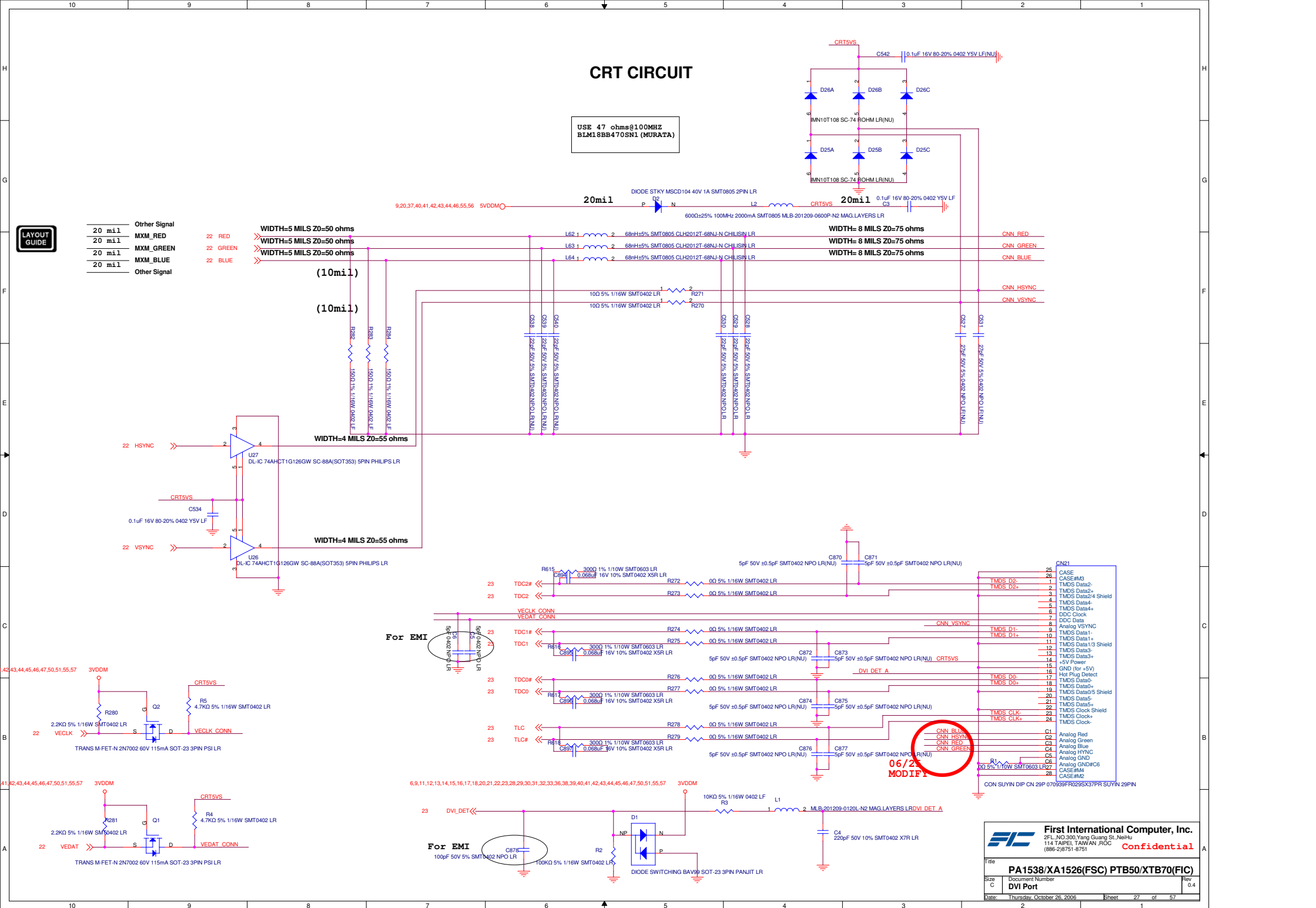


Placed between two VRAM

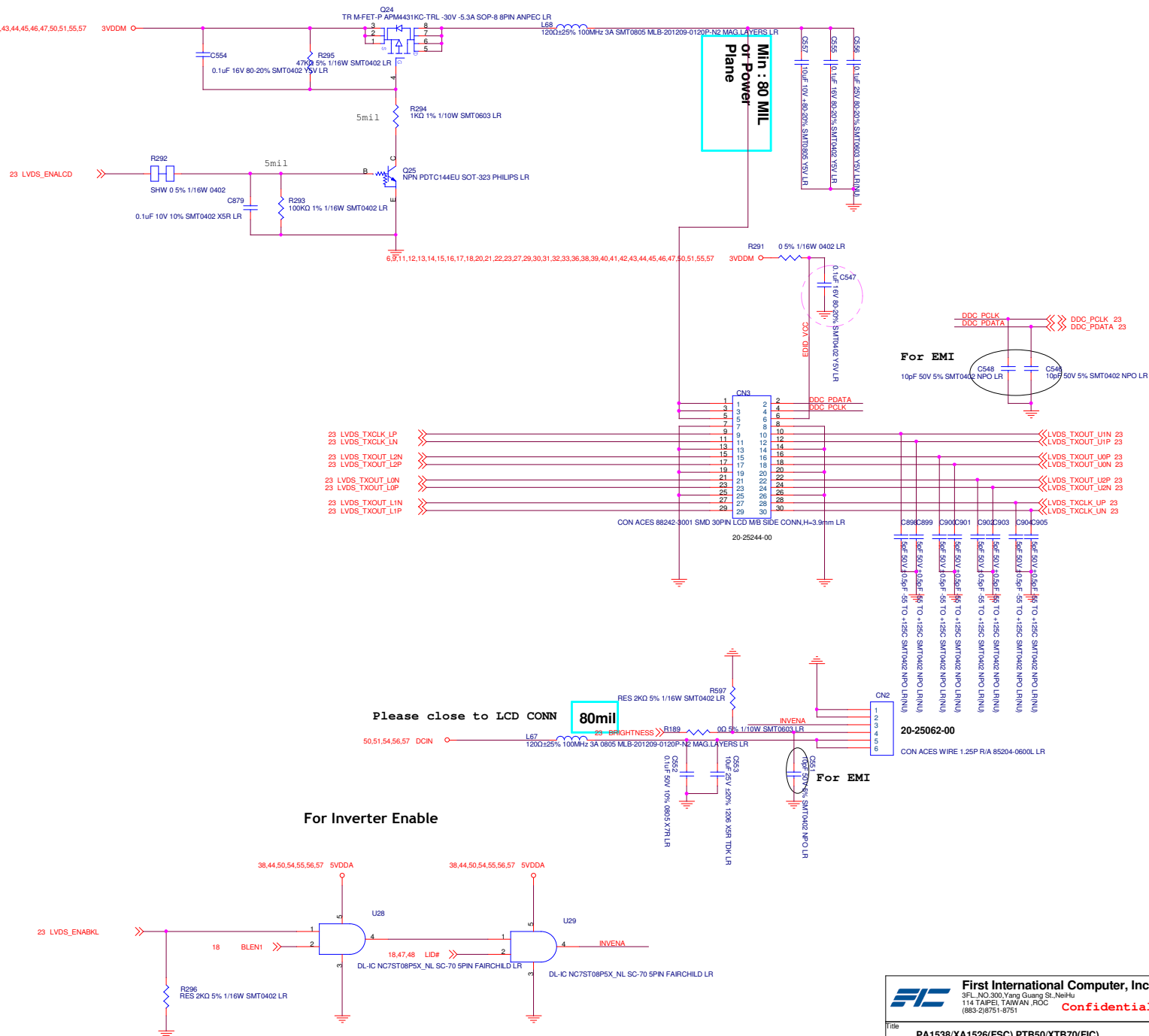
First International Computer, Inc.
3FL NO.300 Yang Guang St. Neihu
114 TAIPEI, TAIWAN, R.O.C.
(8863-2)8751-8751
Confidential

Title				PA1538/XA1526(FSC) PTB50/XTB70(FIC)			
Size C	Document Number			Rev C			
	VGA DDR2_C CHANNEL						
Date:	Thursday, October 26, 2006		Sheet	26	of	57	

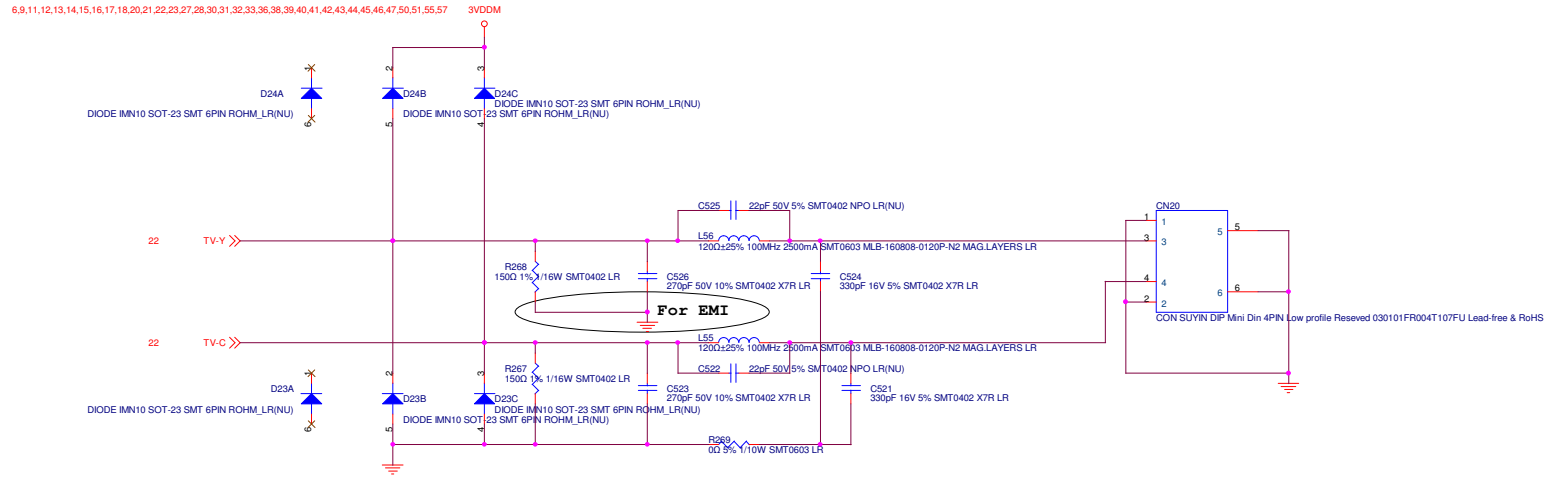
USE 47 ohms@100MHZ
BLM18BB470SN1 (MURATA)

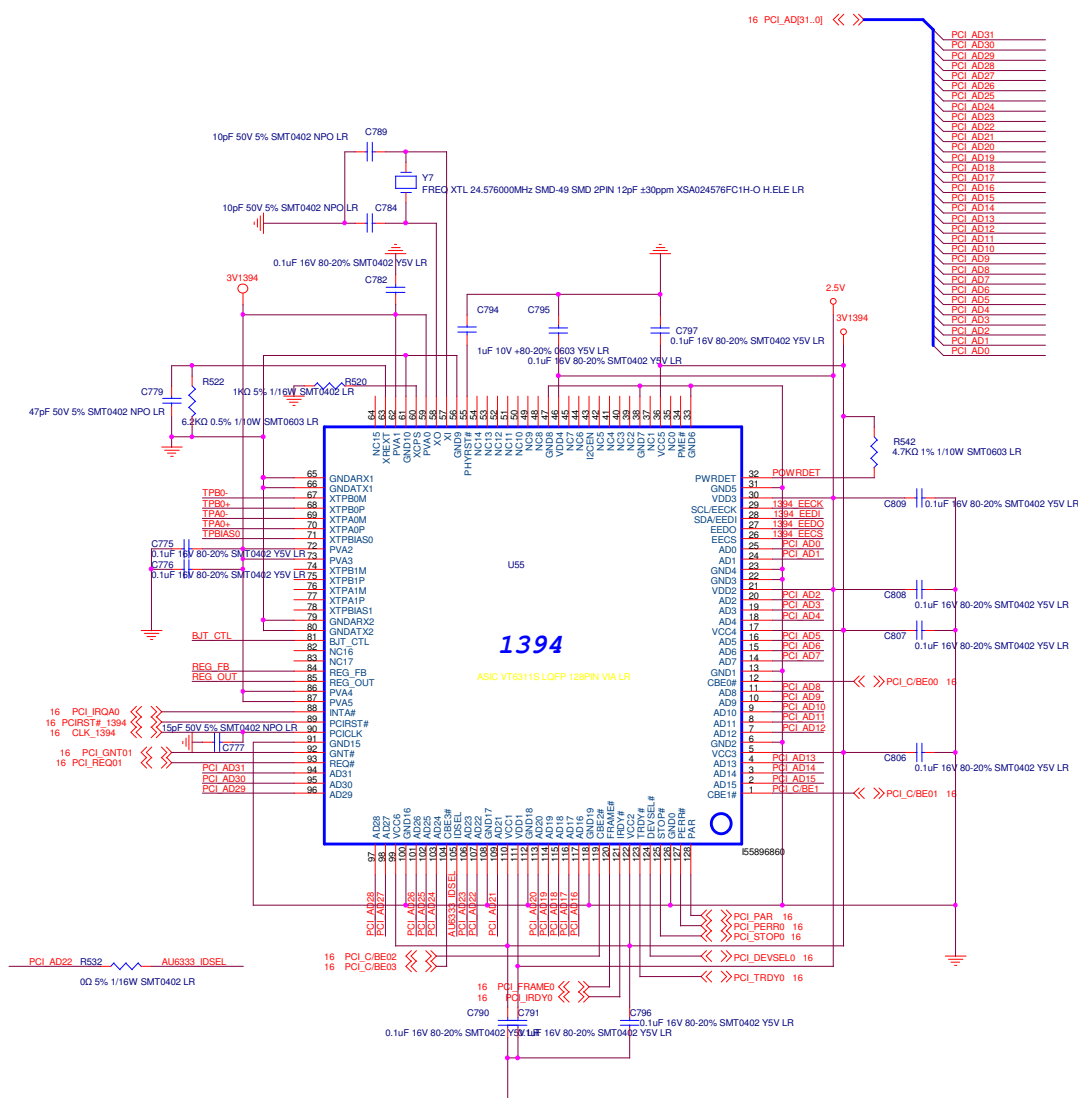


6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,29,30,31,32,33,36,38,39,40,41,42,43,44,45,46,47,50,51,55,57
 ICC_MAX=2A
 PATTERN
 WIDTH=MIN.
 2MM(80MIL)

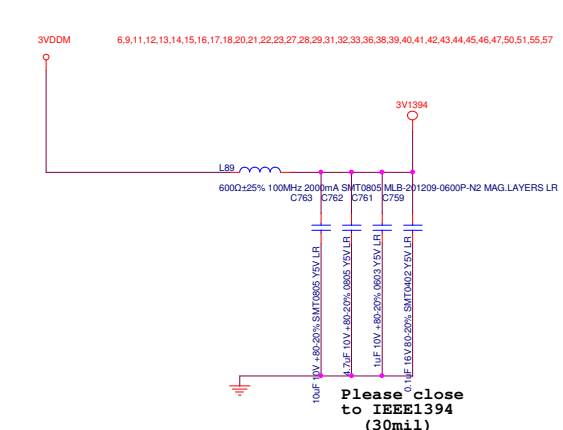
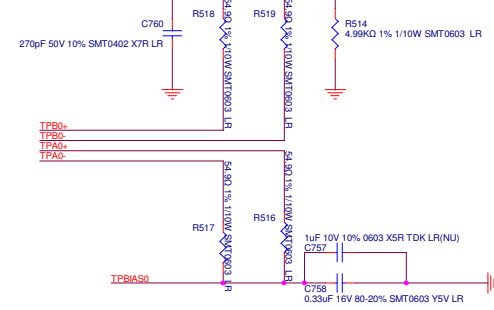


TV OUT CIRCUIT

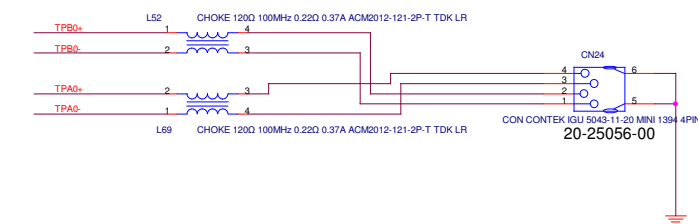
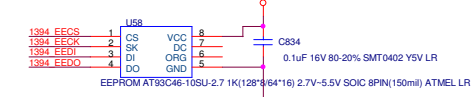
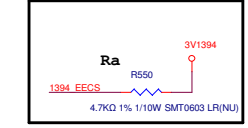




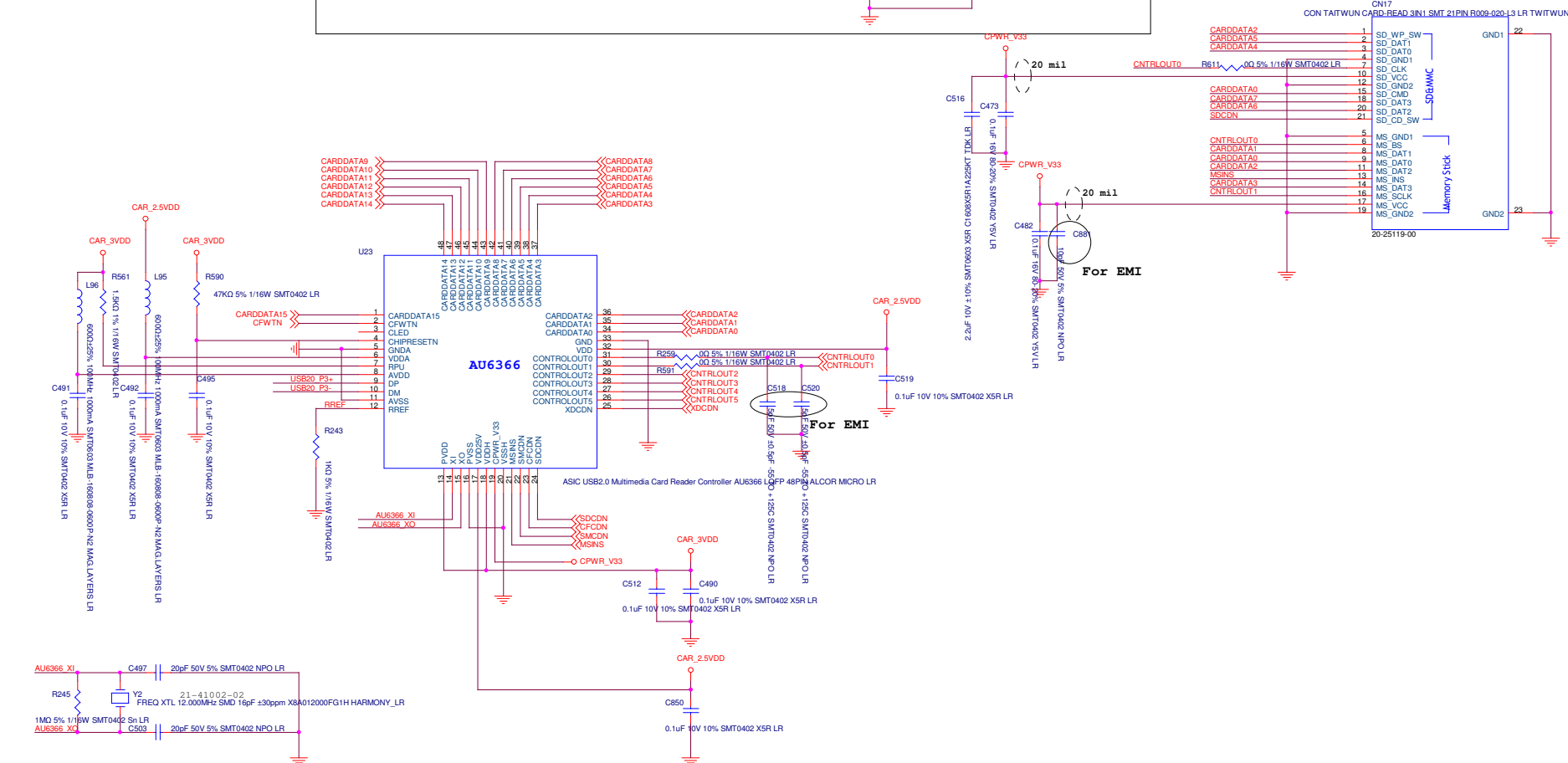
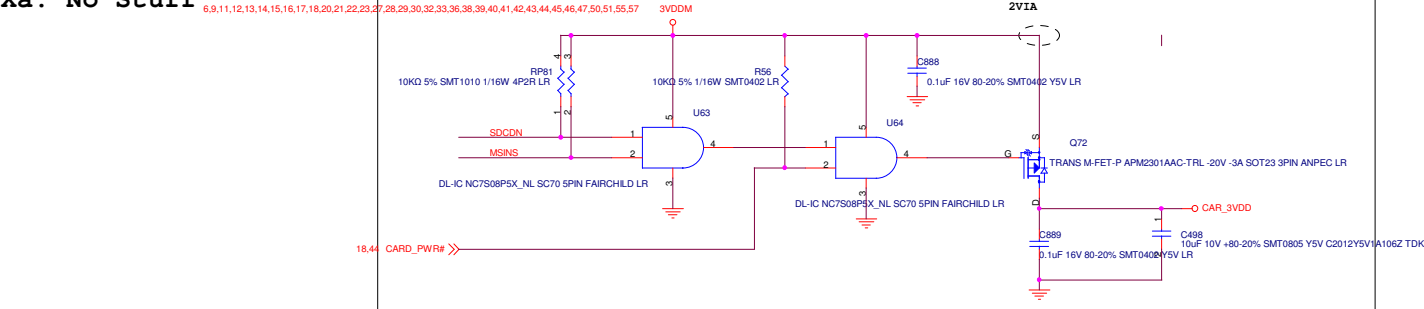
Please close to 1394 Chip

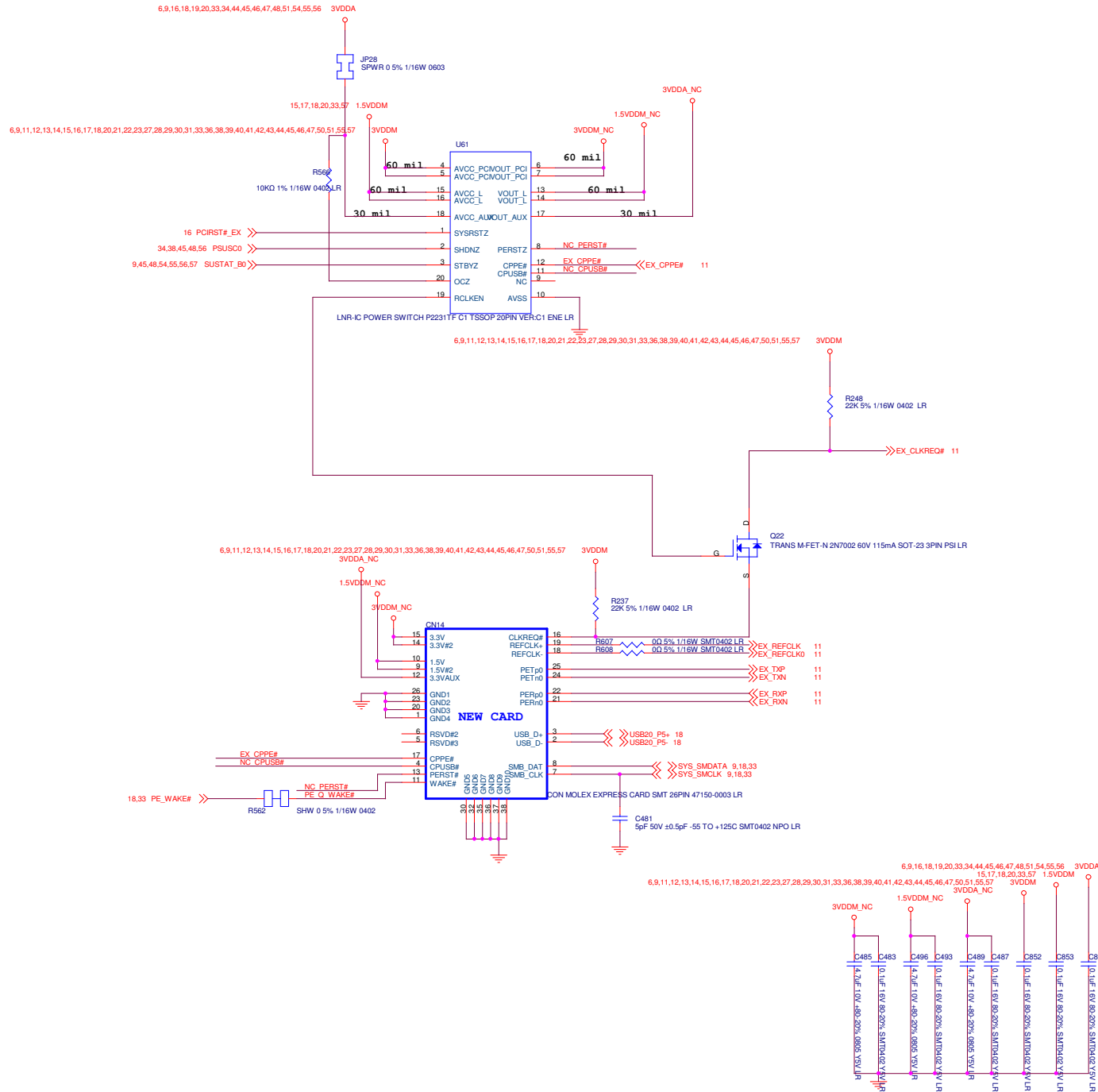


If use EEPROM-less, Ra must stuff



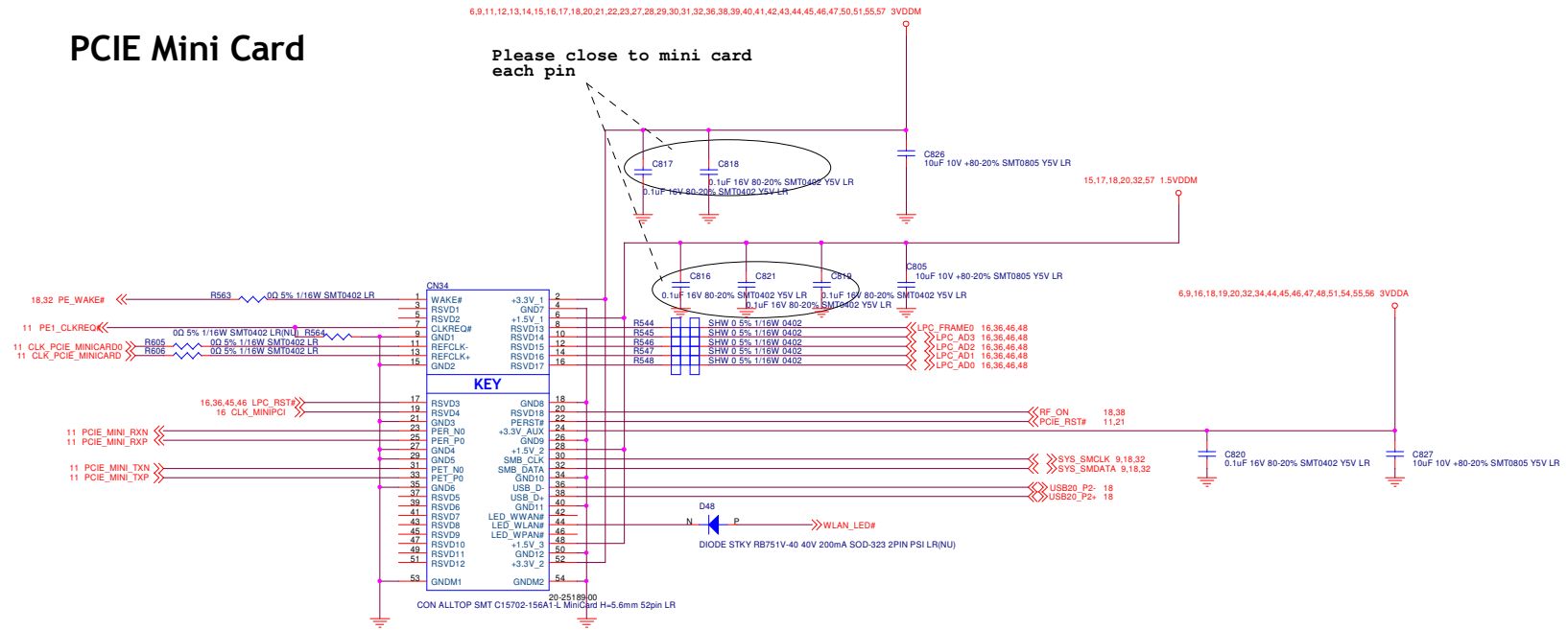
Pa: Stuff
Xa: No Stuff



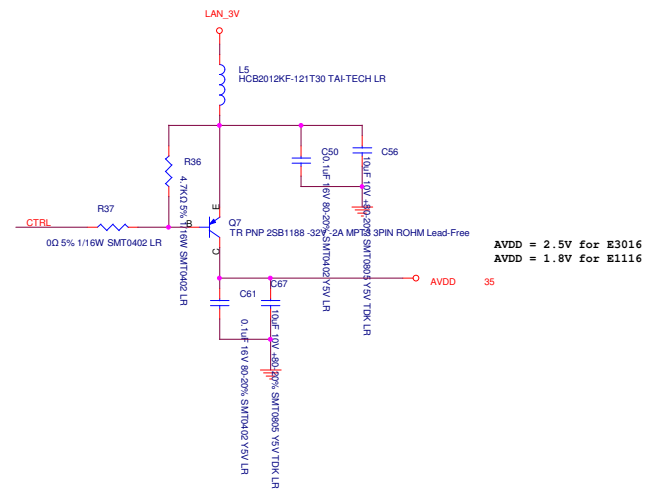


PCIE Mini Card

Please close to mini card
each pin

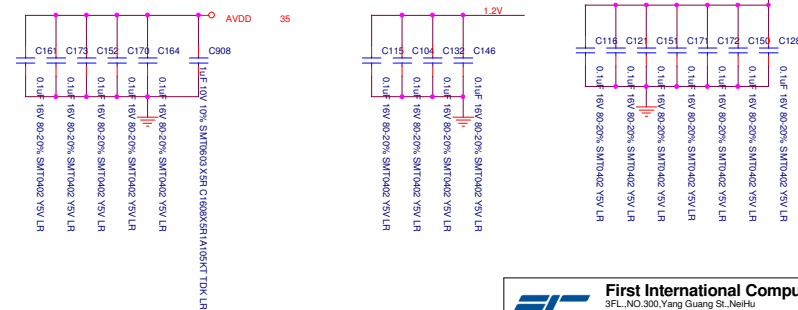


Xa: PHY use 88E1116

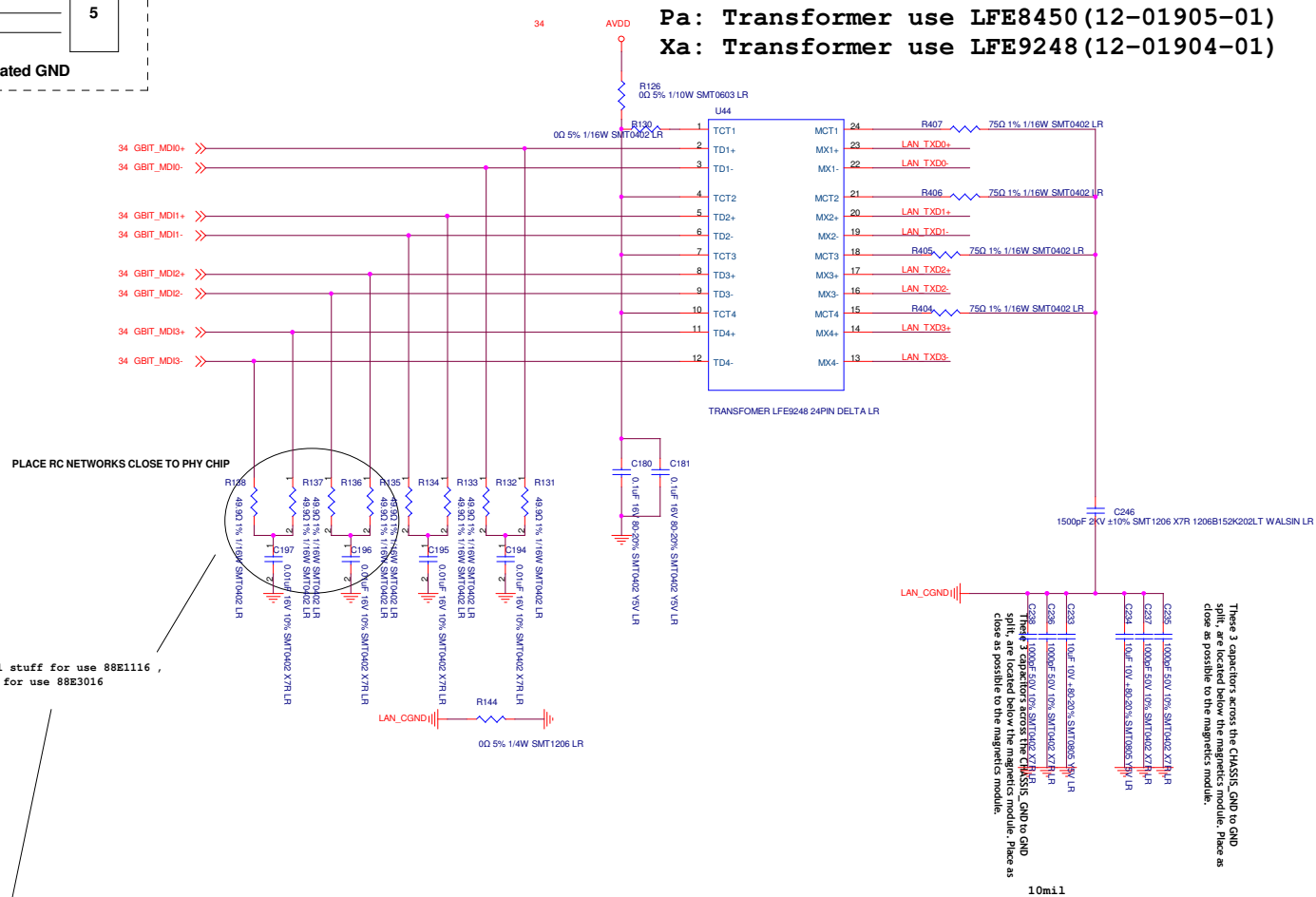
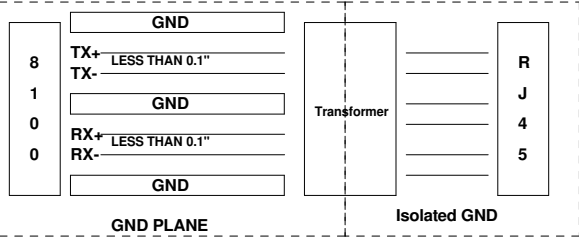


	for 88E3016	for 88E1116
Ra	NU	STUFF
Rb	NU	STUFF
Rc	STUFF	NU
Rd	NU	STUFF
Re	STUFF	NU

1. The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip, and away from signal traces(ex:MDIO4/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. Termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins, such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer, and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum length between Lan Chip and transfer is achievable only when there's no interferences around.
9. The termination resistor(49.9k) must close to Lan Chip, and make them 4pairs as same as distant.
10. PLACE AND PLANE AS LARGE AS POSSIBLE
11. If power pins are next to each other and there is not much room to accommodate multiple capacitors, then the power pins can share the same capacitors.
12. It's important to separate digital signals from analog signals. If it is unavoidable to cross digital signals with analog power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15. The Lan Chip pin 1 facing the transformer, then you can make the signal shorter.

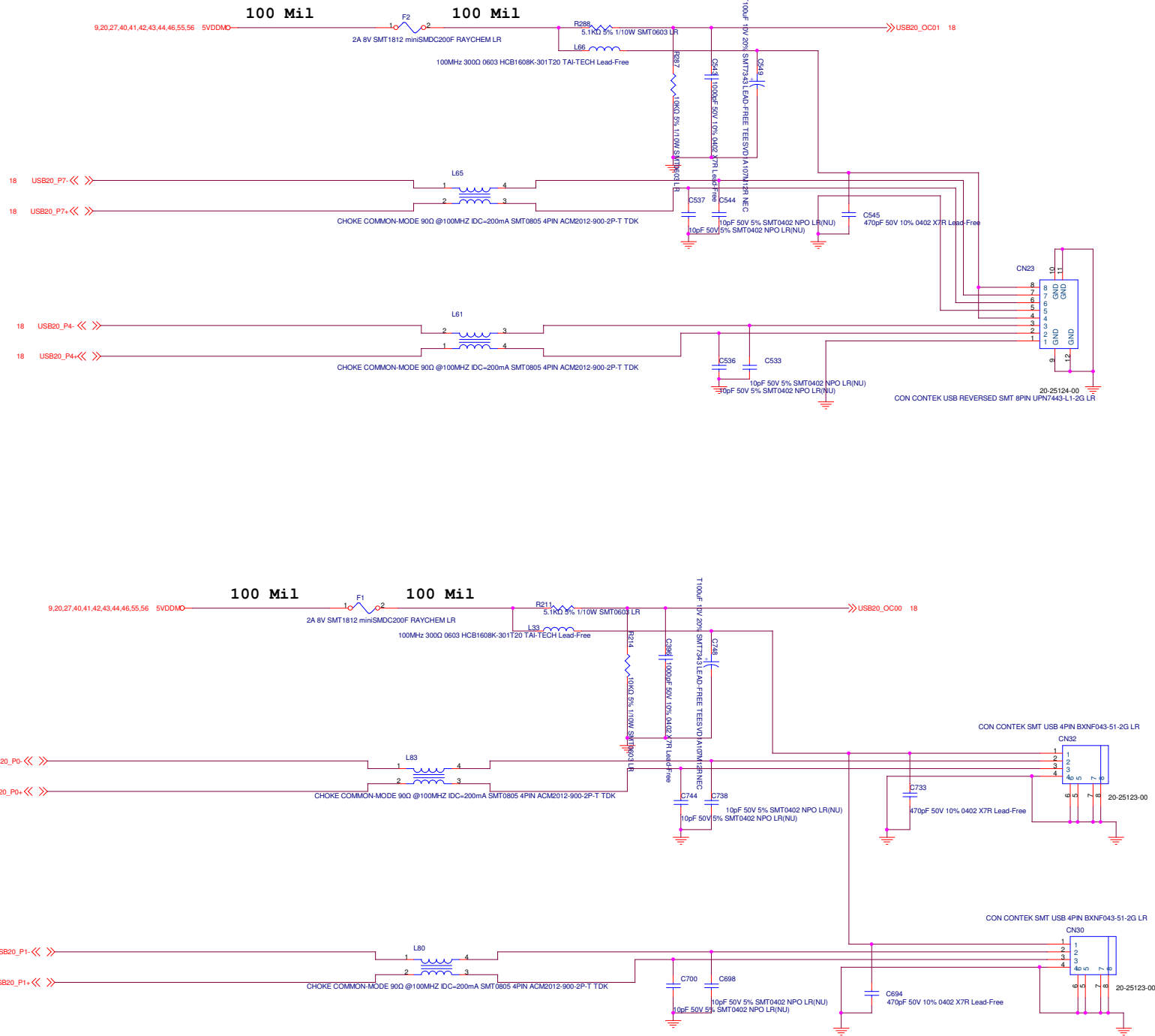


TX 100 ohm ----> trace 4 mil , space 10 mil
RX 50 mil space from other signals
Total Trace Length no more thans 4.8"
2 Differential pairs must have the same length

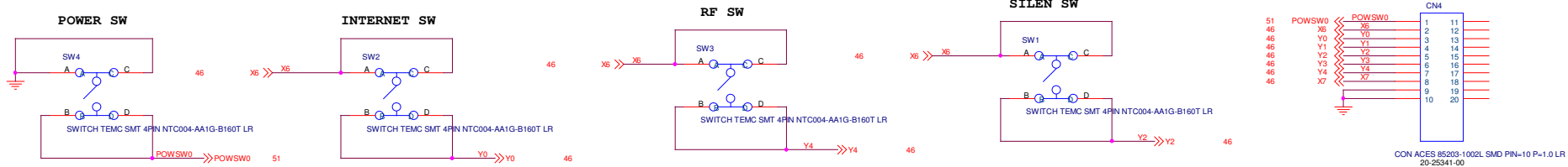


5 mil _____ 10 mil _____ GND_POWER
5 mil _____ 10 mil _____ USB20_P+
5 mil _____ 5 mil _____ USB20_P-
5 mil _____ 10 mil _____ GND_POWER

USBP+/- must same length



Pa: Switch Xa: No stuff



Pa: LED indicator control logic

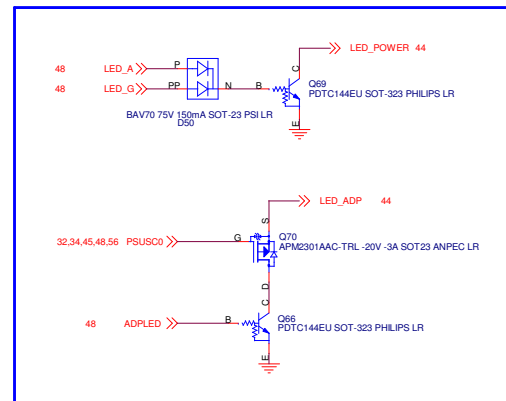
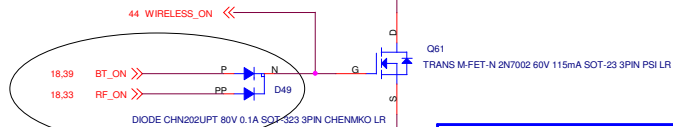
Xa: No stuff

Power indicator

Charge indicator

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,39,40,41,42,43,44,45,46,47,50,51,55,57

Wireless indicator

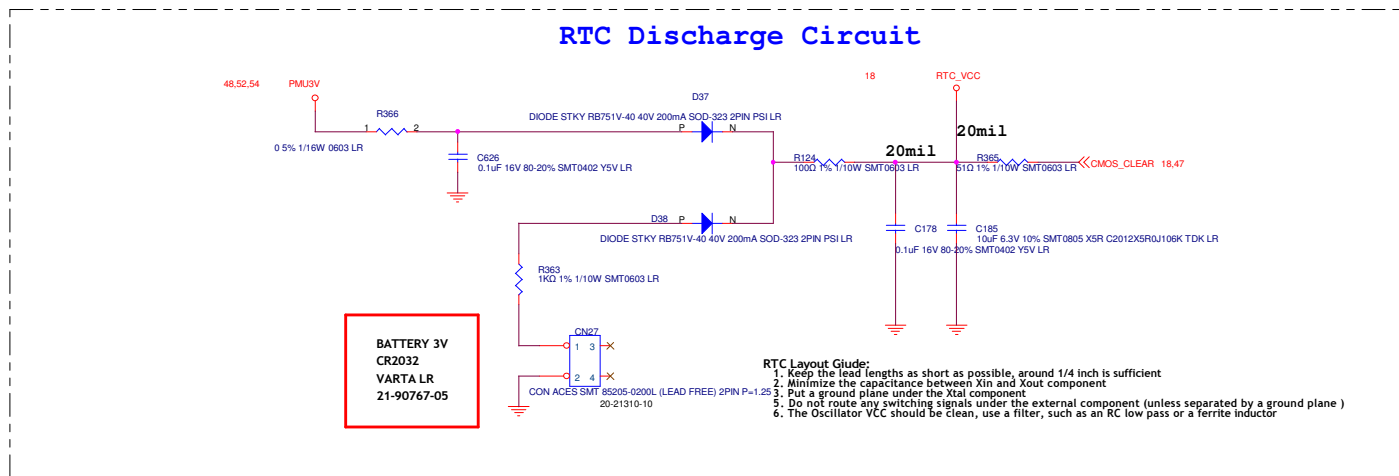


NOTICE

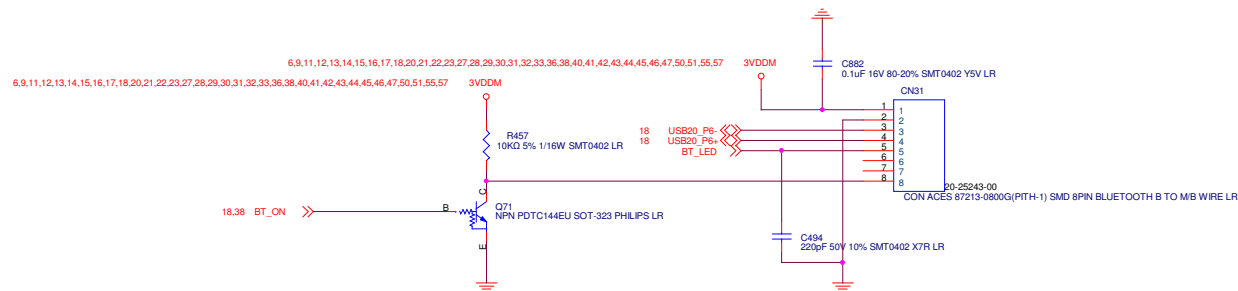
PTB50 → NO STUFF
XTB70 → ALL STUFF

First International Computer, Inc.
3FL NO.300,Yang Guang St.,Neihu
114 TAIPEI TAIWAN, ROC
(883-2)8751-8751

Title			PA1538/XA1526(FSC) PTB50/XTB70(FIC)
Size			Document Number
C			LED / SW
Date:			Thursday, October 26, 2006
Sheet			38 of 57
Rev			0.4



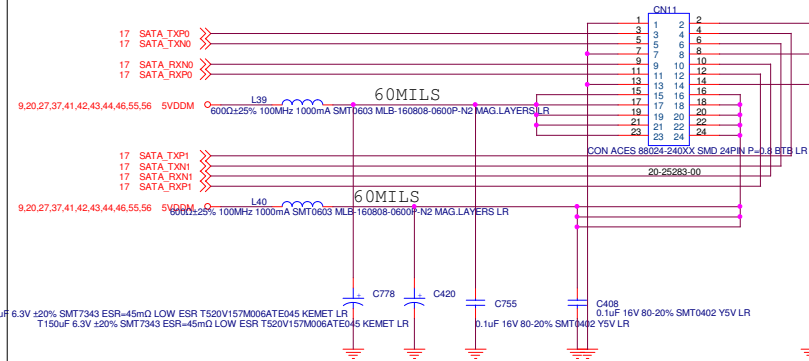
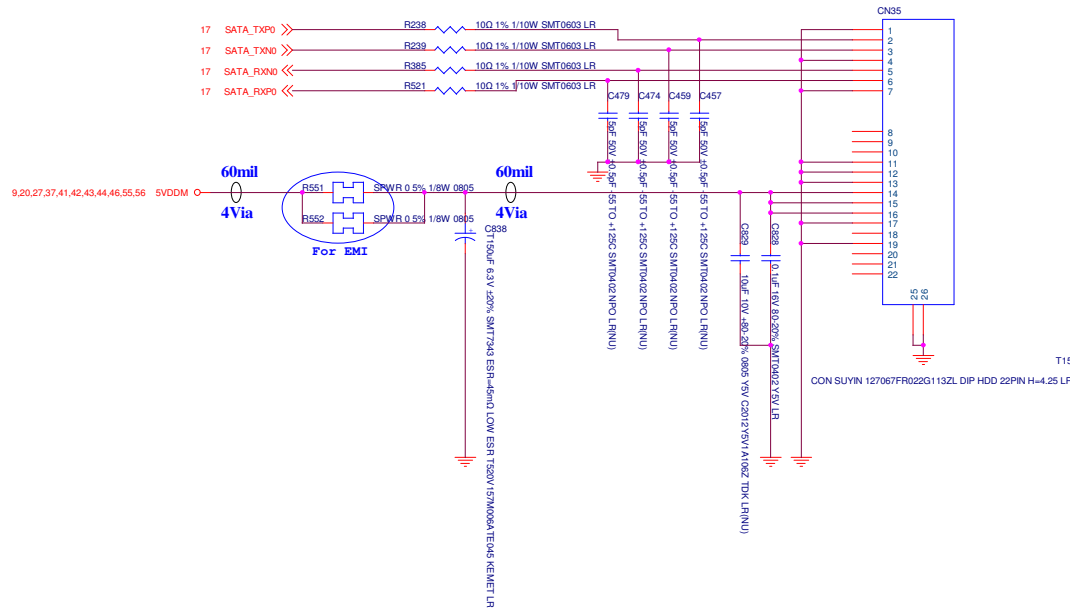
BLUETOOTH



For Pa

HDD I/F

For Xa



SATA Layout Note:

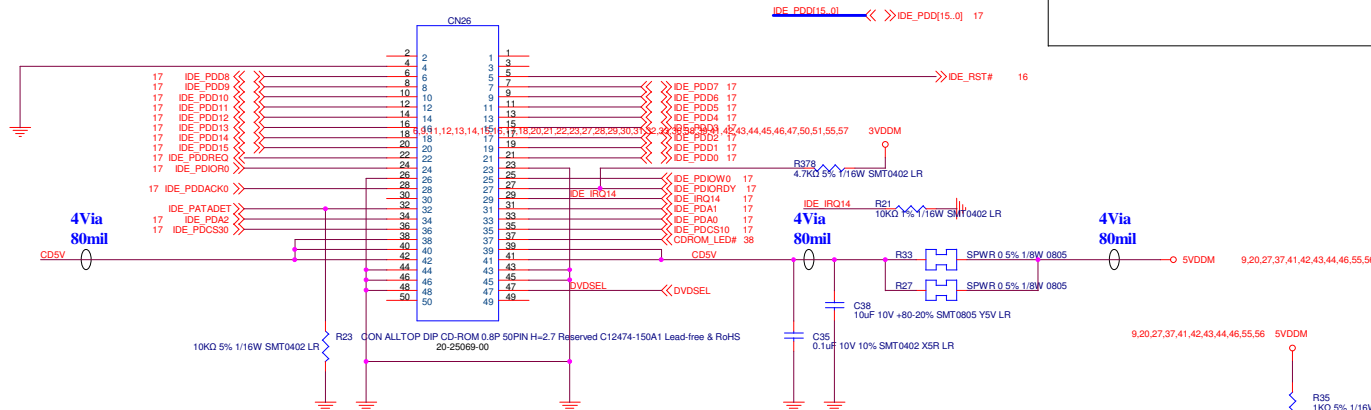
MS or SL:	5mils	5mils	5mils	5mils
20mils	+	8mils	-	20mils

TX

RX

- * Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- * TX/RX trace length < 2 inchs.
- * TX+/- need matching trace ± 10 mils length.
- * RX+/- need matching trace ± 10 mils length.
- * SATA Pair to Pair Trace matching trace ± 10 mils length.

CD-ROM CNN



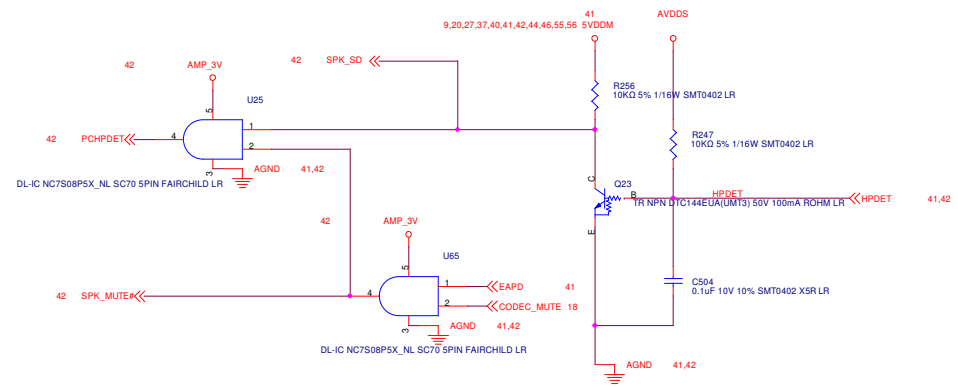
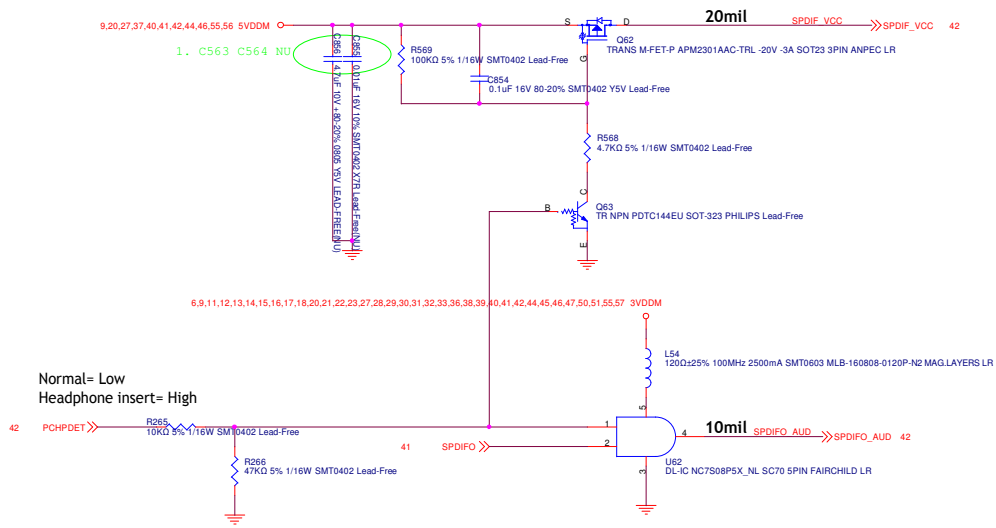
First International Computer, Inc.
3FL NO.300,Yang Guang St.,Neihu
114 TAIPEI, TAIWAN, R.O.C
(883-2)8751-8751

Confidential

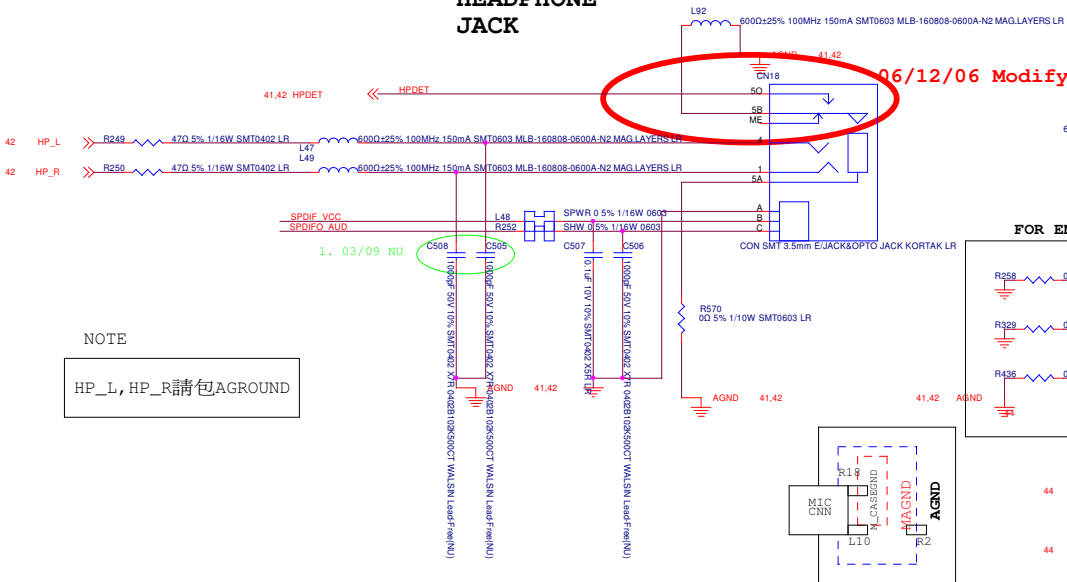
Title	PA1538/XA1526(FSC) PTB50/XTB70(FIC)		
Size	Document Number	Rev	
C	SATA HD / CD-ROM CNN	0.4	
Date:	Thursday, October 26, 2006	Sheet	40 of 57

Title PA1538/XA1526(FSC) PTB50/XTB70(FIC)			
Size	Document Number		Rev
Custom	AMP (G1432&G1410)/AD CN		0.4
Date:	Thursday, October 26, 2006	Sheet	42 of 57

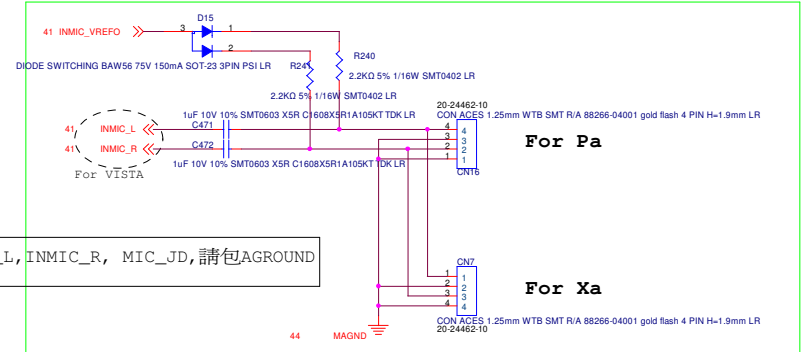
S/PDIF Power



**SPDIF &
HEADPHONE
JACK**



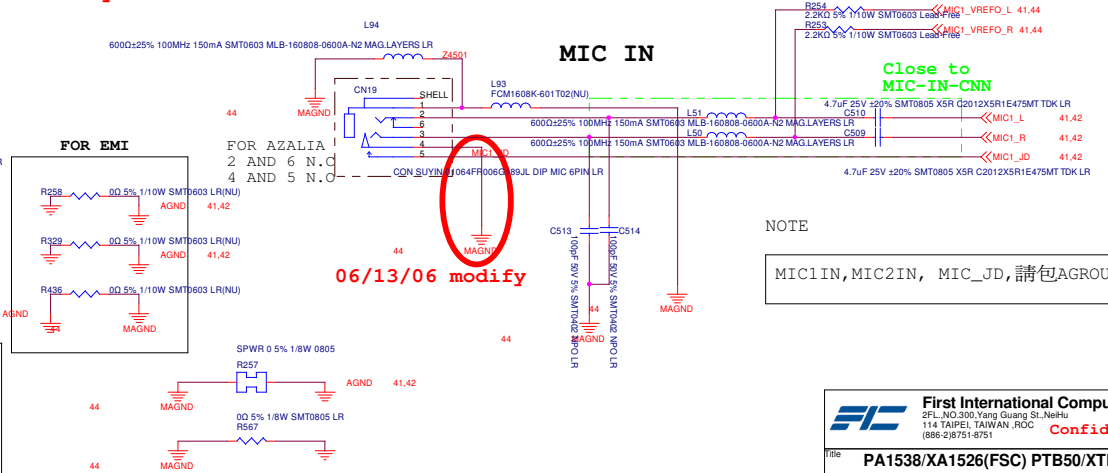
Internal array MIC



NOTE

INMIC_L, INMIC_R, MIC_JD, 請包AGROUND

MIC IN

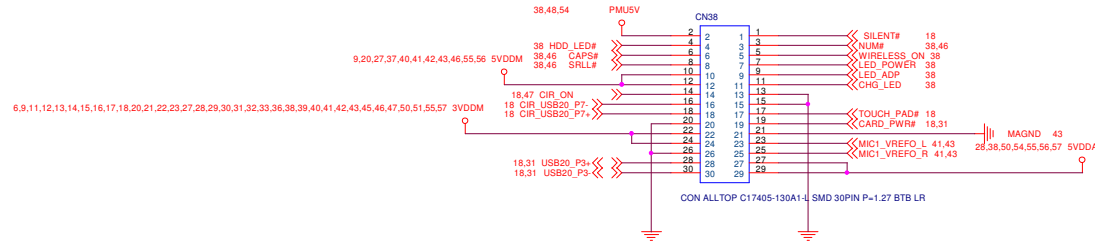


NOTE

MIC1IN, MIC2IN, MIC_JD, 請包AGROUND

Pa: No Stuff
Xa: Stuff

AUDIO B CNN



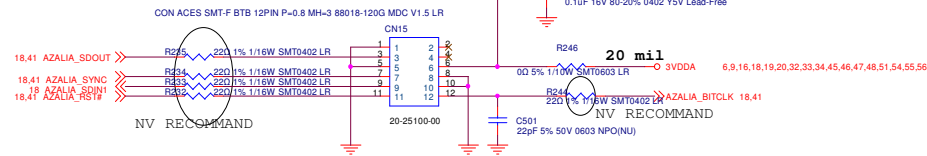
HD Audio-ACZ_SDIN (MDC Connector)



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"-15" L2 = 0.5"-1.5" L3 = 0.5"

*** Breakout can be routed 4 on 4 up to 400 mils

MDC 1.5 CNN



FOR EMI Solution



Trace:5mil, Spacing:5mil

600Ω±25% 100MHz SMT0603 MLB-160808-0600P N2 MAG.LAYERS LR

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDA

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

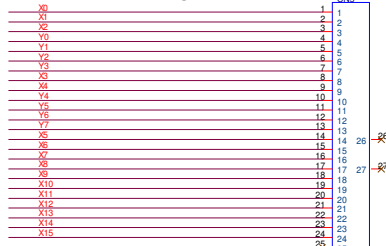
6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

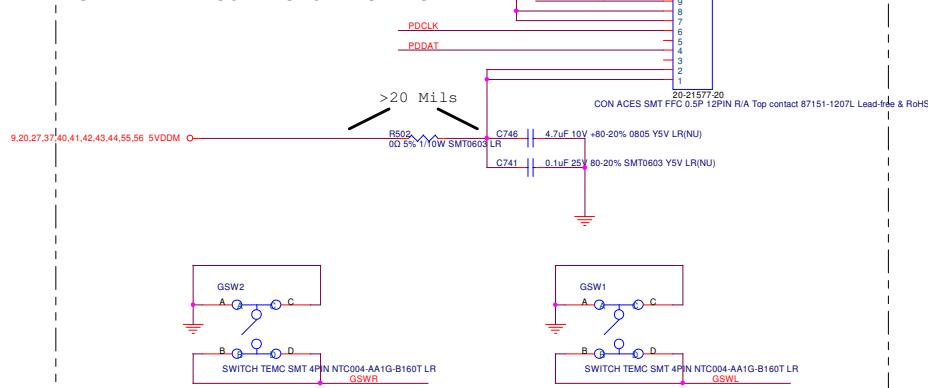
6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

6,9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57 3VDDM

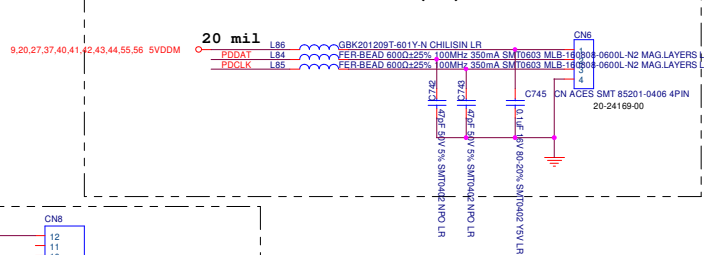
INT KB CNN



GLIDE PAD CONNECTOR For Pa



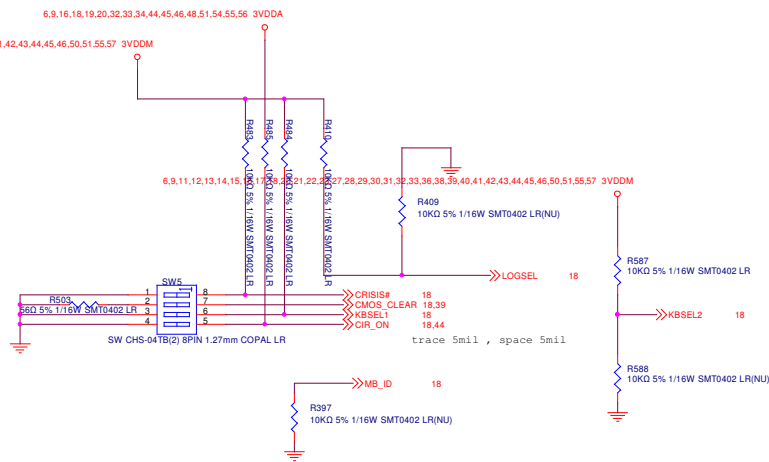
GP BPARD FFC(MB) For Xa



First International Computer, Inc.
3FL NO.300, Yang Guang St., NeiHu
114 TAIPEI, TAIWAN, ROC
(886-2)8751-8751

Confidential
Title: PA1538/XA1526(FSC) PTB50/XTB70(FIC)
Size: C Document Number: LPC KBC (M3886)
Date: Thursday, October 26, 2006 Sheet: 46 of 57

DIP SWITCH



LID Switch

