

Intel Calpella BLOCK DIAGRAM

INTEL DISCRETE SYSTEM DIAGRAM 01

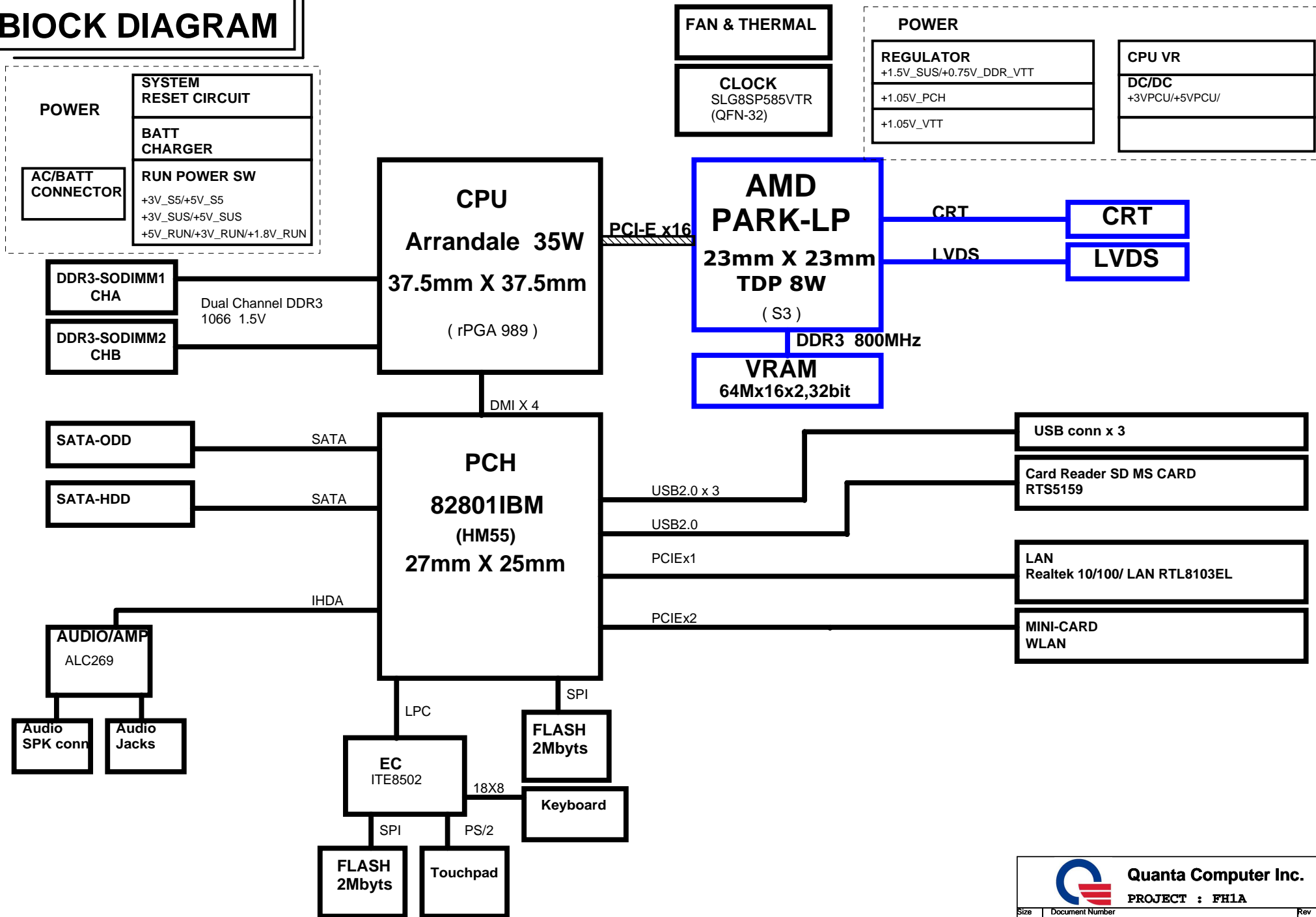
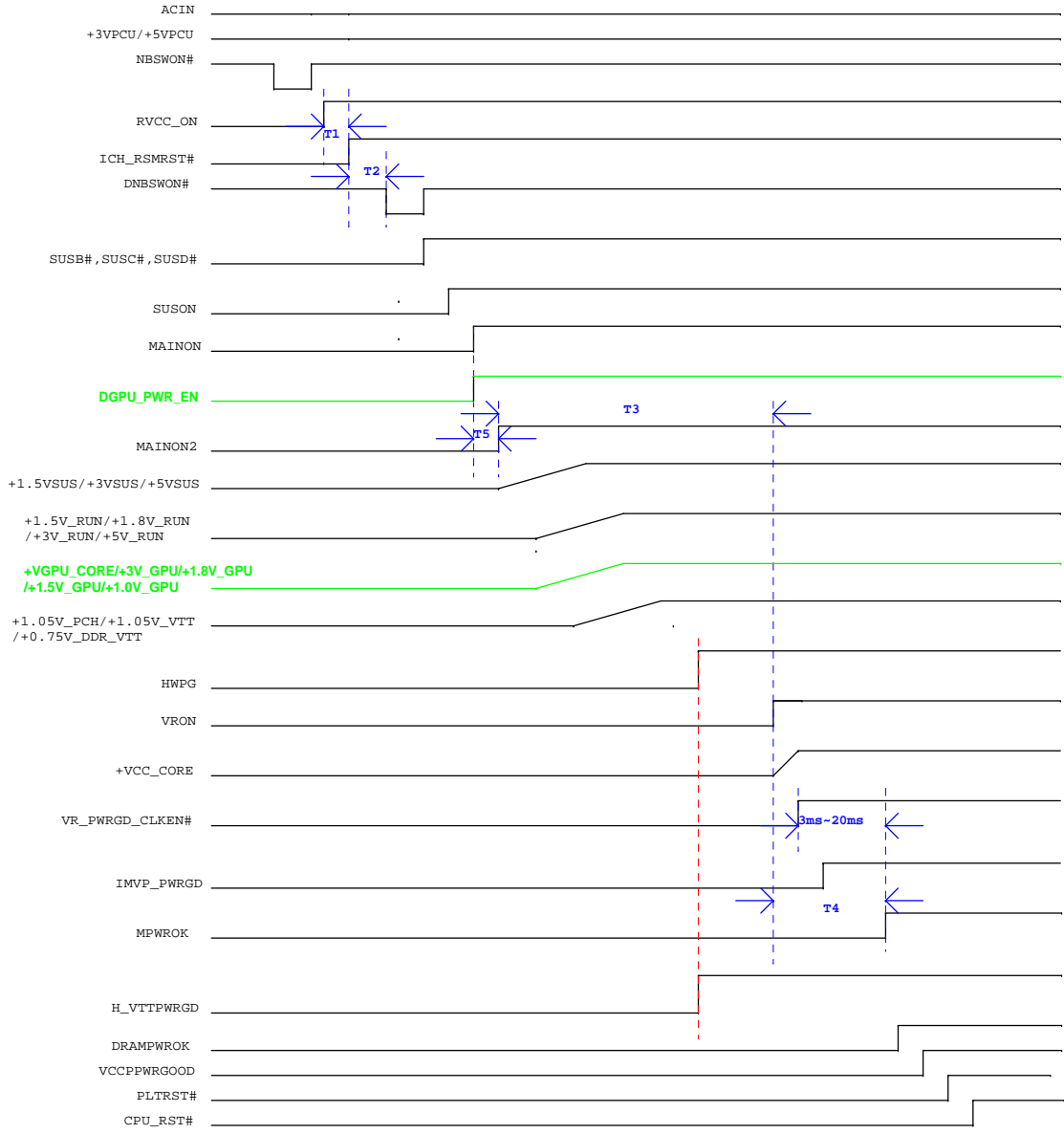



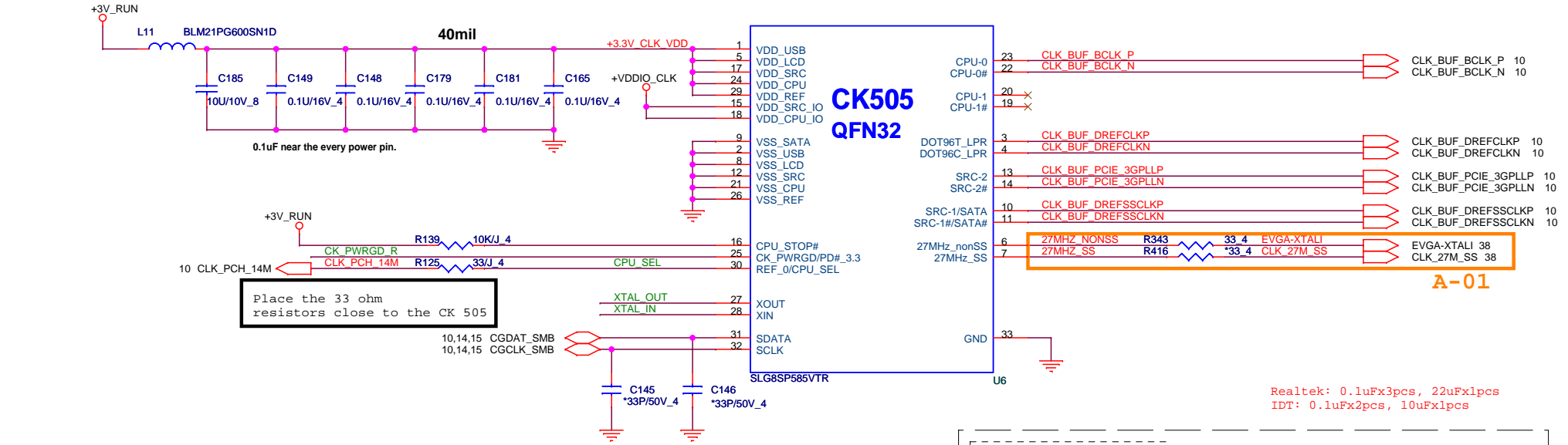
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42	PARK_VRAM (DDR3 BGA96)
43	+VGACORE (RT8208/1.8V)
44	+1.5V_VGA/+1.0V_VGA

Power Sequence



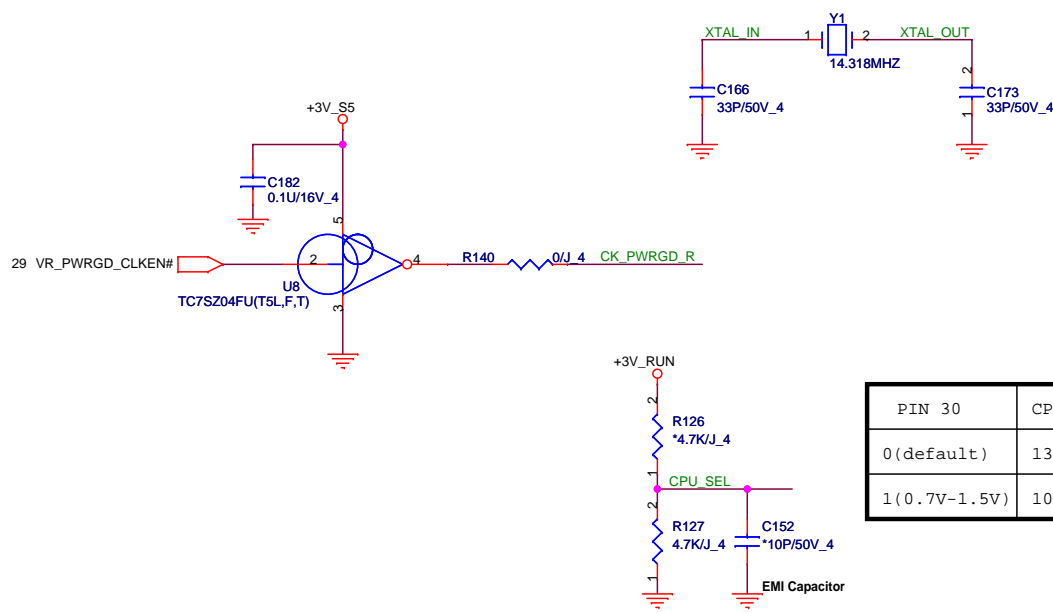
T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us


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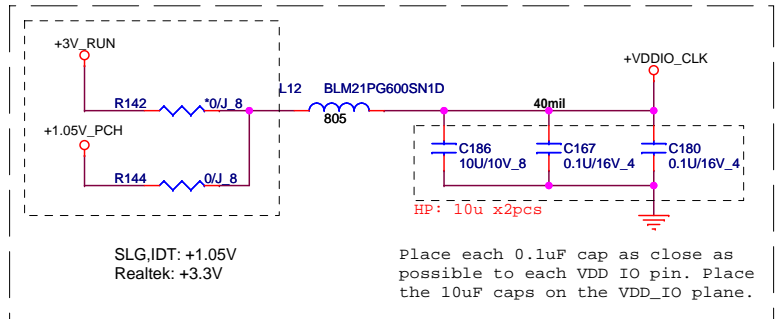


Place the 33 ohm resistors close to the CK 505

Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz



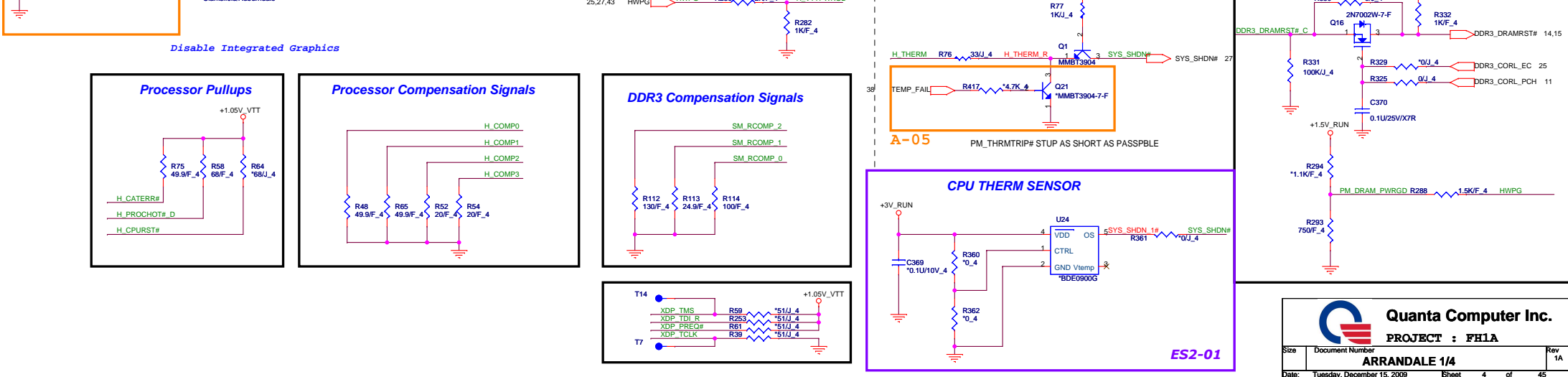
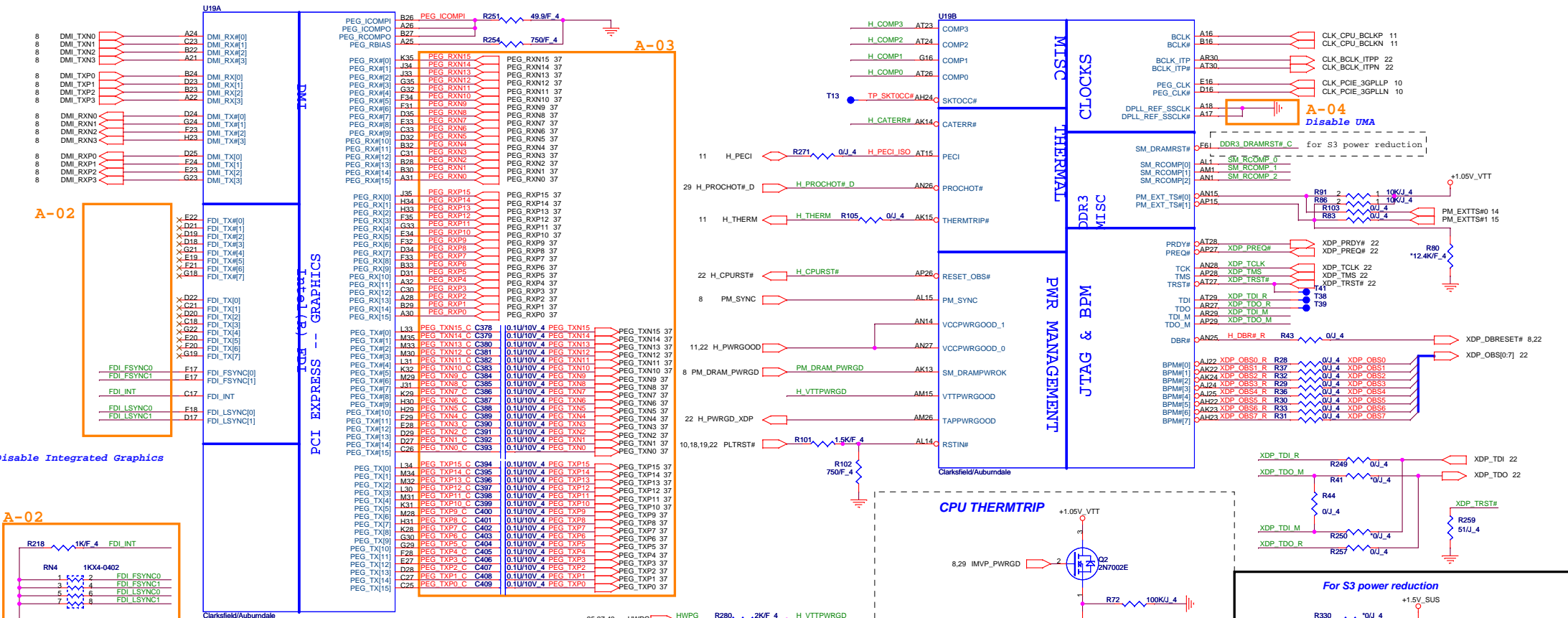
Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

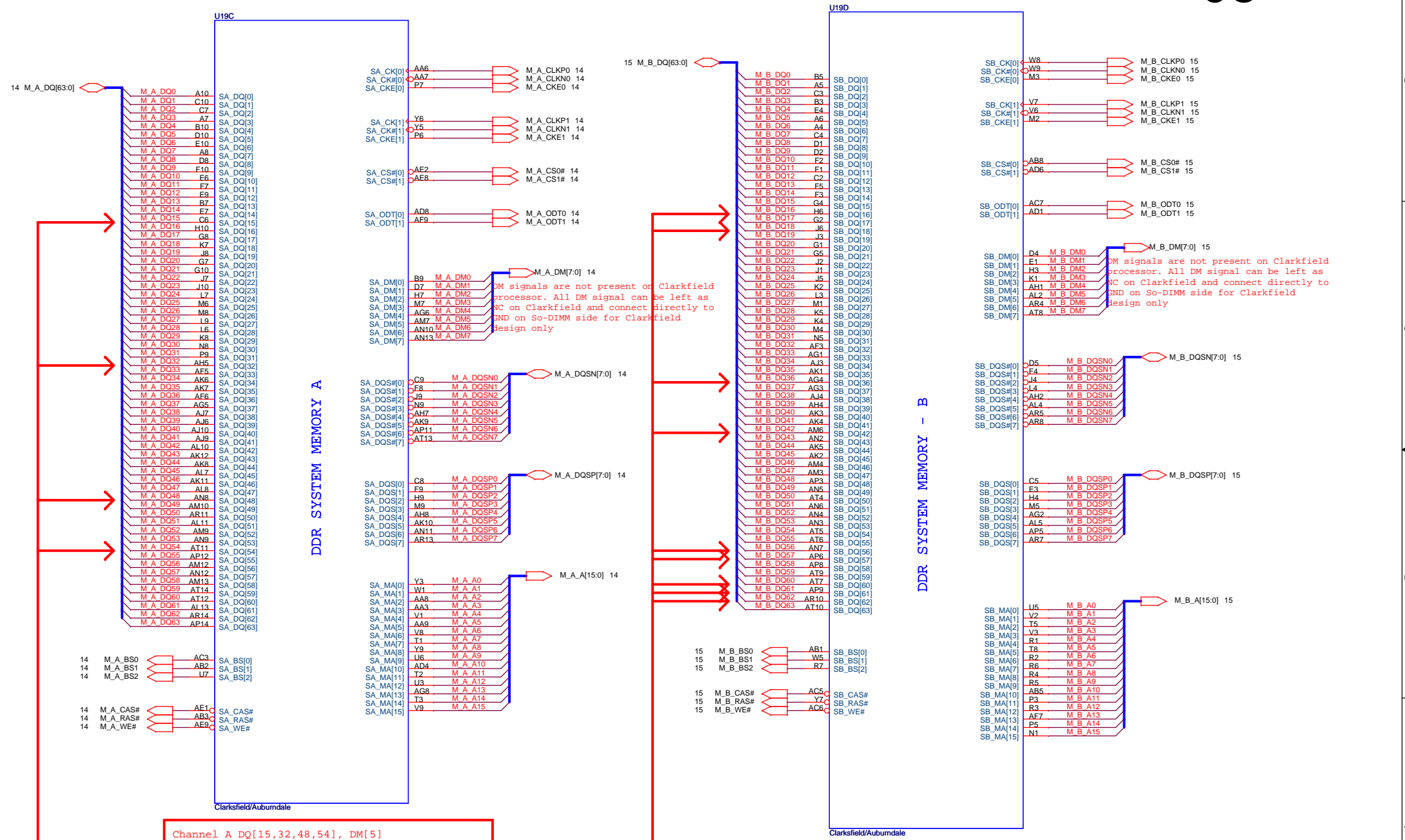
+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V!
Realtek date sheet(V1.2) P11: Min 1.05V, Max 3.3V!
IDT date sheet(V0.7) P10: Min 0.9975V, Max 3.465V!

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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Clock Generator		
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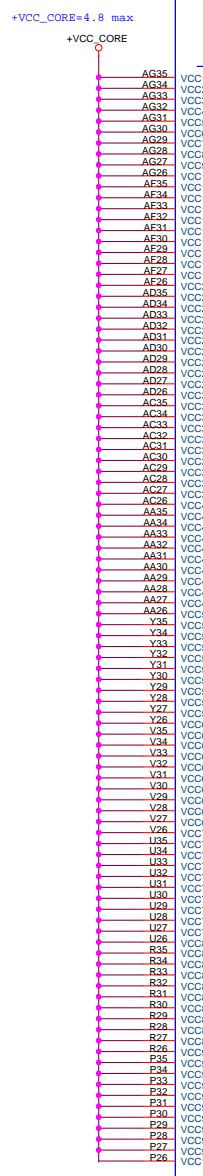
Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

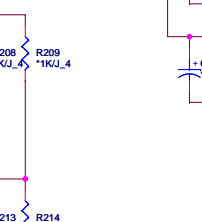
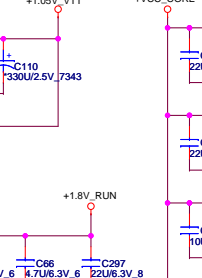
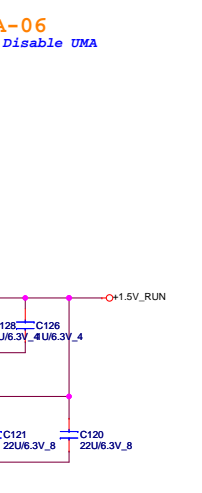
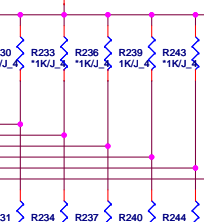
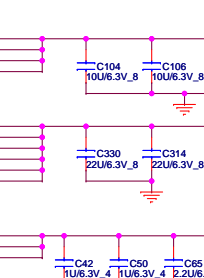
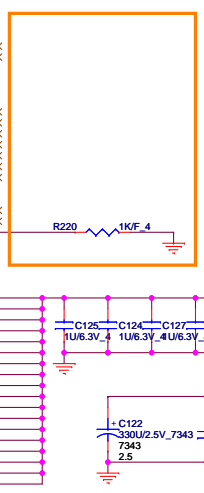
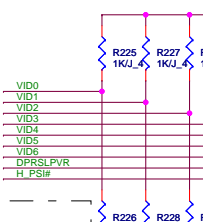
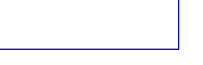
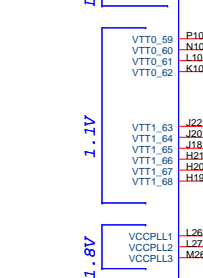
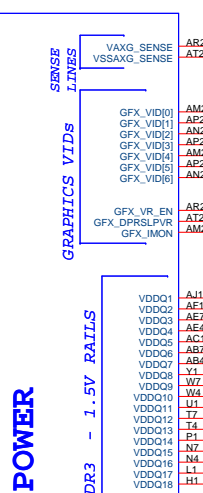
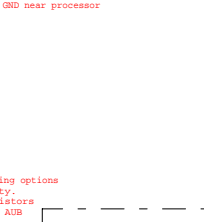
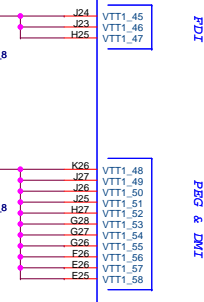
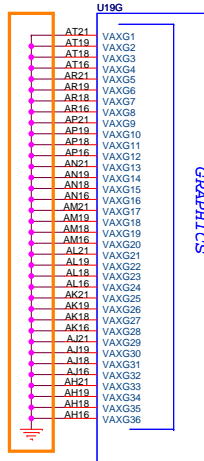


ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU Core Power U19F



AUBURDALE/CLARKSFIELD PROCESSOR (POWER)



For S3 power reduction

Check to ensure that 4 switching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors - caps should be evenly distributed between the connectors

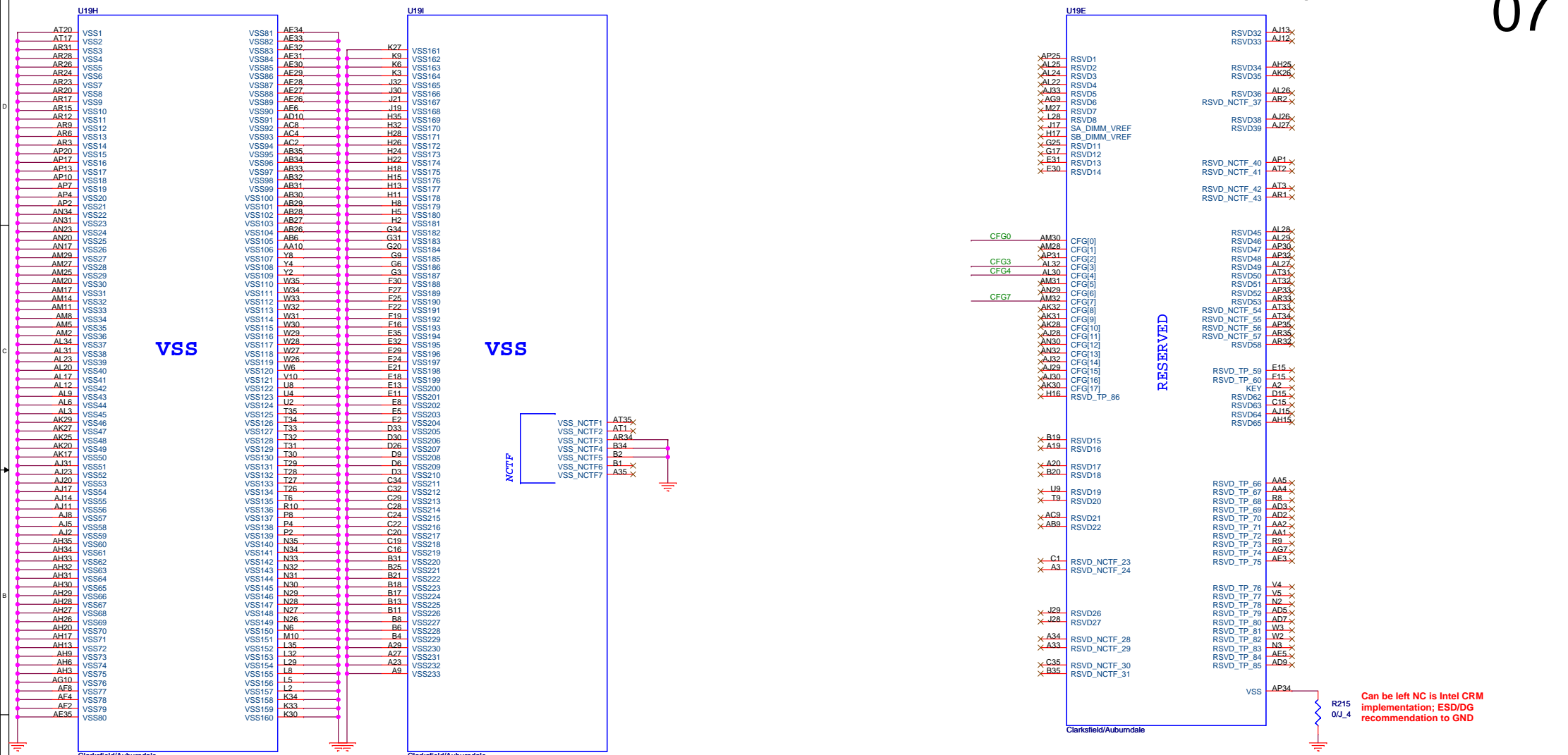
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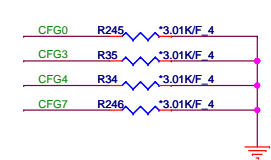
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ARRANDALE PROCESSOR (GND)


ARRANDALE PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



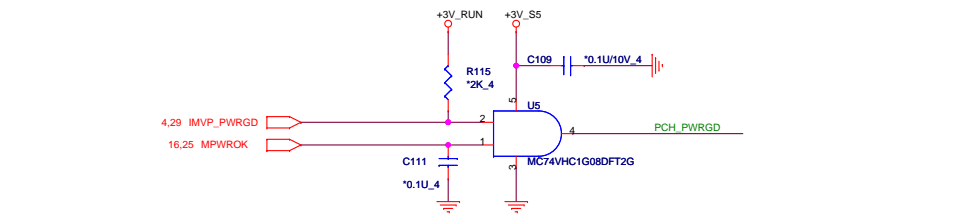
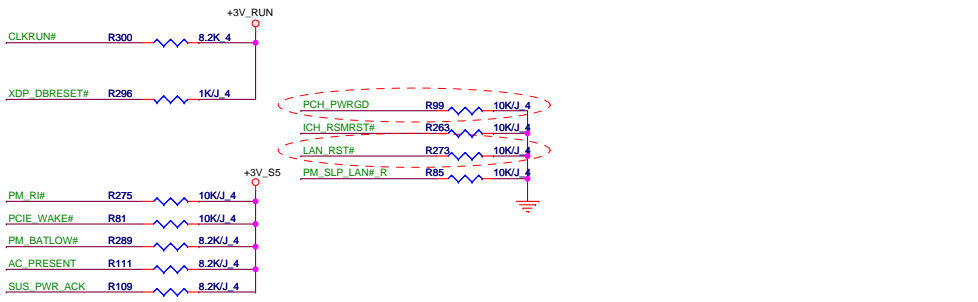
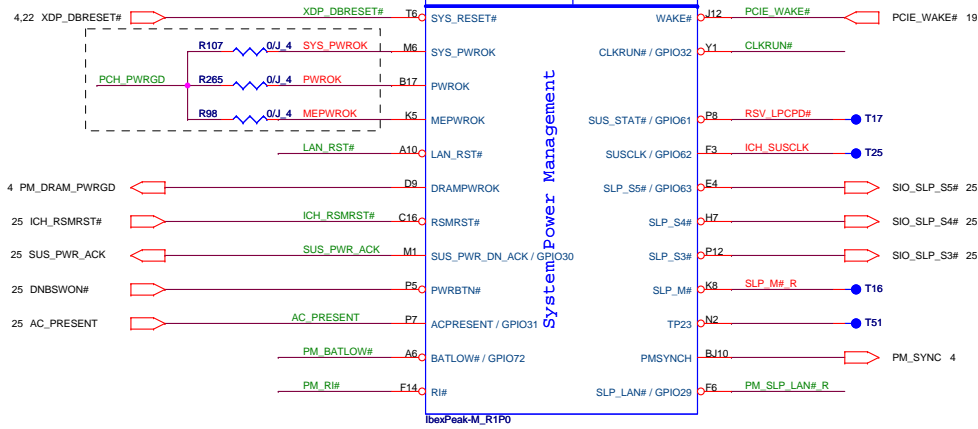
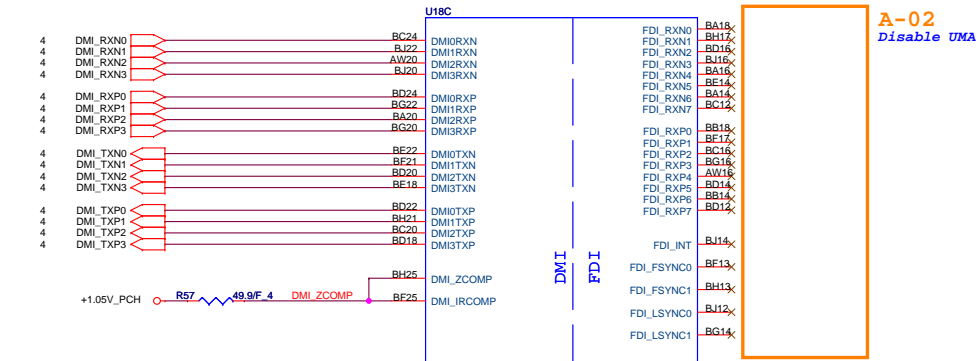
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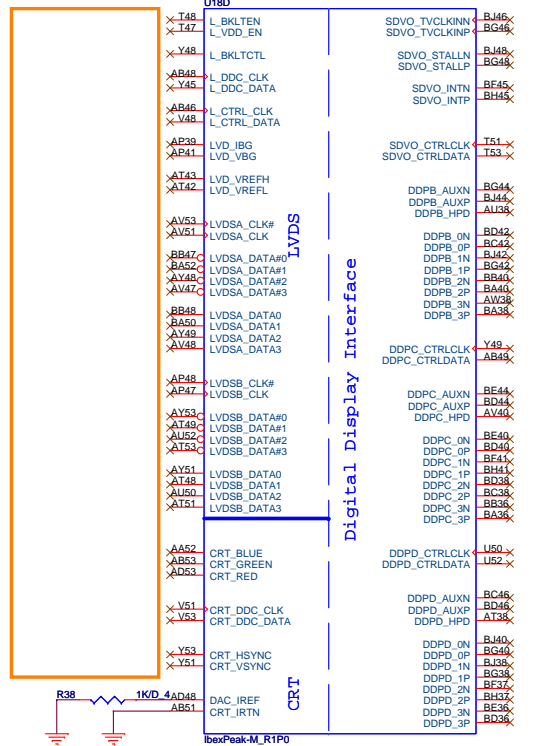
Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

IBEX PEAK-M (DMI,FDI,GPIO)

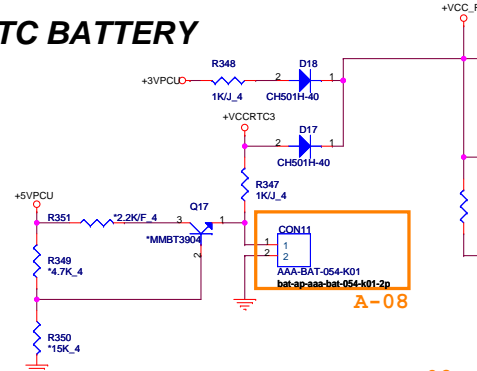
IBEX PEAK-M (LVDS,DDI)



A-07



RTC BATTERY



A-08

A-09

INTVRMEN[Internal Voltage Regulator Enable] :
 This signal enables the internal 1.05 V regulators.
 This signal must be always pulled-up to VccRTC.

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

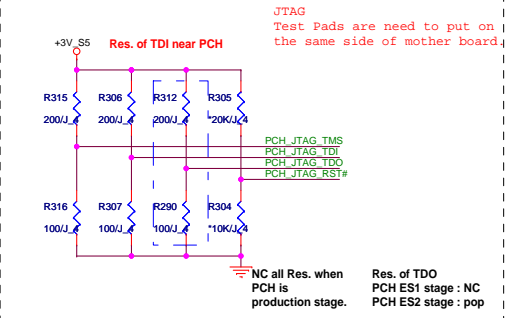
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

No Reboot strap.

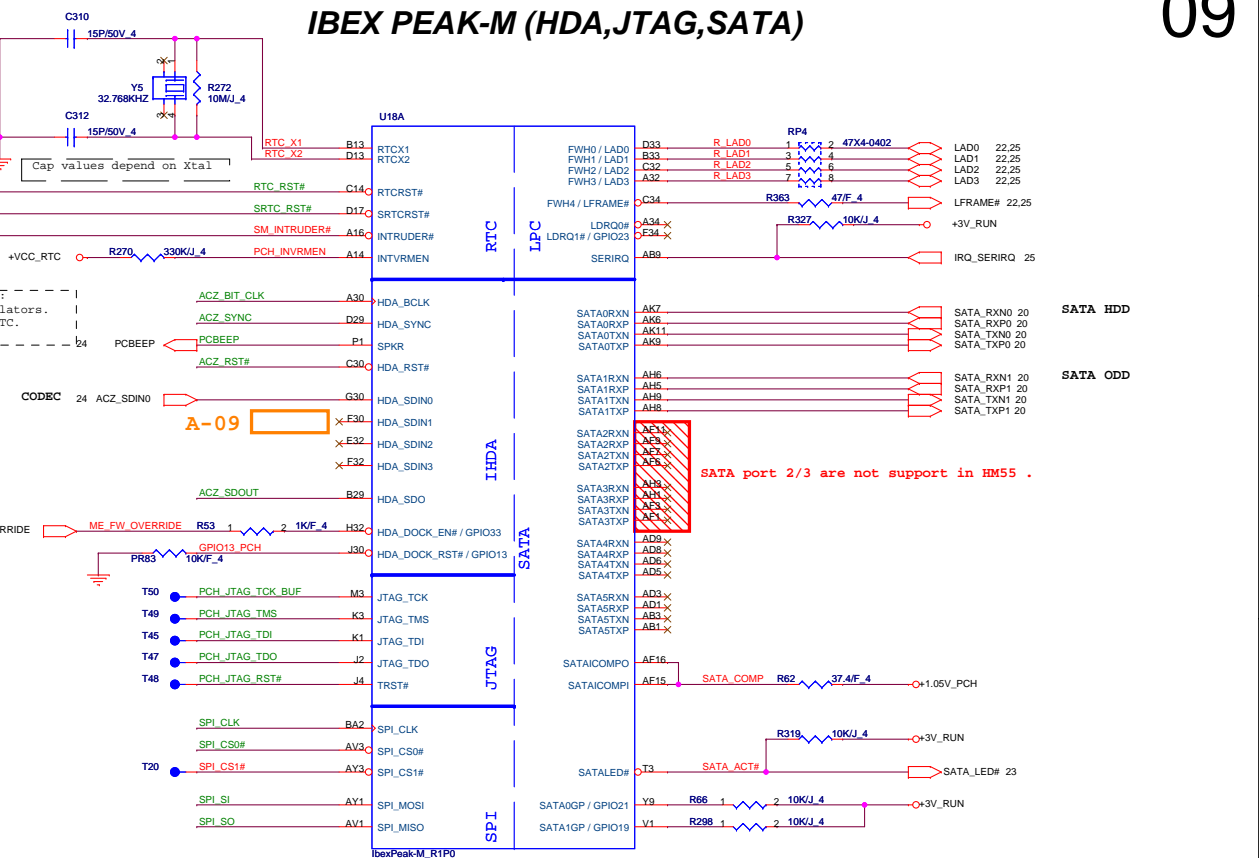
PCBEEP	Low = Default. High = No Reboot.
--------	-------------------------------------



Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

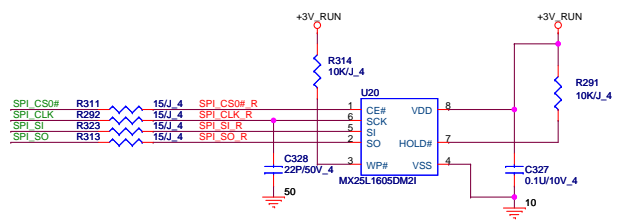
IBEX PEAK-M (HDA, JTAG, SATA)

09

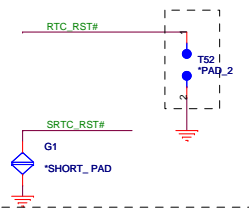


SATA port 2/3 are not support in HM55 .

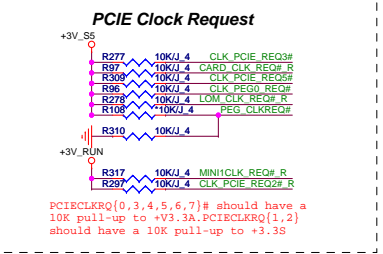
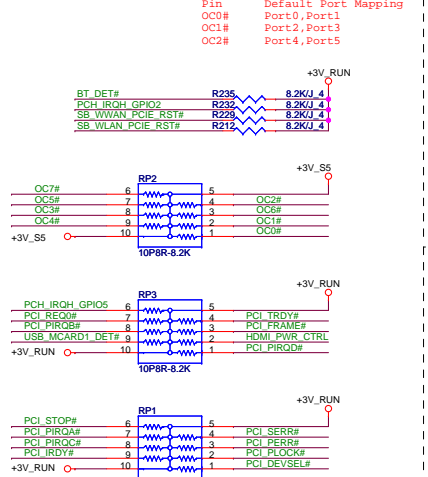
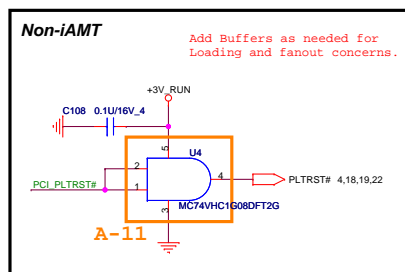
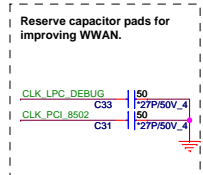
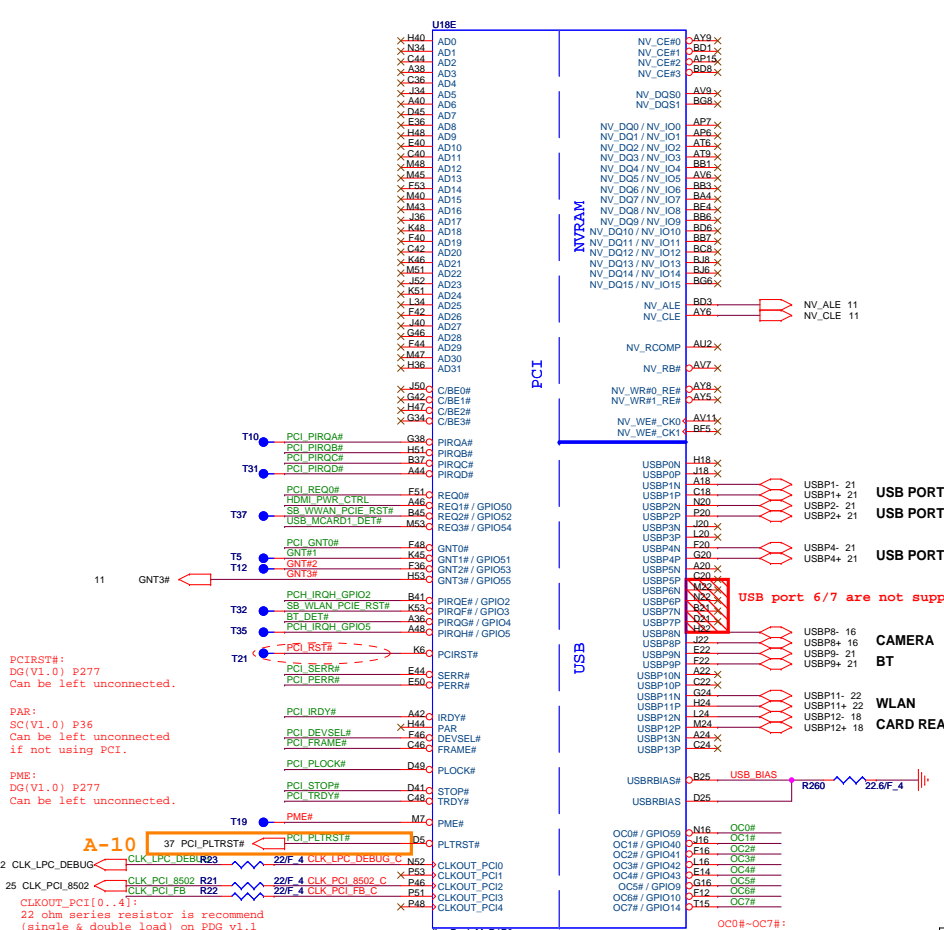
For PCH 32Mbit (4M Byte)



RESET JUMP (Near ROOM DOOR)



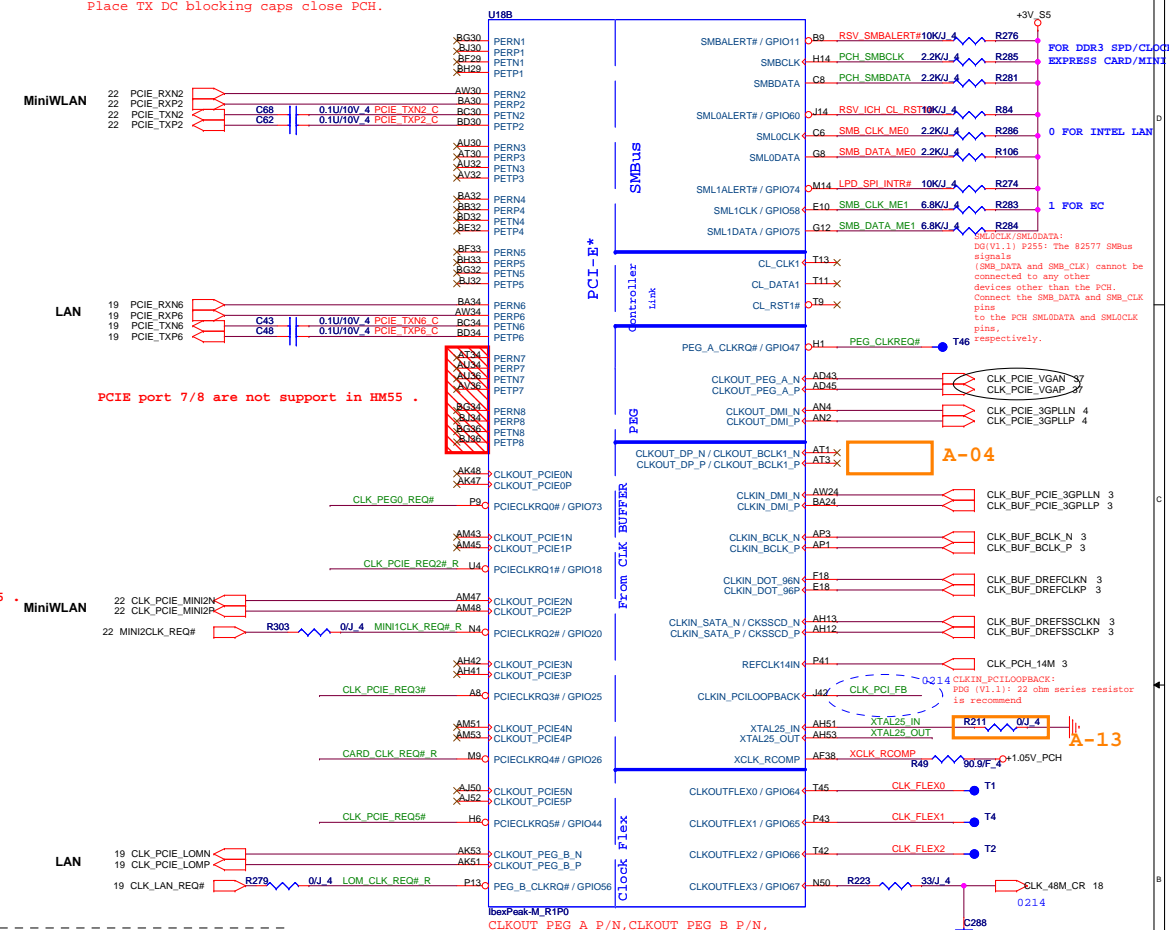
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Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

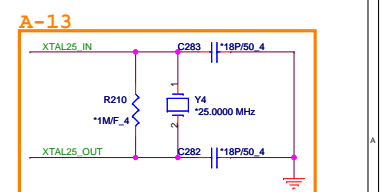
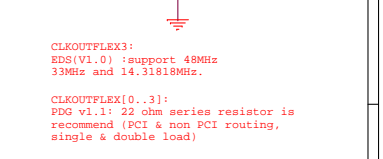
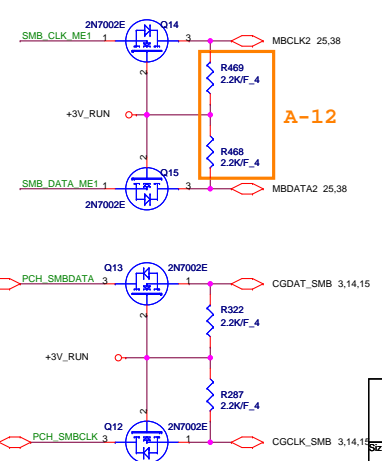
Place TX DC blocking caps close PCH.



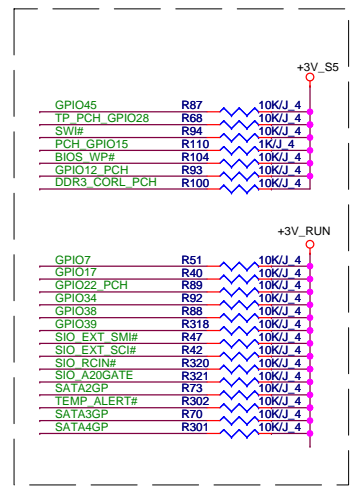
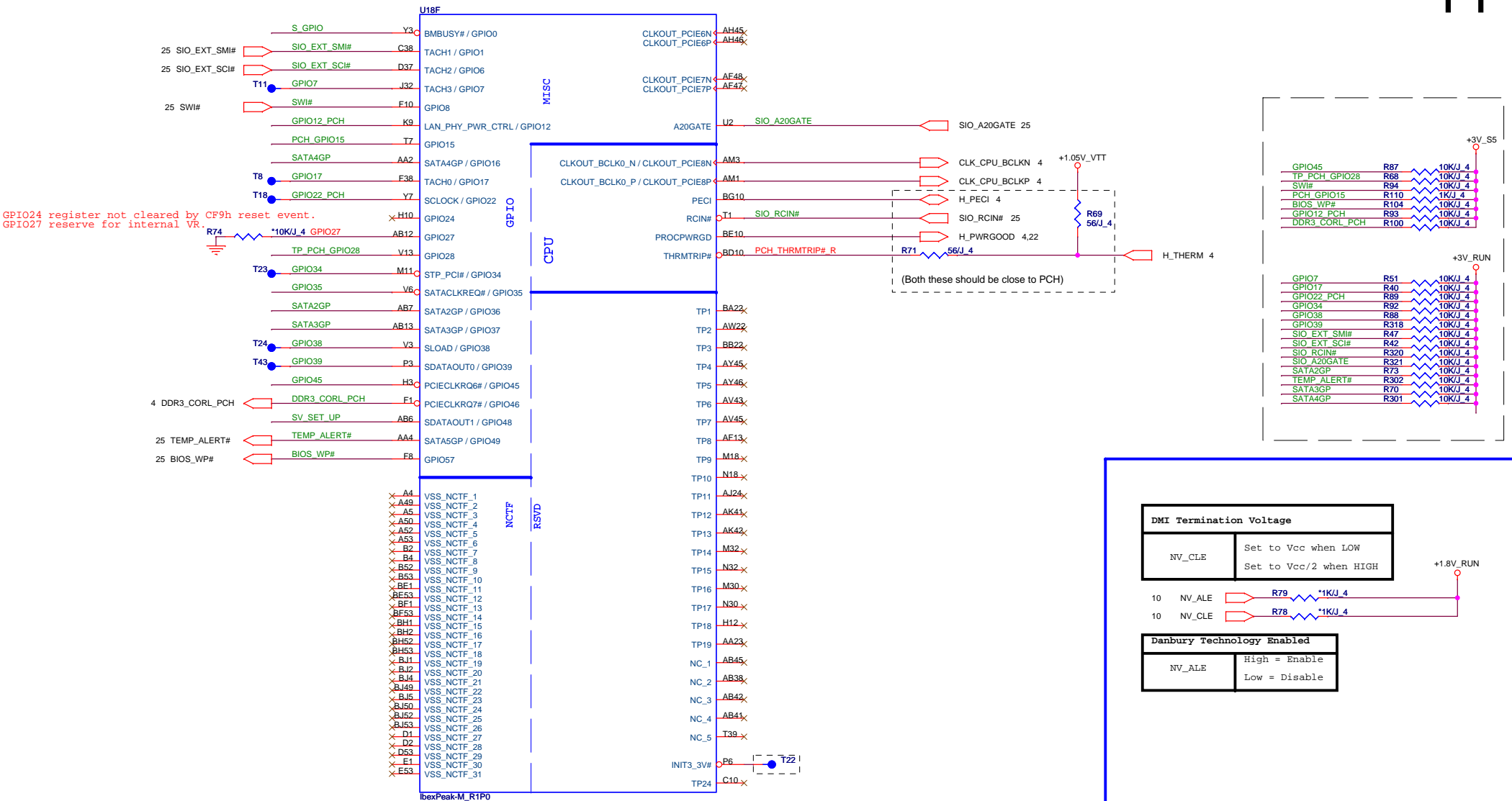
PCI-E port 7/8 are not support in HM55.

USB port 6/7 are not support in HM55.

ibexPeak-M_R1P0
CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N, CLKOUT_DMI_P/N,support GEN-1 and GEN-2

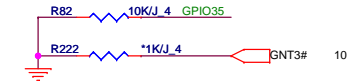
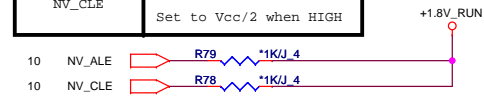


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

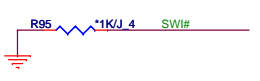


DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW
	Set to Vcc/2 when HIGH

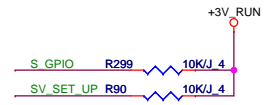
Danbury Technology Enabled	
NV_ALE	High = Enable
	Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high



SV_SET_UP	1-X High = Strong (Default)
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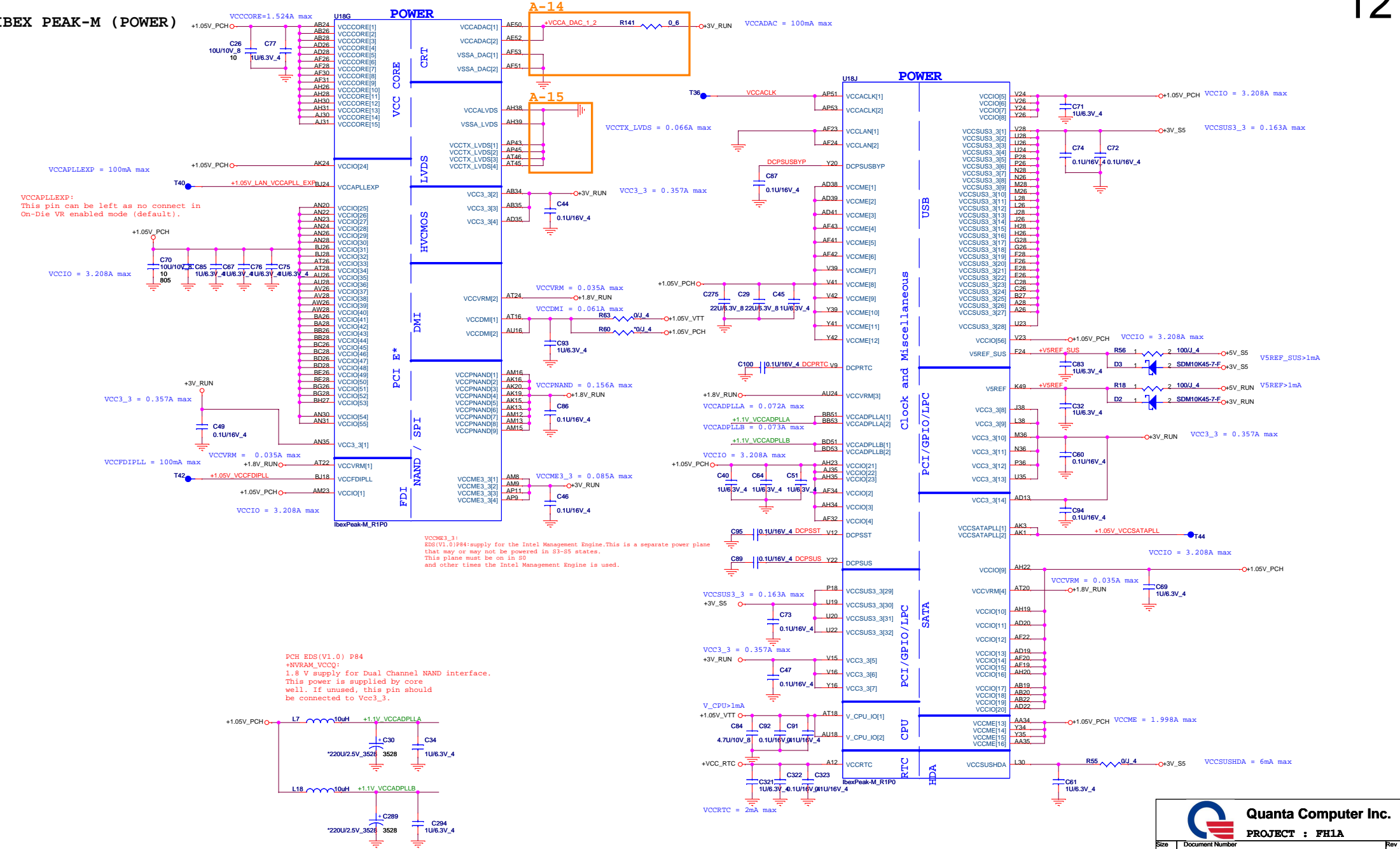
BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

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IBEX PEAK-M (POWER)



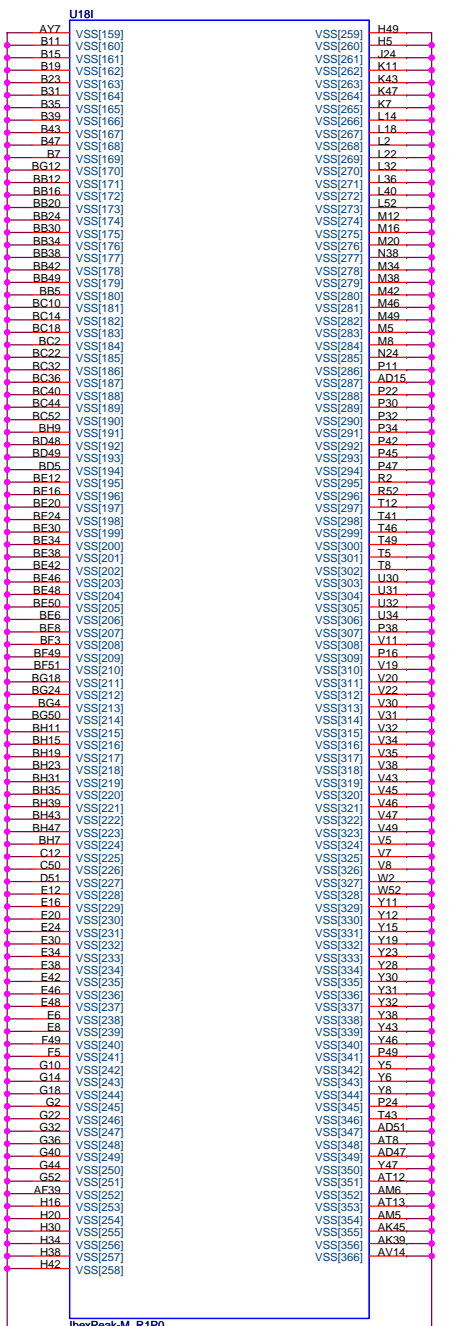
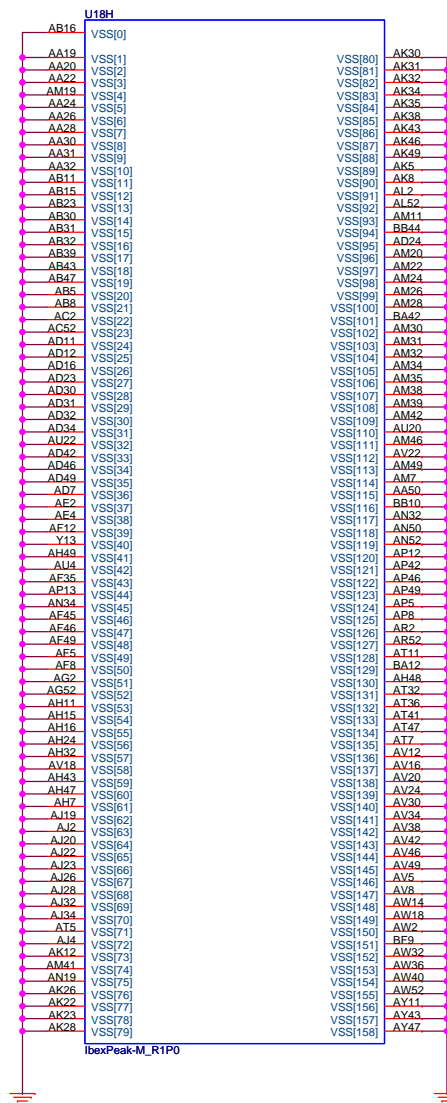
VCCAPLLEXP: This pin can be left as no connect in On-Die VR enabled mode (default).


PCH EDS(V1.0) P84
 +NVRAM_VCCIO:
 1.8 V supply for Dual Channel NAND interface.
 This power is supplied by core well. If unused, this pin should be connected to Vcc3_3.

VCCME3_3:
 ESD(V1.0)P84: supply for the Intel Management Engine. This is a separate power plane that may or may not be powered in S3-S5 states. This plane must be on in S0 and other times the Intel Management Engine is used.

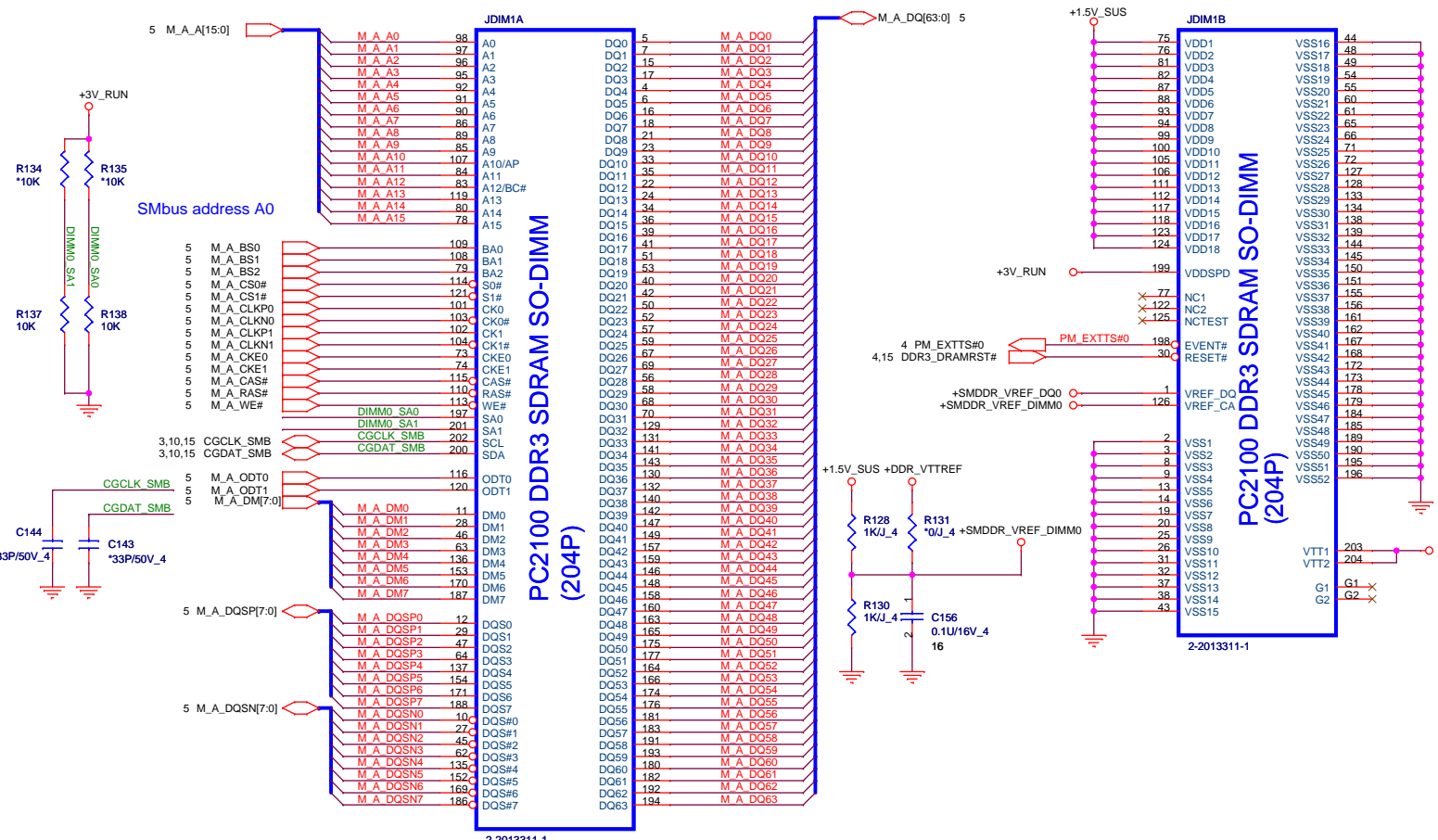
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IBEX PEAK-M (GND)



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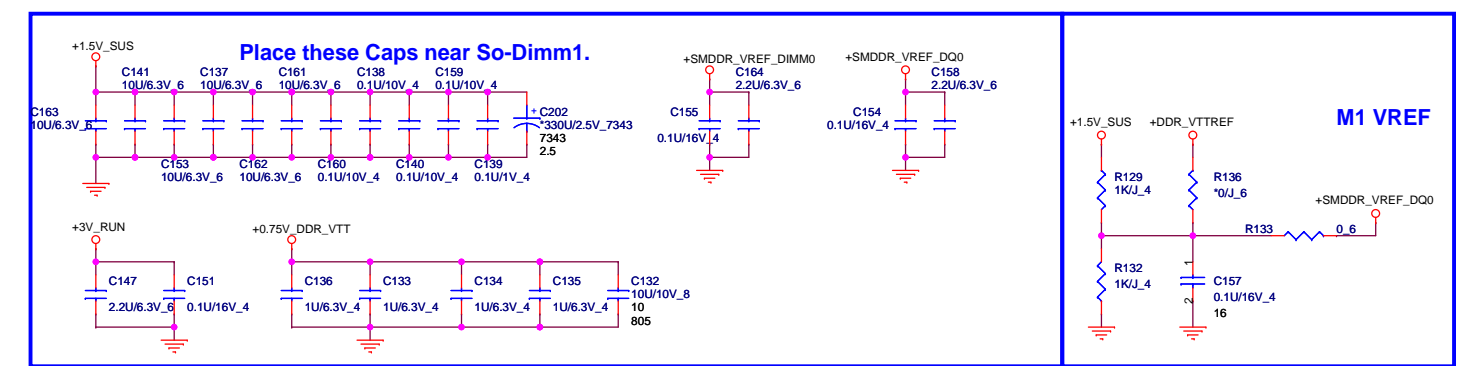


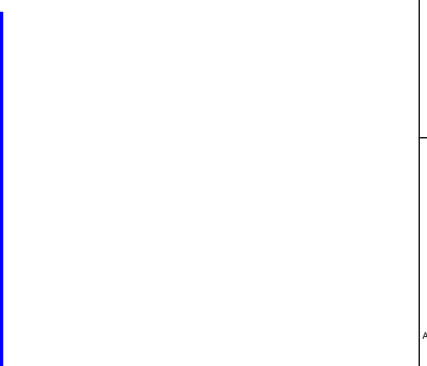
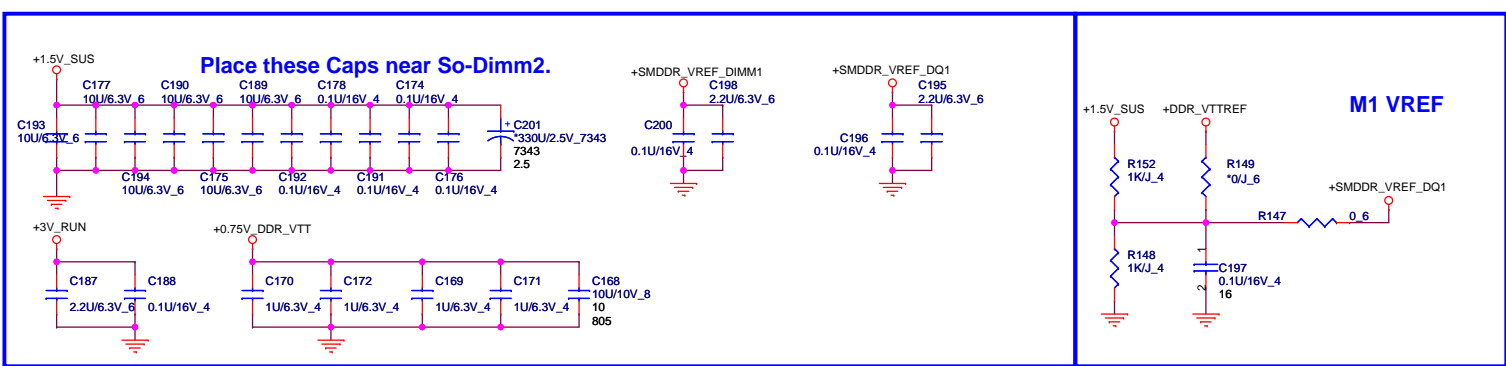
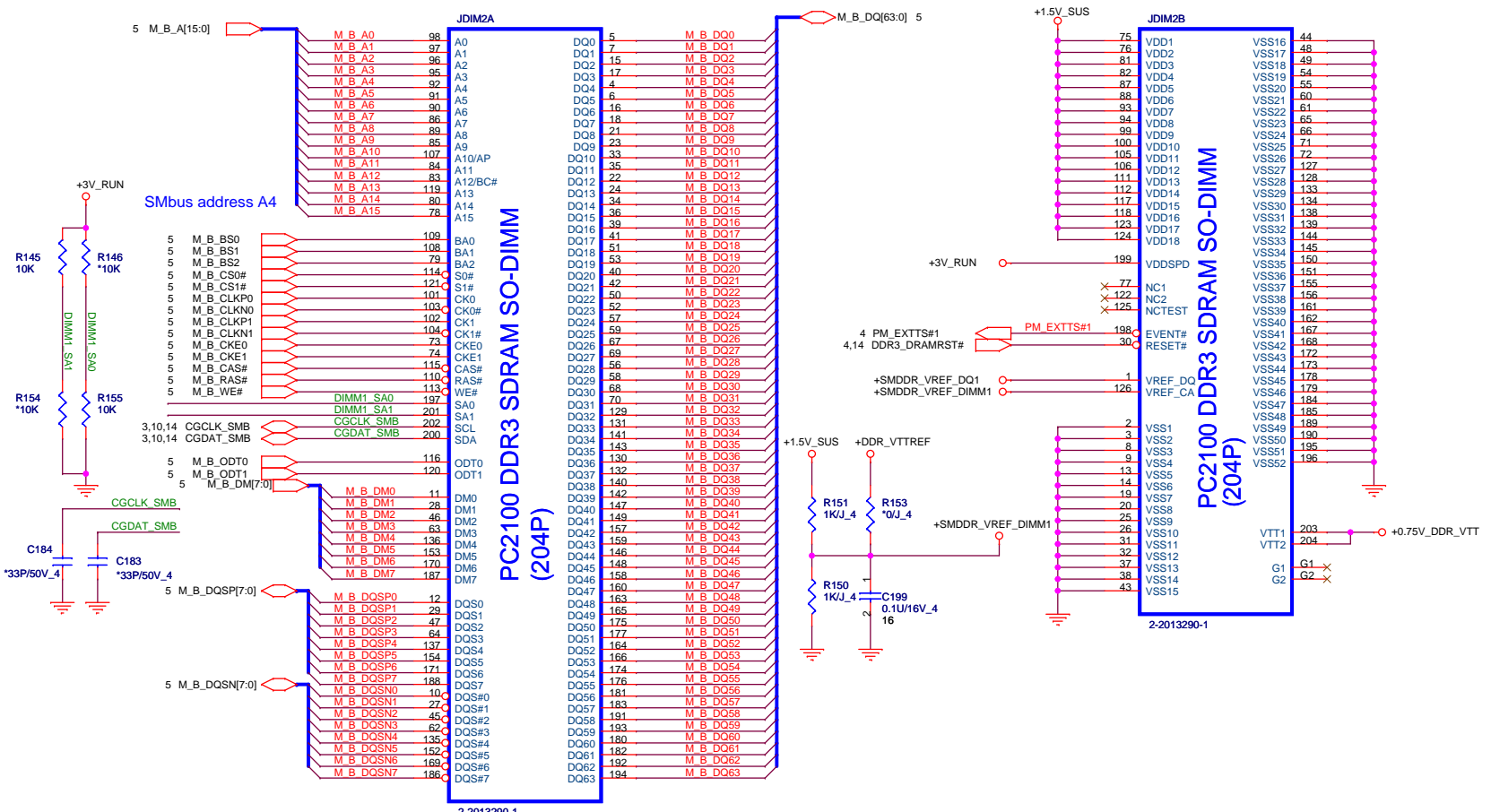
Intel is requesting that customers implement all methods (M1 and M2 and M3) described below to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms, for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1: Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref

M2: A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.

M3: Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.

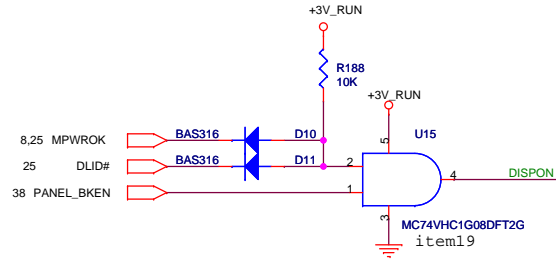




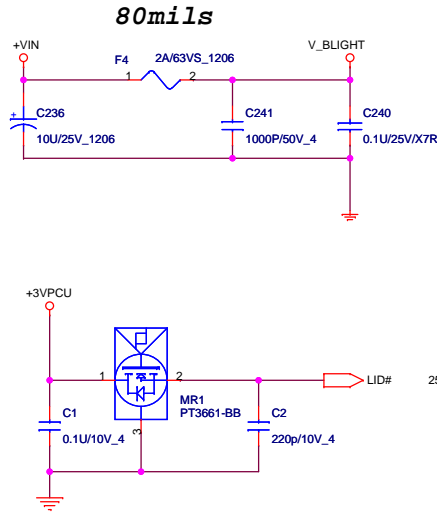
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	DDR3 DIMM-2	1A
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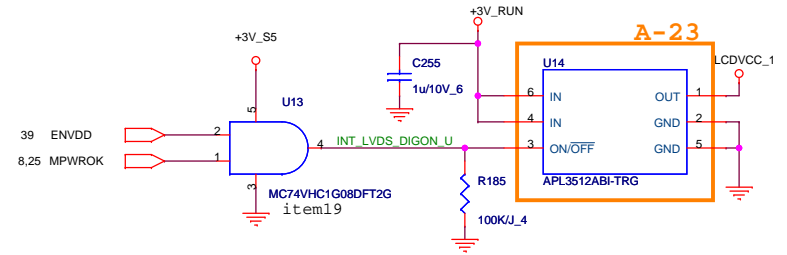
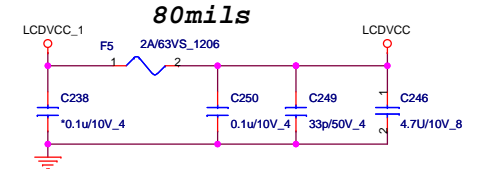
Backlight Control(LDS)



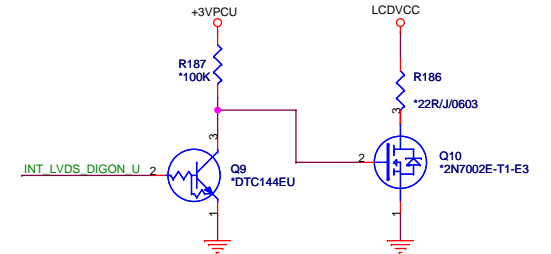
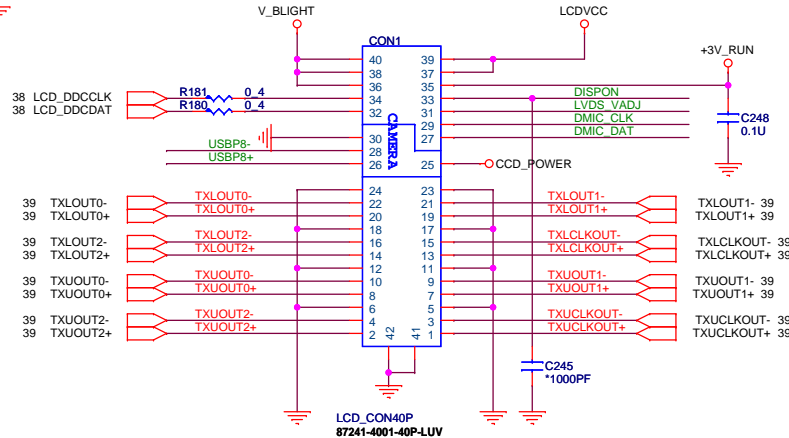
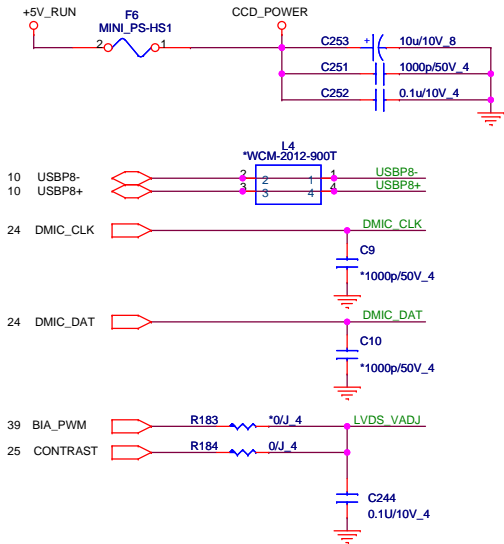
BACKLIGHT POWER




LED Panel POWER SWITCH(LVDS) 16



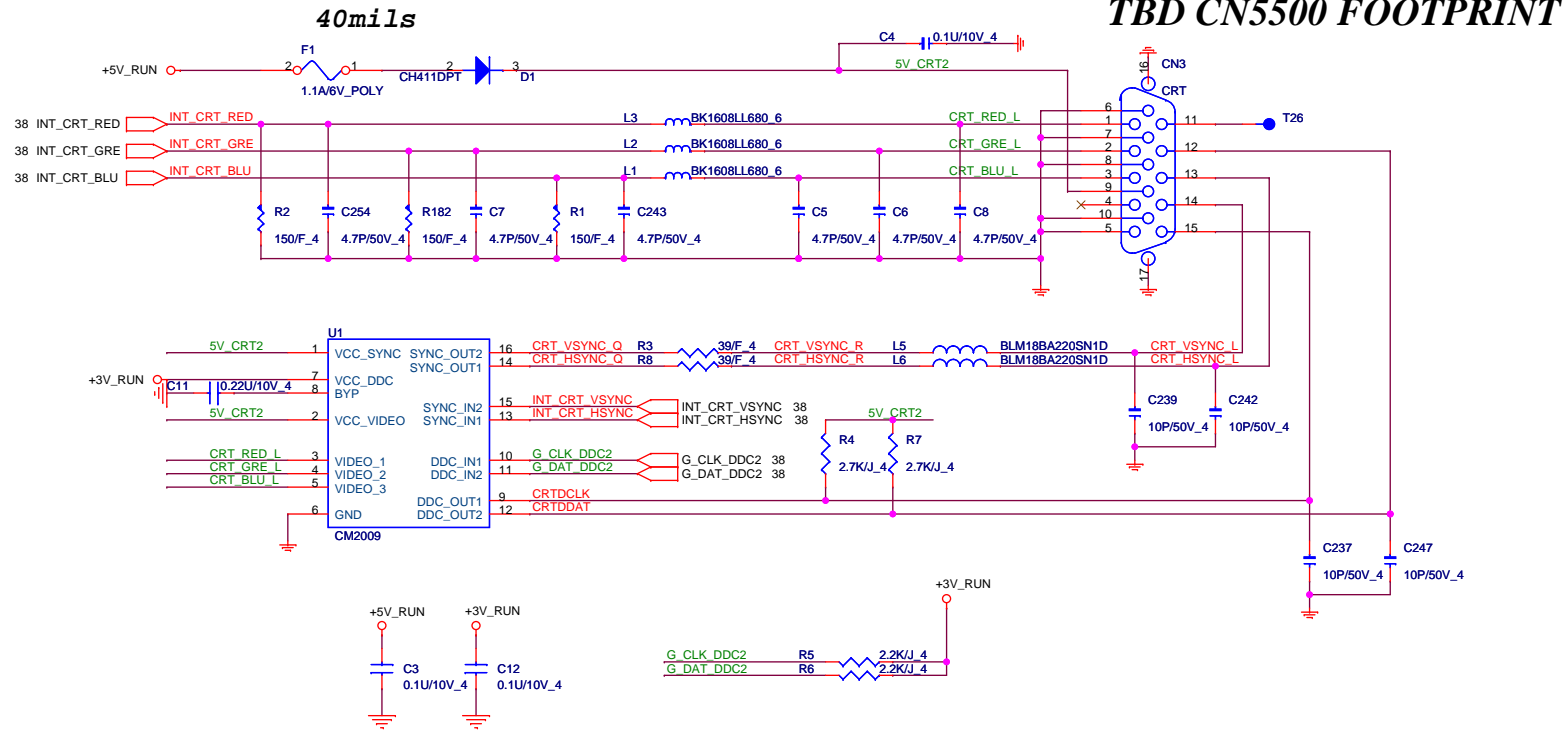
LVDS/CCD



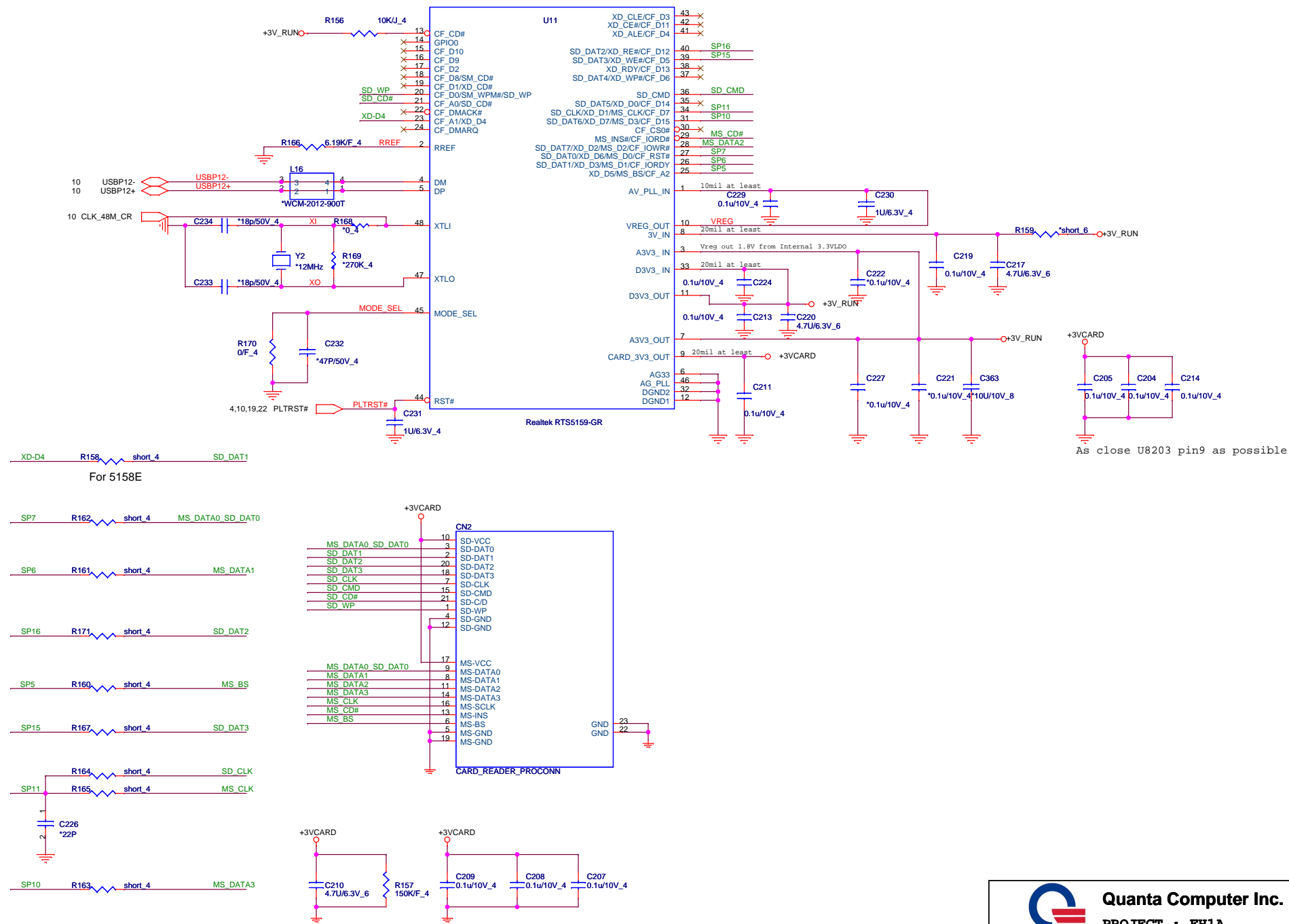

Quanta Computer Inc.
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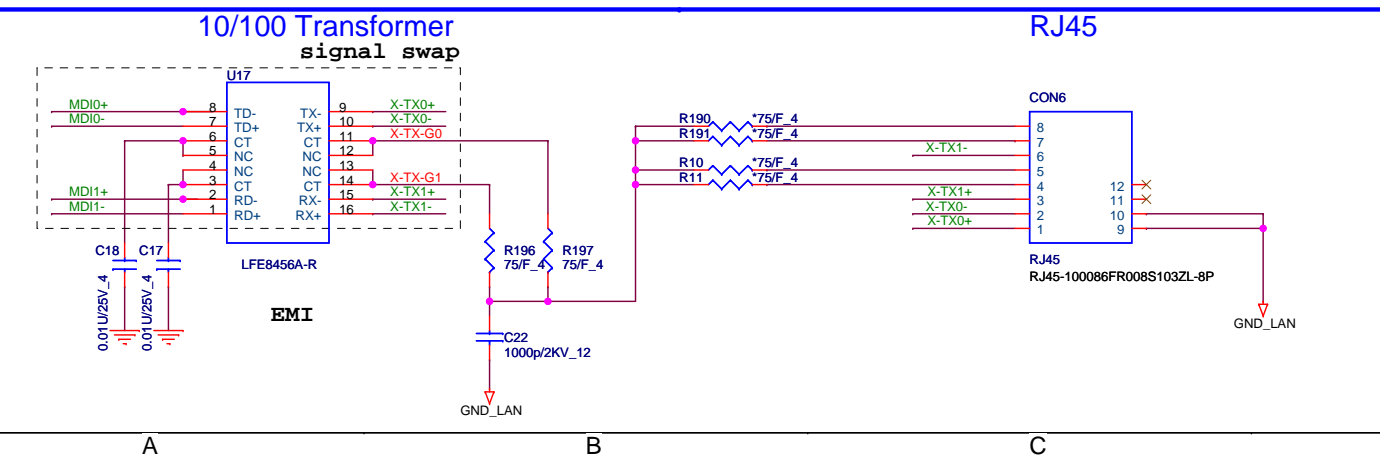
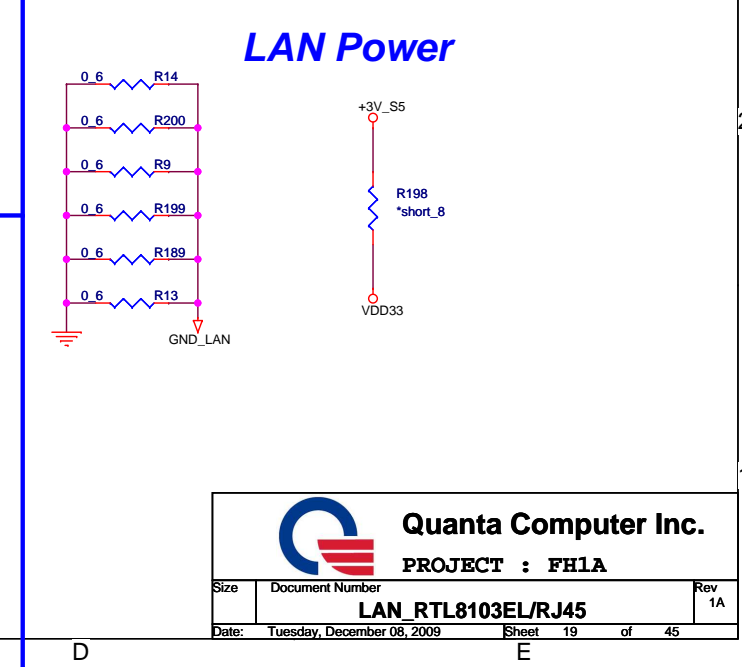
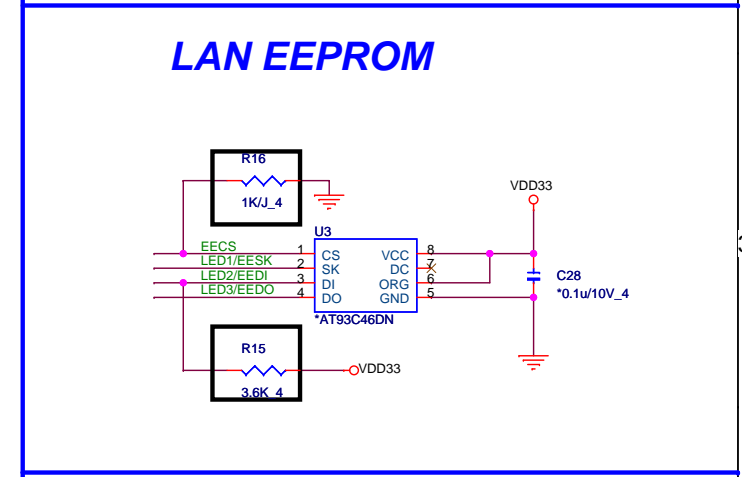
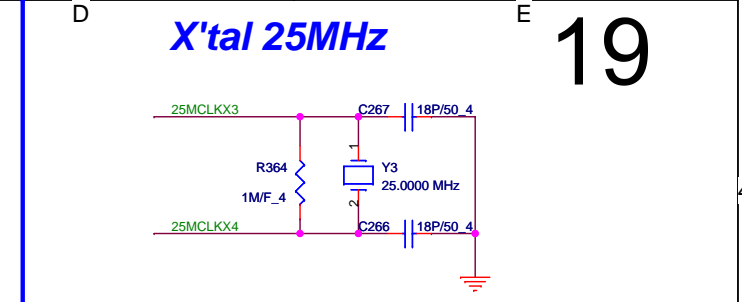
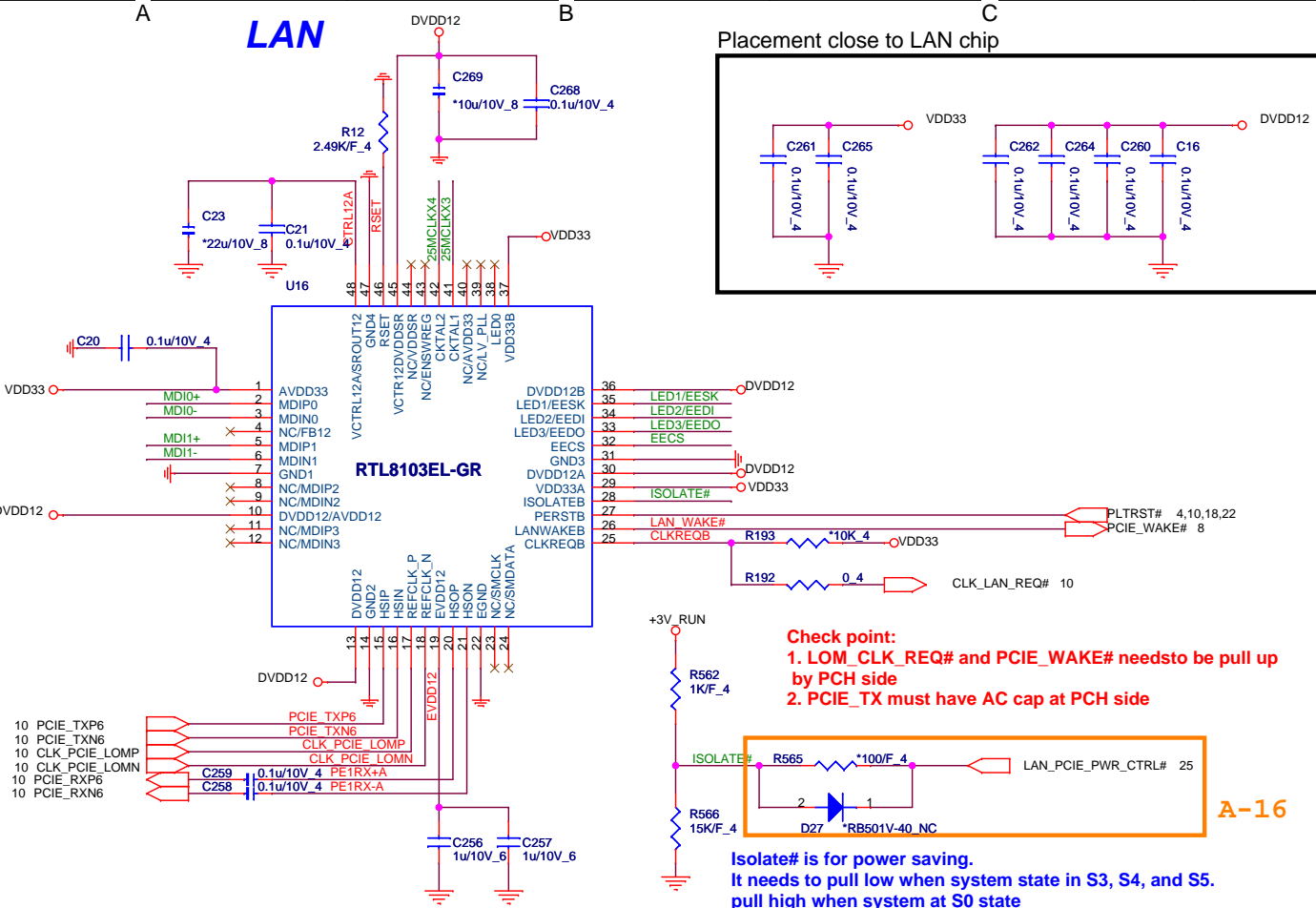
CRT CONN/DDC LEVEL SHIFT



Card Reader

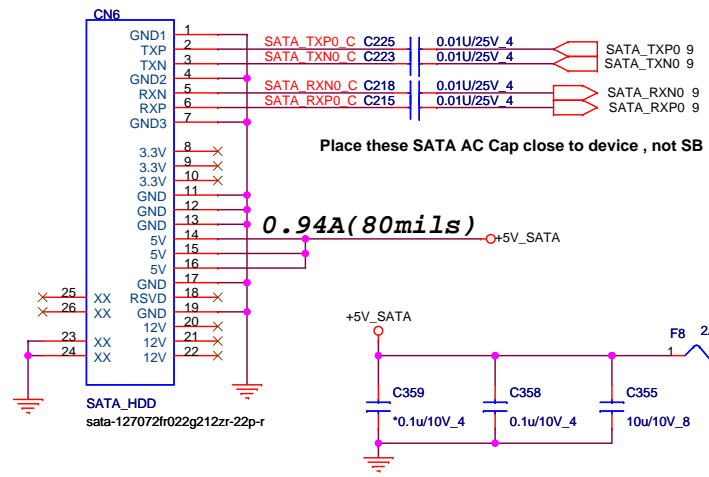


As close U8203 pin9 as possible



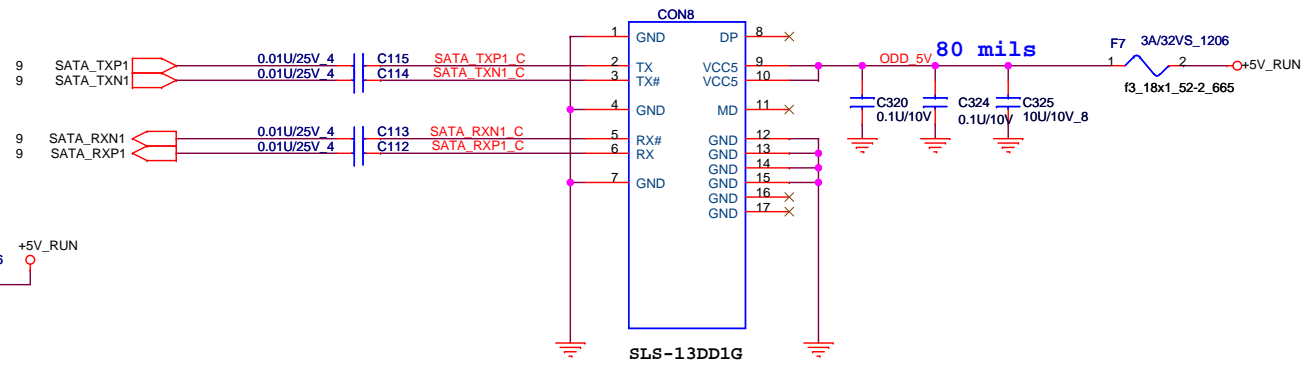
Quanta Computer Inc.
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2.5" SATA HDD



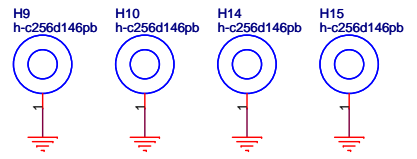
SATA ODD

ODD CONN

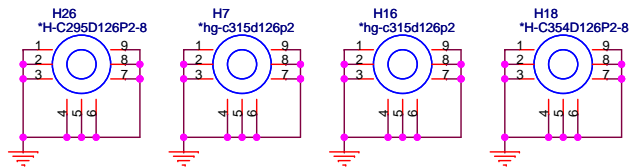


Hole

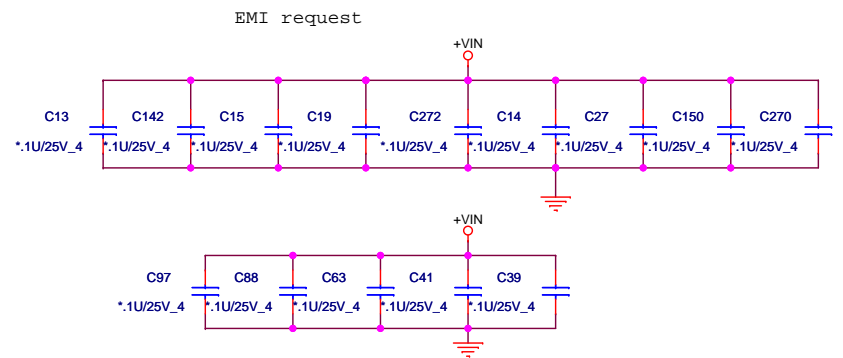
CPU Nut



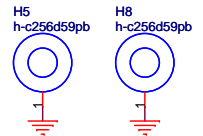
Hole for ESD



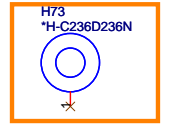
Decoupling Cap



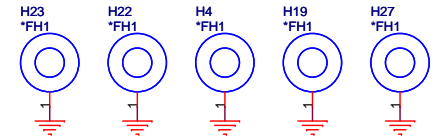
MINI CARD



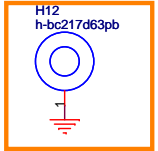
Antenna Hole



A-28

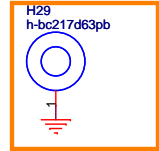


Thermal Module



A-28

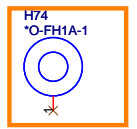
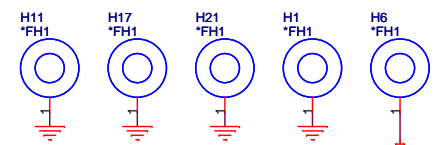
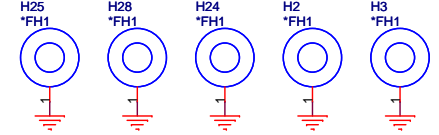
VGA Nut



A-28

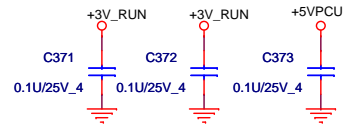
A-17

Fan Hole



A-28

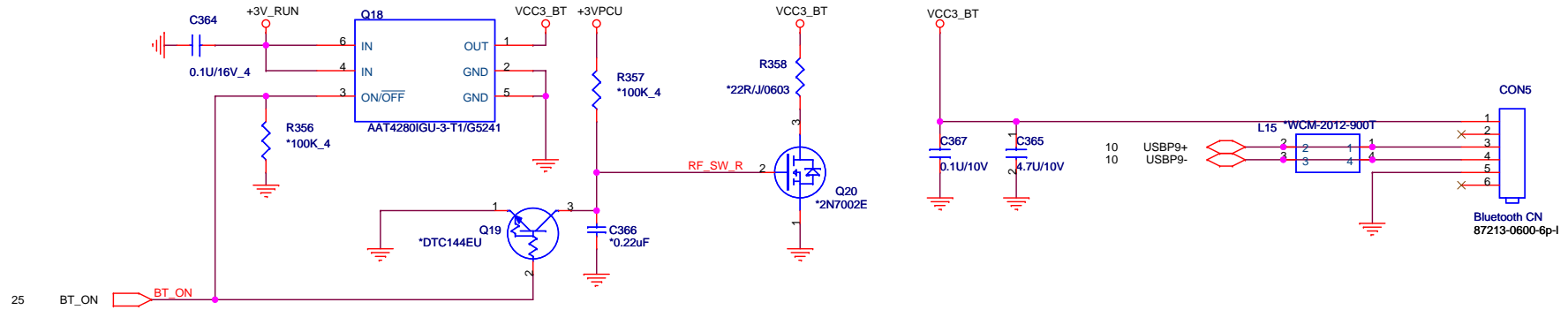
EMI(Decoupling Cap)



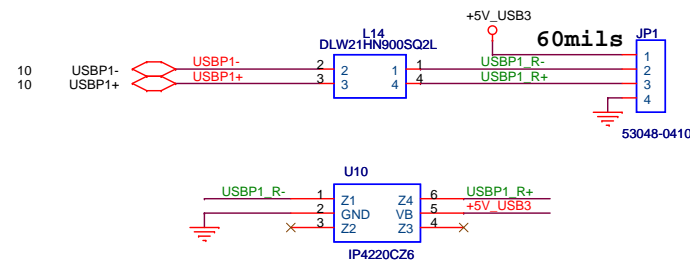
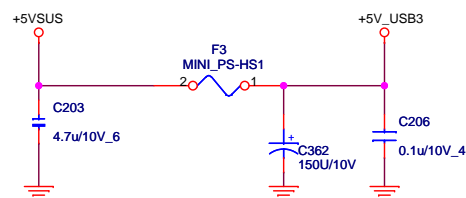
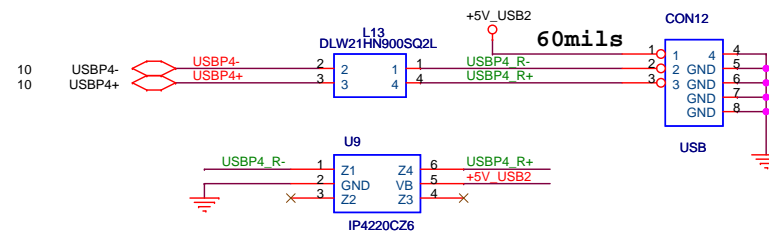
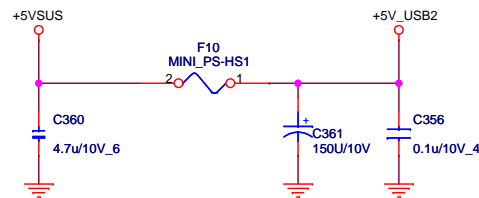
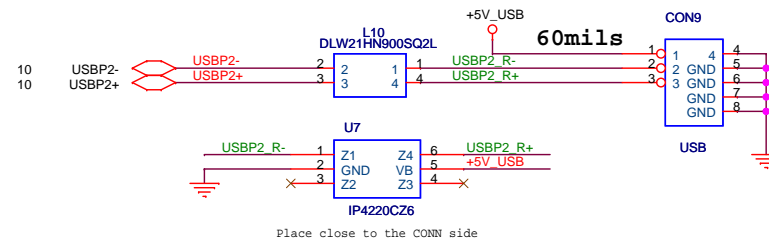
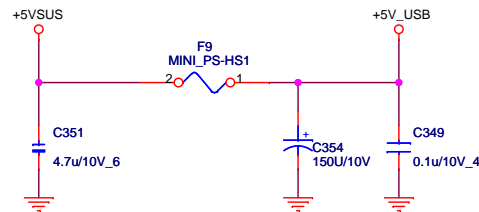
Quanta Computer Inc.

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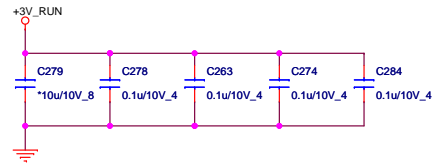
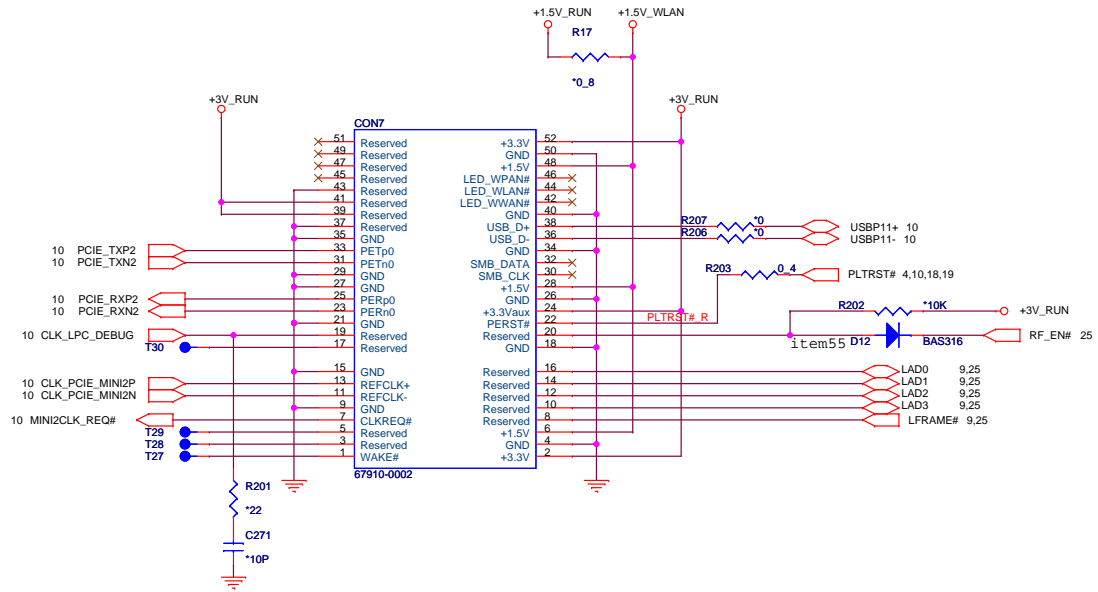
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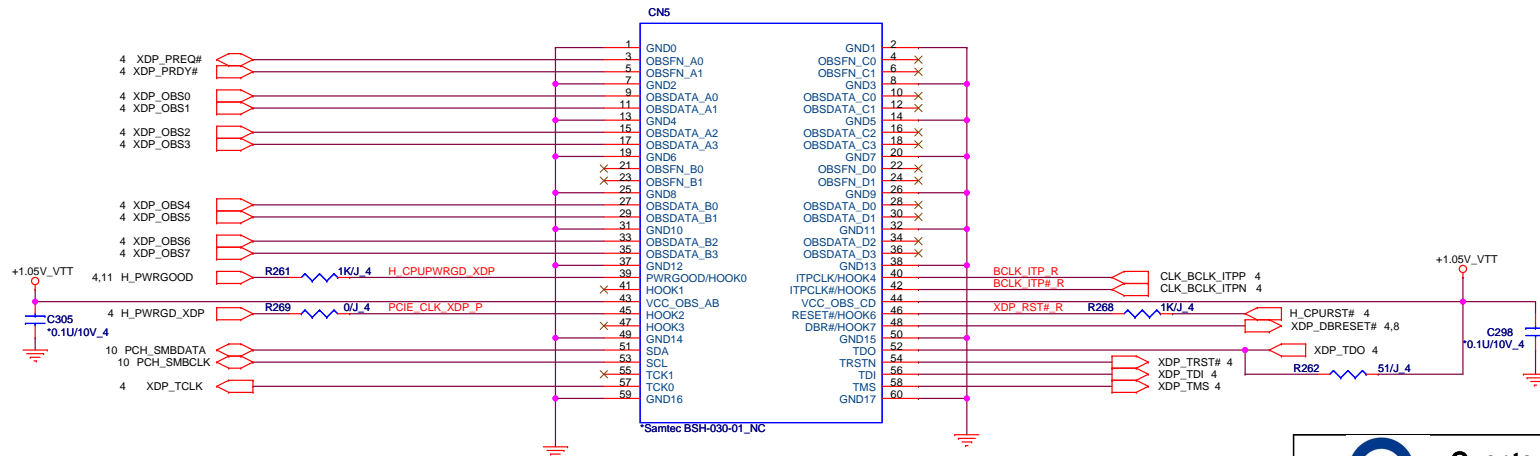
USB Connector



MINI CARD (WLAN)



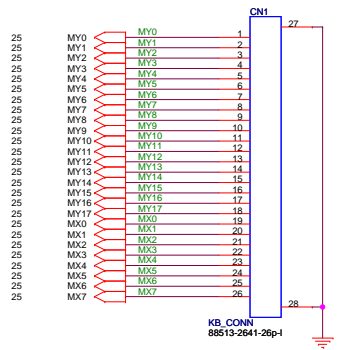
XDP



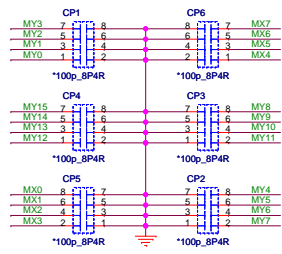
It is for debug. request vndeer provide 200 pcs sample.

		Quanta Computer Inc. PROJECT : FH1A	
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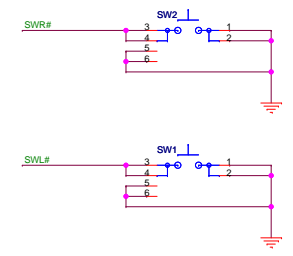
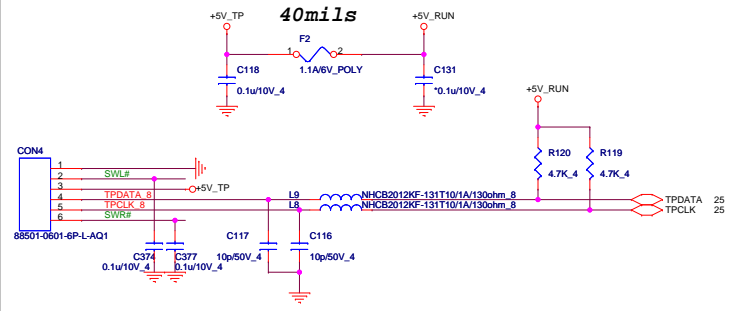
Keyboard(KBC)



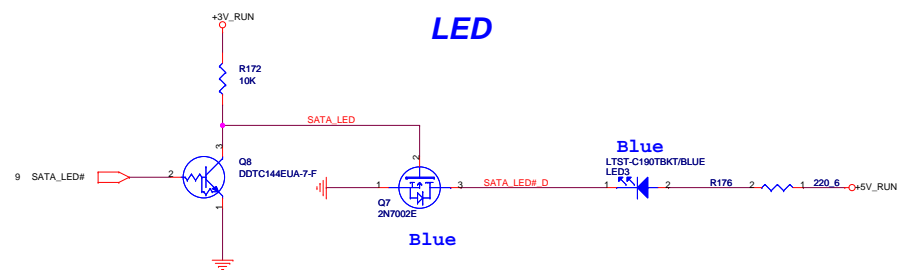
For EMI Reserve Caps for debug



Touch Pad



HDD/ODD



CAPS LED



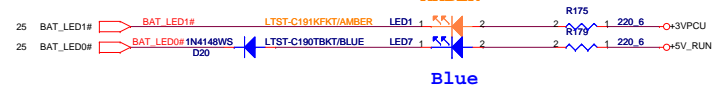
NUM LED



WLAN



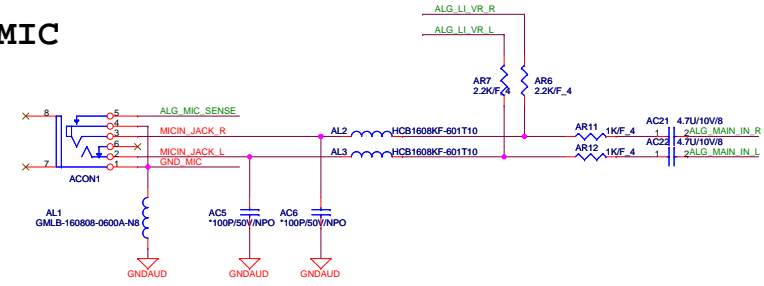
Battery



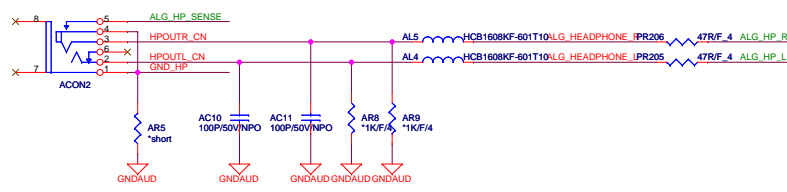
Power Status



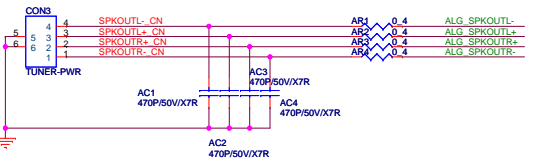
MIC



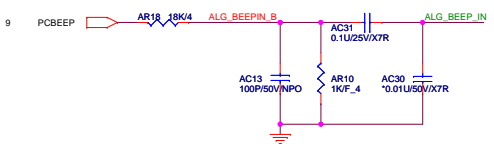
HP



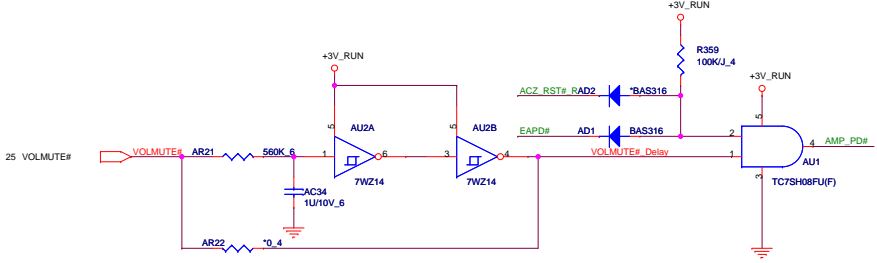
SPKR



BEEP

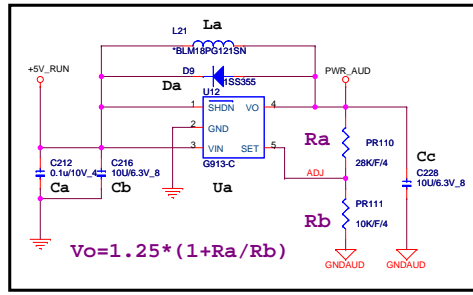
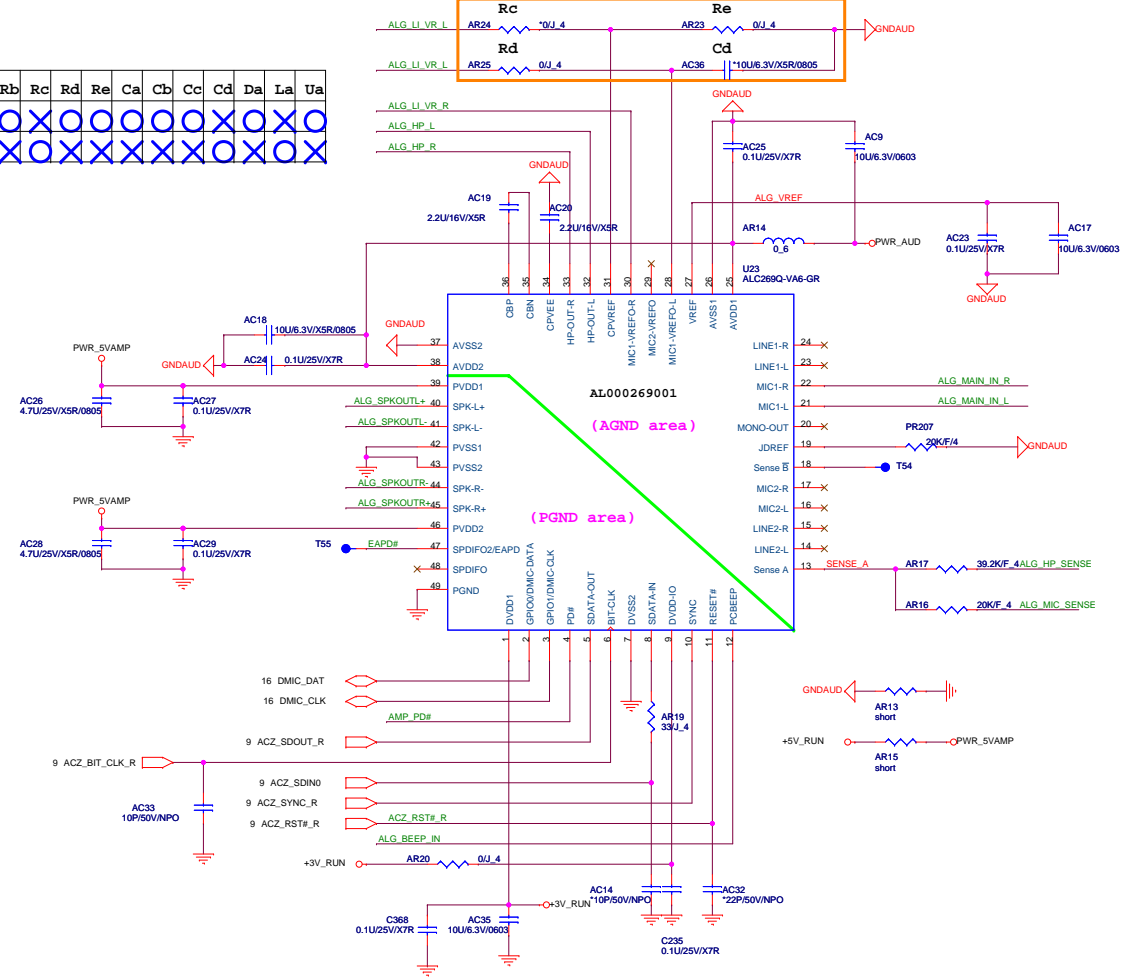


VOLMUTE



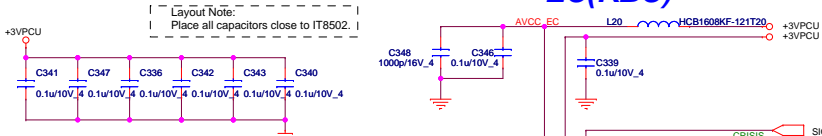
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ALC269Q-VA	○	○	○	○	○	○	○	○	○	○	○	○
ALC269Q-VB	○	○	○	○	○	○	○	○	○	○	○	○

Codec ALC269

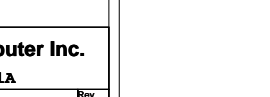
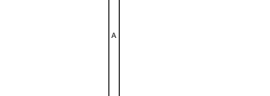
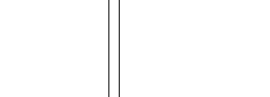
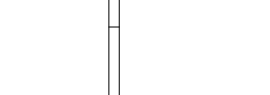
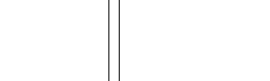
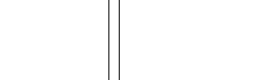
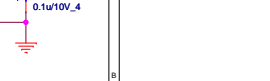
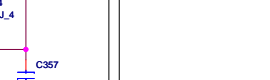
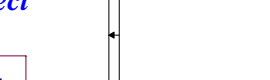
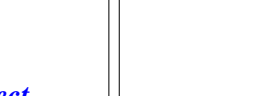
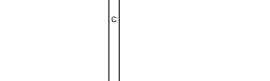
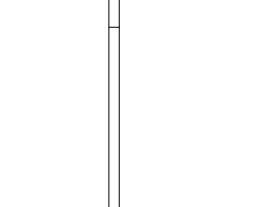
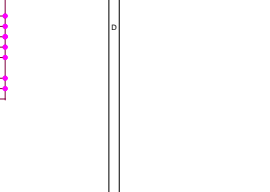
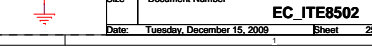
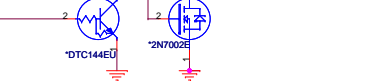
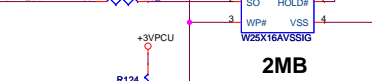
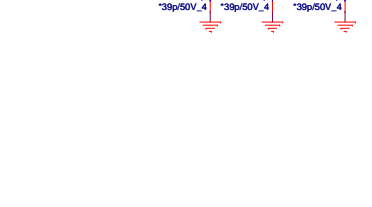
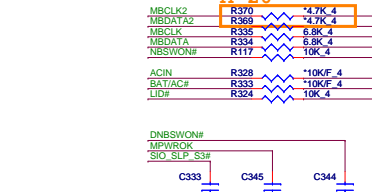
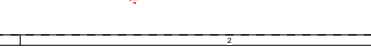
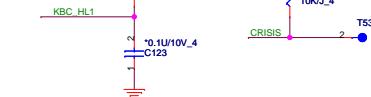
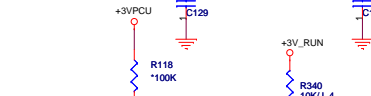
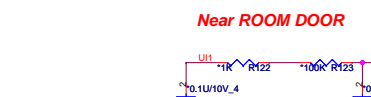
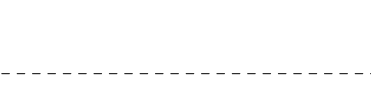
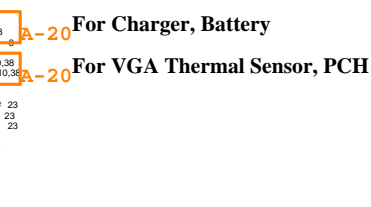
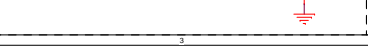
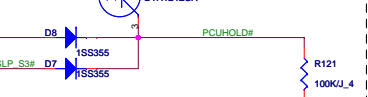
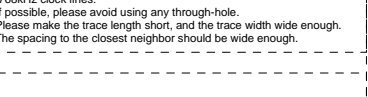
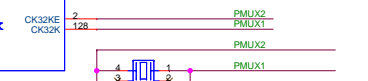
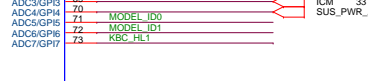
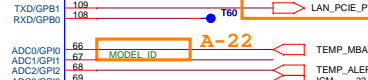
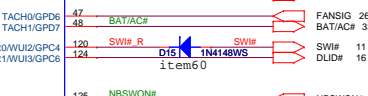
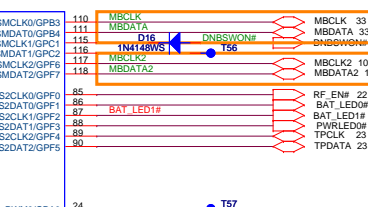
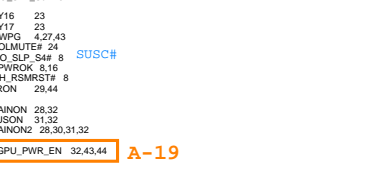
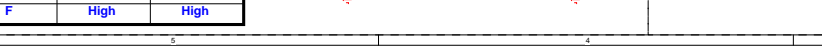
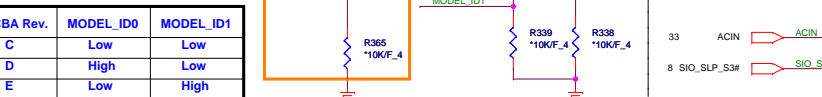
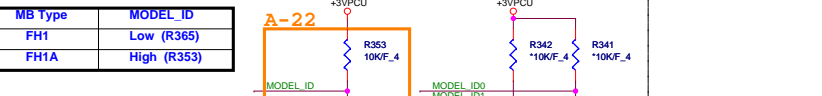
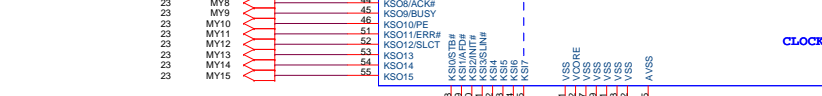
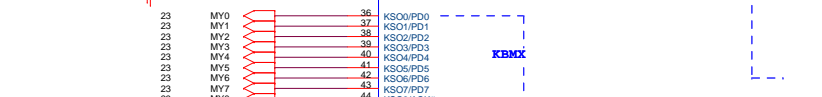
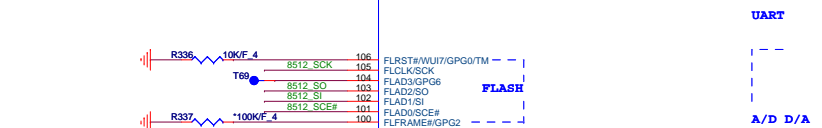
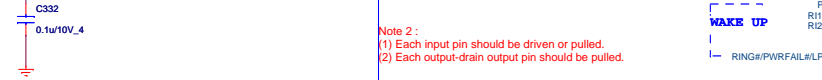
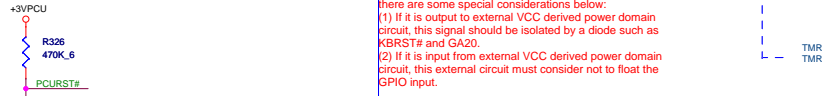
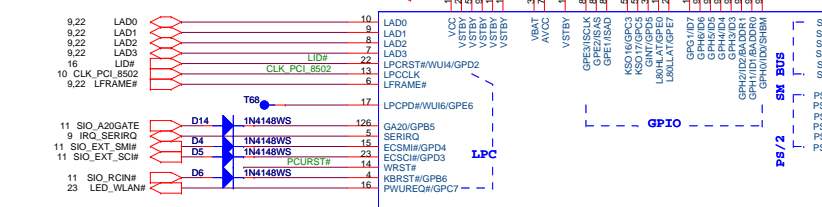
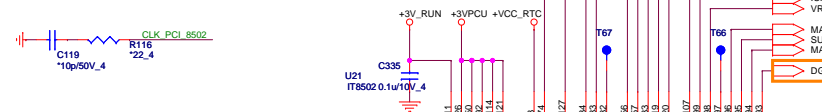


$$Vo = 1.25 * (1 + Ra/Rb)$$

EC(KBC)



Layout Note:
Place all capacitors close to IT8502.



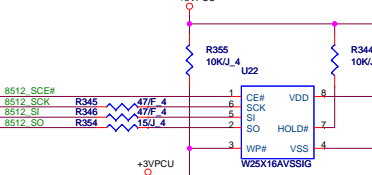
A-20 For Charger, Battery

A-20 For VGA Thermal Sensor, PCH

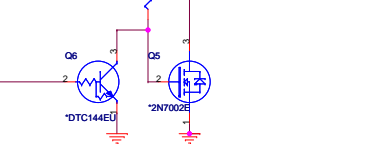
Note 1 : Since all GPIO belong to VSTBY power domain, and here are some special considerations below:
 (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
 (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
 (1) Each input pin should be driven or pulled.
 (2) Each output-drain output pin should be pulled.

BIOS Write Protect

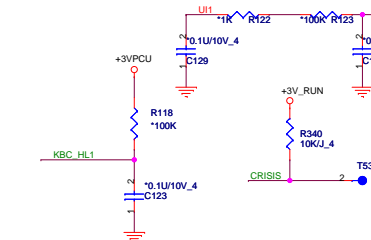


2MB



Layout Note:
 32.768kHz clock lines:
 a. If possible, please avoid using any through-hole.
 b. Please make the trace length short, and the trace width wide enough.
 c. The spacing to the closest neighbor should be wide enough.

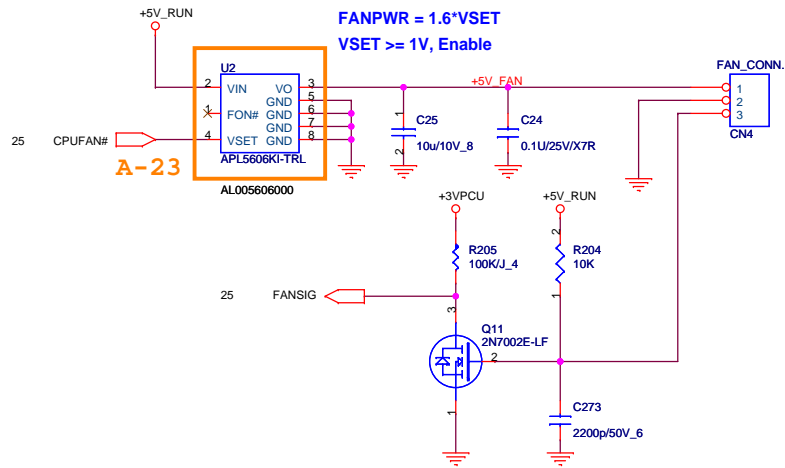
Near ROOM DOOR



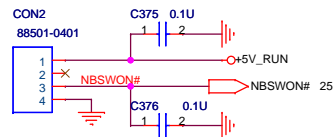
MB Type	MODEL_ID
FH1	Low (R365)
FH1A	High (R353)


PCBA Rev.	MODEL_ID0	MODEL_ID1
C	Low	Low
D	High	Low
E	Low	High
F	High	High

CPU FAN CTRL



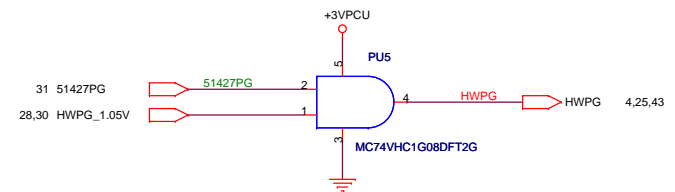
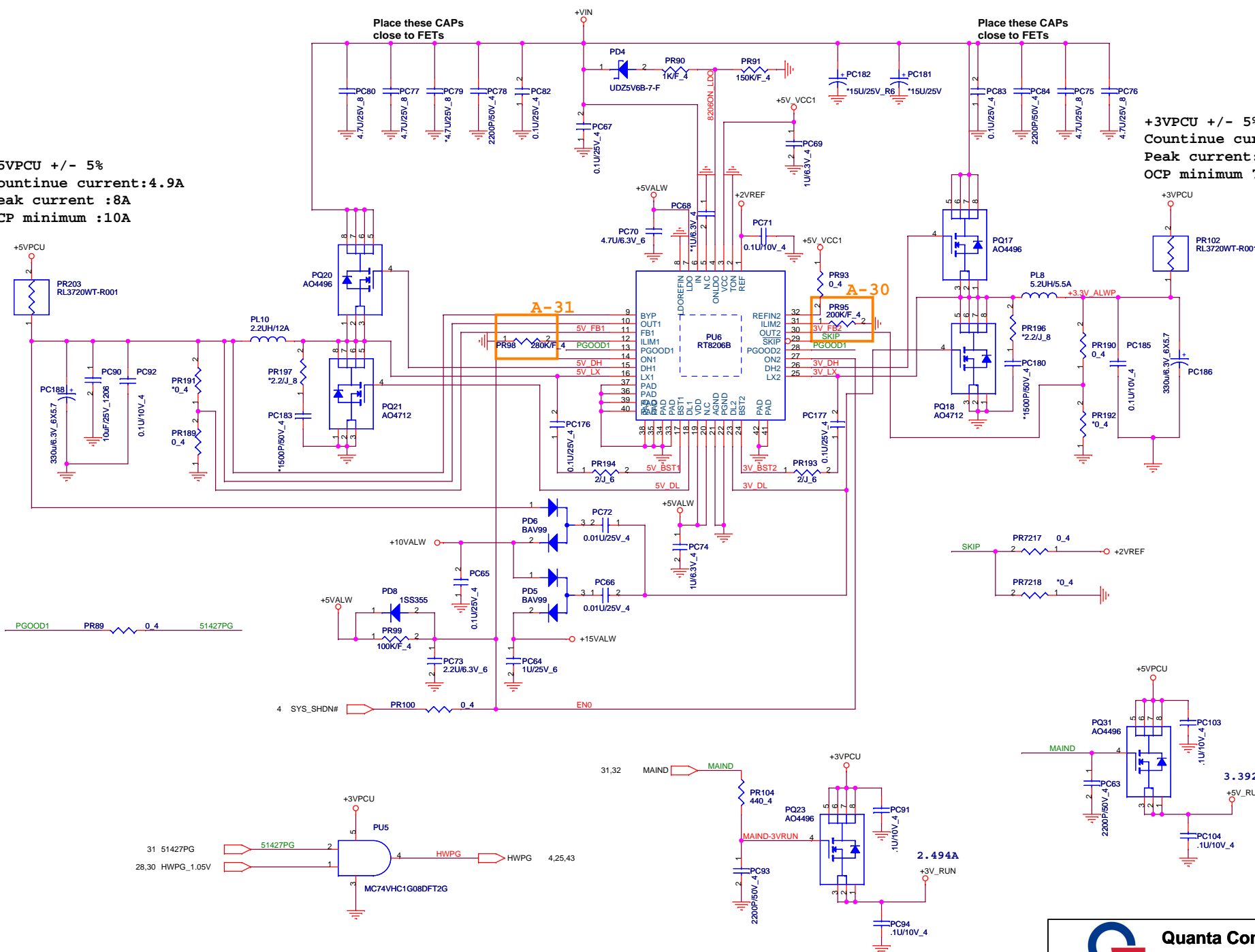
SW BOARD CON

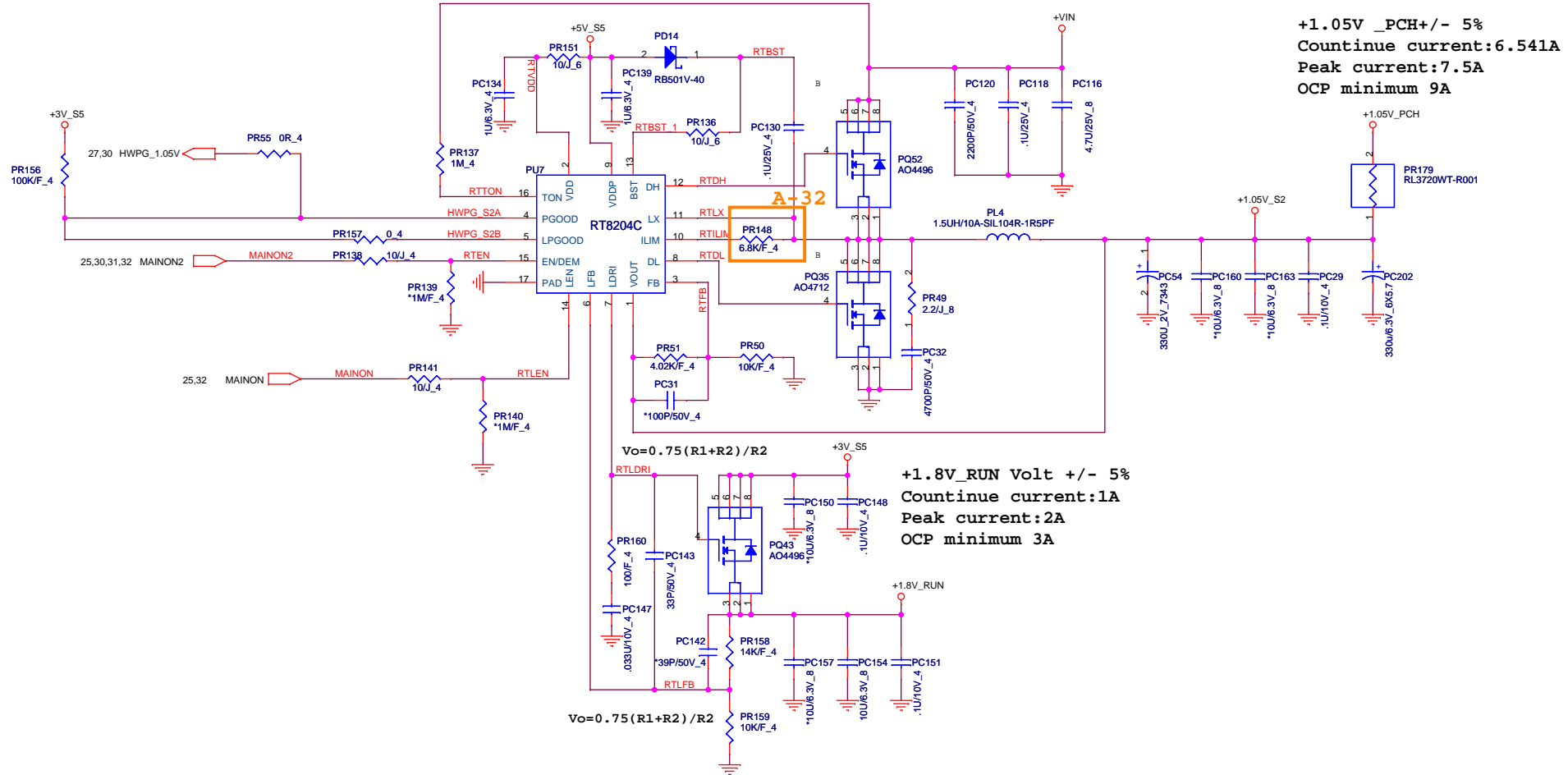


 Quanta Computer Inc. PROJECT : FHLA		Rev
		1A
Size	Document Number	Date
	FAN/SW CON	Tuesday, December 15, 2009
	Sheet	26 of 45

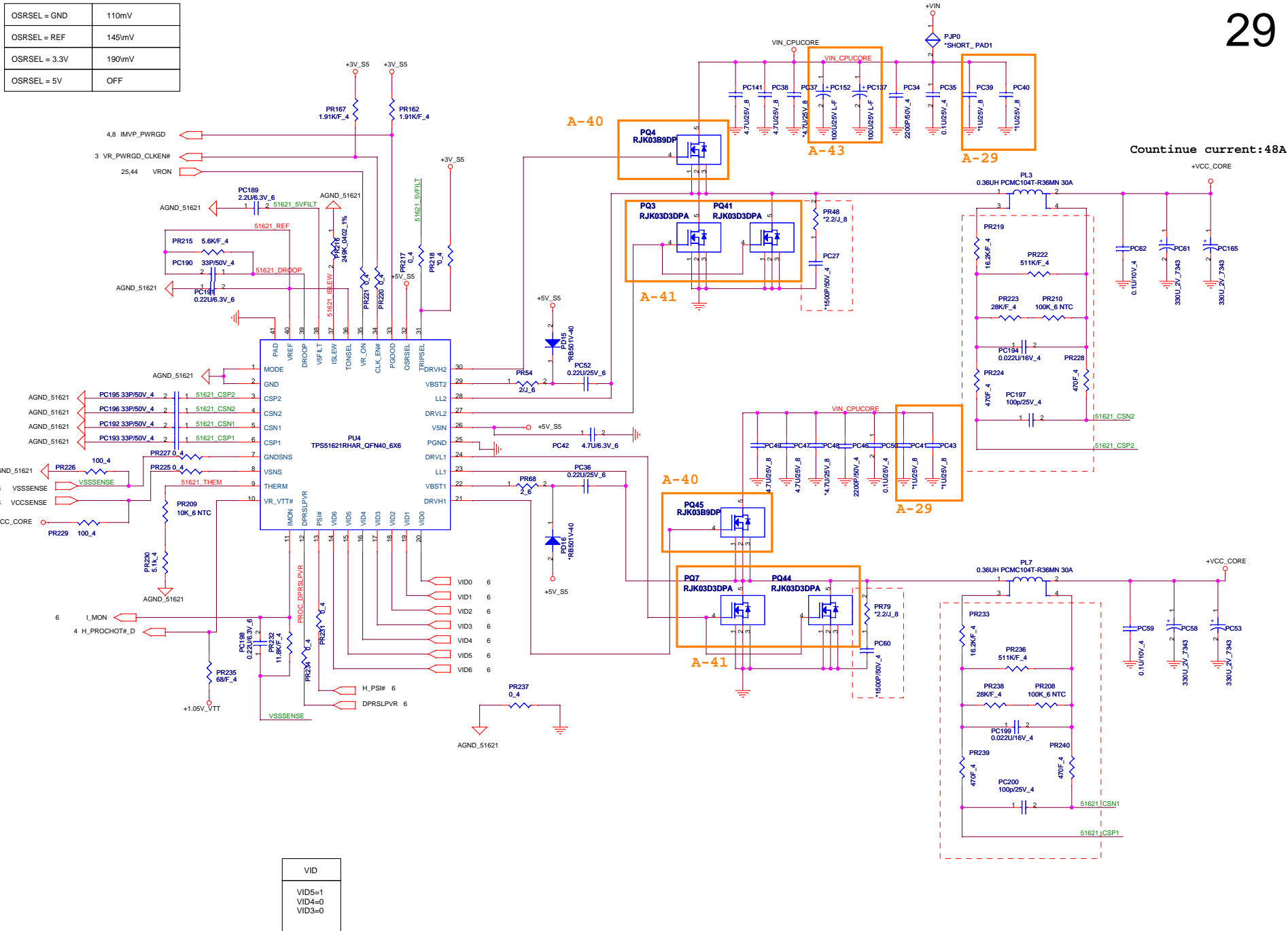
+5VPCU +/- 5%
 Countinue current:4.9A
 Peak current :8A
 OCP minimum :10A

+3VPCU +/- 5%
 Countinue current:5.1A
 Peak current:6A
 OCP minimum 7.5A

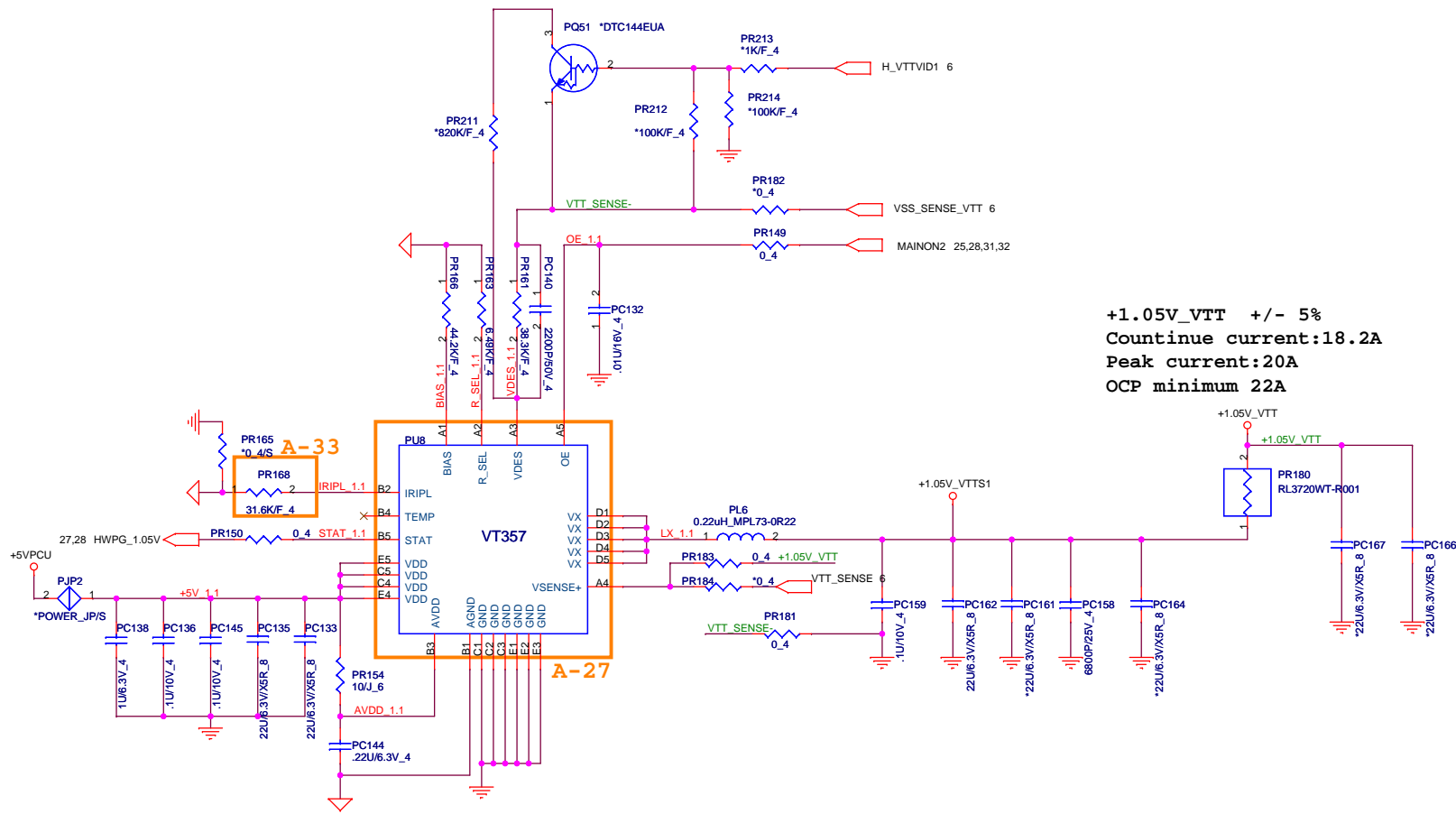




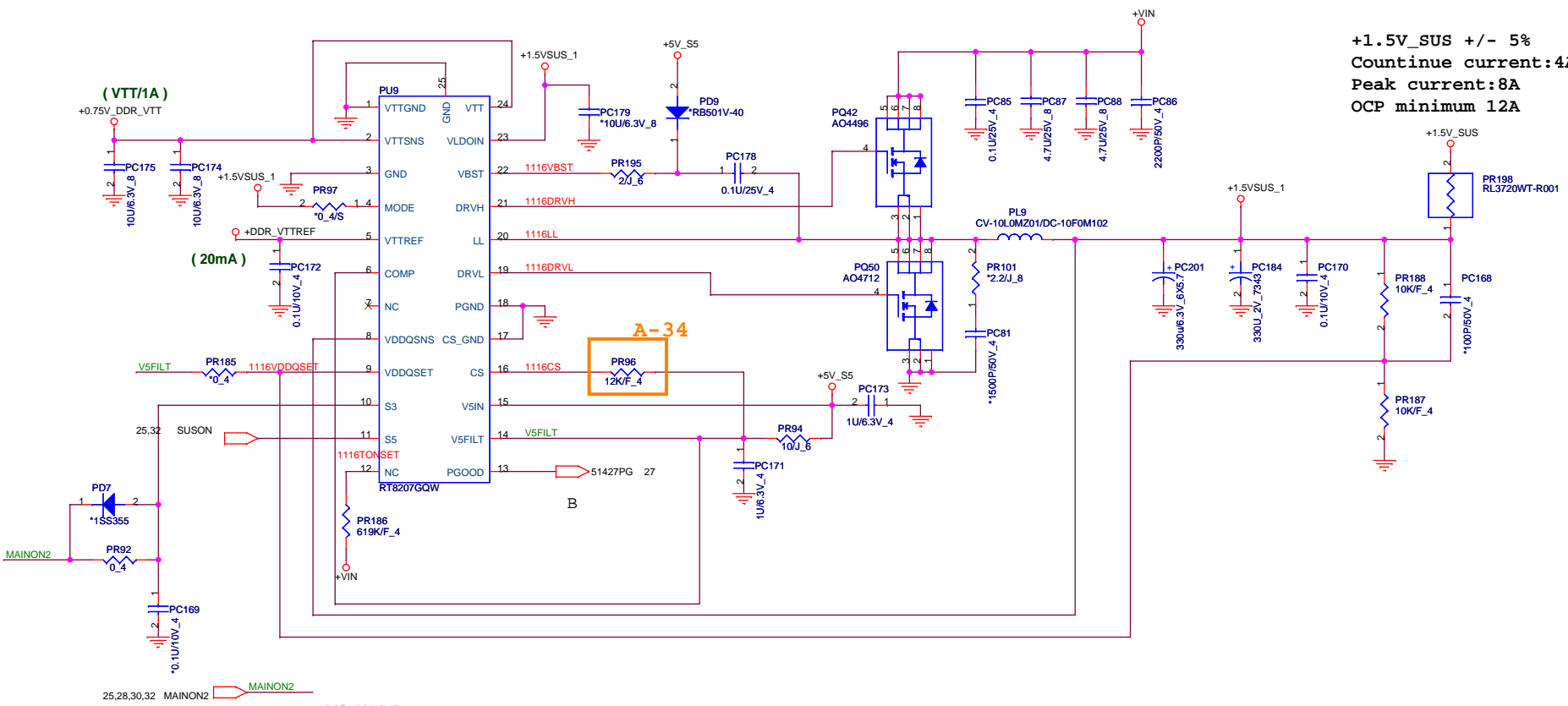
OSRSEL = GND	110mV
OSRSEL = REF	145mV
OSRSEL = 3.3V	190mV
OSRSEL = 5V	OFF



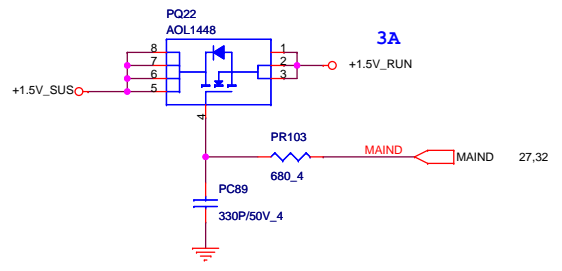
VID
VID5=1
VID4=0
VID3=0

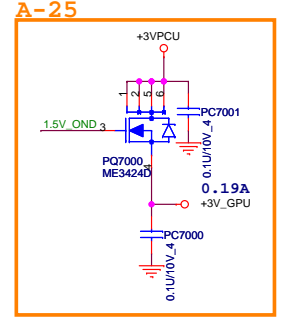
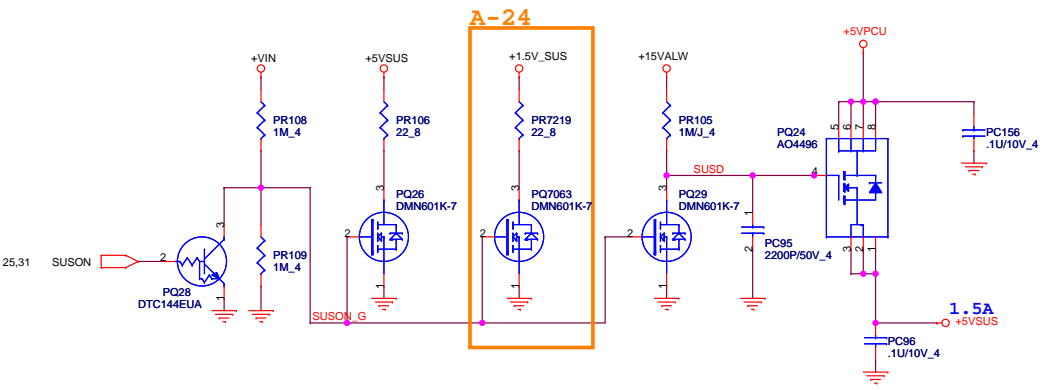
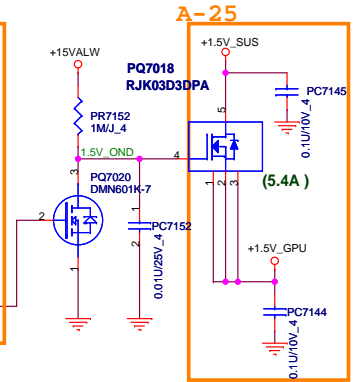
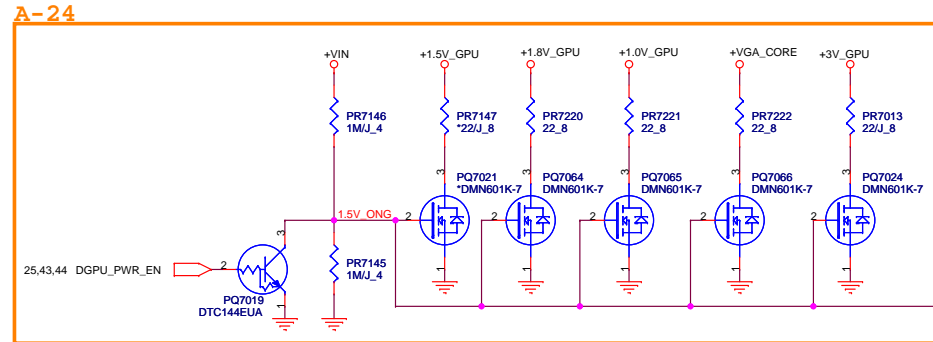
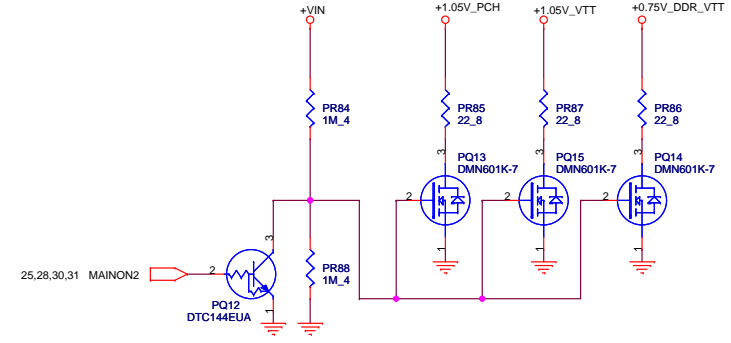
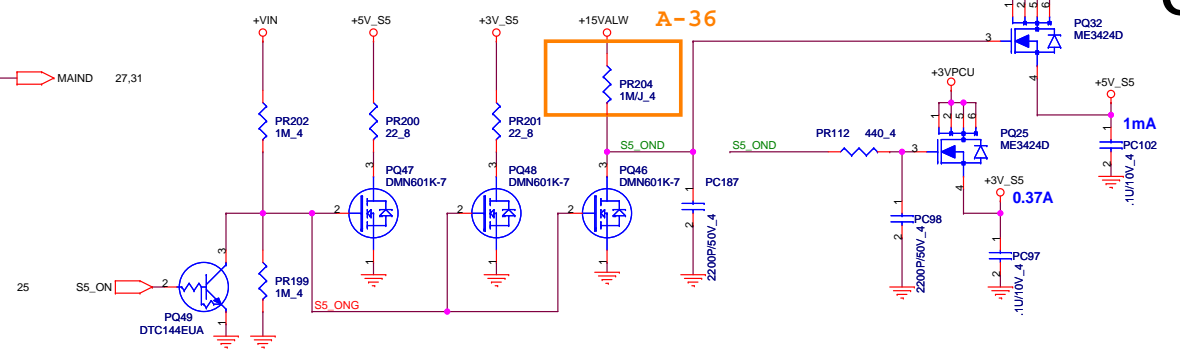
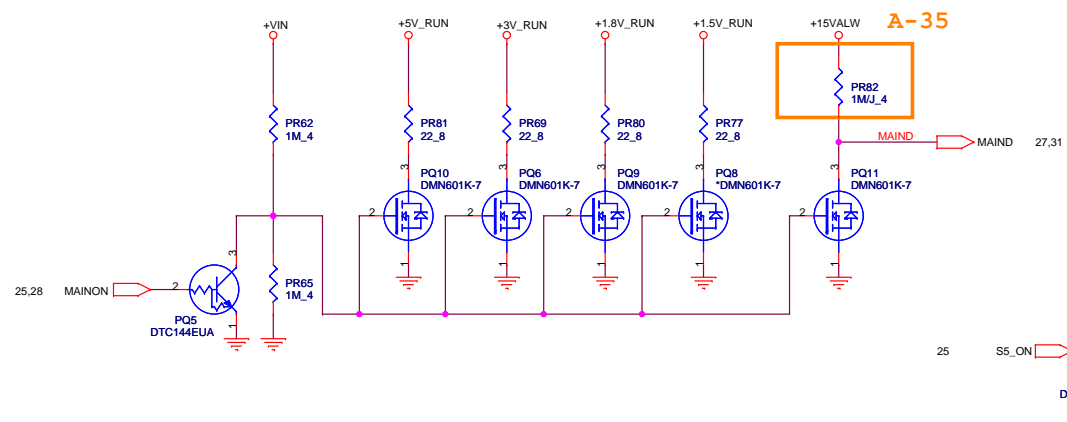


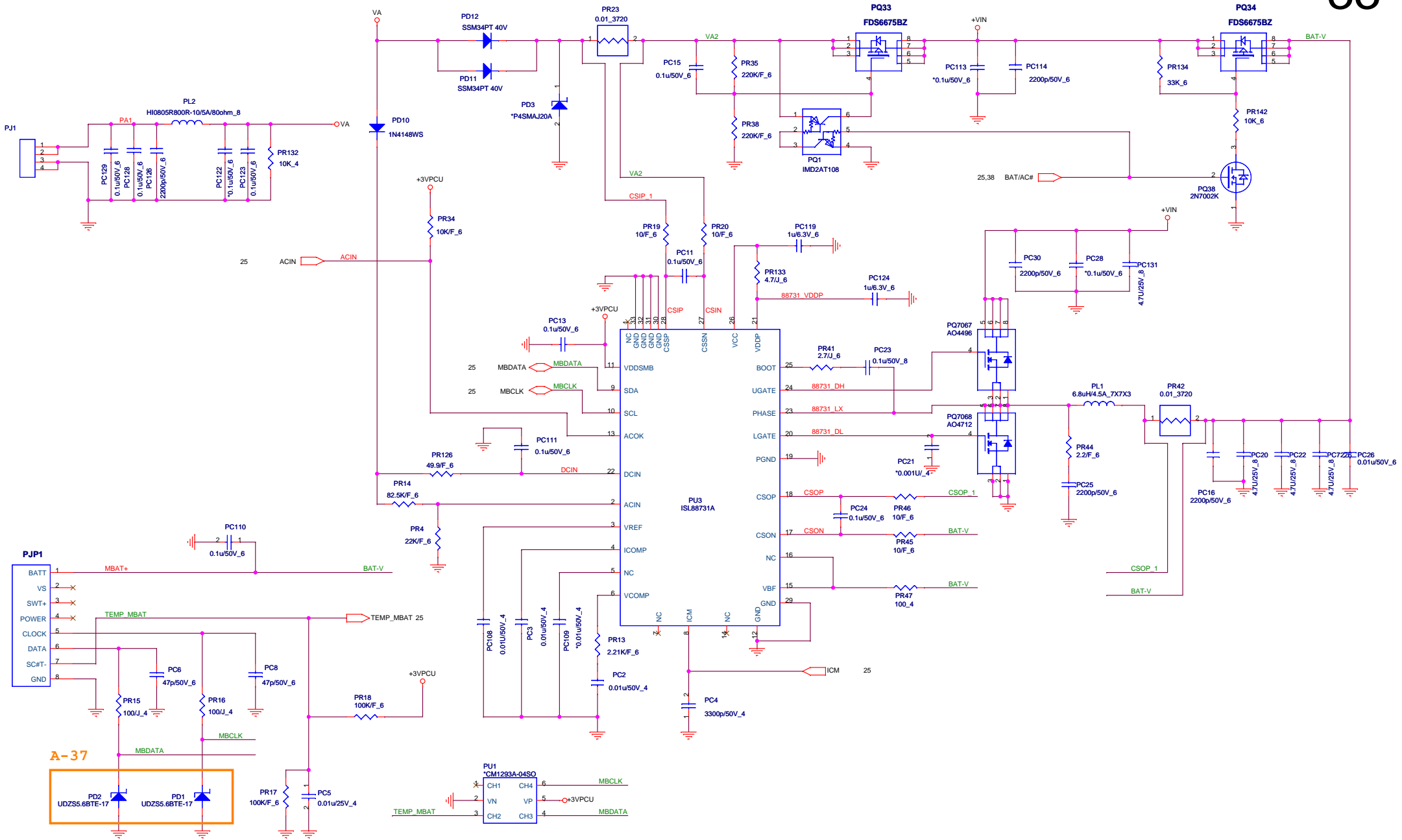
+1.5V_SUS +/- 5%
Countinue current:4A
Peak current:8A
OCP minimum 12A



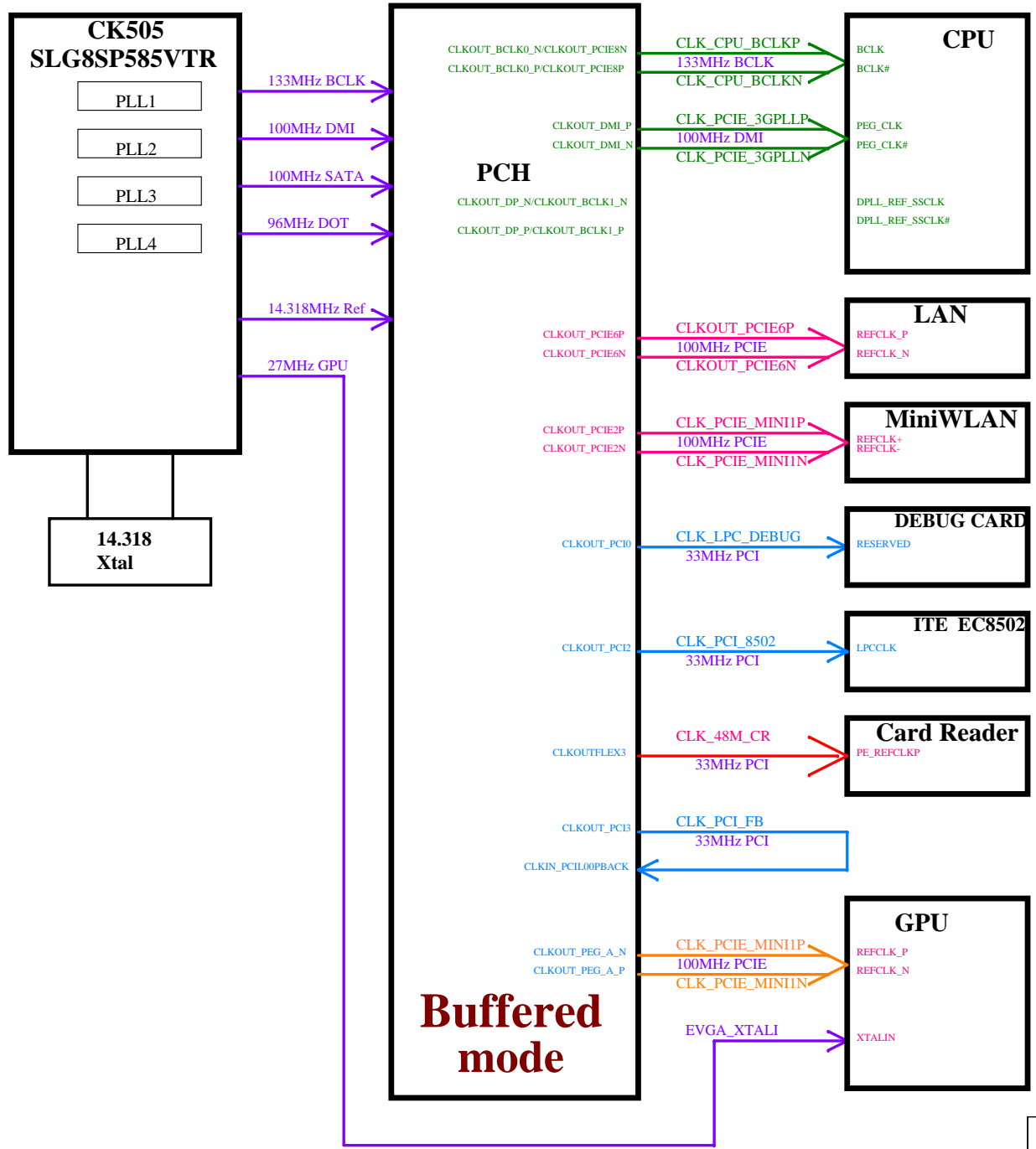
DIS_MODE
 Tracking discharge : VDDQ
 Non tracking discharge : GND
 No discharge : VCC5



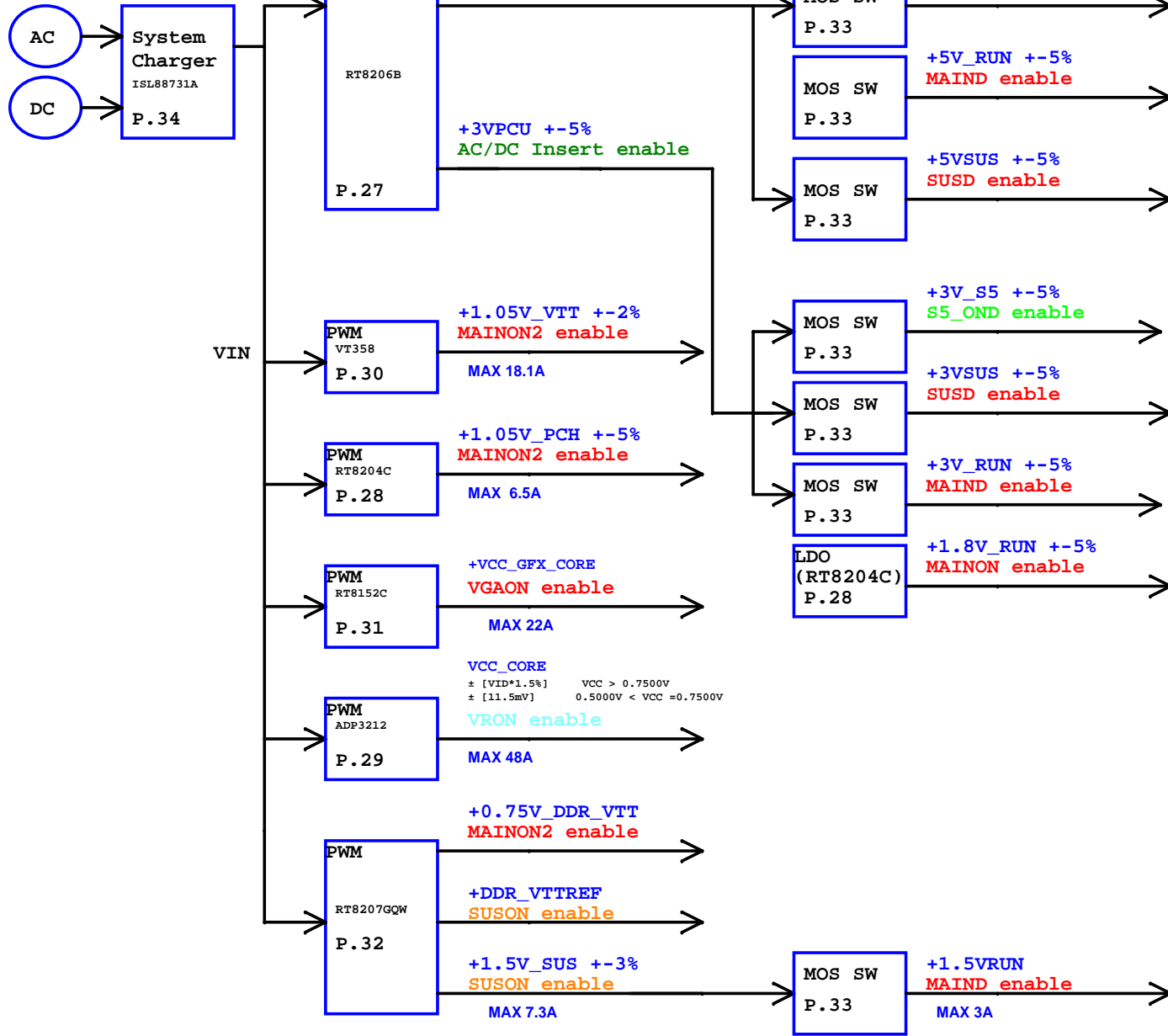


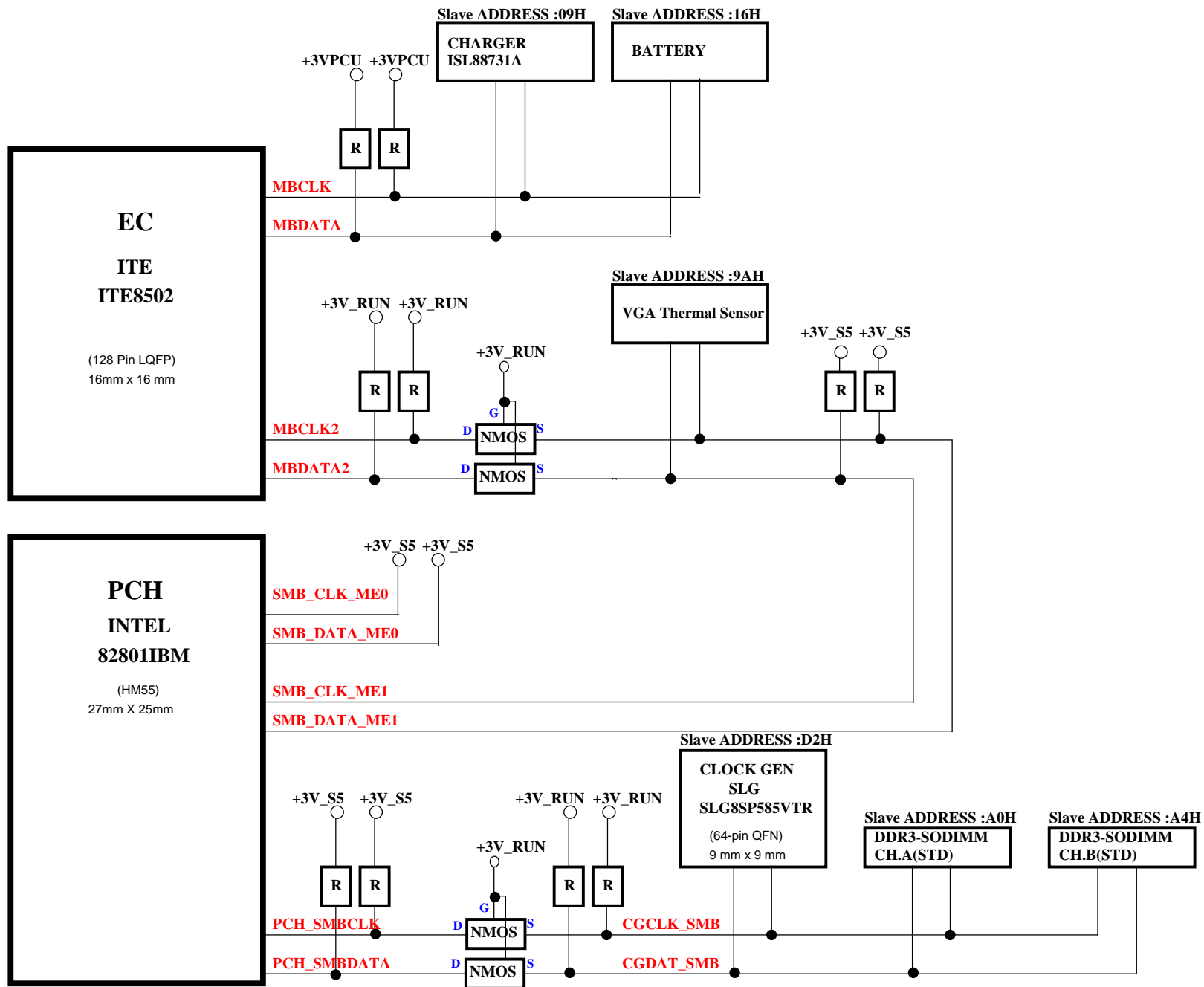


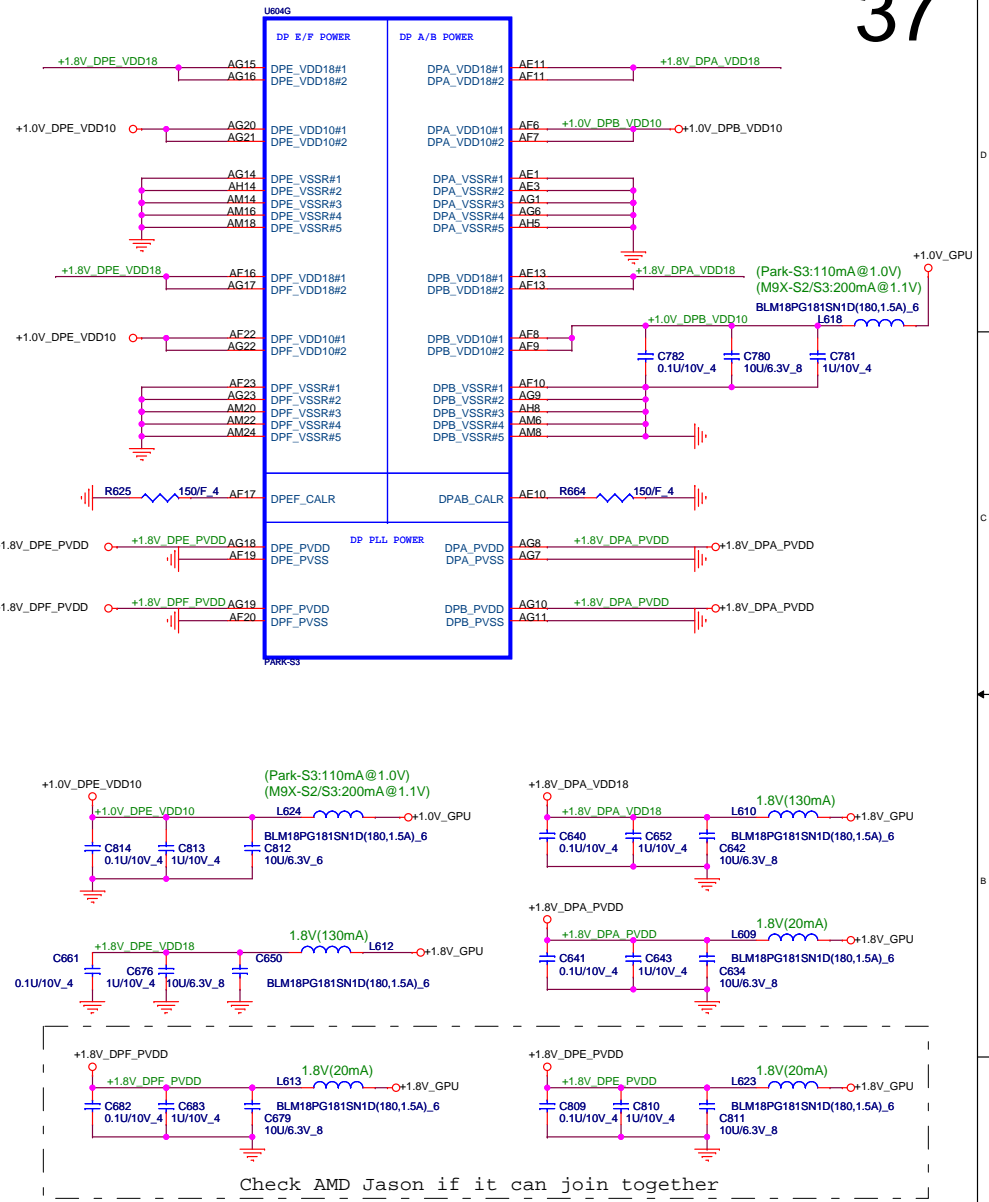
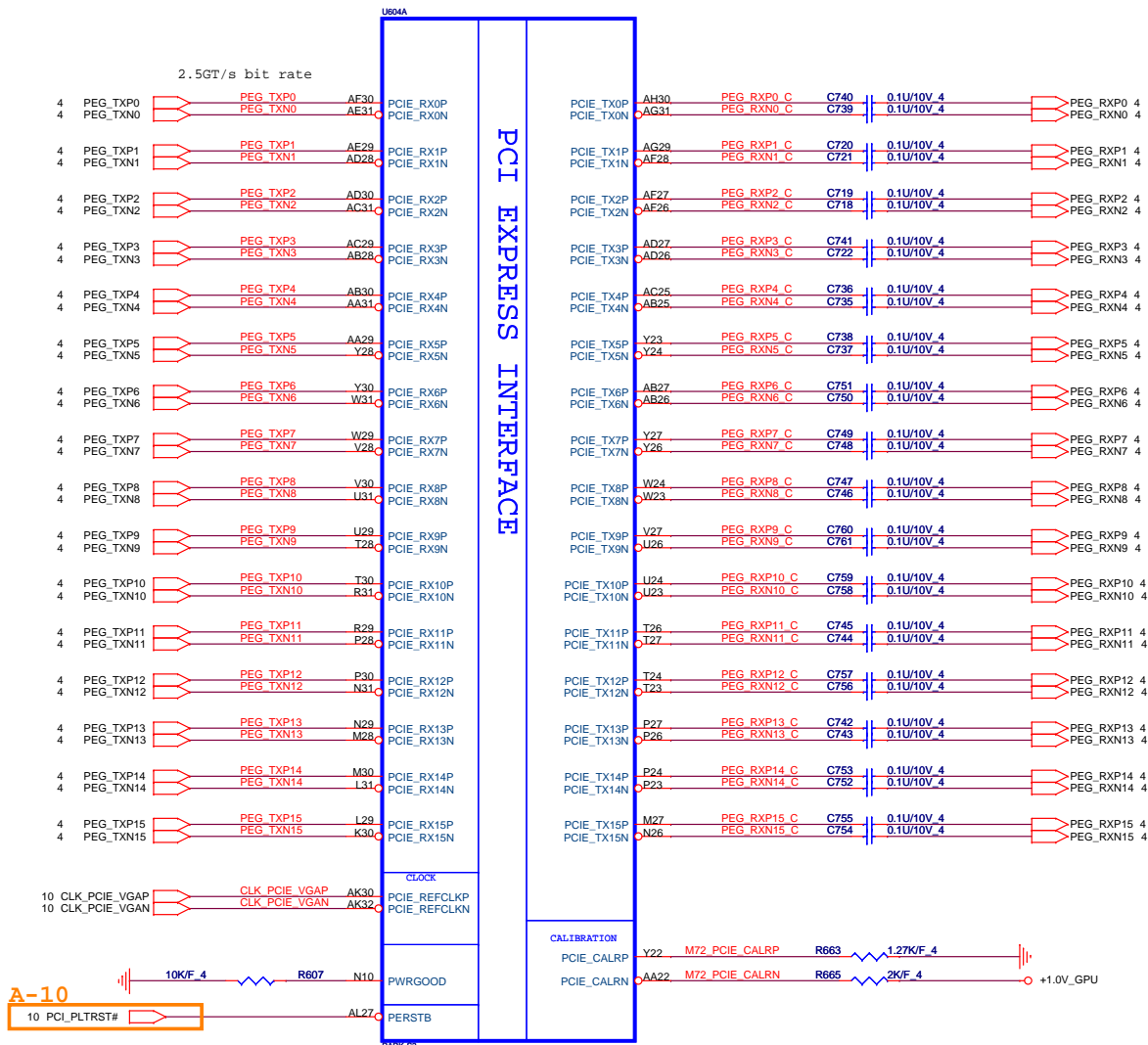
A-37



Power Tree Table







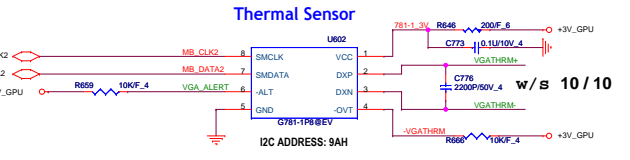
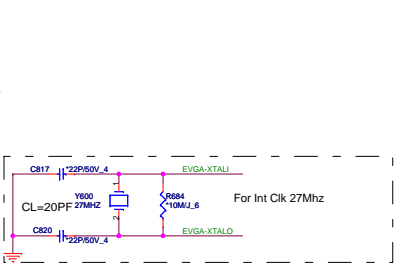
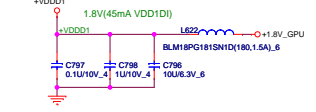
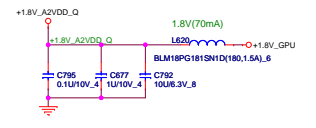
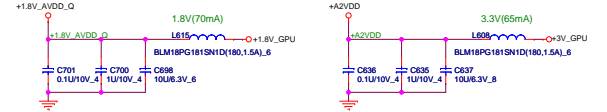
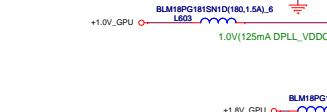
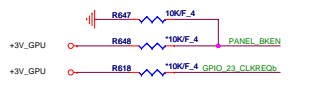
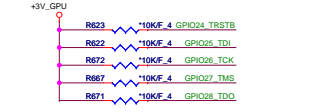
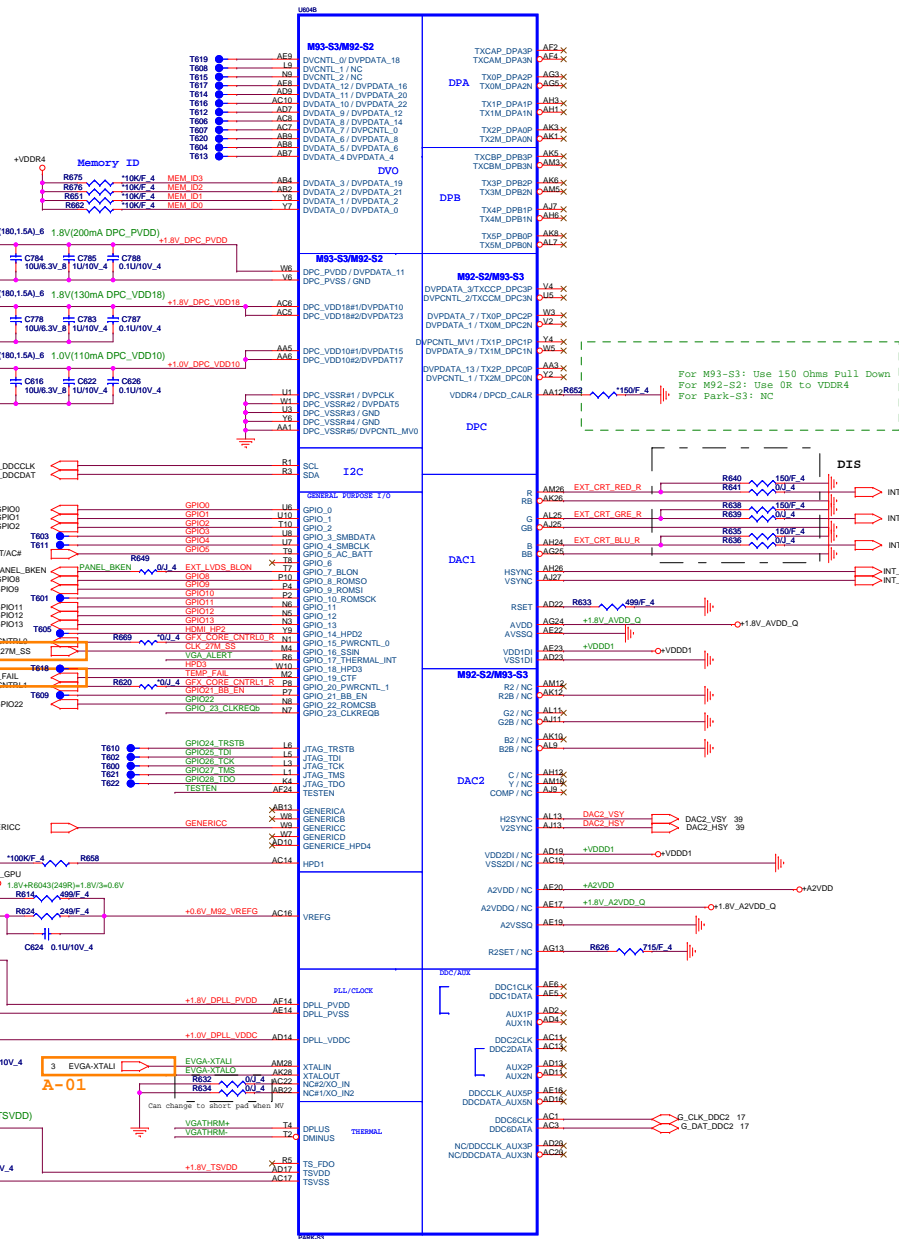
A-10

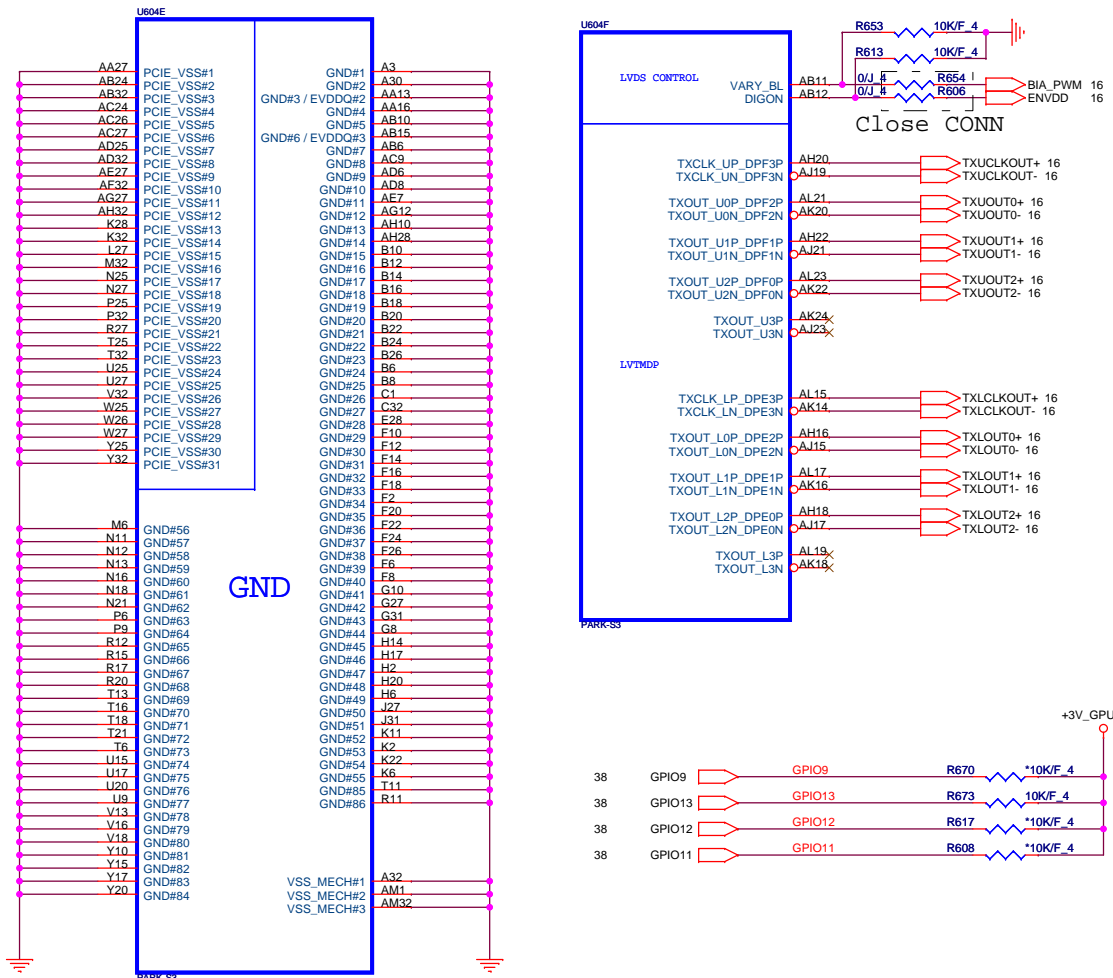
10 PCI_PLTRST#

100MHz (+/-300ppm) input frequency!
0-0.7V single-ended swing

MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000	Hynix Octon-die	64*16-800MHZ	H5T0163BFR-12C	AKD5L2G7W00
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	AKD5LGGT502
0010	Reserved		Reserved	Reserved
0011	Reserved		Reserved	Reserved
0100	Reserved		Reserved	Reserved
0110	Reserved		Reserved	Reserved
1000	Reserved		Reserved	Reserved
1001	Reserved		Reserved	Reserved
1010	Reserved		Reserved	Reserved
1011	Reserved		Reserved	Reserved
1100	Reserved		Reserved	Reserved
1101	Reserved		Reserved	Reserved
1110	Reserved		Reserved	Reserved
1111	Reserved		Reserved	Reserved

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V





CONFIGURATION STRAPS

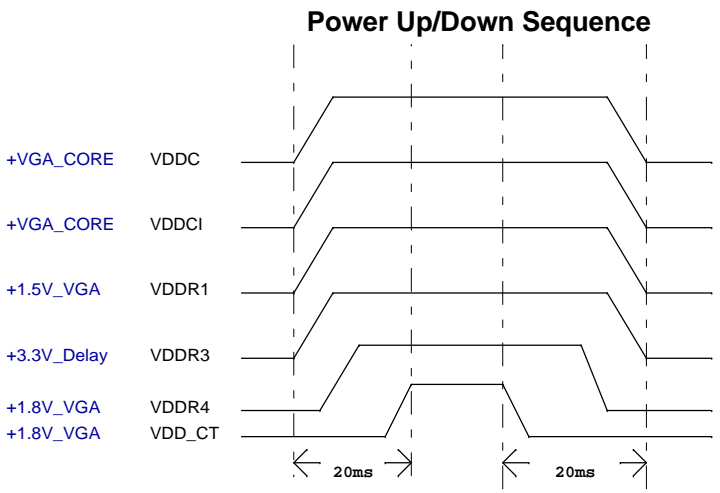
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

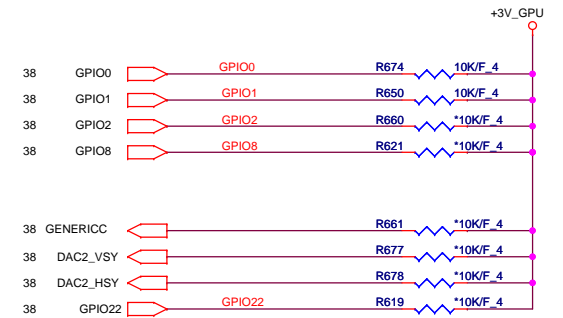
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

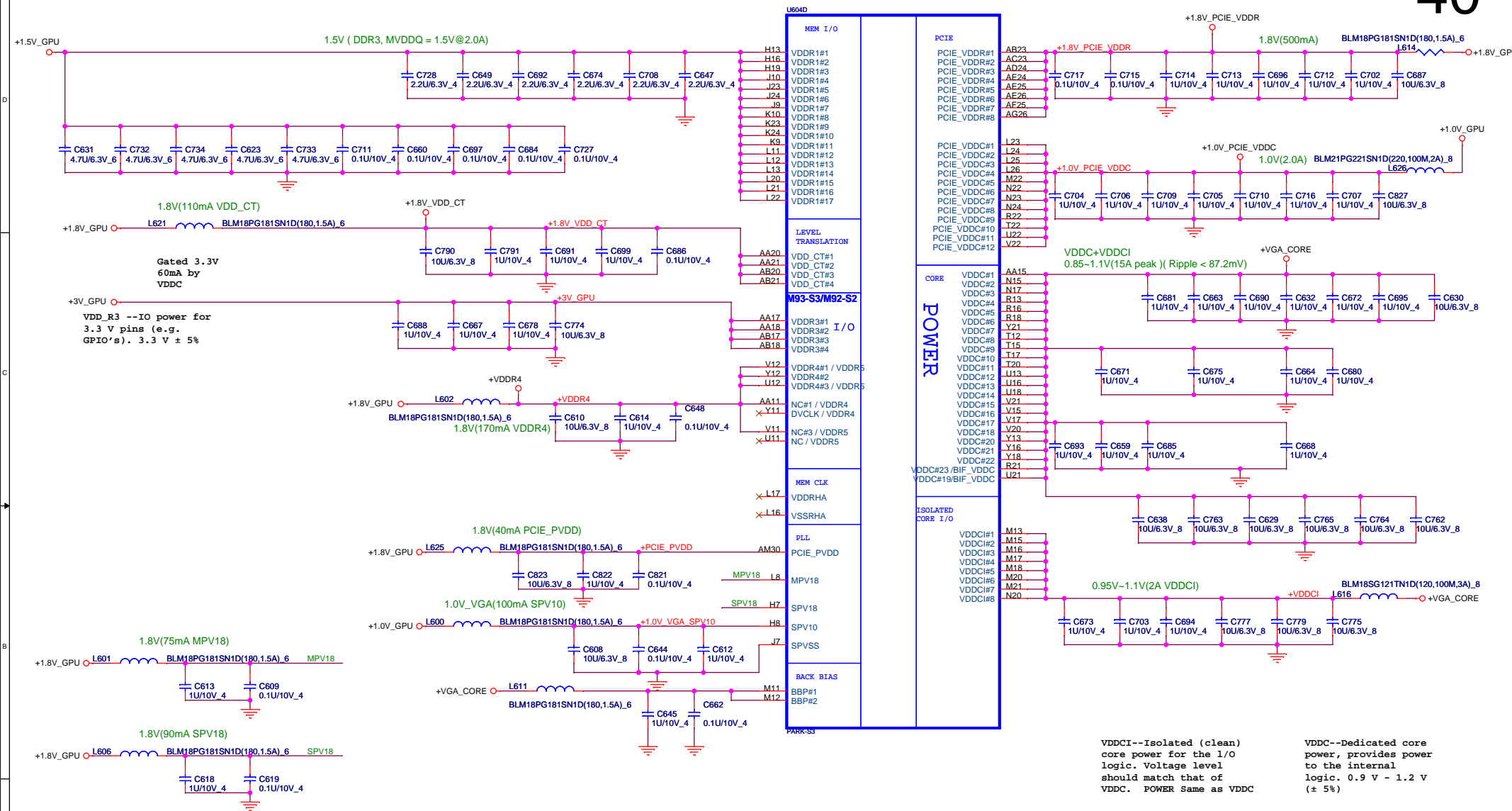


Memory Aperture size

GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



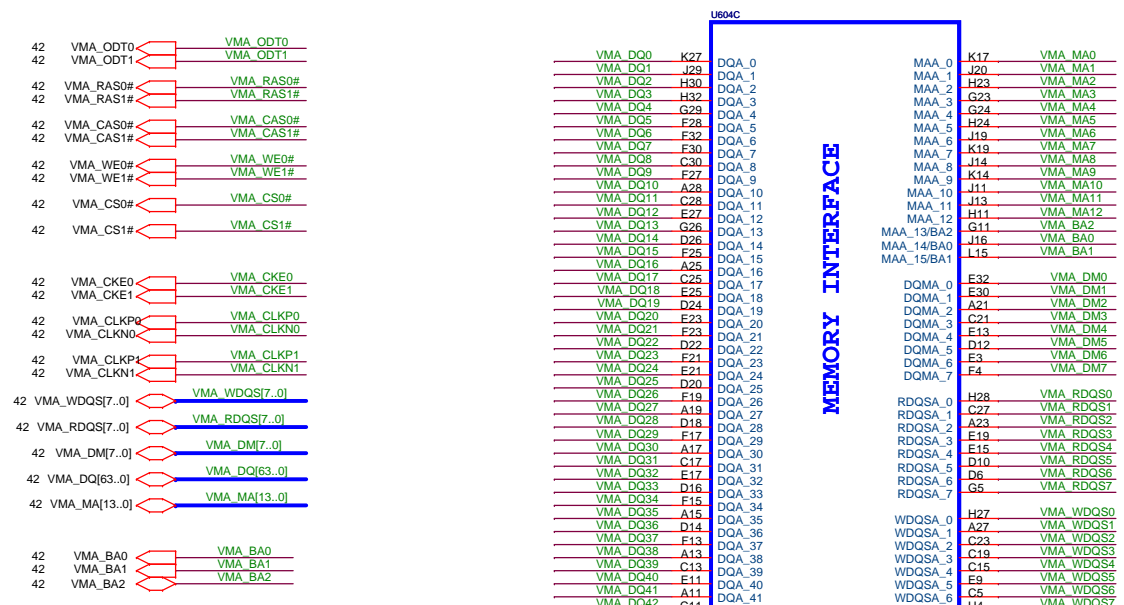


VDDRH_1 & VDDRH_2 --Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.

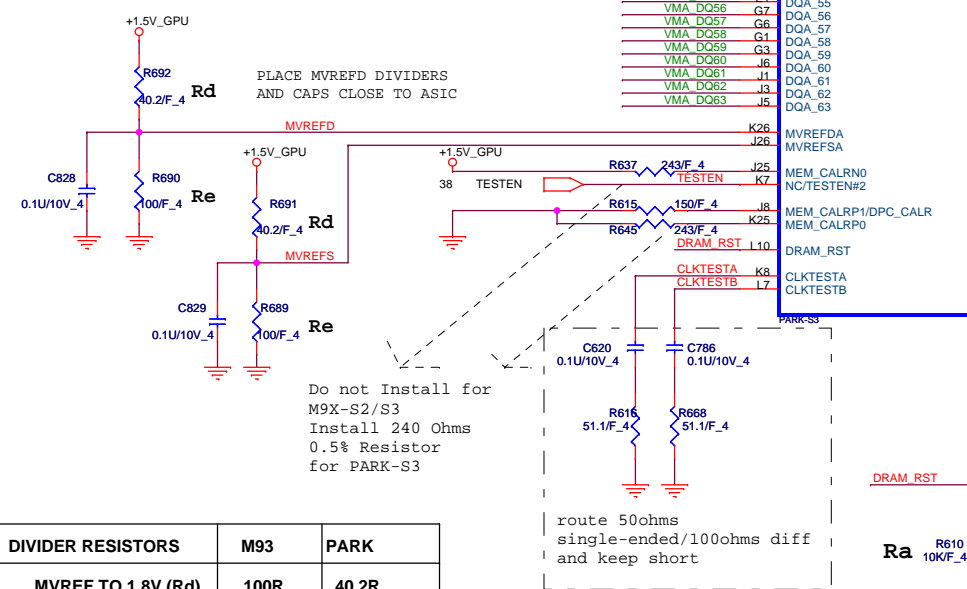
VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

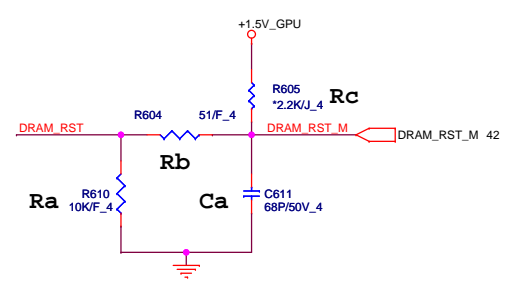
PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%



support 1Gbit
VRAM (64M X 16)



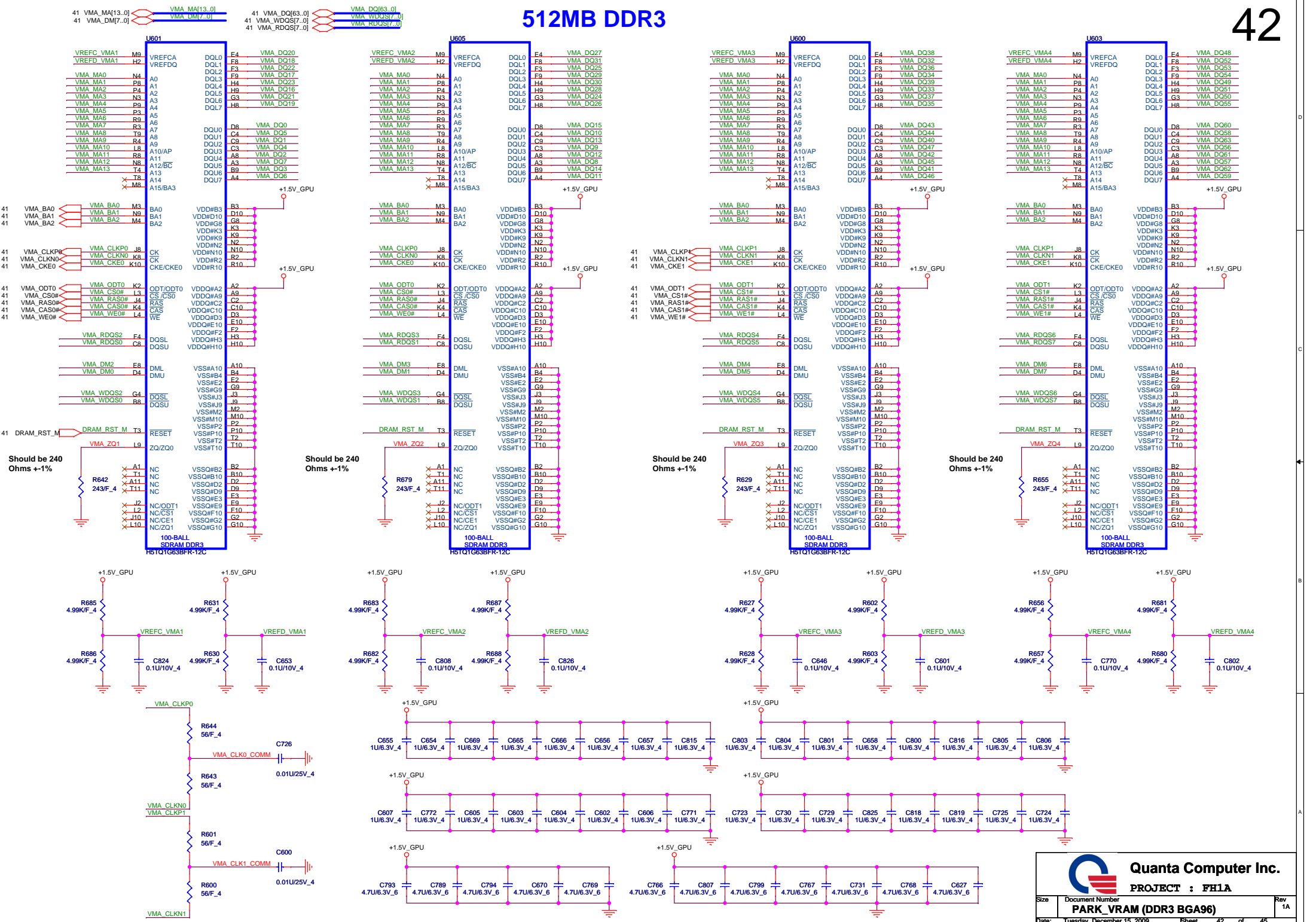
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



For PARK-S3 only
For M9X-S2/S3 with DDR3: this pin is not in use.

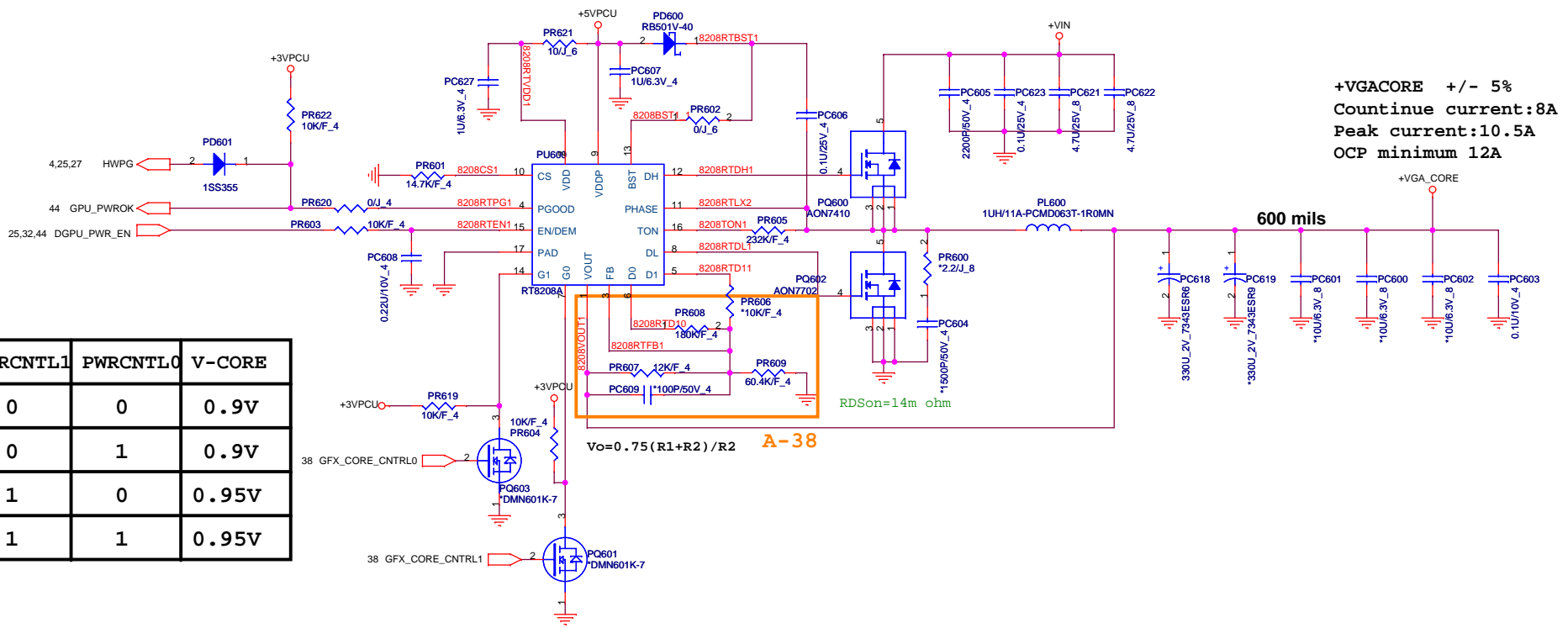
Designator	M9X-S2 and M93-S3	Park-S3
Ra	DNI	10K
Rb	0R/Short	51R
Rc	2.2K	DNI
Ca	2.2nF	68pF

512MB DDR3



Quanta Computer Inc.
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PARK_VRAM (DDR3 BGA96)
 Date: Tuesday, December 15, 2009 Sheet 42 of 45

VGA Core

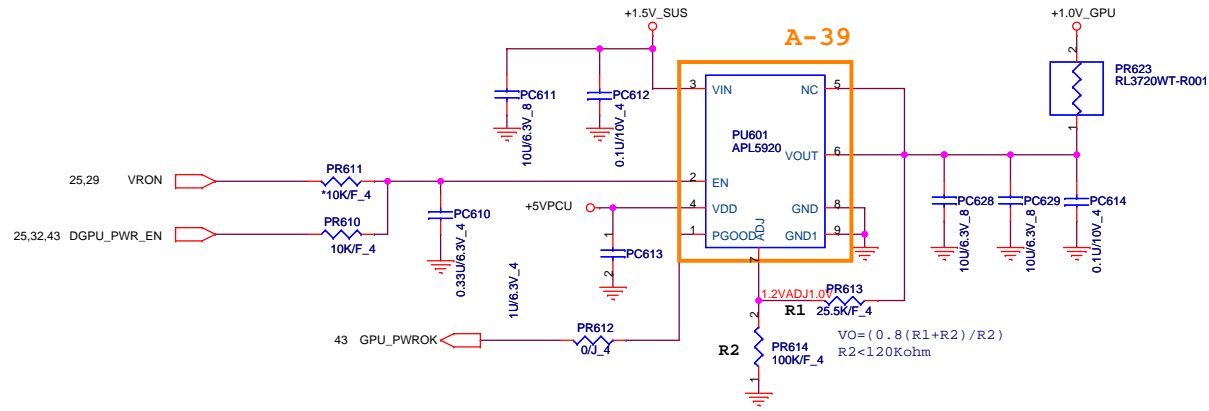


+VGACORE +/- 5%
 Continue current:8A
 Peak current:10.5A
 OCP minimum 12A

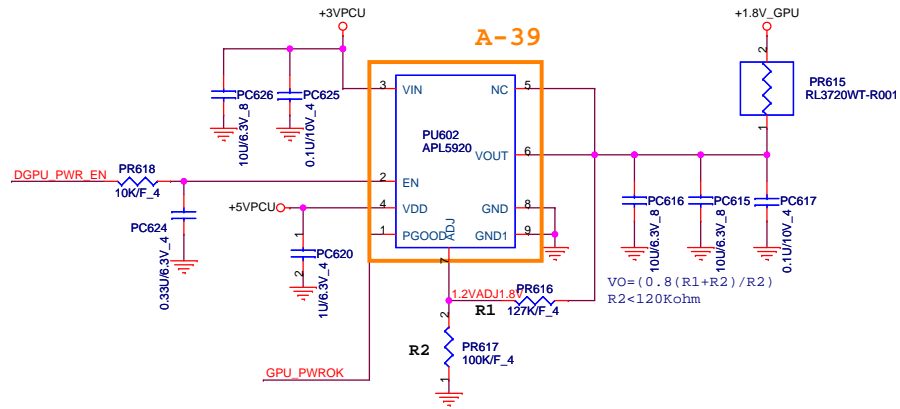
$V_o = 0.75 (R1 + R2) / R2$ **A-38**

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.9V
H	1	0	0.95V
Fixed	1	1	0.95V

+1.0V +/- 5%
Countinue current:2A
Peak current:3A




+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A



Change List

- A-01 PAGE 3,38 : Add EVGA-XTALI and CLK_27M_SS, and stuff R343, nonstuff R416 for providing 27MHz clock.
- A-02 PAGE 4,8 : NC FDI_TX[7:0]/FDI_TX#[7:0], and FDI_INT,FDI_FSYNC0/1,FDI_LSYNC0/1 connect to GND for disable UMA setting.
- A-03 PAGE 4,37 : Add PEG_RXN[15:0],PEG_RXP[15:0],PEG_TXN[15:0],PEG_TXP[15:0] to connect to Park LP PCIE I/F
- A-04 PAGE 4,10 : DPLL_REF_SSCLK/DPLL_REF_SSCLK# pull down and NC in PCH side for Disable UMA setting.
- A-05 PAGE 4,38 : Reserve TEMP_FAIL circuit for GPU thermal detect signal control.
- A-06 PAGE 6 : VAXG_SENSE,VSSAXG_SENSE,GFX_VID[6:0],GFX_VR_EN,GFX DPRSLPVR to be NC, VAXG connect to GND, and IMON pull down via R220 10Kohm for Disable UMA
- A-07 PAGE 8 : LVDS/CRT signals in PCH side to be NC
- A-08 PAGE 9 : RTC Battery Connect CON11 change from Cable type to Socket type(PN : DFHS02FS027)
- A-09 PAGE 9,26 : Remove MDC circuit
- A-10 PAGE 10,37 : PCI_PLTRST# connect to Park LP PinAL23
- A-11 PAGE 10 : Change U4 from OR gate to AND gate
- A-12 PAGE 10 : Add PU resistors R468,R469 2.2Kohm
- A-13 PAGE 10 : Stuff R211 and Nonstuff Y4,R210,C282,C283
- A-14 PAGE 12 : VCCDAC0/1 connecto to +3V_RUN and VSSA_DAC0/1 connect to GND for Disable UMA setting
- A-15 PAGE 12 : VCCALVDS,VCCTX_LVDS[4:1] connect to GND, and VSSA_LVDS to be NC for Disable UMA setting
- A-16 PAGE 19,25 : Reserve R565 and D27, and Add control signal LAN_PCIE_PWR_CTRL# for LAN Power Saving Control
- A-17 PAGE 20 : Delete H13,H20
- A-18 PAGE 24 : Add AR23,AR24,AR25,AC36 for ALC269 VA and VB version control
- A-19 PAGE 25,32,43,44 : Add Contorl Signal DGPU_PWR_EN to control +VGA_CORE,+3V_GPU,+1.8V_GPU,+1.5V_GPU,+1.0V_GPU Power On/Off
- A-20 PAGE 10,25,33,38 : SMBCLK/SMBDATA for Charger and Battery SMBus signals, and SMBCLK2/SMBDATA2 for VGA Thermal Sensor and PCH SMBus signals.
- A-21 PAGE 25 : Delete R353
- A-22 PAGE 25 : Add MODEL_ID signal to U21 Pin67, and stuff PU resistor R353 10Kohm for MODEL selection
- A-23 PAGE 16,26 : Change Fan Controller U2 P/N, and Change LVDS LDO U14 P/N
- A-24 PAGE 32 : Add VGA Power and +1.5V_SUS Discharge Circuit
- A-25 PAGE 32,43,44 : Add +VGA_CORE,+3V_GPU,+1.5V_GPU,+1.8V_GPU,+1.0V_GPU circuits for Park LP Power
- A-26 PAGE 37~42 : Add Park LP circuits
- A-27 PAGE 30 : Change PU8 footprint
- A-28 PAGE 20 : Add VGA thermal Nut H29, Fan Hole H74 and Modify H12 footprint
- A-29 PAGE 29 : Reserve PC39,PC40,PC41,PC43 1uF for Power On/Off Fail issue(Battery Capacity less than 60%)
- A-30 PAGE 27 : Change PR95 from 180K to 200K
- A-31 PAGE 27 : Change PR98 from 237K to 280K
- A-32 PAGE 28 : Change PR148 from 5.1K to 6.8K
- A-33 PAGE 30 : Change PR168 from 40.2K to 31.2K
- A-34 PAGE 31 : Change PR96 from 10.2K to 12K
- A-35 PAGE 32 : Change PR82 from 560 to 1M
- A-36 PAGE 32 : Change PR204 from 560 to 1M
- A-37 PAGE 33 : Change PD1 & PD2 from ZD3.6V to UDZS5.6BTE-17
- A-38 PAGE 43 : Change PR7077 from 10K to 60K, PR7080 from 2K to 12K and PR7095 from 30K to 180K
- A-39 PAGE 44 : Change PU7009 & PU7011 from RT9025 to APL5920
- A-40 PAGE 29 : Change PQ4 & PQ45 from AOL1448 to RJK03B9DP
- A-41 PAGE 29 : Change PQ3, PQ7, PQ41& PQ44 from AOL1718 to RJK03D3DPA
- A-42 PAGE 32 : Change PQ7018 from AOL1718 to RJK03D3DPA
- A-43 PAGE 32 : Change PC137 & PC152 from CC71004MZ81 to CC71004MZ04

		Quanta Computer Inc.	
		PROJECT : FH1A	
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	Change List	1A	
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