

GARUM

(Mobile_Athlon64/RS480M/SB400)

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16	DIMM1	36	Reserve	56	Reserve	76	Reserve	96	Power/ PMU/ Scont
17	CPU HDT	37	Reserve	57	Reserve	77	SEQUENCE	97	Power/ PMU/ Etc
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20	RS480M GDDR	40	Reserve	60	Reserve	80	Power / DDC/CPUCore2		

Version History

Version	Date	Description

PCI REQ#/GNT#

REQ#/GNT#	Device
REQ#0	MiniPCI
REQ#1	(IEEE1394)
REQ#2	Broadcom LAN
REQ#3	PCIC / IEEE1394
REQ#4	
REQ#5	PCIC

PCI BUS NUMBER = #0

Device#	Function#	Device
17	0	SB400 Serial ATA #1
18	0	SB400 Serial ATA #0
19	0	SB400 OHCI USB Controller #1
19	1	SB400 OHCI USB Controller #2
19	2	SB400 EHCI USB Controller
20	0	SB400 SMBus Controller
20	1	SB400 IDE Controller
20	3	SB400 LPC Controller
20	4	SB400 PCI to PCI Bridge
20	5	AC'97 Audio Controller
20	6	AC'97 Modem Controller

PCI BUS NUMBER = #10

IDSEL	Device#	Device
AD24	8	PCIC/IEEE1394
AD25	9	Broadcom LAN
AD26	10	MiniPCI
AD27	11	(IEEE1394)

SMBUS ADDRESS

ADDRESS	Device
A0h	LCD(SPWG)
A2h	DIMM0
A4h	DIMM1
5Eh	Thermal Sensor(MAX6640)
D2h	PLL(ICS951412)
32h	PMU(LUNA)

PCI INTERRUPT

PCIINT#	Device
INT#0	
INT#1	
INT#2	
INT#3	
INT#4	PCIC(Slot1), PCIC(MS/SD), Broadcom LAN
INT#5	
INT#6	MiniPCI 1 (IEEE1394)
INT#7	MiniPCI 2

Net Name	S0	S3	S4	S5	G3	AC Battery OFF
PWR_xxMAIN PWR_CPUCORE	ON	OFF	OFF	OFF	OFF	OFF
PWR_xxSUS	ON	ON	OFF	OFF	OFF	OFF
PWR_xxSTD	ON	ON	ON	ON	OFF	OFF
PWR_PMU	ON	ON	ON	ON	ON	OFF
PWR_RTC	ON	ON	ON	ON	ON	ON

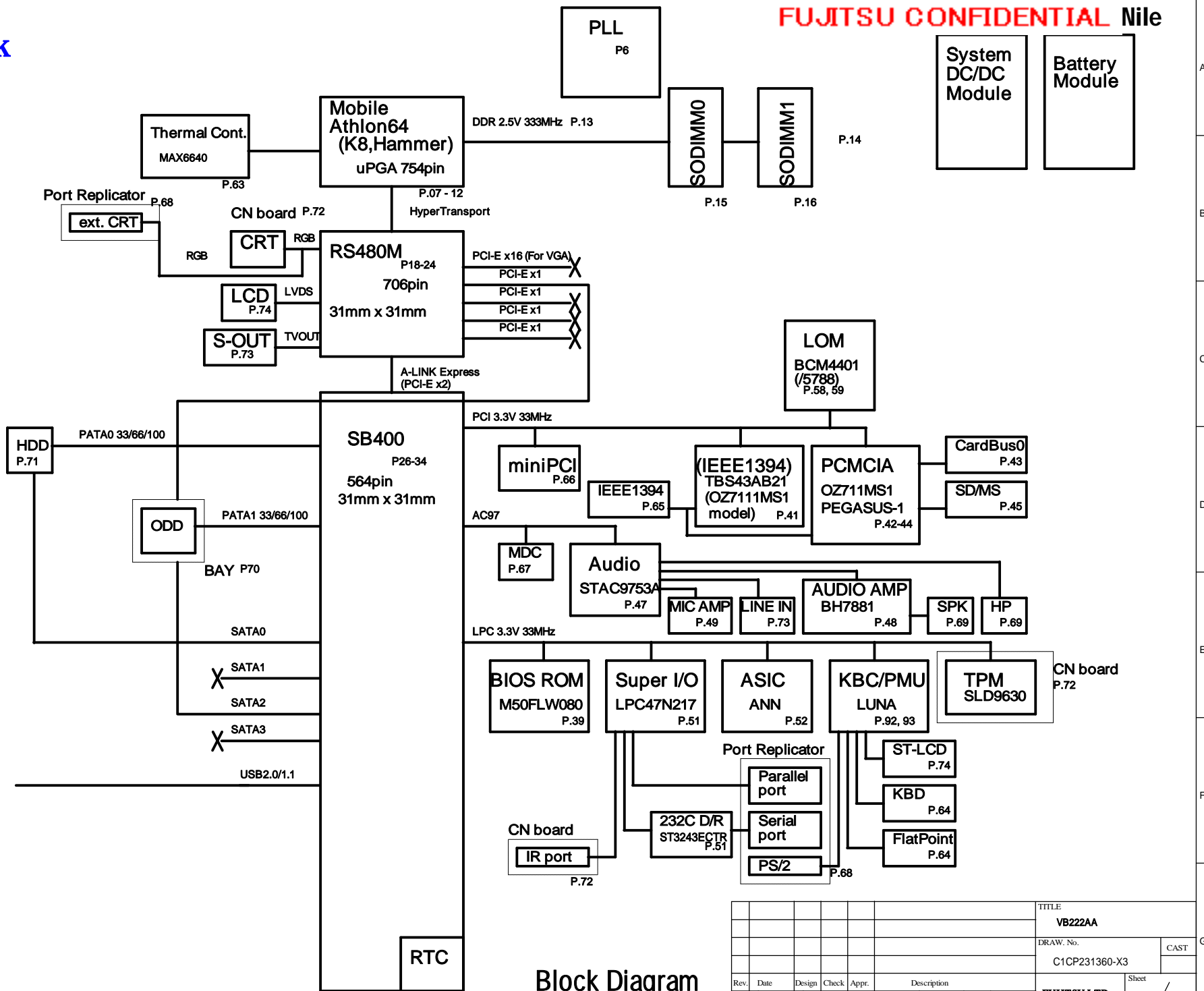
Top Page



Rev.						Date	Design	Check	Appr.	Description	Rev. / Sheet	
											FUJITSU LTD.	1 / 99
						2005/06/27	KOSHA	Check		2005/06/27 Yamada	Appr.	Miura
TITLE											Sheet	
VB222AA											1 / 99	
DRAW. No.											CAST	
C1CP231360-X3												

System block diagram

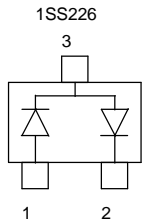
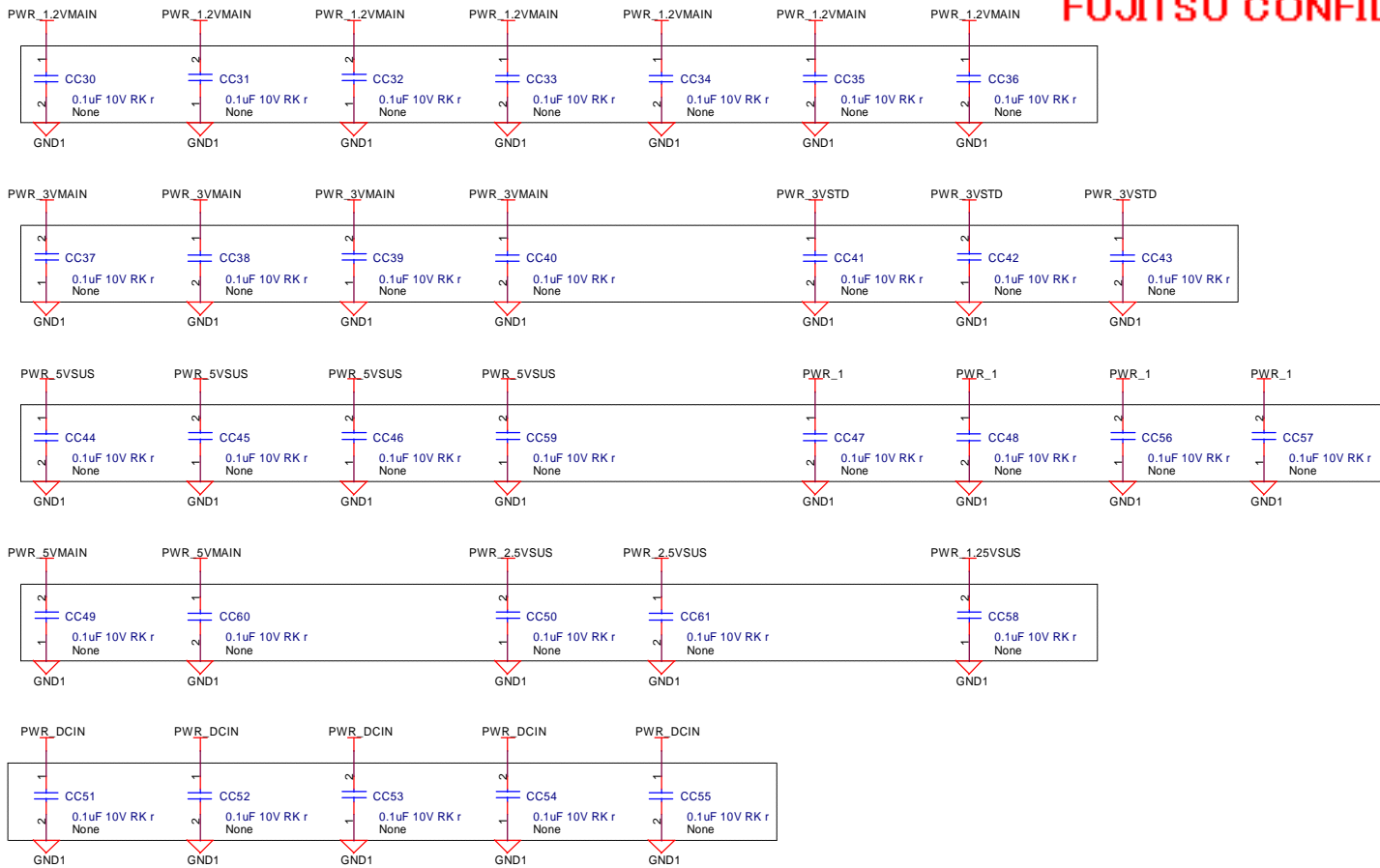
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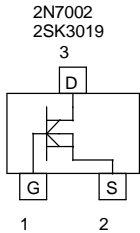
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Block Diagram

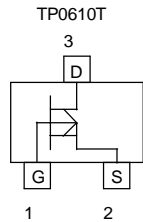
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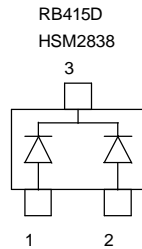
MP009



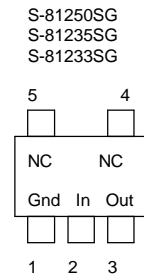
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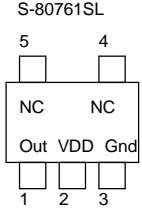
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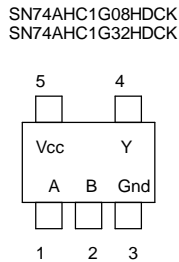
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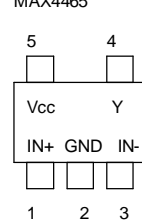
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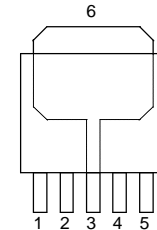
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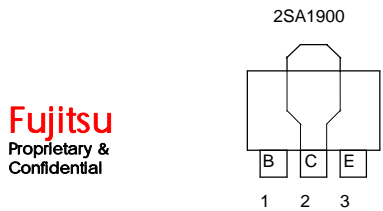
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MP012



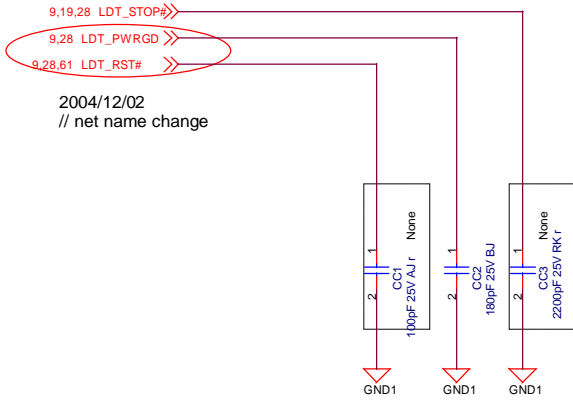
MP027



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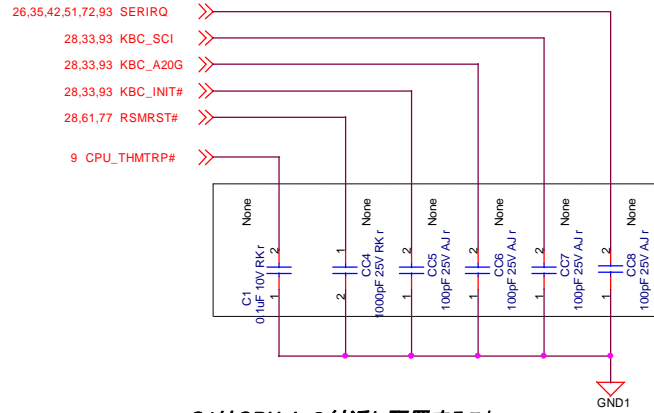
R-C for EMI

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Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.
Design	//	KOSHA	Check		Appr.		Sheet 3 / 99	

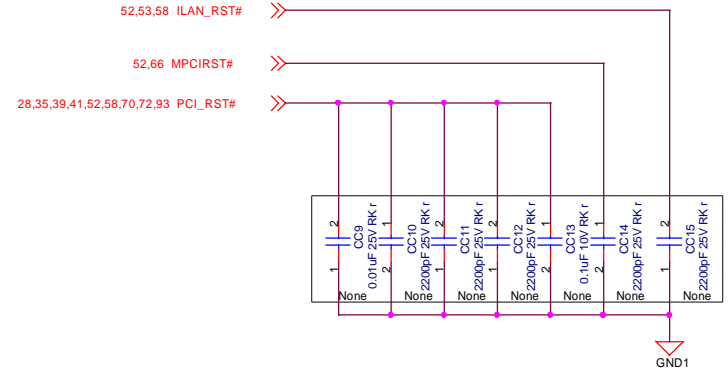


2004/12/02
// net name change

上記部品はCPUのピン近くに配置すること。



C1はCPUpinの付近に配置すること
上記部品はSB400(M5)のピン近くに配置すること。

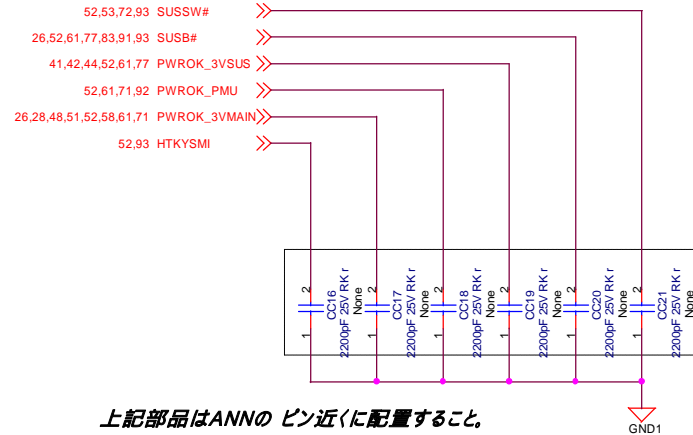


CC12,13,14,15,16はそれぞれデバイスの受端ピン近くに配置すること。

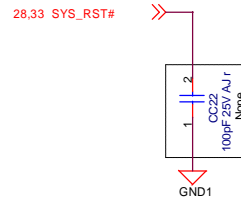
CC18はRealtekのピン近くに配置すること。

CC17はMiniPCI CN近くに配置すること。

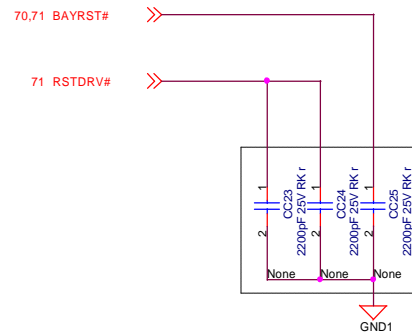
上記部品はネットの終端に配置すること。



上記部品はANNのピン近くに配置すること。

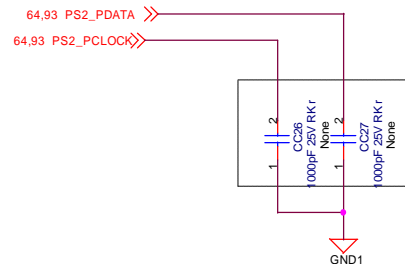


上記部品はSB400のピン近くに配置すること。



CC28はHDD-CNDのピン近くに配置すること。

CC30はBAY-CNDのピン近くに配置すること。



上記部品はLUNAのピン近くに配置すること。

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check					
							FUJITSU LTD.	
							Sheet	
							4 / 99	

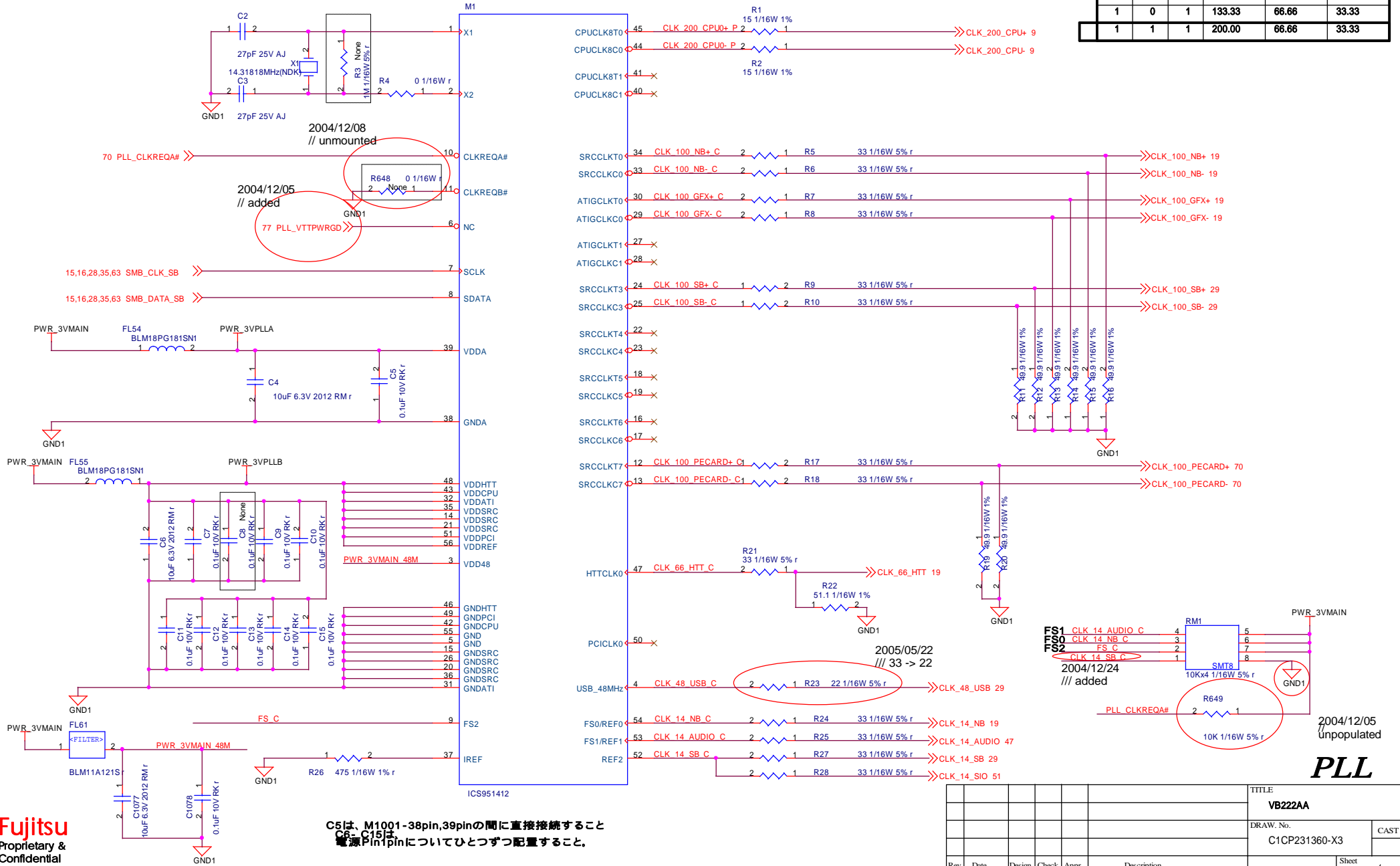
RESERVED

FG-CN

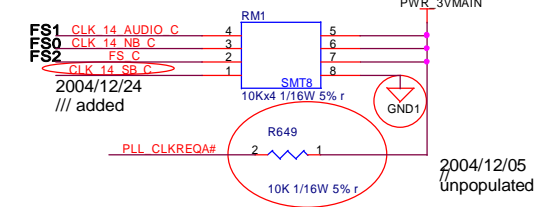
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										TITLE	VB222AA	
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Rev.	Date	Design	Check	Appr.	Description							
Design	//	KOSHA	Check				Appr.			FUJITSU LTD.	Sheet	5 / 99

			Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	36.56	73.12
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

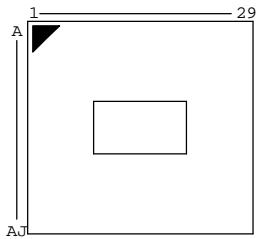


C5は、M1001-38pin,39pinの間に直接接続すること。
電源Pin1pinについてひとつずつ配置すること。

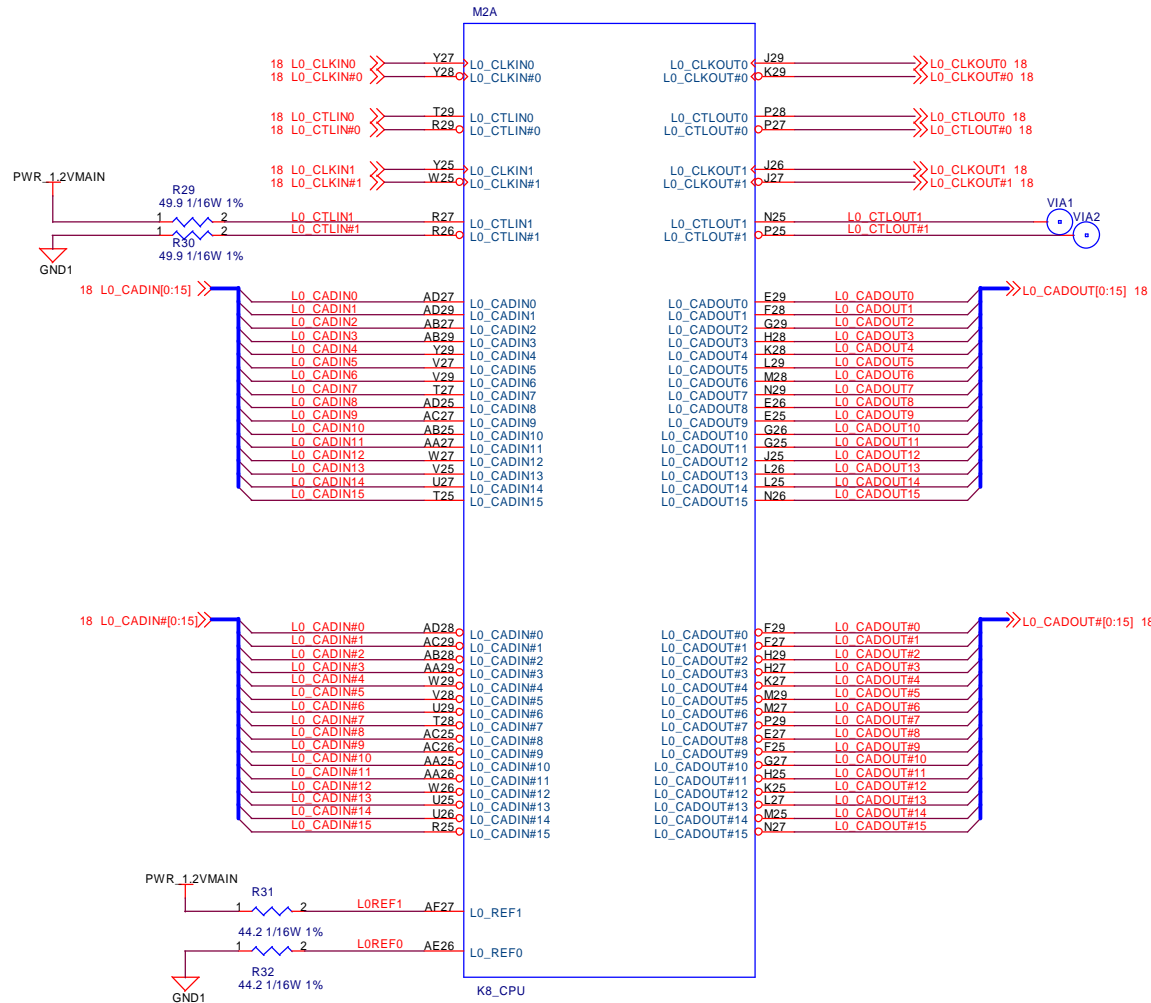


PLL

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				6 / 99	
Rev.	Date	Design	Check	Appr.	Description
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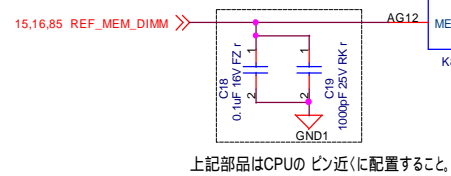
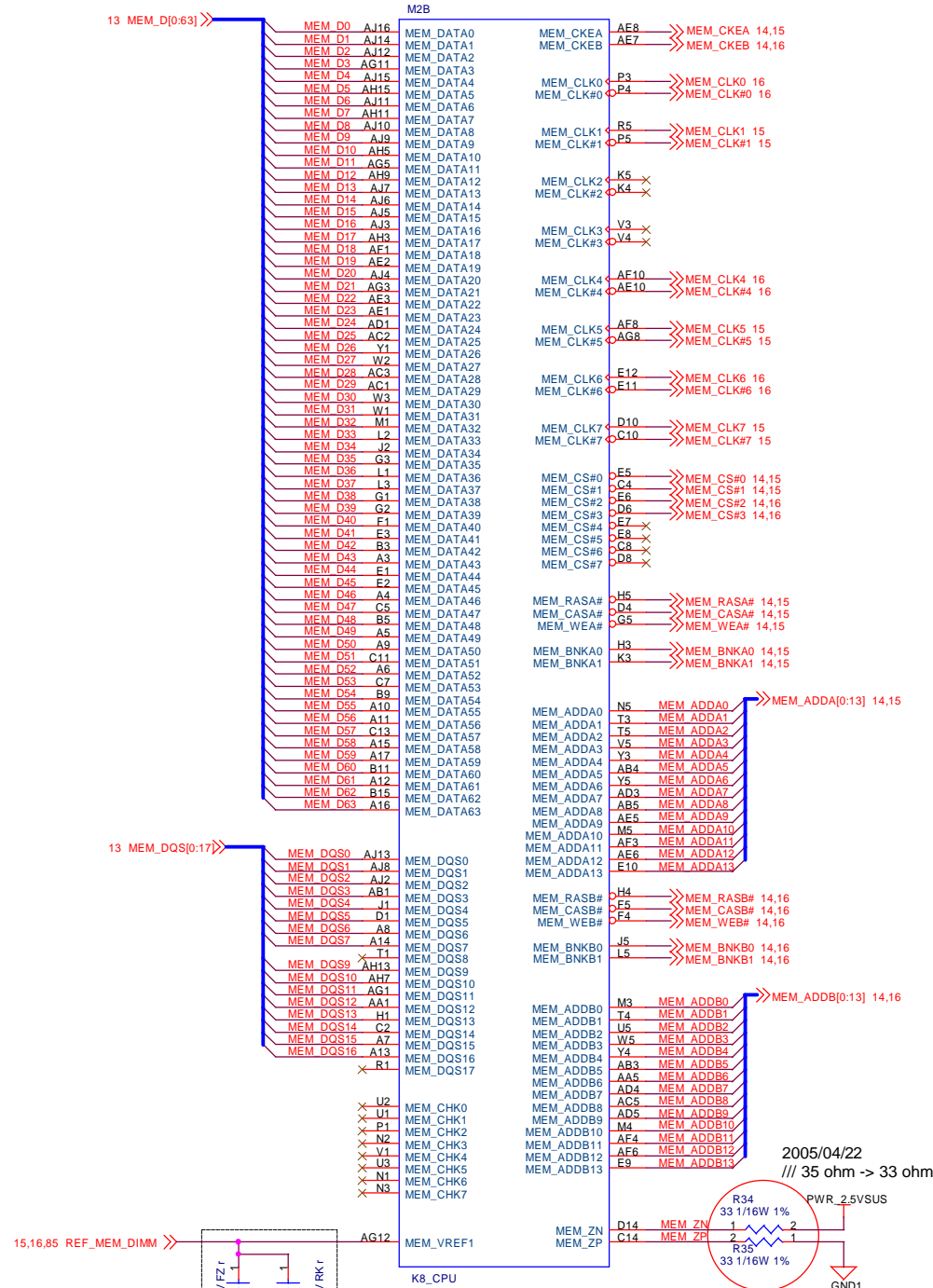
CLAWHAMMER TOP VIEW



LOREF0,LOREF1は0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R1046,R1047は25.4mm以内に配置すること。

K8-1

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check			Appr.		
							FUJITSU LTD.	
							Sheet	
							7 / 99	

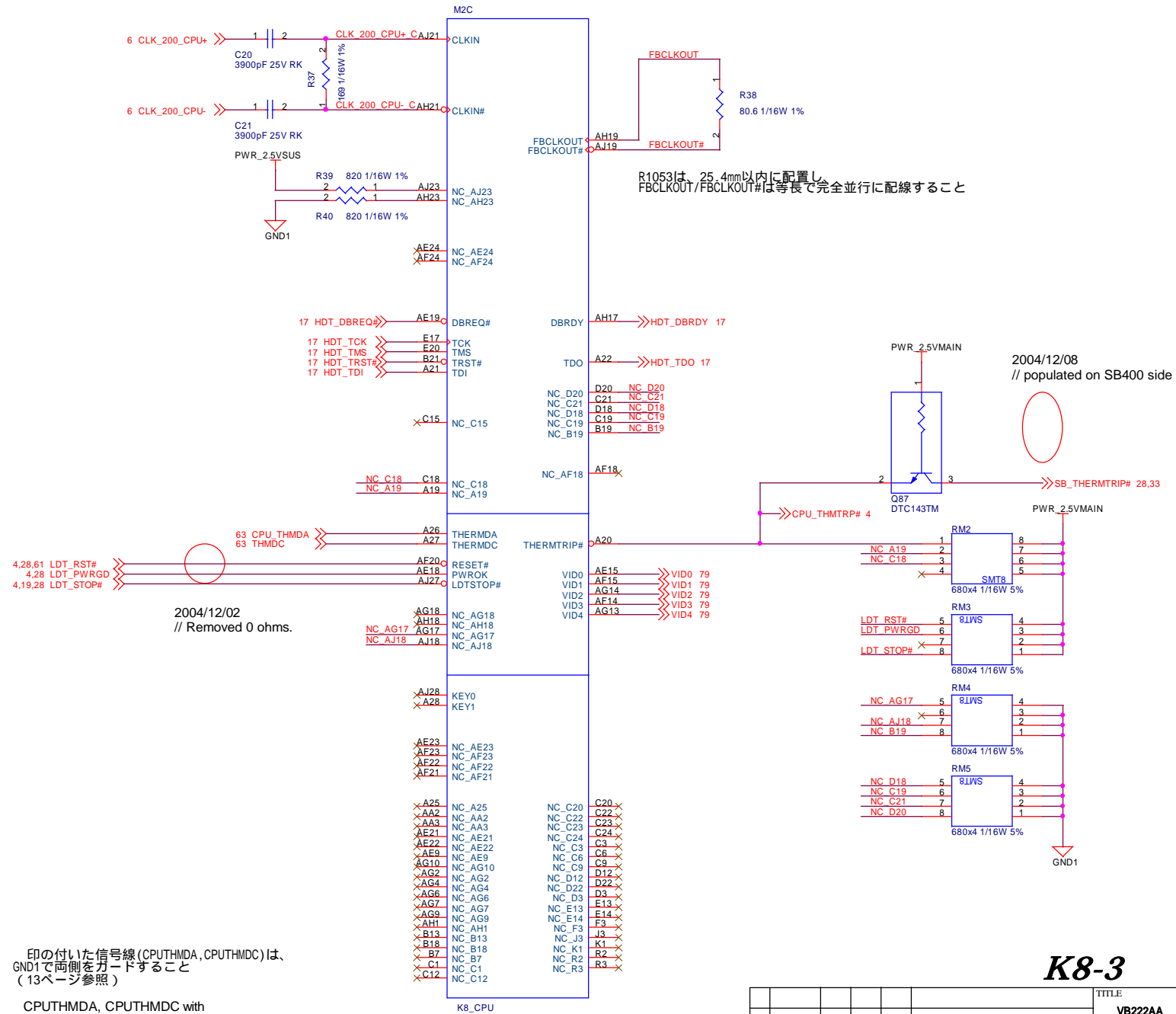


上記部品はCPUのピン近くに配置すること。

MEM_ZN, MEM_ZPは0.127mmの線幅にて配線し、他の信号から0.254mm以上離すこと。
R1049, R1050は25.4mm以内に配置すること。

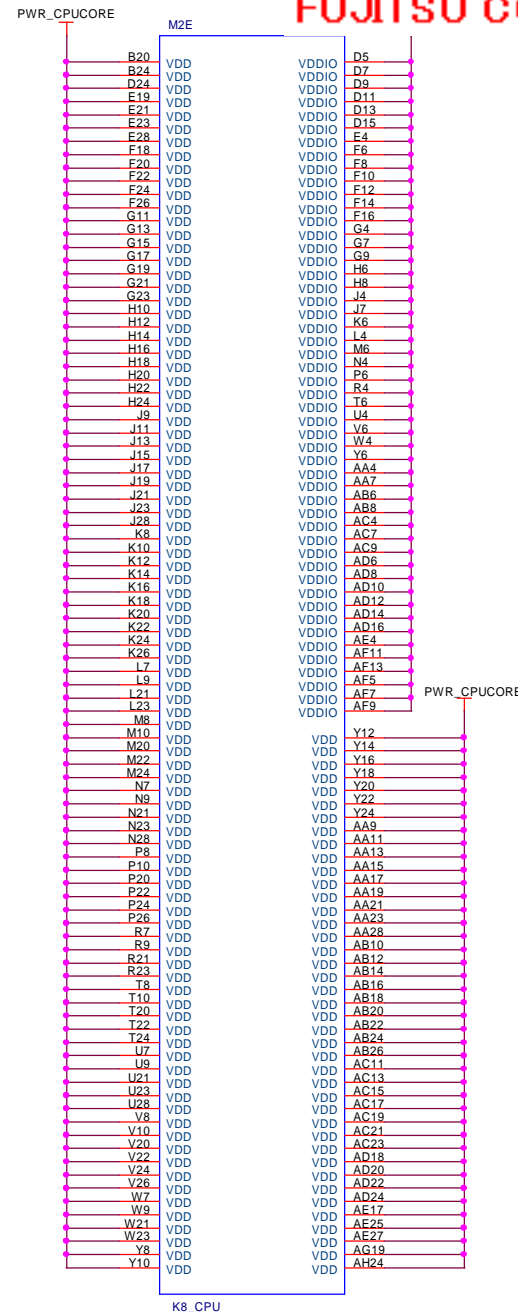
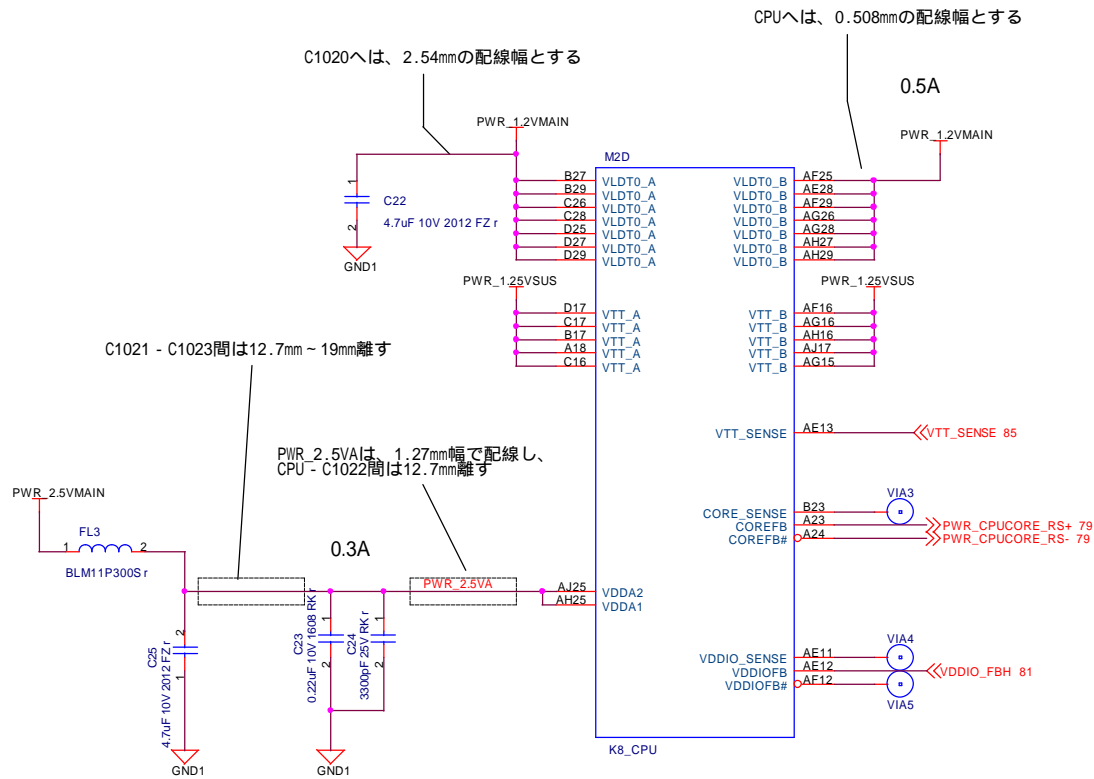
K8-2

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Design	/ /	KOSHA	Check		Appr.			8 / 99
							FUJITSU LTD.	



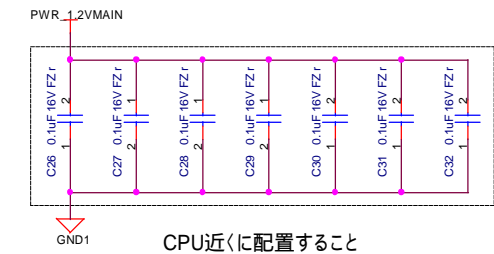
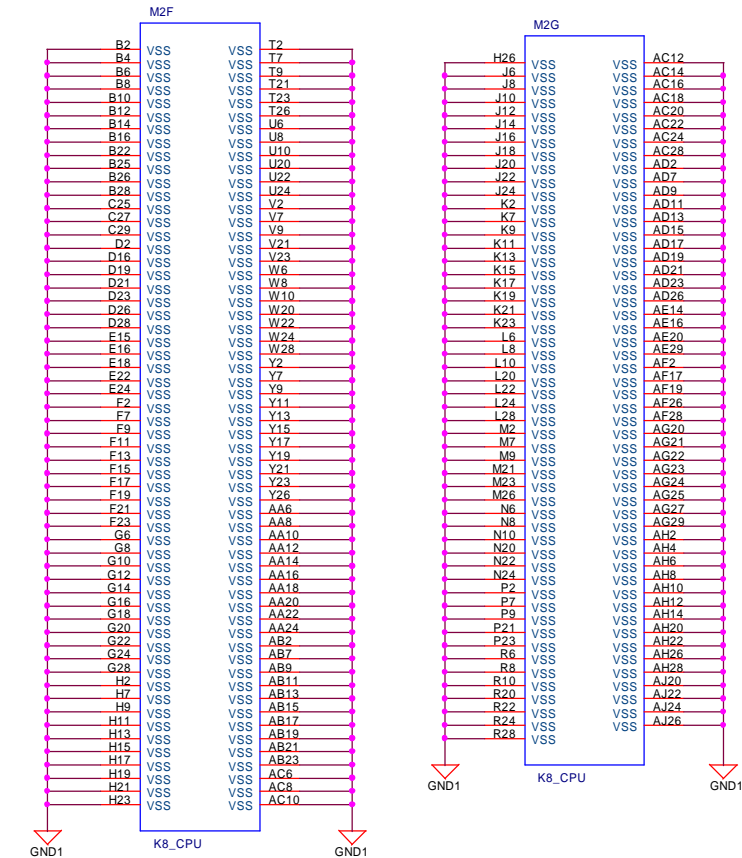
K8-3

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Rev.	Date	Design	Check	Appr.	Description			
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							FUJITSU LTD.	

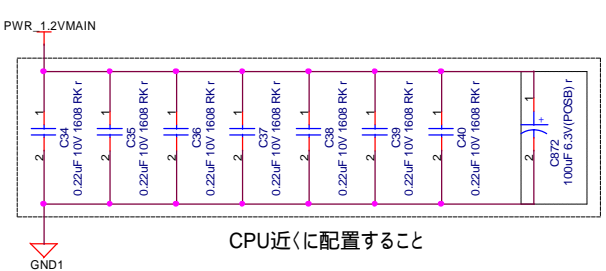


K8-4

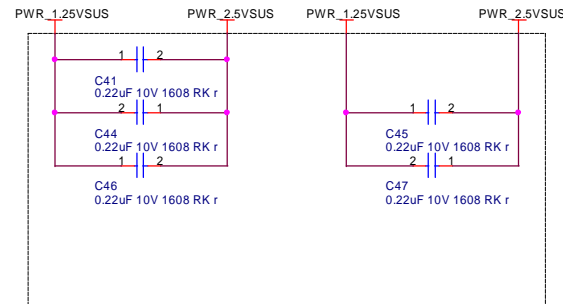
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						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	/ /	KOSHA	Check		Appr.		
						FUJITSU LTD.	
						Sheet 10 / 99	



CPU近くに配置すること

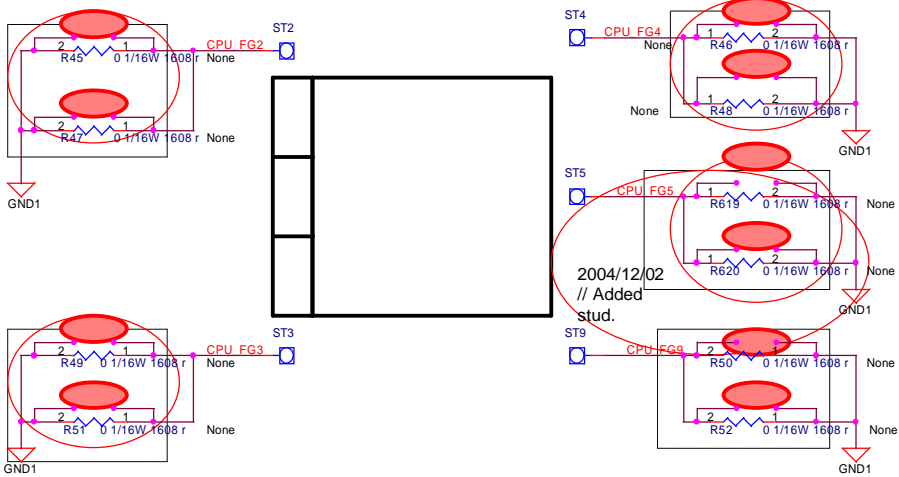


CPU近くに配置すること



PWR_1.25VSUSに沿って均等に配置 (12ページ参照)
 #04,12,17 Delete parts
 C49,C50,C51,C52

K8-5



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							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.		11 / 99	
							FUJITSU LTD.	

CPU逆面の外周に配置

Place on backside under socket. CPU逆面の中央に配置

CPU近くに配置すること
Place close to CPU socket.

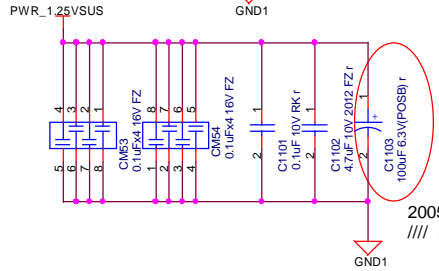
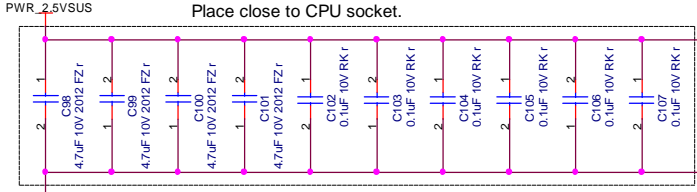
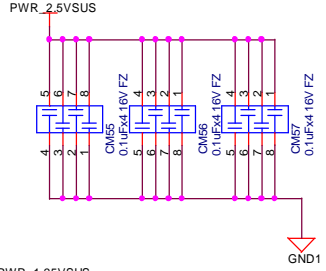
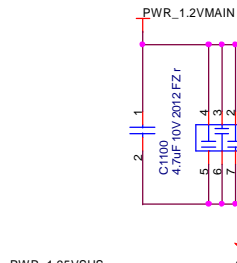
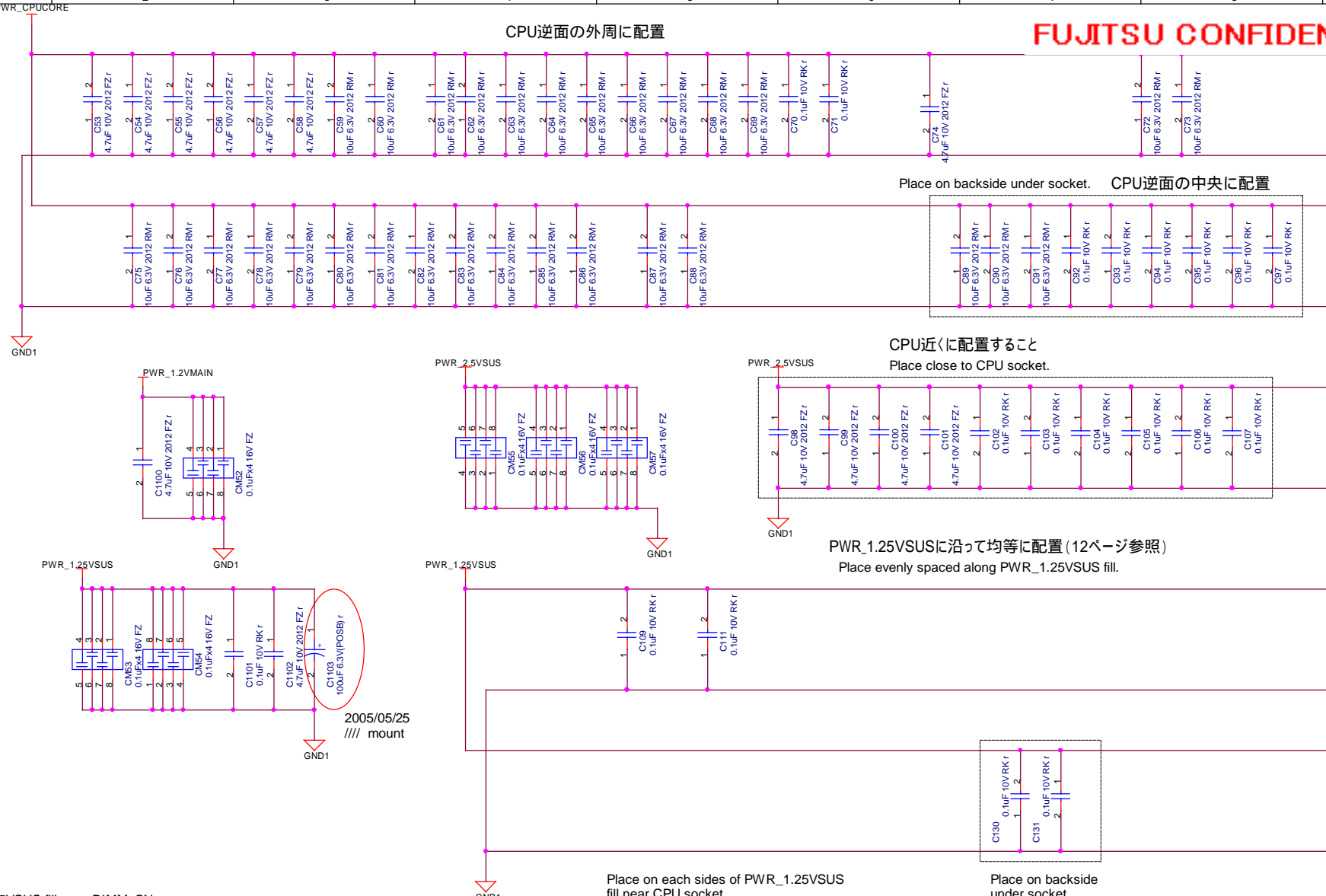
PWR_1.25VSUSに沿って均等に配置 (12ページ参照)
Place evenly spaced along PWR_1.25VSUS fill.

Place on each sides of PWR_1.25VSUS fill near CPU socket.
CPUへの入り口部分に配置

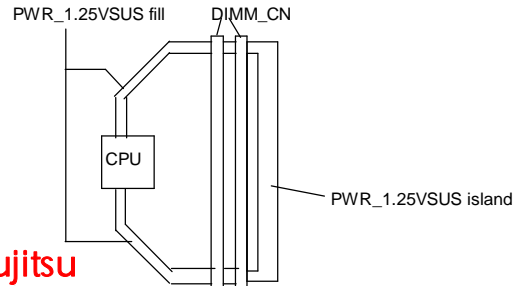
Place on backside under socket.
CPU逆面の中央に配置

#04.12.17 Delete parts
C113,C115,C117,C119,C121,C123,C125,C127,C129,C128,C126
C114,C116,C118,C120,C122,C124

CPU PASS_C



2005/05/25
//// mount

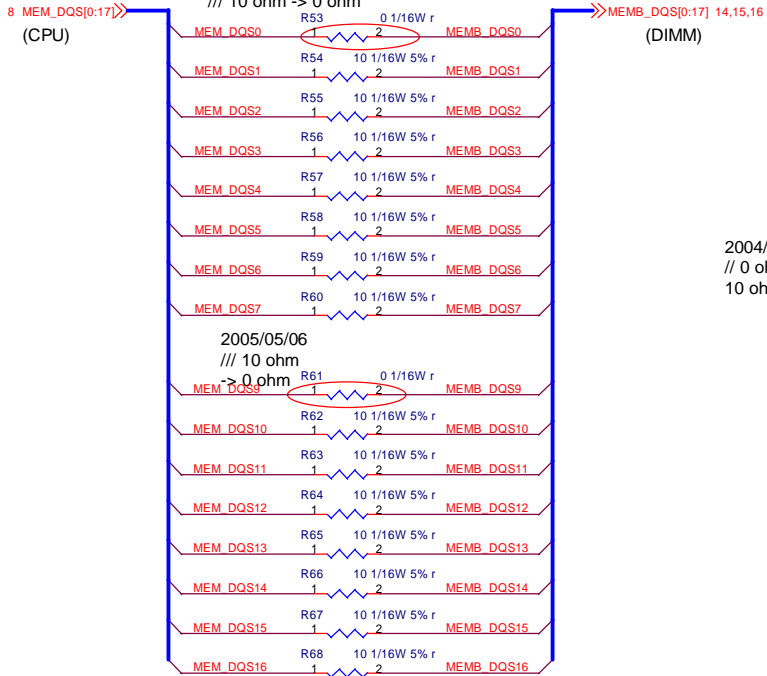


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							CAST	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.
Design	//	KOSHA	Check		Appr.		Sheet 12 / 99	

DIMM_CN側に配置
Place these resistors close to DIMM_CN.

2005/05/06

/// 10 ohm -> 0 ohm



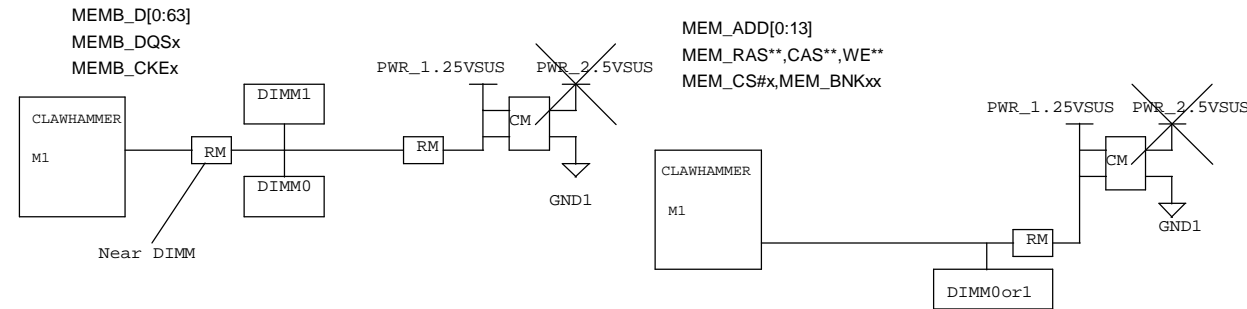
DIMM_C
Place these resist

FUJITSU CONFIDENTIAL Nile



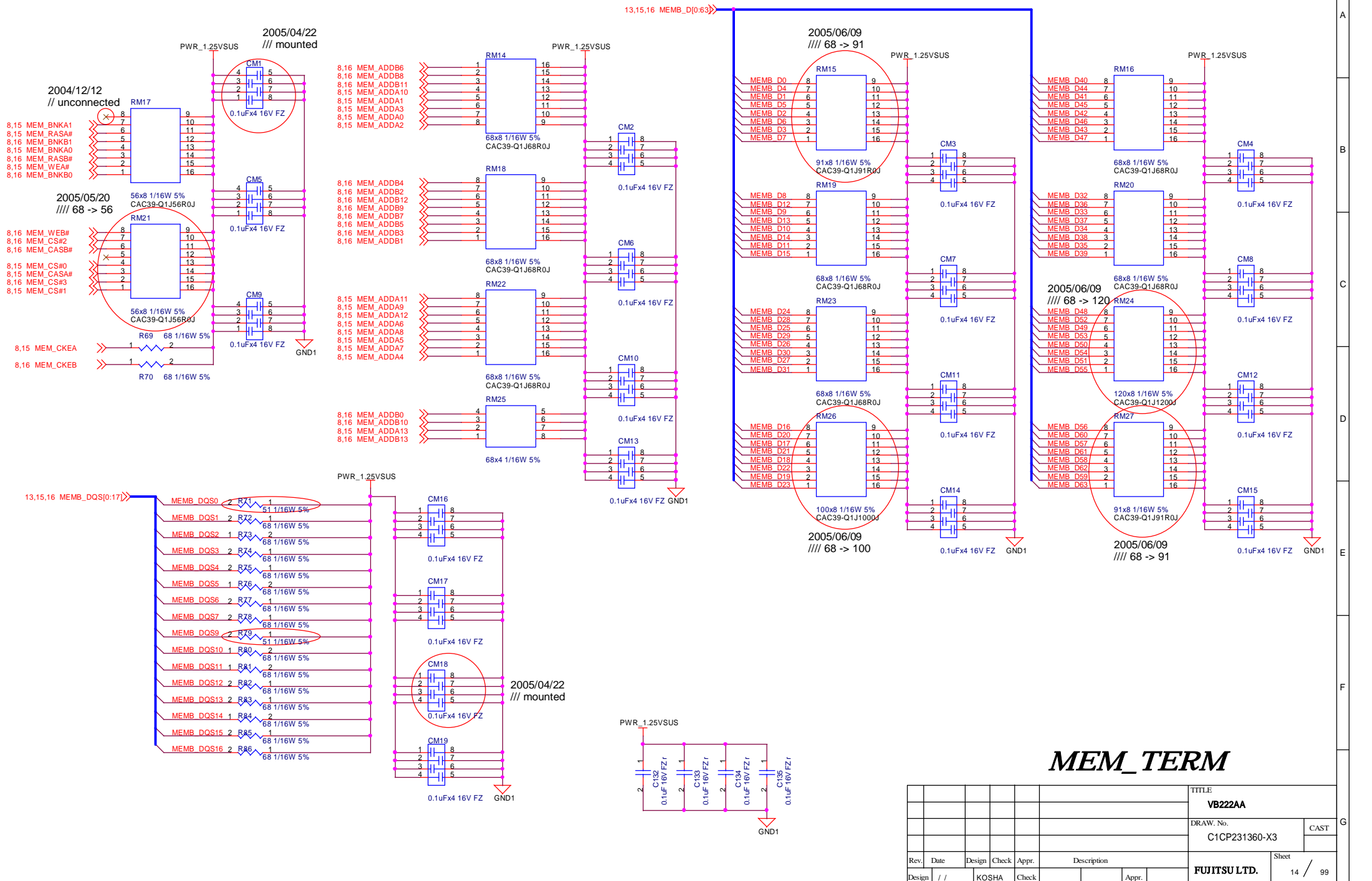
Data系
(Dx,DQSx,CKEx)

Address/Command系
(RAS#,CAS#,WE#,ADDx)



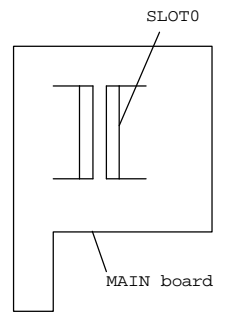
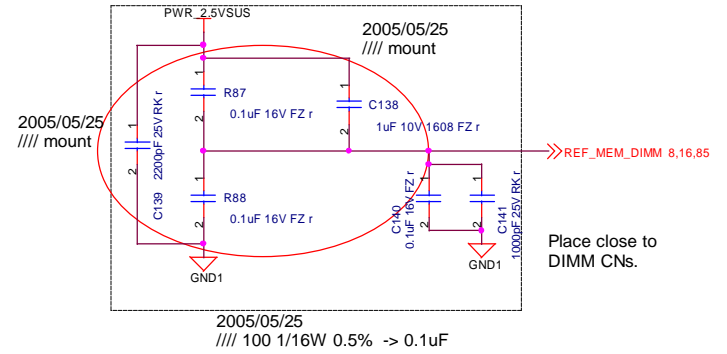
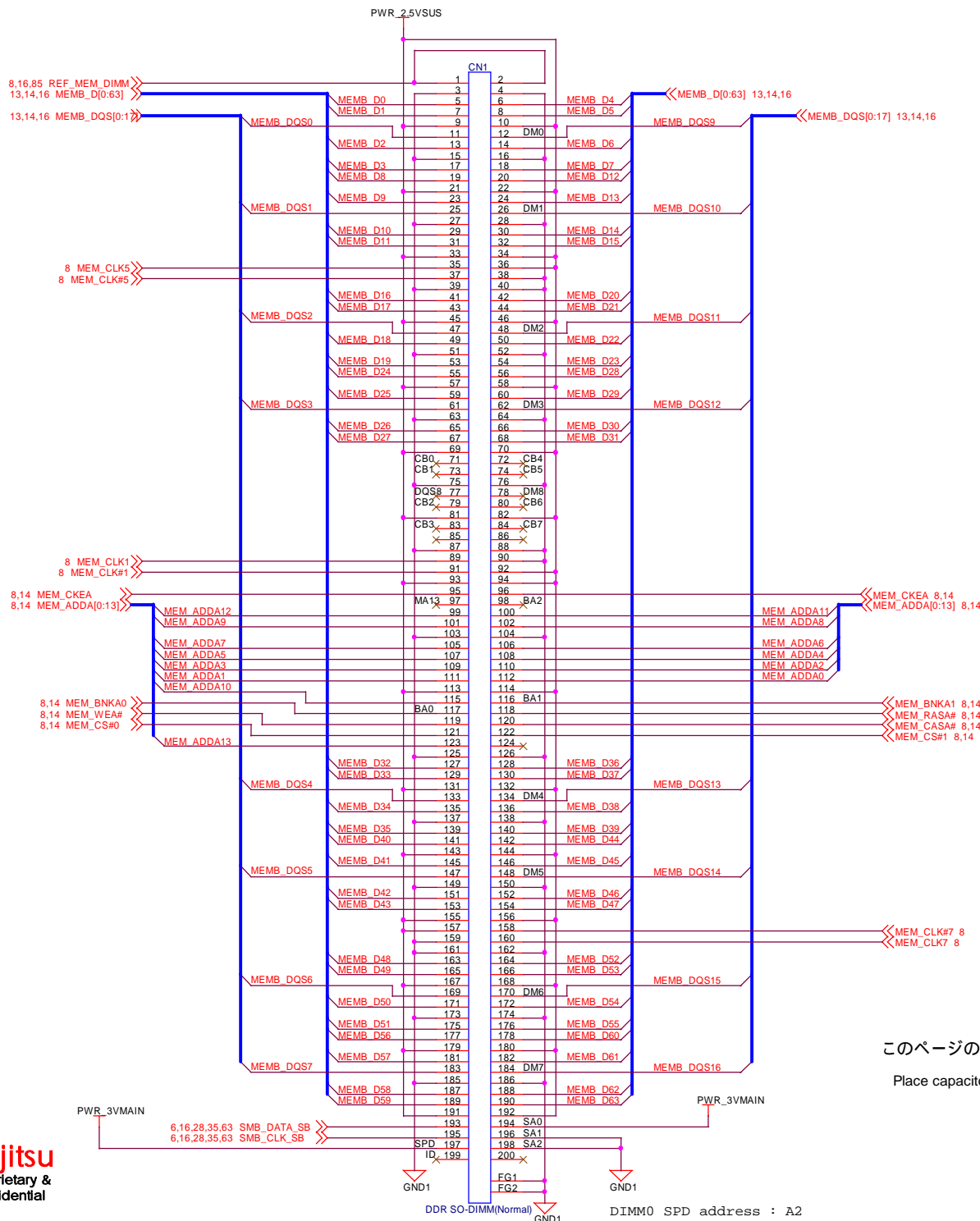
MEM_SERIES
TERMINATION

							TITLE	
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Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check	Appr.	FUJITSU LTD.			
							Sheet	13 / 99



MEM_TERM

							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHA	Check					14 / 99
							FUJITSU LTD.	

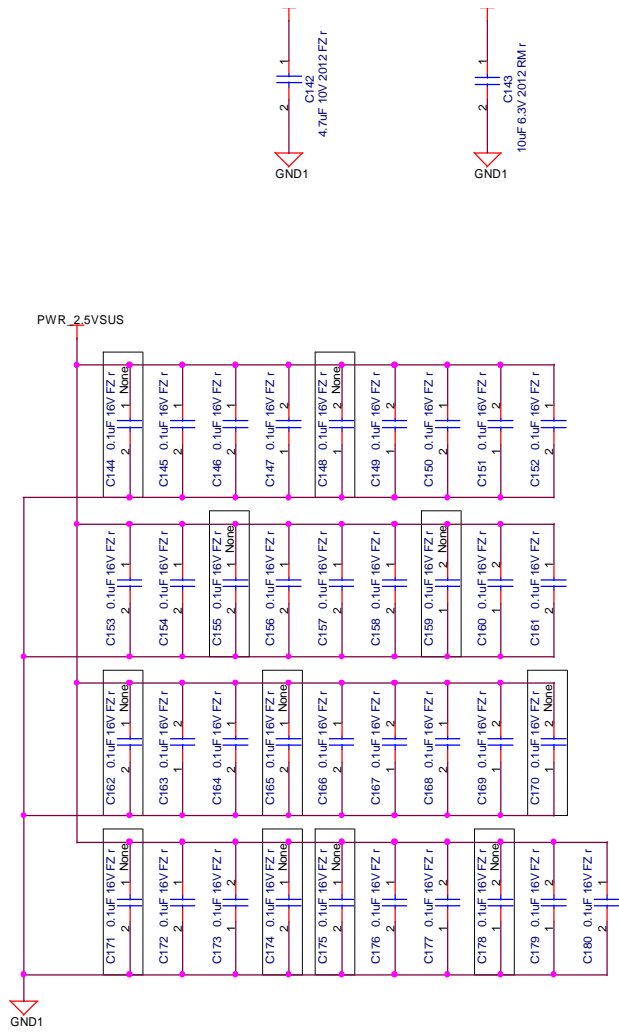
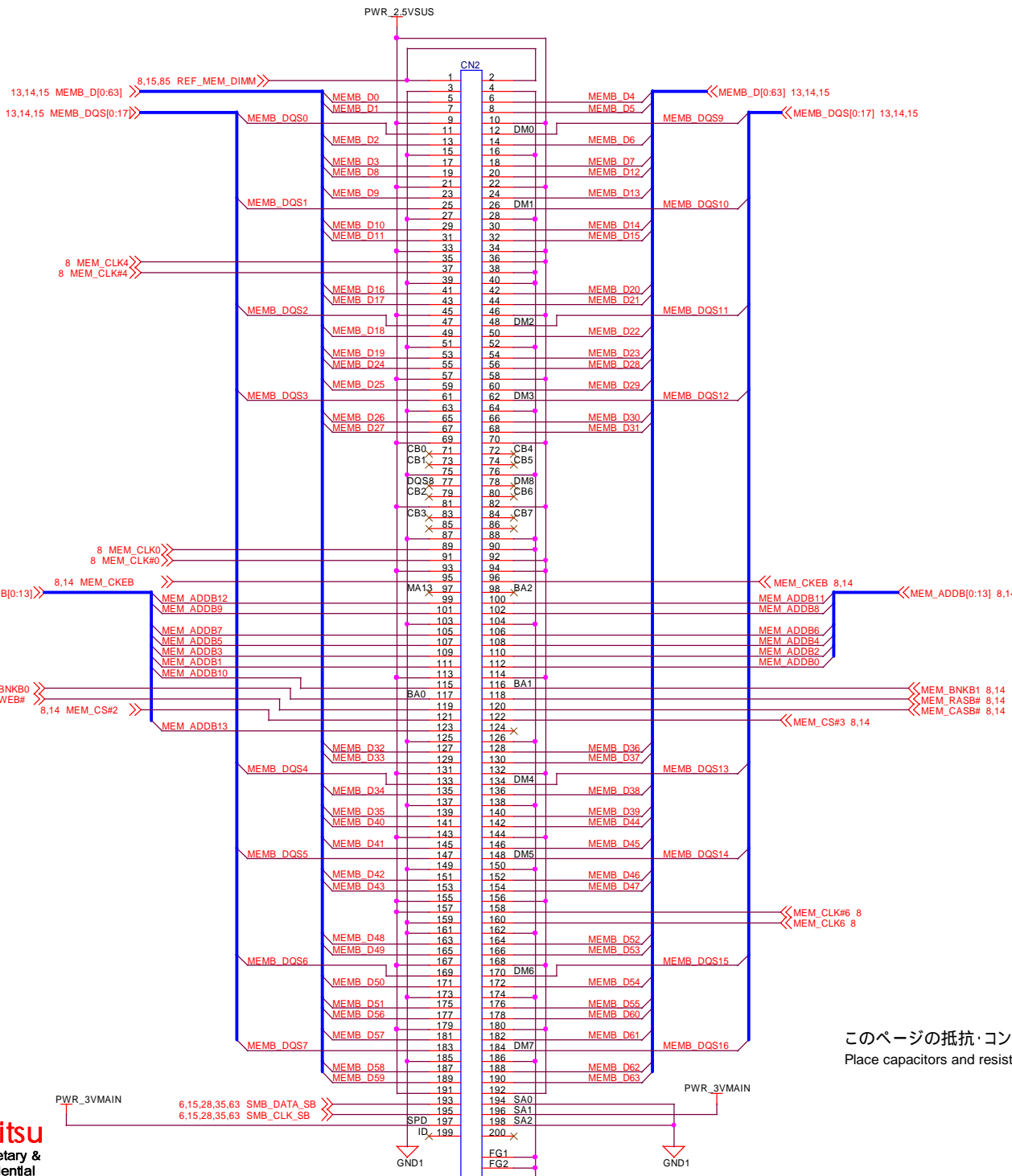


このページの抵抗・コンデンサは、DIMM_CN近くに配置
Place capacitors and resistors in this page close to DIMM_CN.

SO-DIMM0

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						TITLE	
						VB222AA	
						DRAW. No.	
						C1CP231360-X3	
						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	/ /	KOSHA	Check		Appr.		
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						15 / 99	



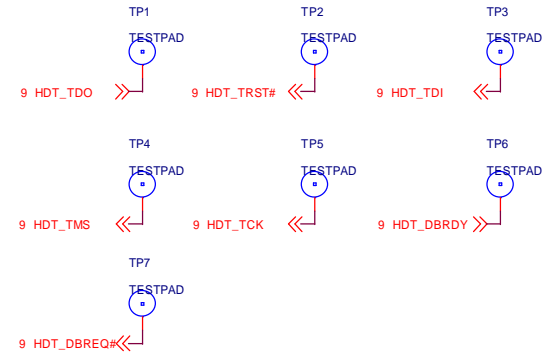
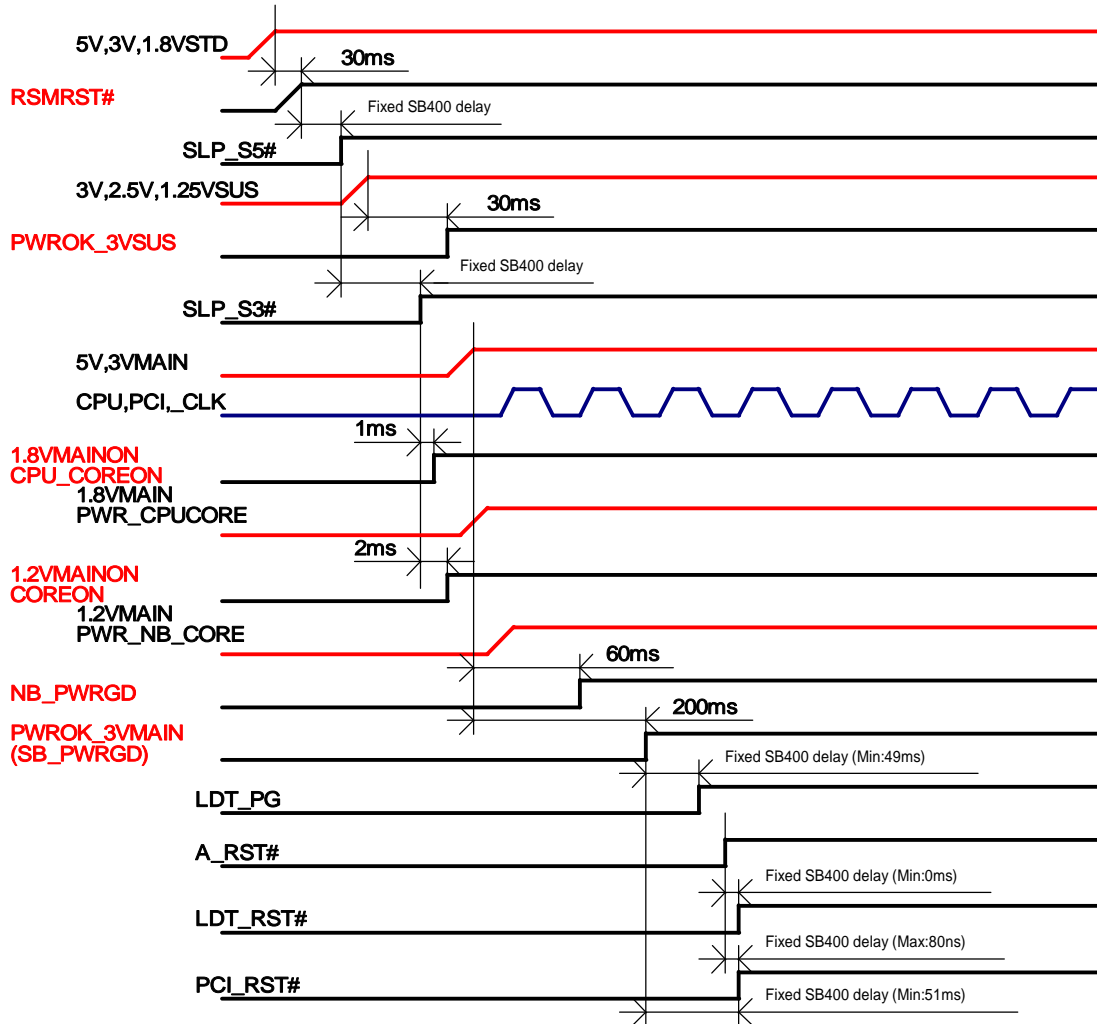
このページの抵抗・コンデンサは、DIMM_CN近くに配置
Place capacitors and resistors in this page close to DIMM_CN.

SO-DIMM1



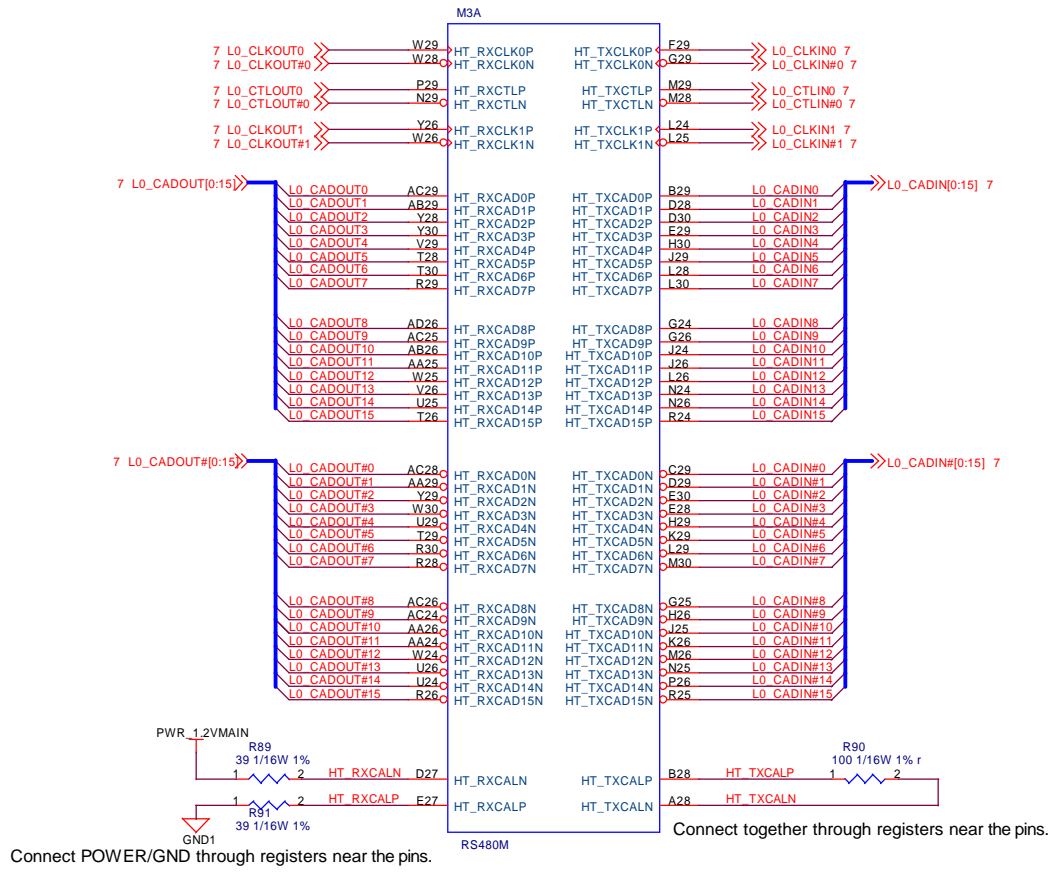
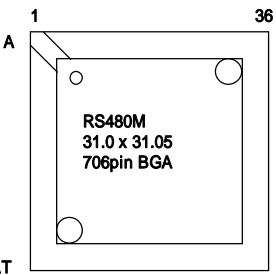
						TITLE VB222AA	
						DRAW. No. C1CP231360-X3	
						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	/ /	KOSHIA	Check		Appr.		
						FUJITSU LTD.	
						Sheet 16 / 99	

DDR SO-DIMM(Reverse) DIMM1 SPD address : A4



HDT

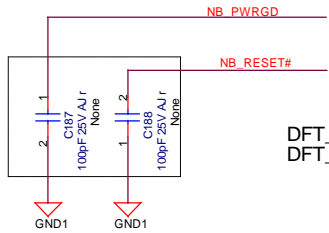
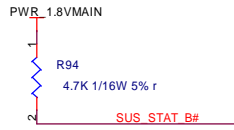
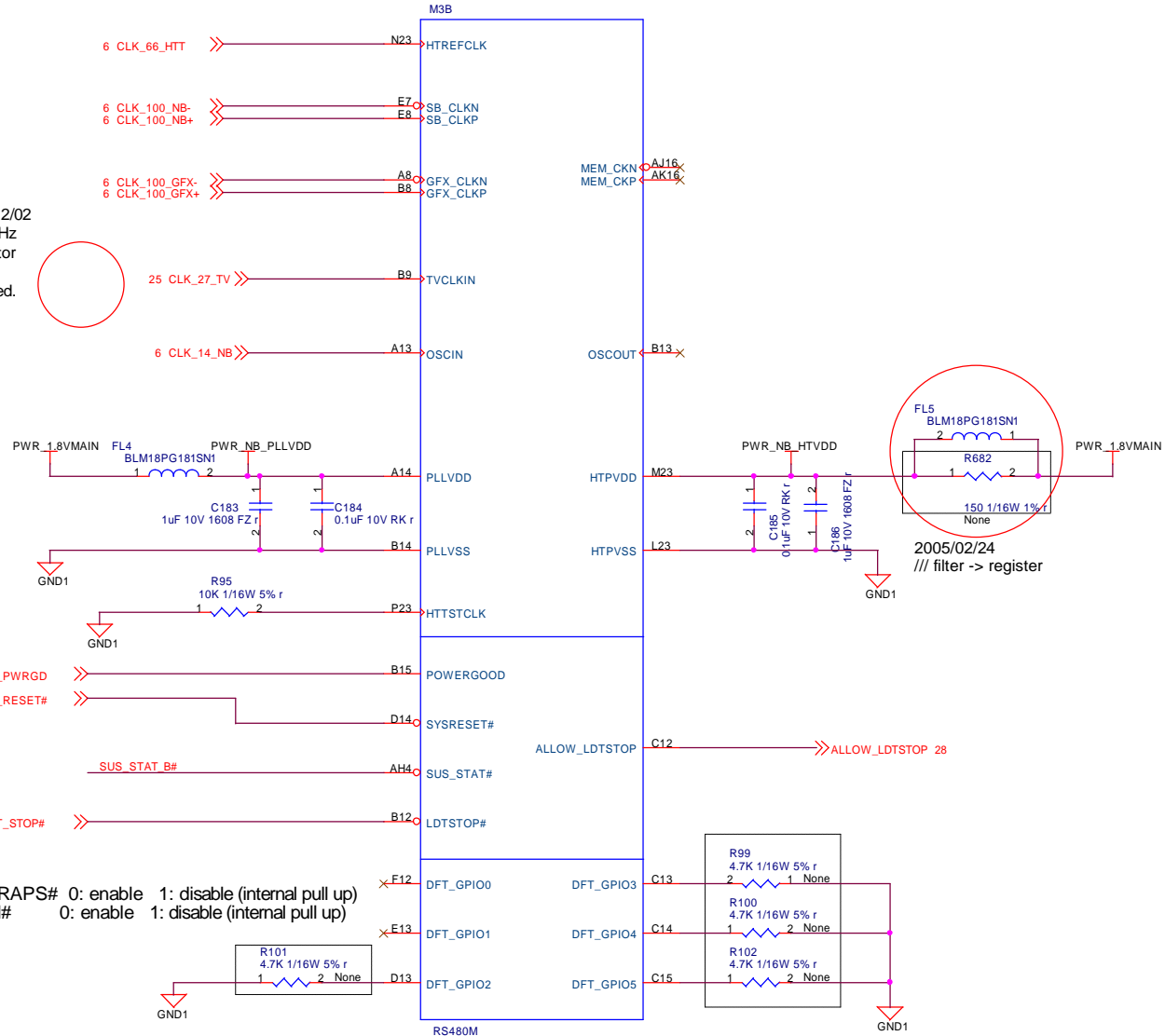
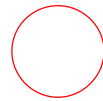
					TITLE		VB222AA	
					DRAW. No.		C1CP231360-X3	
					CAST			
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check			Appr.	FUJITSU LTD.	
							Sheet	17 / 99



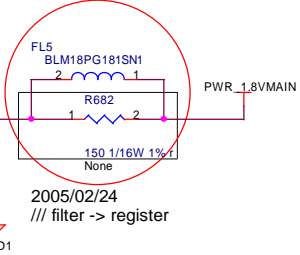
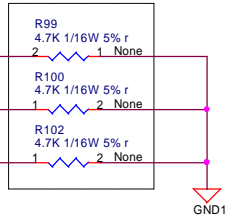
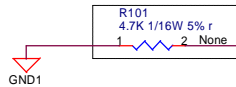
								TITLE	
								VB222AA	
								DRAW. No.	
								C1CP231360-X3	
								CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	/ /	KOSHA	Check					FUJITSU LTD.	
								18 / 99	

S-video
Place near to RS480

2004/12/02
// 27MHz
oscillator
was
removed.



DFT_GPIO1 LOAD_ROM_STRAPS# 0: enable 1: disable (internal pull up)
DFT_GPIO0 SIDE_PORT_EN# 0: enable 1: disable (internal pull up)



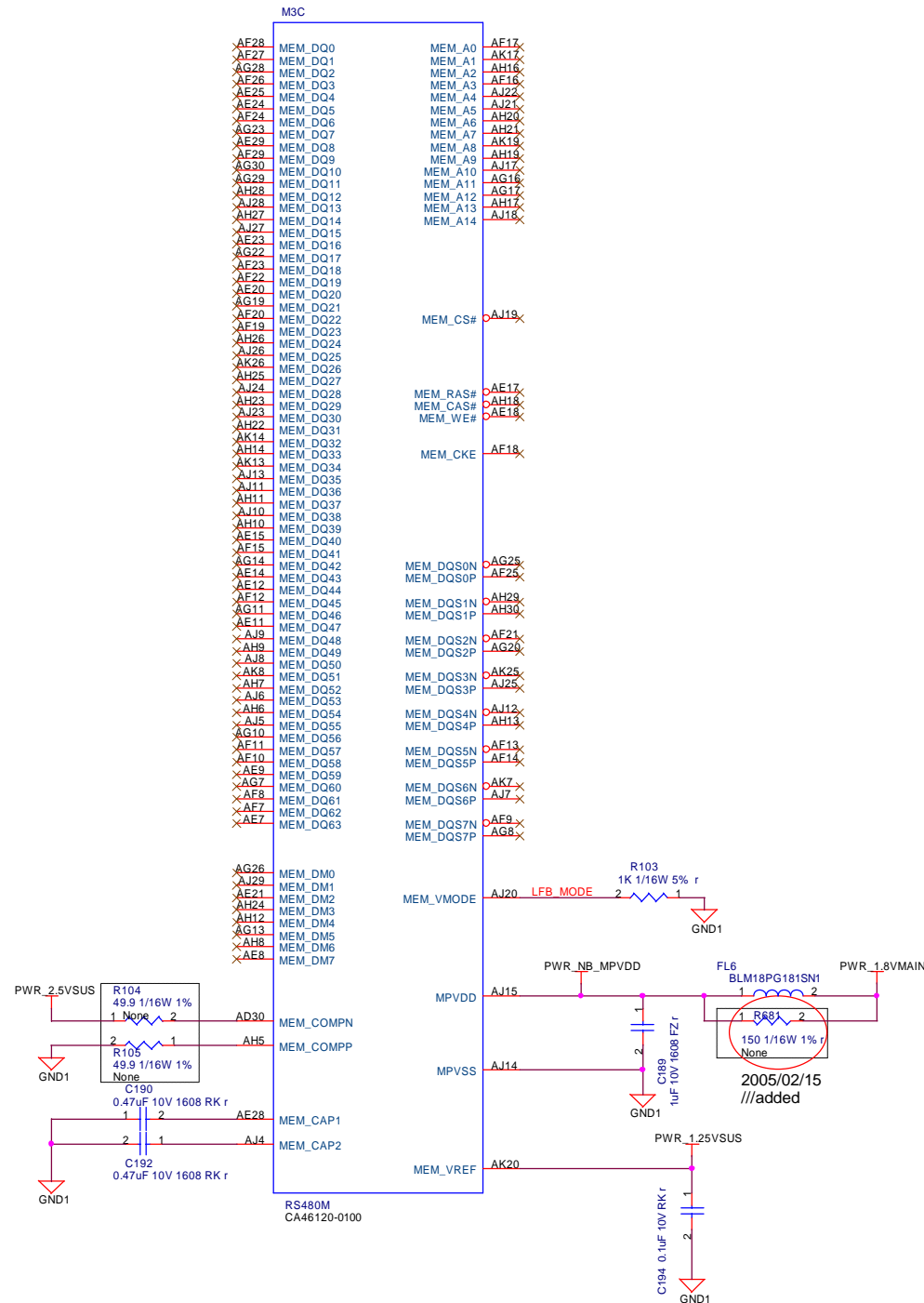
2005/02/24
// filter -> register

以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
PLLVSS(B14pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1200 : PLLVDD(A14pin)とPLLVSS(B14pin)の間

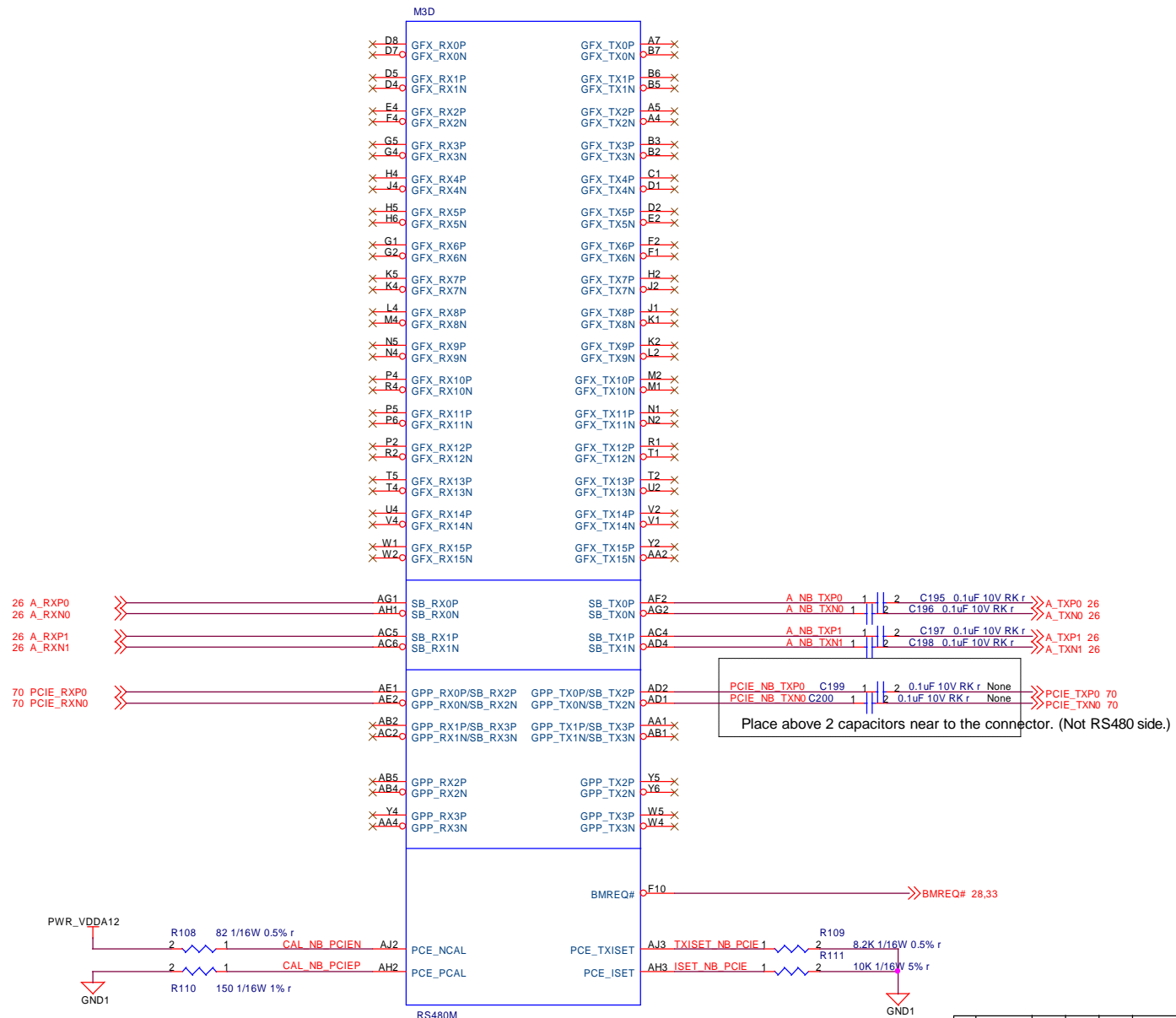
Signal Name	Function	High(Internal Pullup)	Low
LFB.EN#	SIDE_PORT_EN#	Side Port Memory Disable	Side Port Memory Enable
LOAD_ROM#	LOAD_ROM_STRAPS#	Load Rom Strap Disable	Load Rom Strap Enable

							TITLE VB222AA		
							DRAW. No. C1CP231360-X3		
							CAST		
Rev.	Date	Design	Check	Appr.	Description			Fujitsu LTD.	Sheet 19 / 99
Design	/ /	KOSHA	Check		Appr.				



LFB_VREFは、0.508mm以上の幅で配線し、他の信号からは0.508mm以上離すこと。

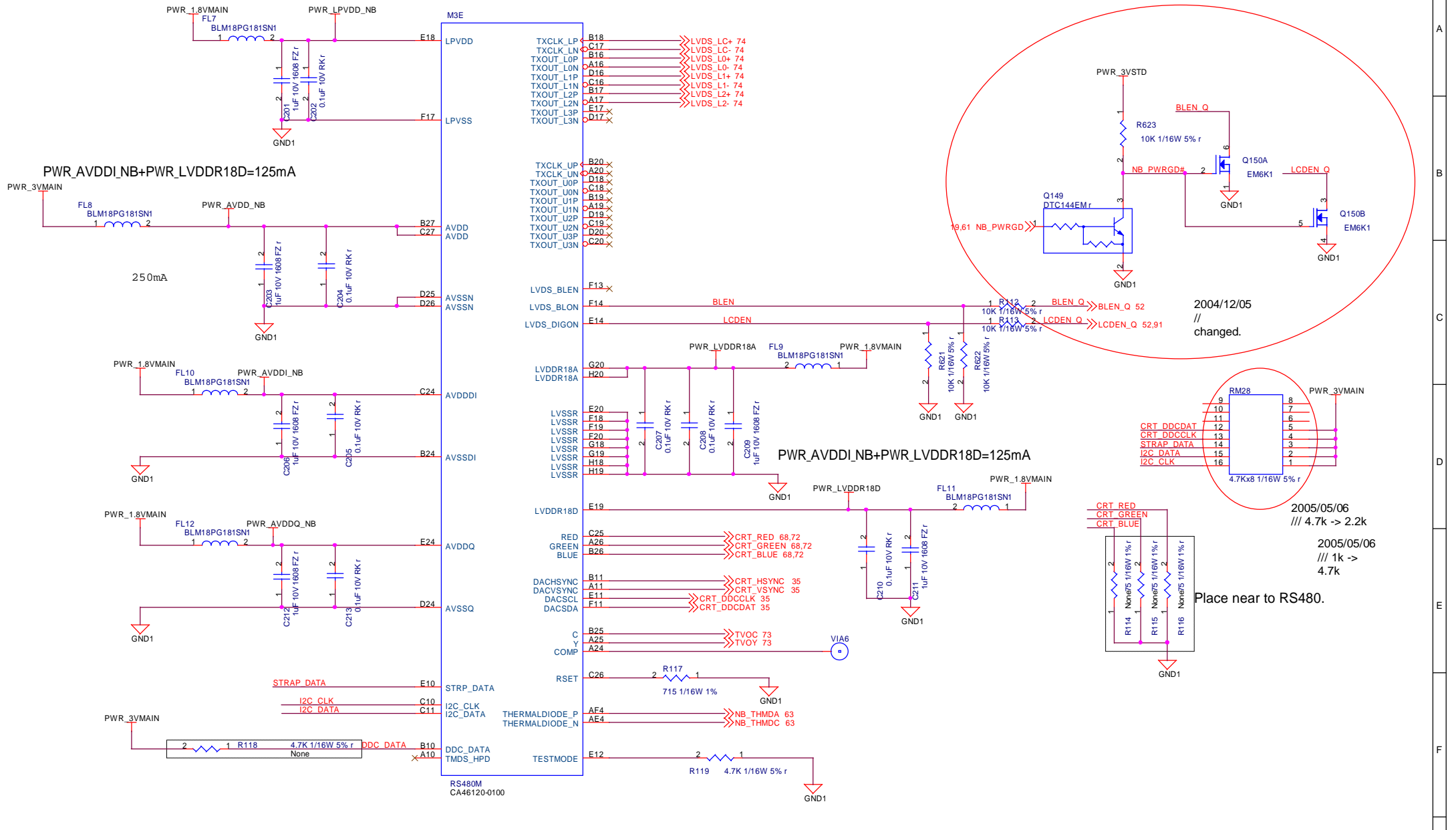
							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHA	Check					20 / 99
							FUJITSU LTD.	



CAL_NB_PCIE, CAL_NB_PCIEISET, TXISET_NB_PCIE, ISET_NB_PCIE
 は0.254mm以上の幅で記録し、
 他の信号から0.254mm以上ギャップを保つこと。
 R129, R1130, R1131, R1132
 は、M1004から12.7mm以内に配置すること

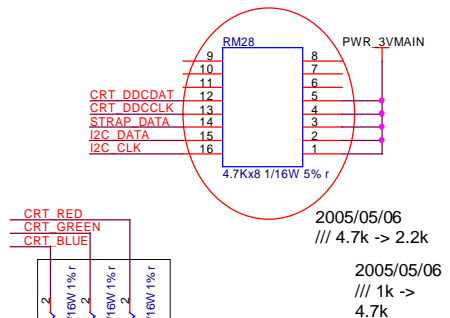
Place above 2 capacitors near to the connector. (Not RS480 side.)

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check					FUJITSU LTD.
							21 / 99	



以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
 LPVSS(F17pin)
 LVSSR(E20,F18,F19,F20,G18,G19,H18,H19pin)
 AVSSN(D25,D26pin)
 AVSSDI(B24pin)
 AVSSQ(D24pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
 C1251 : LPVDD(E18pin)とLPVSS(F17pin)の間
 C1256,C1257 : LVDDR18A(G20,H20pin)とLVSSR(E20,F18,F19,F20,G18,G19,H18,H19pin)の間
 C1253 : AVDD(B27,C27pin)とAVSSN(D25,D26pin)の間
 C1254 : AVDDI(C24pin)とAVSSDI(B24pin)の間
 C1262 : AVDDQ(E24pin)とAVSSQ(D24pin)の間



2004/12/05
 //
 changed.

2005/05/06
 /// 4.7k -> 2.2k
 2005/05/06
 /// 1k -> 4.7k

Place near to RS480.

							TITLE	
							VB222AA	
							DRAW.No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHA	Check					FUJITSU LTD.
							22	99

1.2V

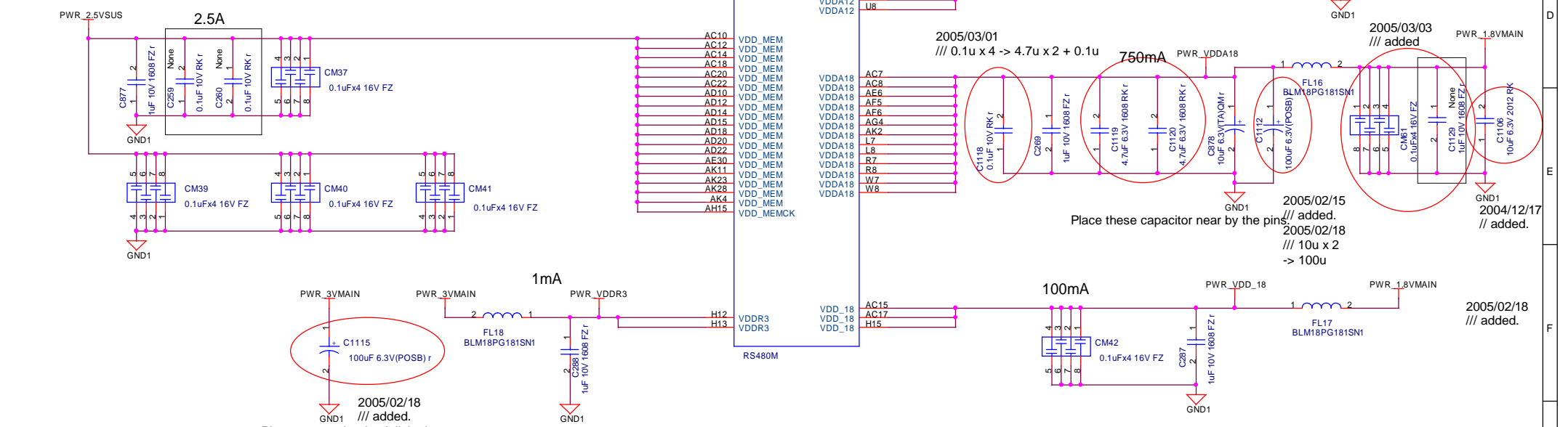
PWR_1.2VMAIN

5.0A

M3F

2005/03/03 FUJITSU CONFIDENTIAL Nile 003/09/03
/// added
Place these capacitor near by the pins.
/// added
/// added

RS480MへのPWR_2.5VSUS_EVAは、Side Port Memoryが無い場合でも必要



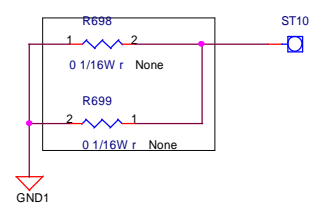
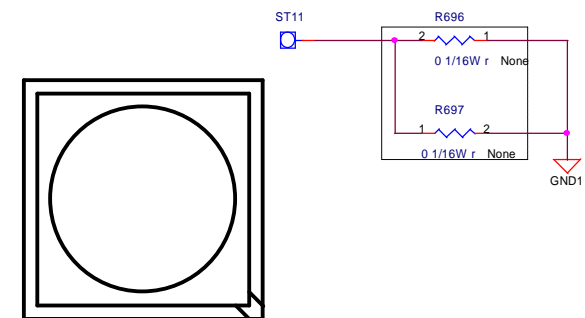
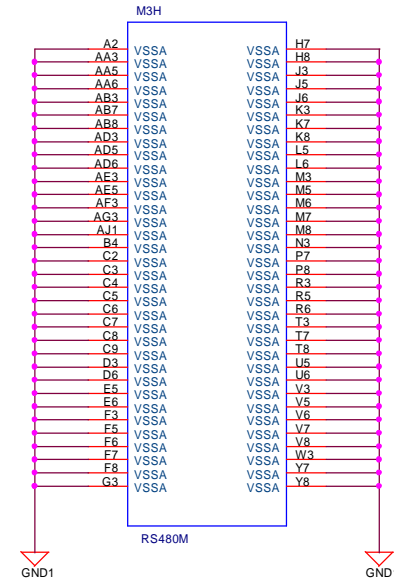
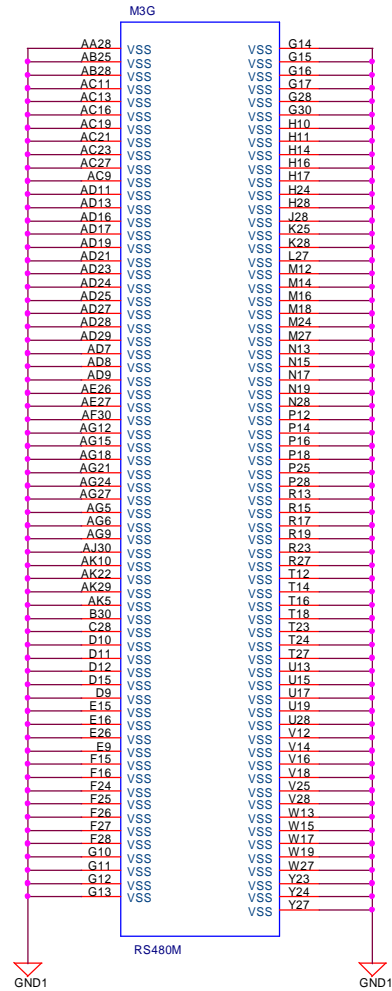
2005/02/18 /// added.
Place near to the the A-link pins.
(AF2, AG2, AC4, AD4, AG1, AH1, AC5, AC6.)

2005/02/15 /// added.
2005/02/18 /// added.
10u x 2 -> 100u

2005/02/18 /// added.



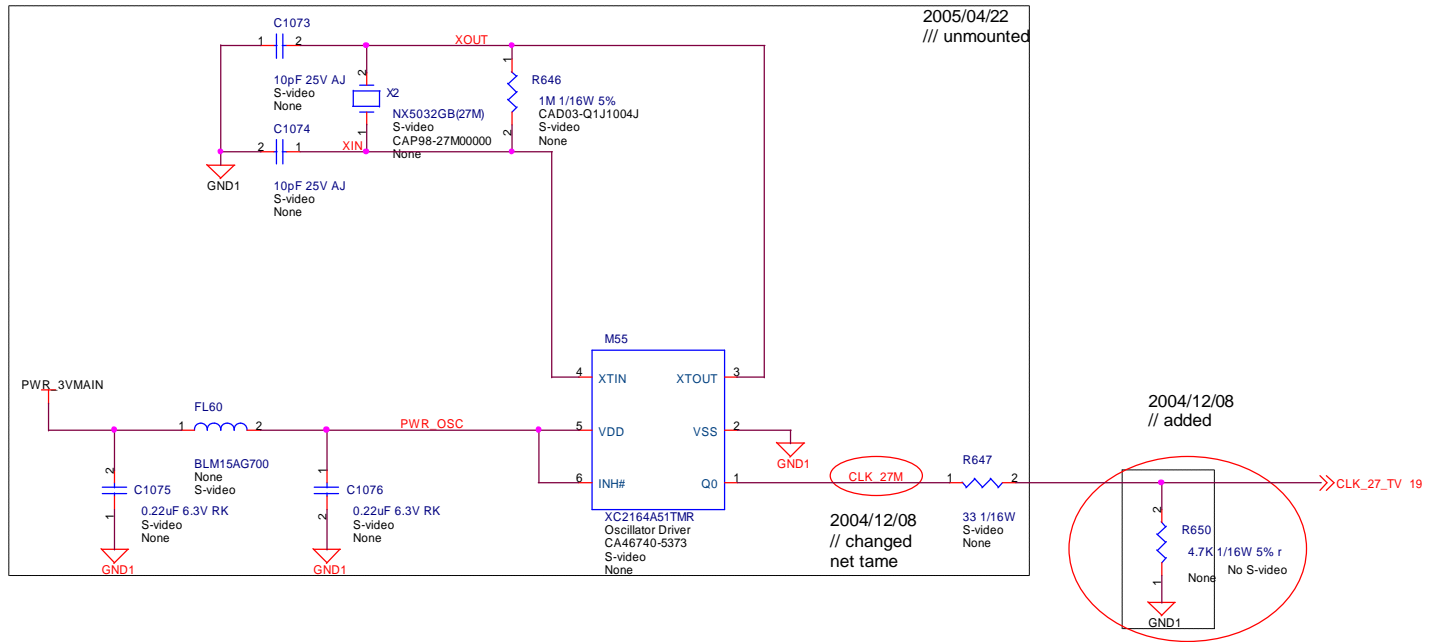
								TITLE VB222AA	
								DRAW. No. C1CP231360-X3	
								CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	/ /	KOSHA	Check	Appr.				23 / 99	
								FUJITSU LTD.	



							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	/ /	KOSHA	Check	Appr.			24 / 99	
							FUJITSU LTD.	

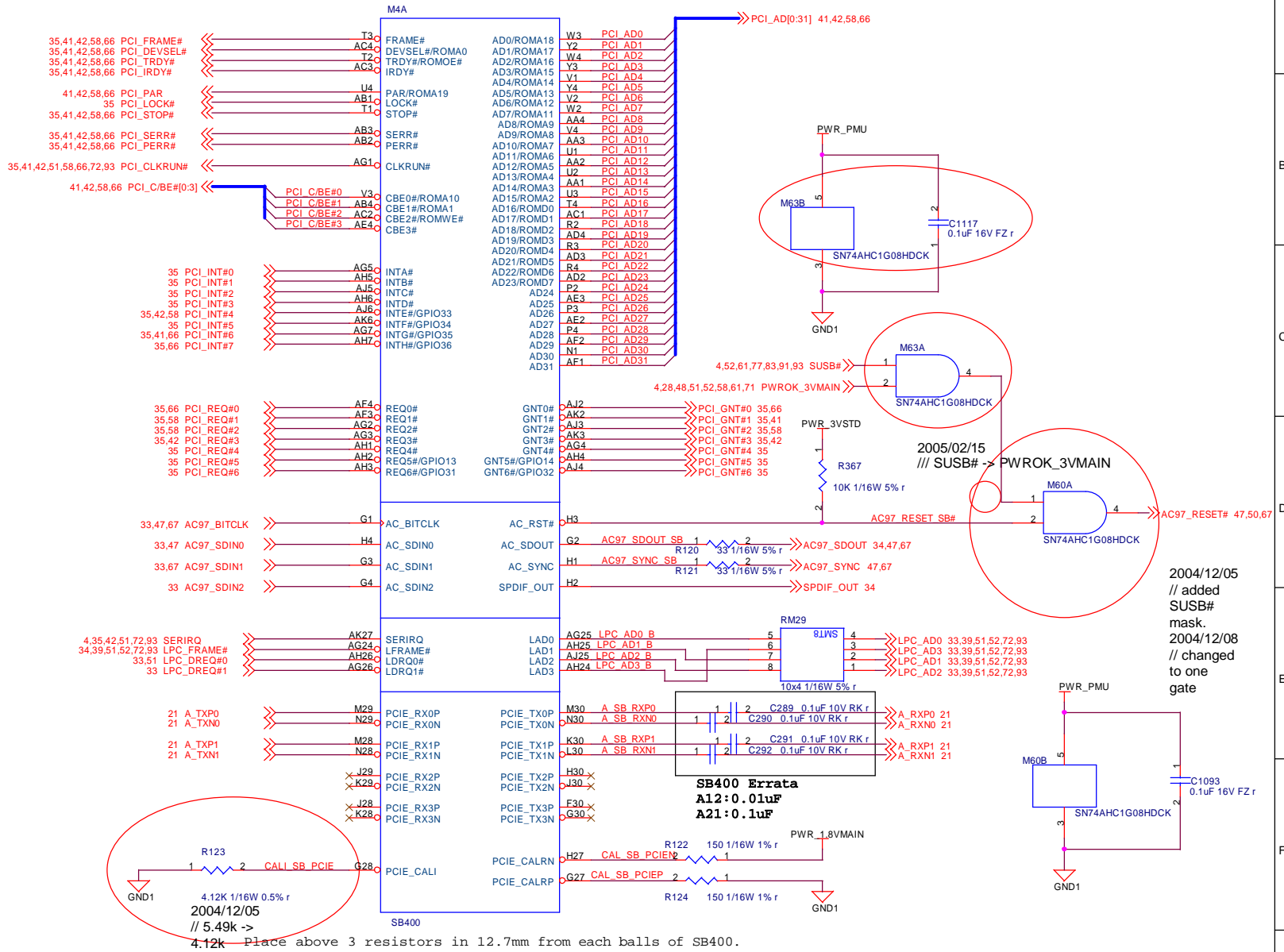
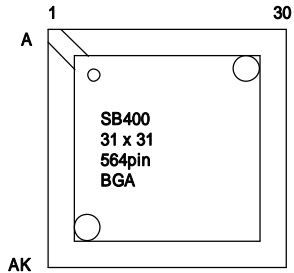
2004/12/02
 // This page was added.

S-video
 Place near to RS480



TV Clock

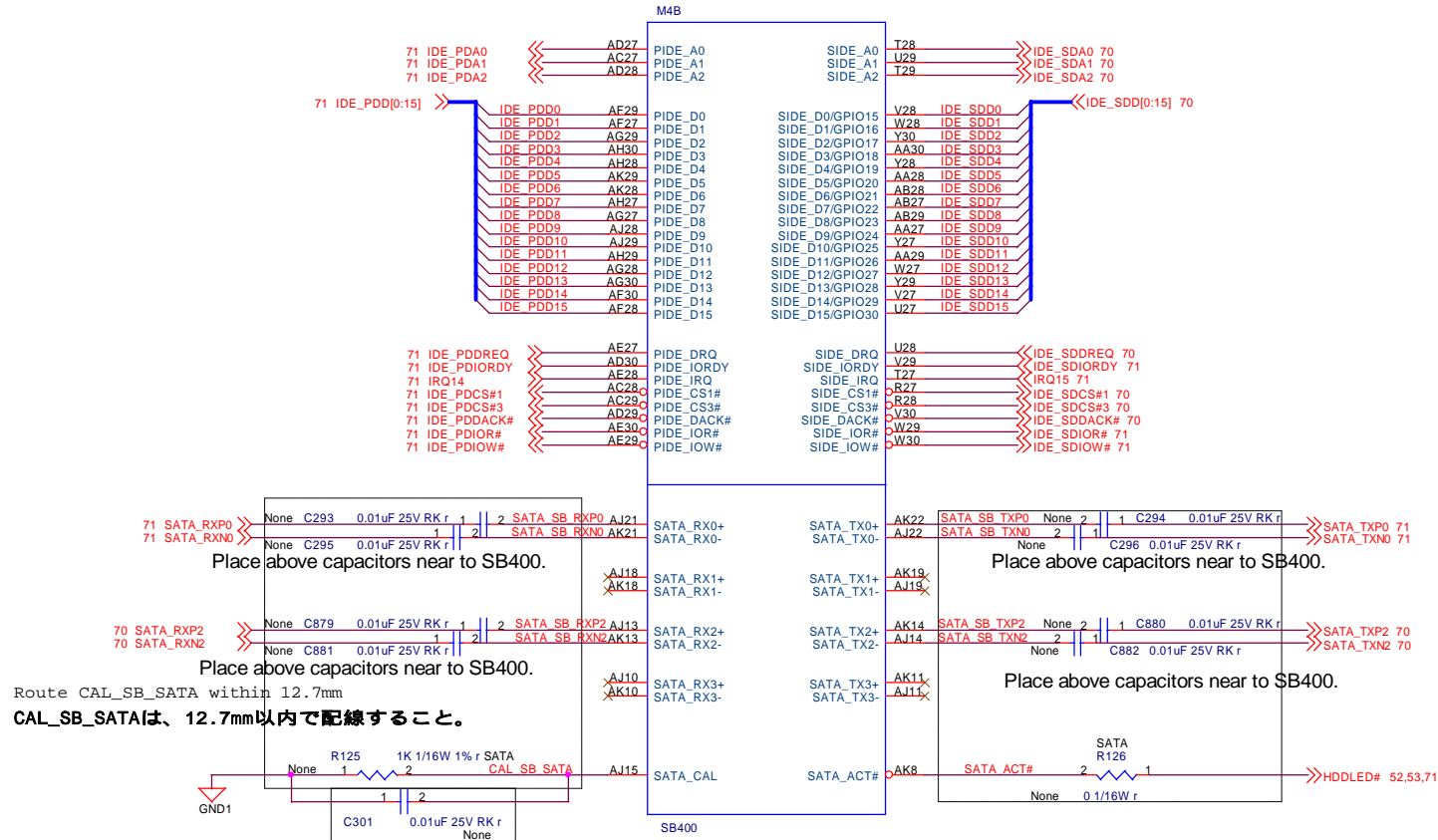
							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check				Appr.	
							FUJITSU LTD.	
							Sheet	
							25 / 99	



Fujitsu
Proprietary &
Confidential

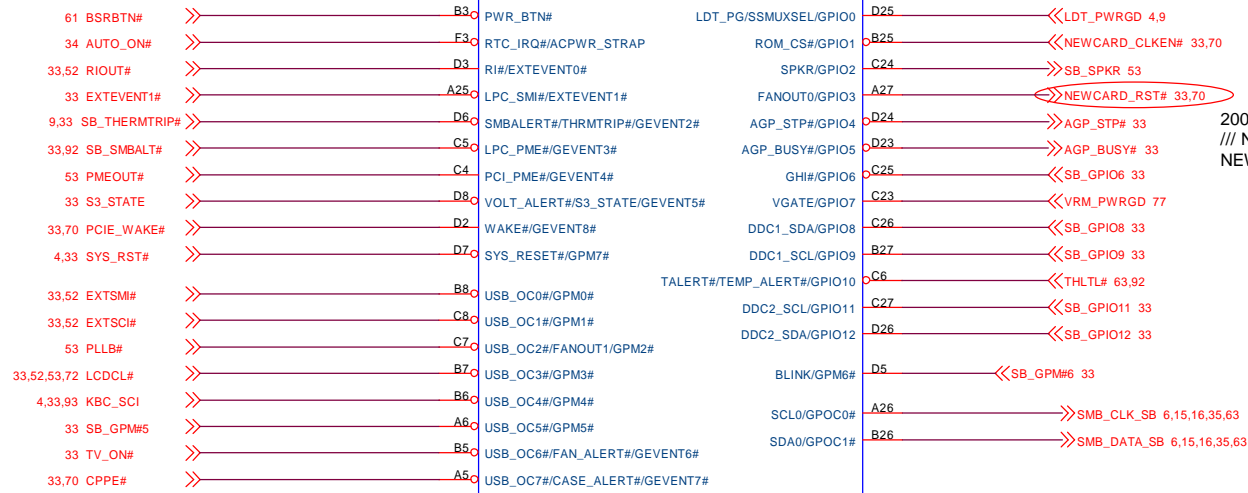
Place R169 no less than 12.7mm from G28pin
 Place R168 no less than 12.7mm from H27pin
 Place R170 no less than 12.7mm from G27pin
R169 is G28pin 12.7mm以内に配置する
R168 is H27pin 12.7mm以内に配置する
R170 is G27pin 12.7mm以内に配置する

TITLE										VB222AA	
DRAW.No.										C1CP231360-X3	
CAST											
Rev.	Date	Design	Check	Appr.	Description					Sheet	
Design	/ /	KOSHA	Check							FUJITSU LTD.	
										26 / 99	

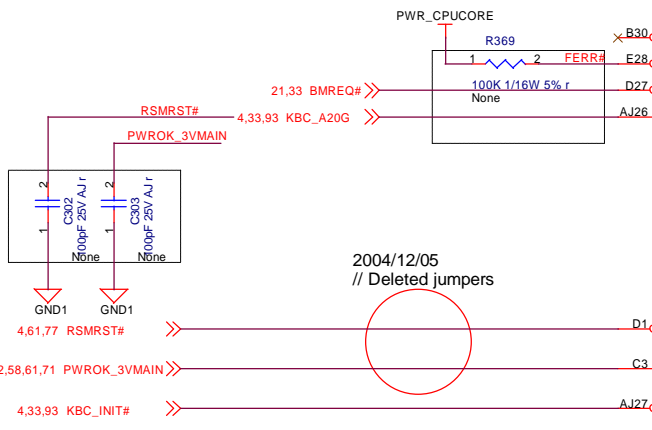
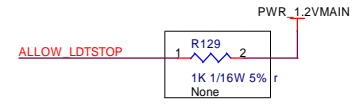


							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check		Appr.			
							FUJITSU LTD.	
							Sheet	
							27 / 99	

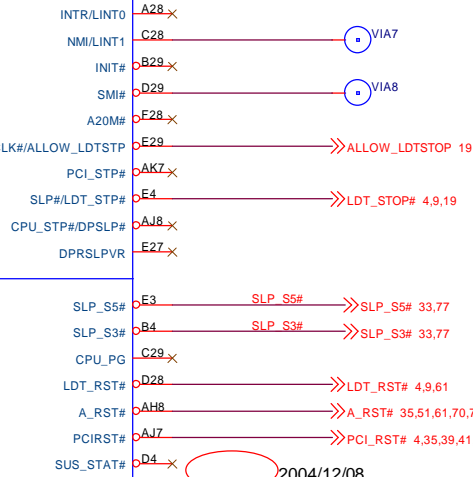
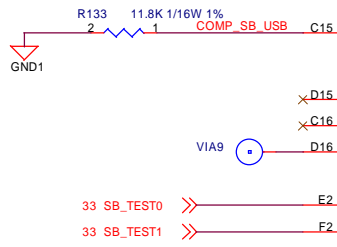
...is signal will output high in s3 state, output low in other states.



2005/02/13
/// NCPOW_RST# ->
NEWCARDRST#



COMP_SB_USBは、12.7mm以内で配線すること。



2004/12/08
// deleted

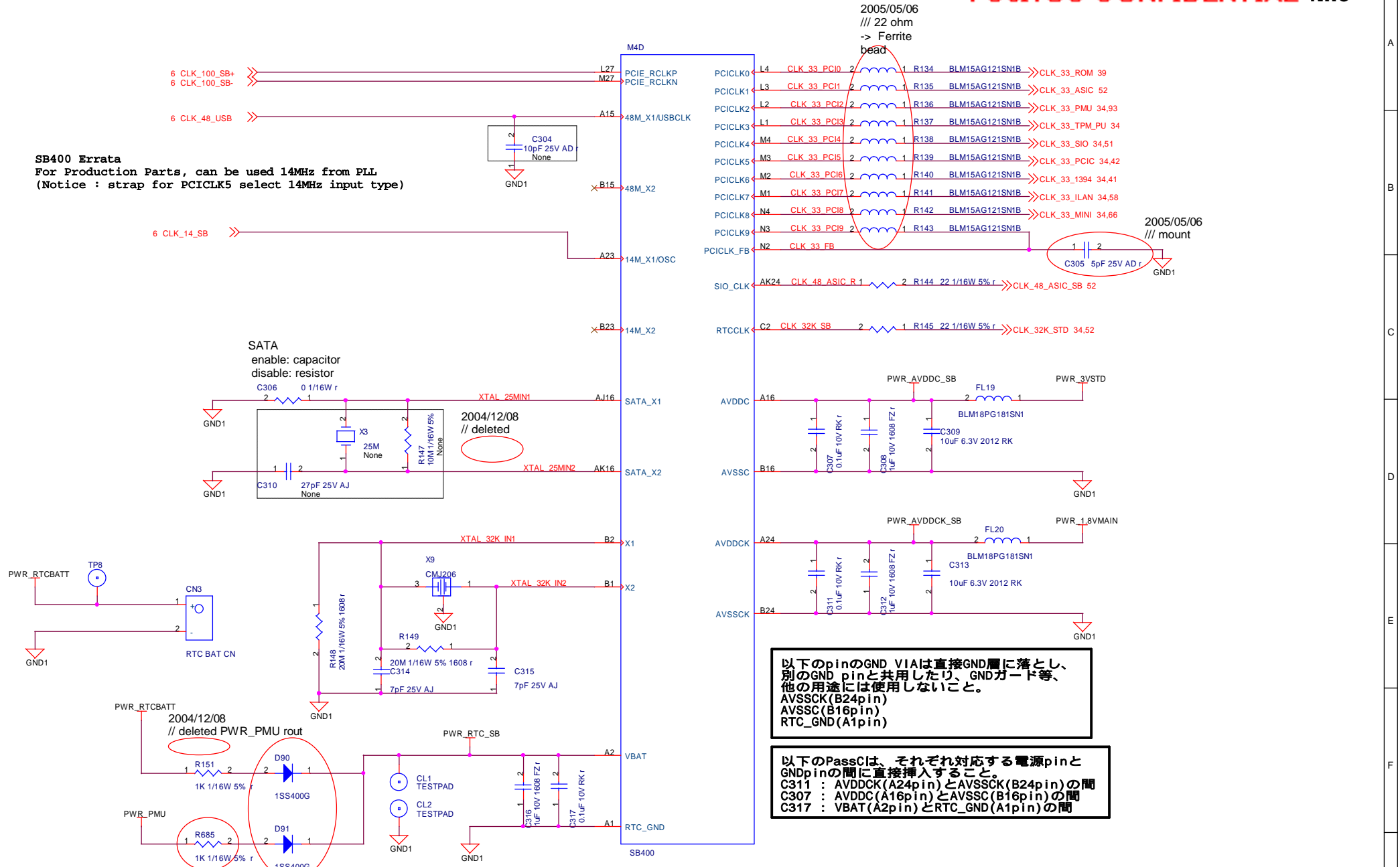
2004/12/08
// populated in PCI
pulldown page

SB400

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
							Sheet	
							28 / 99	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	
	/ /							

2005/05/06
 /// 22 ohm
 -> Ferrite
 bead

SB400 Errata
 For Production Parts, can be used 14MHz from PLL
 (Notice : strap for PCICLK5 select 14MHz input type)

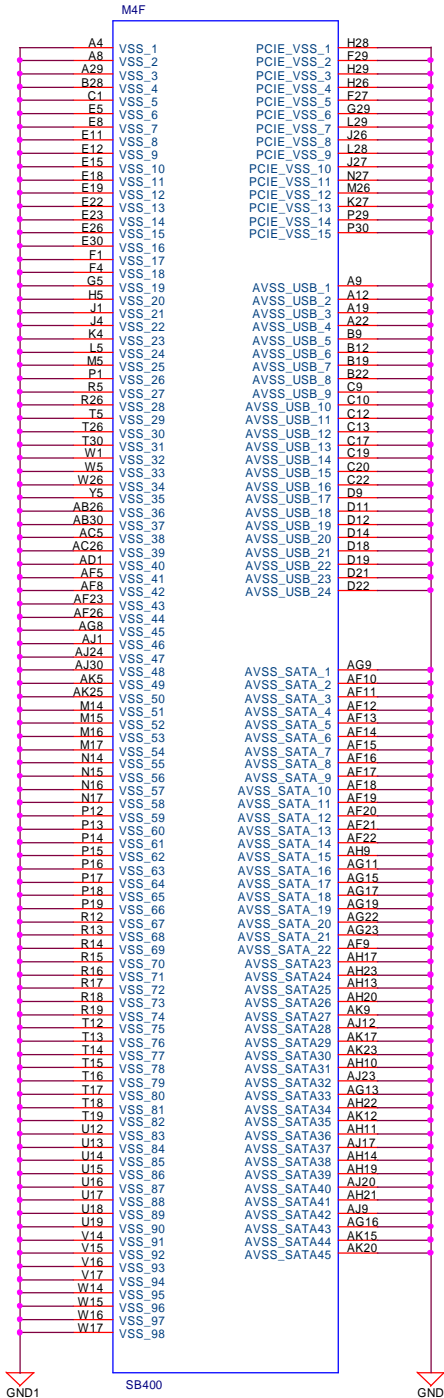


2005/05/06
 /// mount

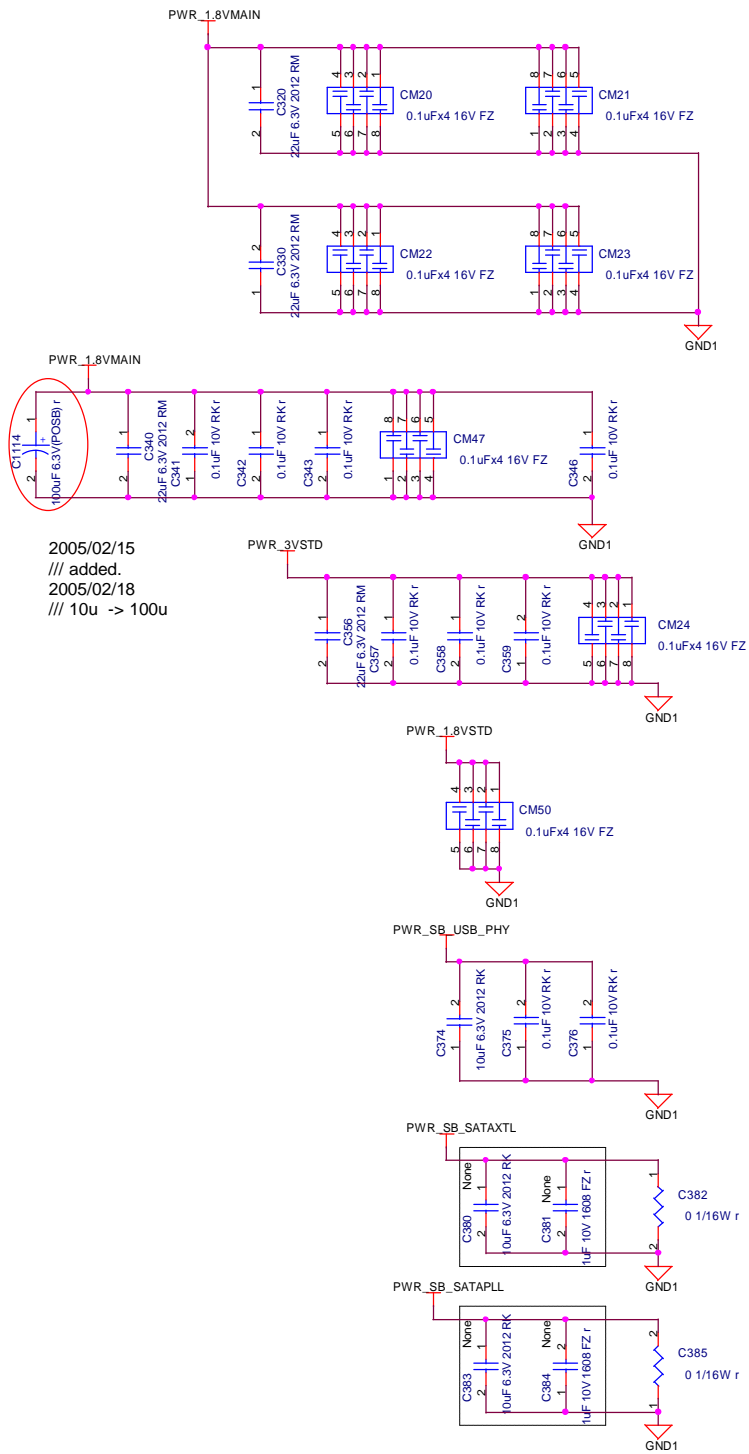
以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
 AVSSCK(B24pin)
 AVSSC(B16pin)
 RTC_GND(A1pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
 C311 : AVDDCK(A24pin)とAVSSCK(B24pin)の間
 C307 : AVDDC(A16pin)とAVSSC(B16pin)の間
 C317 : VBAT(A2pin)とRTC_GND(A1pin)の間

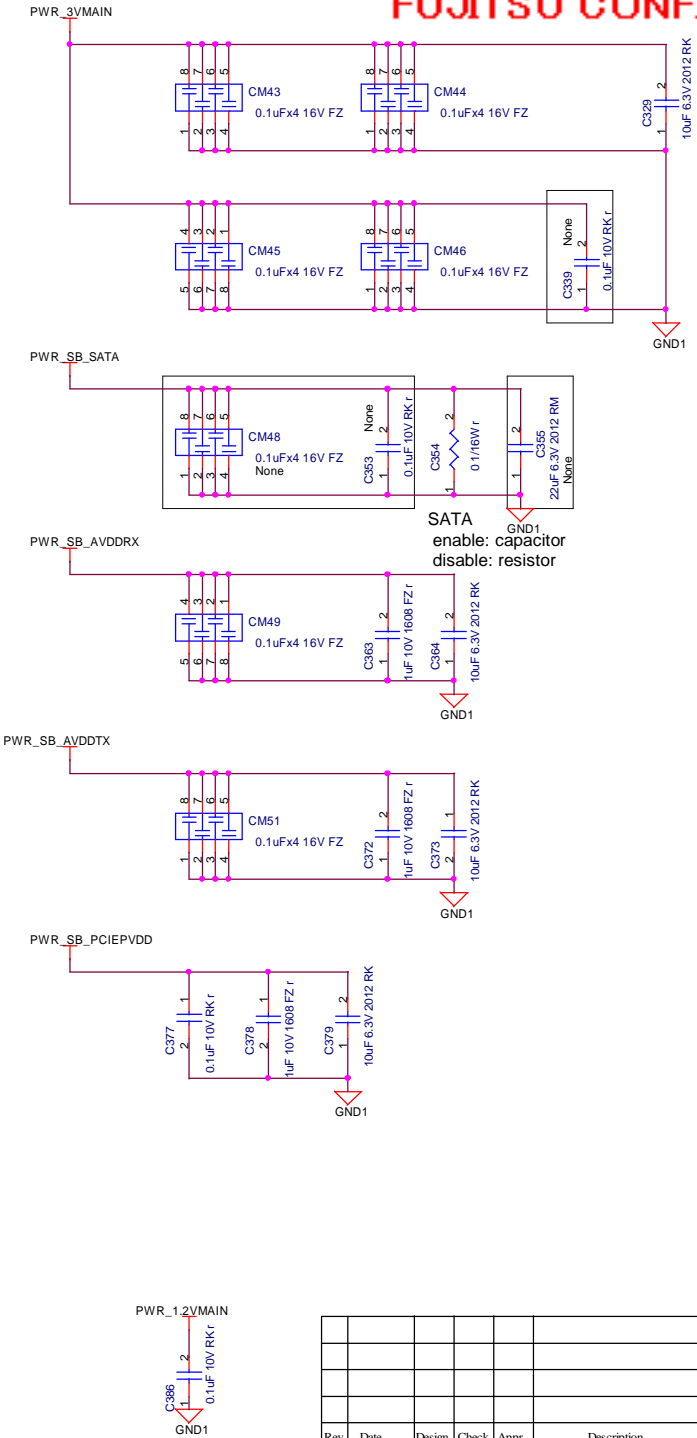
							TITLE	
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							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check					
							FUJITSU LTD.	
							Sheet	
							29 / 99	



							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check					
							FUJITSU LTD.	
							Sheet	
							31 / 99	

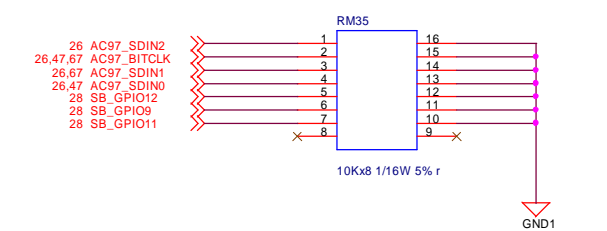
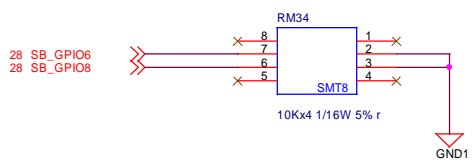
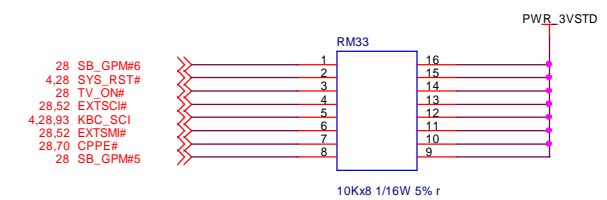
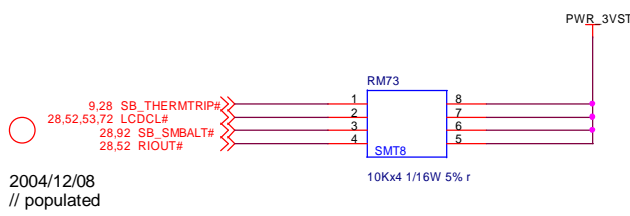
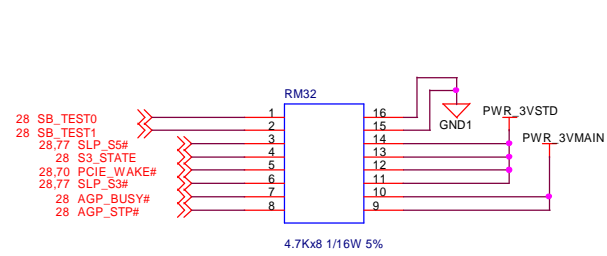
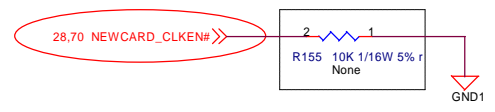
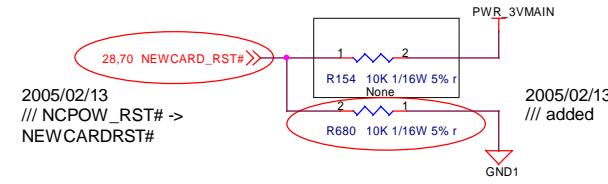
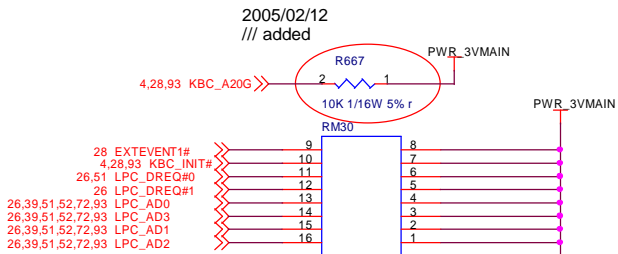


2005/02/15
 /// added.
 2005/02/18
 /// 10u -> 100u

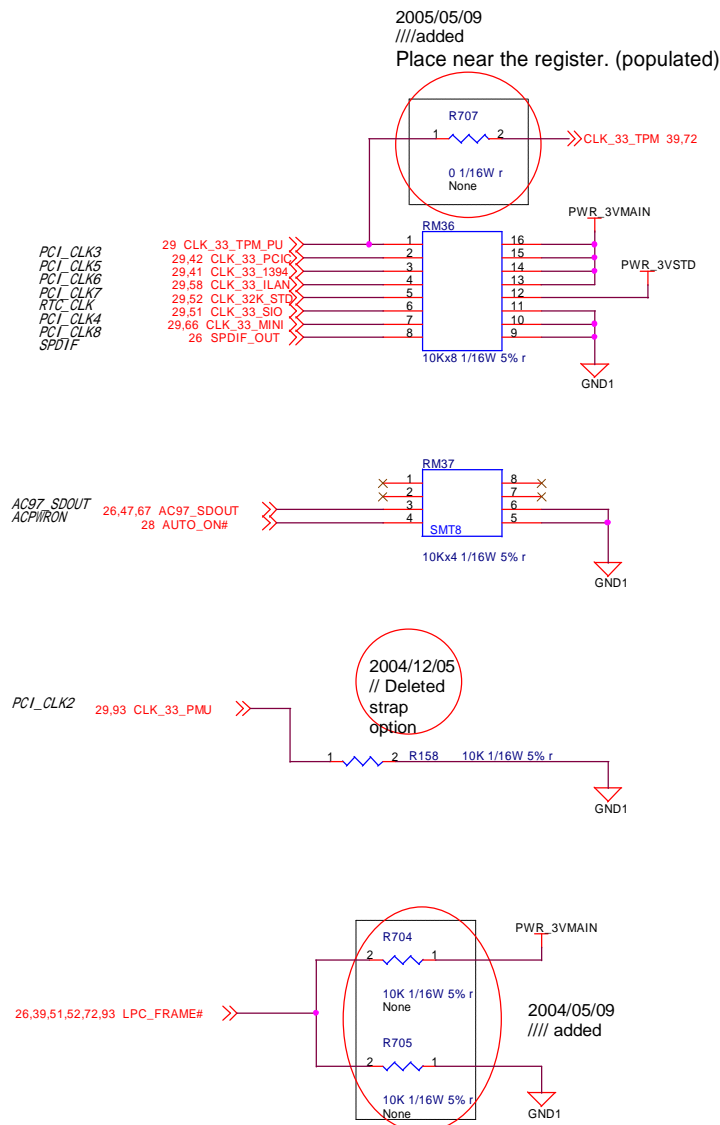


SATA
 enable: capacitor
 disable: resistor

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.			32 / 99
							FUJITSU LTD.	



							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check		Appr.			
FUJITSU LTD.							Sheet	
							33 / 99	



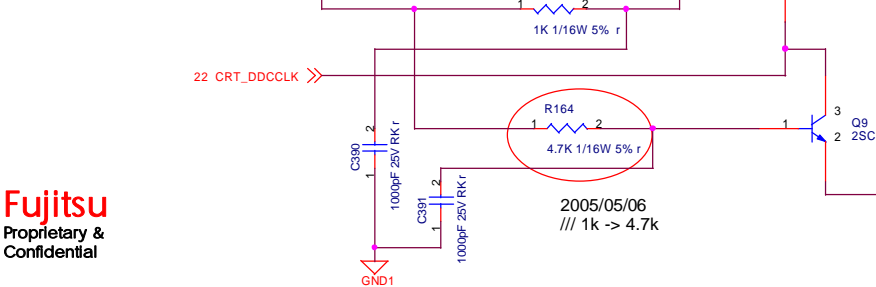
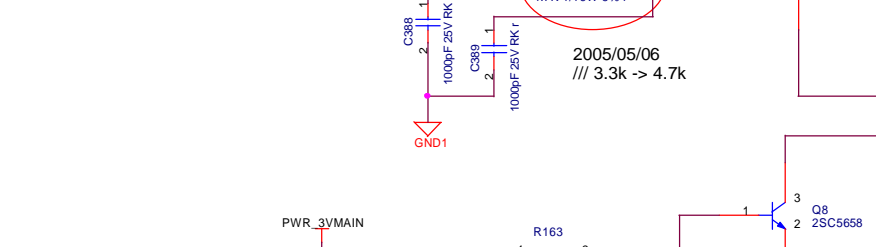
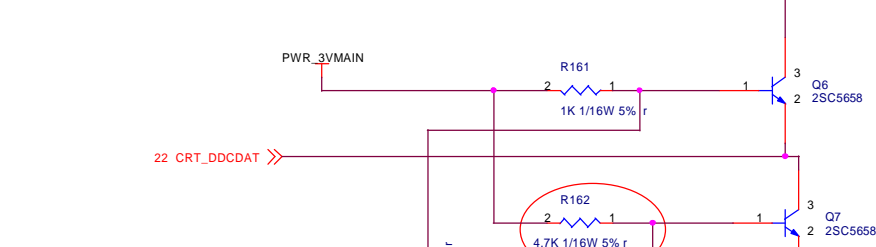
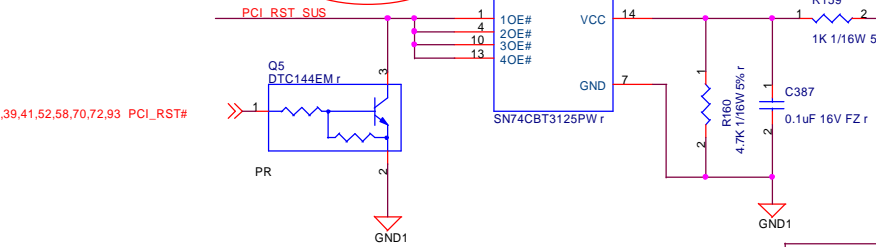
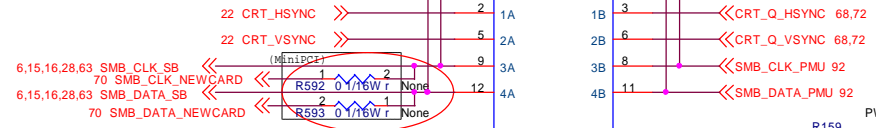
Signal Name (Pin Name)	Description	*0* = Pull-down *1* = Pull-Up
CLK_33_TPM (PCICLK3)	USB PHY Powerdown 0 : Enable 1 : Disable	
CLK_33_SIO (PCICLK4)	Bypass USB PLL 0 : use external 48MHz 1 : use internal USB PLL for 48MHz	
CLK_33_VIEW (PCICLK5)	14MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer	
CLK_33_PCIC (PCICLK6)	Define Type of CPU 0 : Intel Processors 1 : AMD K8 Processors	
ROM Type Select		
CLK_33_ILAN (PCICLK7)	PCICLK7	1 1 0 0
CLK_33_MINI (PCICLK8)	PCICLK8	0 1 0 1
	ROM Type	LPC ROM (256K) BIOS ROM (X-bus) FWH LPC ROM (512K/1M)
SPDIF_OUT (SPDIF)	Select Speed for Super I/O. 0 : SIO Speed is 48MHz 1 : SIO Speed is 24MHz	
CLK_32K_STD (RTC_CLK)	RTC Select 0 : External RTC 1 : Internal RTC	
AC97_SDOUT (AC97SDOUT)	Enable/Disable additional straps for Debugging. 0 : Use Hardcoded defaults for Debug straps 1 : Enable additional Debug Strap	
AUTO_ON# (ACPWON)	Active Manual Power On. 0 : Automatic Power On 1 : Manual Power On	
CLK_33_PMU (PCICLK2)	48MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer	

Pin Name	Description
PCI_AD23	Reserved
PCI_AD24	Bif_core strap from I2ROM enable 0 : Use default Value 1 : getting the value from I2C EPROM
PCI_AD25	Bypass IDE Clock 0 : Use Internal IDE CLK 1 : Bypass Internal IDE CLK
PCI_AD26	Bypass ACPI BCLK 0 : Use internal ACPI_BCLK 1 : Bypass ACPI_BCLK
PCI_AD27	Bypass PCI PLL 0 : Use internal IDE PLL. Generated PCI CLK 1 : Bypass internal PCI PLL
PCI_AD29	PLL VCO control bits
PCI_AD31	PLL Charge Pump control Bit
IDE_PDDACK# (PIDE_DACK#)	Generate Short Reset 0 : Use Long Reset (Default) 1 : Use Short Reset

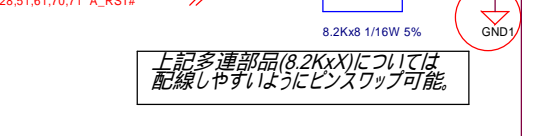
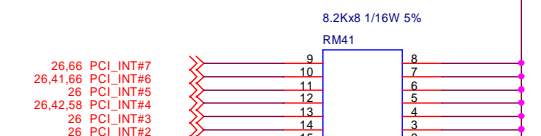
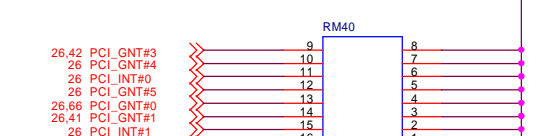
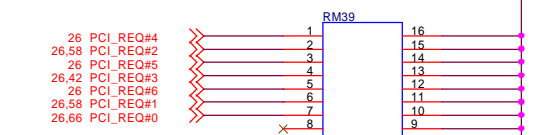
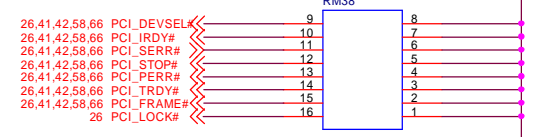
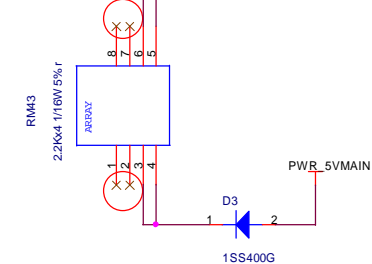
						TITLE VB222AA	
						DRAW. No. C1CP231360-X3	
						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	//	KOSHA	Check			Appr.	
						FUJITSU LTD.	
						Sheet 34 / 99	

2005/02/13

/// PWR_PMU pull up -> PWR_3VMAIN pull up



2005/03/03
/// deleted



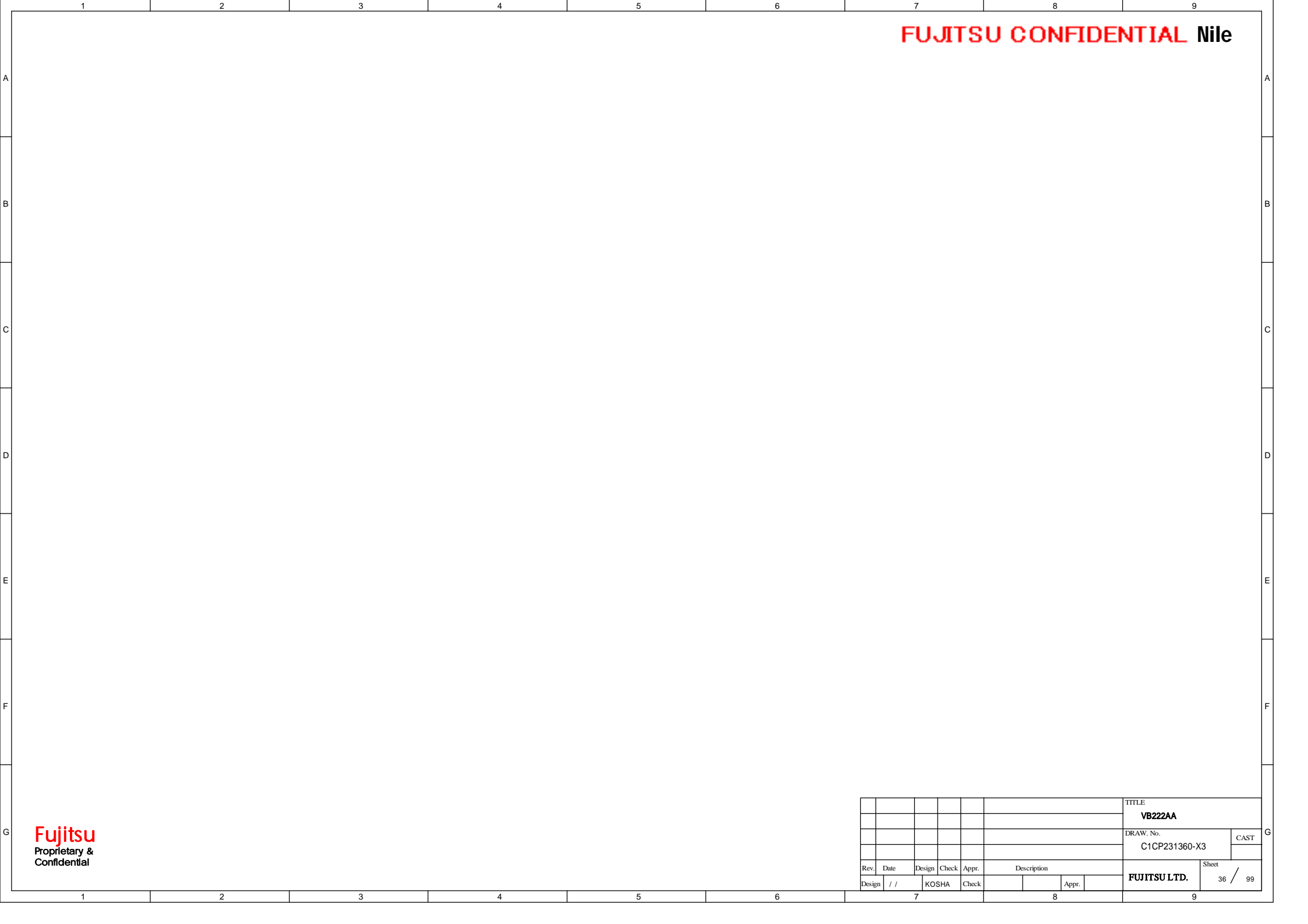
上記多連部品(8.2KxX)については配線しやすいようにピンスワップ可能。

2005/02/13
/// pullup -> pulldown

Pullup for
AGP,PCI,LPC

							TITLE VB222AA	
							DRAW. No. C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHA	Check		Appr.		FUJITSU LTD.	35 / 99

										TITLE	
										VB222AA	
										DRAW. No.	
										C1CP231360-X3	
										CAST	
Rev.	Date	Design	Check	Appr.	Description						
Design	//		KOSHA	Check				Appr.			
										FUJITSU LTD.	
										Sheet	
										36 / 99	

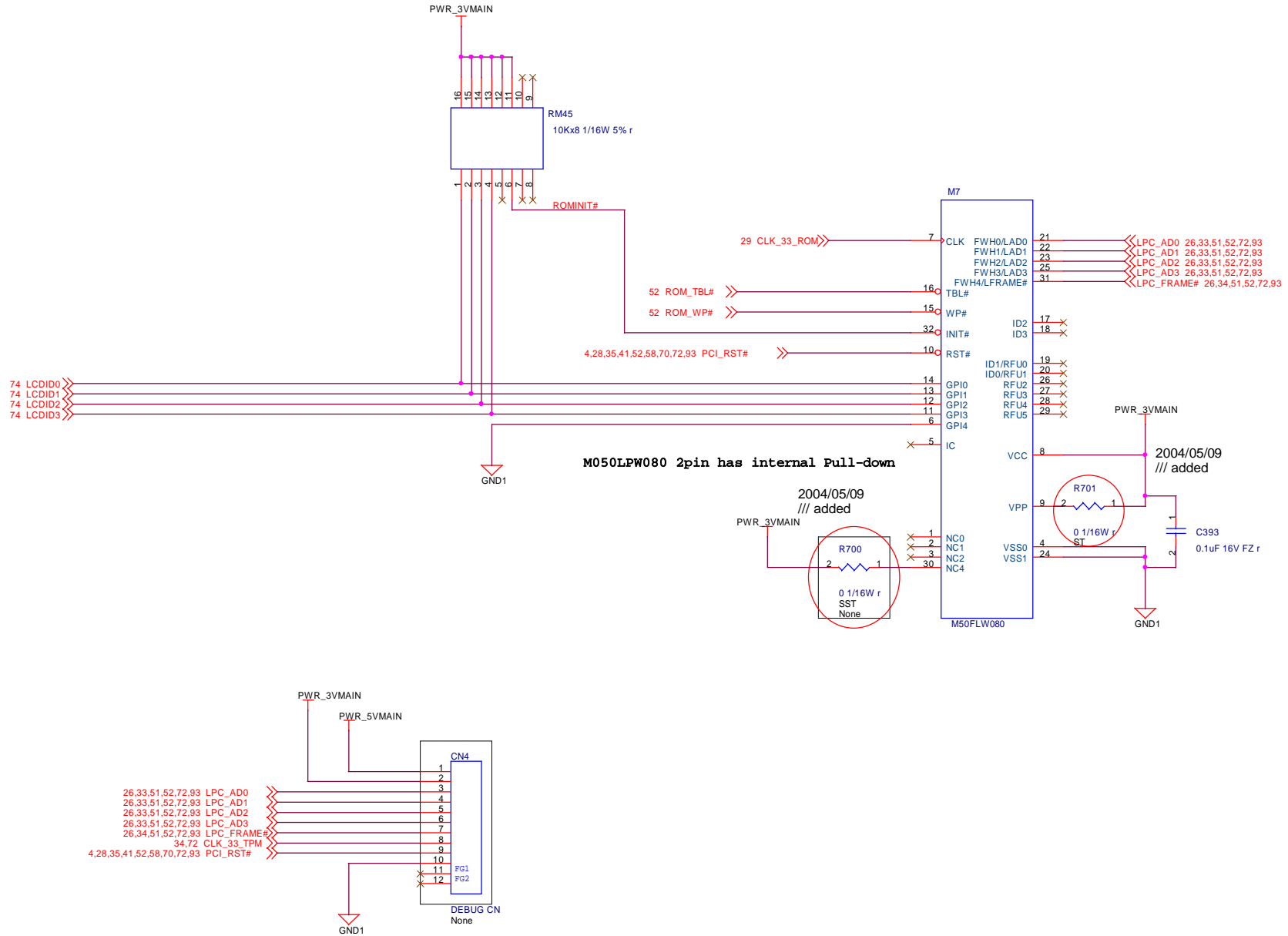


RESERVED

						TITLE		VB222AA	
						DRAW. No.		C1CP231360-X3	
								CAST	
Rev.	Date	Design	Check	Appr.	Description				
Design	//	KOSHA	Check				Appr.	FUJITSU LTD.	
								Sheet	
								37 / 99	

Reserve

					TITLE		VB222AA	
					DRAW. No.		C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check			Appr.	FUJITSU LTD.	
							Sheet	38 / 99



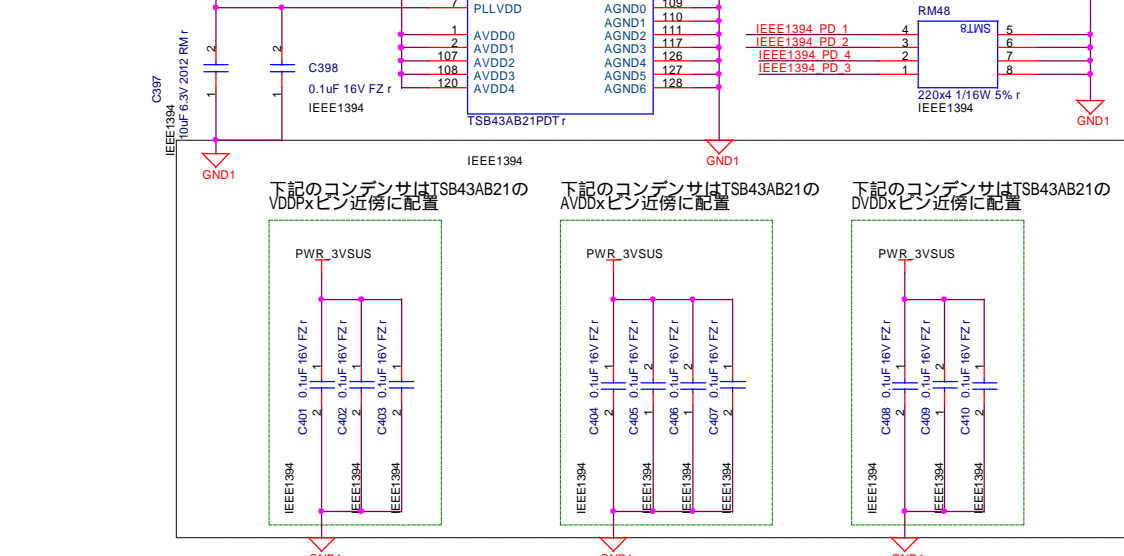
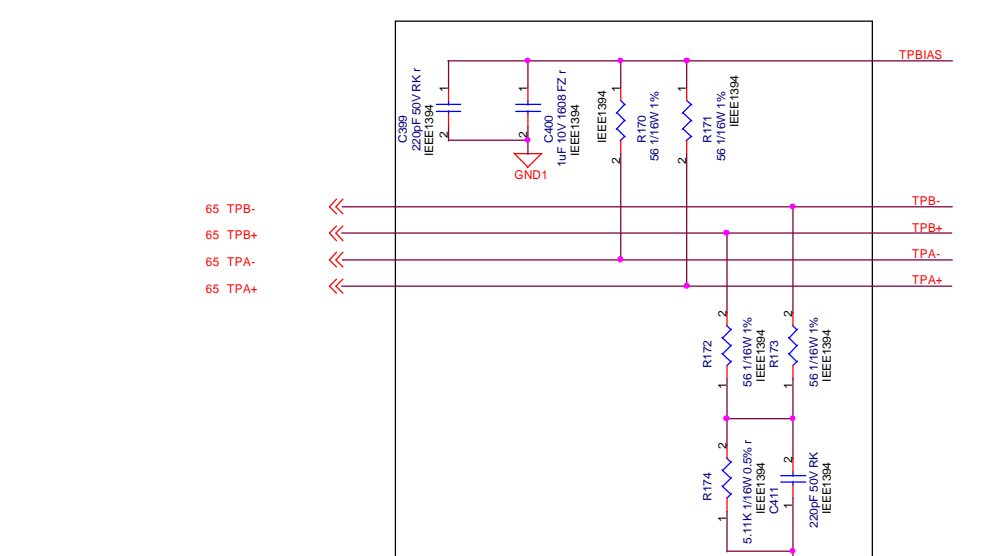
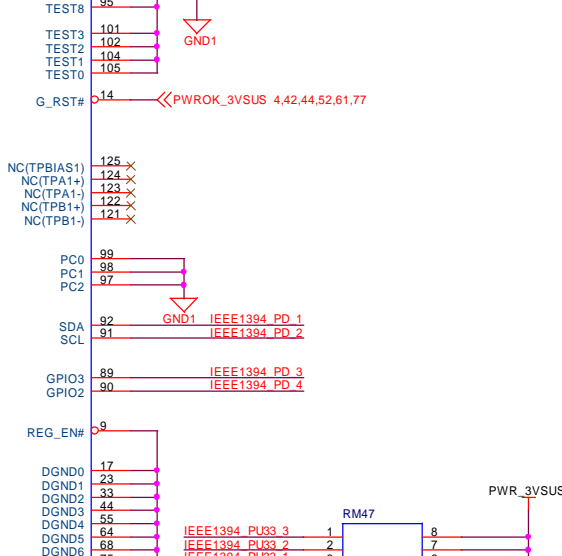
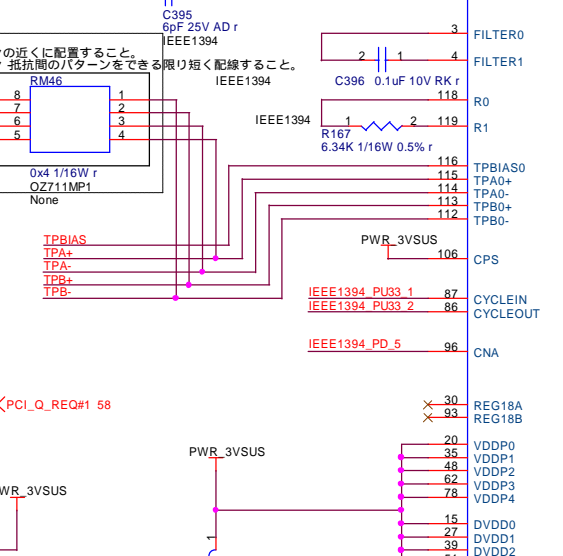
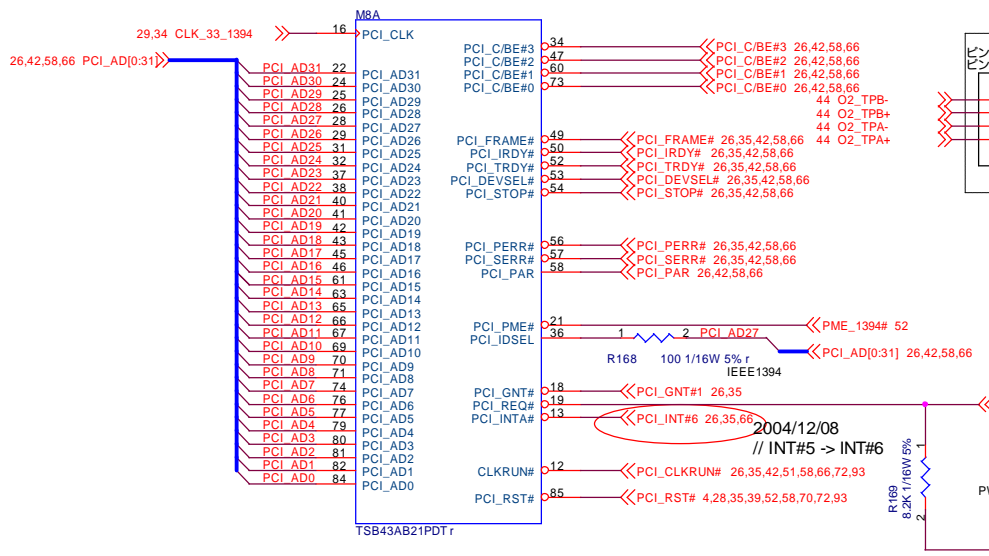
LPC ROM

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check		Appr.			
FUJITSU LTD.							Sheet	
							39 / 99	

VID4	VID3	VID2	VID1	VID0	LPM Voltage
0	0	0	0	0	1.450V
0	0	0	0	1	1.425V
0	0	0	1	0	1.400V
0	0	0	1	1	1.375V
0	0	1	0	0	1.350V
0	0	1	0	1	1.325V
0	0	1	1	0	1.300V
0	0	1	1	1	1.275V
0	1	0	0	0	1.250V
0	1	0	0	1	1.225V
0	1	0	1	0	1.200V
0	1	0	1	1	1.175V
0	1	1	0	0	1.150V
0	1	1	0	1	1.125V
0	1	1	1	0	1.100V
0	1	1	1	1	1.075V
1	0	0	0	0	1.050V
1	0	0	0	1	1.025V
1	0	0	1	0	1.000V
1	0	0	1	1	0.975V
1	0	1	0	0	0.950V
1	0	1	0	1	0.925V
1	0	1	1	0	0.900V
1	0	1	1	1	0.875V
1	1	0	0	0	0.850V
1	1	0	0	1	0.825V
1	1	0	1	0	0.800V
1	1	0	1	1	0.775V
1	1	1	0	0	0.750V
1	1	1	0	1	0.725V
1	1	1	1	0	0.700V
1	1	1	1	1	OFF

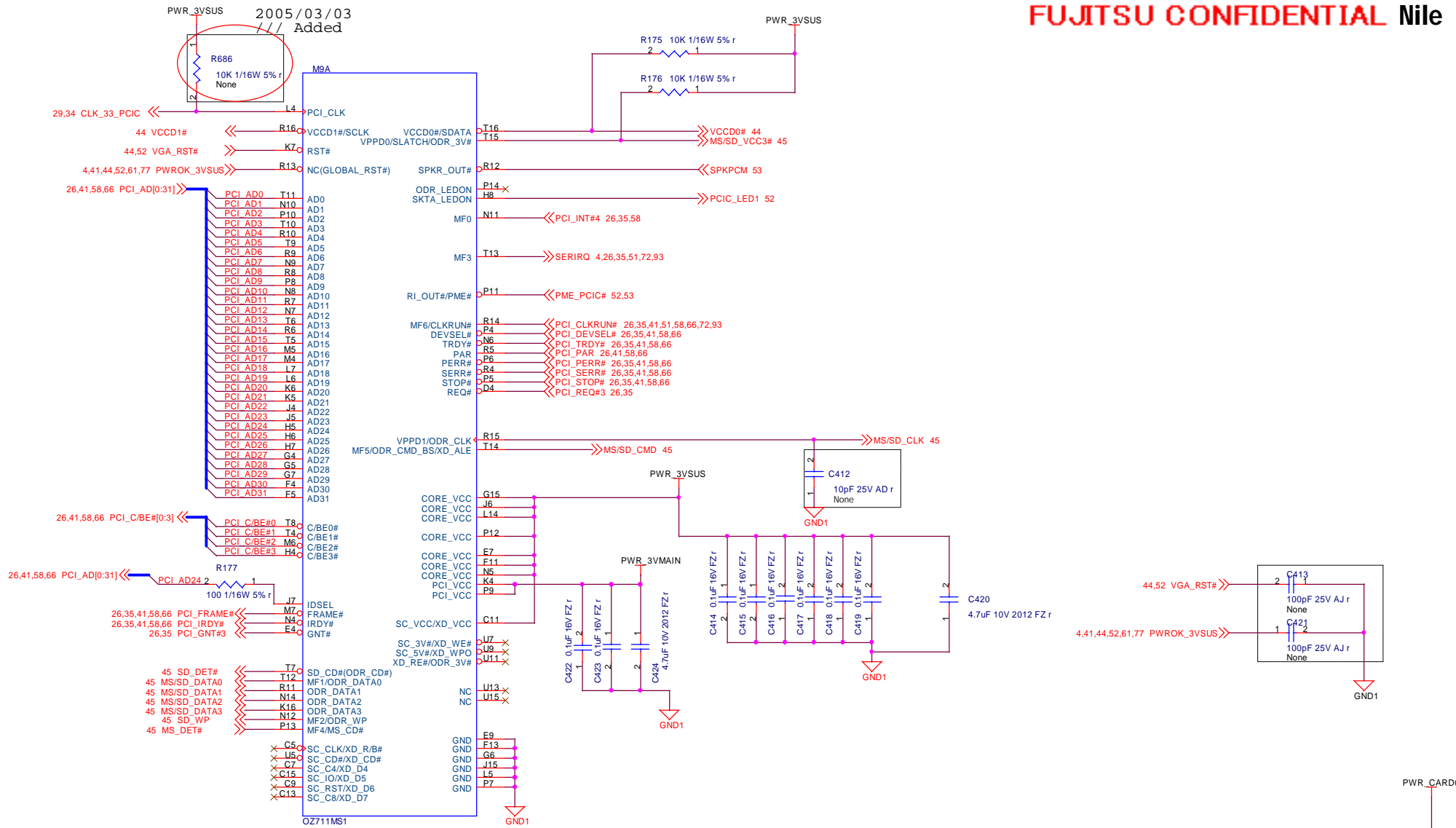
Fujitsu
Proprietary &
Confidential

					TITLE		VB222AA	
					DRAW. No.		C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check			Appr.		
							FUJITSU LTD.	
							Sheet 40 / 99	

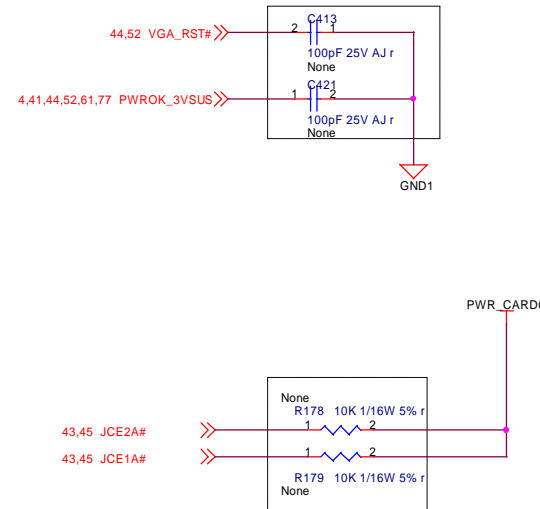


Fujitsu
Proprietary &
Confidential
[Reserve]

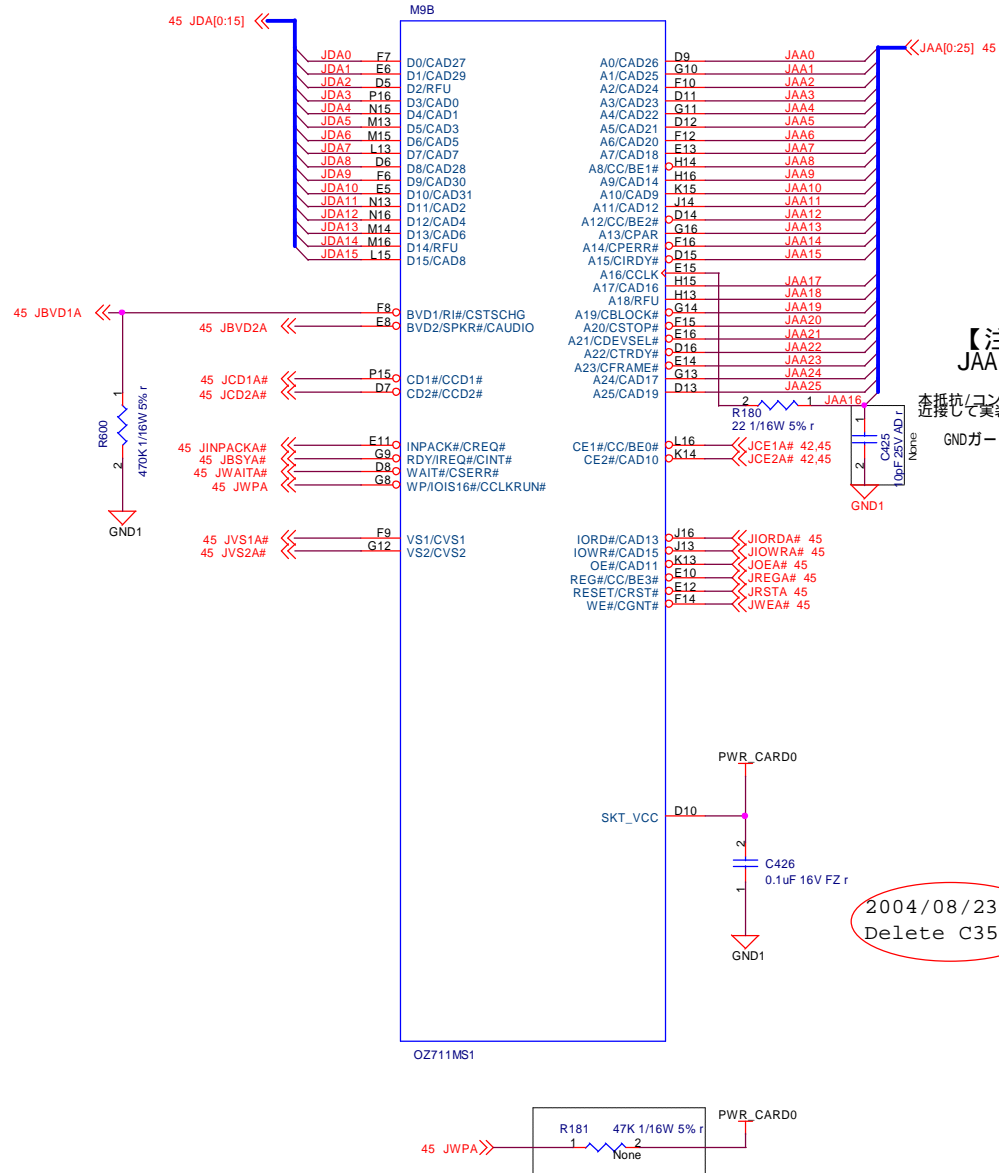
TITLE										VB222AA	
DRAW. No.										C1CP231360-X3	
Rev.										CAST	
Date										Sheet	
Design										FUJITSU LTD.	
Check										41 / 99	
Appr.											
Description											
KOSHA											
Appr.											



M11 A/T/: with SD/MS
 OZ711MC1 (CA)
 C/O: without SD/MS
 PRECID10-1 (CA)

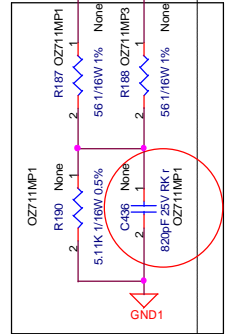
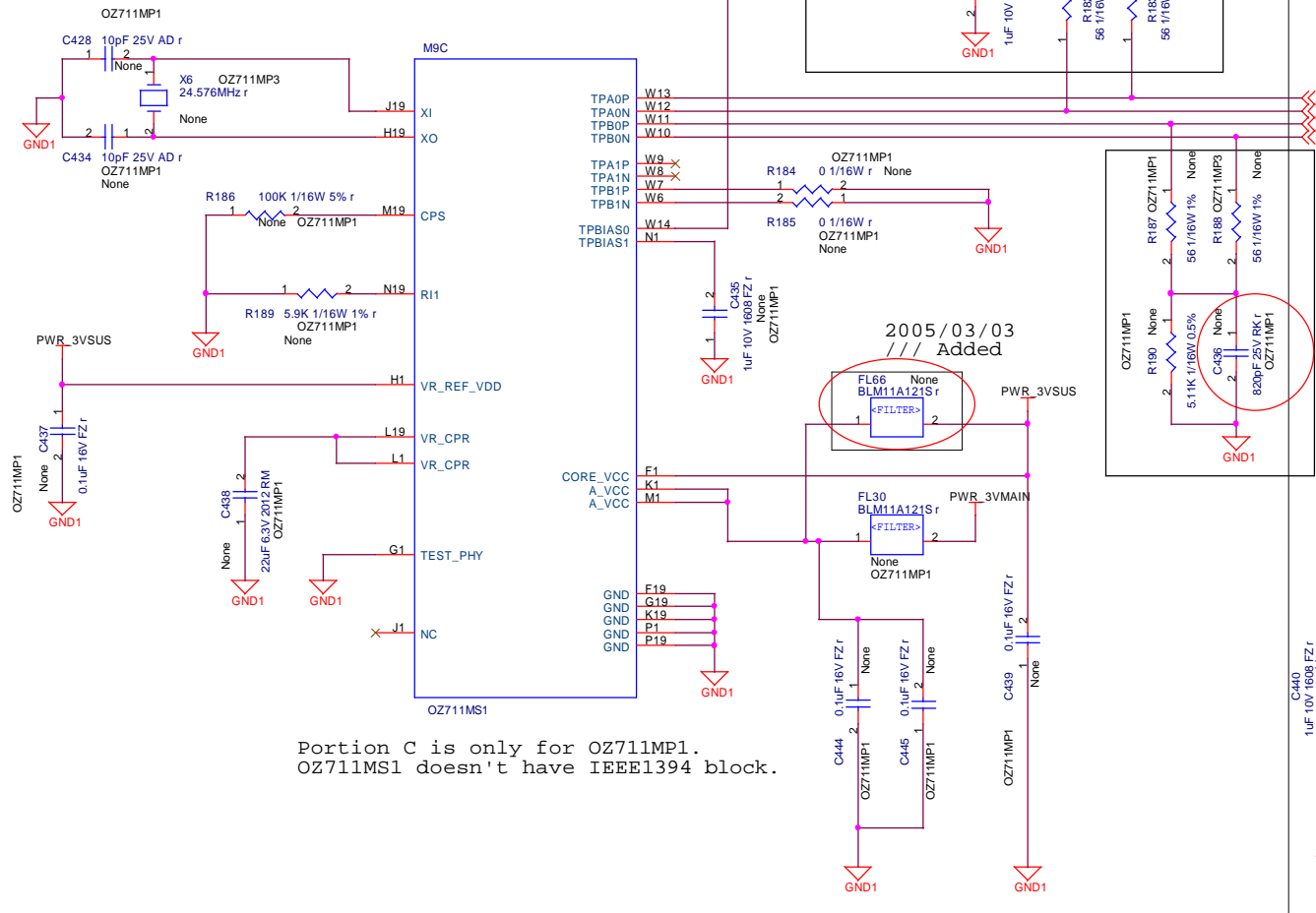
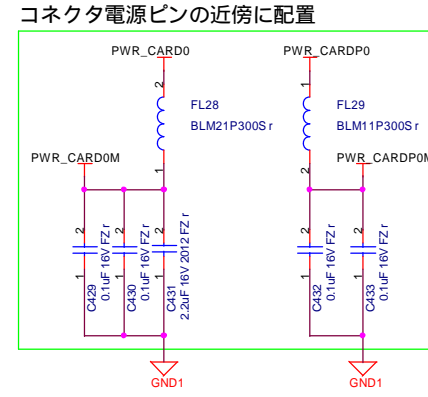
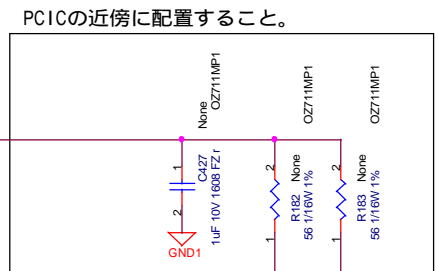


							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHIA	Check					42 / 99
							FUJITSU LTD.	

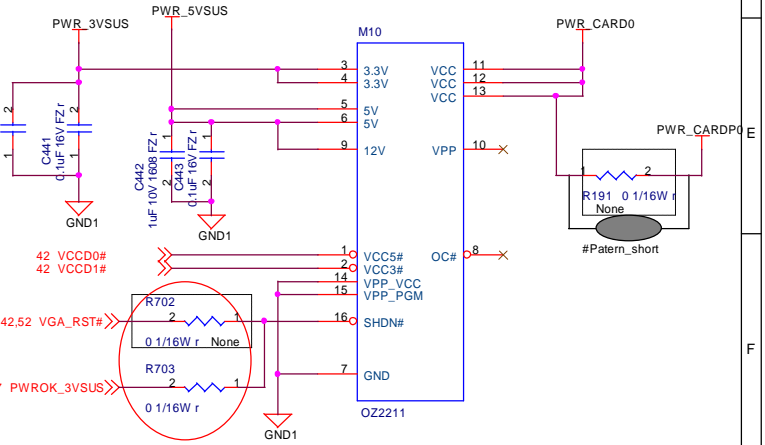


							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check					43 / 99
							FUJITSU LTD.	

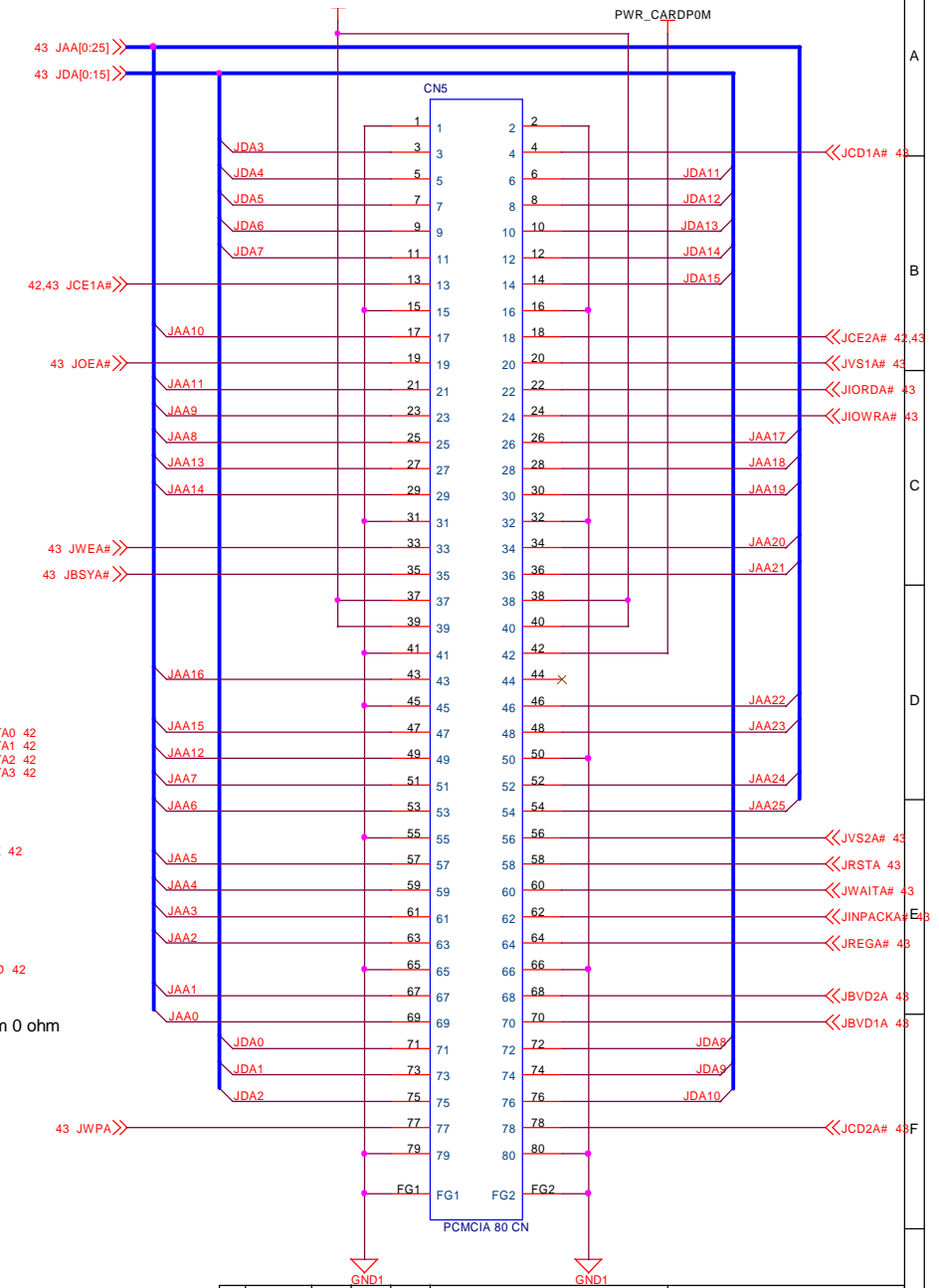
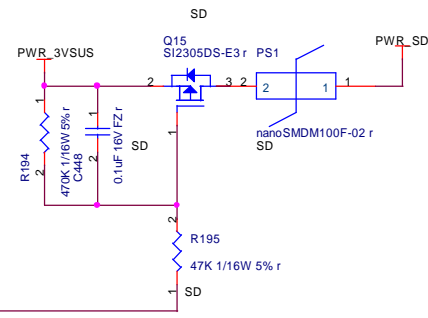
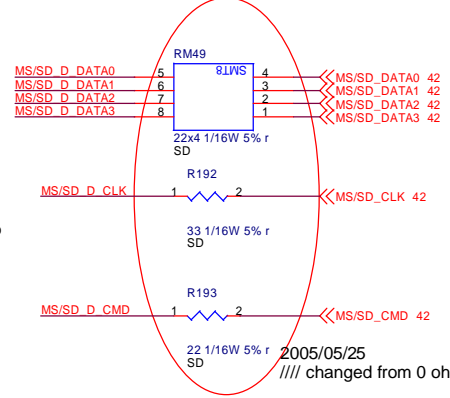
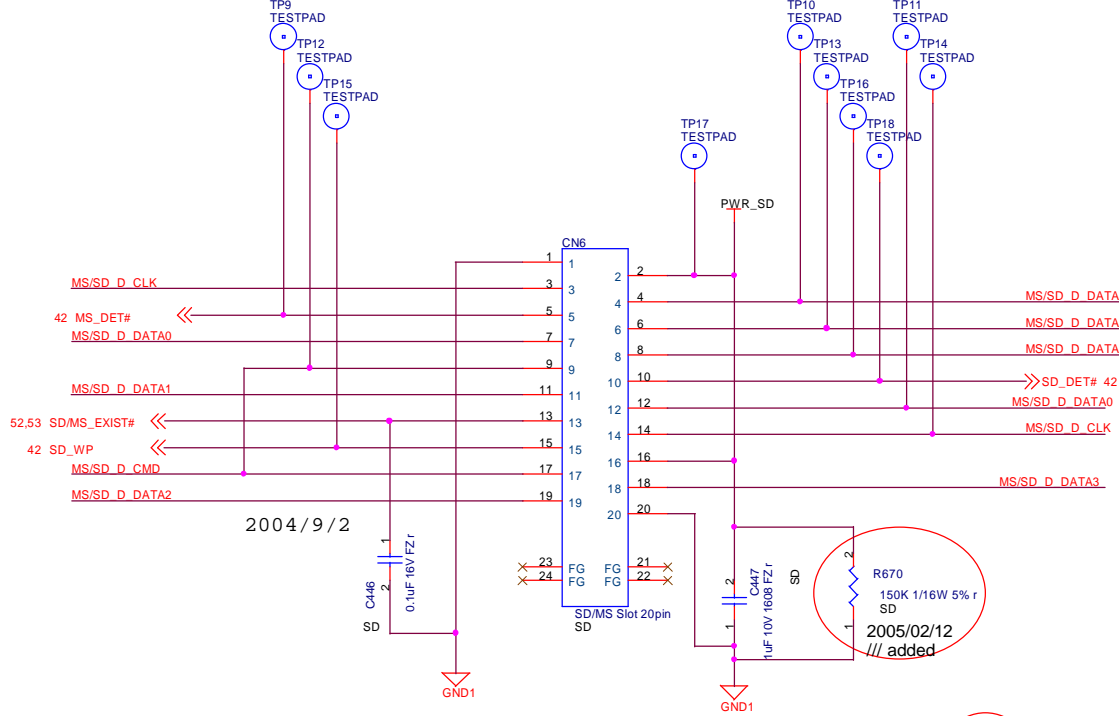
N11pinのパターンはアナログ信号のため、他の信号とは重ねないこと。



2005/02/18
 /// Changed
 2005/03/03
 /// 3300p -> 820p



TITLE										VB222AA		
DRAW. No.										C1CP231360-X3		
CAST												
Rev.	Date	Design	Check	Appr.	Description					Sheet		
Design	//	KOSHA	Check								FUJITSU LTD.	44 / 99



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[SD SLOT]

							TITLE VB222AA	
							DRAW. No. C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.			FUJITSU LTD. 45 / 99

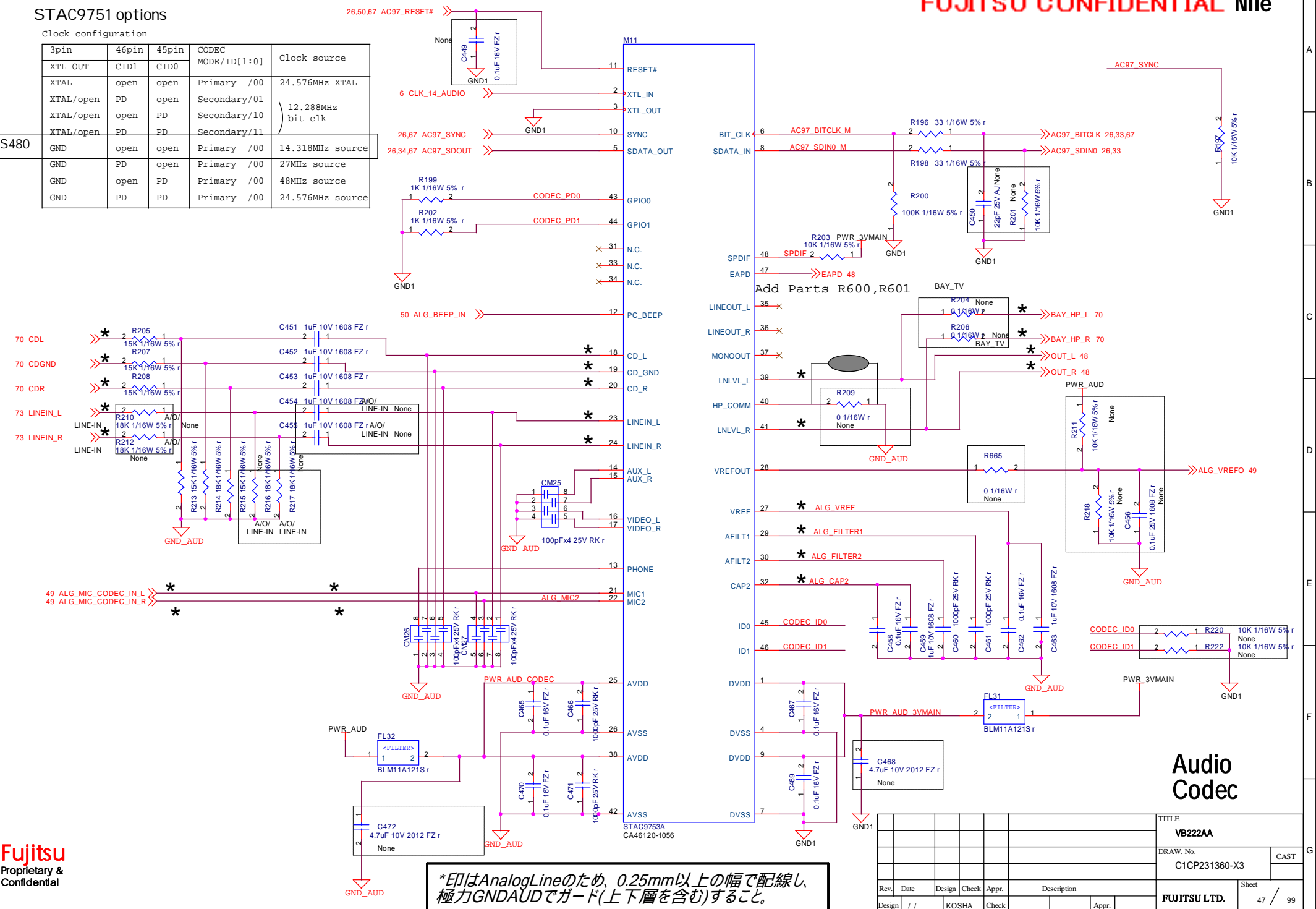
Fujitsu
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Confidential

										TITLE	
										VB222AA	
										DRAW. No.	CAST
										C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description						Sheet
Design	//	KOSHA	Check				Appr.			FUJITSU LTD.	46 / 99

STAC9751 options

Clock configuration

3pin	46pin	45pin	CODEC MODE/ID[1:0]	Clock source
XTAL_OUT	CID1	CID0	Primary /00	24.576MHz XTAL
XTAL/open	open	open	Secondary/01	12.288MHz bit clk
XTAL/open	open	PD	Secondary/10	
XTAL/open	PD	PD	Secondary/11	
RS480	GND	open	Primary /00	14.318MHz source
GND	PD	open	Primary /00	27MHz source
GND	open	PD	Primary /00	48MHz source
GND	PD	PD	Primary /00	24.576MHz source



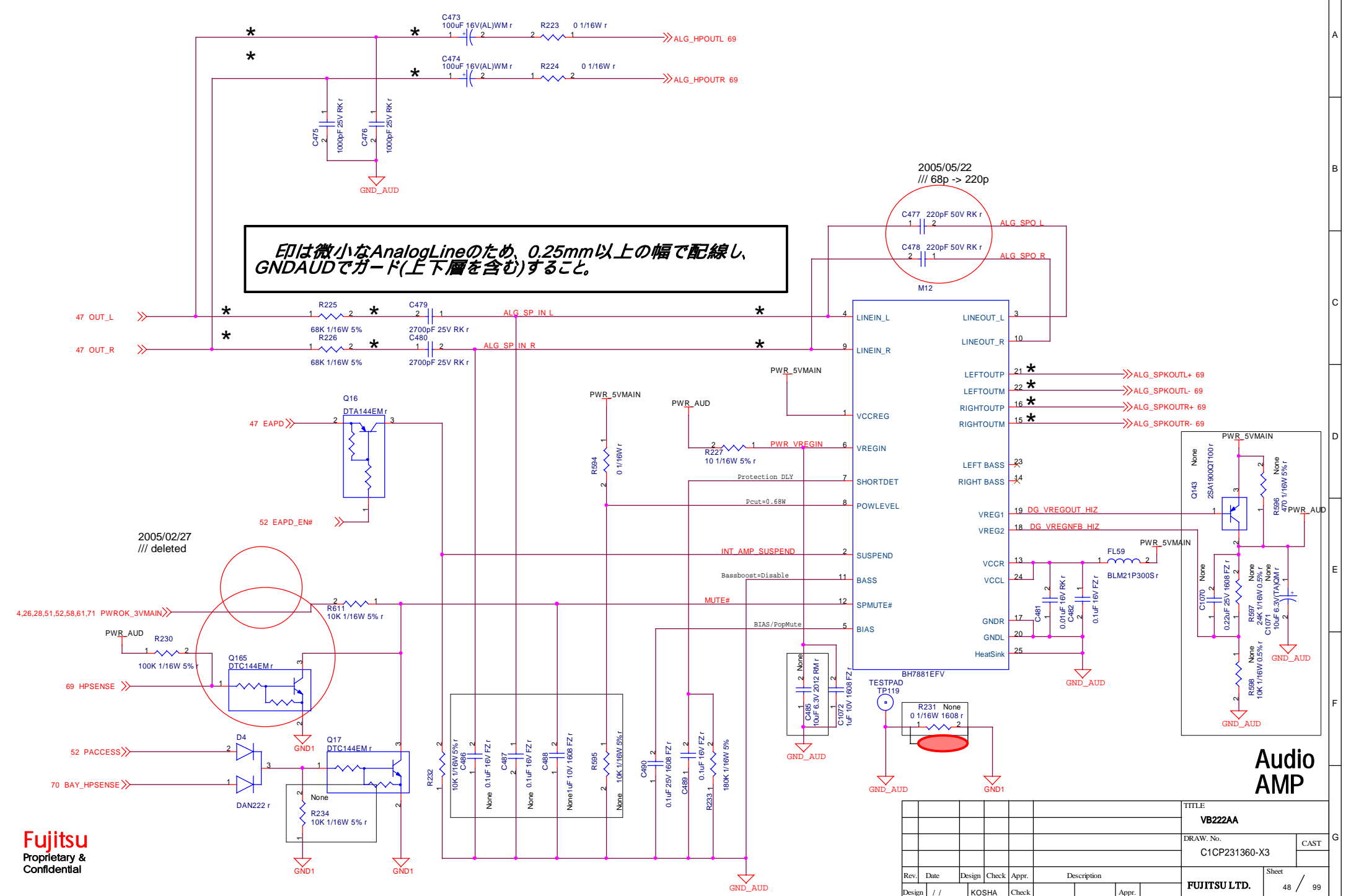
*印はAnalogLineのため、0.25mm以上の幅で配線し、極力GNDAUDでガード(上下層を含む)すること。

Audio Codec

Rev.	Date	Design	Check	Appr.	Description	TITLE	CAST
						VB222AA	
						C1CP231360-X3	
						FUJITSU LTD.	47 / 99

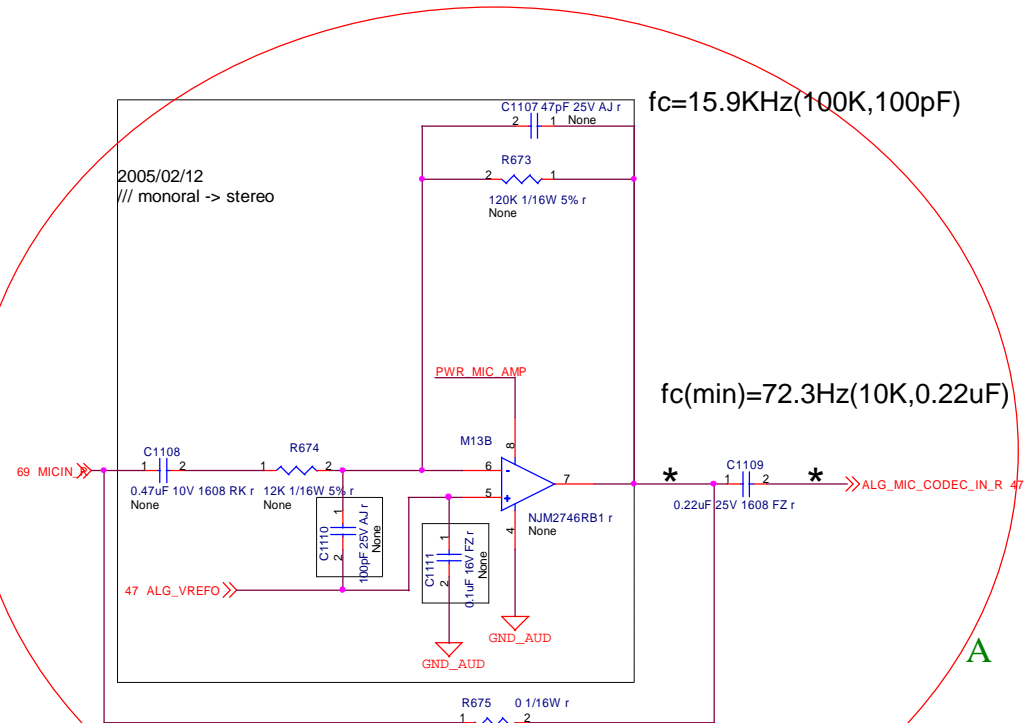
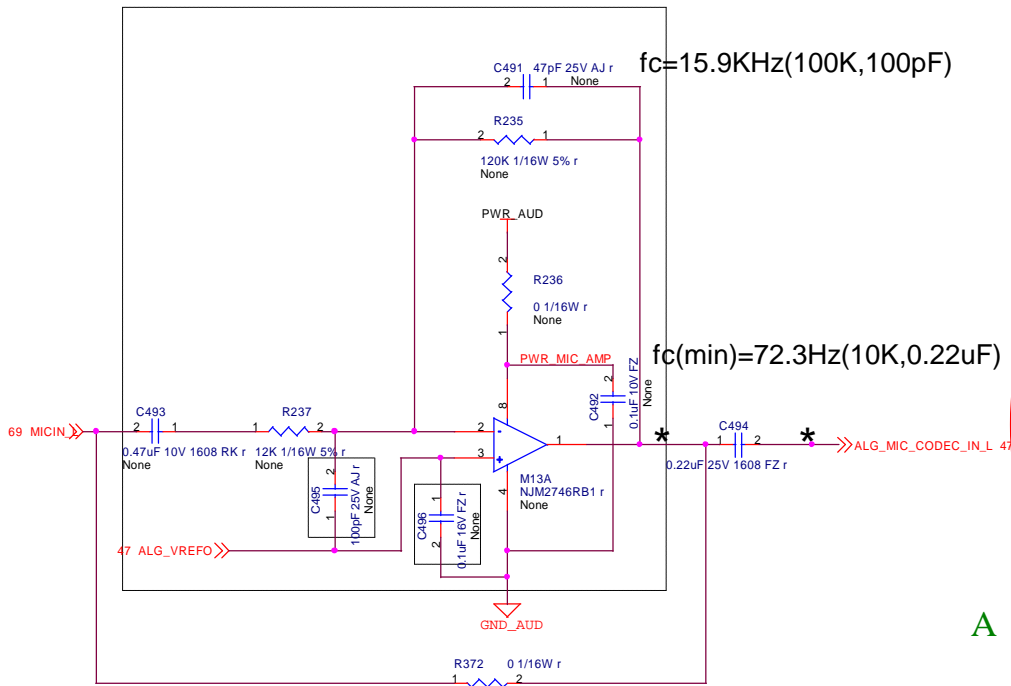
印は微小なAnalogLineのため、0.25mm以上の幅で配線し、GNDAUDでガード(上下層を含む)すること。

2005/05/22
/// 68p -> 220p

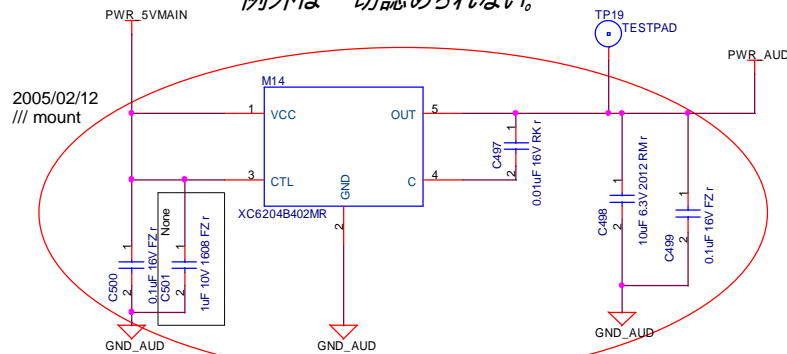


TITLE										VB222AA	
DRAW. No.										C1CP231360-X3	
CAST											
Rev.	Date	Design	Check	Appr.	Description					Sheet	
Design	/ /	KOSHA	Check								48 / 99
FUJITSU LTD.											

*印はAnalog
Lineのため、0.25mm以上の幅で配線し、
極力GNDAUDでガード(上下層を含む)すること。



A部は微小なアナログ信号のため、配線やその
周辺部品、周辺部品のパッドの周辺や上下層を
確実にGNDAUDでガードすること。
例外は一切認められない。

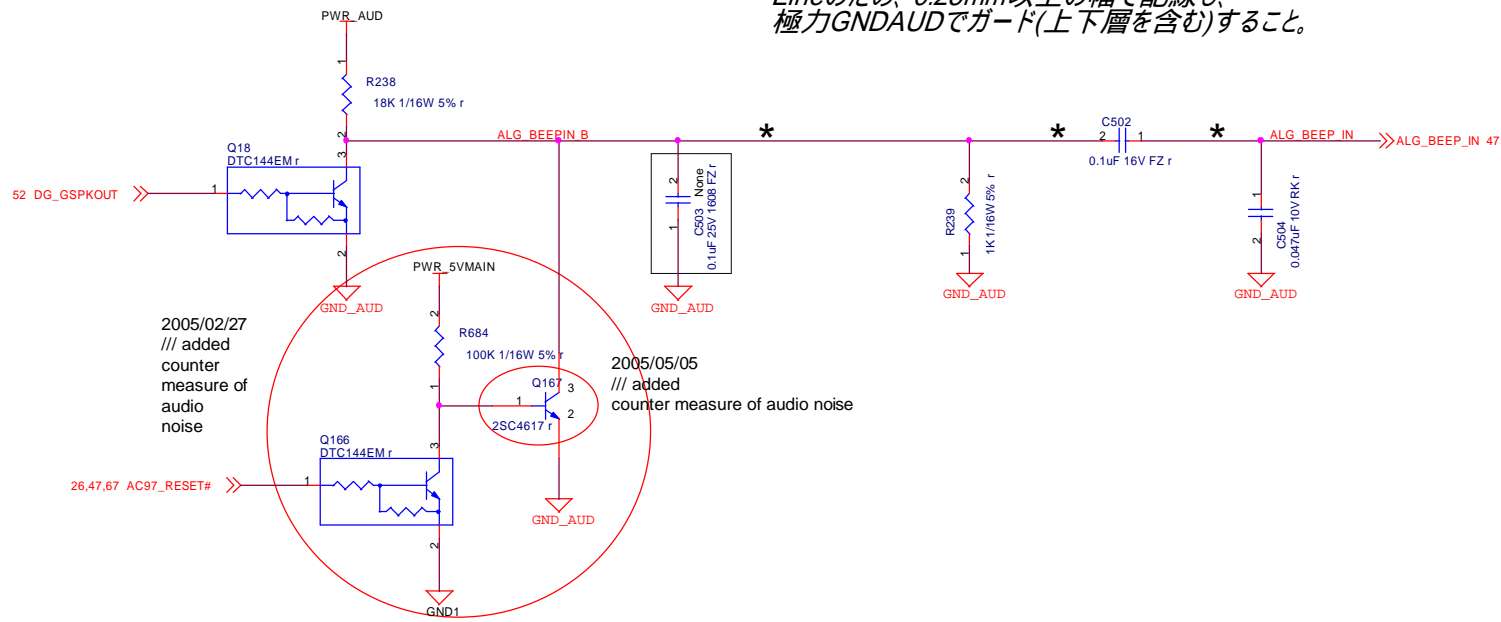


MIC AMP / AUDIO POWER

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	/ /	KOSHA	Check		Appr.			
							FUJITSU LTD.	
							49 / 99	

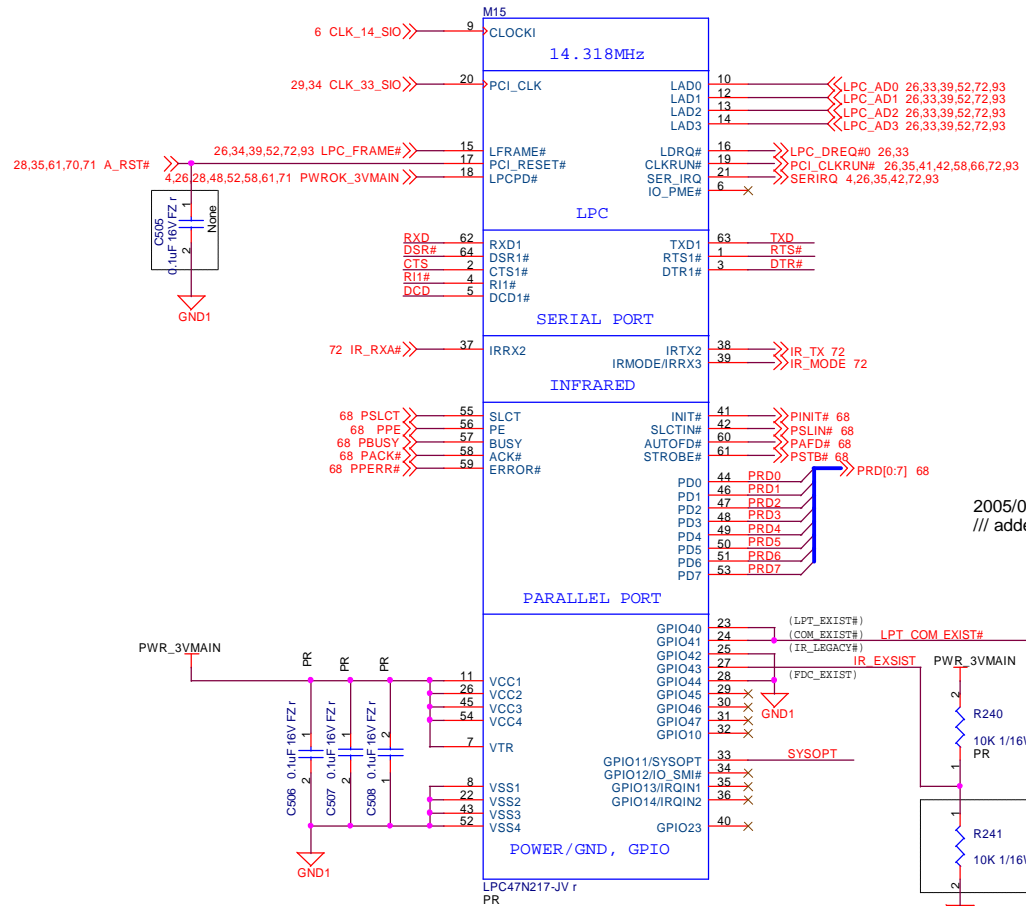
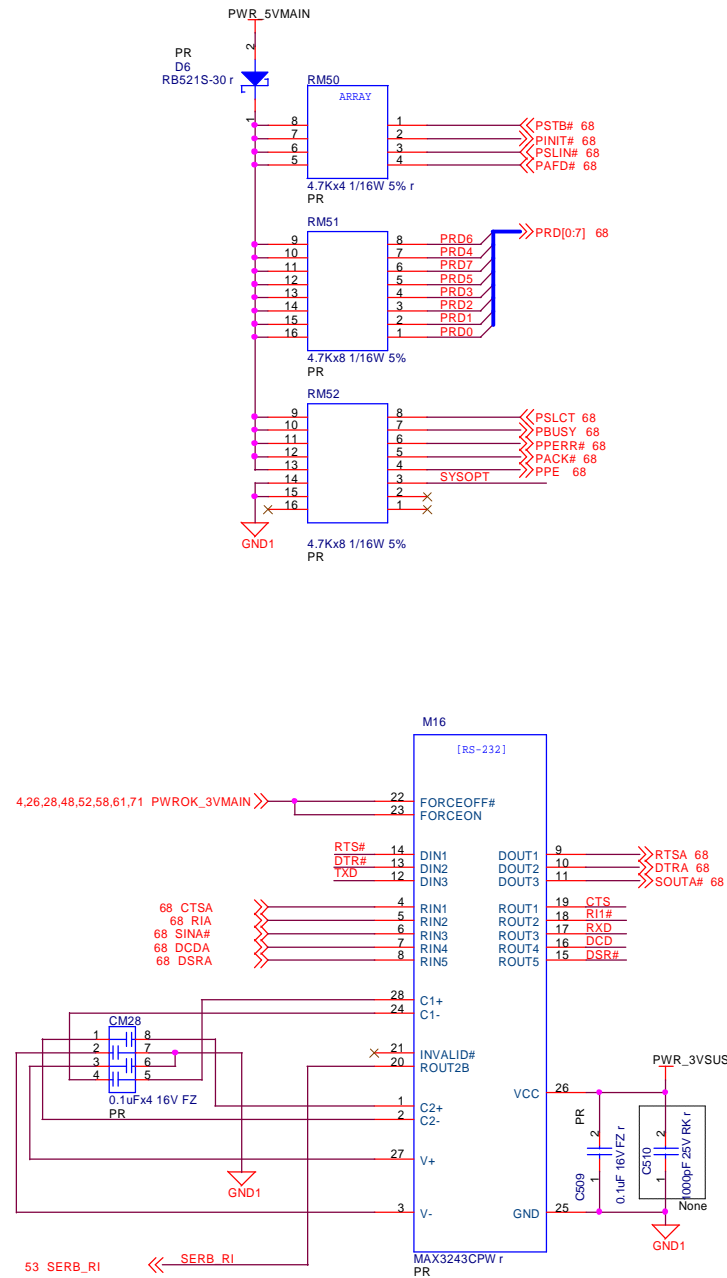
CardbusControllerの仕様で、
 Cardbus時とそれ以外のカードのときでPCSPKの出力が反転する。
 これにより、Audioボード上の最終段のゲート出力が、Cardbus時にHiになり、BEEPの口が開いた状態になって、
 そこにゲートの電源(3VMAIN)のノイズが混入するためAudio電源にてゲートしている。

*印はAnalog
 Lineのため、0.25mm以上の幅で配線し、
 極力GNDAUDでガード(上下層を含む)すること。

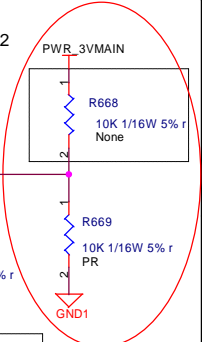


Audio BEEP

										TITLE	
										VB222AA	
										DRAW. No.	
										C1CP231360-X3	
										CAST	
Rev.	Date	Design	Check	Appr.	Description					Sheet	
Design	//	KOSHA	Check							FUJITSU LTD.	
										50 / 99	



2005/02/12
/// added



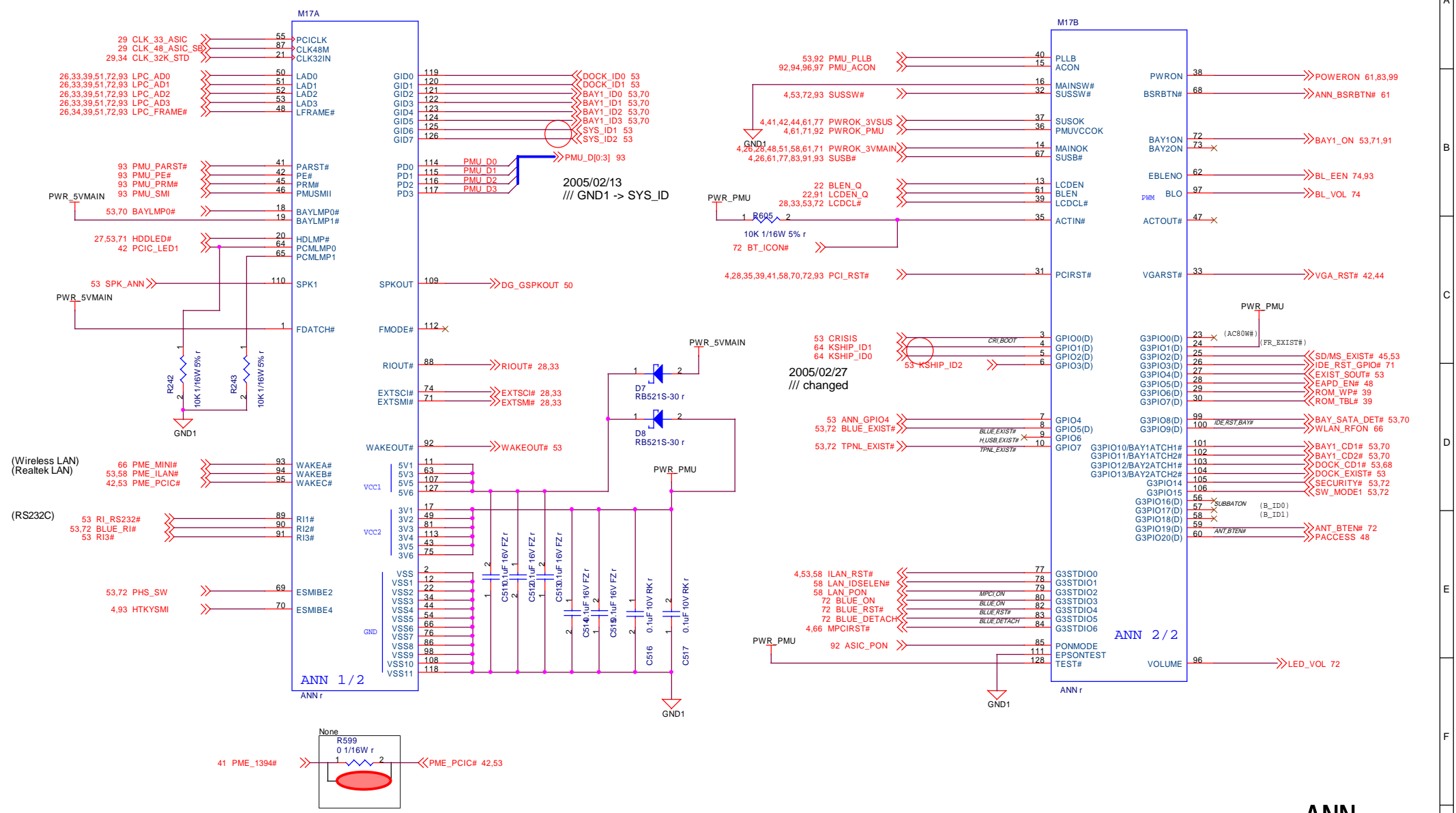
Base I/O Address

GPI011	Address
0	02E
1	04E

本ページの抵抗・コンデンサはKONA付近に配置すること。

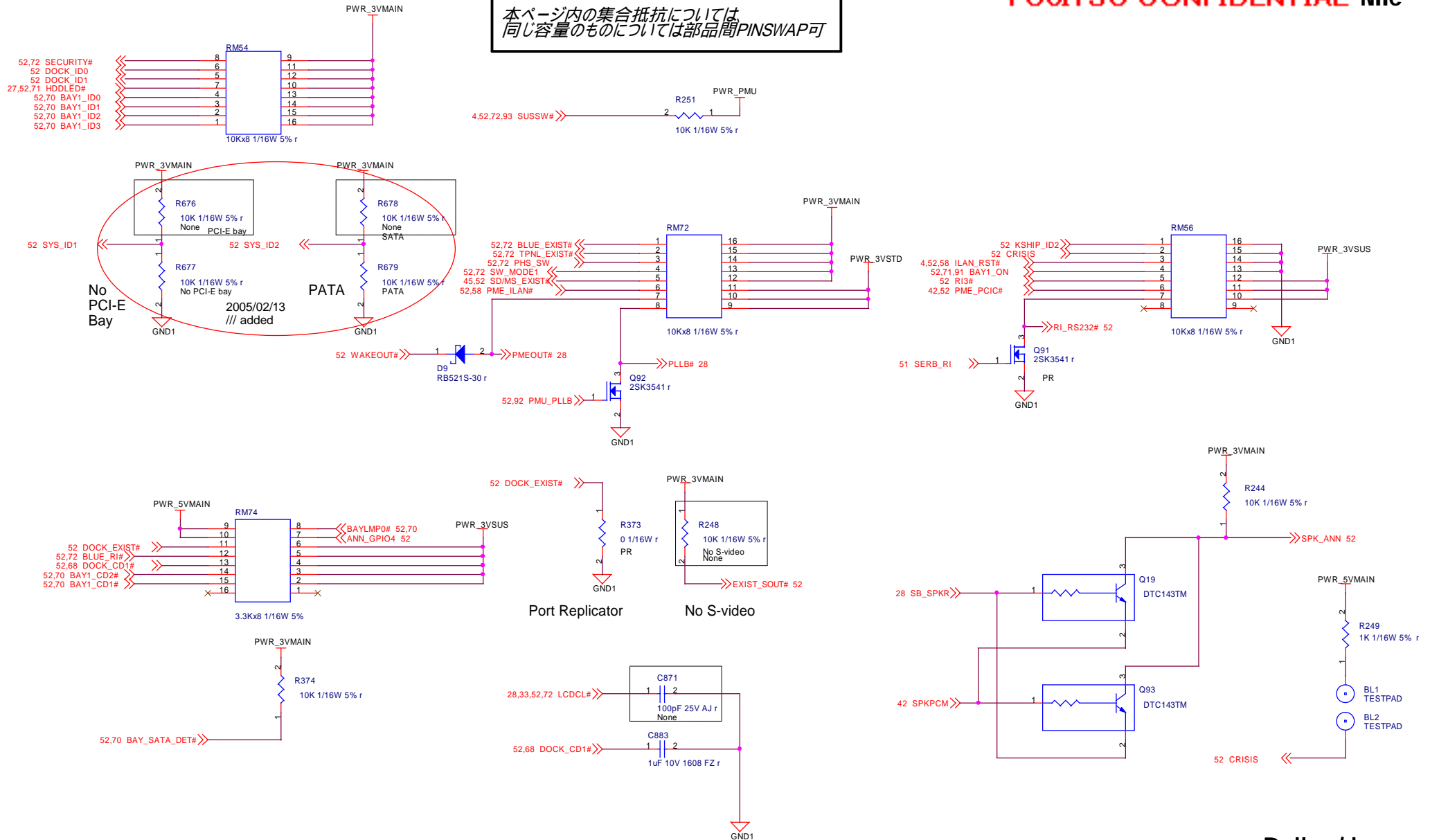
Super I/O

TITLE		VB222AA	
DRAW. No.		C1CP231360-X3	
Rev.		Date	
Design		Appr.	
KOSHA		Check	
Description		Appr.	
FUJITSU LTD.		Sheet 51 / 99	



TITLE										
VB222AA										
DRAW. No.									CAST	
C1CP231360-X3										
Rev.	Date	Design	Check	Appr.	Description			Sheet		
Design	/ /	KOSHA	Check		Appr.			FUJITSU LTD.		
									52 / 99	

本ページ内の集合抵抗については、
同じ容量のものについては部品間PINSWAP可



本ページ内の集合抵抗については、
特に指定の無い限りANNの近傍に配置すること。

Pullup/down
for ANN

							TITLE VB222AA	
							DRAW. No. C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.		FUJITSU LTD.	53 / 99

TPM Configuration

	High	Low
TPM_BADDR	4E / 4Fh	2E / 2Fh
TPM_BACCESS	Physical Presence ON	Physical Presence OFF

										TITLE		
										VB222AA		
										DRAW. No.	CAST	
										C1CP231360-X3		
Rev.	Date	Design	Check	Appr.	Description					FUJITSU LTD.		Sheet
Design	//	KOSHA	Check						Appr.		54 / 99	

										TITLE	
										VB222AA	
										DRAW. No.	CAST
										C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description						Sheet
Design	//		KOSHA	Check				Appr.		FUJITSU LTD.	55 / 99

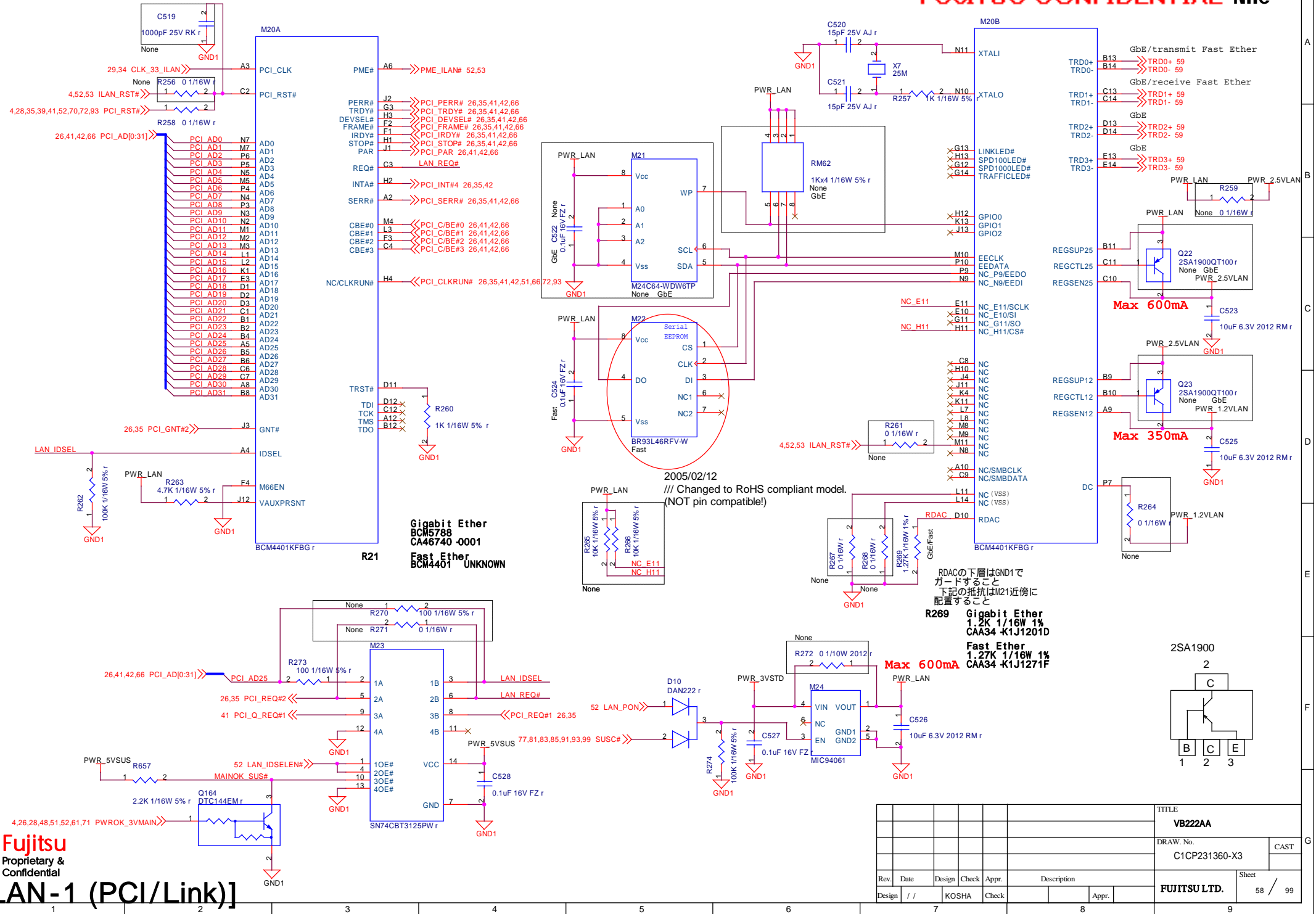
RESERVE

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						TITLE		VB222AA	
						DRAW. No.		C1CP231360-X3	
								CAST	
Rev.	Date	Design	Check	Appr.	Description				
Design	//	KOSHA	Check				Appr.	FUJITSU LTD.	
								Sheet	56 / 99

Fujitsu
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Confidential

						TITLE		VB222AA	
						DRAW. No.		C1CP231360-X3	
								CAST	
Rev.	Date	Design	Check	Appr.	Description				
Design	//	KOSHA	Check				Appr.	FUJITSU LTD.	
								Sheet	57 / 99



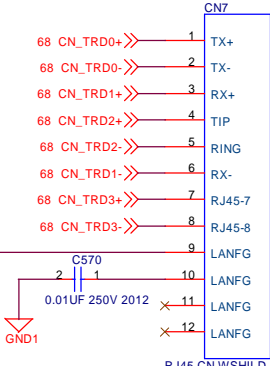
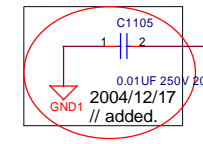
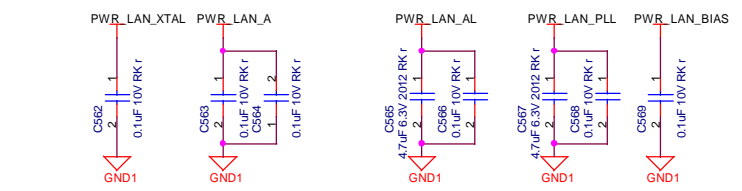
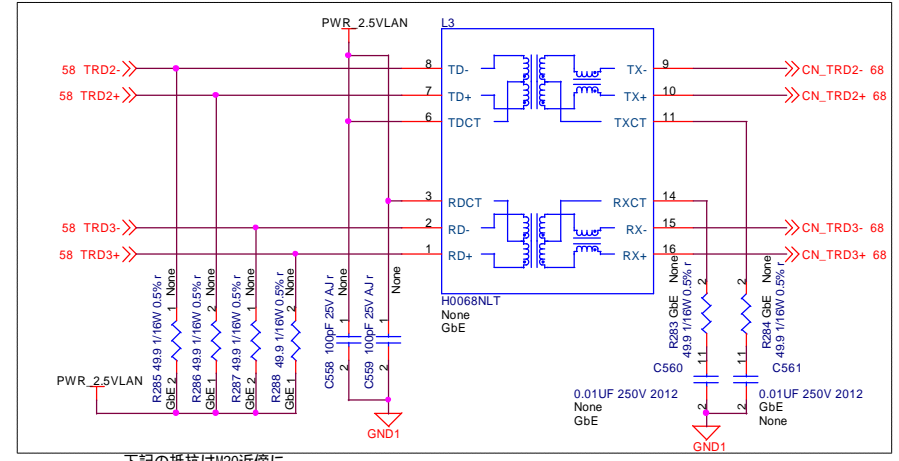
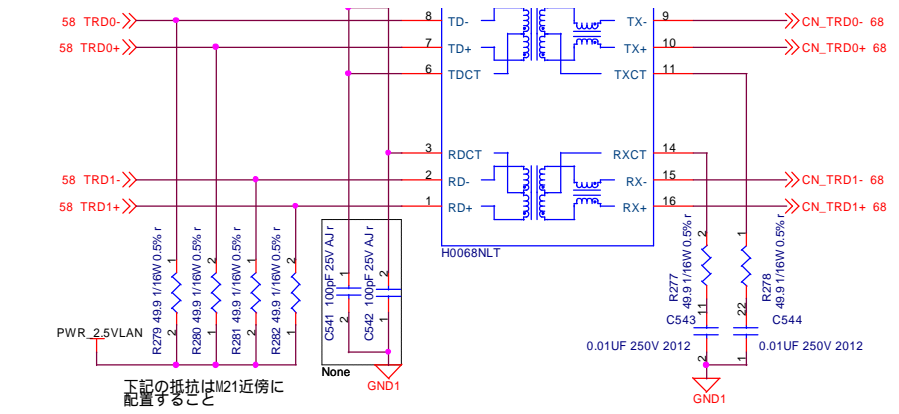
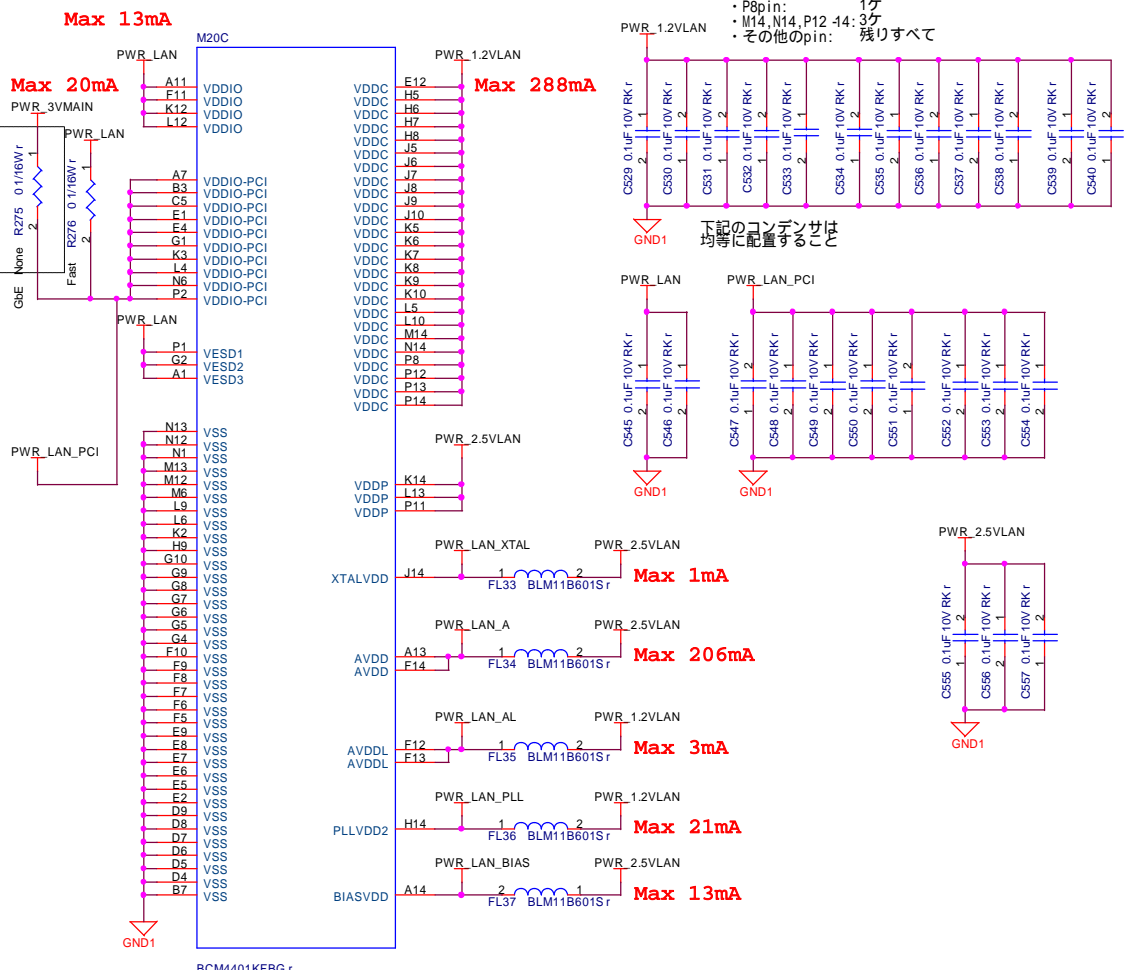
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[LAN-1 (PCI/Link)]

TITLE										VB222AA	
DRAW. No.										C1CP231360-X3	
CAST											
Rev.	Date	Design	Check	Appr.	Description					Sheet	
Design	/ /	KOSHA	Check							FUJITSU LTD.	
										58 / 99	

下記のコンデンサ配置数
 ・E12pin: 1ヶ
 ・P8pin: 1ヶ
 ・M14, N14, P12-14: 3ヶ
 ・その他のpin: 残りすべて

FUJITSU CONFIDENTIAL Nile



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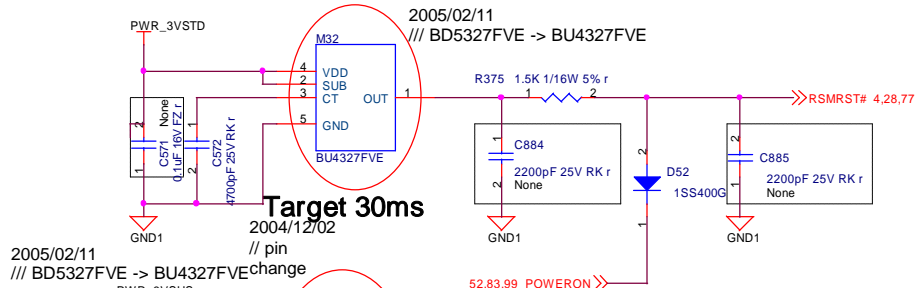
[LAN-2 (POW/TRANS/CN)]

					TITLE	
					VB222AA	
					DRAW.No.	
					C1CP231360-X3	
					CAST	
Rev.	Date	Design	Check	Appr.	Description	
Design	//	KOSHA	Check	Appr.		
					FUJITSU LTD.	
					Sheet	
					59 / 99	

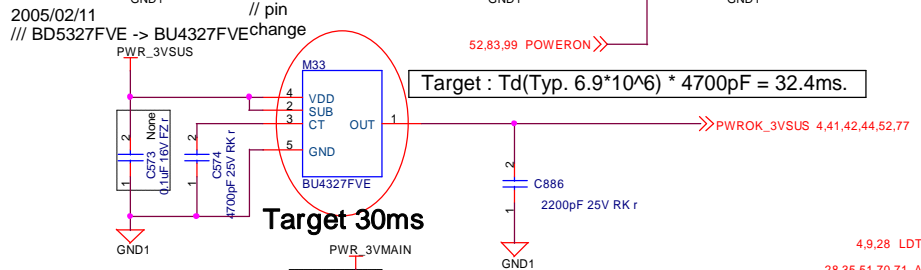
構造仕様: カバーオープン時:SWを押している
 SW仕様: フッシュ時=回路未接続(=HIGH)
 信号要求SW仕様: オープン時=HIGH
 カバークローズ時:SWを離す
 オープン時=回路接続(=LOW)
 クローズ時=LOW



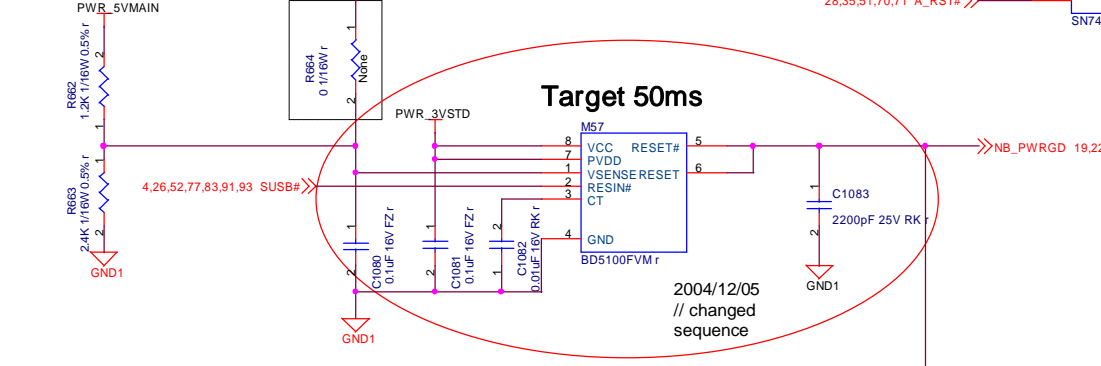
										TITLE		
										VB222AA		
										DRAW. No.	CAST	
										C1CP231360-X3		
Rev.	Date	Design	Check	Appr.	Description					FUJITSU LTD.		Sheet
Design	//	KOSHA	Check						Appr.		60 / 99	



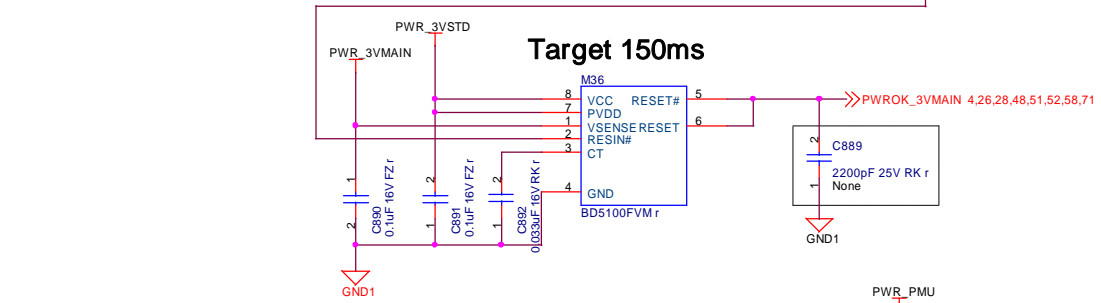
Target 30ms



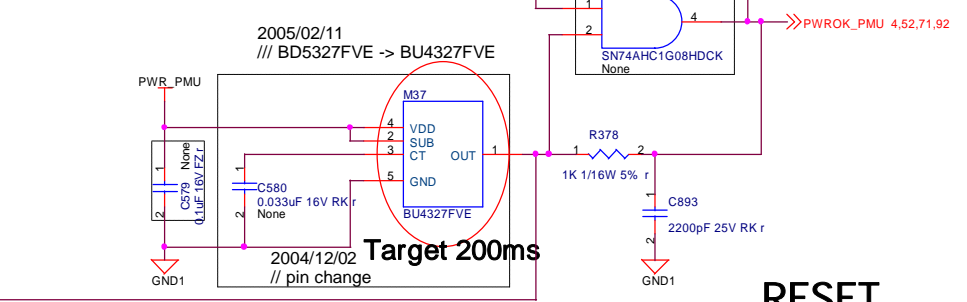
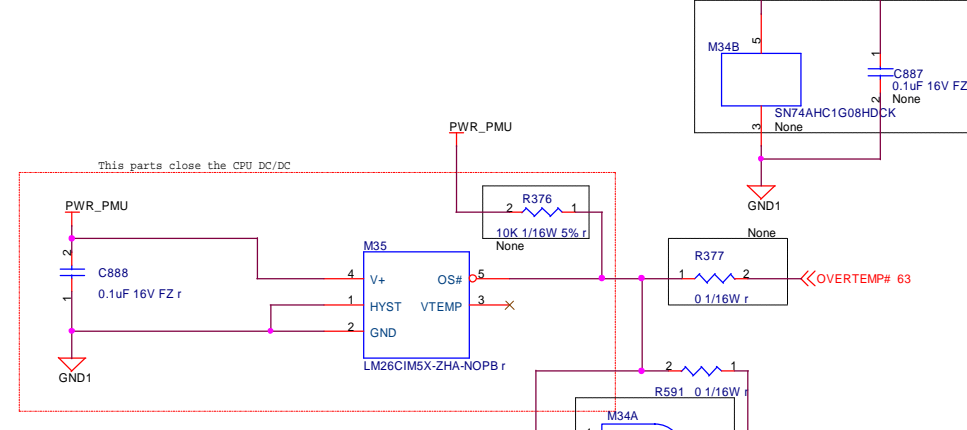
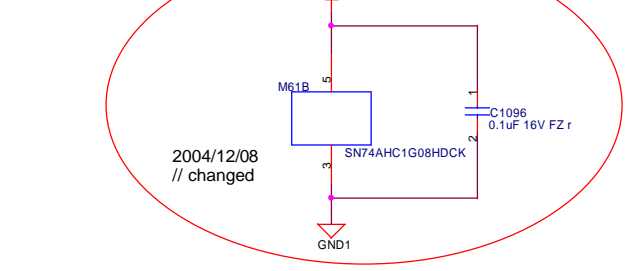
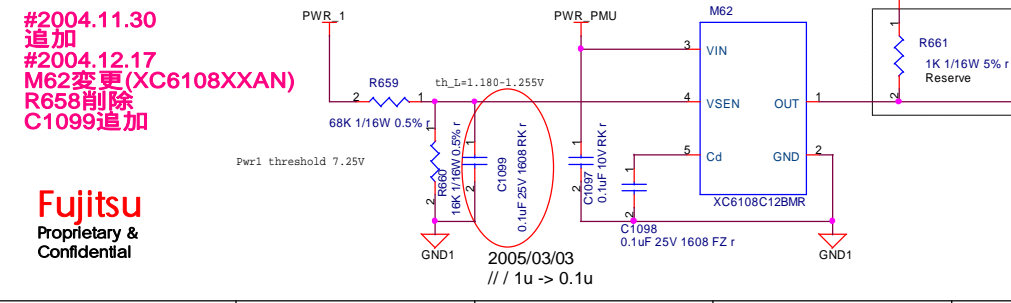
Target 30ms



Target 50ms



Target 150ms



Target 200ms

#2004.11.30 追加
#2004.12.17 M62変更(XC6108XXAN)
R658削除
C1099追加



遅延ターゲット
BU4327FVE / BD5327FVE:
 $T_{plh}(s) = 0.69(TYP) \times 10(M) \times CT(F)$

RESET

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.
Design	//	KOSHA	Check		Appr.			
							Sheet	
							61 / 99	

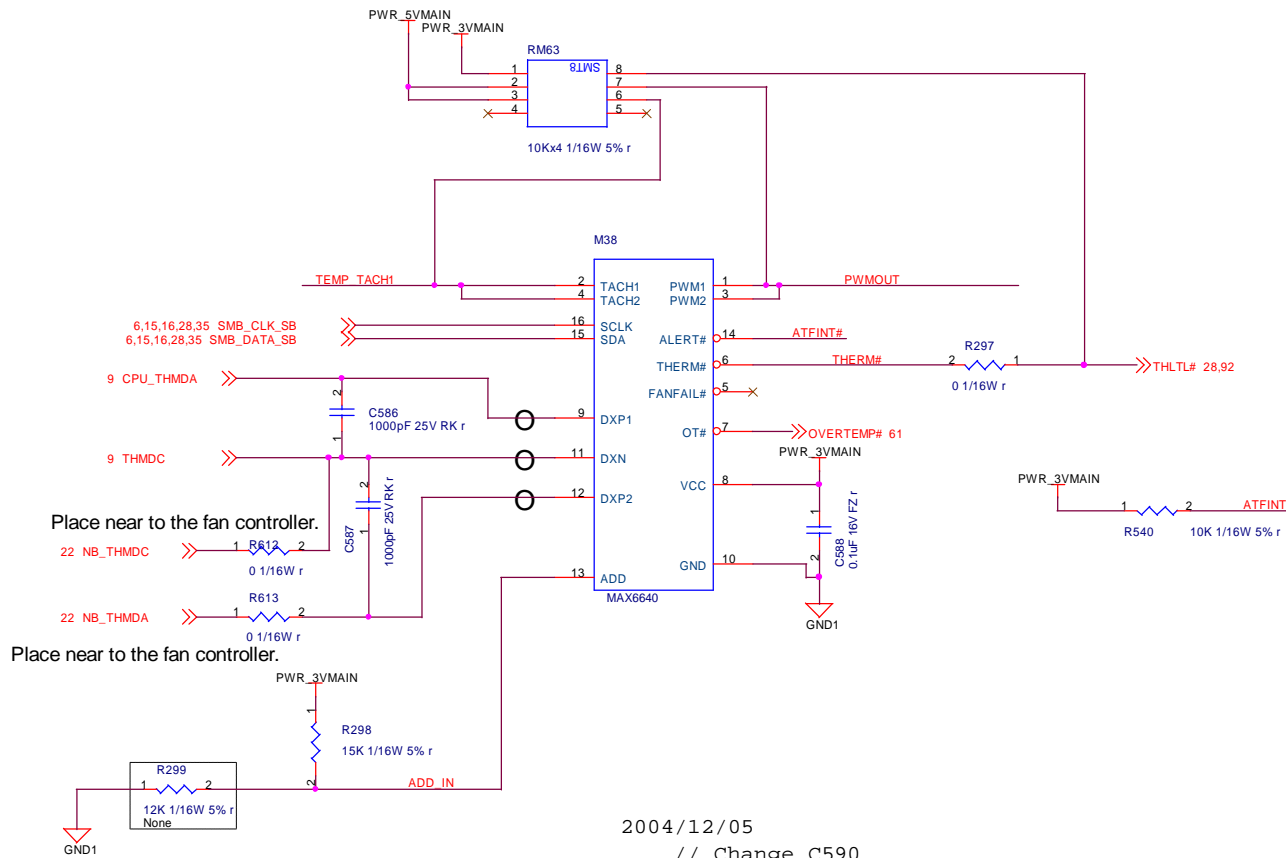
SN74AHCT08
 VCC : 4.5V - 5.5V
 VIH : 2.00V
 VIL : 0.80V
 VI : 0V - 5.5V

Reserve

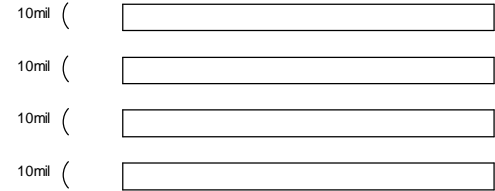
Fujitsu
 Proprietary &
 Confidential

SN74LV05A
 VCC : 2.0V -
 5.5V
 VIH : VCC * 0.7
 VIL : VCC * 0.3
 VI : 0V - 5.5V

										TITLE	
										VB222AA	
										DRAW. No.	
										C1CP231360-X3	
										CAST	
										Sheet	
										62 / 99	
Rev.	Date	Design	Check	Appr.	Description					FUJITSU LTD.	
Design	//	KOSHA	Check						Appr.		

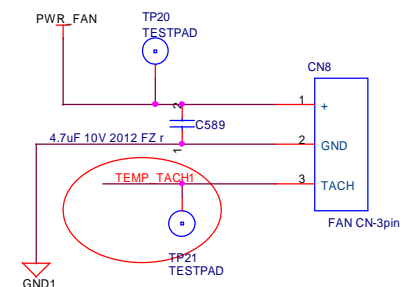
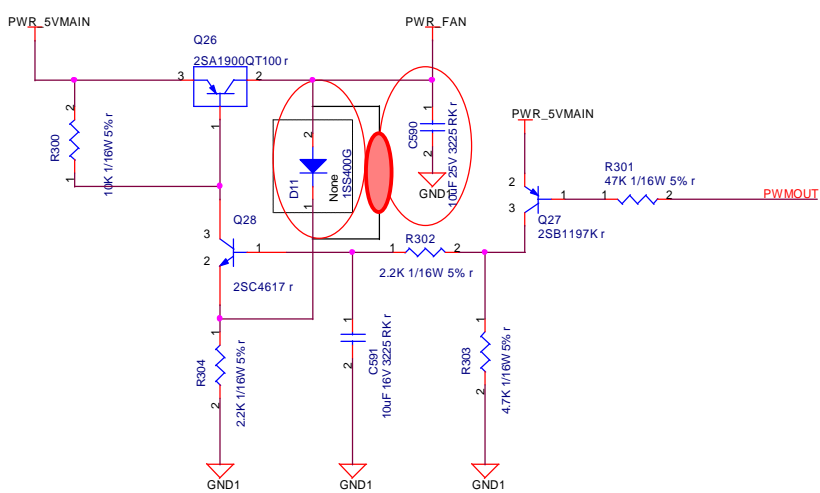


印の付いた信号線(CPU_THMDA,CPU_THMDC)は、GND1で両側をガードすること (下図参照)



ADM1034
SMB Address : 5Eh

2004/12/05
// Change C590
// Unmount D11

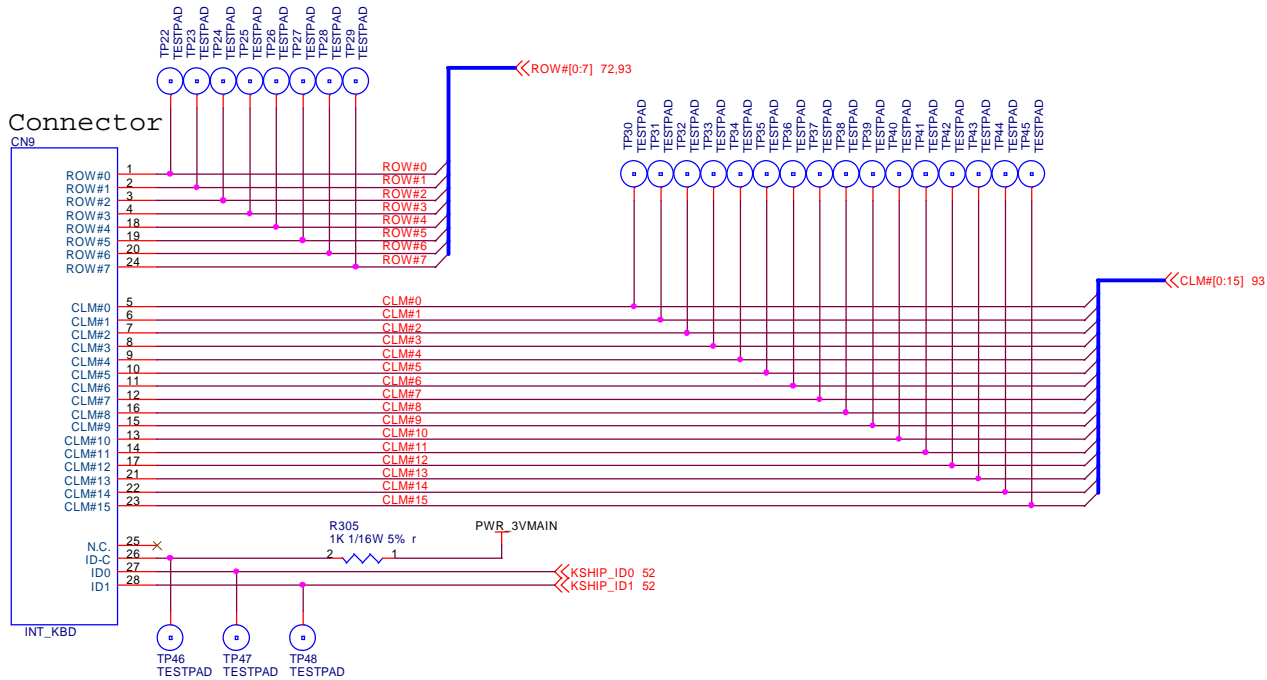


2004/12/08
// net name change

[ADM1034/FAN CN] Thermal IC

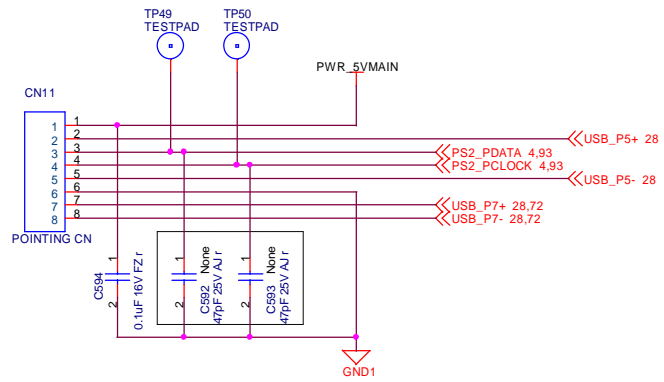
							TITLE		
							VB222AA		
							DRAW. No.		
							C1CP231360-X3		
							CAST		
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet 63 / 99
Design	//	KOSHA	Check		Appr.				

KeyBoard Connector



Keyboard Strap (N86C-7664-0203-E)
 ID1: ID0 (KBC Side)
 JP 1 1
 US 1 0
 UK 0 1

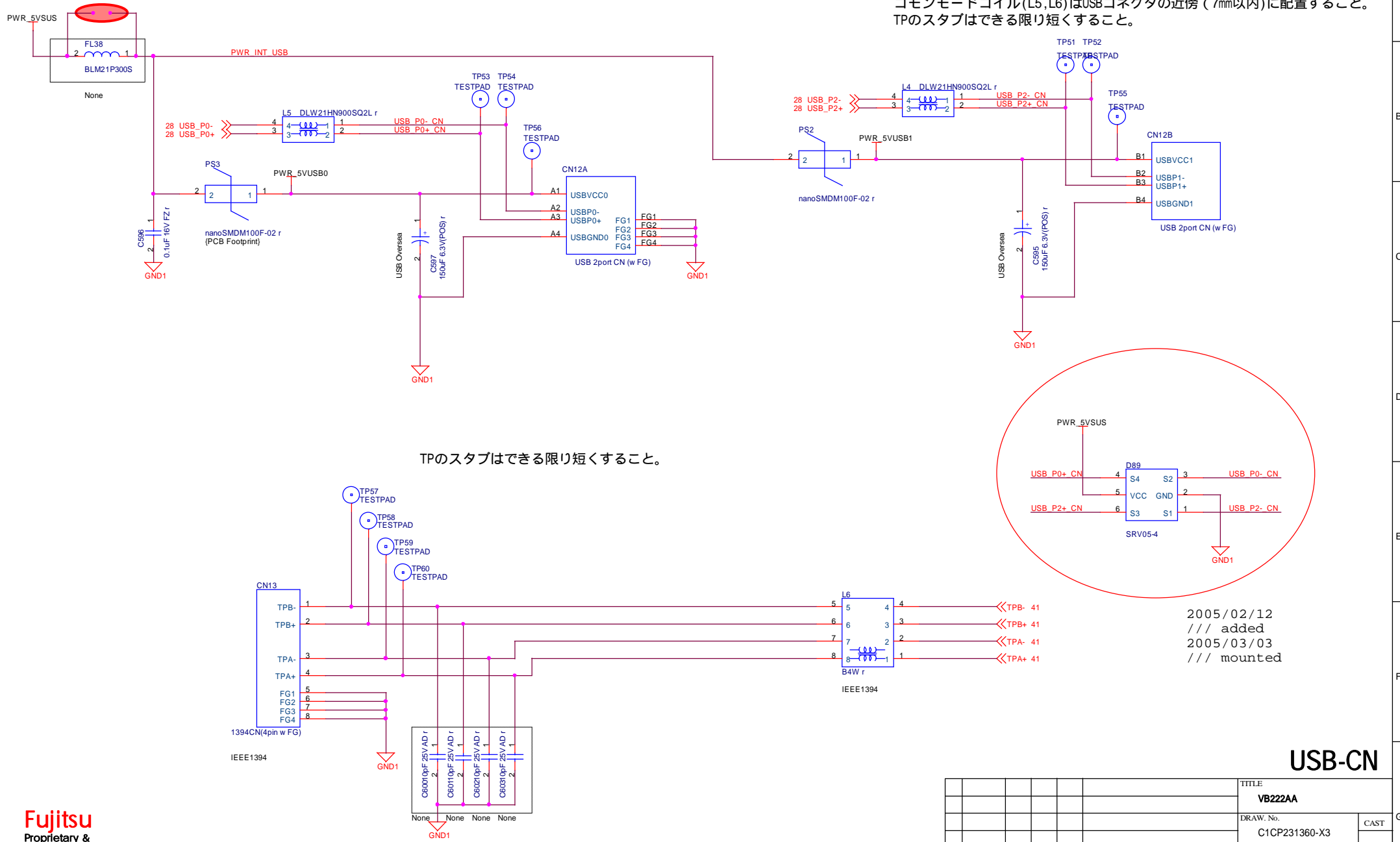
2005/03/03
 /// deleted 6 pins connectr



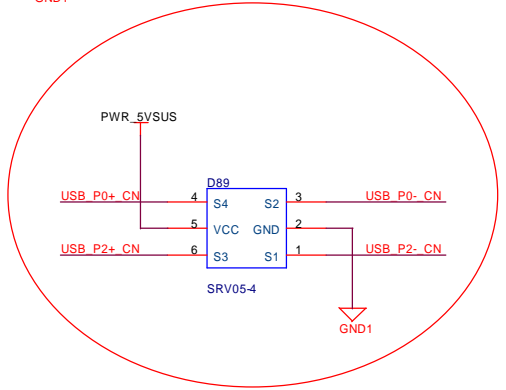
KB/Pointing-CN

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check					
							FUJITSU LTD.	
							Sheet	
							64 / 99	

コモンモードコイル(L5,L6)はUSBコネクタの近傍 (7mm以内)に配置すること。
 TPのスタブはできる限り短くすること。



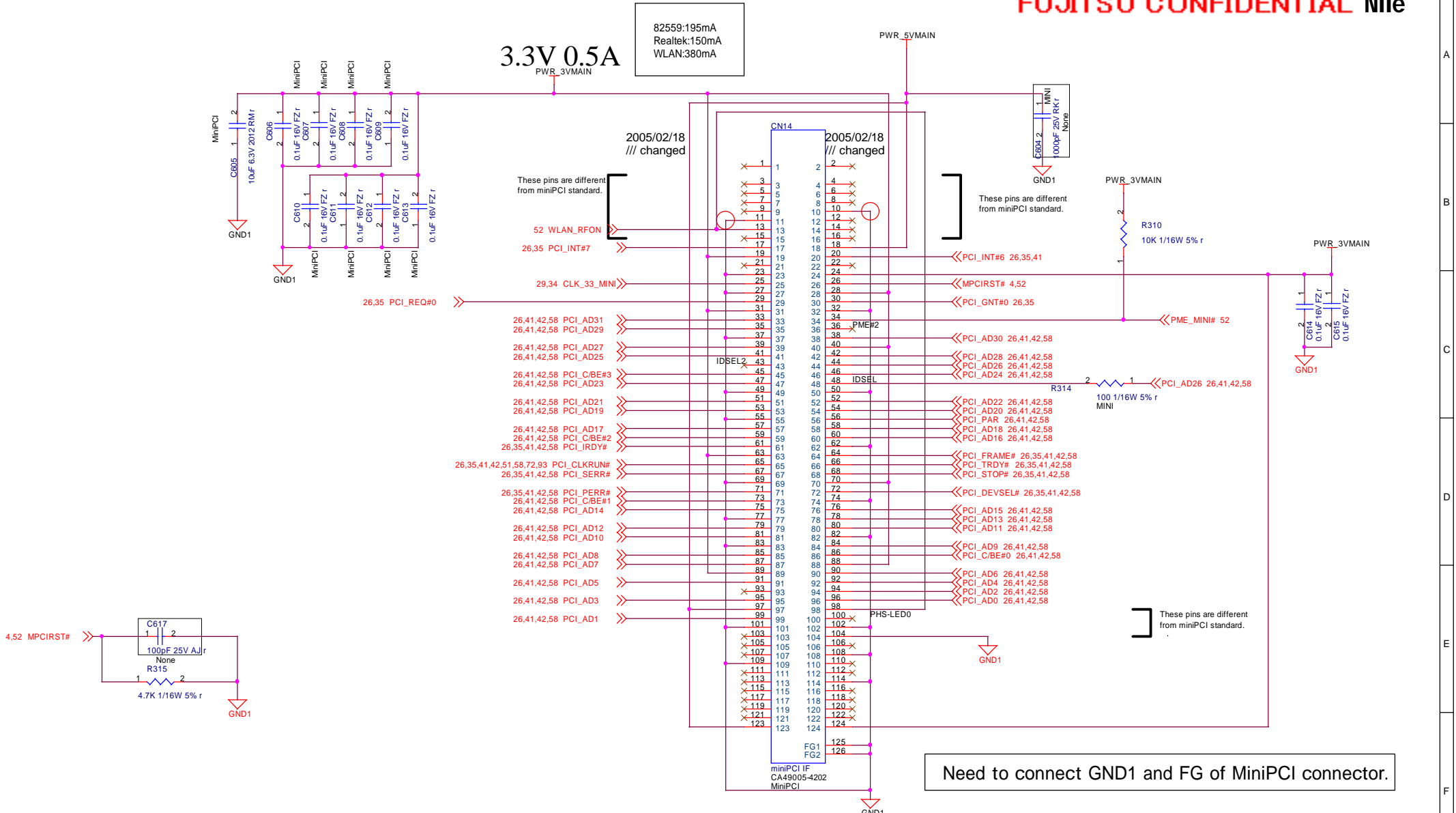
TPのスタブはできる限り短くすること。



2005/02/12
 /// added
 2005/03/03
 /// mounted

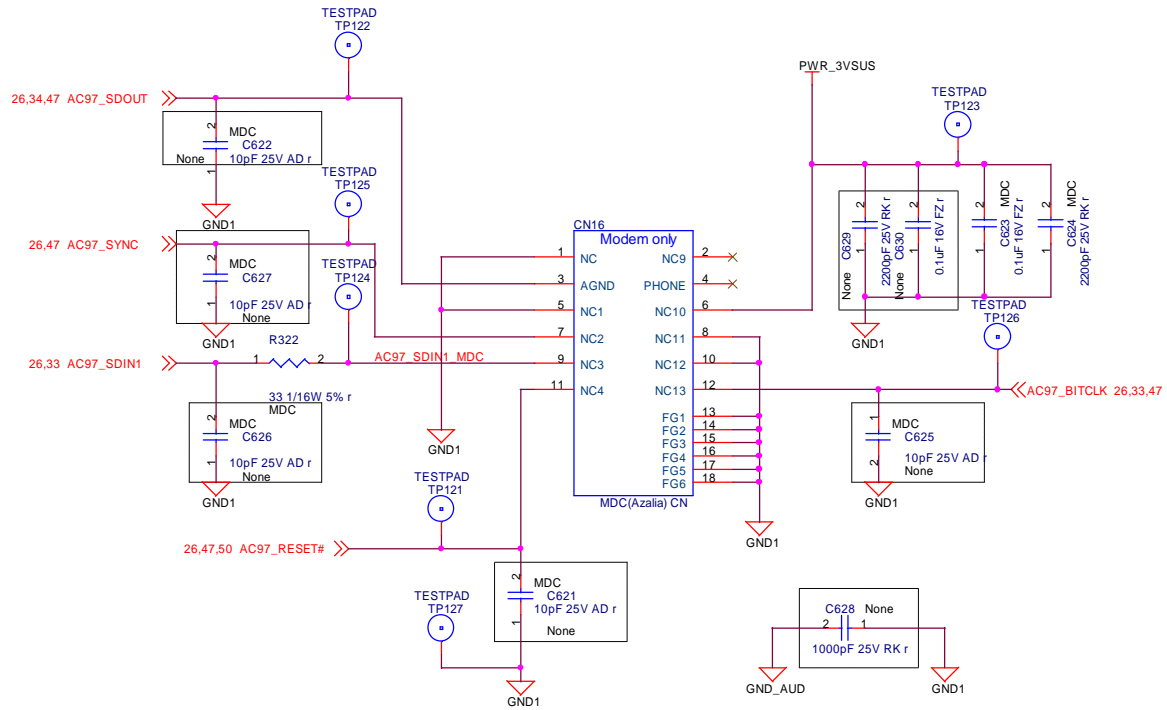
Need to have GND1 guard for USB signal.

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
							Sheet	
							65 / 99	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	
Design	//	KOSHA	Check				Appr.	



MiniPCI CN

							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Sheet 66 / 99
Design	/ /	KOSHA	Check		Appr.			
							FUJITSU LTD.	



AC97_BITCLK, AC97_RESET#はGND1でガードすること。

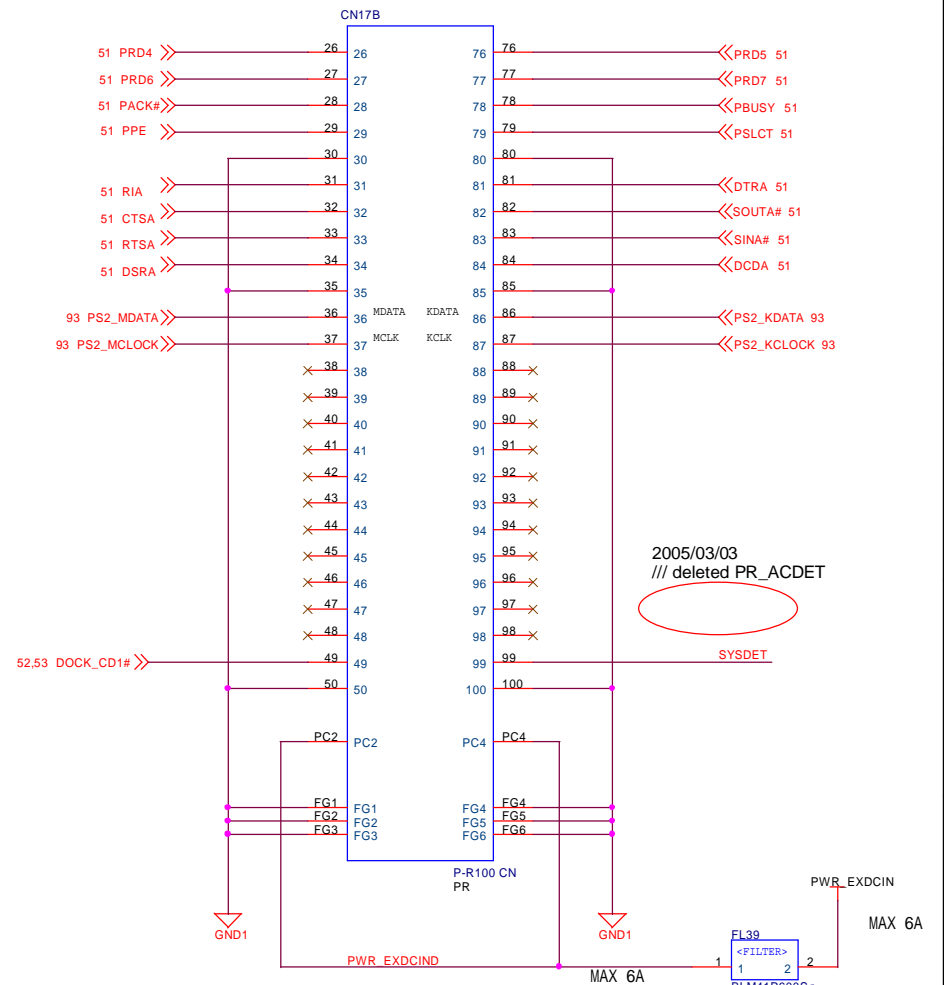
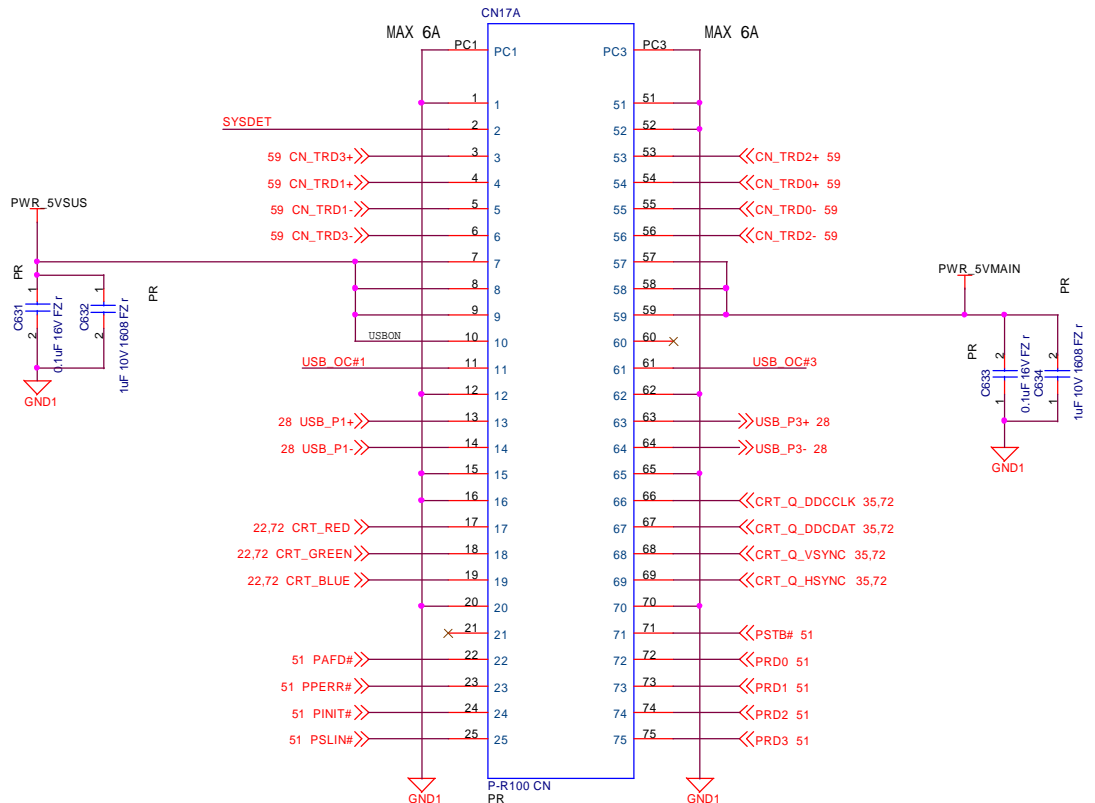
モジュールの固定用ネジ穴はGND1に接続する。

2004/12/08
// MDC 1.0
connector
deleted

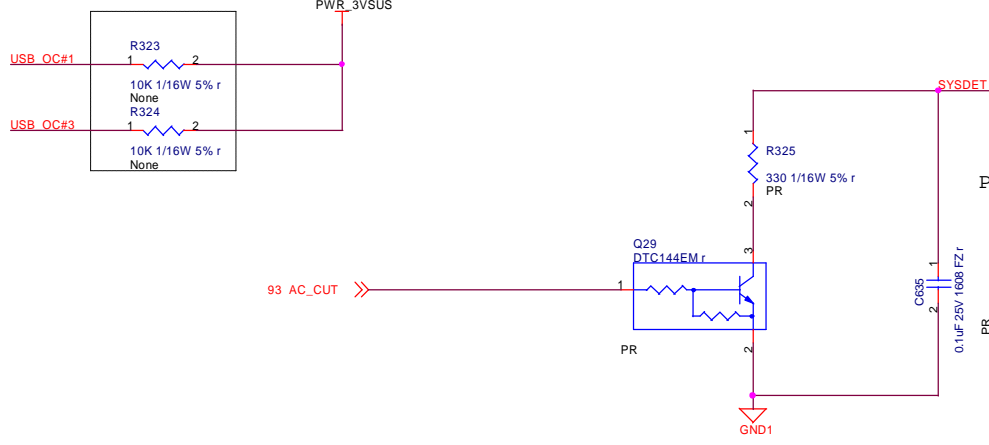
2004/12/08
// net name
change

MDC Modem

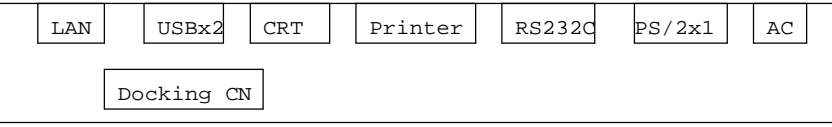
							TITLE VB222AA	
							DRAW. No. C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet 67 / 99
Design	//	KOSHA	Check		Appr.			
							FUJITSU LTD.	



2005/03/03
// deleted PR_ACDET



Port replicator Layout

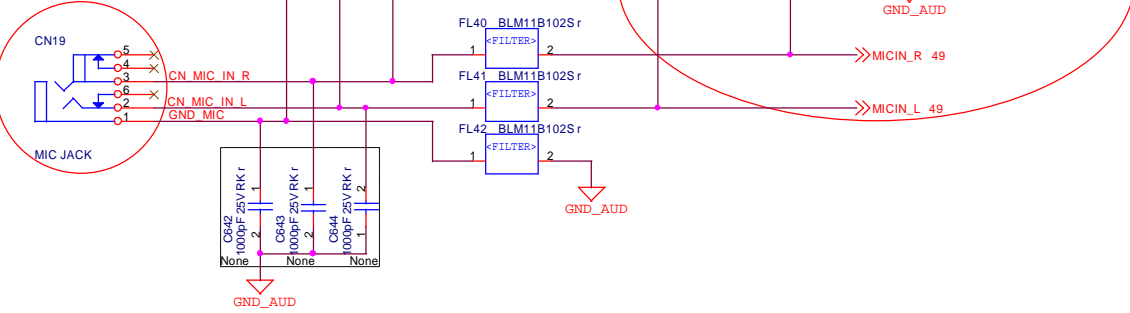


[CN P-R]

TITLE VB222AA								DRAW. No. C1CP231360-X3	
Rev.								CAST	
Description								Sheet 68 / 99	
Design	Date	Design	Check	Appr.	Appr.			Fujitsu Ltd.	

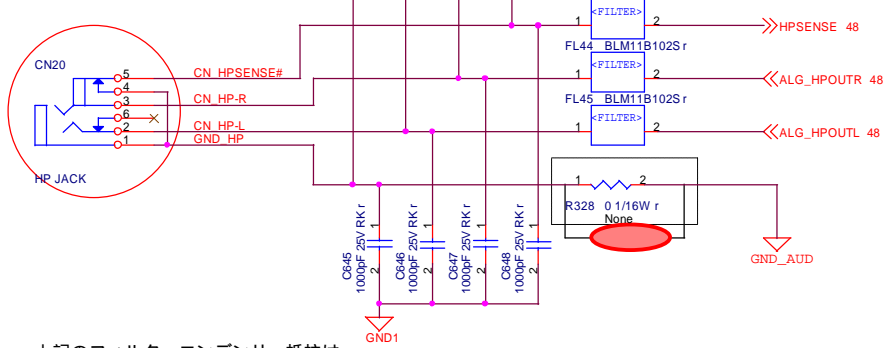
全項AUDIO AREA

2005/02/16
/// changed



上記のフィルタ、コンデンサ、抵抗は MIC JACKの近くに配置すること。

2005/02/16
/// changed



上記のフィルタ、コンデンサ、抵抗は HP JACKの近くに配置すること。

本ページ中に記載されているフィルタ(FLxx)はそれぞれ接続されているコネクタの近くに配置し、フィルターコネクタ間の配線は非常に短く配線すること。

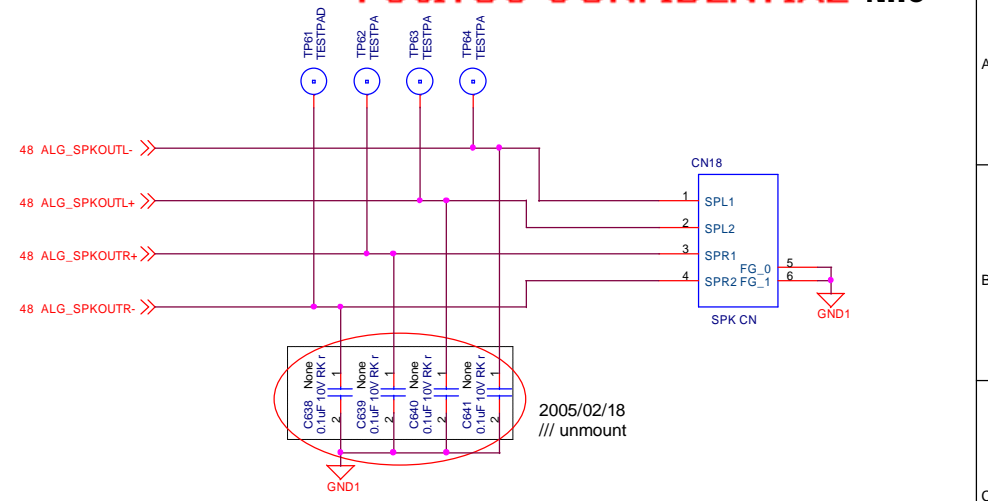
The filters in this page (referred with FLxx) have to be placed near each connector connecting to respective filters. The traces between connector and filter have to be short as much as possible.

本項中 印のついたパターンは、GND_AUDでガードし、その上下はGND_AUDのベタパターンで覆うこと。また、Mxの下の基板面およびその下の層には、デジタル系の信号線を配線しないこと。

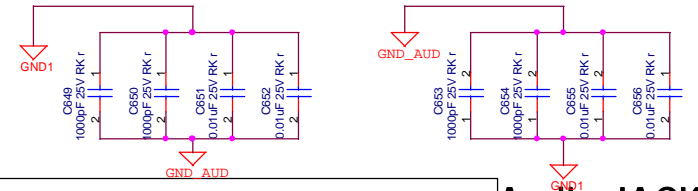
The traces marked with 印 have to be guarded both side and both adjacent layer with AUDIOGND. Underneath Mx on surface layer and in one more internal layer don't allow digital traces to be run.

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Proprietary &
Confidential

本Pageの部品は、それぞれのコネクタの近くに配置すること。 Audio-JACK

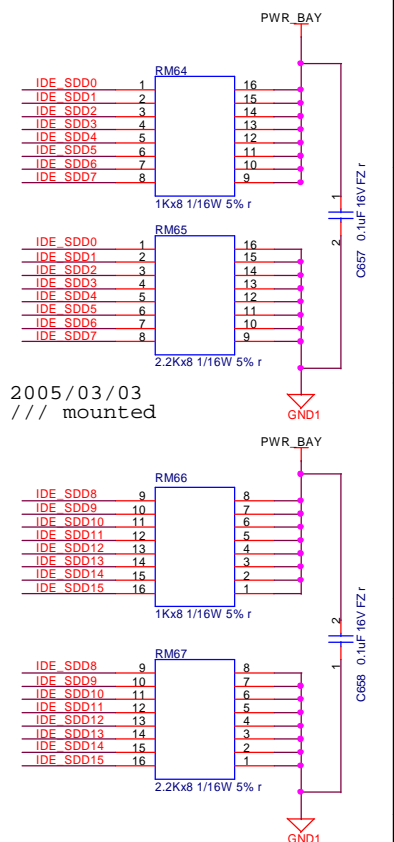
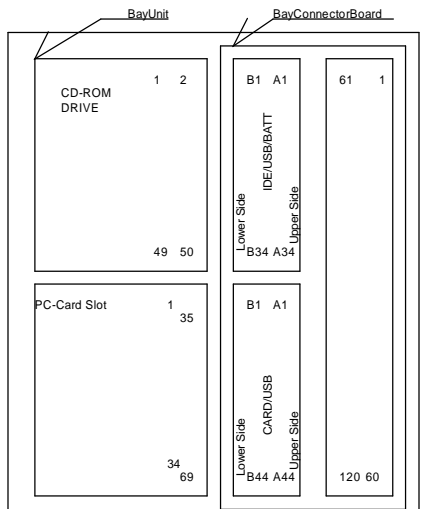
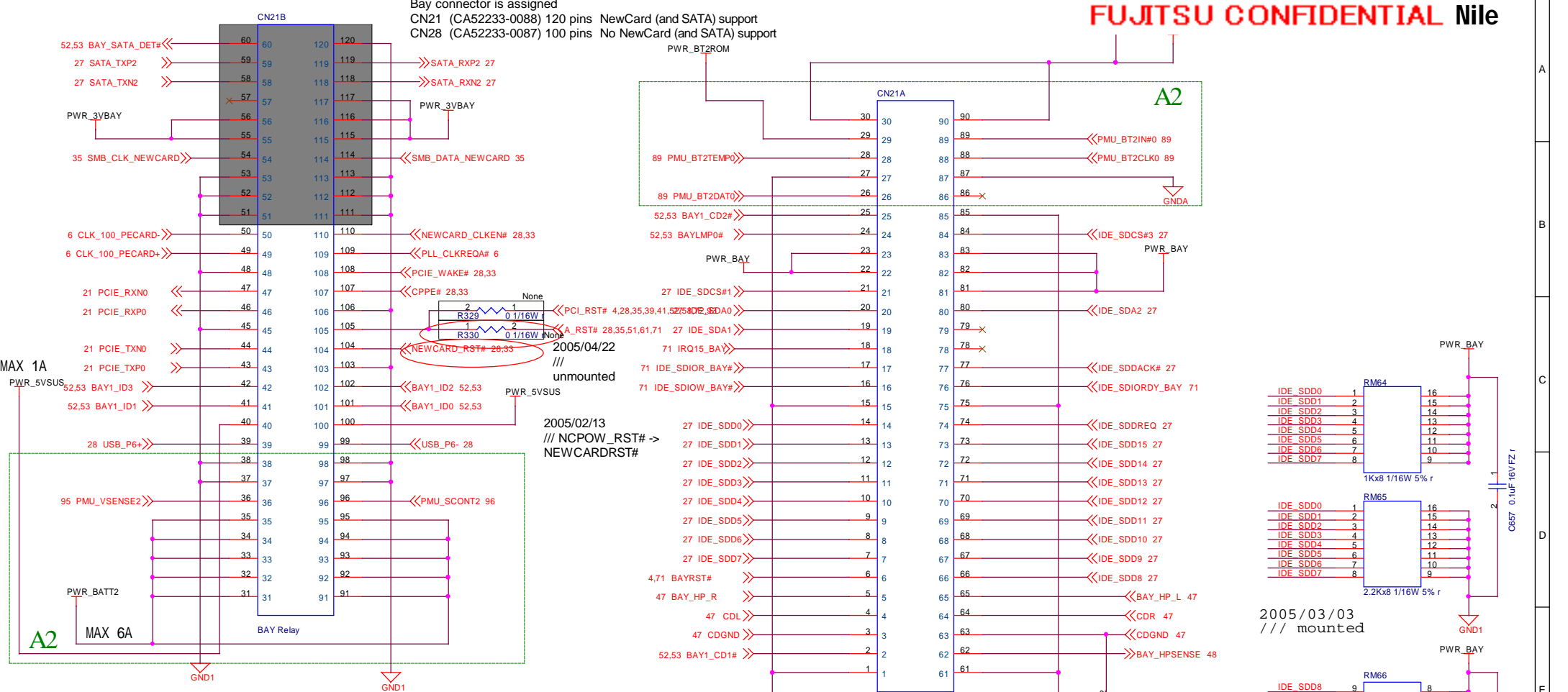


2005/02/18
/// unmount



							TITLE VB222AA	
							DRAW. No. C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet 69 / 99
Design	//	KOSHA	Check		Appr.			
							FUJITSU LTD.	

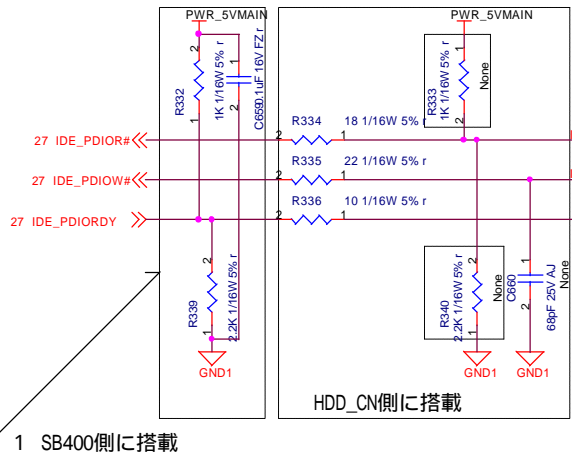
Bay connector is assigned
 CN21 (CA52233-0088) 120 pins NewCard (and SATA) support
 CN28 (CA52233-0087) 100 pins No NewCard (and SATA) support



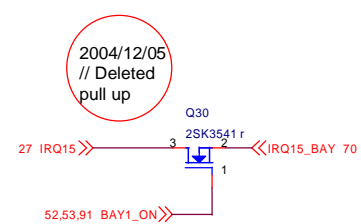
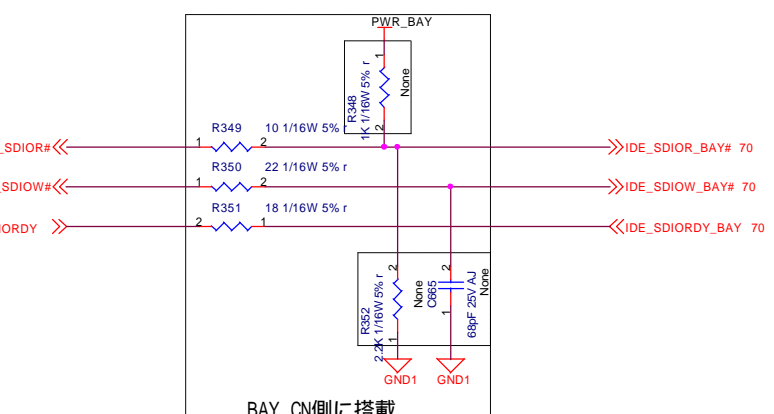
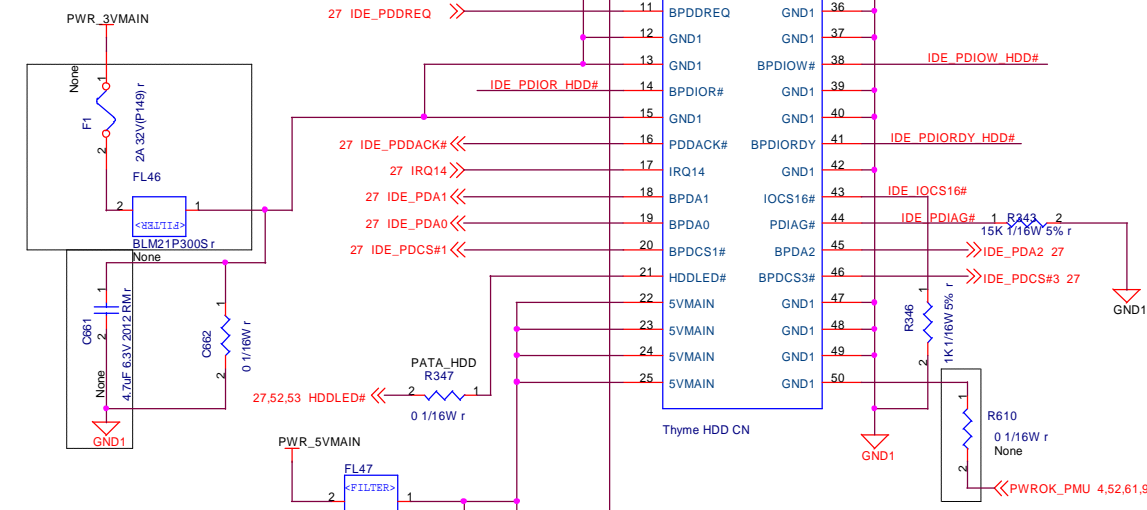
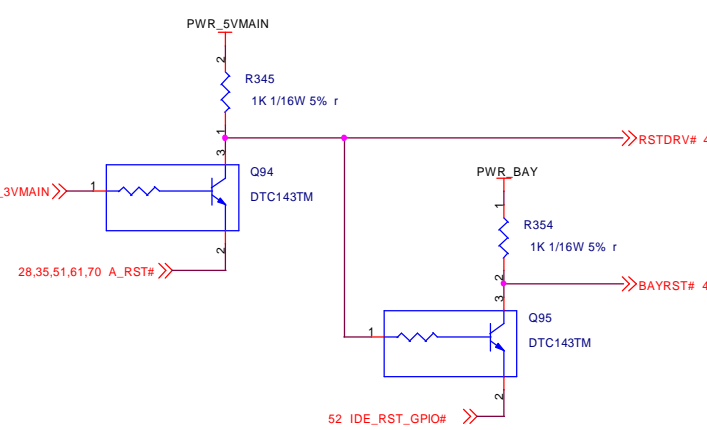
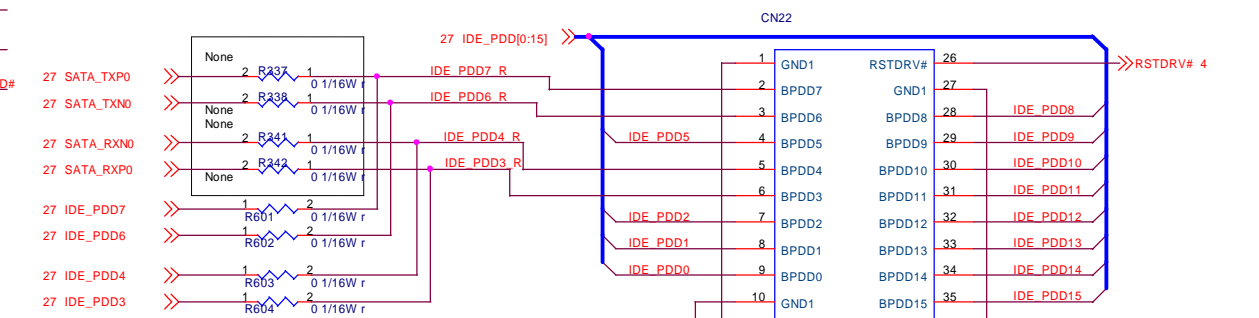
ODD/BAY-CN

					TITLE		VB222AA	
					DRAW. No.		C1CP231360-X3	
					CAST			
					Rev.		Date	
					Design		Appr.	
					Description		Sheet	
					Design		70 / 99	
					KOSHA		Appr.	
					Check		FUJITSU LTD.	

IDE_PDIOR_HDD#, IDE_PDIOW_HDD#, IDE_PDIORDY_HDD#は
それぞれGND1のガードを付けて付線すること。

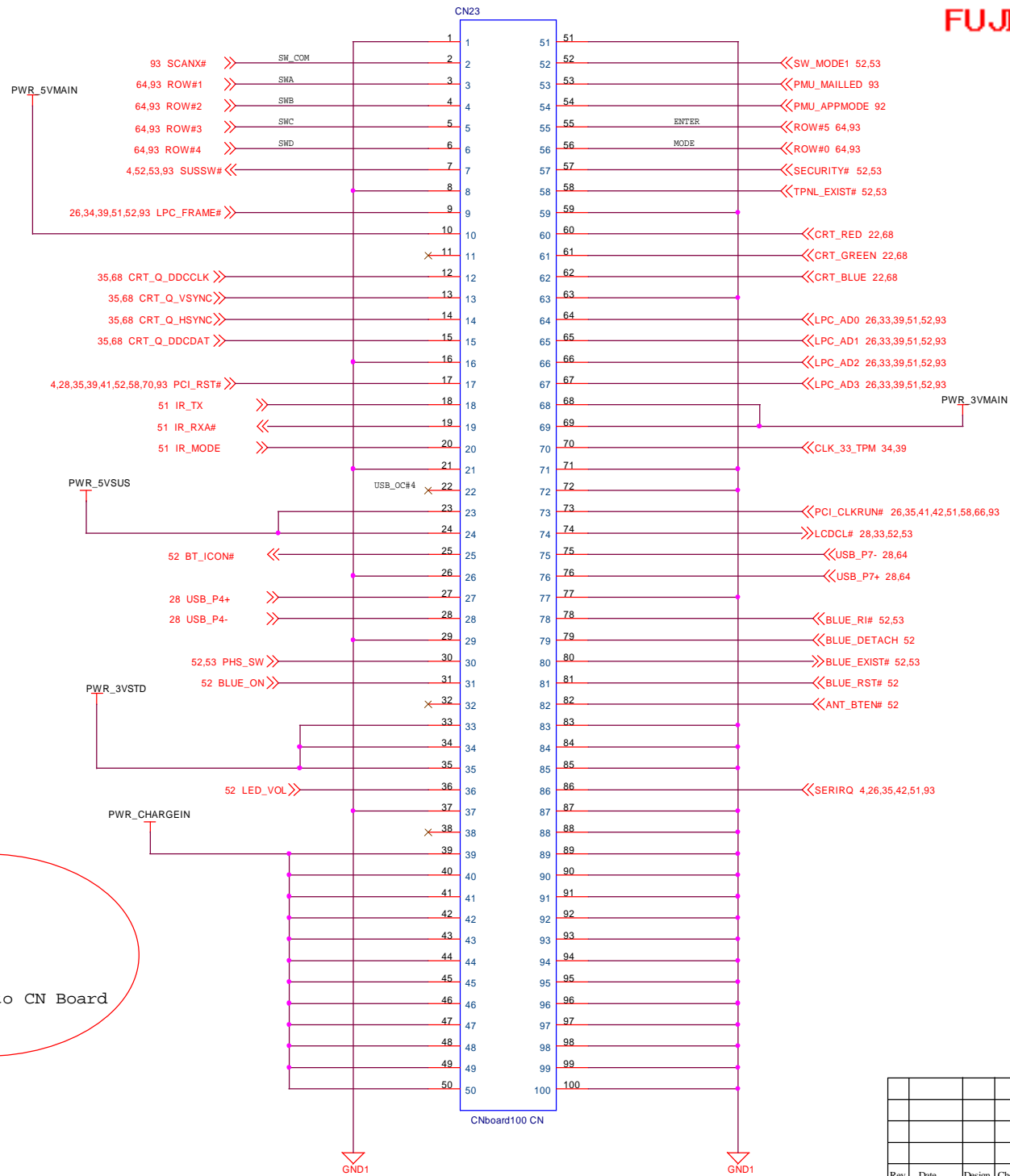


HDD_CN側に搭載



HDD-CN

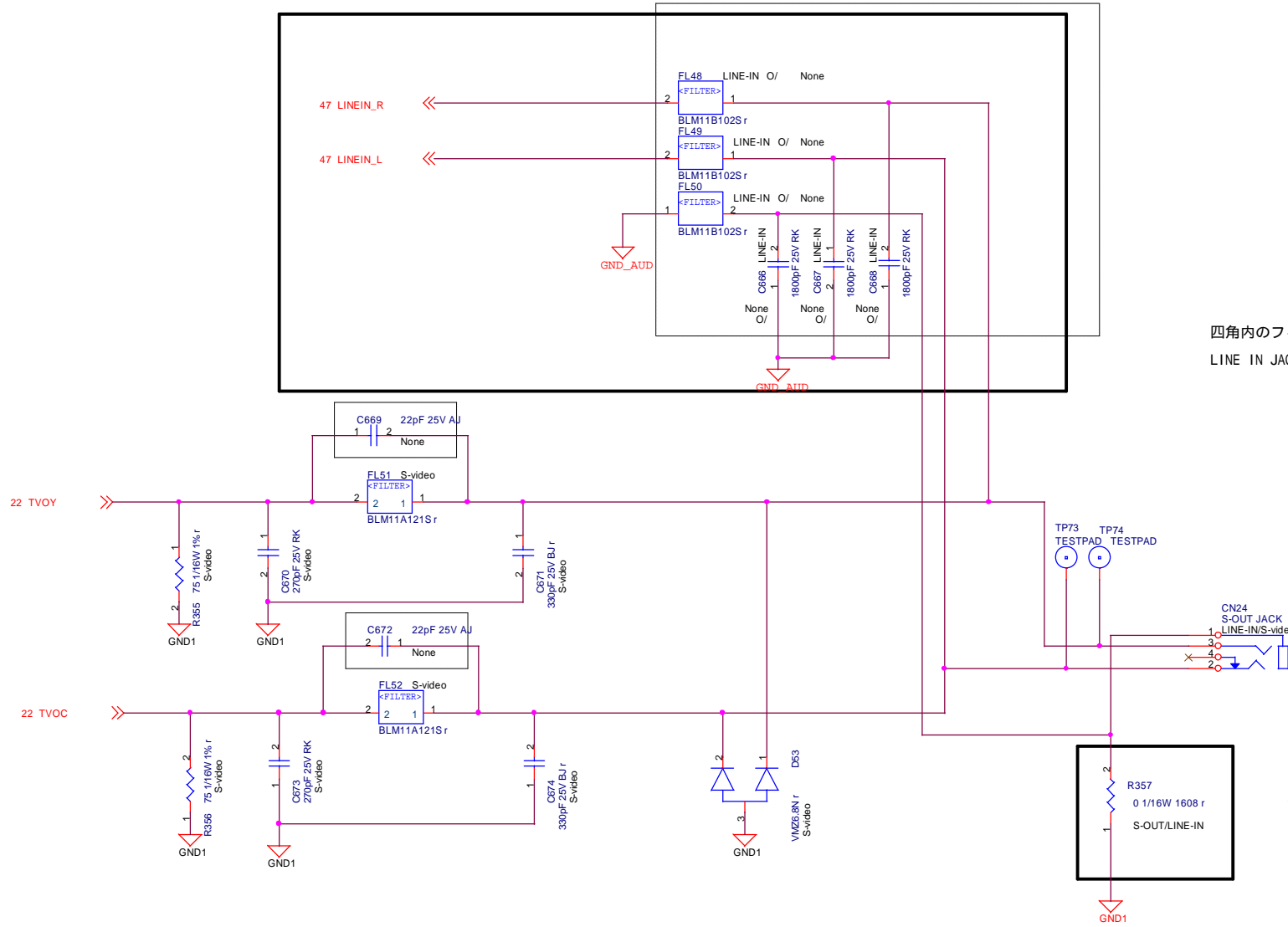
TITLE				VB222AA	
DRAW. No.				C1CP231360-X3	
Rev.				CAST	
Date					
Design				Description	
Design				Appr.	
KOSHA				Appr.	
FUJITSU LTD.				Sheet	
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2005/02/18
 /// Added
 2005/03/03
 /// mounted
 2005/05/09
 //// moved to CN Board

[CN CN-Board]

							TITLE		VB222AA	
							DRAW. No.		C1CP231360-X3	
									CAST	
							Rev.		Date	
							Design		Check	
							Appr.		Description	
							Design		Appr.	
							KOSHA		Check	
							Appr.		Appr.	
							Fujitsu Ltd.		Sheet	
									72 / 99	



四角内のフィルタ、コンデンサ、抵抗は
LINE IN JACKの近くに配置すること。

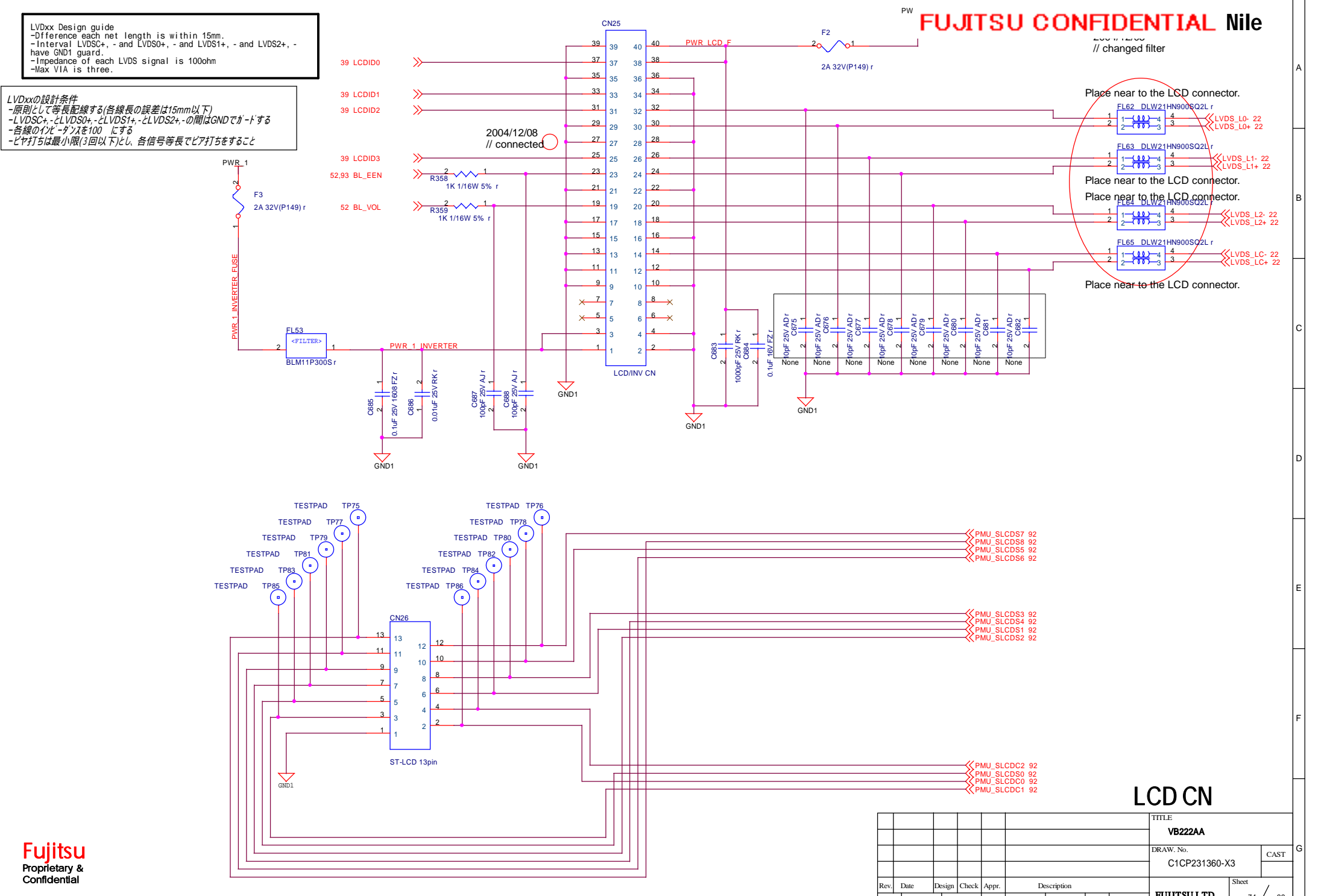
A/T: S-OUT
(CA53003-0422)
C/O: LINE-IN
(CAF33-R1H1001K)

TV Encoder

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check					
							Fujitsu LTD.	
							Sheet	
							73 / 99	

LVDxx Design guide
 -Difference each net length is within 15mm.
 -Interval LVDS0+, - and LVDS0+, - and LVDS1+, - and LVDS2+, - have GND1 guard.
 -Impedance of each LVDS signal is 100ohm
 -Max VIA is three.

LVDxxの設計条件
 -原則として等長配線する(各線長の誤差は15mm以下)
 -LVDS0+,-とLVDS0+,-とLVDS1+,-とLVDS2+,-の間はGNDでガードする
 -各線のインピーダンスを100にする
 -ビヤ打ちは最小限(3回以下)とし、各信号等長でビヤ打ちをすること



Place near to the LCD connector.
 FL62_DLW21HN900SQ2L r
 LVDS_L0- 22
 LVDS_L0+ 22
 Place near to the LCD connector.
 FL63_DLW21HN900SQ2L r
 LVDS_L1- 22
 LVDS_L1+ 22
 Place near to the LCD connector.
 FL64_DLW21HN900SQ2L r
 LVDS_L2- 22
 LVDS_L2+ 22
 Place near to the LCD connector.
 FL65_DLW21HN900SQ2L r
 LVDS_LC- 22
 LVDS_LC+ 22

PMU_SLCD57 92
 PMU_SLCD58 92
 PMU_SLCD55 92
 PMU_SLCD56 92

PMU_SLCD53 92
 PMU_SLCD54 92
 PMU_SLCD51 92
 PMU_SLCD52 92

PMU_SLCDC2 92
 PMU_SLCD50 92
 PMU_SLCDC0 92
 PMU_SLCDC1 92

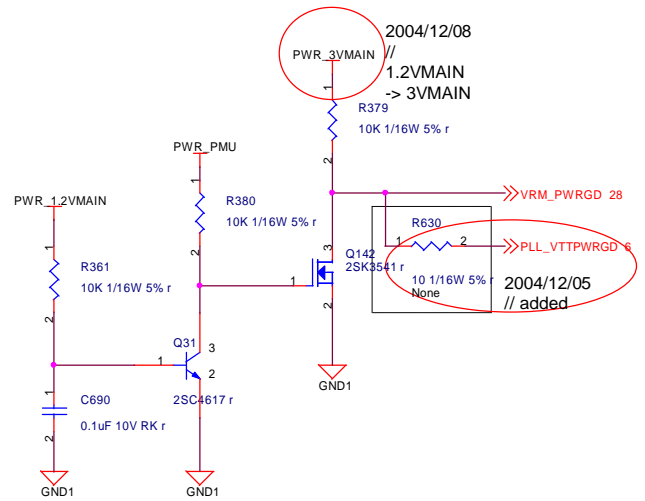
LCD CN

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
							Description	
							FUJITSU LTD.	
							Sheet	
							74 / 99	
Rev.	Date	Design	Check	Appr.				
	/ /	KOSHA	Check					

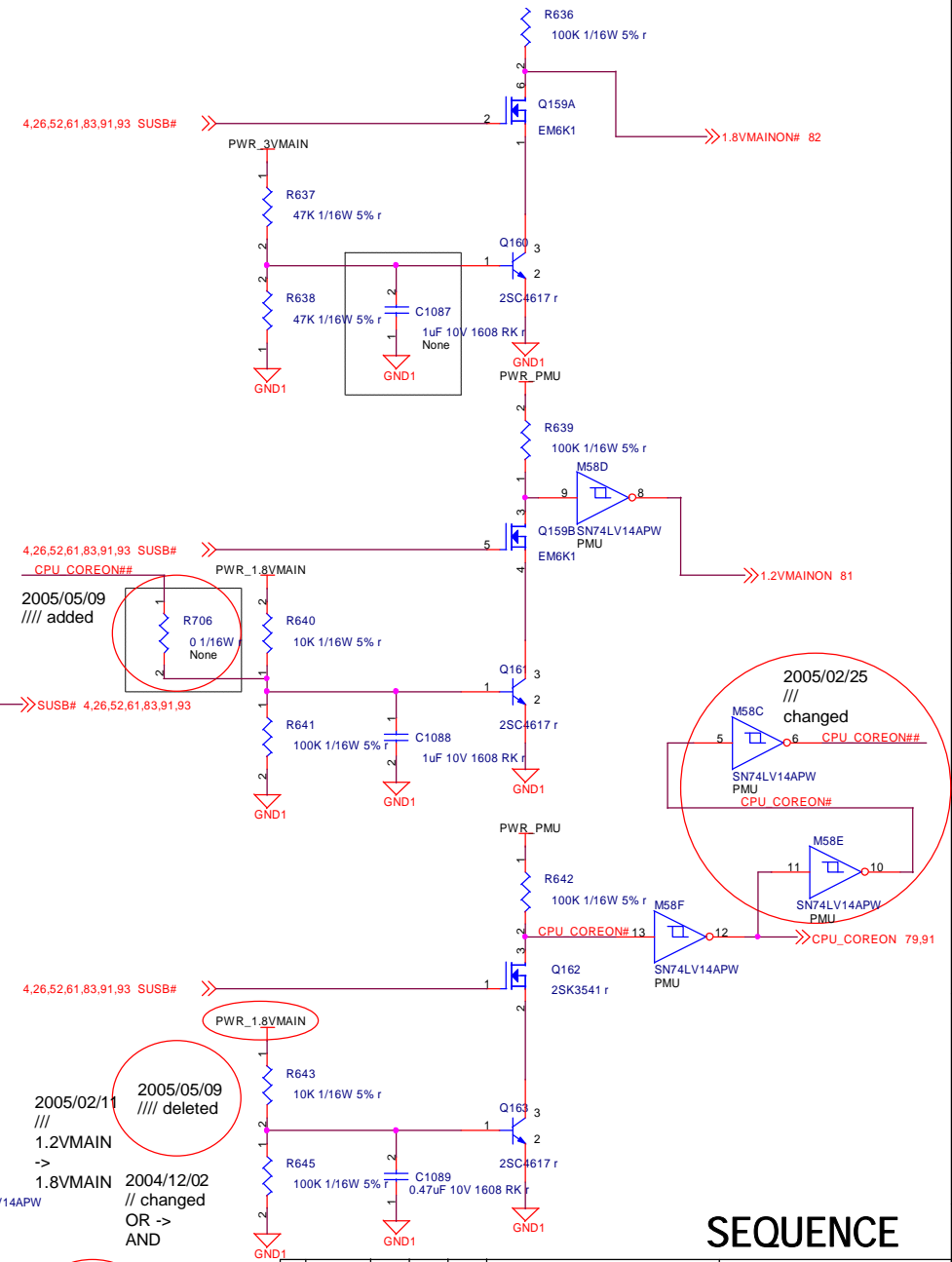
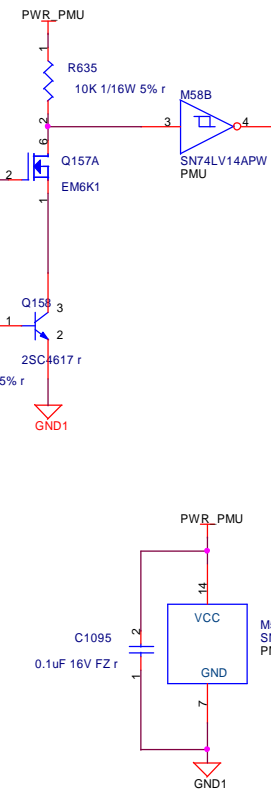
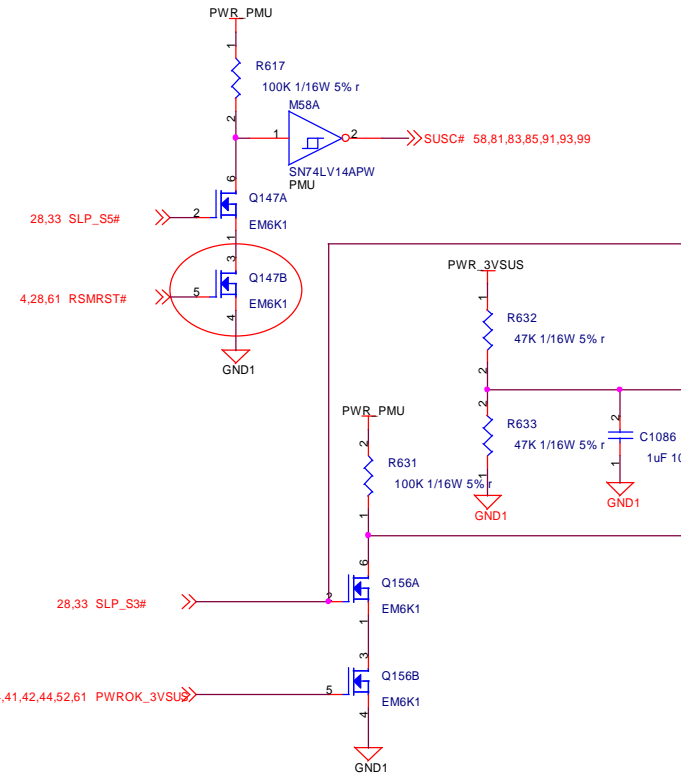
										TITLE	
										VB222AA	
										DRAW. No.	CAST
										C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description						Sheet
Design	//	KOSHA	Check				Appr.			FUJITSU LTD.	75 / 99

[Status LED CN]

										TITLE	VB222AA	
										DRAW. No.	C1CP231360-X3	CAST
Rev.	Date	Design	Check	Appr.	Description							
Design	//	KOSHA	Check				Appr.			FUJITSU LTD.	Sheet	76 / 99



SLP_S3, SLP_S5#に3VSTDでPull-Upがあるためマスク回路追加

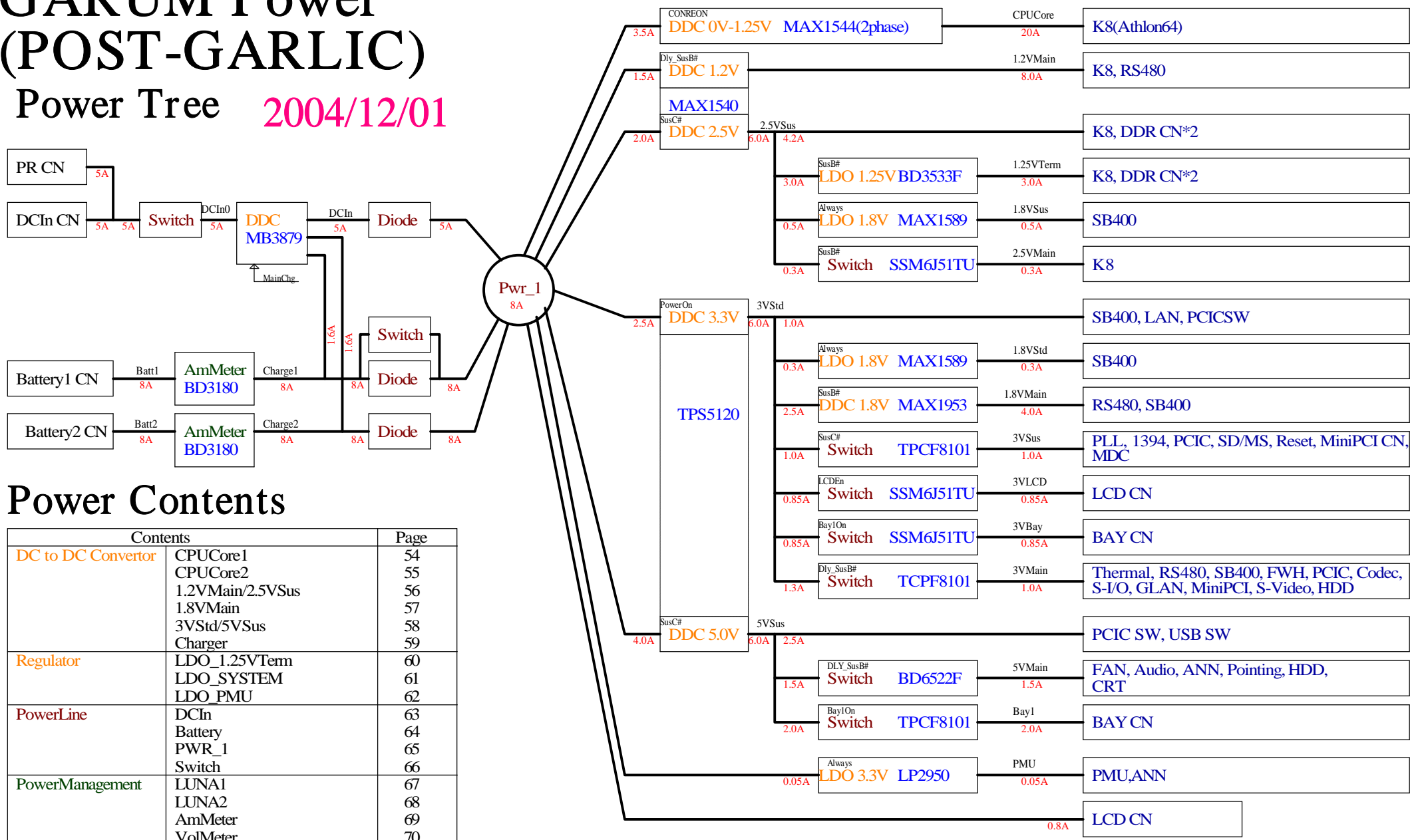


SEQUENCE

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
							Sheet	
							77 / 99	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	
Design	//	KOSHA	Check					

GARUM Power (POST-GARLIC)

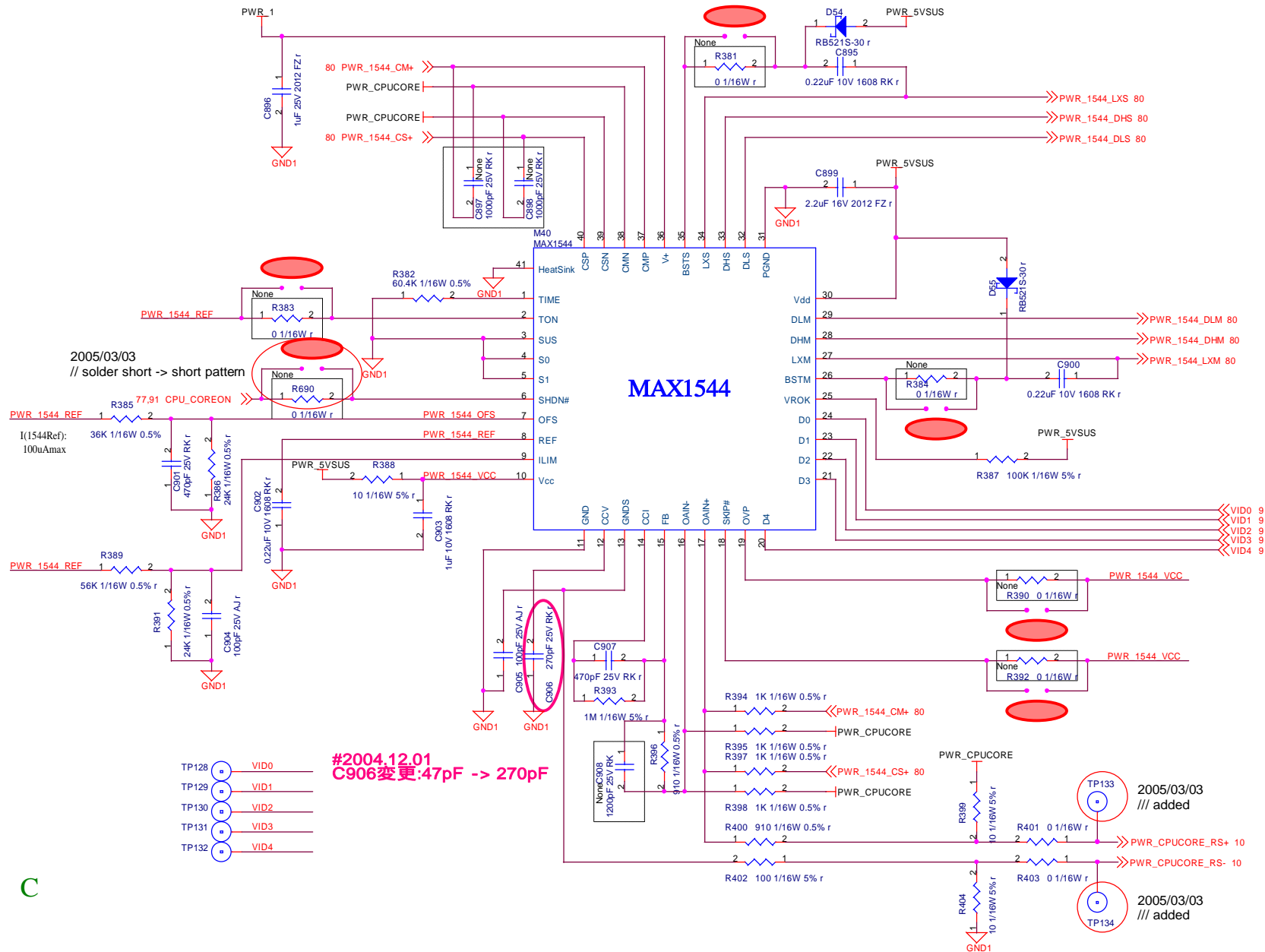
Power Tree 2004/12/01



Power Contents

Contents		Page
DC to DC Converter	CPUCore1	54
	CPUCore2	55
	1.2VMain/2.5VSus	56
	1.8VMain	57
	3VStd/5VSus	58
	Charger	59
	Regulator	LDO_1.25VTerm
LDO_SYSTEM		61
LDO_PMU		62
PowerLine		DCIn
	Battery	64
	PWR_1	65
	Switch	66
	PowerManagement	LUNA1
LUNA2		68
AmMeter		69
VolMeter		70
Scont		71
Etc		72
Power Sequence		73

							TITLE		
							VB222AA		
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Design	/ /	KOSHA	Check			Appr.			



2005/03/03
// solder short -> short pattern

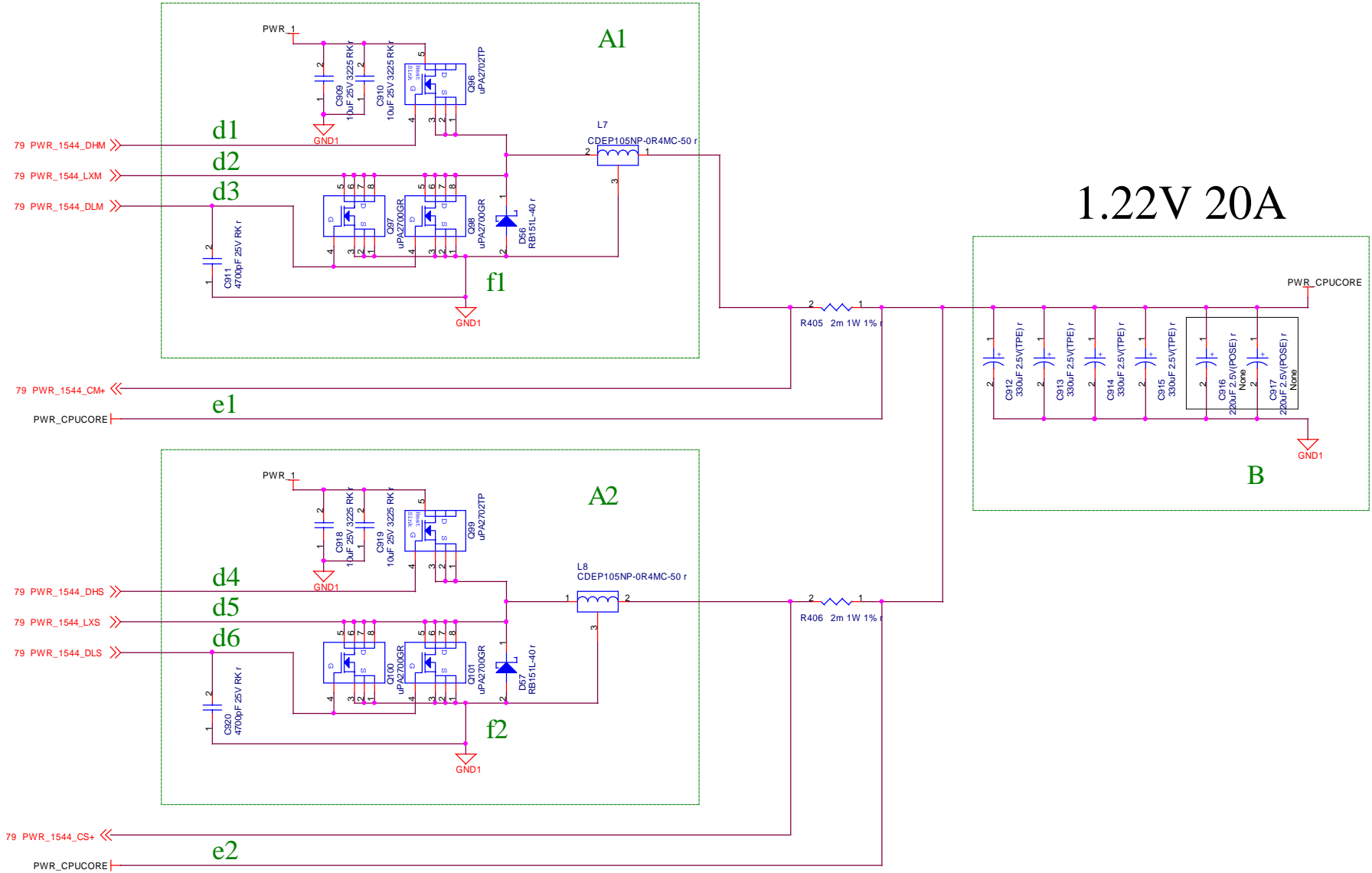
#2004.12.01
C906变更:47pF -> 270pF

- TP128 VID0
- TP129 VID1
- TP130 VID2
- TP131 VID3
- TP132 VID4

2005/03/03
/// added

2005/03/03
/// added

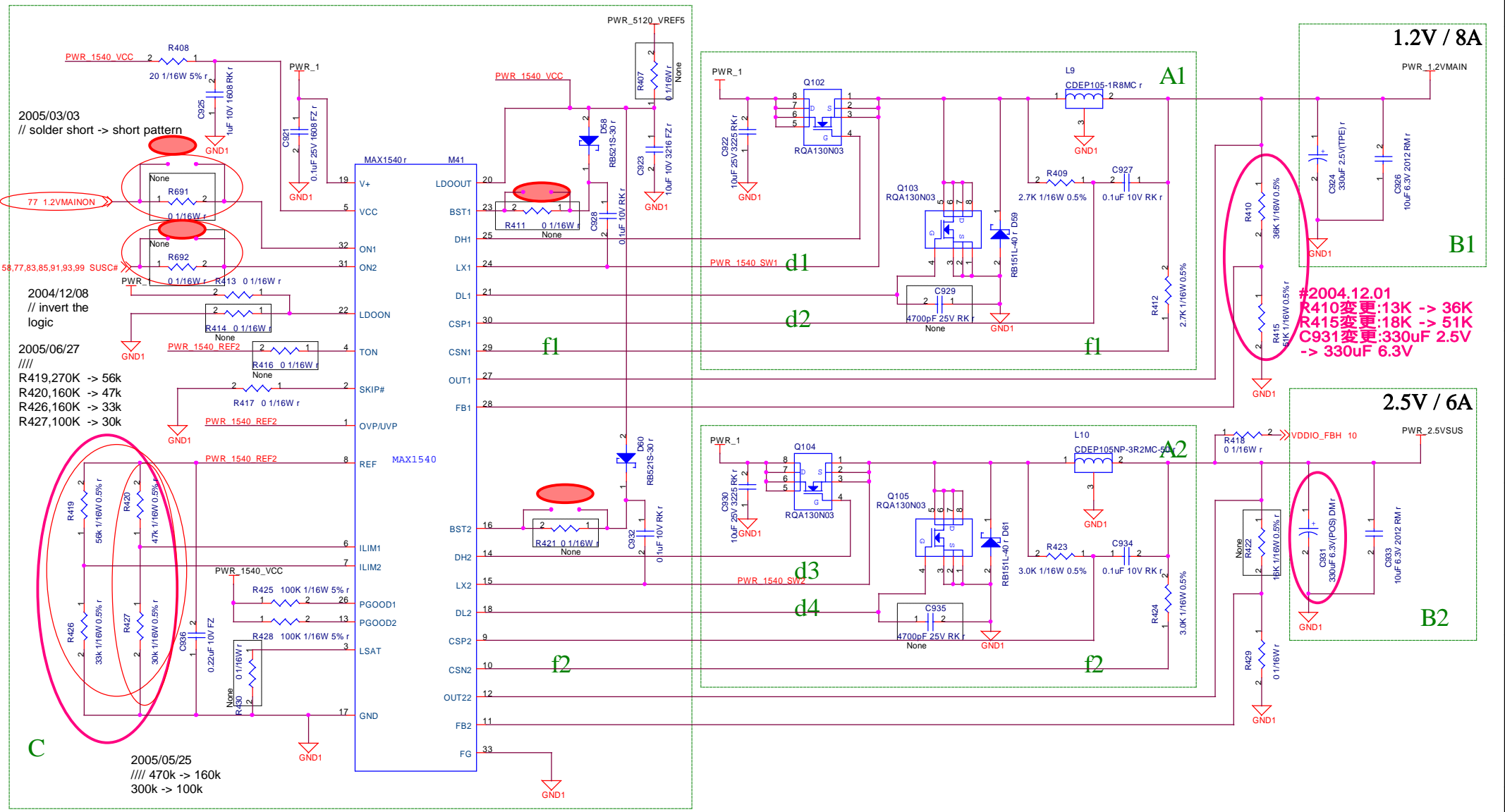
							TITLE	
							VB222AA	
							DRAW. No.	CAST
							C1CP231360-X3	
Rev.	Date	Design	Check	Appr.	Description			Fujitsu Ltd.
Design	/ /	KOSHA	Check		Appr.		Sheet 79 / 99	



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Confidential

Power/ DDC/ CPUCore2

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.			
							FUJITSU LTD.	
							80 / 99	



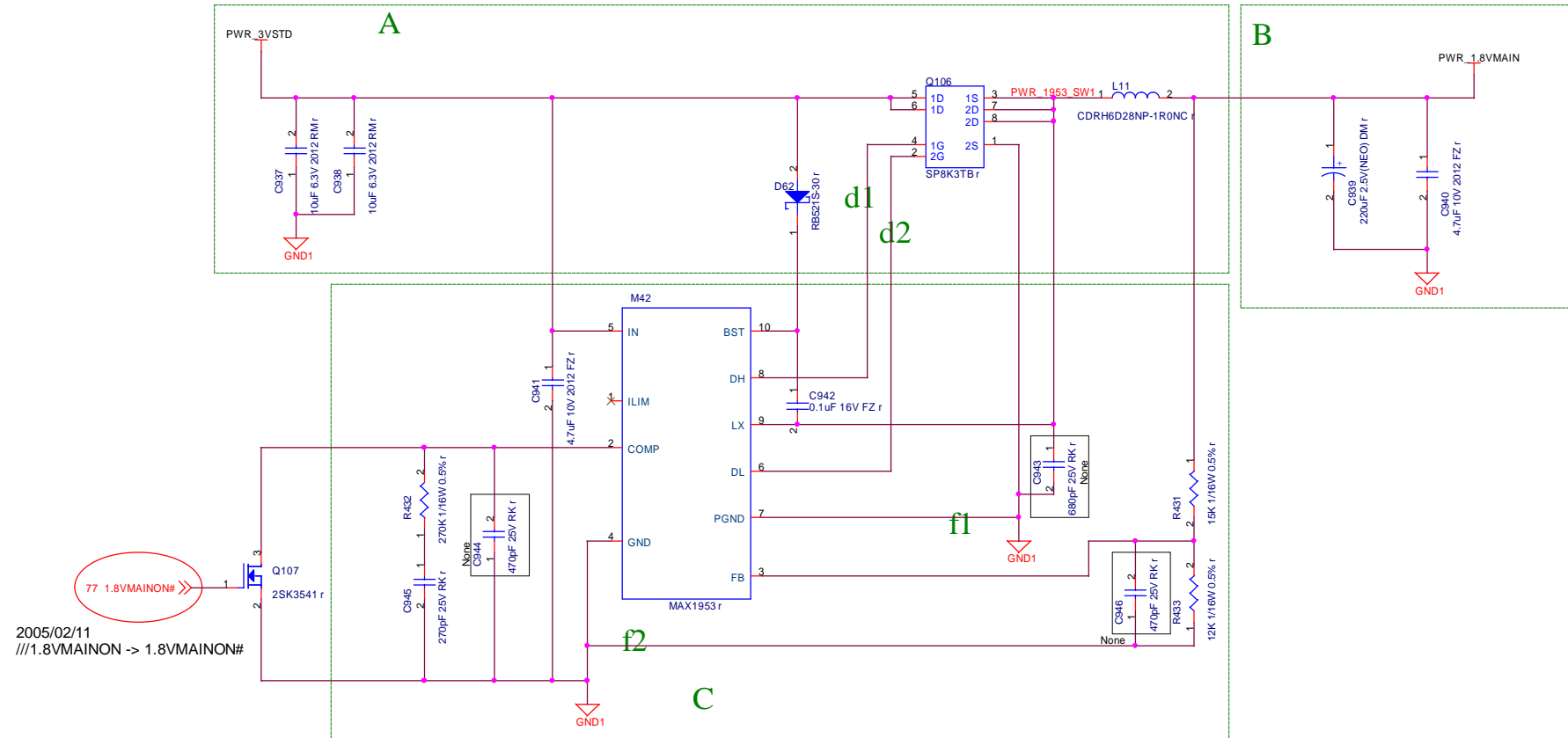
Fujitsu
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#2004.12.01
R419変更:390K -> 270K
R420変更:390K -> 470K
R426変更:270K -> 160K
R427変更:200K -> 300K

Power/ DDC/ 1.2VMain, 2.5VSus

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check					81 / 99
							FUJITSU LTD.	

1.8V / 3.5A



Fujitsu
Proprietary &
Confidential

Power/DDC/1.5VMAIN

							TITLE	
							VB222AA	
							DRAW. No.	
							C1CP231360-X3	
							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check					
							FUJITSU LTD.	
							Sheet	
							82 / 99	

2005/03/03
// solder short -> short pattern

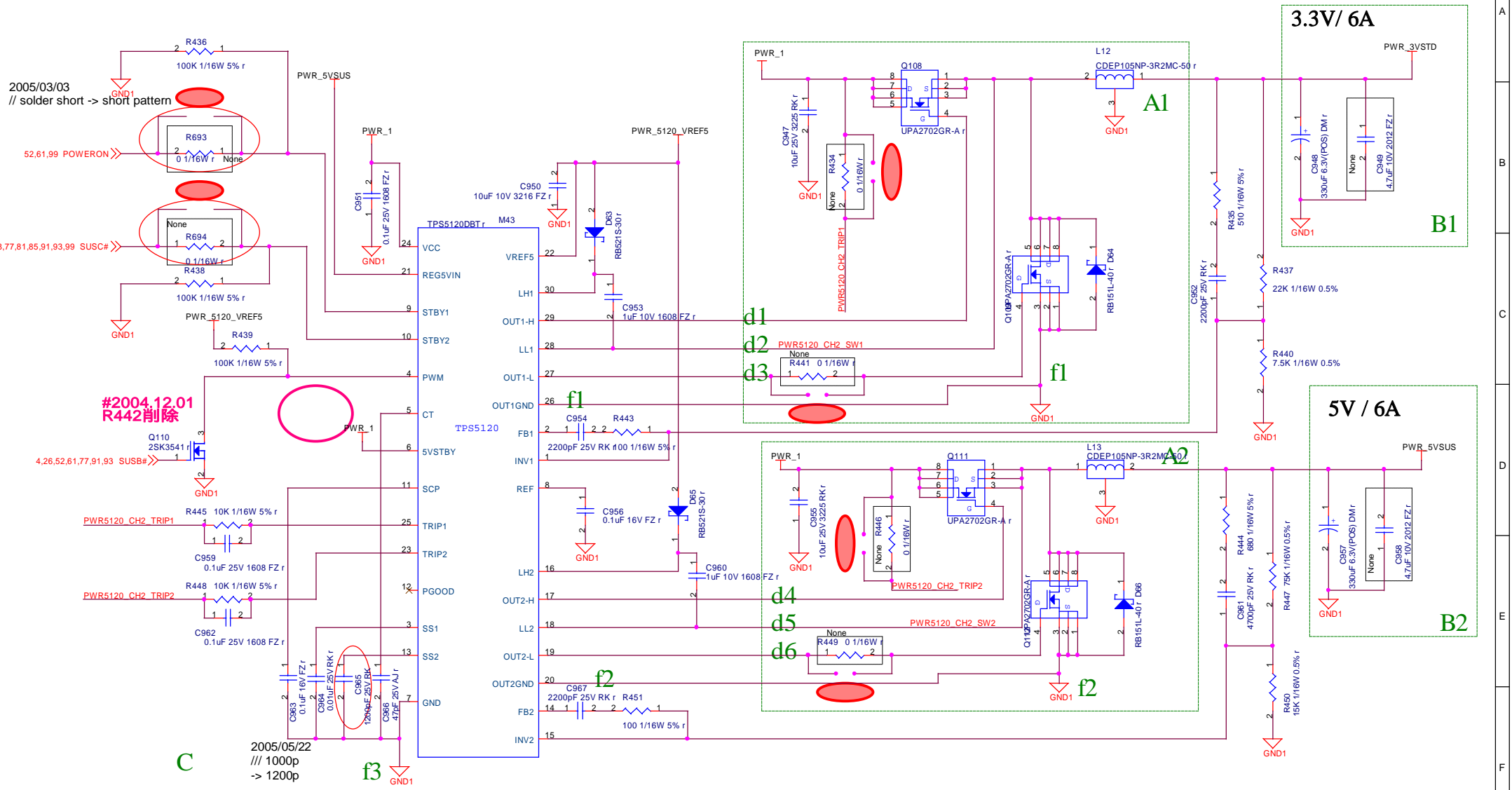
52,61,99 POWERON

#2004.12.01
R442削除

4,26,52,61,77,91,93 SUSB#

2005/05/22
/// 1000p
-> 1200p

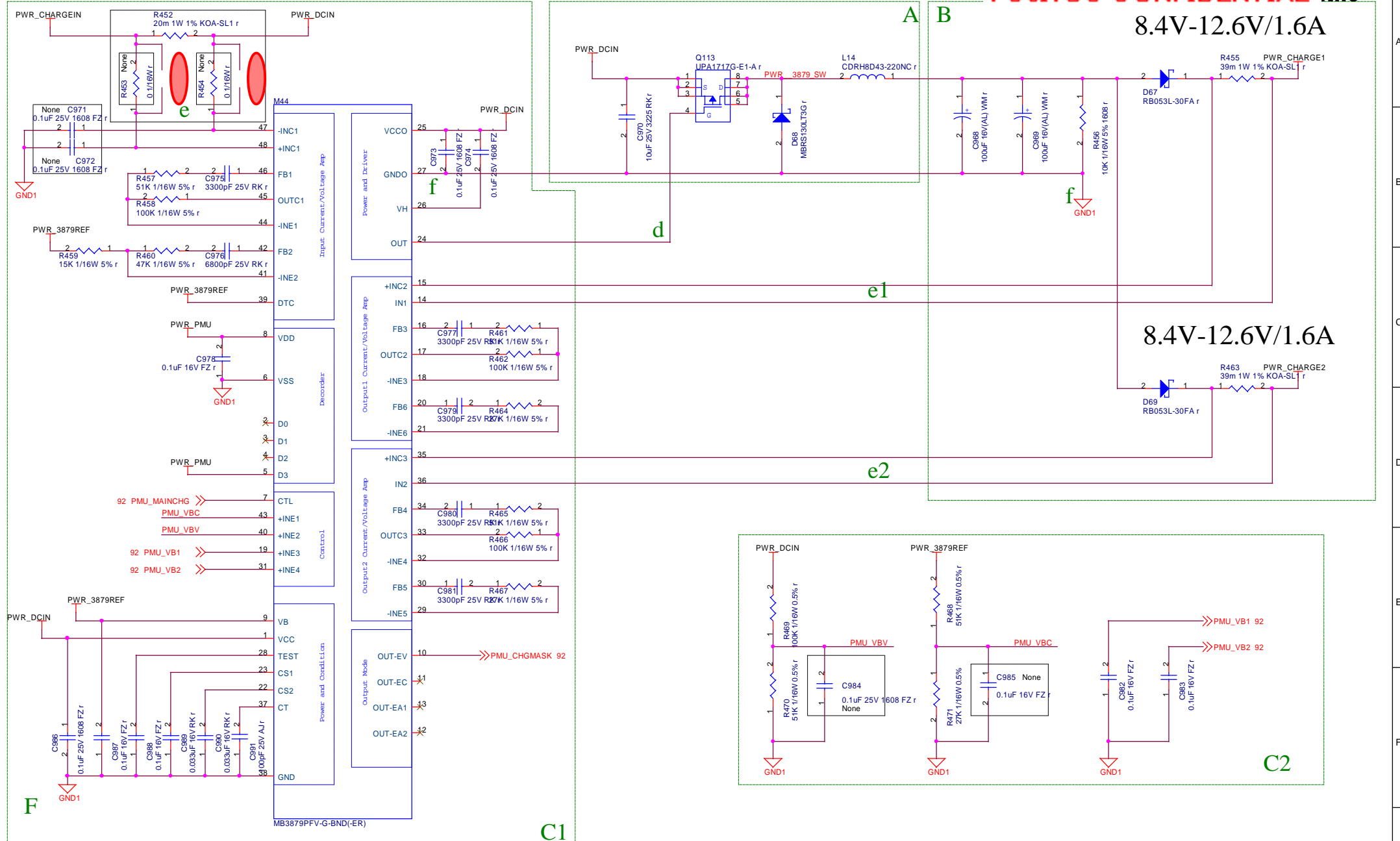
Fujitsu
Proprietary &
Confidential
Power/ DDC/ 3VSTD,5VSUS



							TITLE	
							VB222AA	
							DRAW. No.	
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							CAST	
Rev.	Date	Design	Check	Appr.	Description		Sheet	
Design	//	KOSHA	Check				FUJITSU LTD.	
							83 / 99	

8.4V-12.6V/1.6A

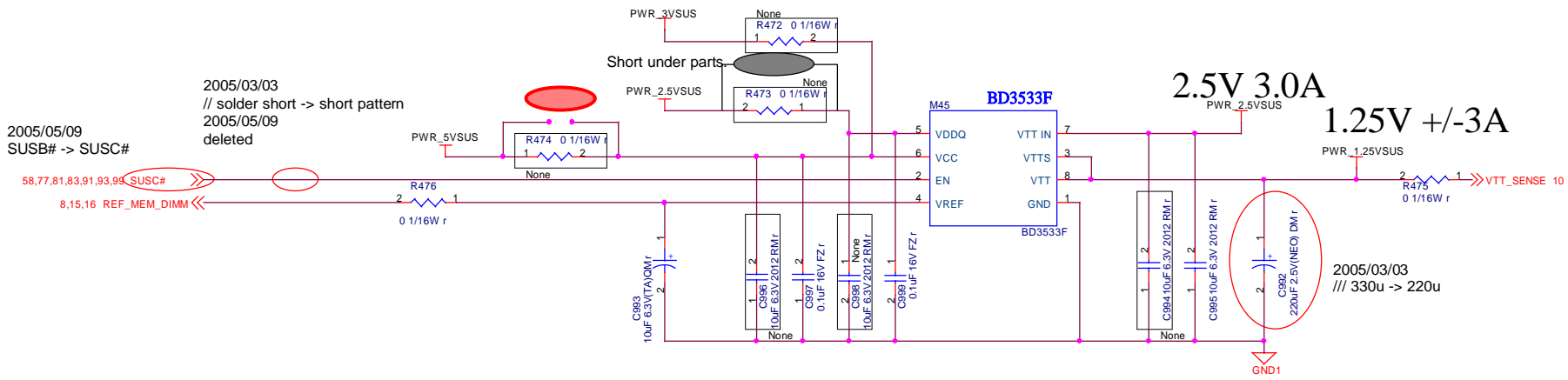
8.4V-12.6V/1.6A



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Power/DCD/Charger

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							CAST	
Rev.	Date	Design	Check	Appr.	Description			
Design	/ /	KOSHA	Check		Appr.			
							FUJITSU LTD.	
							Sheet	
							84 / 99	



2005/03/03
 // solder short -> short pattern
 2005/05/09
 deleted

2005/05/09
 SUSB# -> SUSC#
 58,77,81,83,91,93,95 >>> SUSC#
 8,15,16 REF_MEM_DIMM <<<

2.5V 3.0A
 PWR_2.5VSUS
 1.25V +/-3A
 PWR_1.25VSUS

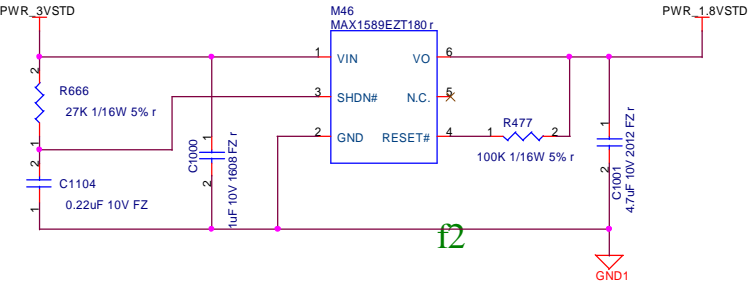
2005/03/03
 /// 330u -> 220u

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Power/ DDC/ 1.25VSus

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Rev.	Date	Design	Check	Appr.	Description			
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							85 / 99	

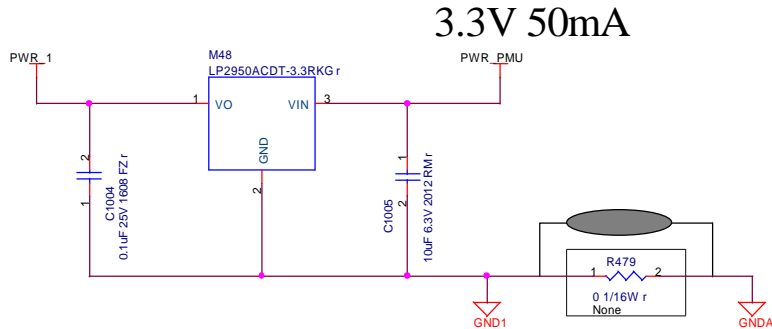
1.8V 0.3A



2005/03/03
 ///
 Deleted

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Power/ LDO/ System

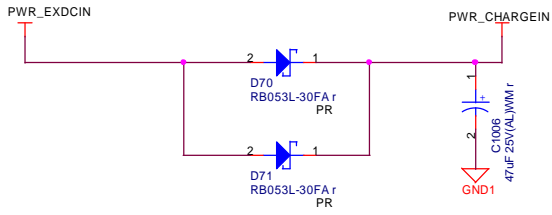
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					86 / 99	



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Power/ LDO/ PMU

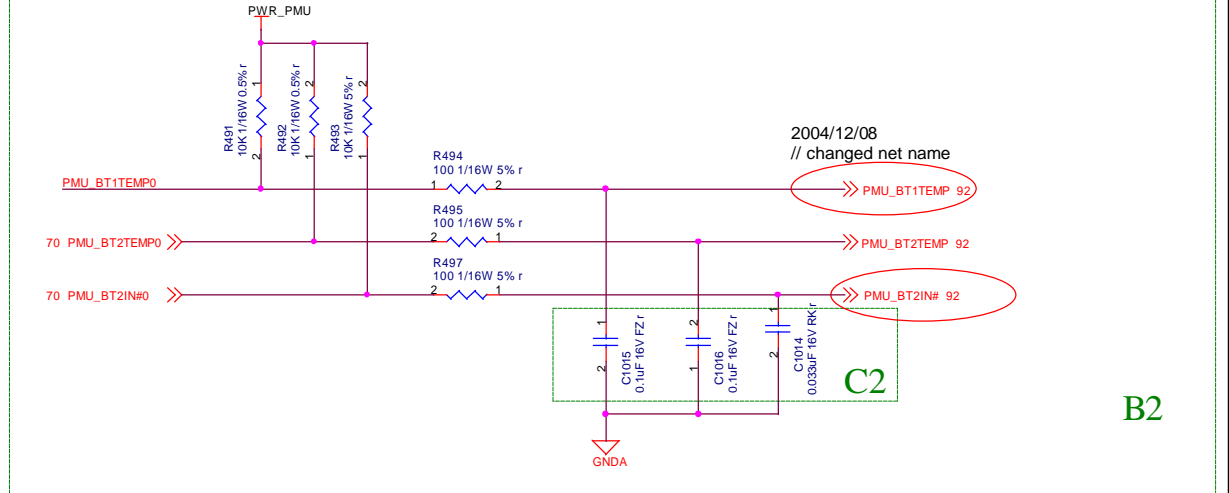
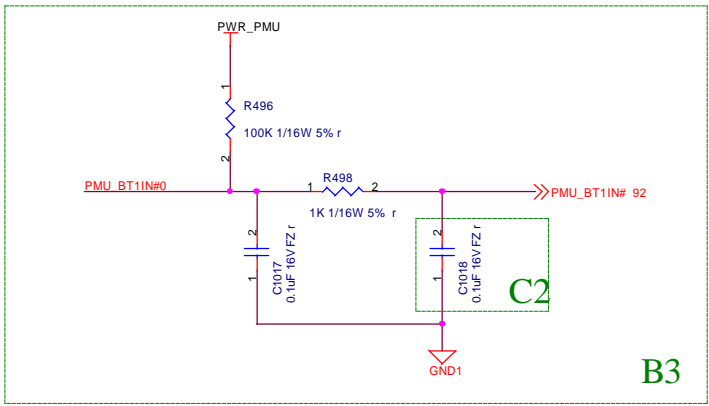
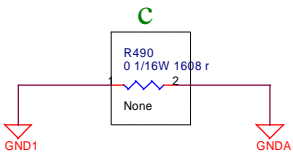
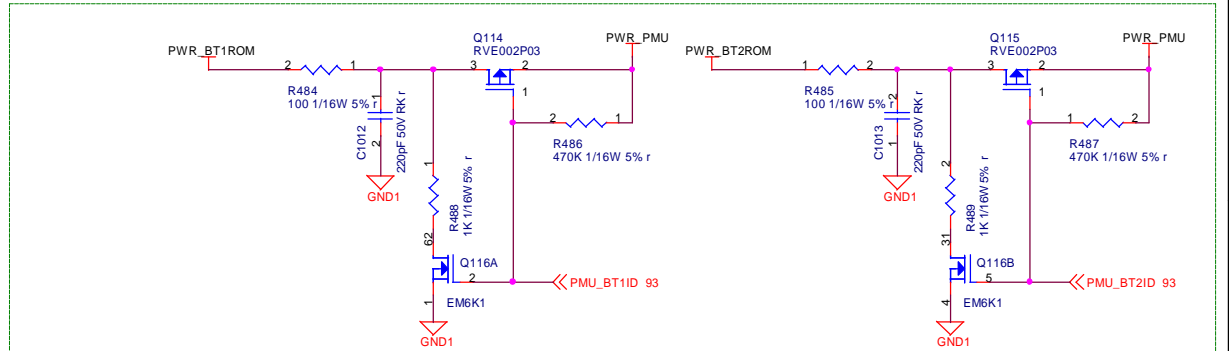
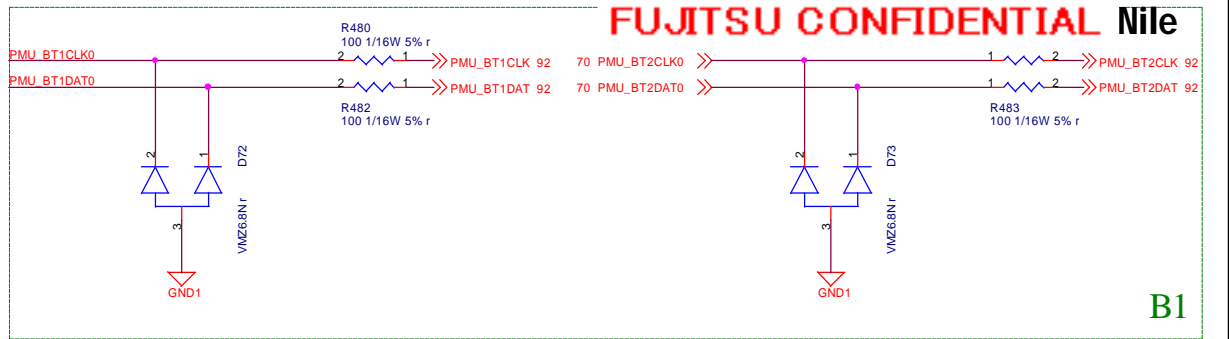
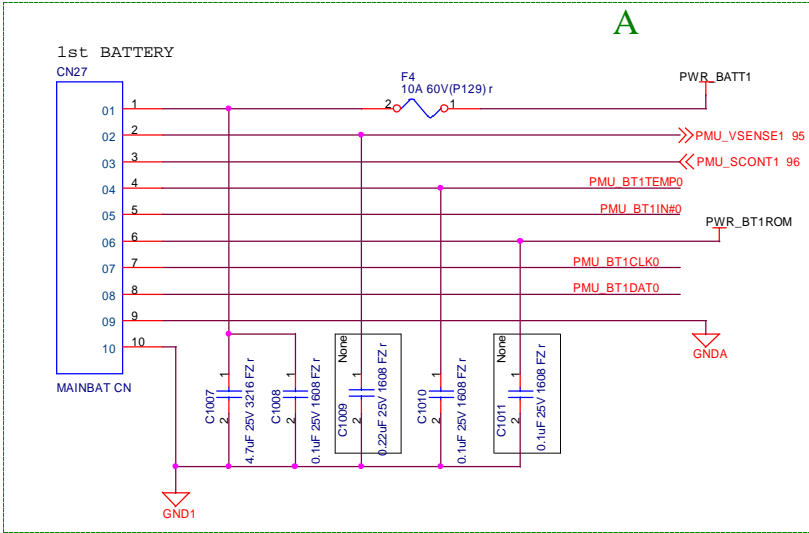
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Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check			Appr.	FUJITSU LTD.	
							Sheet	87 / 99



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Power/ Node/ DCIn

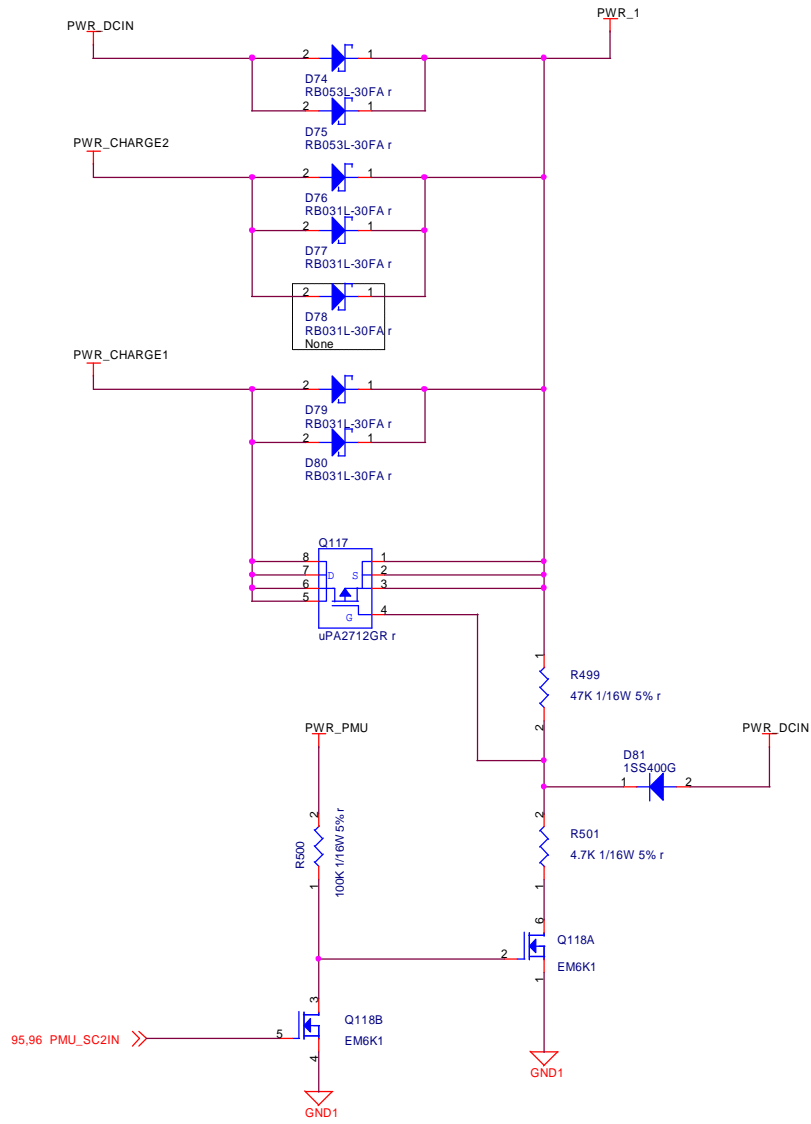
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Design	//	KOSHA	Check			Appr.
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					Sheet	
					88 / 99	



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Power/Node/Battery

							TITLE	
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							DRAW. No.	
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							89 / 99	

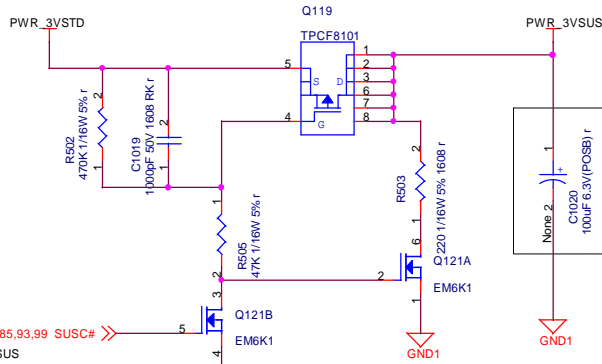


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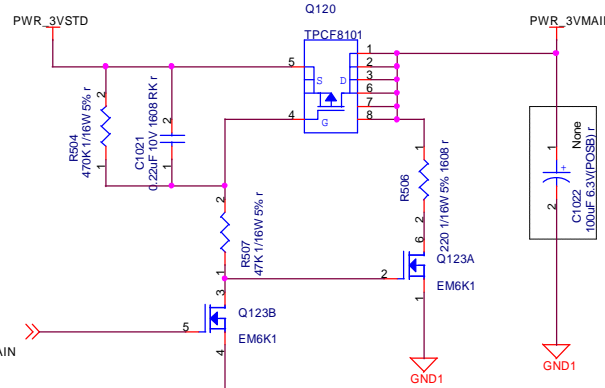
Power/Node/PWR_1

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Rev.	Date	Design	Check	Appr.	Description			
Design	//	KOSHA	Check			Appr.		
FUJITSU LTD.							Sheet 90 / 99	

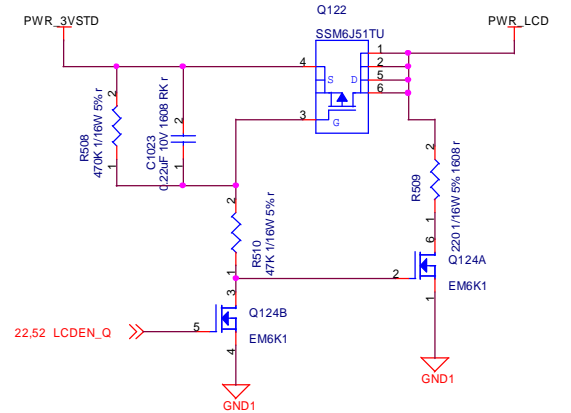
3.3V 2.0A



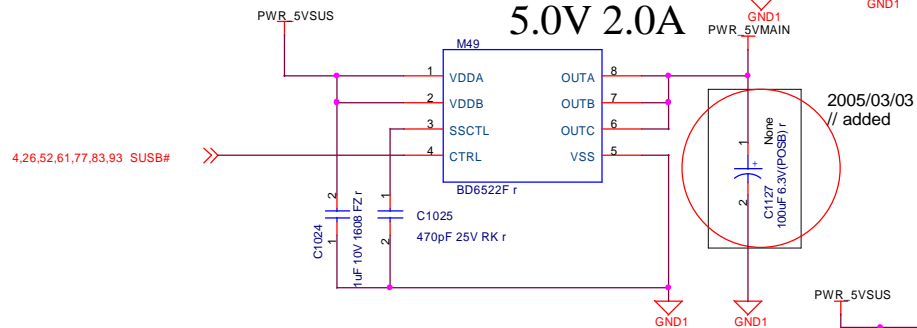
3.3V 2.0A



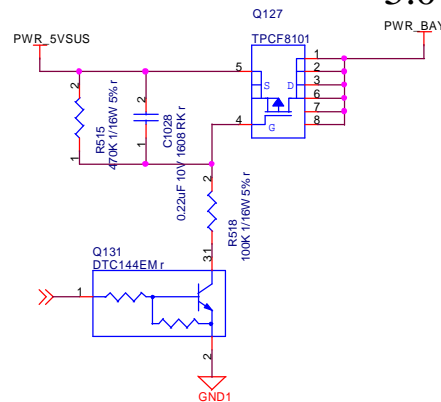
3.3V 1.0A



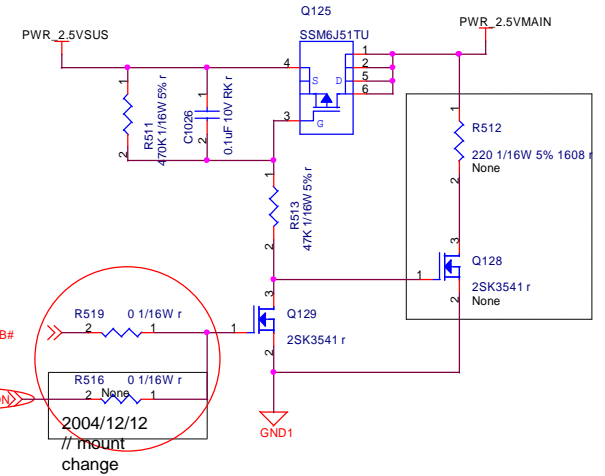
5.0V 2.0A



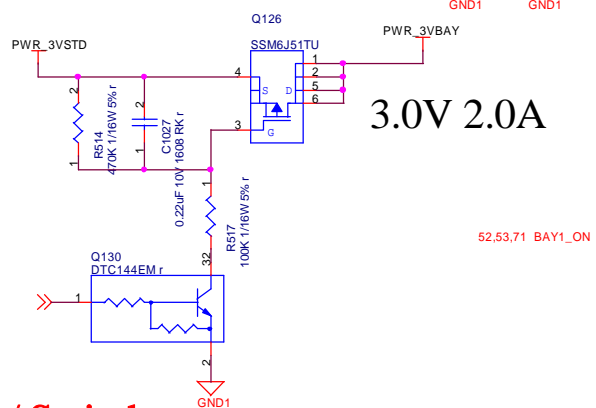
5.0V 2.0A



2.5V 0.3A



3.0V 2.0A



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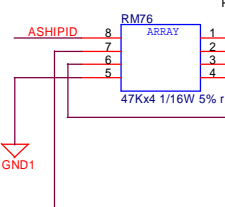
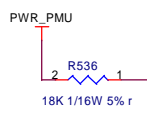
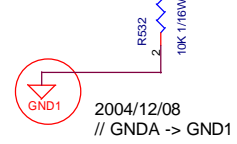
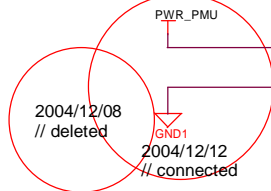
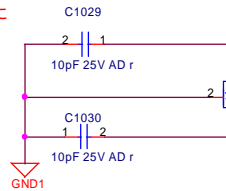
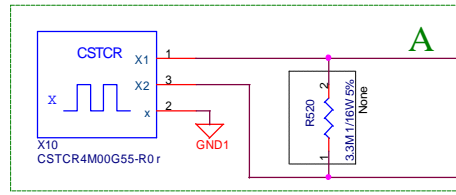
Power/Node/Switch

77,79 CPU_COREON
2005/05/09
//// 1.2VMAINON ->
CPU_COREON

R519 0 1/16W r
R516 0 1/16W r
2004/12/12
// mount
change

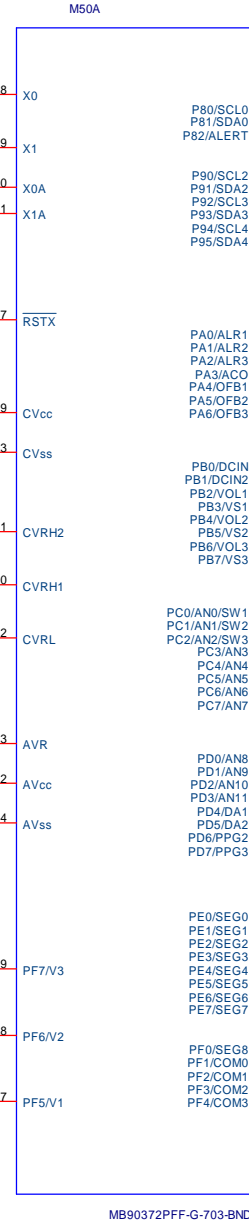
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Rev.	Date	Design	Check	Appr.	Description			Sheet
Design	//	KOSHA	Check		Appr.			91 / 99
							FUJITSU LTD.	

本クロックはノイズに弱い
ため上下層に高速な信号が
走らないように配線
すること

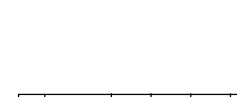
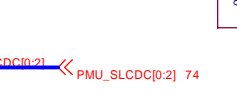
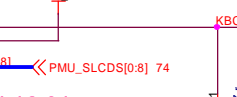
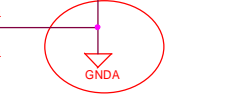
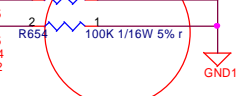
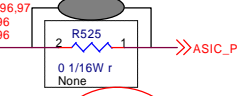
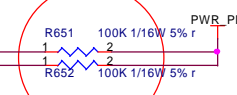
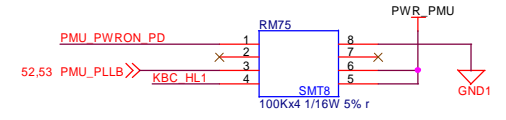
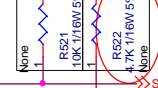


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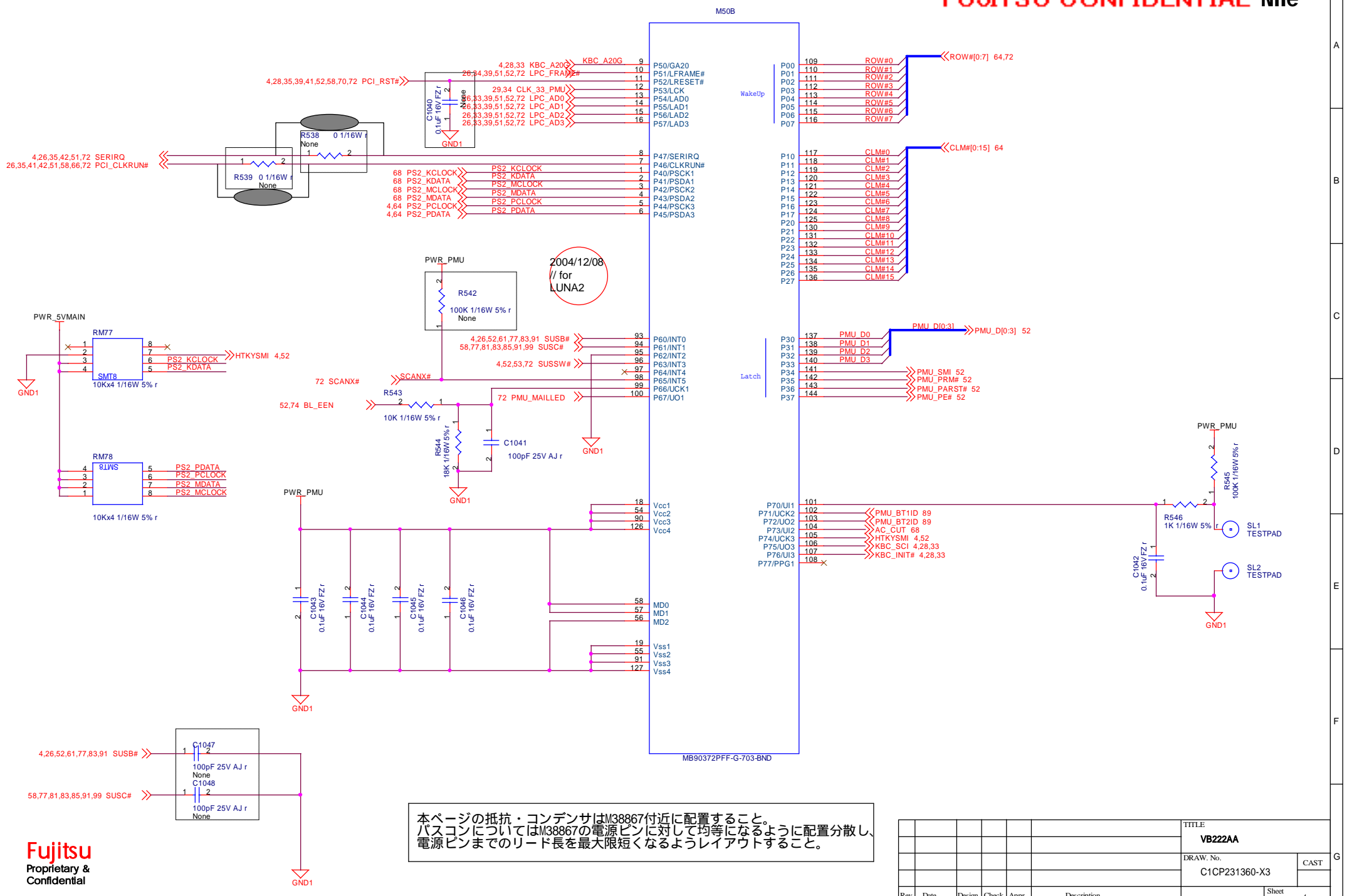
Power/ PMU/ LUNA1



PWR_PMU 2004/12/08
// populated in SM bus selector
page



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								C1CP231360-X3	
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Rev.	Date	Design	Check	Appr.	Description			Sheet	
Design	//	KOSHA	Check		Appr.			FUJITSU LTD.	
								92 / 99	

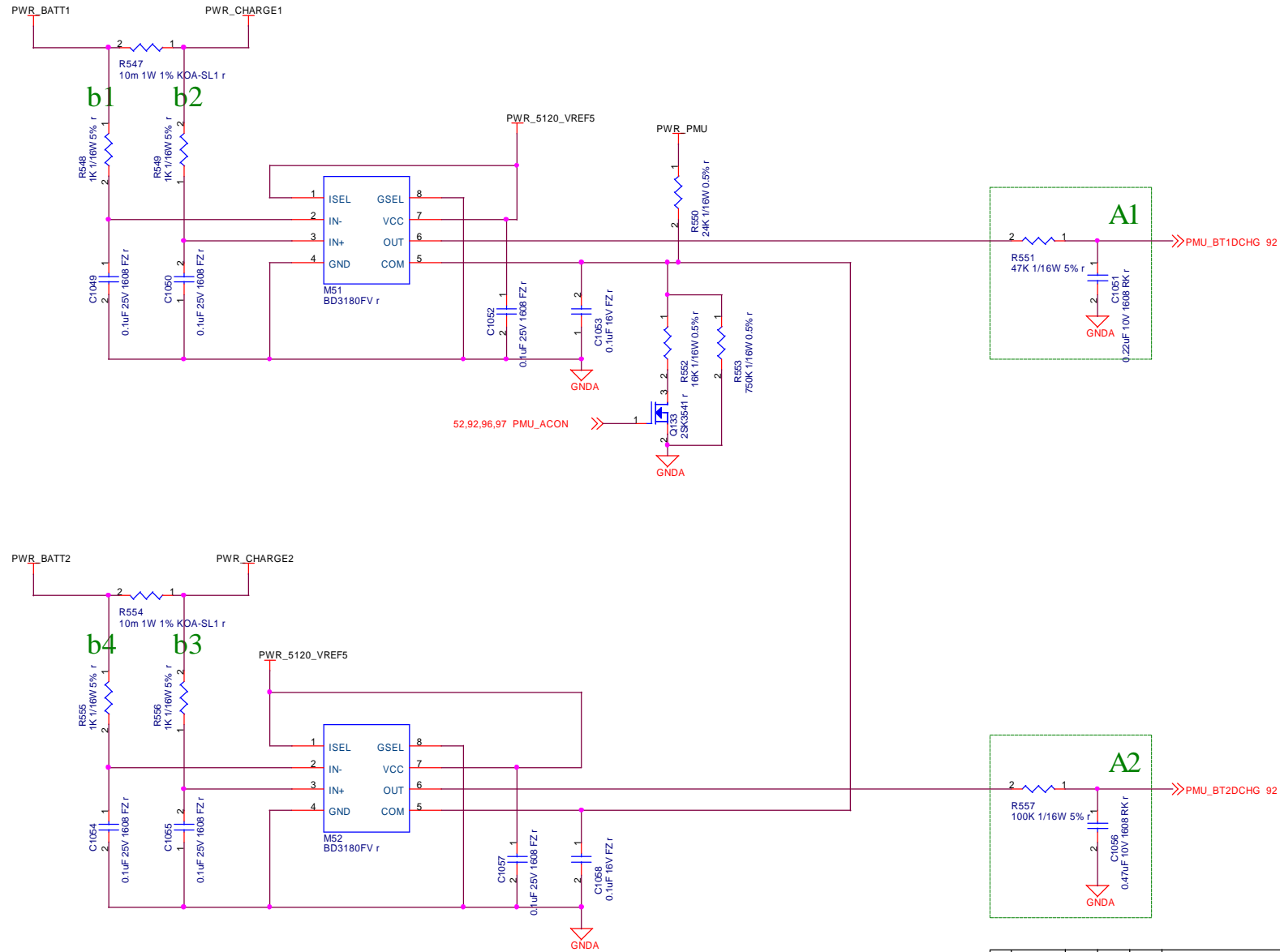


本ページの抵抗・コンデンサはM38867付近に配置すること。
 パソコンについてはM38867の電源ピンに対して均等になるように配置分散し、
 電源ピンまでのリード長を最大限短くなるようレイアウトすること。

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Power/PMU/LUNA2

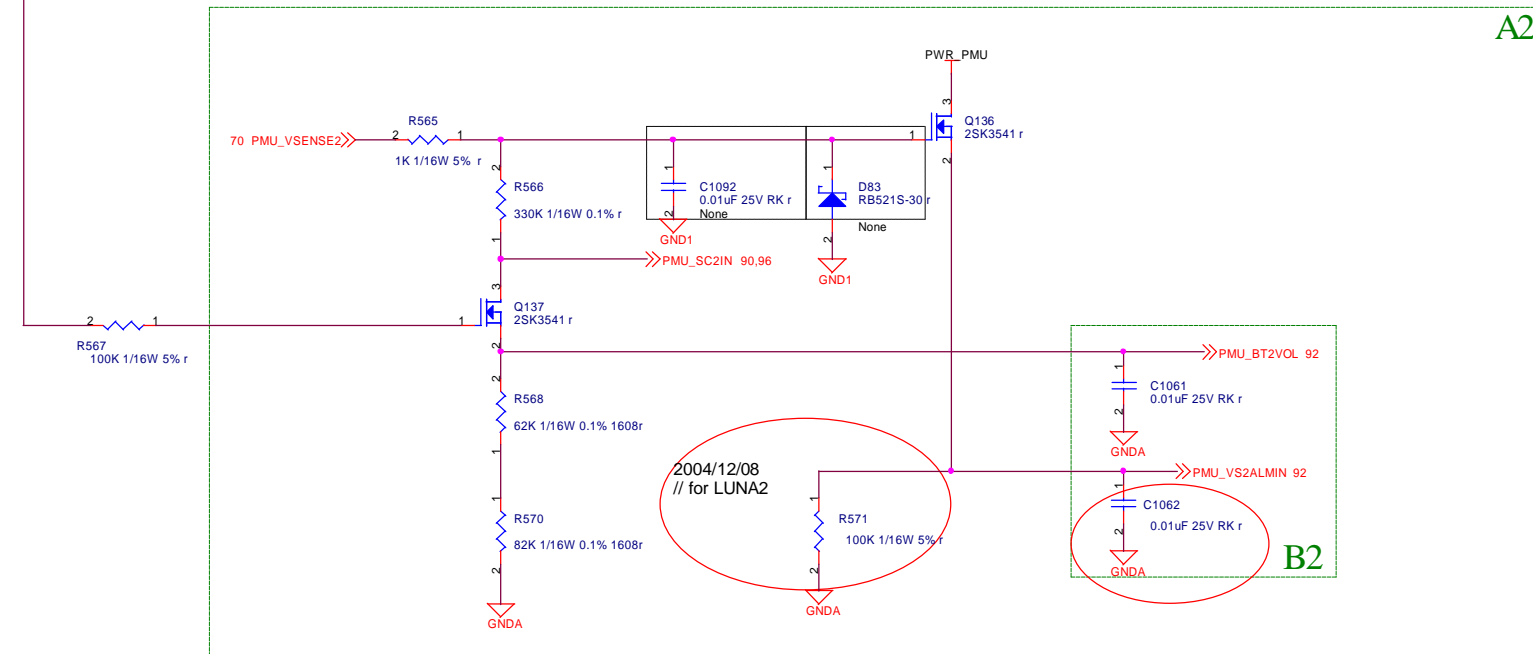
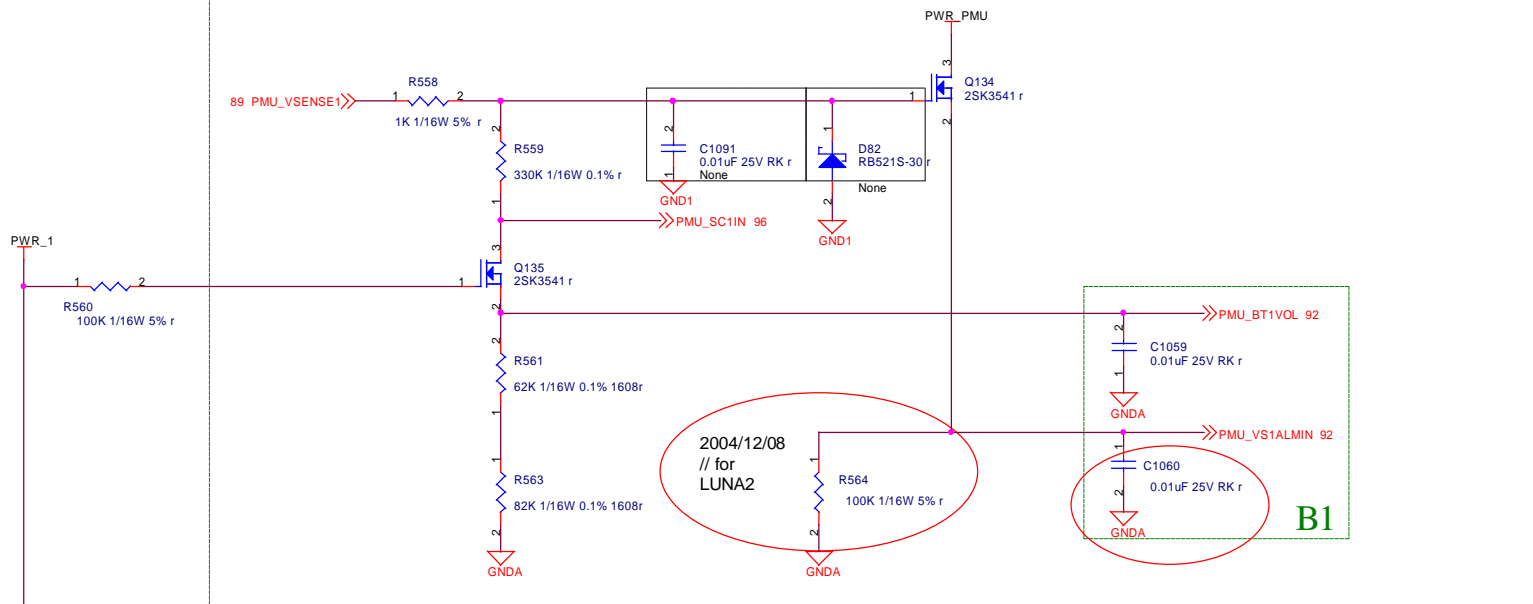
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Rev.	Date	Design	Check	Appr.	Description			Sheet
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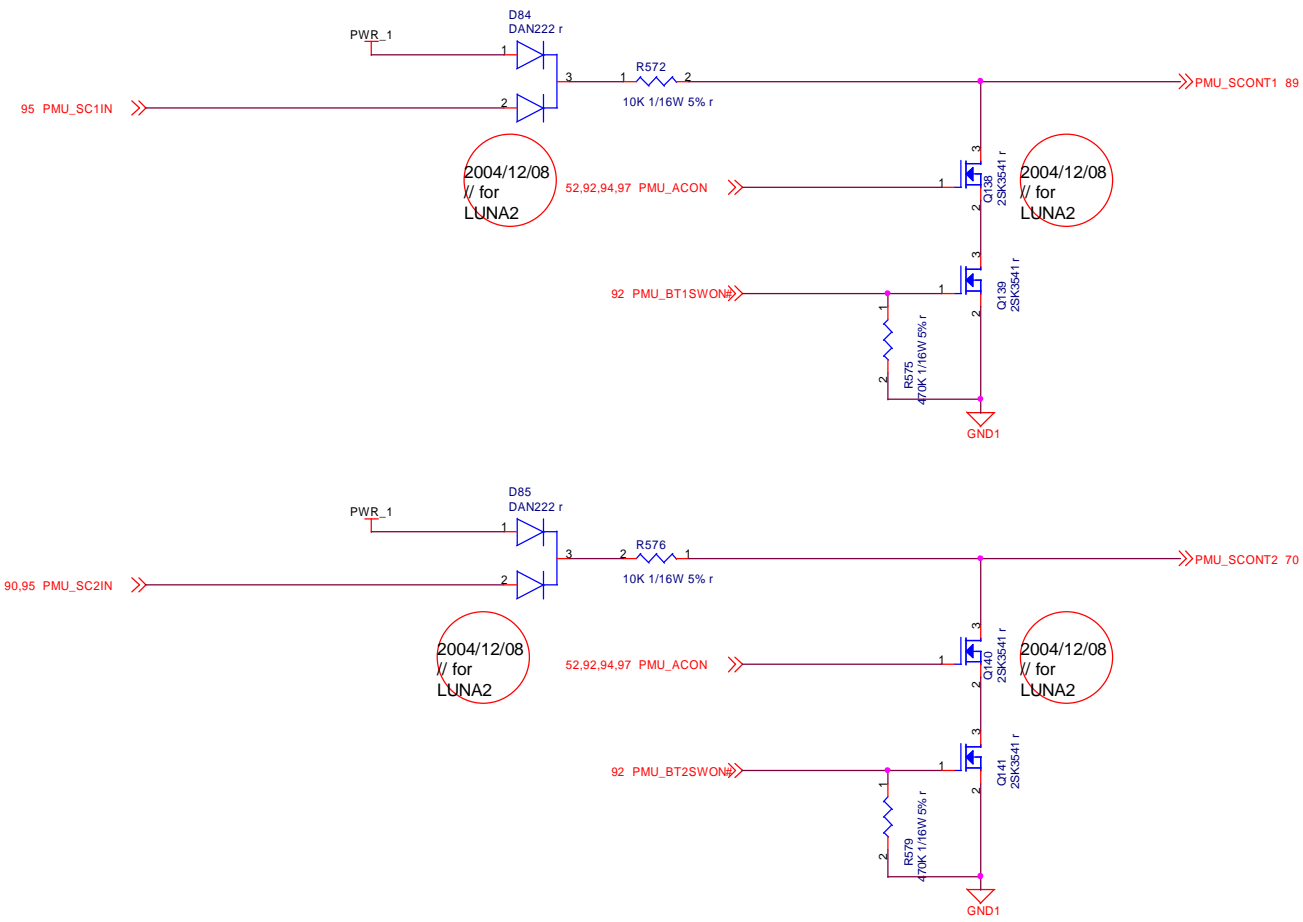
Power/ PMU/ AmMeter

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							94 / 99	



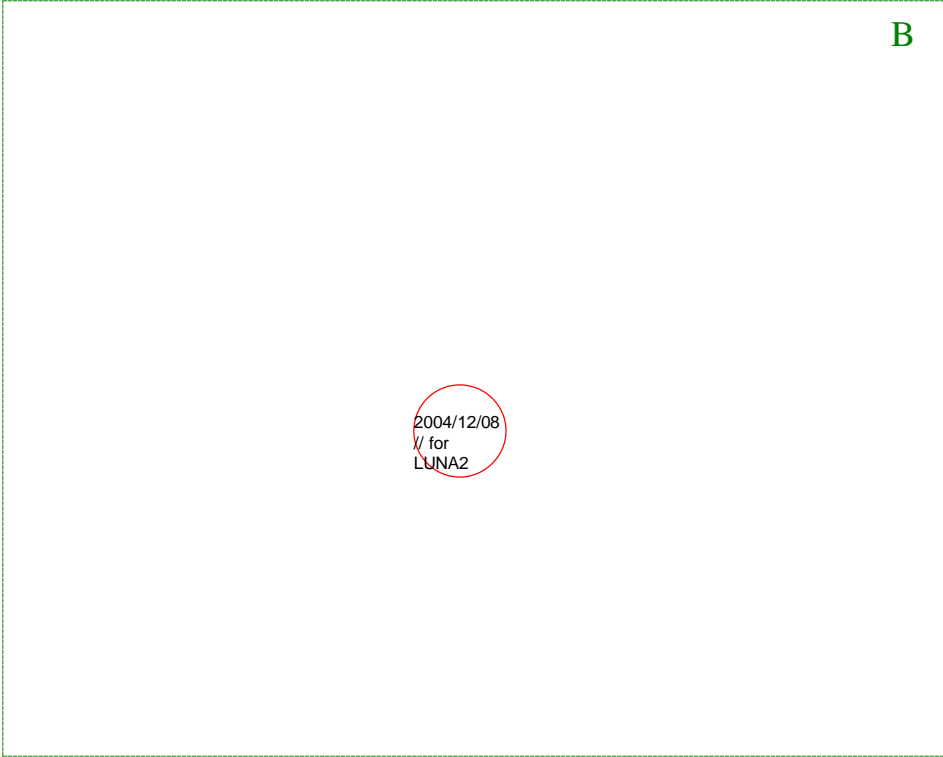
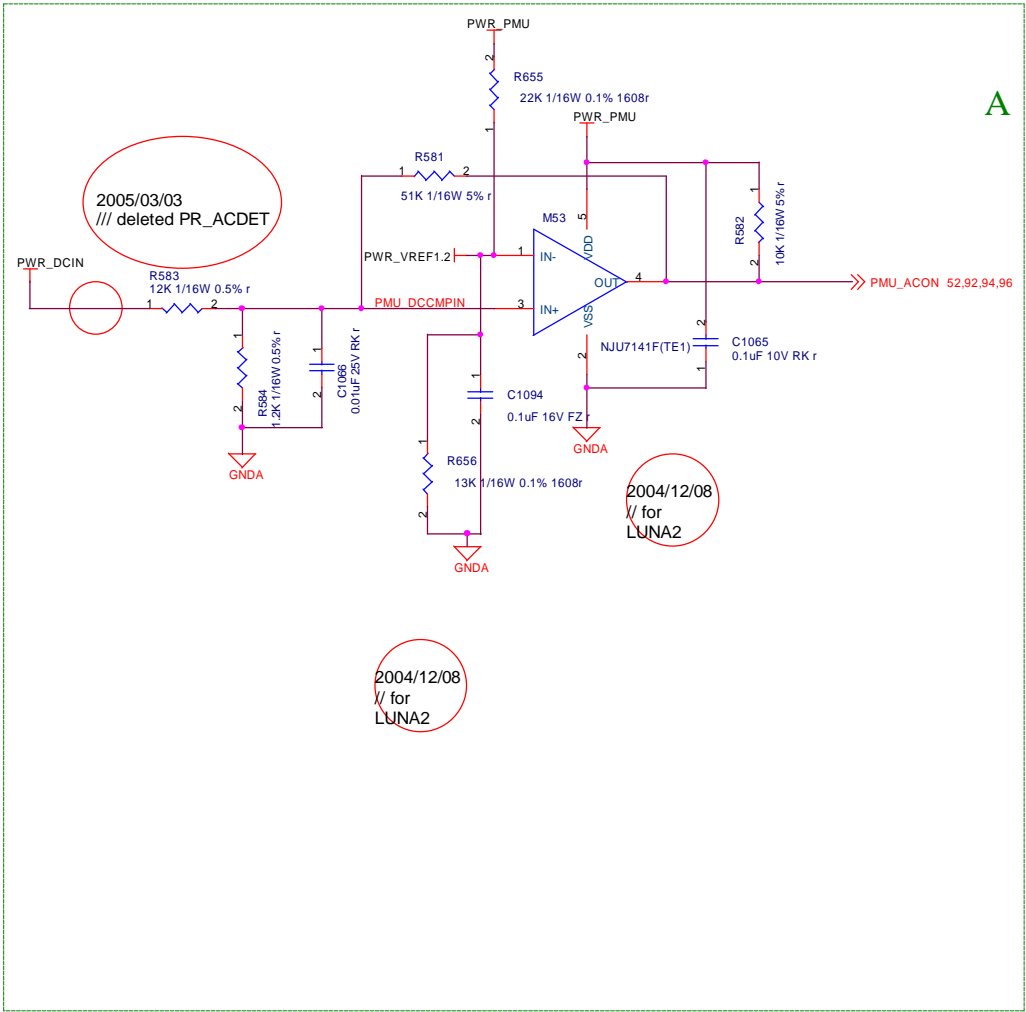
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Power/ PMU/ VolMeter

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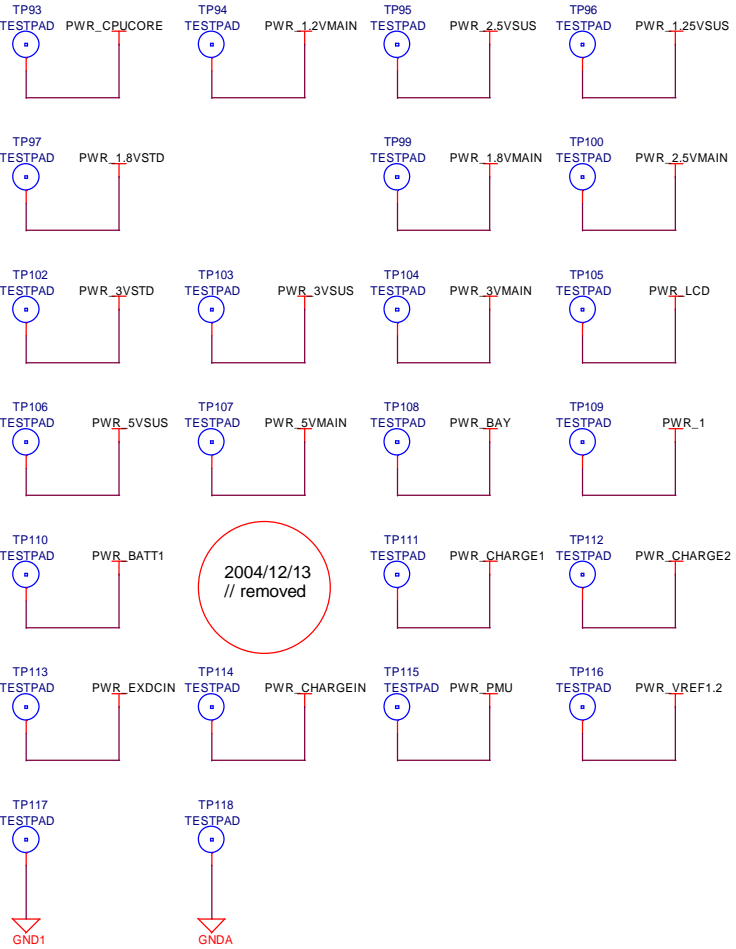
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Power/ PMU/ Scout

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Power/ PMU/ Etc1

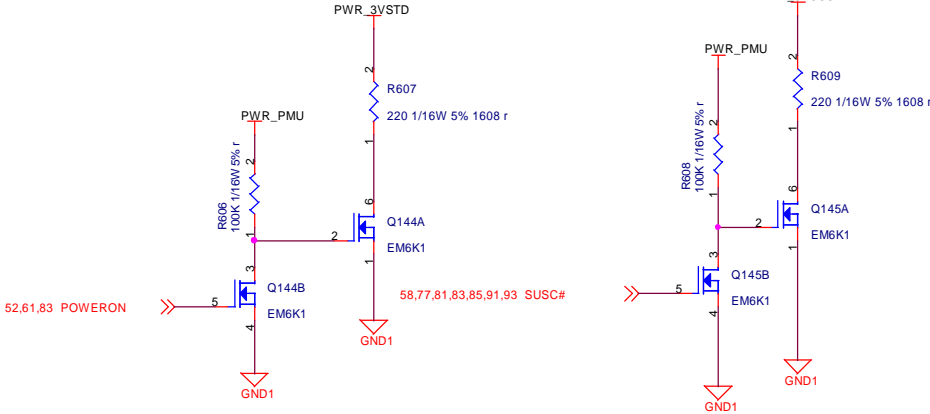
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[TestPad]

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FUJITSU LTD.							Sheet	98 / 99



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FUJITSU LTD.							Sheet 99 / 99	