

VULCAIN Discrete

SI Build

2008.12.26

DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC		
DESIGN							
CHECK							
RESPONSIBLE							
TITLE					VV Discrete		
SIZE =	3	VER :					
FILE NAME :	XXXX XXXXXX-XX			SIZE	CODE	DOC NUMBER	REV
P/N	XXXXXXXXXXXX			A3	CS	J310A22294-0-MTR	A01
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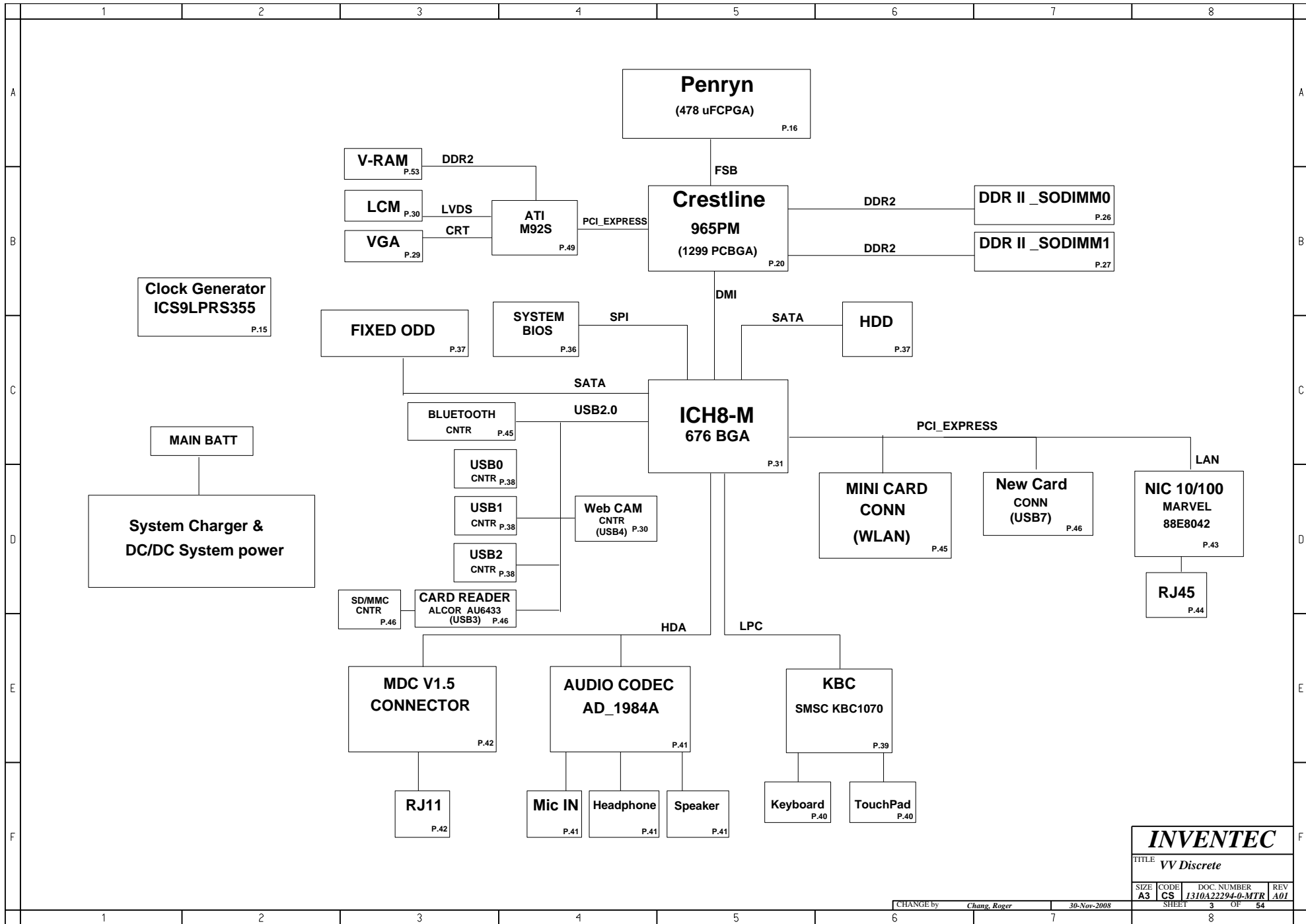
INVENTEC

TITLE *VV Discrete*

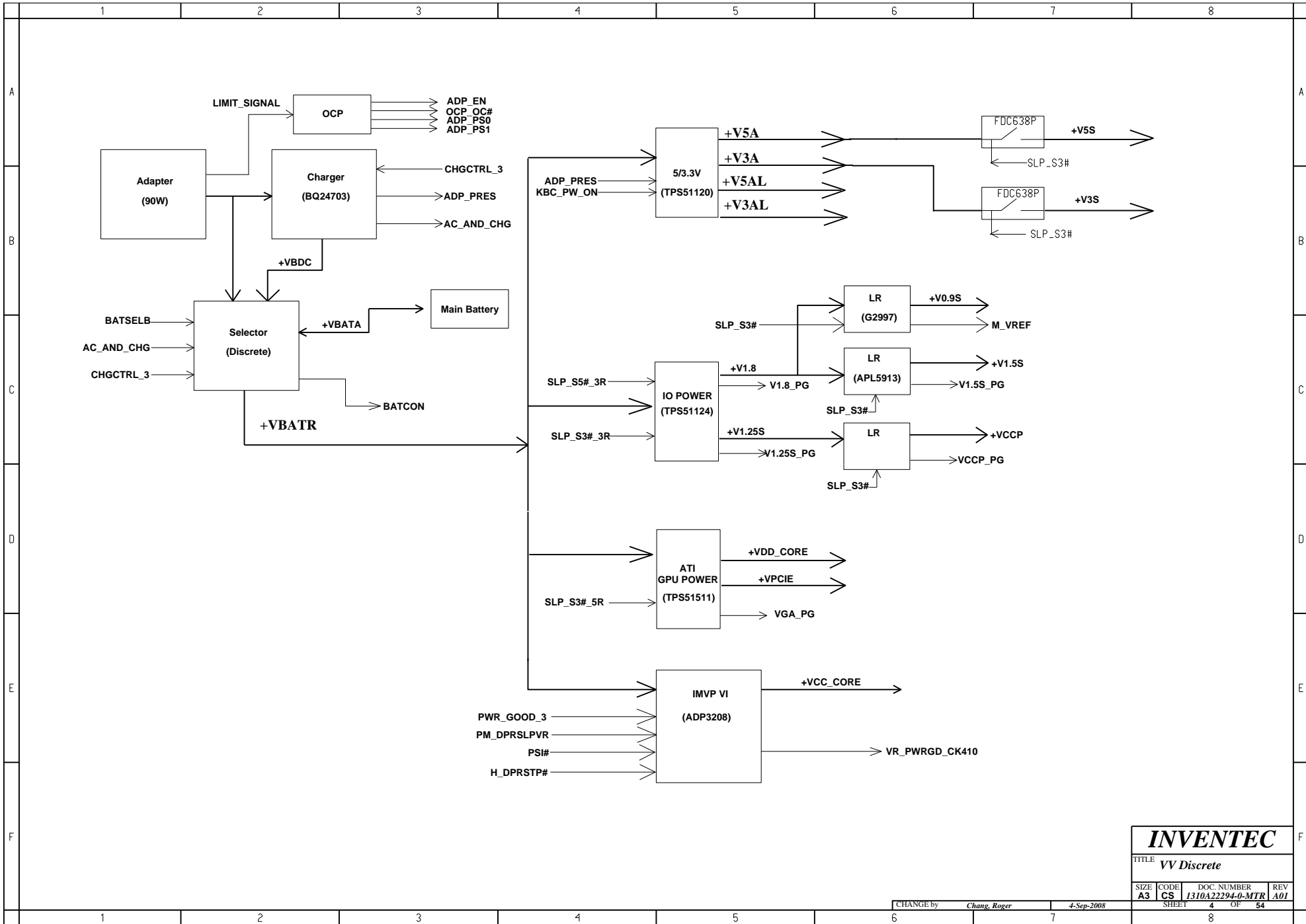
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

CHANGE by *Chang, Roger* 30-Nov-2008

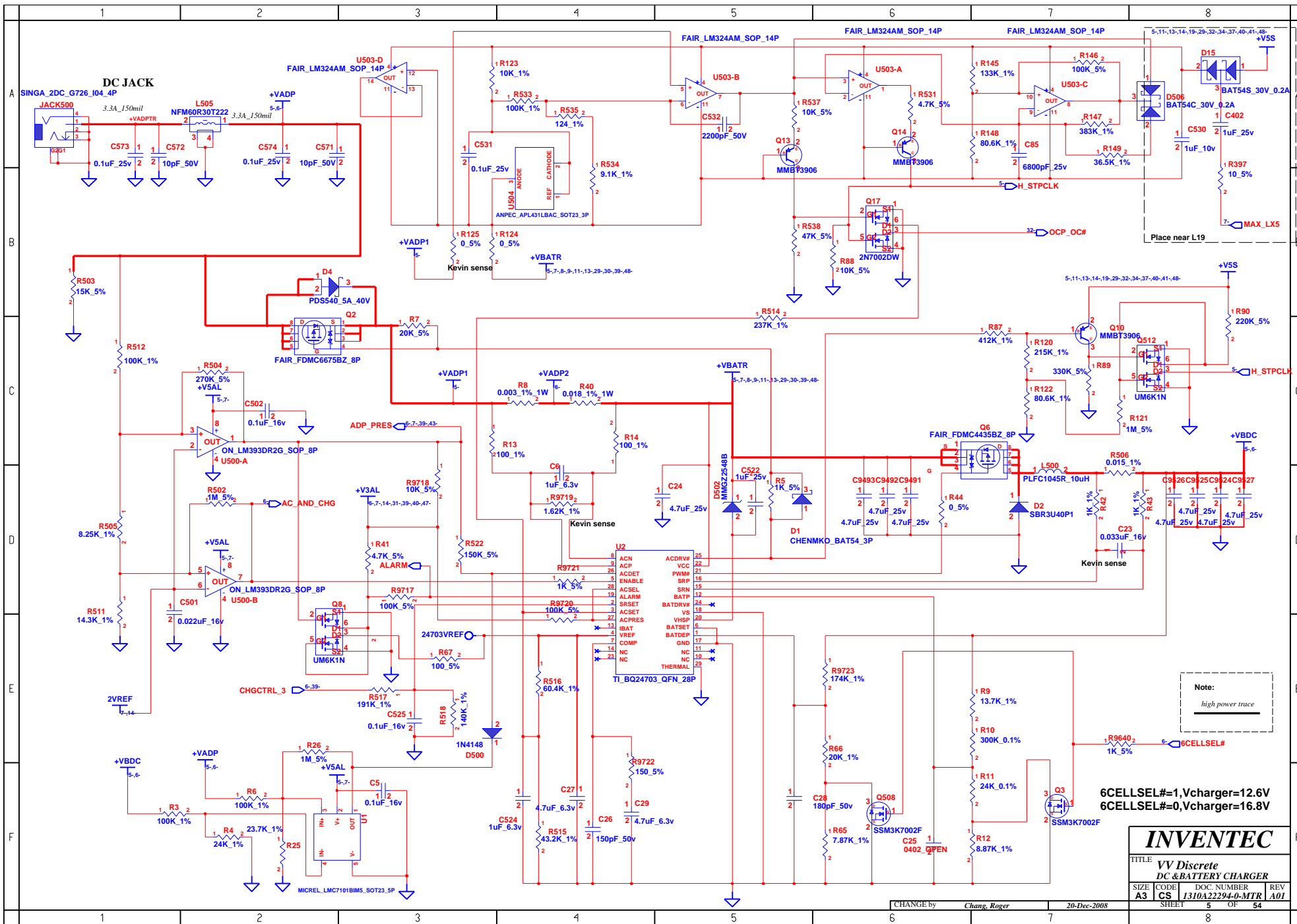
SHEET 2 OF 54



INVENTEC			
TITLE <i>VV Discrete</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A22294-0-MTR</i>	REV A01
CHANGE by <i>Chang, Roger</i>		30-Nov-2008	
SHEET 3		OF 54	



INVENTEC			
TITLE <i>VV Discrete</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A22294-0-MTR</i>	REV A01
CHANGE by <i>Chang, Roger</i>		4-Sep-2008	
SHEET 4		OF 54	



6CELLSEL#=1,Vcharger=12.6V
6CELLSEL#=0,Vcharger=16.8V

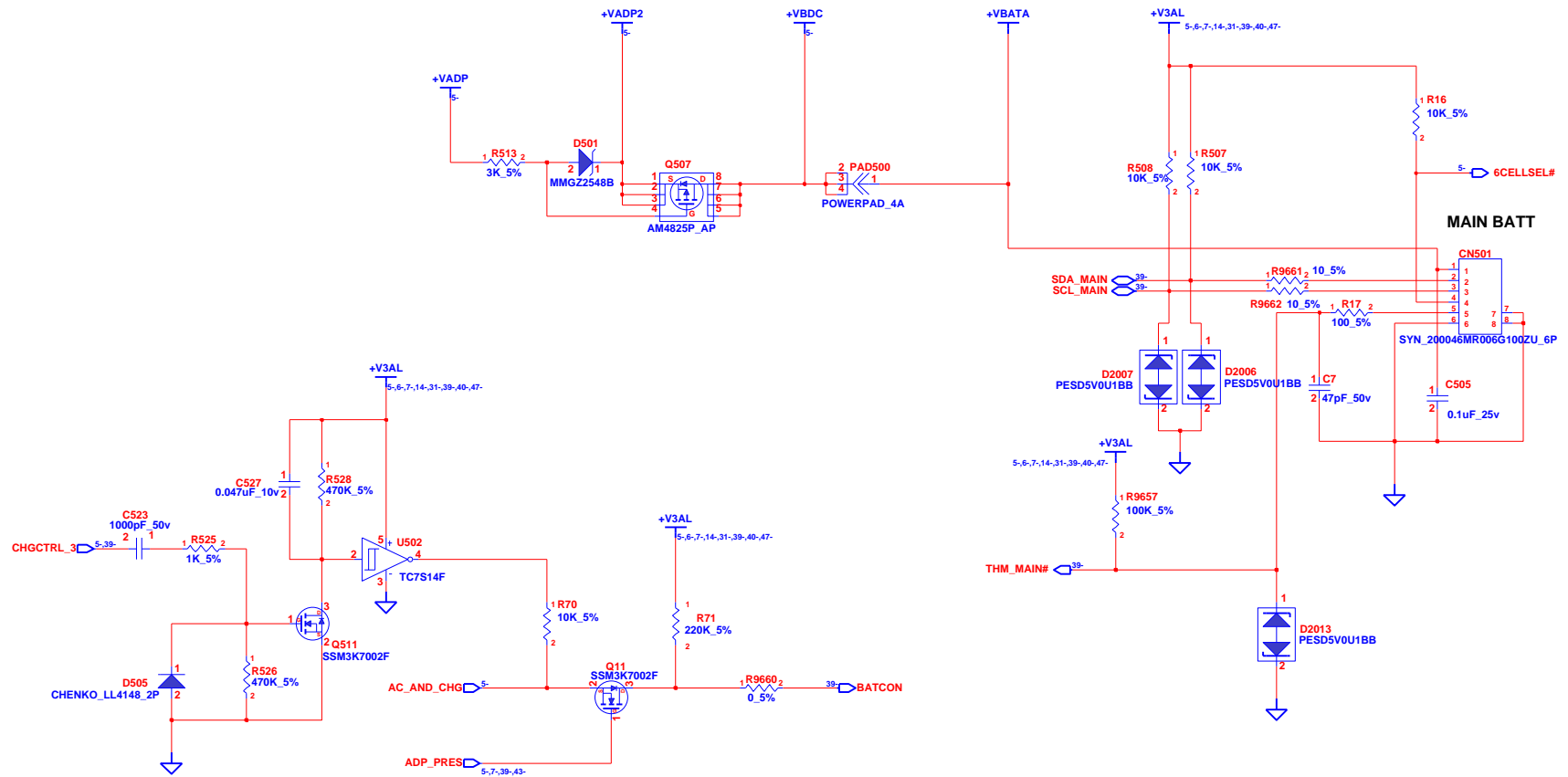
INVENTEC

TITLE: VV Discrete
DC & BATTERY CHARGER

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

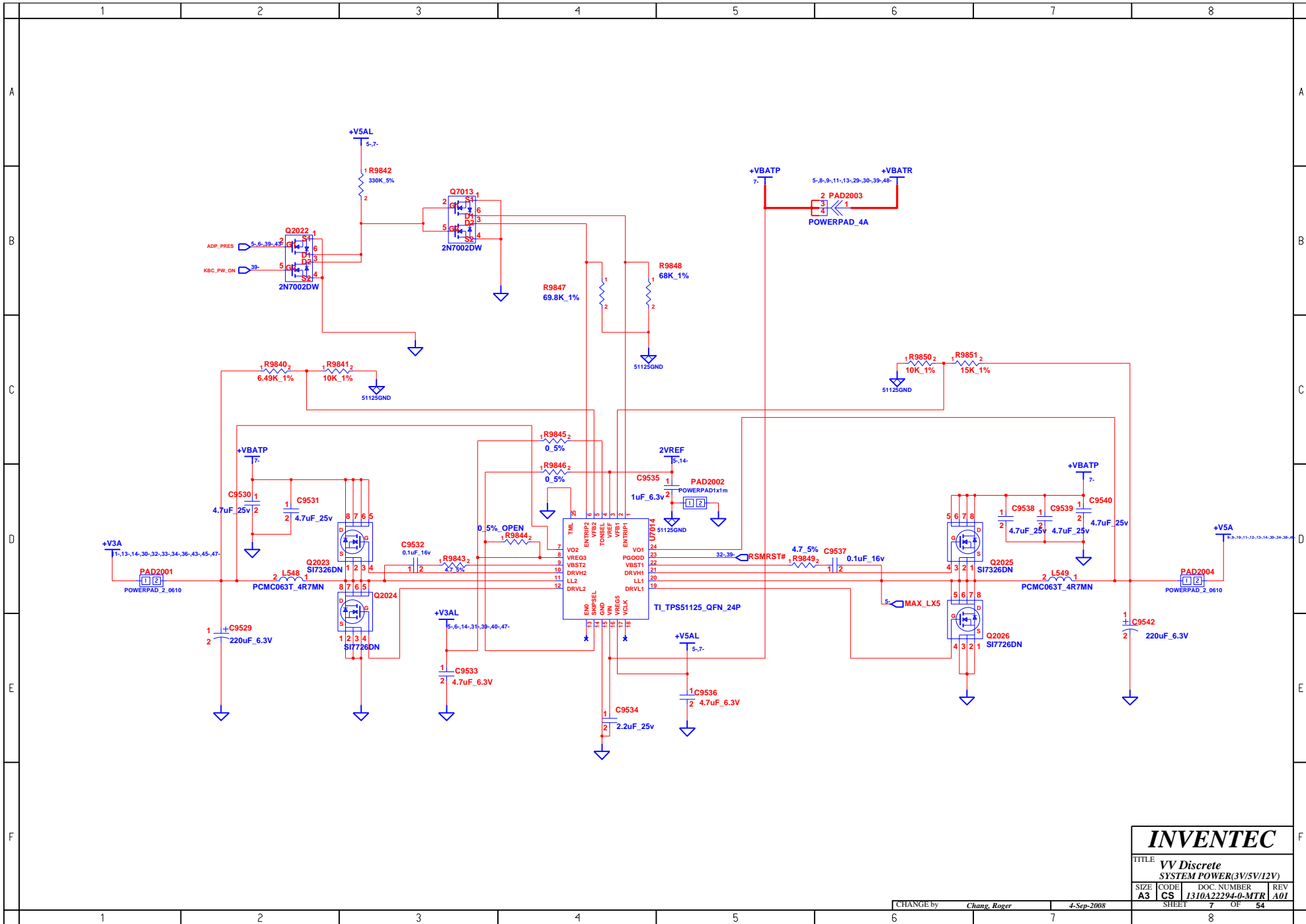
CHANGE by Chang, Roger 20-Dec-2008

SHEET 5 OF 54

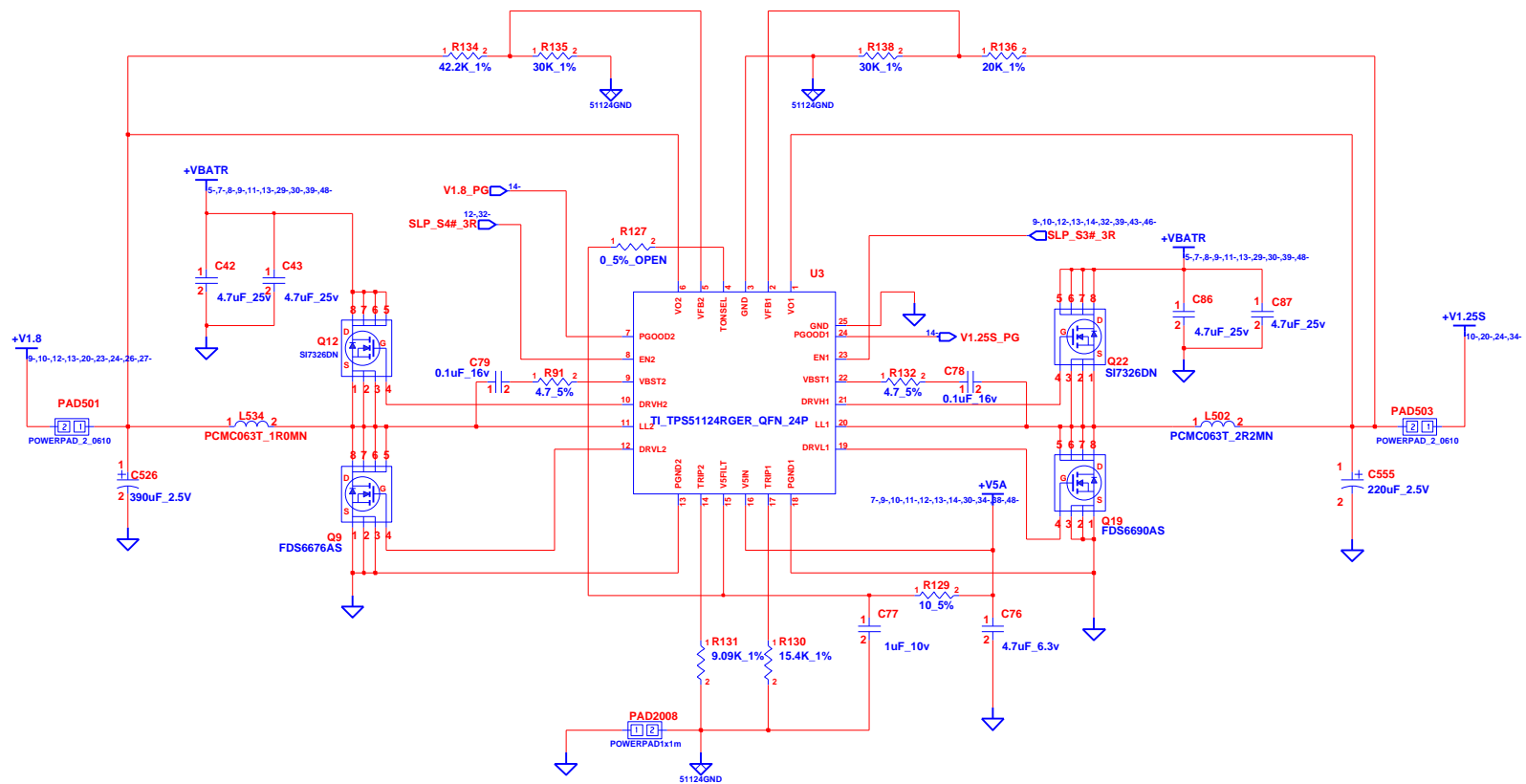


TITLE			
VV Discrete			
SELECT & BATTERY CONN			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01
CHANGE by		SHEET	
Chang, Roger		6 OF 54	

20-Dec-2008



INVENTEC			
TITLE VV Discrete SYSTEM POWER(3V/5V/12V)			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		4-Sep-2008	
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INVENTEC			
TITLE VV Discrete			
SYSTEM POWER(+V1.8/+V1.25S)			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		20-Dec-2008	
SHEET 8		OF 54	

1 2 3 4 5 6 7 8

A

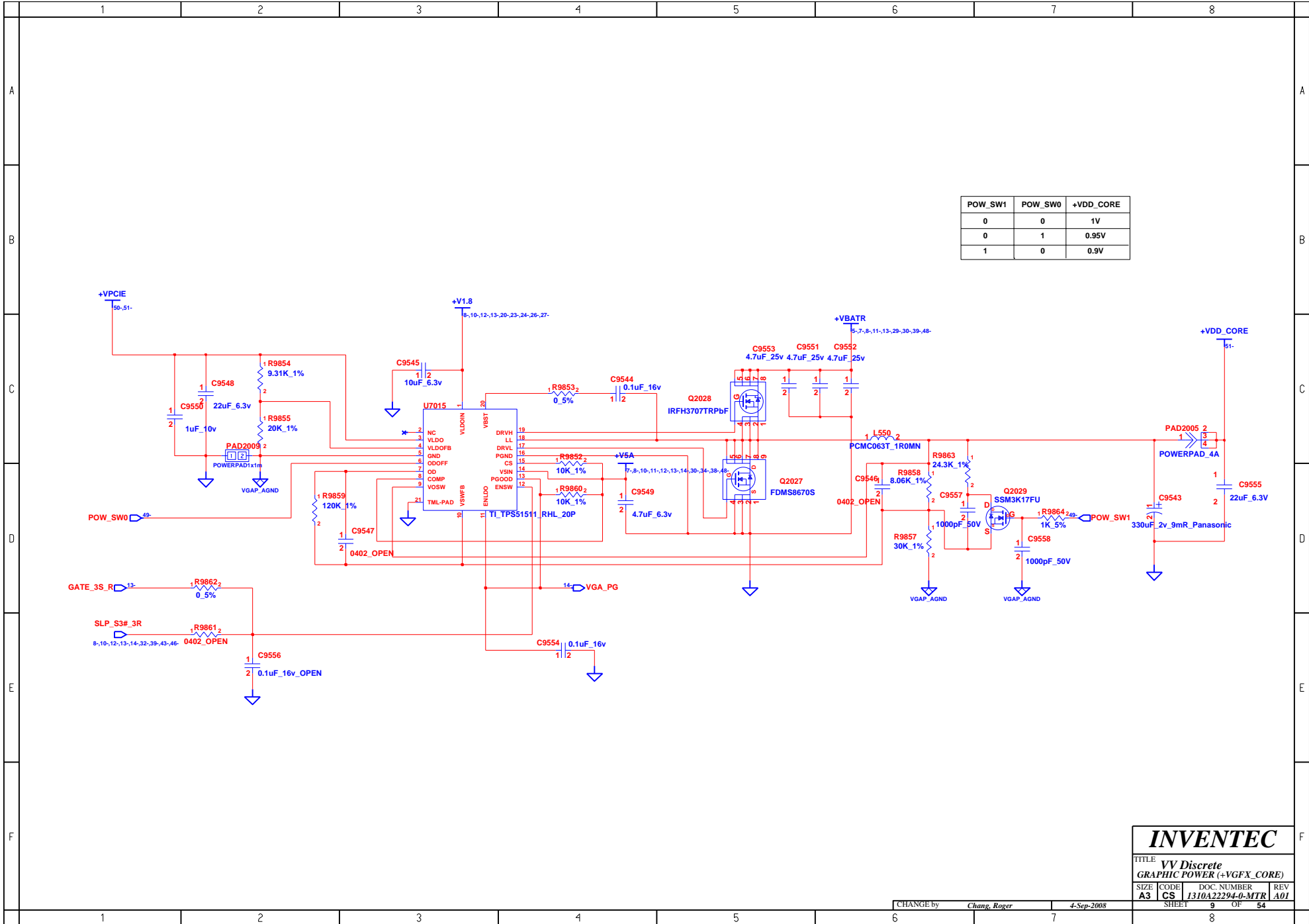
B

C

D

E

F



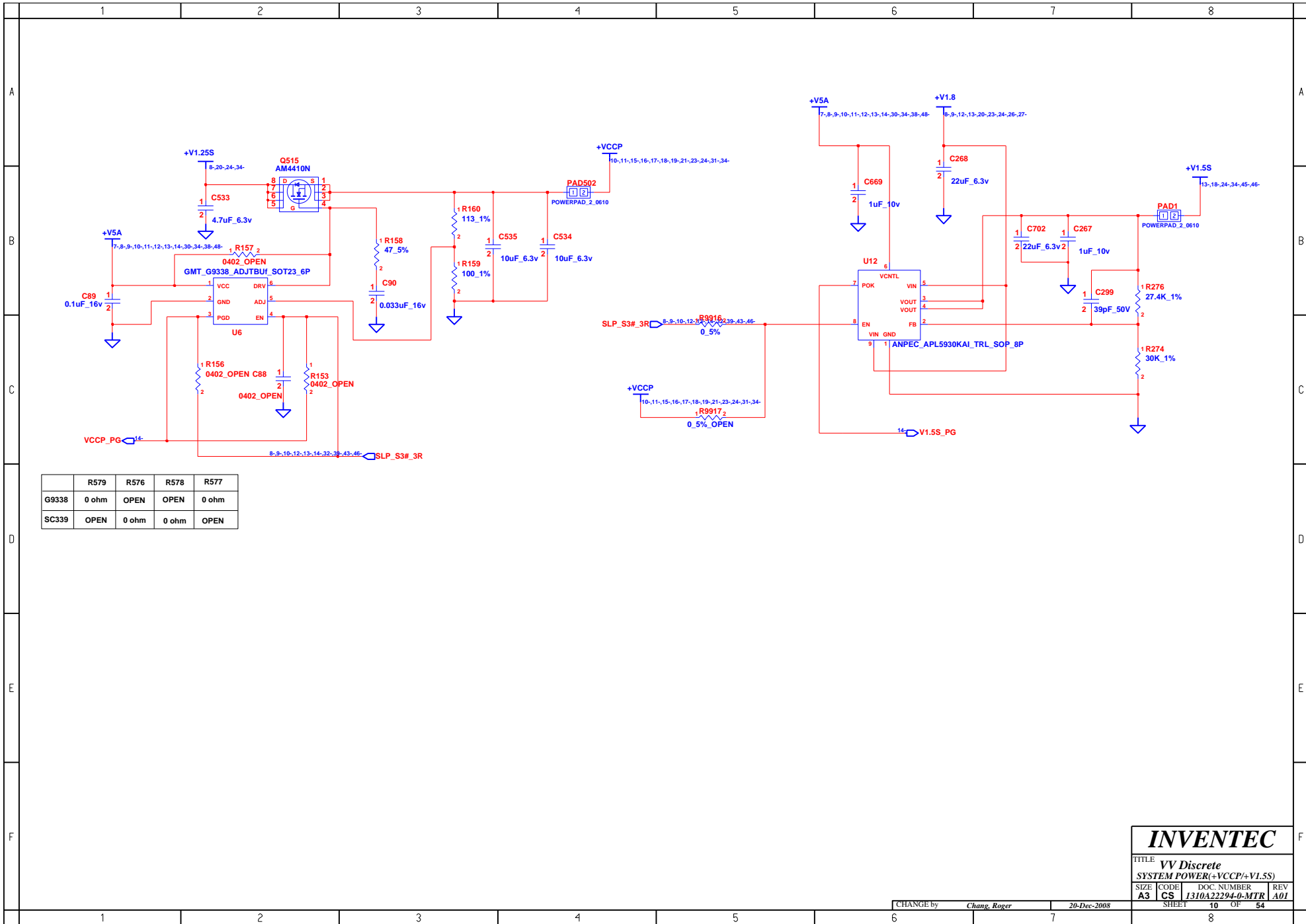
POW_SW1	POW_SW0	+VDD_CORE
0	0	1V
0	1	0.95V
1	0	0.9V

INVENTEC

TITLE **VV Discrete GRAPHIC POWER (+VGF_X_CORE)**

SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
SHEET 9		OF 54	

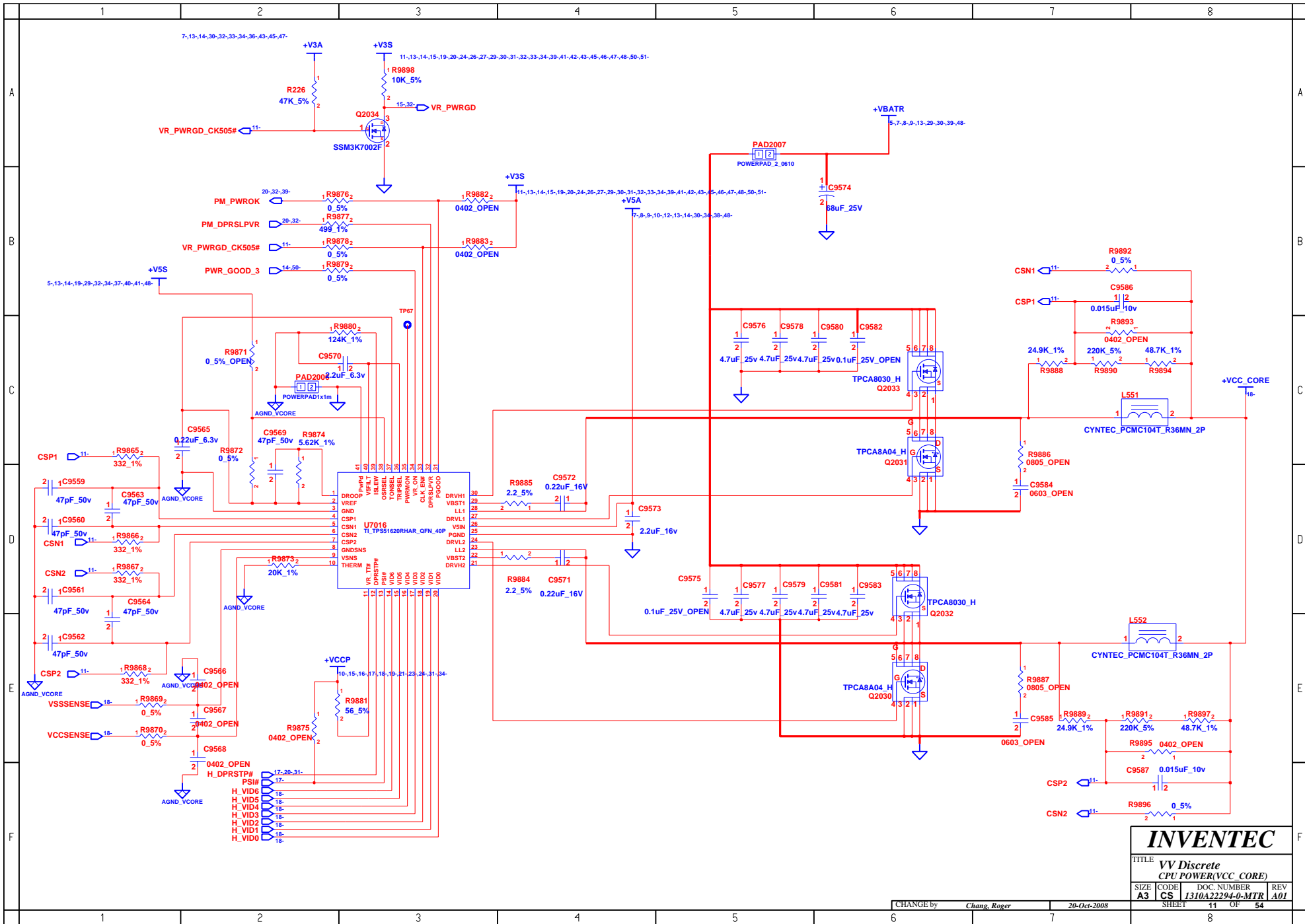
CHANGE by *Chang, Roger* 4-Sep-2008



INVENTEC

TITLE **VV Discrete**
SYSTEM POWER(+VCCP/+V1.5S)

SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger		20-Dec-2008	SHEET 10 OF 54

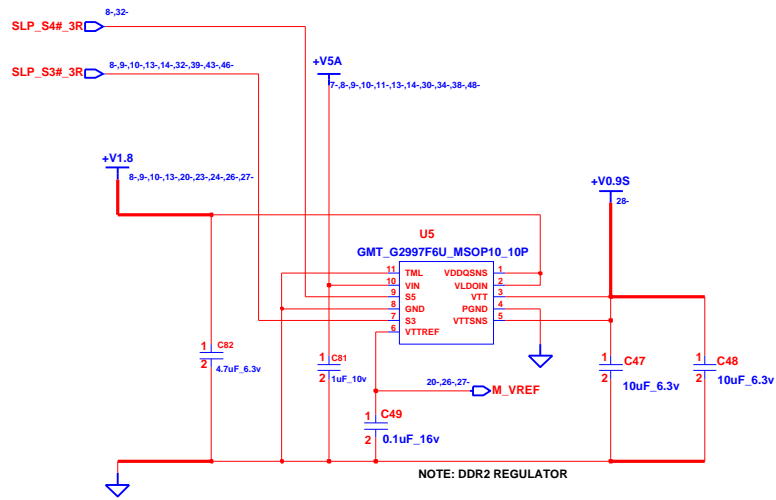


INVENTEC

TITLE: VV Discrete CPU POWER(VCC CORE)

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

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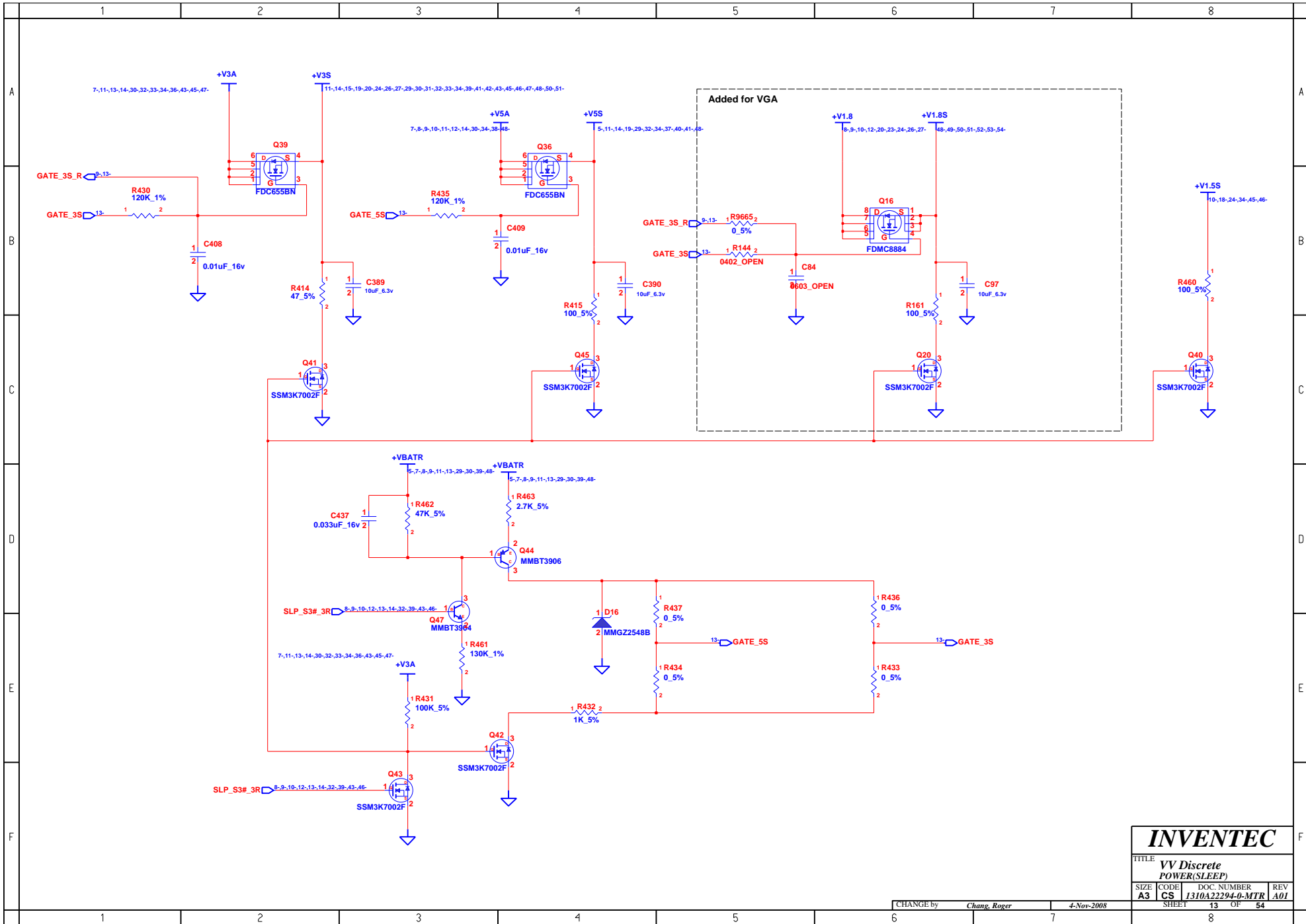


INVENTEC

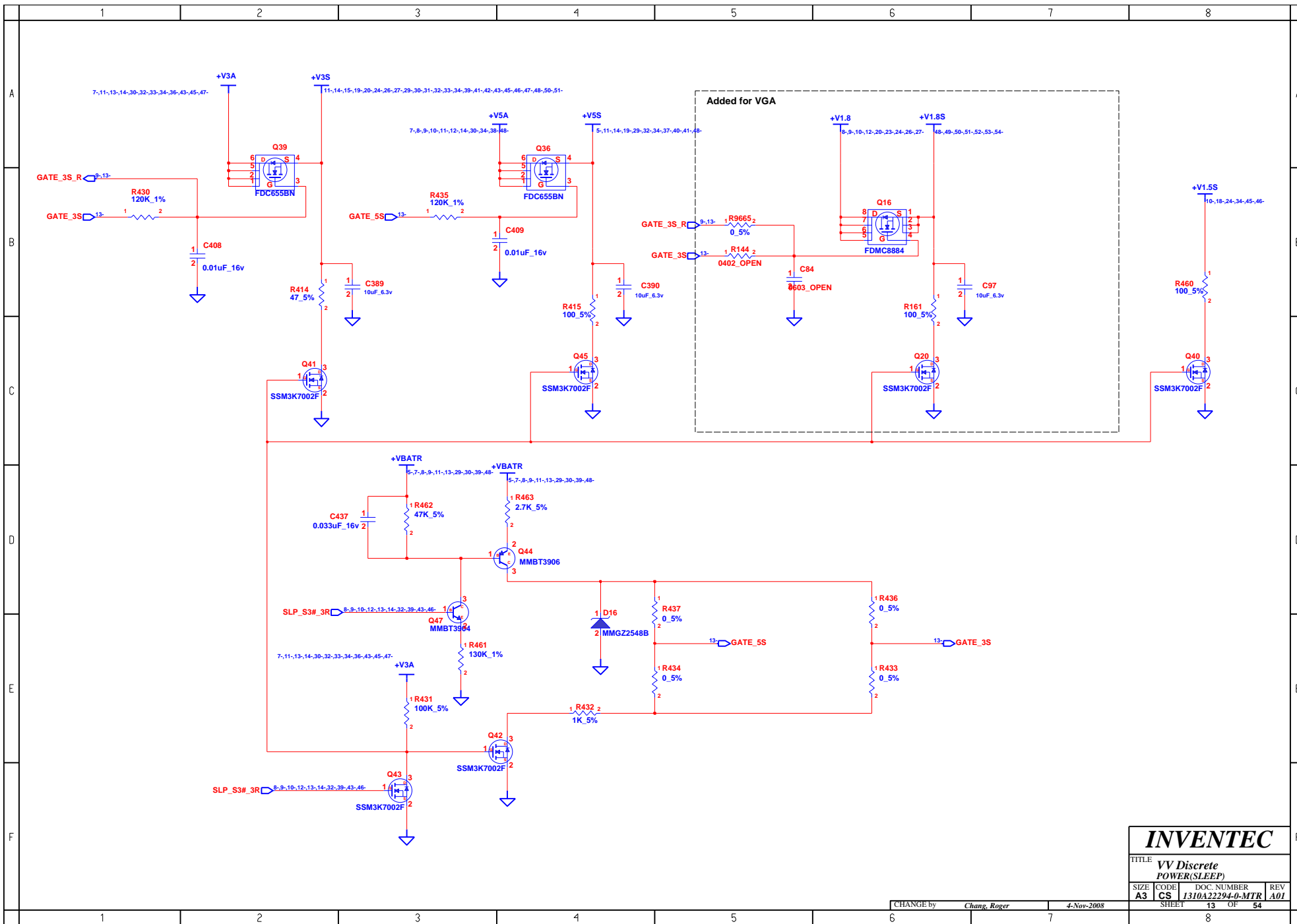
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DDR TERMINATION VOLTAGE			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01
SHEET		12	OF 54

CHANGE by *Chang, Roger* 4-Sep-2008

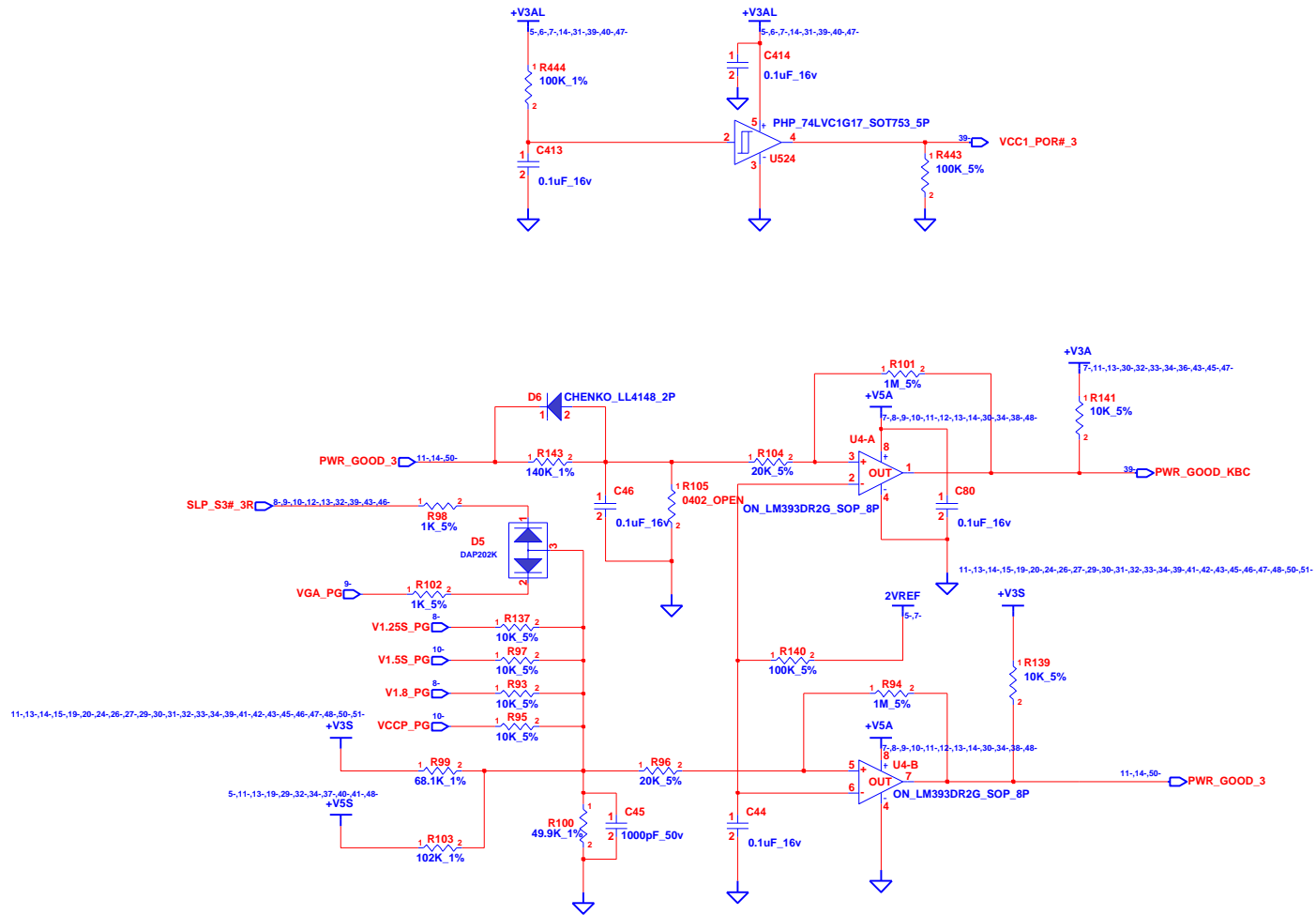
	1	2	3	4	5	6	7	8		
A										A
B										B
C										C
D										D
E										E
F										F
	1	2	3	4	5	6	7	8		



INVENTEC			
TITLE VV Discrete POWER(SLEEP)			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		4-Nov-2008	
SHEET 13		OF 54	



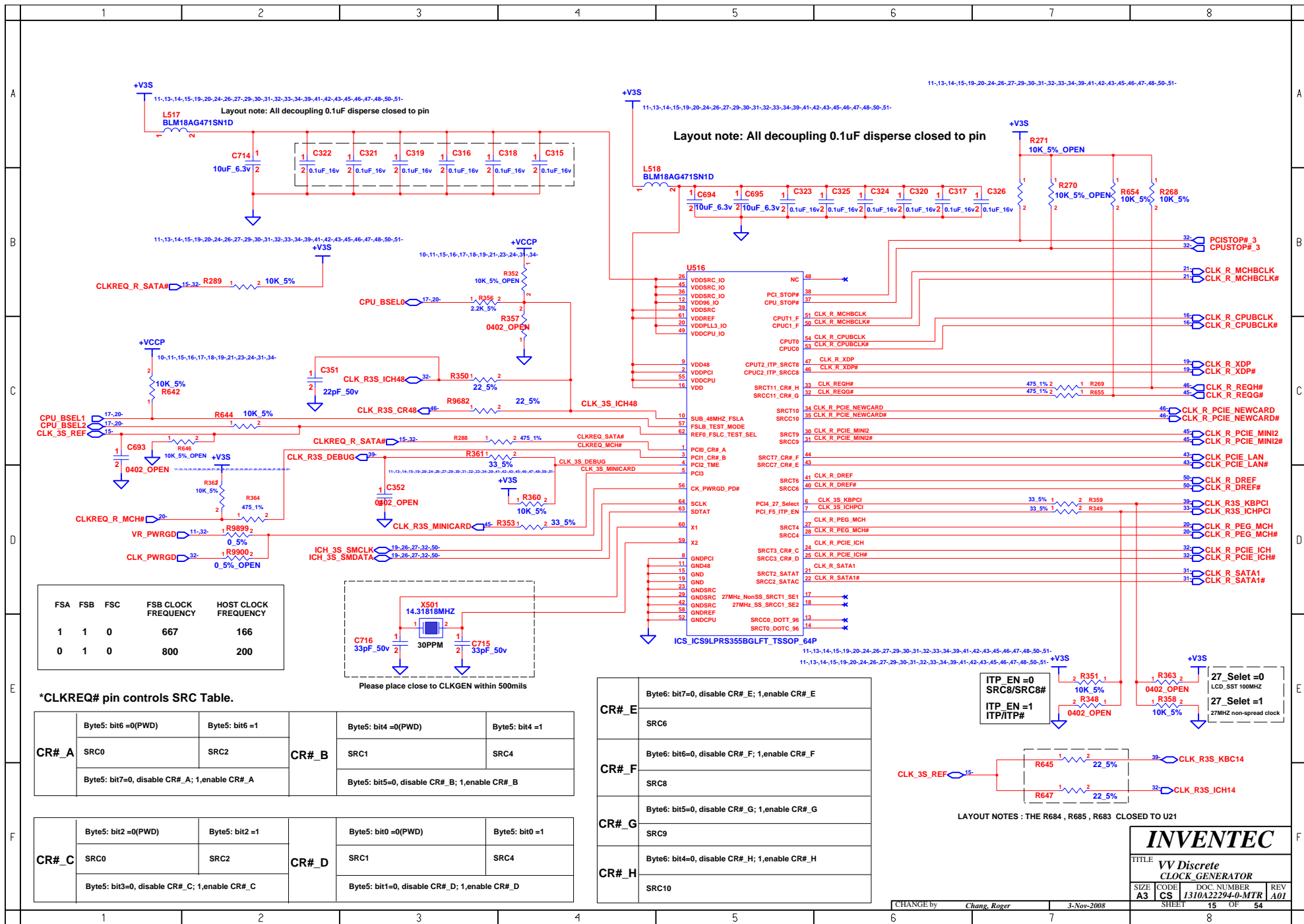
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TITLE VV Discrete POWER(SLEEP)			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		4-Nov-2008	
SHEET 13		OF 54	



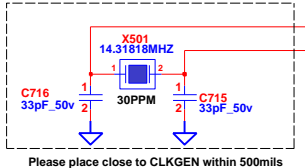
INVENTEC

TITLE			
VV Discrete POWER(SEQUENCE)			
SIZE	CODE	DOC NUMBER	REV
A3	CS	I310A22294-0-MTR	A01
SHEET		OF	
14		54	

CHANGE by Chang, Roger 4-Nov-2008



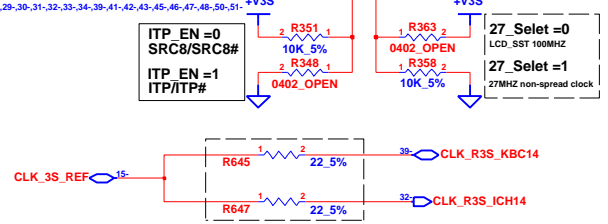
FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200



*CLKREQ# pin controls SRC Table.

CR#_A	Byte5: bit6 =0(PWD)		Byte5: bit6 =1		CR#_B	Byte5: bit4 =0(PWD)		Byte5: bit4 =1	
	SRC0	SRC2	SRC1	SRC4		SRC1	SRC4		
Byte5: bit7=0, disable CR#_A; 1,enable CR#_A		Byte5: bit5=0, disable CR#_B; 1,enable CR#_B		CR#_C		Byte5: bit2 =0(PWD)		Byte5: bit2 =1	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_D		Byte5: bit0 =0(PWD)		Byte5: bit0 =1	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_E		Byte5: bit7=0, disable CR#_E; 1,enable CR#_E		Byte5: bit7=0, disable CR#_F; 1,enable CR#_F	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_F		Byte5: bit6=0, disable CR#_F; 1,enable CR#_F		Byte5: bit6=0, disable CR#_G; 1,enable CR#_G	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_G		Byte5: bit5=0, disable CR#_G; 1,enable CR#_G		Byte5: bit5=0, disable CR#_H; 1,enable CR#_H	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_H		Byte5: bit4=0, disable CR#_H; 1,enable CR#_H		Byte5: bit4=0, disable CR#_I; 1,enable CR#_I	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_I		Byte5: bit3=0, disable CR#_I; 1,enable CR#_I		Byte5: bit3=0, disable CR#_J; 1,enable CR#_J	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_J		Byte5: bit2=0, disable CR#_J; 1,enable CR#_J		Byte5: bit2=0, disable CR#_K; 1,enable CR#_K	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_K		Byte5: bit1=0, disable CR#_K; 1,enable CR#_K		Byte5: bit1=0, disable CR#_L; 1,enable CR#_L	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_L		Byte5: bit0=0, disable CR#_L; 1,enable CR#_L		Byte5: bit0=0, disable CR#_M; 1,enable CR#_M	
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D		CR#_M		Byte5: bit0=0, disable CR#_M; 1,enable CR#_M		Byte5: bit0=0, disable CR#_N; 1,enable CR#_N	

CR#_E	Byte6: bit7=0, disable CR#_E; 1,enable CR#_E
SRC6	
CR#_F	Byte6: bit6=0, disable CR#_F; 1,enable CR#_F
SRC8	
CR#_G	Byte6: bit5=0, disable CR#_G; 1,enable CR#_G
SRC9	
CR#_H	Byte6: bit4=0, disable CR#_H; 1,enable CR#_H
SRC10	



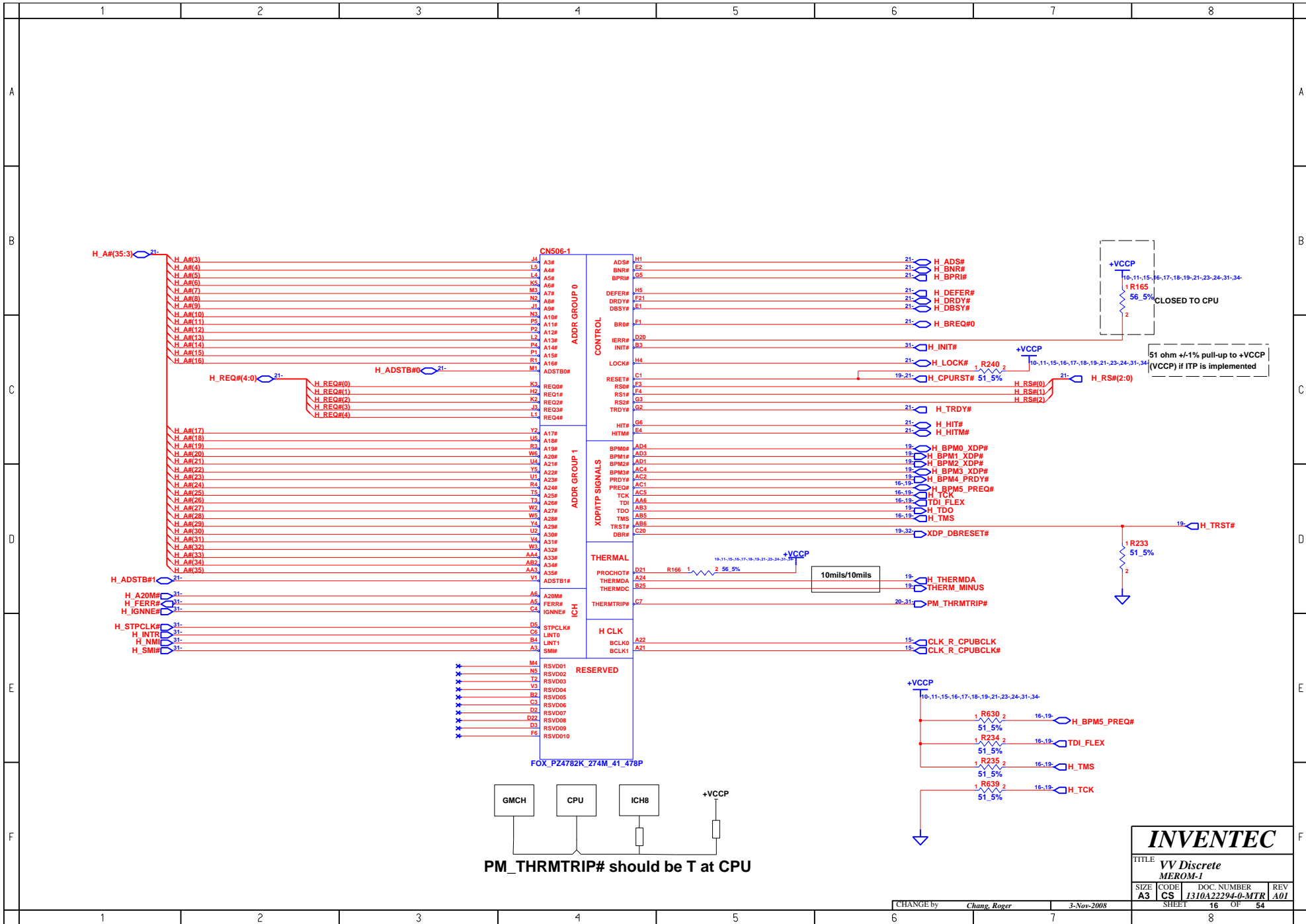
LAYOUT NOTES : THE R684 , R685 , R683 CLOSED TO U21

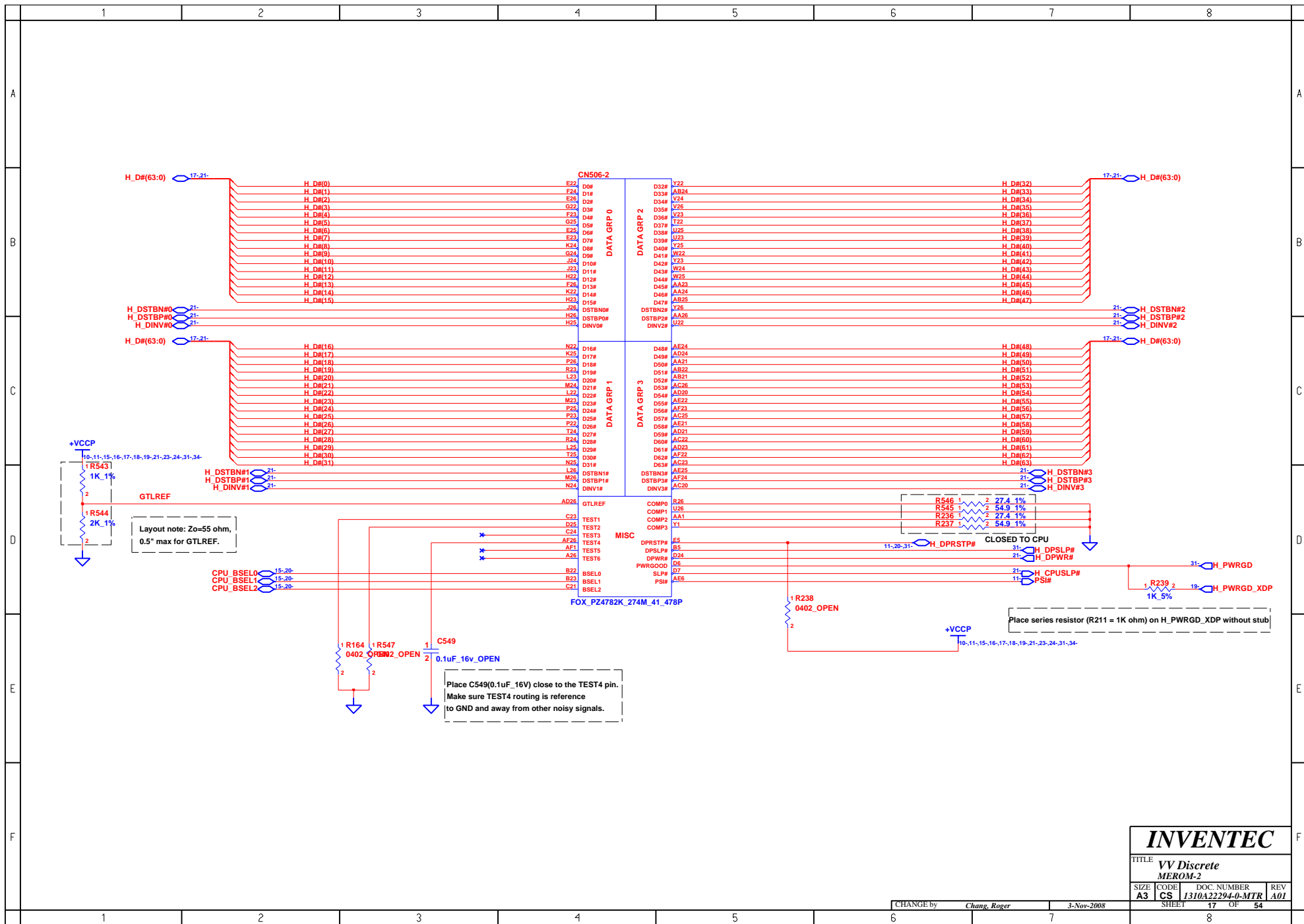
INVENTEC

TITLE: VV Discrete CLOCK GENERATOR

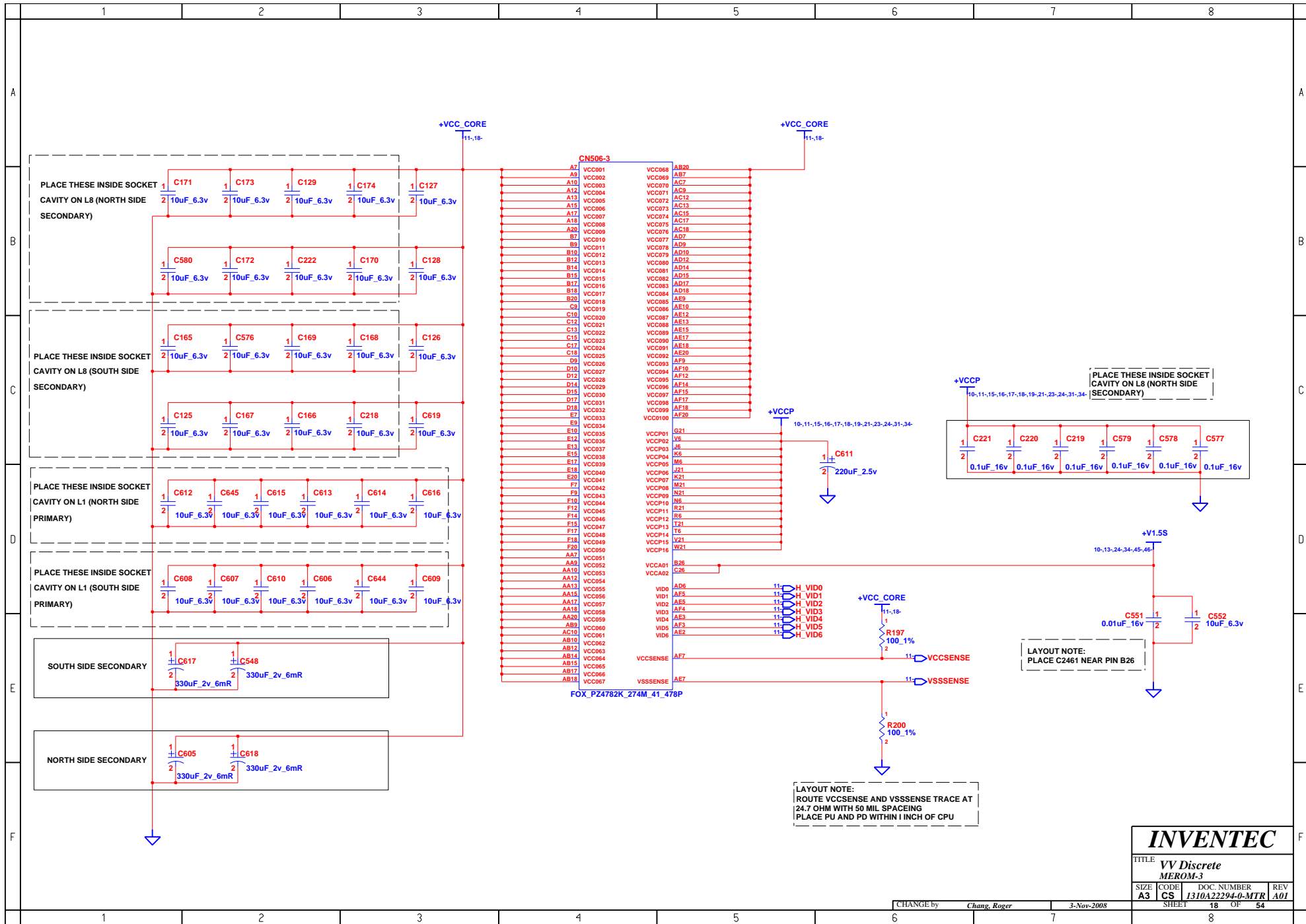
SIZE: A3 CODE: CS DOC NUMBER: 1310A22294-0-MTR REV: A01

SHEET: 15 OF 54

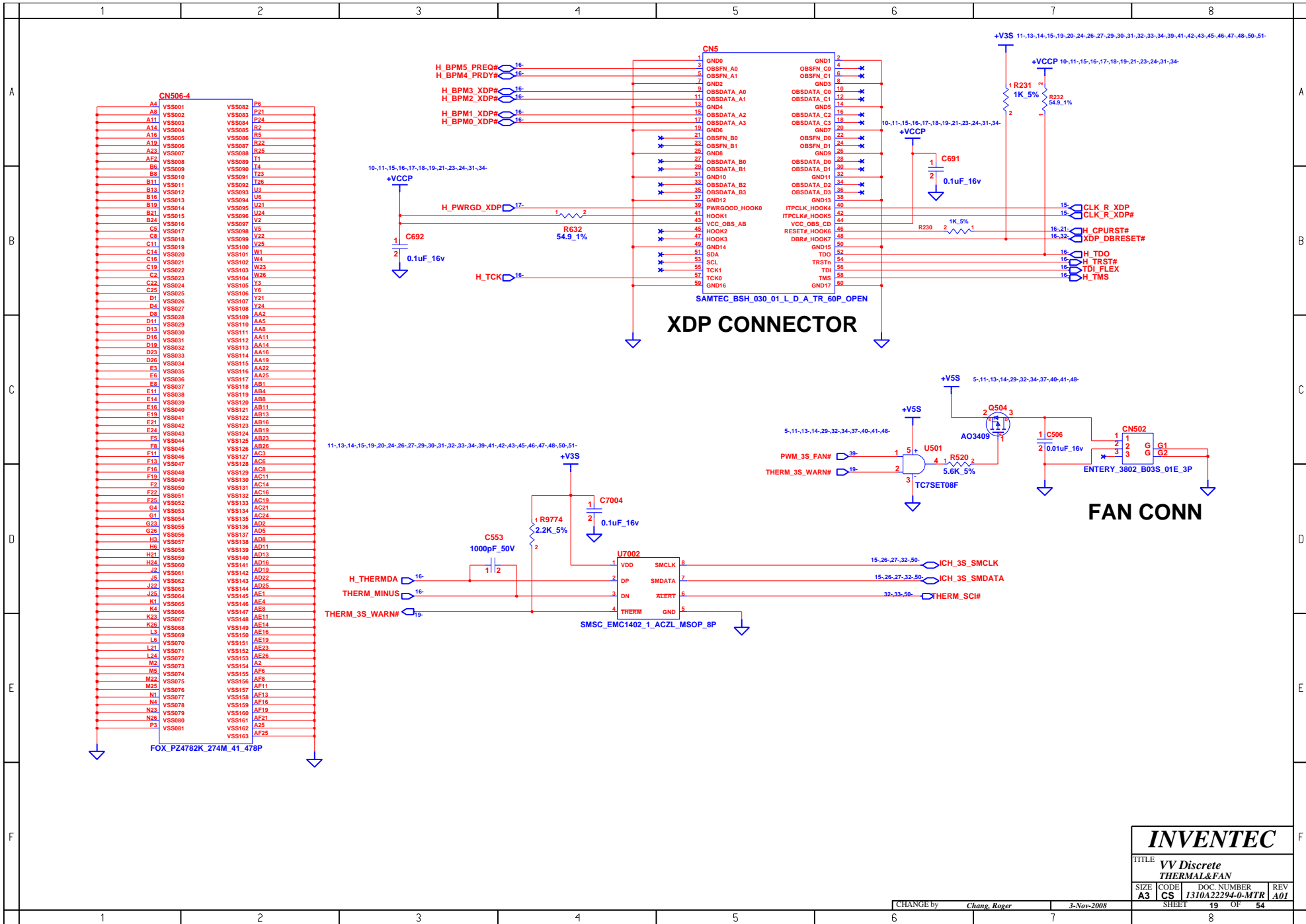




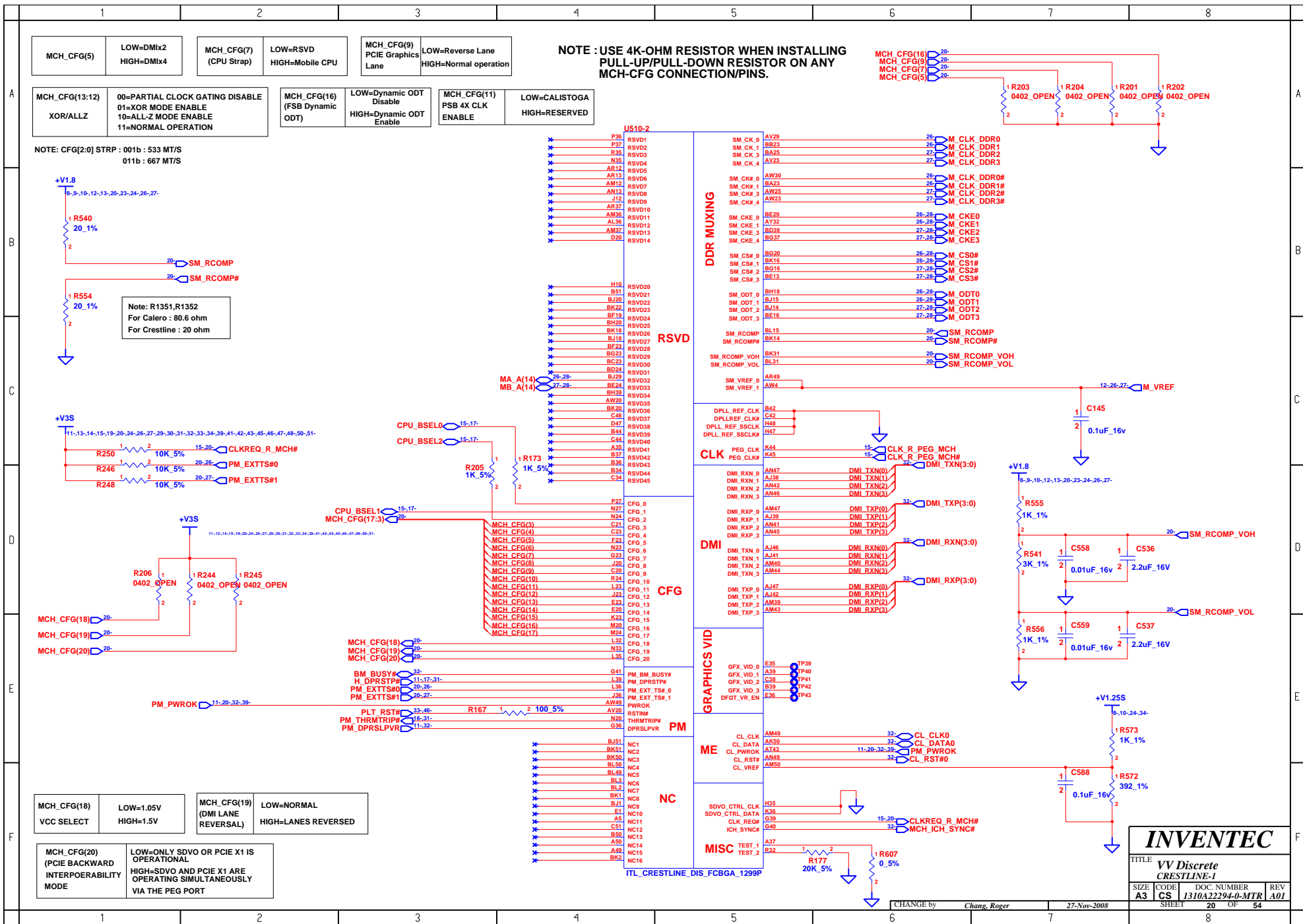
INVENTEC			
TITLE VV Discrete MEROM-2			
SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		3-Nov-2008	
SHEET 17		OF 54	



INVENTEC			
TITLE: VV Discrete MEROM-3			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22394-0-MTR	REV: A01
CHANGE by: Chang, Roger		3-Nov-2008	
SHEET: 18		OF: 54	



INVENTEC			
TITLE VV Discrete THERMAL&FAN			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger		3-Nov-2008	
SHEET 19		OF 54	



MCH_CFG(5) LOW=DMiX2 HIGH=DMiX4	MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU	MCH_CFG(9) PCIE Graphics Lane	LOW=Reverse Lane HIGH=Normal operation
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MCH_CFG(13:12) XOR/ALLZ	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION	MCH_CFG(16) MCH Dynamic ODT)	LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable	MCH_CFG(11) PSB 4X CLK ENABLE	LOW=CALISTOGA HIGH=RESERVED
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NOTE: CFG[2:0] STRP : 001b : 533 MT/S
011b : 667 MT/S

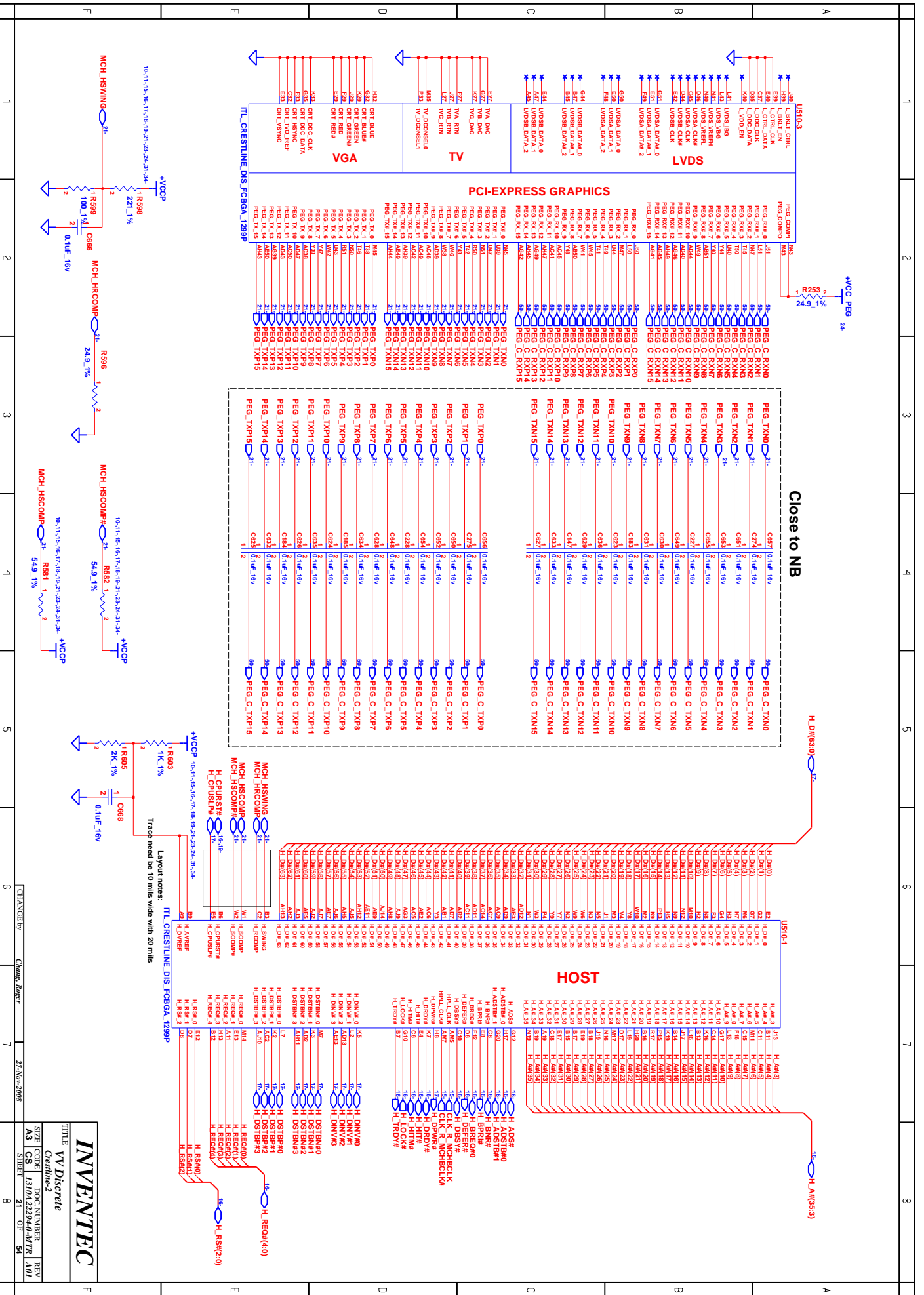
Note: R1351,R1352
For Calero : 80.6 ohm
For Crestline : 20 ohm

NOTE: USE 4K-OHM RESISTOR WHEN INSTALLING
PULL-UP/PULL-DOWN RESISTOR ON ANY
MCH-CFG CONNECTION/PINS.

MCH_CFG(18) VCC SELECT	LOW=1.05V HIGH=1.5V	MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED
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MCH_CFG(20) PCIE BACKWARD INTERPOERABILITY MODE	LOW=ONLY SDVO OR PCIE X1 IS OPERATIONAL HIGH=SDVO AND PCIE X1 ARE OPERATING SIMULTANEOUSLY VIA THE PEG PORT
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INVENTEC			
TITLE VV Discrete CRESTLINE-1			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
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INVENTTEC

Doc Number: **1310A22294P2MTR**

Rev: **A01**

DATE: **21-07-2008**

SIZE: **A3**

CODE: **CS**

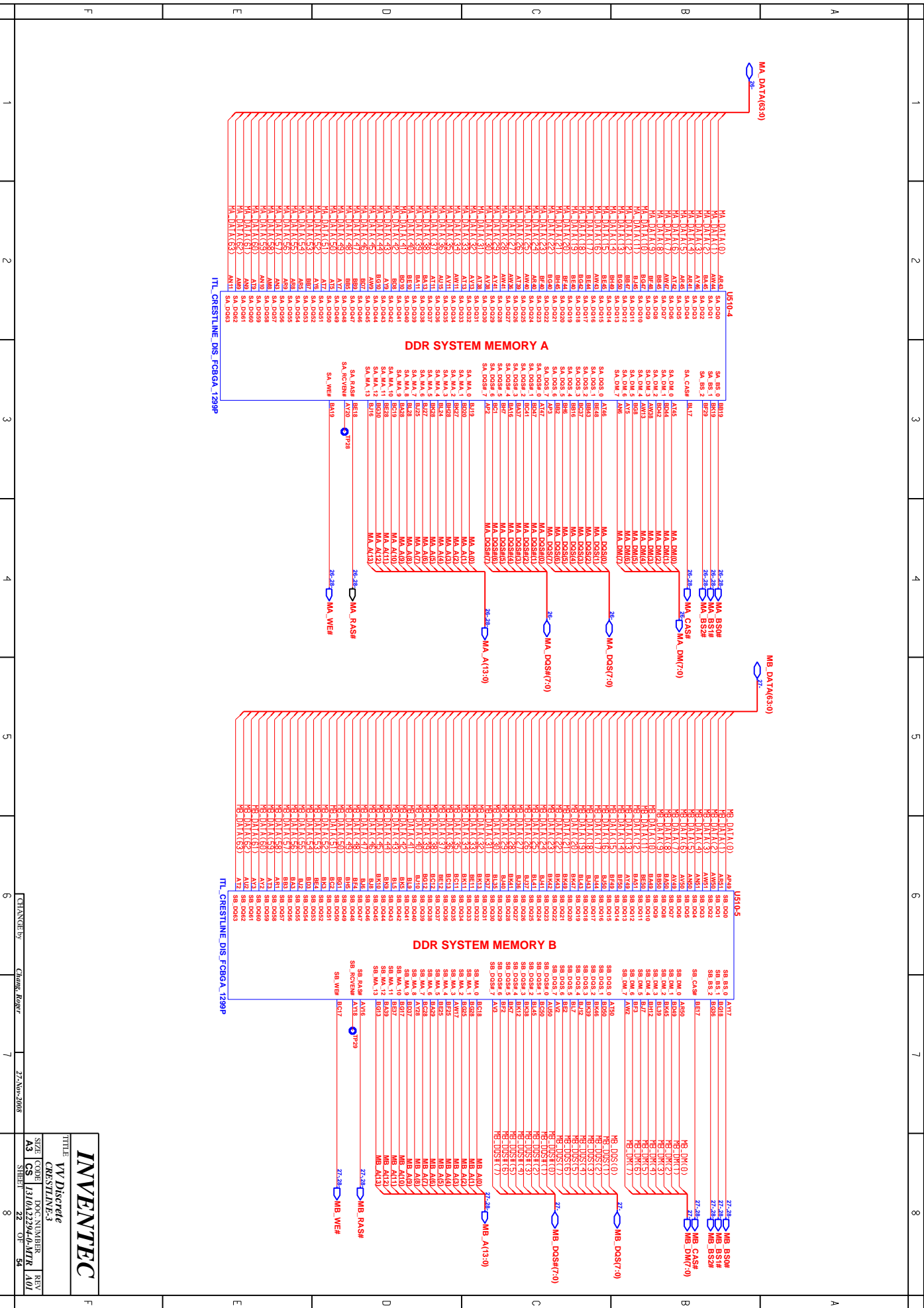
STREET: **Z1**

REV: **54**

Layout notes:
 1. Trace need be 10 mils wide with 20 mils spacing.

CHANGE BY: **Change Range**

27-Nov-2008



DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

ITL_CRESTRINE_DIS_F0BGA_1299P

ITL_CRESTRINE_DIS_F0BGA_1299P

A

B

C

D

E

F

1

2

3

4

5

6

7

8

A

B

C

D

E

F

1

2

3

4

5

6

7

8

A

B

C

D

E

F

1

2

3

4

5

6

7

8

A

B

C

D

E

F

INVENTTEC

VV Discrete

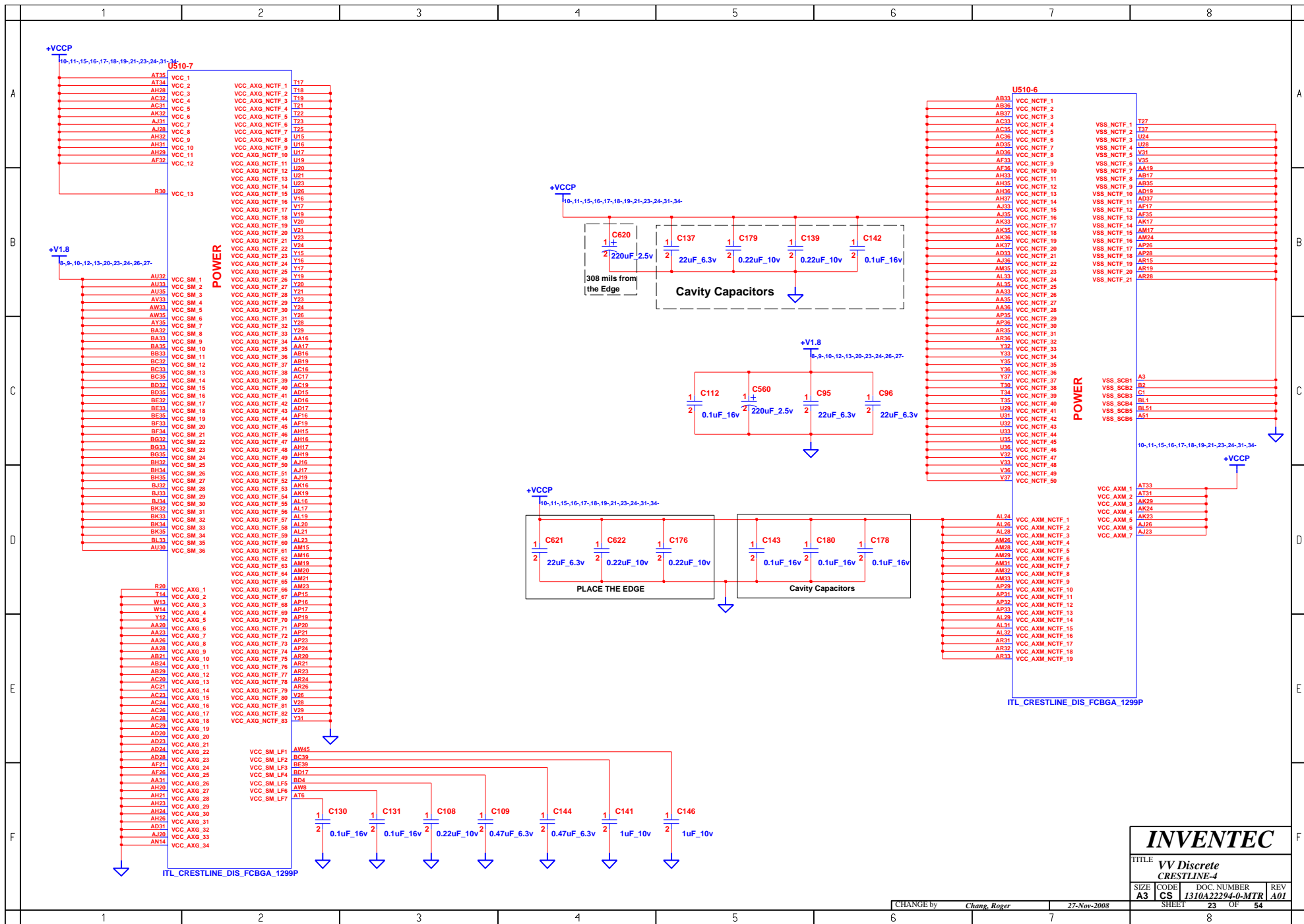
CRESTRINE-V3

SIZE CODE DOC NUMBER REV

A3 CS 1310A2204-1MR A01

CHANGED BY Chang Rong

27-Nov-2008

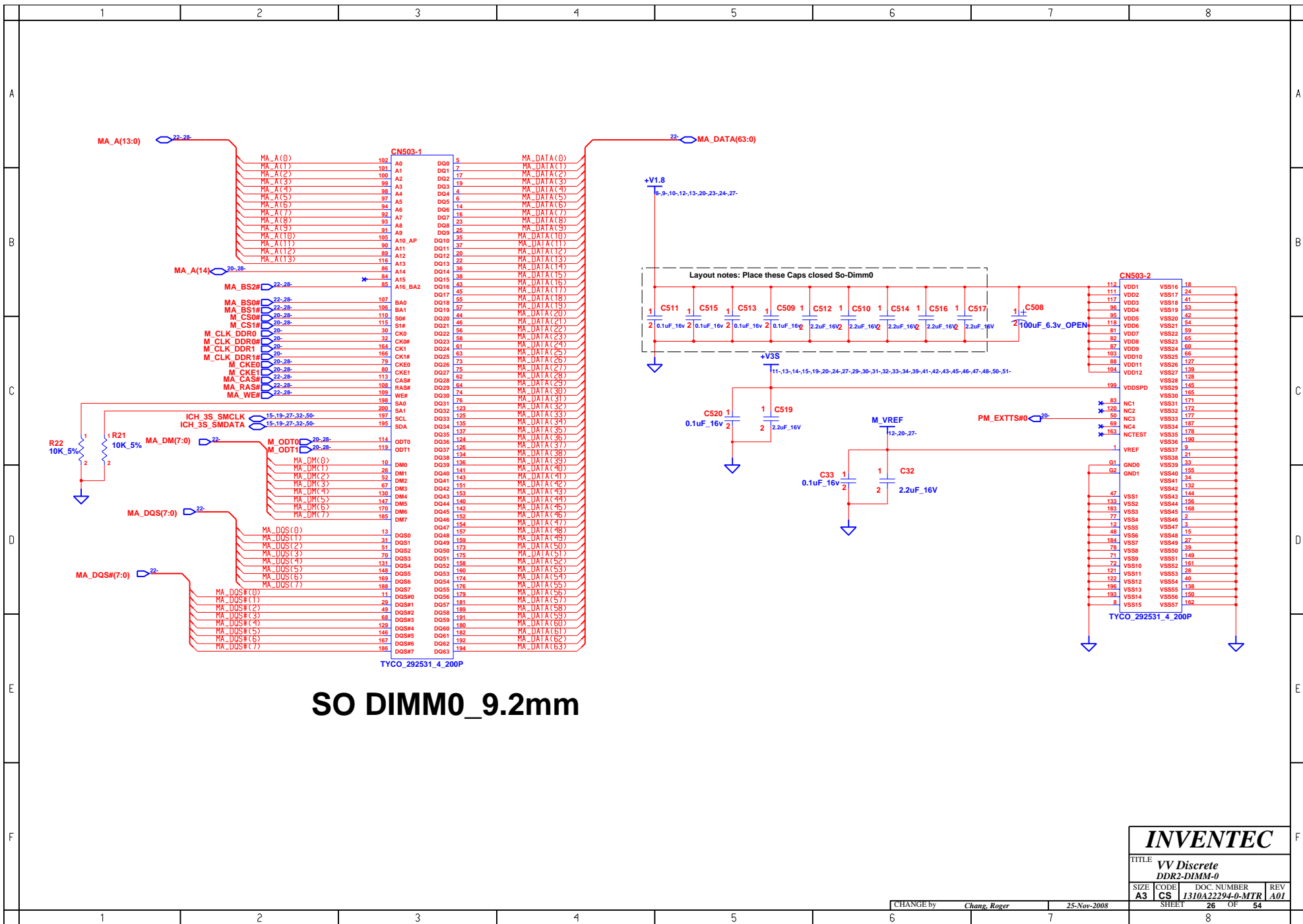


INVENTEC

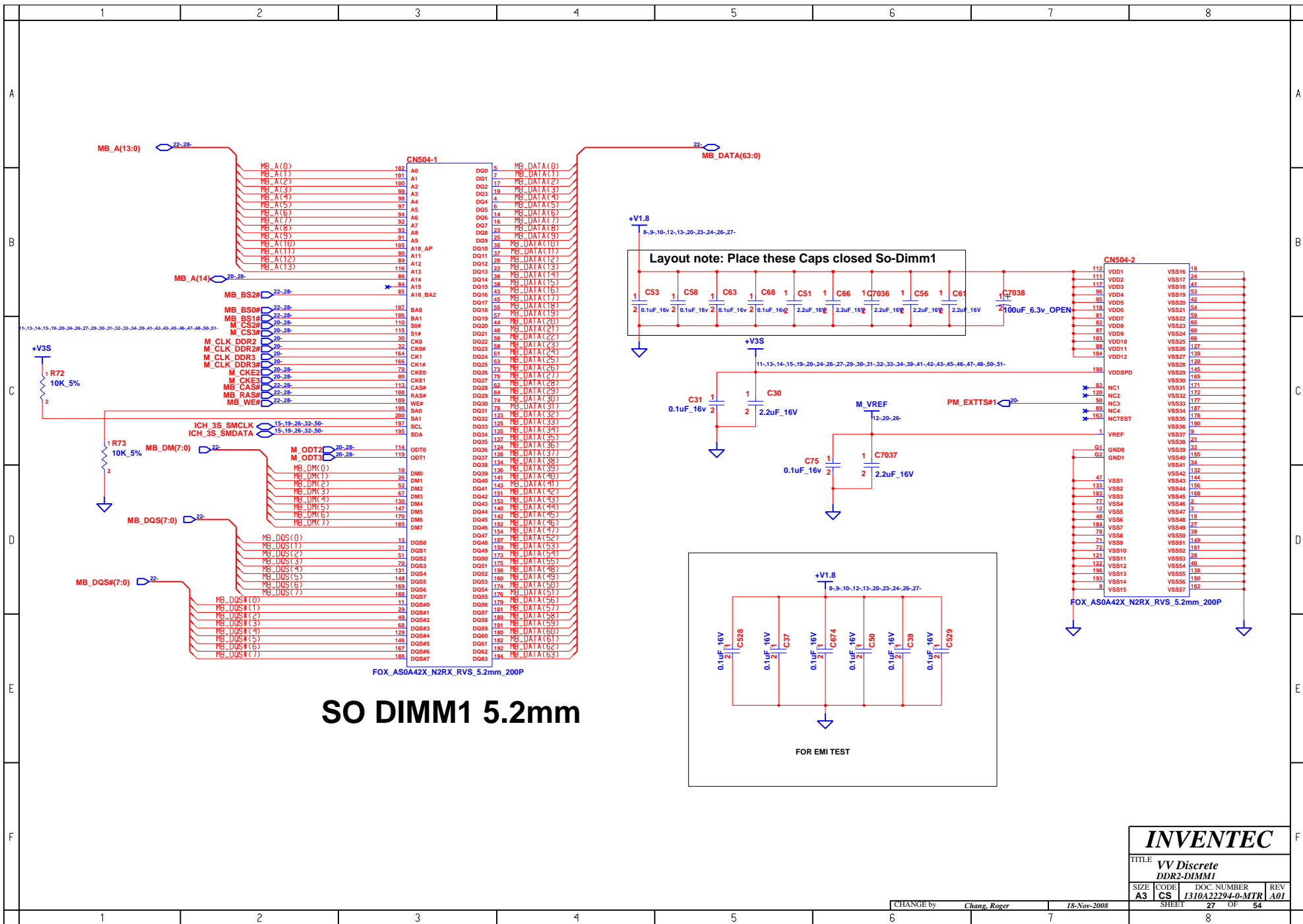
TITLE: VV Discrete
CRESTLINE-4

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

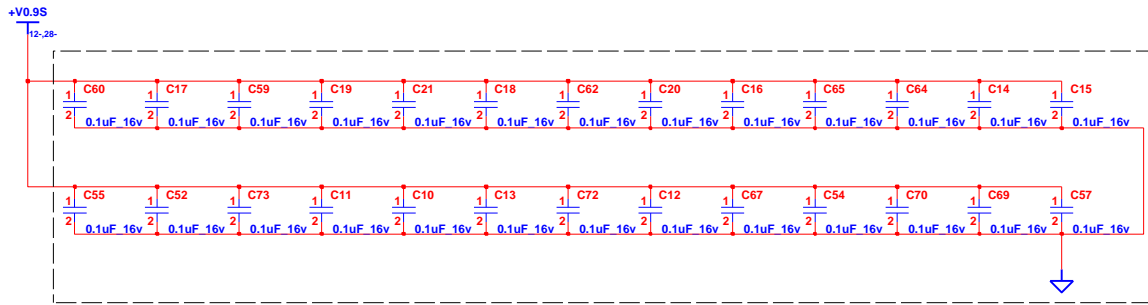
SHEET 23 OF 54



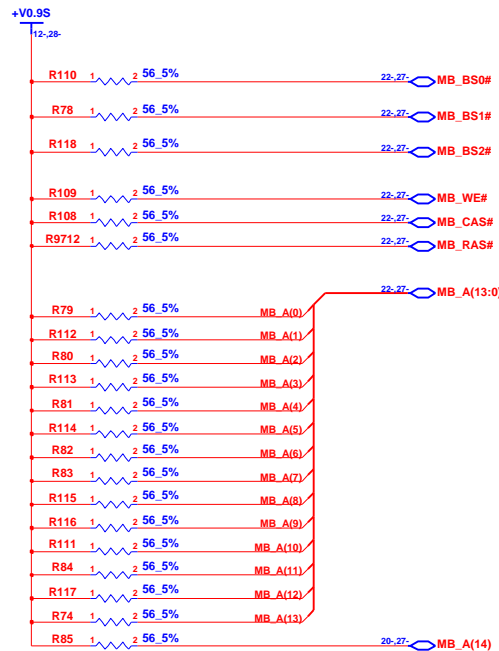
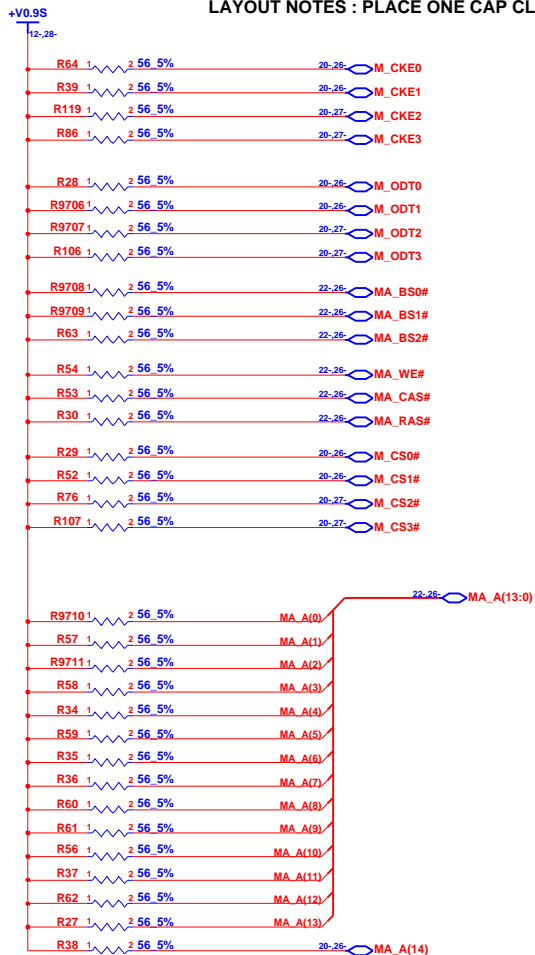
INVENTEC			
TITLE VV Discrete DDR2-DIMM-0			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		25-Nov-2008	
SHEET 26		OF 54	



INVENTEC			
TITLE: VV Discrete DDR2-DIMM1			
SIZE: A3	CODE: CS	DOC NUMBER: 1310A22294-0-MTR	REV: A01
CHANGE by: <i>Chang, Roger</i>		18-Nov-2008	
SHEET: 27		OF: 54	



LAYOUT NOTES : PLACE ONE CAP CLOSE TO EVERY 2 PULL UP RESISTOR TERMINATED TO +V0.9S

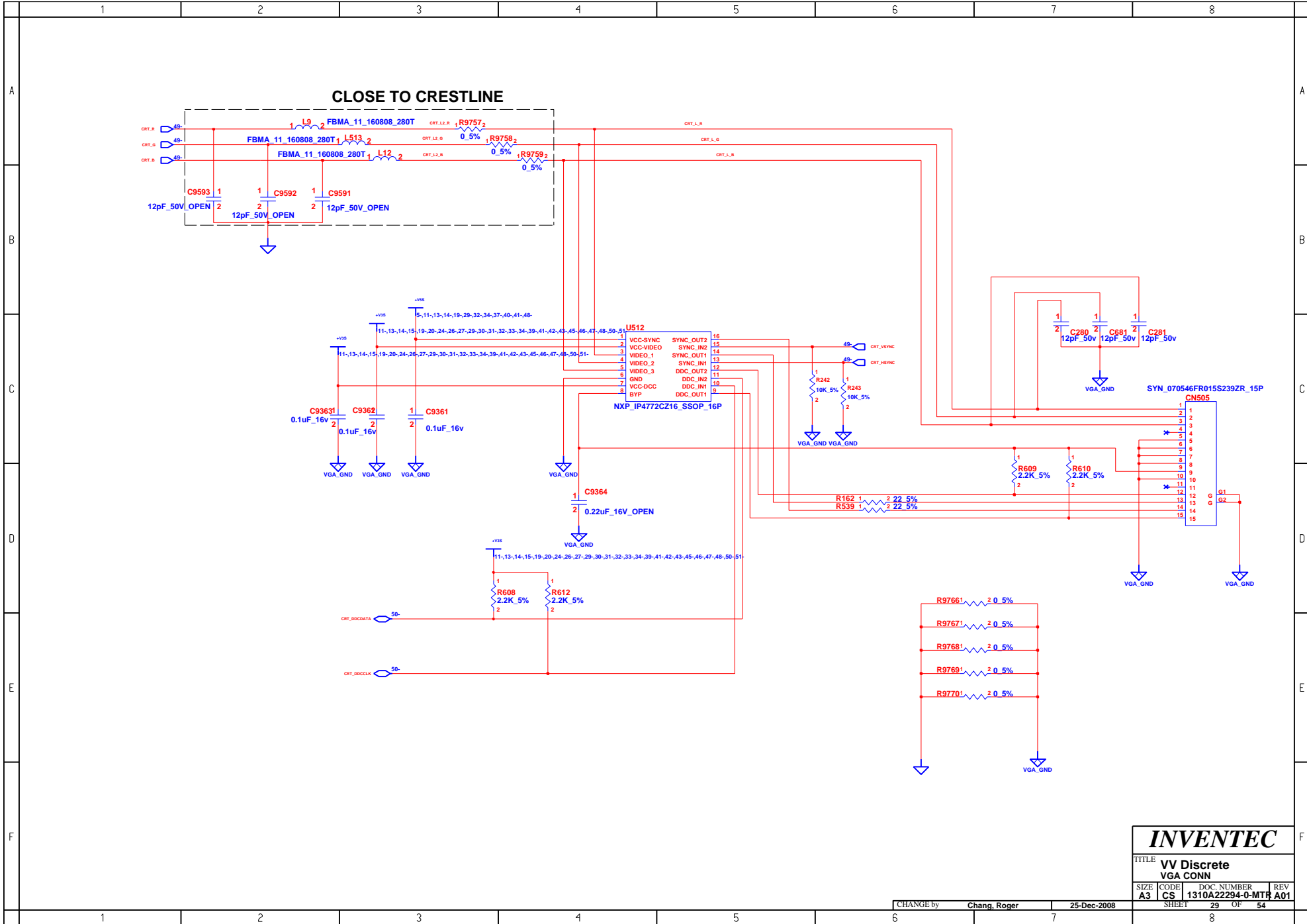


INVENTEC

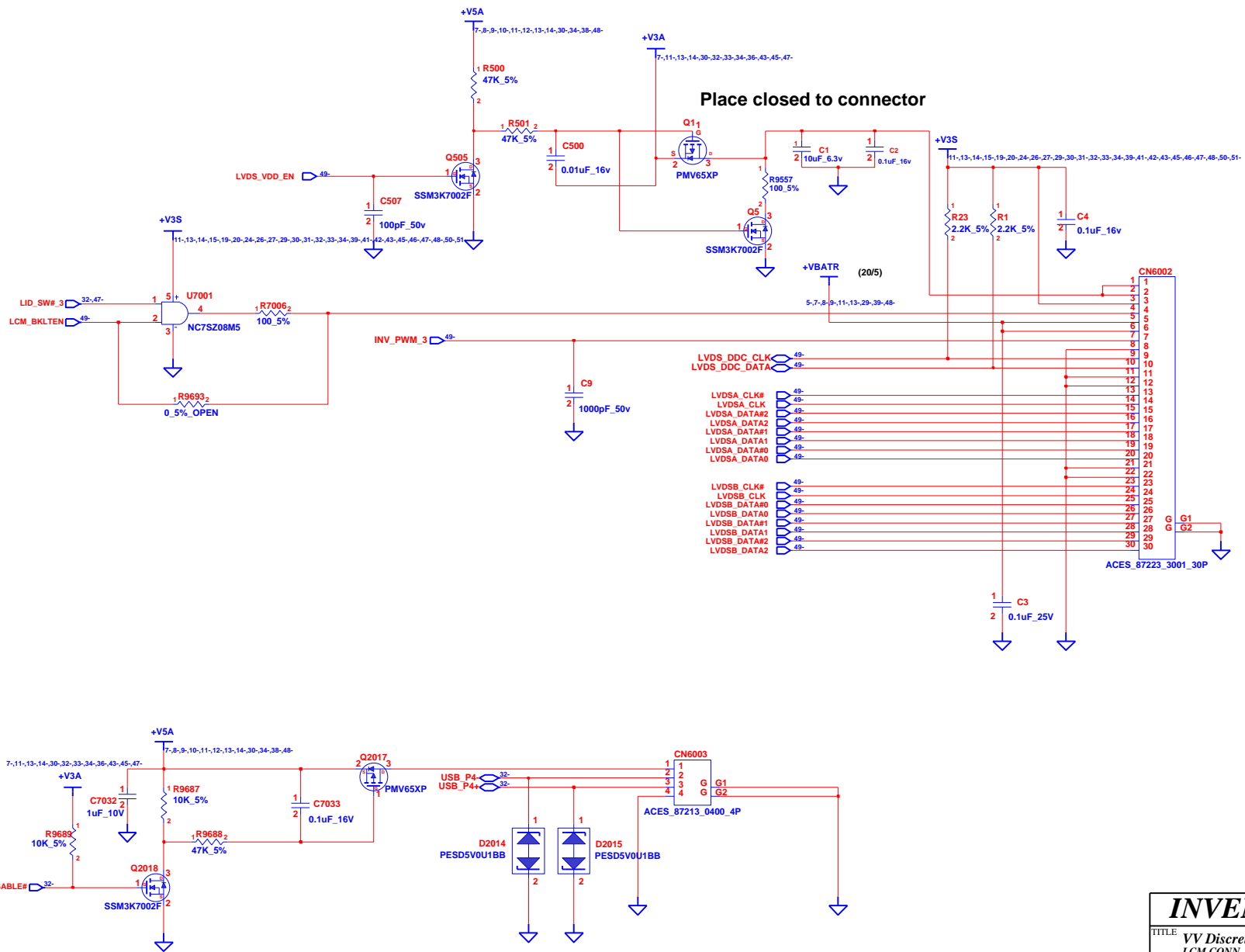
TITLE
**VV Discrete
 DDR2-DAMPING**

SIZE A3	CODE CS	DOC NUMBER I310A22294-0-MTRAO1	REV
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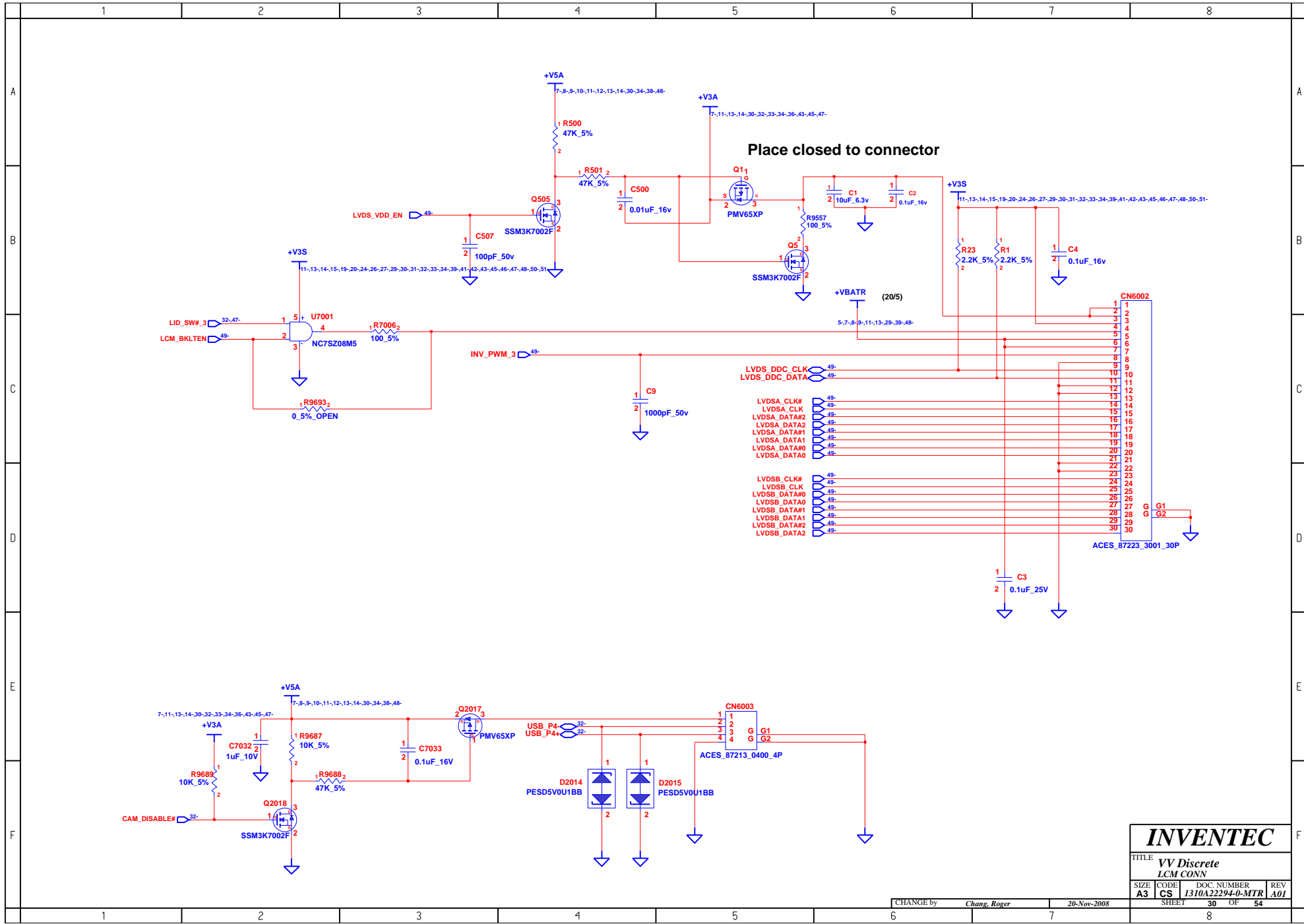
CHANGE by **Chang, Roger** 27-Sep-2003

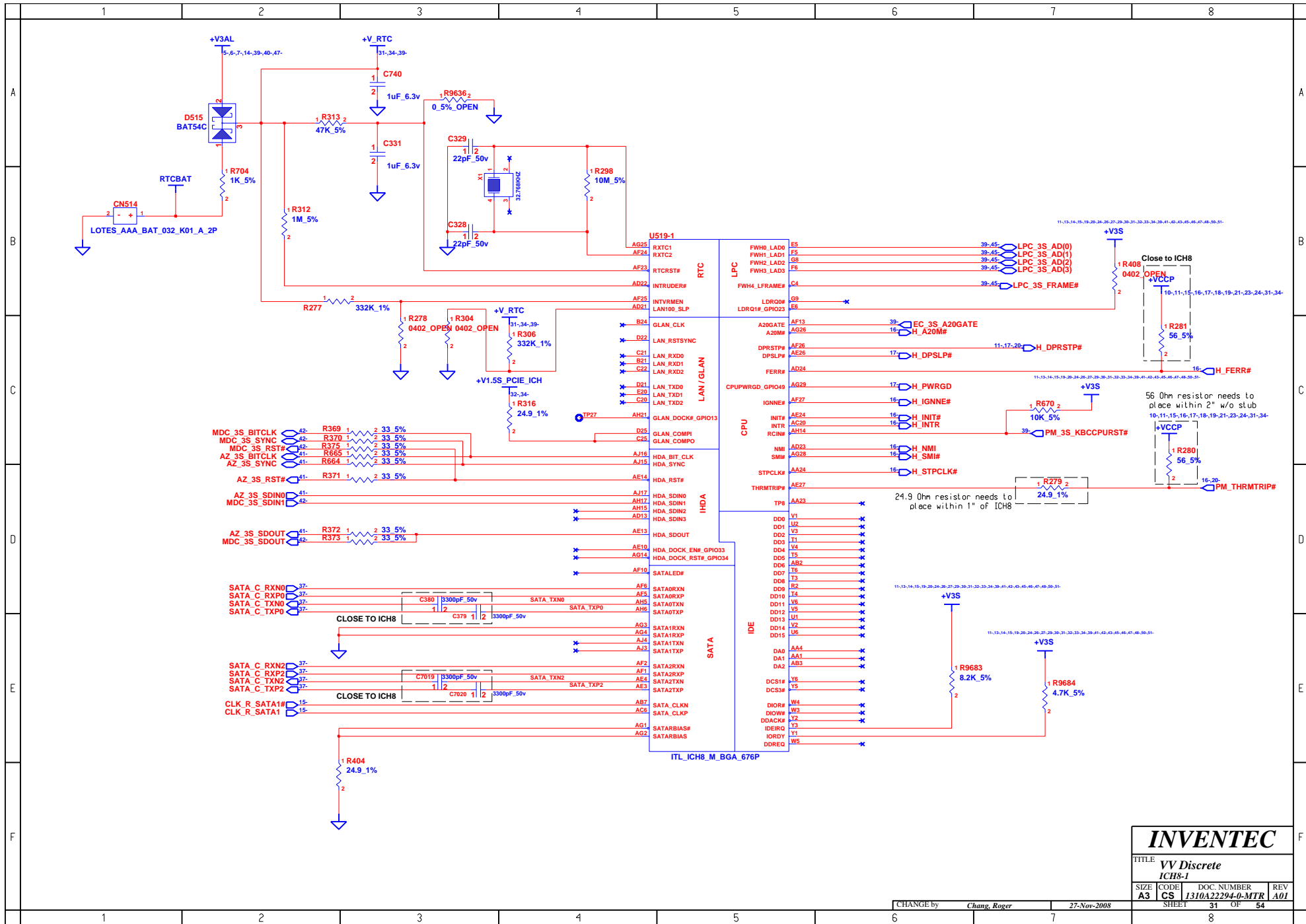


INVENTEC			
TITLE VV Discrete VGA CONN			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger		25-Dec-2008	
SHEET 29		OF 54	



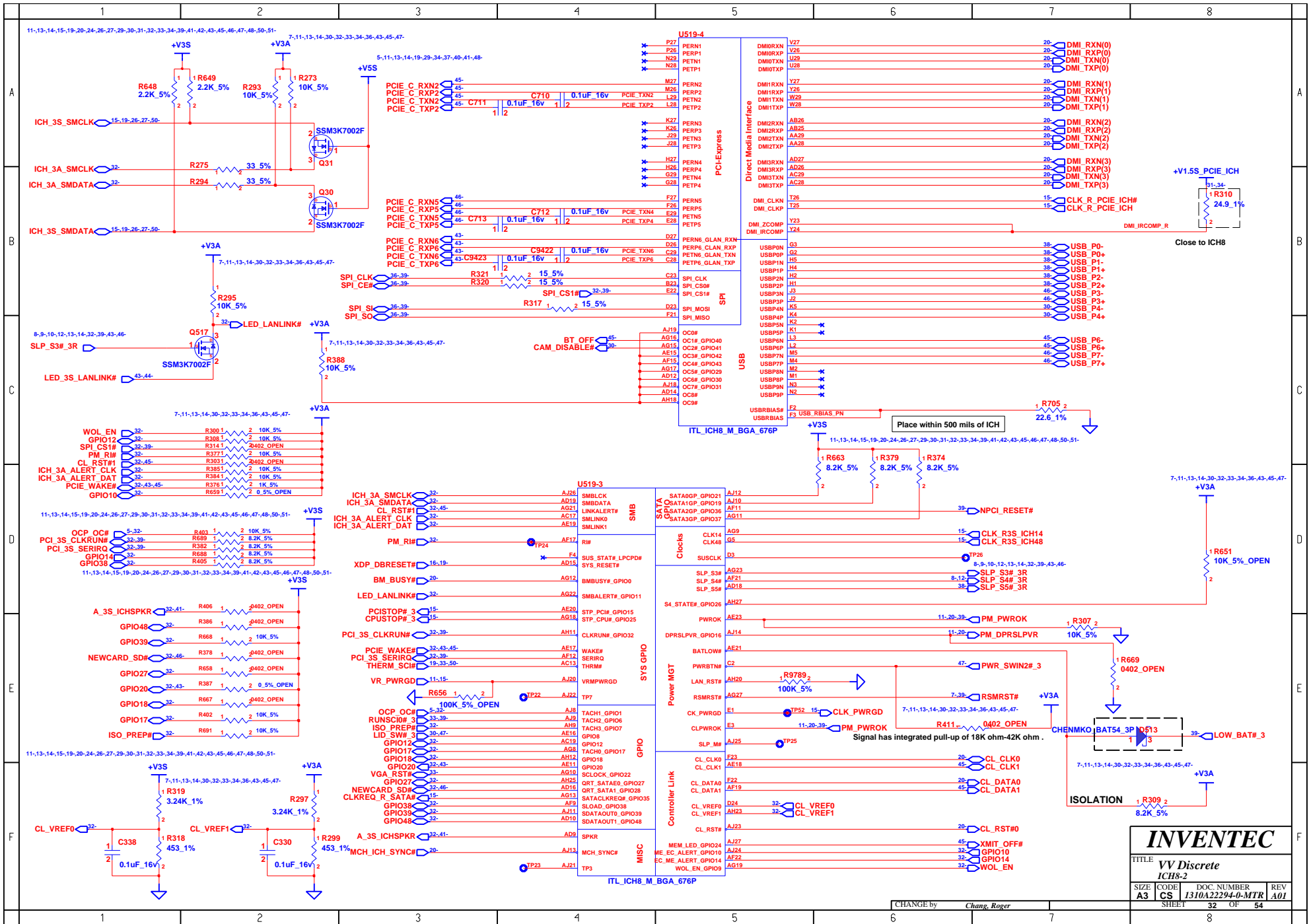
INVENTEC			
TITLE VV Discrete LCM CONN			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		20-Nov-2008	
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INVENTEC			
TITLE VV Discrete ICH8-1			
SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
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CHANGE by *Chang, Roger* 27-Nov-2008



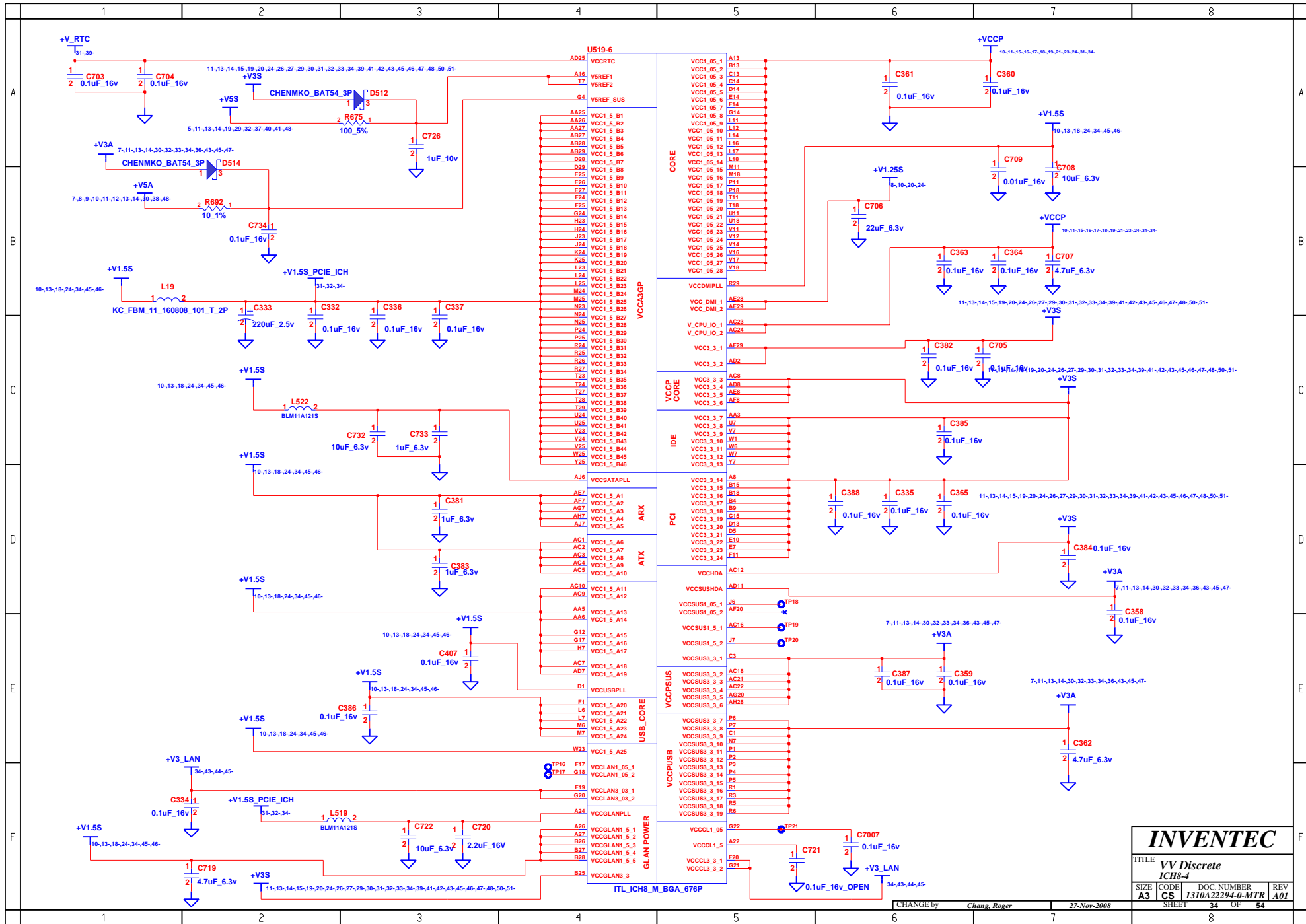
INVENTEC

TITLE **VV Discrete ICH8-2**

SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
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SHEET 32	OF 54
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CHANGE by *Chang, Roger*



INVENTEC

TITLE *VV Discrete ICH8-4*

SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
SHEET 34		OF 54	

CHANGE by *Chang, Roger* 27-Nov-2008

	1	2	3	4	5	6	7	8	
A									
B									
C									
D									
E									
F									

U519-5

A21	VSS001	VSS099	K7
AA	VSS002	VSS100	L1
AA2	VSS003	VSS101	L13
AA7	VSS004	VSS102	L15
AA8	VSS005	VSS103	L26
AB1	VSS006	VSS104	L27
AB24	VSS007	VSS105	L4
AC11	VSS008	VSS106	L5
AC14	VSS009	VSS107	M12
AC25	VSS010	VSS108	M13
AC28	VSS011	VSS109	M14
AC27	VSS012	VSS110	M15
AD11	VSS013	VSS111	M16
AD20	VSS014	VSS112	M17
AD23	VSS015	VSS113	M23
AD29	VSS016	VSS114	M28
AD3	VSS017	VSS115	M29
AD4	VSS018	VSS116	M3
AD5	VSS019	VSS117	N1
AE1	VSS020	VSS118	N11
AE15	VSS021	VSS119	N12
AE2	VSS022	VSS120	N13
AE22	VSS023	VSS121	N14
AD1	VSS024	VSS122	N15
AE24	VSS025	VSS123	N16
AE3	VSS026	VSS124	N17
AE5	VSS027	VSS125	N18
AE9	VSS028	VSS126	N26
AF14	VSS029	VSS127	N27
AF16	VSS030	VSS128	N4
AF18	VSS031	VSS129	N5
AF3	VSS032	VSS130	N6
AF4	VSS033	VSS131	P12
AG5	VSS034	VSS132	P13
AG6	VSS035	VSS133	P14
AH10	VSS036	VSS134	P15
AH13	VSS037	VSS135	P16
AH16	VSS038	VSS136	P17
AH19	VSS039	VSS137	P23
AH2	VSS040	VSS138	P28
AF23	VSS041	VSS139	P29
AH22	VSS042	VSS140	R11
AH24	VSS043	VSS141	R12
AH25	VSS044	VSS142	R13
AH3	VSS045	VSS143	R14
AH4	VSS046	VSS144	R15
AH5	VSS047	VSS145	R16
AH5	VSS048	VSS146	R17
B11	VSS049	VSS147	R18
B14	VSS050	VSS148	R28
B17	VSS051	VSS149	R4
B3	VSS052	VSS150	T12
B20	VSS053	VSS151	T13
B22	VSS054	VSS152	T14
B5	VSS055	VSS153	T15
C24	VSS056	VSS154	T16
C28	VSS057	VSS155	T17
C27	VSS058	VSS156	T2
C5	VSS059	VSS157	U12
D12	VSS060	VSS158	U13
D15	VSS061	VSS159	U14
D18	VSS062	VSS160	U15
D3	VSS063	VSS161	U16
D4	VSS064	VSS162	U17
E21	VSS065	VSS163	U23
E24	VSS066	VSS164	U26
E4	VSS067	VSS165	U27
E9	VSS068	VSS166	U3
F14	VSS069	VSS167	U5
E24	VSS070	VSS168	V13
F24	VSS071	VSS169	V15
F29	VSS072	VSS170	V28
F7	VSS073	VSS171	V29
G1	VSS074	VSS172	W2
E3	VSS075	VSS173	W26
G10	VSS076	VSS174	W27
G13	VSS077	VSS175	Y28
G19	VSS078	VSS176	Y29
G25	VSS079	VSS177	Y4
G25	VSS080	VSS178	AB4
G25	VSS081	VSS179	AB23
G27	VSS082	VSS180	AB5
H25	VSS083	VSS181	AB6
H28	VSS084	VSS182	AD5
H29	VSS085	VSS183	U4
H3	VSS086	VSS184	W24
HE	VSS087	VSS_NCTF_01	A1
J1	VSS088	VSS_NCTF_02	A2
J26	VSS089	VSS_NCTF_03	A28
J26	VSS090	VSS_NCTF_04	A29
J27	VSS091	VSS_NCTF_05	AH1
J4	VSS092	VSS_NCTF_06	AH29
J4	VSS093	VSS_NCTF_07	AJ1
K25	VSS094	VSS_NCTF_08	AJ2
K29	VSS095	VSS_NCTF_09	AJ28
K29	VSS096	VSS_NCTF_10	AJ29
K3	VSS097	VSS_NCTF_11	B1
K3	VSS098	VSS_NCTF_12	B29

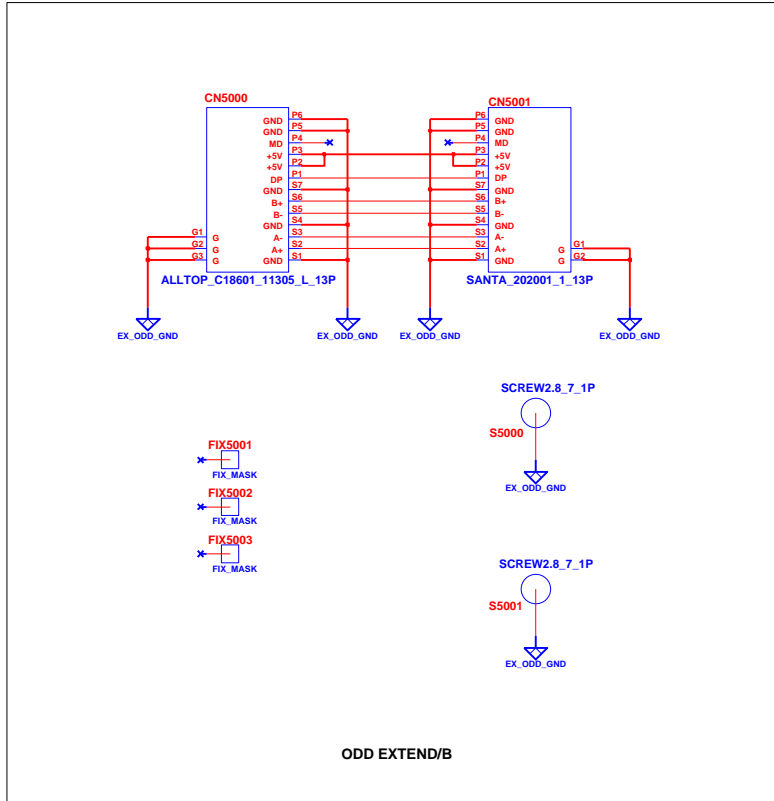
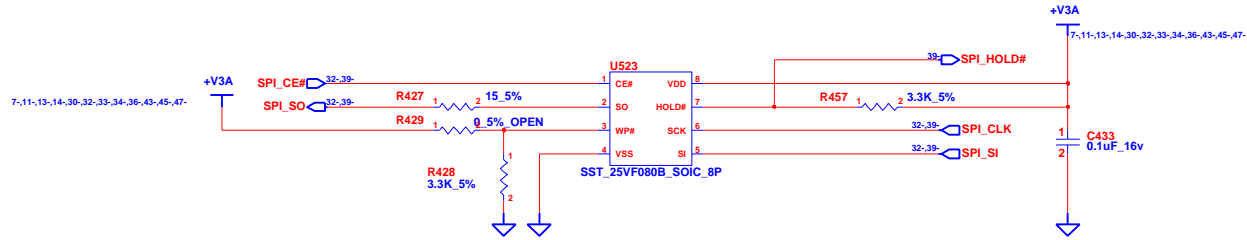
ITL_ICH8_M_BGA_676P

INVENTEC

TITLE **VV Discrete**
ICH8-5

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

SHEET 35 OF 54



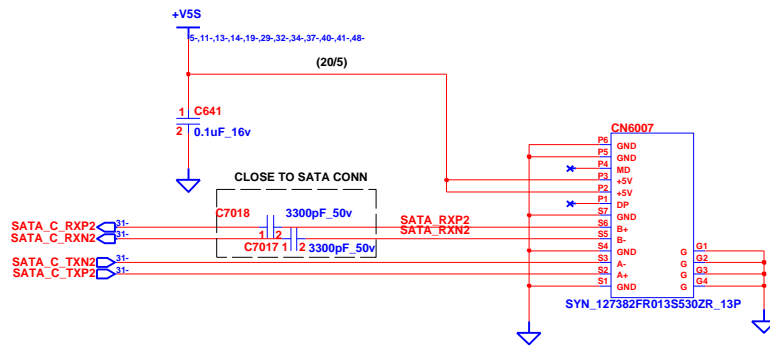
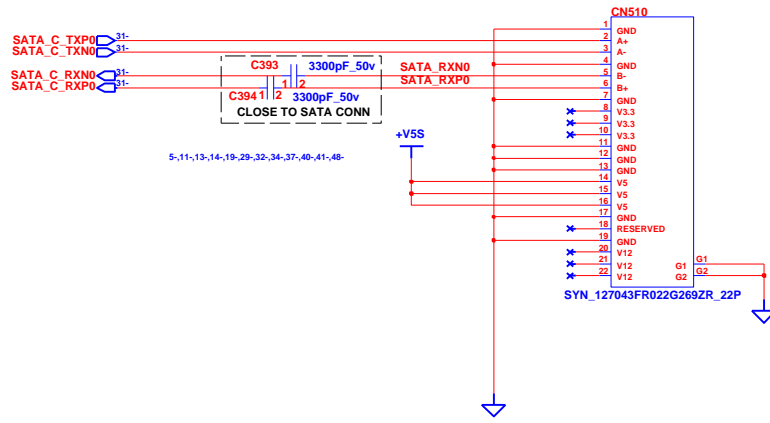
INVENTEC

TITLE **VV Discrete SYSTEM BIOS**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

CHANGE by *Chang, Roger* 27-Nov-2008

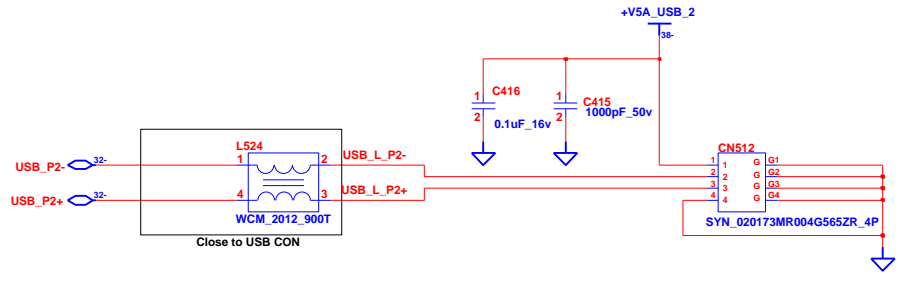
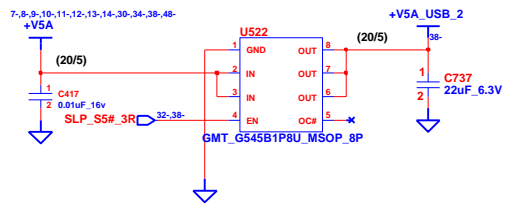
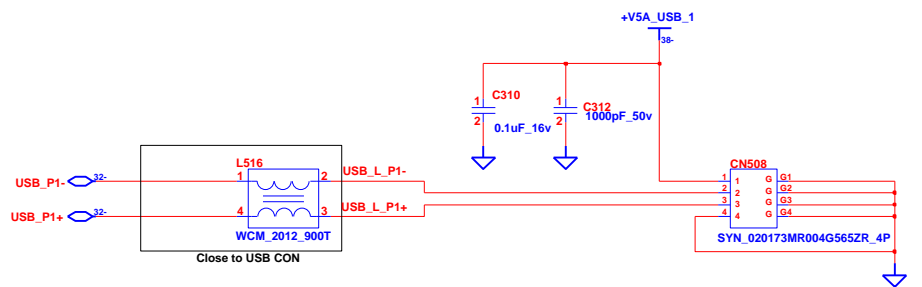
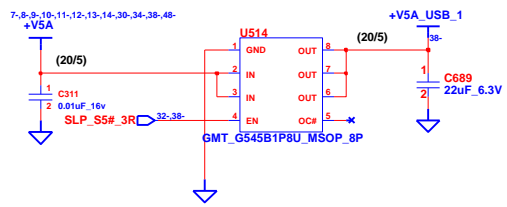
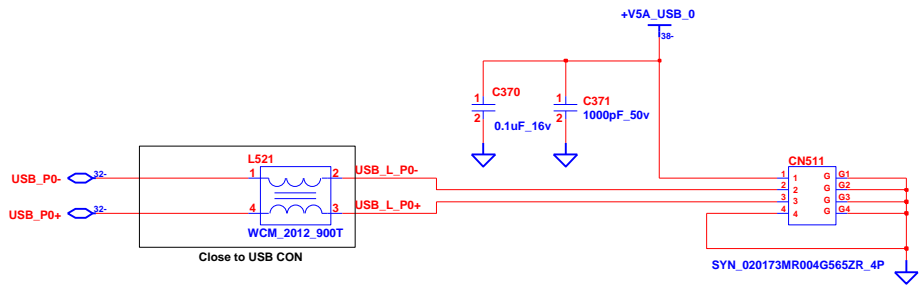
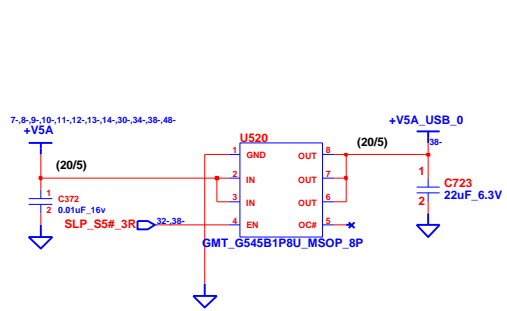
SHEET 36 OF 54



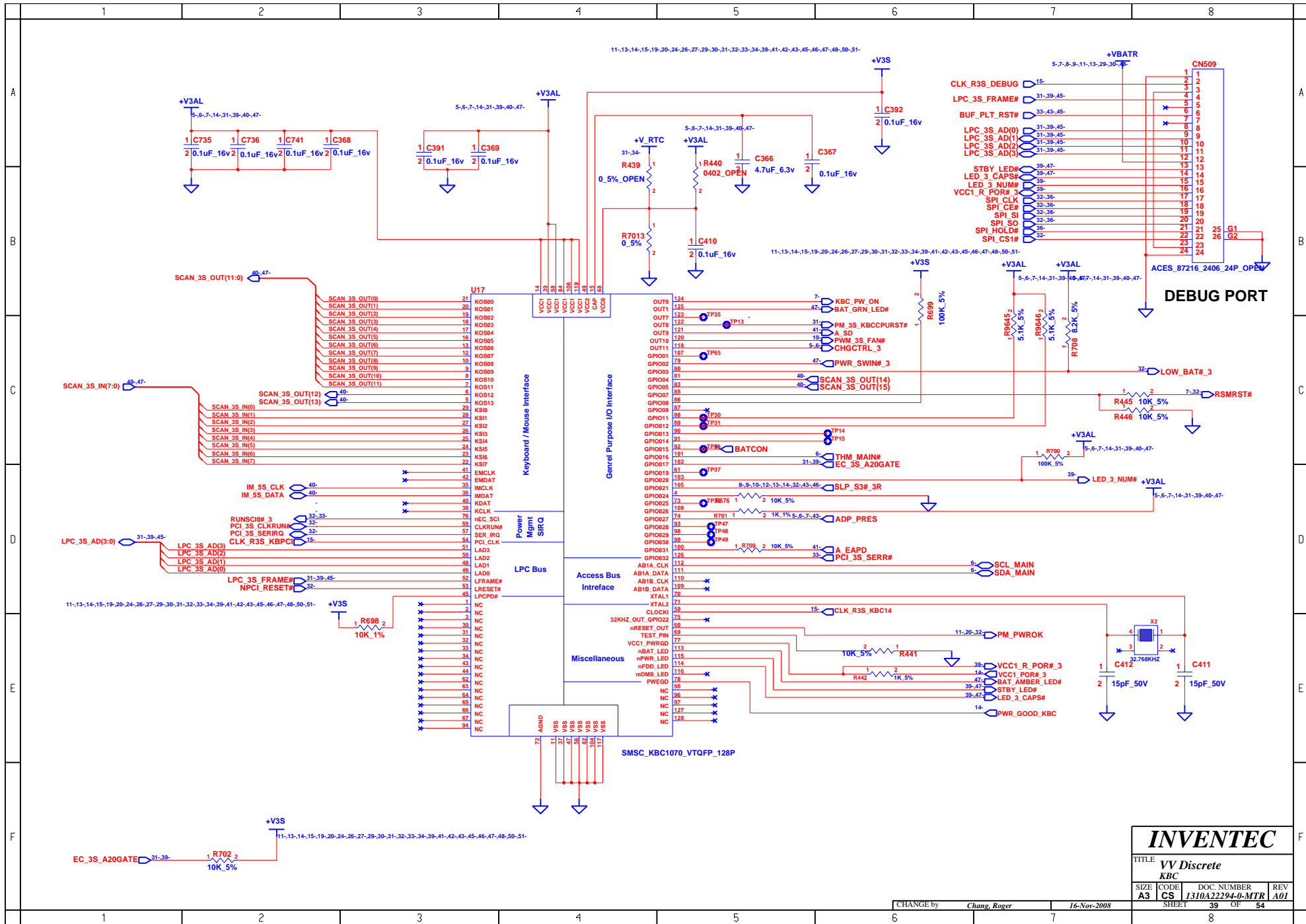
INVENTEC

TITLE			
VV Discrete			
HDD & ODD CONN			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01
SHEET		OF	
37		54	

CHANGE by Chang, Roger 18-Nov-2008

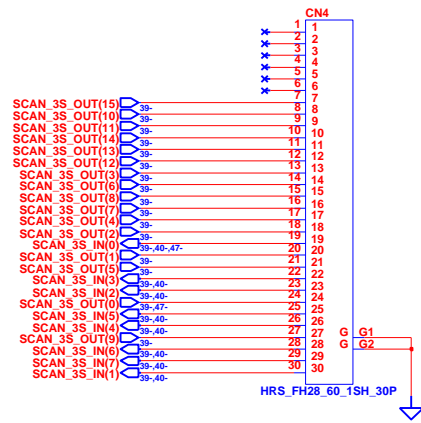


INVENTEC			
TITLE VV Discrete USB CONN			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		4-Nov-2008	
SHEET 38		OF 54	

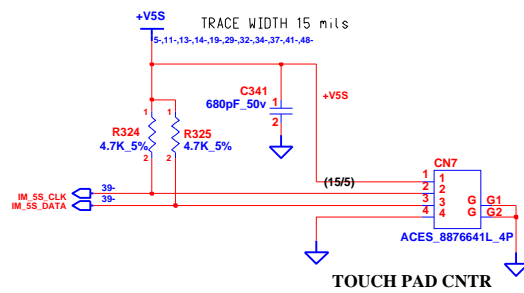
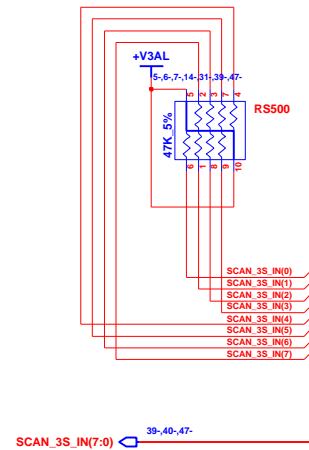


INVENTEC			
TITLE VV Discrete			
KBC			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
SHEET 39		OF 54	

CHANGE by *Chang, Roger* 16-Nov-2008

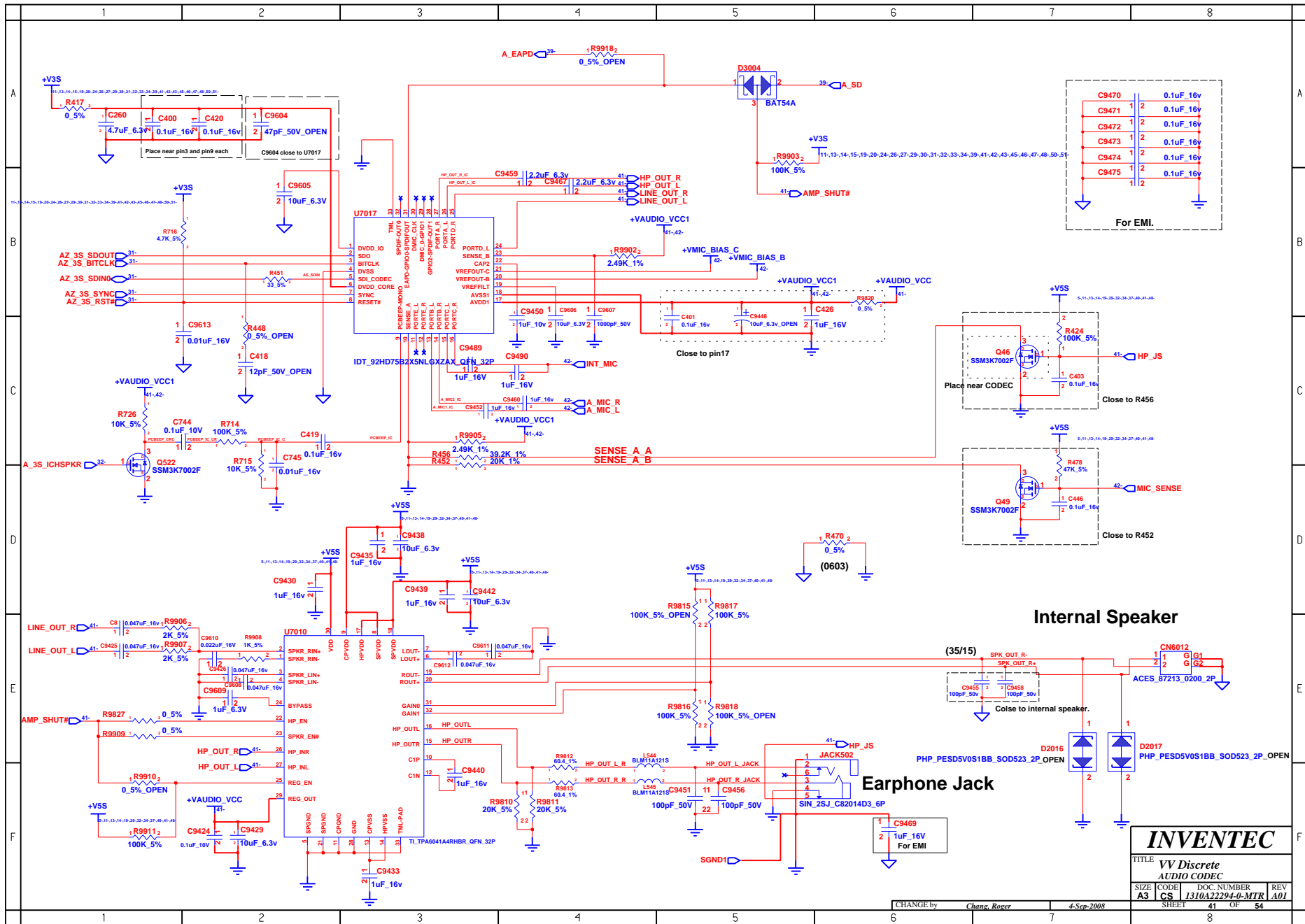


KEYBOARD CONN



TOUCH PAD CNTR

INVENTEC			
TITLE <i>VV Discrete</i> <i>KB & TP CONN</i>			
SIZE A3	CODE CS	DOC. NUMBER <i>1310A22294-0-MTR</i>	REV A01
CHANGE by <i>Chang, Roger</i>		15-Dec-2008	
SHEET 40		OF 54	



For EMI.

C9470	1	2	0.1uF_16v
C9471	1	2	0.1uF_16v
C9472	1	2	0.1uF_16v
C9473	1	2	0.1uF_16v
C9474	1	2	0.1uF_16v
C9475	1	2	0.1uF_16v

Place near CODEC

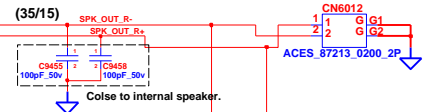
Q46	1	1	SSM3K7002F
R424	1	1	100K_5%
C403	1	2	0.1uF_16v

Close to R456

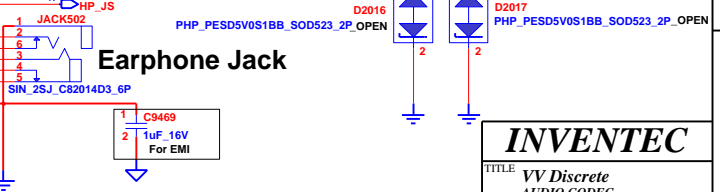
Close to R452

Q49	1	1	SSM3K7002F
R478	1	1	47K_5%
C446	1	2	0.1uF_16v

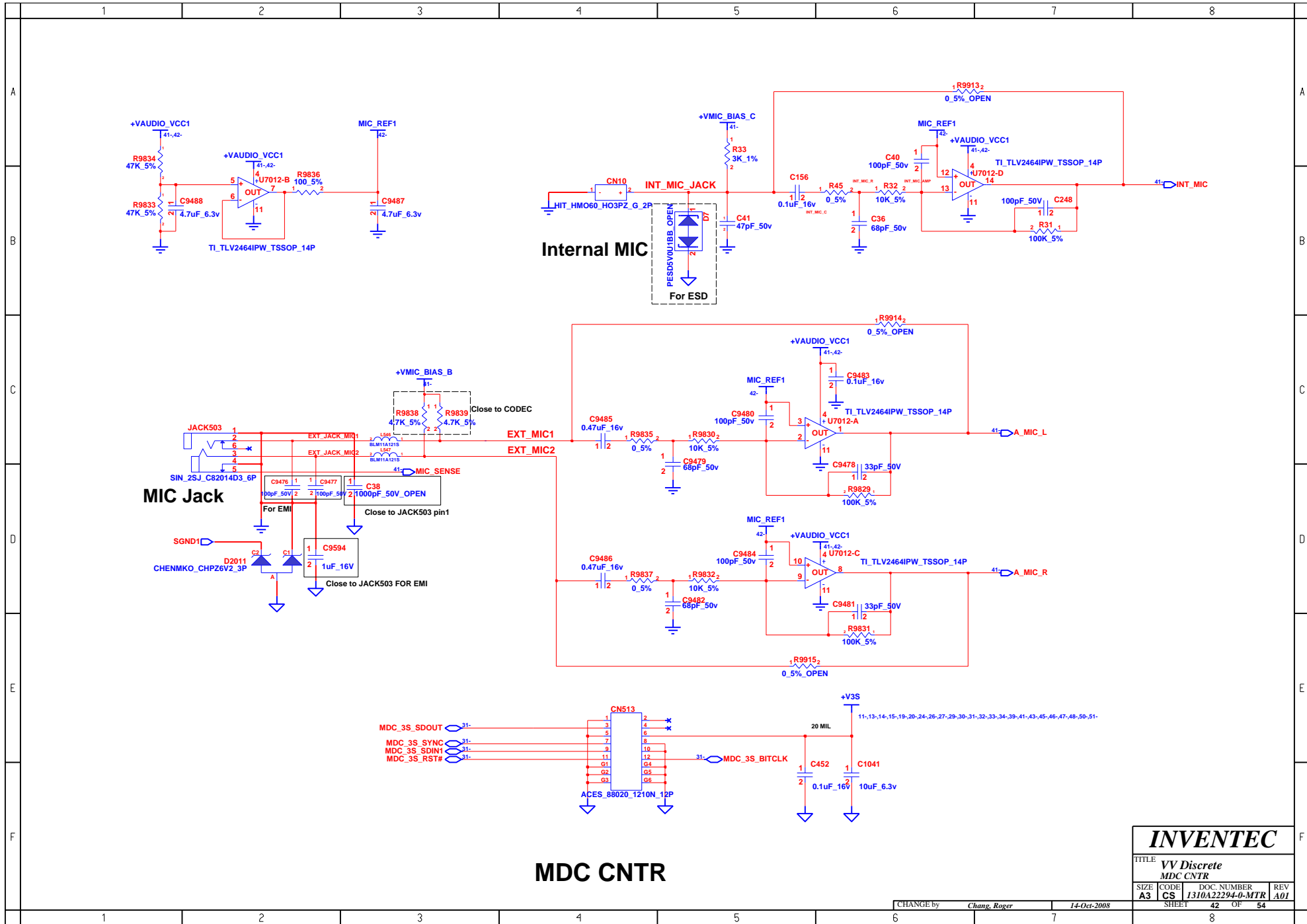
Internal Speaker



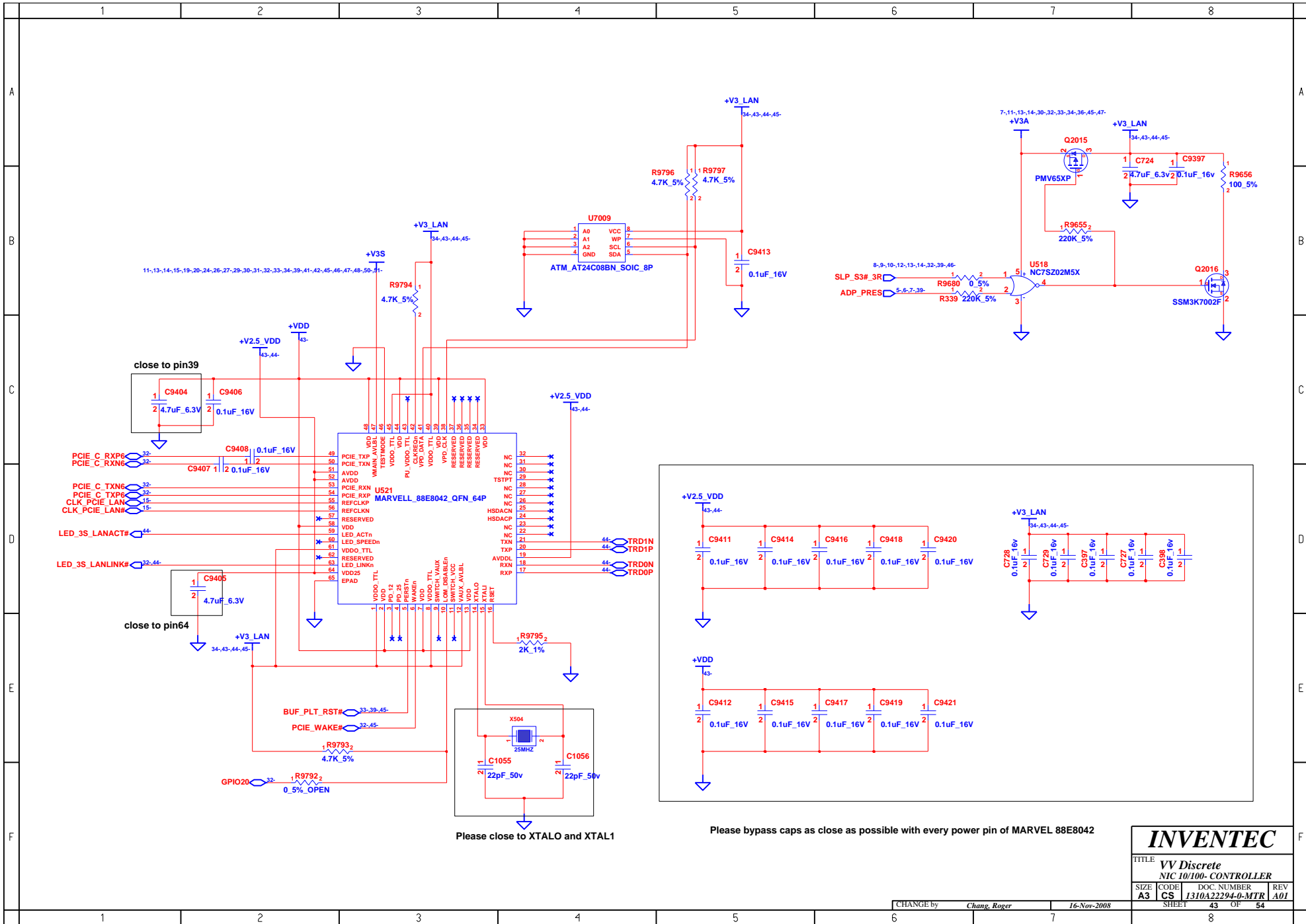
Earphone Jack



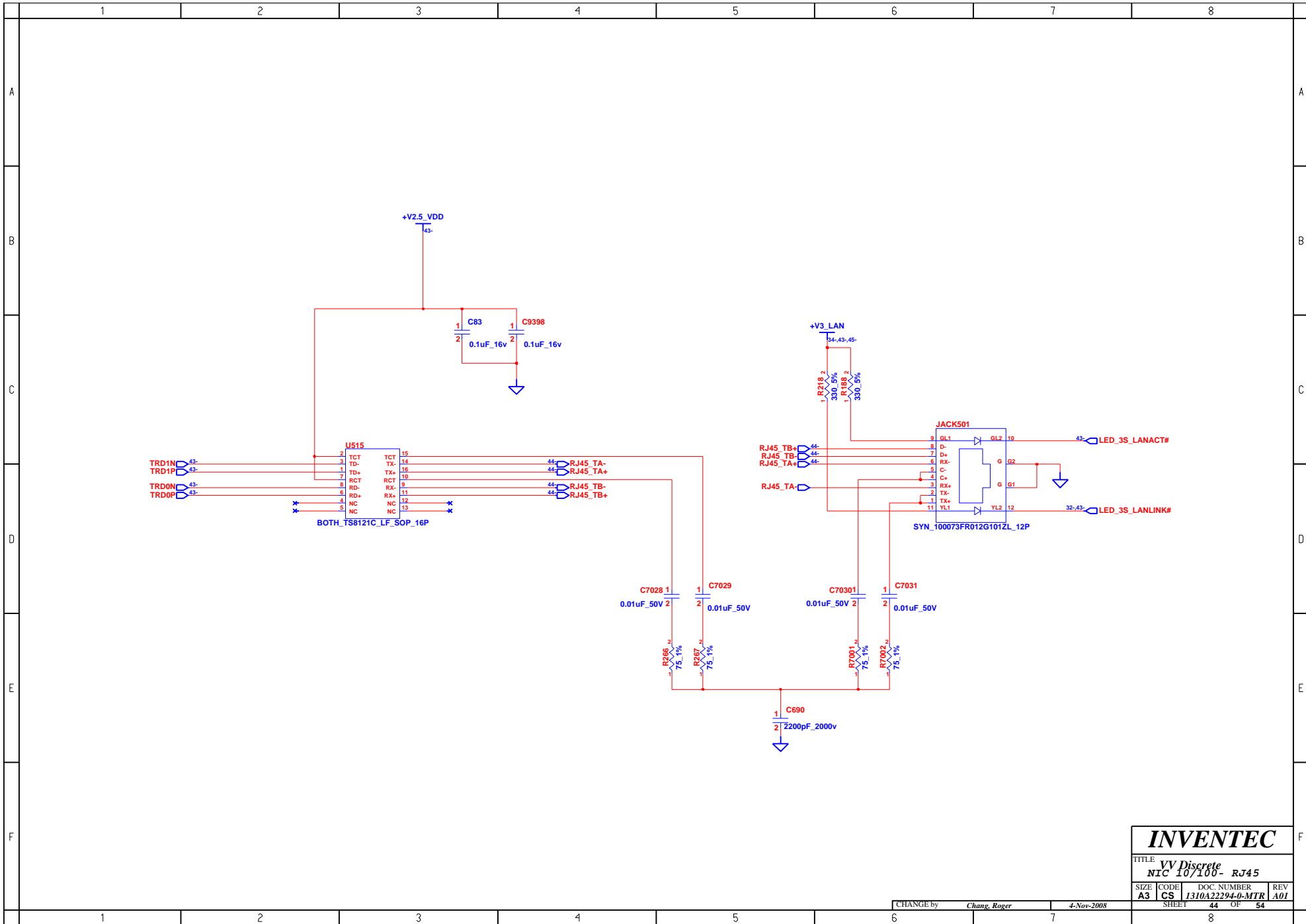
INVENTEC			
TITLE VV Discrete AUDIO CODEC			
SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger			4-Sep-2008
SHEET 41			OF 54



INVENTEC			
TITLE VV Discrete MDC CNTR			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger		14-Oct-2008	
SHEET 42		OF 54	



INVENTEC			
TITLE VV Discrete NIC 10/100- CONTROLLER			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by Chang, Roger		16-Nov-2008	SHEET 43 OF 54



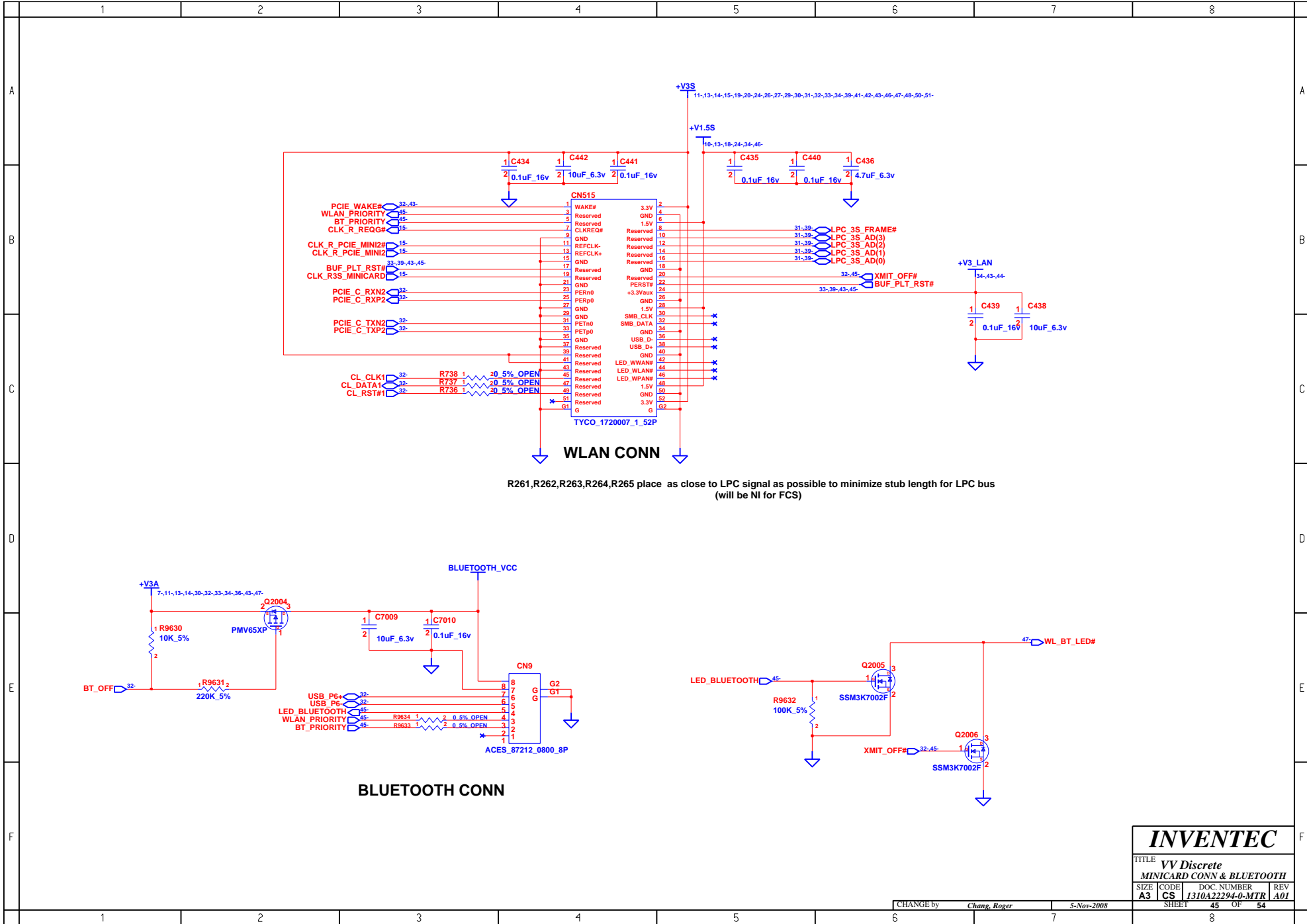
INVENTEC

TITLE *VV Discrete*
NIC 10/100 - RJ45

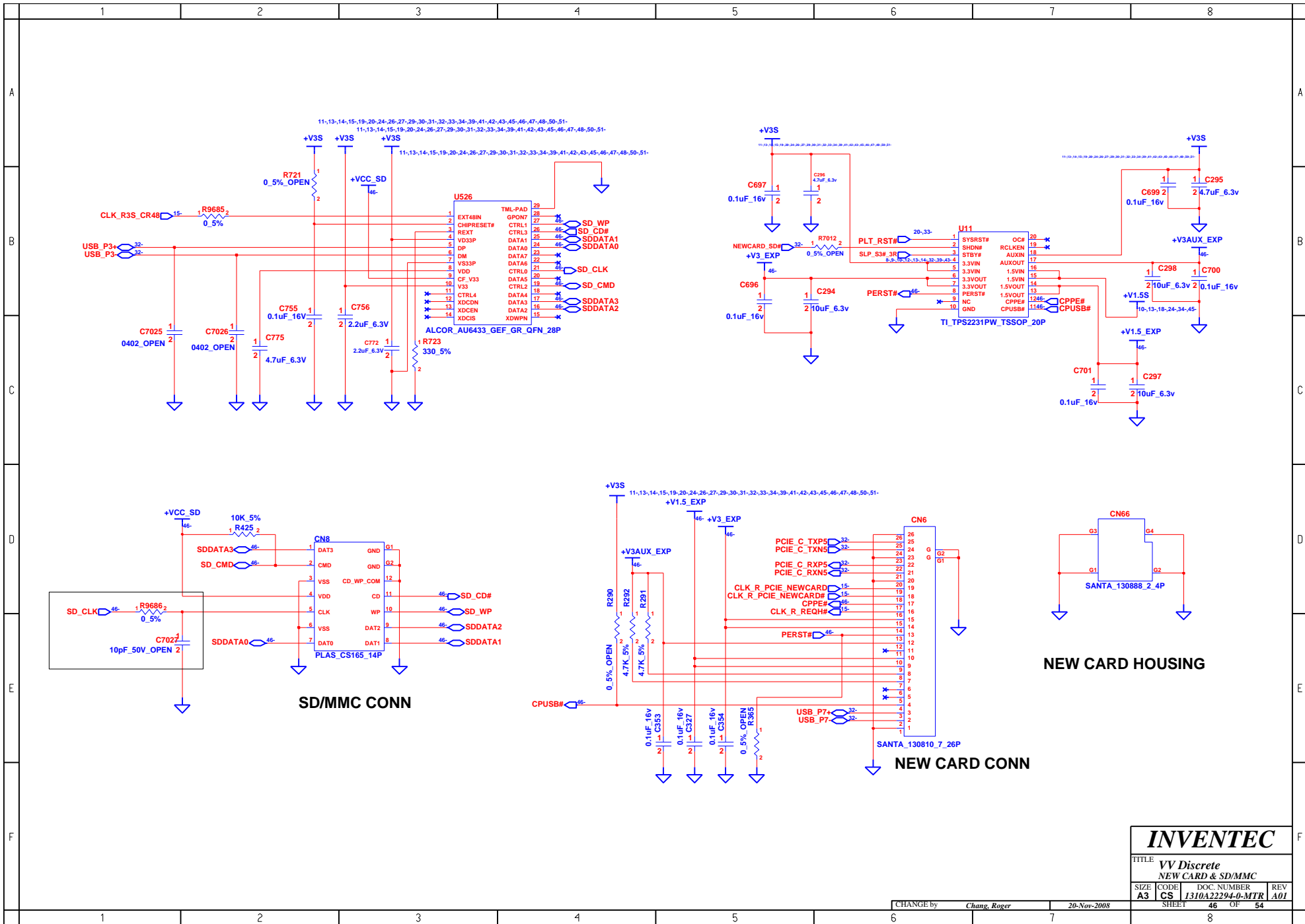
SIZE A3	CODE CS	DOC. NUMBER 1310A22294-0-MTR	REV A01
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CHANGE by *Chang, Roger* 4-Nov-2008

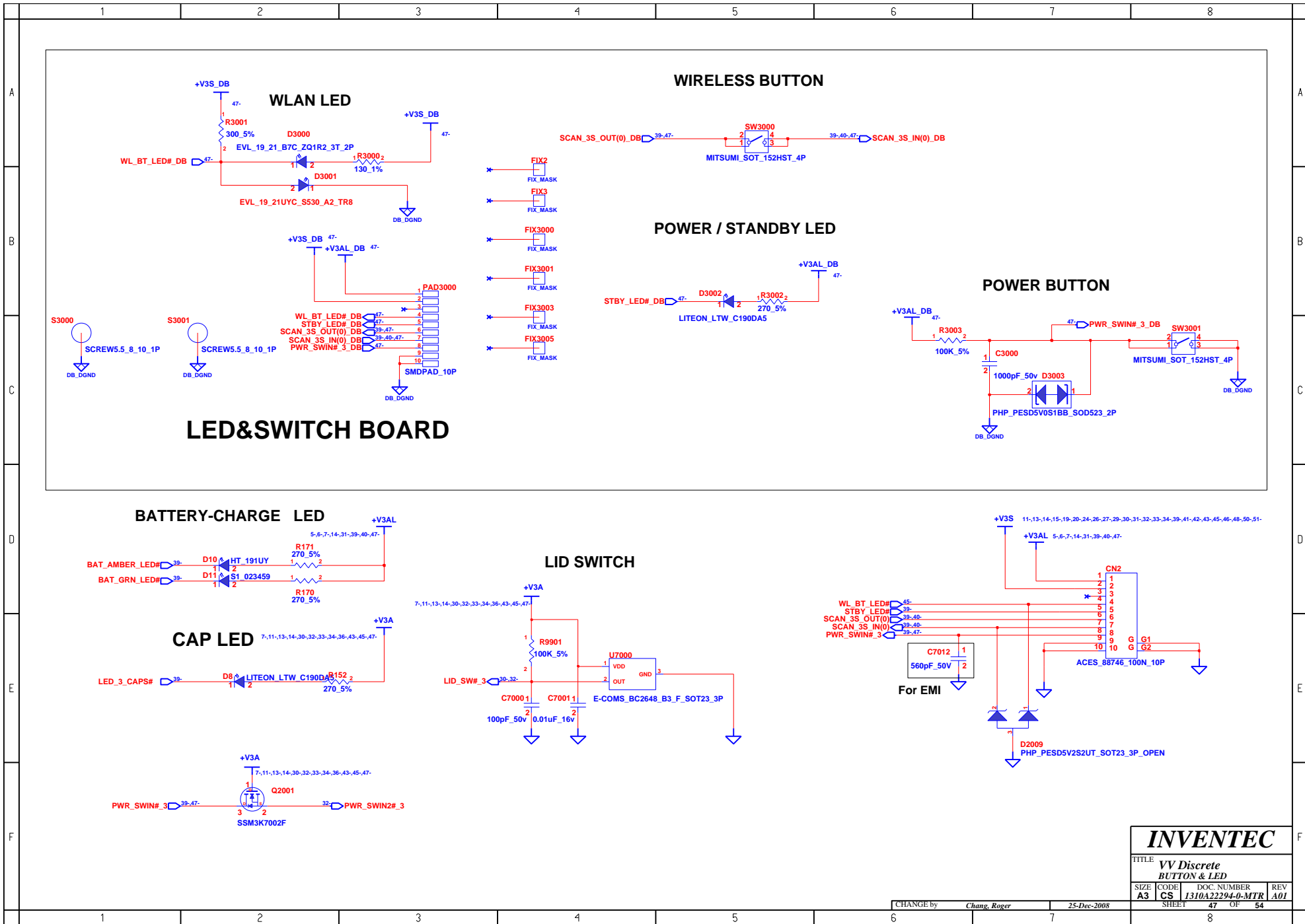
SHEET 44 OF 54



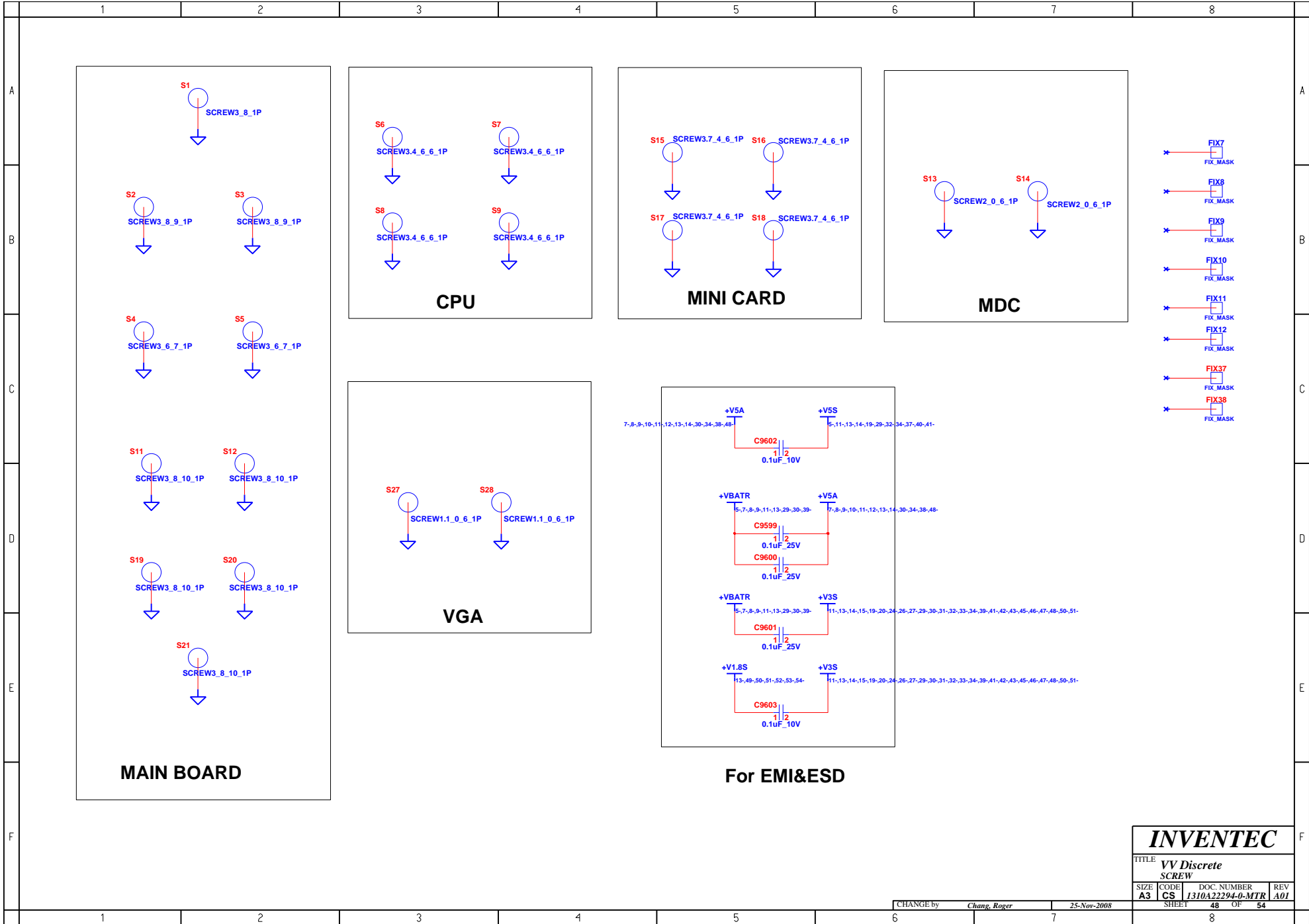
INVENTEC			
TITLE VV Discrete			
MINICARD CONN & BLUETOOTH			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01
CHANGE by <i>Chang, Roger</i>		5-Nov-2008	SHEET 45 OF 54



INVENTEC			
TITLE: VV Discrete NEW CARD & SD/MMC			
SIZE: A3	CODE: CS	DOC NUMBER: 1310A22294-0-MTR	REV: A01
CHANGE by: Chang, Roger		20-Nov-2008	
SHEET: 46		OF: 54	



INVENTEC			
TITLE VV Discrete BUTTON & LED			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		25-Dec-2008	
SHEET 47		OF 54	



INVENTEC			
TITLE VV Discrete SCREW			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
CHANGE by <i>Chang, Roger</i>		25-Nov-2008	
SHEET 48		OF 54	

STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIe full TX output swing.	0
TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enabled.	0
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT
 0 = DO NOT INSTALL RESISTOR
 1 = INSTALL 10K RESISTOR

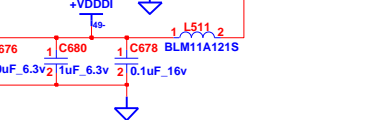
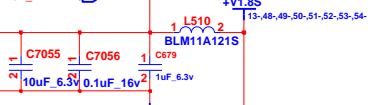
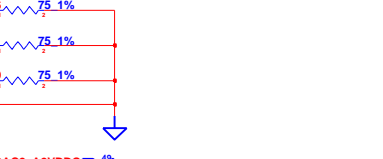
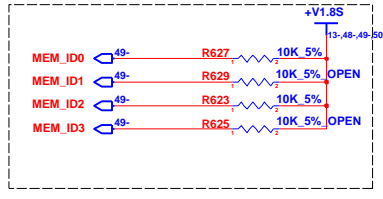
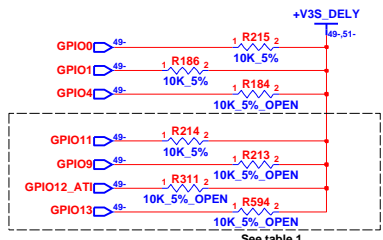
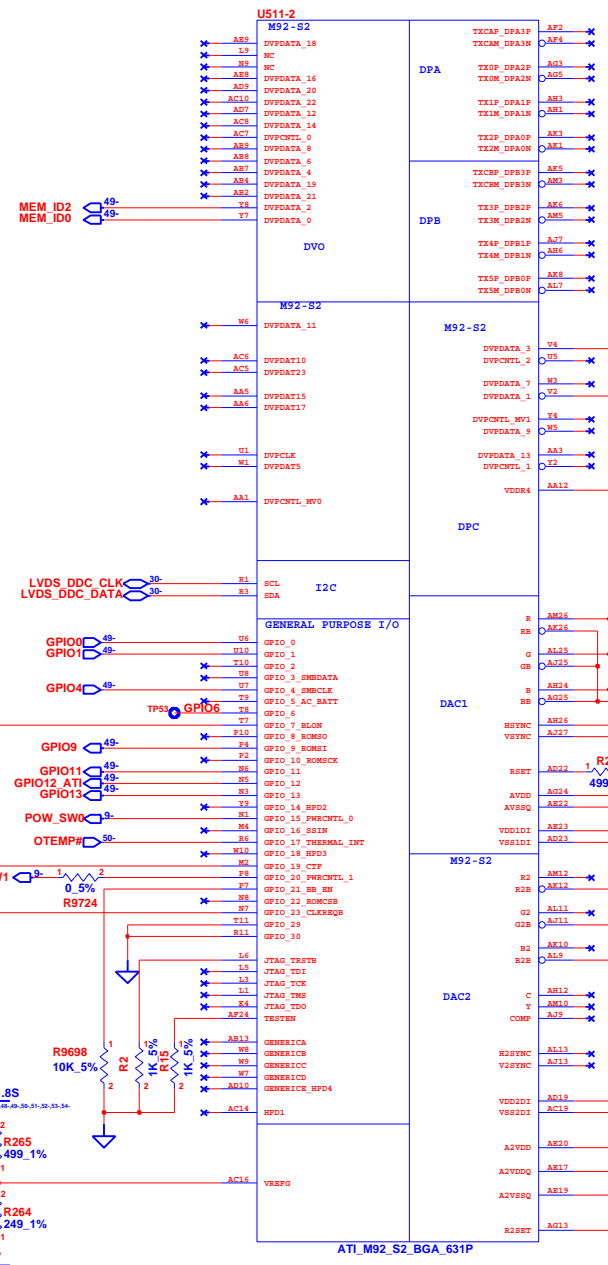
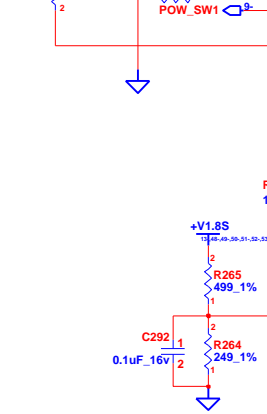
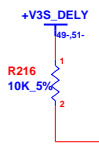
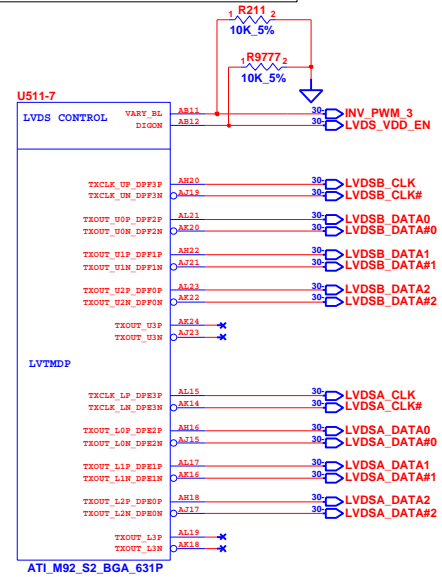
Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2
0	0	0	128M memory aperture
0	0	1	256M memory aperture (Default)
1	1	0	reserved

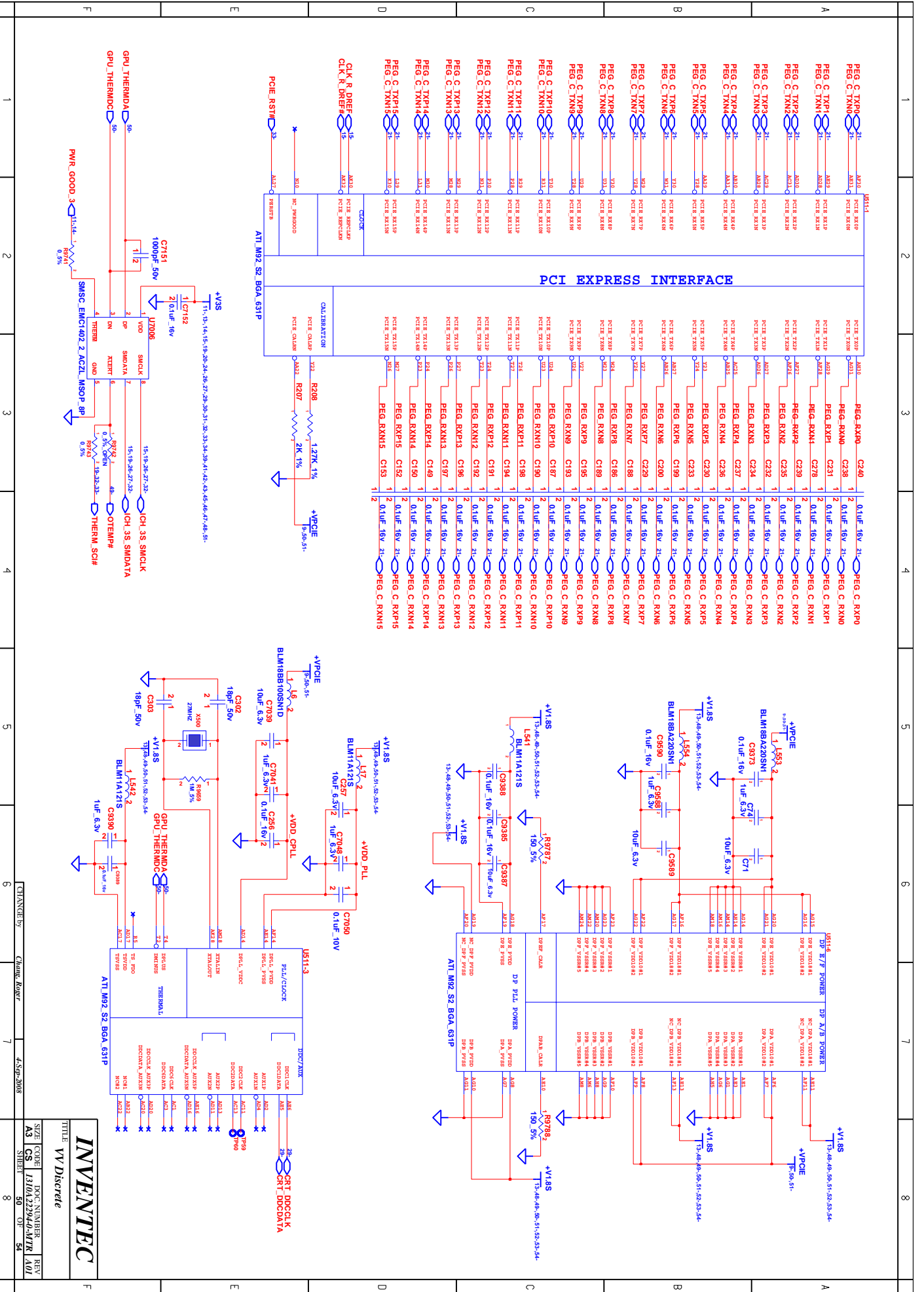
POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor
0	1	0	1	samsung (256MB)
0	1	1	0	Qimonda(256M) (Default)
0	1	1	1	hynix (256MB)

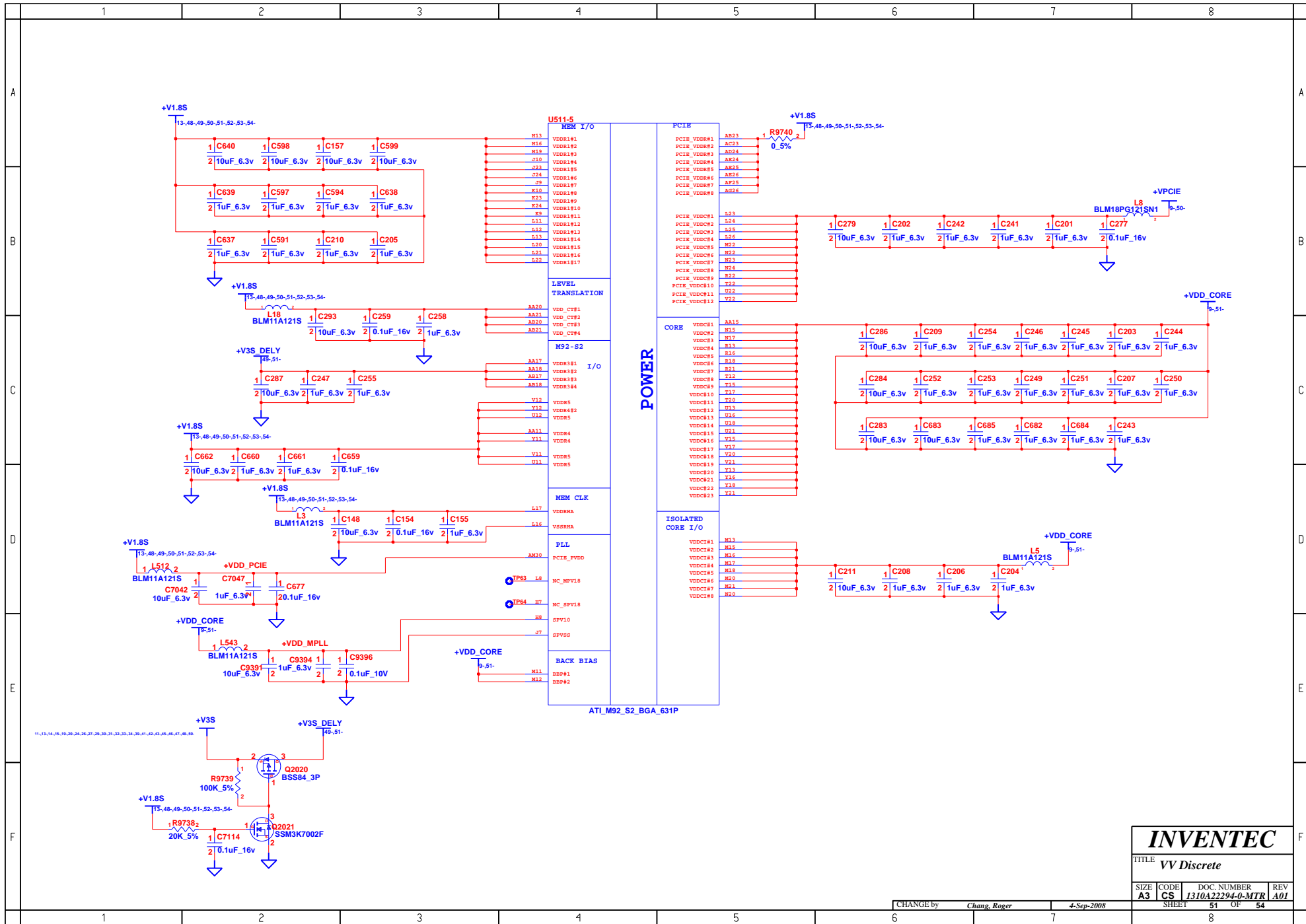


INVENTEC			
TITLE VV Discrete			
SIZE A3	CODE CS	DOC NUMBER 1310A22294-0-MTR	REV A01
SHEET 49		OF 54	

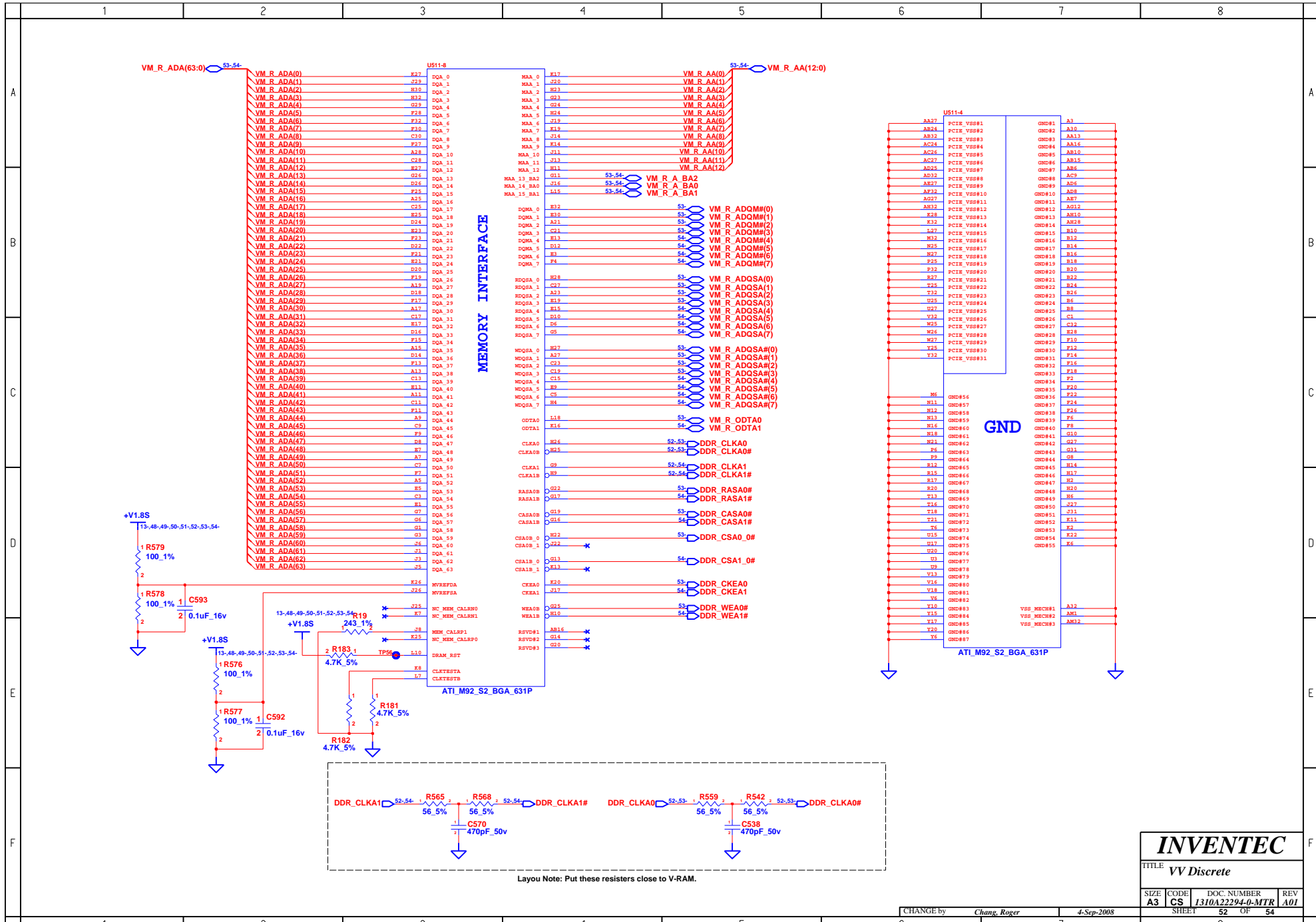


INVENTTEC
 TITLE: VV Discrete
 CODE: DOC NUMBER
 SIZE: A3 CS: I310A22942MTR_A01
 SHEET: 90 OF 94
 REV: 4S-SEP-2008

DESIGNED BY: Chang Rong
 CHECKED BY: Chang Rong
 DATE: 4S-SEP-2008



INVENTEC				
TITLE VV Discrete				
SIZE	CODE	DOC. NUMBER	REV	
A3	CS	1310A22394-0-MTR	A01	
CHANGE by <i>Chang, Roger</i>			4-Sep-2008	
SHEET 51			OF 54	

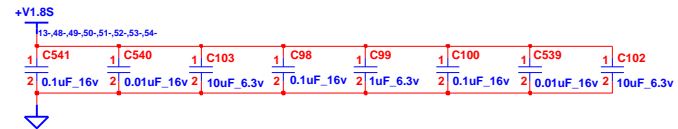
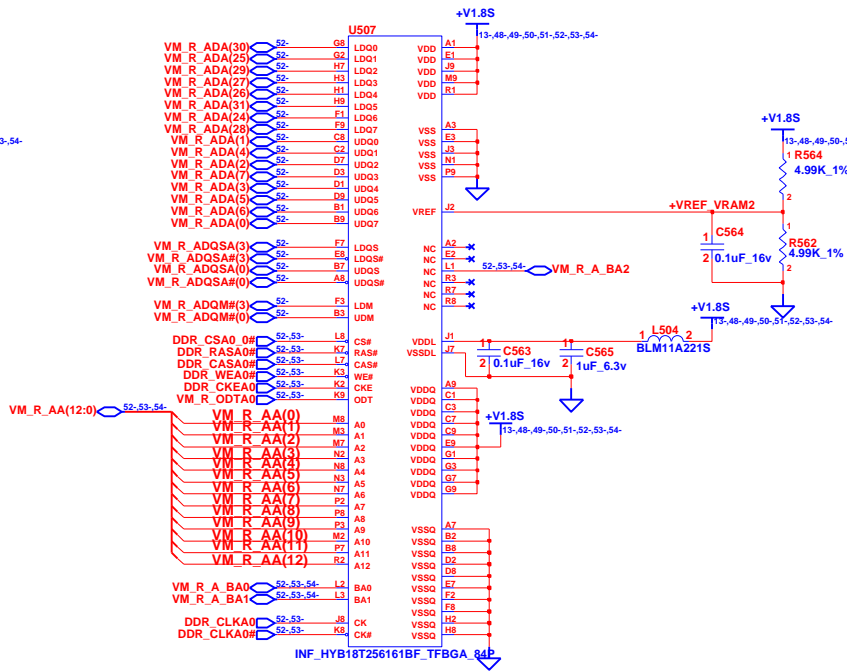
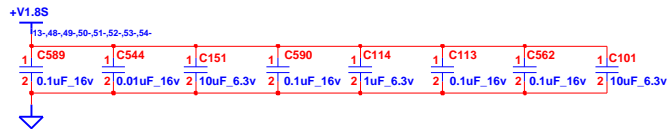
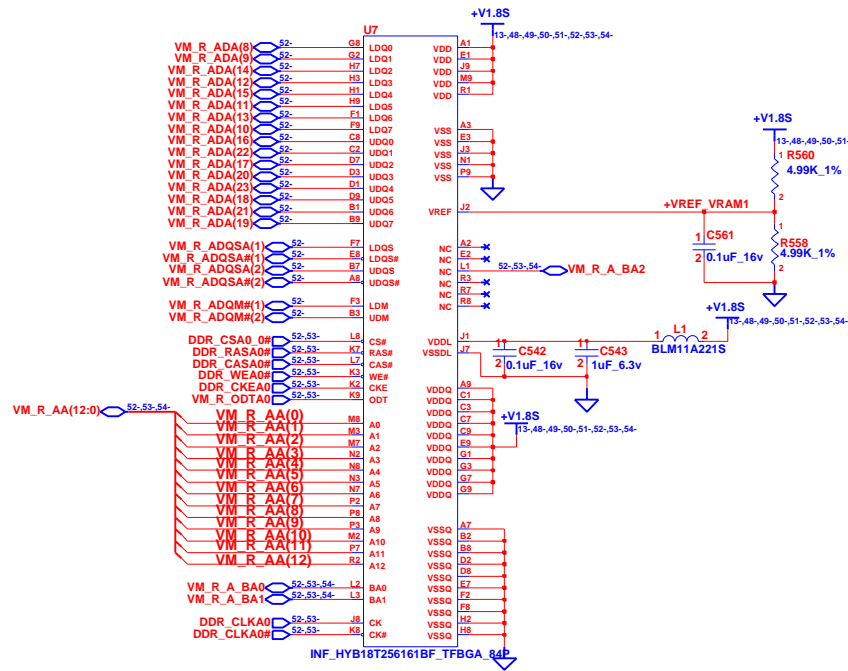


INVENTEC

TITLE: *VV Discrete*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22294-0-MTR	A01
SHEET		52	OF 54

Layout Note: Put these resistors close to V-RAM.



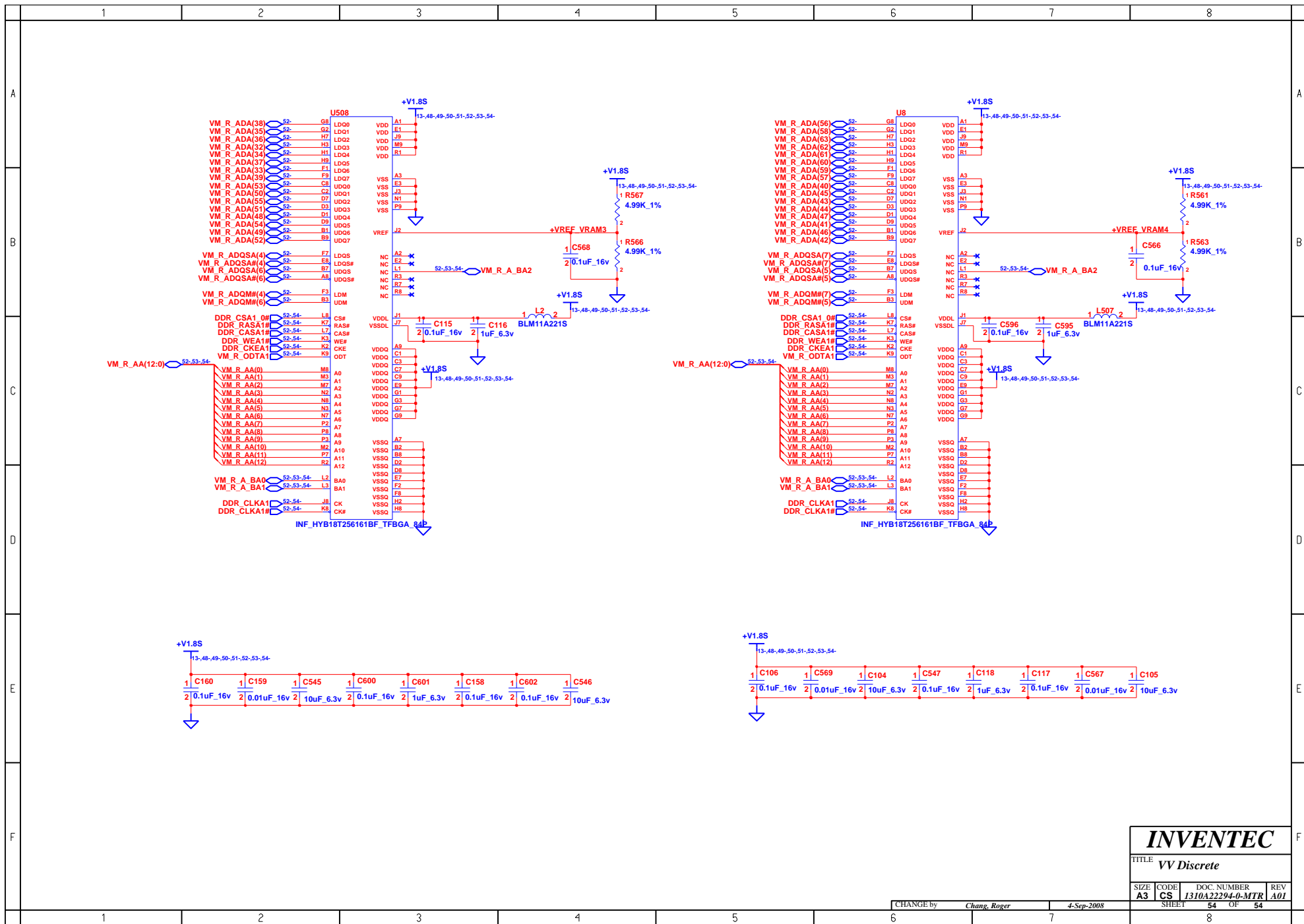
INVENTEC

TITLE VV Discrete

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310A22294-0-MTR	A01

CHANGE by Chang, Roger 4-Sep-2008

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INVENTEC				
TITLE VV Discrete				
SIZE	CODE	DOC. NUMBER	REV	
A3	CS	1310A2294-0-MTR	A01	
CHANGE by <i>Chang, Roger</i>			4-Sep-2008	
SHEET 54			OF 54	