AMD-DISCRETE
Volna
MV Build

2009.04.24

DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE = 3 VER :
FILE NAME : XXXX-XXXXXX-XX
P/N XXXXXXXXXXX

INVENTEC

TITLE *VV09 AMD-DIS*

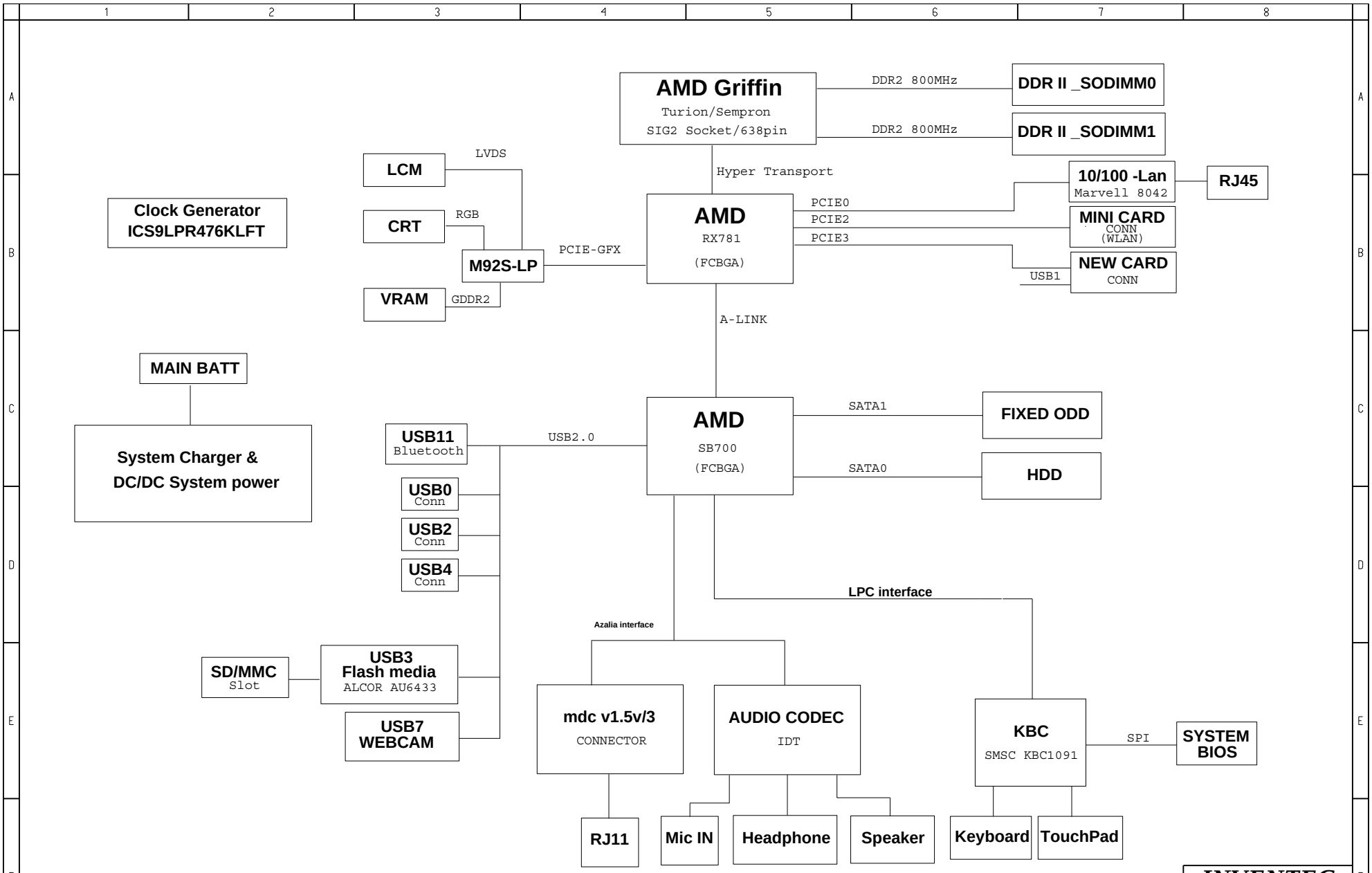
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 1 OF 58

TABLE OF CONTENTS

CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC			
TITLE: VV09 AMD-DIS Table OF Content			
SIZE: A3	CODE: CS	DOC. NUMBER: 1310A22588-0-MTRA03	REV
SHEET 2 OF 58			



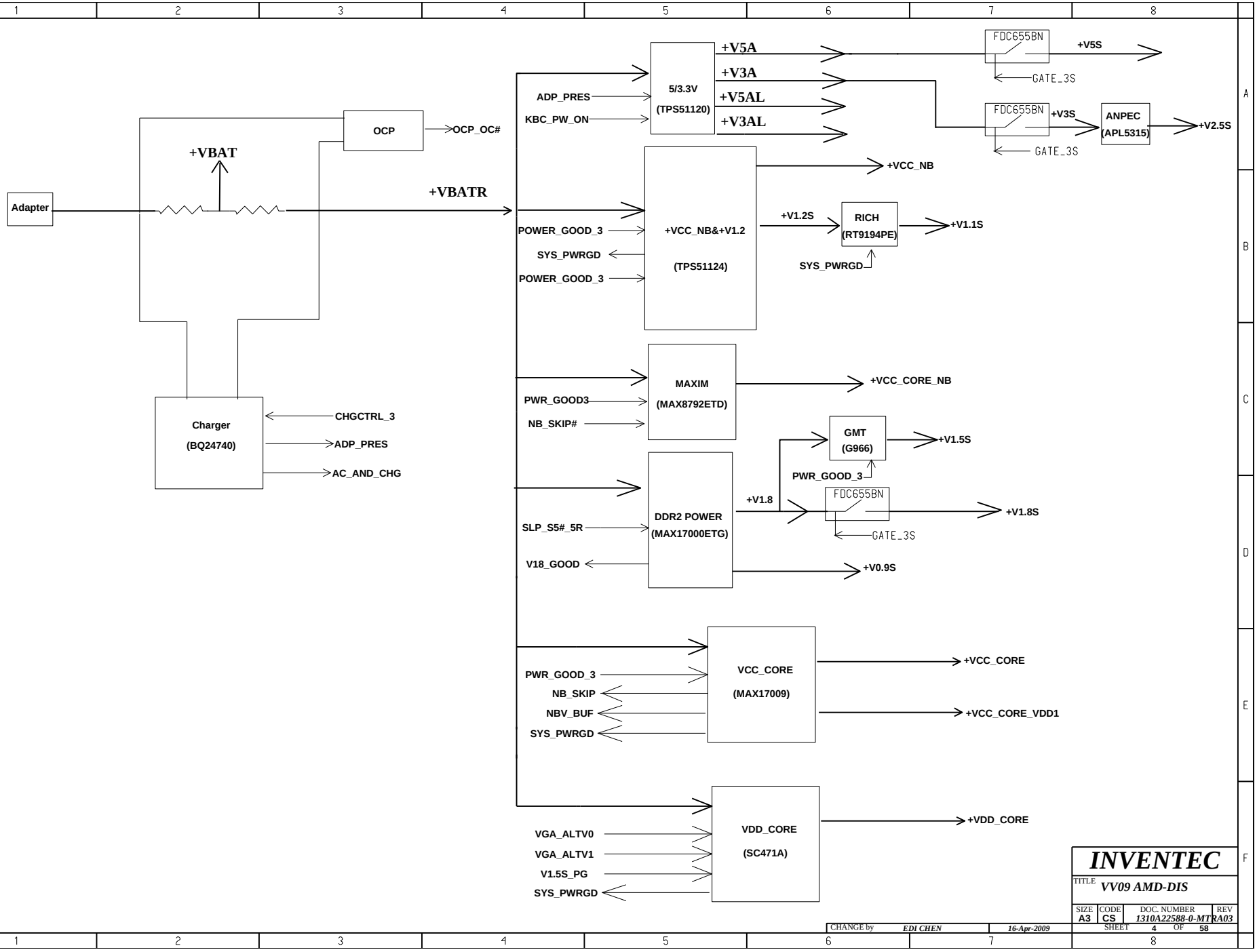
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
Block Diagram

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 3 OF 58



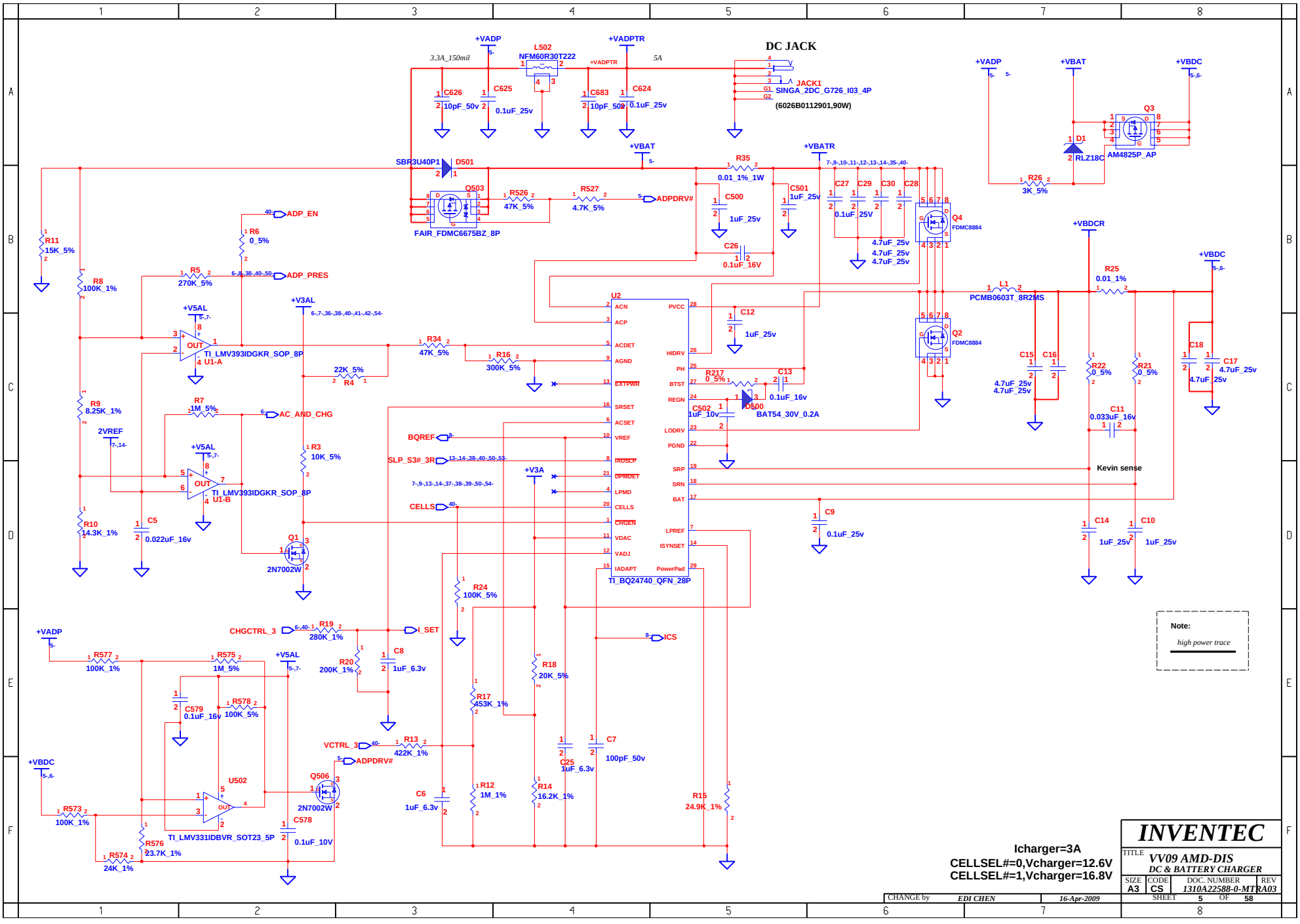
CHANGE by	EDI CHEN	16-Apr-2009	

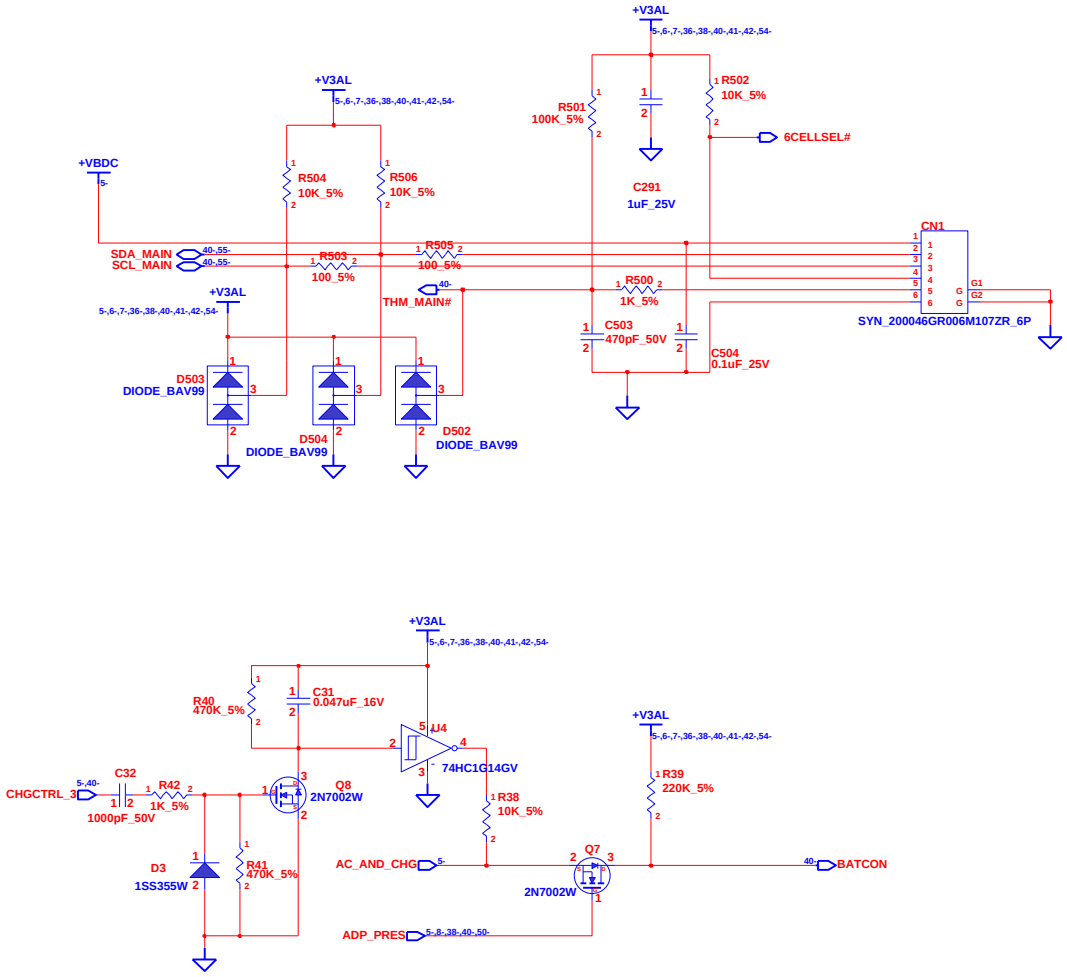
INVENTEC

TITLE: *VV09 AMD-DIS*

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTRA03	

SHEET 4 OF 58


DC JACK
JACK1
SINGA_2DC_G726_I03_4P
(6026B0112901,90W)
L502
NFM60R30T222
3.3A_150mil
5A
+VADP
+VADPTR
+VBAT
+VBATR
+VBDC
+VBDCR
SBR3U40P1
D501
Q503
FAIR_FDMC6675BZ_8P
R35
0.01_1%_1W
R526
47K_5%
R527
4.7K_5%
ADPDRV#
Q3
AM4825P_AP
D1
RLZ18C
R26
3K_5%
Q4
Q2
FDMC8884
L1
PCMB0603T_8R2MS
R25
0.01_1%
R11
15K_5%
R8
100K_1%
R5
270K_5%
ADP_PRES
ADP_EN
R6
0_5%
+V5AL
+V3AL
TI_LMV393IDGKR_SOP_8P
U1-A
U1-B
R4
22K_5%
R34
47K_5%
R16
300K_5%
R9
8.25K_1%
R7
1M_5%
AC_AND_CHG
2VREF
R3
10K_5%
R10
14.3K_1%
C5
0.022uF_16v
Q1
2N7002W
U2
TI_BQ24740_QFN_28P
BQREF
SLP_S3#_3R
CELLS
+V3A
R217
0_5%
C13
0.1uF_16v
D500
BAT54_30V_0.2A
C502
1uF_10v
C12
1uF_25v
C500
1uF_25v
C501
1uF_25v
C26
0.1uF_16V
C27
C29
C30
C28
0.1uF_25V
4.7uF_25v
C15
C16
4.7uF_25v
C18
C17
4.7uF_25v
C11
0.033uF_16v
Kevin sense
C9
0.1uF_25v
C14
C10
1uF_25v
C626
10pF_50v
C625
0.1uF_25v
C683
10pF_50v
C624
0.1uF_25v
CHGCTRL_3
R19
280K_1%
I_SET
ICS
R24
100K_5%
R18
20K_5%
R17
453K_1%
R20
200K_1%
C8
1uF_6.3v
R577
100K_1%
R575
1M_5%
C579
0.1uF_16v
R578
100K_5%
VCTRL_3
R13
422K_1%
ADPDRV#
C7
100pF_50v
C25
1uF_6.3v
C6
1uF_6.3v
R12
1M_1%
R14
16.2K_1%
R15
24.9K_1%
Q506
2N7002W
U502
TI_LMV331IDBVR_SOT23_5P
R573
100K_1%
R576
23.7K_1%
R574
24K_1%
C578
0.1uF_10V
Note:
high power trace
Icharger=3A
CELLSEL#=0,Vcharger=12.6V
CELLSEL#=1,Vcharger=16.8V
INVENTEC
TITLE
VV09 AMD-DIS
DC & BATTERY CHARGER
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 5 OF 58
CHANGE by EDI CHEN 16-Apr-2009



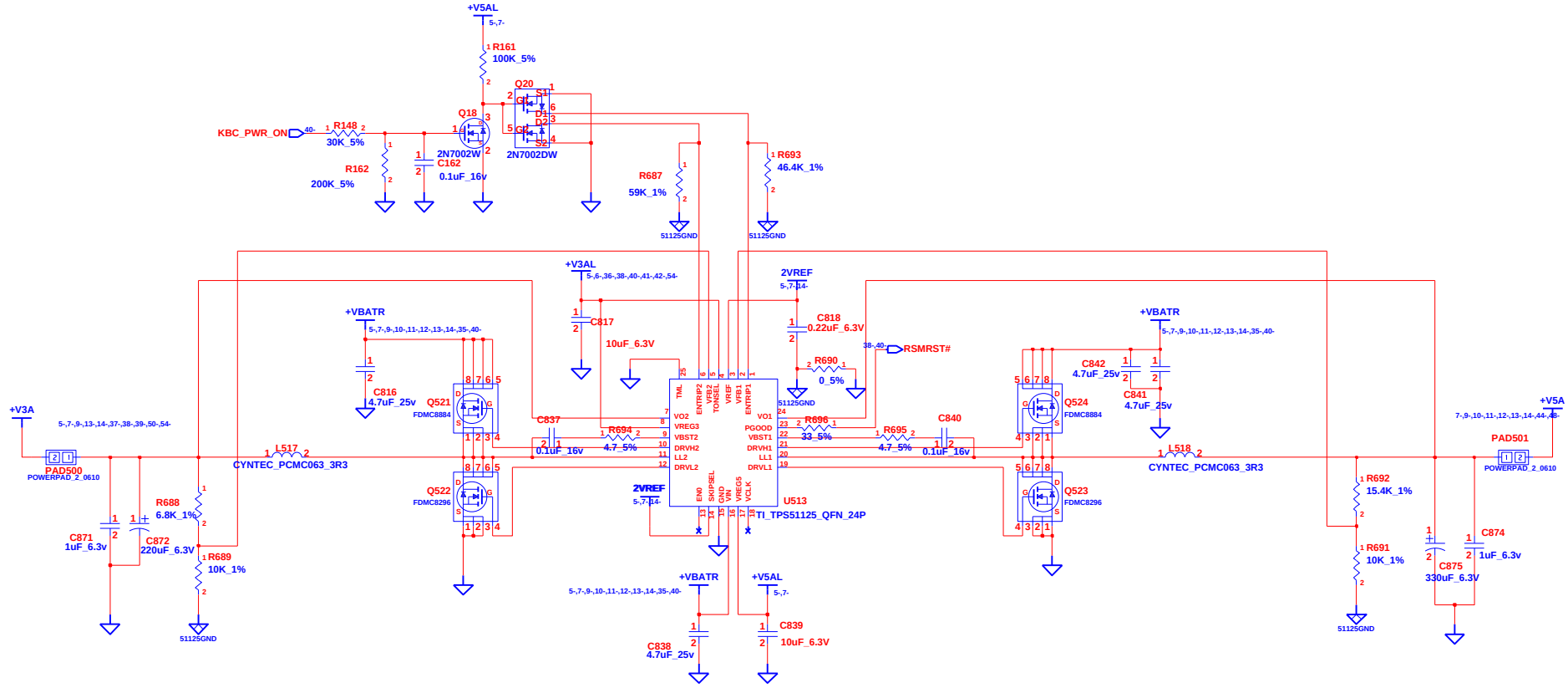
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
SELECT & BATTERY CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 6 OF 58



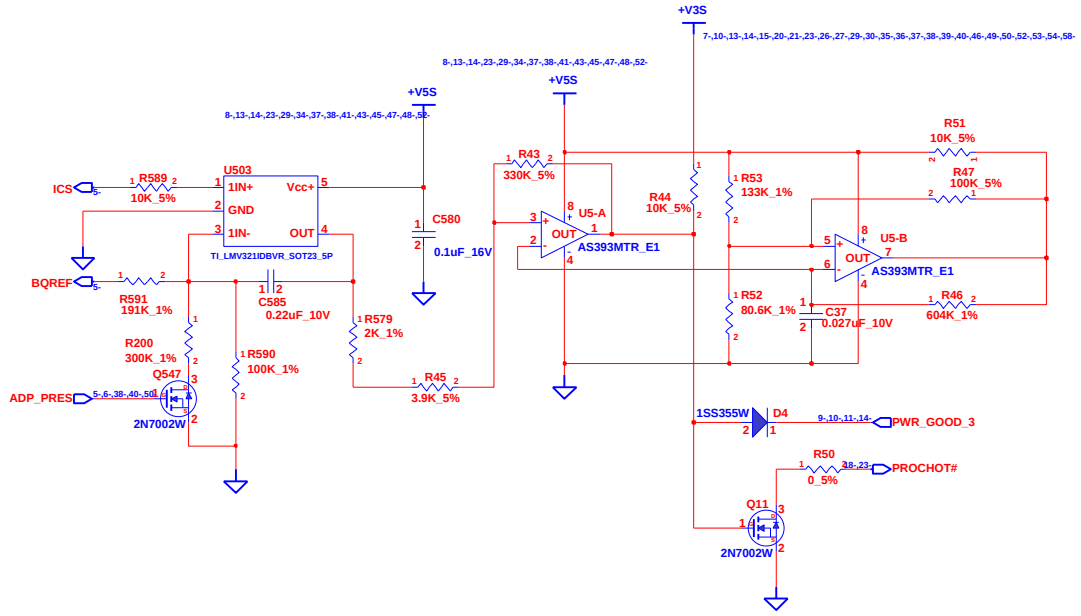
CHANGE by	EDI CHEN	24-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
+V5A,+V3A&+V2.5S

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 7 OF 58



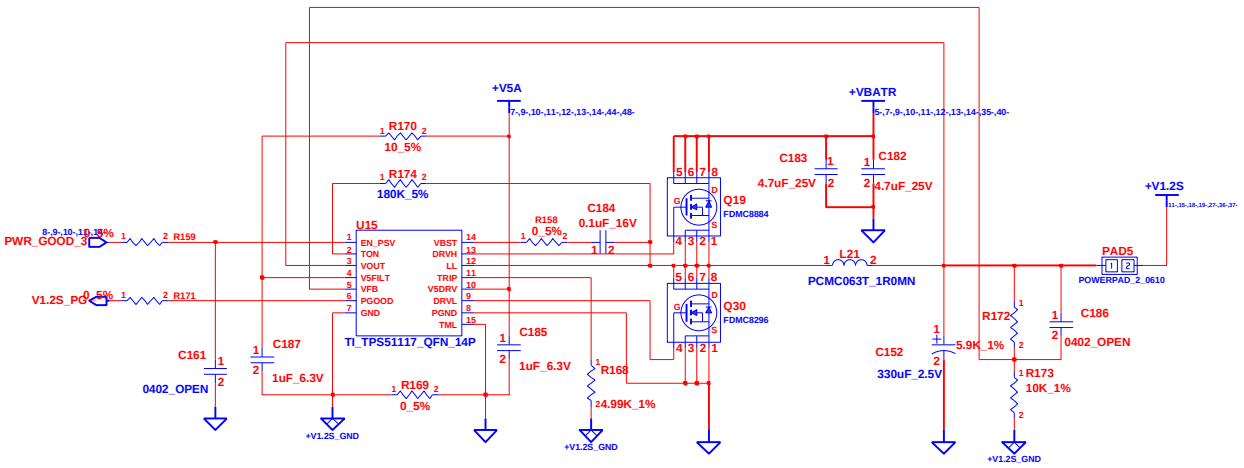
CHANGE by	EDI CHEN	16-Apr-2009	

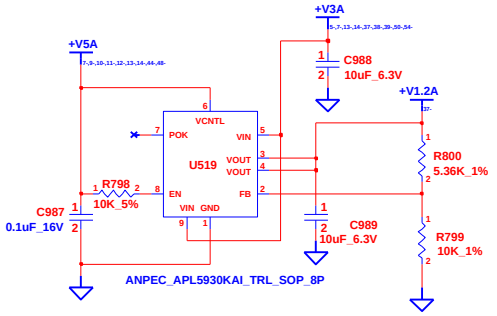
INVENTEC

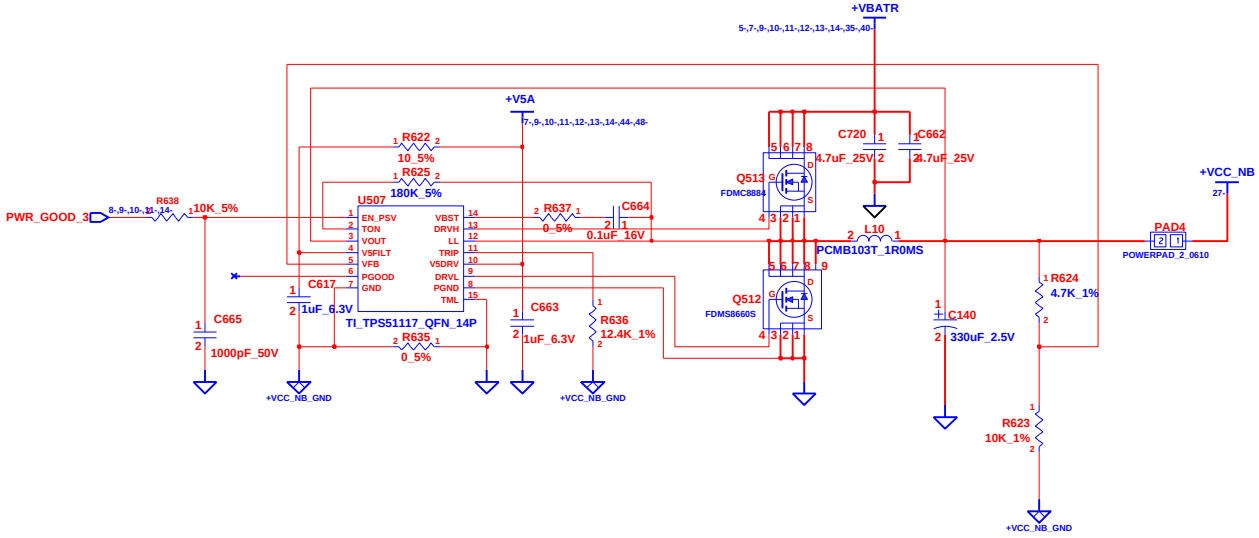
TITLE: *VV09 AMD-DIS*
OCP

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 8 OF 58







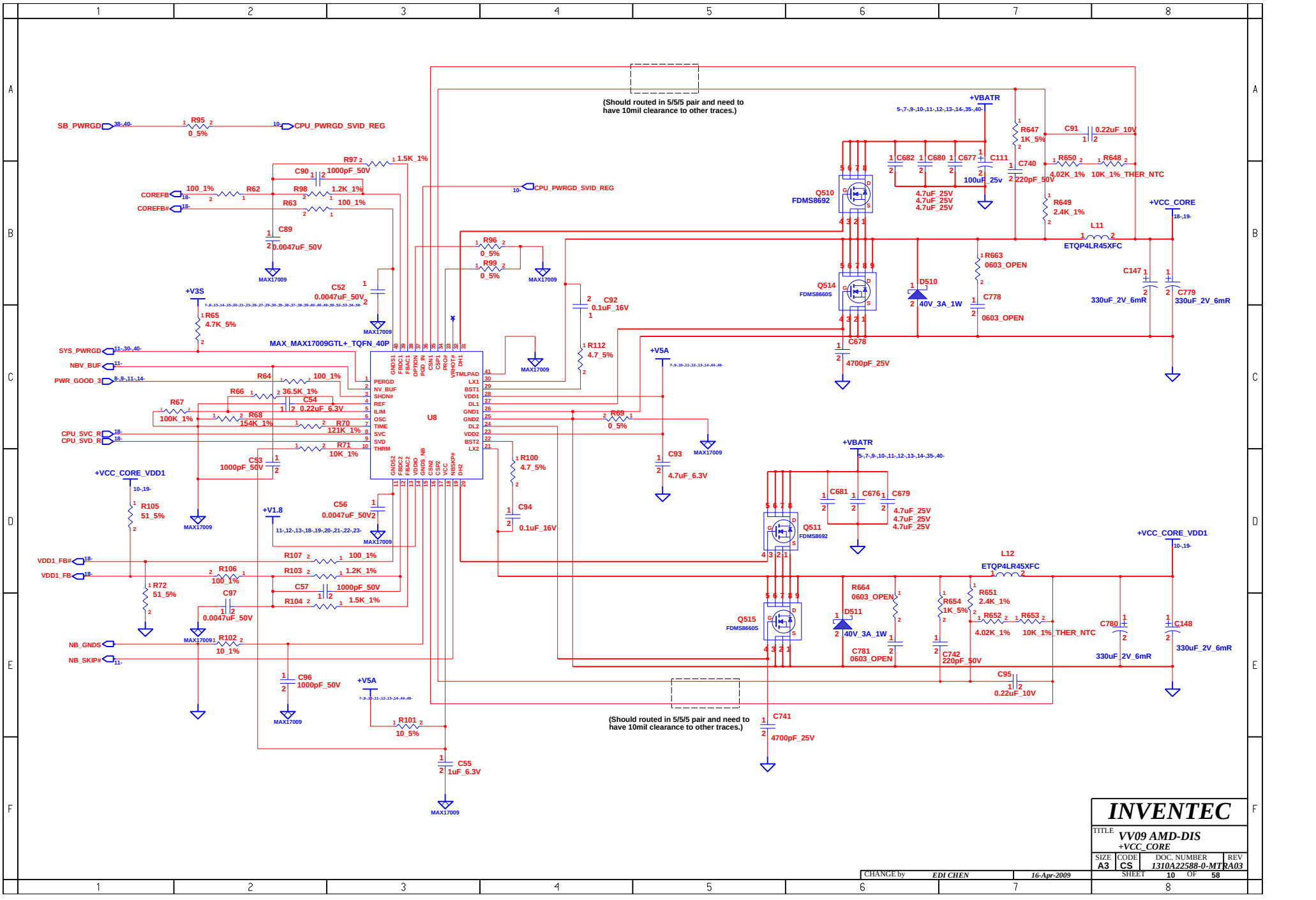
CHANGE by	EDI CHEN	16-Apr-2009		

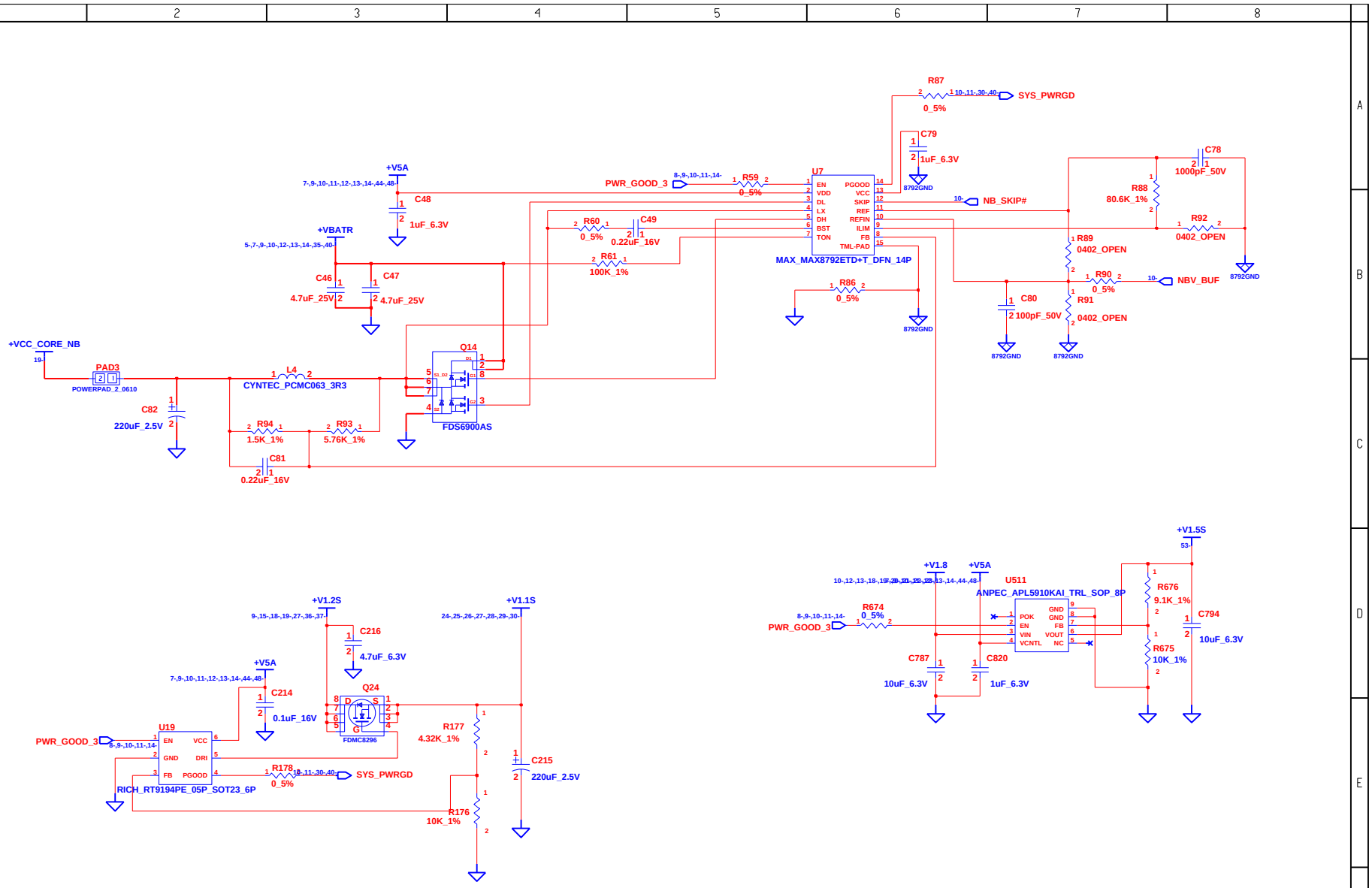
INVENTEC

TITLE: *VV09 AMD-DIS*
+VCC_NB & +V1.2A

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 9 OF 58


(Should routed in 5/5/5 pair and need to have 10mil clearance to other traces.)
(Should routed in 5/5/5 pair and need to have 10mil clearance to other traces.)
SB_PWRGD
CPU_PWRGD_SVID_REG
R95 0_5%
R97 1.5K_1%
C90 1000pF_50V
R98 1.2K_1%
R62 100_1%
R63 100_1%
COREFB
COREFB#
C89 0.0047uF_50V
C52 0.0047uF_50V
MAX17009
+V3S
R65 4.7K_5%
MAX_MAX17009GTL+_TQFN_40P
U8
SYS_PWRGD
NBV_BUF
PWR_GOOD_3
R64 100_1%
R66 36.5K_1%
C54 0.22uF_6.3V
R67 100K_1%
R68 154K_1%
R70 121K_1%
R71 10K_1%
CPU_SVC_R
CPU_SVD_R
C53 1000pF_50V
+VCC_CORE_VDD1
R105 51_5%
R72 51_5%
C97 0.0047uF_50V
R106 100_1%
R102 10_1%
NB_GNDS
NB_SKIP#
+V1.8
C56 0.0047uF_50V
R107 100_1%
R103 1.2K_1%
C57 1000pF_50V
R104 1.5K_1%
VDD1_FB#
VDD1_FB
C96 1000pF_50V
+V5A
R101 10_5%
C55 1uF_6.3V
R96 0_5%
R99 0_5%
C92 0.1uF_16V
R112 4.7_5%
R69 0_5%
R100 4.7_5%
C94 0.1uF_16V
C93 4.7uF_6.3V
+VBATR
Q510 FDMS8692
C682 C680 C677 C111 100uF_25v
4.7uF_25V 4.7uF_25V 4.7uF_25V
C740 220pF_50V
R647 1K_5%
C91 0.22uF_10V
R650 4.02K_1%
R648 10K_1%_THER_NTC
R649 2.4K_1%
+VCC_CORE
L11 ETQP4LR45XFC
Q514 FDMS8660S
D510 40V_3A_1W
R663 0603_OPEN
C778 0603_OPEN
C147 330uF_2V_6mR
C779 330uF_2V_6mR
C678 4700pF_25V
Q511 FDMS8692
C681 C676 C679 4.7uF_25V 4.7uF_25V 4.7uF_25V
L12 ETQP4LR45XFC
Q515 FDMS8660S
R664 0603_OPEN
D511 40V_3A_1W
C781 0603_OPEN
R654 1K_5%
R651 2.4K_1%
R652 4.02K_1%
R653 10K_1%_THER_NTC
C742 220pF_50V
C780 330uF_2V_6mR
C148 330uF_2V_6mR
C95 0.22uF_10V
C741 4700pF_25V
INVENTEC
TITLE VV09 AMD-DIS
+VCC_CORE
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 10 OF 58
CHANGE by EDI CHEN
16-Apr-2009



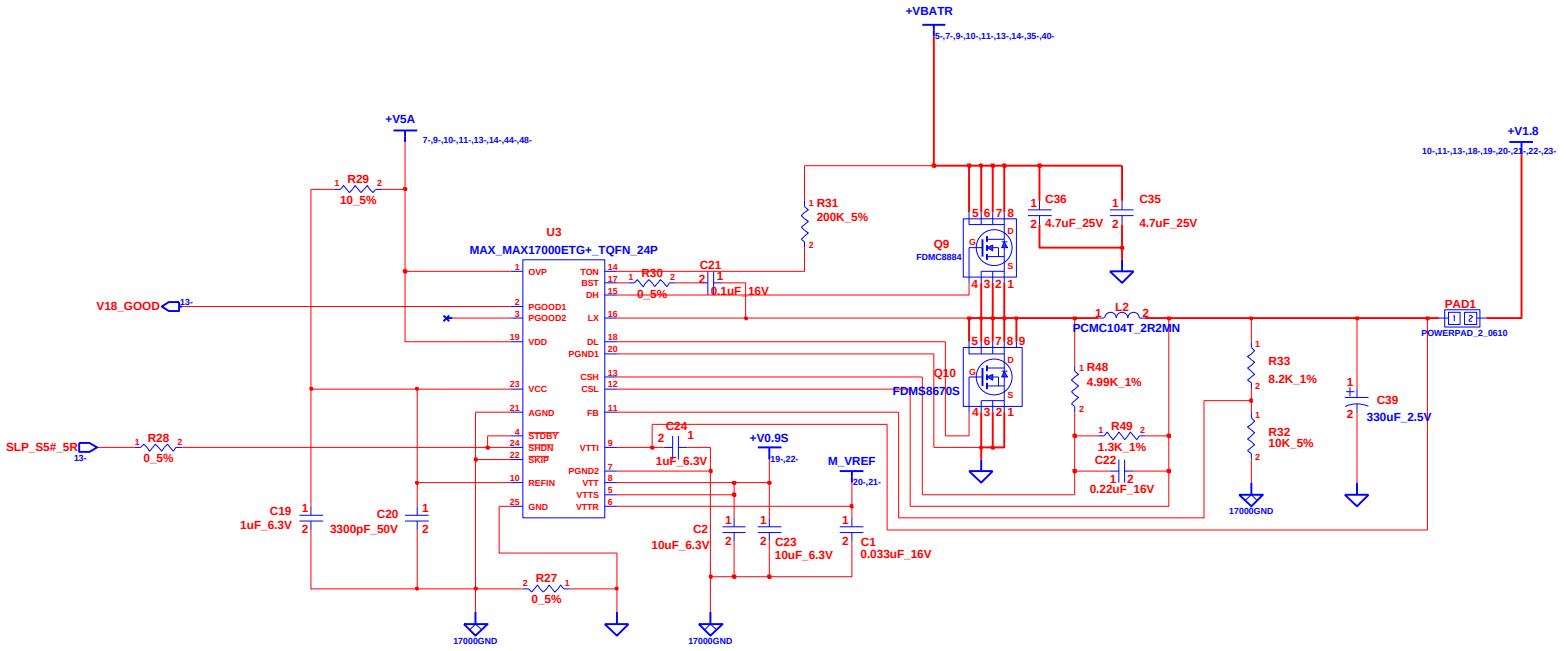
CHANGE by	EDI CHEN
	16-Apr-2009

INVENTEC

TITLE: *VV09 AMD-DIS*
POWER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 11 OF 58



NOTE: DDR2 REGULATOR

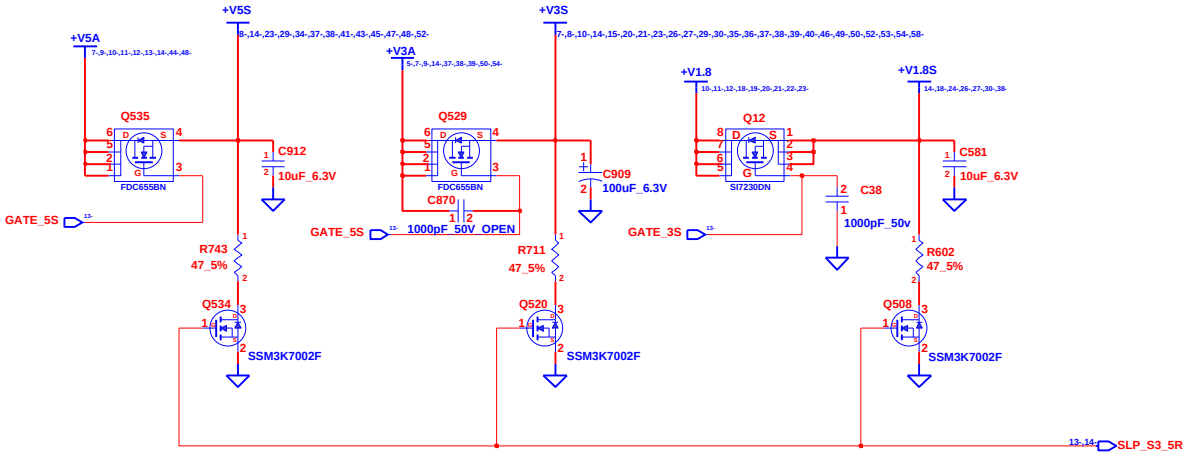
CHANGE by	*EDI CHEN*	*16-Apr-2009*	

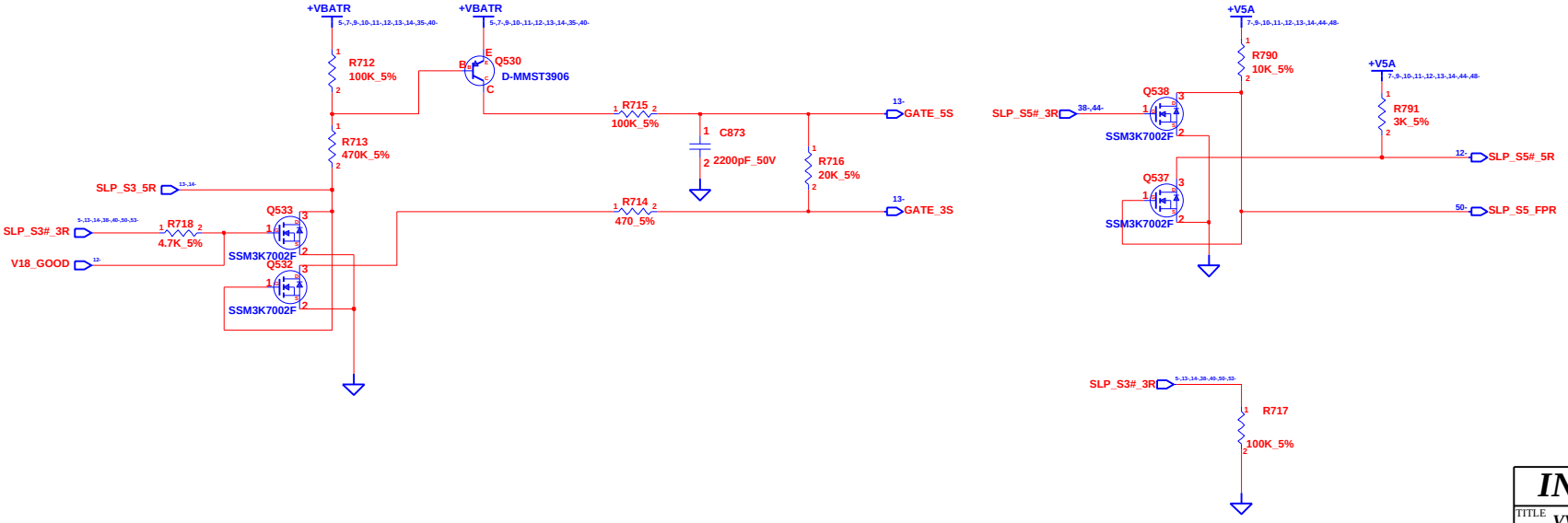
INVENTEC

TITLE: *VV09 AMD-DIS*
DDR2 POWER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 12 OF 58





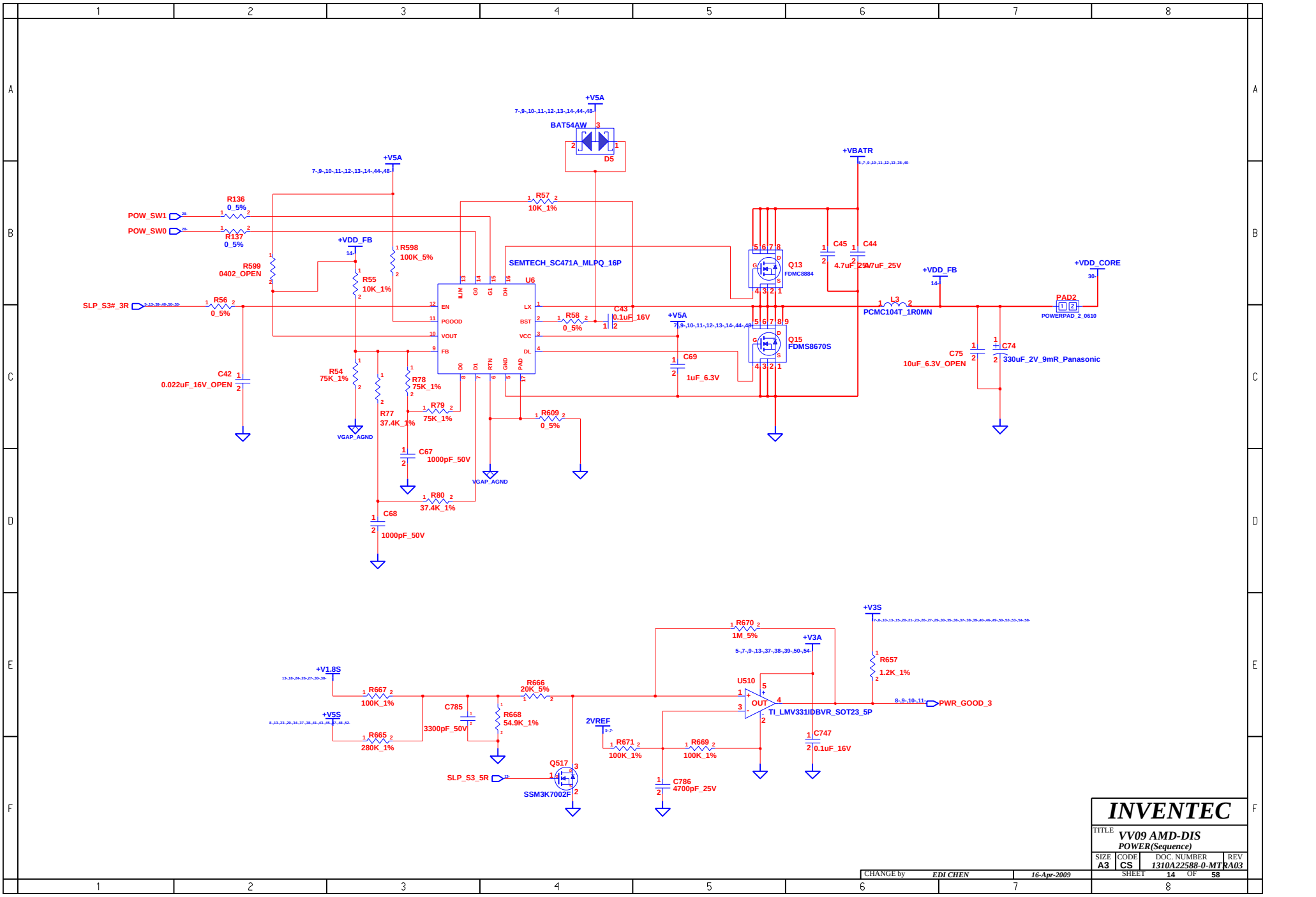
INVENTEC

TITLE: *VV09 AMD-DIS*
POWER(Sleep)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

CHANGE by *EDI CHEN* *16-Apr-2009*

SHEET 13 OF 58



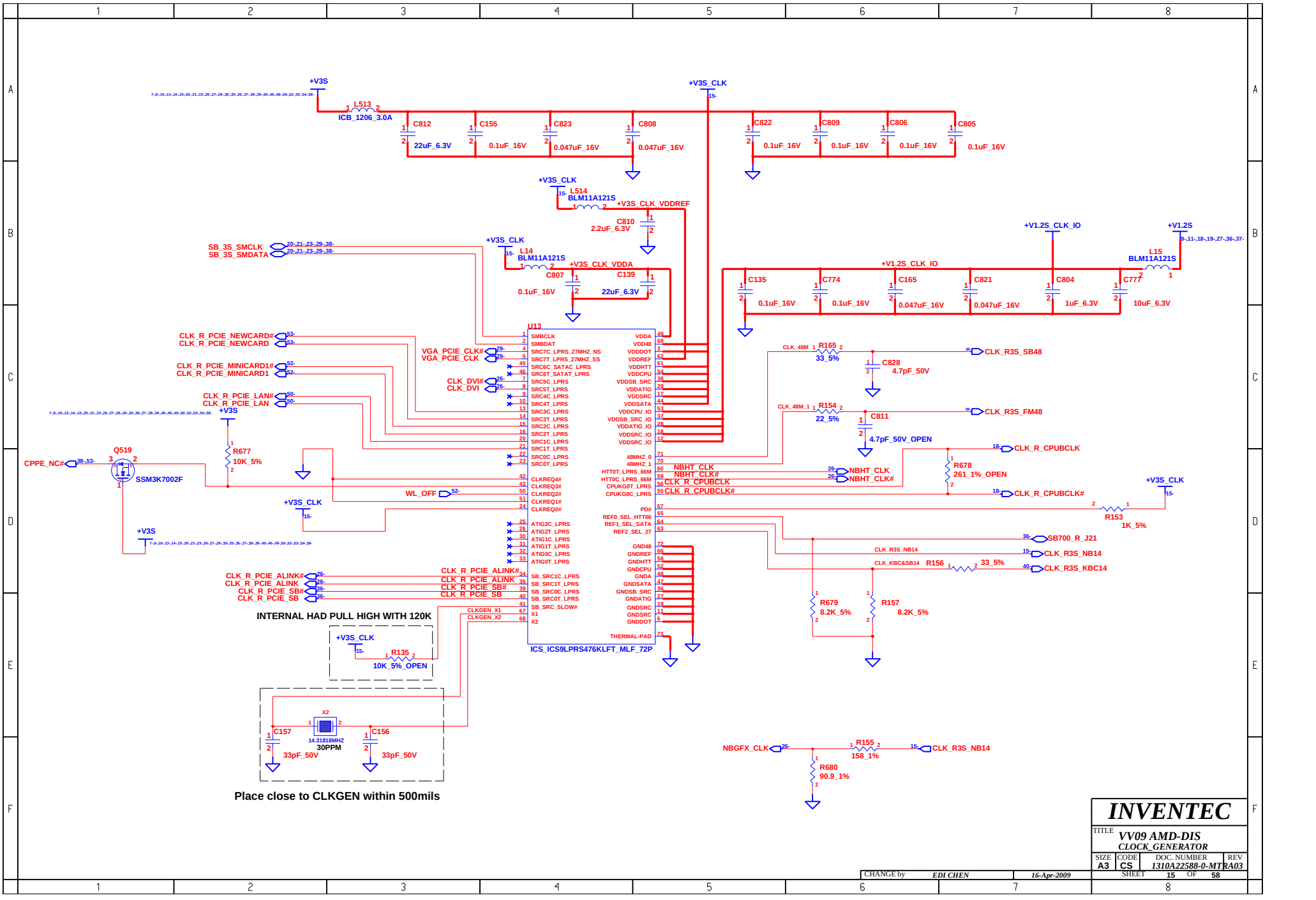
CHANGE by	EDI CHEN	16-Apr-2009	

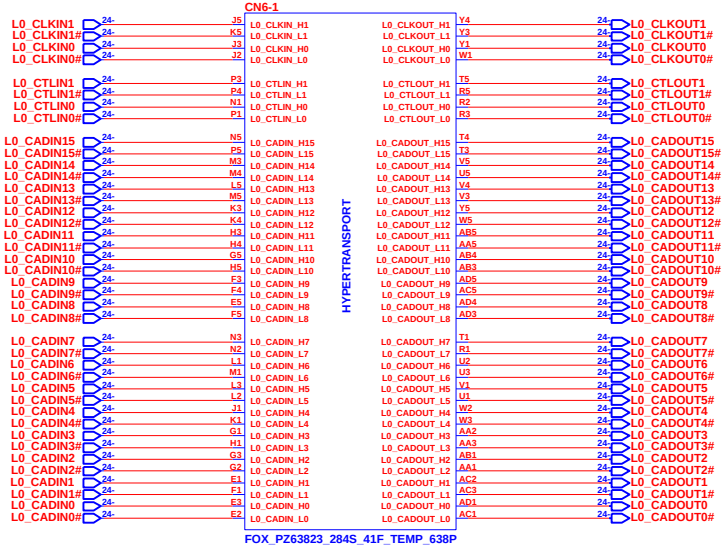
INVENTEC

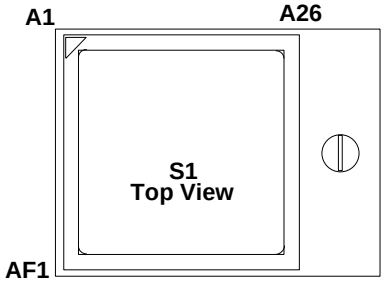
TITLE: *VV09 AMD-DIS*
POWER(Sequence)

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 14 OF 58


+V3S
L513
ICB_1206_3.0A
C812
22uF_6.3V
C155
0.1uF_16V
C823
0.047uF_16V
C808
0.047uF_16V
+V3S_CLK
C822
0.1uF_16V
C809
0.1uF_16V
C806
0.1uF_16V
C805
0.1uF_16V
+V3S_CLK
L514
BLM11A121S
+V3S_CLK_VDDREF
C810
2.2uF_6.3V
SB_3S_SMCLK
SB_3S_SMDATA
+V3S_CLK
L14
BLM11A121S
+V3S_CLK_VDDA
C807
0.1uF_16V
C139
22uF_6.3V
+V1.2S_CLK_IO
+V1.2S
L15
BLM11A121S
C135
0.1uF_16V
C774
0.1uF_16V
C165
0.047uF_16V
C821
0.047uF_16V
C804
1uF_6.3V
C777
10uF_6.3V
U13
ICS_ICS9LPRS476KLFT_MLF_72P
CLK_R_PCIE_NEWCARD#
CLK_R_PCIE_NEWCARD
VGA_PCIE_CLK#
VGA_PCIE_CLK
CLK_R_PCIE_MINICARD1#
CLK_R_PCIE_MINICARD1
CLK_DVI#
CLK_DVI
CLK_R_PCIE_LAN#
CLK_R_PCIE_LAN
CPPE_NC#
Q519
SSM3K7002F
R677
10K_5%
WL_OFF
R165
33_5%
CLK_R3S_SB48
C828
4.7pF_50V
R154
22_5%
CLK_R3S_FM48
C811
4.7pF_50V_OPEN
R678
261_1%_OPEN
CLK_R_CPUBCLK
CLK_R_CPUBCLK#
NBHT_CLK
NBHT_CLK#
CLK_R_CPUBCLK
CLK_R_CPUBCLK#
R153
1K_5%
SB700_R_J21
CLK_R3S_NB14
CLK_KBC&SB14
R156
33_5%
CLK_R3S_KBC14
R679
8.2K_5%
R157
8.2K_5%
CLK_R_PCIE_ALINK#
CLK_R_PCIE_ALINK
CLK_R_PCIE_SB#
CLK_R_PCIE_SB
INTERNAL HAD PULL HIGH WITH 120K
R135
10K_5%_OPEN
X2
14.31818MHZ
30PPM
C157
33pF_50V
C156
33pF_50V
Place close to CLKGEN within 500mils
NBGFX_CLK
R155
158_1%
CLK_R3S_NB14
R680
90.9_1%
INVENTEC
TITLE
VV09 AMD-DIS
CLOCK_GENERATOR
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 15 OF 58
CHANGE by EDI CHEN
16-Apr-2009





Layout: Add stitching caps if crossing plane split.

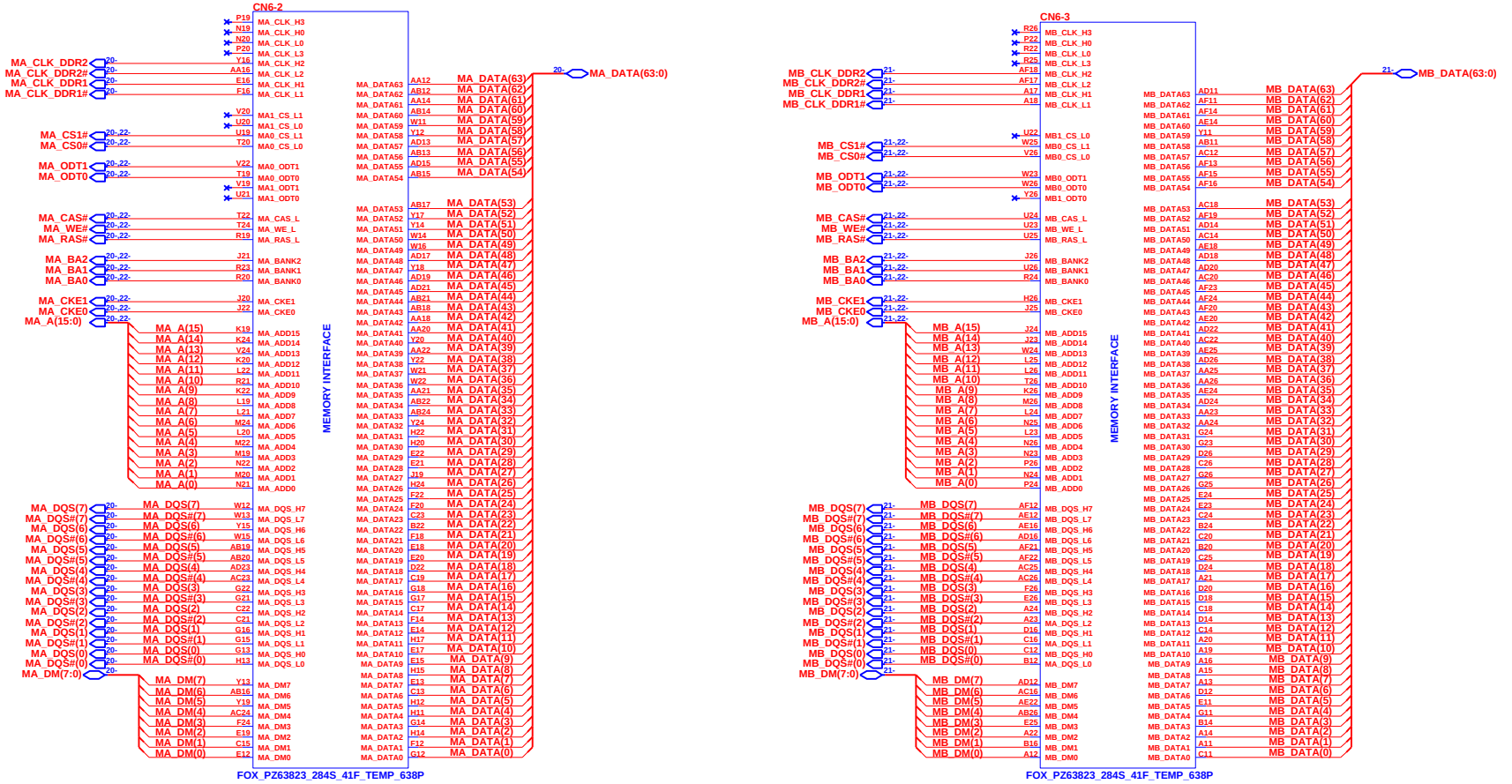
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: VV09 AMD-DIS
CPU-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTRA03	

SHEET 16 OF 58



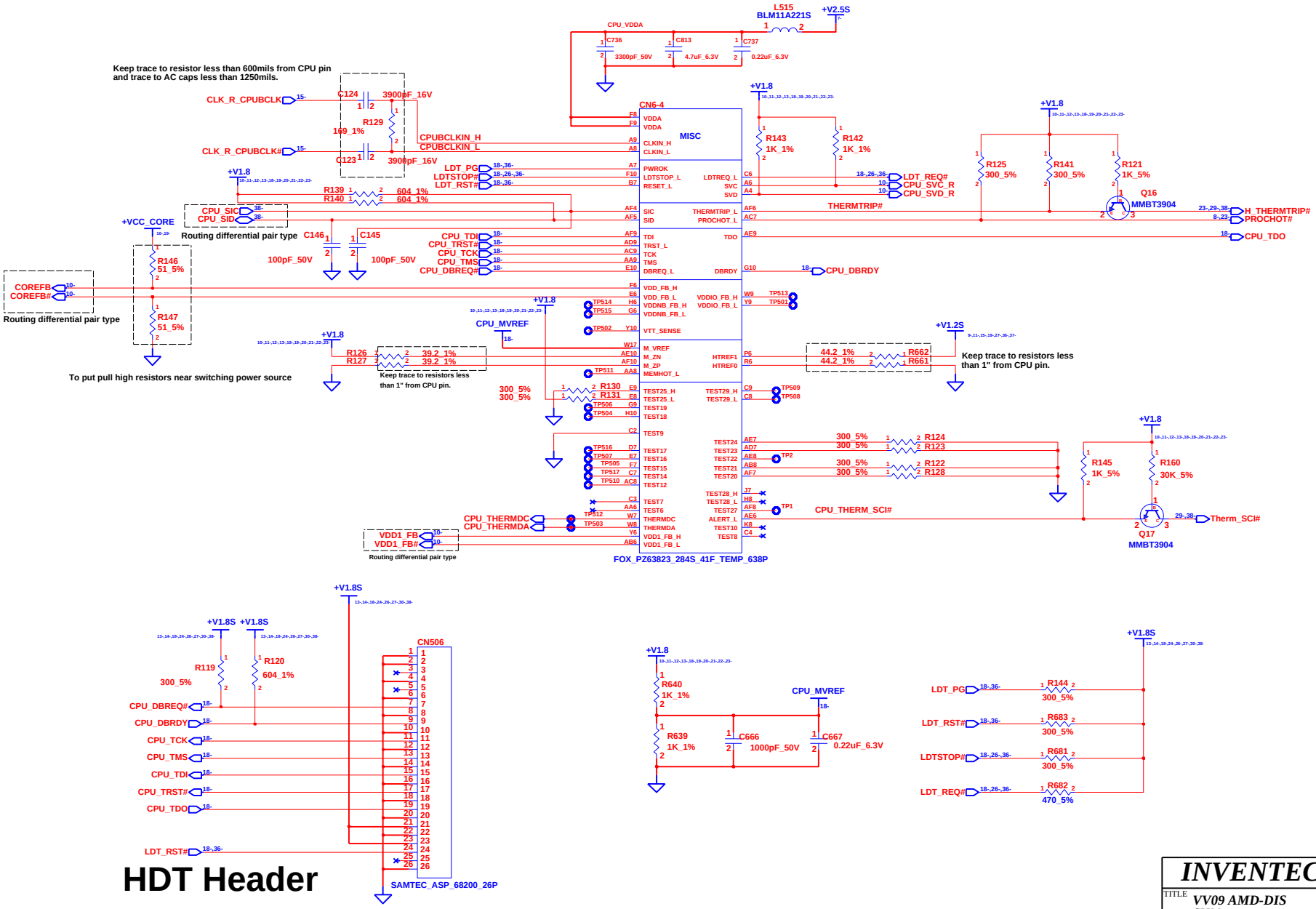
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
CPU-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 17 OF 58



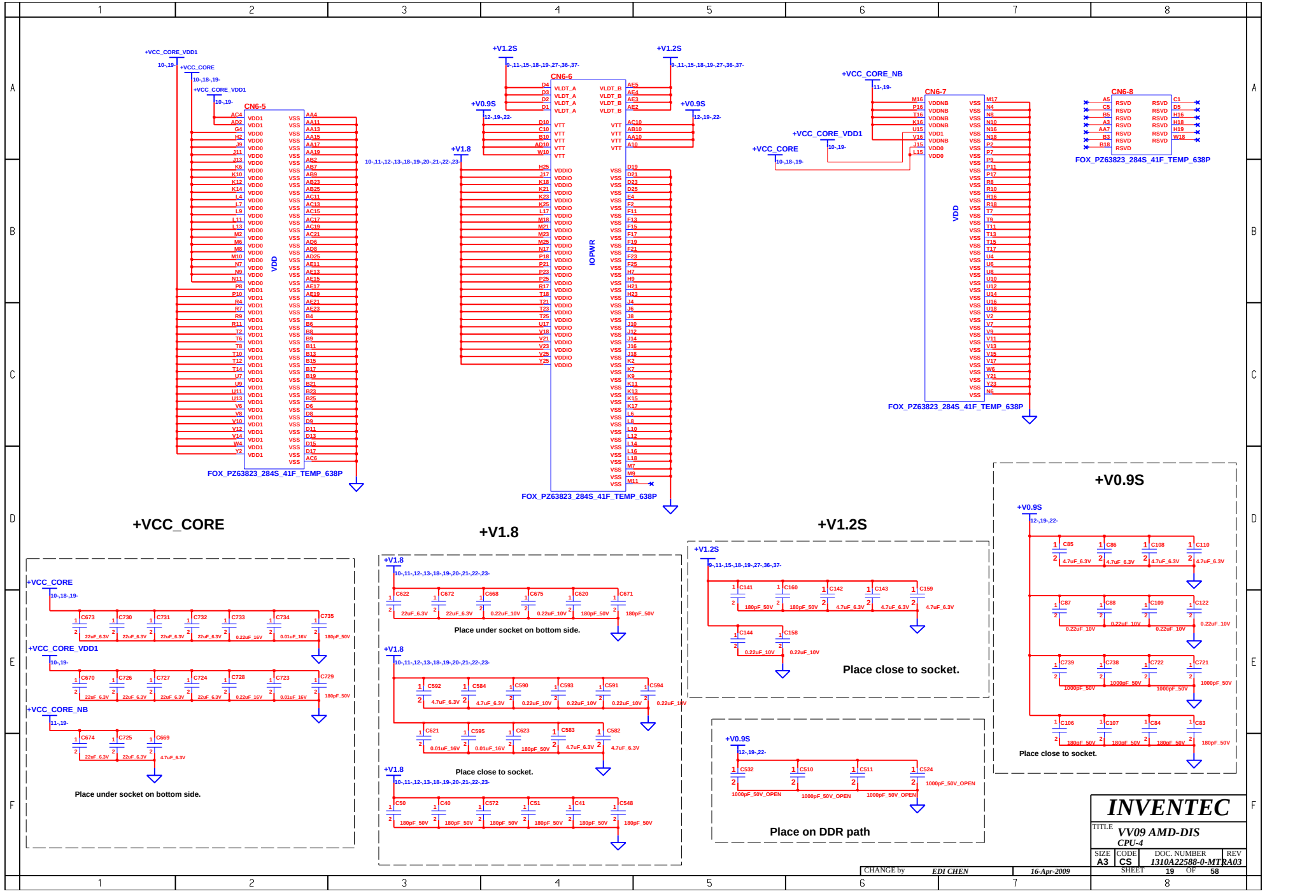
CHANGE by	EDI CHEN	16-Apr-2009		

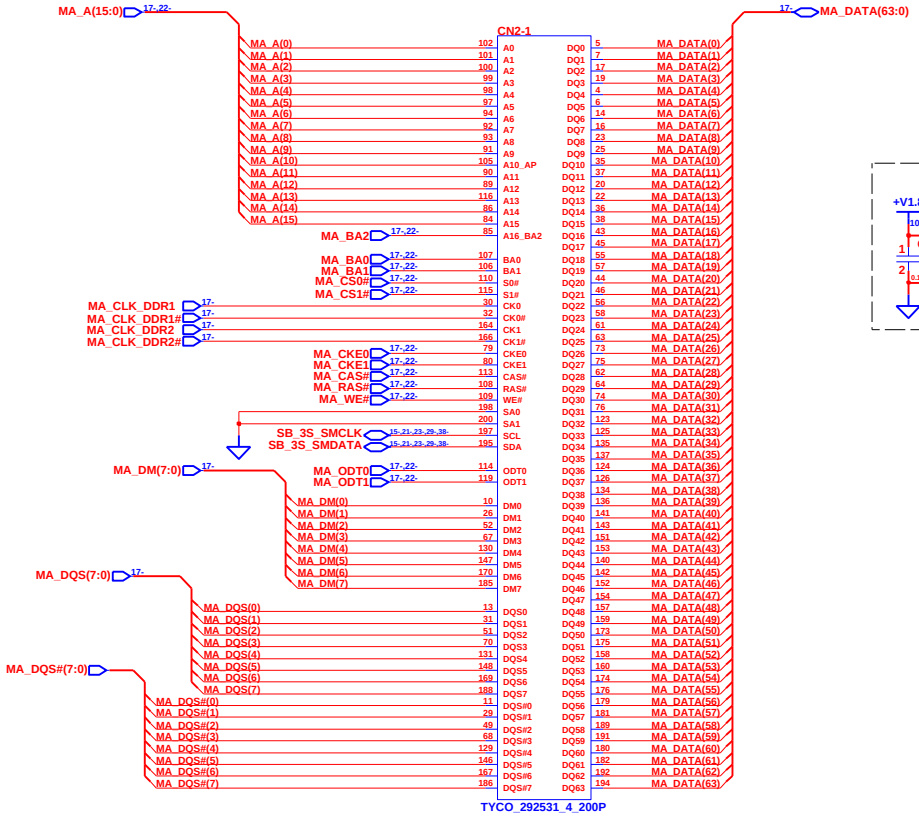
INVENTEC

TITLE: *VV09 AMD-DIS*
CPU-3

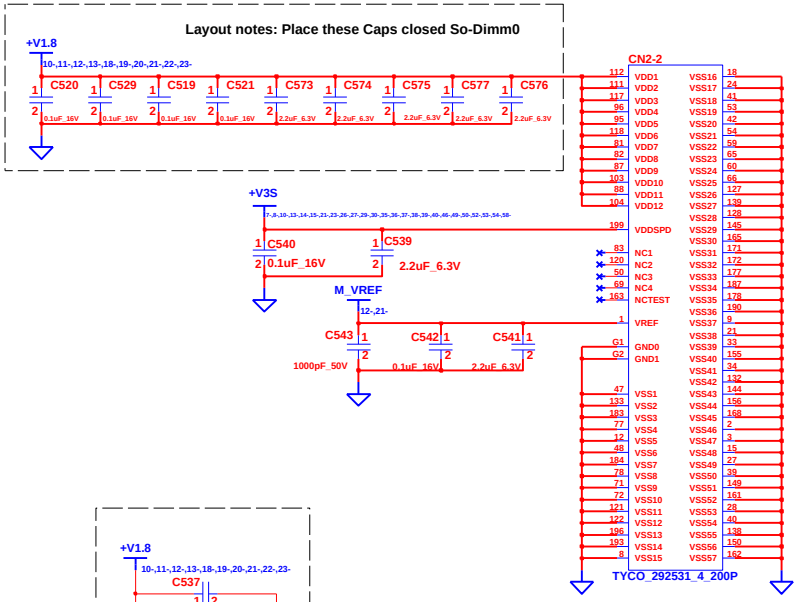
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

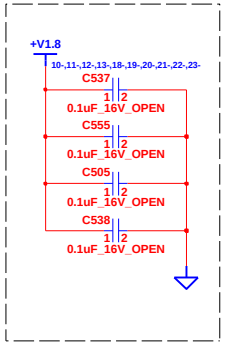
SHEET 18 OF 58


+VCC_CORE_VDD1
+VCC_CORE
+VCC_CORE_VDD1
CN6-5
VDD
FOX_PZ63823_284S_41F_TEMP_638P
+V1.2S
+V0.9S
+V1.8
CN6-6
VLDT_A
VLDT_B
VTT
VDDIO
IOPWR
FOX_PZ63823_284S_41F_TEMP_638P
+VCC_CORE_NB
CN6-7
VDDNB
VDD0
VDD1
VDD
FOX_PZ63823_284S_41F_TEMP_638P
CN6-8
RSVD
FOX_PZ63823_284S_41F_TEMP_638P
+VCC_CORE
+VCC_CORE_VDD1
+VCC_CORE_NB
Place under socket on bottom side.
+V1.8
Place under socket on bottom side.
Place close to socket.
+V1.2S
Place close to socket.
+V0.9S
Place on DDR path
+V0.9S
Place close to socket.
INVENTEC
TITLE
VV09 AMD-DIS
CPU-4
SIZE
A3
CODE
CS
DOC. NUMBER
1310A22588-0-MTRA03
REV
SHEET
19
OF
58
CHANGE by
EDI CHEN
16-Apr-2009



SO DIMM_9.2mm





For EMI Test

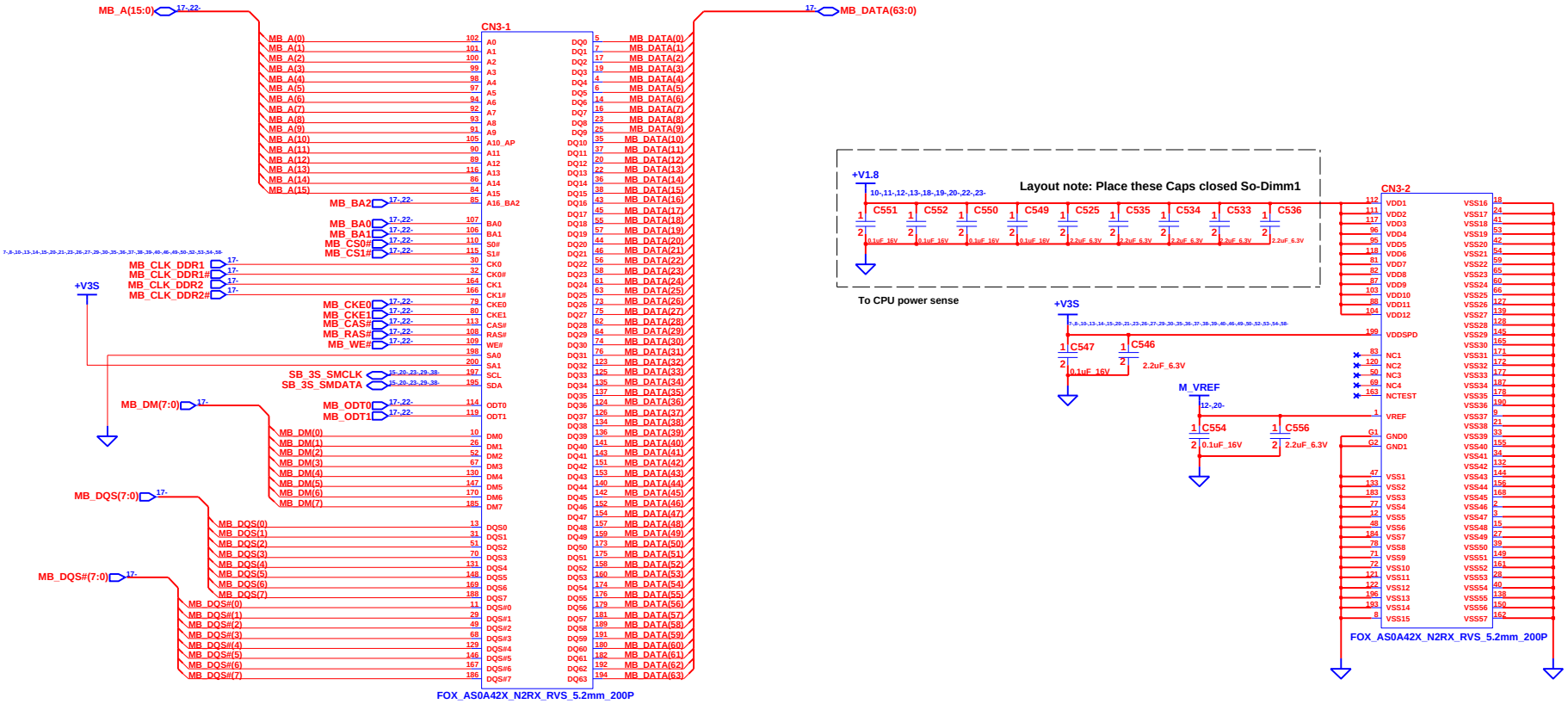
CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC

TITLE: *VV09 AMD-DIS*
DDR2-DIMM-0

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 20 OF 58



SODIMM_5.2mm

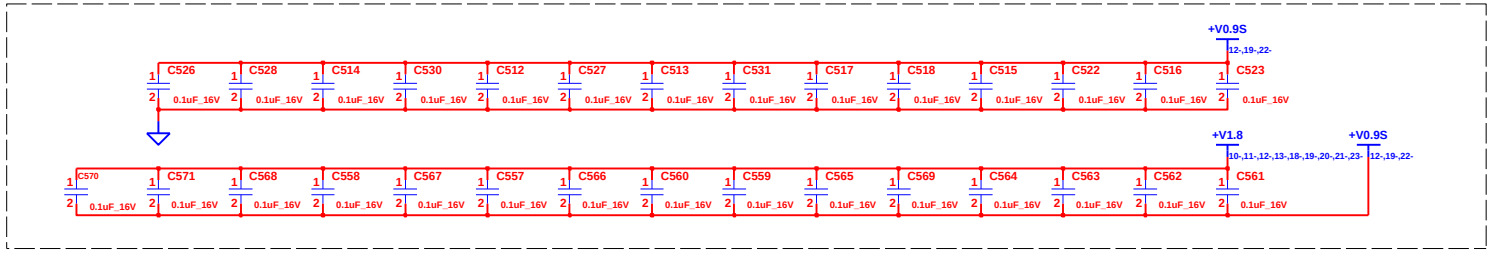
INVENTEC

TITLE: *VV09 AMD-DIS*
DDR2-DIMM-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

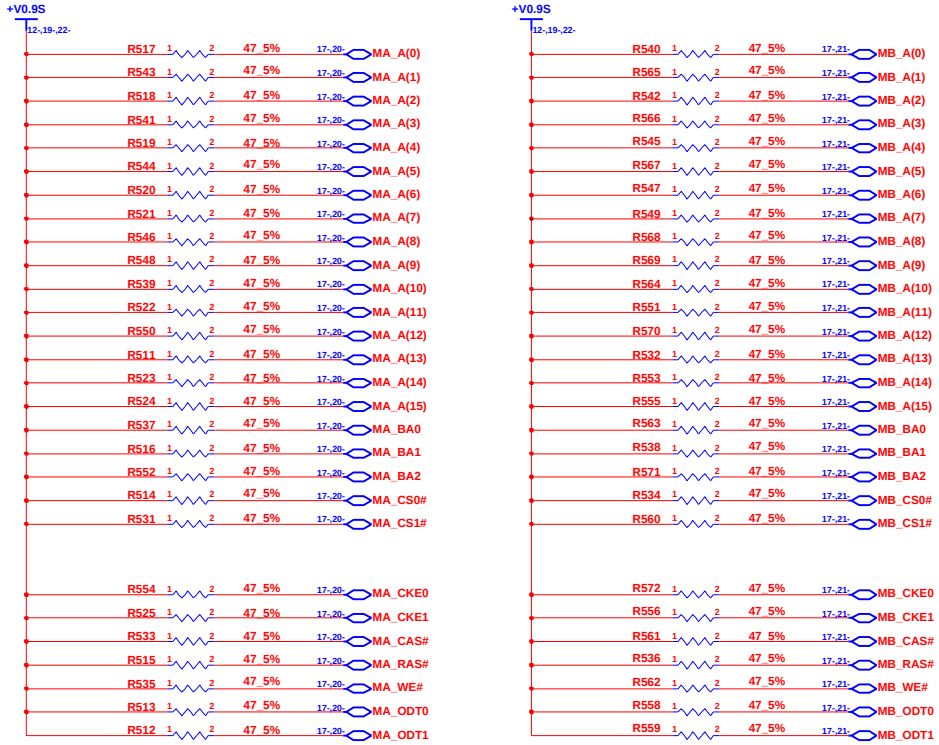
SHEET 21 OF 58

CHANGE by *EDI CHEN* *16-Apr-2009*



To CPU power sense

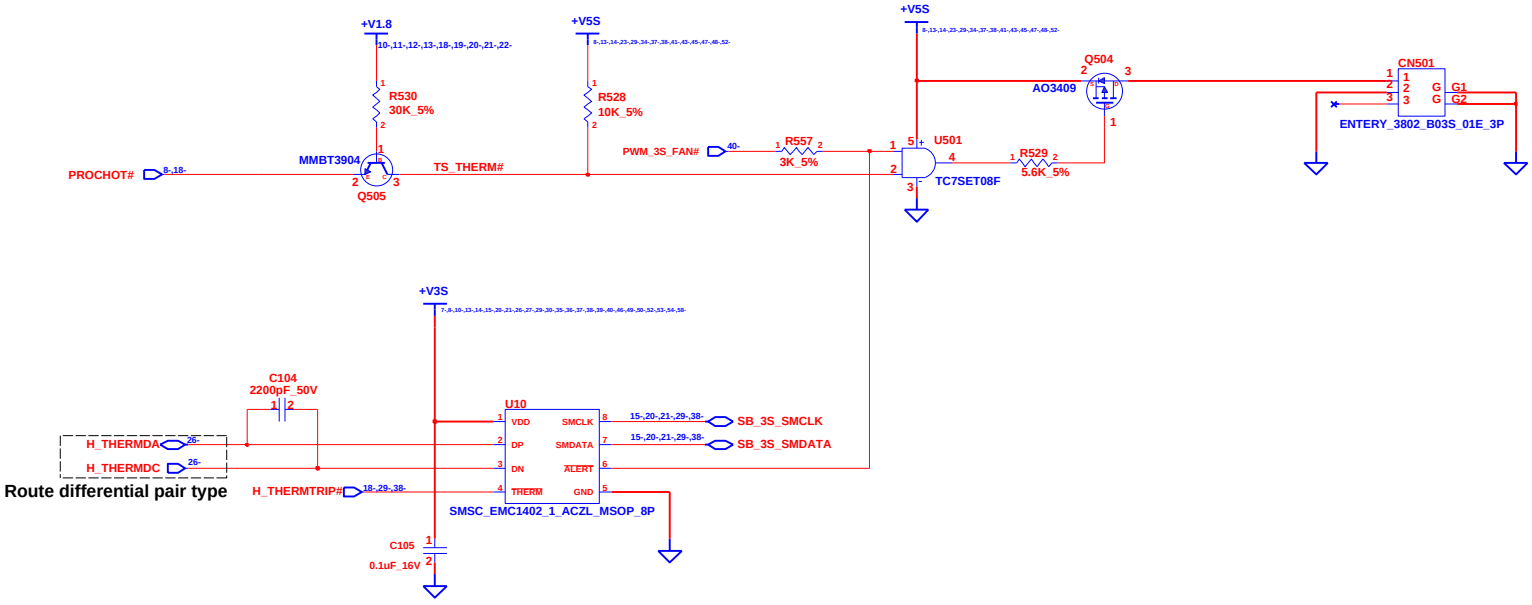
Place CAPs close to DIMM



CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC

TITLE	VV09 AMD-DIS DDR2-DAMPING		
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTRA03	
SHEET	22	OF	58



Route differential pair type

LAYOUT Note: Put the thermal sensor close to CPU.

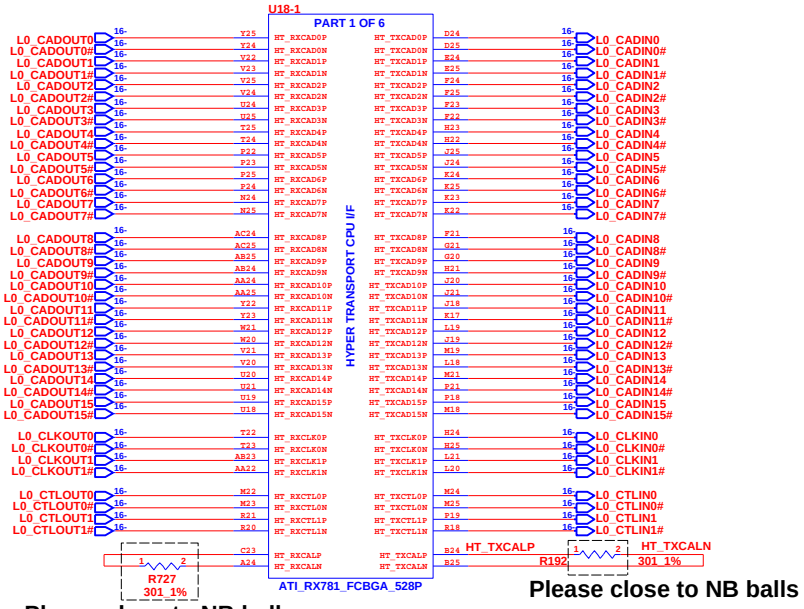
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
THERMAL & FAN CONTROLLER

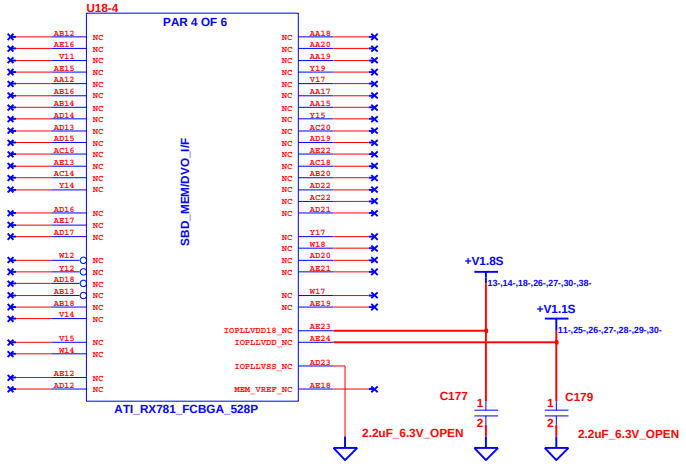
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 23 OF 58



Please close to NB balls

Please close to NB balls



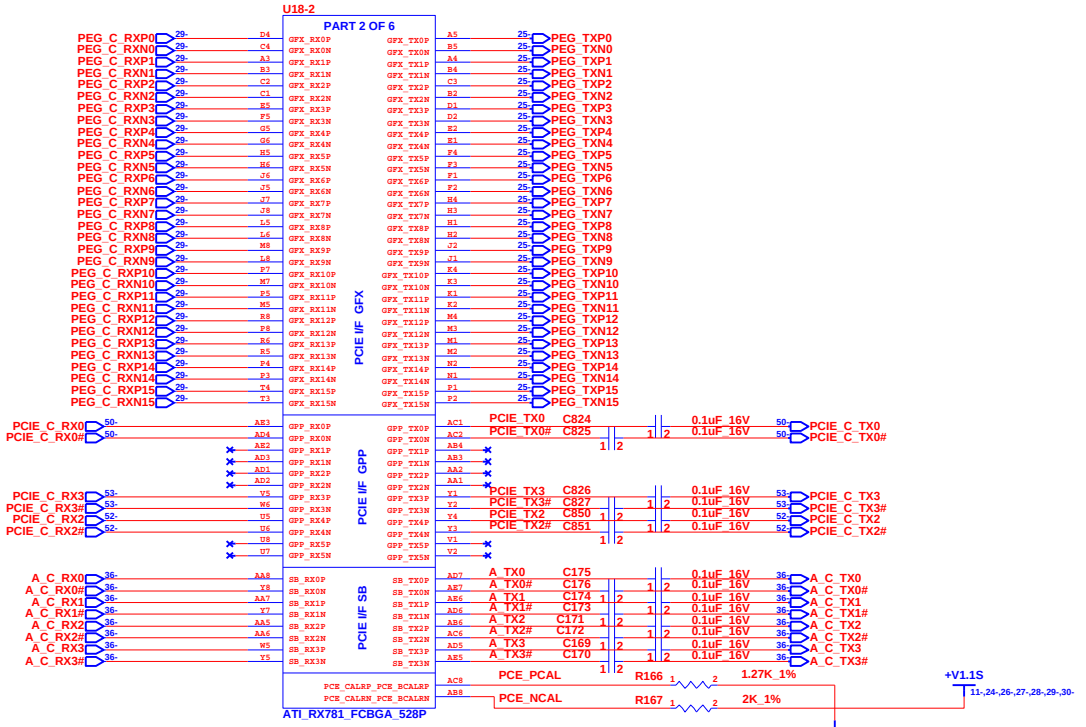
CHANGE by	EDI CHEN	16-Apr-2009	

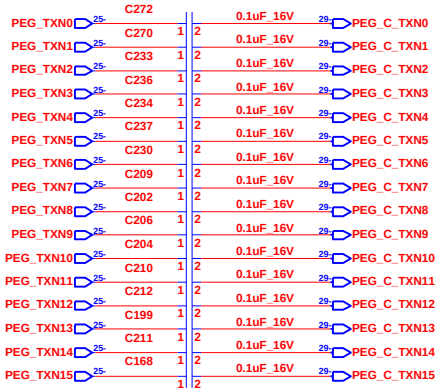
INVENTEC

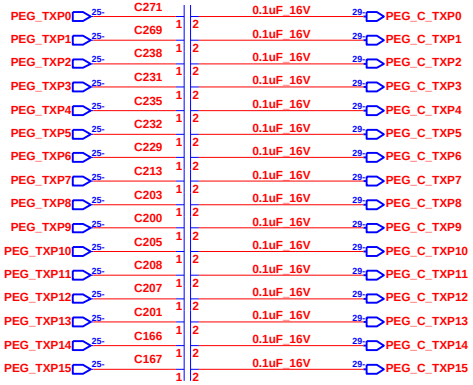
TITLE: *VV09 AMD-DIS*
RS780-1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 24 OF 58







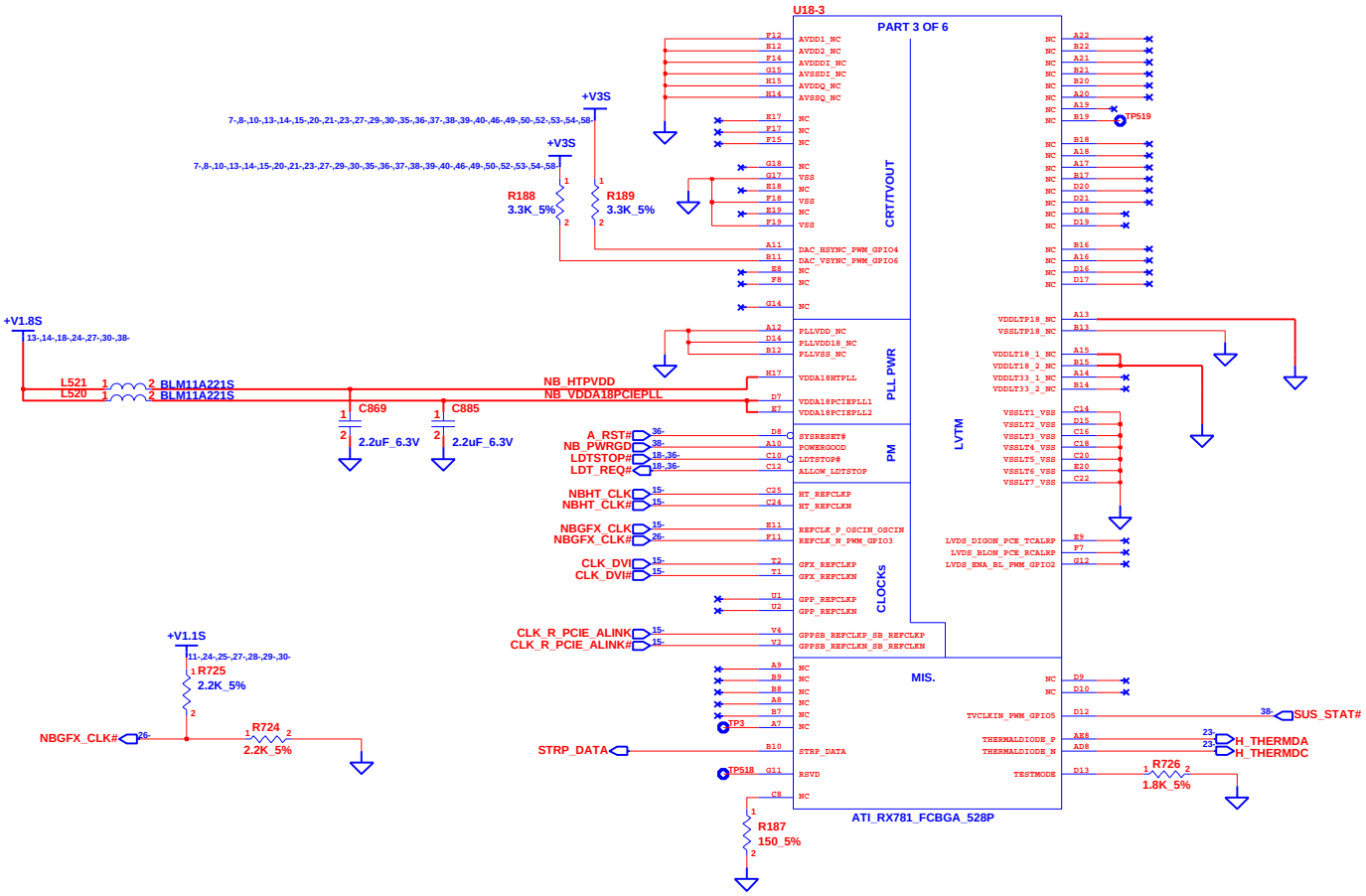
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
RS780-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 25 OF 58



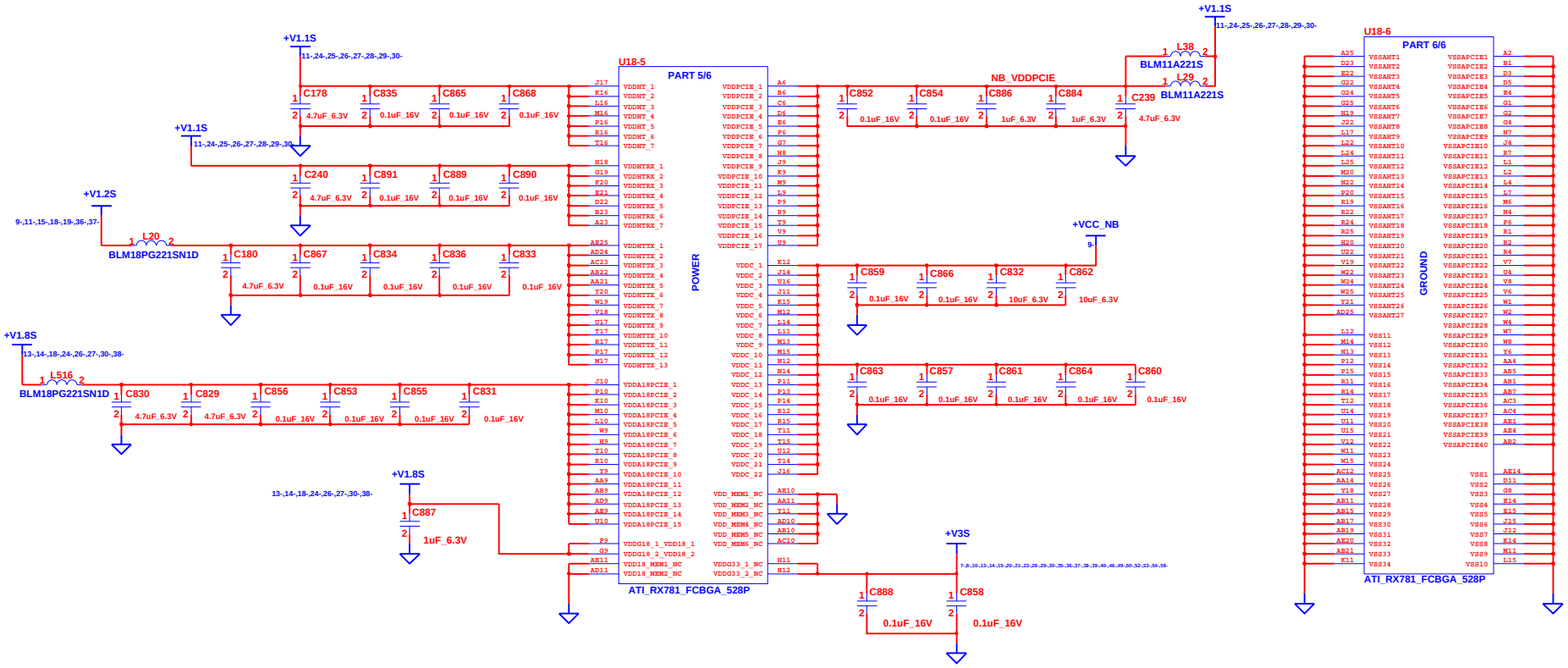
CHANGE by	EDI CHEN	16-Apr-2009			

INVENTEC

TITLE: *VV09 AMD-DIS*
RS780-3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 26 OF 58



CHANGE by	EDI CHEN	16-Apr-2009					

INVENTEC

TITLE: *VV09 AMD-DIS*
RS780-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 27 OF 58

STRAPS	PIN	Description of default settings	
TX_PWRS_ENB	GPIO0	PCIE 50% TX output swing.	1
TX_DEEMPH_EN	GPIO1	PCIE transmitter de-emphasis disabled.	1
BIF_DEBUG_ACCESS	GPIO4	Debug signals muxed out.	0
ROMIDCFG(0:3)	GPIO[11:13,9]	Memory aperture type	X X X X

X = DESIGN DEPENDANT

0 = DO NOT INSTALL RESISTOR

1 = INSTALL 10K RESISTOR

Table 1

GPIO_13	GPIO_12	GPIO_11	For DIS-GDDR2
0	0	1	(512/256M) memory aperture (Default)
1	1	0	reserved

POW_SW1	POW_SW0	+VDD_CORE
0	0	1.0V
0	1	0.95V
1	0	0.9V

Table 2

For DIS-GDDR2				
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	vendor
0	1	1	1	hynix (256MB)
0	1	1	0	Qimonda(256M)
0	1	0	1	Samsung(256MB) (Default)

U12-2 M92-S2 ATI_M92_S2_BGA_631P

U12-3 ATI_M92_S2_BGA_631P

See table 1.

See table 2.

CHANGE by	EDI CHEN	16-Apr-2009		

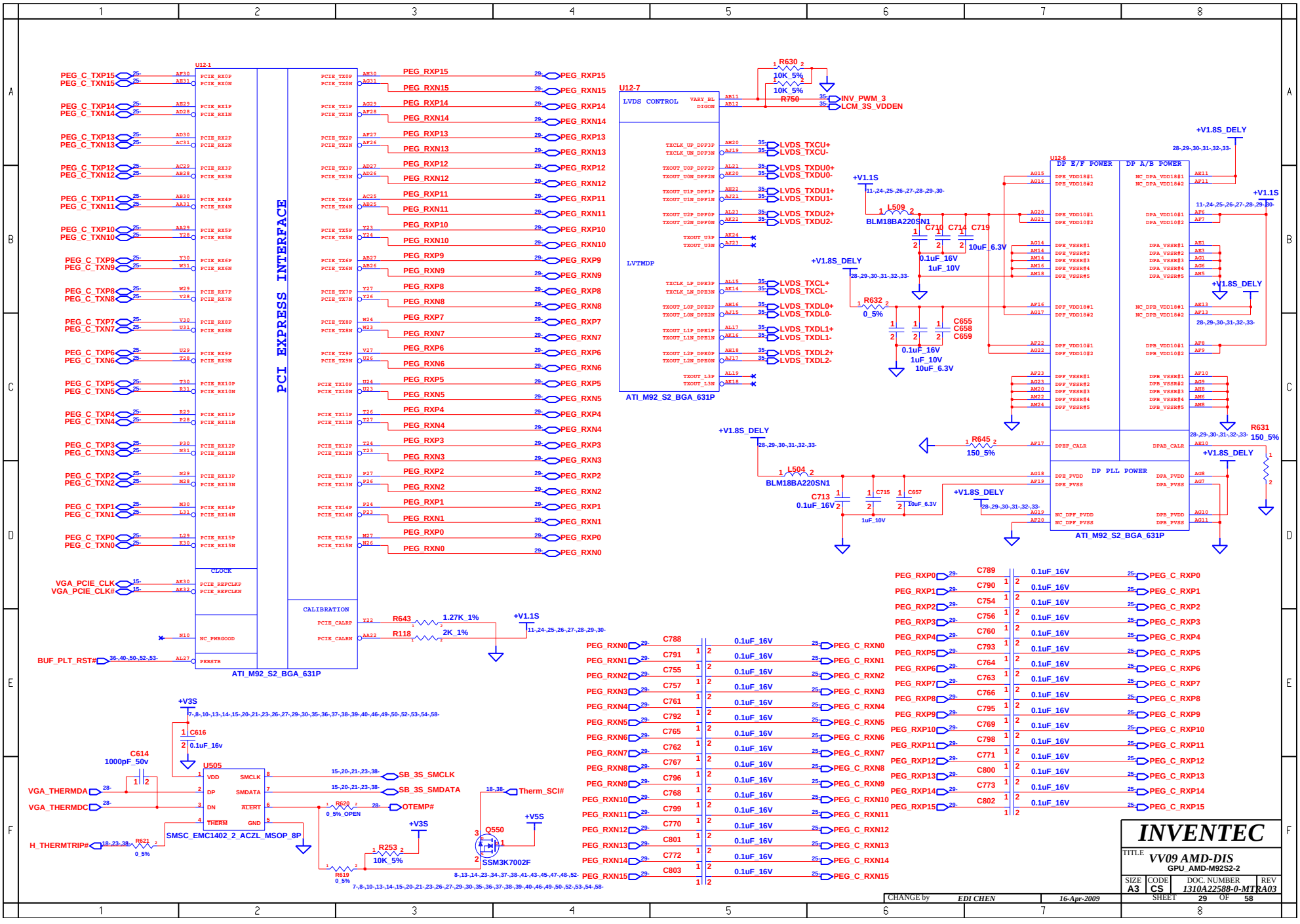
INVENTEC

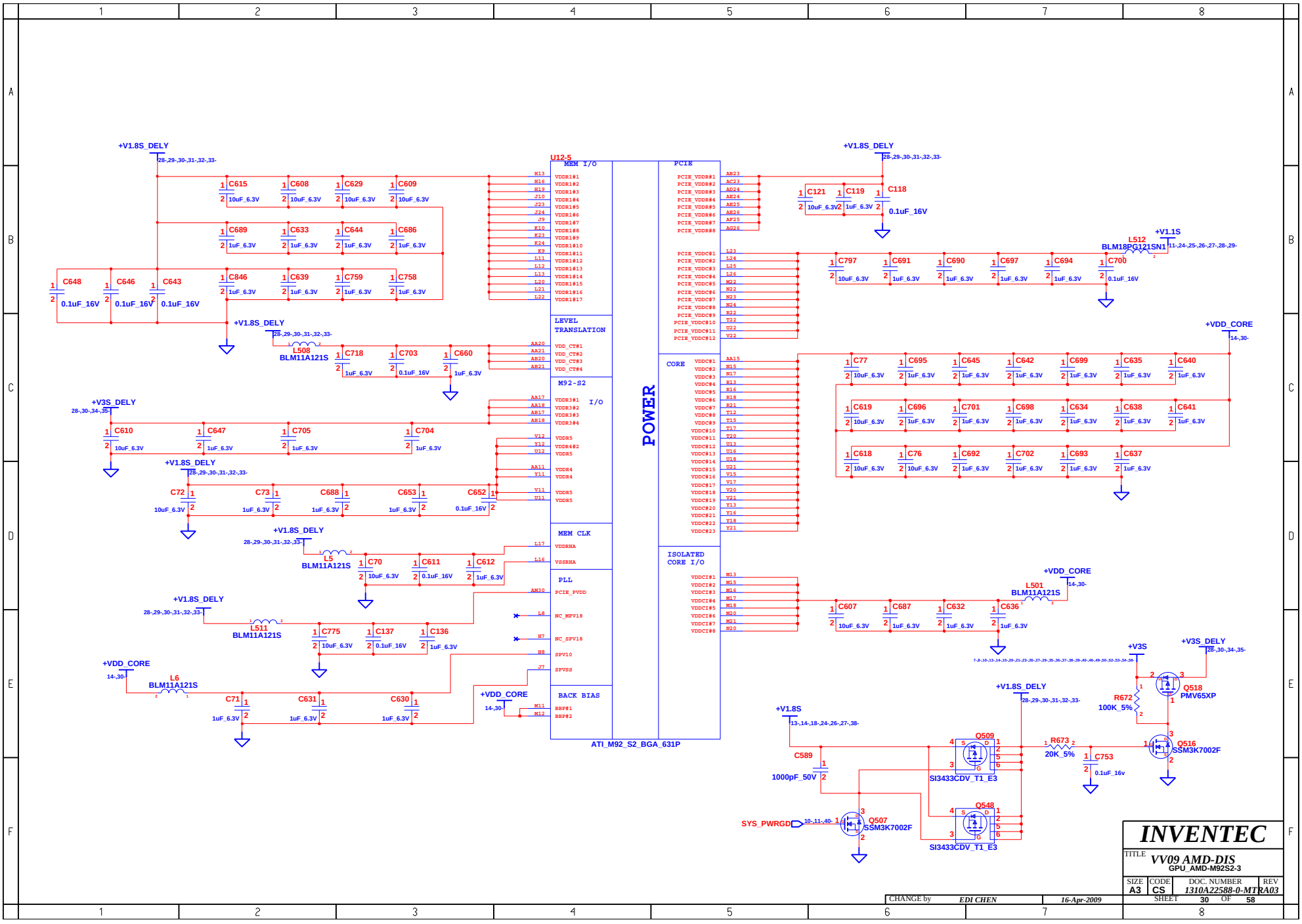
TITLE: VV09 AMD-DIS

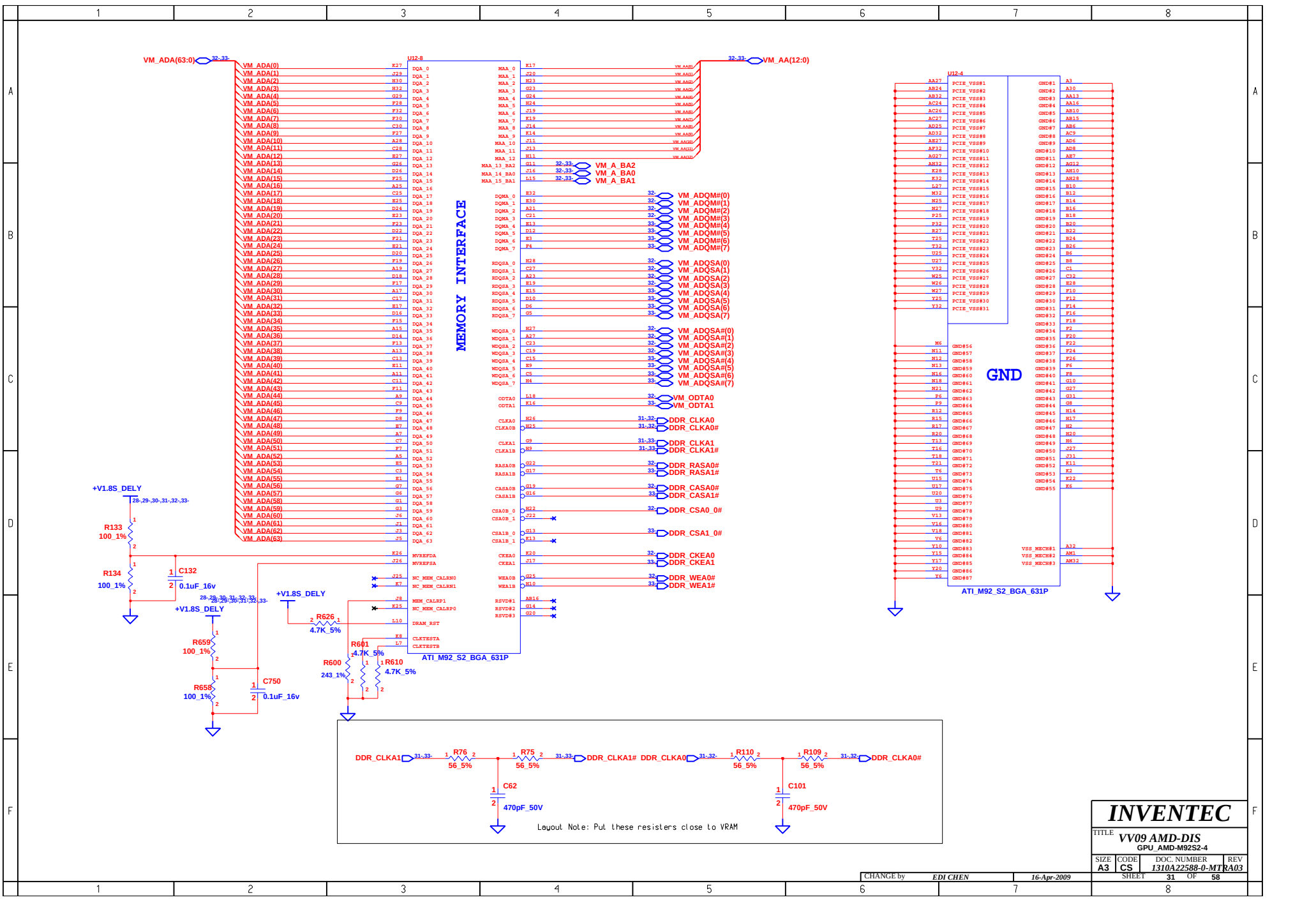
GPU_AMD_M92S2_1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTR	A03

SHEET 28 OF 58


U12-1
PCI EXPRESS INTERFACE
PEG_C_TXP15
PEG_C_TXN15
PEG_C_TXP14
PEG_C_TXN14
PEG_C_TXP13
PEG_C_TXN13
PEG_C_TXP12
PEG_C_TXN12
PEG_C_TXP11
PEG_C_TXN11
PEG_C_TXP10
PEG_C_TXN10
PEG_C_TXP9
PEG_C_TXN9
PEG_C_TXP8
PEG_C_TXN8
PEG_C_TXP7
PEG_C_TXN7
PEG_C_TXP6
PEG_C_TXN6
PEG_C_TXP5
PEG_C_TXN5
PEG_C_TXP4
PEG_C_TXN4
PEG_C_TXP3
PEG_C_TXN3
PEG_C_TXP2
PEG_C_TXN2
PEG_C_TXP1
PEG_C_TXN1
PEG_C_TXP0
PEG_C_TXN0
PEG_RXP15
PEG_RXN15
PEG_RXP14
PEG_RXN14
PEG_RXP13
PEG_RXN13
PEG_RXP12
PEG_RXN12
PEG_RXP11
PEG_RXN11
PEG_RXP10
PEG_RXN10
PEG_RXP9
PEG_RXN9
PEG_RXP8
PEG_RXN8
PEG_RXP7
PEG_RXN7
PEG_RXP6
PEG_RXN6
PEG_RXP5
PEG_RXN5
PEG_RXP4
PEG_RXN4
PEG_RXP3
PEG_RXN3
PEG_RXP2
PEG_RXN2
PEG_RXP1
PEG_RXN1
PEG_RXP0
PEG_RXN0
CLOCK
VGA_PCIE_CLK
VGA_PCIE_CLK#
NC_PWRGOOD
BUF_PLT_RST#
PERSTB
CALIBRATION
R643 1.27K_1%
R118 2K_1%
+V1.1S
ATI_M92_S2_BGA_631P
U12-7
LVDS CONTROL
LVTMDP
R630 10K_5%
R750 10K_5%
INV_PWM_3
LCM_3S_VDDEN
LVDS_TXCU+
LVDS_TXCU-
LVDS_TXDU0+
LVDS_TXDU0-
LVDS_TXDU1+
LVDS_TXDU1-
LVDS_TXDU2+
LVDS_TXDU2-
LVDS_TXCL+
LVDS_TXCL-
LVDS_TXDL0+
LVDS_TXDL0-
LVDS_TXDL1+
LVDS_TXDL1-
LVDS_TXDL2+
LVDS_TXDL2-
ATI_M92_S2_BGA_631P
+V1.8S_DELY
+V1.1S
L509 BLM18BA220SN1
C710 C714 C719
10uF_6.3V
0.1uF_16V
1uF_10V
R632 0_5%
C655 C658 C659
0.1uF_16V
1uF_10V
10uF_6.3V
U12-6
DP E/F POWER
DP A/B POWER
DP PLL POWER
R645 150_5%
L504 BLM18BA220SN1
C713 0.1uF_16V
C715 1uF_10V
C657 10uF_6.3V
R631 150_5%
ATI_M92_S2_BGA_631P
+V3S
C616 0.1uF_16v
C614 1000pF_50v
U505
VGA_THERMDA
VGA_THERMDC
H_THERMTRIP#
SMSC_EMC1402_2_ACZL_MSOP_8P
SB_3S_SMCLK
SB_3S_SMDATA
OTEMP#
Therm_SCI#
R620 0_5%_OPEN
R621 0_5%
R619 0_5%
R253 10K_5%
+V5S
Q550
SSM3K7002F
C788
C791
C755
C757
C761
C792
C765
C762
C767
C796
C768
C799
C770
C801
C772
C803
C789
C790
C754
C756
C760
C793
C764
C763
C766
C795
C769
C798
C771
C800
C773
C802
0.1uF_16V
PEG_C_RXP0
PEG_C_RXP1
PEG_C_RXP2
PEG_C_RXP3
PEG_C_RXP4
PEG_C_RXP5
PEG_C_RXP6
PEG_C_RXP7
PEG_C_RXP8
PEG_C_RXP9
PEG_C_RXP10
PEG_C_RXP11
PEG_C_RXP12
PEG_C_RXP13
PEG_C_RXP14
PEG_C_RXP15
PEG_C_RXN0
PEG_C_RXN1
PEG_C_RXN2
PEG_C_RXN3
PEG_C_RXN4
PEG_C_RXN5
PEG_C_RXN6
PEG_C_RXN7
PEG_C_RXN8
PEG_C_RXN9
PEG_C_RXN10
PEG_C_RXN11
PEG_C_RXN12
PEG_C_RXN13
PEG_C_RXN14
PEG_C_RXN15
INVENTEC
TITLE
VV09 AMD-DIS
GPU_AMD-M92S2-2
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 29 OF 58
CHANGE by EDI CHEN
16-Apr-2009


+V1.8S_DELY
28-,29-,30-,31-,32-,33-
U12-5
MEM I/O
LEVEL TRANSLATION
M92-S2
I/O
MEM CLK
PLL
BACK BIAS
POWER
PCIE
CORE
ISOLATED CORE I/O
ATI_M92_S2_BGA_631P
C615
C608
C629
C609
C689
C633
C644
C686
C648
C646
C643
C846
C639
C759
C758
0.1uF_16V
10uF_6.3V
1uF_6.3V
L508
BLM11A121S
C718
C703
C660
+V3S_DELY
28-,30-,34-,35-
C610
C647
C705
C704
C72
C73
C688
C653
C652
L5
C70
C611
C612
L511
C775
C137
C136
+VDD_CORE
14-,30-
L6
C71
C631
C630
+V1.8S_DELY
C121
C119
C118
+V1.1S
11-,24-,25-,26-,27-,28-,29-
L512
BLM18PG121SN1
C797
C691
C690
C697
C694
C700
C77
C695
C645
C642
C699
C635
C640
C619
C696
C701
C698
C634
C638
C641
C618
C76
C692
C702
C693
C637
C607
C687
C632
C636
L501
BLM11A121S
+V3S
+V3S_DELY
28-,30-,34-,35-
Q518
PMV65XP
R672
100K_5%
+V1.8S
13-,14-,18-,24-,26-,27-,38-
Q509
SI3433CDV_T1_E3
R673
20K_5%
Q516
SSM3K7002F
C589
1000pF_50V
C753
0.1uF_16v
Q548
SI3433CDV_T1_E3
SYS_PWRGD
10-,11-,40-
Q507
SSM3K7002F
INVENTEC
TITLE
VV09 AMD-DIS
GPU_AMD-M92S2-3
SIZE
A3
CODE
CS
DOC. NUMBER
1310A22588-0-MTRA03
REV
SHEET
30
OF
58
CHANGE by
EDI CHEN
16-Apr-2009



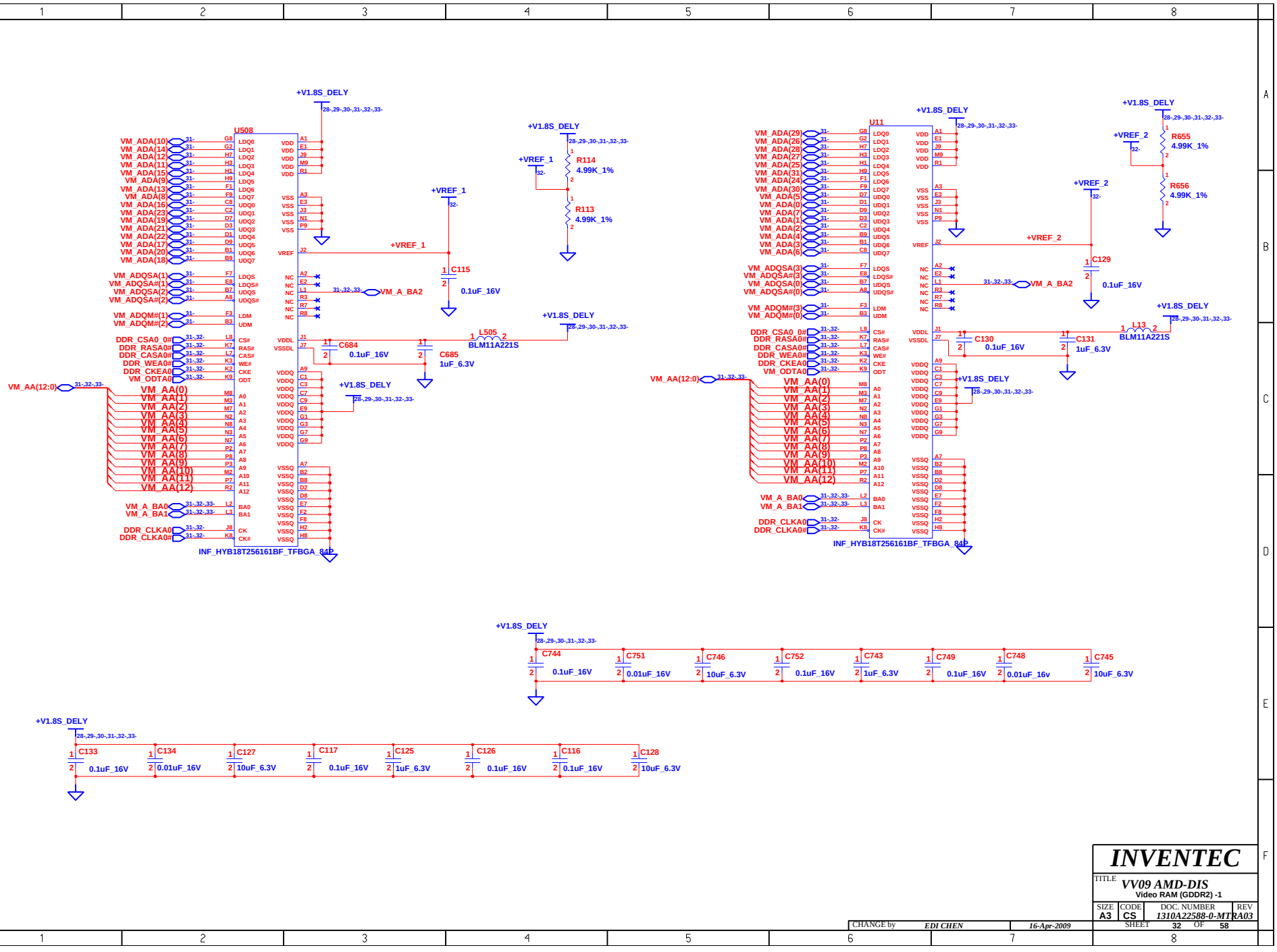
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: VV09 AMD-DIS
GPU_AMD-M92S2-4

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTRA03	

SHEET 31 OF 58



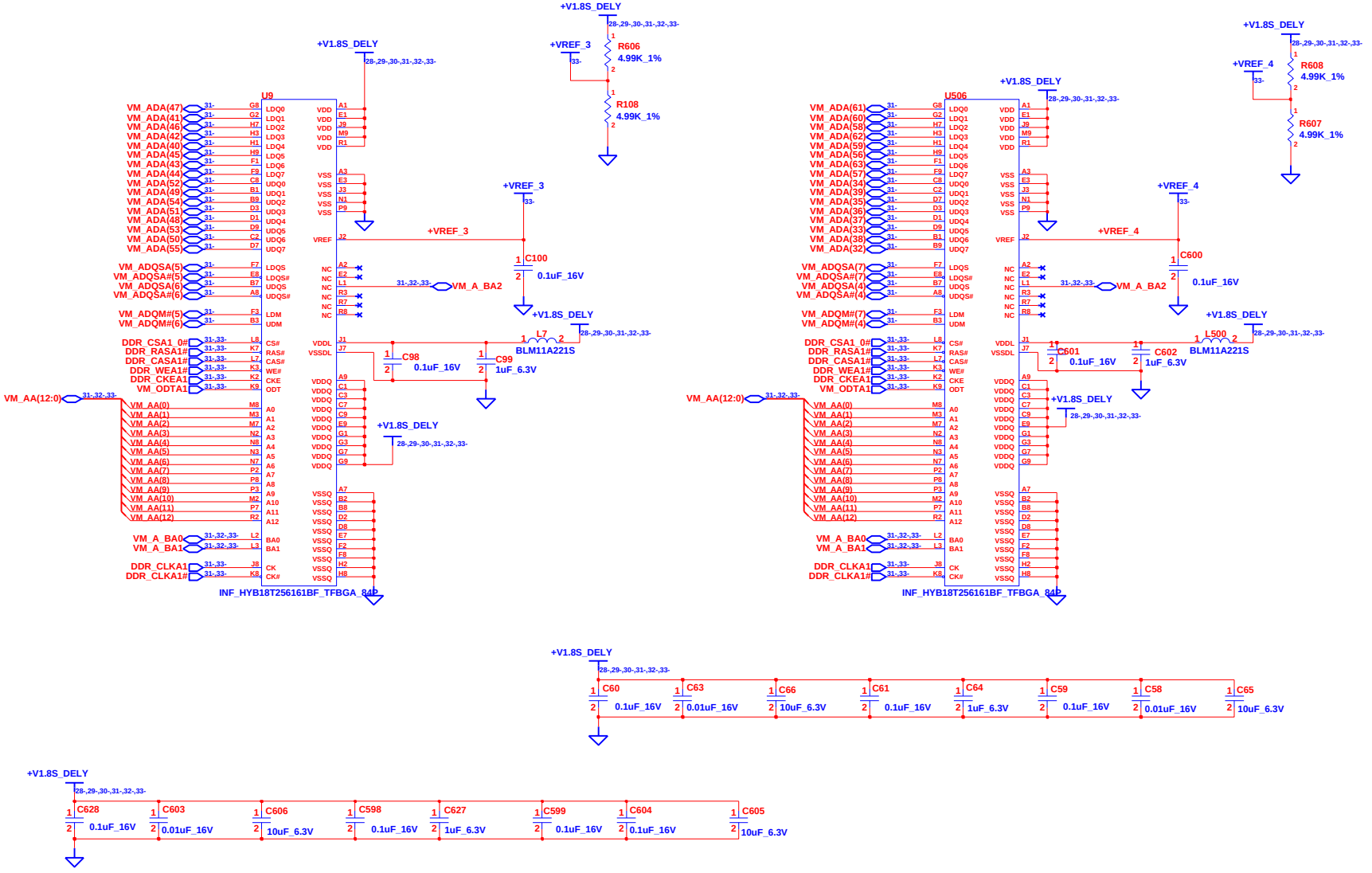
CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC

TITLE: *VV09 AMD-DIS*
Video RAM (GDDR2) -1

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 32 OF 58



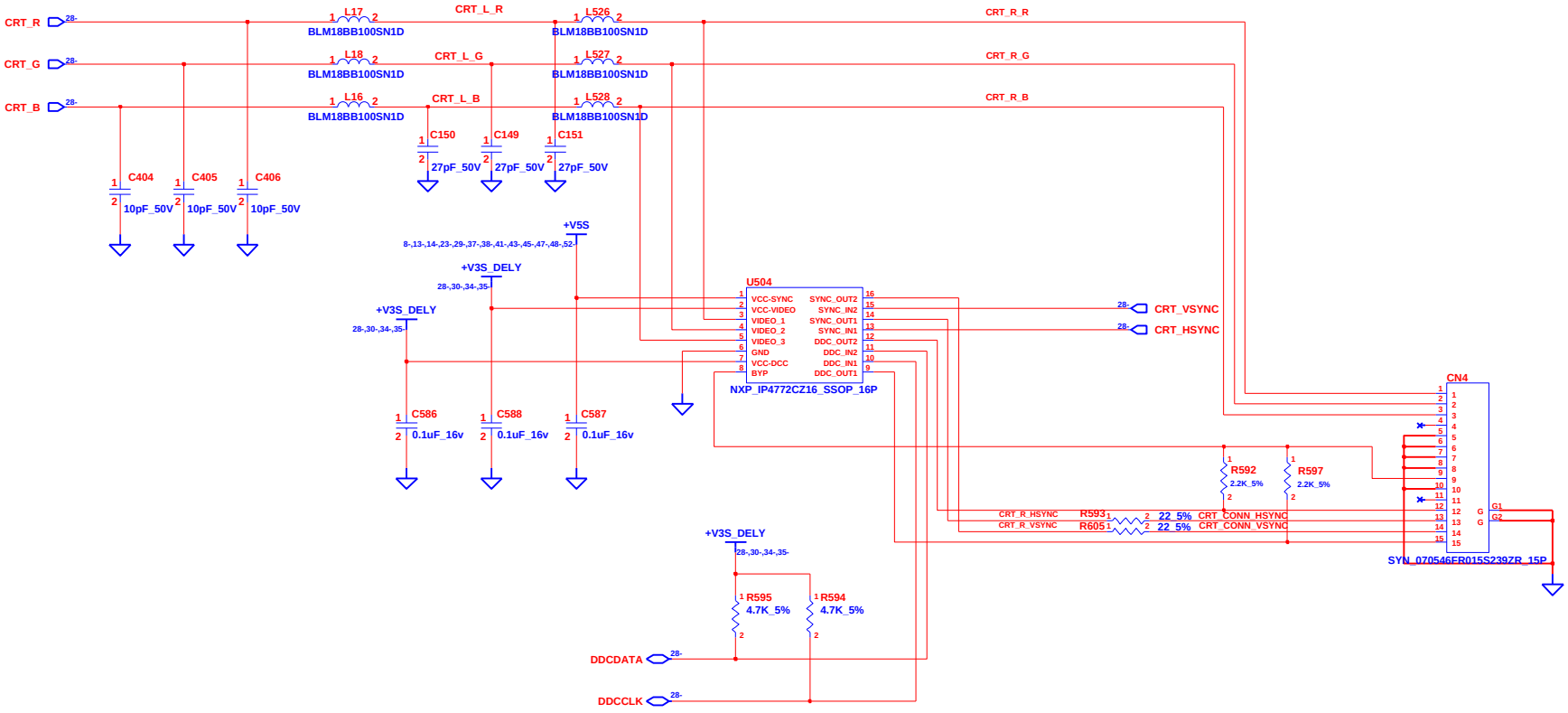
CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC

TITLE: *VV09 AMD-DIS*
Video RAM (GDDR2)-2

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 33 OF 58



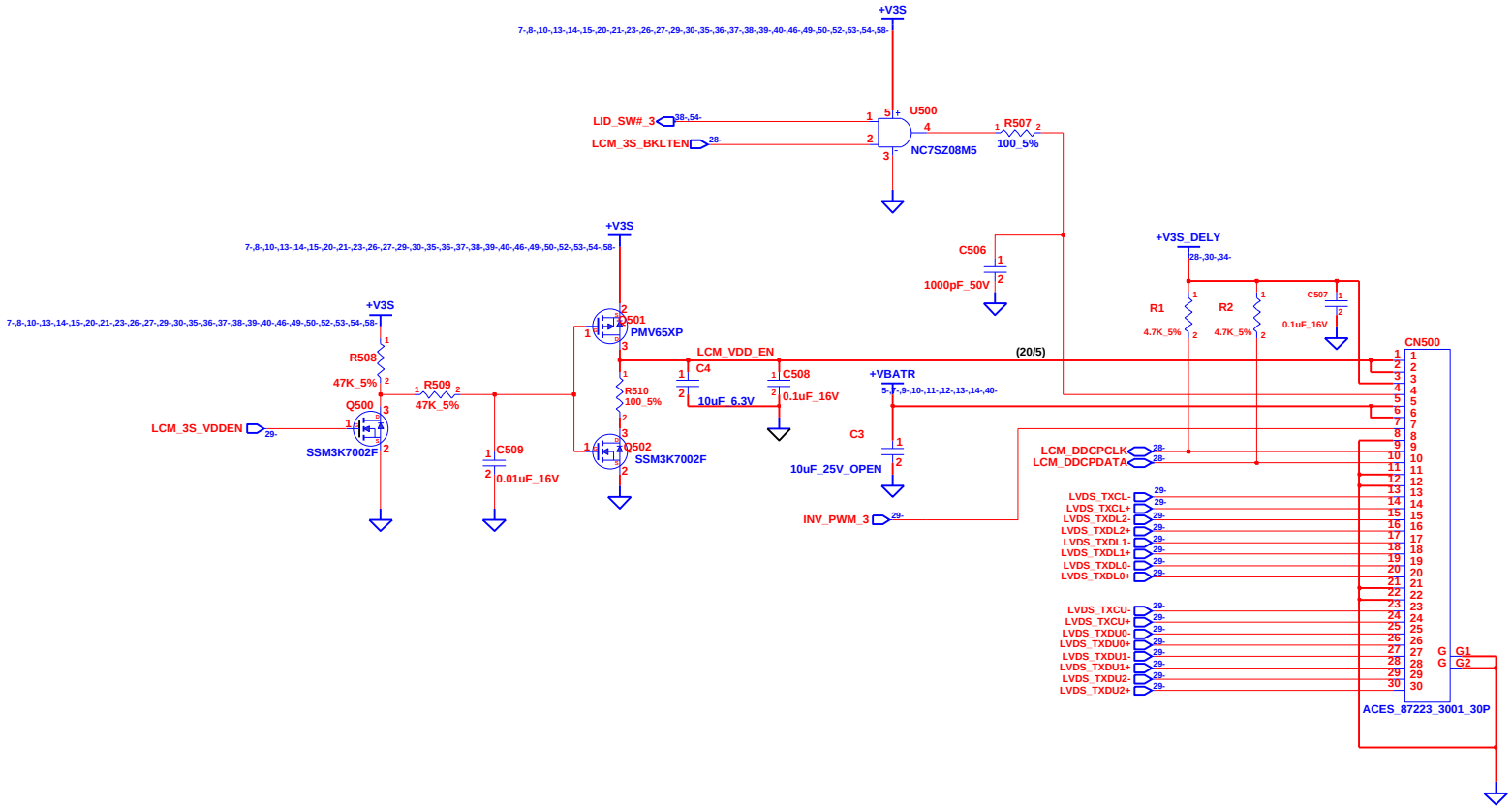
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
CRT

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 34 OF 58



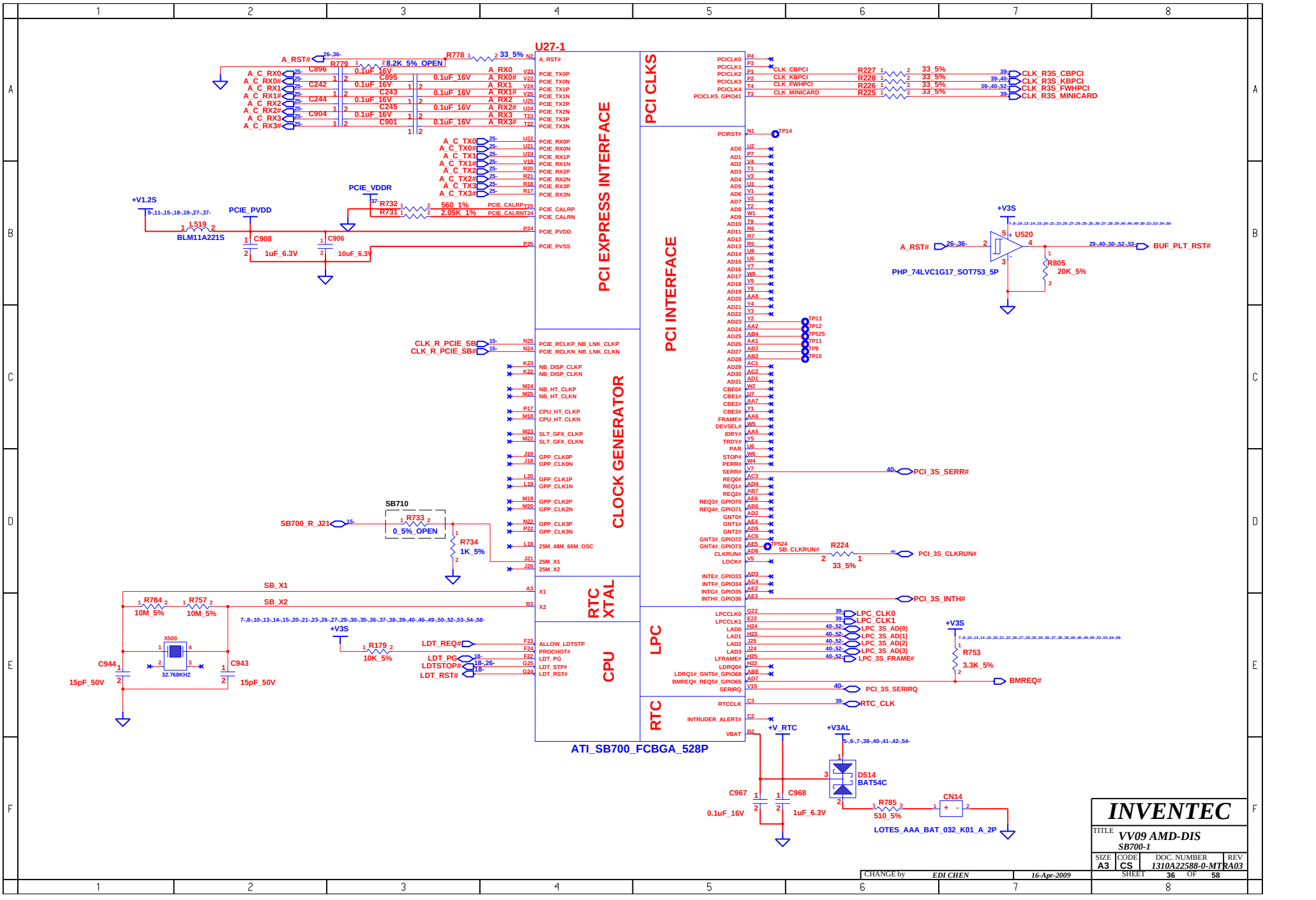
CHANGE by	EDI CHEN	16-Apr-2009		

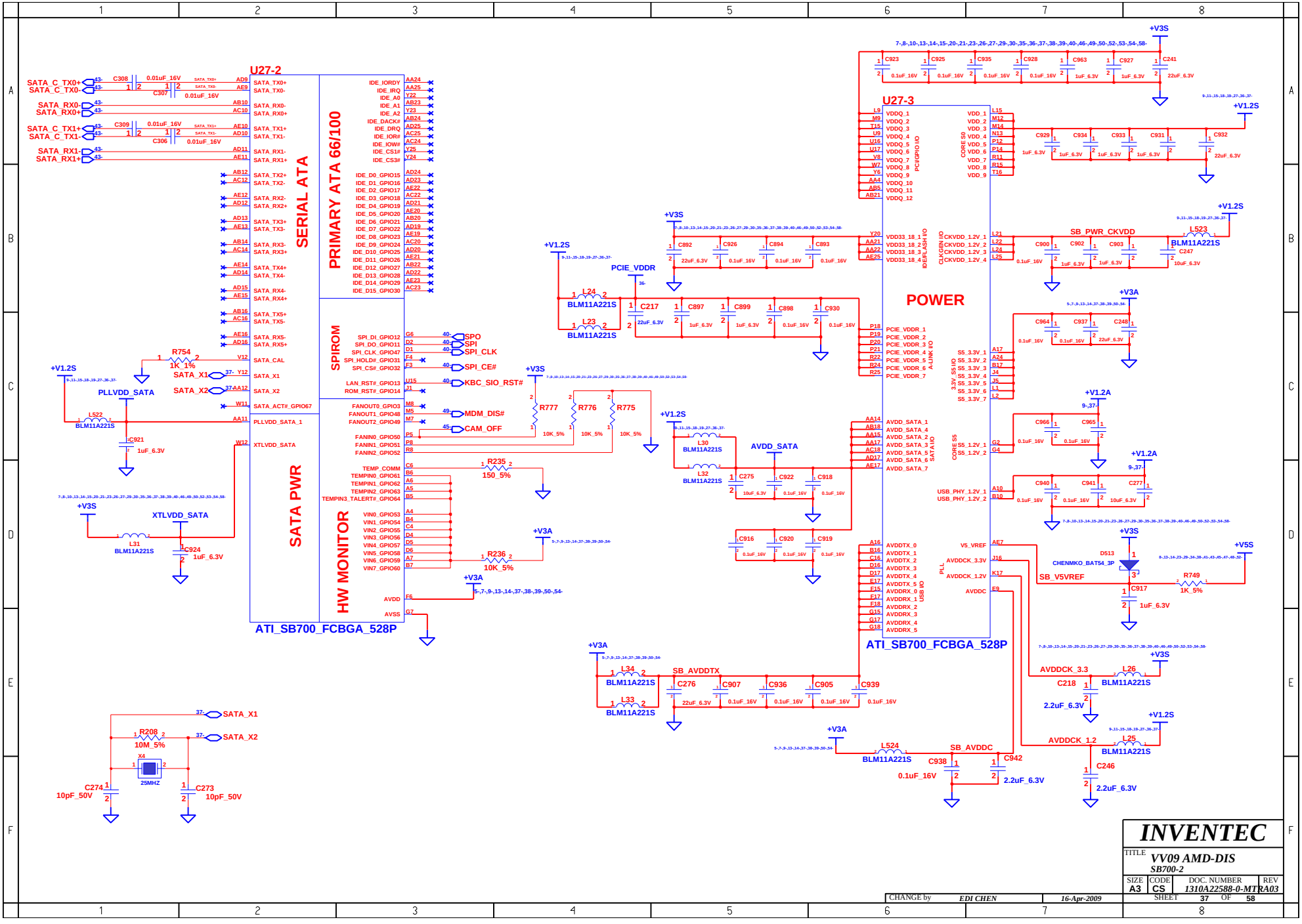
INVENTEC

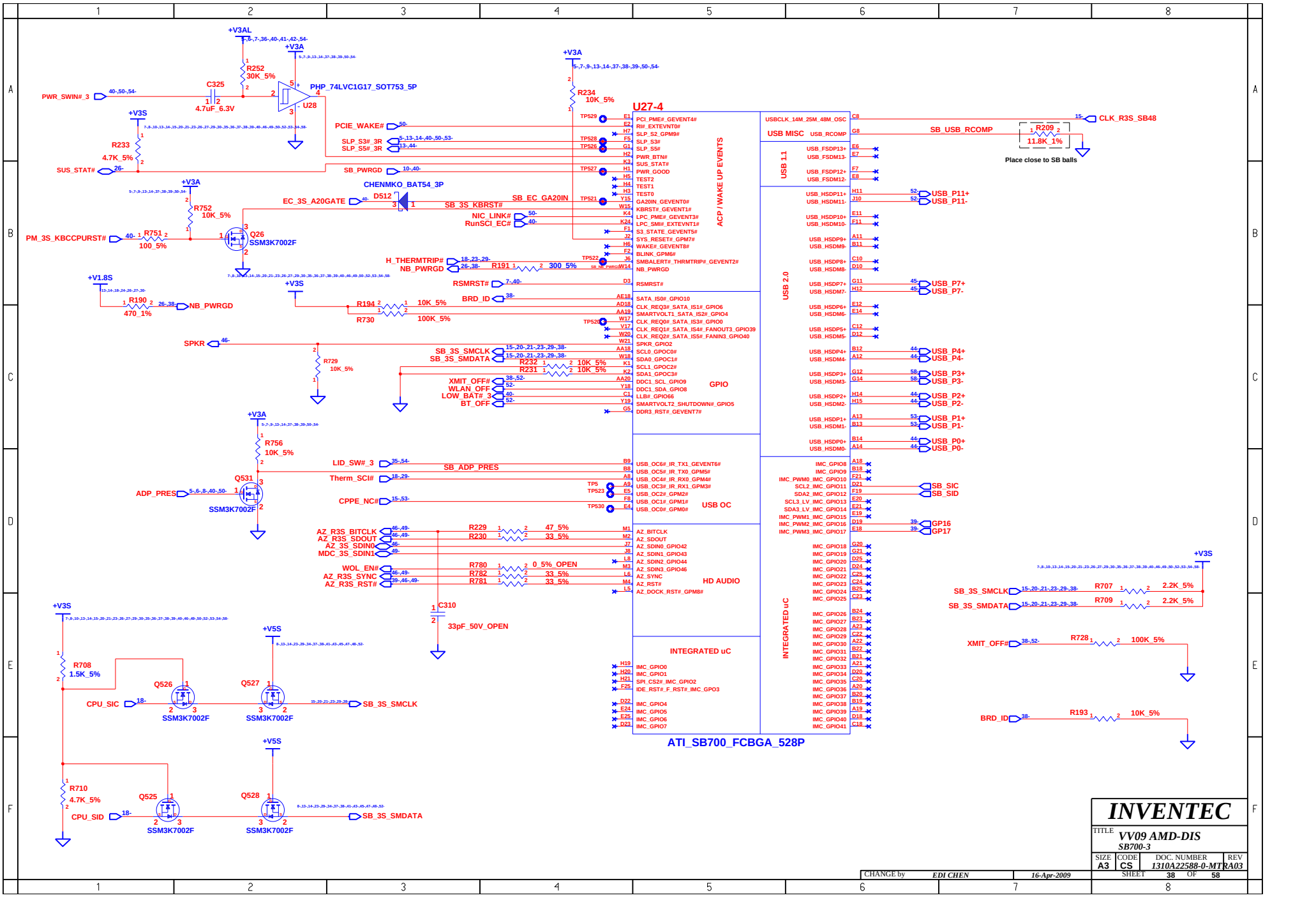
TITLE: *VV09 AMD-DIS*
LCD CONN

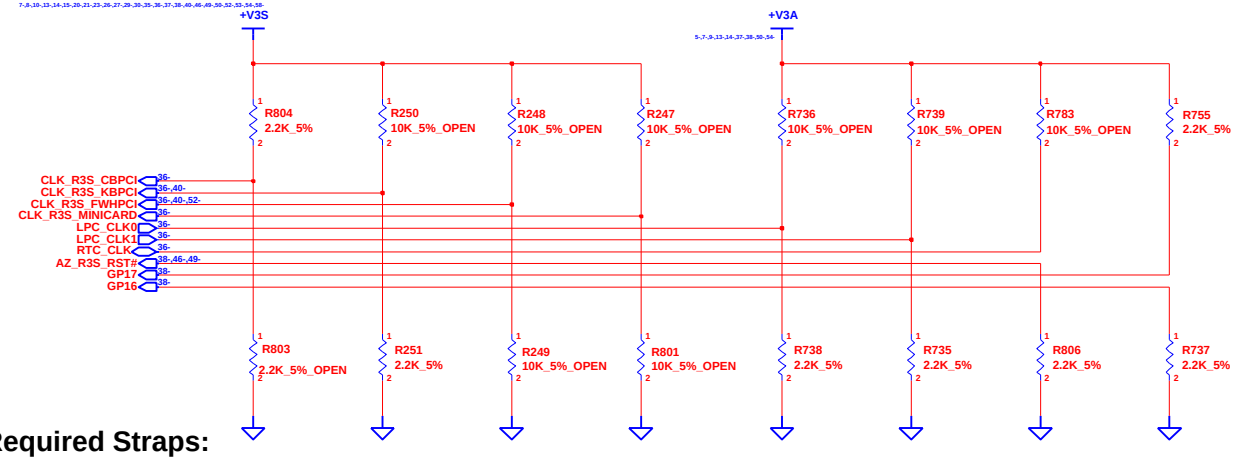
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

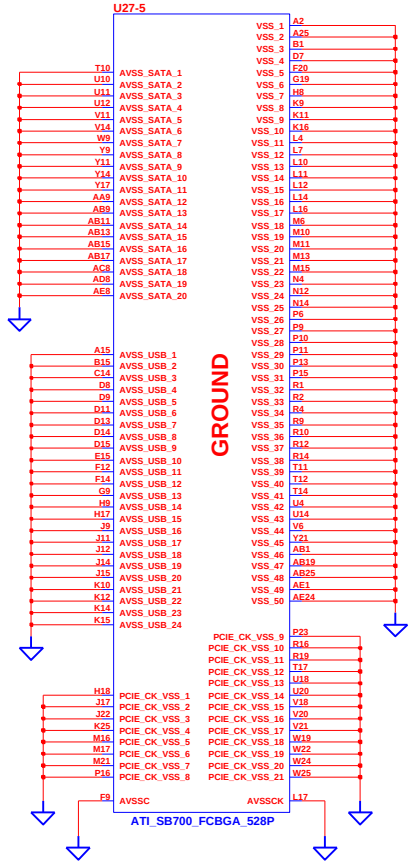
SHEET 35 OF 58


U27-1
PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
CPU
LPC
RTC
ATI_SB700_FCBGA_528P
A_RST#
R778 33_5%
R779 8.2K_5%_OPEN
A_C_RX0 A_C_RX0# A_C_RX1 A_C_RX1# A_C_RX2 A_C_RX2# A_C_RX3 A_C_RX3#
C896 C895 C242 C243 C244 C245 C904 C901 0.1uF_16V
A_RX0 A_RX0# A_RX1 A_RX1# A_RX2 A_RX2# A_RX3 A_RX3#
A_C_TX0 A_C_TX0# A_C_TX1 A_C_TX1# A_C_TX2 A_C_TX2# A_C_TX3 A_C_TX3#
PCIE_VDDR
R732 560_1%
R731 2.05K_1%
PCIE_CALRP PCIE_CALRN
+V1.2S
L519 BLM11A221S
PCIE_PVDD
C908 1uF_6.3V
C906 10uF_6.3V
PCIE_PVSS
CLK_R_PCIE_SB CLK_R_PCIE_SB#
SB710
SB700_R_J21
R733 0_5%_OPEN
R734 1K_5%
SB_X1 SB_X2
R784 10M_5%
R757 10M_5%
X500 32.768KHZ
C944 C943 15pF_50V
+V3S
R179 10K_5%
LDT_REQ# LDT_PG LDTSTOP# LDT_RST#
R227 R228 R226 R225 33_5%
CLK_CBPCI CLK_KBPCI CLK_FWHPCI CLK_MINICARD
CLK_R3S_CBPCI CLK_R3S_KBPCI CLK_R3S_FWHPCI CLK_R3S_MINICARD
PCIRST#
PCI_3S_SERR#
SB_CLKRUN#
R224 33_5%
PCI_3S_CLKRUN#
PCI_3S_INTH#
LPC_CLK0 LPC_CLK1
LPC_3S_AD(0) LPC_3S_AD(1) LPC_3S_AD(2) LPC_3S_AD(3)
LPC_3S_FRAME#
R753 3.3K_5%
BMREQ#
PCI_3S_SERIRQ
RTC_CLK
+V_RTC
+V3AL
D514 BAT54C
C967 0.1uF_16V
C968 1uF_6.3V
R785 510_5%
CN14 LOTES_AAA_BAT_032_K01_A_2P
+V3S
U520 PHP_74LVC1G17_SOT753_5P
R805 20K_5%
BUF_PLT_RST#
INVENTEC
TITLE VV09 AMD-DIS
SB700-1
SIZE A3 CODE CS DOC. NUMBER 1310A22588-0-MTRA03 REV
SHEET 36 OF 58
CHANGE by EDI CHEN 16-Apr-2009


U27-2
SERIAL ATA
PRIMARY ATA 66/100
SPIROM
SATA PWR
HW MONITOR
ATI_SB700_FCBGA_528P
U27-3
POWER
ATI_SB700_FCBGA_528P
INVENTEC
TITLE
VV09 AMD-DIS
SB700-2
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 37 OF 58
CHANGE by EDI CHEN
16-Apr-2009


U27-4
ATI_SB700_FCBGA_528P
PHP_74LVC1G17_SOT753_5P
SSM3K7002F
CHENMKO_BAT54_3P
ACP / WAKE UP EVENTS
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
USB MISC
PWR_SWIN#_3
PCIE_WAKE#
SLP_S3#_3R
SLP_S5#_3R
SUS_STAT#
SB_PWRGD
EC_3S_A20GATE
SB_3S_KBRST#
NIC_LINK#
RunSCI_EC#
PM_3S_KBCCPURST#
H_THERMTRIP#
NB_PWRGD
RSMRST#
BRD_ID
SPKR
SB_3S_SMCLK
SB_3S_SMDATA
XMIT_OFF#
WLAN_OFF
LOW_BAT#_3
BT_OFF
LID_SW#_3
Therm_SCI#
ADP_PRES
CPPE_NC#
AZ_R3S_BITCLK
AZ_R3S_SDOUT
AZ_3S_SDIN0
MDC_3S_SDIN1
WOL_EN#
AZ_R3S_SYNC
AZ_R3S_RST#
CPU_SIC
CPU_SID
SB_USB_RCOMP
CLK_R3S_SB48
Place close to SB balls
USB_P11+
USB_P11-
USB_P7+
USB_P7-
USB_P4+
USB_P4-
USB_P3+
USB_P3-
USB_P2+
USB_P2-
USB_P1+
USB_P1-
USB_P0+
USB_P0-
SB_SIC
SB_SID
GP16
GP17
INVENTEC
VV09 AMD-DIS
SB700-3
1310A22588-0-MTRA03
CHANGE by EDI CHEN 16-Apr-2009





Required Straps:

	CLK_R3S_CBPCI	CLK_R3S_KBPCI	CLK_R3S_FWHPCI	CLK_R3S _MINICARD	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE H, H = Reserved H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK	EC DISABLED DEFAULT	

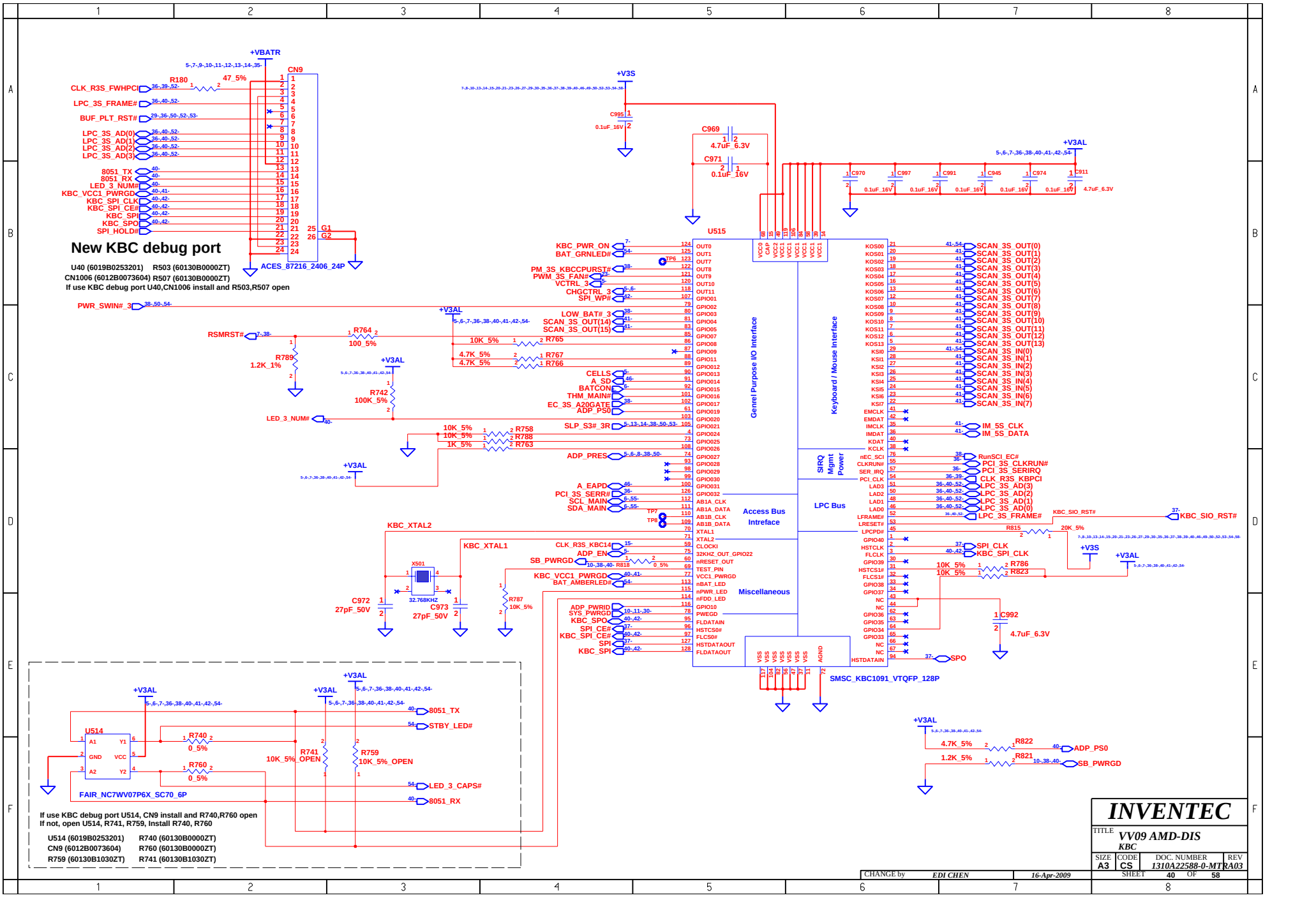
CHANGE by	EDI CHEN	16-Apr-2009	

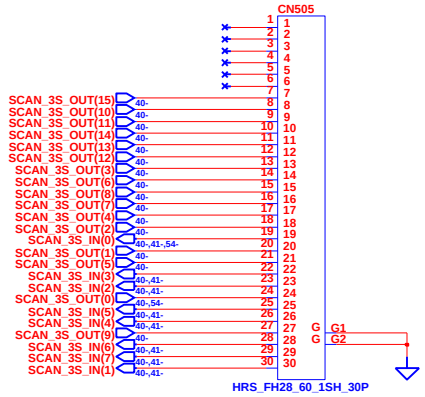
INVENTEC

TITLE: *VV09 AMD-DIS*
SB700-4

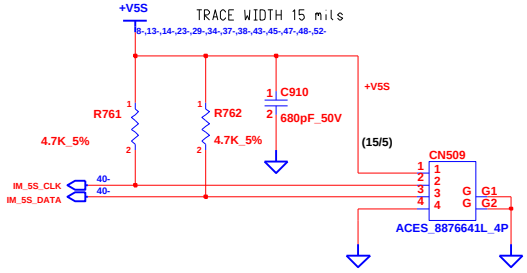
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 39 OF 58

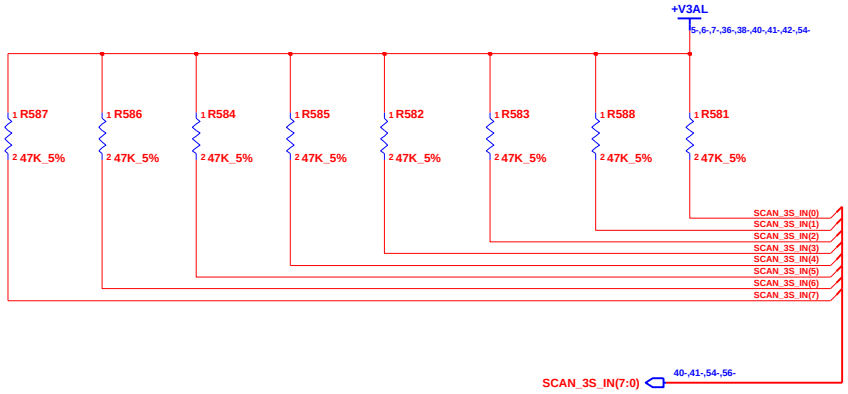

New KBC debug port
U40 (6019B0253201) R503 (60130B0000ZT)
CN1006 (6012B0073604) R507 (60130B0000ZT)
If use KBC debug port U40,CN1006 install and R503,R507 open
ACES_87216_2406_24P
SMSC_KBC1091_VTQFP_128P
FAIR_NC7WV07P6X_SC70_6P
If use KBC debug port U514, CN9 install and R740,R760 open
If not, open U514, R741, R759, Install R740, R760
U514 (6019B0253201) R740 (60130B0000ZT)
CN9 (6012B0073604) R760 (60130B0000ZT)
R759 (60130B1030ZT) R741 (60130B1030ZT)
INVENTEC
TITLE VV09 AMD-DIS
KBC
SIZE A3 CODE CS DOC. NUMBER 1310A22588-0-MTRA03 REV
SHEET 40 OF 58
CHANGE by EDI CHEN 16-Apr-2009

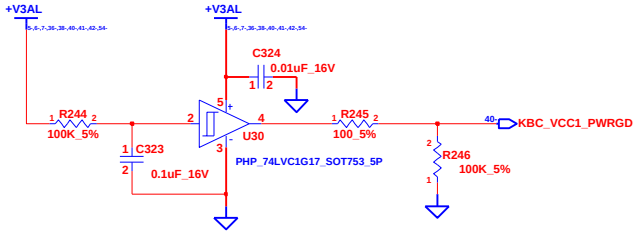


KEYBOARD CONN



TOUCH PAD CNTR





U35 should be placed close to U39.

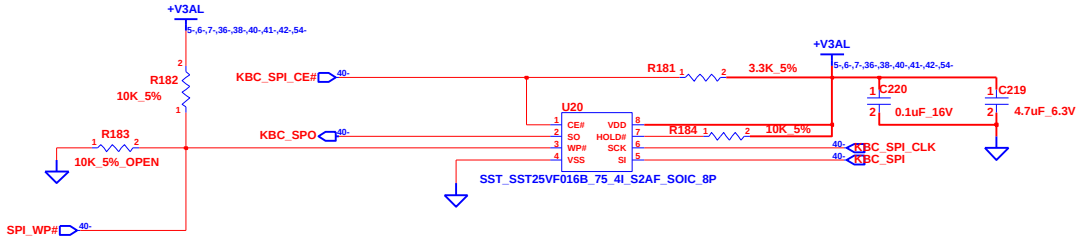
CHANGE by	*EDI CHEN*	*16-Apr-2009*		

INVENTEC

TITLE: ***VV09 AMD-DIS***
KB&TP CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 41 OF 58

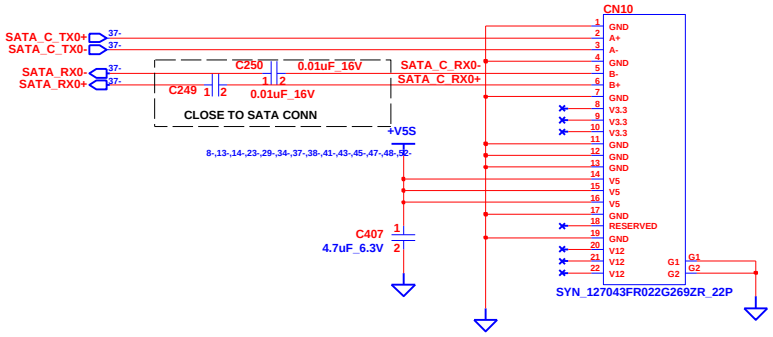


SPI Flash

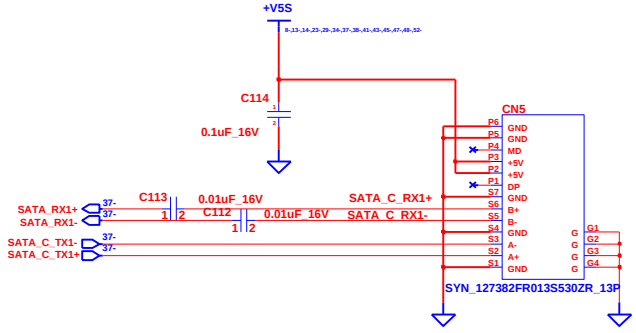
CHANGE by	EDI CHEN	16-Apr-2009		

INVENTEC

TITLE	VV09 AMD-DIS SPI		
SIZE A3	CODE CS	DOC. NUMBER 1310A22588-0-MTRA03	REV 03
		SHEET 42 OF 58	



HDD CONNECTOR



ODD SATA CONNECTOR

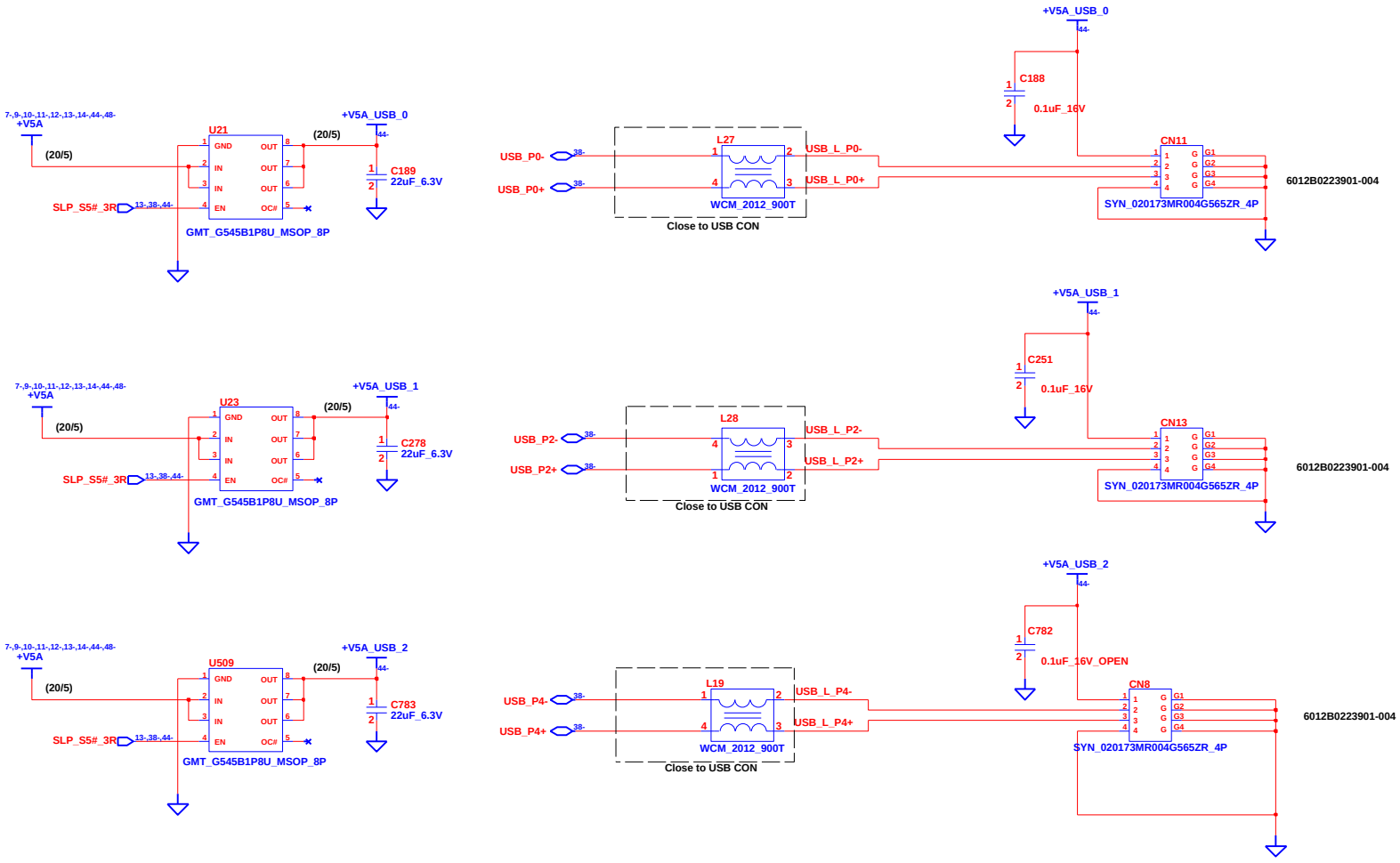
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
HDD & ODD CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 43 OF 58



CHANGE by	EDI CHEN	16-Apr-2009	

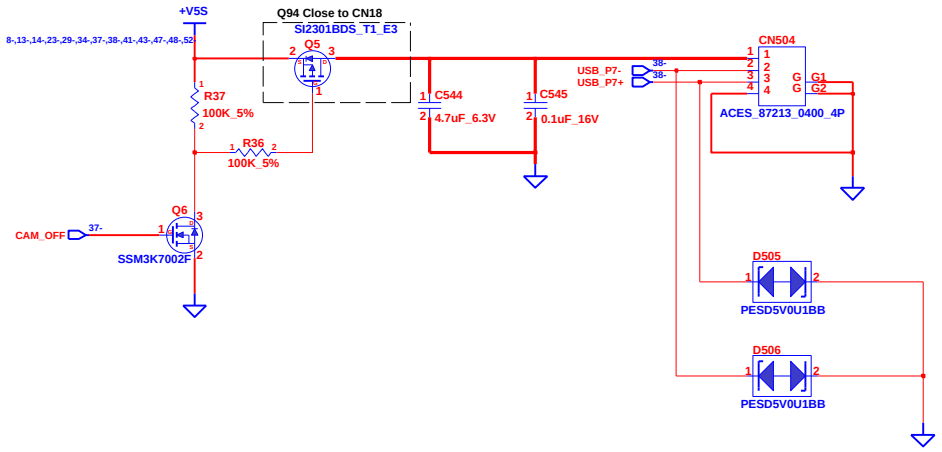
INVENTEC

TITLE: *VV09 AMD-DIS*
USB CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 44 OF 58

(At least 20mils.)



USB WEBCAM CONNECTOR

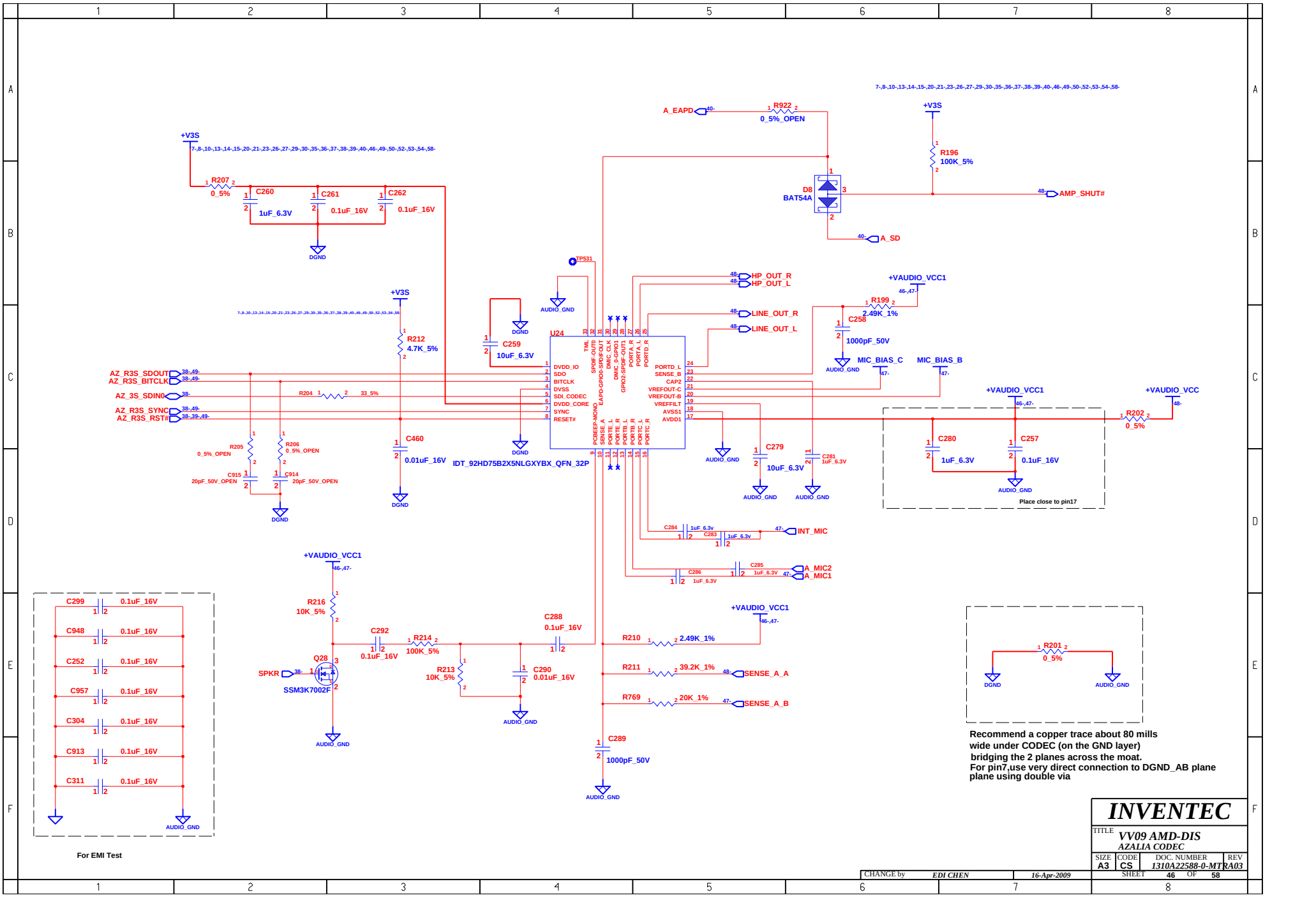
CHANGE by	EDI CHEN	16-Apr-2009			

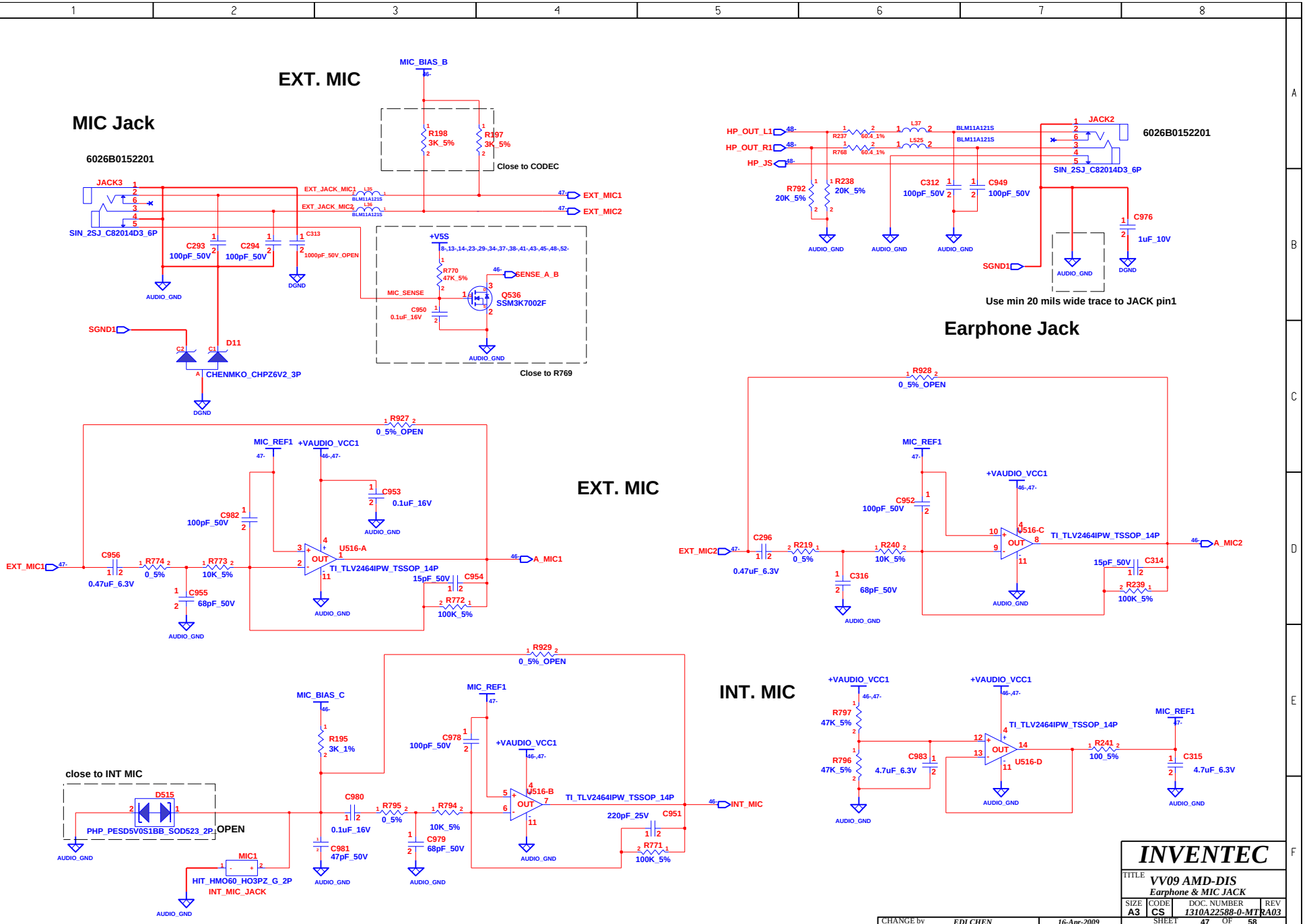
INVENTEC

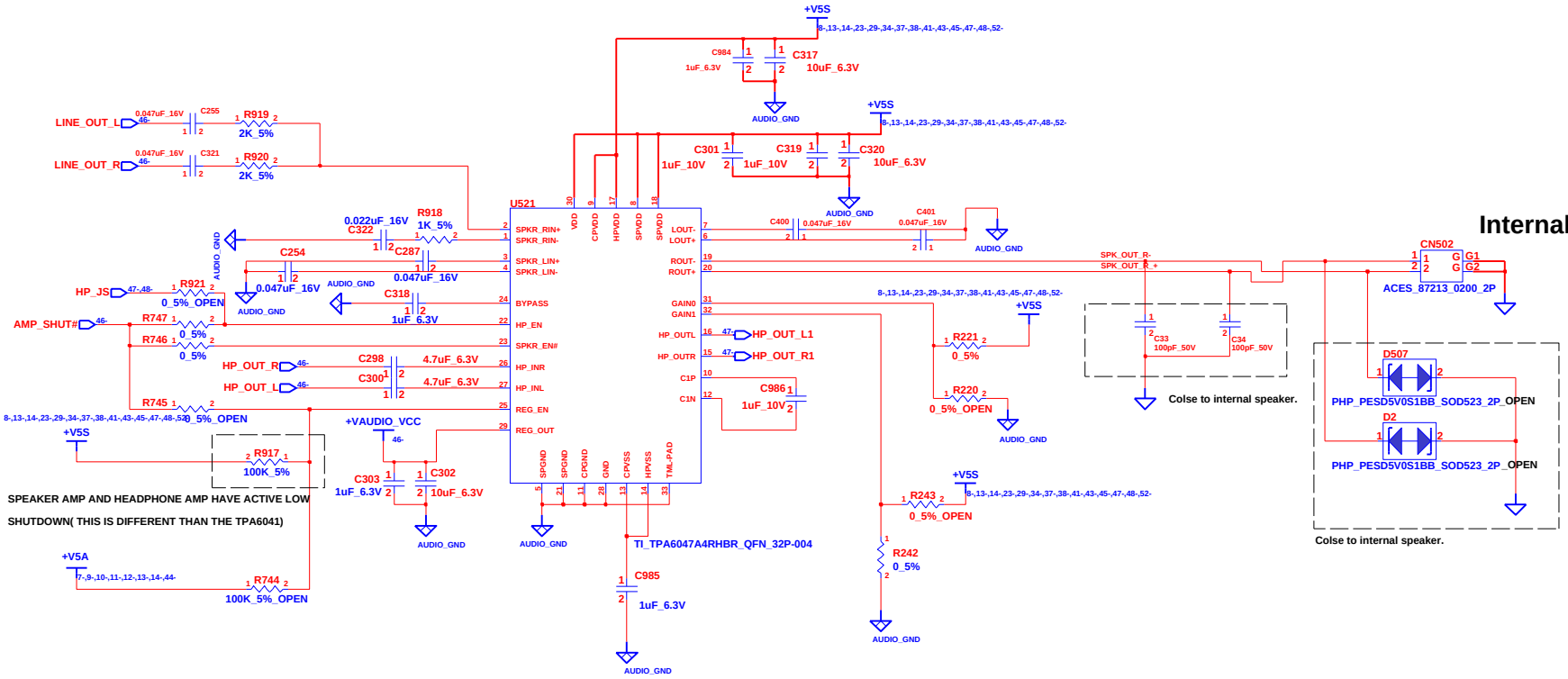
TITLE: *VV09 AMD-DIS*
USB WEBCAM CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

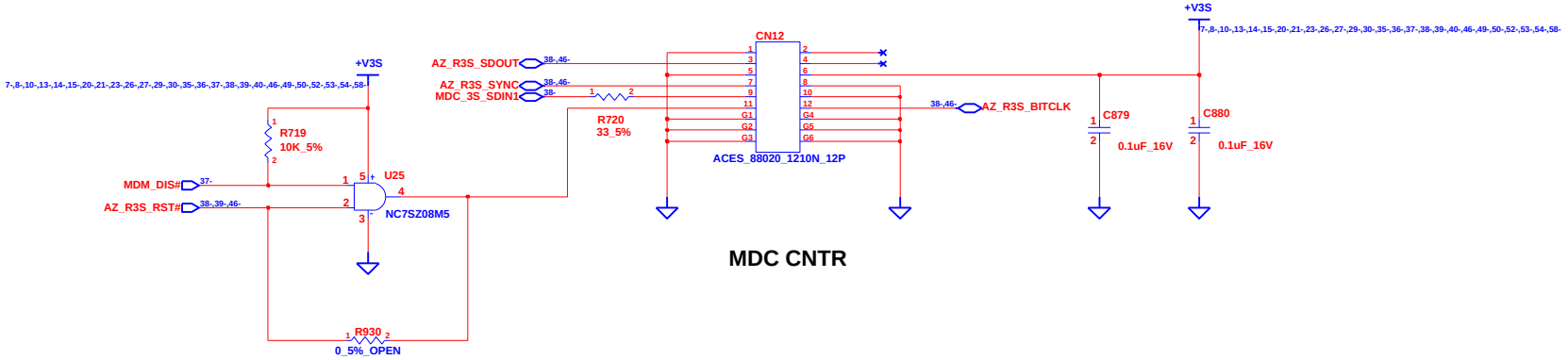
SHEET 45 OF 58


+V3S
R207 0_5%
C260 1uF_6.3V
C261 0.1uF_16V
C262 0.1uF_16V
DGND
A_EAPD
R922 0_5%_OPEN
D8 BAT54A
R196 100K_5%
AMP_SHUT#
A_SD
TPS31
AUDIO_GND
HP_OUT_R
HP_OUT_L
LINE_OUT_R
LINE_OUT_L
+VAUDIO_VCC1
R199 2.49K_1%
C258 1000pF_50V
MIC_BIAS_C
MIC_BIAS_B
R212 4.7K_5%
C259 10uF_6.3V
U24
IDT_92HD75B2X5NLGXYBX_QFN_32P
AZ_R3S_SDOUT
AZ_R3S_BITCLK
AZ_3S_SDIN0
AZ_R3S_SYNC
AZ_R3S_RST#
R204 33_5%
R205 0_5%_OPEN
R206 0_5%_OPEN
C915 20pF_50V_OPEN
C914 20pF_50V_OPEN
C460 0.01uF_16V
C279 10uF_6.3V
C281 1uF_6.3V
+VAUDIO_VCC
R202 0_5%
C280 1uF_6.3V
C257 0.1uF_16V
Place close to pin17
C284 1uF_6.3v
C283 1uF_6.3v
INT_MIC
C285 1uF_6.3V
C286 1uF_6.3V
A_MIC2
A_MIC1
R216 10K_5%
C292 0.1uF_16V
R214 100K_5%
C288 0.1uF_16V
R213 10K_5%
C290 0.01uF_16V
Q28 SSM3K7002F
SPKR
R210 2.49K_1%
R211 39.2K_1%
SENSE_A_A
R769 20K_1%
SENSE_A_B
C289 1000pF_50V
C299 0.1uF_16V
C948 0.1uF_16V
C252 0.1uF_16V
C957 0.1uF_16V
C304 0.1uF_16V
C913 0.1uF_16V
C311 0.1uF_16V
For EMI Test
R201 0_5%
Recommend a copper trace about 80 mills wide under CODEC (on the GND layer) bridging the 2 planes across the moat.
For pin7,use very direct connection to DGND_AB plane plane using double via
INVENTEC
TITLE VV09 AMD-DIS
AZALIA CODEC
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 46 OF 58
CHANGE by EDI CHEN
16-Apr-2009


EXT. MIC
MIC Jack
6026B0152201
MIC_BIAS_B
R198 3K_5%
R197 3K_5%
Close to CODEC
JACK3
SIN_2SJ_C82014D3_6P
EXT_JACK_MIC1
EXT_JACK_MIC2
EXT_MIC1
EXT_MIC2
C293 100pF_50V
C294 100pF_50V
C313 1000pF_50V_OPEN
AUDIO_GND
DGND
+V5S
R770 47K_5%
SENSE_A_B
MIC_SENSE
Q536 SSM3K7002F
C950 0.1uF_16V
SGND1
D11
CHENMKO_CHPZ6V2_3P
Close to R769
HP_OUT_L1
HP_OUT_R1
HP_JS
R237 60.4_1%
R768 60.4_1%
L37 BLM11A121S
L525 BLM11A121S
JACK2
SIN_2SJ_C82014D3_6P
6026B0152201
R792 20K_5%
R238 20K_5%
C312 100pF_50V
C949 100pF_50V
C976 1uF_10V
Use min 20 mils wide trace to JACK pin1
Earphone Jack
R927 0_5%_OPEN
MIC_REF1
+VAUDIO_VCC1
C953 0.1uF_16V
C982 100pF_50V
C956 0.47uF_6.3V
R774 0_5%
R773 10K_5%
C955 68pF_50V
U516-A
TI_TLV2464IPW_TSSOP_14P
C954 15pF_50V
R772 100K_5%
EXT_MIC1
A_MIC1
EXT. MIC
R928 0_5%_OPEN
C952 100pF_50V
C296 0.47uF_6.3V
R219 0_5%
R240 10K_5%
C316 68pF_50V
U516-C
C314 15pF_50V
R239 100K_5%
EXT_MIC2
A_MIC2
R929 0_5%_OPEN
MIC_BIAS_C
R195 3K_1%
C978 100pF_50V
close to INT MIC
D515
PHP_PESD5V0S1BB_SOD523_2P
OPEN
C980 0.1uF_16V
R795 0_5%
R794 10K_5%
C979 68pF_50V
C981 47pF_50V
MIC1
HIT_HMO60_HO3PZ_G_2P
INT_MIC_JACK
U516-B
C951 220pF_25V
R771 100K_5%
INT_MIC
INT. MIC
R797 47K_5%
R796 47K_5%
C983 4.7uF_6.3V
U516-D
R241 100_5%
C315 4.7uF_6.3V
INVENTEC
TITLE
VV09 AMD-DIS
Earphone & MIC JACK
SIZE A3
CODE CS
DOC. NUMBER 1310A22588-0-MTRA03
REV
SHEET 47 OF 58
CHANGE by EDI CHEN 16-Apr-2009



INVENTEC			
TITLE	VV09 AMD-DIS AUDIO AMP & HP JACK		
SIZE A3	CODE CS	DOC. NUMBER 1310A22588-0-MTRA03	REV
CHANGE by EDI CHEN	16-Apr-2009	SHEET 48 OF 58	



MDC CNTR

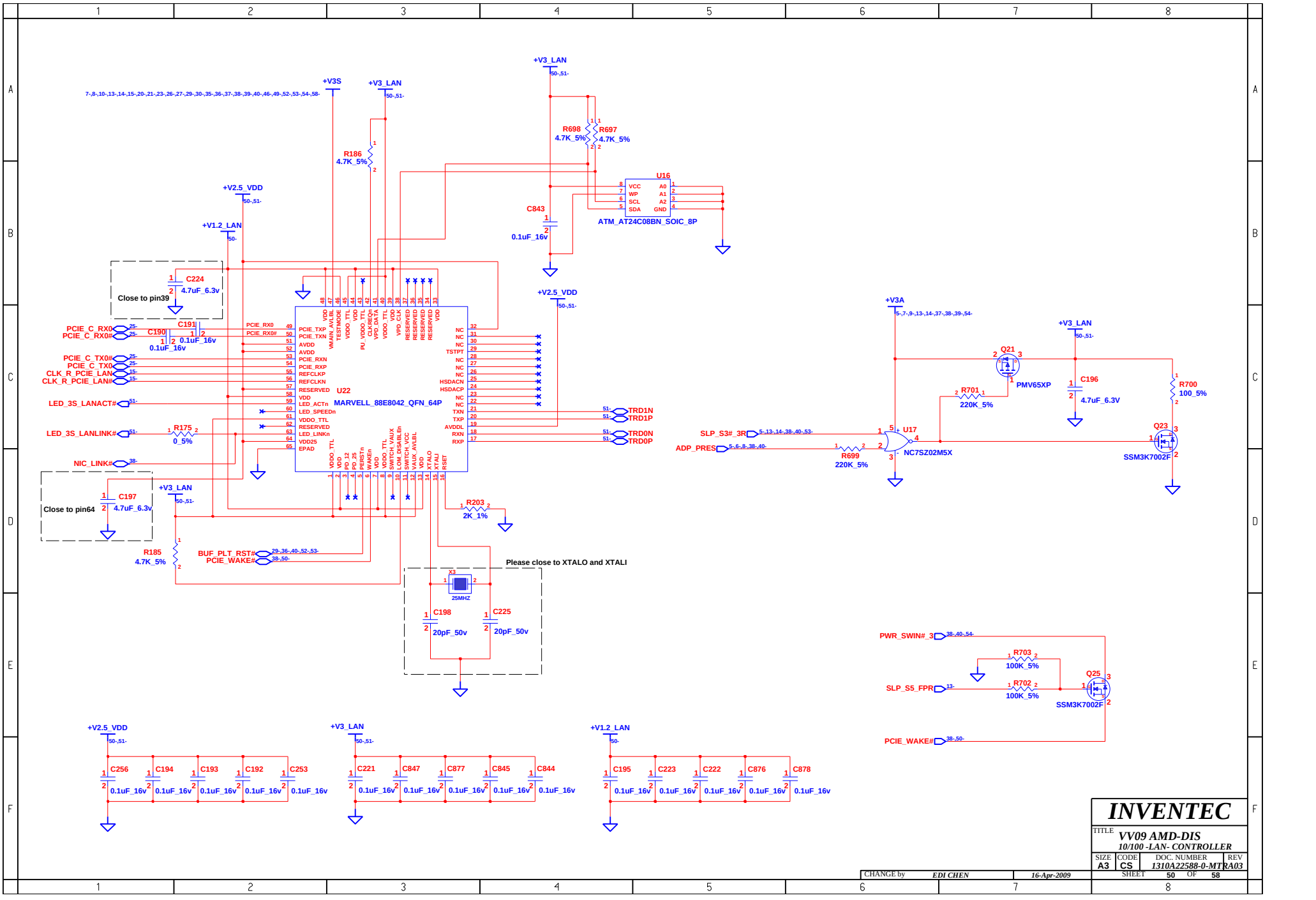
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
MDC CNTR

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 49 OF 58



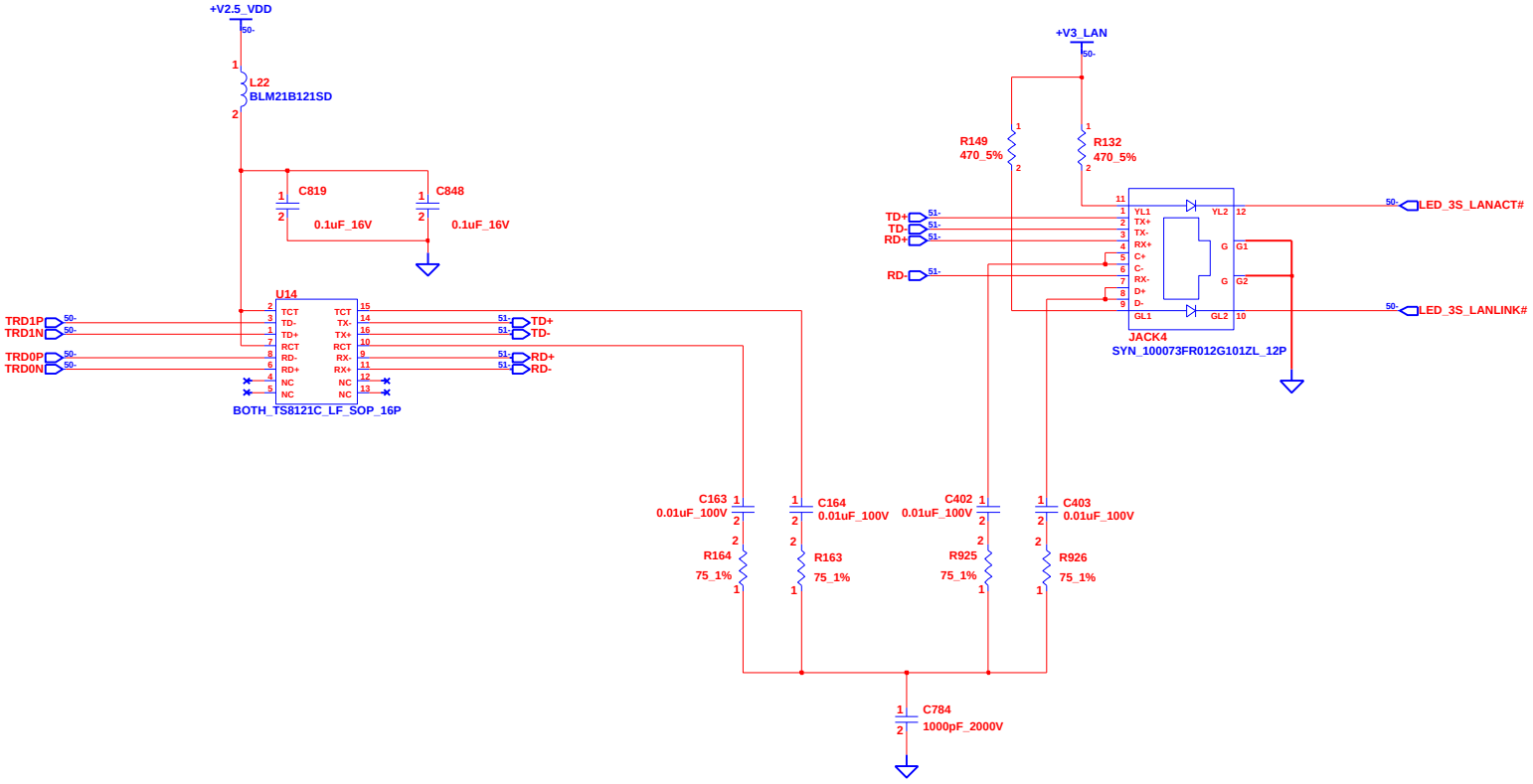
CHANGE by	EDI CHEN
	16-Apr-2009

INVENTEC

TITLE: *VV09 AMD-DIS*
10/100 -LAN- CONTROLLER

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 50 OF 58



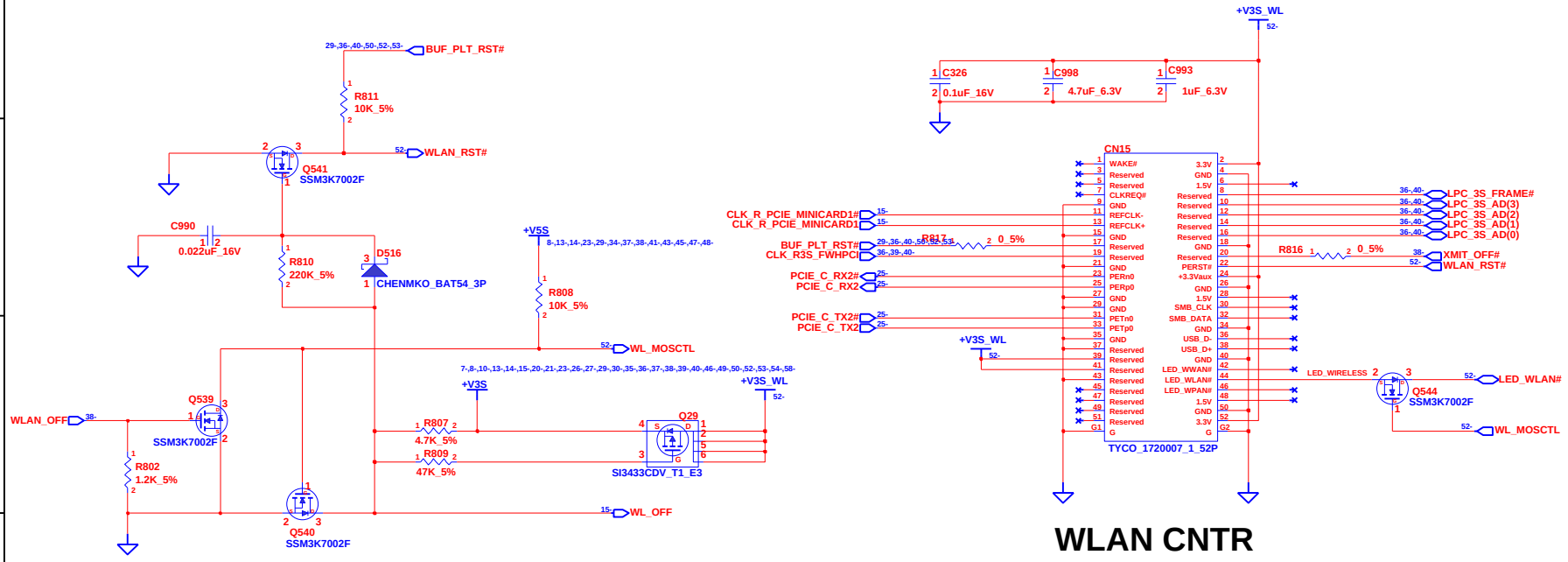
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

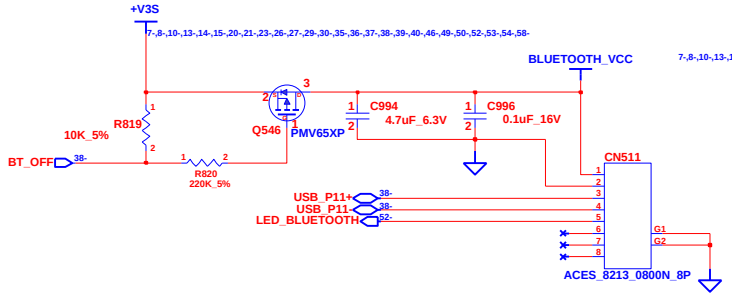
TITLE: *VV09 AMD-DIS*
NIC 10/100-RJ45 CONN

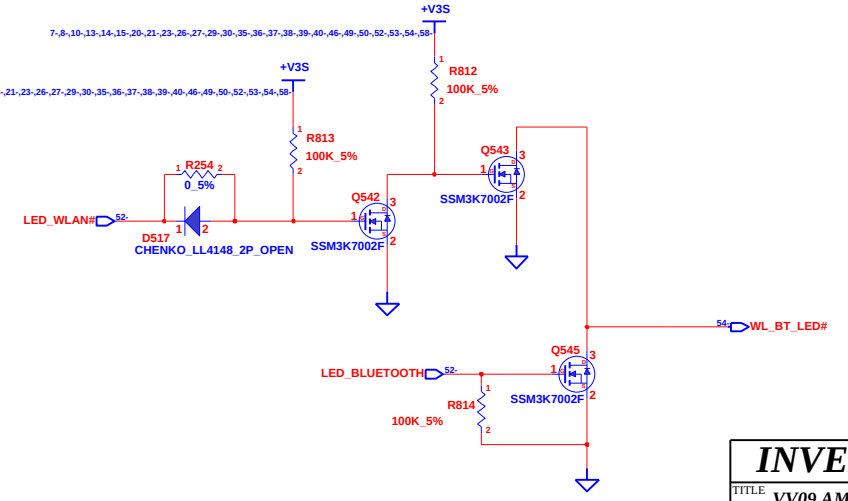
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 51 OF 58



WLAN CNTR





BLUETOOTH CNTR

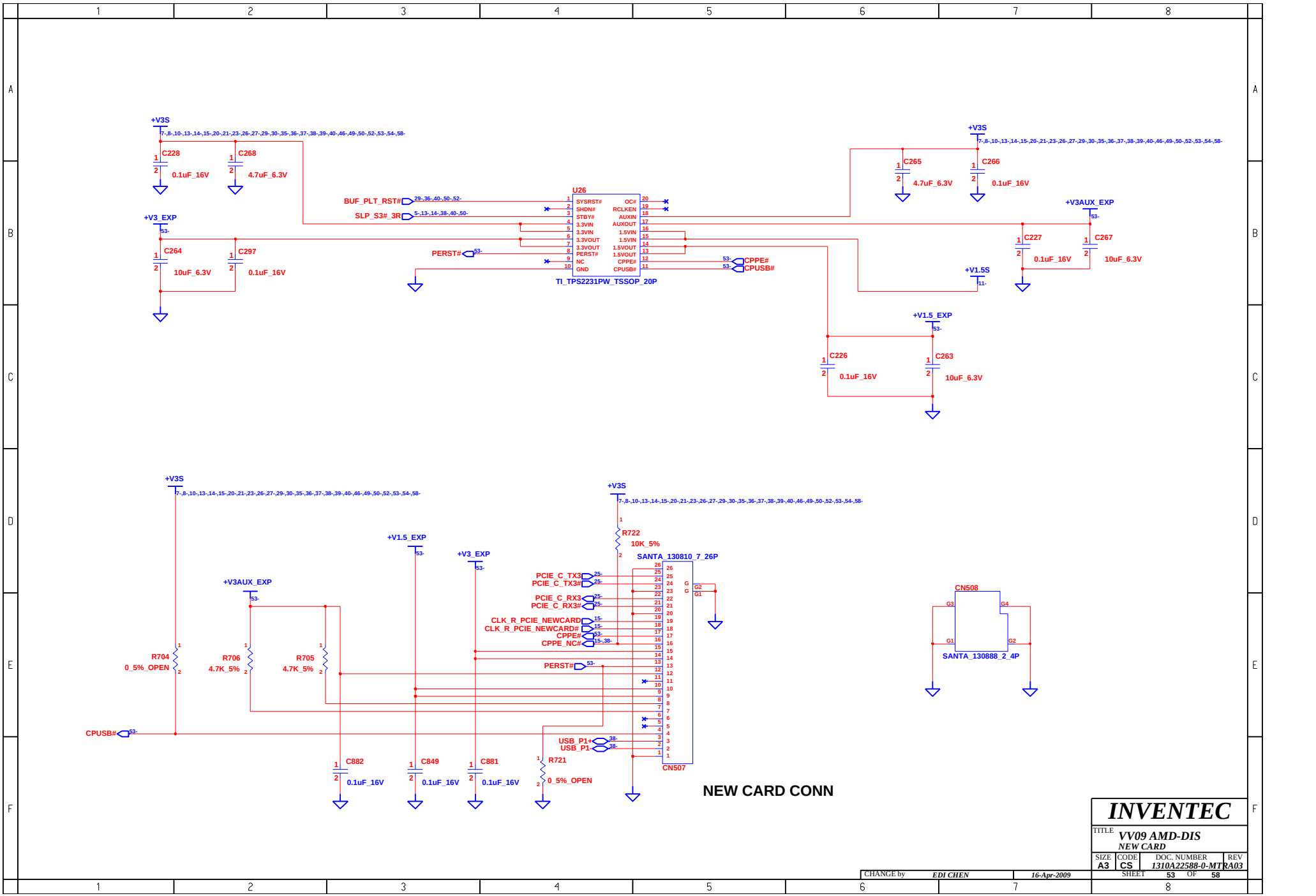
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
MINICARD & BT CONN

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 52 OF 58



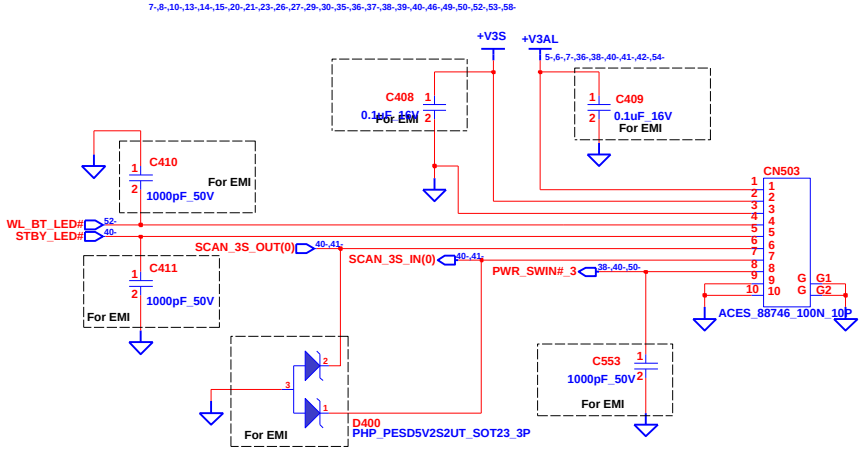
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

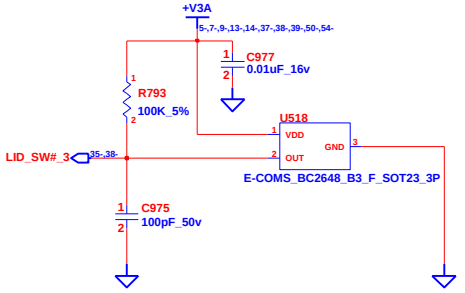
TITLE: *VV09 AMD-DIS*
NEW CARD

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

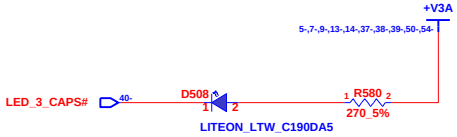
SHEET 53 OF 58



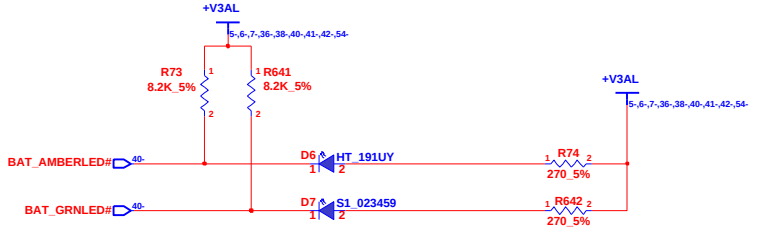
SWITCH DAUGHTER CONNECTOR



LID SWITCH



CAP LED



BATTERY-CHARGE LED

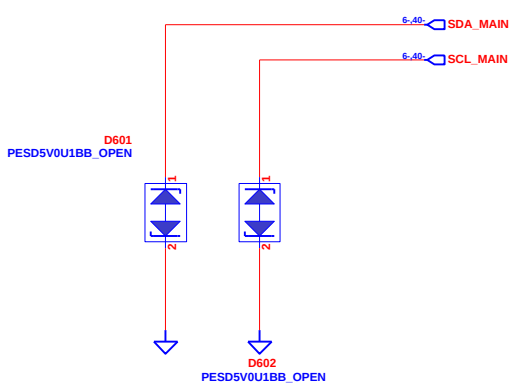
CHANGE by	EDI CHEN	16-Apr-2009	

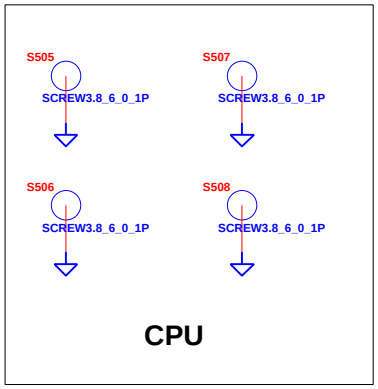
INVENTEC

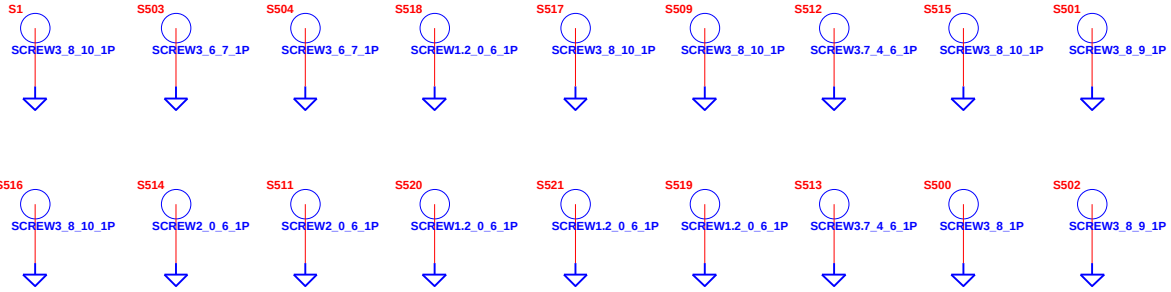
TITLE: *VV09 AMD-DIS*
BUTTON & LED

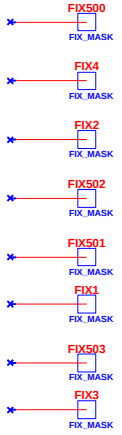
SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 54 OF 58









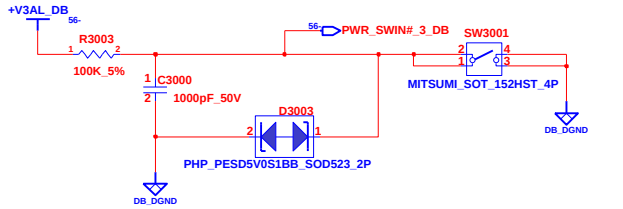
CHANGE by	EDI CHEN	16-Apr-2009

INVENTEC

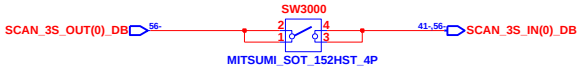
TITLE: *VV09 AMD-DIS*
SCREW

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

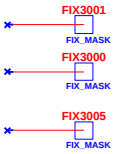
SHEET 55 OF 58

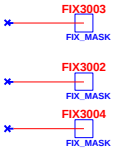


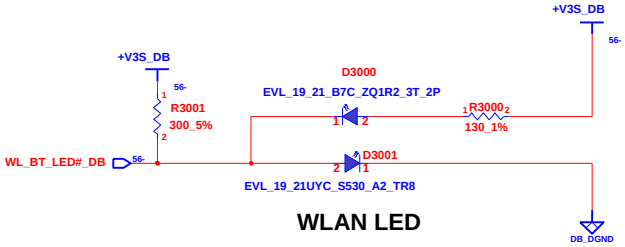
POWER BUTTON



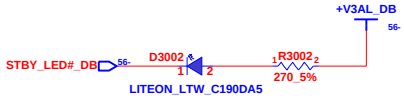
WIRELESS BUTTON



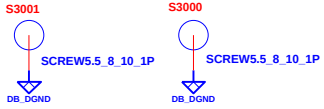


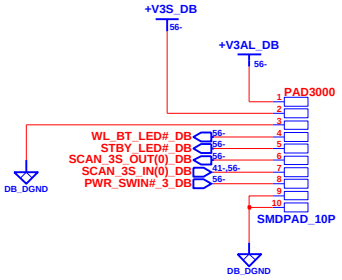


WLAN LED



POWER / STANDBY LED





LED&SWITCH BOARD

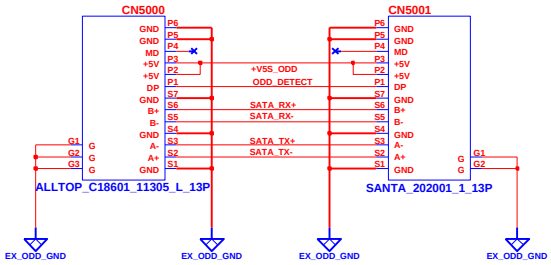
CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

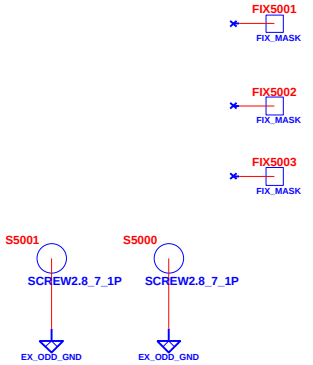
TITLE: *VV09 AMD-DIS*
SWITCH Board

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 56 OF 58



15" ODD Extend Board



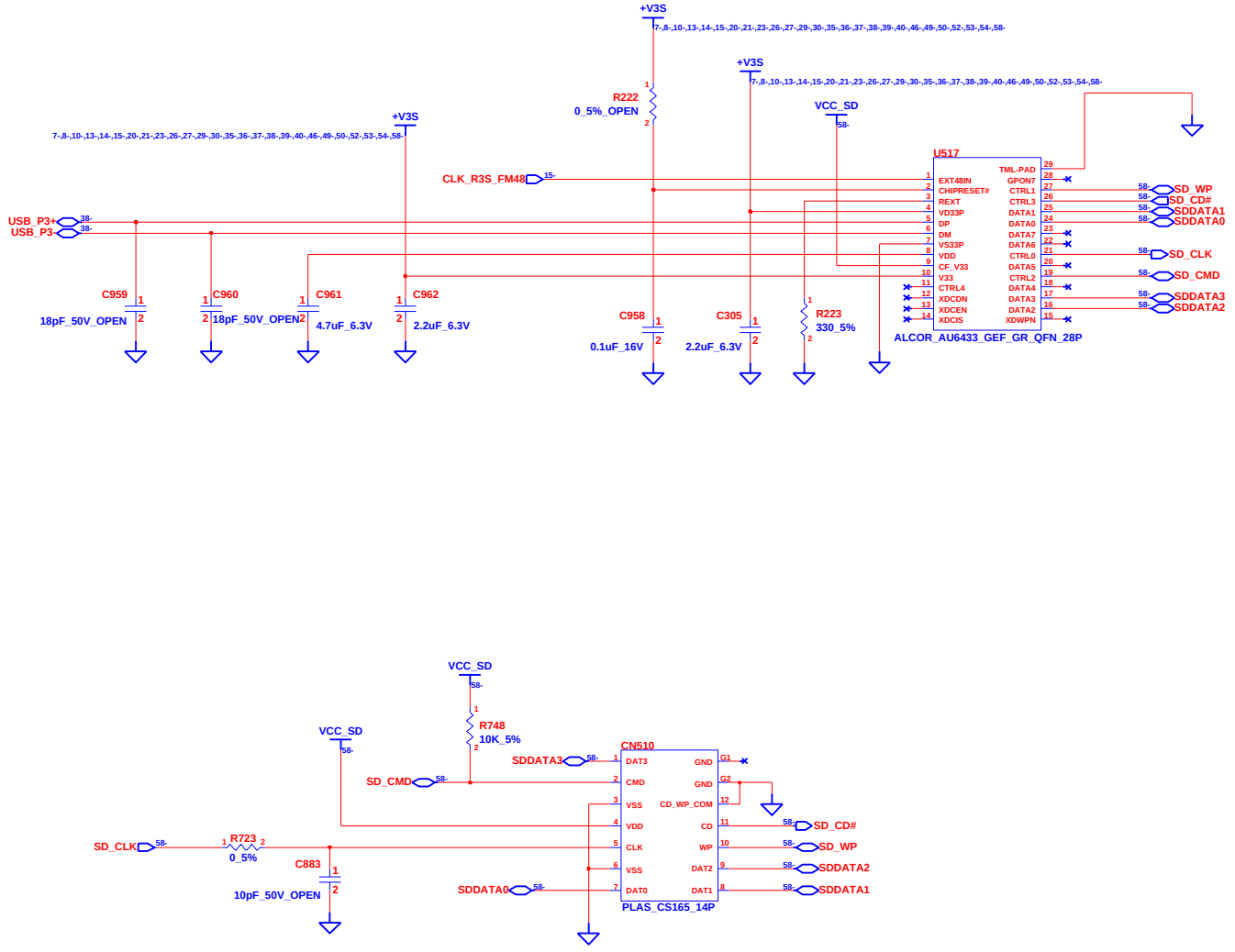
CHANGE by	EDI CHEN	16-Apr-2009		

INVENTEC

TITLE: *VV09 AMD-DIS*
15'' ODD Extend Board

SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310A22588-0-MTRA03	

SHEET 57 OF 58



CHANGE by	EDI CHEN	16-Apr-2009	

INVENTEC

TITLE: *VV09 AMD-DIS*
FLASH MEDIA CARD

SIZE	CODE	DOC. NUMBER	REV
A3	CS	*1310A22588-0-MTRA03*	

SHEET 58 OF 58