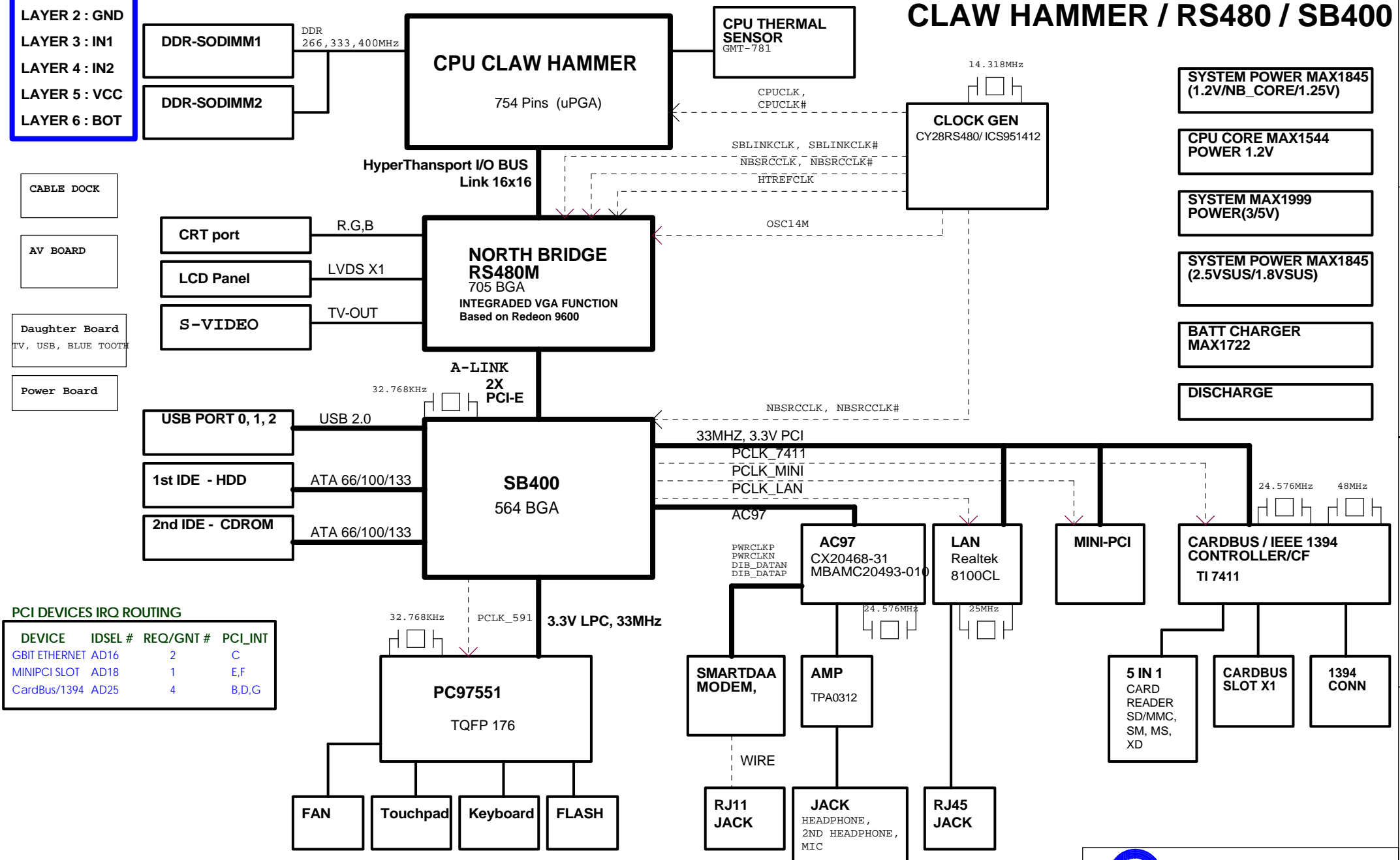


CT8 BLOCK DIAGRAM

CLAW HAMMER / RS480 / SB400

PCB STACK UP

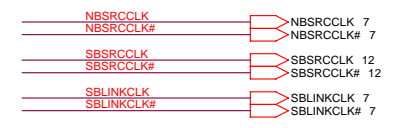
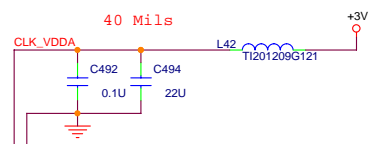
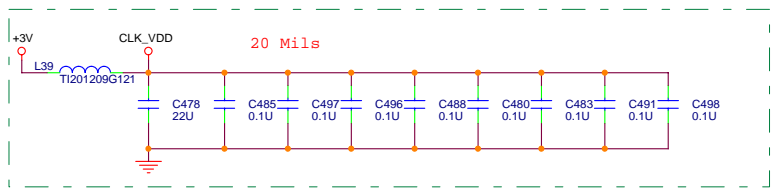
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT



- SYSTEM POWER MAX1845 (1.2V/NB_CORE/1.25V)
- CPU CORE MAX1544 POWER 1.2V
- SYSTEM MAX1999 POWER(3/5V)
- SYSTEM POWER MAX1845 (2.5VSUS/1.8VSUS)
- BATT CHARGER MAX1722
- DISCHARGE

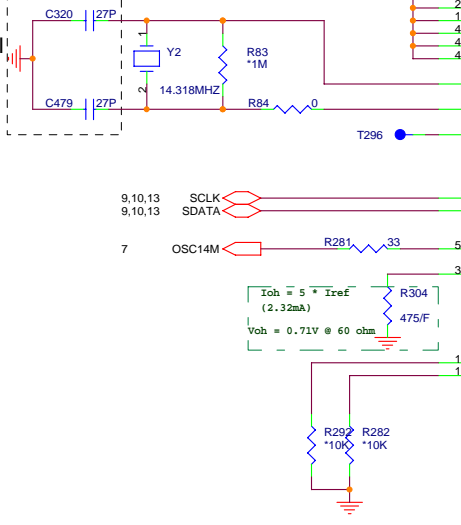
PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET AD16		2	C
MINIPCI SLOT AD18		1	E,F
CardBus/1394 AD25		4	B,D,G

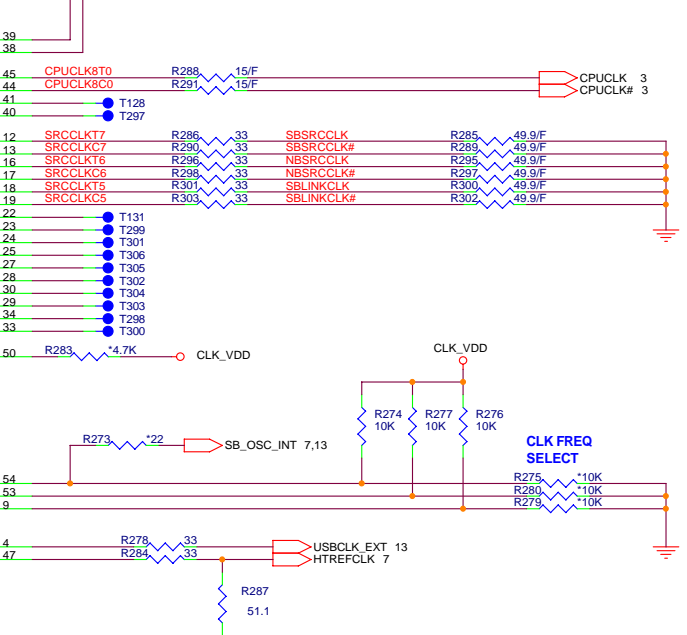
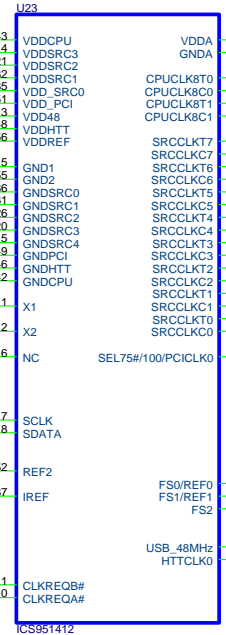


REV. B

Parallel Resonance Crystal
Tolerance: 35ppm (max)
Load: 20pf



Operating Current: 400mA



Layout Note:

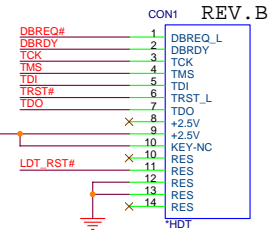
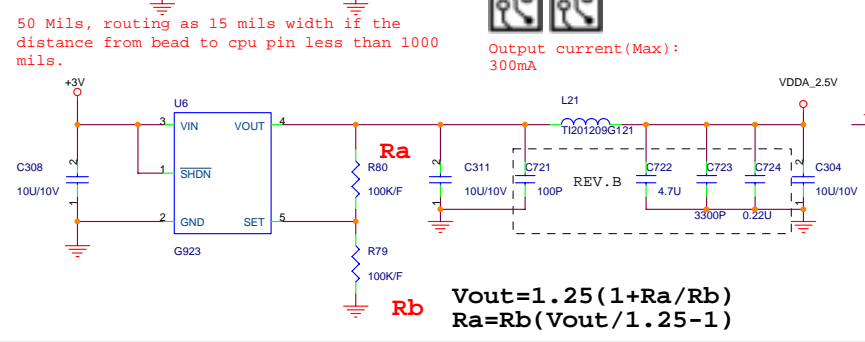
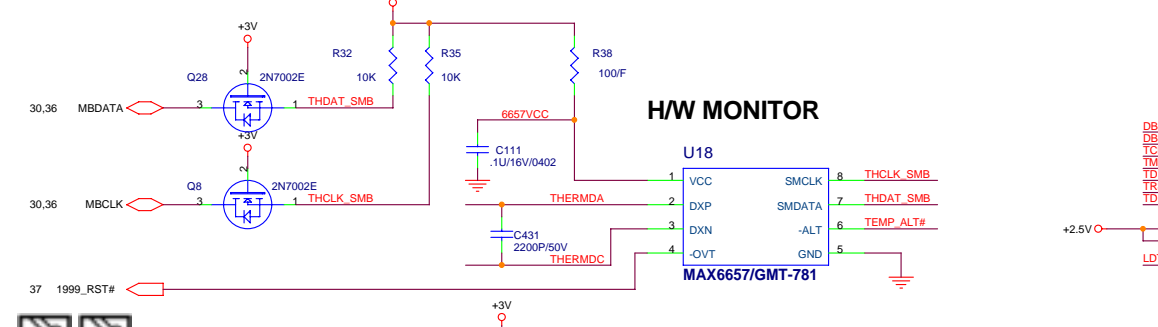
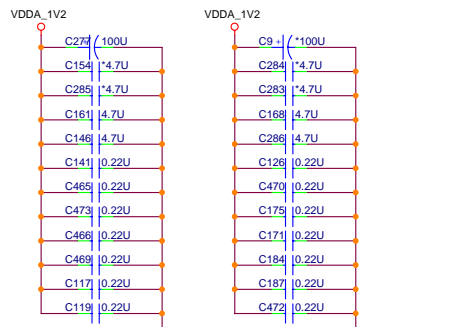
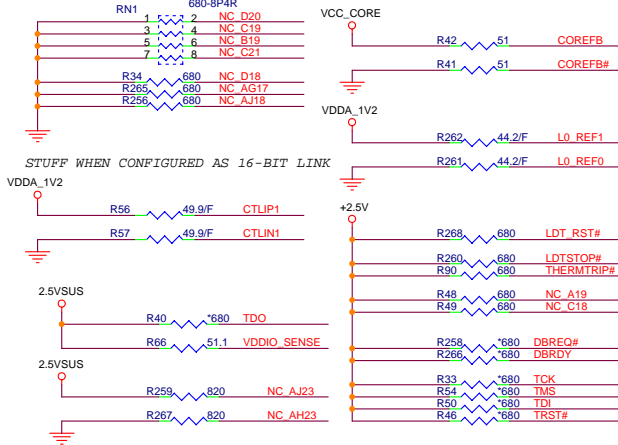
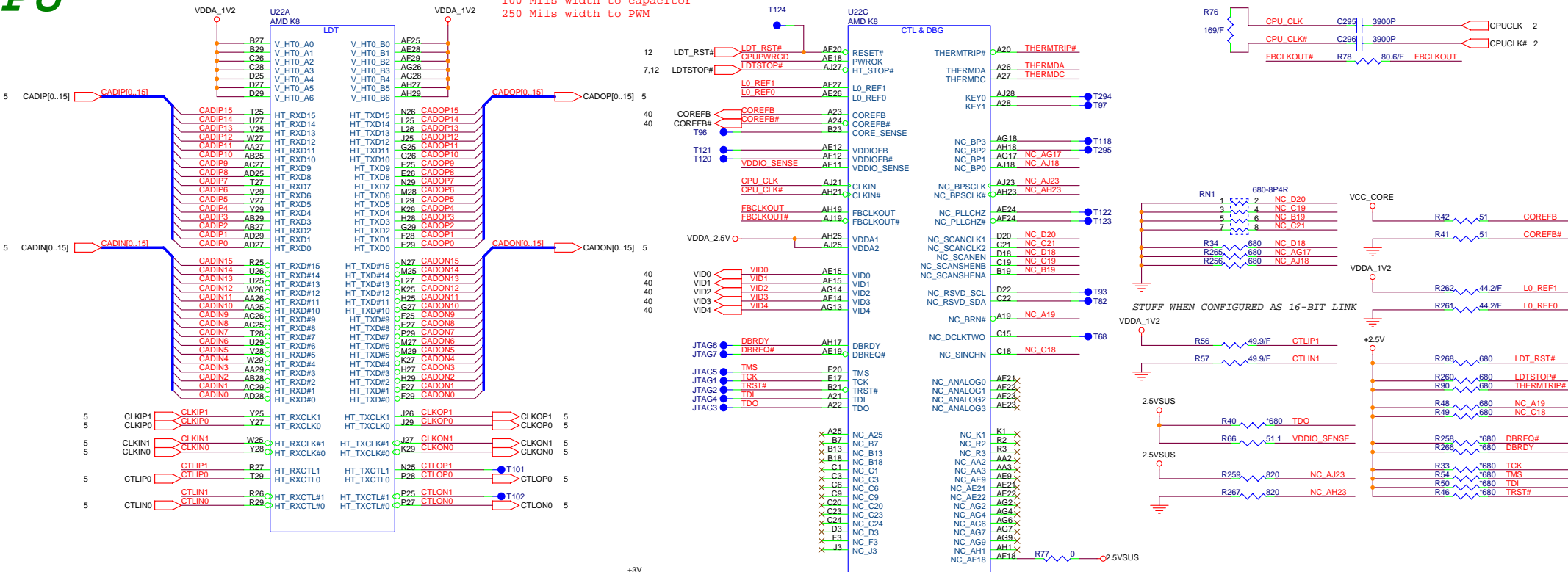
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CKG. AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

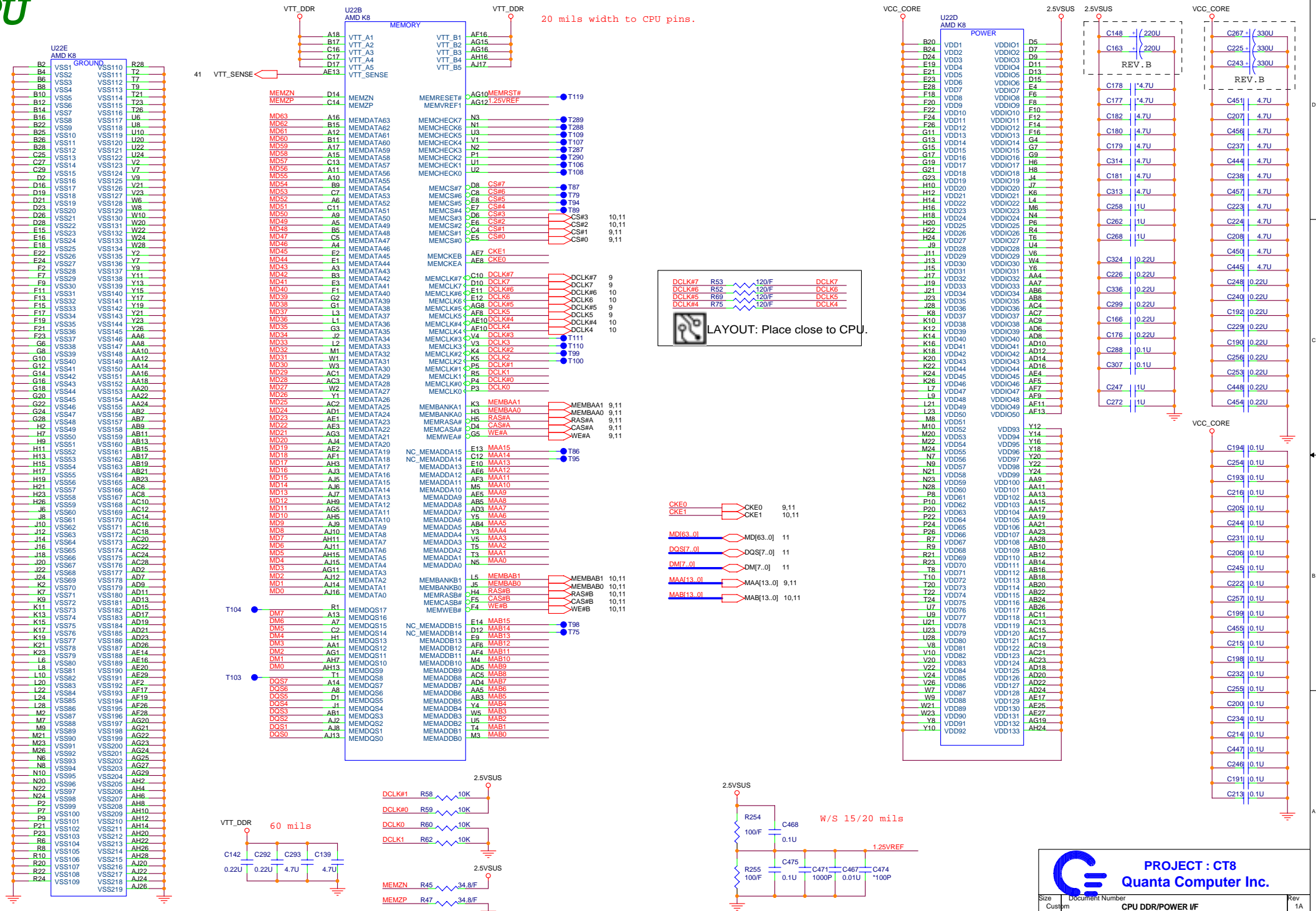
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

CPU

20 Mils width to pin
100 Mils width to capacitor
250 Mils width to PWM



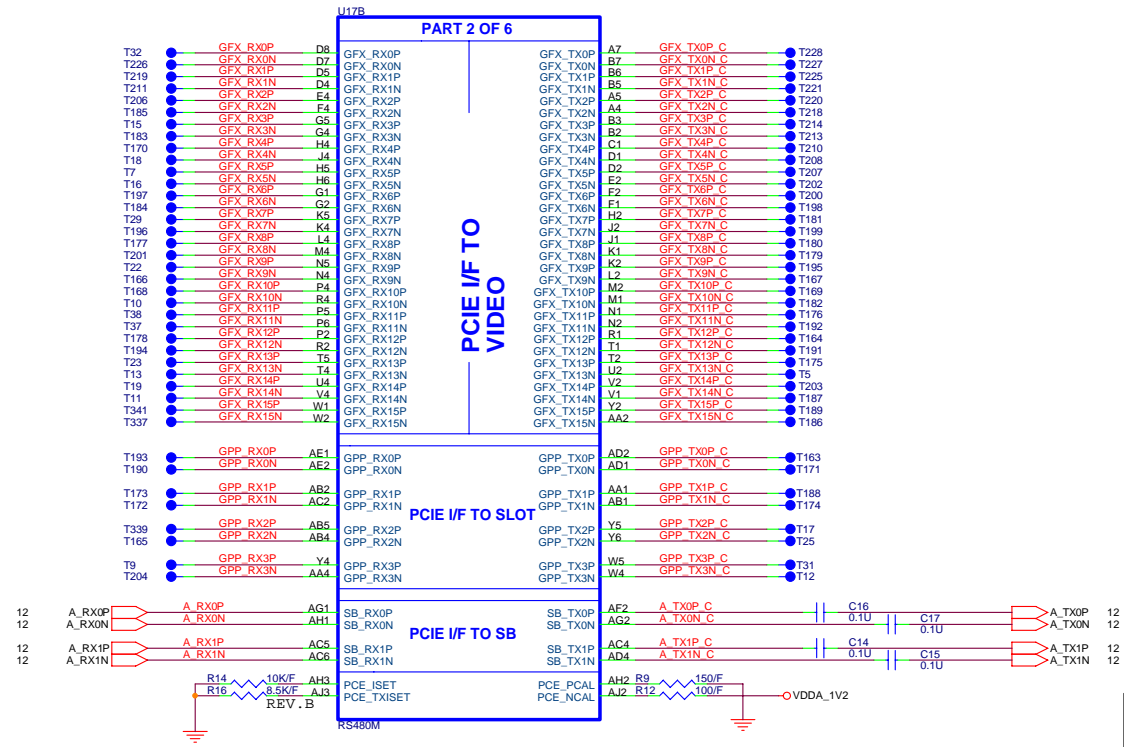
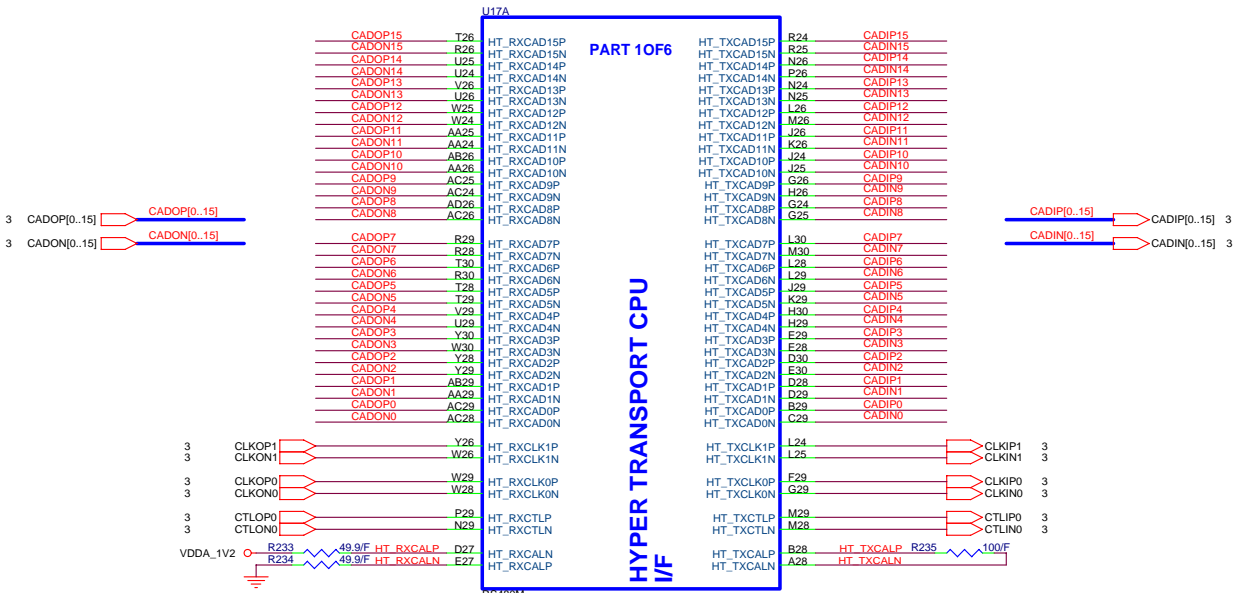


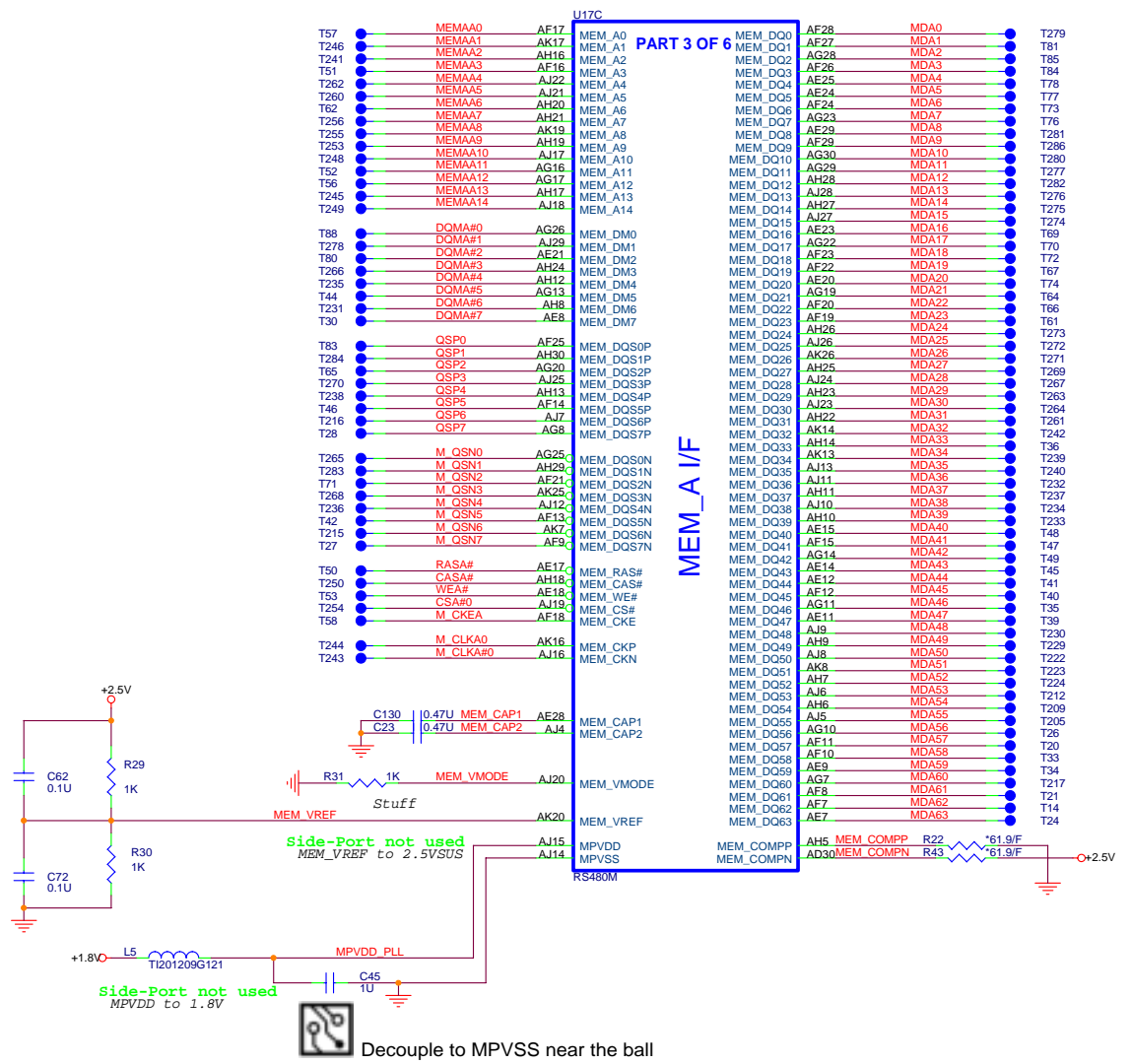
20 mils width to CPU pins.

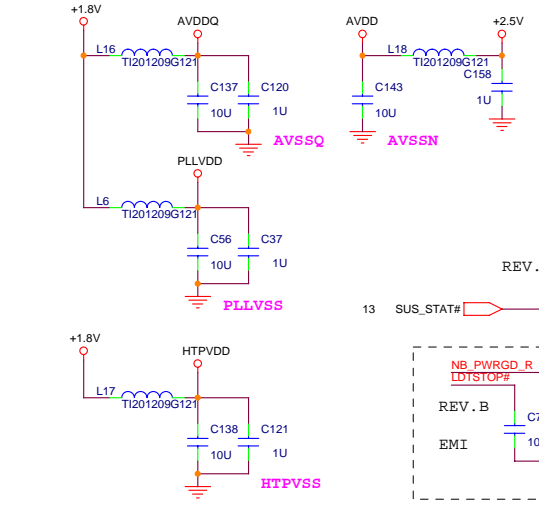
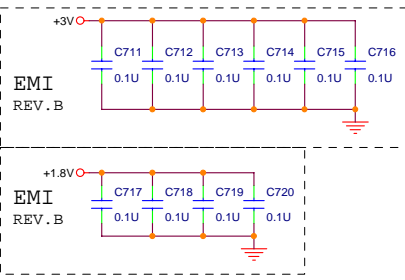
LAYOUT: Place close to CPU.

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	CPU DDR/POWER I/F	Rev
Custom			1A
Date:	Monday, December 13, 2004	Sheet	4 of 42

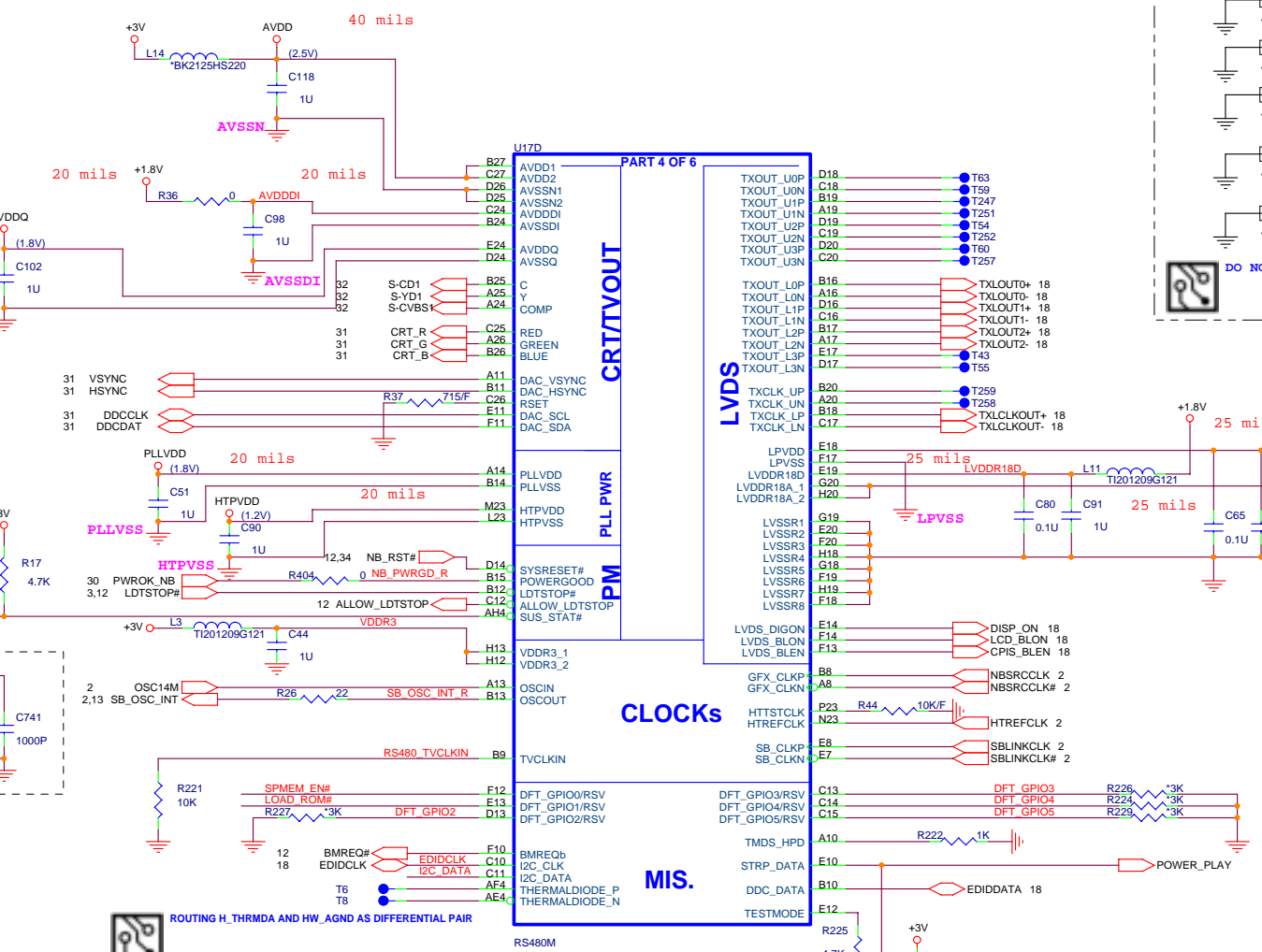
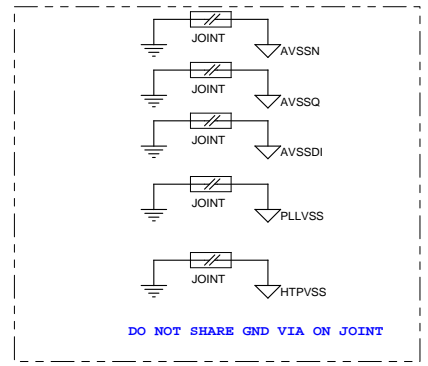






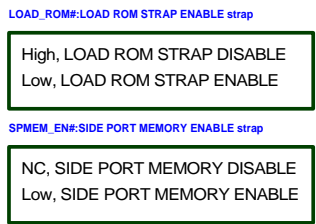
AVDD	DAC VDD (2.5V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVDD	PLL VDD (1.8V)
HTPVDD	HT PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ, PLLVDD, HTPVDD DECOUPLING CAPS ON THE BOTTOM, CLOSE TO BALLS



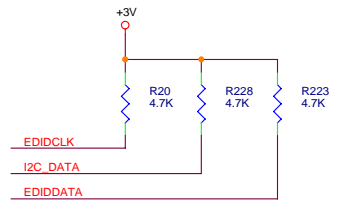
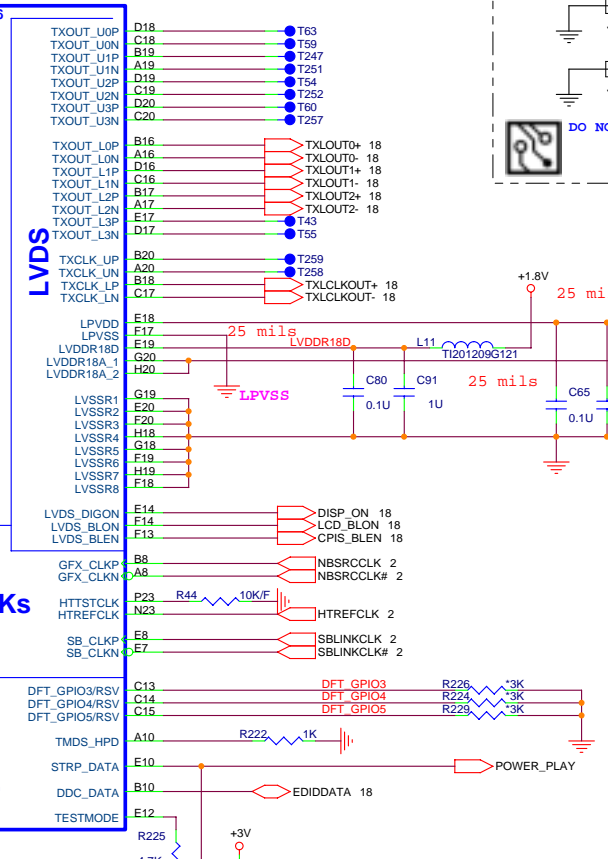
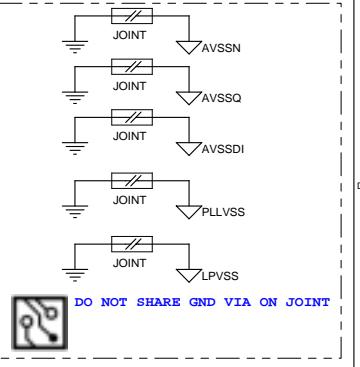
ROUTING H_THRMCA AND HW_AGND AS DIFFERENTIAL PAIR

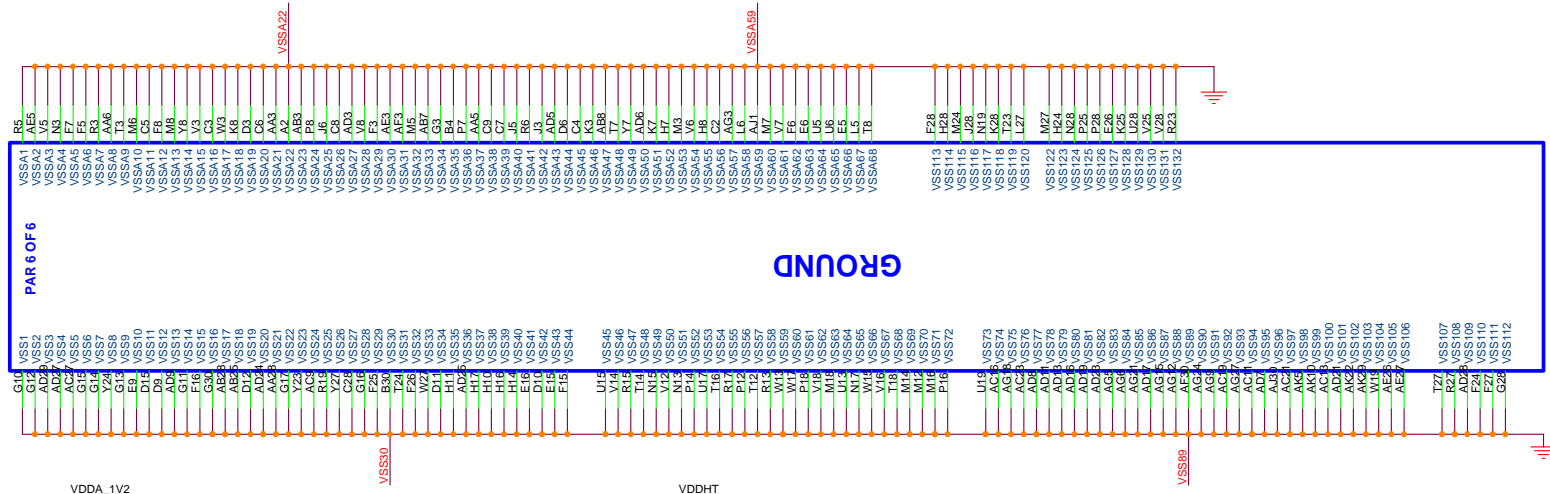
REV.B DEL Y1 AND U3 CIRCUIT.



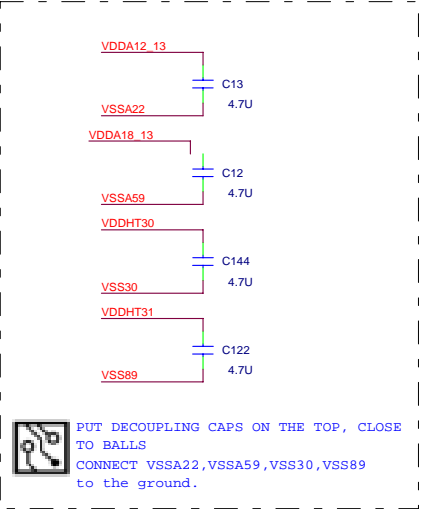
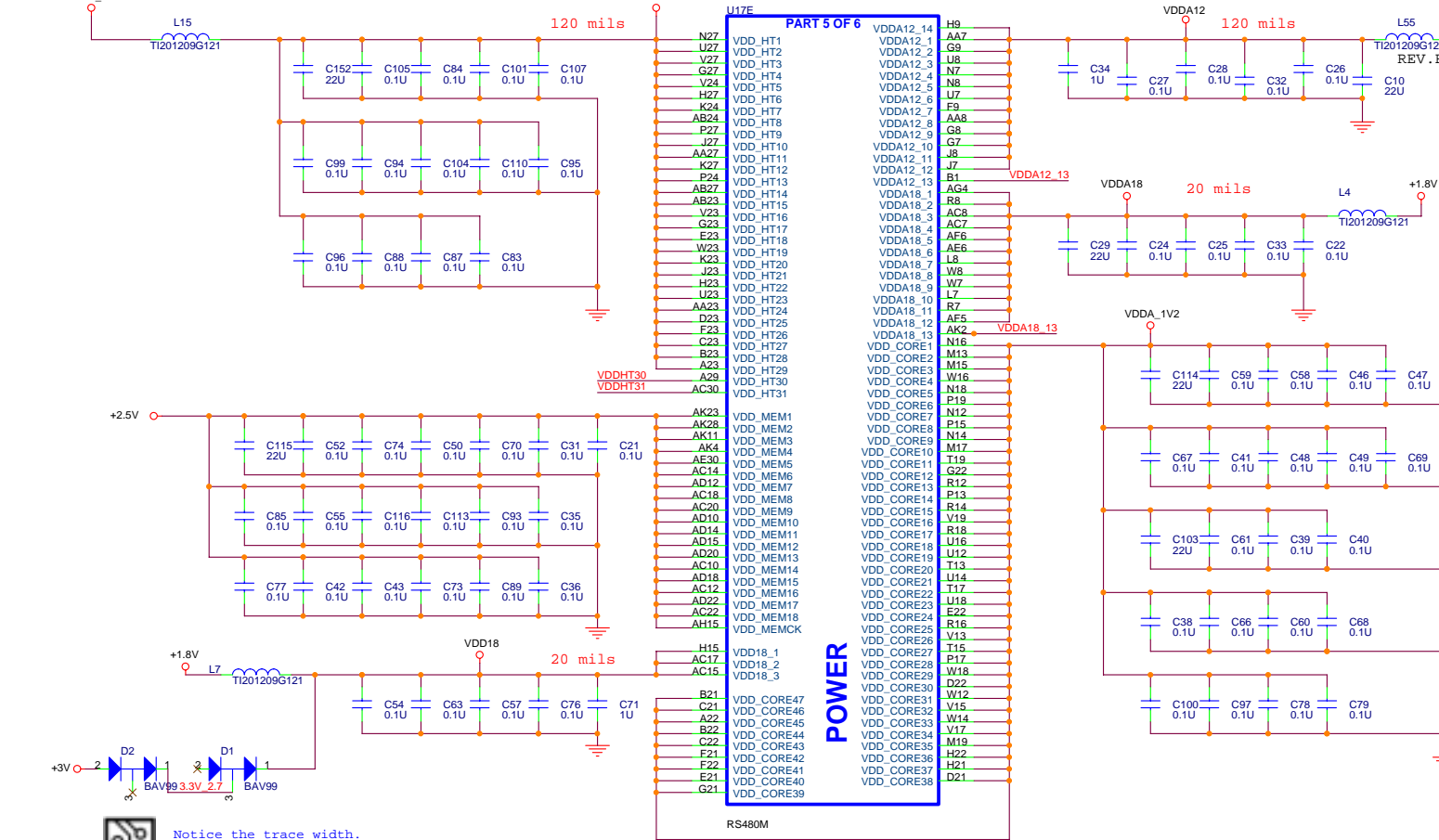
LOAD_ROM#: LOAD ROM STRAP ENABLE strap
 High, LOAD ROM STRAP DISABLE
 Low, LOAD ROM STRAP ENABLE

SPMEM_EN#: SIDE PORT MEMORY ENABLE strap
 NC, SIDE PORT MEMORY DISABLE
 Low, SIDE PORT MEMORY ENABLE

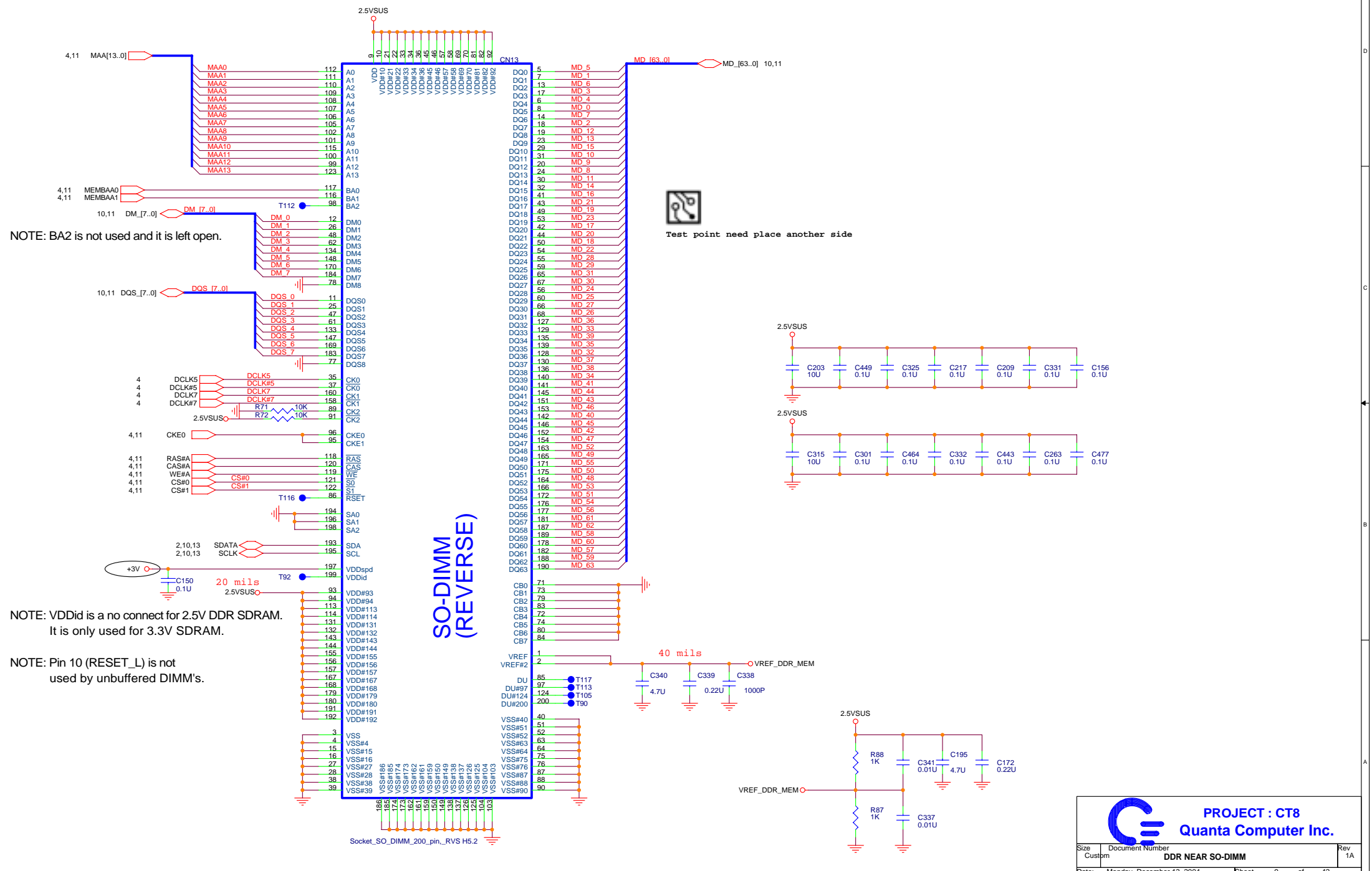




NB RS480 POWER STATES					
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	ON	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
ELLVDD	ON	ON	OFF	OFF	OFF
HTPVD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22, VSSA59, VSS30, VSS89 to the ground.



NOTE: BA2 is not used and it is left open.

Test point need place another side

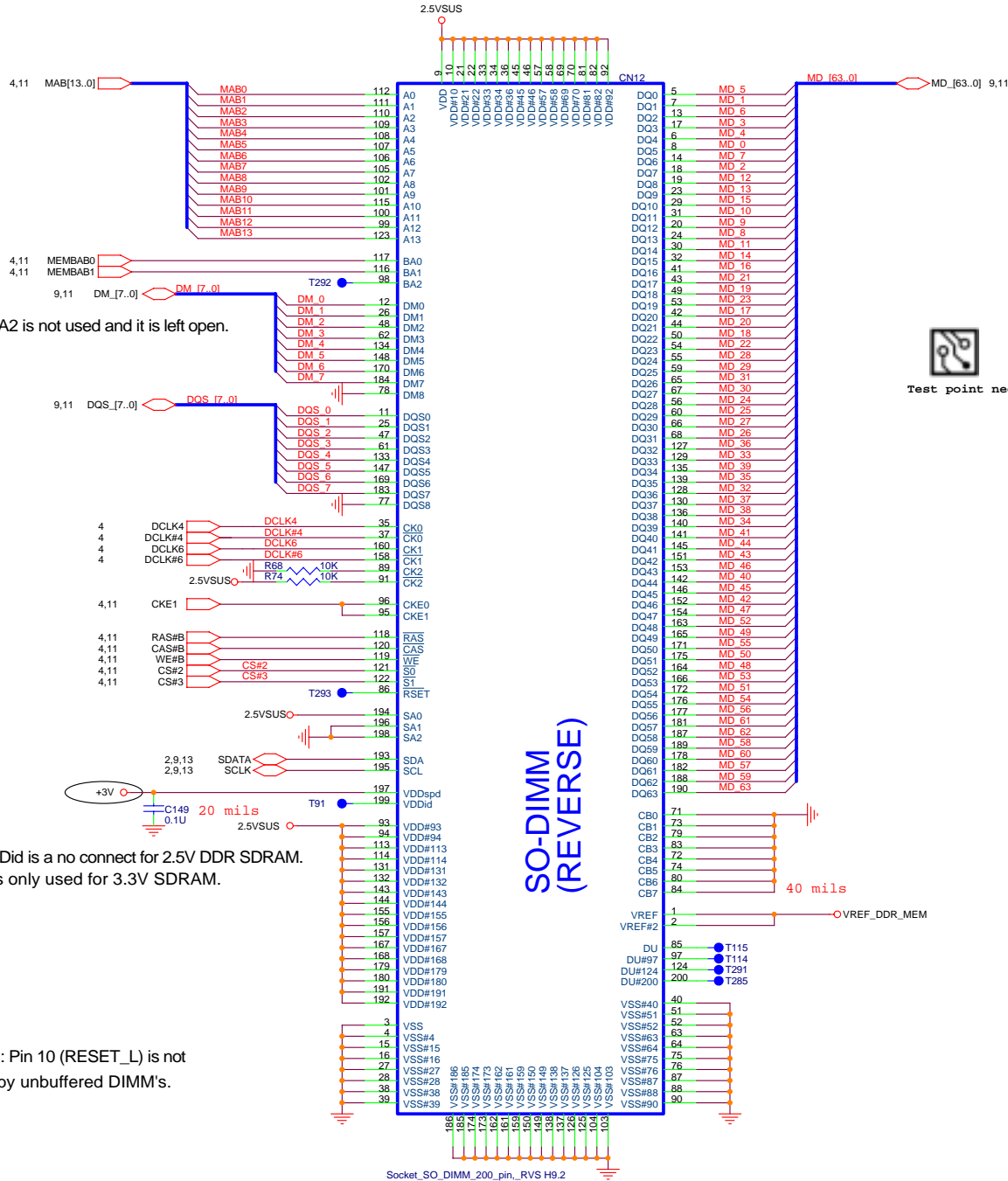
NOTE: VDDid is a no connect for 2.5V DDR SDRAM. It is only used for 3.3V SDRAM.

NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.


**SO-DIMM
(REVERSE)**

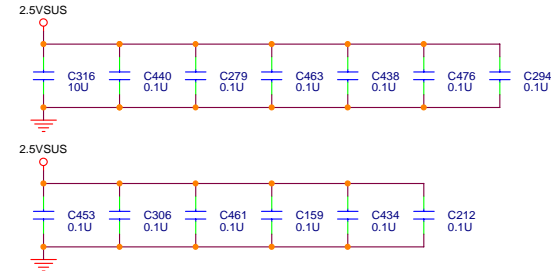
PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR NEAR SO-DIMM	1A
Date:	Monday, December 13, 2004	Sheet 9 of 42



NOTE: BA2 is not used and it is left open.



Test point need place another side



NOTE: VDDid is a no connect for 2.5V DDR SDRAM.
It is only used for 3.3V SDRAM.

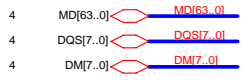
NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.

Socket_SO_DIMM_200_pin_RVS H9.2

 PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR FAR SO-DIMM	1A
Date:	Monday, December 13, 2004	Sheet 10 of 42

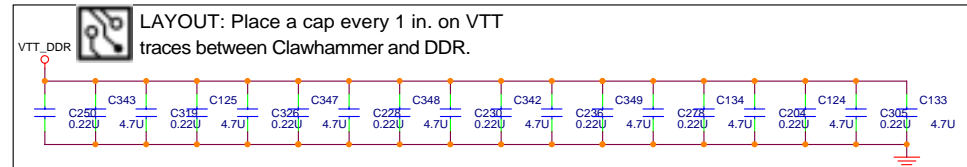
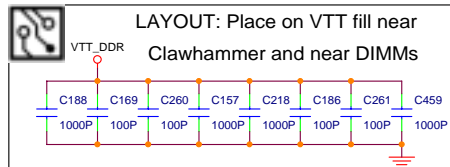
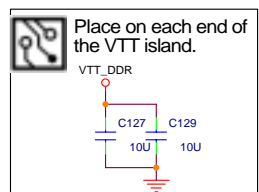
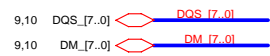
DDR



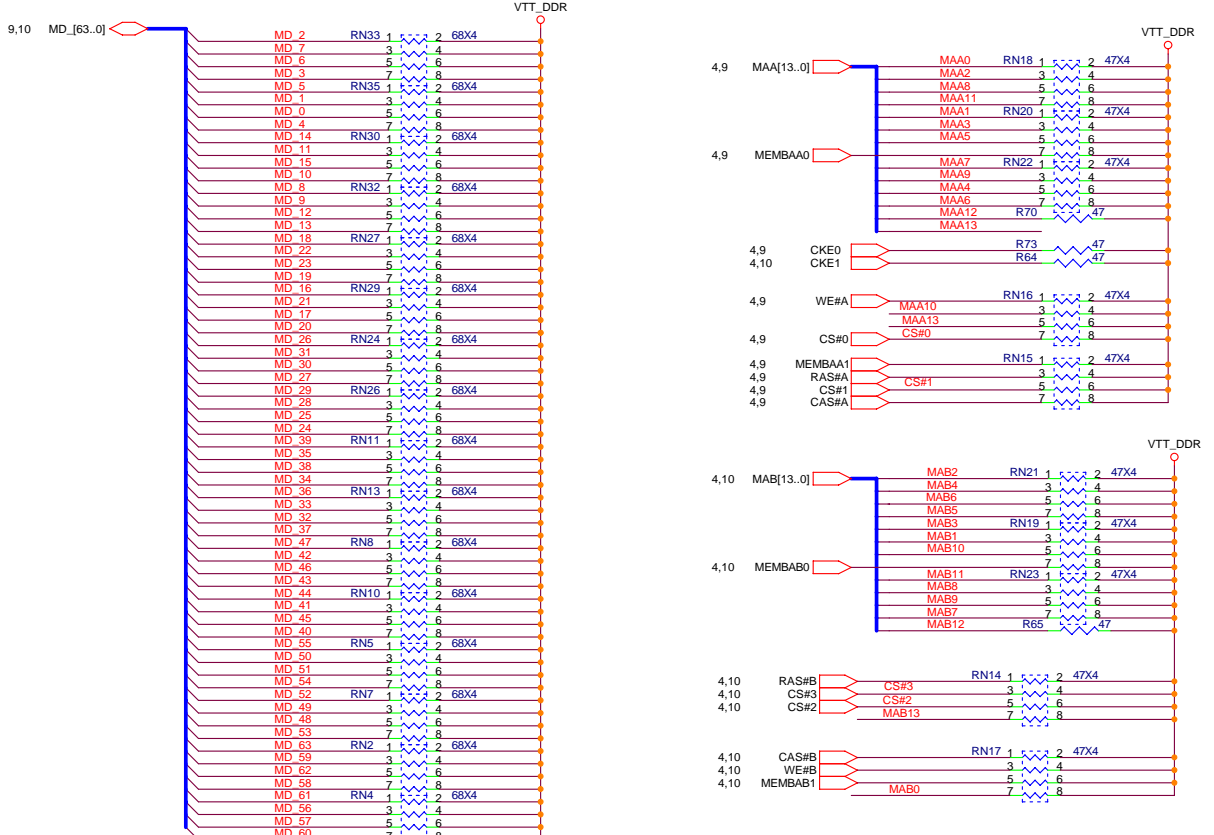
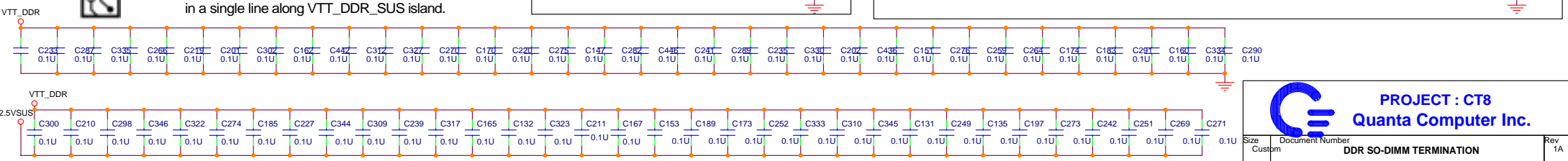
MD62	RN46	1	2	10X2	MD 62
MD58		3	4		MD 58
MD56	RN48	1	2	10X2	MD 56
MD61		3	4		MD 61
MD59	RN47	1	2	10X2	MD 59
MD63		3	4		MD 63
MD60	RN49	1	2	10X2	MD 60
MD57		3	4		MD 57
MD55	RN50	1	2	10X2	MD 55
MD50		3	4		MD 50
MD48	RN53	1	2	10X2	MD 48
MD53		3	4		MD 53
MD51	RN51	1	2	10X2	MD 51
MD54		3	4		MD 54
MD49	RN52	1	2	10X2	MD 49
MD52		3	4		MD 52
MD42	RN55	1	2	10X2	MD 42
MD47		3	4		MD 47
MD45	RN58	1	2	10X2	MD 45
MD40		3	4		MD 40
MD43	RN54	1	2	10X2	MD 43
MD46		3	4		MD 46
MD41	RN56	1	2	10X2	MD 41
MD44		3	4		MD 44
MD38	RN59	1	2	10X2	MD 38
MD34		3	4		MD 34
MD32	RN61	1	2	10X2	MD 32
MD37		3	4		MD 37
MD39	RN57	1	2	10X2	MD 39
MD35		3	4		MD 35
MD36	RN60	1	2	10X2	MD 36
MD33		3	4		MD 33
MD27	RN63	1	2	10X2	MD 27
MD26		3	4		MD 26
MD25	RN65	1	2	10X2	MD 25
MD24		3	4		MD 24
MD31	RN62	1	2	10X2	MD 31
MD30		3	4		MD 30
MD28	RN64	1	2	10X2	MD 28
MD29		3	4		MD 29
MD22	RN67	1	2	10X2	MD 22
MD18		3	4		MD 18
MD17	RN69	1	2	10X2	MD 17
MD20		3	4		MD 20
MD19	RN66	1	2	10X2	MD 19
MD23		3	4		MD 23
MD16	RN68	1	2	10X2	MD 16
MD21		3	4		MD 21
MD11	RN71	1	2	10X2	MD 11
MD14		3	4		MD 14
MD9	RN73	1	2	10X2	MD 9
MD8		3	4		MD 8
MD10	RN70	1	2	10X2	MD 10
MD15		3	4		MD 15
MD12	RN72	1	2	10X2	MD 12
MD13		3	4		MD 13
MD7	RN75	1	2	10X2	MD 7
MD2		3	4		MD 2
MD4	RN77	1	2	10X2	MD 4
MD0		3	4		MD 0
MD8	RN74	1	2	10X2	MD 8
MD3		3	4		MD 3
MD5	RN76	1	2	10X2	MD 5
MD1		3	4		MD 1

DQS0	R271	10-0402	DQS 0
DQS1	R269	10-0402	DQS 1
DQS2	R268	10-0402	DQS 2
DQS3	R259	10-0402	DQS 3
DQS4	R243	10-0402	DQS 4
DQS5	R241	10-0402	DQS 5
DQS6	R238	10-0402	DQS 6
DQS7	R236	10-0402	DQS 7

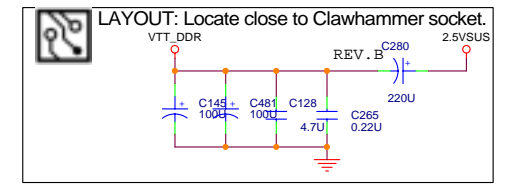
DM0	R272	10-0402	DM 0
DM1	R270	10-0402	DM 1
DM2	R269	10-0402	DM 2
DM3	R259	10-0402	DM 3
DM4	R245	10-0402	DM 4
DM5	R242	10-0402	DM 5
DM6	R238	10-0402	DM 6
DM7	R237	10-0402	DM 7

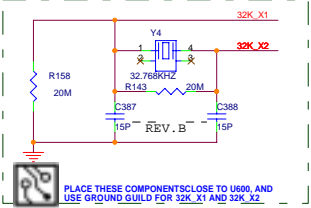


LAYOUT: Place alternating caps to GND and VDD_2.5V_SUS in a single line along VTT_DDR_SUS island.



03/19 Modify ->Quanta stock haven't 68x4 (8P4R-0402)

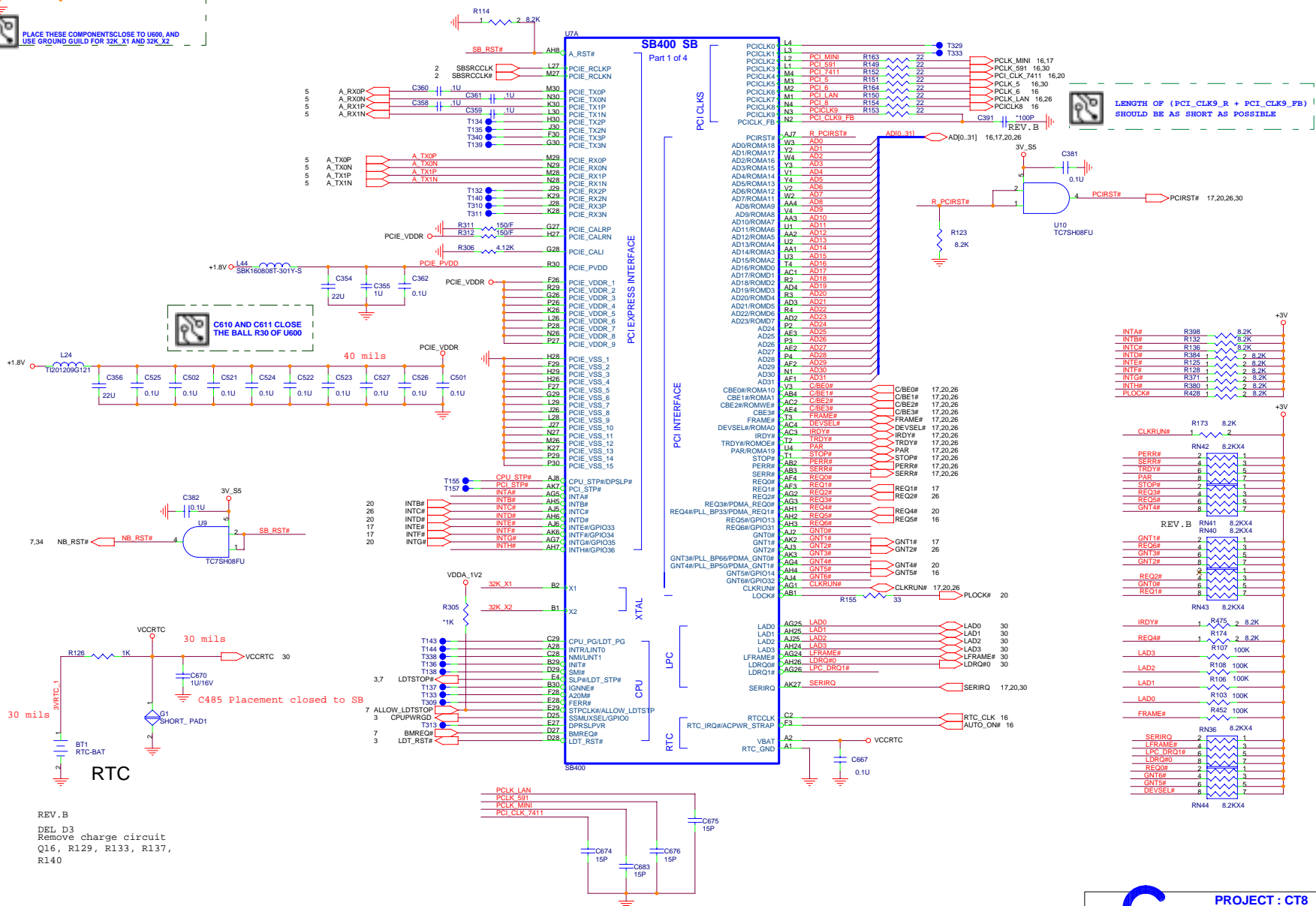




PLACE THESE CAPS CLOSE TO THE CONNECTOR

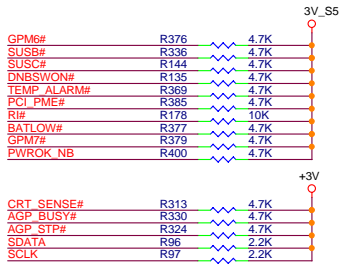
C610 AND C611 CLOSE THE BALL R30 OF U600

LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD BE AS SHORT AS POSSIBLE



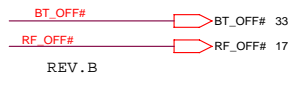
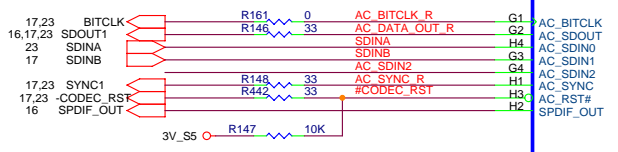
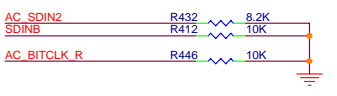
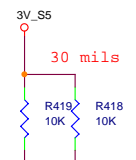
REV. B
DEL D3
Remove charge circuit
Q16, R129, R133, R137,
R140

Please double check SB400 pin D5 & pin A27 define, because can't meet ATI library/symbols.

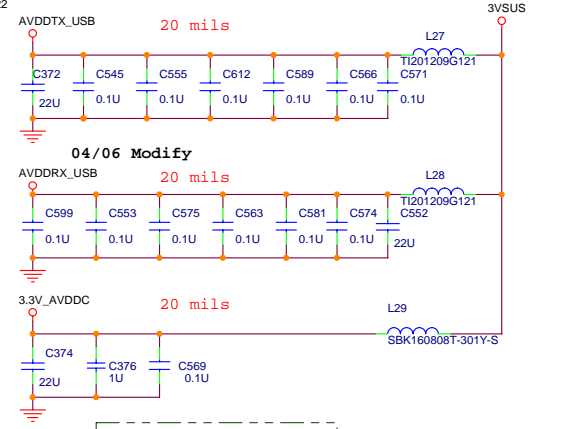
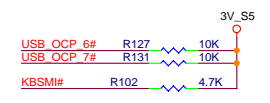
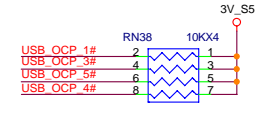
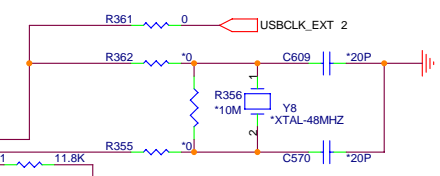
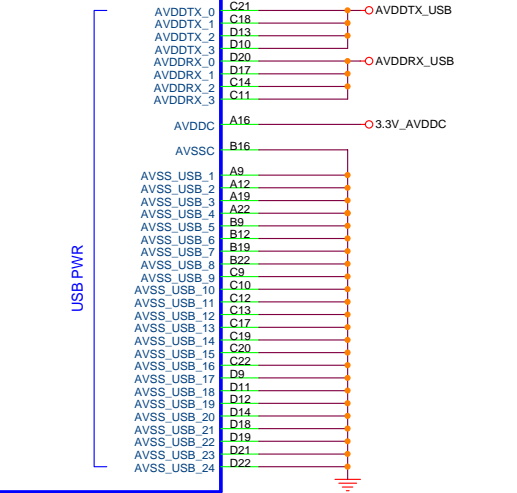
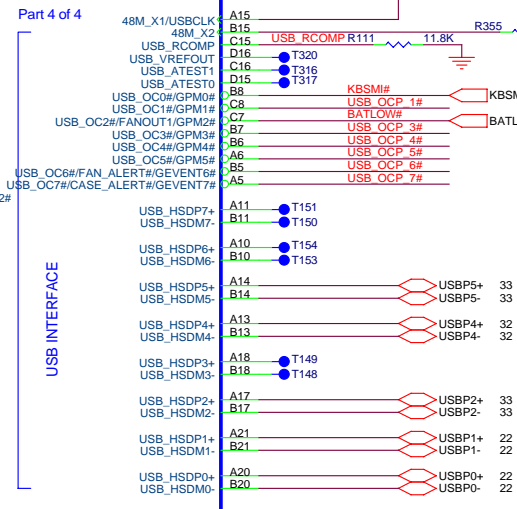
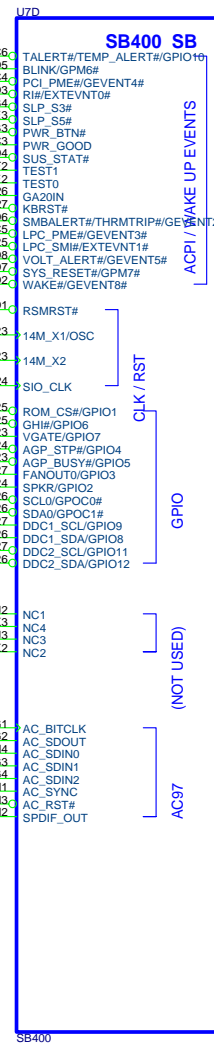
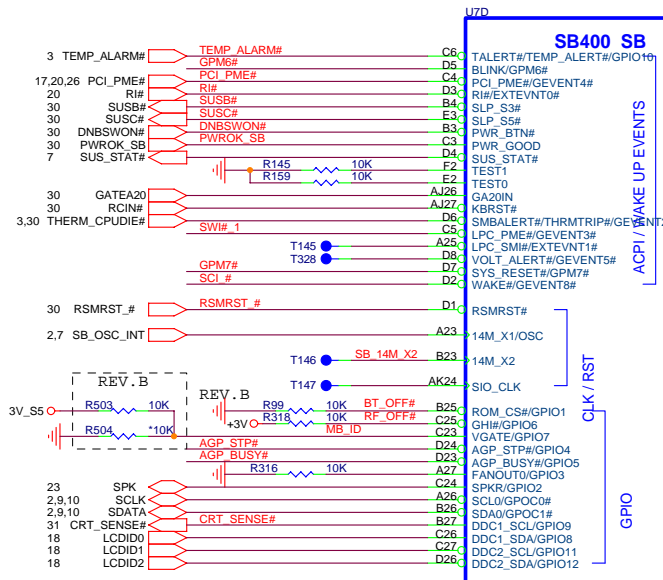


PWROK_SB is 33ms ~
500ms after NB_PWRGD

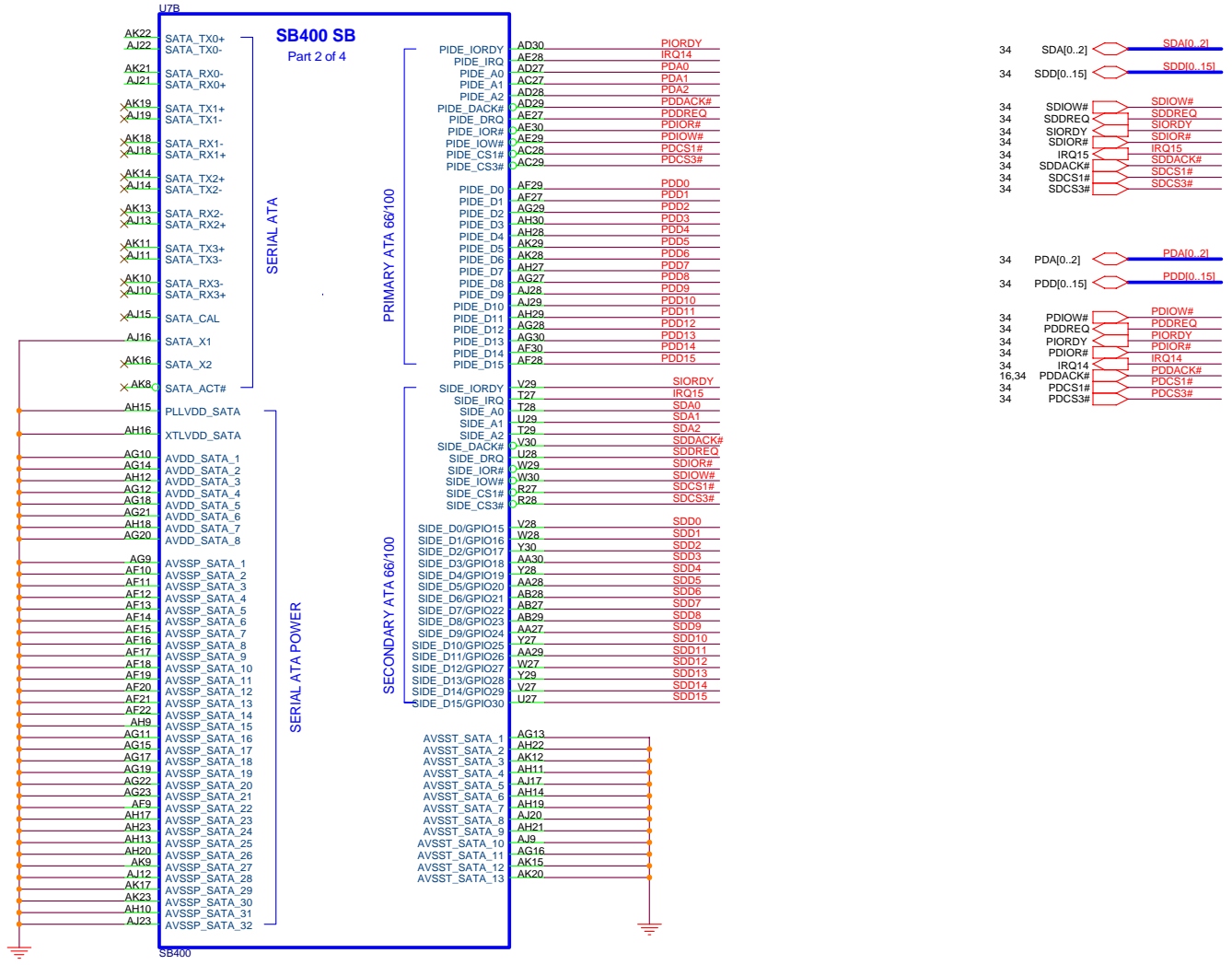
R503 STUFF IS FULL FEATURE.
R504 STUFF IS DE-FEATURE.



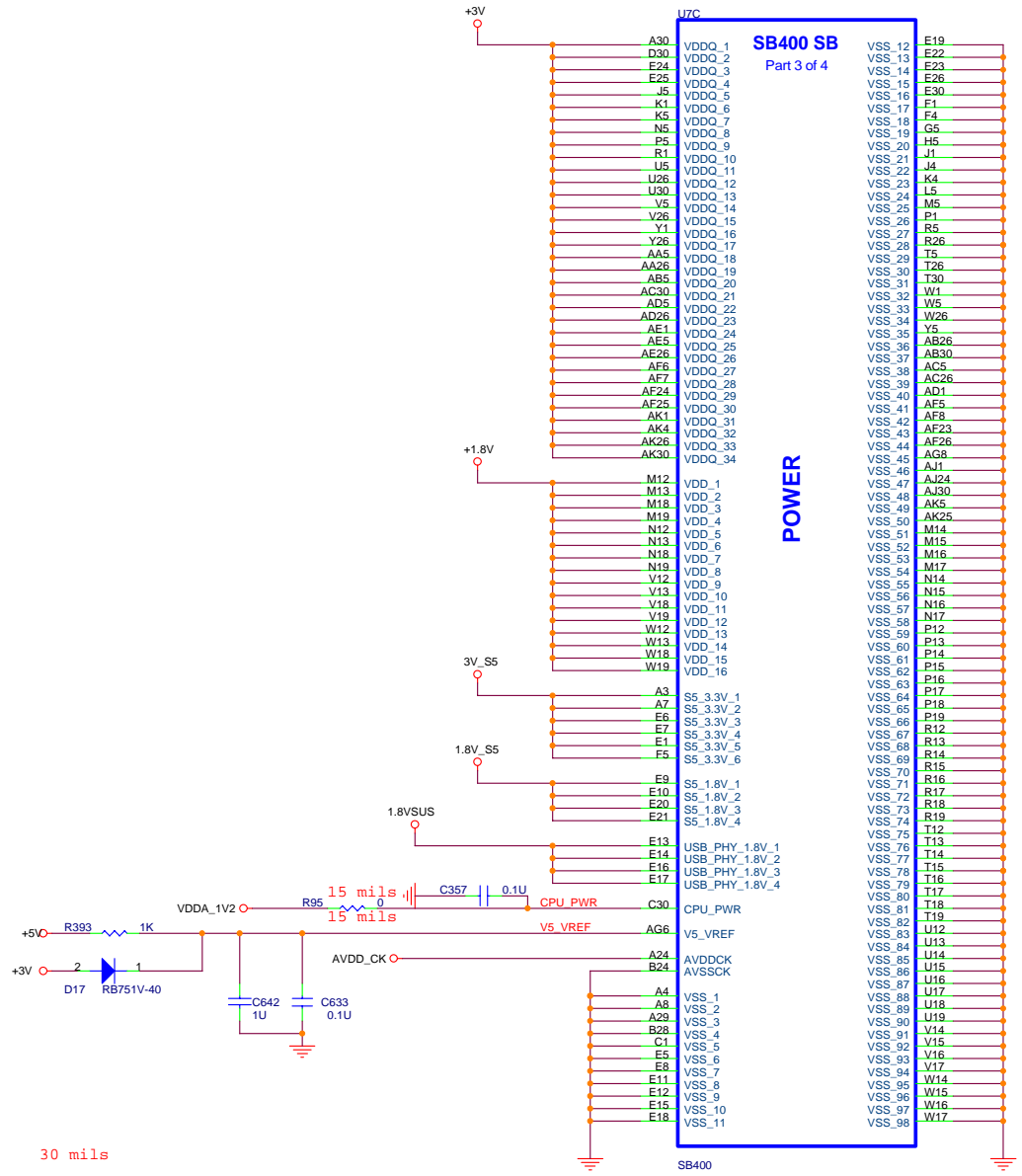
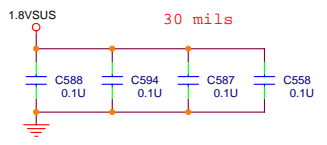
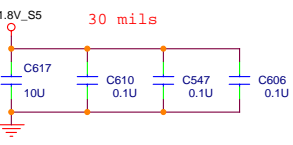
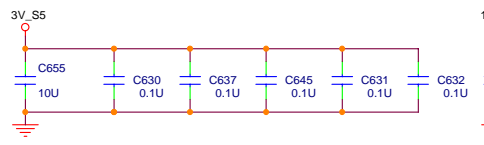
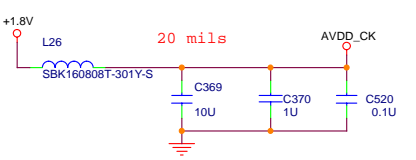
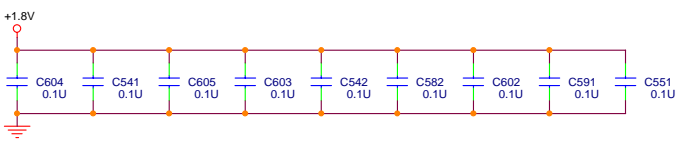
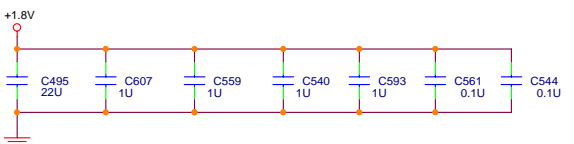
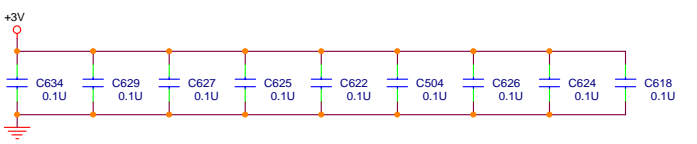
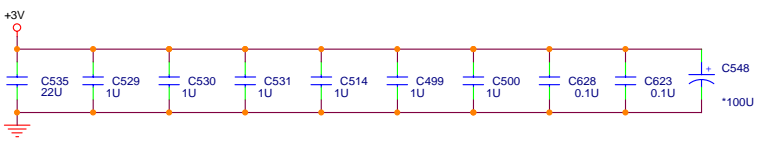
REV . B

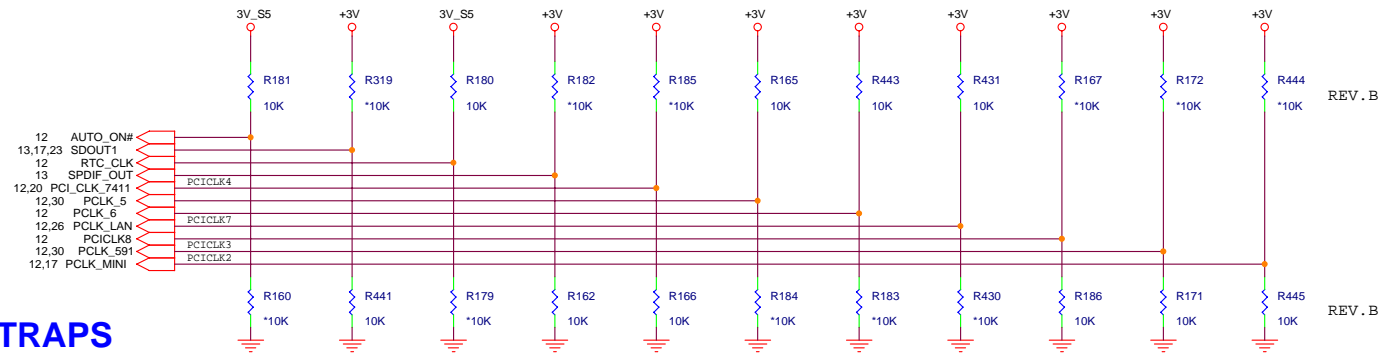


04/06 Modify
C641 AND C642 CLOSE THE BALL A16 OF U600



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



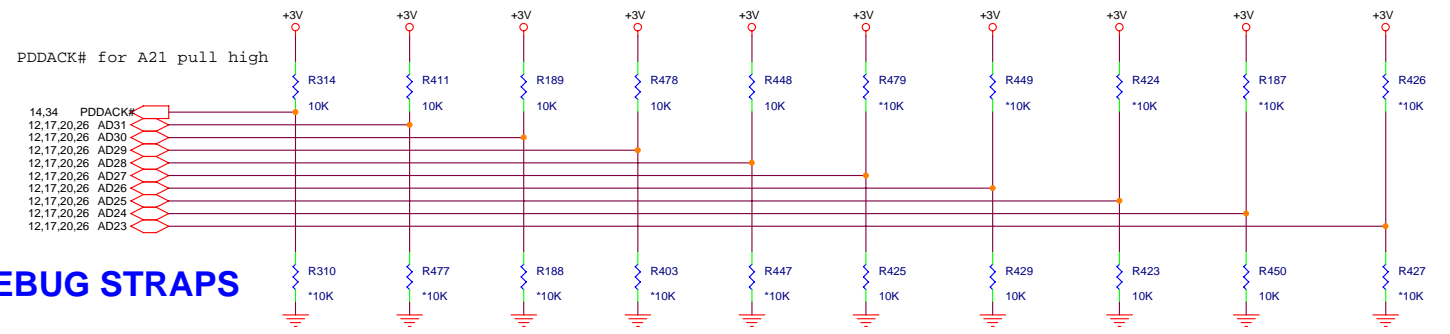


REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3
PULL HIGH	MANUAL PWR ON <i>DEFAULT</i>	USE DEBUG STRAPS	INTERNAL RTC <i>DEFAULT</i>	SIO 24MHz	48MHz OSC MODE <i>DEFAULT</i>	14MHz OSC MODE <i>DEFAULT</i>	CPU I/F = K8 <i>DEFAULT</i>	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	USB PHY PWRDOWN DISABLE <i>DEFAULT</i>	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS <i>DEFAULT</i>	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz <i>DEFAULT</i>	48MHz XTAL MODE	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM	USB PHY PWRDOWN ENABLE	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

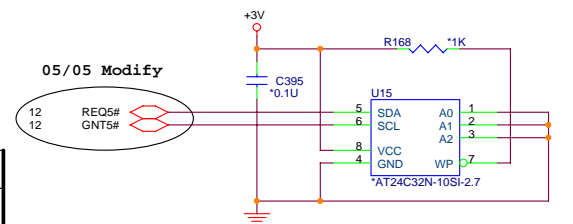
Need to check



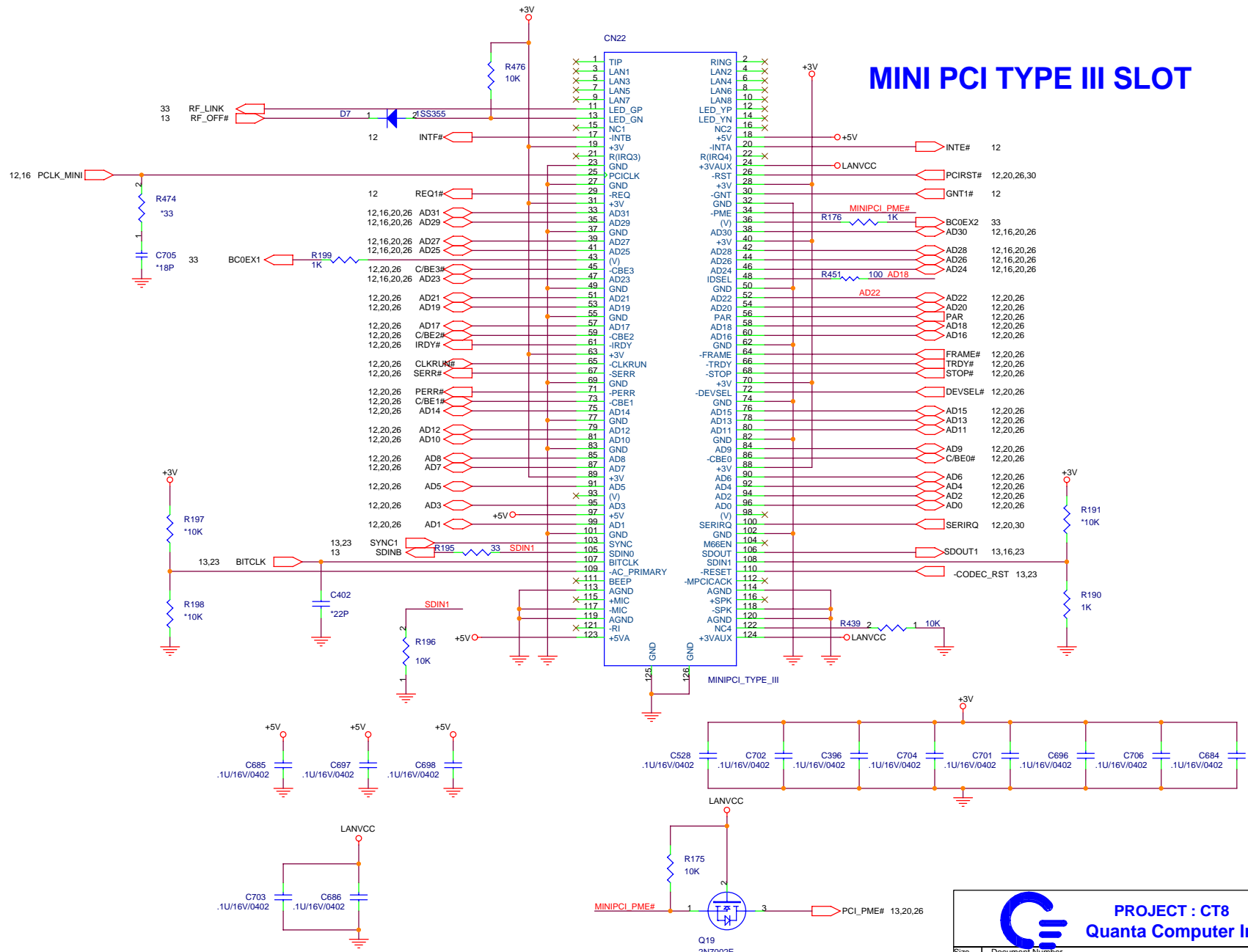
DEBUG STRAPS

	PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI <i>DEFAULT</i>	PLL CHARGE PUMP CTRL BIT 0 HI <i>DEFAULT</i>	PLL VCO CTRL BIT 1 HI <i>DEFAULT</i>	PLL VCO CTRL BIT 0 HI <i>DEFAULT</i>	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BY PASS USB PLL
PULL LOW	USE LONG RESET <i>DEFAULT</i>	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL <i>DEFAULT</i>	USE ACPI BCLK <i>DEFAULT</i>	USE IDE PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	USE USB PLL <i>DEFAULT</i>

Need to check



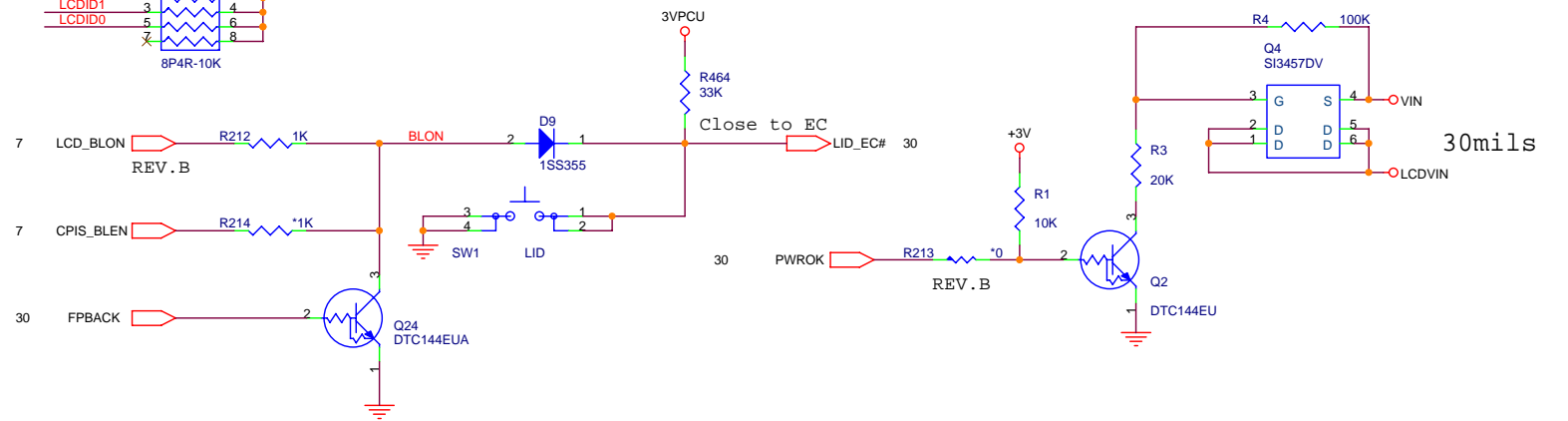
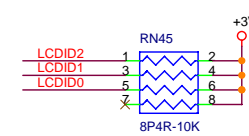
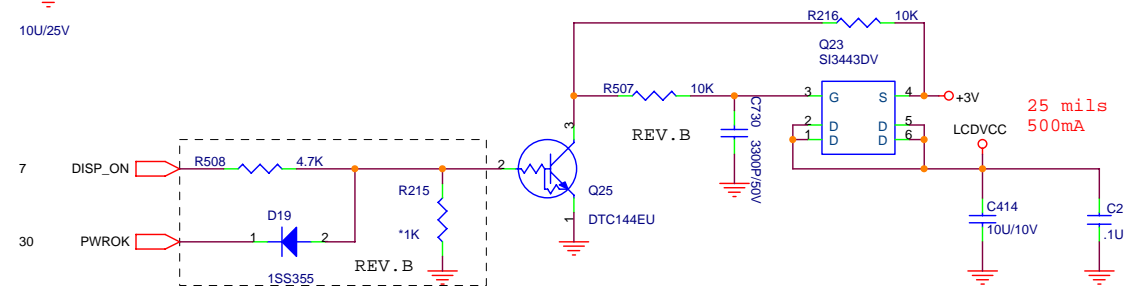
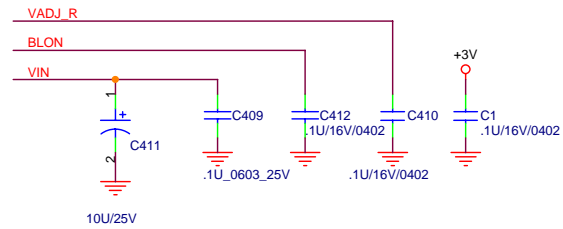
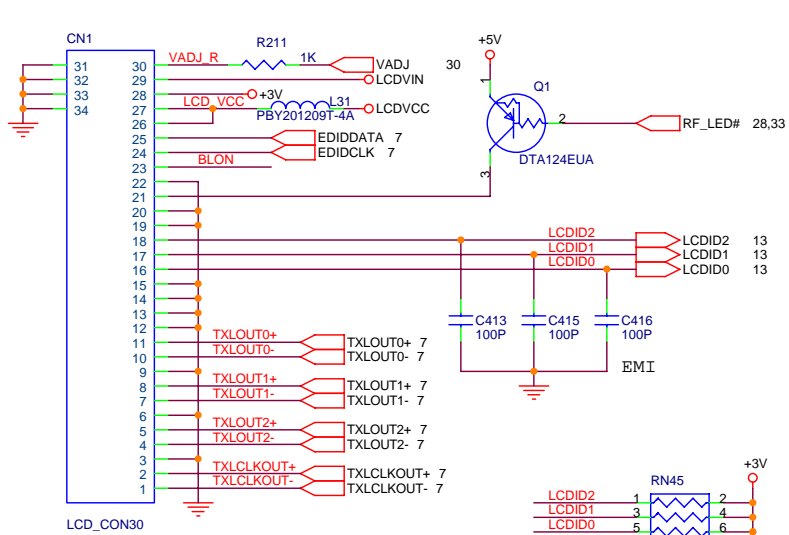
SB PCIE EEPROM STRAPS



MINI PCI TYPE III SLOT

PROJECT : CT8
Quanta Computer Inc.

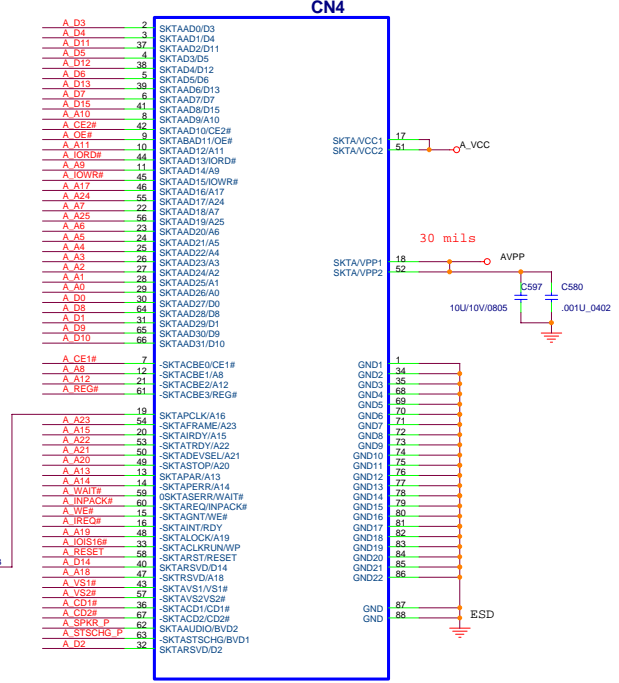
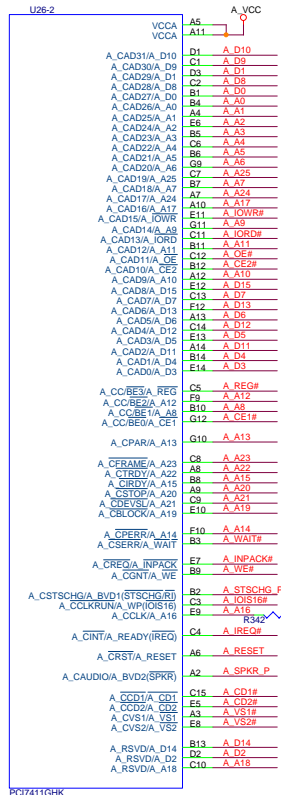
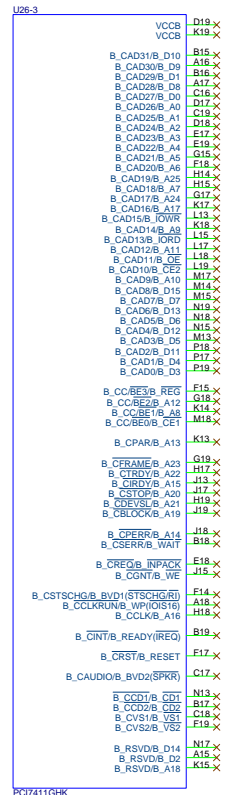
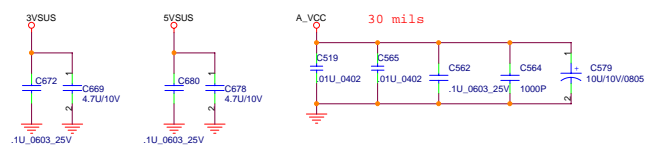
Size	Document Number	Rev
Custom		1A
Date:	Monday, December 13, 2004	Sheet 17 of 42



PROJECT : CT8
Quanta Computer Inc.

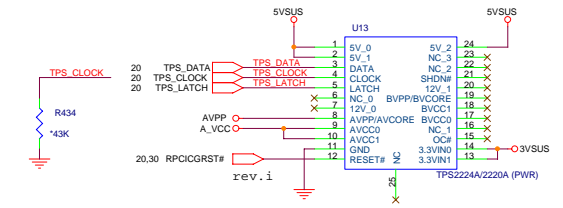
Size B	Document Number	Rev 1A
Date: Monday, December 13, 2004	Sheet 18 of 42	

CardBus Connector

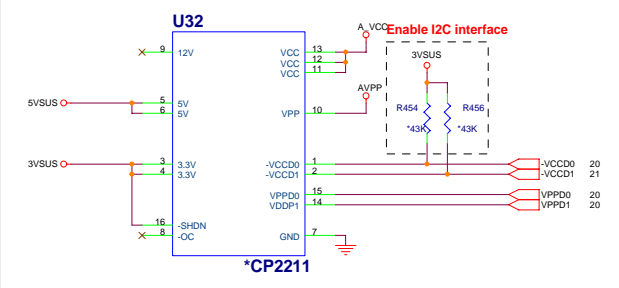


CARDBUS SLOT
FOX=WZ21131-G2

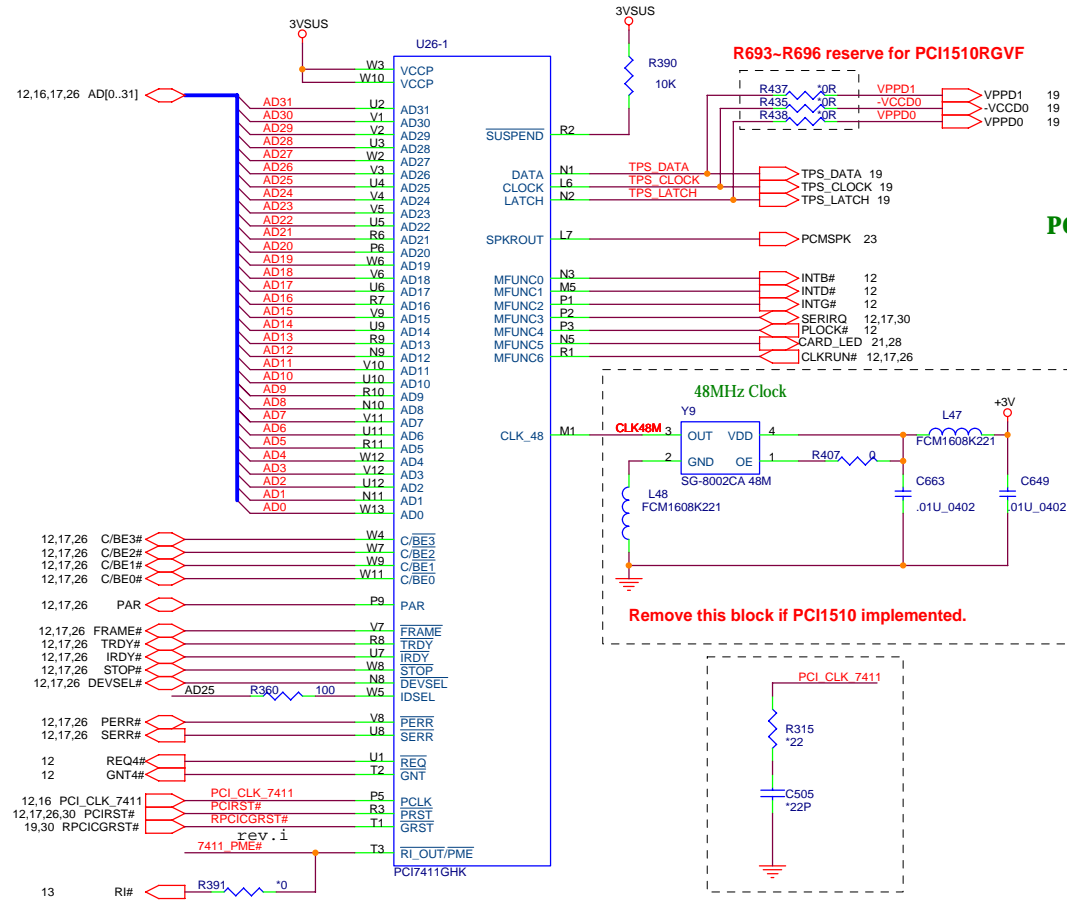
For PCI7411



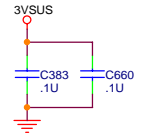
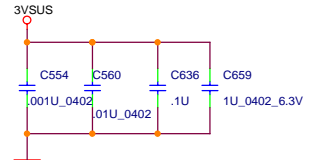
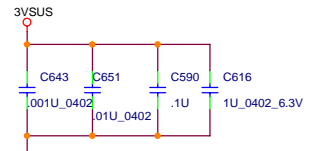
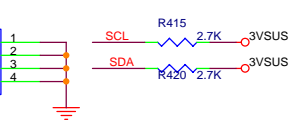
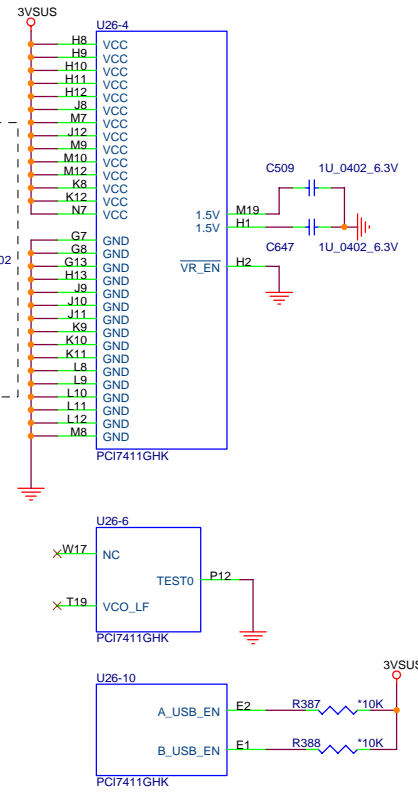
For PCI1510



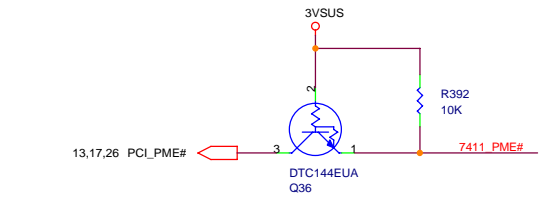
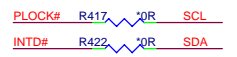
CardBus



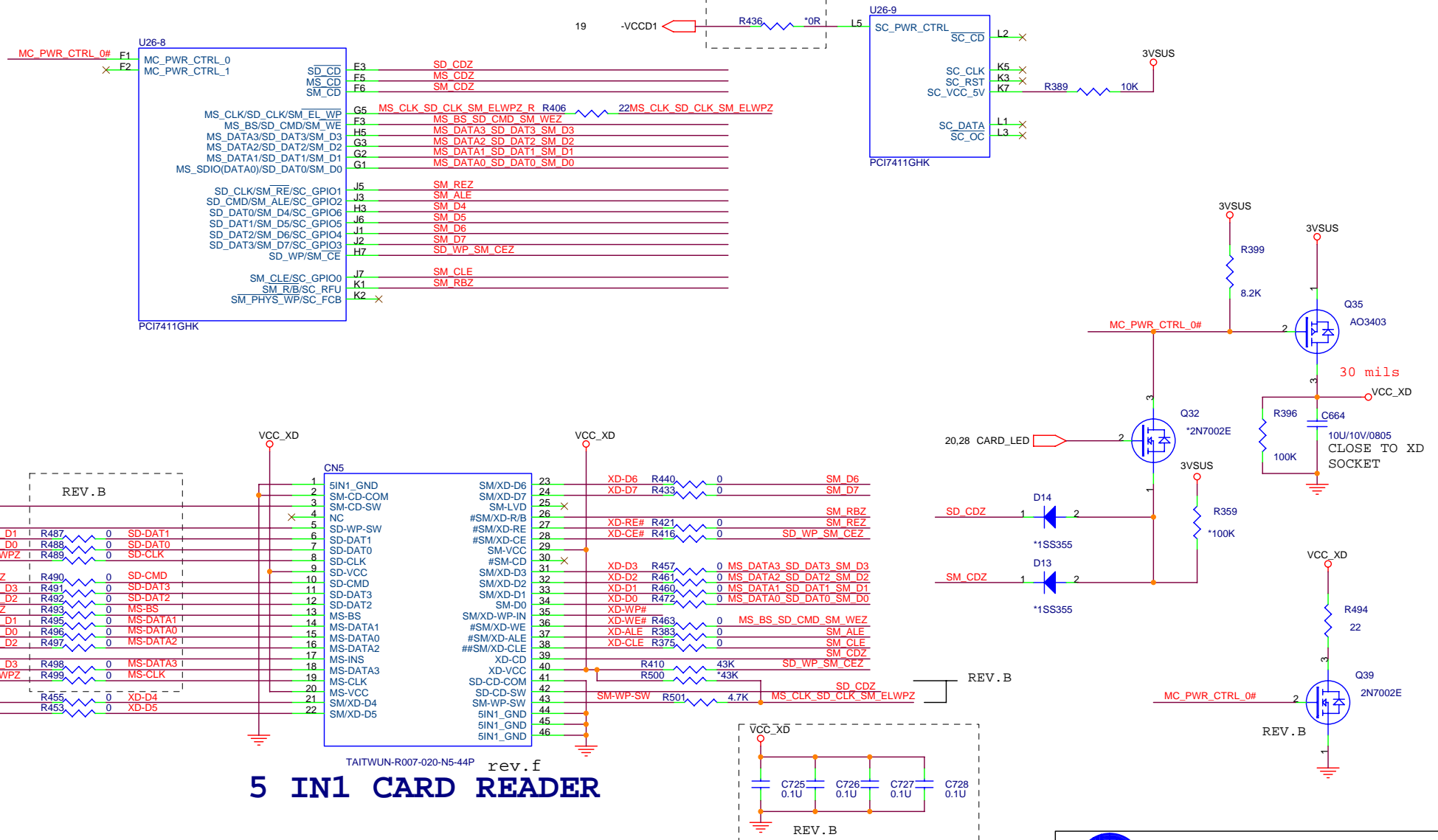
PCIXX21 Power Terminals



When -VCCD0 and -VCCD1 asserted high, PLOCK# and INTF# will provide a SDA signaling for I2C bus, PLOCK# will provide a SCL signaling for I2C bus. for PCI1510.



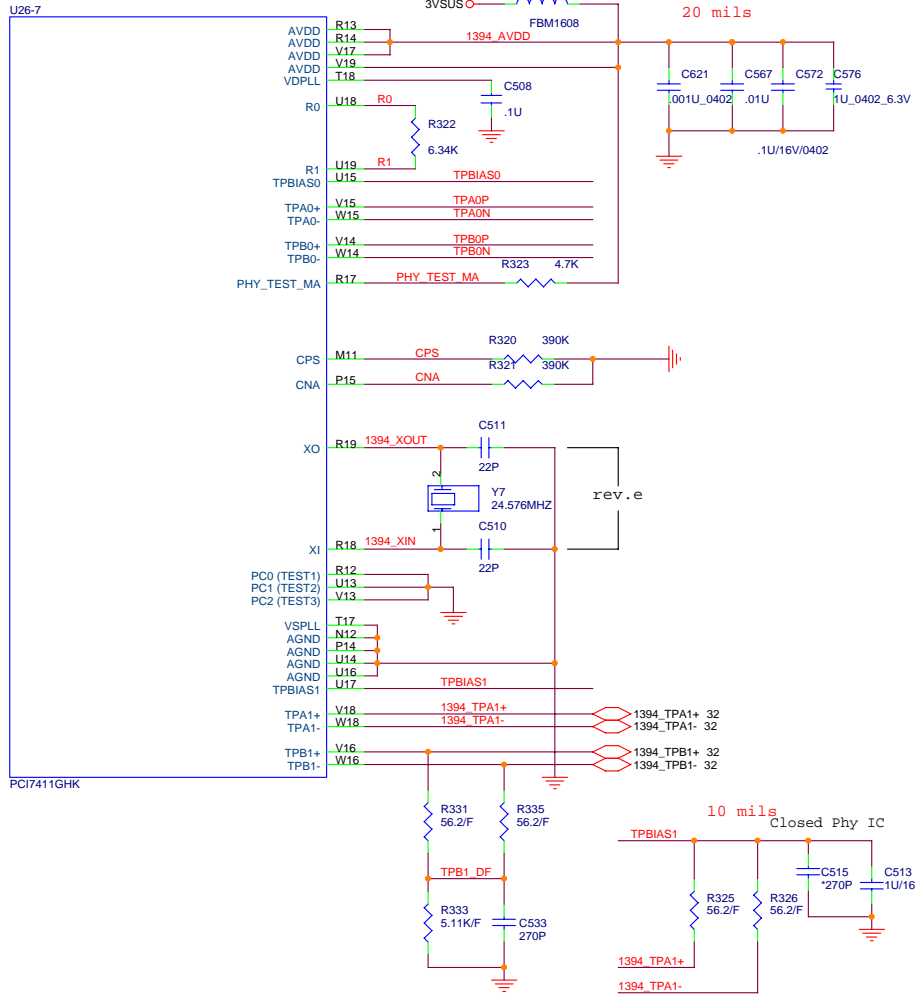
CARD POWER CONTROL



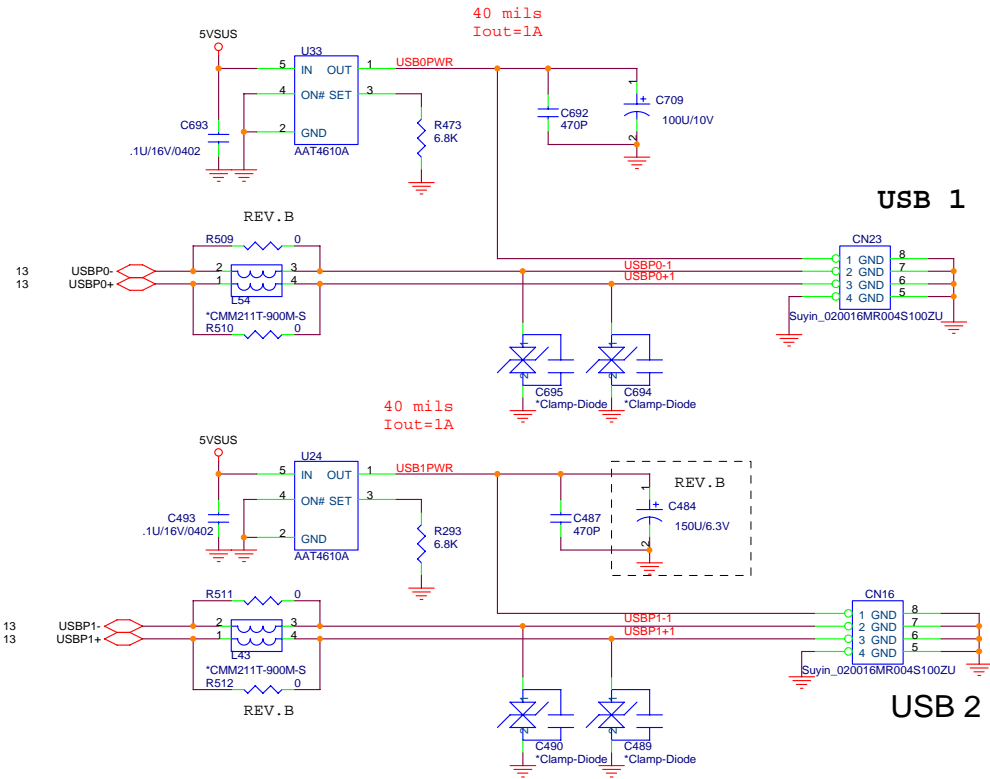
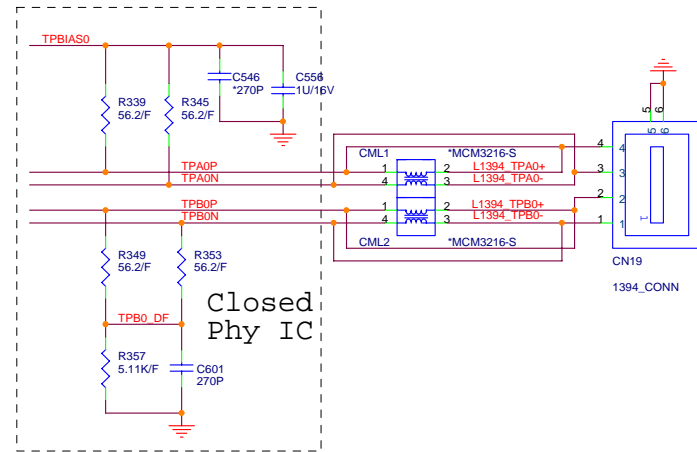
PROJECT : CT8
Quanta Computer Inc.

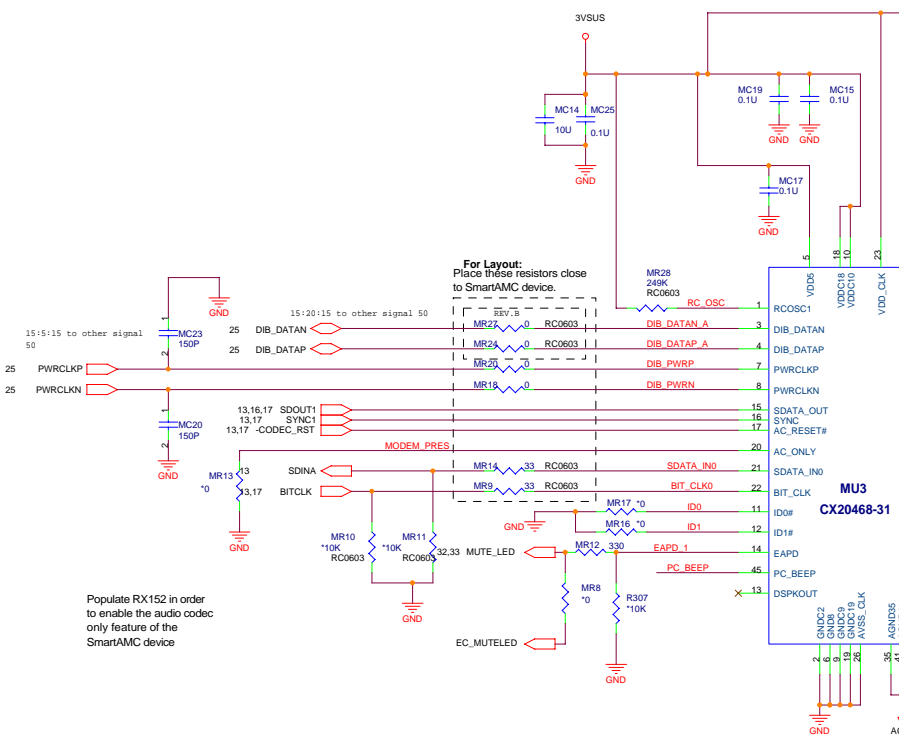
Size	Document Number	Rev
Custom		1A
Date:	Monday, December 13, 2004	Sheet 21 of 42

IEEE 1394a



IEEE 1394 CONNECTOR

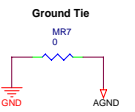
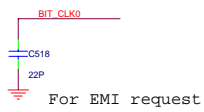




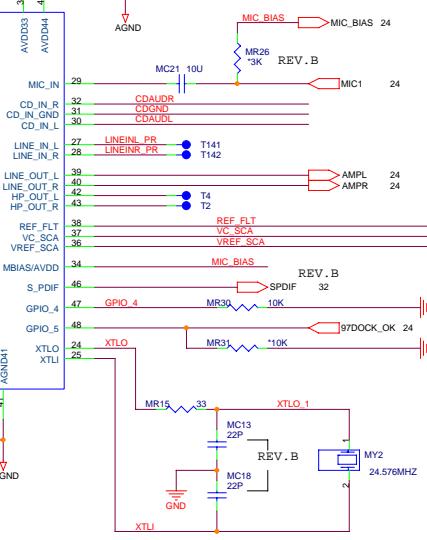
For Layout:
Place these resistors close to SmartAMC device.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

Populate RX152 in order to enable the audio codec only feature of the SmartAMC device

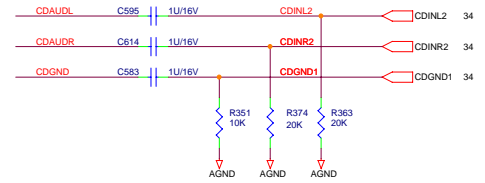


MU3
CX20468-31



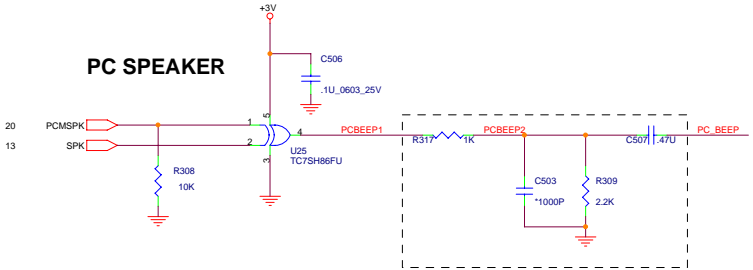
For Layout:

FROM CD-ROM



For Layout:
Place CX132, CX133, CX135, CX136 near SmartAMC device

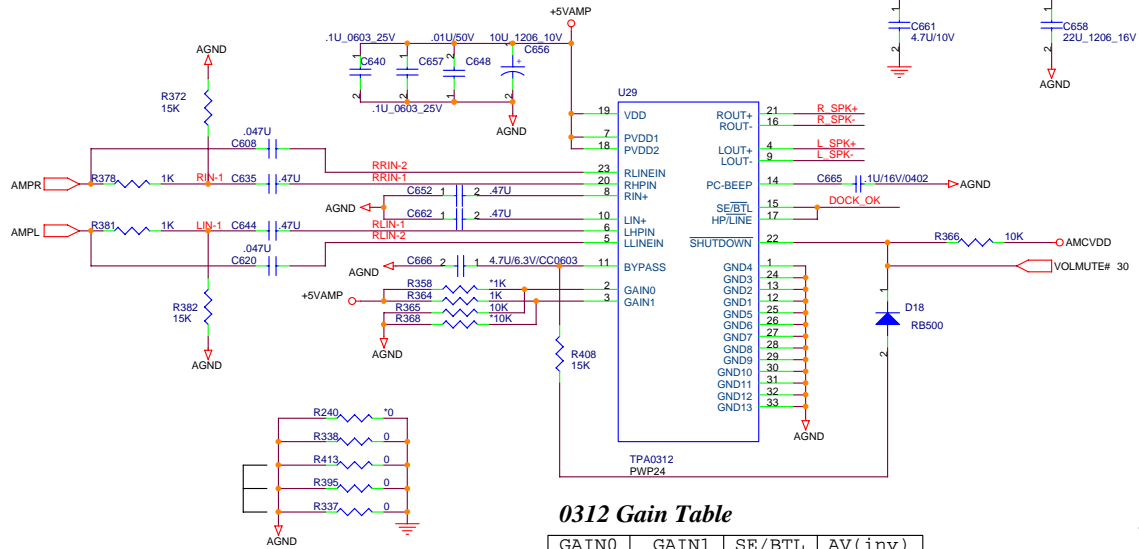
PC SPEAKER



Place crystal and associated circuitry very near SmartAMC Device.

CX20468-21:	ADD R20, MR8
	REMOVE MR12, R413, D24, MR30, MR31
	REV:B SETTING
CX20468-31:	ADD MR12, R413, D24, MR30
	REMOVE R20, MR31, MR8
CX20468-31 without software EQ:	ADD MR12, MR31, MR30
	REMOVE R413, D24, MR8, R20

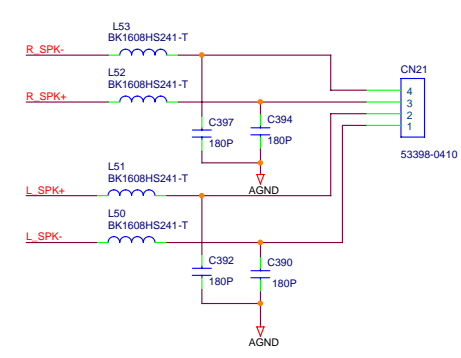
AUDIO AMPLIFIER



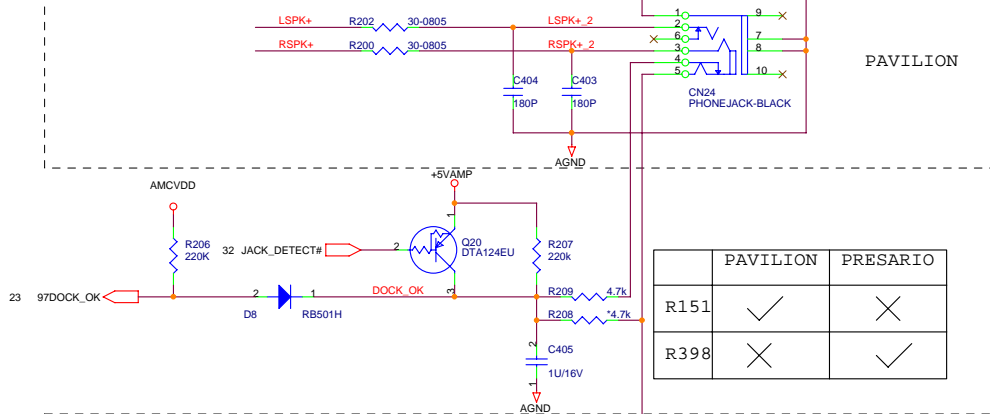
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV (inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

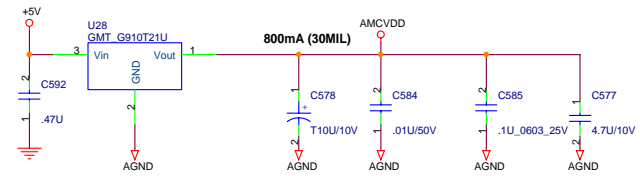
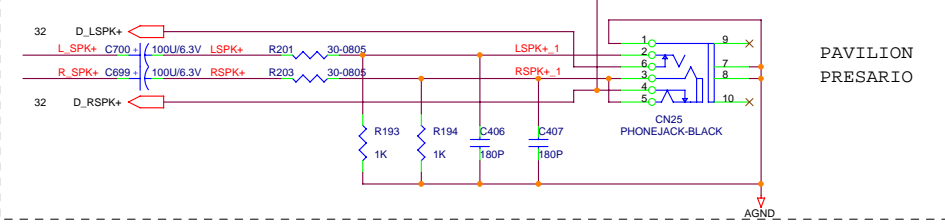
SPEAKER OUT



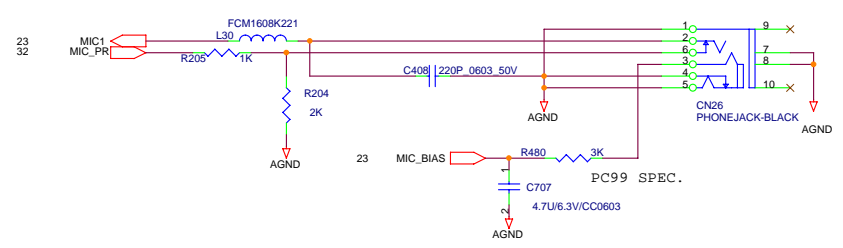
2ND HEADPHONE OUT



HEADPHONE OUT



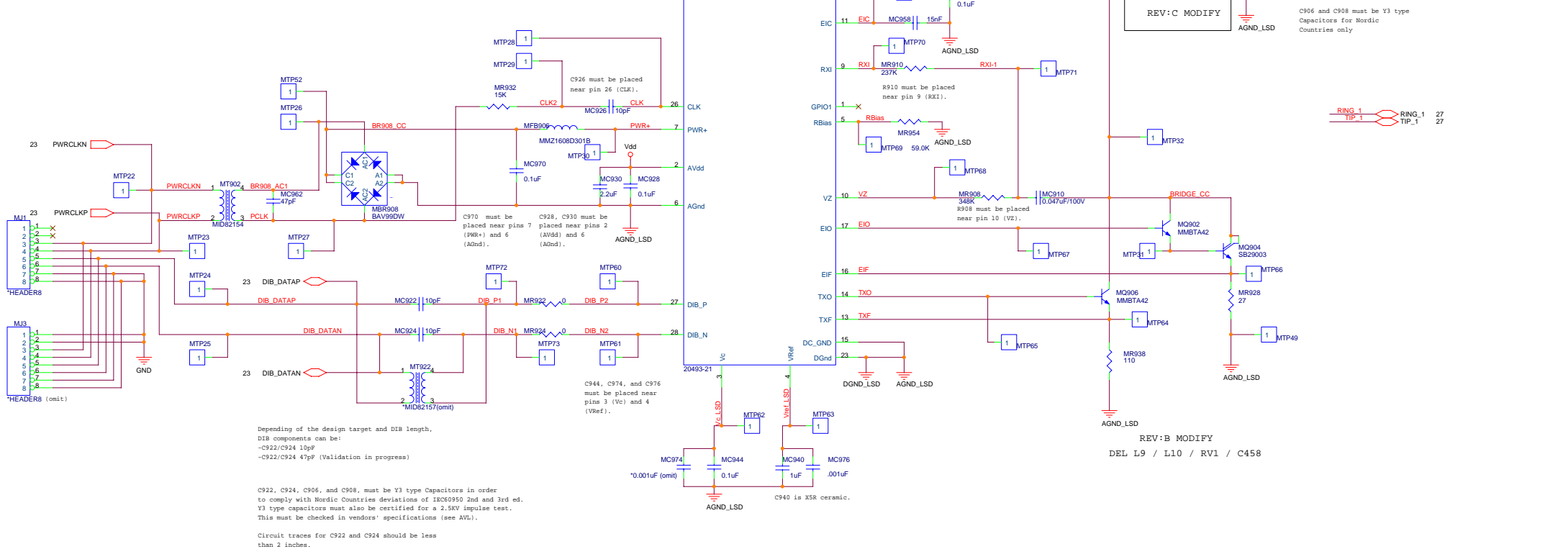
MICROPHONE



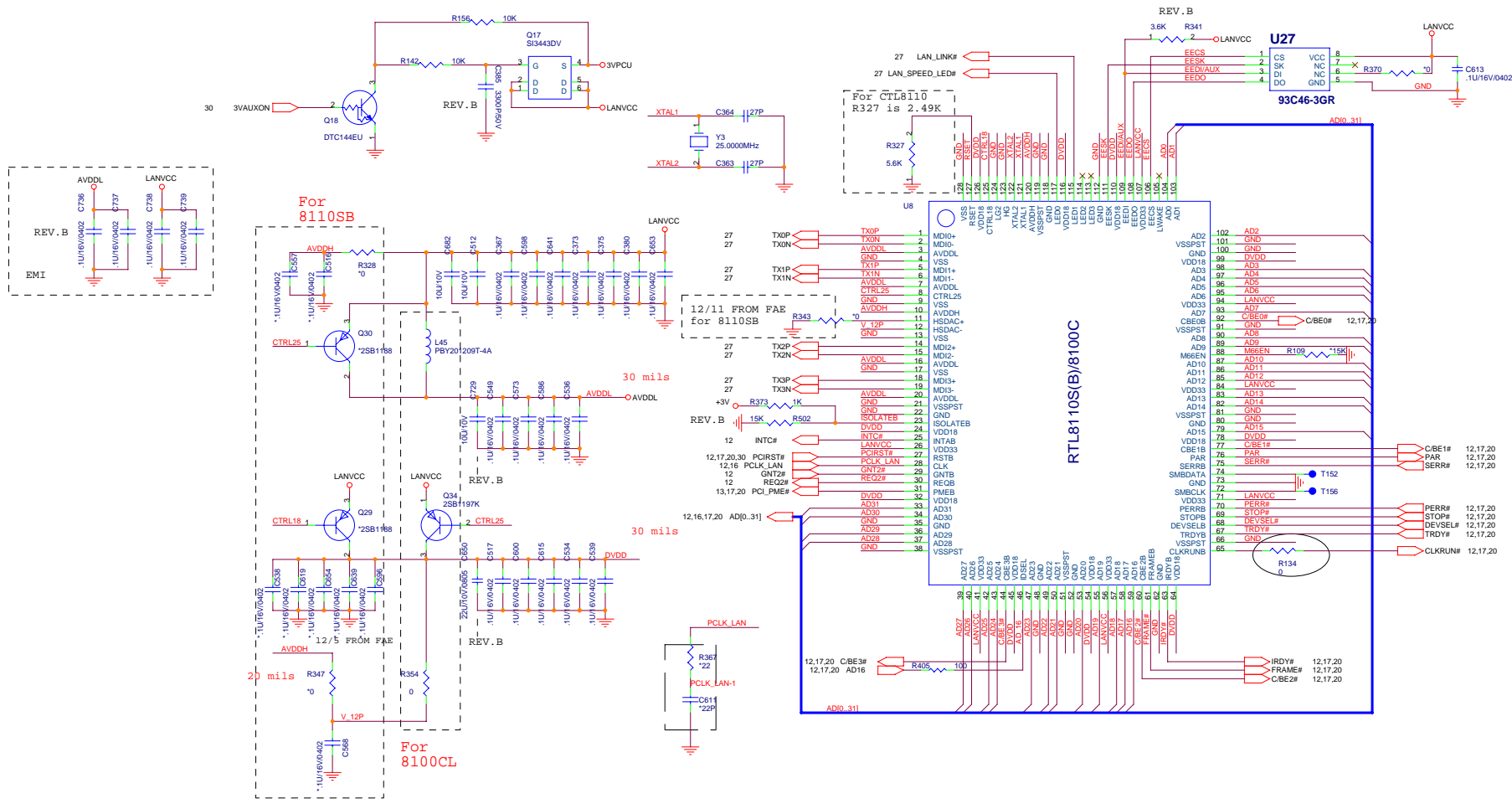
Revision History

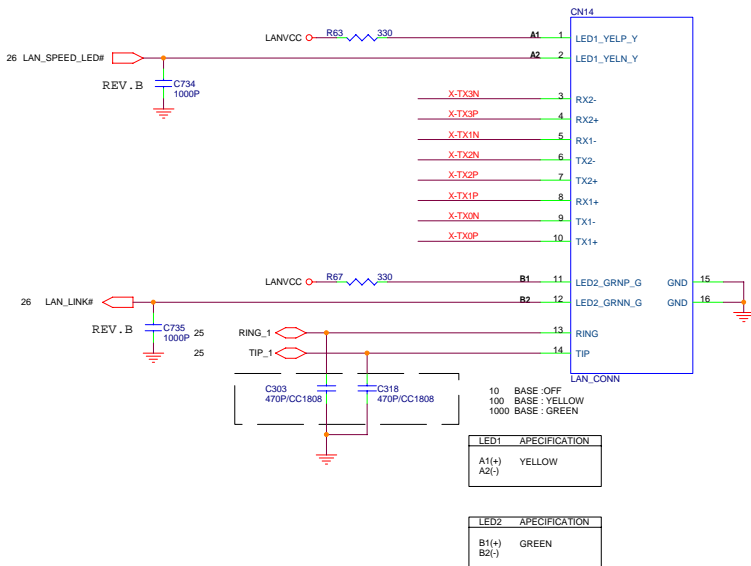
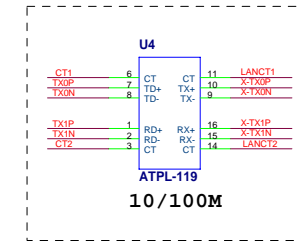
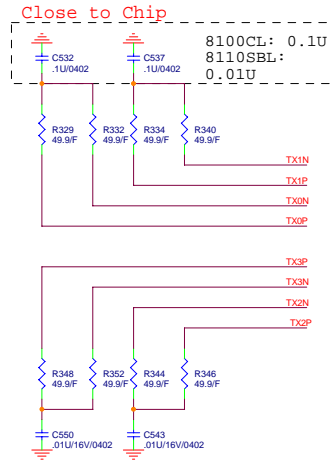
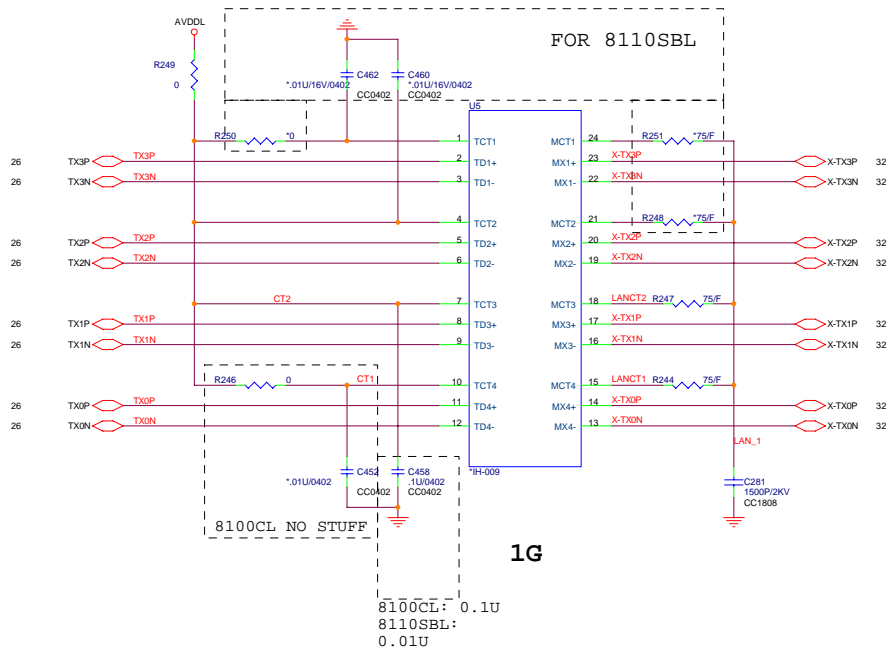
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators for MC986 from 3.3nF to 10nF, 100nF, +/-20%, V5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	September 24, 2003
08		November 06, 2003

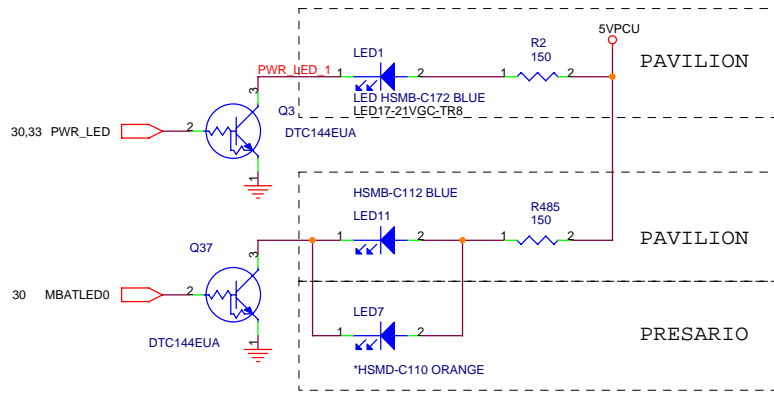
REV:B MODIFY FOR USE NEW MODEM MODULE



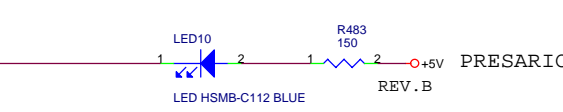
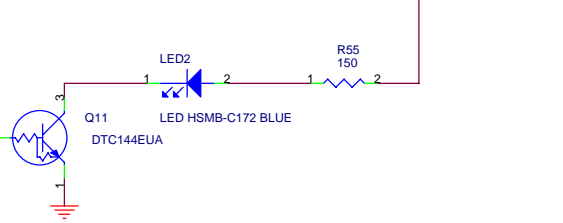
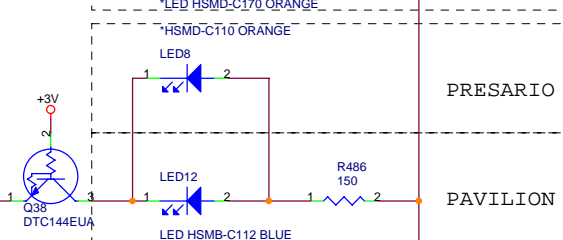
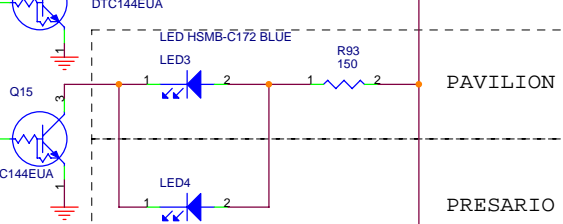
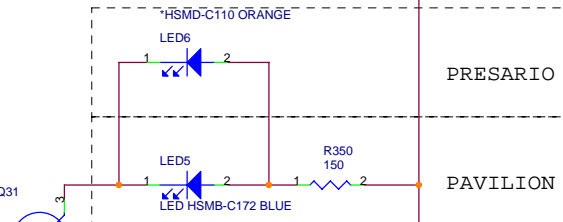
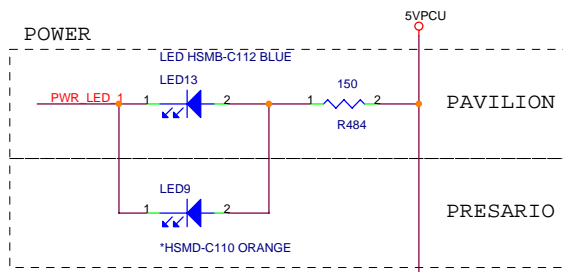
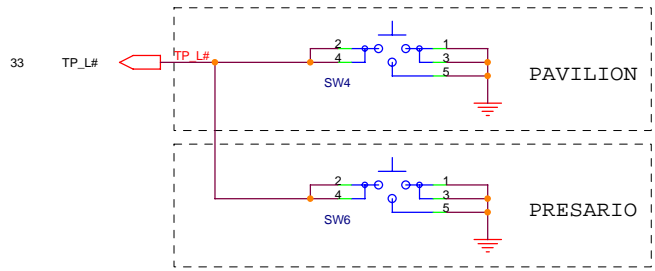
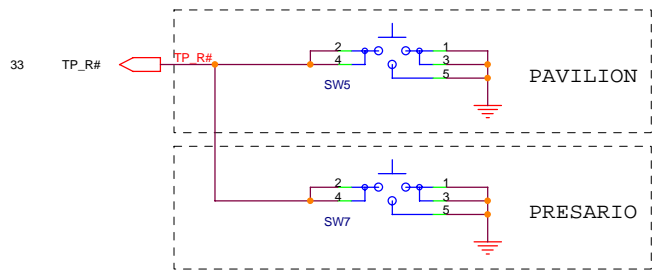
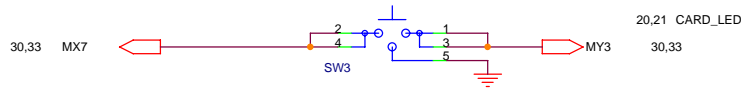
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120



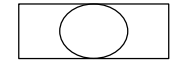




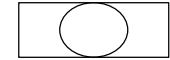
Touchpad control



LED HSMD-C170 ORANGE



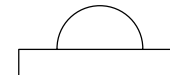
LED HSMB-C172 BLUE




LED HSMD-C110 ORANGE



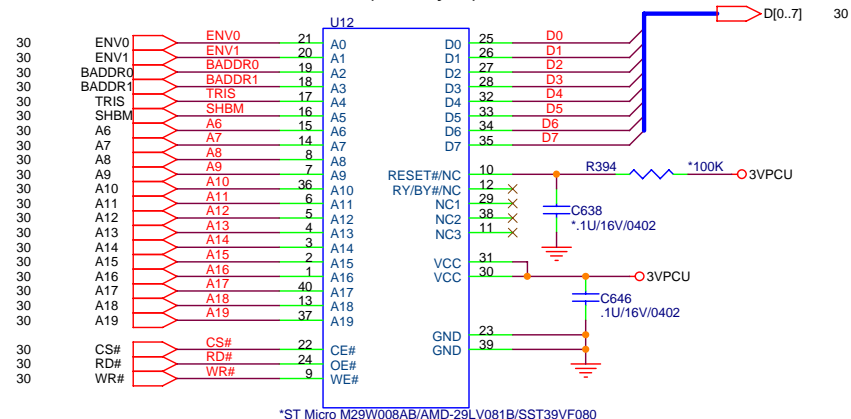
LED HSMD-C112 BLUE



REV.B: LED7 AND LED8 SWAP

 PROJECT : CT8 Quanta Computer Inc.		Rev 1A
		Document Number
Size Custom	Date: Monday, December 13, 2004	Sheet 28 of 42

8Mbit (1M Byte), TSSOP40

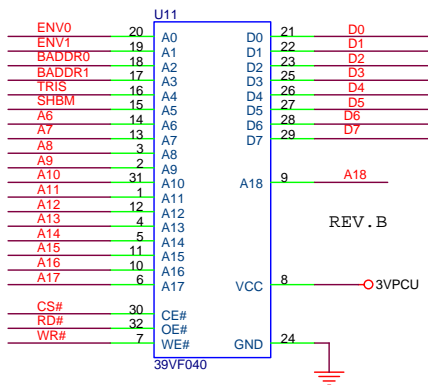


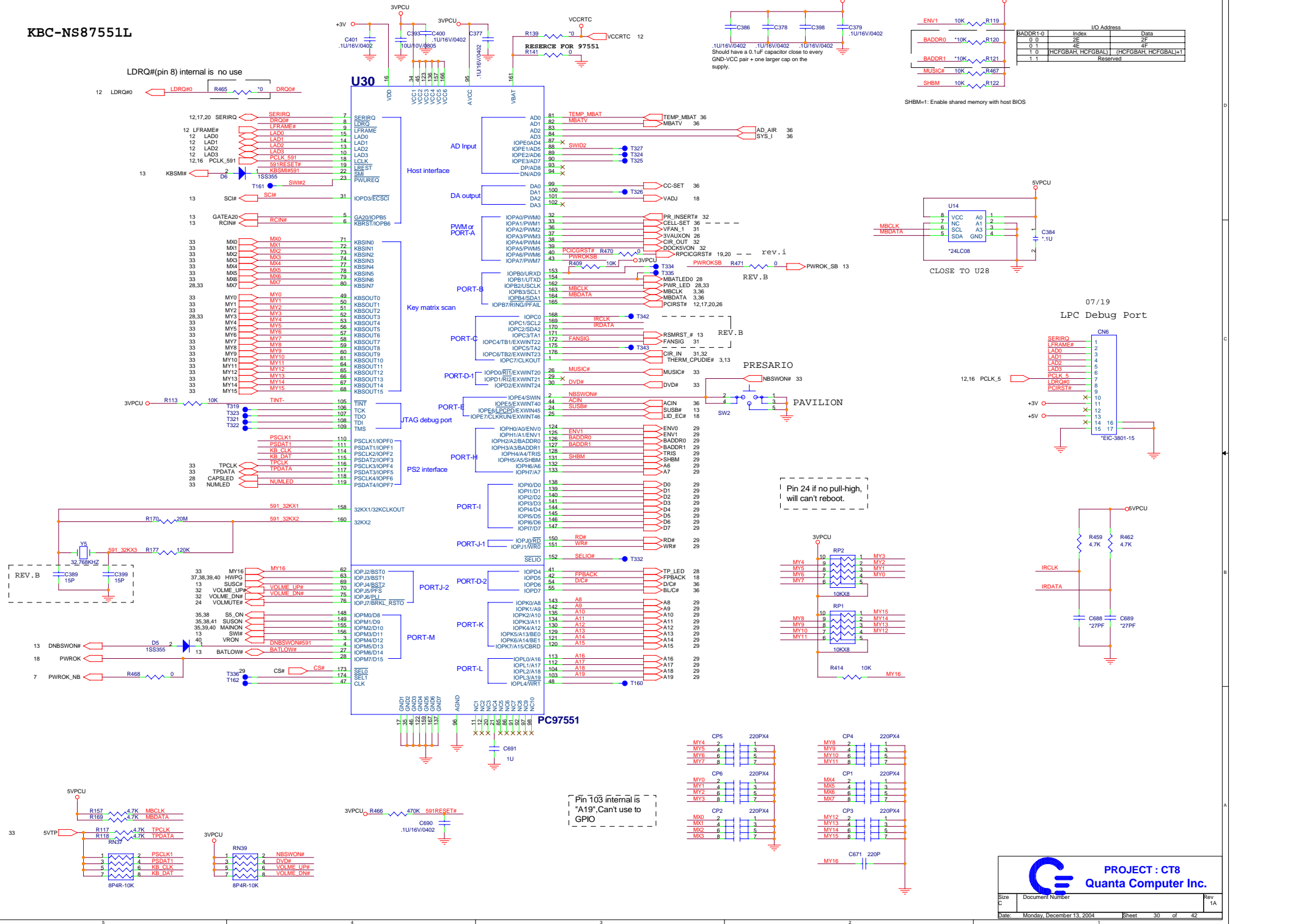
*ST Micro M29W008AB/AMD-29LV081B/SST39VF080

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100ms reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32



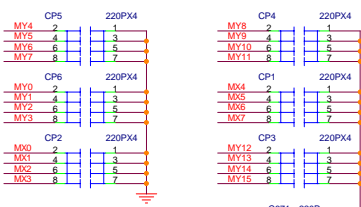


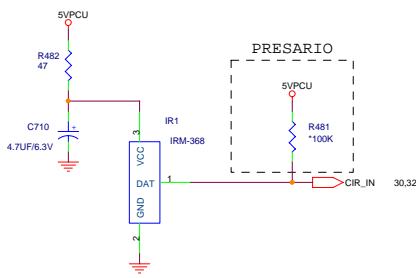
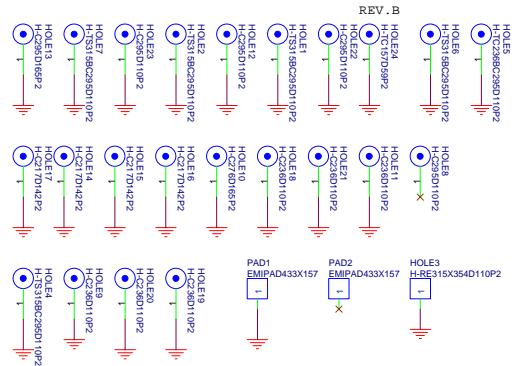
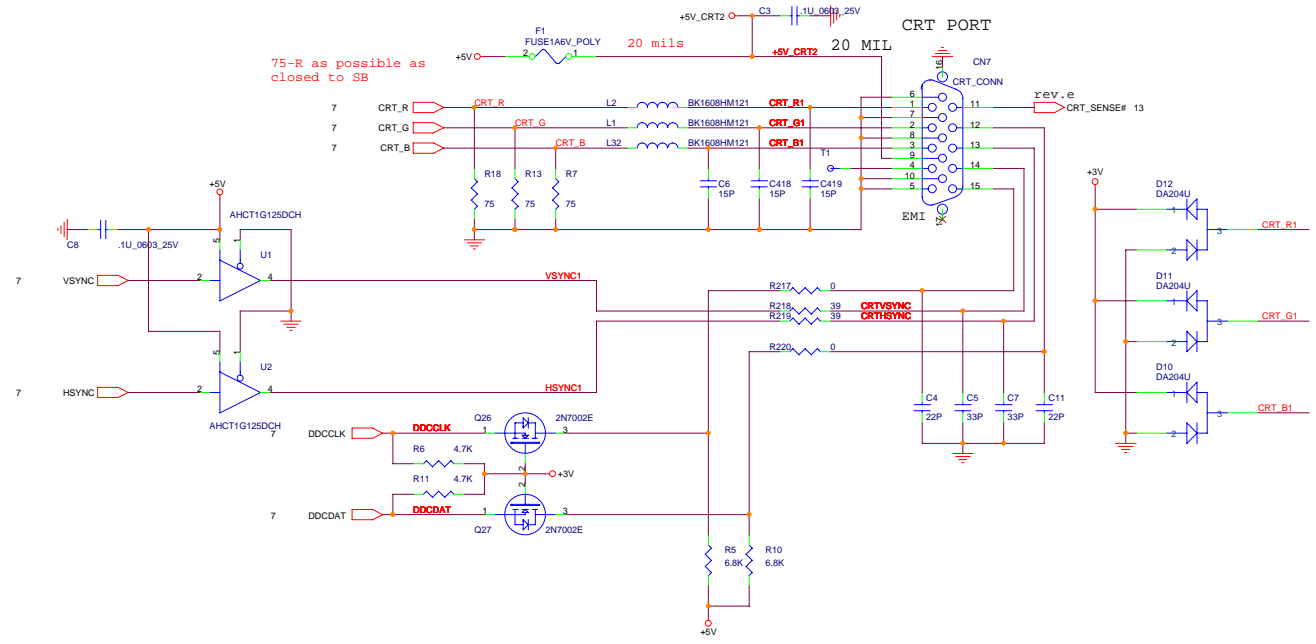
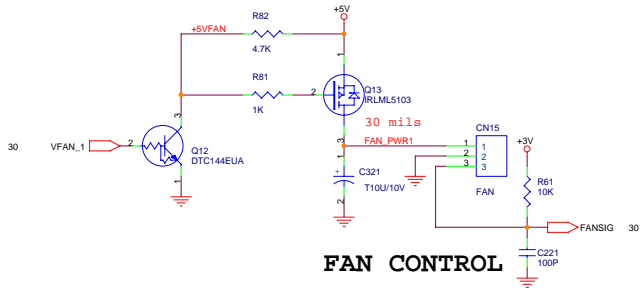
IO Address			
BADDR1-0	Index	Data	
0 0	2E	2F	4F
0 1	4E	4F	4F
1 0	HCFCGBAH, HCFCGBAL	HCFCGBAH, HCFCGBAL	HCFCGBAL+1
1 1	Reserved		

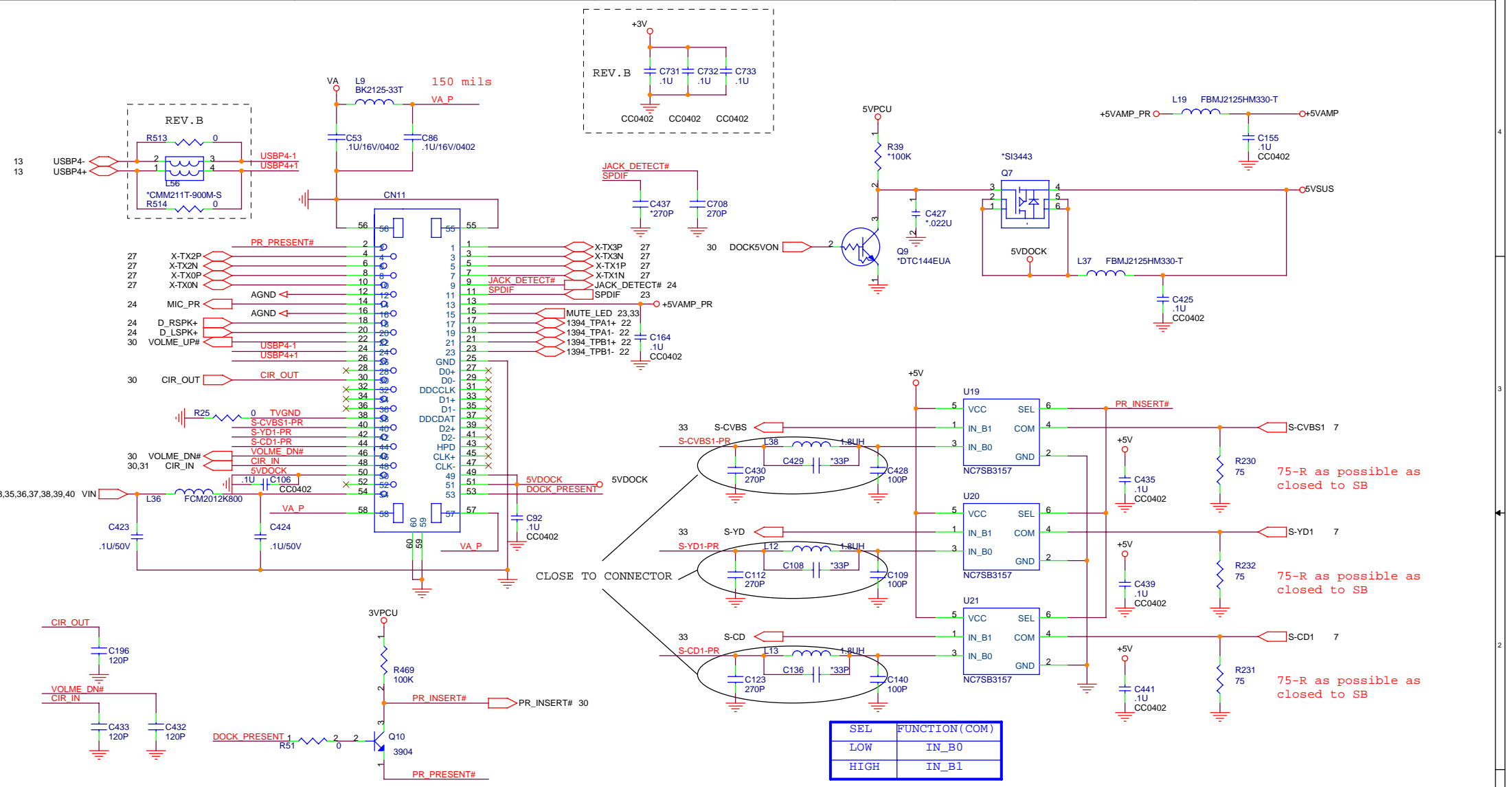
07/19
LPC Debug Port

Pin 24 if no pull-high, will can't reboot.

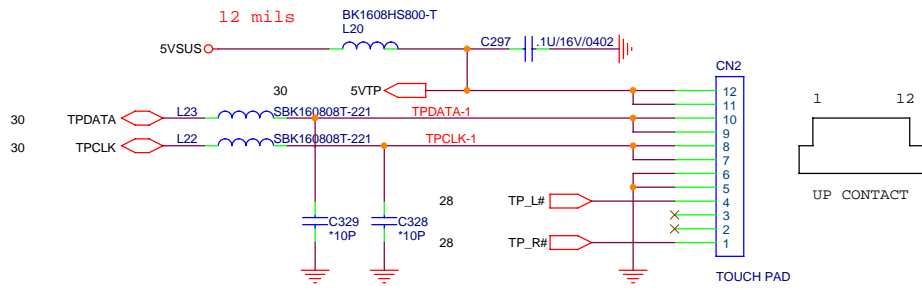
Pin 103 internal is "A19", Can't use to GPIO





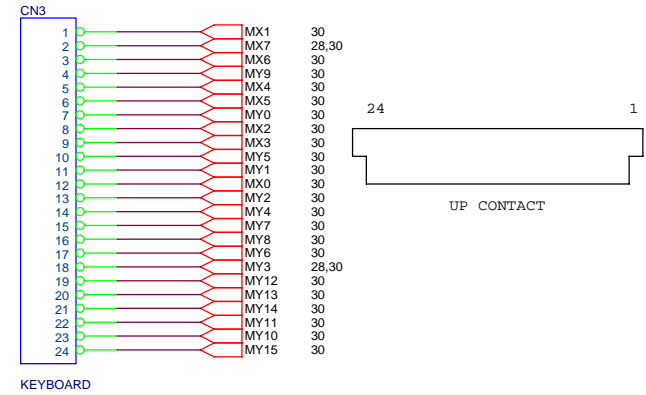


TOUCH PAD CONNECTOR

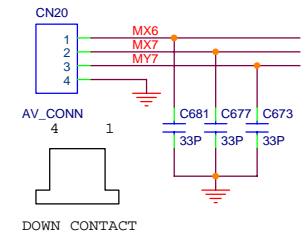


CHECK PIN DEFINE

KEYBOARD CONNECTOR

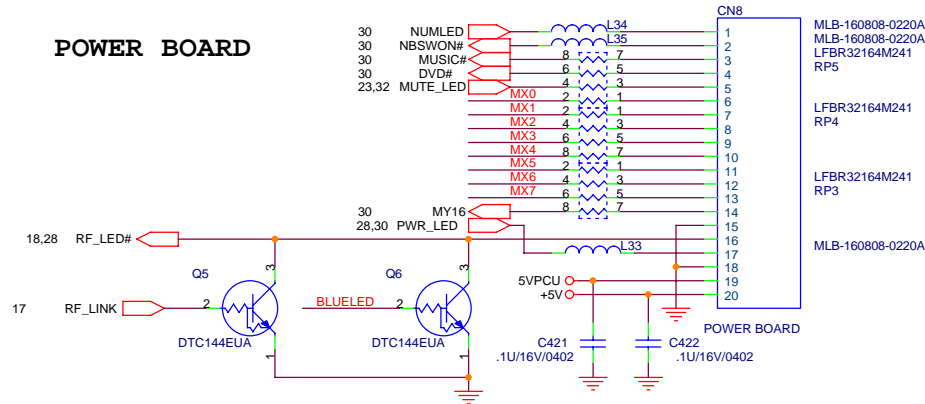


AV BOARD



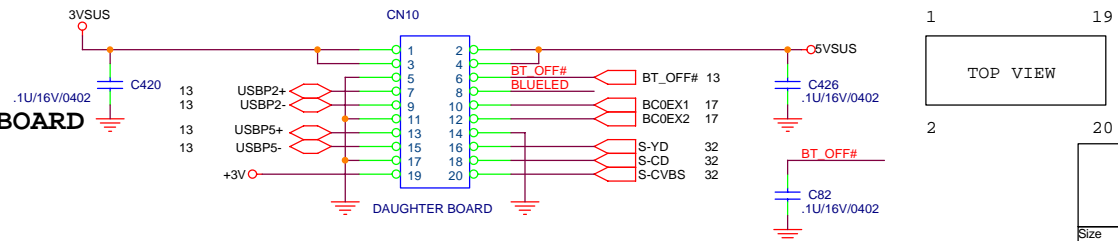
MX6	MX7
ENTER	MENU

POWER BOARD



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARD	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD

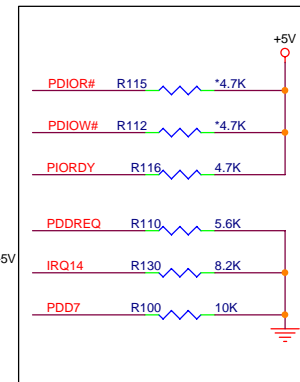
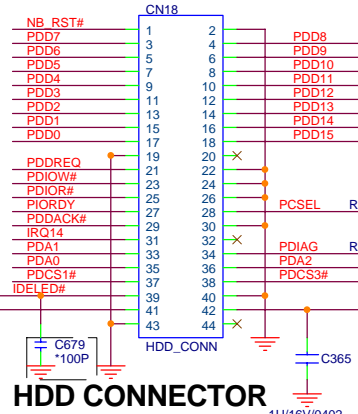
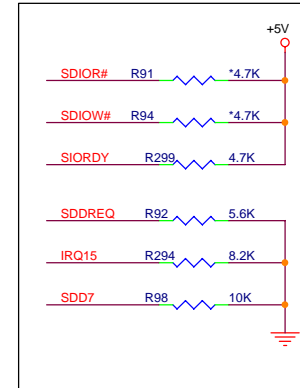
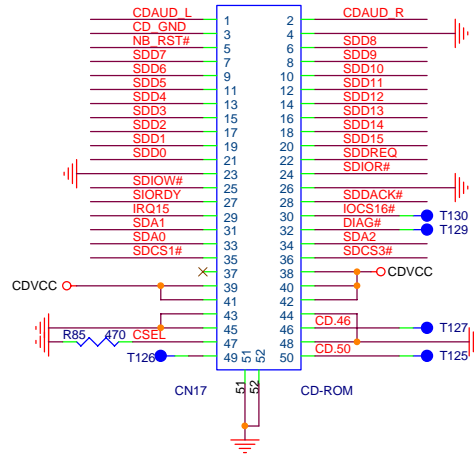
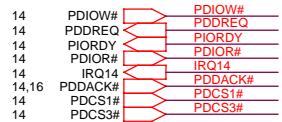
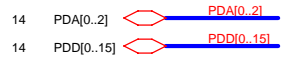
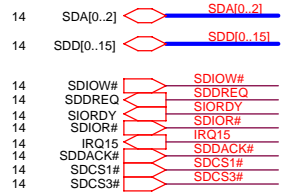
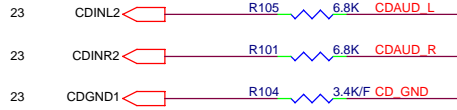
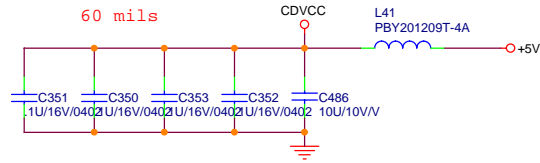


PROJECT : CT8
Quanta Computer Inc.

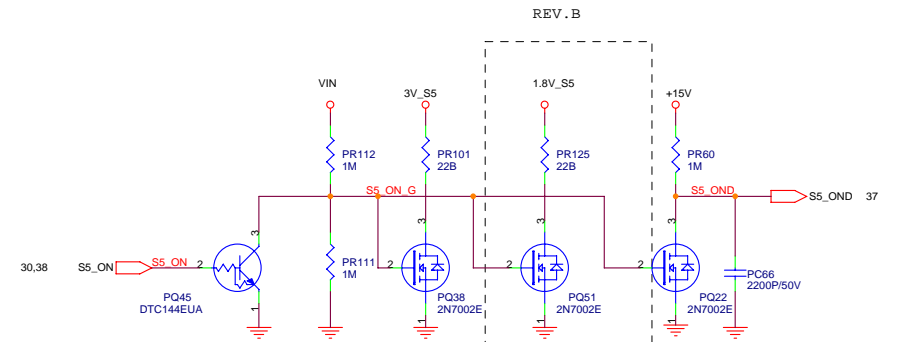
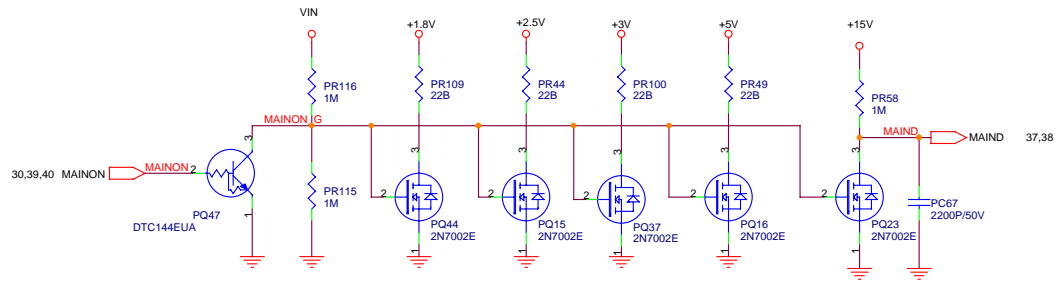
Size	Document Number	Rev
Custom	MDC	1A

Date: Monday, December 13, 2004 Sheet 33 of 42

CD-ROM

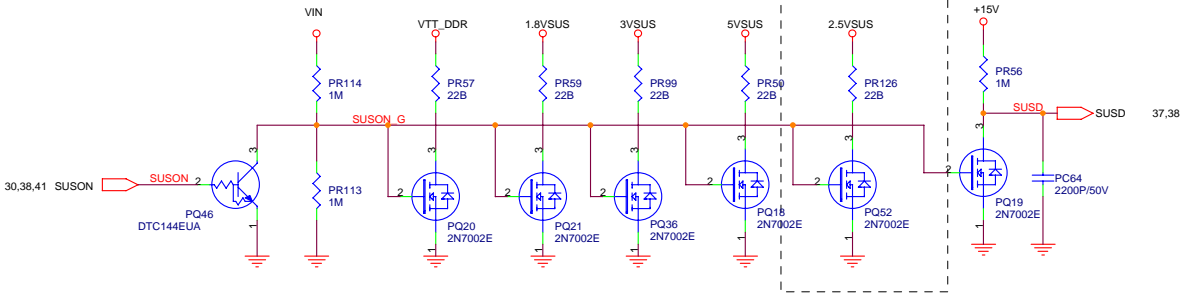


PROJECT : CT8
Quanta Computer Inc.



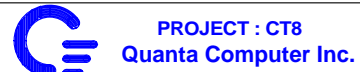
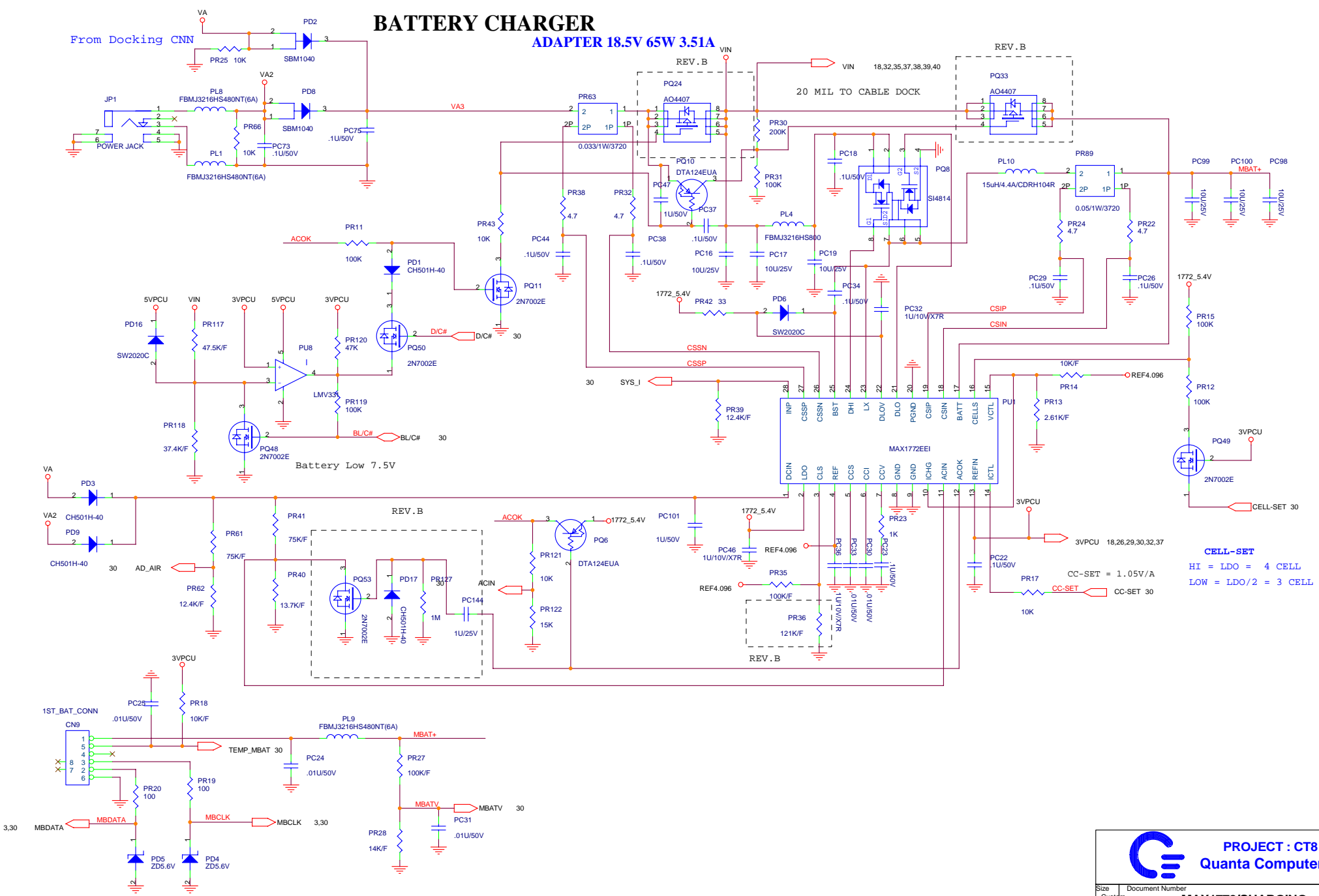
REV . B

REV . B



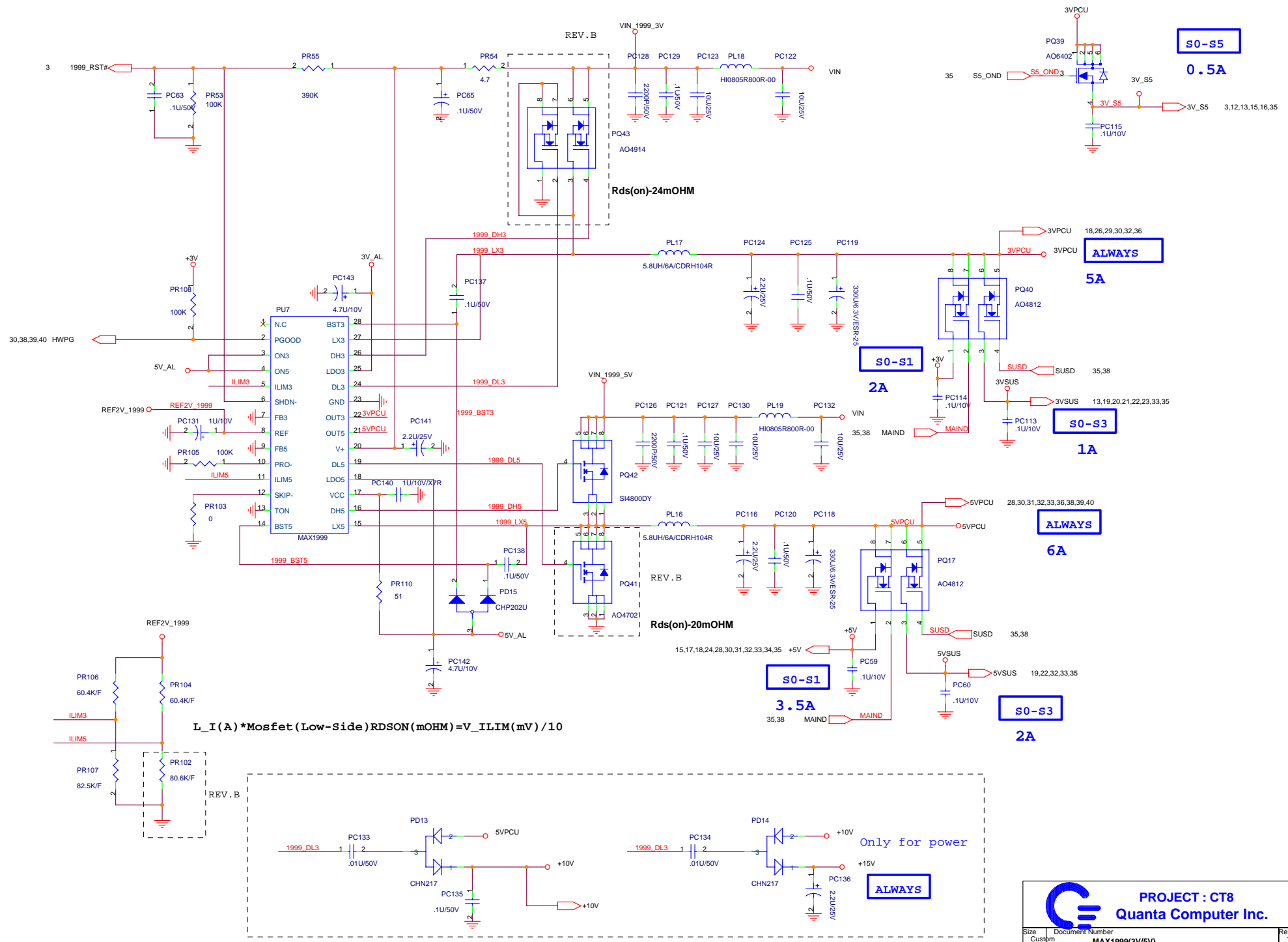
BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A

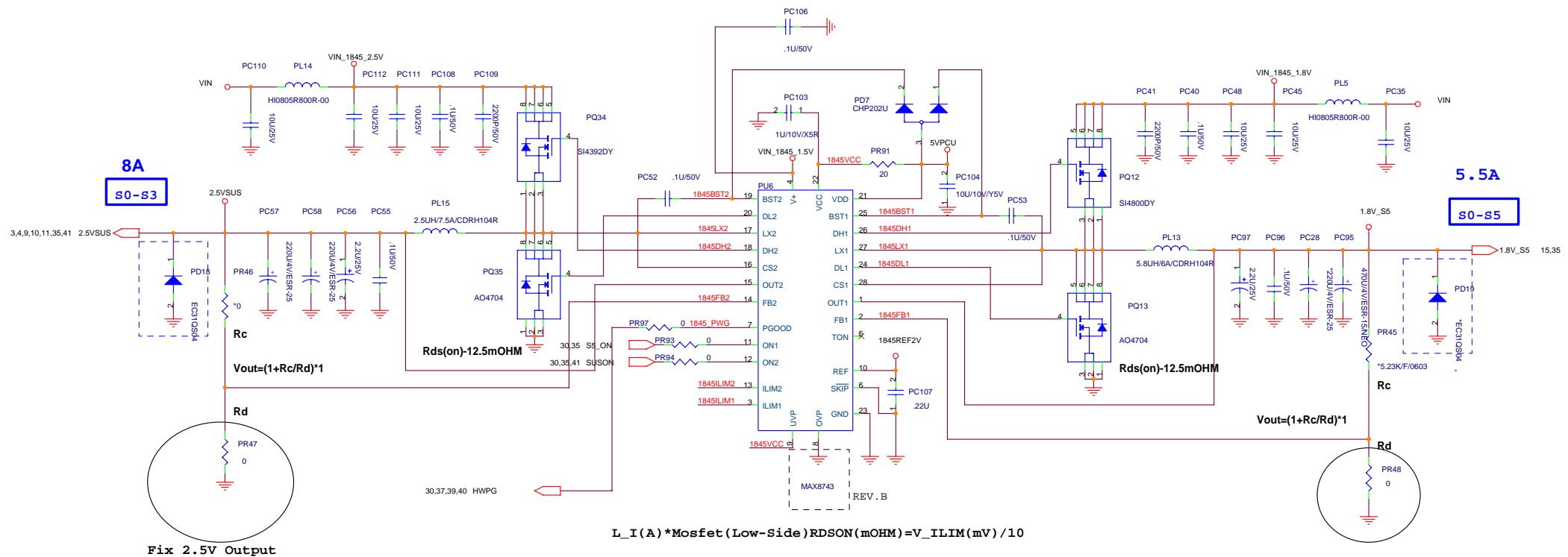


PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1772/CHARGING	3A
Date:	Monday, December 13, 2004	Sheet 36 of 42



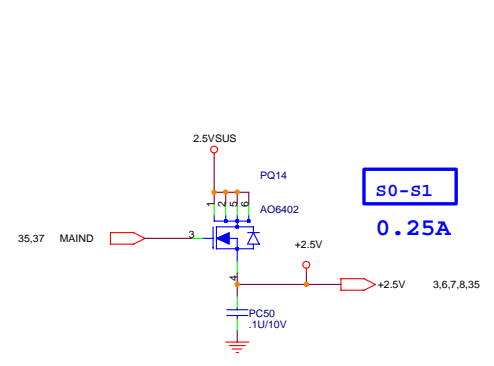
$$I_L (A) * \text{Mosfet (Low-Side) } R_{DS(ON)} (m\Omega) = V_{ILIM} (mV) / 10$$



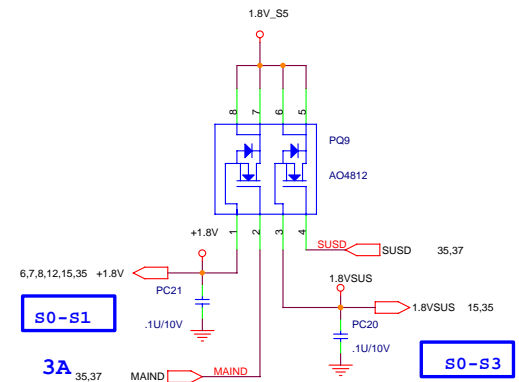
Fix 2.5V Output

Fix 1.8V Output

$$L_I (A) * \text{Mosfet (Low-Side)} R_{DS(on)} (m\Omega) = V_{ILIM} (mV) / 10$$



S0-S1
0.25A



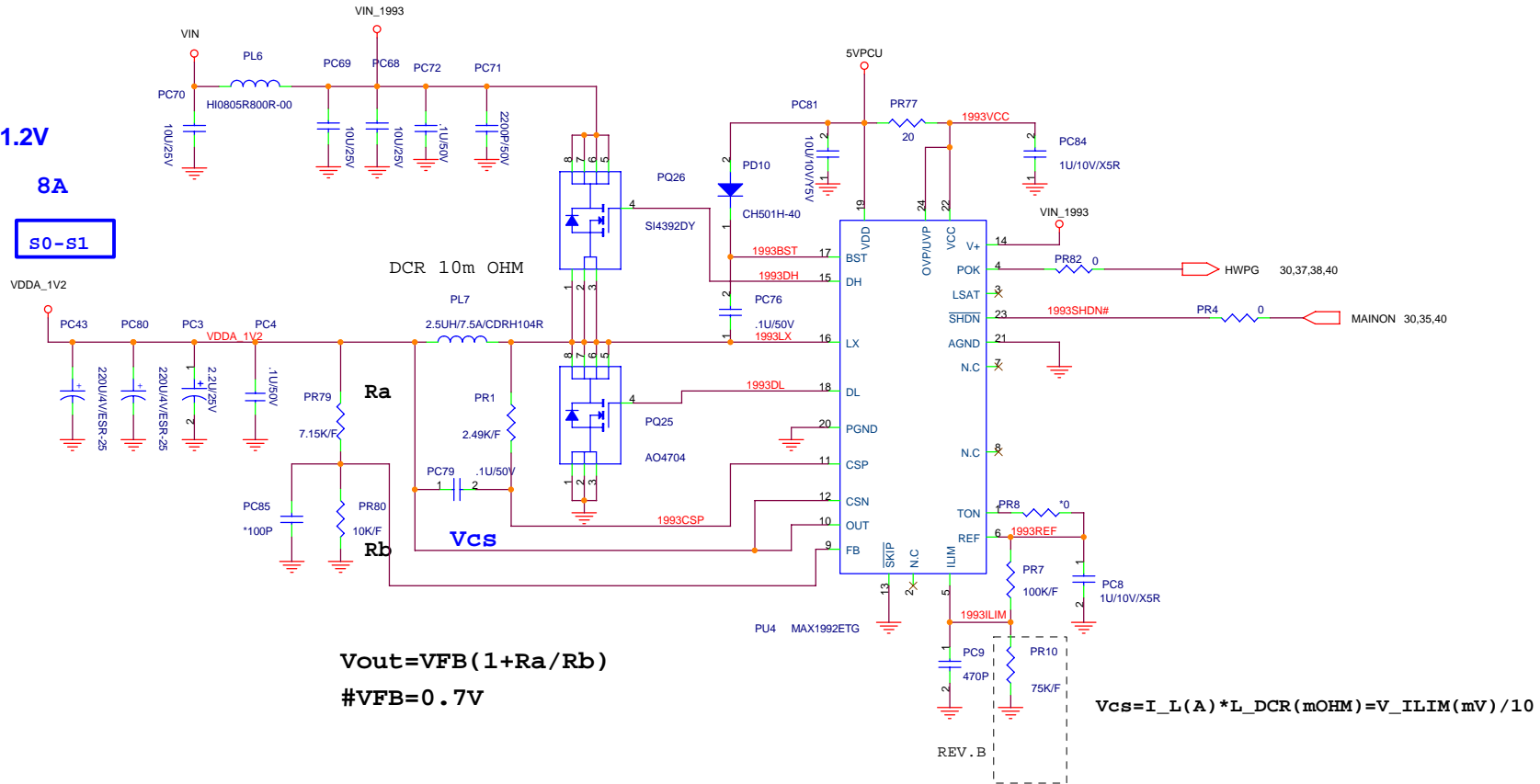
S0-S1
3A

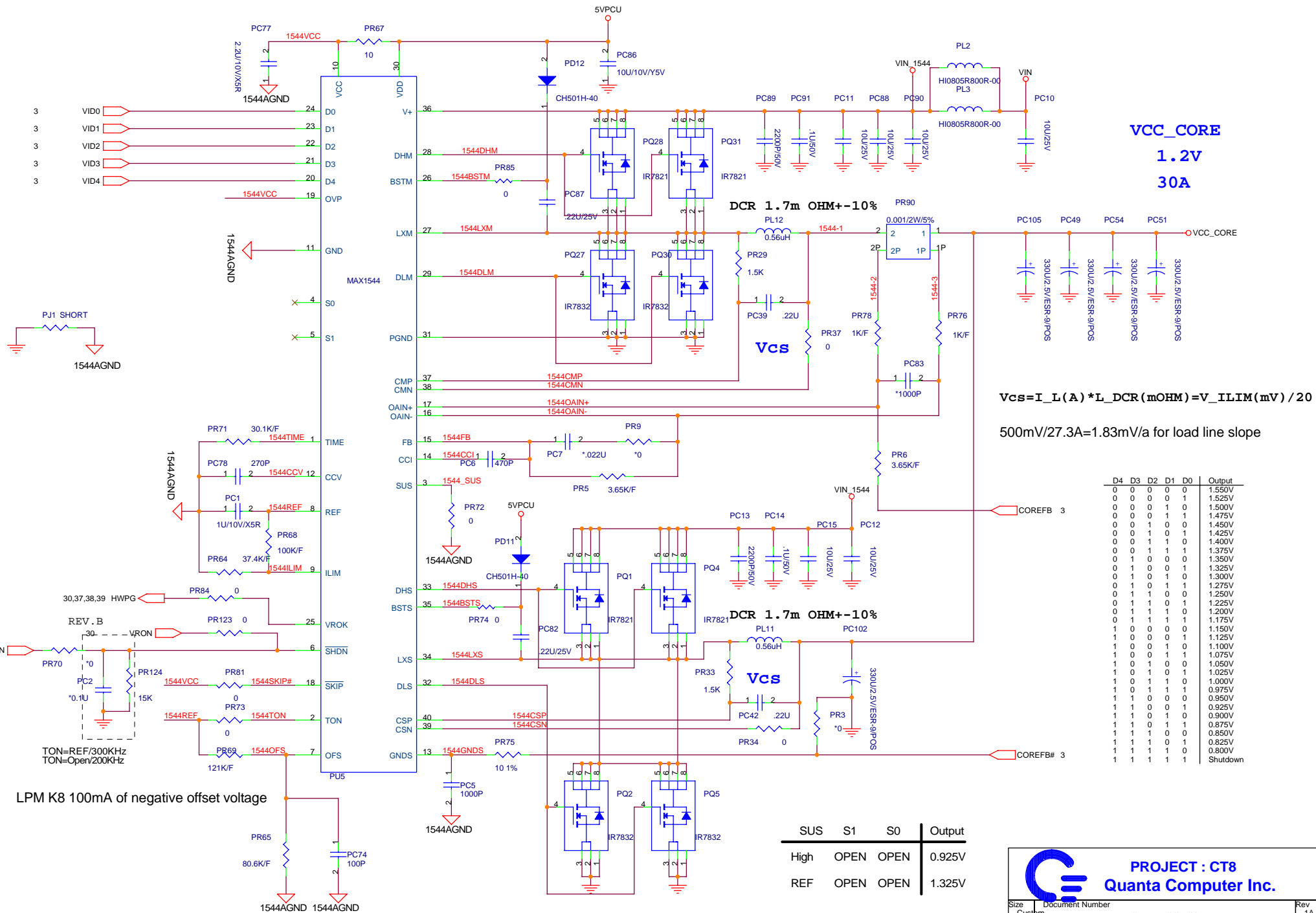
S0-S3
0.2A

1.2V

8A

S0-S1





VCC_CORE
1.2V
30A

DCR 1.7m OHM+-10%

Vcs

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 20$$

500mV/27.3A = 1.83mV/a for load line slope

D4	D3	D2	D1	D0	Output
0	0	0	0	0	1.550V
0	0	0	0	1	1.525V
0	0	0	0	1	1.500V
0	0	0	0	1	1.475V
0	0	0	1	0	1.450V
0	0	0	1	0	1.425V
0	0	0	1	0	1.400V
0	0	1	0	0	1.375V
0	0	1	0	0	1.350V
0	0	1	0	0	1.325V
0	0	1	0	0	1.300V
0	1	0	0	0	1.275V
0	1	0	0	0	1.250V
0	1	0	0	1	1.225V
0	1	0	1	0	1.200V
0	1	0	1	0	1.175V
0	1	0	1	0	1.150V
0	1	0	1	0	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	1	0	0	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	0	1	0.950V
1	1	0	0	0	0.925V
1	1	0	0	1	0.900V
1	1	0	1	0	0.875V
1	1	0	1	0	0.850V
1	1	1	0	0	0.825V
1	1	1	0	1	0.800V
1	1	1	1	1	Shutdown

SUS	S1	S0	Output
High	OPEN	OPEN	0.925V
REF	OPEN	OPEN	1.325V

LPM K8 100mA of negative offset voltage

PROJECT : CT8
Quanta Computer Inc.

Size: Custom Document Number: CPU VCC CORE Rev: 1A

Date: Monday, December 13, 2004 Sheet: 40 of 42

