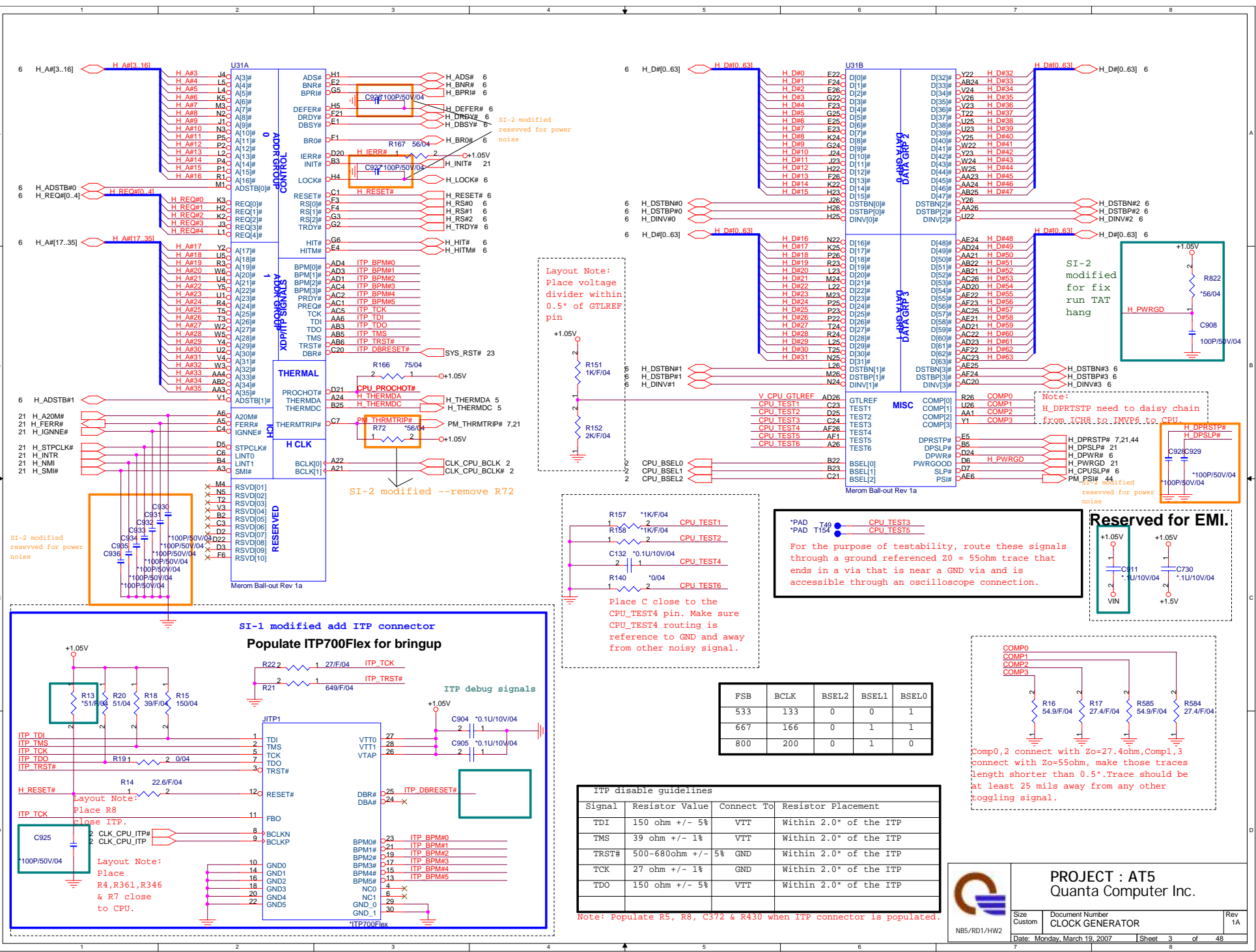


**PROJECT : AT5**  
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Layout Note:  
Place voltage divider within 0.5" of GTLREF pin

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU\_TEST4 pin. Make sure CPU\_TEST4 routing is reference to GND and away from other noisy signal.

Reserved for EMI.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

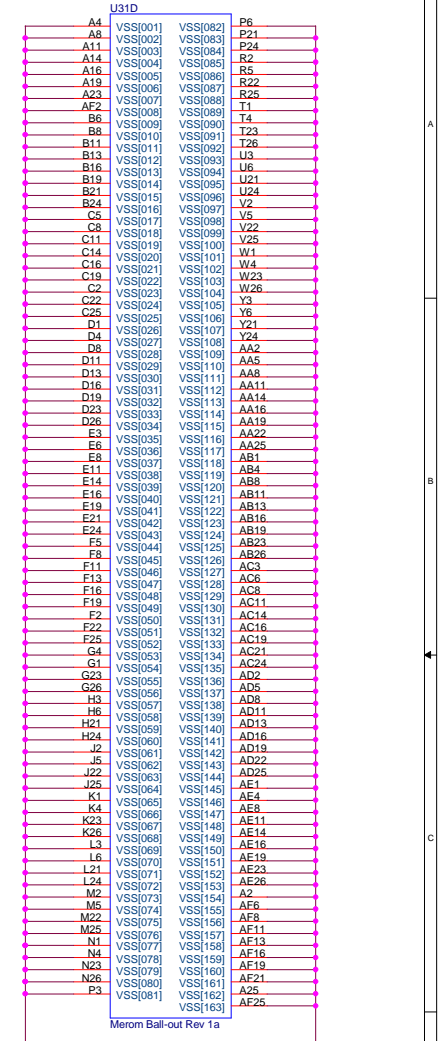
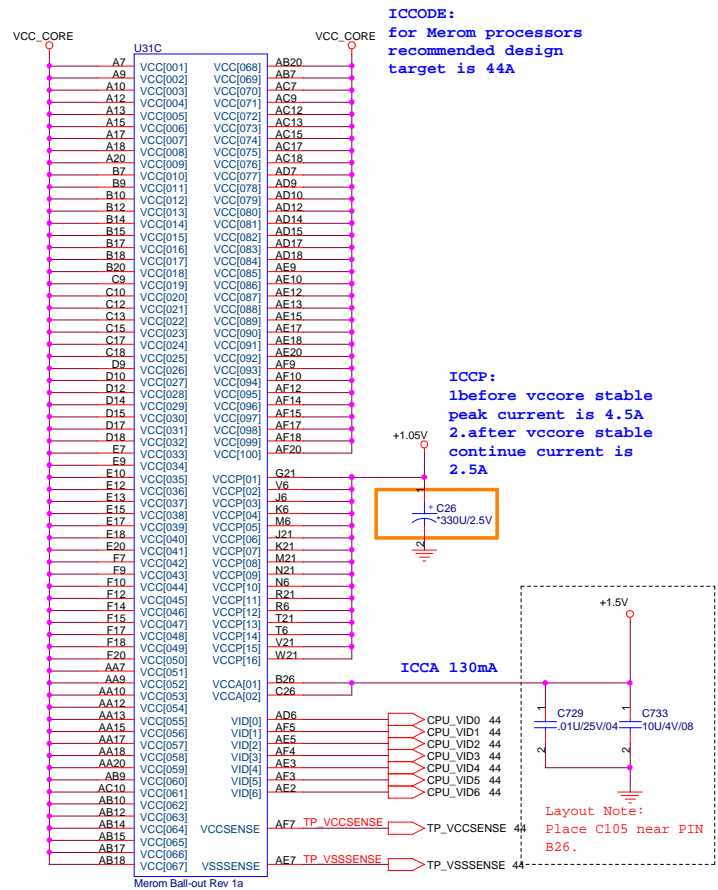
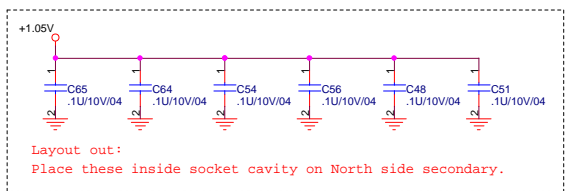
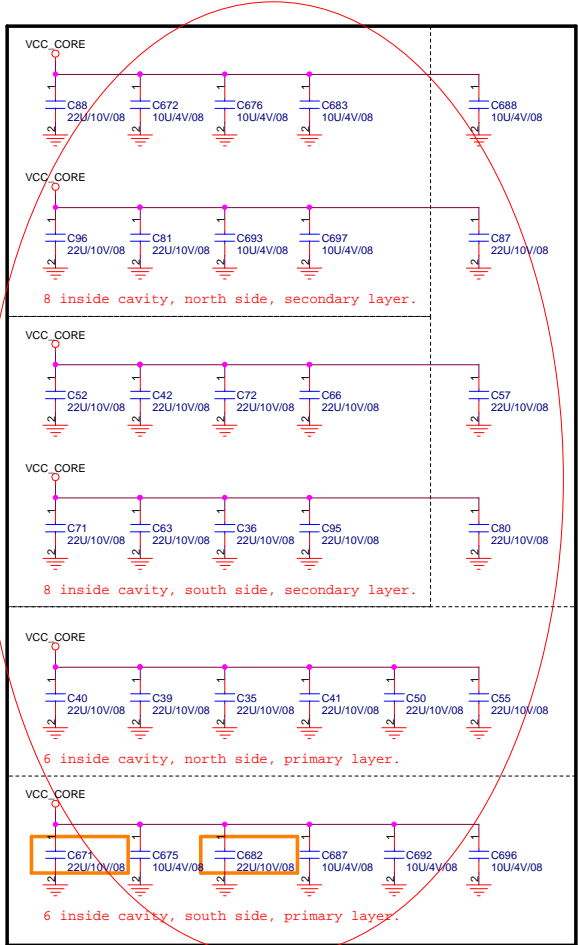
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

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**Quanta Computer Inc.**

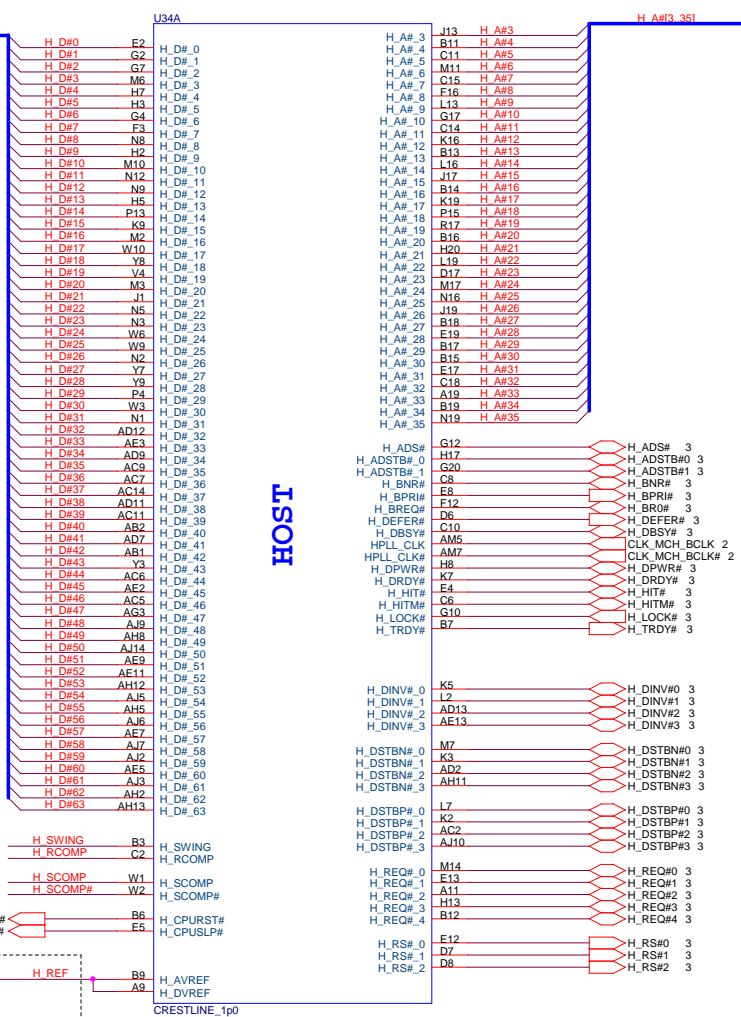
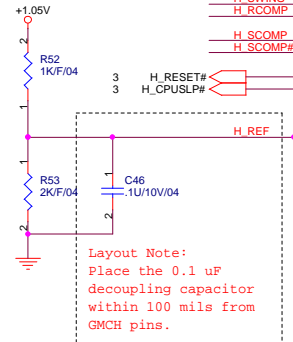
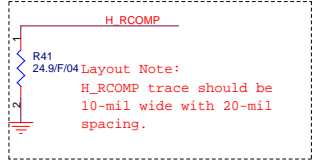
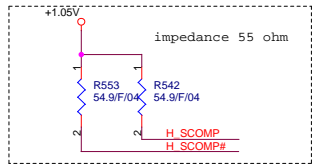
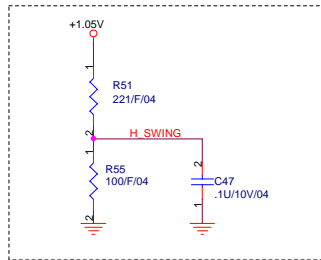
Size Custom Document Number  
**CLOCK GENERATOR** Rev 1A

Date: Monday, March 19, 2007 Sheet 3 of 48

Note: Populate R5, R8, C372 & R430 when ITP connector is populated.





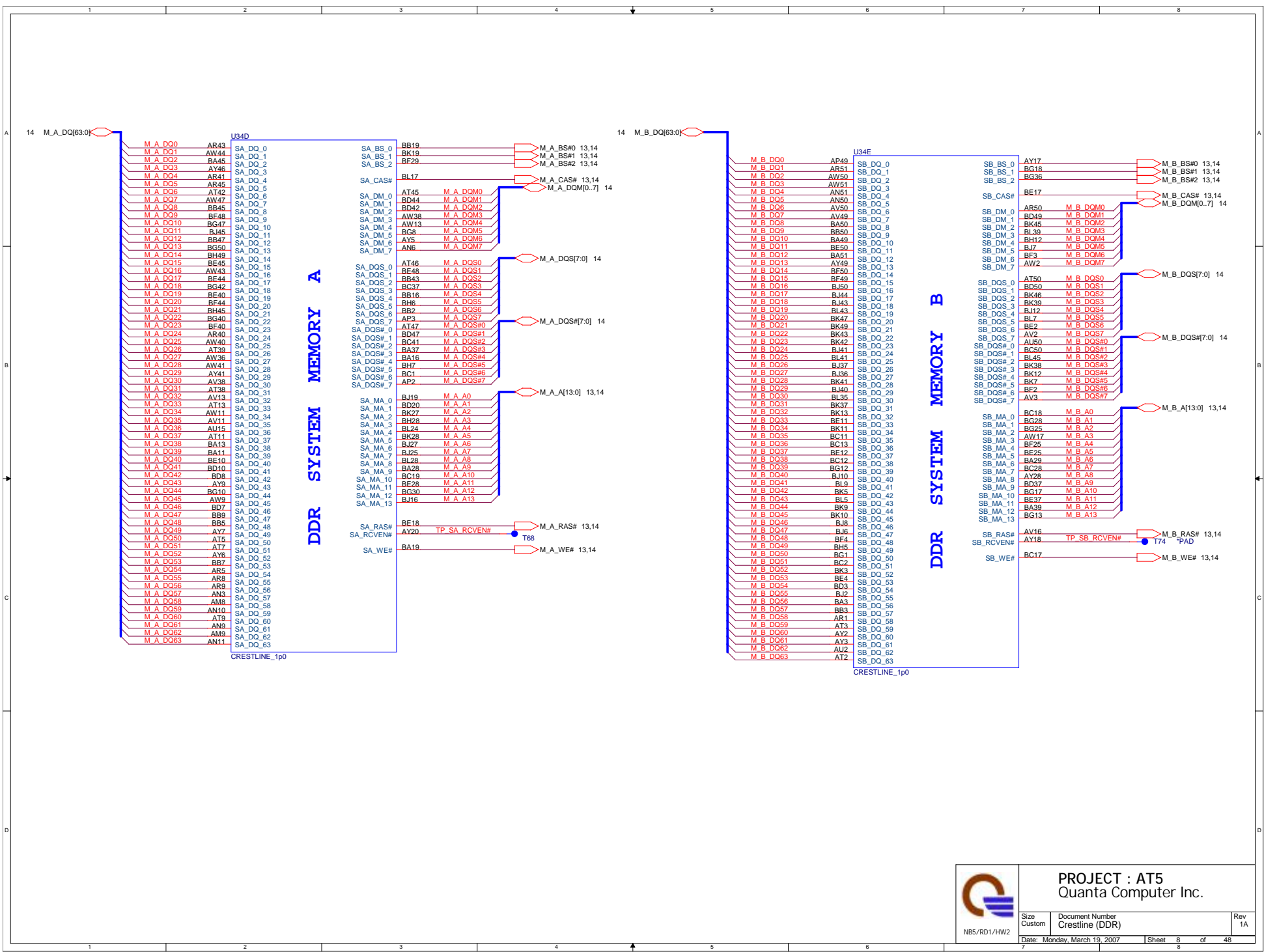


**PROJECT : AT5**  
Quanta Computer Inc.

Size Custom	Document Number Crestline (HOST)	Rev 1A
Date: Monday, March 19, 2007		
Sheet 6 of 48		







PROJECT : AT5  
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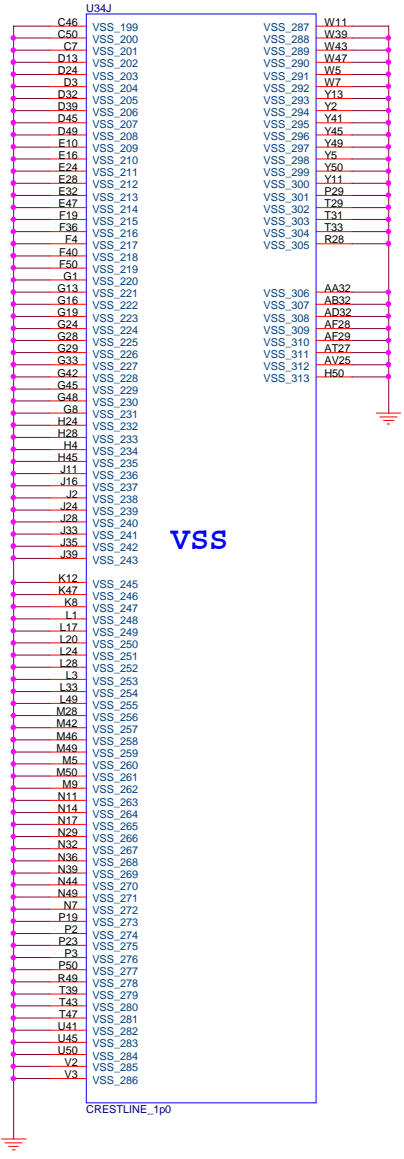
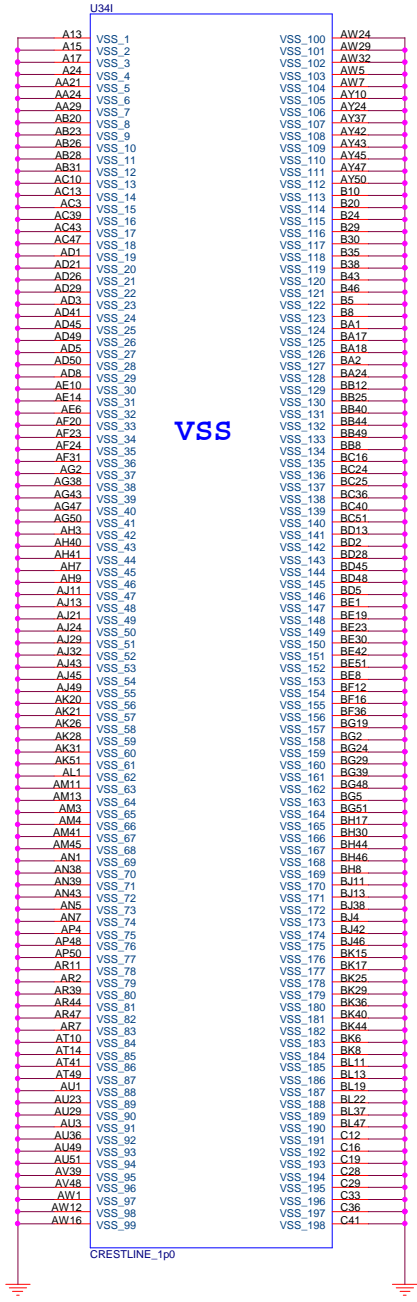
Size Custom	Document Number Crestline (DDR)	Rev 1A
Date: Monday, March 19, 2007		Sheet 8 of 48

NB5/RD1/HW2









PROJECT : AT5  
Quanta Computer Inc.

Size Custom	Document Number Crestline (VSS)	Rev 1A
Date: Monday, March 19, 2007		Sheet 11 of 48

5 4 3 2 1

5 4 3 2 1

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal  
 CFG[17:3] Have internal Pull-up  
 CFG[18:19] Have internal Pull-down  
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
-----------	---------------------------------------

DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--

XOR /ALLz /Clock Un-gating

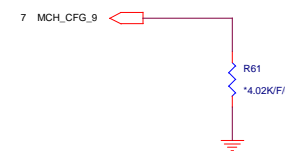
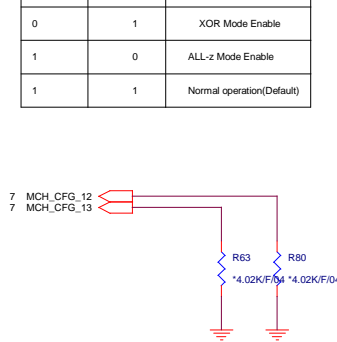
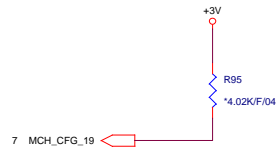
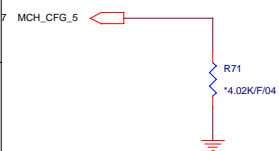
MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

SDVO Present

Strap define at External DVI control page

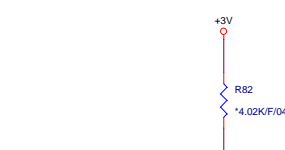


FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---

SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---

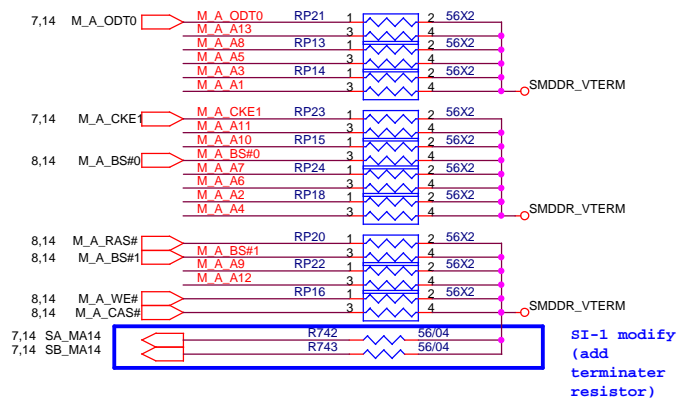
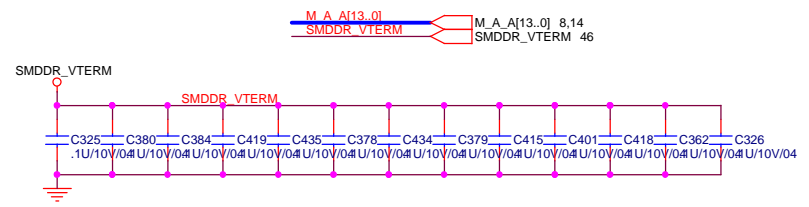


PROJECT : AT5  
Quanta Computer Inc.

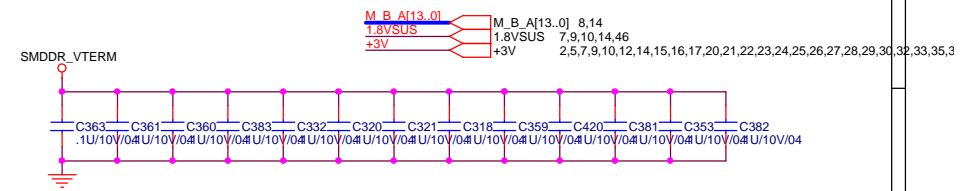
Size Custom	Document Number 10 - GMCH STRAP-3(6 of 6)	Rev 1A
Date: Monday, March 19, 2007		Sheet 12 of 48

# DDRII DUAL CHANNEL A,B.

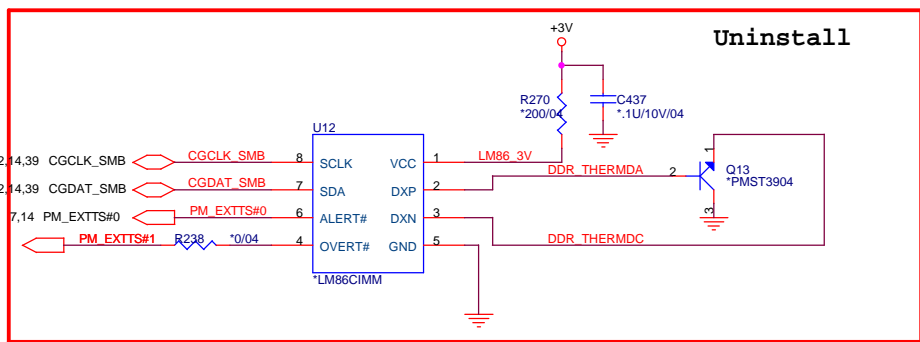
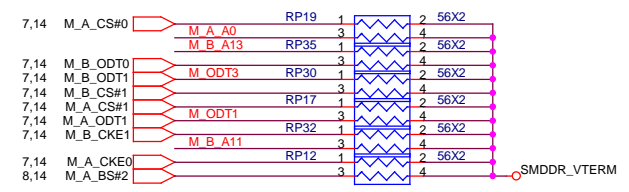
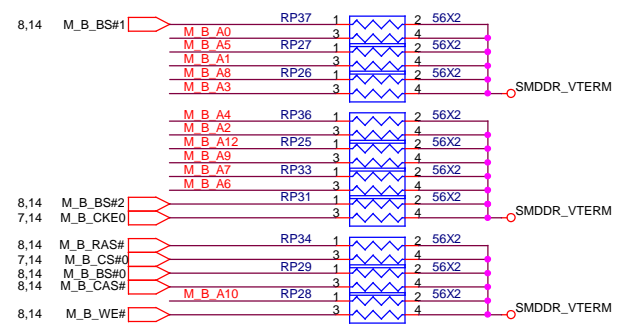
## DDRII A CHANNEL



## DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM



**PROJECT : AT5**  
Quanta Computer Inc.

Size B Document Number  
NBS/RD1/HW2 DDRII RES.ARRAY Rev 1A

Date: Monday, March 19, 2007 Sheet 13 of 48

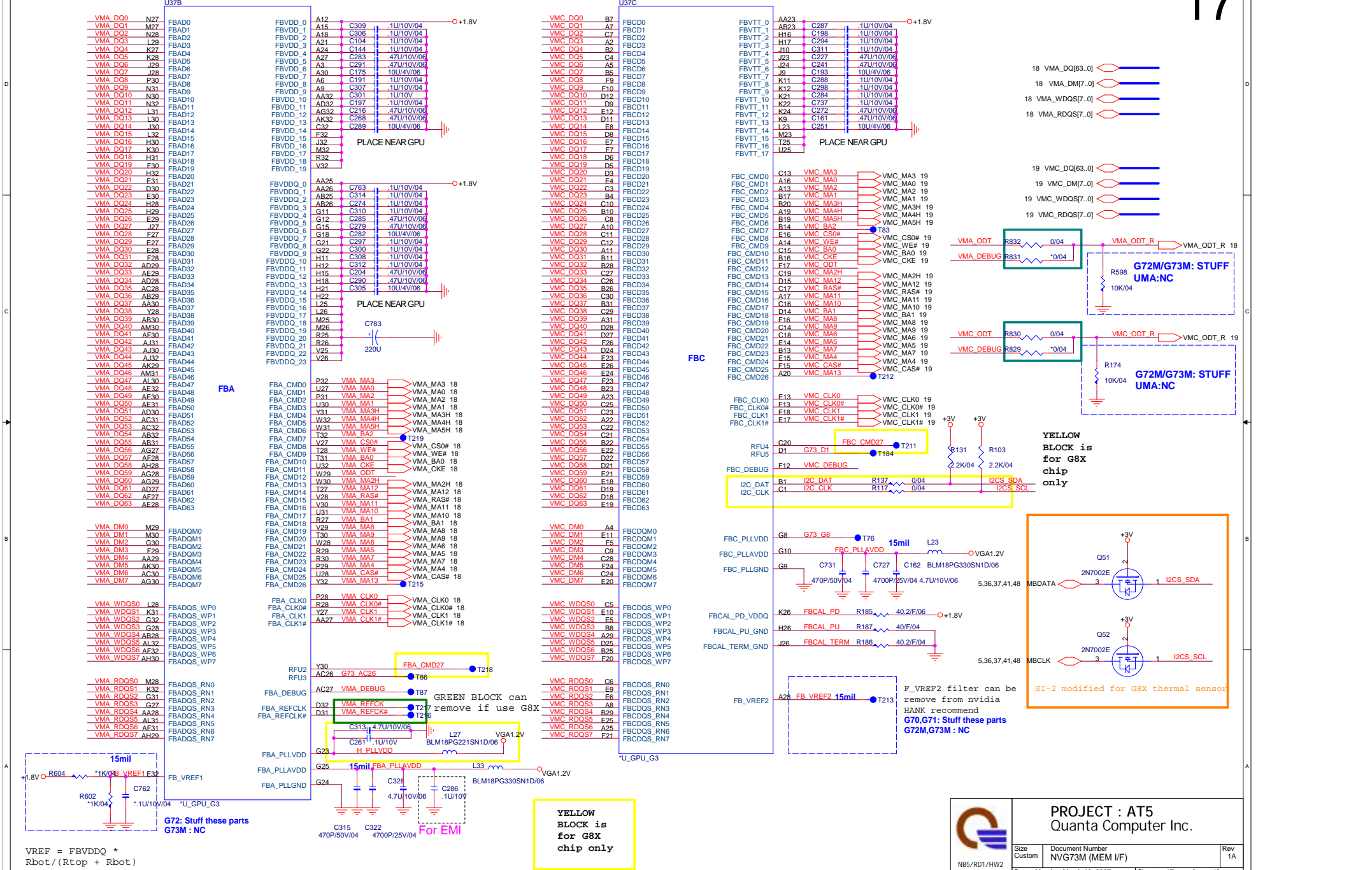








Channel C is available on G73M only





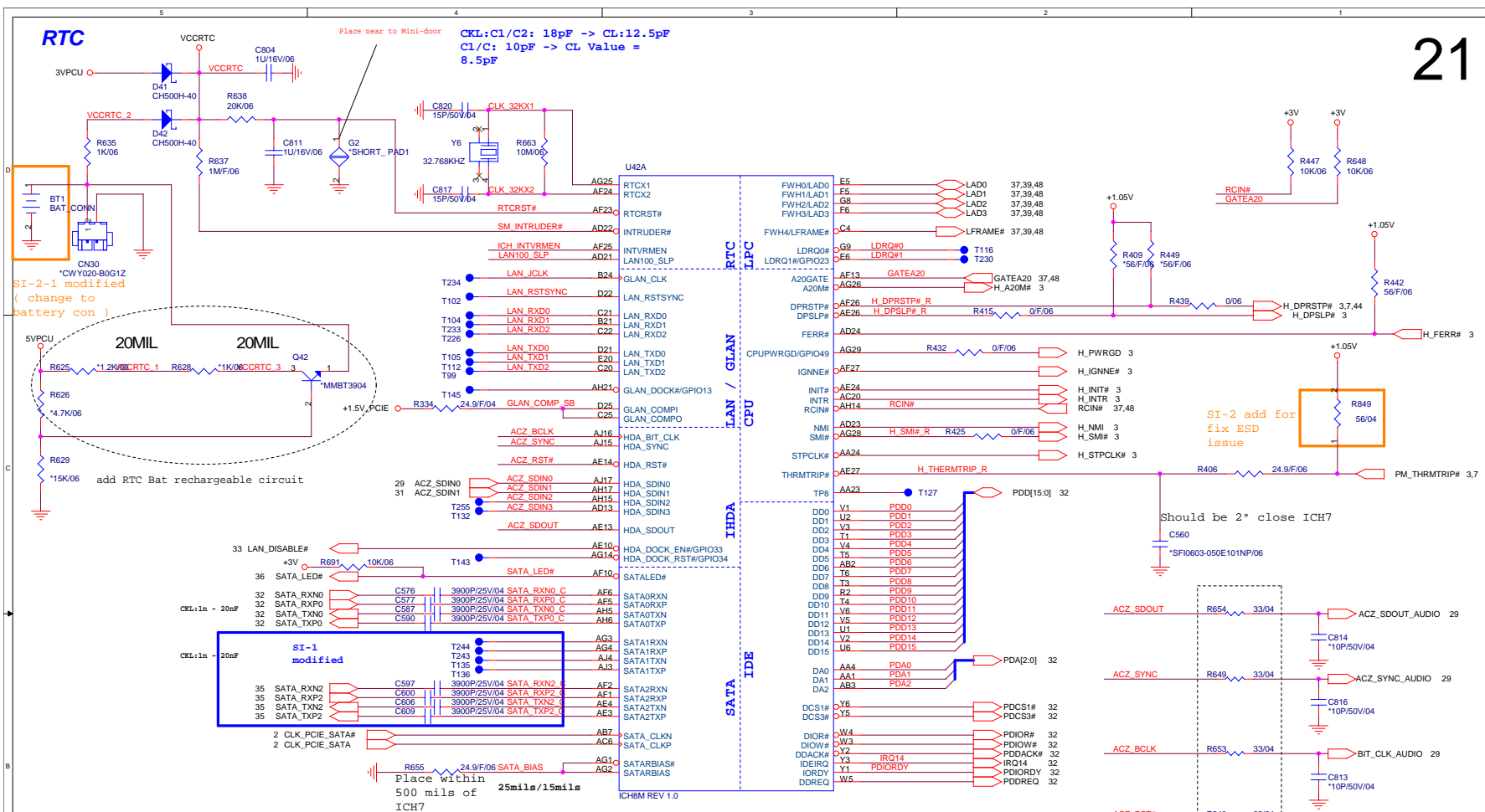








RTC



SB Strap

ICH8-M Internal VR Enable strap  
(Internal VR for Vccsus1\_05, VccSus1\_5 and VccCL1\_5)

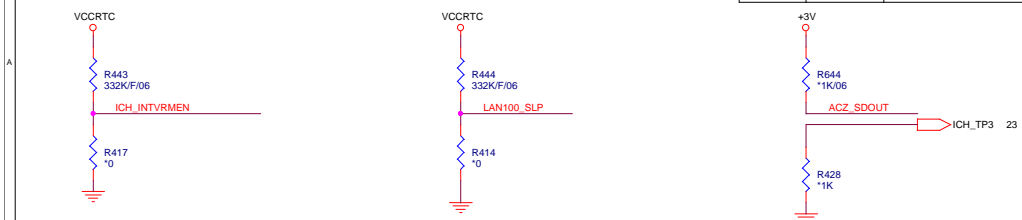
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
----------	---

ICH8-M LAN100\_SLP Strap  
(Internal VR for VccLAN1\_05 and VccCL1\_05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

XOR Chain Entrance Strap

ICH_RSVD0	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1



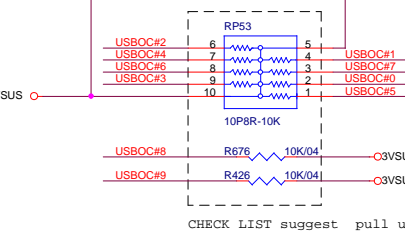
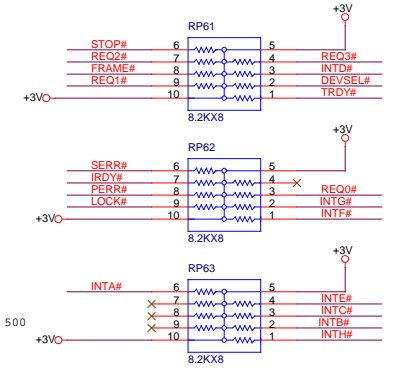
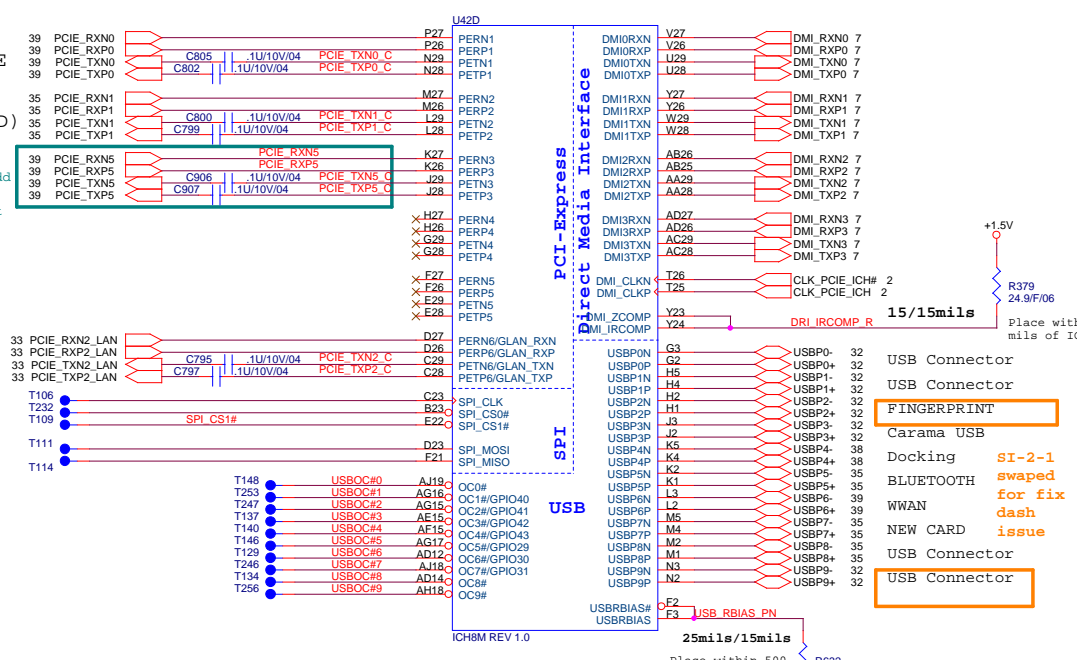
PROJECT : AT5  
Quanta Computer Inc.

Size Custom	Document Number ICH7-M HOST(1/4)	Rev 1A
Date: Monday, March 19, 2007		Sheet 21 of 48

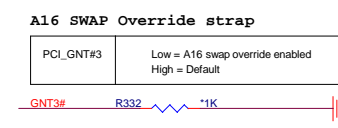
MINI CARD PCI-E  
EXPRESS CARD (NEW CARD)

SI-2 Add for support RBSON card

PCI-E-LAN

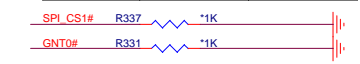


USB Connector  
USB Connector  
FINGERPRINT  
Carama USB  
Docking  
BLUETOOTH  
WWAN  
NEW CARD  
USB Connector  
USB Connector



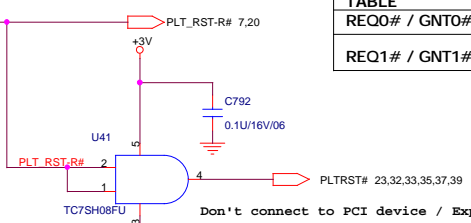
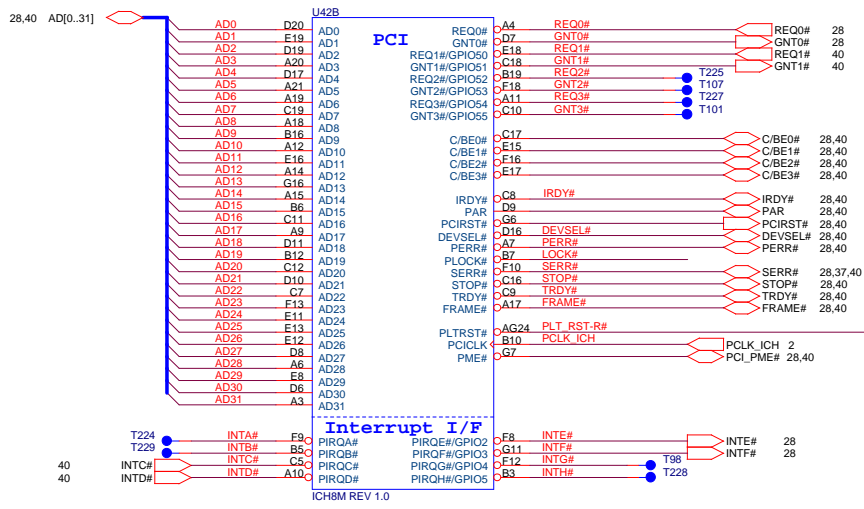
IC8H Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

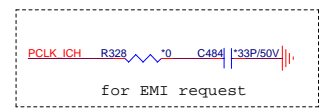


PCI ROUTING TABLE

REQ0# / GNT0#	IDSEL	INTERUPT	DEVICE
AD25	INTC# ,INTD#	RICOH832	
REQ1# / GNT1#	AD22	INTC# ,INTD#	MINI PCI for debug

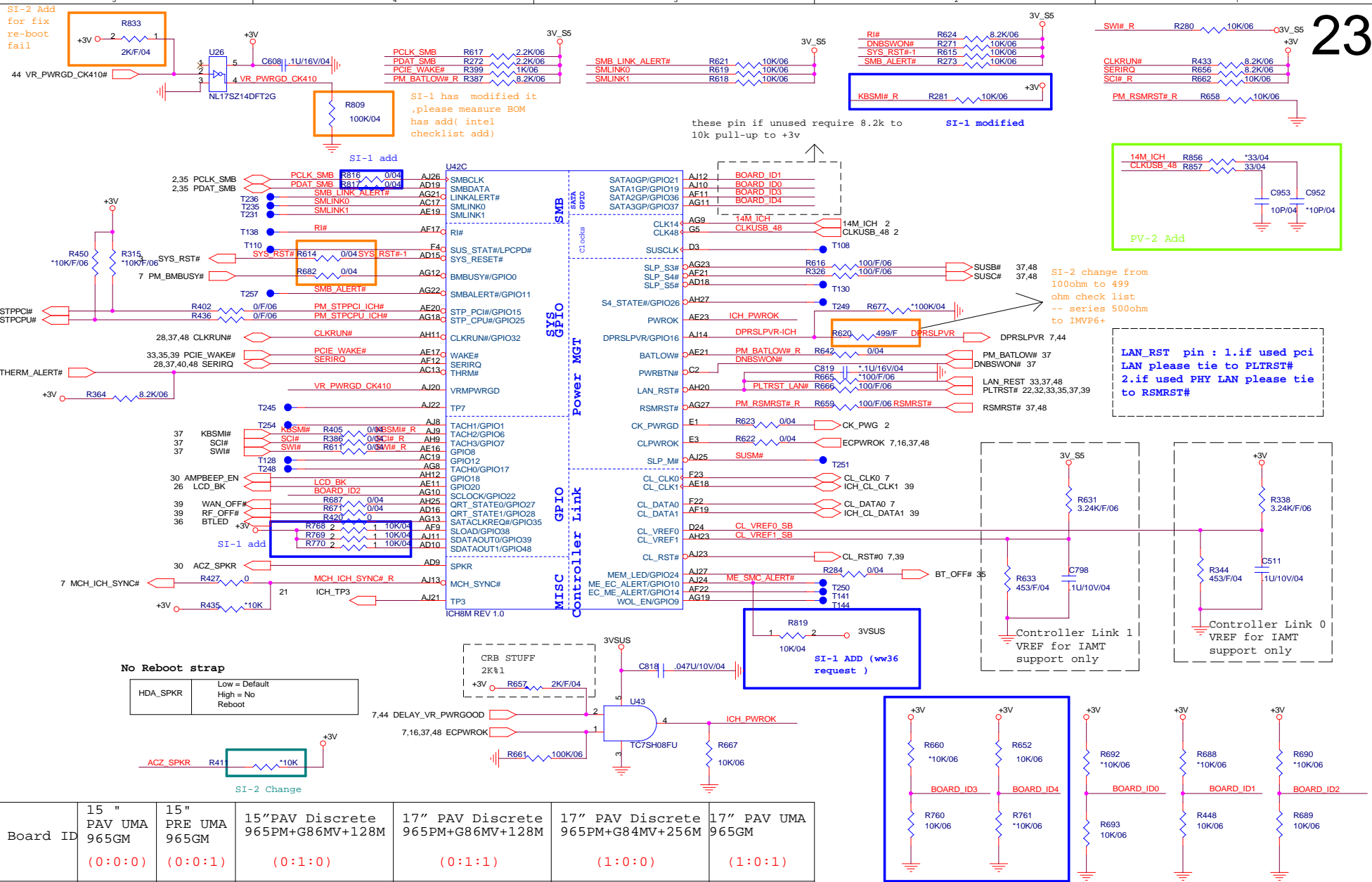


Don't connect to PCI device / Express card



**PROJECT : AT5**  
Quanta Computer Inc.

Size Custom	Document Number ICH7-M M PCI E(2/4)	Rev 1A
Date: Monday, March 19, 2007 Sheet 22 of 48		



**No Reboot strap**

HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

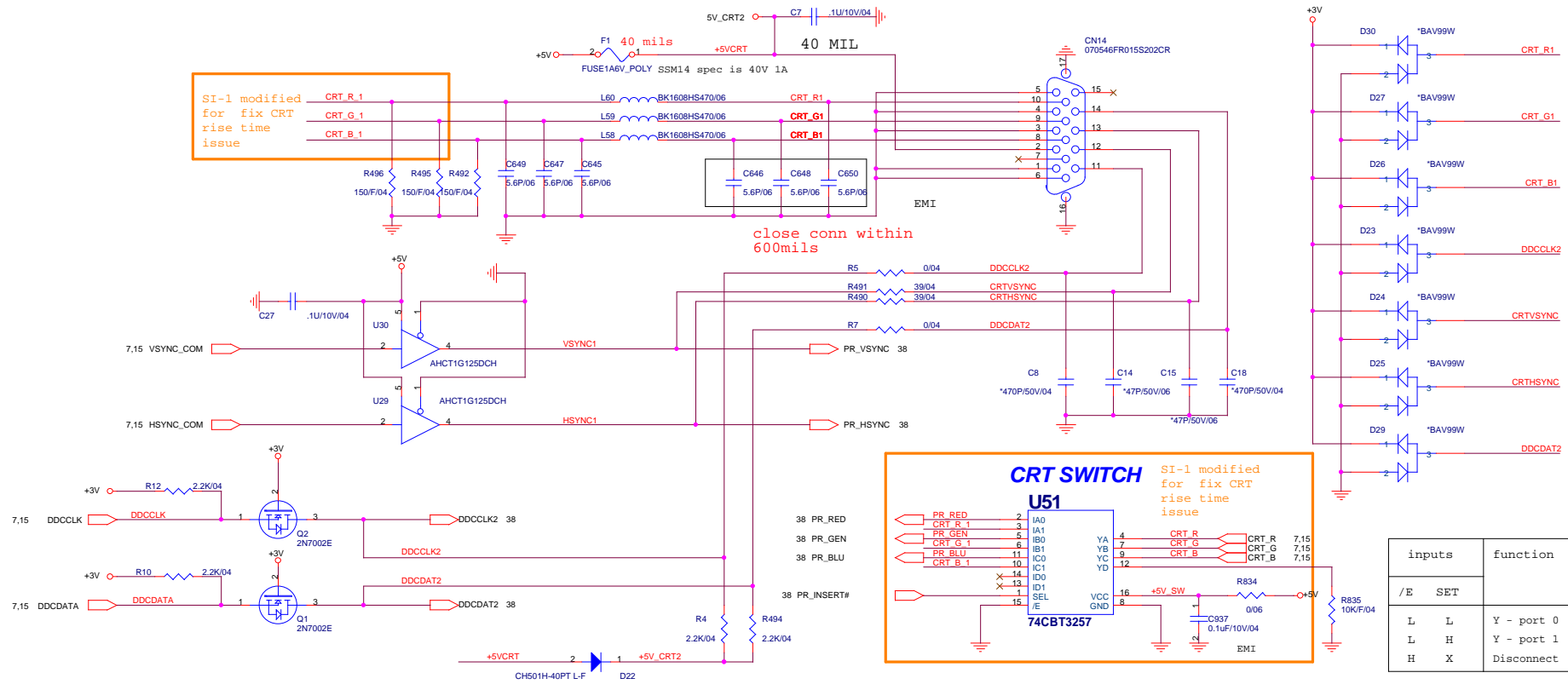
Board ID	15" PAV UMA 965GM	15" PRE UMA 965GM	15" PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G86MV+128M	17" PAV Discrete 965PM+G84MV+256M	17" PAV UMA 965GM
	(0:0:0)	(0:0:1)	(0:1:0)	(0:1:1)	(1:0:0)	(1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff



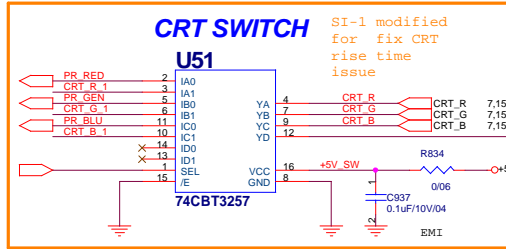
**PROJECT : AT5**  
Quanta Computer Inc.



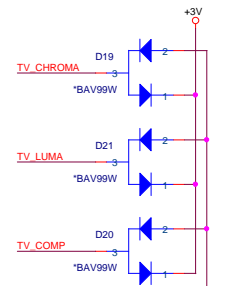
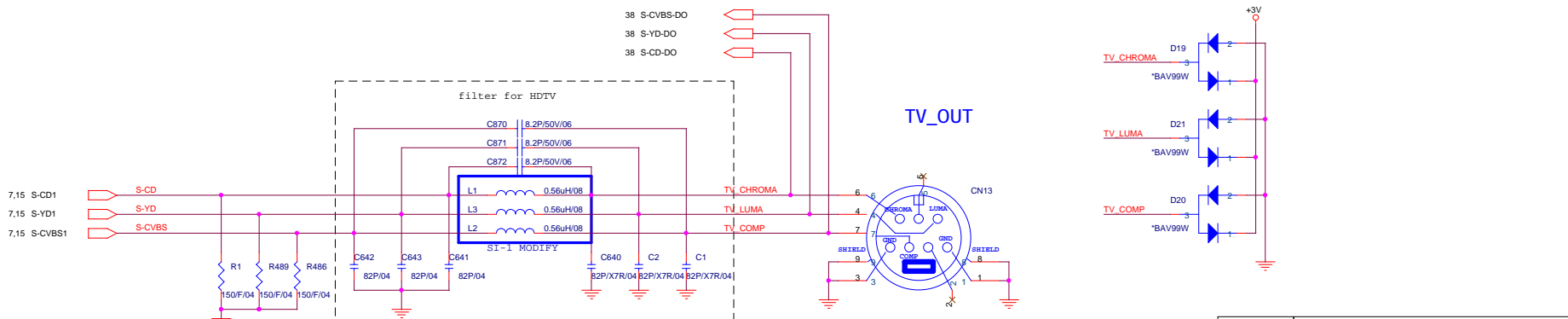
# CRT PORT



SI-1 modified for fix CRT rise time issue

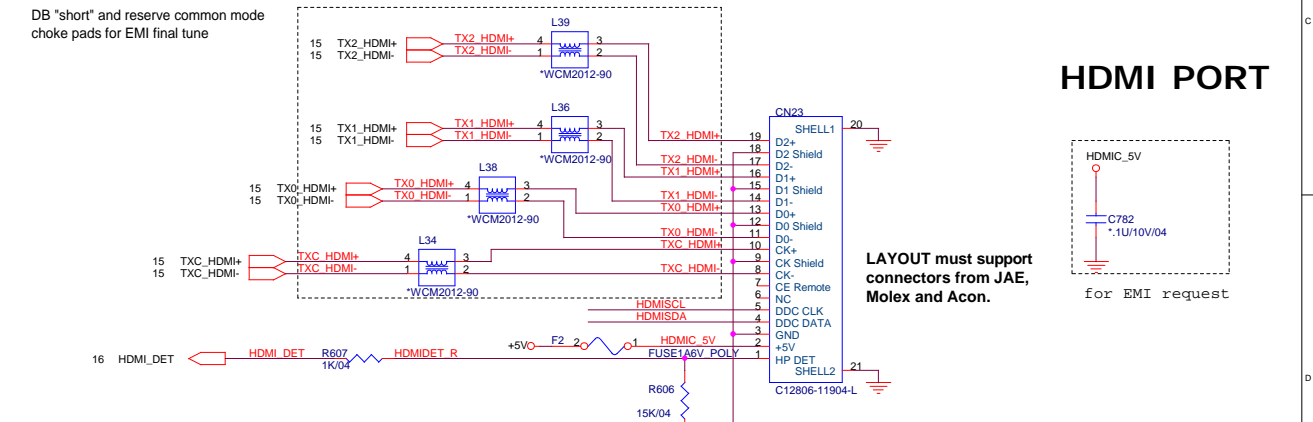
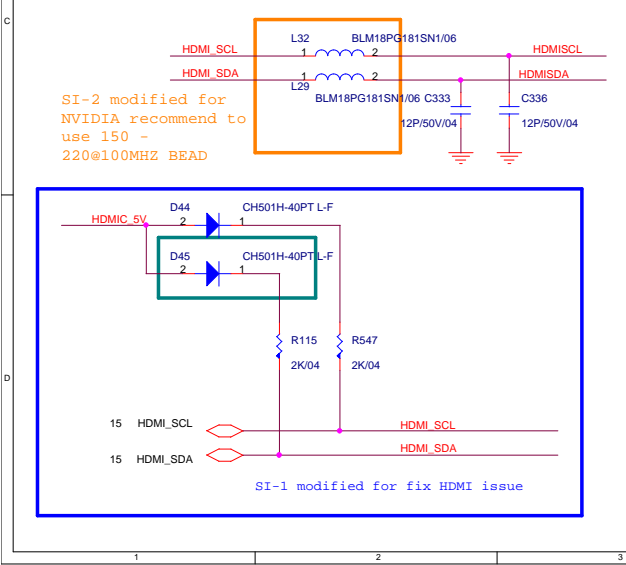
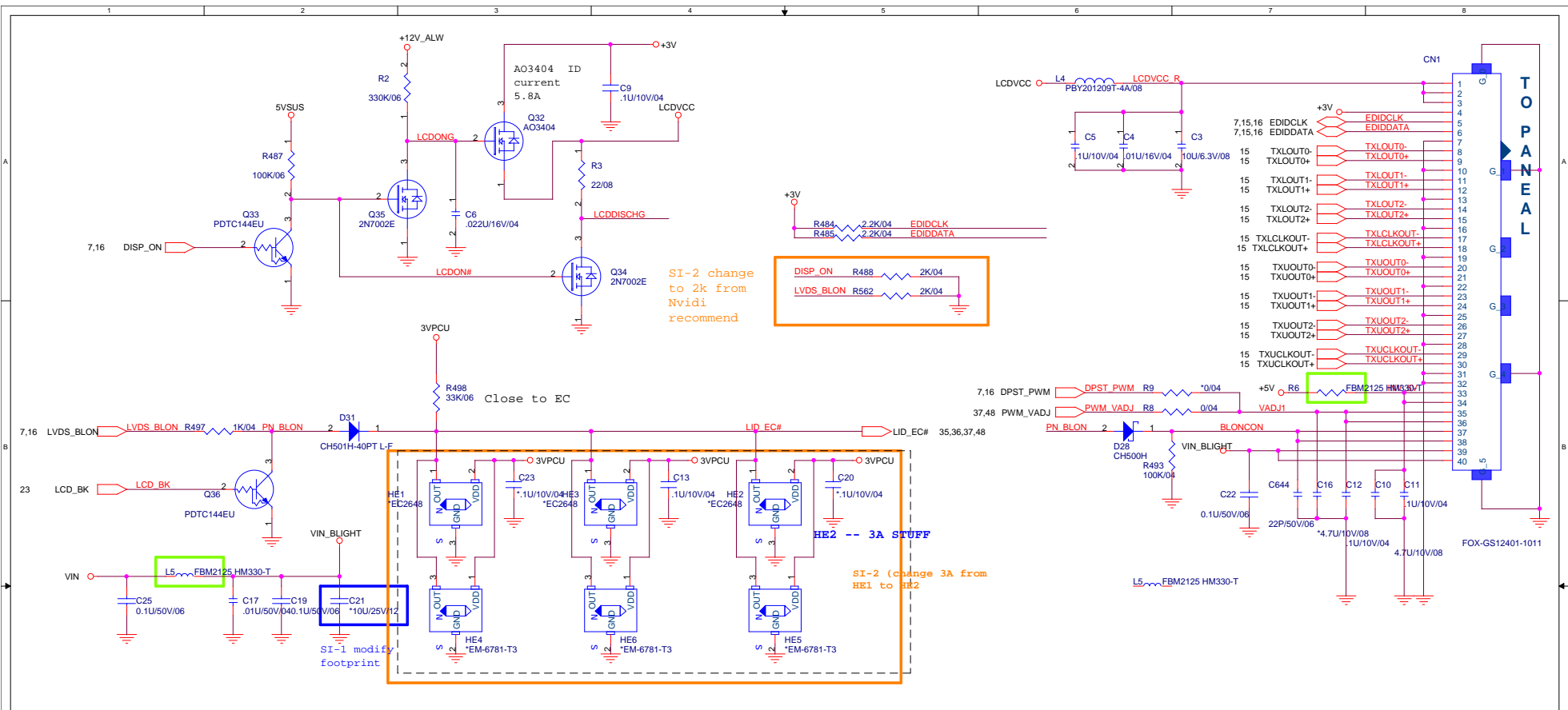


inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



**PROJECT : AT5**  
Quanta Computer Inc.

Size Custom	Document Number CRT/TV_OUT	Rev 1A
Date: Monday, March 19, 2007		Sheet 25 of 48



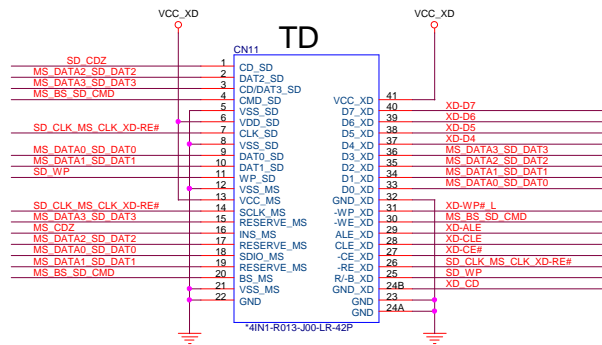
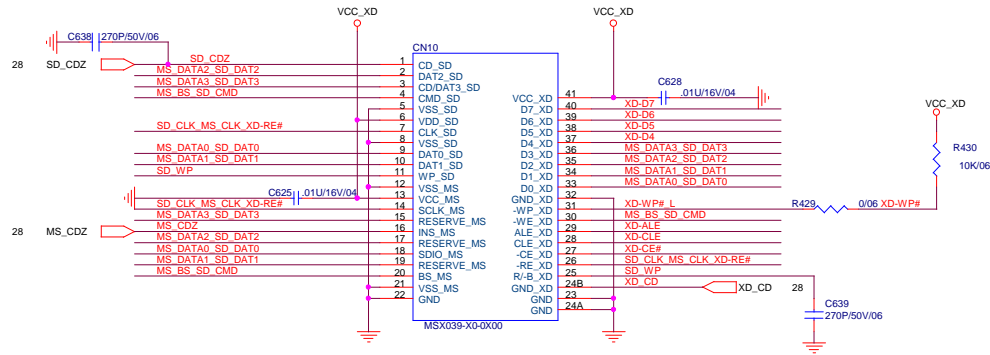
**PROJECT : AT5**  
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/HDMI CONN	Rev 1A
Date: Monday, March 19, 2007		Sheet 26 of 48

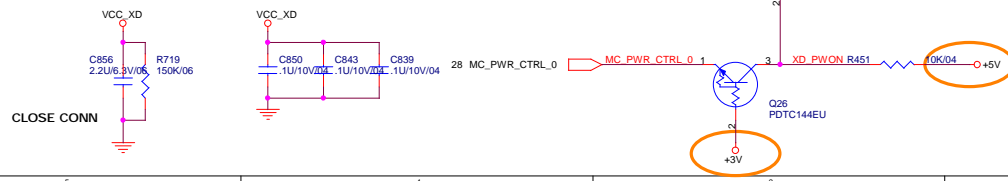
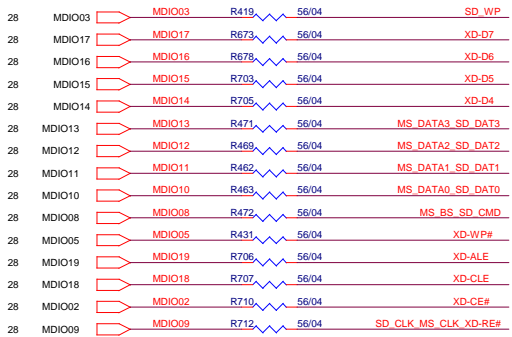
NBS/RD1/HW2



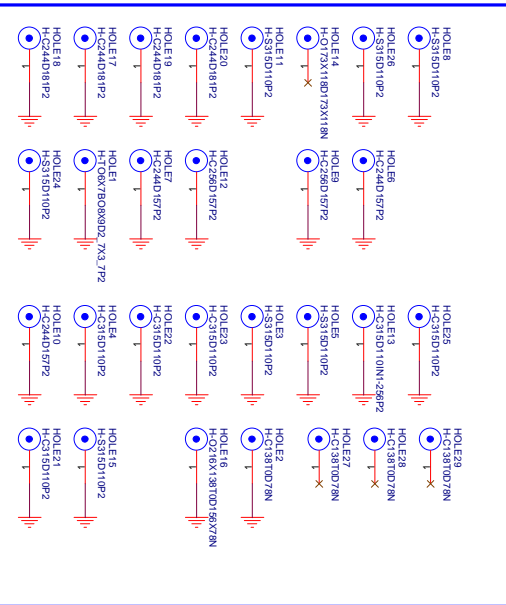
5 IN1 CARD READER  
XD, MMC / SD, MS / MSP



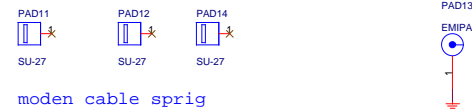
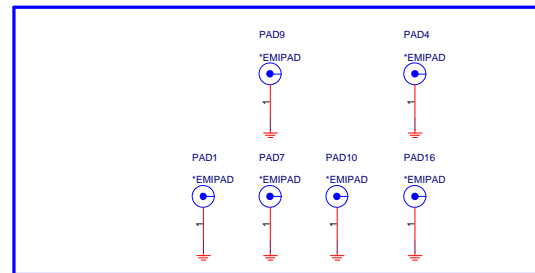
bom create 2'nd source



SCREW HOLE

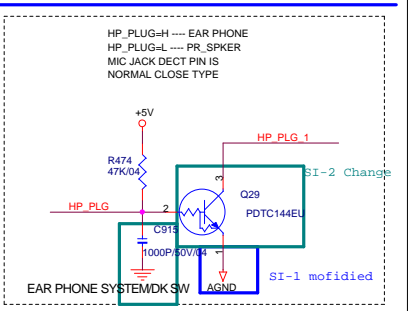
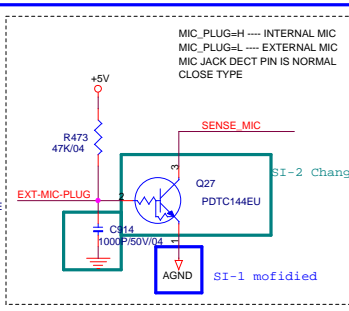
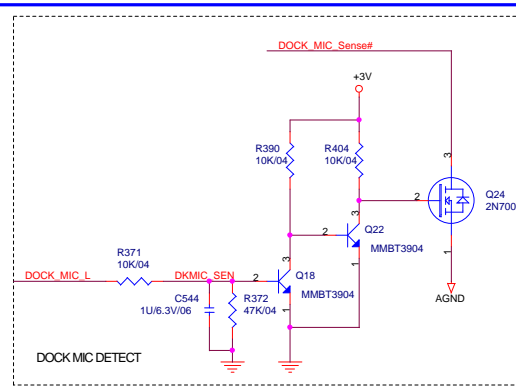
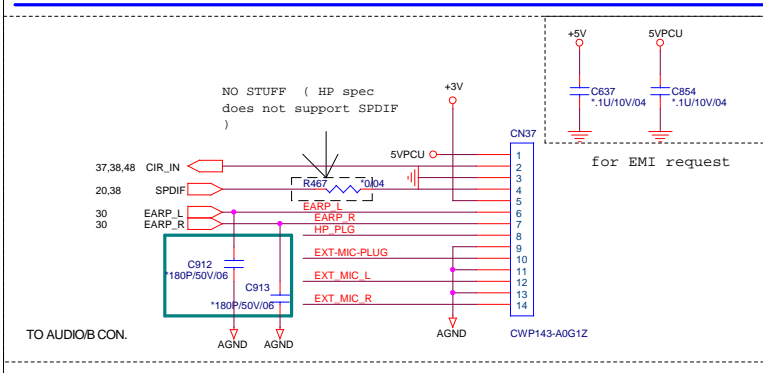
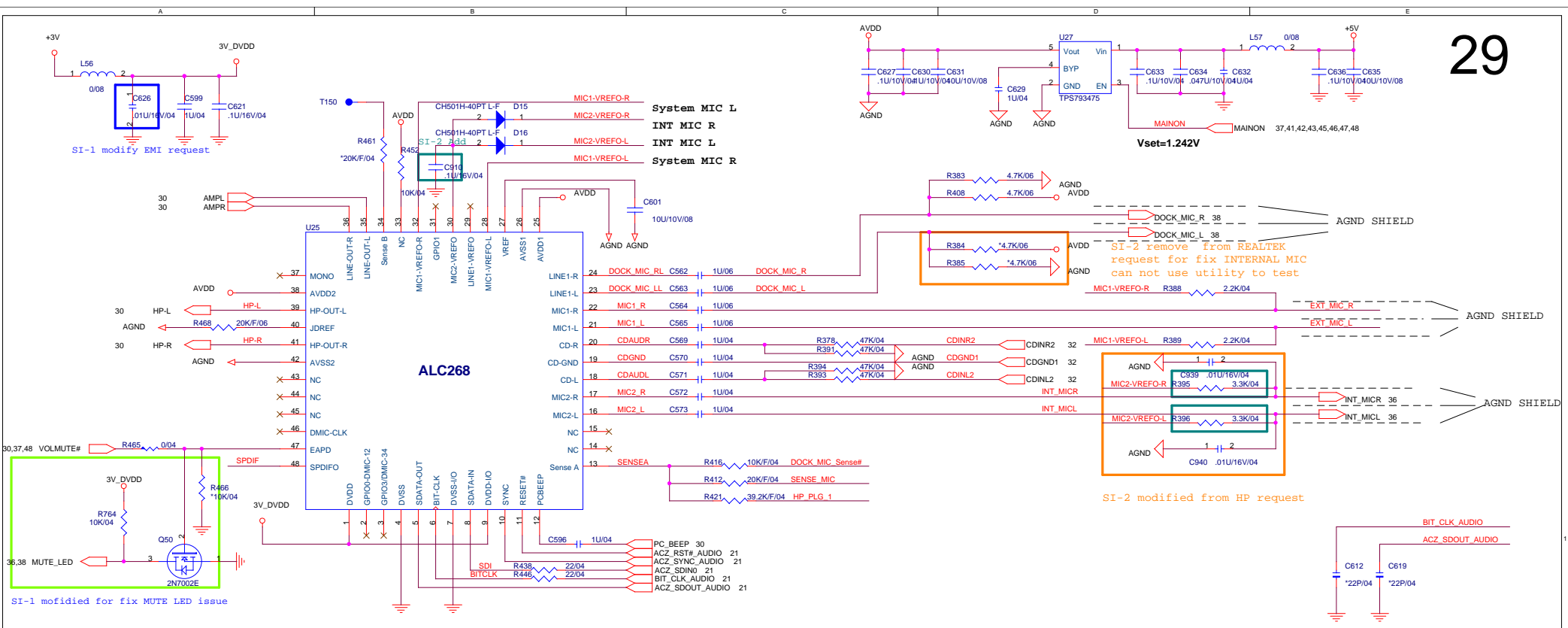


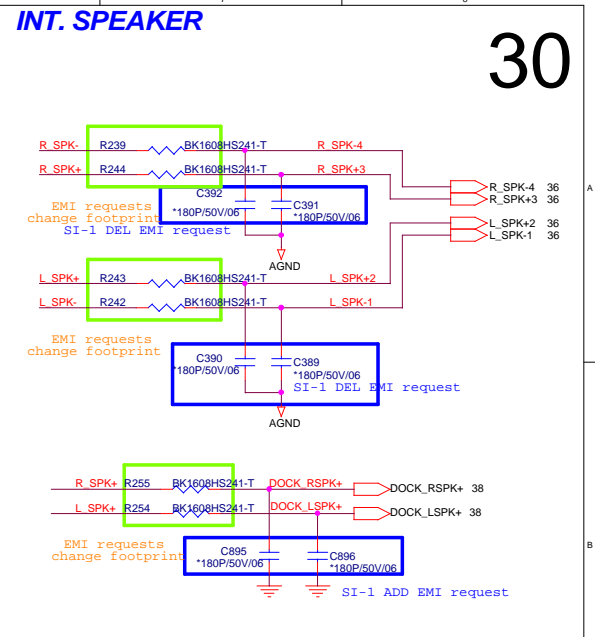
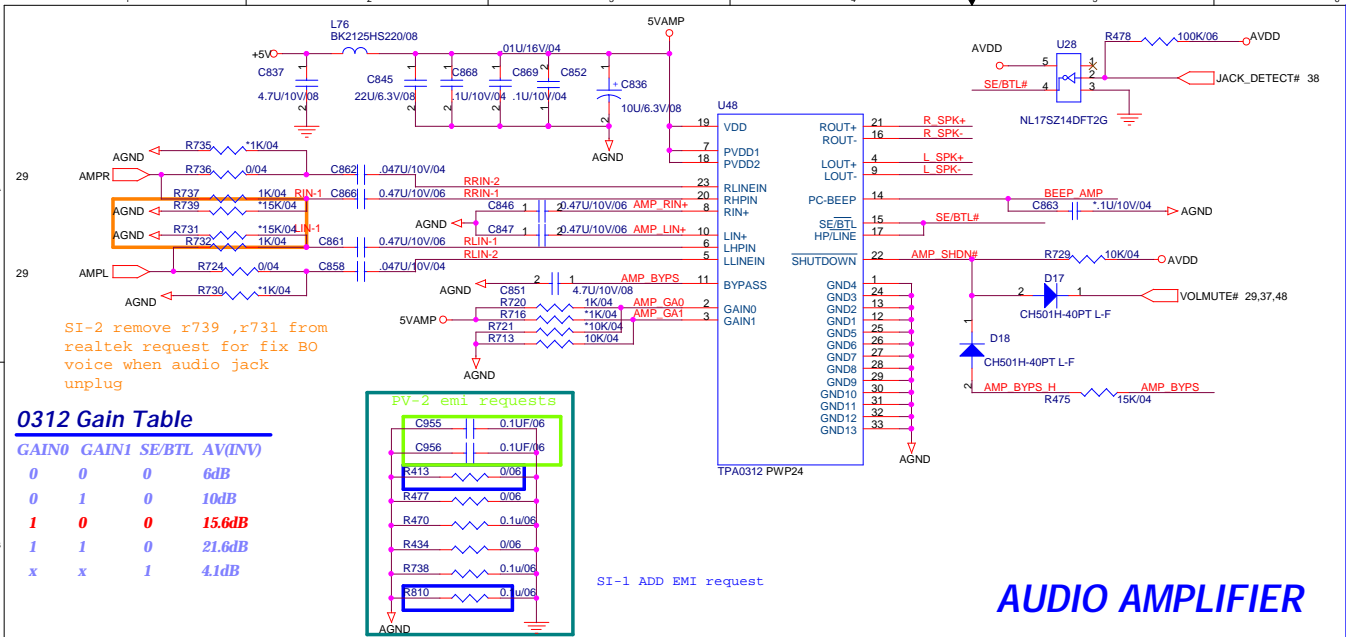
EMI PAD



	PROJECT : AT5 Quanta Computer Inc.		
	Size Custom	Document Number CARD READER/HOLE	Rev 1A
	Date: Monday, March 19, 2007	Sheet 27 of 48	

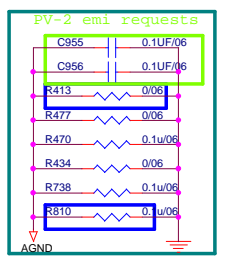






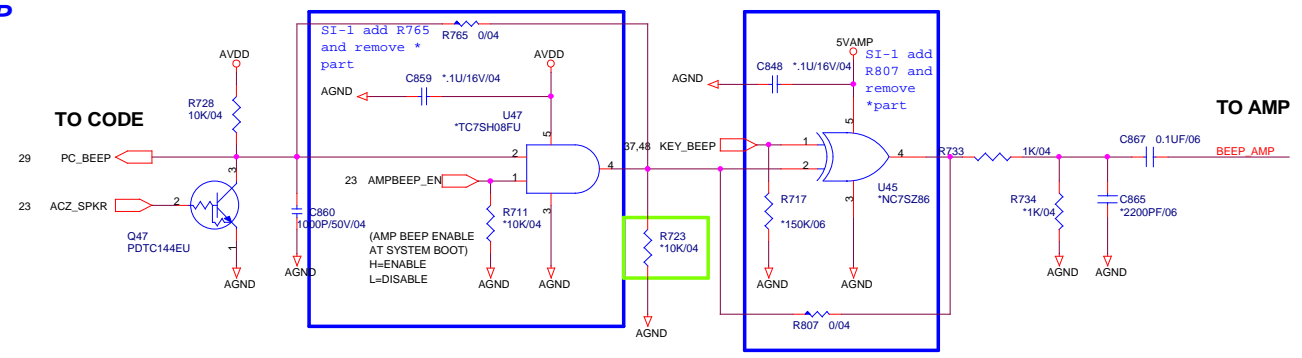
### 0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

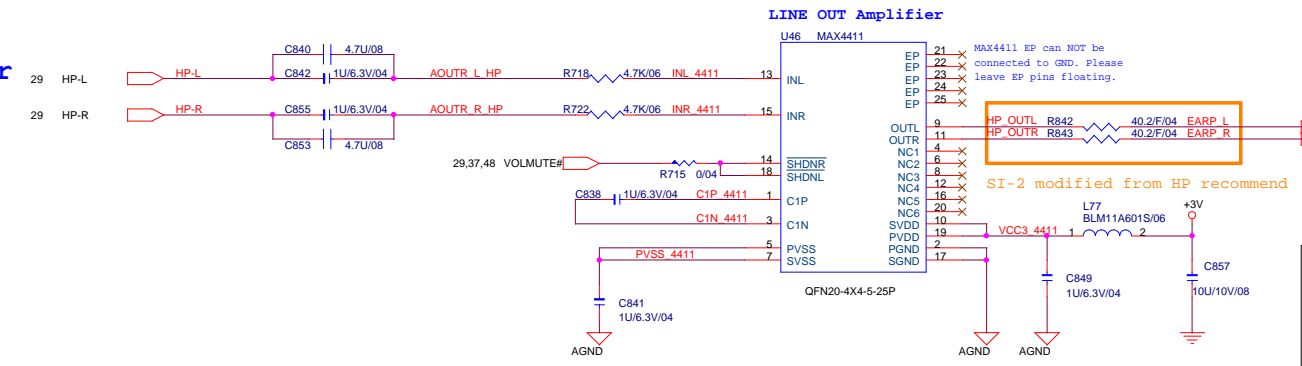


## AUDIO AMPLIFIER

## PCSPK BEEP



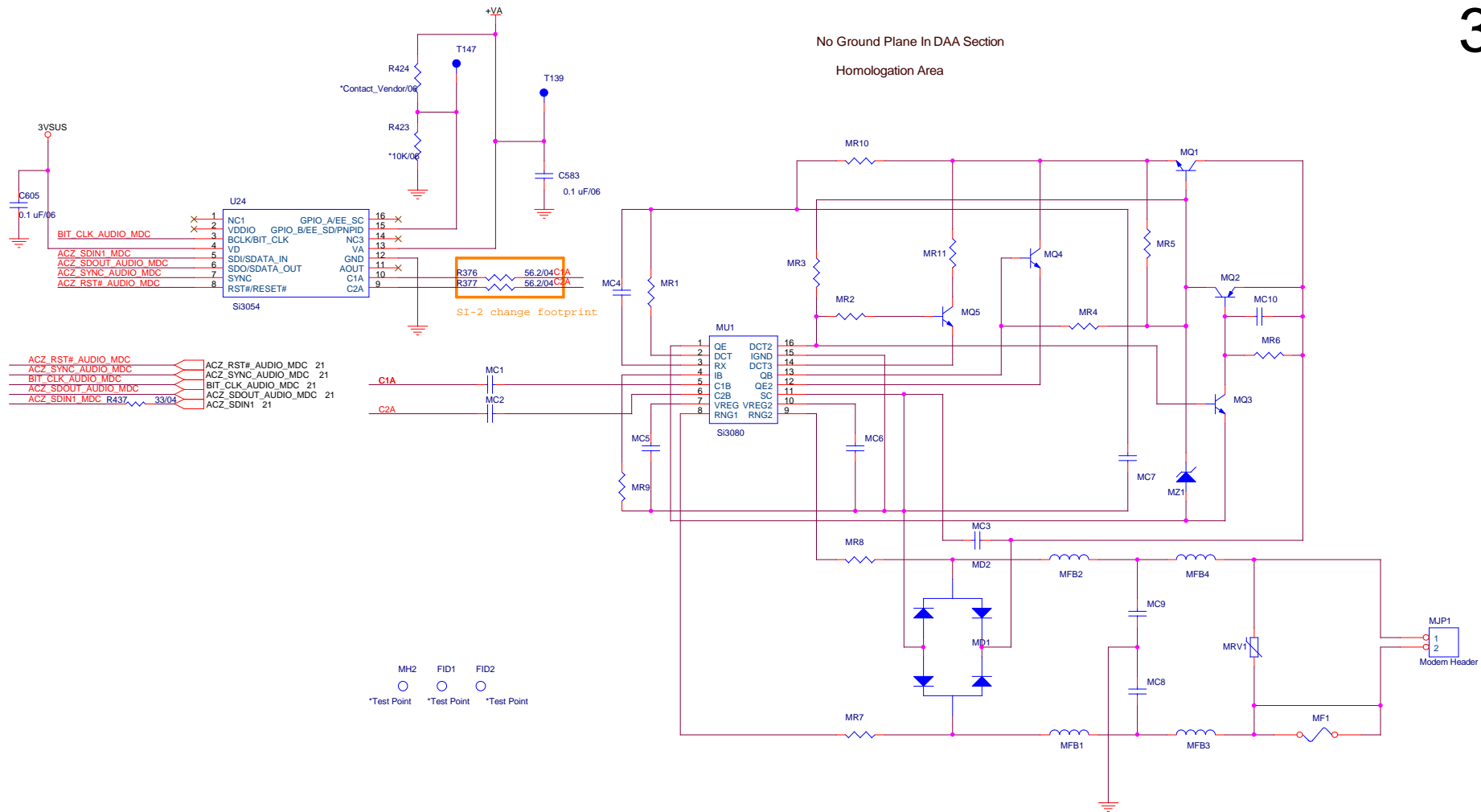
## LINE OUT Amplifier



**PROJECT : AT5**  
Quanta Computer Inc.


Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
Date: Monday, March 19, 2007		Sheet 30 of 48

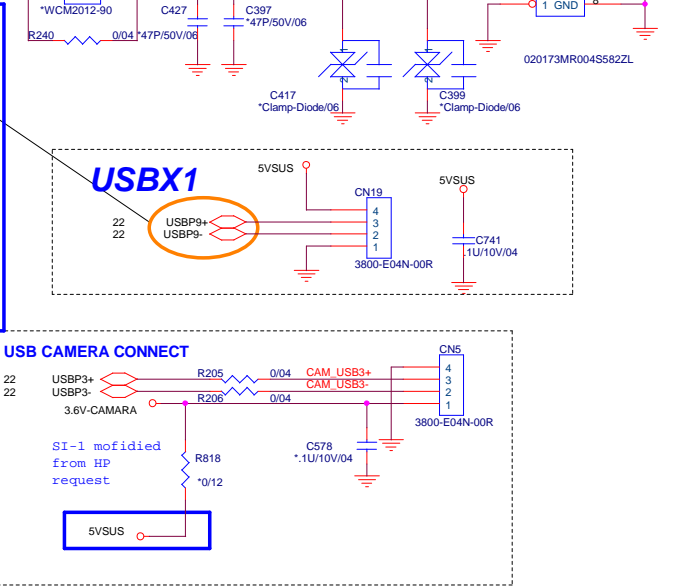
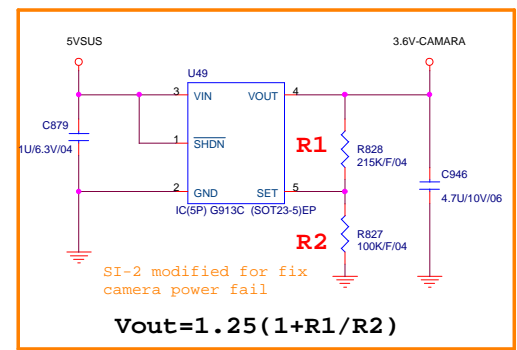
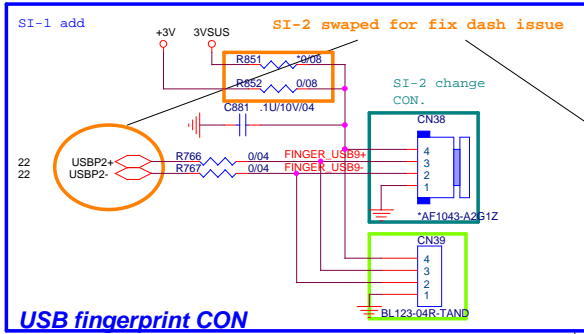
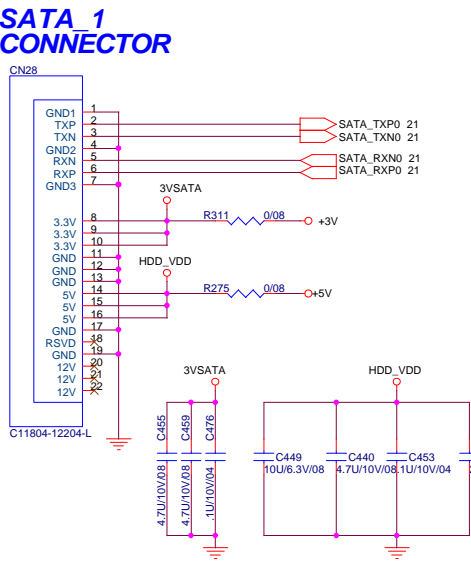
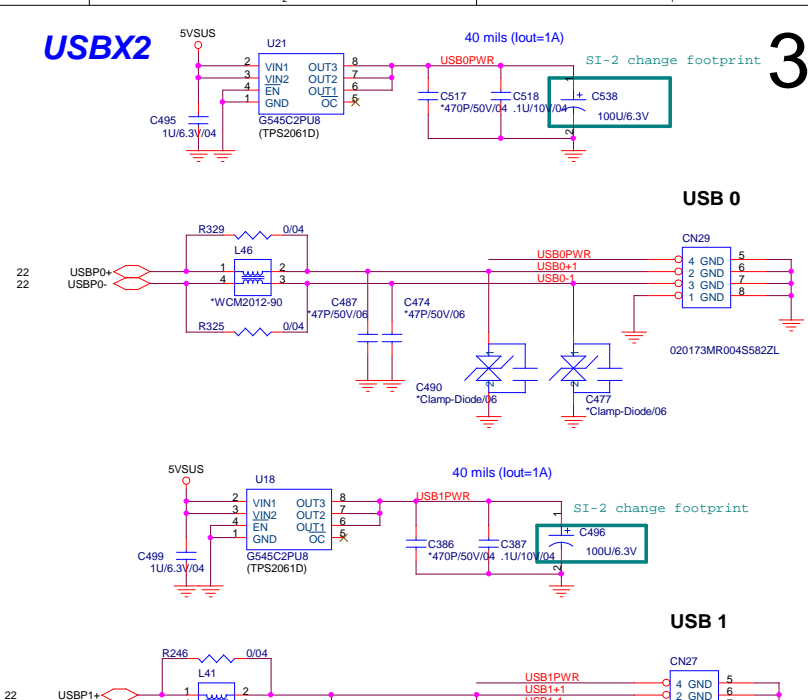
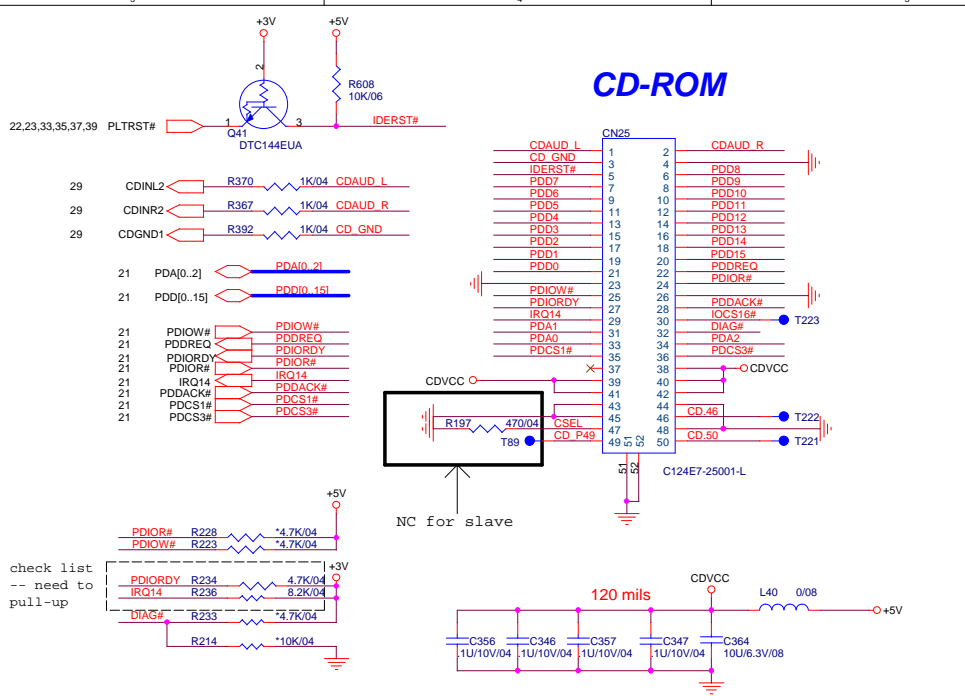
No Ground Plane In DAA Section  
Homologation Area



DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

		PROJECT : AT5 Quanta Computer Inc.	
		Size Custom	Document Number MODEM(DAA)
NB5/RD1/HW2		Date: Monday, March 19, 2007	Sheet 31 of 48



PROJECT : AT5  
Quanta Computer Inc.

Size Custom	Document Number SATA HDD/CD-ROM/USBX3	Rev 1A
Date: Monday, March 19, 2007		Sheet 32 of 48

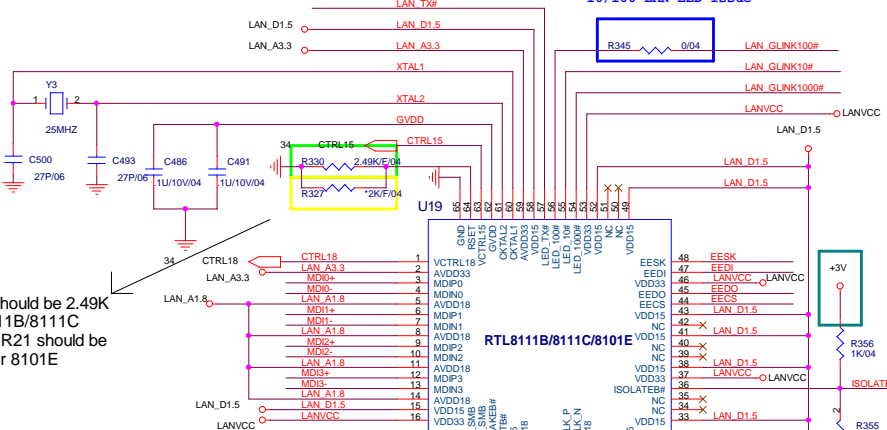


T : Stuffed for RTL8111B(10/100/1000)

giga LAN part number AJ081110006

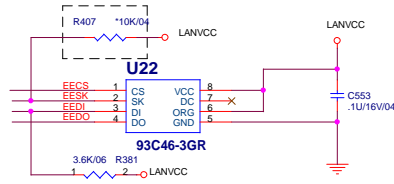
E : Stuffed for 8101E(10/100)

SI-1 BOM add to fix 10/100 LAN LED issue



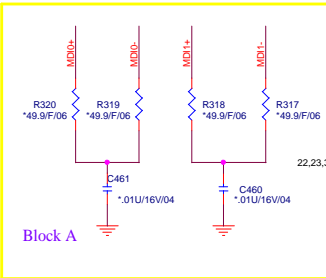
R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

for 93C56 used. NC if 93C46 is used.

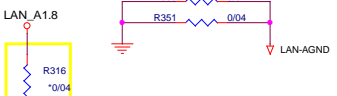


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs ( excluding PCIE\_WAKE# pin )

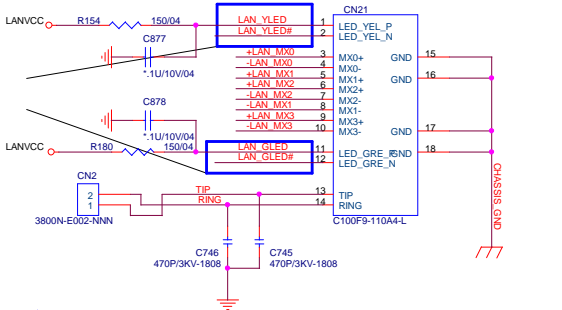
BLOCK A is only for RTL8101E application.



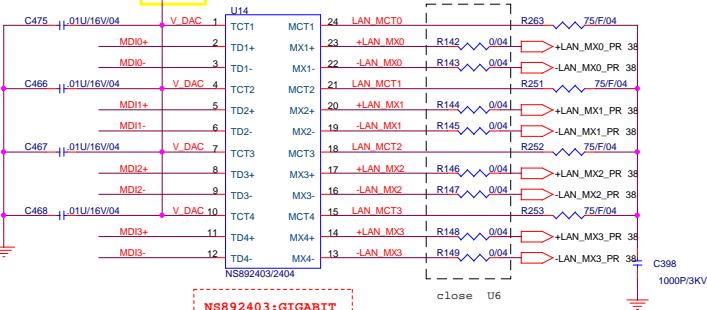
Remove R70 for 8111B and 8111C



RJ45



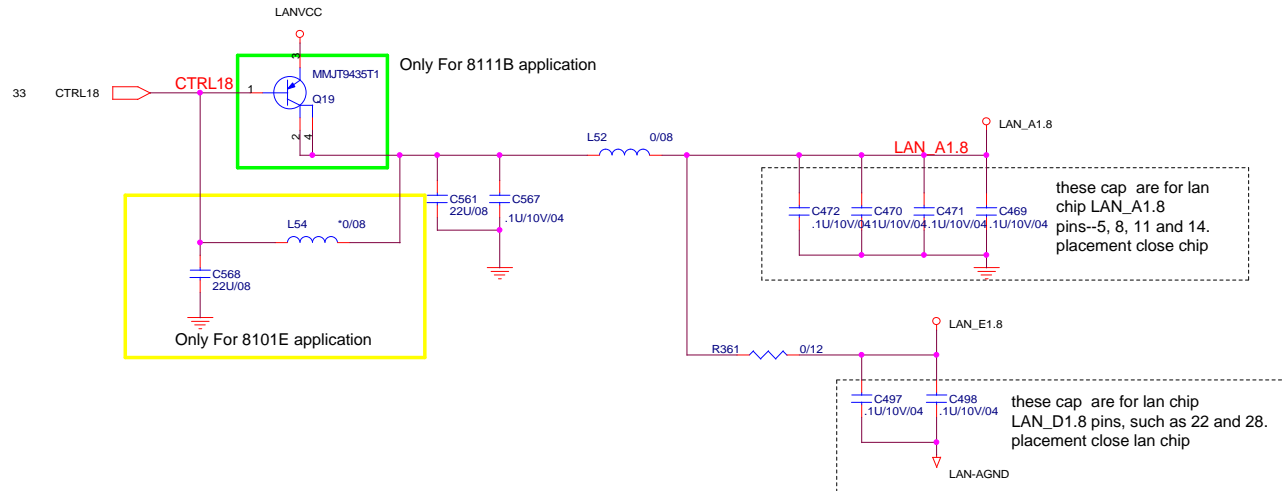
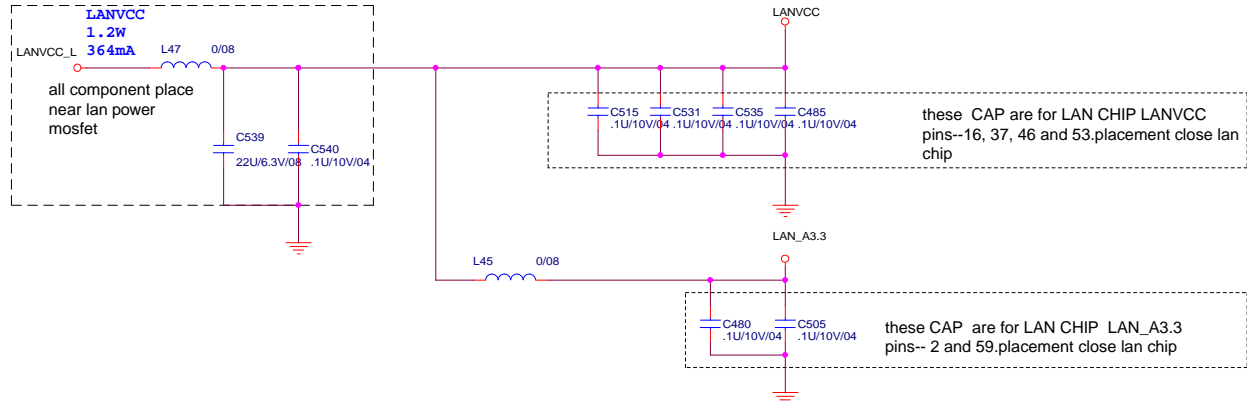
SI-1 modified to fix giga LAN LED issue



NS892403:GIGABIT NS892405:10/100

T : Stuffed for RTL8111B(10/100/1000)

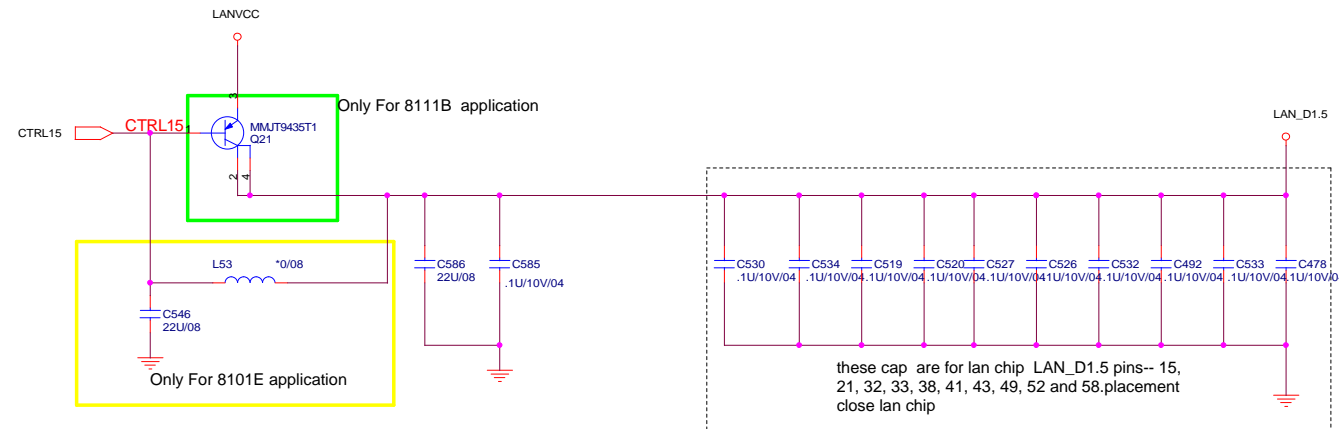
E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B/ RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

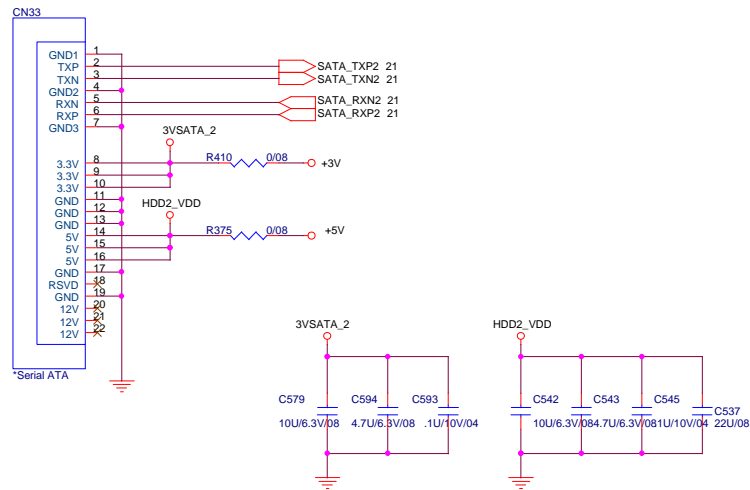
	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A



PROJECT : AT5  
Quanta Computer Inc.

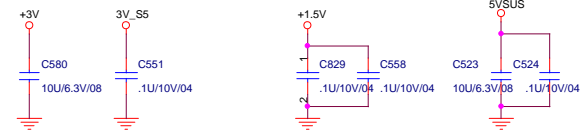
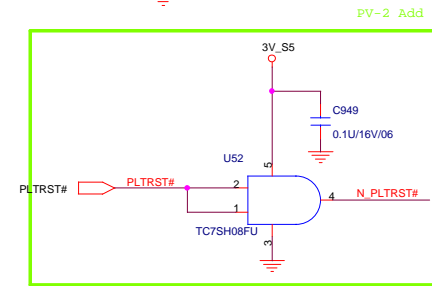
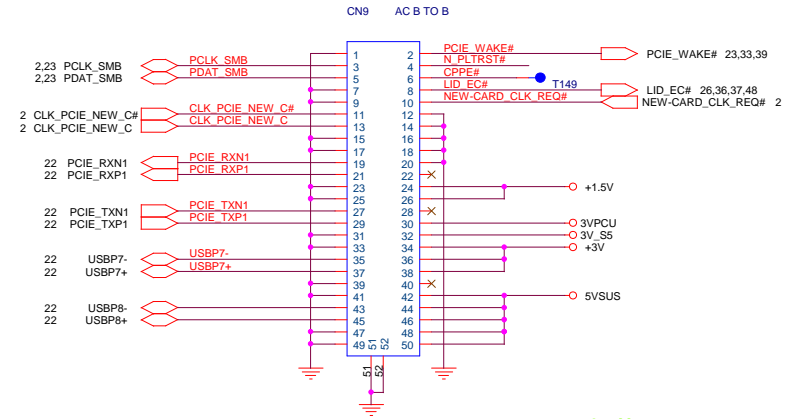
Size A3	Document Number LAN POWER	Rev 1A
Date: Monday, March 19, 2007		Sheet 34 of 48

# SATA\_2 CONNECTOR For 17"W Second HDD

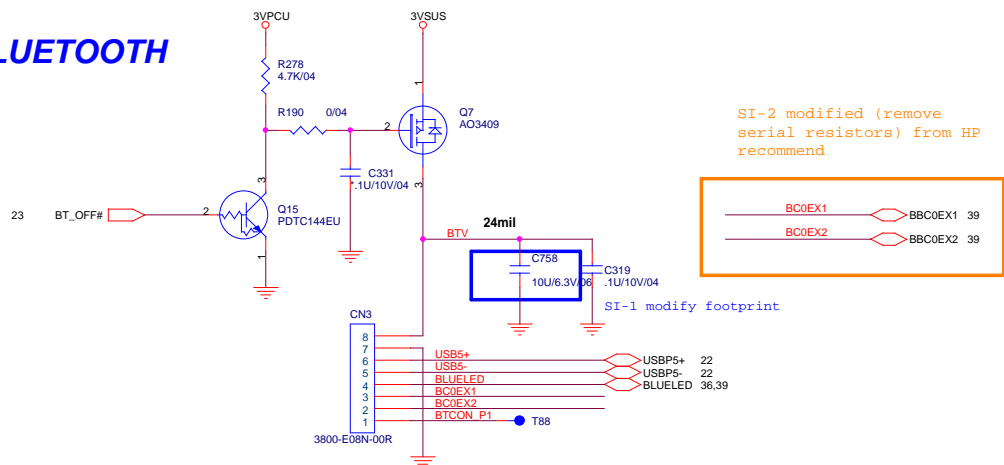


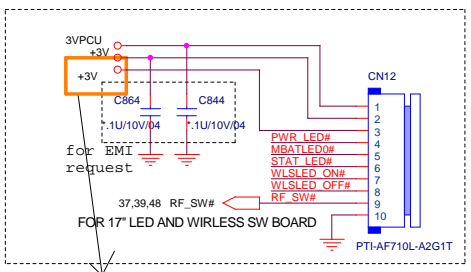
# NEWCARD

35

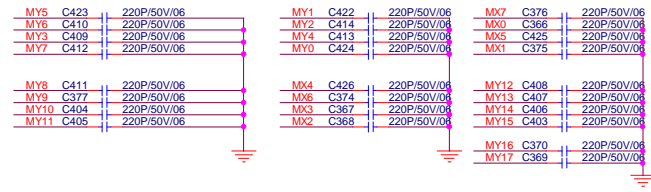
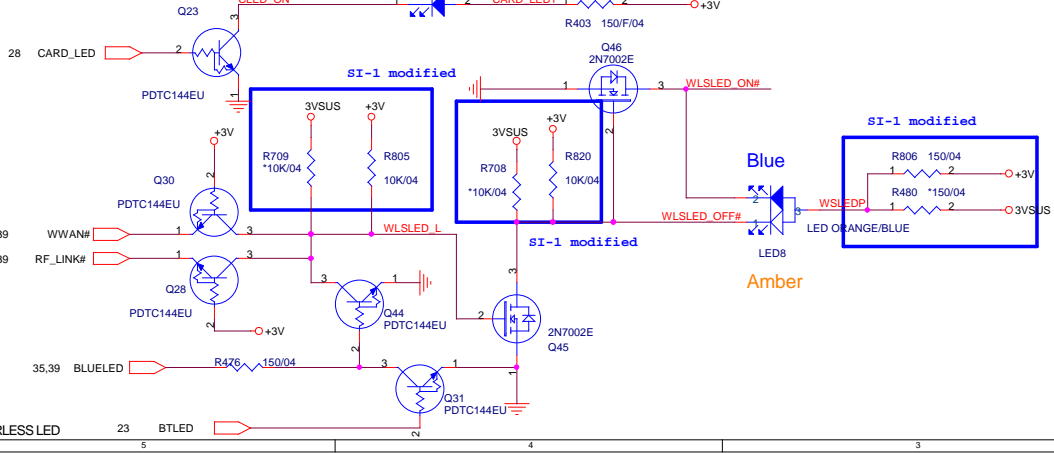
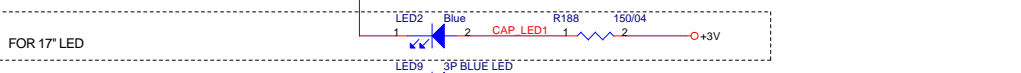
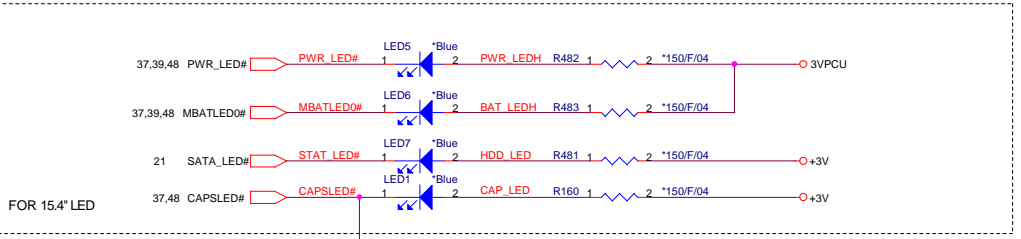
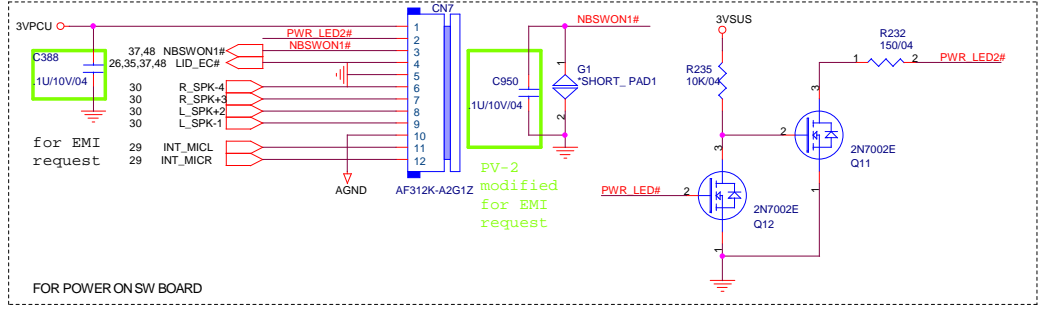
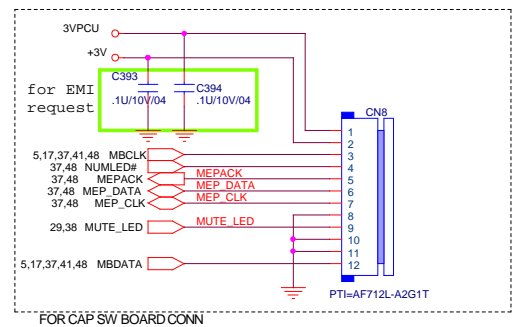


# BLUETOOTH

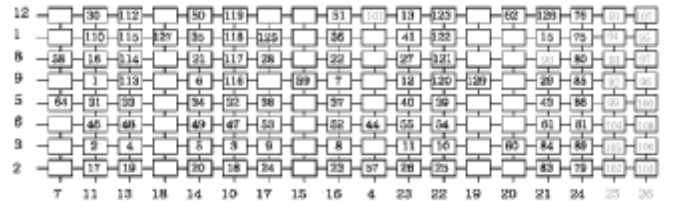
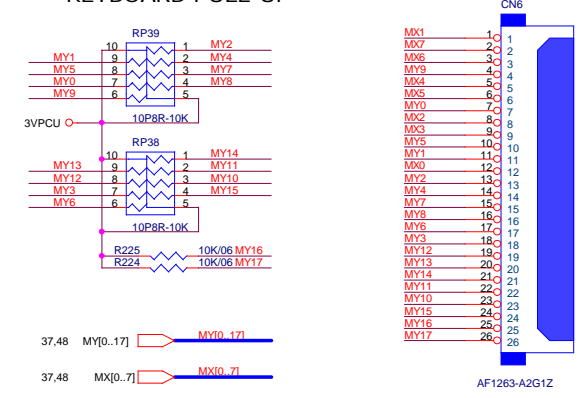




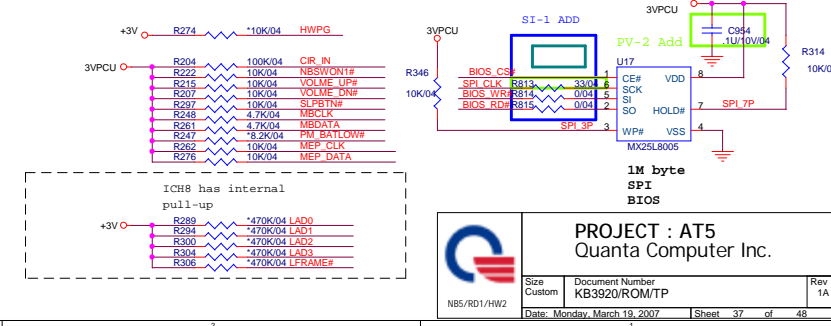
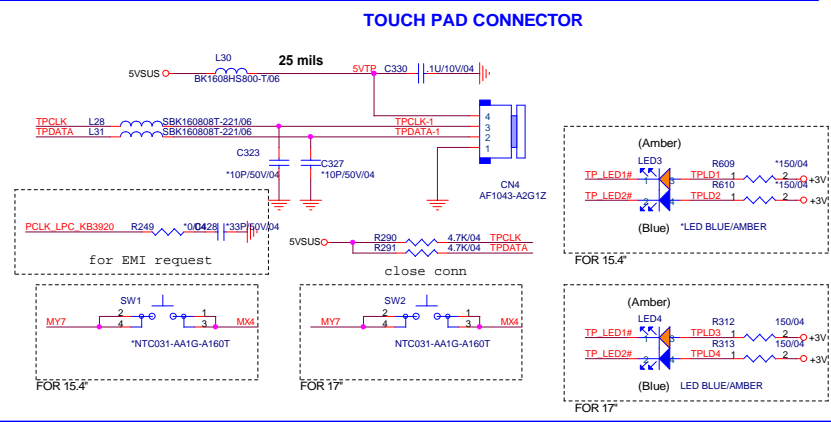
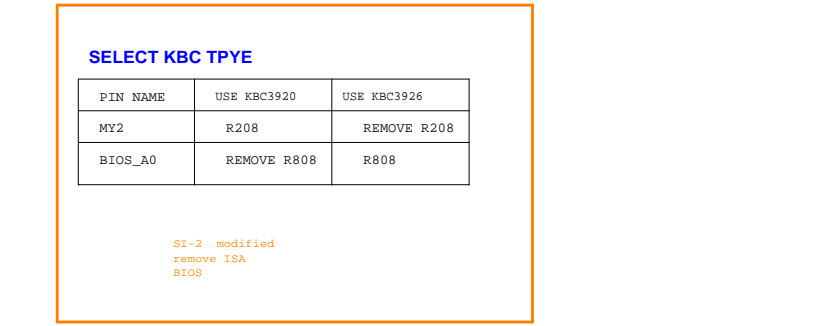
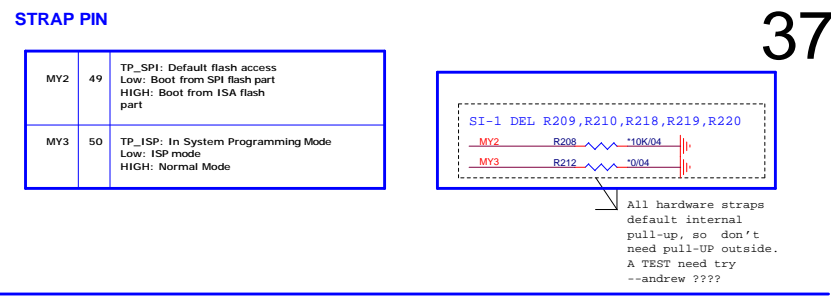
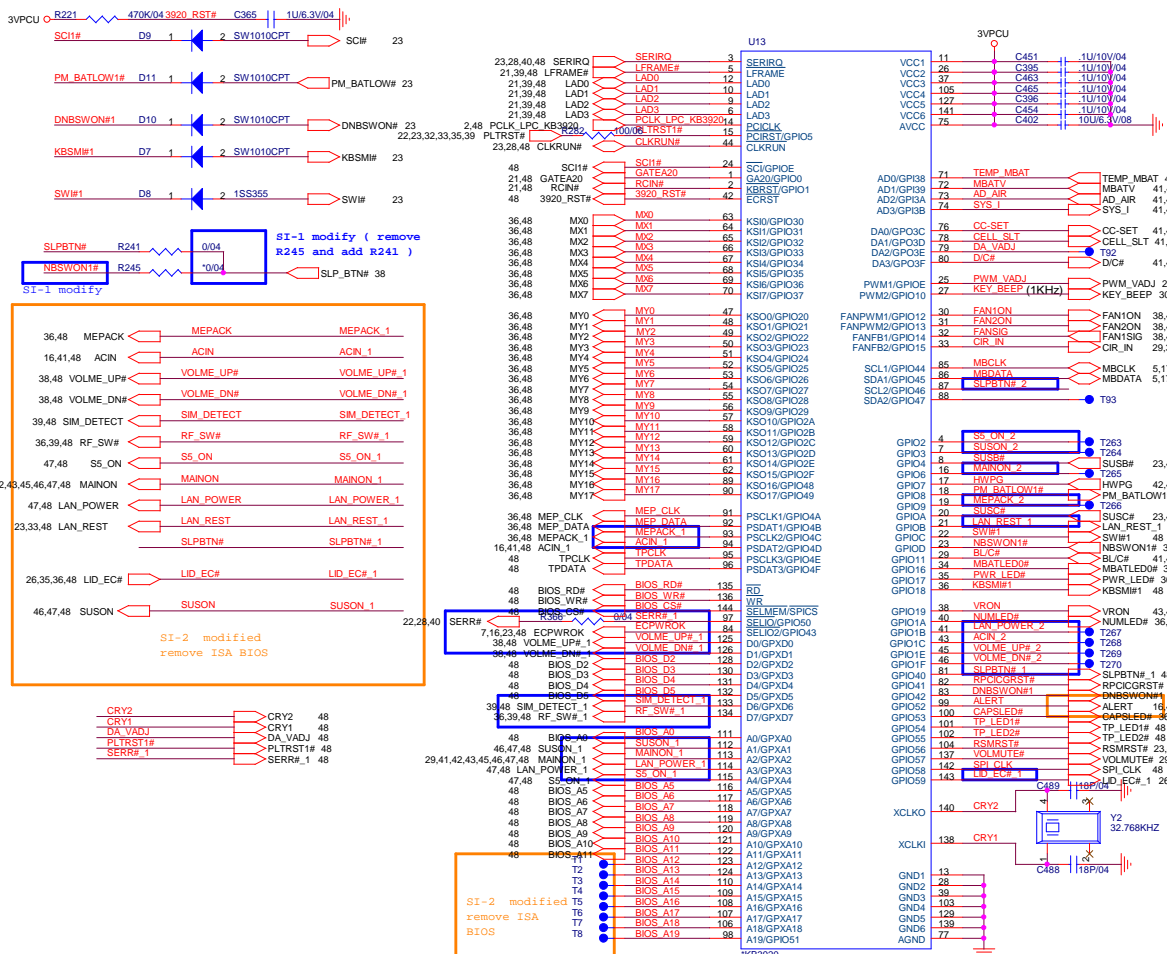
SI-2 modified for fix s3 not support wireless LED



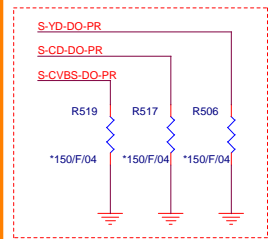
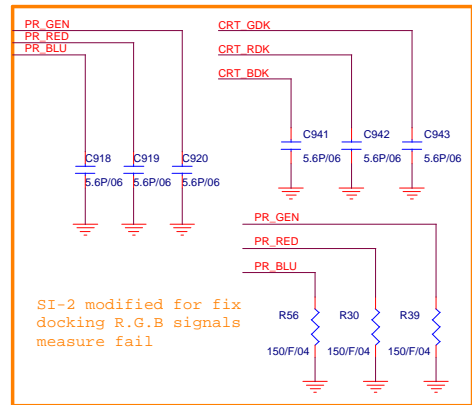
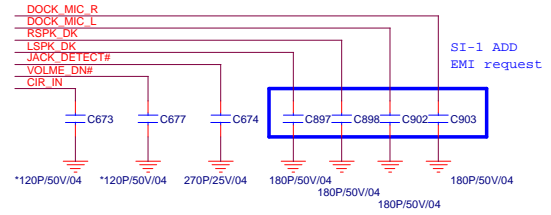
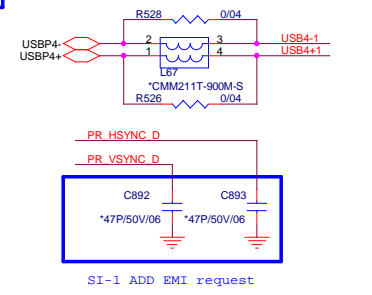
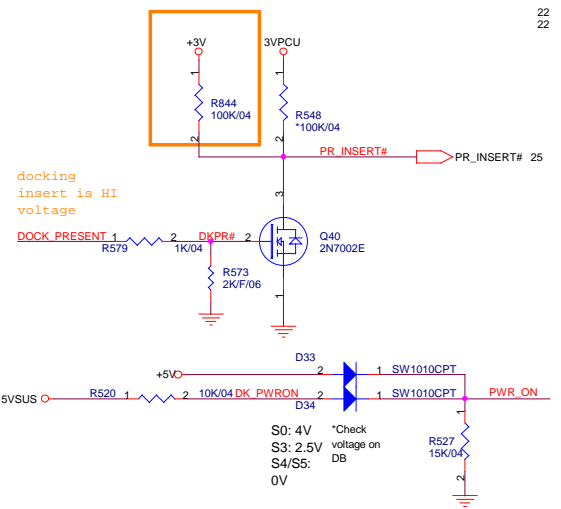
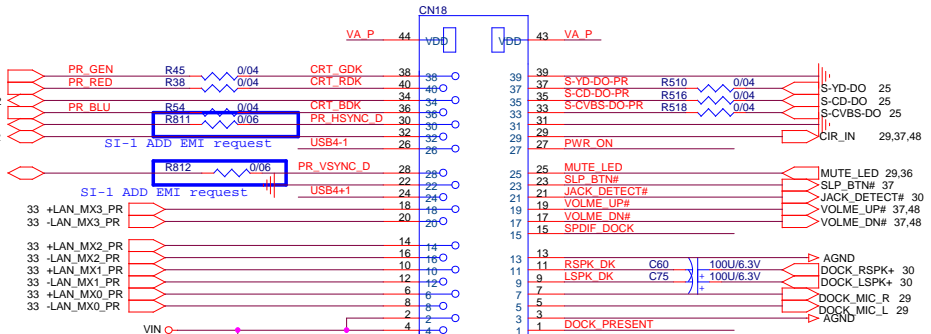
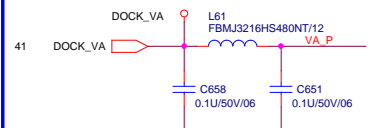
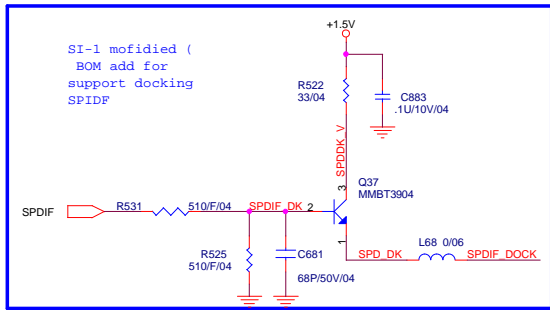
KEYBOARD PULL-UP



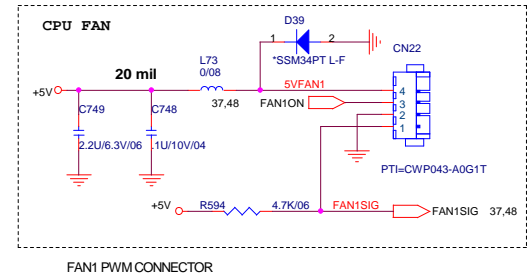
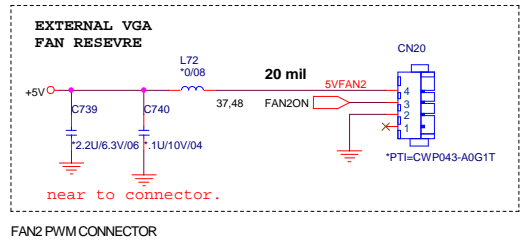
		<p><b>PROJECT : AT5</b> Quanta Computer Inc.</p>	
Size Custom	Document Number LED/KEYBOARD/SW	Rev 1A	
Date: Monday, March 19, 2007		Sheet 36 of 48	



support 6A 200mils  
CX000480005



FAN

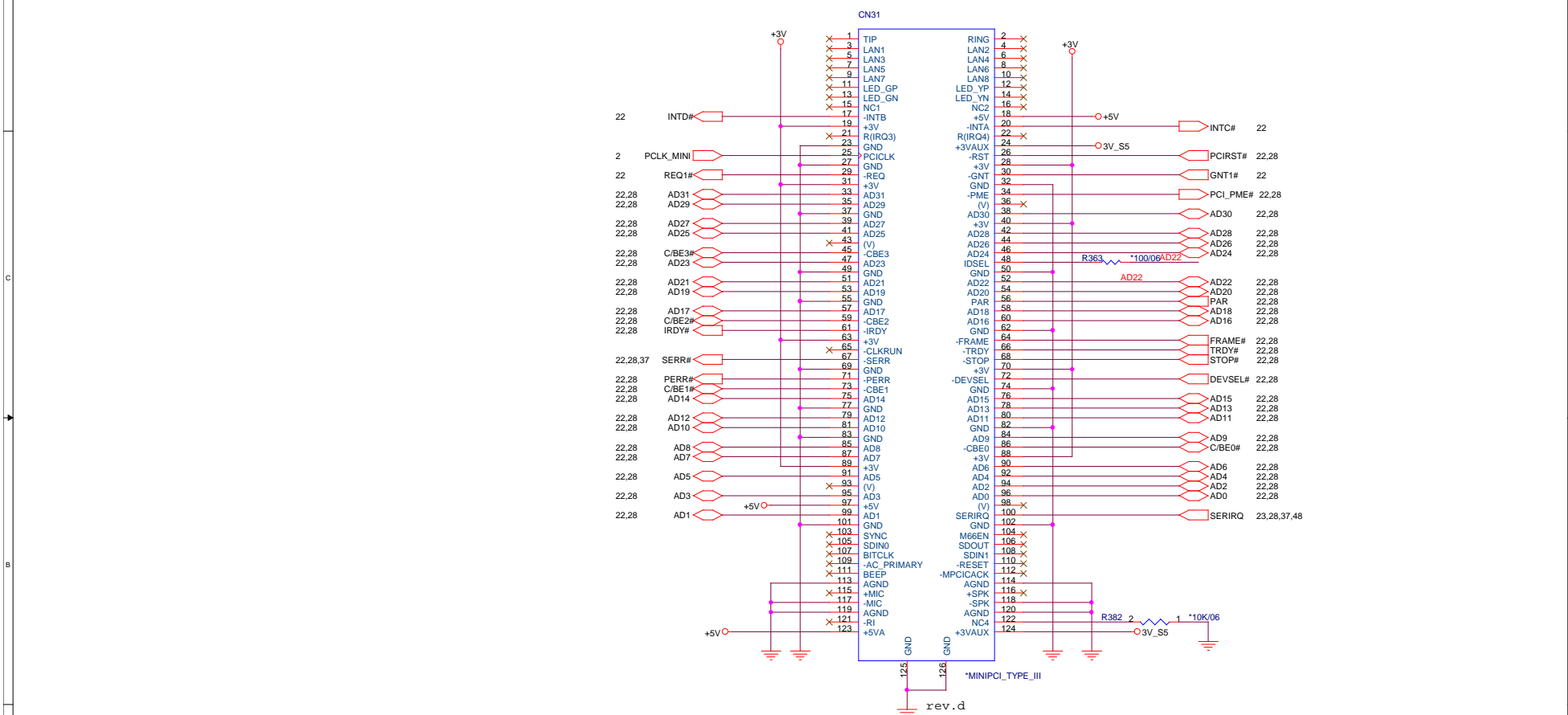




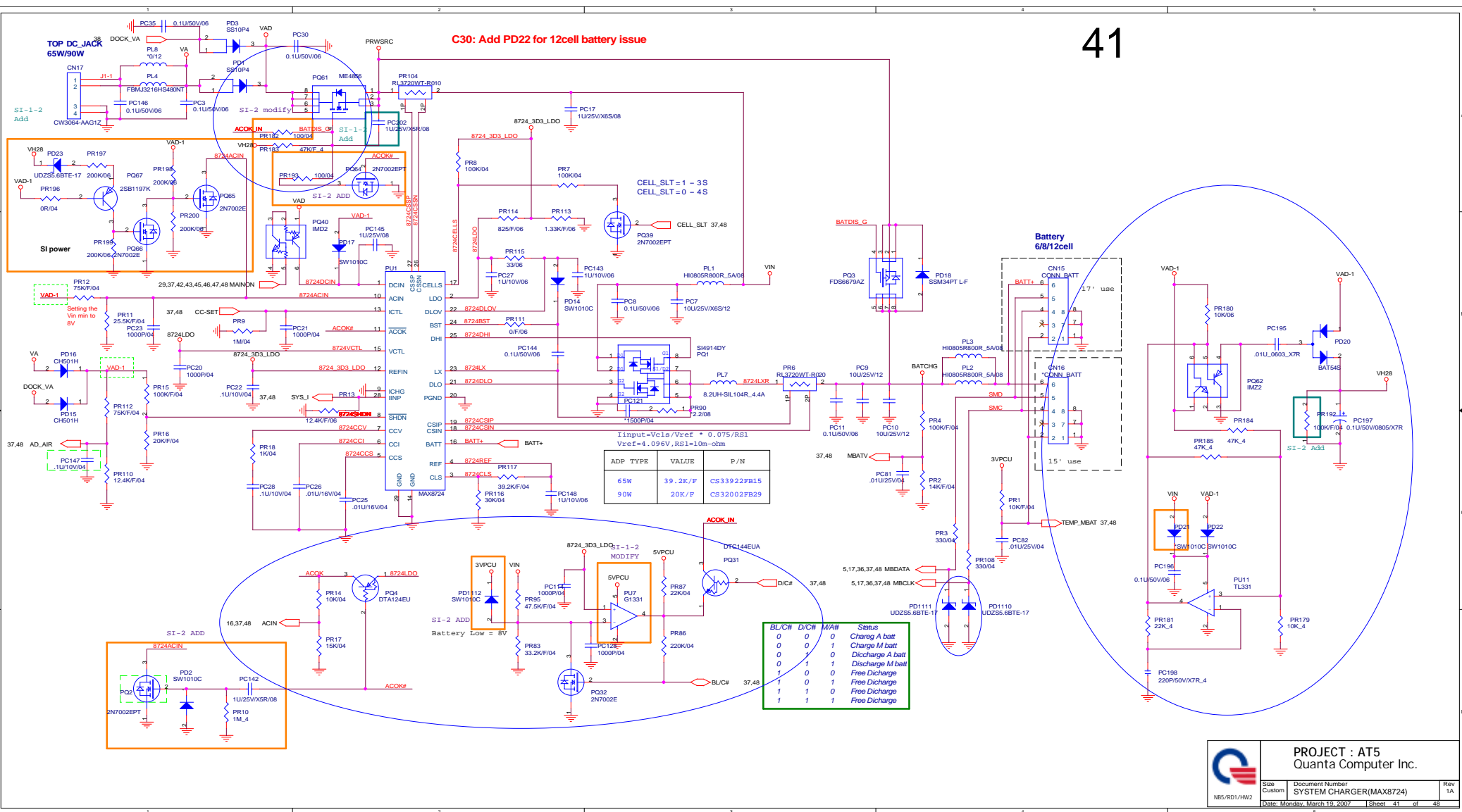


# MINI PCI TYPE III SLOT

INTC#, INTD#  
REQ1#/GNT1#  
D\_ID : AD22



C30: Add PD22 for 12cell battery issue



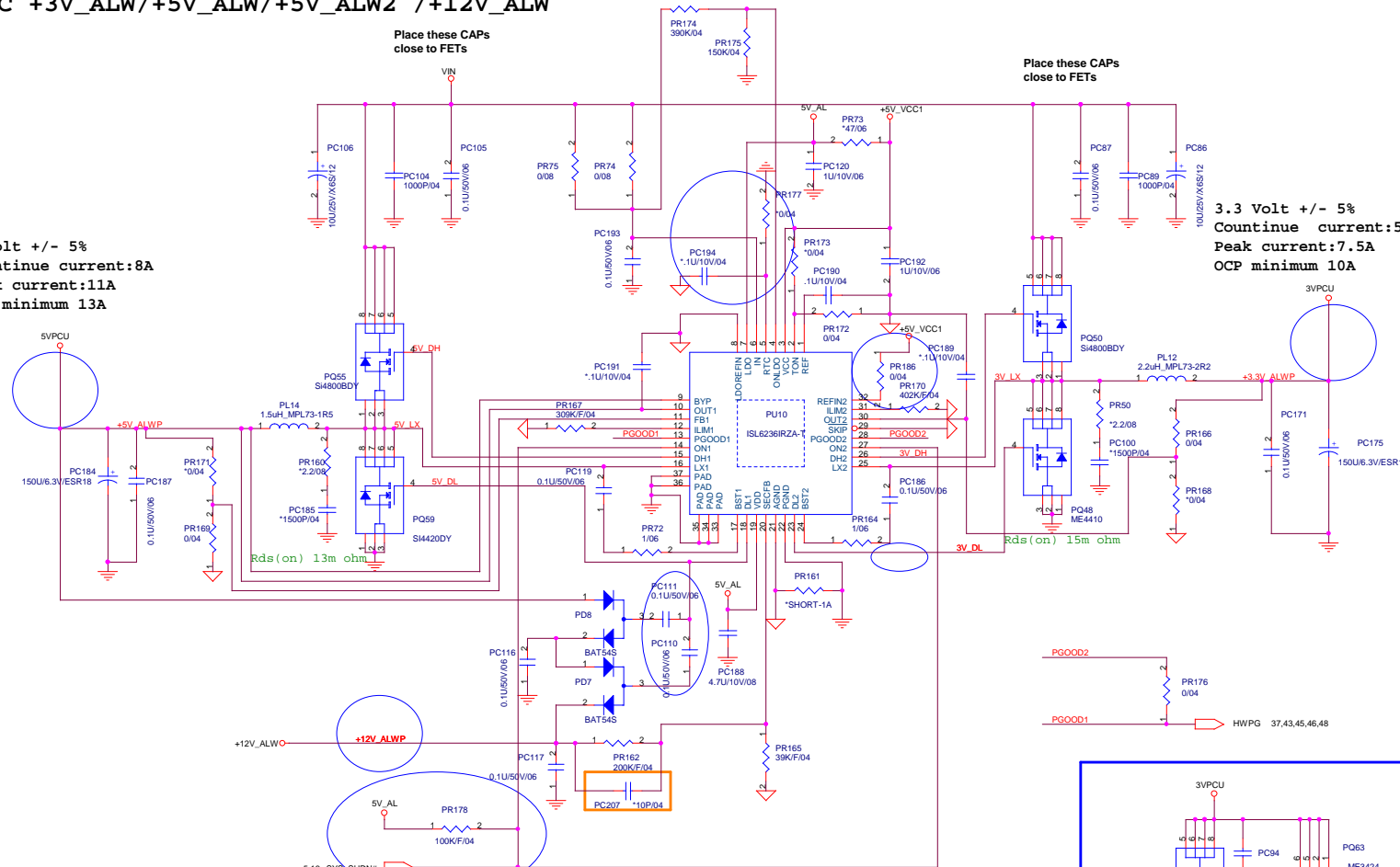
DC/DC +3V\_ALW/+5V\_ALW/+5V\_ALW2 /+12V\_ALW

Place these CAPS close to FETs

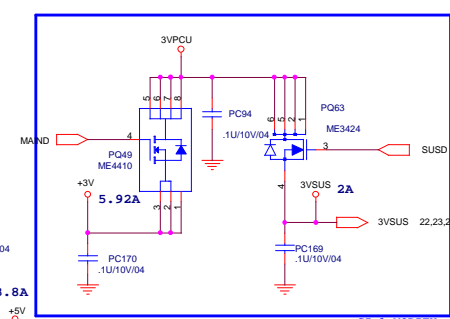
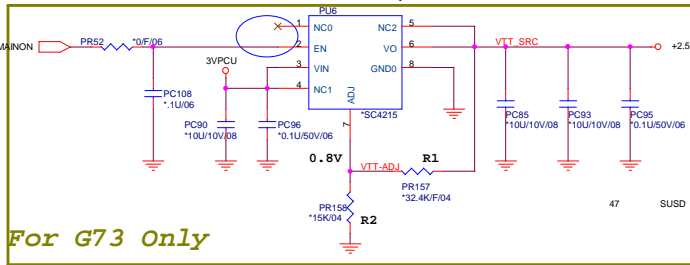
Place these CAPS close to FETs

5 Volt +/- 5%  
Countinue current:8A  
Peak current:11A  
OCP minimum 13A

3.3 Volt +/- 5%  
Countinue current:5A  
Peak current:7.5A  
OCP minimum 10A



Max Power Consumption 1.6W



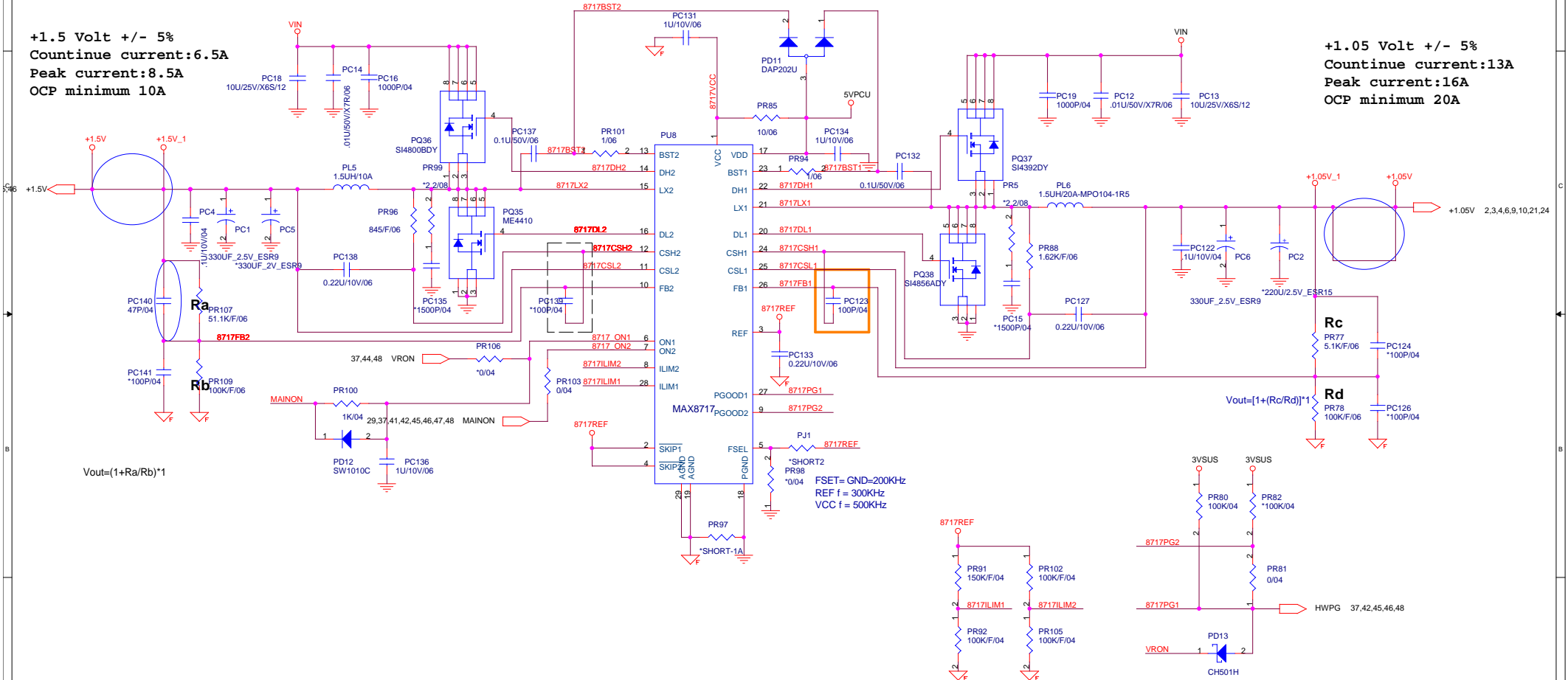
PROJECT : AT5  
Quanta Computer Inc.

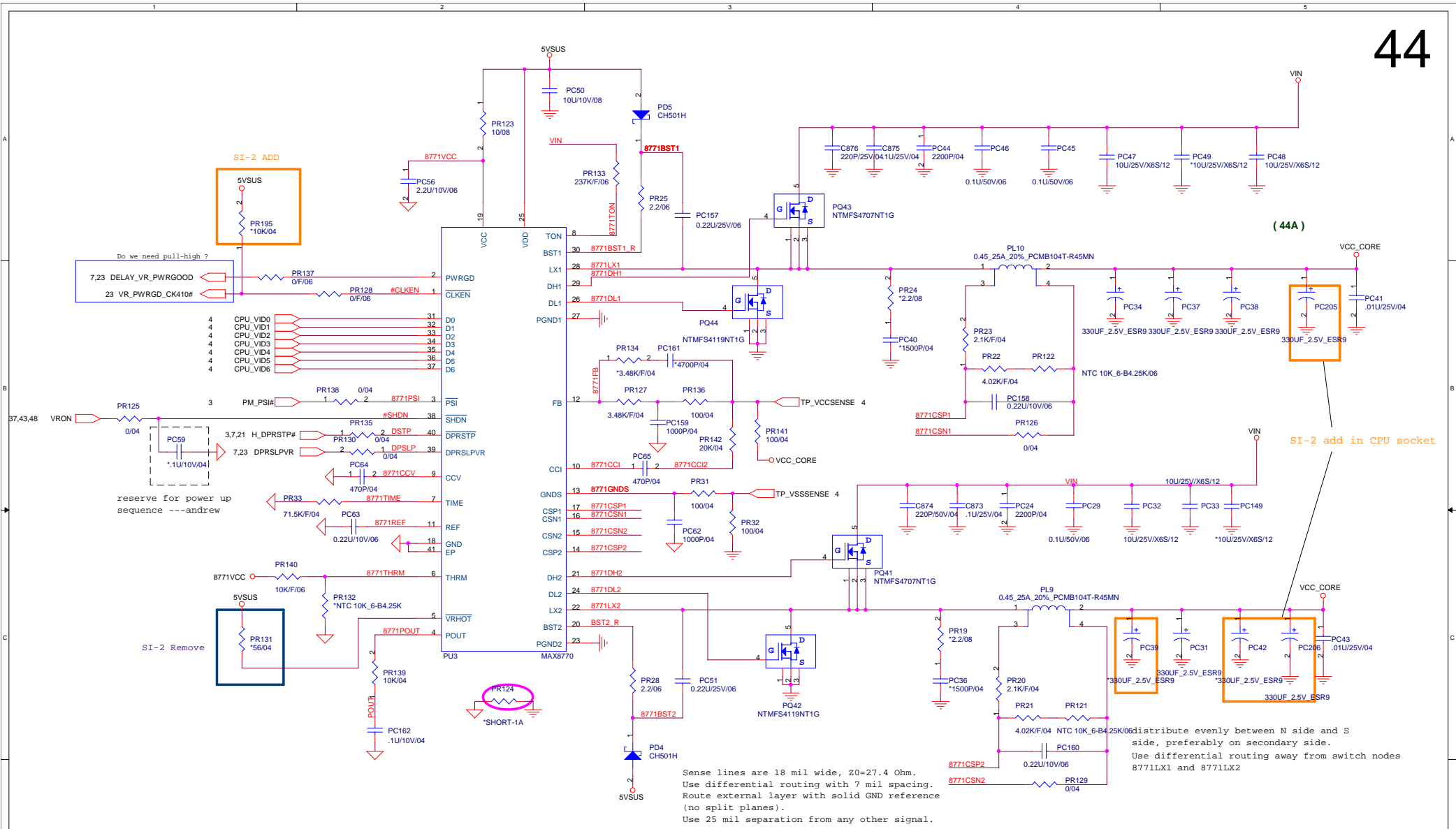
Size Custom	Document Number 3V/5V	Rev 1A
Date: Monday, March 19, 2007		Sheet 42 of 48

NBS/RD1/HW2

**+1.5 Volt +/- 5%**  
**Countinue current:6.5A**  
**Peak current:8.5A**  
**OCP minimum 10A**


**+1.05 Volt +/- 5%**  
**Countinue current:13A**  
**Peak current:16A**  
**OCP minimum 20A**





Sense lines are 18 mil wide, Z0=27.4 Ohm.  
 Use differential routing with 7 mil spacing.  
 Route external layer with solid GND reference  
 (no split planes).  
 Use 25 mil separation from any other signal.

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

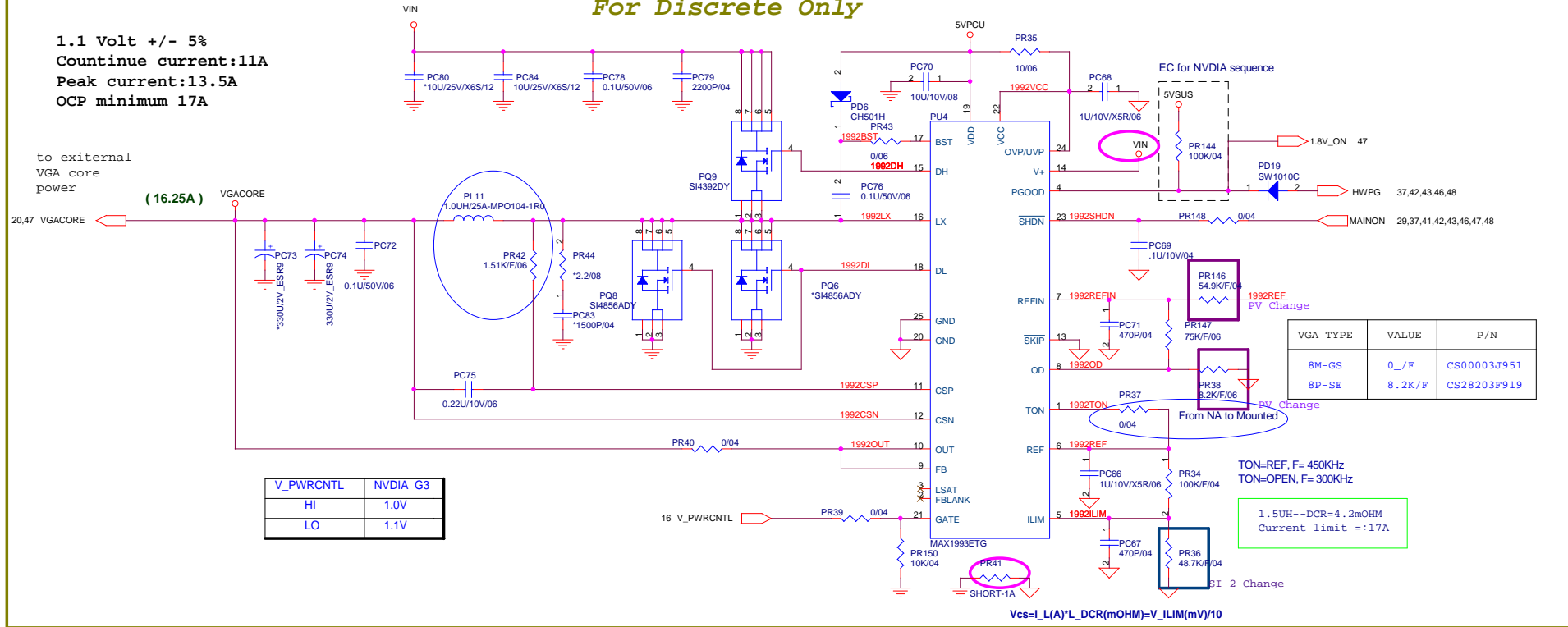
		<b>PROJECT : AT5</b> Quanta Computer Inc.	
		Size Custom NBS/RD1/HW2	Document Number CPU_CORE(MAX8771)
Date: Monday, March 19, 2007		Sheet 44 of 48	



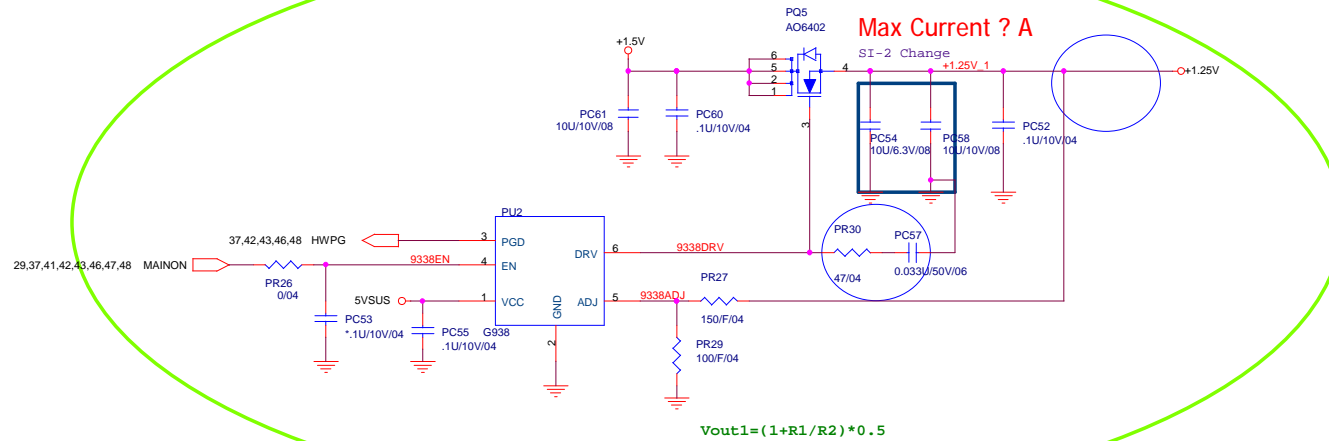
For Discrete Only

1.1 Volt +/- 5%  
 Countinue current:11A  
 Peak current:13.5A  
 OCP minimum 17A

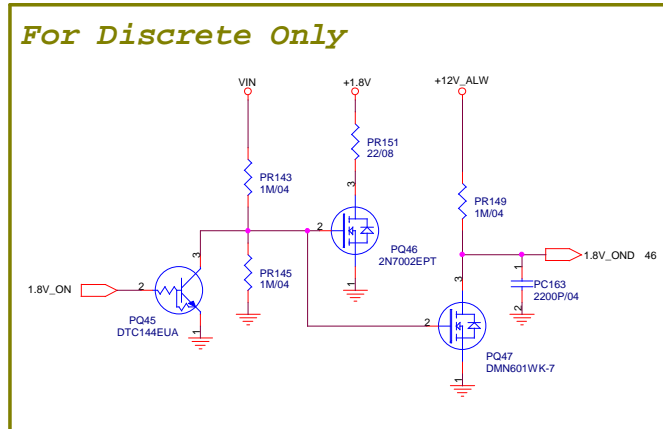
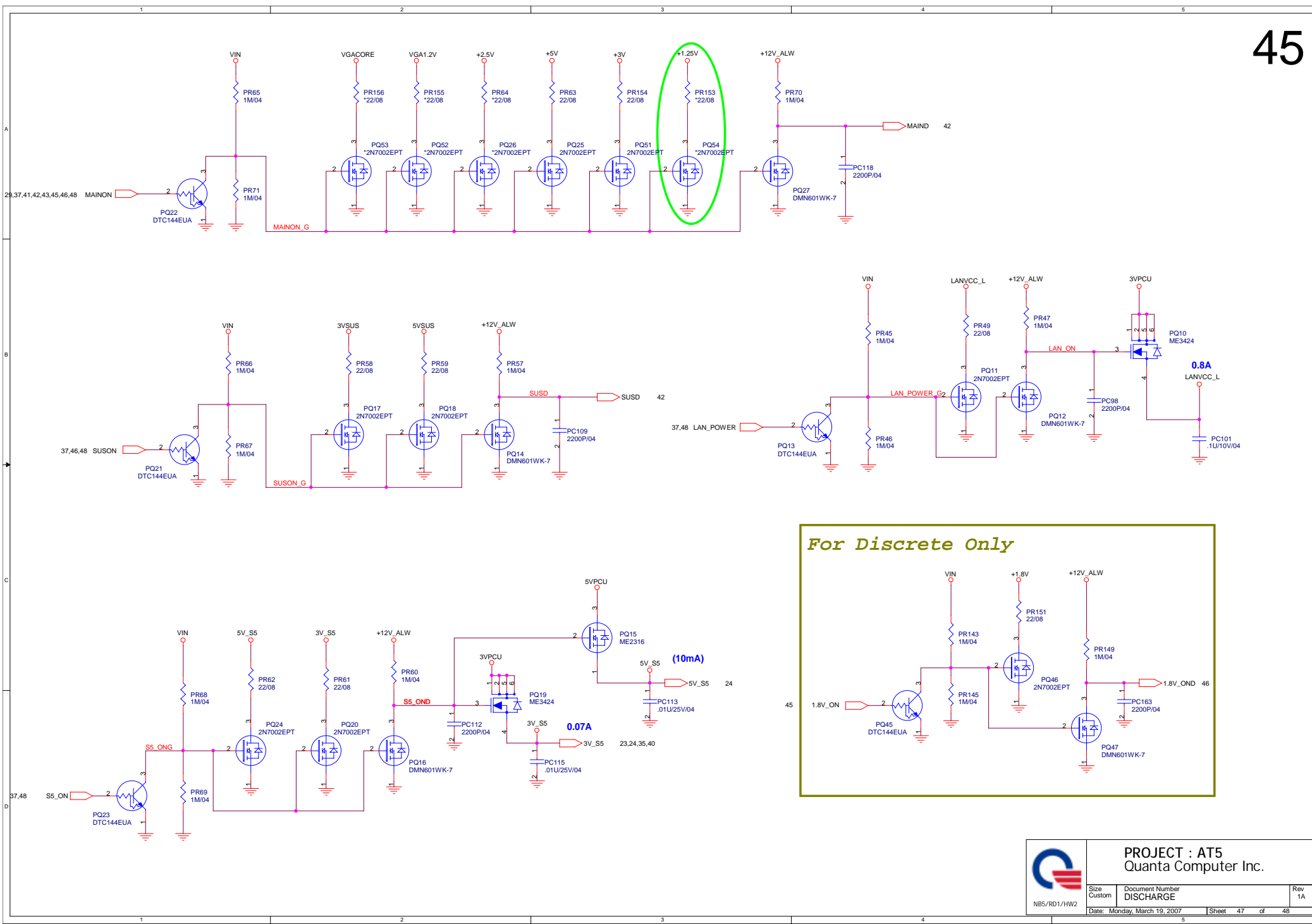
to external  
 VGA core  
 power




Max Current ? A







	<b>PROJECT : AT5</b> Quanta Computer Inc.	
	Size Custom	Document Number DISCHARGE
Date: Monday, March 19, 2007		Sheet 47 of 48

