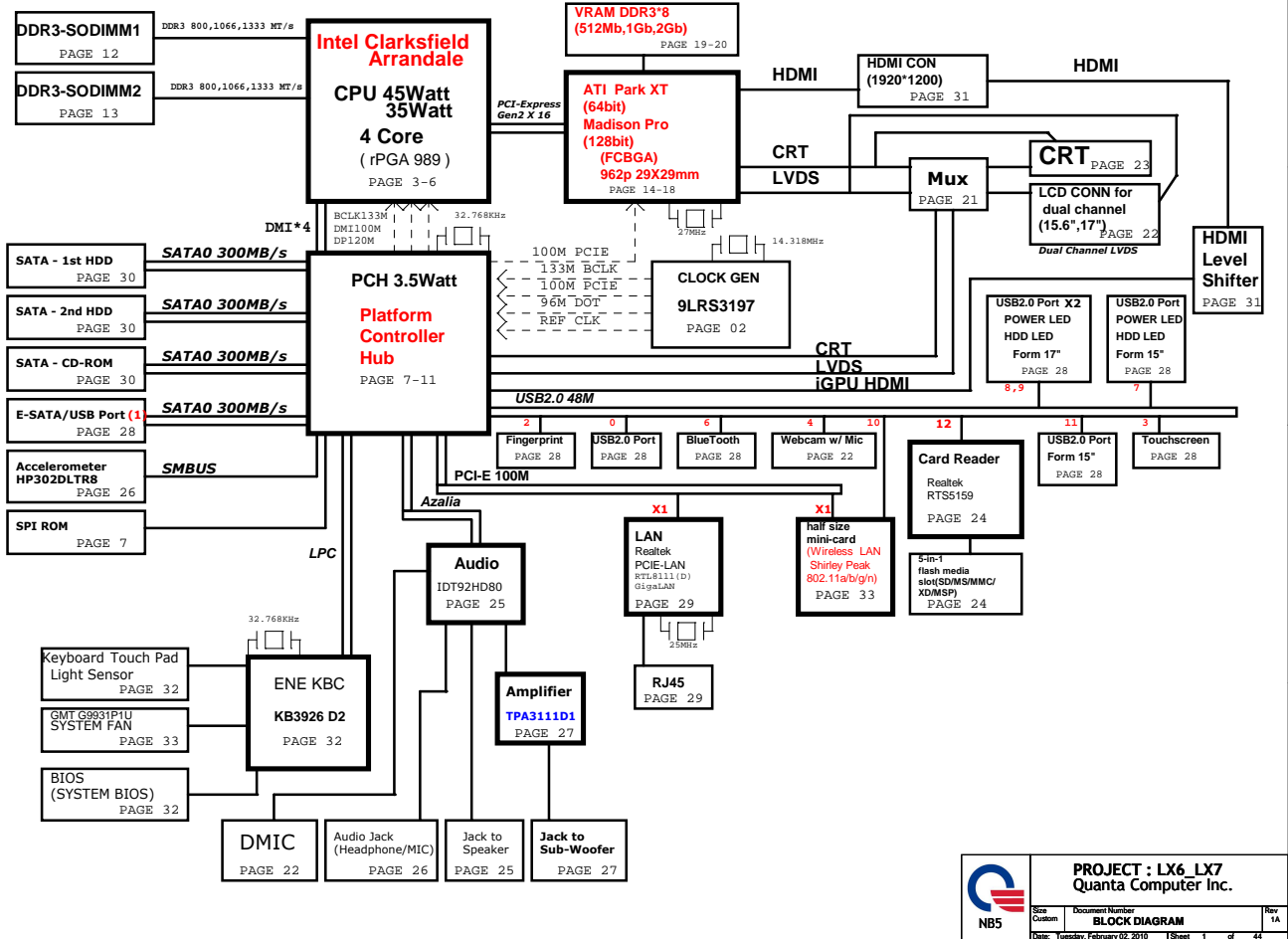


LX6/7 (Liverpool) BLOCK DIAGRAM

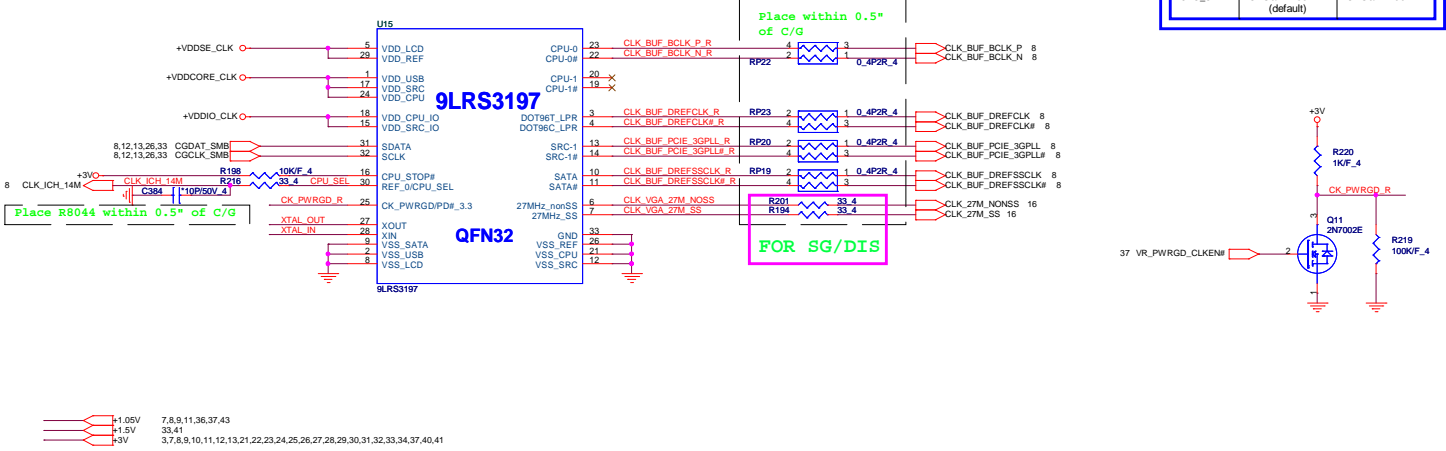
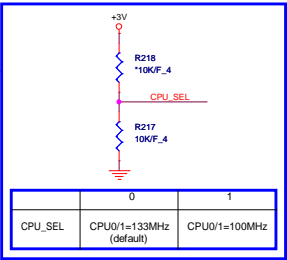
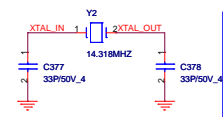
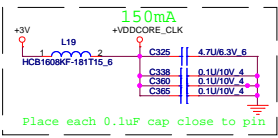
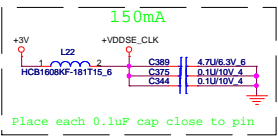
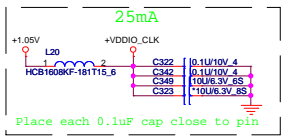
PCB STACK UP
6L Dis.

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT



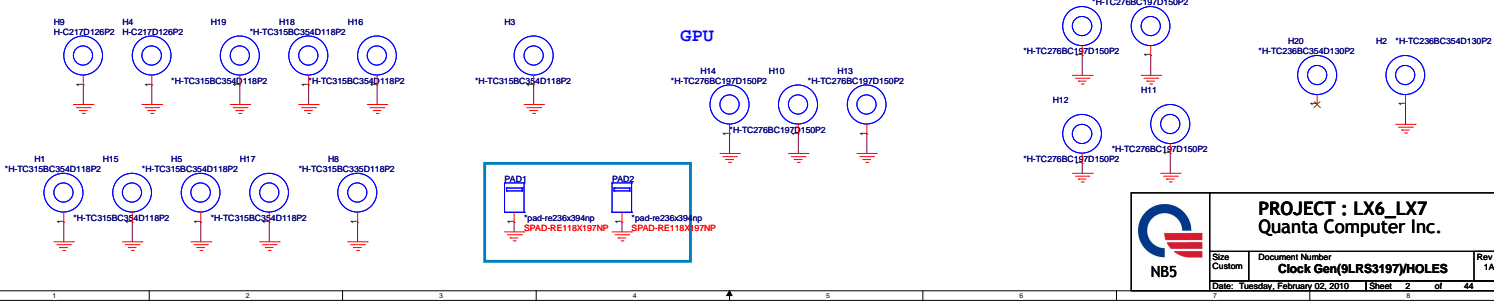
DDR III SMD DR VTERM and GPU+1.5V/+1.0V(RT8207G)	PAGE 40
BATTERY SELECTOR	PAGE 42
SYSTEM CHARGER(P2806)	PAGE 41
SYSTEM POWER RT8206B	PAGE 35
+1.05V_VTT and GPU +1.8V/+3V(VT358)	PAGE 38
VCCP +1.05V/+1.8V(RT8204)	PAGE 36
VGACORE/VDDC(RT8208/RT9018A)	PAGE 39
CPU CORE (ADP3212)	PAGE 37

	PROJECT : LX6_LX7 Quanta Computer Inc.	
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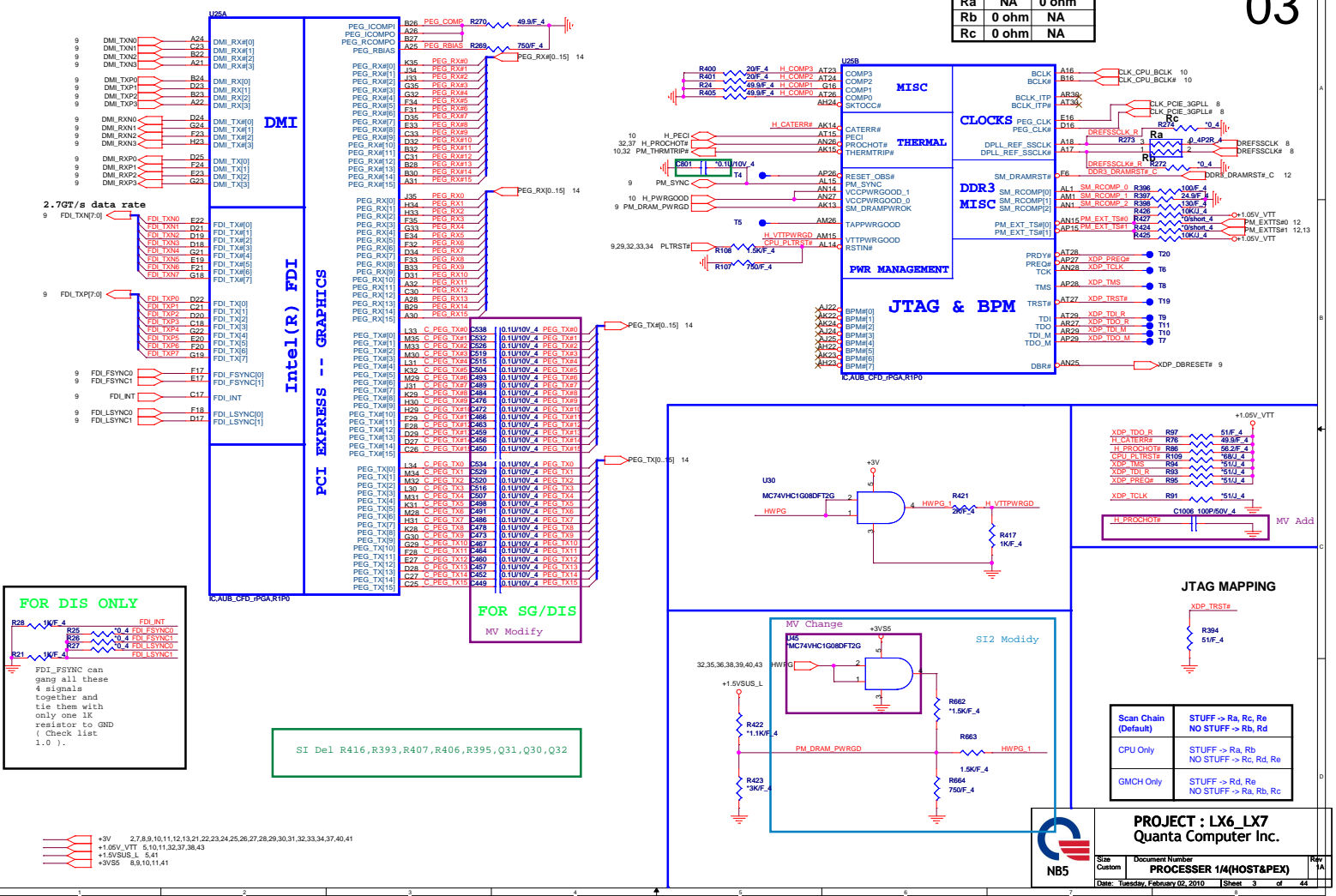


+1.05V	7, 8, 9, 11, 36, 37, 43
+1.5V	33, 41
+3V	3, 7, 8, 9, 10, 11, 12, 13, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 37, 40, 41

SOLE



DIS	NA	0 ohm
Ra	0 ohm	NA
Rb	0 ohm	NA
Rc	0 ohm	NA



FOR DIS ONLY

R28 10K_F_4
R25 10K_F_4
R26 10K_F_4
R27 10K_F_4
R21 10K_F_4

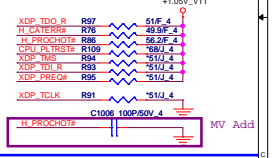
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

FOR SG/DIS

MV Modify

SI Del R416, R393, R407, R406, R395, Q31, Q30, Q32



JTAG MAPPING

XDP_TRST# R34 51K_F_4

Scan Chain	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : LX6 LX7
Quanta Computer Inc.

Rev: A

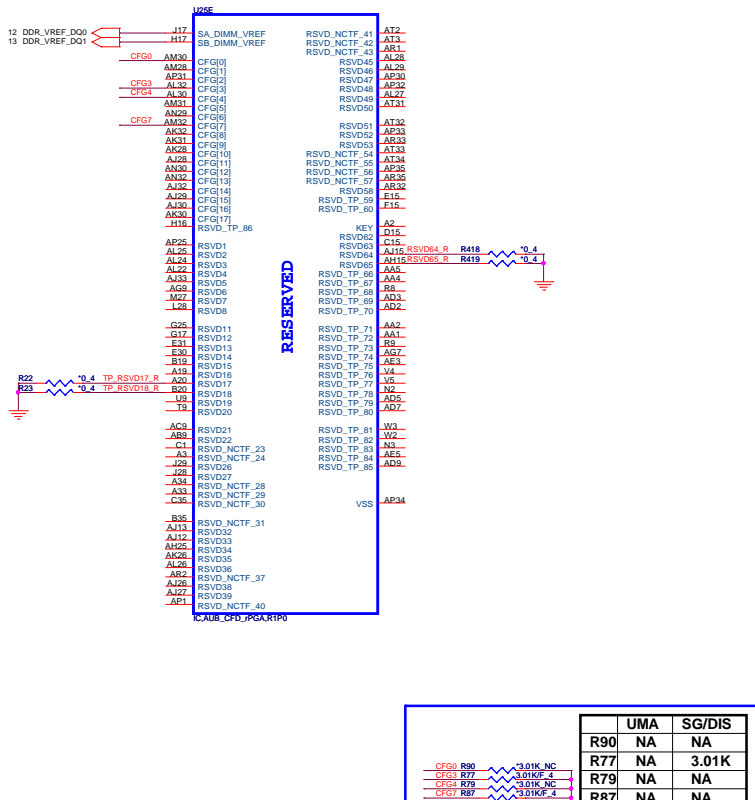
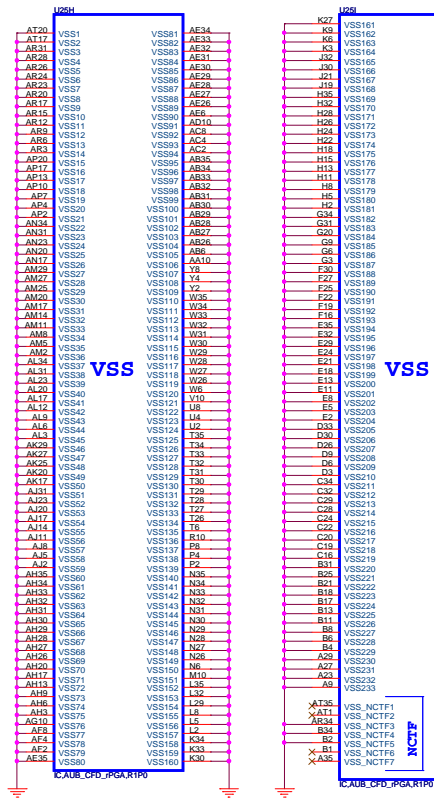
Docu: PROCESSOR 1M(HOST&PEX)

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- +3V 2,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41
- +1.05V_VTT 5,10,11,32,37,38,43
- +1.5VSUS_L 5,41
- +3VS5 8,9,10,11,41

AUBURDALE/CLARKSFIELD PROCESSOR (GND)

AUBURDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both vPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

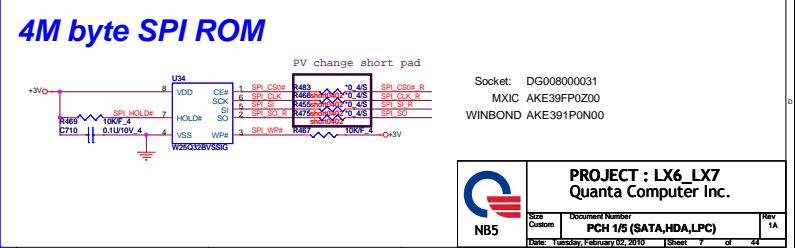
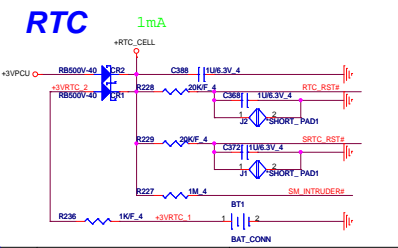
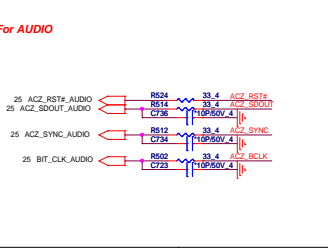
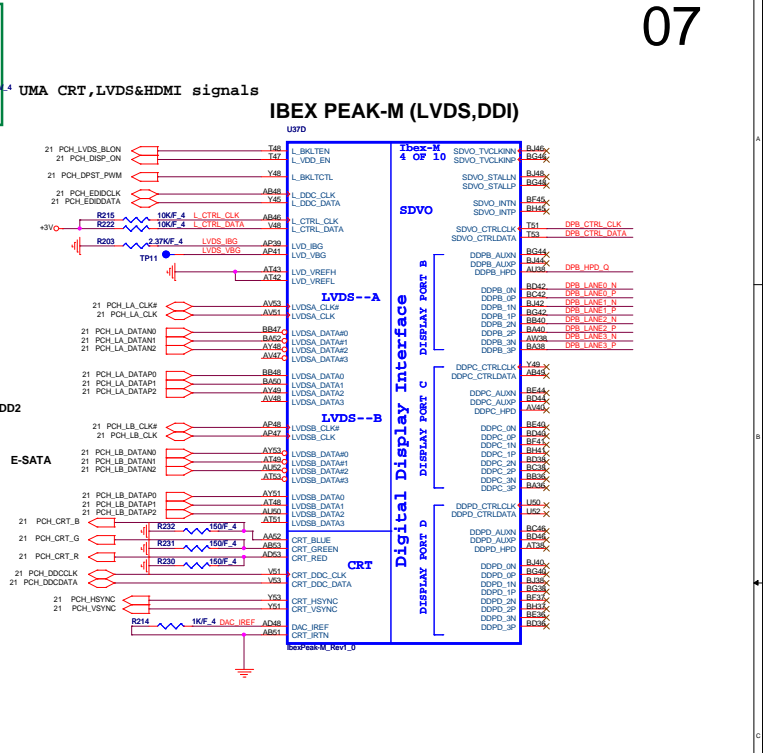
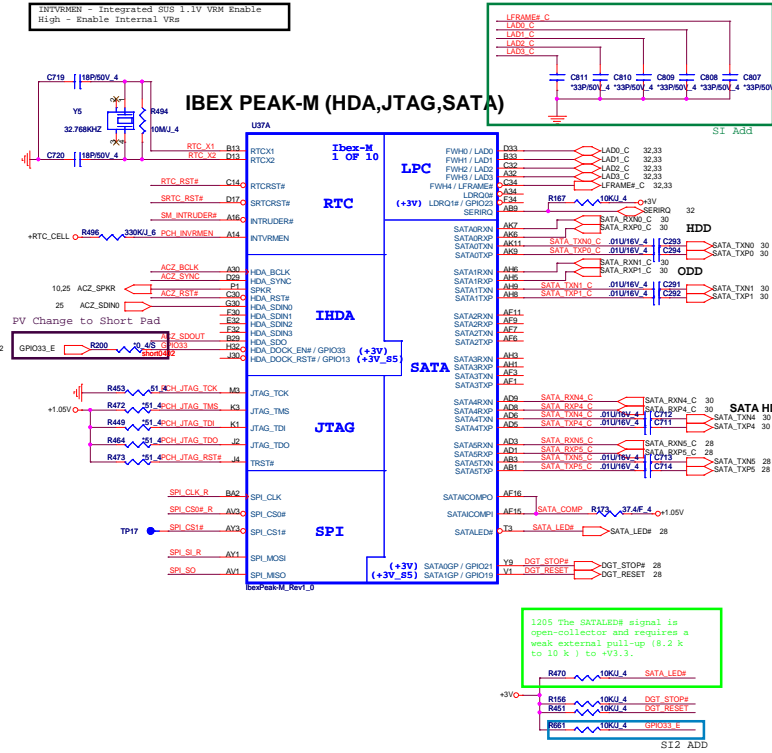
	UMA	SG/DIS
R90	NA	NA
R77	NA	3.01K
R79	NA	NA
R87	NA	NA

CFG[1:0] - PCI_Epress Configuration Select
 * 11 = 1 x 16 PEG
 * 10 = 2 x 8 PEG

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Quanta Computer Inc.

NB5
 Size Custom Document Number **PROCESSOR 4/4 (GND)** Rev 1A
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INTRVMMEN - Integrated VMM 1.1V VMM Enable
High - Enable Internal VRs

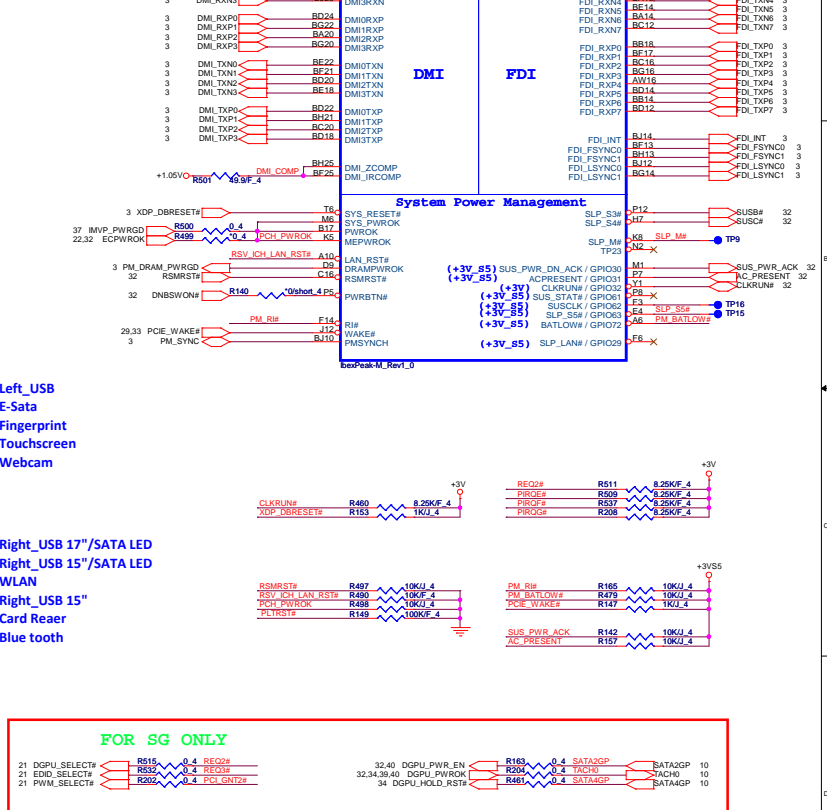
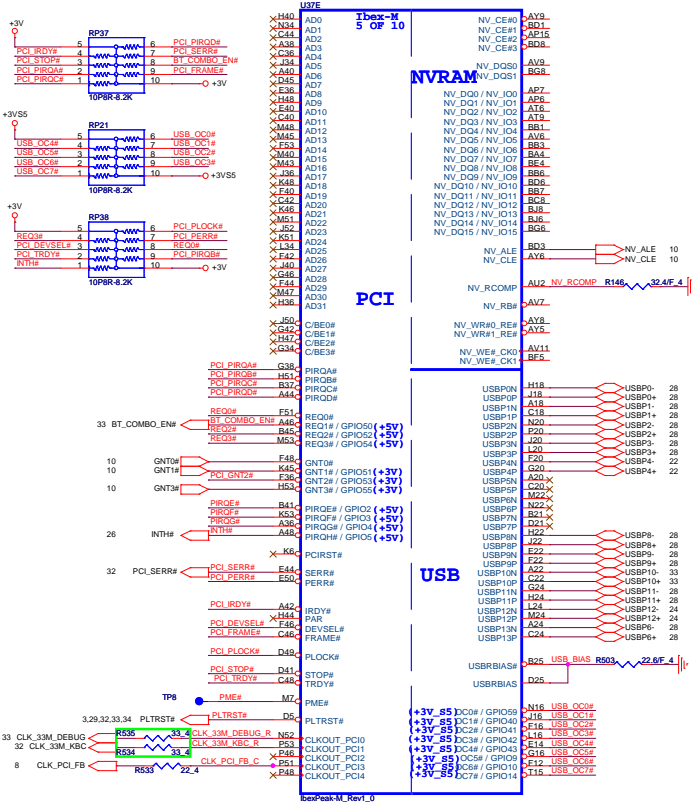


Socket: DG008000031
MXIC AKE39FP0Z00
WINBOND AKE391P0N00

PROJECT : LX6_LX7
Quanta Computer Inc.

NBS	Doc Number	PCH 1/5 (SATA,HDA,LPC)	Rev 1A
	Date		

IBEX PEAK-M (PCI,USB,NVRAM)



Left_Usb
E-sata
Fingerprint
Touchscreen
Webcam

Right_Usb 17"/SATA LED
Right_Usb 15"/SATA LED
WLAN
Right_Usb 15"
Card Reaer
Blue tooth

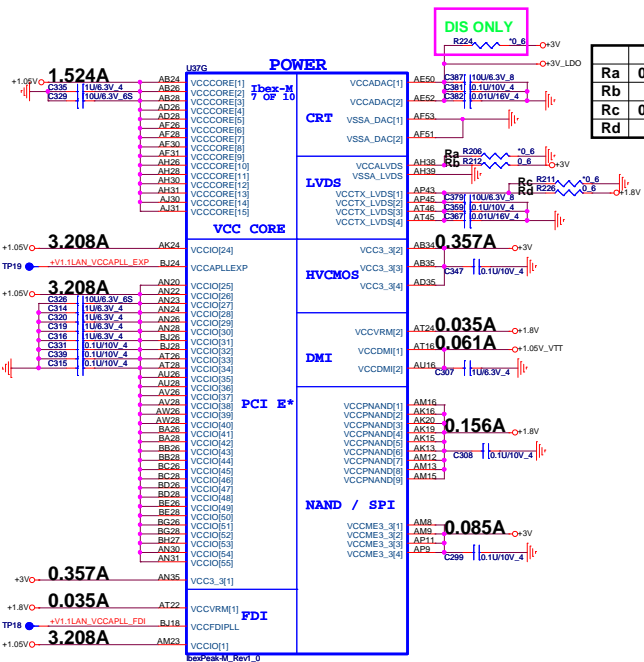
Quanta Computer Inc.

Project : LX6 LX7

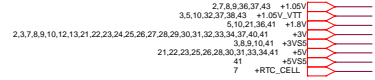
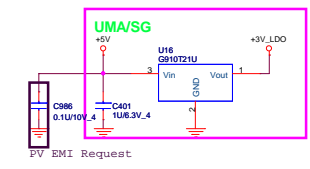
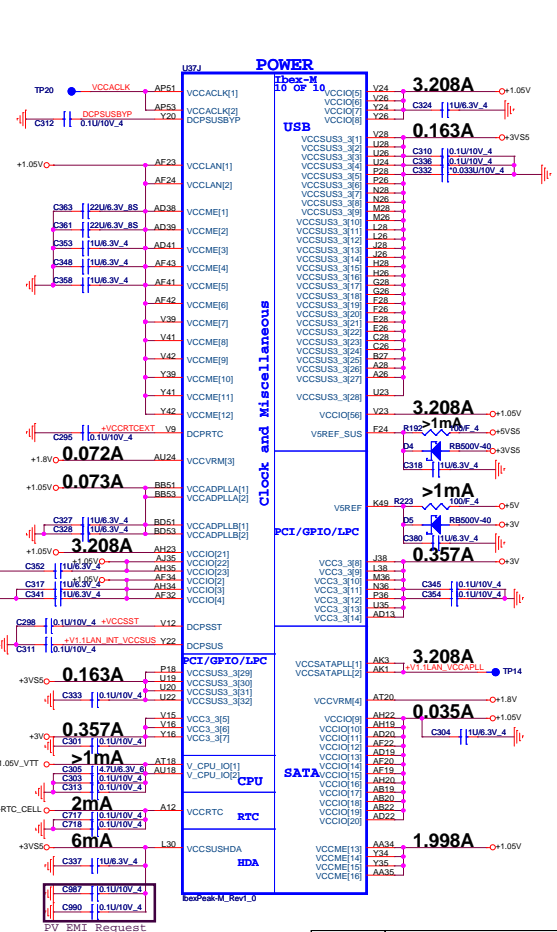
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2.7,8,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41, 3.8,10,11,41 +3V +3V5



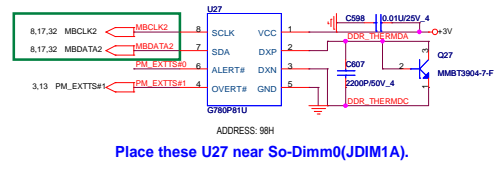
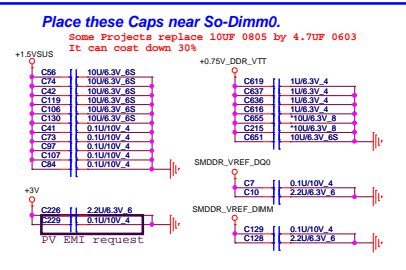
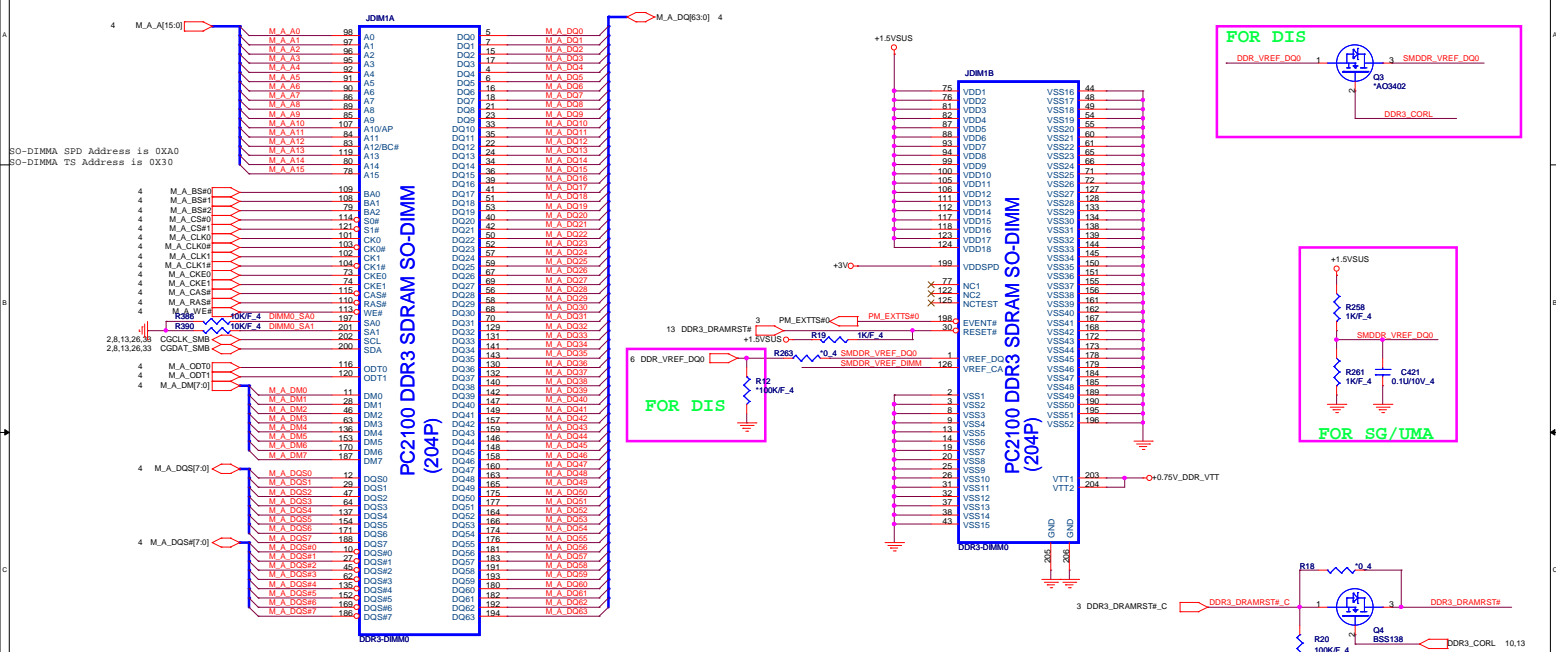
	DIS	SG/UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm



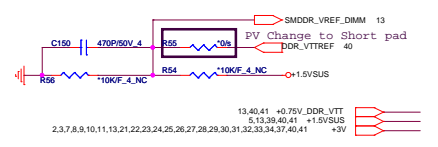
PROJECT : LX6_LX7
Quanta Computer Inc.

Size: Custom
Document Number: **PCH S/S (POWER)**
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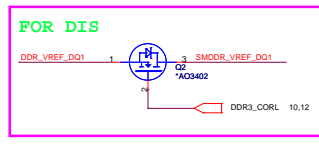
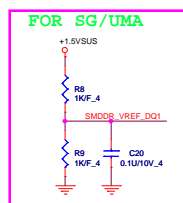
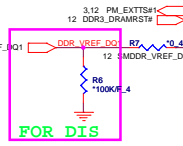
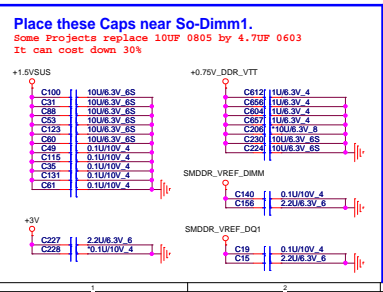
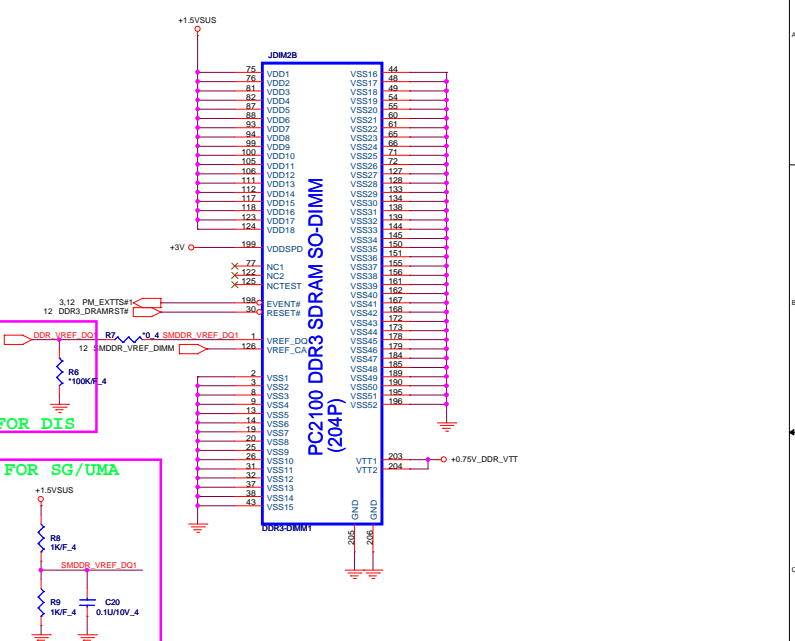
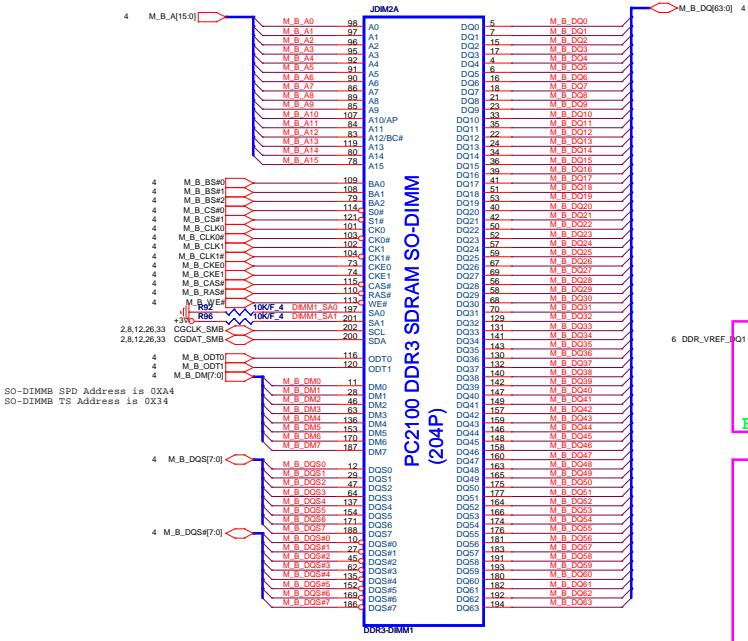


Place these U27 near So-Dimm0(JDM1A).



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Quanta Computer Inc.

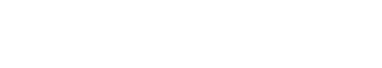
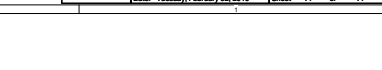
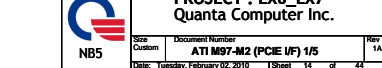
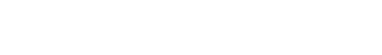
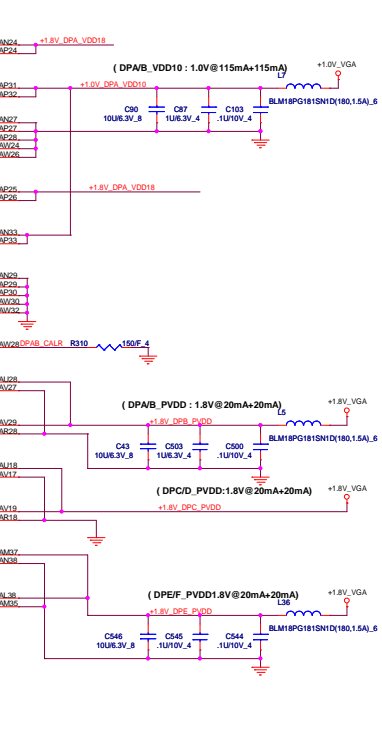
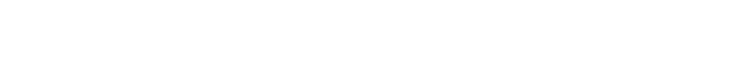
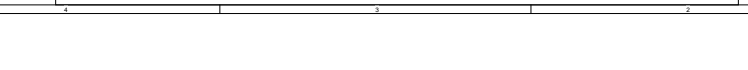
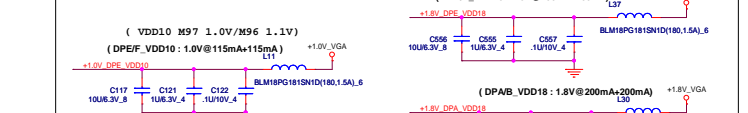
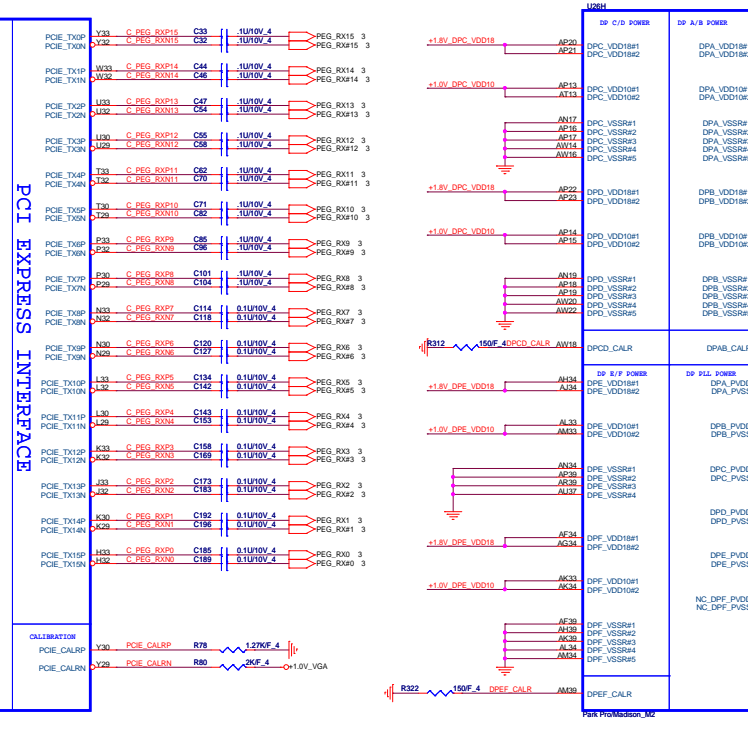
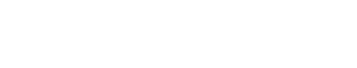
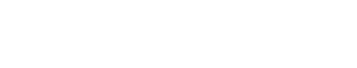
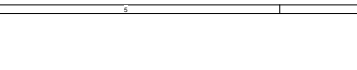
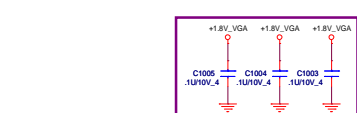
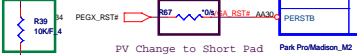
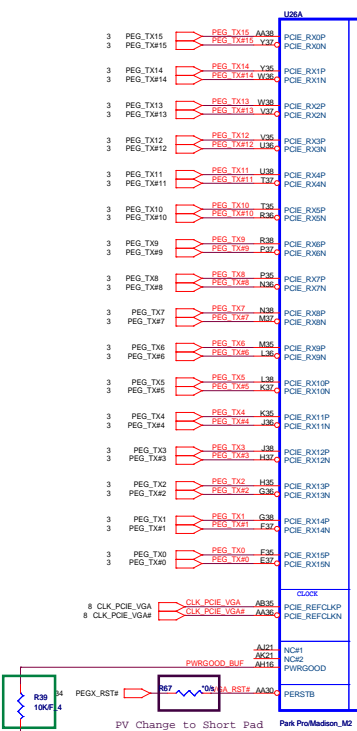
Size Custom	Document Number DDR3 DIMM-0	Rev 1A
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12.40.41 +0.75V_DDR_VTT
 5.12.39-40.41 +1.5VSUS
 2.3.7.8.9.10.11.12.21.22.23.24.25.26.27.28.29.30.31.32.33.34.37.40.41 +3V

PROJECT : LX6_LX7
Quanta Computer Inc.

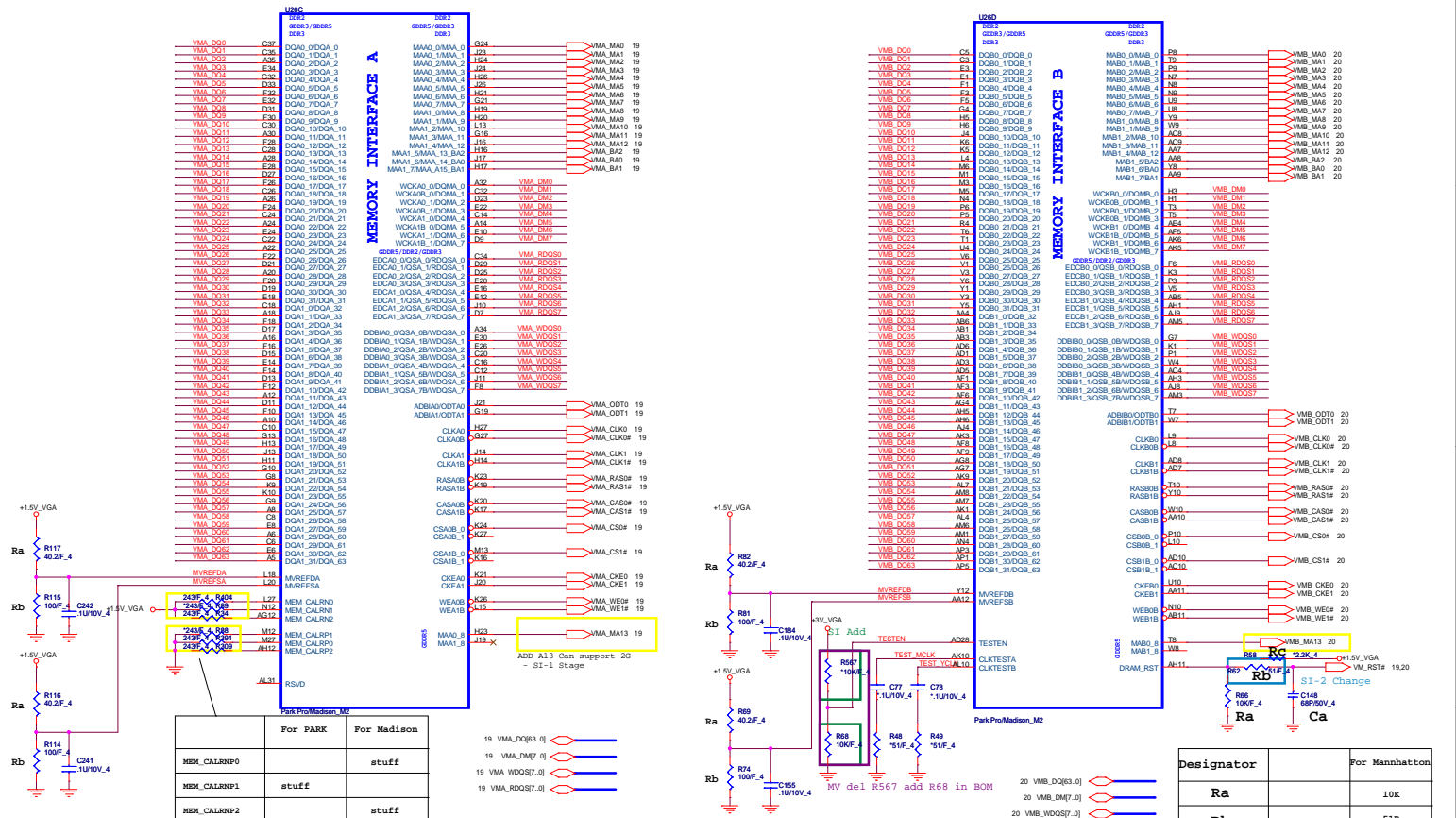
Size: Custom
 Document Number: **DDR3 DIMM-1**
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Legend:
 +3V
 +1.0V_VGA
 +1.8V_VGA

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Quanta Computer Inc.

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 Sheet: 14 of 44



Designator	For PARK	For Madison
MEM_CALRNP0	stuff	stuff
MEM_CALRNP1	stuff	stuff
MEM_CALRNP2	stuff	stuff

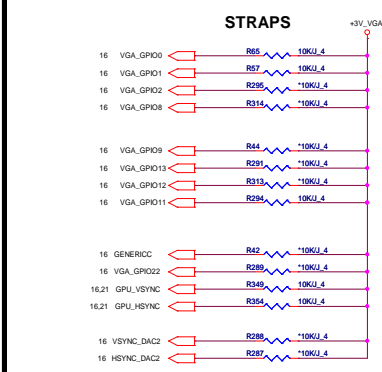
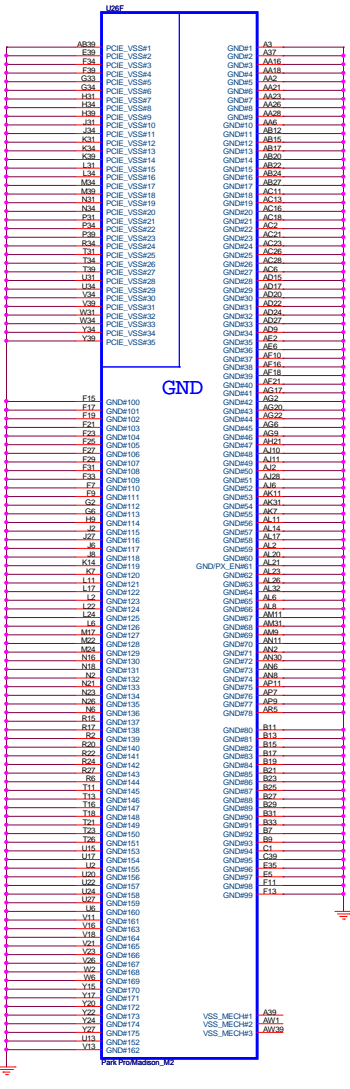
DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	For Manhattan
Ra	10K
Rb	51R
Rc	DNI
Ca	68pF

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Quanta Computer Inc.

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Memory Aperture size fix 256M

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	0
0	4G	1	1

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

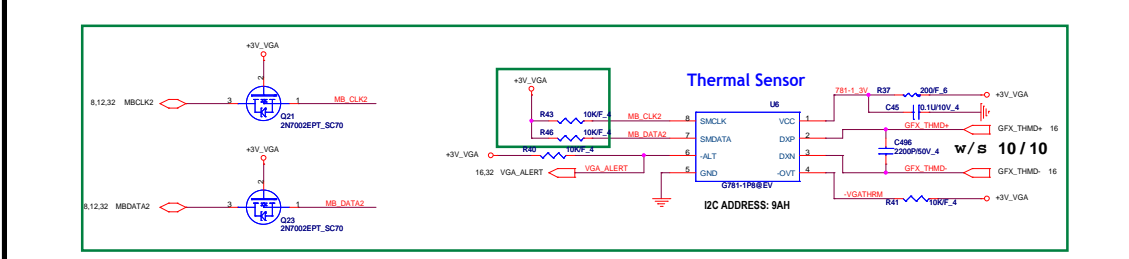
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output saving for mobile mode 1: 50% Tx output saving (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1: Advertises the PCI-E device as 3.0 GT/s capable at power-on. E: GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO 22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(S)	GPIO13-11	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD1[0] AUD0[0]	GENERIC HSYNC V2SYNC	AUD1[0] AUD0[0] 0: No audio function 1: 0 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC	GENERIC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

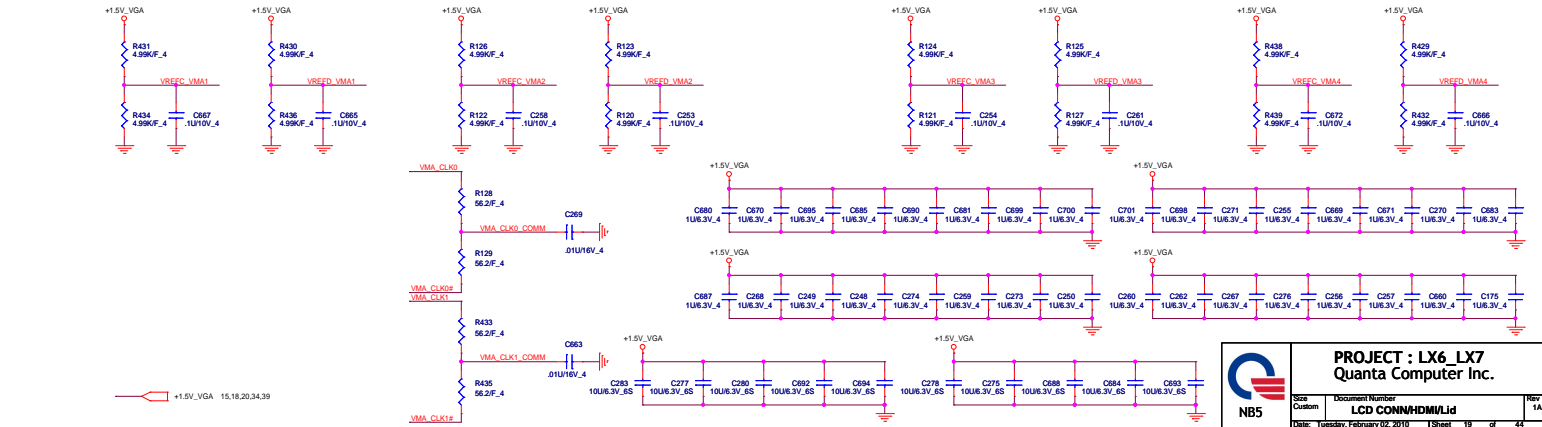
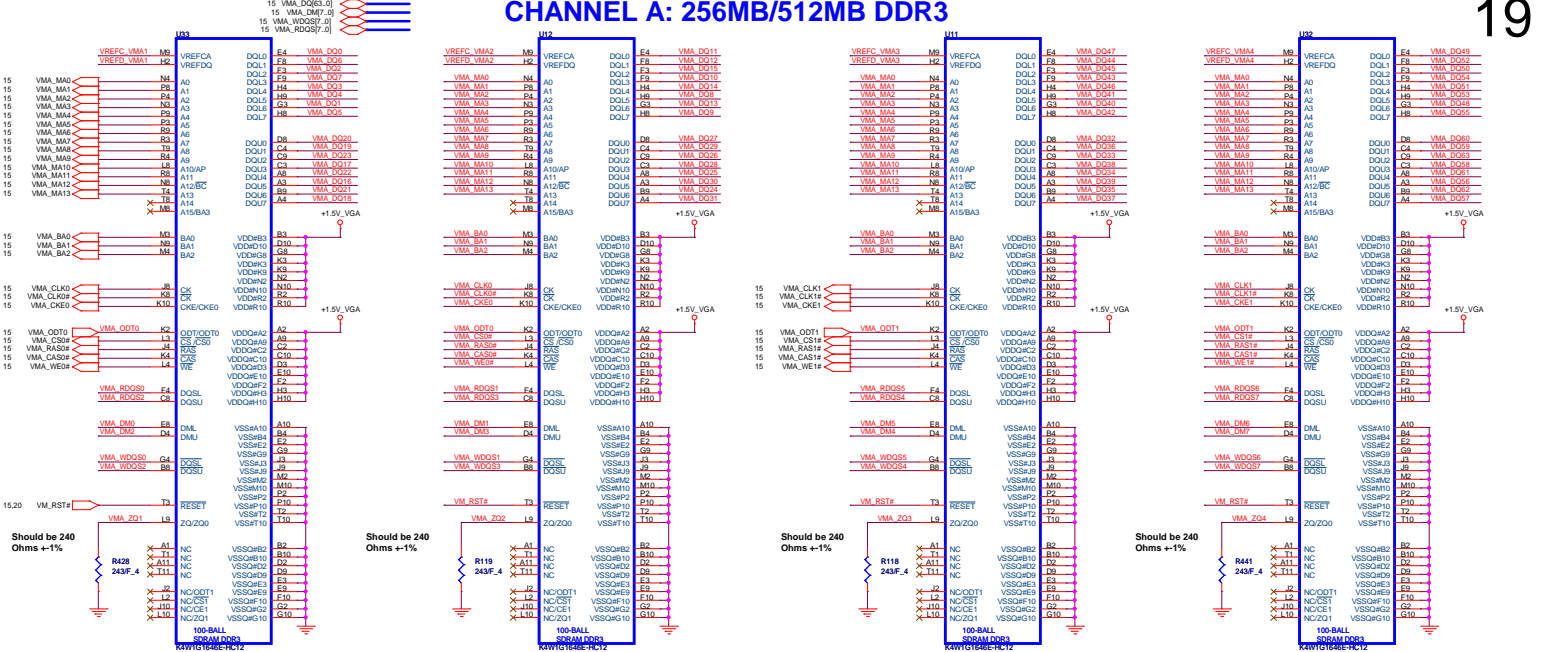
It is a shared pin strap with CONF1G[2:0] if BIOS_ROM_EN is set to 0.



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Quanta Computer Inc.

Site: Custom	Document Number: ATI M97(GND&Str&Ther)4/5	REV: 1A
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CHANNEL A: 256MB/512MB DDR3

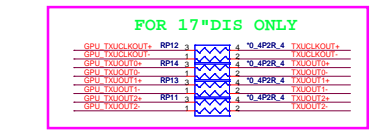
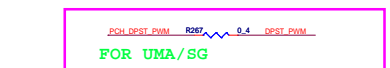
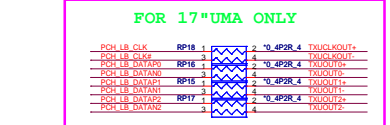
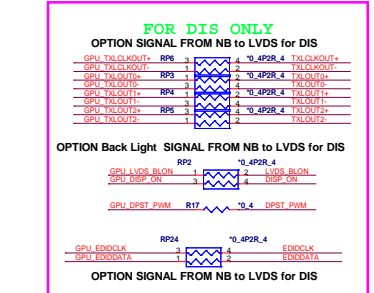
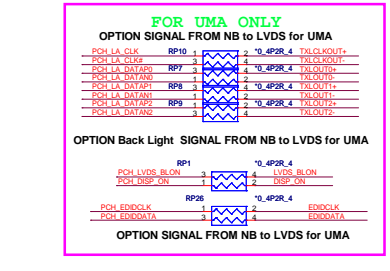
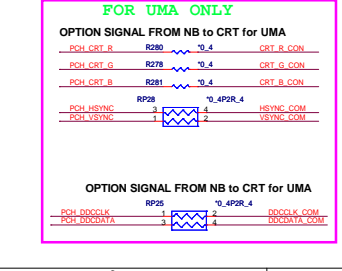
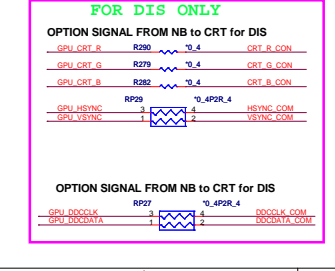
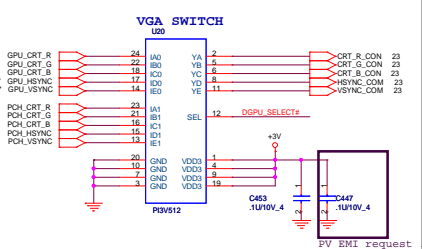
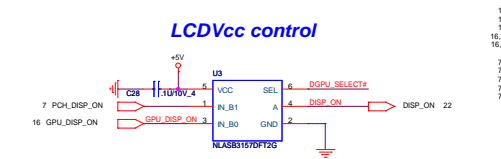
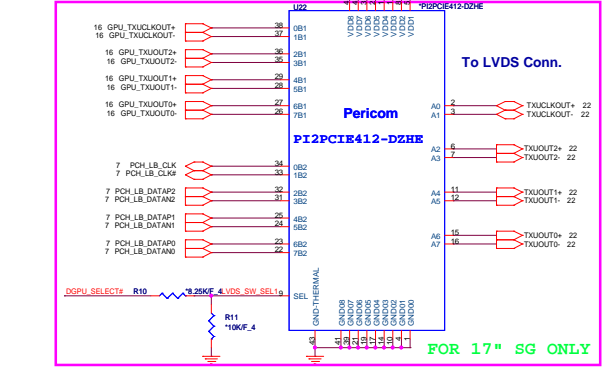
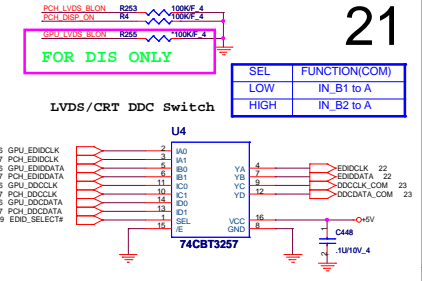
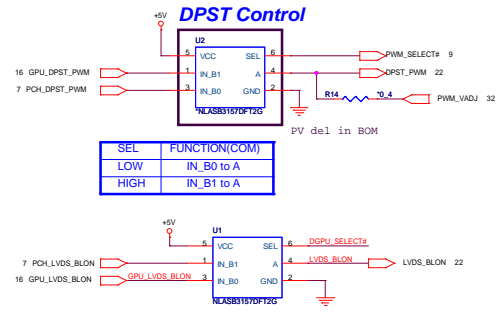
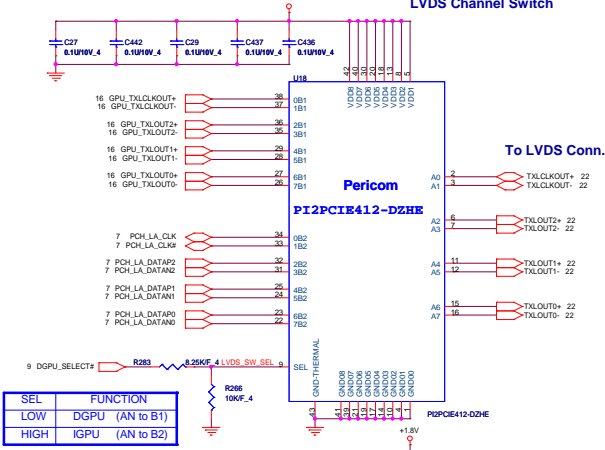


PROJECT : LX6_LX7
Quanta Computer Inc.

Doc Number: **LCD CONNHDM/19**

Date: **Issued, February 02, 2010** Sheet **19** of **44**

NB5



+3V
+5V
+1.8V

2,3,7,8,9,10,11,12,13,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41
5,10,11,36,41

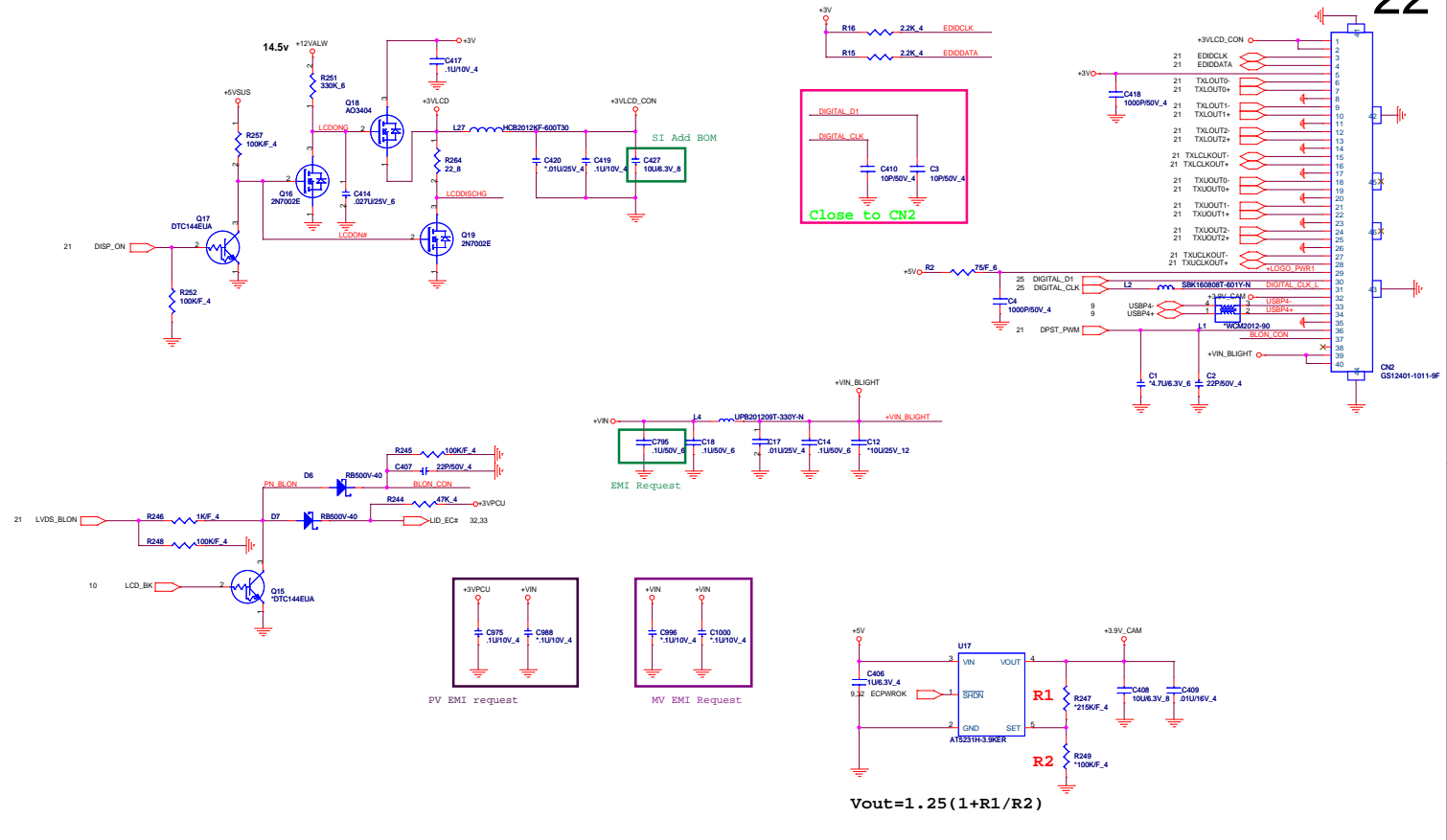
PROJECT : LX6_LX7
Quanta Computer Inc.

NB5

Doc Number: **SWITCHABLE**

Date: Tuesday, February 02, 2010 | Sheet 21 of 44

Rev 1A

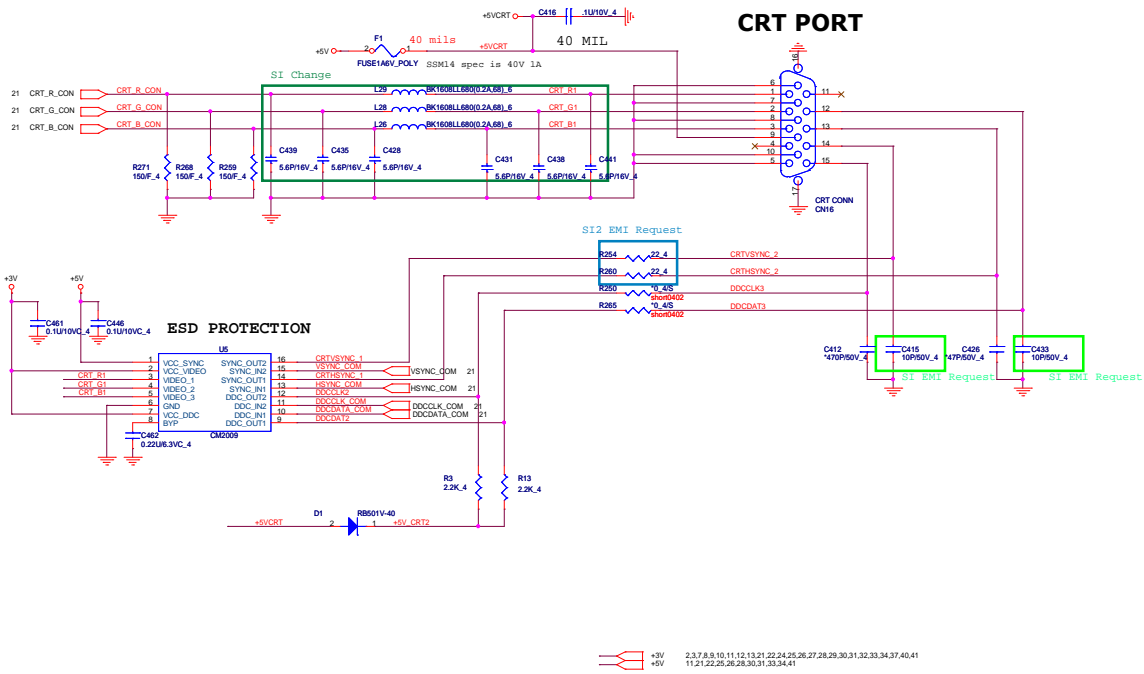


2,3,7,8,9,10,11,12,13,21,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41 +3V
 11,21,23,25,26,28,30,31,33,34,41 +5V
 27,35,36,37,39,40,41,42,43 +VIN
 7,28,32,33,34,35,36,39,41,42,43 +3VPCU
 30,34,39,41 +12VALW

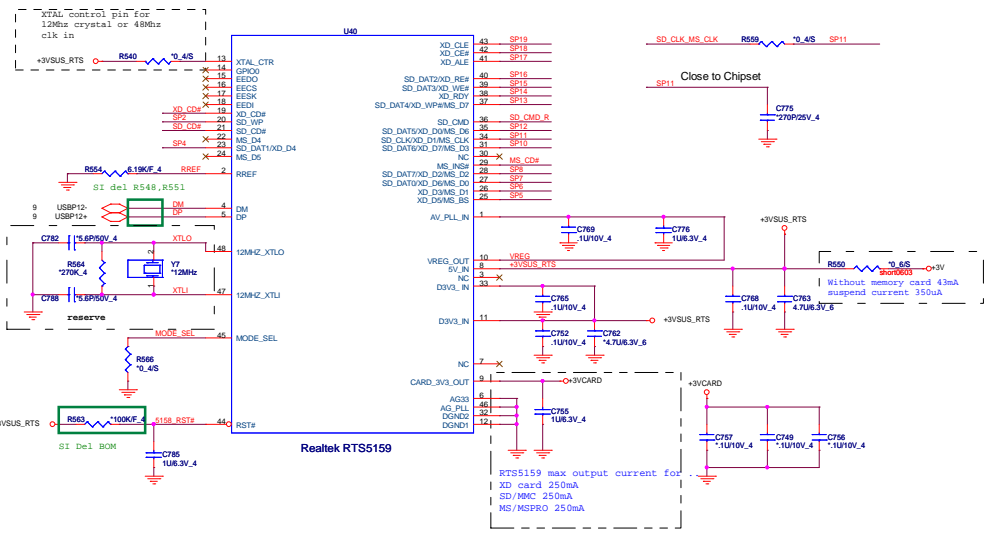
$$V_{out} = 1.25 (1 + R1/R2)$$

PROJECT : LX6_LX7
Quanta Computer Inc.

Doc No	Document Number	Rev
C1	LCD_CONN1J2 function	1A
Date	Wednesday, February 03, 2010	Sheet 22 of 44



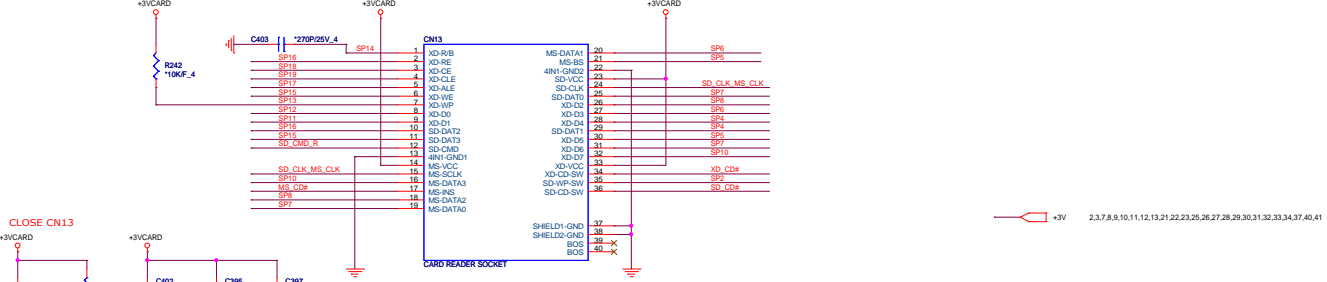
	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Ssn Custom	Document Number CRT/HDMI Conn
Date: Tuesday, February 03, 2010		Sheet 23 of 44



Note:

SP0	SD/MMC	MS	XID
SP1	SD_WP		XID_CK0
SP2	SD_CD0		XID_CK1
SP3	SD_CD1		XID_CK2
SP4	SD_CD2		XID_CK3
SP5	SD_CD3		XID_CK4
SP6	SD_CD4		XID_CK5
SP7	SD_CD5		XID_CK6
SP8	SD_CD6		XID_CK7
SP9	SD_CD7		XID_CK8
SP10	SD_CD8		XID_CK9
SP11	SD_CD9		XID_CK10
SP12	SD_CD10		XID_CK11
SP13	SD_CD11		XID_CK12
SP14	SD_CD12		XID_CK13
SP15	SD_CD13		XID_CK14
SP16	SD_CD14		XID_CK15
SP17	SD_CD15		XID_CK16
SP18	SD_CD16		XID_CK17
SP19	SD_CD17		XID_CK18
SP20	SD_CD18		XID_CK19
SP21	SD_CD19		XID_CK20
SP22	SD_CD20		XID_CK21
SP23	SD_CD21		XID_CK22
SP24	SD_CD22		XID_CK23
SP25	SD_CD23		XID_CK24
SP26	SD_CD24		XID_CK25
SP27	SD_CD25		XID_CK26
SP28	SD_CD26		XID_CK27
SP29	SD_CD27		XID_CK28
SP30	SD_CD28		XID_CK29
SP31	SD_CD29		XID_CK30
SP32	SD_CD30		XID_CK31
SP33	SD_CD31		XID_CK32
SP34	SD_CD32		XID_CK33
SP35	SD_CD33		XID_CK34
SP36	SD_CD34		XID_CK35
SP37	SD_CD35		XID_CK36
SP38	SD_CD36		XID_CK37
SP39	SD_CD37		XID_CK38
SP40	SD_CD38		XID_CK39
SP41	SD_CD39		XID_CK40

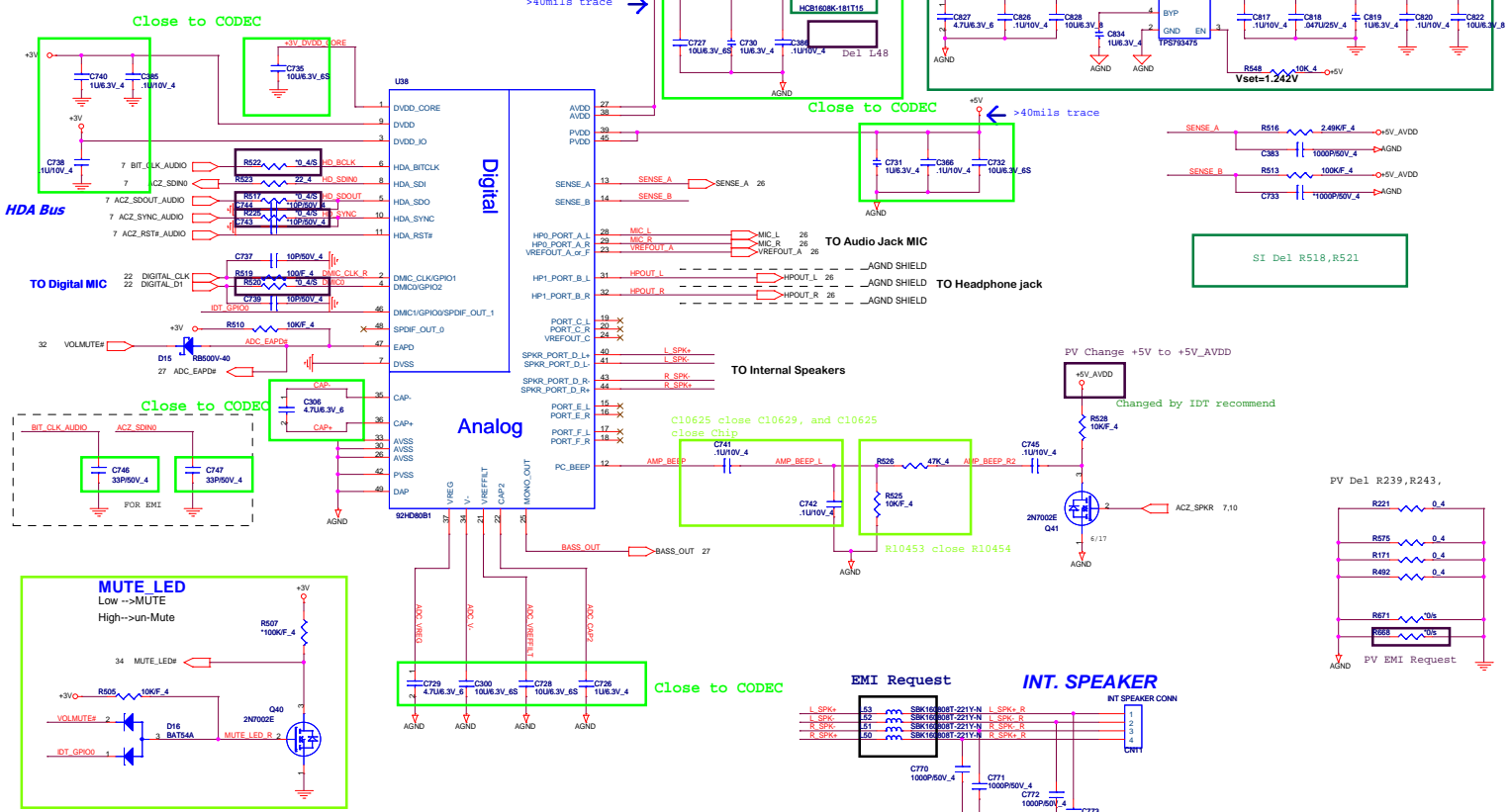
**XID, MMC/SD, MS/MSP
5 IN1 CARD READER**



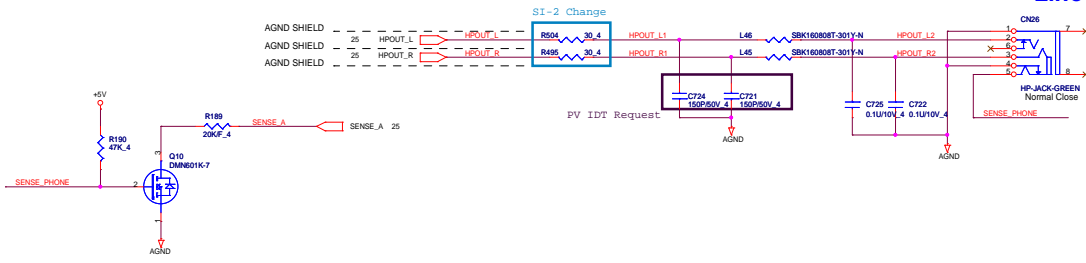
PROJECT : LX6_LX7
Quanta Computer Inc.

Doc No	RTSS159 & CR SOCKET	Rev	1A
Date	Tuesday, February 02, 2010	Sheet	31 of 44

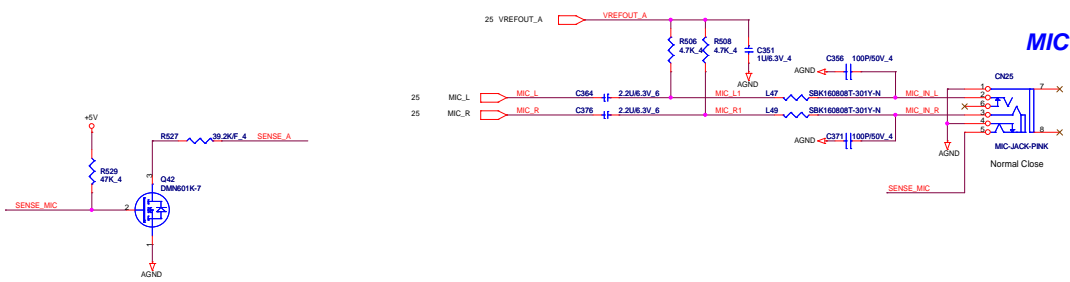
2,3,7,8,9,10,11,12,13,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40,41
27 +4.75VAVDD
11,21,22,23,26,28,30,31,33,34,41 +5V



Line out

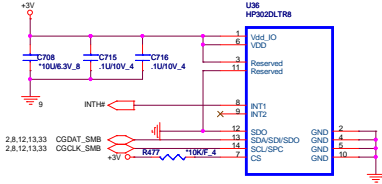


MIC



Accelerometer Sensor

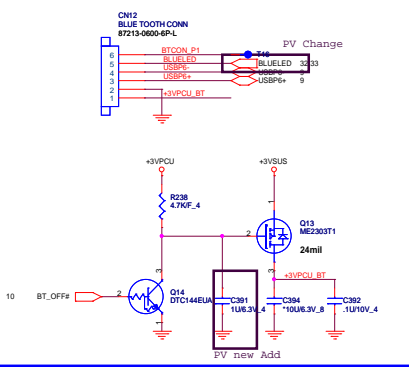
SOT-LI6302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



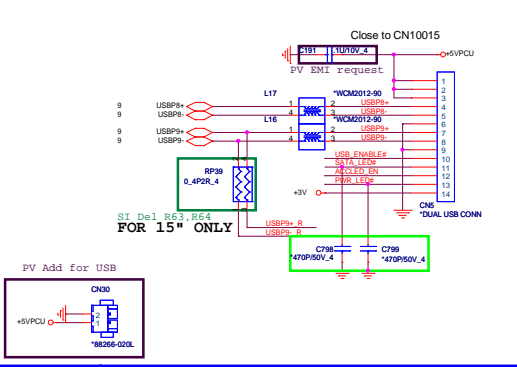
Pin 12: Low 38hex
 Pin 12: unconnected/floating 3Ahex

	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Sess Custom	Document Number Audio Jack/Accelerometer
Date: Tuesday, February 13, 2010 1:58:25		of 44

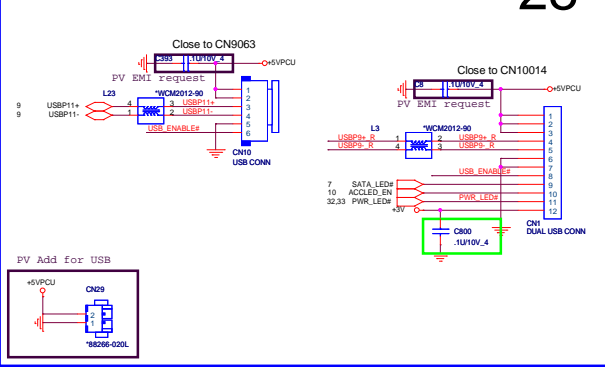
BLUETOOTH



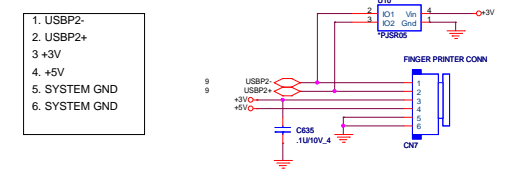
RIGHT SIDE USB2 for 17"



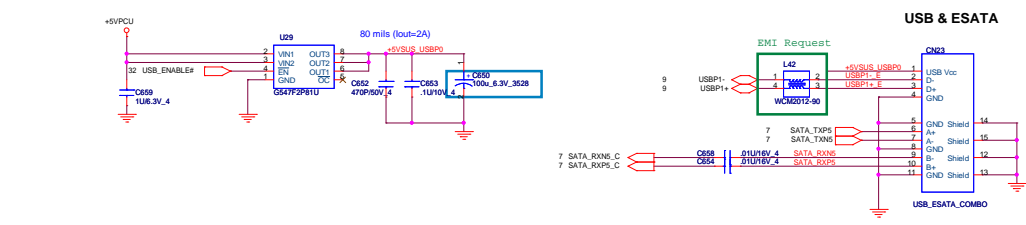
RIGHT SIDE USB for 15"



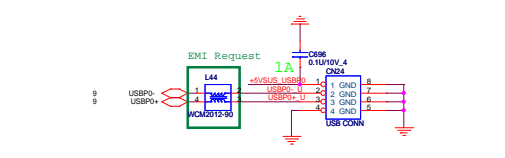
USB fingerprint CON



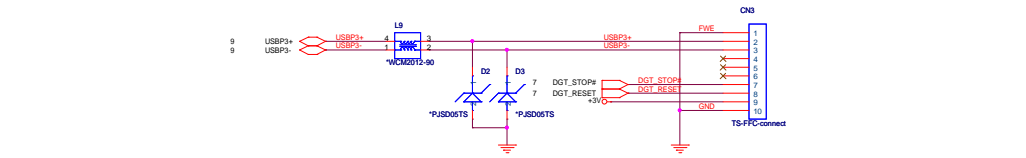
E-SATA



LEFT USB PORT



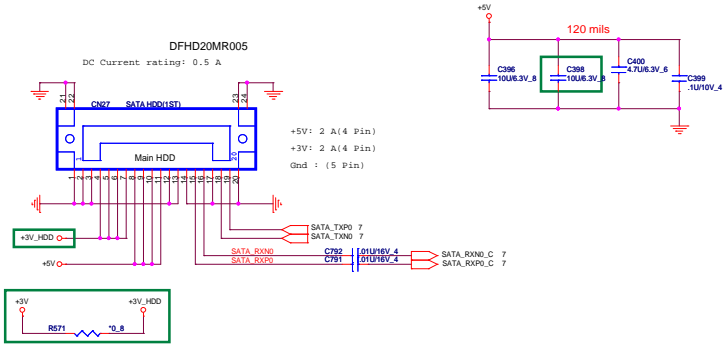
Touch screen for 15"



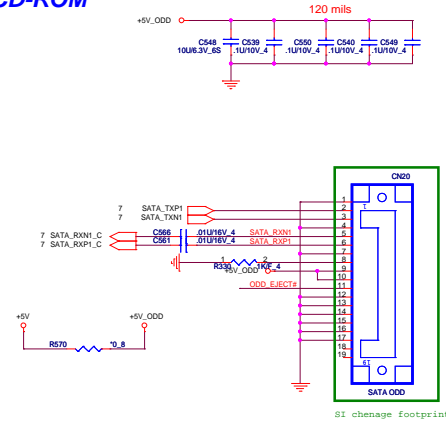
PROJECT : LX6_LX7
Quanta Computer Inc.

Site: Custom	Document Number: BT/WO/FIT/Touchscreen	Rev: 1A
Date: Tuesday, February 03, 2010	Sheet: 28	of 44

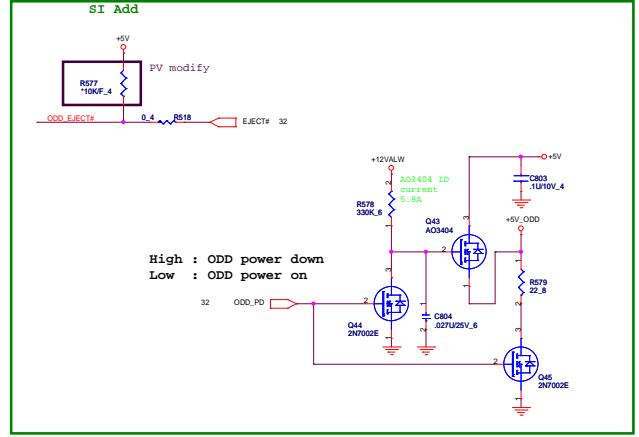
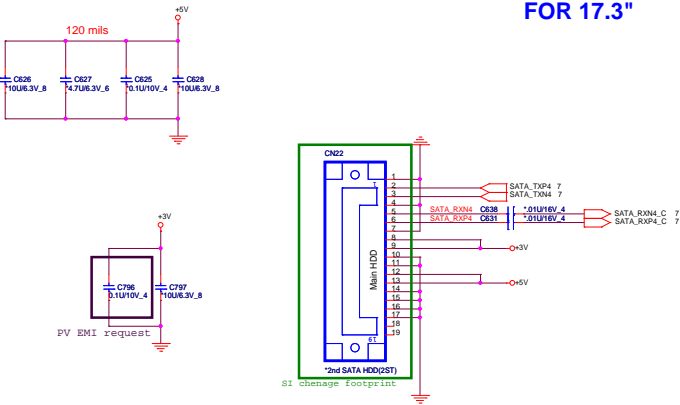
SATA HDD CONNECTOR



SATA CD-ROM

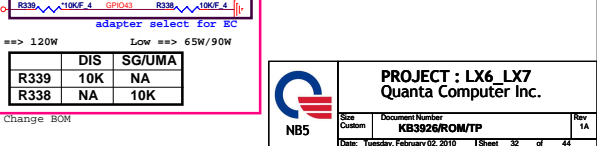
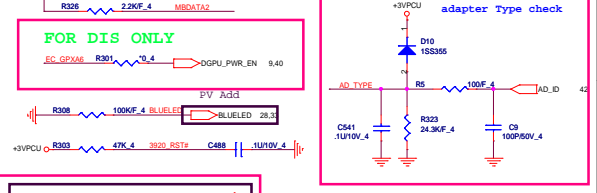
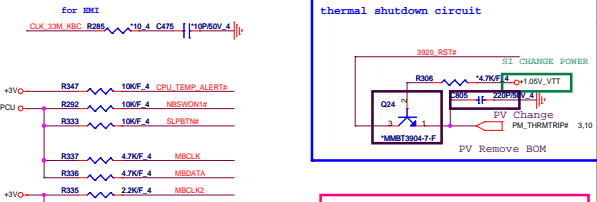
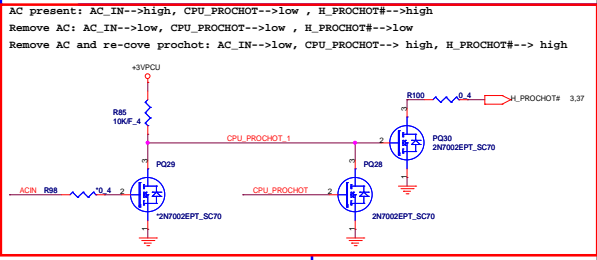
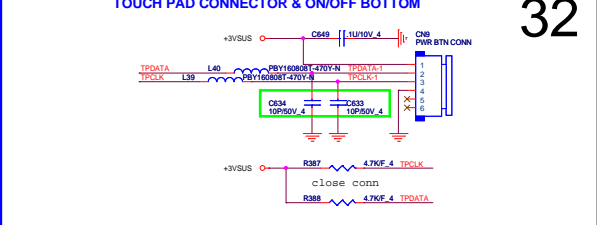
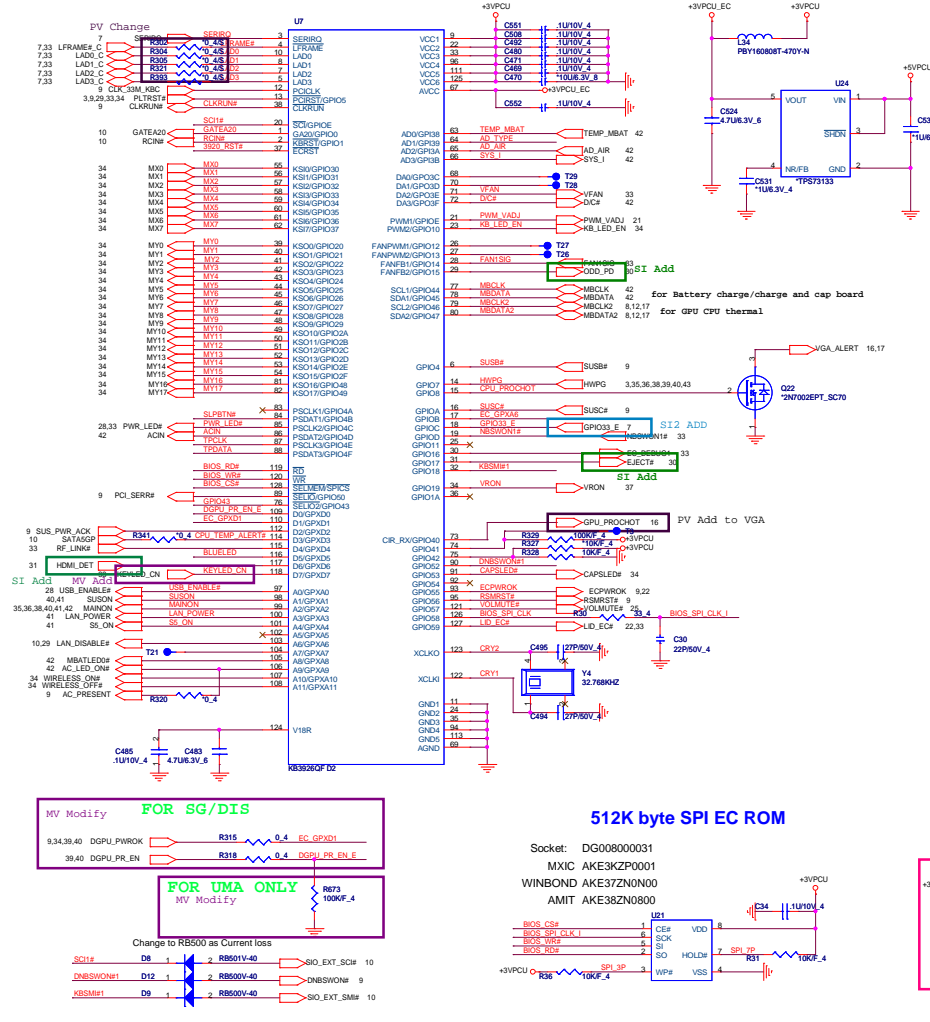


SATA_2 CONNECTOR FOR 17.3"



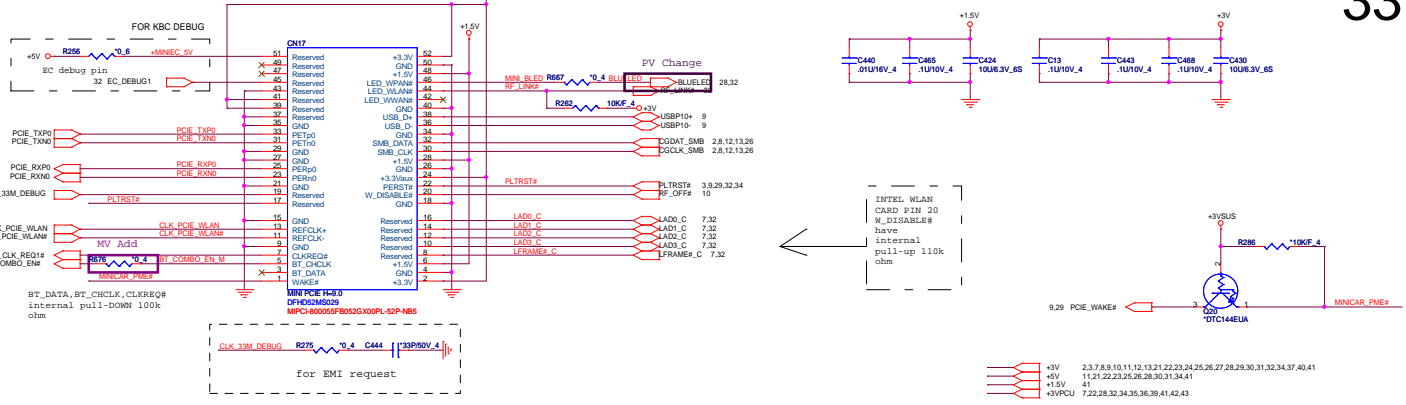
- ≡ +3V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40,41
- ≡ +5V 11,21,22,23,25,26,28,31,33,34,41
- ≡ +12VALW 22,34,39,41

	PROJECT : LX6_LX7		Rev 1A
	Quanta Computer Inc.		
	Soc Custom	Document Number ODD/HDD/ANT	
Date: Tuesday, February 03, 2010 1:58:00 PM		Sheet 30 of 44	



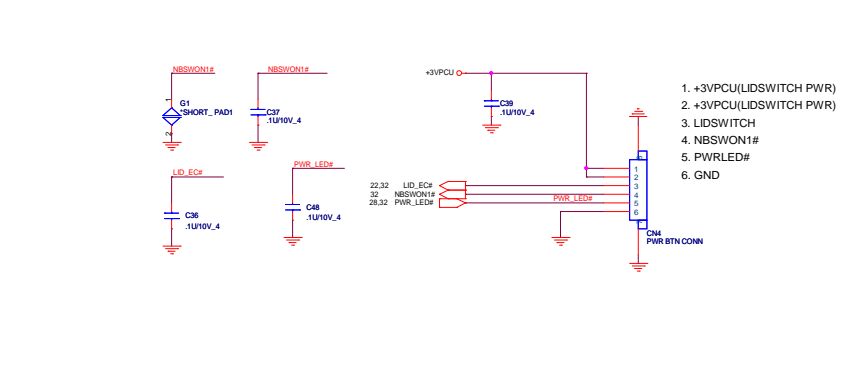
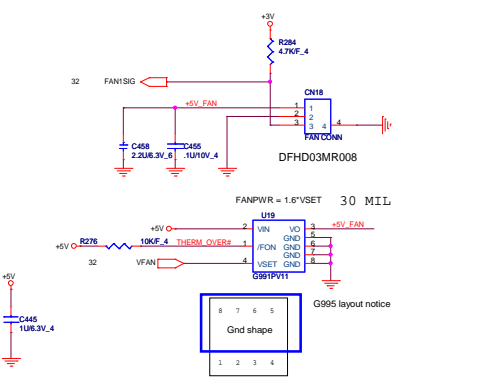
PROJECT : LX6_LX7
Quanta Computer Inc.

Doc: Monday, February 13, 2010 | Sheet 32 of 44



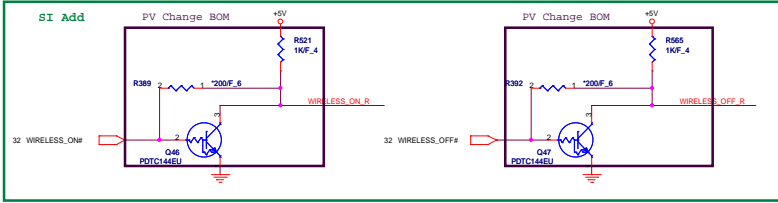
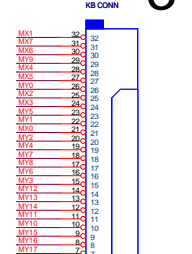
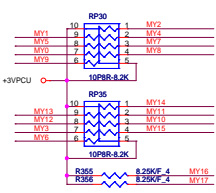
CPU FAN

POWER BOTTON CONNECT

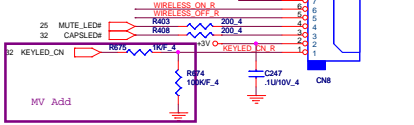


	PROJECT : LX6_LX7 Quanta Computer Inc.		Rev 1A
	Doc Title	Document Number MINI PCI-E CONN/FAN	

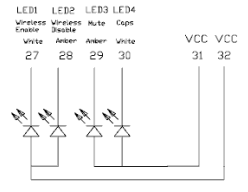
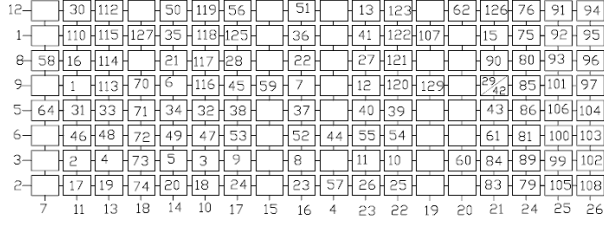
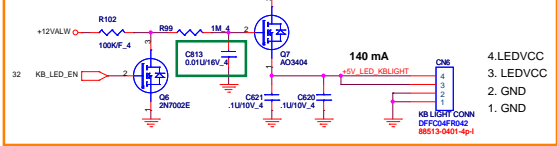
KEYBOARD PULL-UP

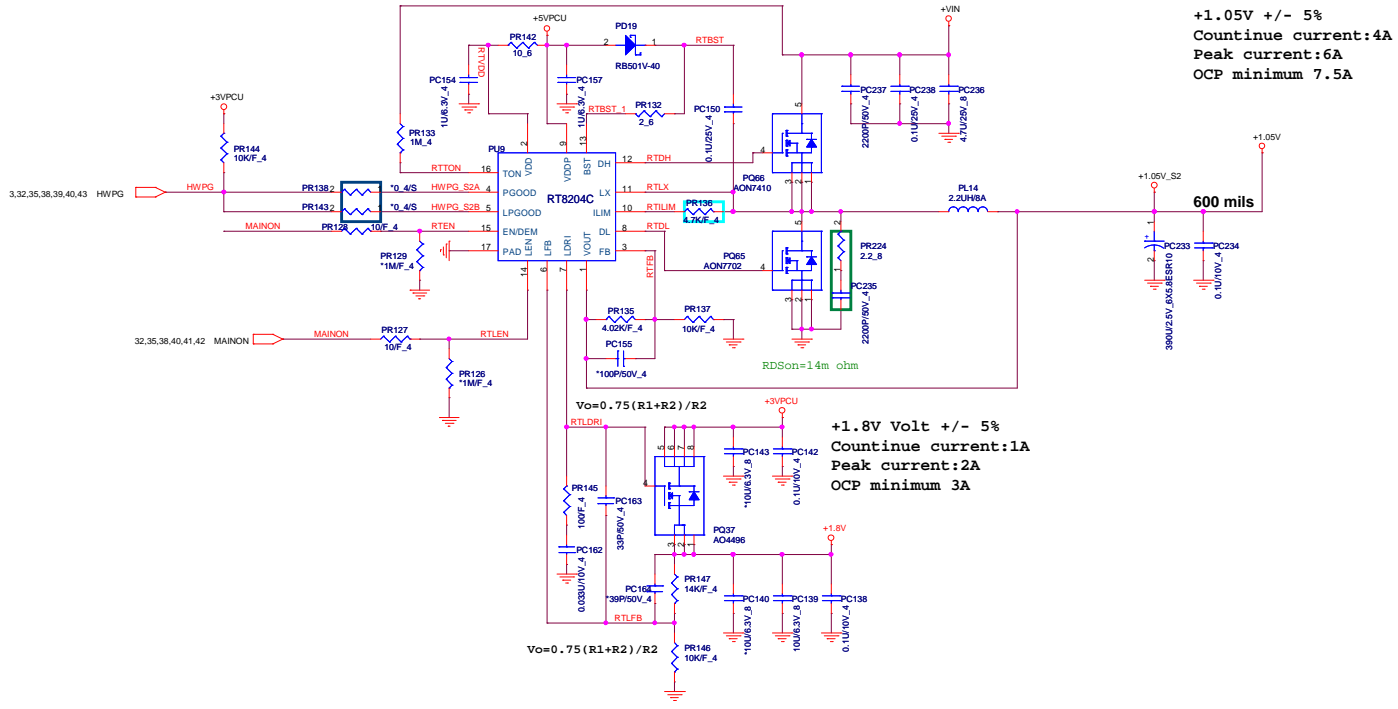


clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)



KB backlight for 15"






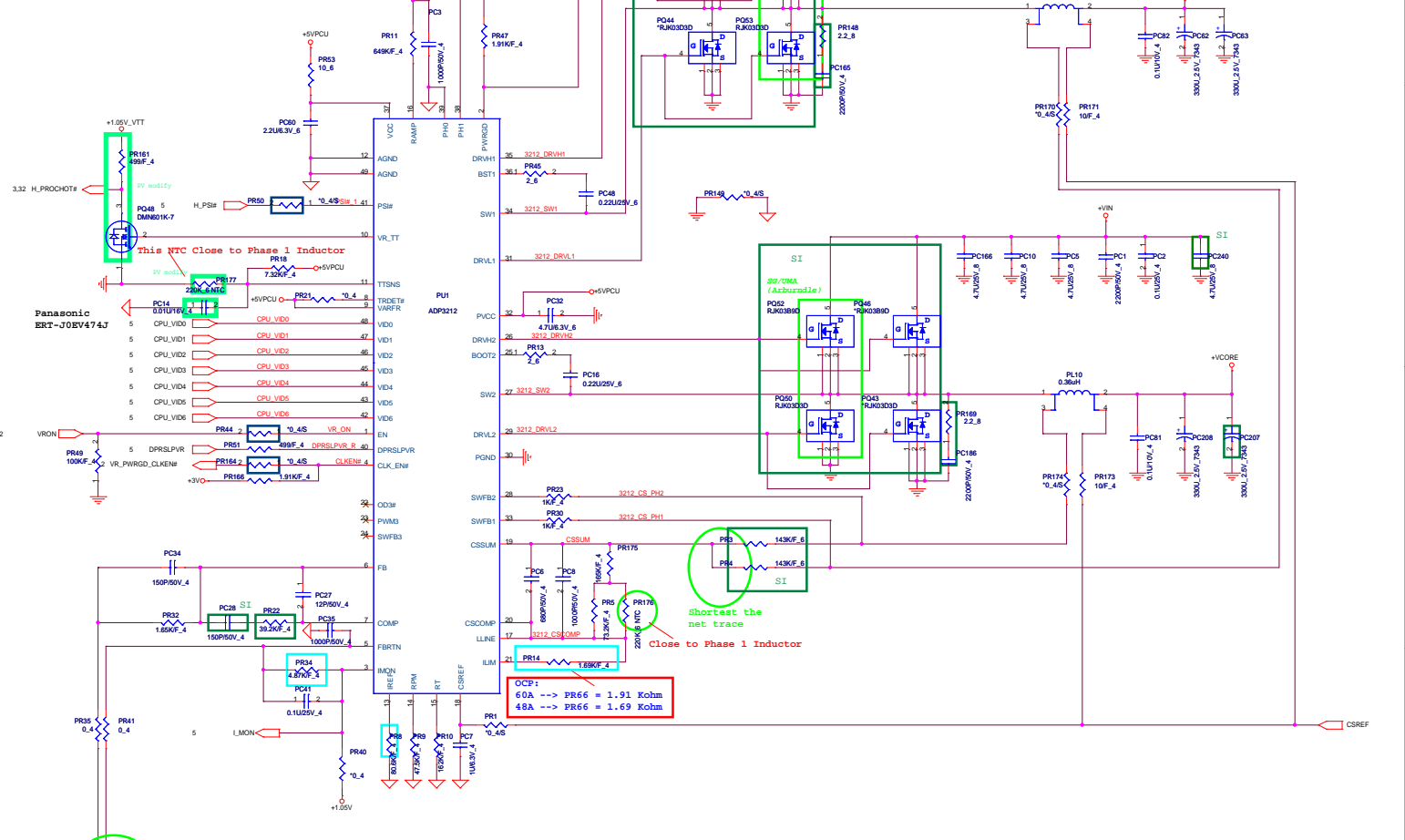
+1.05V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum 7.5A

+1.8V Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A

- +1.8V 5,10,11,21,41
- +VIN 22,27,35,37,39,40,41,42,43
- +1.05V 2,7,8,9,11,37,43
- +3VPCU 7,22,28,32,33,34,35,39,41,42,43
- +5VPCU 28,32,35,37,39,39,40,41,42,43

 NB5	PROJECT : LX6_LX7		Rev 1A
	Document Number +1.05V/+1.8V (RT8204C)		
Date: Tuesday, February 02, 2010		Sheet 36 of 44	

	DIS (Clarksfield)	SG/UMA (Arburndle)
不上件		PQ45 PQ46 PQ43 PQ44
PR14	1.91k (OCP=63A) (CS21912FB13)	1.69k (OCP=55A) (CS21692FB01)
PR34	4.7k (CS24702FB10)	4.87k (CS24872FB07)



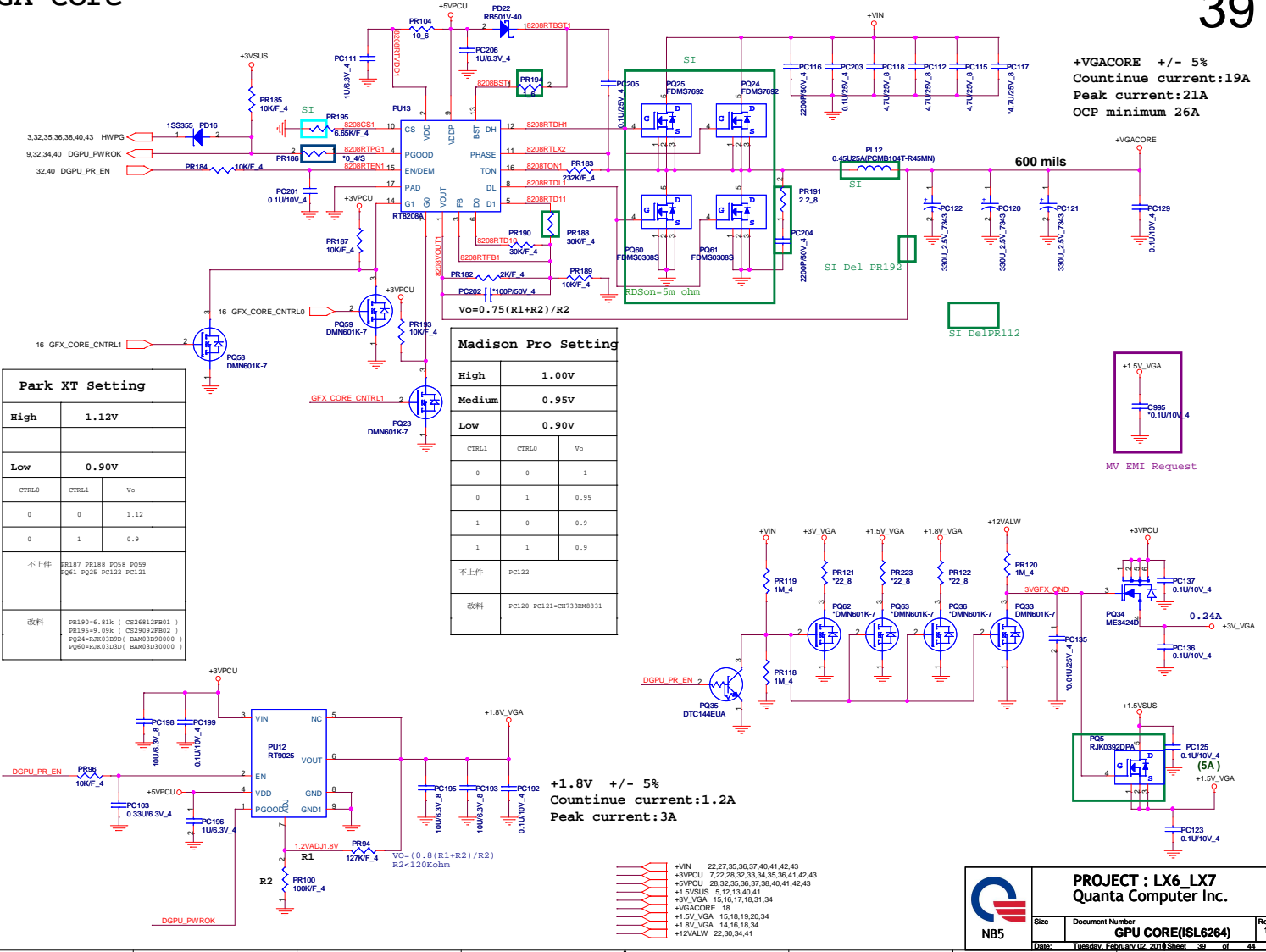
+VCORE
 Countinue current:24A
 Peak current:40A
 OCP minimum 48A

- +V 2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,40,41
- +VIN 2,27,35,36,39,40,41,42,43
- +1.05V 2,7,8,9,11,36,43
- +5VPCU 38,39,35,36,38,39,40,41,42,43
- +VCORE 5
- +1.05V_VTT 3,5,10,11,32,38,43

	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Sea Custom Document Number CPU Core (ADP3212)	Rev 1A
Date: Tuesday, February 02, 2010 13:58:37 of 44		

VGA Core

+VGACORE +/- 5%
Countinue current:19A
Peak current:21A
OCP minimum 26A

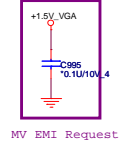


Park XT Setting

High	1.12V	
Low	0.90V	
CTRL0	CTRL1	Vo
0	0	1.12
0	1	0.9
不上件	PR187 PR188 PQ58 PQ59 PQ61 PQ25 PC122 PC121	
改料	PR190=4.81k (CS26812F801) PR191=9.09k (CS29092F802) PQ64=RT803D3D(BAK03D30000) PQ60=RT803D3D(BAK03D30000)	

Madison Pro Setting

High	1.00V	
Medium	0.95V	
Low	0.90V	
CTRL1	CTRL0	Vo
0	0	1
0	1	0.95
1	0	0.9
1	1	0.9
不上件	PC122	
改料	PC120 PC121=CH733R8831	



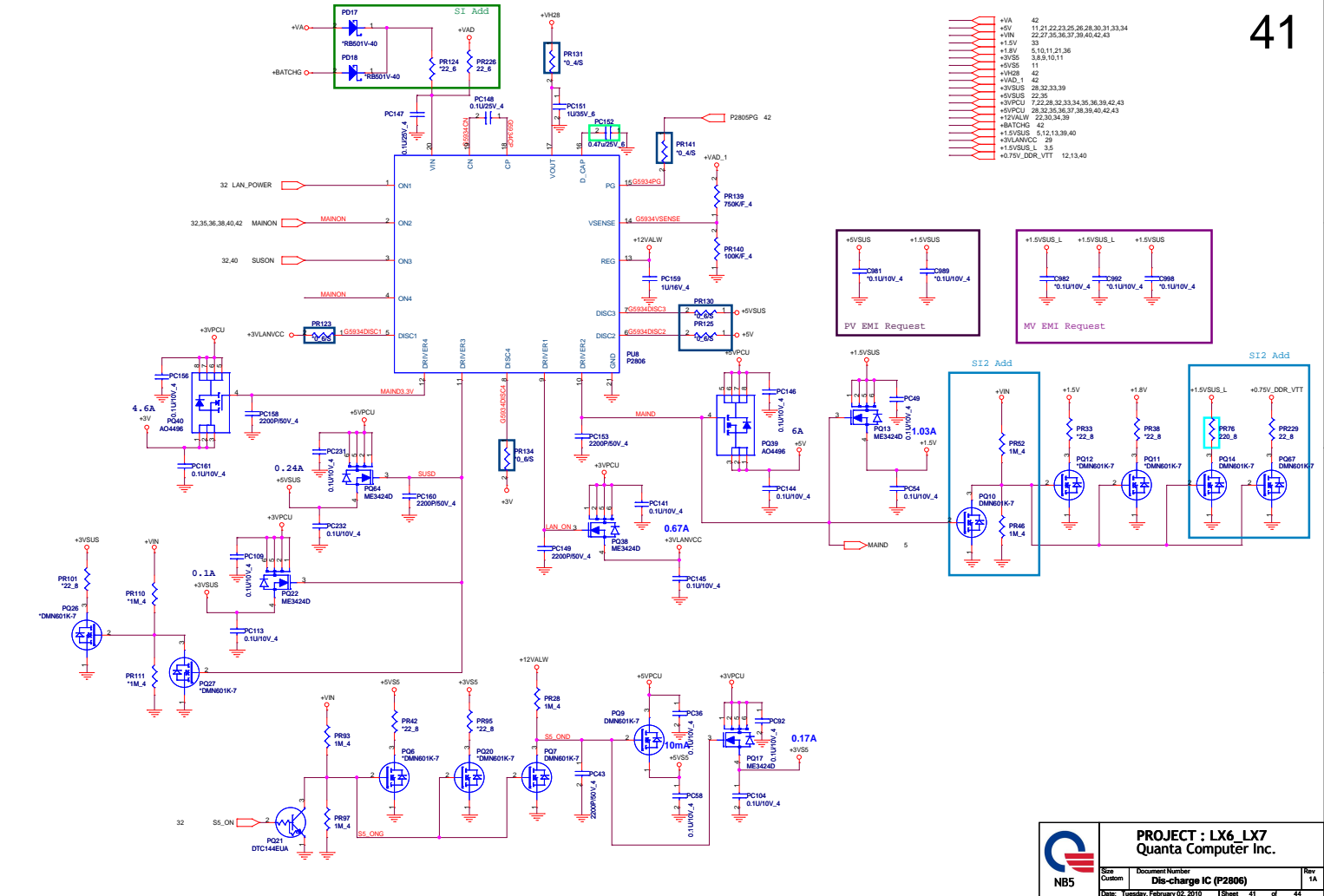
MV EMI Request

+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A

- +VIN 22,27,35,36,37,40,41,42,43
- +3VPCU 7,22,28,32,33,34,35,36,41,42,43
- +5VPCU 26,32,35,36,37,38,40,41,42,43
- +1.5V_VGA 5,12,13,40,41
- +3V_VGA 15,16,17,18,31,34
- +VGACORE 18
- +1.5V_VGA 15,18,19,20,34
- +1.8V_VGA 14,16,18,34
- +12VALW 22,30,34,41

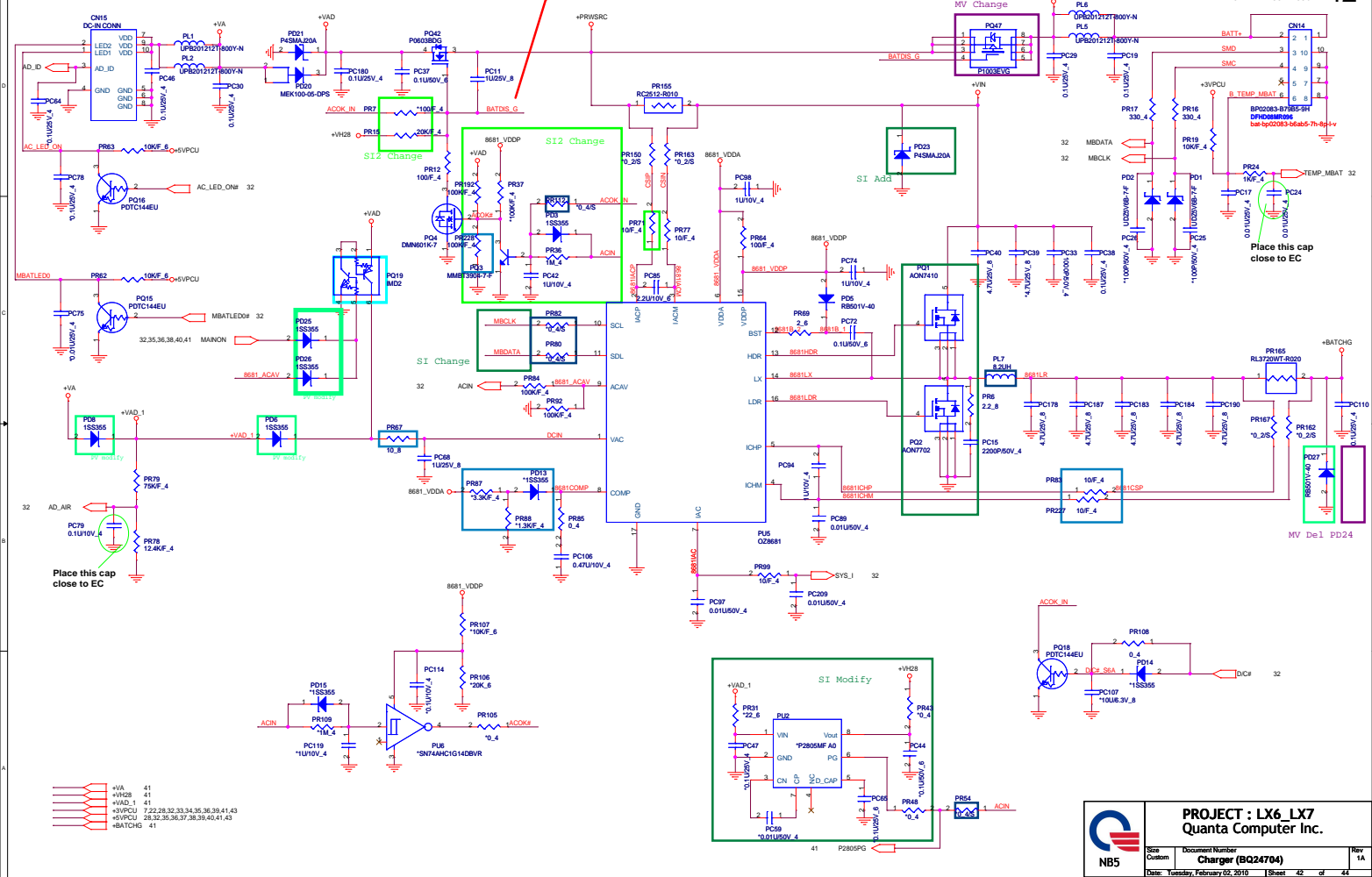
PROJECT : LX6_LX7
Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(ISL6264)	1A
Date:	Tuesday, February 02, 2011	Sheet 39 of 44

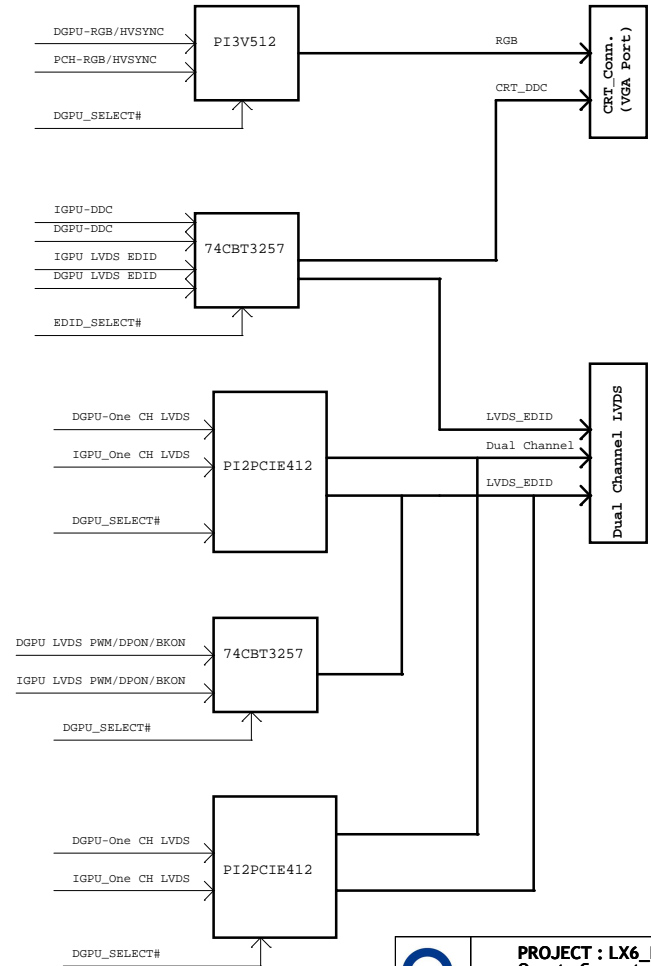
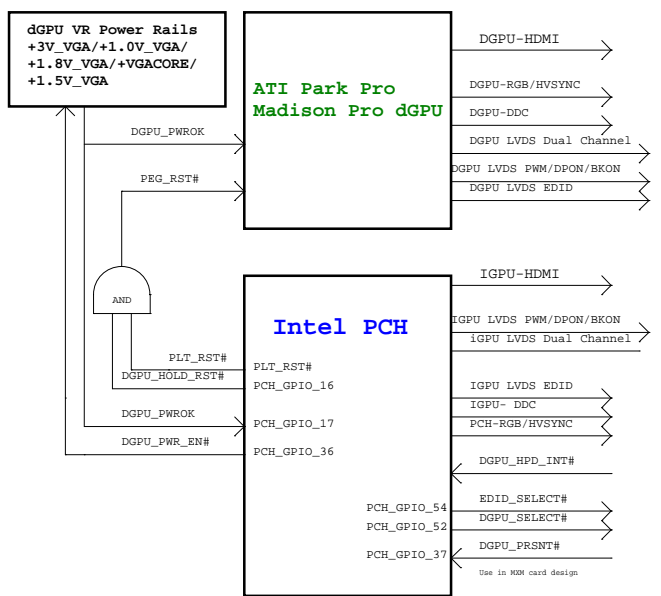


	PROJECT : LX6_LX7		
	Quanta Computer Inc.		
	Doc: Custom	Document Number: Dis-charge IC (P2806)	Rev: 1A
Date: Tuesday, February 13, 2010		Sheet: 41 of 44	

Do Not add test pad on BATDIS_G signal



	PROJECT : LX6 LX7		Rev 1A
	Quanta Computer Inc.		
	Size: Custom Document Number: Charger (BQ24704) Date: Tuesday, February 05, 2010 15:28:42	Sheet 42 of 44	



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO16	DGPU_HOLD_RST#
PCH_GPIO36	DGPU_PWR_EN#
PCH_GPIO17	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO37	DGPU_PRSENT#

PROJECT : LX6 LX7
Quanta Computer Inc.

Size Custom	Document Number Switch Blockdiagram	Rev 1A
Date: Tuesday, February 02, 2010	Sheet	44 of 44