ZZZ2
PCB
DAZ@

ZZZ1 LA-6951P DA2@
ZZZ3 LS-6951P DA2@
ZZZ4 LS-6953P DA2@
ZZZ5 LS-6955P DA2@
ZZZ6 LS-6956P DA2@
ZZZ7 LS-6957P DA2@
ZZZ8 LS-6958P DA2@

Compal Confidential

PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2011-02-24

REV:1.A

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Title: Cover Page

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

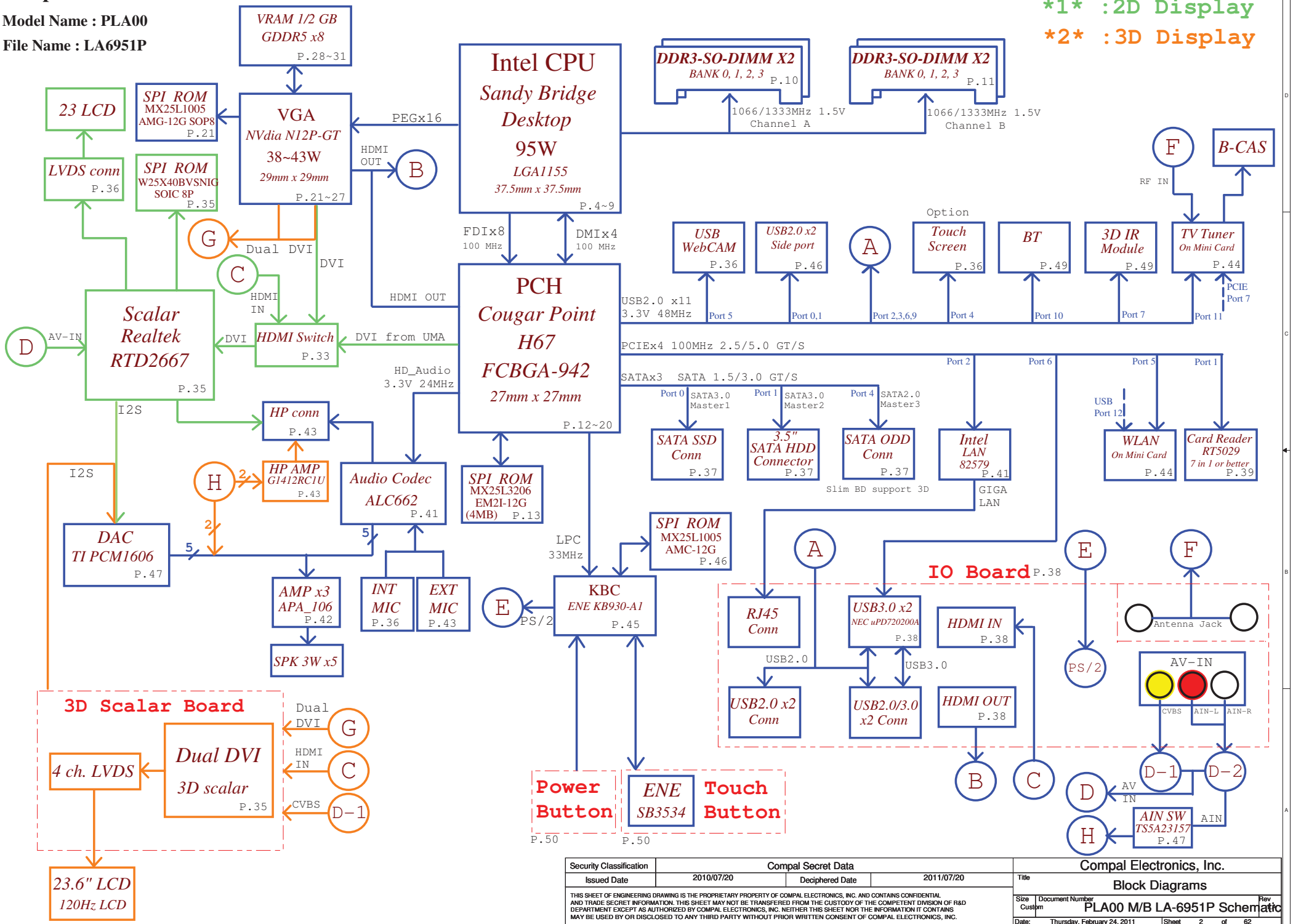
Date: Thursday, February 24, 2011 | Sheet 1 of 62

Model Name : PLA00

File Name : LA6951P

1 :2D Display

2 :3D Display



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	

Date: Thursday, February 24, 2011 Sheet 2 of 62

Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	ON	ON	OFF
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

BOARD ID Table

Board ID	Ra/Rb	Vad-bid
AV SKU	R442 100K	3.3V
NON AV SKU	R445 0 ohm	0 V

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@(VRAM:Hynix)
0	1	0	DIS@(VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
		7	3D IR
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(WLAN)
	UHCI6	12	Mini Car(TV Tuner)
		13	

BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
CRT	CRT@
PCM1606	1606@
Samsung VRAM(1G)	X76_SAM@
Hynix VRAM(1G)	X76_HYN@
Samsung VRAM(2G)	X76_SAM2G@
Hynix VRAM(2G)	X76_HYN2G@
AV-IN SKU	AV@
No AV-IN SKU	NON_AV@

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Title: Notes List

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 3 of 62

DMI_PTX_HRX_N[0..3] <14>
DMI_PTX_HRX_P[0..3] <14>
DMI_HTX_PRX_N[0..3] <14>
DMI_HTX_PRX_P[0..3] <14>

PEG_GTX_C_HRX_P[0..15] <22>
PEG_GTX_C_HRX_N[0..15] <22>
PEG_HTX_C_GRX_P[0..15] <22>
PEG_HTX_C_GRX_N[0..15] <22>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

JCPU1C SKT_H2

<REV>

PEG

PEG_GTX_C_HRX_P15	B11	PEG_RX[0]	PEG_TX[0]	C13	PEG_HTX_GRX_P15	C1	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P15
PEG_GTX_C_HRX_N15	B12	PEG_RX#[0]	PEG_TX#[0]	C14	PEG_HTX_GRX_N15	C2	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N15
PEG_GTX_C_HRX_P14	D12	PEG_RX[1]	PEG_TX[1]	E14	PEG_HTX_GRX_P14	C3	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P14
PEG_GTX_C_HRX_N14	D11	PEG_RX#[1]	PEG_TX#[1]	E13	PEG_HTX_GRX_N14	C4	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N14
PEG_GTX_C_HRX_P13	C10	PEG_RX[2]	PEG_TX[2]	G14	PEG_HTX_GRX_P13	C5	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P13
PEG_GTX_C_HRX_N13	C9	PEG_RX#[2]	PEG_TX#[2]	G13	PEG_HTX_GRX_N13	C6	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N13
PEG_GTX_C_HRX_P12	E10	PEG_RX[3]	PEG_TX[3]	F12	PEG_HTX_GRX_P12	C7	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P12
PEG_GTX_C_HRX_N12	E9	PEG_RX#[3]	PEG_TX#[3]	F11	PEG_HTX_GRX_N12	C8	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N12
PEG_GTX_C_HRX_P11	B8	PEG_RX[4]	PEG_TX[4]	J14	PEG_HTX_GRX_P11	C9	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P11
PEG_GTX_C_HRX_N11	B7	PEG_RX#[4]	PEG_TX#[4]	J13	PEG_HTX_GRX_N11	C10	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N11
PEG_GTX_C_HRX_P10	C6	PEG_RX[5]	PEG_TX[5]	D8	PEG_HTX_GRX_P10	C11	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P10
PEG_GTX_C_HRX_N10	C5	PEG_RX#[5]	PEG_TX#[5]	D7	PEG_HTX_GRX_N10	C12	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N10
PEG_GTX_C_HRX_P9	A5	PEG_RX[6]	PEG_TX[6]	D3	PEG_HTX_GRX_P9	C13	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P9
PEG_GTX_C_HRX_N9	A6	PEG_RX#[6]	PEG_TX#[6]	C3	PEG_HTX_GRX_N9	C14	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N9
PEG_GTX_C_HRX_P8	E2	PEG_RX[7]	PEG_TX[7]	E6	PEG_HTX_GRX_P8	C15	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P8
PEG_GTX_C_HRX_N8	E1	PEG_RX#[7]	PEG_TX#[7]	E5	PEG_HTX_GRX_N8	C16	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N8
PEG_GTX_C_HRX_P7	F4	PEG_RX[8]	PEG_TX[8]	F8	PEG_HTX_GRX_P7	C17	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P7
PEG_GTX_C_HRX_N7	F3	PEG_RX#[8]	PEG_TX#[8]	F7	PEG_HTX_GRX_N7	C18	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N7
PEG_GTX_C_HRX_P6	G2	PEG_RX[9]	PEG_TX[9]	G10	PEG_HTX_GRX_P6	C19	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P6
PEG_GTX_C_HRX_N6	G1	PEG_RX#[9]	PEG_TX#[9]	G9	PEG_HTX_GRX_N6	C20	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N6
PEG_GTX_C_HRX_P5	H3	PEG_RX[10]	PEG_TX[10]	G5	PEG_HTX_GRX_P5	C21	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P5
PEG_GTX_C_HRX_N5	H4	PEG_RX#[10]	PEG_TX#[10]	G6	PEG_HTX_GRX_N5	C22	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N5
PEG_GTX_C_HRX_P4	J1	PEG_RX[11]	PEG_TX[11]	K7	PEG_HTX_GRX_P4	C23	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P4
PEG_GTX_C_HRX_N4	J2	PEG_RX#[11]	PEG_TX#[11]	K8	PEG_HTX_GRX_N4	C24	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N4
PEG_GTX_C_HRX_P3	K3	PEG_RX[12]	PEG_TX[12]	J5	PEG_HTX_GRX_P3	C25	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P3
PEG_GTX_C_HRX_N3	K4	PEG_RX#[12]	PEG_TX#[12]	J6	PEG_HTX_GRX_N3	C26	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N3
PEG_GTX_C_HRX_P2	L1	PEG_RX[13]	PEG_TX[13]	M8	PEG_HTX_GRX_P2	C27	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P2
PEG_GTX_C_HRX_N2	L2	PEG_RX#[13]	PEG_TX#[13]	M7	PEG_HTX_GRX_N2	C28	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N2
PEG_GTX_C_HRX_P1	M3	PEG_RX[14]	PEG_TX[14]	L6	PEG_HTX_GRX_P1	C29	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P1
PEG_GTX_C_HRX_N1	M4	PEG_RX#[14]	PEG_TX#[14]	L5	PEG_HTX_GRX_N1	C30	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N1
PEG_GTX_C_HRX_P0	N1	PEG_RX[15]	PEG_TX[15]	N5	PEG_HTX_GRX_P0	C31	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_P0
PEG_GTX_C_HRX_N0	N2	PEG_RX#[15]	PEG_TX#[15]	N6	PEG_HTX_GRX_N0	C32	VGA@ .1U_0402_16V7K	PEG_HTX_C_GRX_N0

DMI

DMI_PTX_HRX_P0	W5	DMI_RX[0]	DMI_TX[0]	V7	DMI_HTX_PRX_P0
DMI_PTX_HRX_N0	W4	DMI_RX#[0]	DMI_TX#[0]	V6	DMI_HTX_PRX_N0
DMI_PTX_HRX_P1	V3	DMI_RX[1]	DMI_TX[1]	W7	DMI_HTX_PRX_P1
DMI_PTX_HRX_N1	V4	DMI_RX#[1]	DMI_TX#[1]	W8	DMI_HTX_PRX_N1
DMI_PTX_HRX_P2	Y3	DMI_RX[2]	DMI_TX[2]	Y6	DMI_HTX_PRX_P2
DMI_PTX_HRX_N2	Y4	DMI_RX#[2]	DMI_TX#[2]	Y7	DMI_HTX_PRX_N2
DMI_PTX_HRX_P3	AA4	DMI_RX_3	DMI_TX[3]	AA7	DMI_HTX_PRX_P3
DMI_PTX_HRX_N3	AA5	DMI_RX#[3]	DMI_TX#[3]	AA8	DMI_HTX_PRX_N3

GEN

	P3	PE_RX[0]	PE_TX[0]	P8	
	P4	PE_RX#[0]	PE_TX#[0]	P7	
	R2	PE_RX[1]	PE_TX[1]	T7	
	R1	PE_RX#[1]	PE_TX#[1]	T8	
	T4	PE_RX[2]	PE_TX[2]	R6	
	T3	PE_RX#[2]	PE_TX#[2]	R5	
	U2	PE_RX[3]	PE_TX[3]	U5	
	U1	PE_RX#[3]	PE_TX#[3]	U6	

7/20 PE_RX[0~3]/PE_RX#[0~3] only use on Workstation.

7/20 PE_TX[0~3]/PE_TX#[0~3] only use on Workstation.

+1.05VS

24.9_0402_1% 2 1 R1 PEG_IRCOMP

B5	PEG_ICOMPO	
C4	PEG_RCOMPO	
B4	PEG_ICOMPI	

LOTES_ACAZIF096P01_SANDYBRIDGE 3 OF 11 CONN@

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)

1000P_0402_50V7K @ 2 1	C1007	H_FDI_FSYNC0	
1000P_0402_50V7K @ 2 1	C1008	H_FDI_LSYNC0	
1000P_0402_50V7K @ 2 1	C1009	H_FDI_FSYNC1	
1000P_0402_50V7K @ 2 1	C1010	H_FDI_LSYNC1	
1000P_0402_50V7K @ 2 1	C1011	H_FDI_INT	

8/23 Add

H_FDI_TXN[0..7] <16>
H_FDI_TXP[0..7] <16>

JCPU1D SKT_H2

FDI_TX[0]

<16> H_FDI_FSYNC0	AC5	FDI_FSYNC_0	FDI_TX[0]	AC8	H_FDI_TXP0
<16> H_FDI_LSYNC0	AC4	FDI_LSYNC_0	FDI_TX#[0]	AC7	H_FDI_TXN0
			FDI_TX[1]	AC2	H_FDI_TXP1
			FDI_TX#[1]	AC3	H_FDI_TXN1
			FDI_TX[2]	AD2	H_FDI_TXP2
			FDI_TX#[2]	AD1	H_FDI_TXN2
			FDI_TX[3]	AD4	H_FDI_TXP3
			FDI_TX#[3]	AD3	H_FDI_TXN3
			FDI_TX[4]	AD7	H_FDI_TXP4
			FDI_TX#[4]	AD6	H_FDI_TXN4
			FDI_TX[5]	AE7	H_FDI_TXP5
			FDI_TX#[5]	AE8	H_FDI_TXN5
			FDI_TX[6]	AE3	H_FDI_TXP6
			FDI_TX#[6]	AE2	H_FDI_TXN6
			FDI_TX[7]	AG2	H_FDI_TXP7
			FDI_TX#[7]	AG1	H_FDI_TXN7
<16> H_FDI_FSYNC1	AE5	FDI_FSYNC_1			
<16> H_FDI_LSYNC1	AE4	FDI_LSYNC_1			
<16> H_FDI_INT	AG3	FDI_INT			
+1.05VS 24.9_0402_1% 2 1 R2	FDI_ICOMP	AE2	FDI_COMPIO		
		AE1	FDI_ICOMPO		

FDI LINK

LOTES_ACAZIF096P01_SANDYBRIDGE 4 OF 11 CONN@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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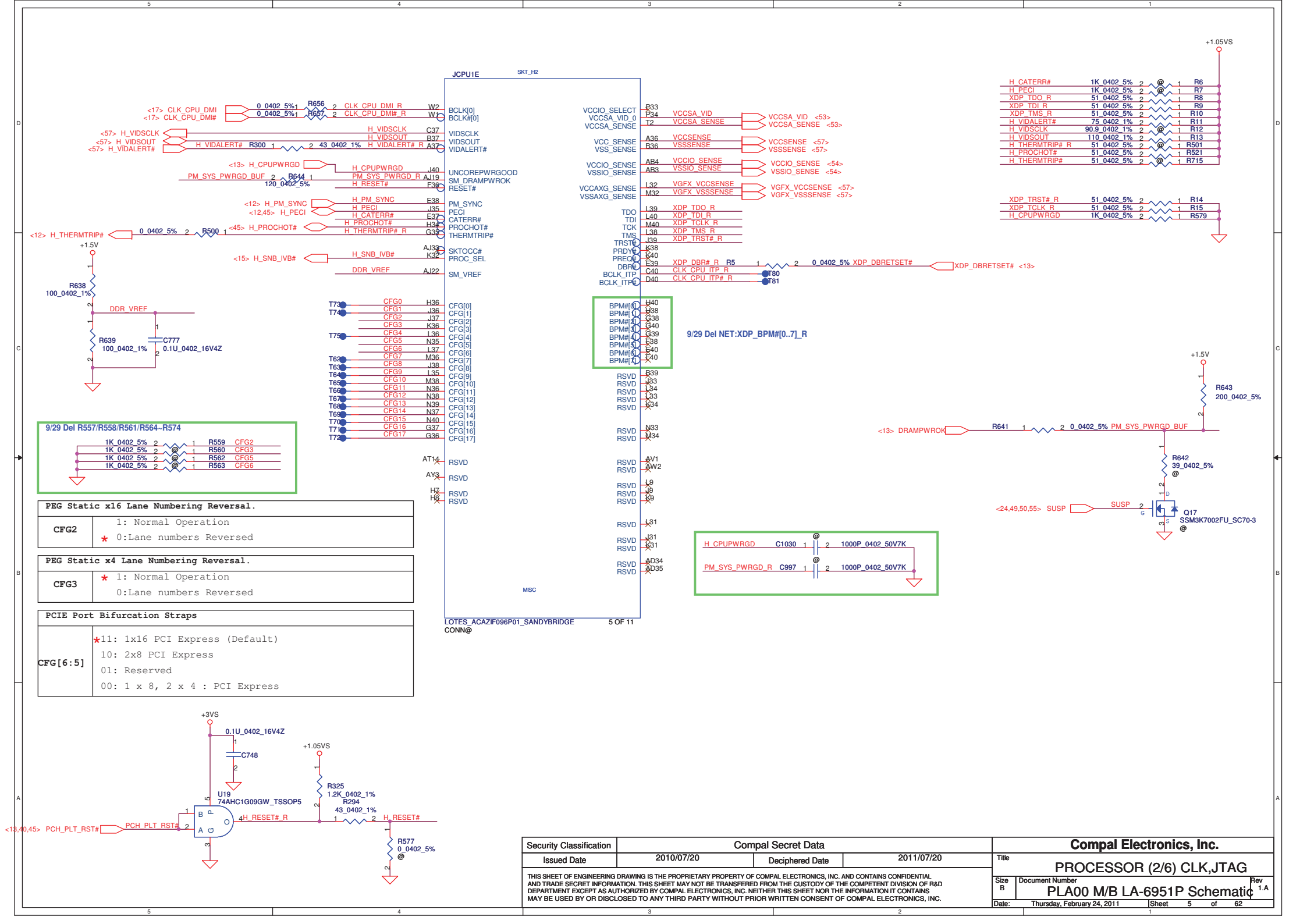
Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 Sheet 4 of 62


JCPU1E
SKT_H2
LOTES_ACAZIF096P01_SANDYBRIDGE
5 OF 11
CONN@
MISC
9/29 Del R557/R558/R561/R564~R574
9/29 Del NET:XDP_BPM#[0..7]_R
PEG Static x16 Lane Numbering Reversal.
CFG2
1: Normal Operation
* 0:Lane numbers Reversed
PEG Static x4 Lane Numbering Reversal.
CFG3
* 1: Normal Operation
0:Lane numbers Reversed
PCIE Port Bifurcation Straps
CFG[6:5]
*11: 1x16 PCI Express (Default)
10: 2x8 PCI Express
01: Reserved
00: 1 x 8, 2 x 4 : PCI Express
+1.05VS
+1.5V
+3VS
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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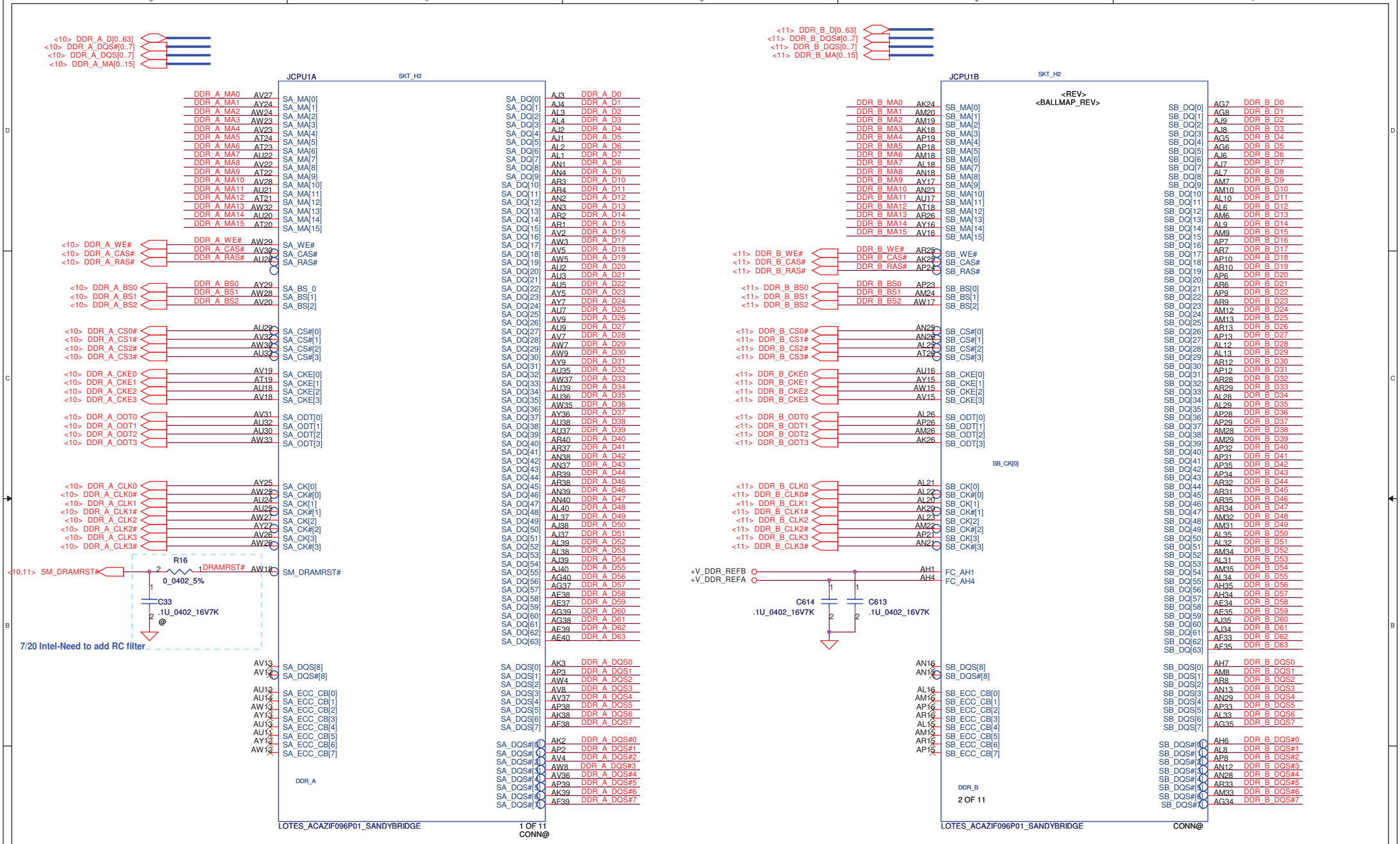
Title
PROCESSOR (2/6) CLK,JTAG
Size B
Document Number
PLA00 M/B LA-6951P Schematic
Rev 1.A
Date: Thursday, February 24, 2011
Sheet 5 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

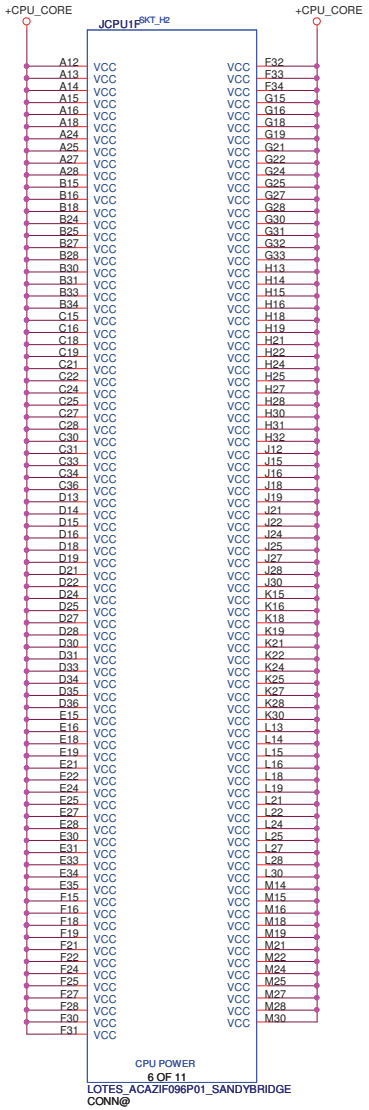
Compal Electronics, Inc.

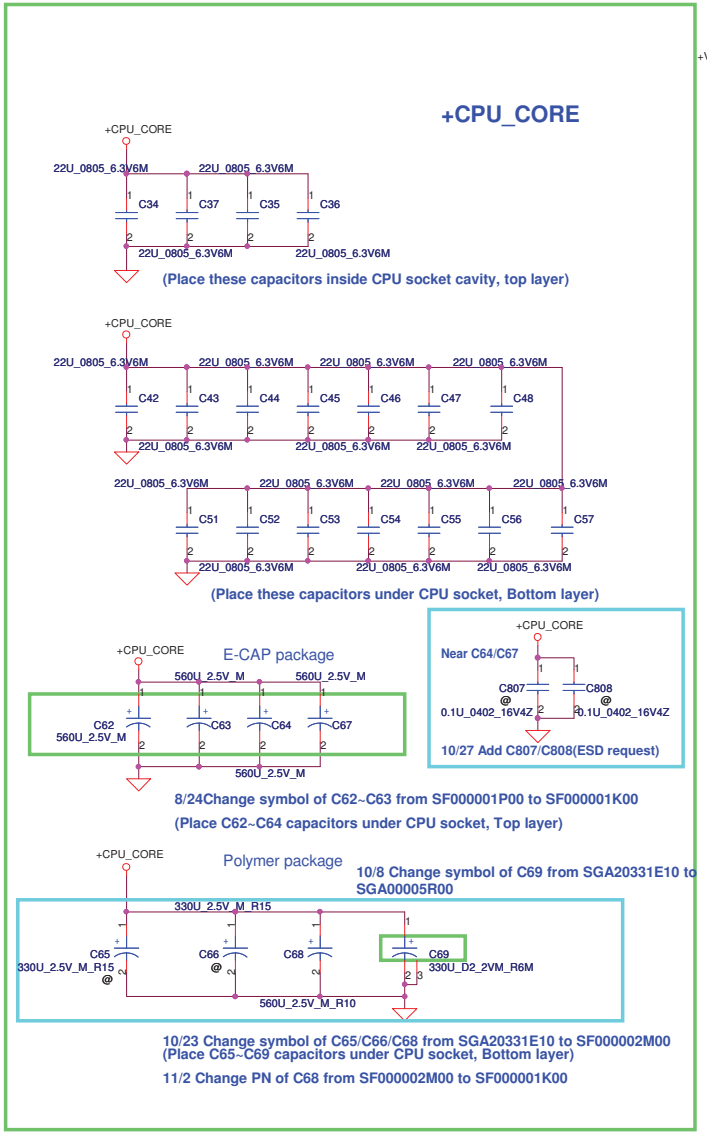
Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	1.A

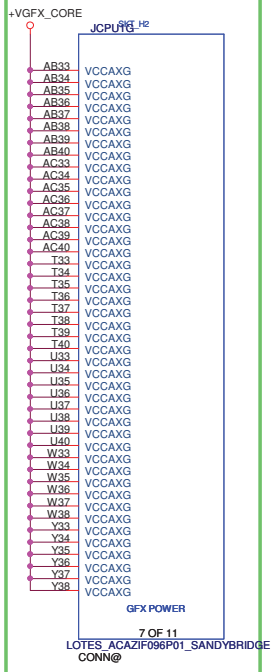
Date: Thursday, February 24, 2011 | Sheet 6 of 62

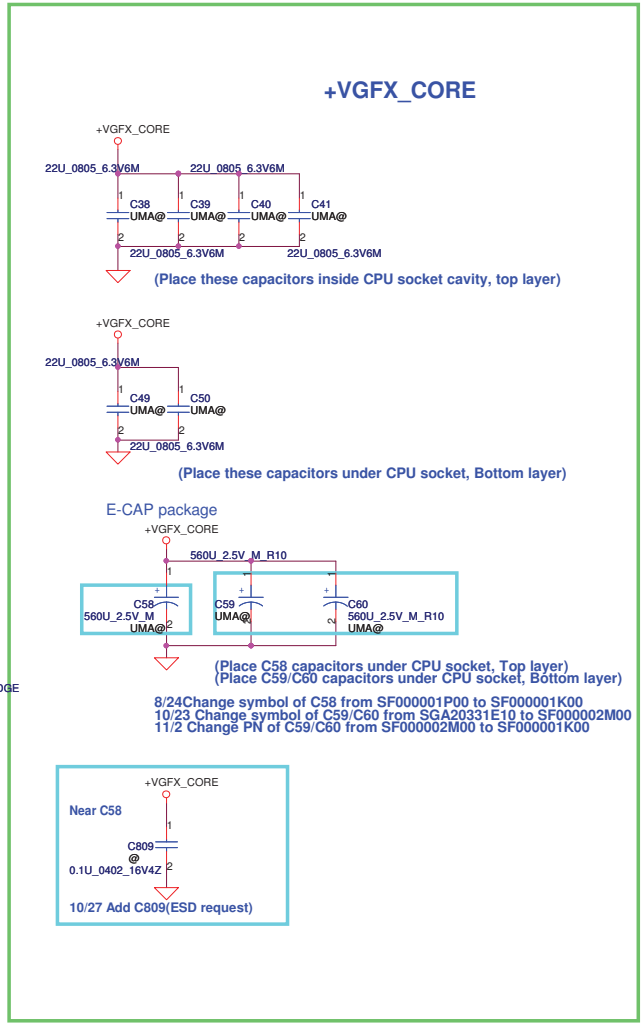
+CPU_CORE : 112A





+VGFX_CORE : 35A





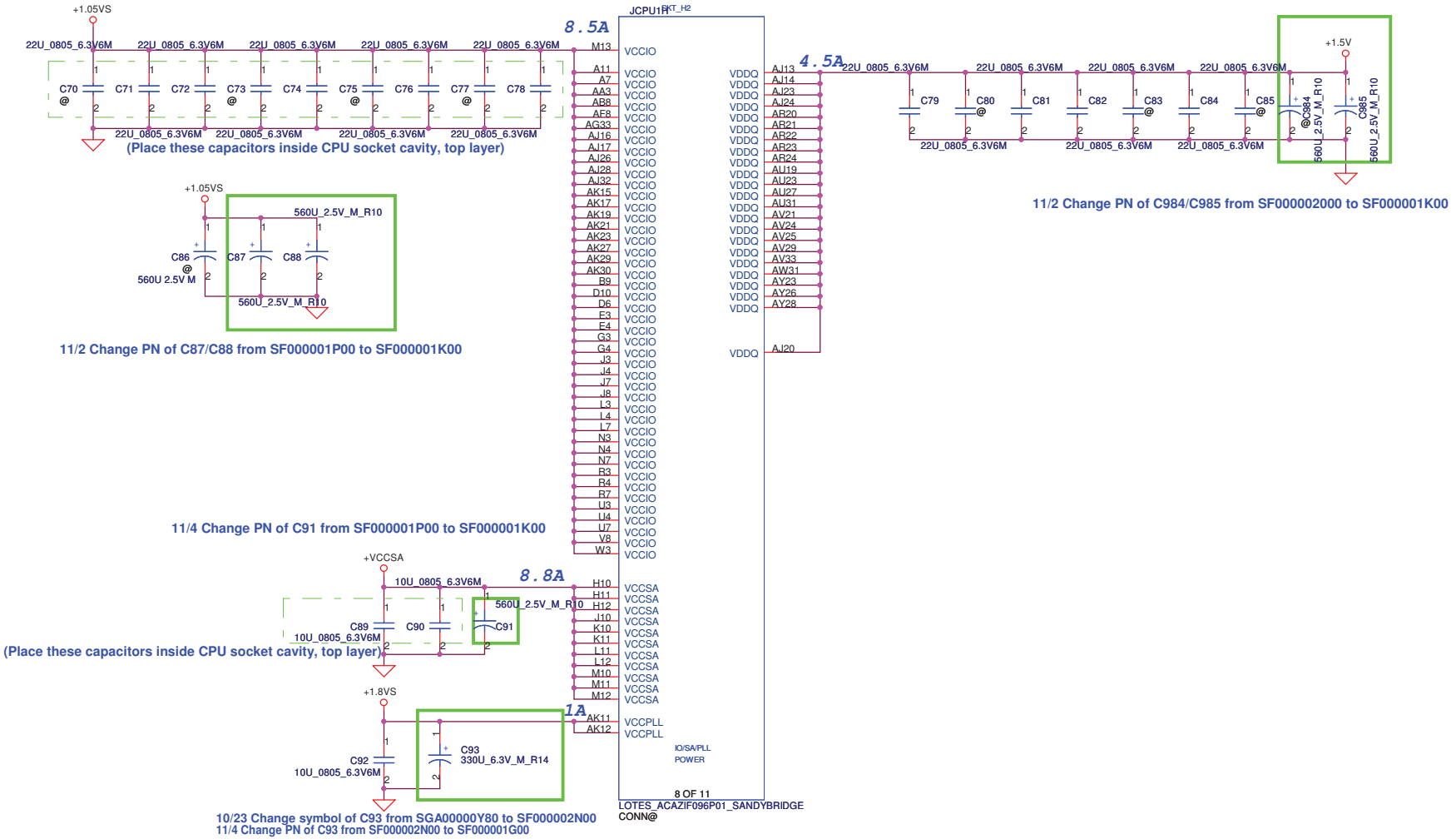
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 7 of 62



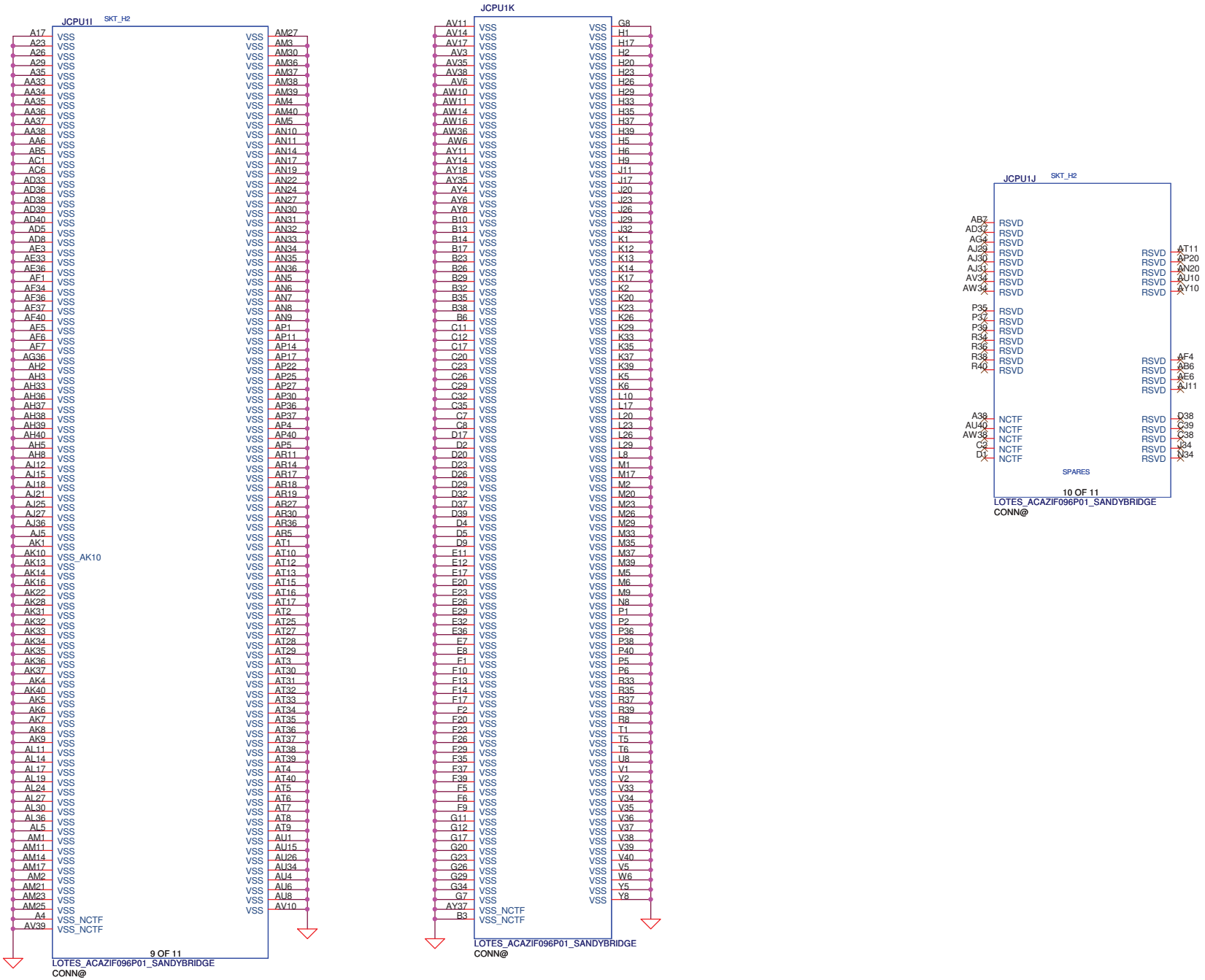
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 8 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 9 of 62

Layout Note:Place C94 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMA

Layout Note: Place near JDIMMA

10/23 Change symbol of C107 from SGA20331E10 to SF000002M00

Layout Note:Place near JDIMM1.203/204

Layout Note:Place near JDIMM2.203/204

STANDARD:9.2mm

STANDARD:5.2mm

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: DDRIII CHANNELA

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 10 of 62

Layout Note:Place C124 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMB

Layout Note: Place near JDIMMB

10/23 Change symbol of C129 from SGA20331E10 to SF000002M00
11/2 Change PN of C129 from SF000002M00 to SF000001K00

Layout Note:Place near JDIMM4.203/204

Layout Note:Place near JDIMM3.203/204

<Address: 01>

Reverse H:5.2mm

Reverse H:9.2mm

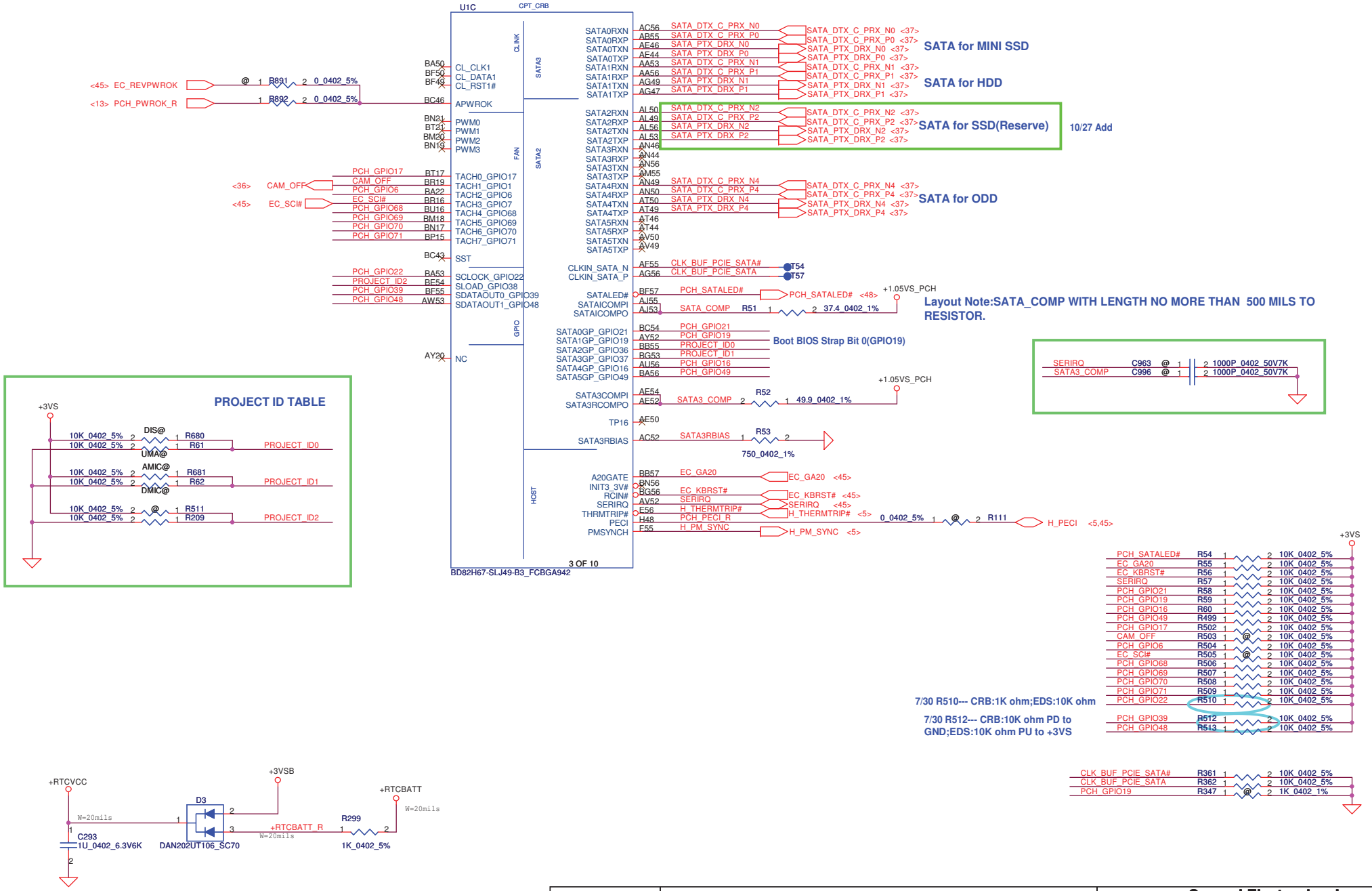
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: DDRIII CHANNELB

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 11 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (1/9) SATA,FAN

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 12 of 62

HDA for AUDIO

<41> HDA_BITCLK_AUDIO — R69 33_0402_5% — HDA_BITCLK_PCH
<41> HDA_RST#_AUDIO — R72 33_0402_5% — HDA_RST#_PCH
<41> HDA_SDOUT_AUDIO — R73 33_0402_5% — HDA_SDOUT_PCH

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
*Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
*Need to pull high for Huron River platform

<41> HDA_SYNC_AUDIO — R70 33_0402_5% — HDA_SYNC_AUDIO_R
R356 @ 1M_0402_5%

PCH_RSMRST# R303 0_0402_5% PCH_DPWROK
Stuff R303 if do not support DeepSX state
EC_PWROK R344 0_0402_5% PCH_PWROK_R

U1D

BA20	LDRQ1#_GPIO23	
BK15	FWH0_LAD0	
BJ17	FWH1_LAD1	
BJ20	FWH2_LAD2	
BG20	FWH3_LAD3	
BK17	LDRQ0#	
BG17	FWH4_LFRAME#	
BU22	HDA_BCLK	
BC22	HDA_RST#	
BD22	HDA_SDIN0	
BF22	HDA_SDIN1	
BK22	HDA_SDIN2	
BJ22	HDA_SDIN3	
BT23	HDA_SDO	
BP23	HDA_SYNC	
AU53	SPI_MOSI	
AT55	SPI_MISO	
AT57	SPI_CS0#	
AR54	SPI_CLK	
AR56	SPI_CS1#	
BR39	RTCX1	
BN39	RTCX2	
BT41	RTCRST#	
BN37	SRTCRST#	
BM38	INTRUDER#	
BJ38	PWROK	
BK38	RSMRST#	
BN41	INTVRMEN	
BT37	DPWROK	
BR42	DSWVRMEN	
BN49	SMBALERT#_GPIO11	
BT47	SMBCLK	
BR49	SMBDATA	
BU49	SML0ALERT#_GPIO60	
BT51	SML0CLK	
BM50	SML0DATA	
BR46	SML1ALERT#_PCHHOT#_GPIO74	
BJ46	SML1CLK_GPIO58	
BK46	SML1DATA_GPIO75	

4 OF 10
BD82H67-SLJ49-B3_FCBGA942

AW55	BMBUSY#_GPIO0	PCH_GPIO0
BC56	CLKRUN#_GPIO32	CLKRUN# <45>
BC25	HDA_DOCK_EN#_GPIO33	PCH_GPIO33
BL56	STP_PCI#_GPIO34	PCH_GPIO34
BJ57	GPIO35	PCH_GPIO35
BP51	GPIO8	EC_SMI# <38,45>
BK50	LAN_PHY_PWR_CTRL_GPIO12	PM_LANPHY_ENABLE <40>
BA25	HDA_DOCK_RST#_GPIO13	PCH_GPIO13
BM55	GPIO15	SMIB <38>
BP53	GPIO24_MEM_LED	T1
BJ55	GPIO28	PCH_GPIO28
BH49	SLP_LAN#_GPIO29	SLP_LAN# <40>
AV43	PCIECLKRQ2#_GPIO20	LAN_CLKREQ# <40>
BL54	PCIECLKRQ5#_GPIO44	WLAN_CLKREQ# <44>
AV44	PCIECLKRQ6#_GPIO45	CLKREQ_USB30# <38>
BP55	PCIECLKRQ7#_GPIO46	TV_CLKREQ# <44>
BT53	GPIO57	PCH_GPIO57
BJ53	SYS_PWROK	SYS_PWROK_R
BJ48	RI#	EC_SWI# <45>
BK48	PLTRST#	PCH_PLT_RST# <5,40,45>
BC44	WAKE#	PCH_PCIE_WAKE# <38,44>
BC41	SLP_A#	
BM53	SLP_S3#	PM_SLP_S3# <45>
BN52	SLP_S4#	PM_SLP_S4# <45>
BH50	SLP_S5#_GPIO63	PM_SLP_S5# <45>
BN54	SUS_STAT#_GPIO61	T2
BA47	SUSCLK_GPIO62	PCH_SUSCLK_R
AV46	BATLOW#_GPIO72	PCH_GPIO72
BP45	SUSACK#	SUS_PWR_ACK_R
BU46	SUSWARN#-SUS_PWR_DN_ACK-GPIO30	SUSWARN#_R
BG46	DRAMPWROK	DRAMPWROK <5>
BJ43	GPIO27	PCH_GPIO27
BG43	GPIO31	PCH_GPIO31
BD43	SLP_SUS#	T51
BT43	PWRBTN#	PBTN_OUT# <45>
BE52	SYS_RESET#	XDP_DBRETSET# <5>
BE56	SPKR	PCH_SPKR <41>
D53	PROCPWRGD	H_CPUPWRGD <5>
BC49	TP12	PCH_JTAG_RST#
BA43	JTAG_TCK	PCH_JTAG_TCK
BC52	JTAG_TDI	PCH_JTAG_TDI
BF47	JTAG_TDO	PCH_JTAG_TDO
BC50	JTAG_TMS	PCH_JTAG_TMS

+3VALW

EC_SMI#	R324	10K_0402_5%
EC_SWI#	R74	10K_0402_5%
PCH_GPIO74	R75	10K_0402_5%
PCH_SML1CLK	R63	4.7K_0402_5%
PCH_SML1DAT	R76	4.7K_0402_5%
LAN_SMBCLK	R64	2.2K_0402_5%
LAN_SMBDATA	R65	2.2K_0402_5%
PCH_GPIO60	R77	2.2K_0402_5%
PM_LANPHY_ENABLE	R66	10K_0402_5%
SMIB	R67	10K_0402_5%
PCH_GPIO28	R68	1K_0402_1%
PCH_GPIO13	R896	10K_0402_5%
SUSWARN#_R	R448	10K_0402_5%
PCH_GPIO57	R71	10K_0402_5%
PCH_GPIO27	R78	10K_0402_5%
WLAN_CLKREQ#	R530	10K_0402_5%
CLKREQ_USB30#	R531	10K_0402_5%
TV_CLKREQ#	R532	10K_0402_5%
DRAMPWROK	R646	200_0402_5%
PCH_GPIO31	R675	10K_0402_5%
PCH_GPIO72	R676	200_0402_5%
PCH_PCIE_WAKE#_R	R203	1K_0402_1%
PCH_GPIO11	R716	10K_0402_5%

SUS_PWR_ACK_R R391 0_0402_5% SUSWARN#_R
Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit

PCH_GPIO33	R894	10K_0402_5%
PCH_GPIO0	R82	10K_0402_5%
PCH_GPIO34	R84	10K_0402_5%
LAN_CLKREQ#	R529	10K_0402_5%
XDP_DBRETSET#	R581	10K_0402_5%
PCH_SPKR	R583	1K_0402_5%

PCH_SPKR:HIGH= Enable (No Reboot);
* LOW= Disable(Default)

CLKRUN#	R926	10K_0402_5%
SLP_LAN#	R897	1K_0402_1%
PCH_GPIO33	R895	1K_0402_1%
SYS_PWROK	R719	10K_0402_5%
PCH_GPIO35	R85	2.2K_0402_5%
EC_SMI#	R86	1K_0402_1%
SUSWARN#_R	R207	1K_0402_1%
EC_PWROK	R718	10K_0402_5%
PCH_GPIO28	R340	1K_0402_1%

* On-Die PLL Voltage Regulator
H: Enable
L: Disable

XDP_DBRETSET# C676 0.1U_0402_16V4Z <EMI>
8/13 Add C676 close to U1(EMI request)

8/20 Add
1000P_0402_50V7K C987 LAN_CLKREQ#
1000P_0402_50V7K C988 PCH_JTAG_TDO

C146 18P_0402_50V8J
X1 32.768KHZ_12.5PF_Q13MC14610002
C147 18P_0402_50V8J
R87 10M_0402_5%
PCH_RTCX1 — PCH_RTCX2

+RTCVCC close to RAM door RC Delay 18~25mS
R99 20K_0402_1% PCH_SRTCRST#
J2 10K_0603_5%
C149 1U_0402_6.3V6K

+RTCVCC close to RAM door RC Delay 18~25mS
R90 20K_0402_1% PCH_RTCRST#
J1 10K_0603_5%
C148 1U_0402_6.3V6K

8/19 Change footprint of U2 to WIESO_G6179-100000_8P
SA000041P00 4MB
U2
CS# VCC
WP# SCLK
HOLD# SI
GND SO
S IC FL 32M MX25L3206EM2I-12G SOP 8P
SPI ROM Footprint 200mil

R94 4.7K_0402_5% SPI_WP1#
R96 4.7K_0402_5% SPI_HOLD1#
PCH_SPI_CS0# — PCH_SPI_CLK_1 — PCH_SPI_MOSI_1 — PCH_SPI_MISO_1

R655 4.7K_0402_5%
PCH_SMBCLK — D_CK_SCLK — D_CK_SCLK <10,11>
Q32 SSM3K7002FU_SC70-3

R654 4.7K_0402_5%
PCH_SMBDATA — D_CK_SDATA — D_CK_SDATA <10,11>
Q31 SSM3K7002FU_SC70-3

R348 0_0402_5%
U20 NC7SZ08P5X_NL_SC70-5
SYS_PWROK — EC_PWROK — EC_PWROK <45>
VGATE — VGATE <45,57>

R342 0_0402_5%
Q18 MMBT3906_SOT23-3
PCH_RSMRST# — EC_RSMRST# <45>
R717 10K_0402_5%
R319 4.7K_0402_5% +3VALW
D38A D38B BAV99DW-7-F_SOT363-N
R343 2.2K_0402_5%

R943 0_0402_5%
U25 NC7SZ08P5X_NL_SC70-5
PCH_PLT_RST# — PLT_RST# — PLT_RST# <22,38,39,44>
R944 100K_0402_5%

SYS_PWROK_R R349 0_0402_5% SYS_PWROK
R350 @ 0_0402_5% VGATE

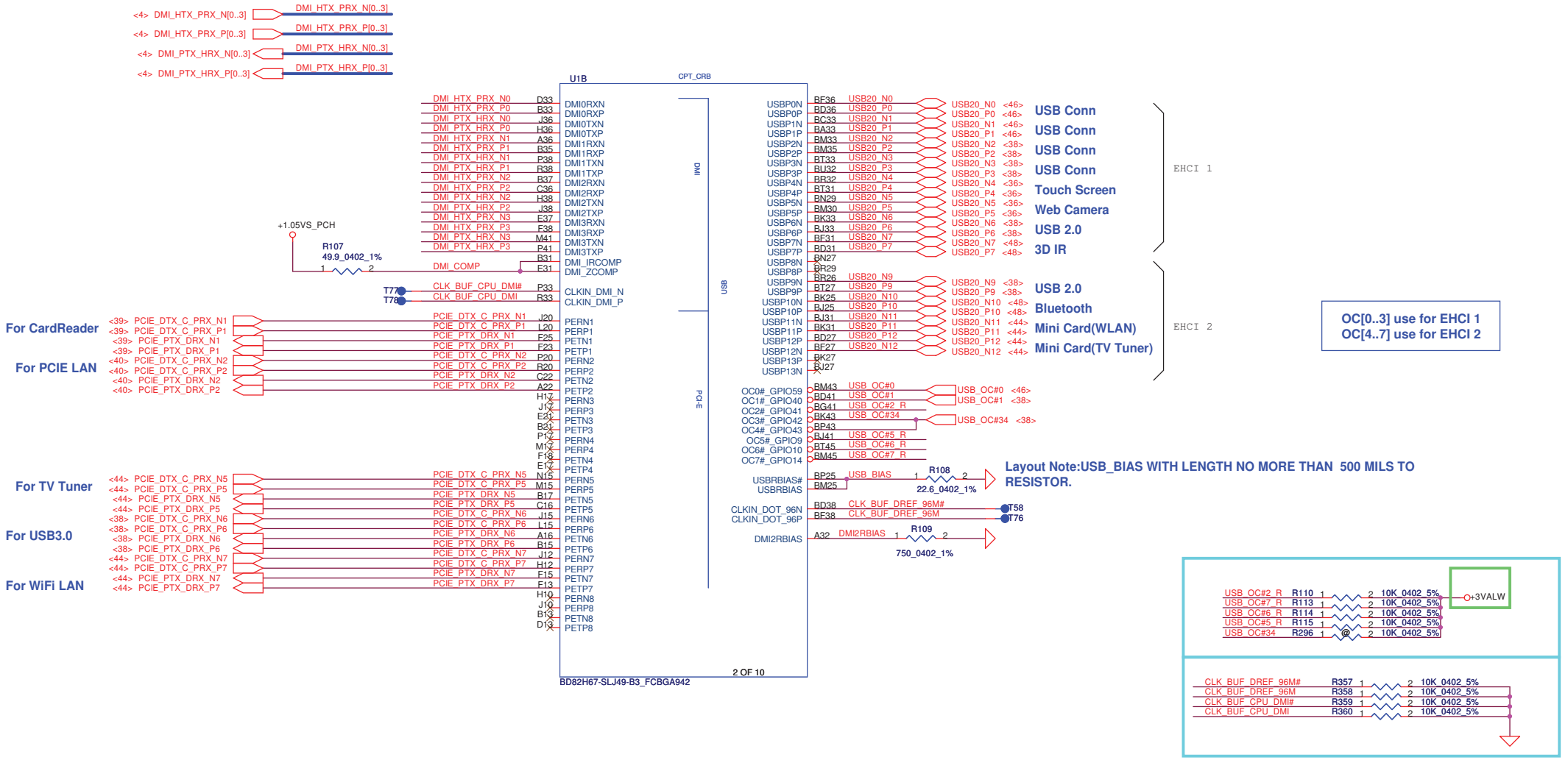
+RTCVCC
1M_0402_5% R103 SM_INTRUDER#
390K_0402_5% R104 PCH_DSWVRMEN
390K_0402_5% R105 PCH_INTVRMEN
R106 1K_0402_5% @

PCH_JTAG_TMS	R91	R92	200_0402_5% / 100_0402_5%
PCH_JTAG_TDO	R93	R95	200_0402_5% / 100_0402_5%
PCH_JTAG_TDI	R97	R98	200_0402_5% / 100_0402_5%
PCH_JTAG_RST#	R100	R101	20K_0402_5% / 10K_0402_5%
PCH_JTAG_TCK	R102		51_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title	PCH (2/9) LPC, HDA, SMBUS		
Size	Custom	Document Number	PLA00 M/B LA-6951P Schematic
Rev	1.A		
Date:	Thursday, February 24, 2011	Sheet	13 of 62



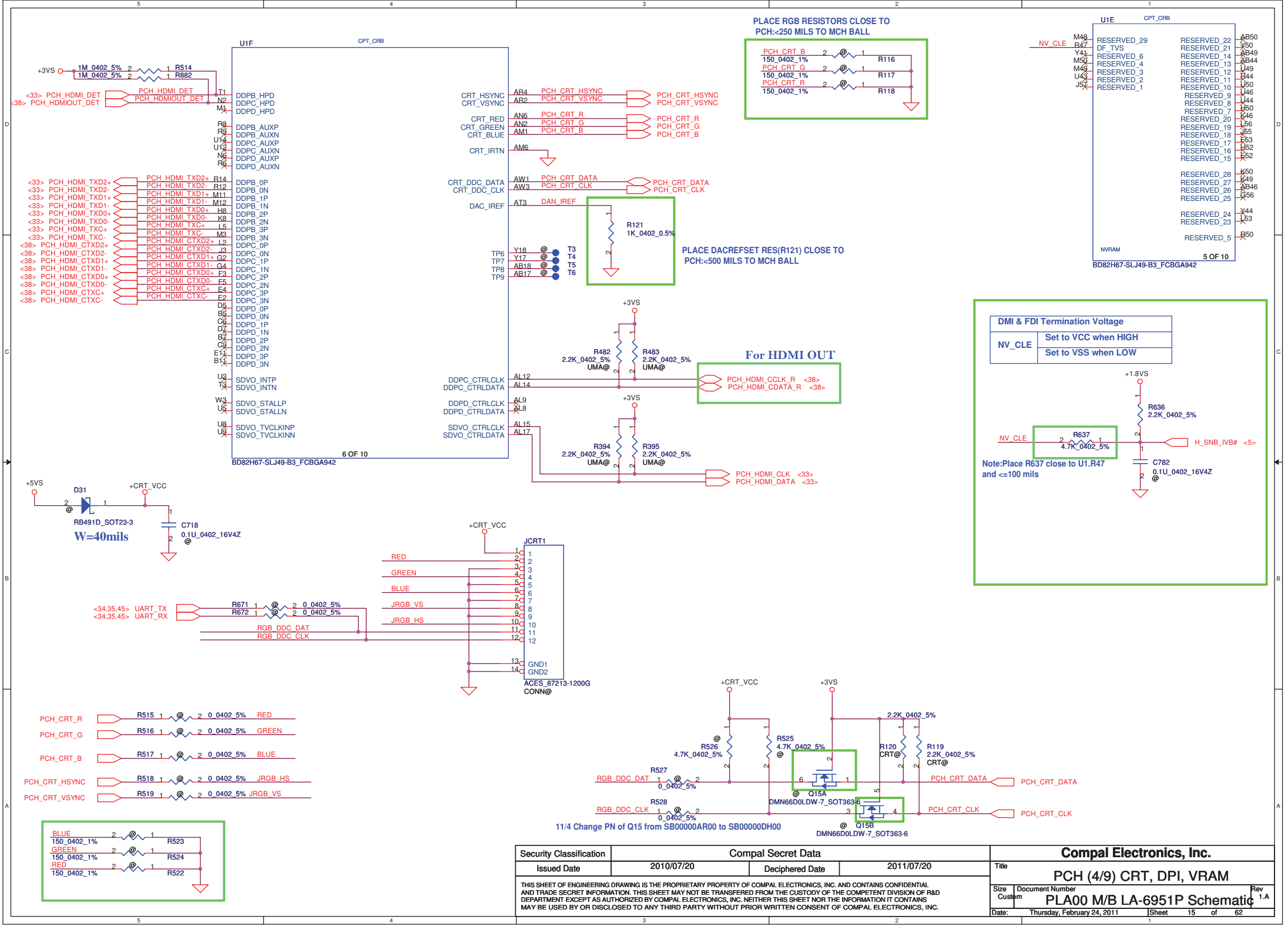
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (3/9) DMI, USB, PCIE

Size	Document Number	Rev
A	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 14 of 62


U1F
CPT_CRB
6 OF 10
BD82H67-SLJ49-B3_FCBGA942
PLACE RGB RESISTORS CLOSE TO PCH:<250 MILS TO MCH BALL
PLACE DACREFSET RES(R121) CLOSE TO PCH:<500 MILS TO MCH BALL
For HDMI OUT
U1E
5 OF 10
NVRAM
DMI & FDI Termination Voltage
NV_CLE
Set to VCC when HIGH
Set to VSS when LOW
Note:Place R637 close to U1.R47 and <=100 mils
W=40mils
11/4 Change PN of Q15 from SB00000AR00 to SB00000DH00
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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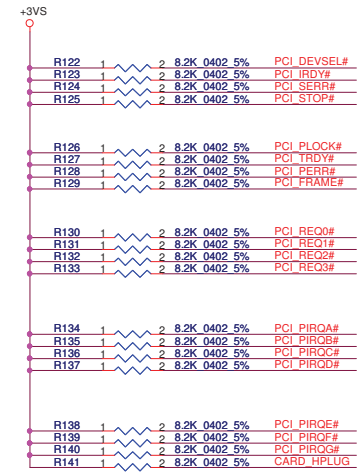
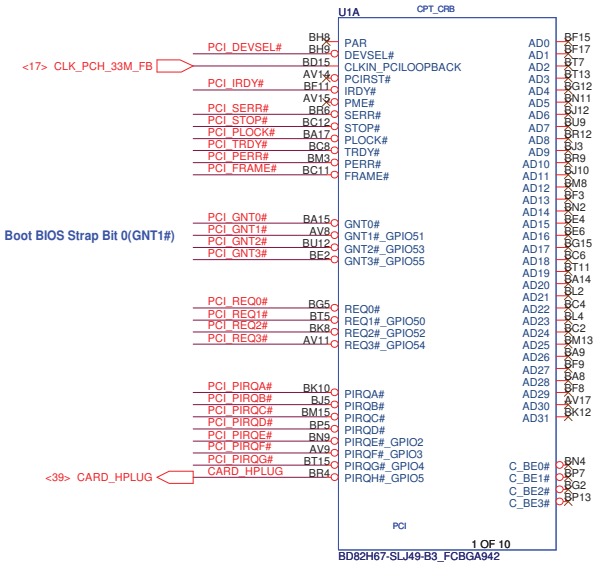
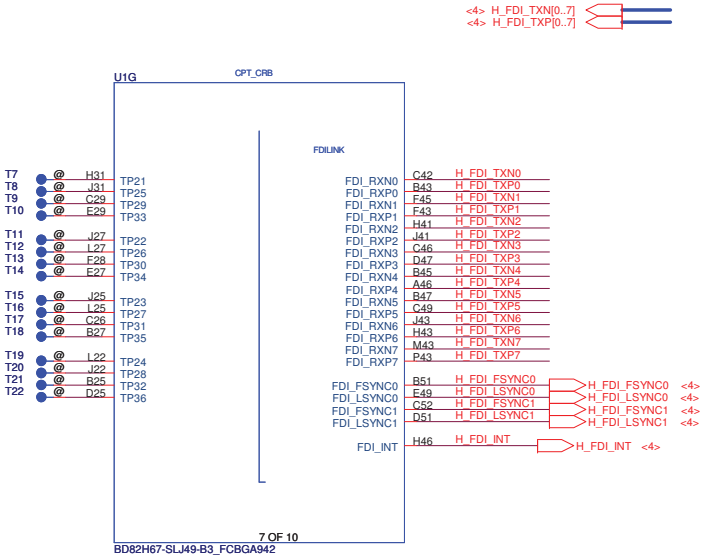
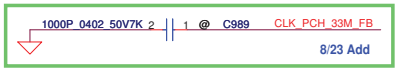
Compal Electronics, Inc.
Title
PCH (4/9) CRT, DPI, VRAM
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
Rev
1.A
Date:
Thursday, February 24, 2011
Sheet
15
of
62

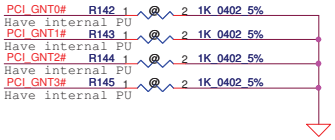








Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (5/9) PCI,FDI

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 16 of 62

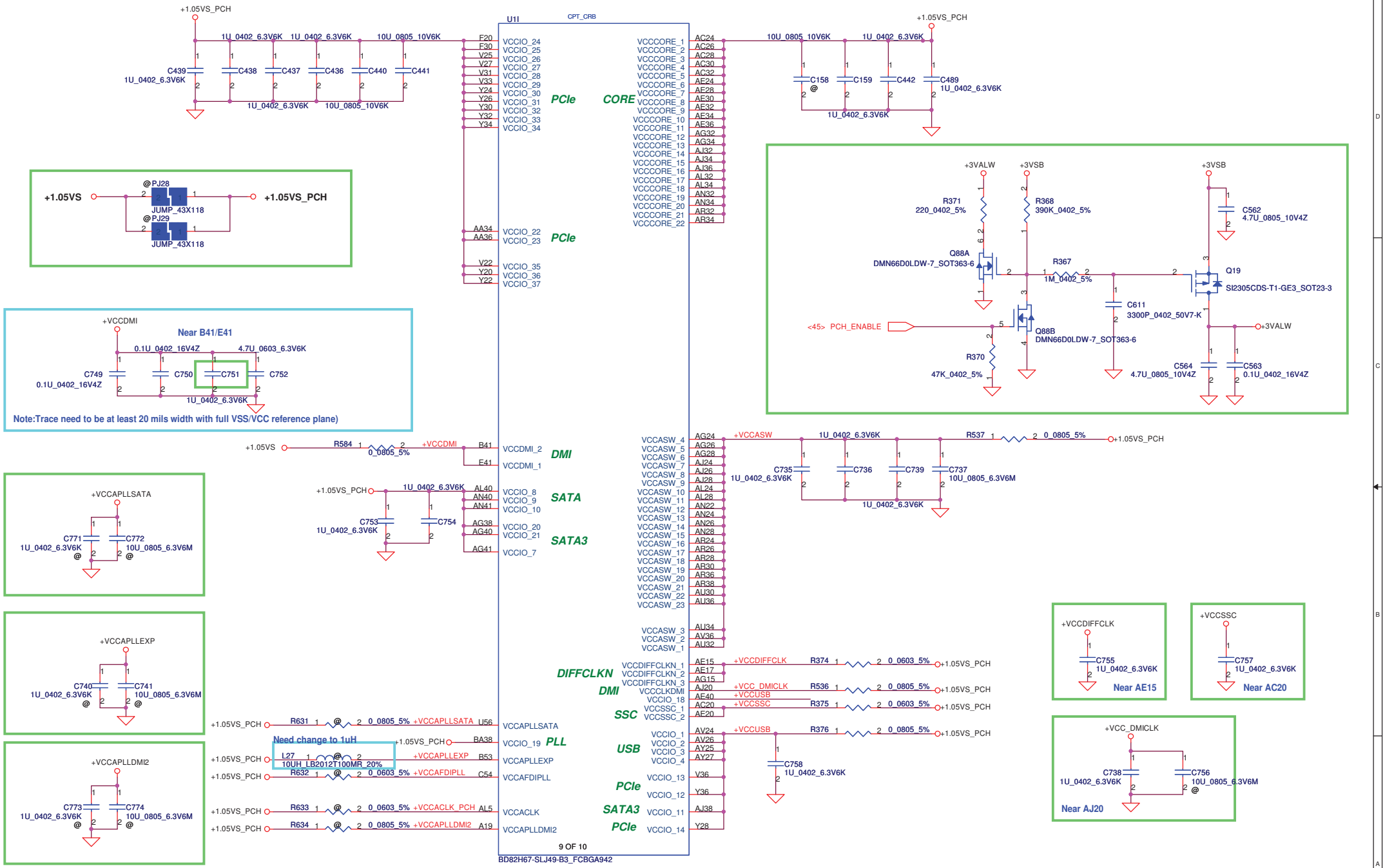
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (6/9) CLOCK

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 17 of 62



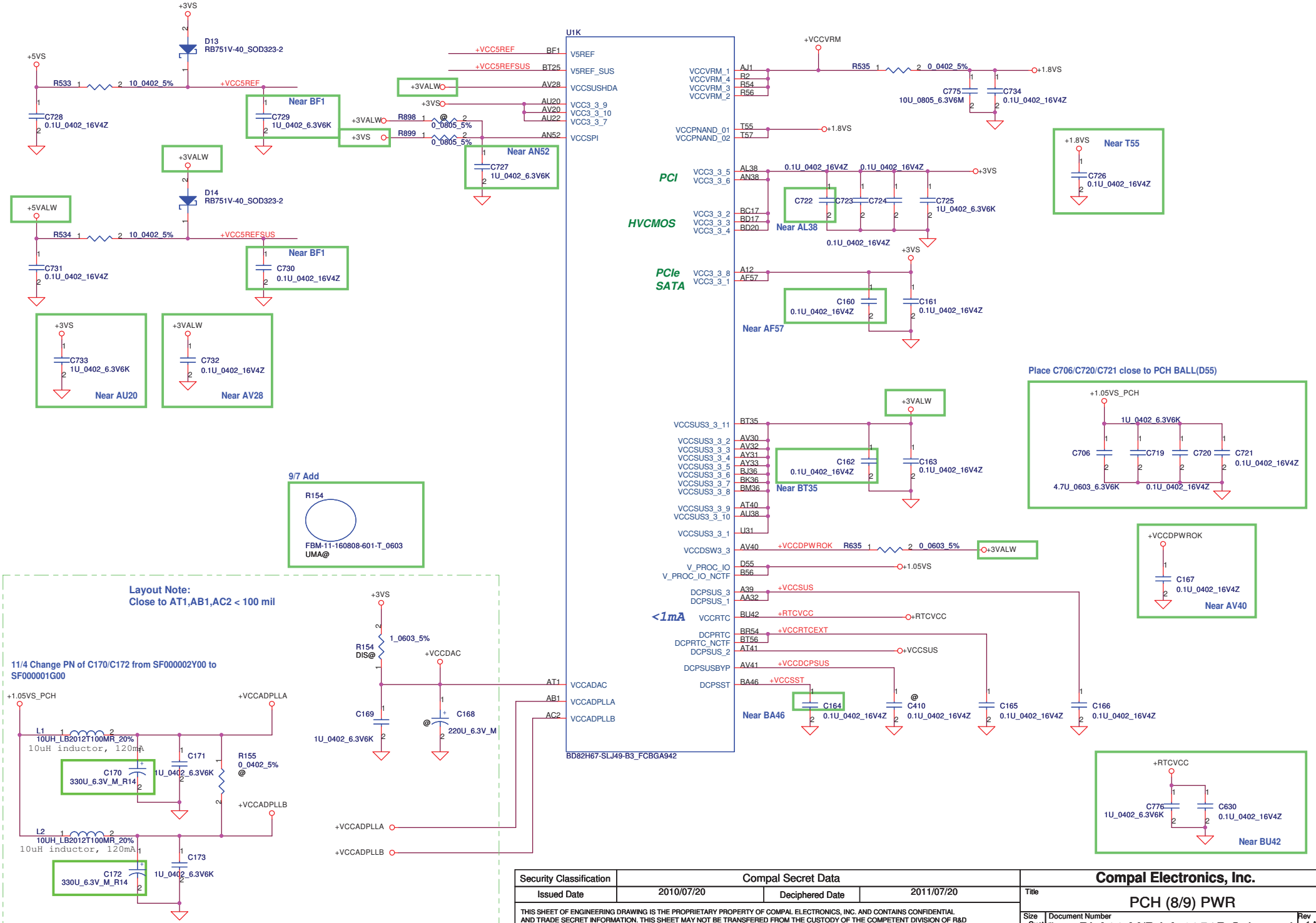
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 18 of 62



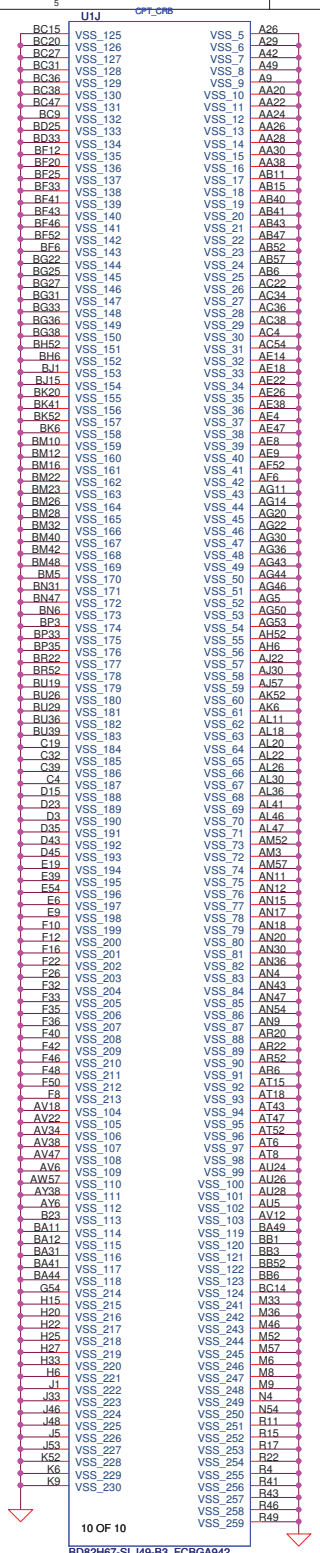
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 19 of 62



NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

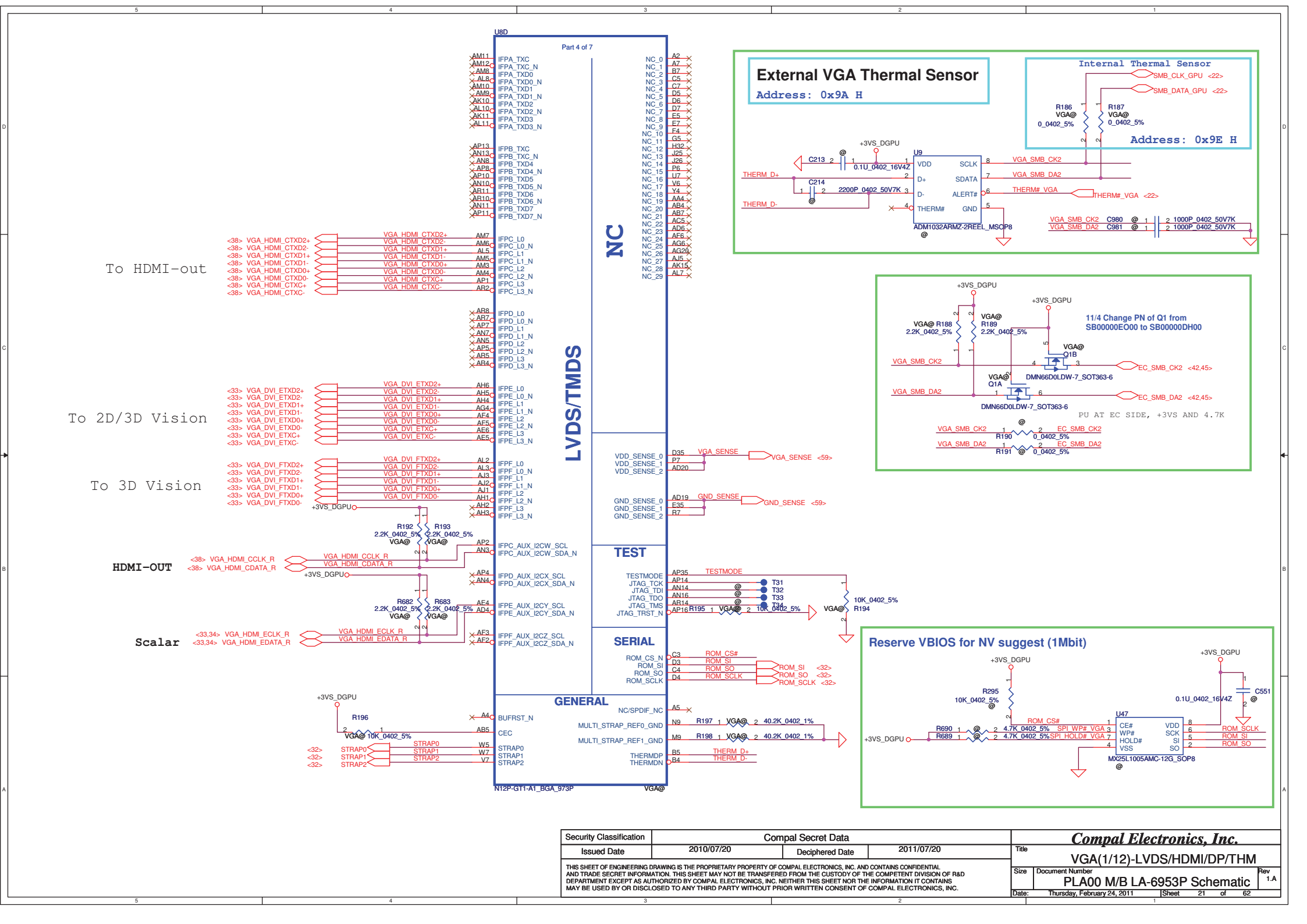
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **PCH(9/9)VSS**

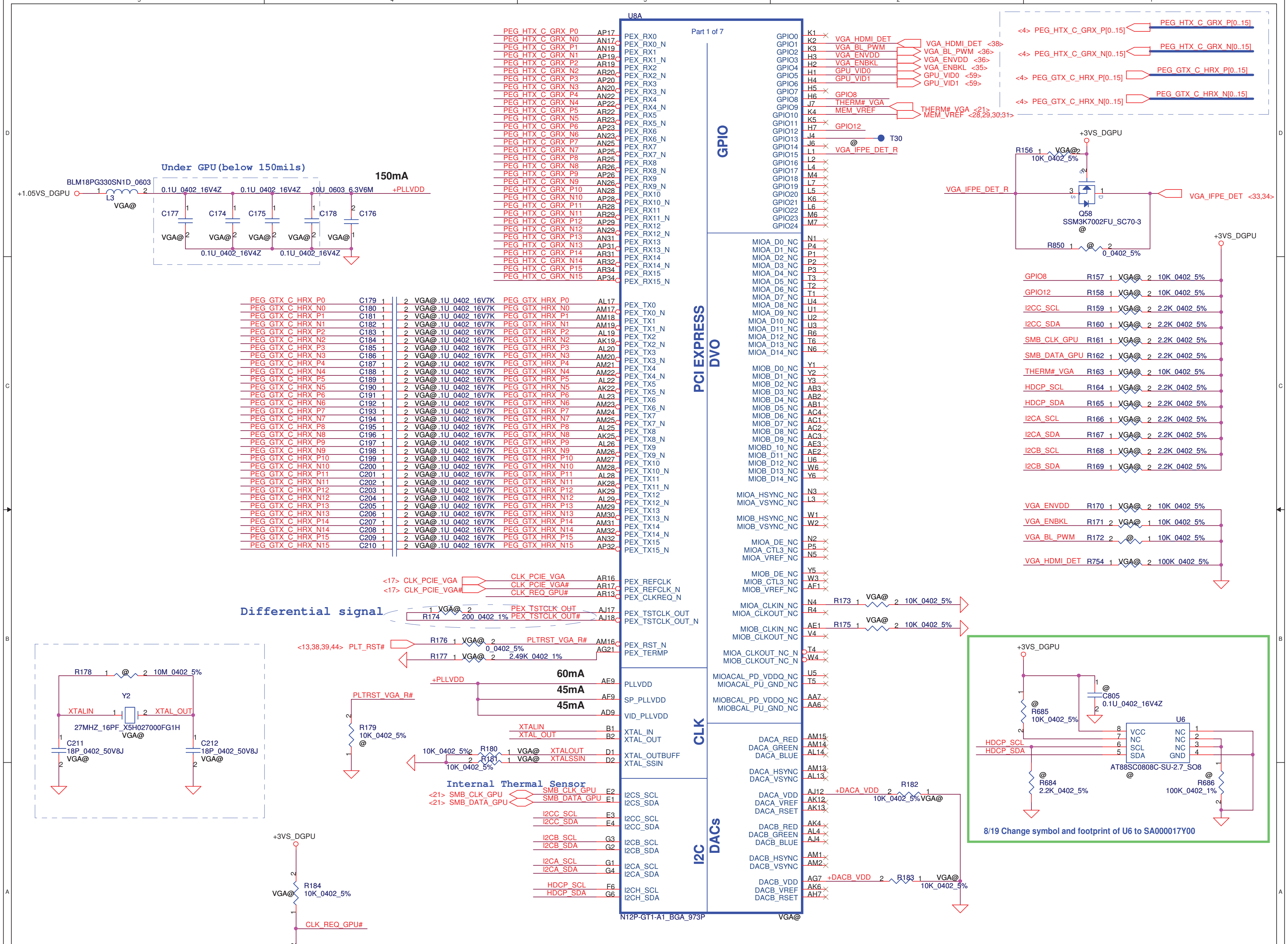
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 20 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.
Title: VGA(1/12)-LVDS/HDMI/DP/THM
Size: Document Number: PLA00 M/B LA-6953P Schematic
Rev: 1.A
Date: Thursday, February 24, 2011
Sheet 21 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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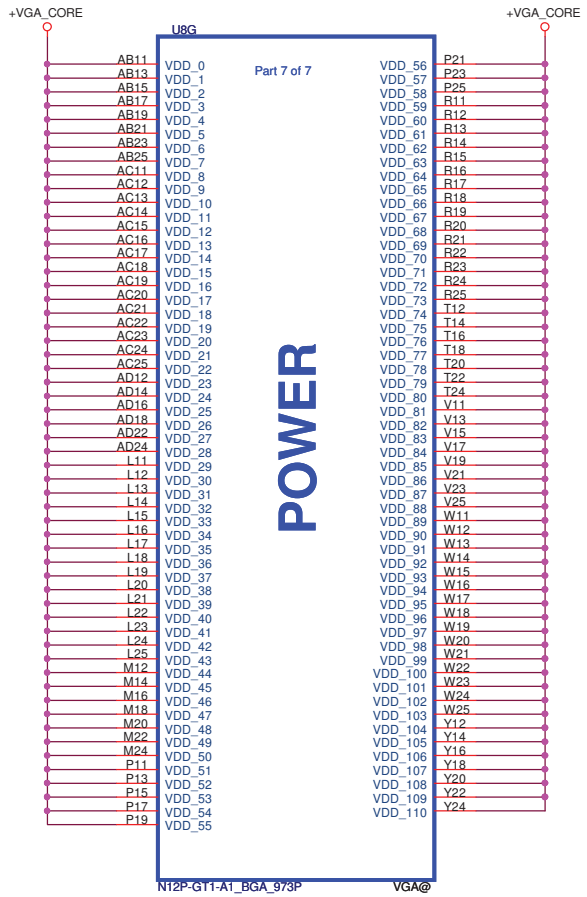
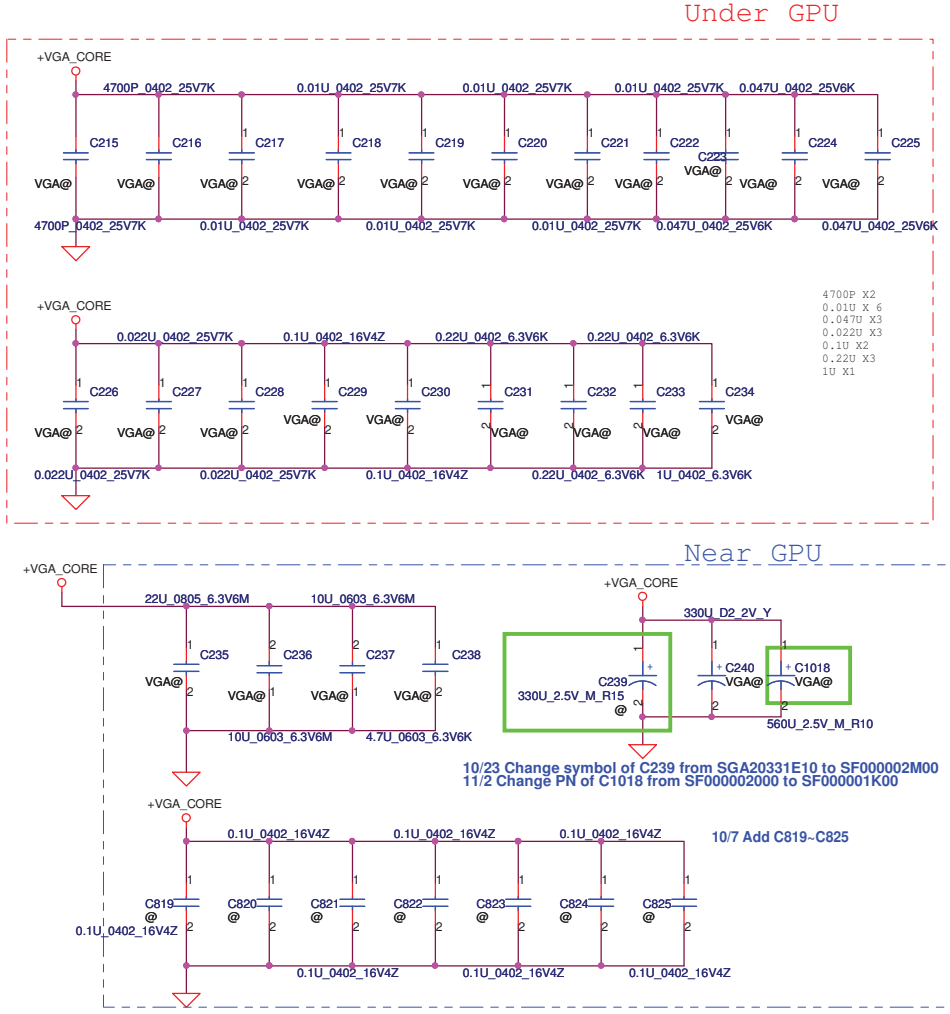
Compal Electronics, Inc.

Title: VGA(2/12)-PCIE/DAC/GPIO

Size | Document Number: PLA00 M/B LA-6953P Schematic | Rev 1.A

Date: Thursday, February 24, 2011 | Sheet 22 of 62





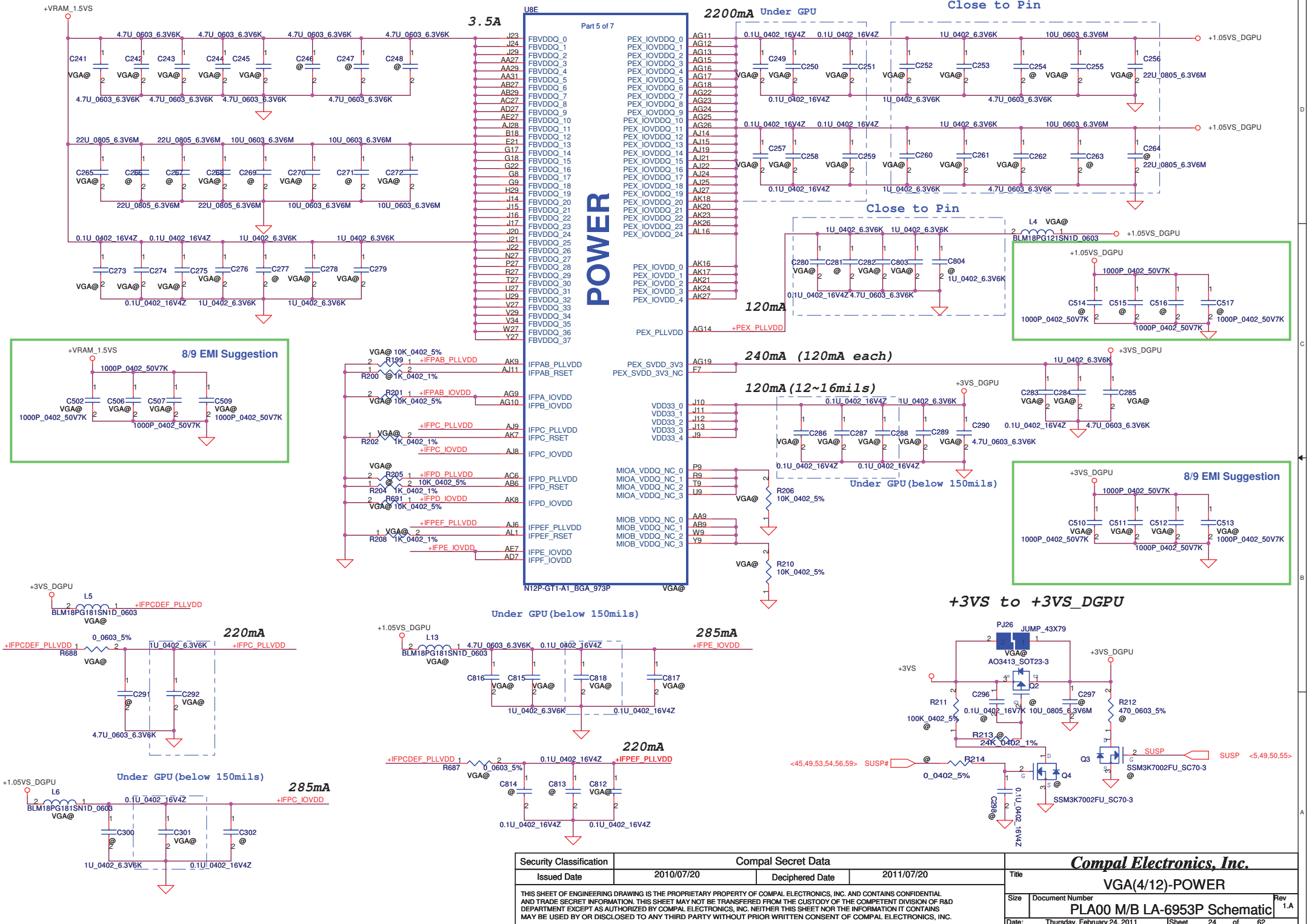
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

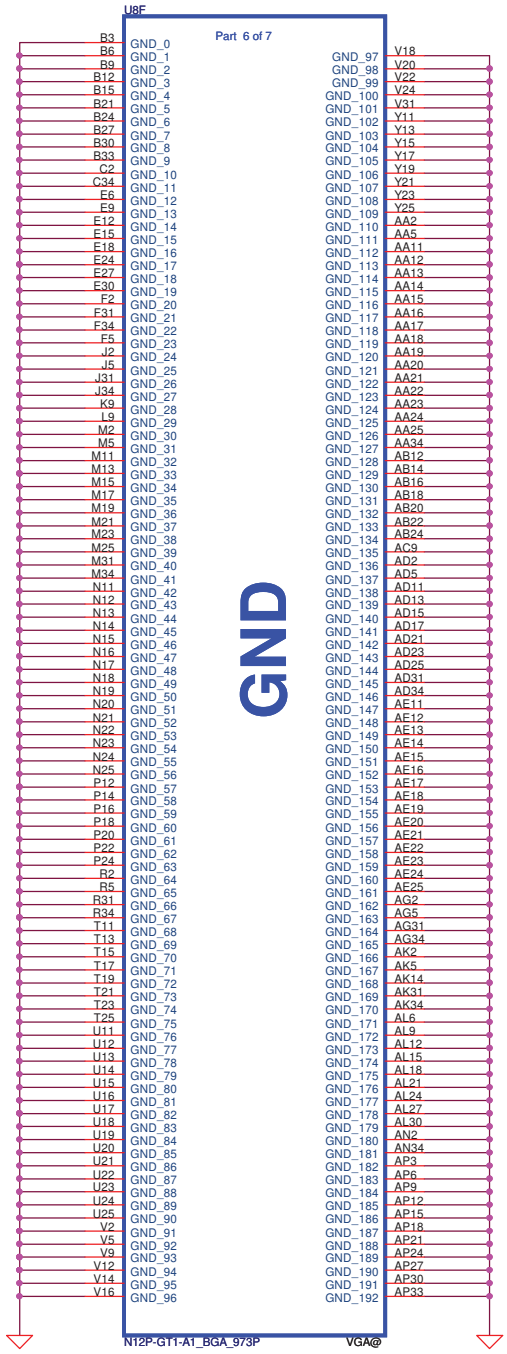
Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

Size	Document Number	Rev
	PLA00 M/B LA-6953P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 23 of 62


POWER
Part 5 of 7
U8E
N12P-GT1-A1_BGA_973P
3.5A
2200mA Under GPU
Close to Pin
120mA
240mA (120mA each)
120mA(12~16mils)
Under GPU(below 150mils)
8/9 EMI Suggestion
+3VS to +3VS_DGPU
220mA
285mA
+VRAM_1.5VS
+1.05VS_DGPU
+3VS_DGPU
+PEX_PLLVDD
+IFPAB_PLLVDD
+IFPAB_IOVDD
+IFPC_PLLVDD
+IFPC_IOVDD
+IFPD_PLLVDD
+IFPD_IOVDD
+IFPEF_PLLVDD
+IFPE_IOVDD
+IFPCDEF_PLLVDD
+IFPE_IOVDD
+IFPC_IOVDD
SUSP
SUSP#
Compal Secret Data
2010/07/20
2011/07/20
Compal Electronics, Inc.
VGA(4/12)-POWER
PLA00 M/B LA-6953P Schematic
Rev 1.A
Thursday, February 24, 2011
Sheet 24 of 62



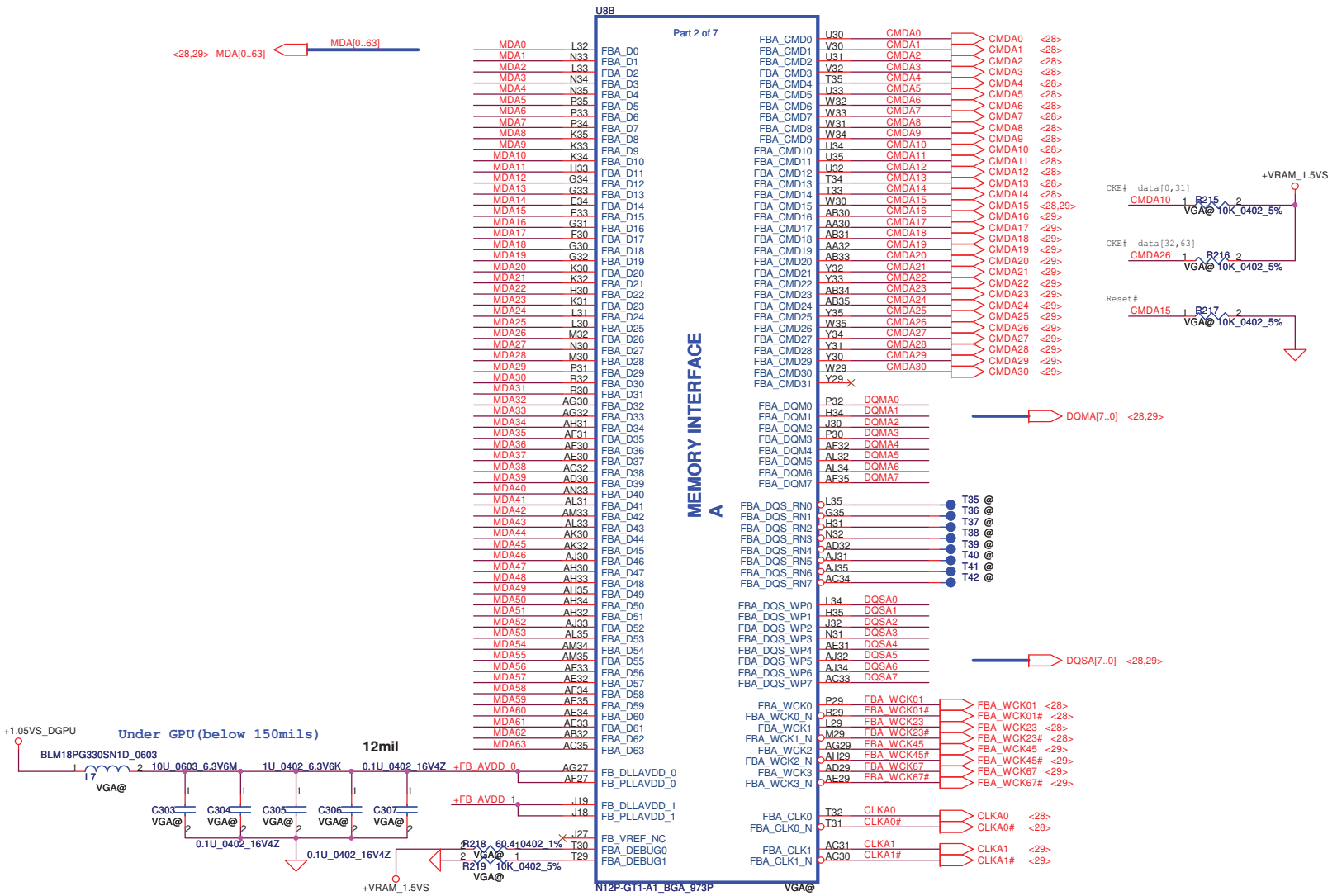
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PLA00 M/B LA-6953P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 25 of 62



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

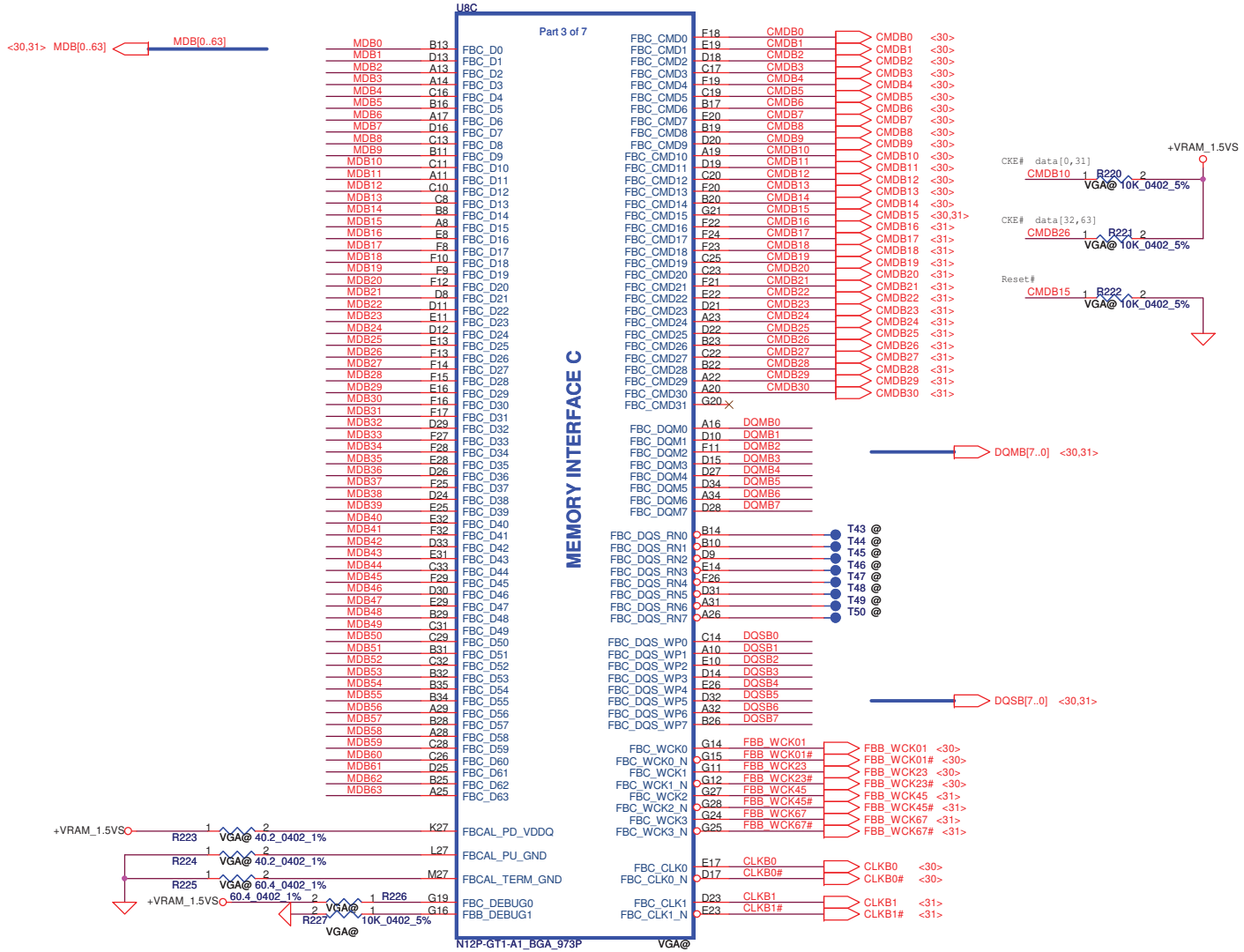
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PLA00 M/B LA-6953P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 26 of 62



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: PLA00 M/B LA-6953P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 27 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U10

U11

MF=0 MF=1 MF=1 MF=0

DQSA0 DQSA2 DQMA0 DQMA2

<26> CLKA0 CLKA0# CMDA10

<26> CMDA2 CMDA4 CMDA3 CMDA1

<26> CMDA6 CMDA11 CMDA12 CMDA7 CMDA9

R234 1K 0402 5% VGA@

R236 121 0402 1% VGA@

<26> CMDA8 CMDA13 CMDA0 CMDA14 CMDA5

<26> FBA_WCK01# FBA_WCK01

<26> FBA_WCK23# FBA_WCK23

+FBA_VREFD +FBA_VREFD +FBA_VREFC

C315 0.01U_0402_25V7K VGA@

<26,29> CMDA15

DQSA3 DQSA1 DQMA3 DQMA1

<26> CLKA0 CLKA0# CMDA10

<26> CMDA3 CMDA1 CMDA2 CMDA4

<26> CMDA12 CMDA7 CMDA6 CMDA11 CMDA9

R235 1K 0402 5% VGA@

R237 121 0402 1% VGA@

<26> CMDA8 CMDA14 CMDA5 CMDA13 CMDA0

<26> FBA_WCK23# FBA_WCK23

<26> FBA_WCK01# FBA_WCK01

+FBA_VREFD +FBA_VREFD +FBA_VREFC

<26,29> CMDA15

+VRAM_1.5VS

VDD VDDQ VSS VSSQ

170-BALL SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170 X76_HYN@

MDA[0..63] <26,29>

DQMA[7..0] <26,29>

DQSA[7..0] <26,29>

+VRAM_1.5VS

R228 549_0402_1% VGA@

R230 1.33K_0402_1% VGA@

C313 0.01U_0402_25V7K VGA@

+FBA_VREFC

R229 549_0402_1% VGA@

R231 1.33K_0402_1% VGA@

C314 0.01U_0402_25V7K VGA@

+FBA_VREFD

R232 931_0402_1% VGA@

R233 931_0402_1% VGA@

<22,29,30,31> MEM_VREF

Q5 SSM3K7002FU_SC70-3 VGA@

CLKA0 CLKA0#

R238 40.2_0402_1% VGA@

R239 160_0402_1% @

R240 40.2_0402_1% VGA@

C316 0.01U_0402_25V7K VGA@

CLKA0_R

+VRAM_1.5VS

10U_0603_6.3V6M

C317 C318 C319 VGA@

0.1U_0402_16V4Z

C320 C321 C322 C323 C324 C325 VGA@

1U_0402_6.3V6K

C326 C327 C328 C329 C330 C331 C332 C333 VGA@

C742 330U_6.3V_M_R14 @

C1017 330U_6.3V_M @

10/23 Change symbol of C742 from SGA20331E10 to SF000002M00
11/2 Change PN of C742 from SF000002M00 to SF000001G00

9/7 Add

U10	U11
K4G10325FE-HC04 X76_SAM@	K4G10325FE-HC04 X76_SAM@
K4G20325FC-HC04 X76_SAM2G@	K4G20325FC-HC04 X76_SAM2G@
H5GQ2H24MFR-T2C X76_HYN2G@	H5GQ2H24MFR-T2C X76_HYN2G@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VRAM_GDDR5 / Channel A

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 28 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U12

U13

MDA[0..63] <26,28>
DQMA[7..0] <26,28>
DQSA[7..0] <26,28>

+VRAM_1.5VS

R241 549_0402_1% VGA@
R242 549_0402_1% VGA@
R243 1.33K_0402_1% VGA@
R244 1.33K_0402_1% VGA@
16mil +FBA_VREFD_U
16mil +FBA_VREFC_U
C334 0.01U_0402_25V7K VGA@
C335 0.01U_0402_25V7K VGA@
R247 VGA@ 931_0402_1%
R248 VGA@ 931_0402_1%
<22,28,30,31> MEM_VREF
Q6 SSM3K7002FU_SC70-3 VGA@

R251 40.2_0402_1% VGA@
R252 @ 160_0402_1%
R253 40.2_0402_1% VGA@
CLKA1
CLKA1#
C337 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M
C338 VGA@
C339 VGA@
C340 VGA@

0.1U_0402_16V4Z
C341 VGA@
C342 VGA@
C343 VGA@
C344 VGA@
C345 VGA@
C346 VGA@

1U_0402_6.3V6K
C347 VGA@
C348 VGA@
C349 VGA@
C350 VGA@
C351 VGA@
C352 VGA@
C353 VGA@
C354 VGA@

C336 0.01U_0402_25V7K VGA@
<26,28> CMDA15

R245 VGA@ 1K_0402_1%
R246 VGA@ 1K_0402_1%
R249 VGA@ 121_0402_1%
R250 VGA@ 121_0402_1%

170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
X76_HYN@

	U12	U13
K4G10325FE-HC04 X76_SAM@		
K4G20325FC-HC04 X76_SAM2G@		
H5GQ2H24MFR-T2C X76_HYN2G@		

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **VRAM_DDDR5 / Channel A**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 29 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U14

U15

MDB[0..63] <27,31>
DQMB[7..0] <27,31>
DQSB[7..0] <27,31>

+VRAM_1.5VS

R254 549_0402_1% VGA@
R255 549_0402_1% VGA@
+FBB_VREFD
+FBB_VREFC
R256 1.33K_0402_1% VGA@
R257 1.33K_0402_1% VGA@
C355 0.01U_0402_25V7K VGA@
C356 0.01U_0402_25V7K VGA@
R260 931_0402_1% VGA@
R261 931_0402_1% VGA@
<22,28,29,31> MEM_VREF
Q7 SSM3K7002FU_SC70-3 VGA@

R264 40.2_0402_1%
R265 160_0402_1%
R266 40.2_0402_1%
CLKB0
CLKB0#
C358 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M
C359 C360 C361 VGA@

0.1U_0402_16V4Z
C362 C363 C364 C365 C366 C367 VGA@

1U_0402_6.3V6K
C368 C369 C370 C371 C372 C373 C374 C375 VGA@

C357 0.01U_0402_25V7K VGA@
<27,31> CMDB15

R258 1K_0402_1% VGA@
R262 121_0402_1% VGA@
R259 1K_0402_1% VGA@
R263 121_0402_1% VGA@

170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
X76_HYN@

C743 330U_6.3V_M_R14 VGA@

10/23 Change symbol of C743 from SGA20331E10 to SF000002M00
11/2 Change PN of C743 from SF000002M00 to SF000001G00

U14 / U15
K4G10325FE-HC04 X76_SAM@
K4G10325FE-HC04 X76_SAM@
K4G20325FC-HC04 X76_SAM2G@
K4G20325FC-HC04 X76_SAM2G@
H5GQ2H24MFR-T2C X76_HYN2G@
H5GQ2H24MFR-T2C X76_HYN2G@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VRAM_GDDR5 / Channel B

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 30 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U16

U17

MDB[0..63] <27,30>

DQMB[7..0] <27,30>

DQSB[7..0] <27,30>

+VRAM_1.5VS

R267 549_0402_1% VGA@

R268 549_0402_1% VGA@

16mil +FBB_VREFD_U

16mil +FBB_VREFC_U

R269 1.33K_0402_1% VGA@

C376 0.01U_0402_25V7K VGA@

R270 1.33K_0402_1% VGA@

C377 0.01U_0402_25V7K VGA@

R275 VGA@ 931_0402_1%

R276 VGA@ 931_0402_1%

<22,28,29,30> MEM_VREF

Q8 SSM3K7002FU_SC70-3 VGA@

R277 40.2_0402_1% VGA@

R278 @ 160_0402_1%

R279 40.2_0402_1% VGA@

CLKB1

CLKB1#

C379 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M

C380 VGA@

C381 VGA@

C382 VGA@

C383 VGA@

C384 VGA@

C385 VGA@

C386 VGA@

C387 VGA@

C388 VGA@

0.1U_0402_16V4Z

C389 VGA@

C390 VGA@

C391 VGA@

C392 VGA@

C393 VGA@

C394 VGA@

C395 VGA@

C396 VGA@

1U_0402_6.3V6K

C378 0.01U_0402_25V7K VGA@

R271 VGA@ 1K_0402_1%

R273 VGA@ 121_0402_1%

R272 VGA@ 1K_0402_1%

R274 VGA@ 121_0402_1%

+FBB_VREFD_U

+FBB_VREFC_U

VREFD

VREFC

RESET#

VSS

VDD

VDDQ

VSSQ

VDDO

VSSO

170-BALL SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

10/22 Add C522~C525

C522 @ 0.1U_0402_16V4Z

C523 @ 0.1U_0402_16V4Z

C524 @ 0.1U_0402_16V4Z

C525 @ 0.1U_0402_16V4Z

U16	U17
K4G10325FE-HC04 X76_SAM@	K4G10325FE-HC04 X76_SAM@
K4G20325FC-HC04 X76_SAM2G@	K4G20325FC-HC04 X76_SAM2G@
H5GQ2H24MFR-T2C X76_HYN2G@	H5GQ2H24MFR-T2C X76_HYN2G@

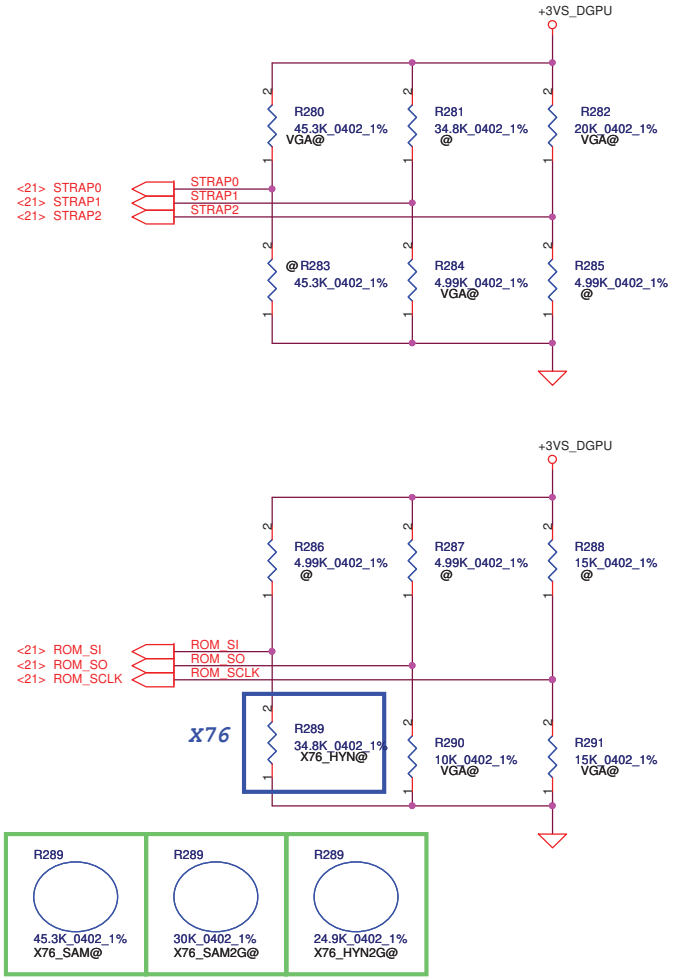
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **VRAM_DDDR5 / Channel B**

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 31 of 62



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	256MB (Default)
1	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.
Title: VGA(12/12)-MISC
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A
Date: Thursday, February 24, 2011 | Sheet 32 of 62

0804 Vendor suggest close to Cap.

8/18 Add C923~C926(Vendor suggest)

S2 (pin33)	S1 (pin32)	TMDS/DDC output
H	H	PORT1/SCL1,SDA1
H	L	PORT2/SCL2,SDA2
L	H	All disconnected

8/18 Add L56(Vendor suggest)

11/29 Add R755 for fine tune (vendor suggest)

9/29 Add

11/29 Add R735 (vendor suggest)

PORT 1 (PC-mode)

PORT 2 (Monitor-mode)

AZHW251RH_64P_LQFP

To Scaler

10/22 Add(EMI Request)

11/29 Add R734 (vendor suggest)

11/29 Add R752, R753 for fine tune (vendor suggest)

10/7 Change U18 symbol

11/29 Add R734 from SA00003RJ00 to SA00004LX00

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

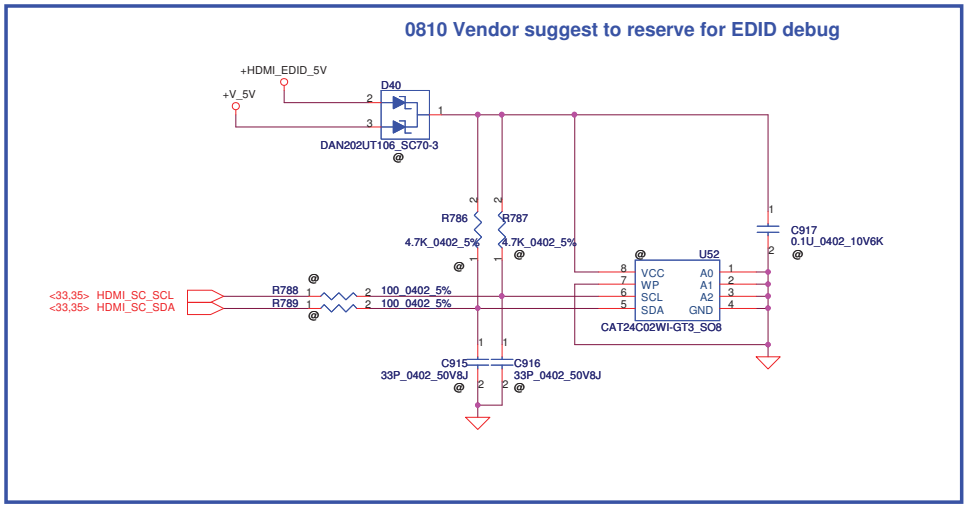
Compal Electronics, Inc.

Title: HDMI Switch

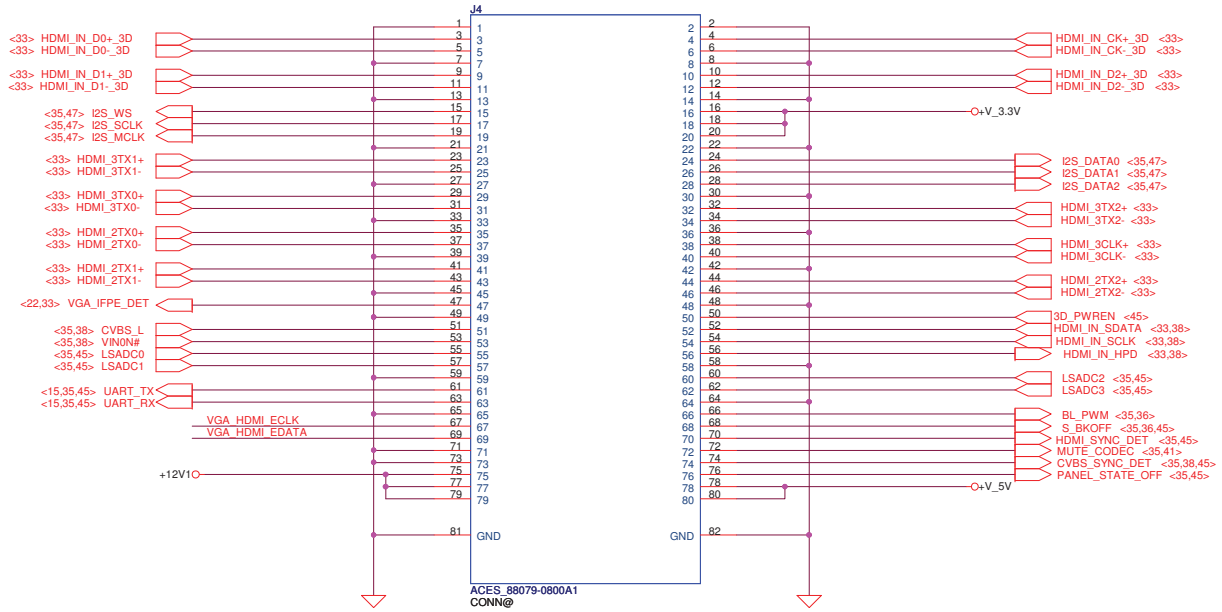
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 33 of 62

0810 Vendor suggest to reserve for EDID debug



12/11 3D Scaler Pin define update



12/6 Change symbol of J4 from LTCX002TM00 to SP010011B00(60pin to 80pin)

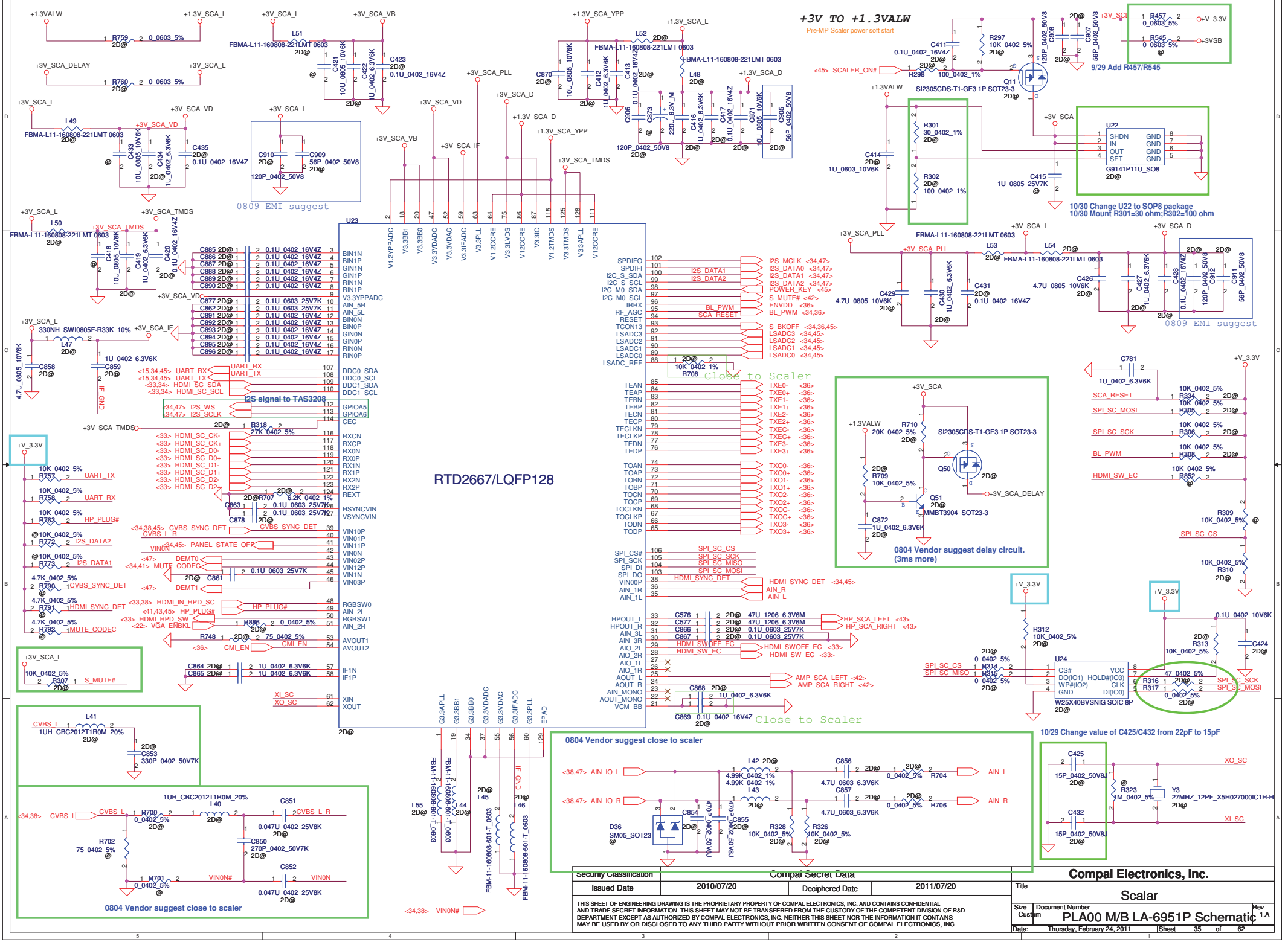
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 3D Scalar

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 34 of 62

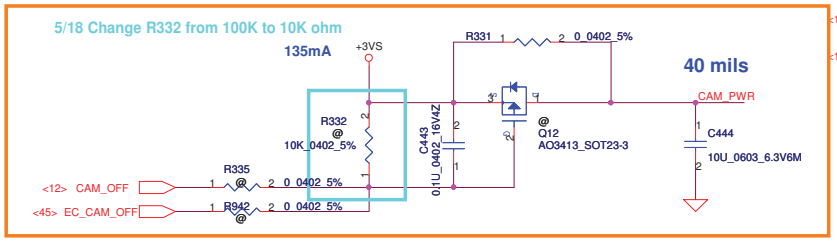

+3V TO +1.3VALW
Pre-MP Scaler power soft start
9/29 Add R457/R545
10/30 Change U22 to SOP8 package
10/30 Mount R301=30 ohm;R302=100 ohm
0809 EMI suggest
I2S signal to TAS3208
RTD2667/LQFP128
Close to Scaler
0804 Vendor suggest delay circuit. (3ms more)
0804 Vendor suggest close to scaler
10/29 Change value of C425/C432 from 22pF to 15pF
Compal Secret Data
Compal Electronics, Inc.
Scalar
PLA00 M/B LA-6951P Schematic
Issued Date 2010/07/20
Deciphered Date 2011/07/20
Thursday, February 24, 2011

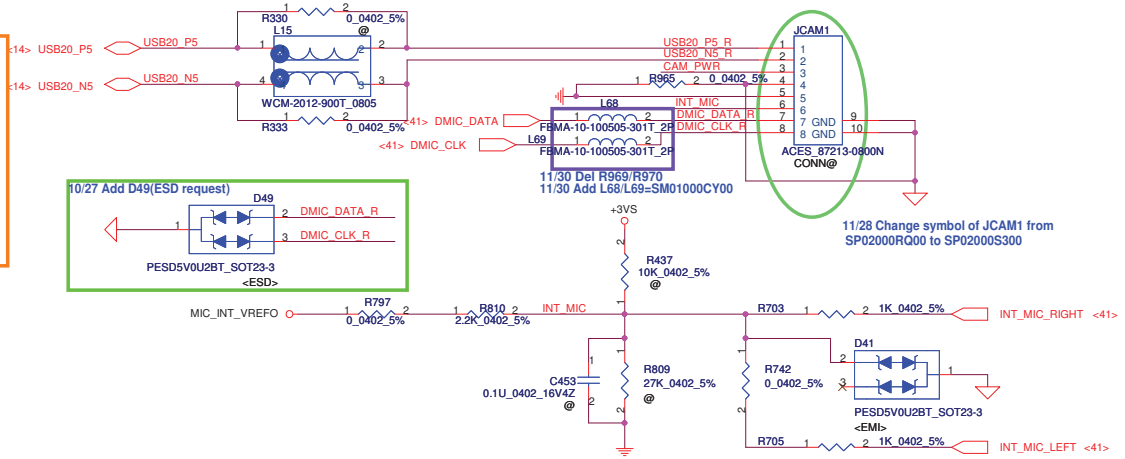
WebCam+Digital Mic

5/18 Change R332 from 100K to 10K ohm

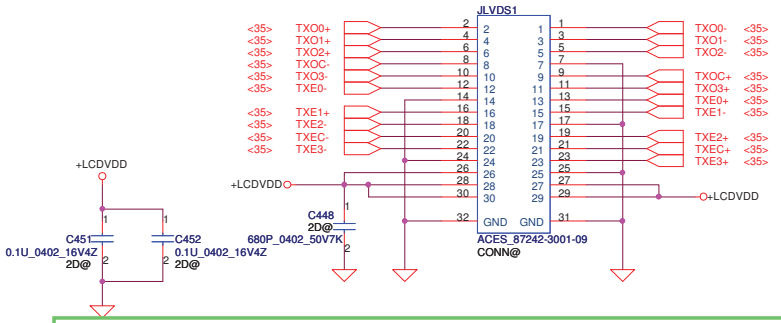
135mA

40 mils





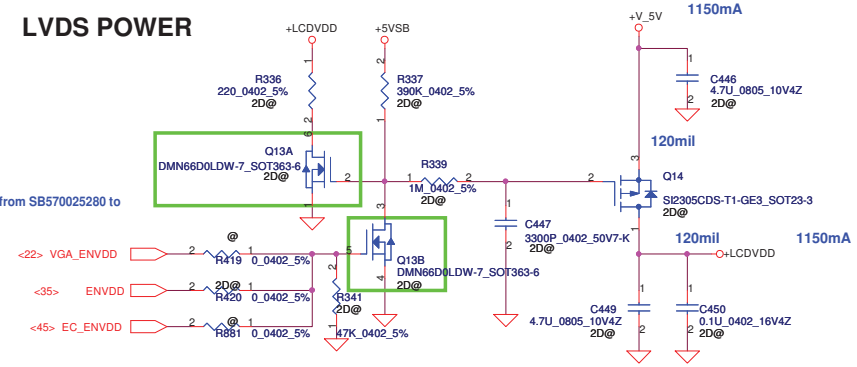
LVDS CONN



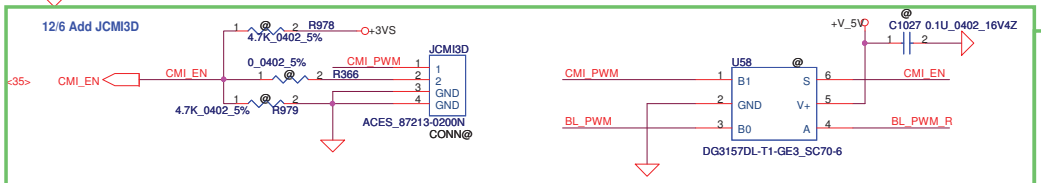
LVDS POWER

1150mA

11/4 Change PN of Q13 from SB570025280 to SB00000DH00

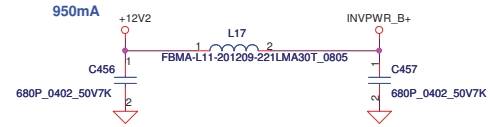


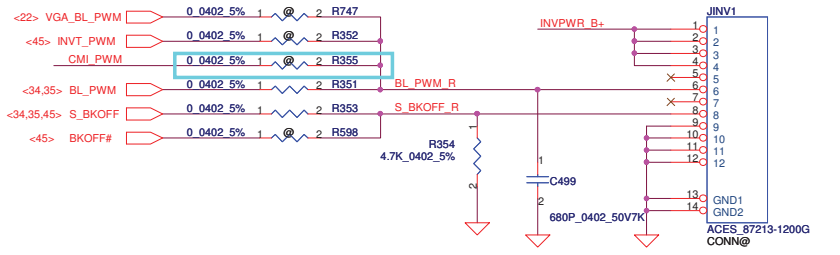
12/6 Add JCMI3D



INVERTER

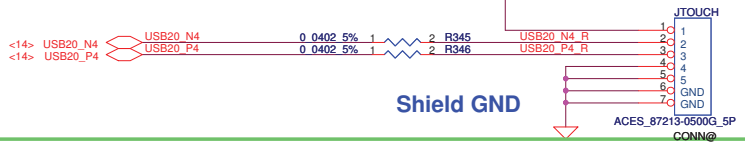
ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20





Touch Panel

PVT change from alw to vs for EUP.



Shield GND

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: LCD CONN. / WebCam

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 36 of 62

HDD POWER Conn

+12VS 8/18 Add C918~C921

C920 0.1U_0402_16V4Z
C918 10U_0805_25V_K
C921 0.1U_0402_16V4Z
C919 10U_0805_6.3V6M

+5VS

Layout Note:Place C918/C919/C920/C921 close to JWAFER1

HDD

+12VS
+5VS

JWAF1
ACES_88290-044G
CONN@

12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

SATA HDD Conn.

<12> SATA_PTX_DRX_P1
<12> SATA_PTX_DRX_N1
SATA_PTX_DRX_P1 C461 0.01U_0402_16V7K SATA_PTX_C_DRX_P1
SATA_PTX_DRX_N1 C462 0.01U_0402_16V7K SATA_PTX_C_DRX_N1

<12> SATA_DTX_C_PRX_N1
<12> SATA_DTX_C_PRX_P1
SATA_DTX_C_PRX_N1 C463 0.01U_0402_16V7K SATA_DTX_PRX_N1
SATA_DTX_C_PRX_P1 C464 0.01U_0402_16V7K SATA_DTX_PRX_P1

JHDD1
GND A+ A- GND B- B+ GND GND GND
TYCO_4-1775058-8
CONN@

ODD POWER Conn

+12VS 10/29 Add C930/C931

C930 0.1U_0402_16V4Z
C931 10U_0805_25V_K
C928 0.1U_0402_16V4Z
C929 10U_0805_6.3V6M

+5VS

10/28 Add C928/C929

Layout Note:Place C928/C929 close to JWAFER2

+12VS
+5VS

JWAF2
ACES_88290-044G
CONN@

12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

ODD

SATA ODD Conn.

<12> SATA_PTX_DRX_P4
<12> SATA_PTX_DRX_N4
C470 0.01U_0402_16V7K SATA_PTX_C_DRX_P4
C471 0.01U_0402_16V7K SATA_PTX_C_DRX_N4

<12> SATA_DTX_C_PRX_N4
<12> SATA_DTX_C_PRX_P4
C469 0.01U_0402_16V7K SATA_DTX_PRX_N4
C472 0.01U_0402_16V7K SATA_DTX_PRX_P4

JODD1
GND A+ A- GND B- B+ GND GND GND
TYCO_4-1775058-5
CONN@

SSD

+1.5VS

1U_0402_6.3V6K
C476 10U_0805_6.3V6M
C475
C474
C473 1000P_0402_50V7K
0.1U_0402_16V4Z

+3VS

1U_0402_6.3V6K
C481 1000P_0402_50V7K
C482
C483
C484
0.1U_0402_16V4Z
10U_0805_6.3V6M

MINI SSD Conn.

+3VS
+1.5VS

JMINI3

<12> SATA_DTX_C_PRX_P0
<12> SATA_DTX_C_PRX_N0
SATA_DTX_C_PRX_P0 C744 0.01U_0402_16V7K SATA_DTX_PRX_P0_RC
SATA_DTX_C_PRX_N0 C745 0.01U_0402_16V7K SATA_DTX_PRX_N0_RC

<12> SATA_PTX_DRX_N0
<12> SATA_PTX_DRX_P0
SATA_PTX_DRX_N0 C746 0.01U_0402_16V7K SATA_PTX_DRX_N0_RC
SATA_PTX_DRX_P0 C747 0.01U_0402_16V7K SATA_PTX_DRX_P0_RC

@ R745 0_0402_5% PCH_SMBCLK <13,44>
@ R746 0_0402_5% PCH_SMBDATA <13,44>

+3VS

<45> SSD_DET#

BELLW_80003-1021
CONN@

SATA SSD Conn.

<12> SATA_PTX_DRX_P2
<12> SATA_PTX_DRX_N2
SATA_PTX_DRX_P2 C478 0.01U_0402_16V7K SATA_PTX_C_DRX_P2
SATA_PTX_DRX_N2 C477 0.01U_0402_16V7K SATA_PTX_C_DRX_N2

<12> SATA_DTX_C_PRX_N2
<12> SATA_DTX_C_PRX_P2
SATA_DTX_C_PRX_N2 C479 0.01U_0402_16V7K SATA_DTX_PRX_N2
SATA_DTX_C_PRX_P2 C480 0.01U_0402_16V7K SATA_DTX_PRX_P2

JSSD1
GND A+ A- GND B- B+ GND GND GND
TYCO_4-1775058-5
CONN@

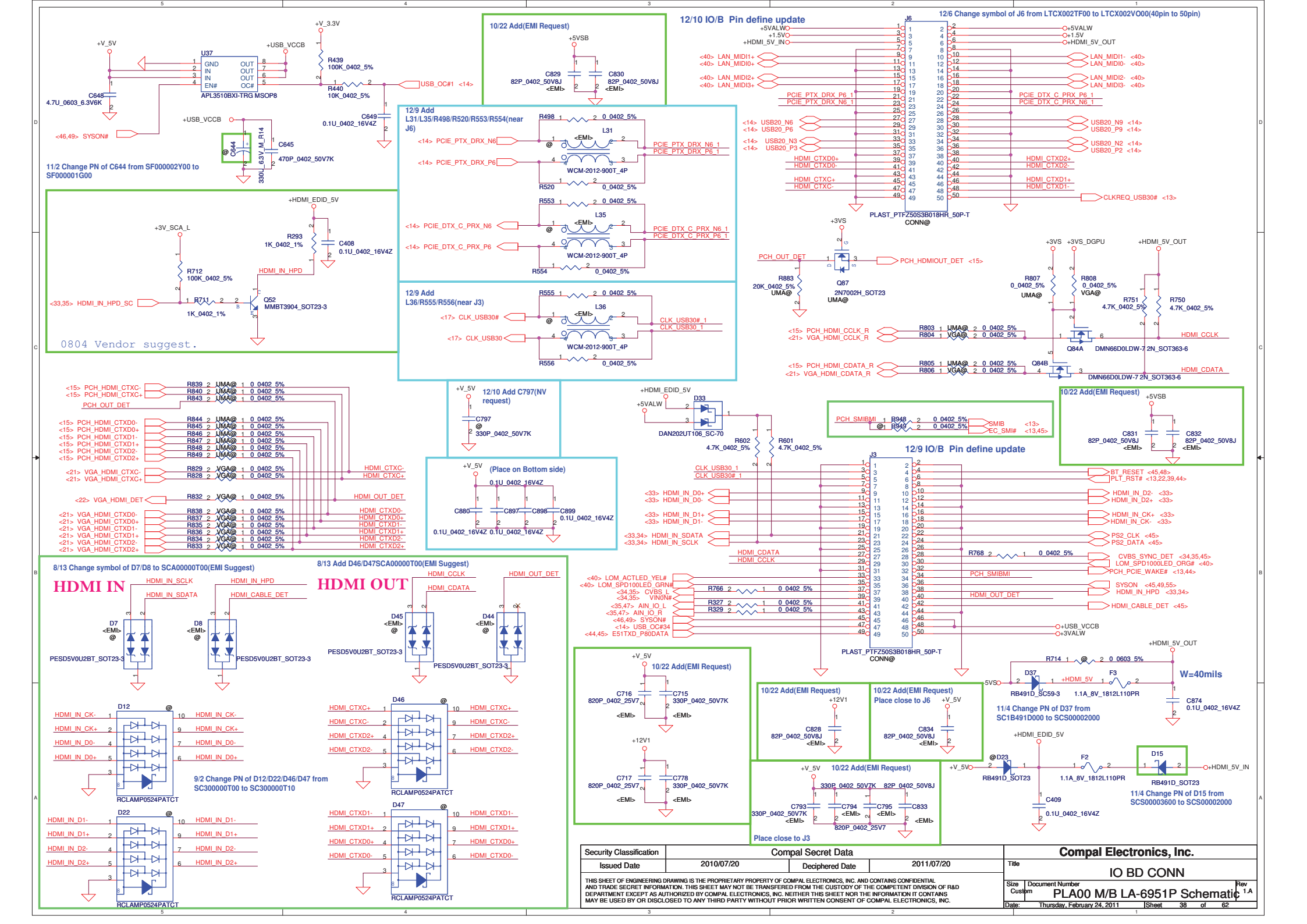
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: HDD & ODD & SSD Connector

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 37 of 62


12/10 IO/B Pin define update
12/6 Change symbol of J6 from LTCX002TF00 to LTCX002VO00(40pin to 50pin)
J6
PLAST_PTFZ50S3B018HR_50P-T
CONN@
10/22 Add(EMI Request)
12/9 Add
L31/L35/R498/R520/R553/R554(near J6)
WCM-2012-900T_4P
12/9 Add
L36/R555/R556(near J3)
11/2 Change PN of C644 from SF000002Y00 to SF000001G00
0804 Vendor suggest.
12/10 Add C797(NV request)
(Place on Bottom side)
12/9 IO/B Pin define update
J3
PLAST_PTFZ50S3B018HR_50P-T
CONN@
10/22 Add(EMI Request)
Place close to J6
Place close to J3
8/13 Change symbol of D7/D8 to SCA00000T00(EMI Suggest)
HDMI IN
8/13 Add D46/D47SCA00000T00(EMI Suggest)
HDMI OUT
PESD5V0U2BT_SOT23-3
RCLAMP0524PATCT
9/2 Change PN of D12/D22/D46/D47 from SC300000T00 to SC300000T10
11/4 Change PN of D37 from SC1B491D000 to SCS00002000
11/4 Change PN of D15 from SCS00003600 to SCS00002000
W=40mils
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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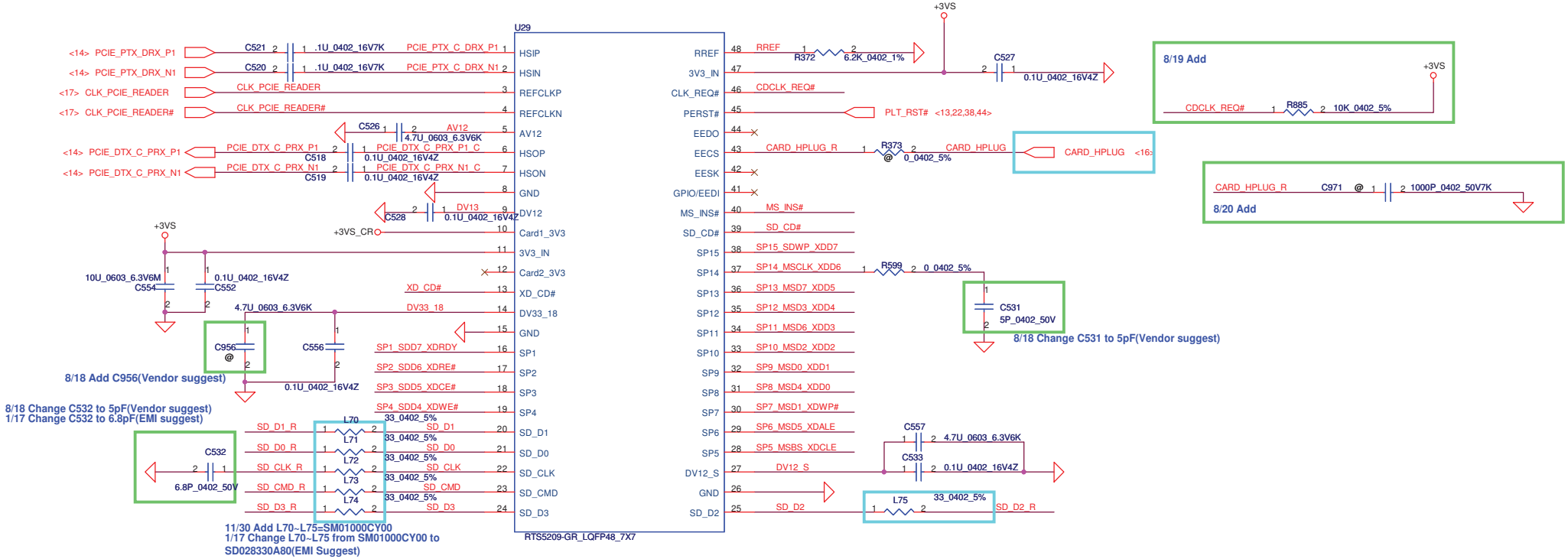
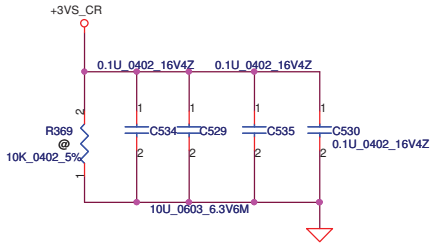
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
Rev
1.A
Date:
Thursday, February 24, 2011
Sheet
38
of
62





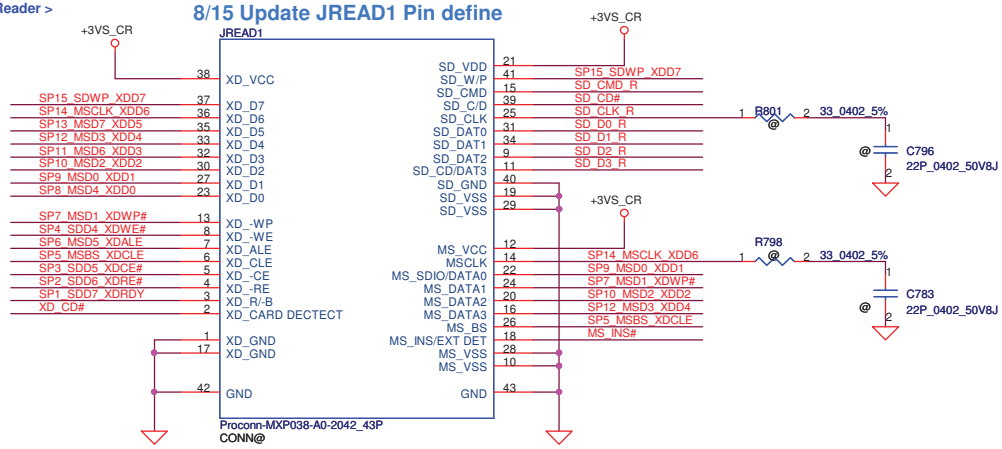
Place C534 close to socket pin 38

Place C529 close to socket pin 21

Place C535 close to socket pin 21

Place C530 close to socket pin 12

< 7 in 1 Card Reader >



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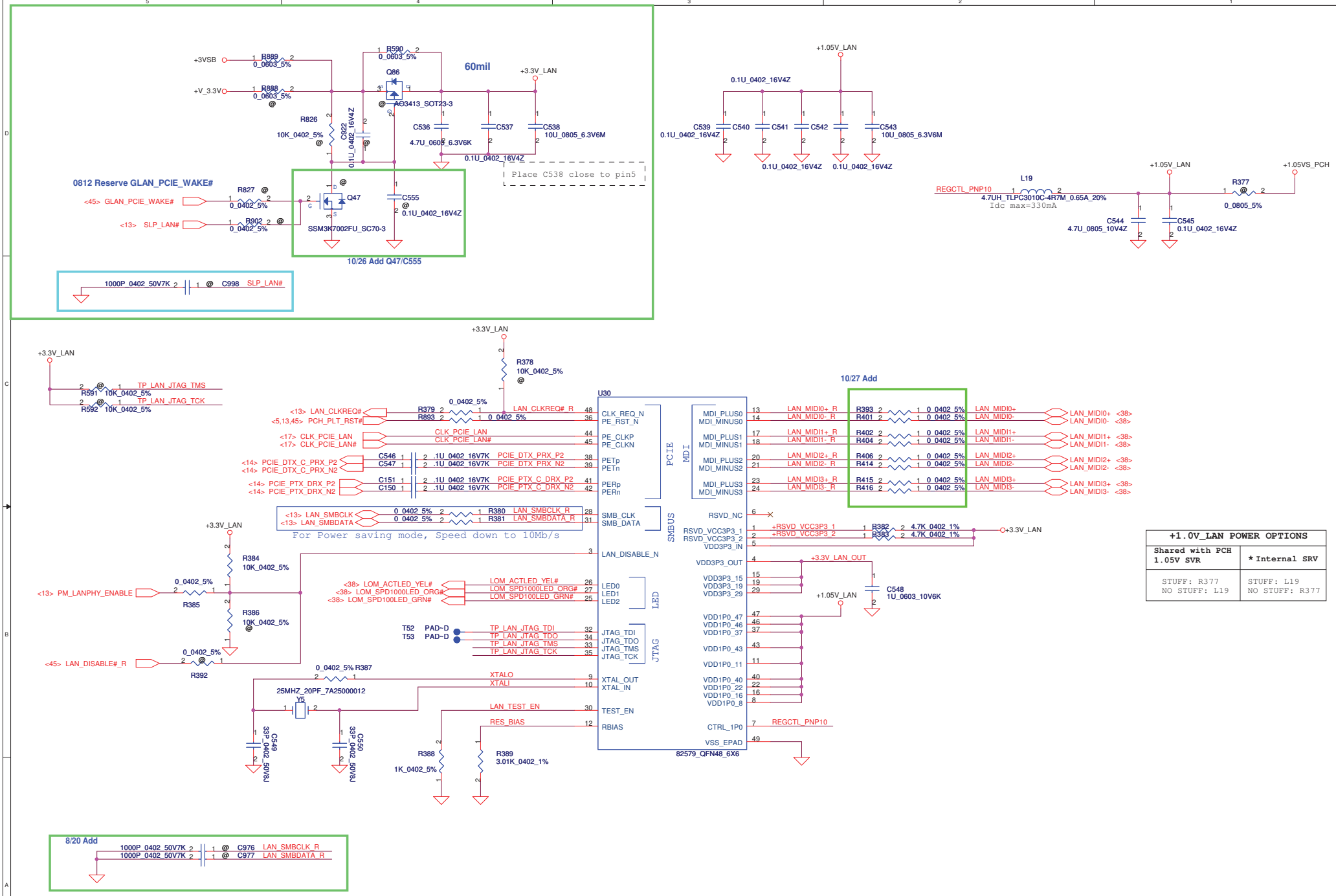
Compal Electronics, Inc.

Title: PCIE-Card Reader-RTS5209

Size | Document Number: PLA00 M/B LA-6953P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 39 of 62



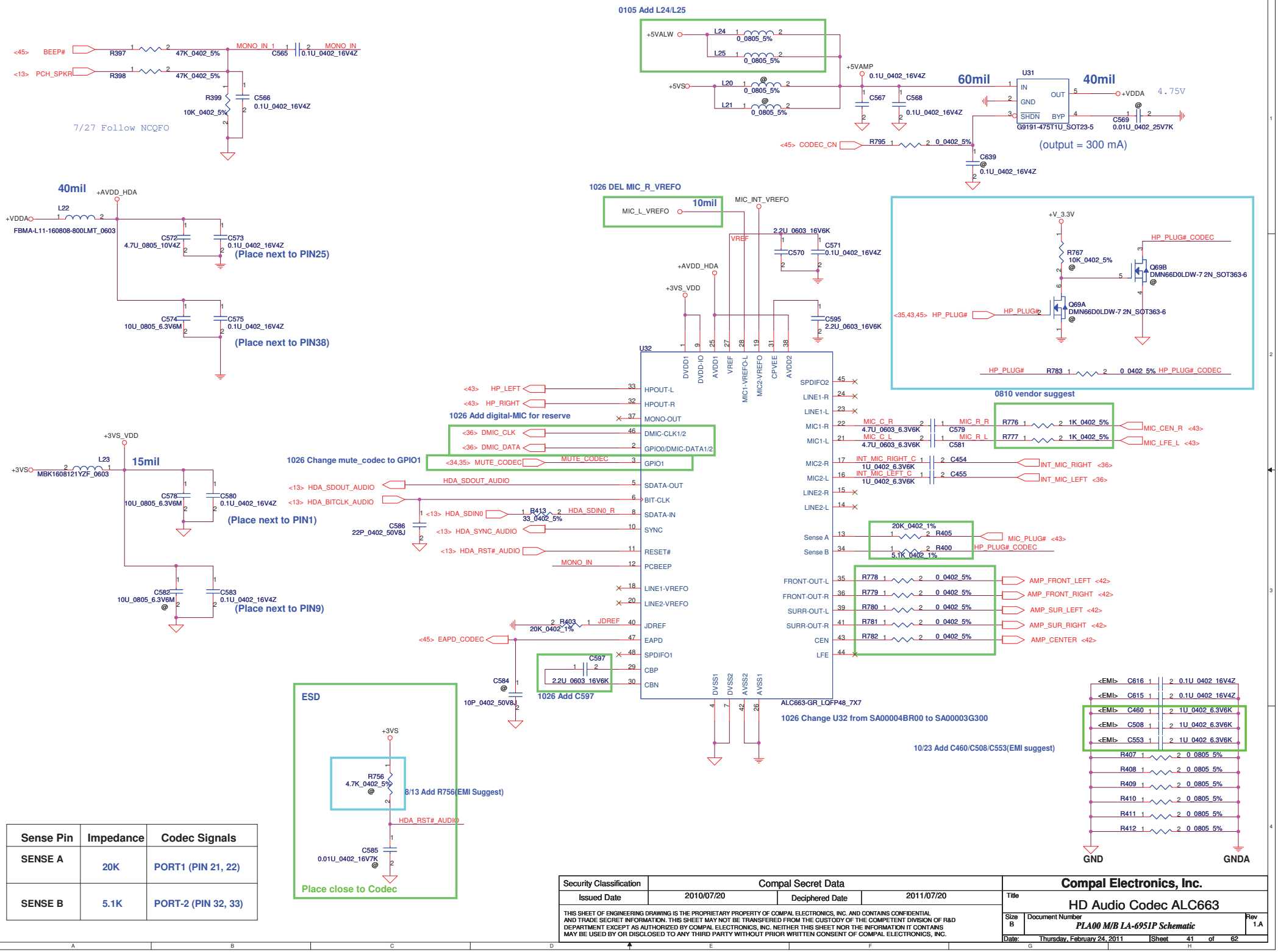
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Intel LAN-82579

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 40 of 62



Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

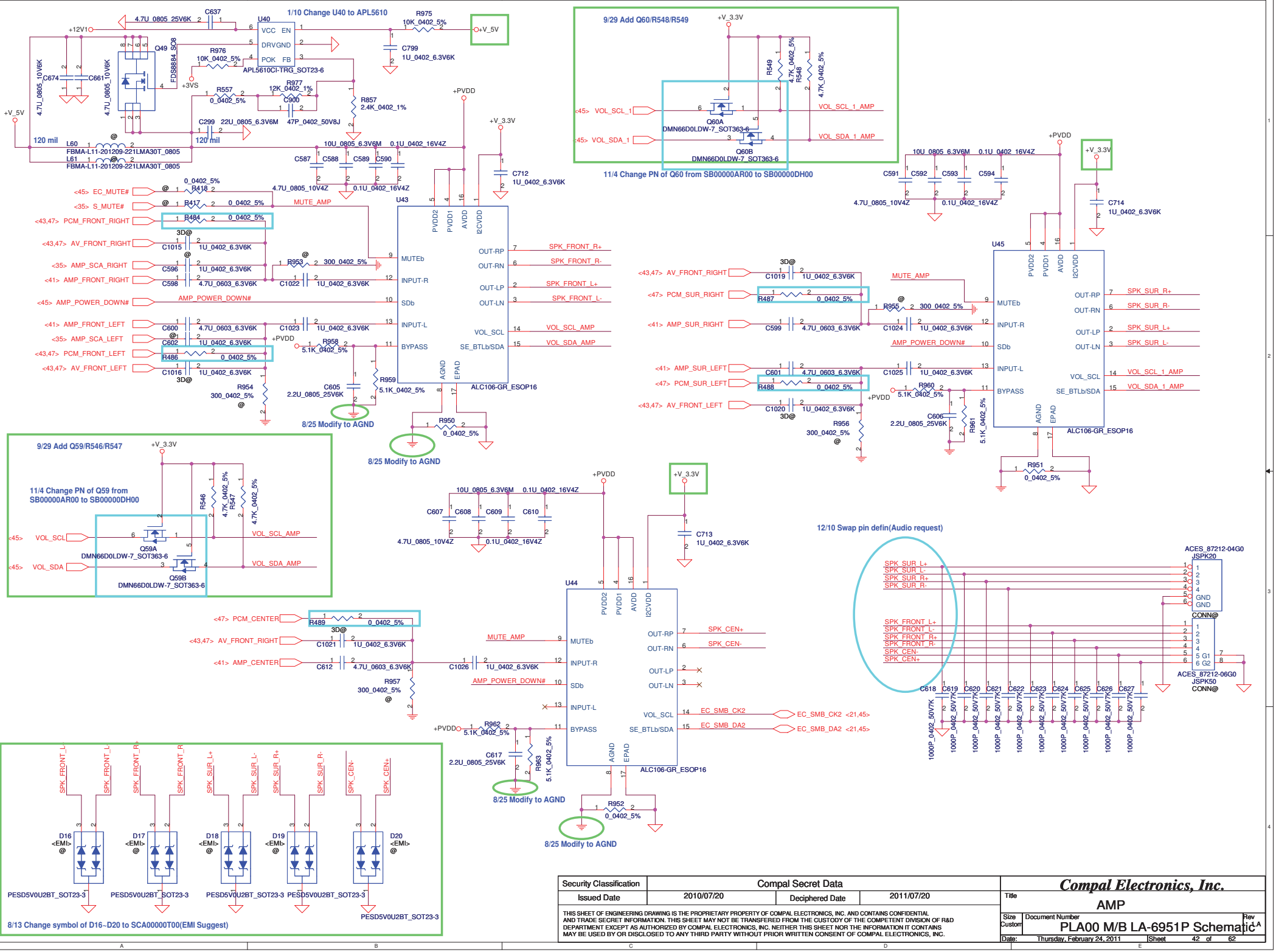
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: HD Audio Codec ALC663

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 41 of 62



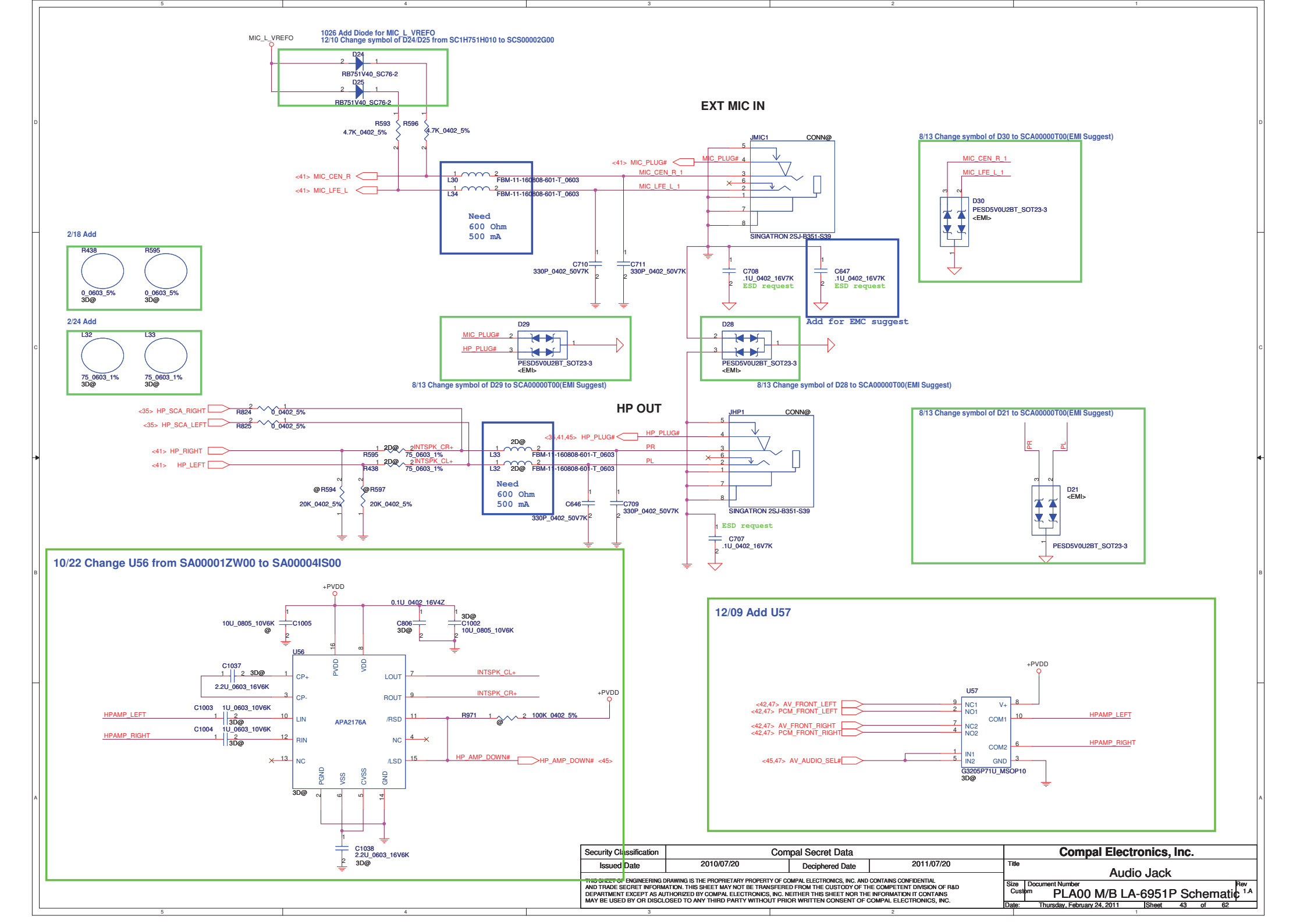
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: AMP

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 42 of 62


MIC_L_VREFO
1026 Add Diode for MIC_L_VREFO
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00
D24
RB751V40_SC76-2
D25
RB751V40_SC76-2
R593
4.7K_0402_5%
R596
4.7K_0402_5%
EXT MIC IN
<41> MIC_CEN_R
<41> MIC_LFE_L
L30
FBM-11-160808-601-T_0603
L34
FBM-11-160808-601-T_0603
Need
600 Ohm
500 mA
<41> MIC_PLUG#
MIC_PLUG#
MIC_CEN_R_1
MIC_LFE_L_1
JMIC1
CONN@
SINGATRON 2SJ-B351-S39
C710
330P_0402_50V7K
C711
330P_0402_50V7K
C708
.1U_0402_16V7K
ESD request
C647
.1U_0402_16V7K
ESD request
Add for EMC suggest
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)
MIC_CEN_R_1
MIC_LFE_L_1
D30
PESD5V0U2BT_SOT23-3
<EMI>
2/18 Add
R438
0_0603_5%
3D@
R595
0_0603_5%
3D@
2/24 Add
L32
75_0603_1%
3D@
L33
75_0603_1%
3D@
D29
MIC_PLUG#
HP_PLUG#
PESD5V0U2BT_SOT23-3
<EMI>
8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)
D28
PESD5V0U2BT_SOT23-3
<EMI>
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)
HP OUT
<35> HP_SCA_RIGHT
<35> HP_SCA_LEFT
R824
0_0402_5%
R825
0_0402_5%
<41> HP_RIGHT
<41> HP_LEFT
R595
75_0603_1%
R438
75_0603_1%
INTSPK_CR+
INTSPK_CL+
@R594
20K_0402_5%
@R597
20K_0402_5%
L33
FBM-11-160808-601-T_0603
L32
FBM-11-160808-601-T_0603
Need
600 Ohm
500 mA
<34,41,45> HP_PLUG#
HP_PLUG#
PR
PL
JHP1
CONN@
SINGATRON 2SJ-B351-S39
C646
330P_0402_50V7K
C709
330P_0402_50V7K
ESD request
C707
.1U_0402_16V7K
8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)
PR
PL
D21
<EMI>
PESD5V0U2BT_SOT23-3
10/22 Change U56 from SA00001ZW00 to SA00004IS00
+PVDD
10U_0805_10V6K
@
C1005
0.1U_0402_16V4Z
C806
3D@
3D@
C1002
10U_0805_10V6K
U56
C1037
3D@
2.2U_0603_16V6K
CP+
CP-
PVDD
VDD
LOUT
ROUT
INTSPK_CL+
INTSPK_CR+
HPAMP_LEFT
C1003
1U_0603_10V6K
3D@
LIN
APA2176A
/RSD
R971
100K_0402_5%
HPAMP_RIGHT
C1004
1U_0603_10V6K
3D@
RIN
NC
/LSD
HP_AMP_DOWN#
HP_AMP_DOWN# <45>
PGND
VSS
CVSS
GND
3D@
C1038
2.2U_0603_16V6K
3D@
12/09 Add U57
+PVDD
<42,47> AV_FRONT_LEFT
<42,47> PCM_FRONT_LEFT
<42,47> AV_FRONT_RIGHT
<42,47> PCM_FRONT_RIGHT
<45,47> AV_AUDIO_SEL#
U57
NC1
NO1
NC2
NO2
IN1
IN2
V+
COM1
COM2
GND
HPAMP_LEFT
HPAMP_RIGHT
G3205P71U_MSOP10
3D@
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Title
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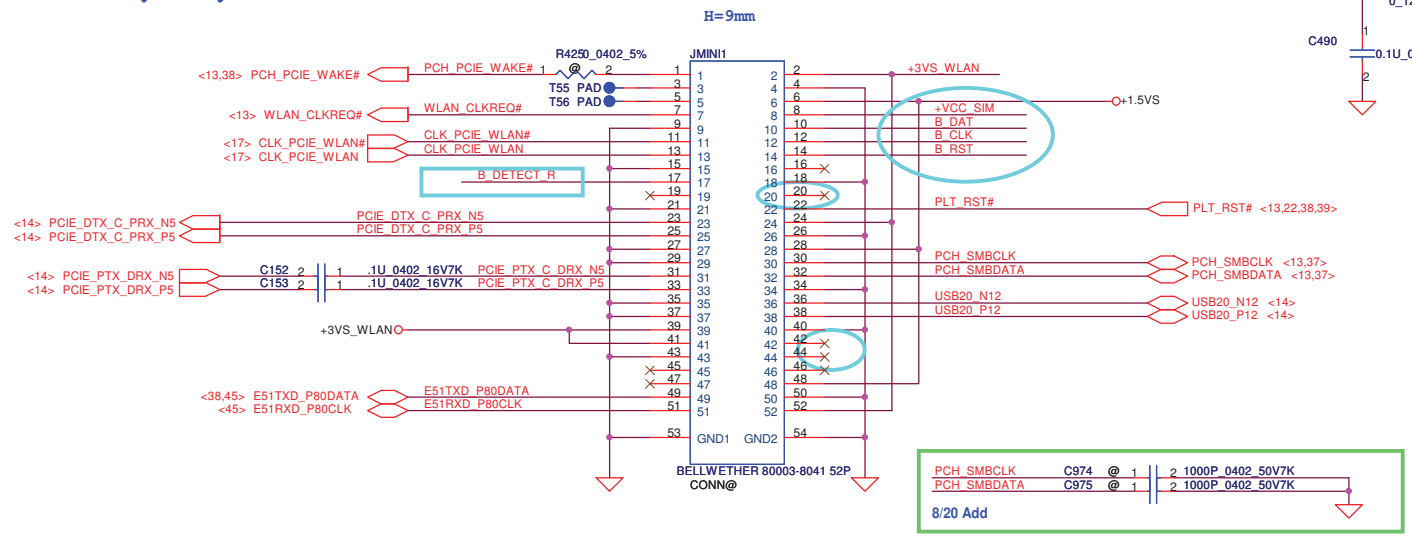
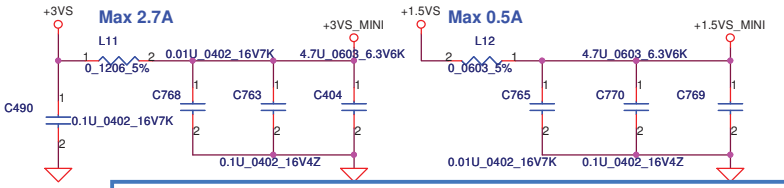
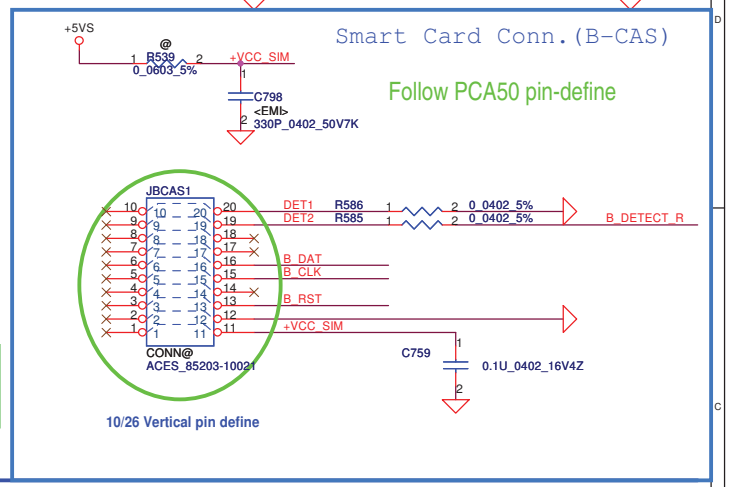
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
Rev
1.A
Date:
Thursday, February 24, 2011
Sheet
43
of
62

MINI (TV)

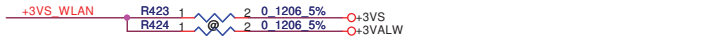
Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA

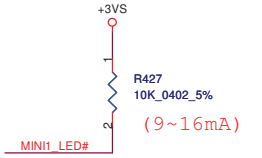


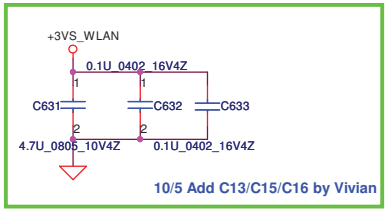


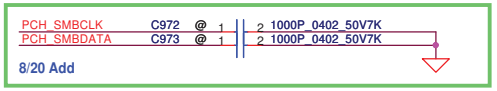


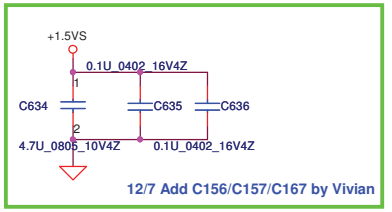
WLAN











Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **WLAN&MINI**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 44 of 62

Place closely pin 12

CLK_PCI_LPC — R444 10_0402_5% — C657 18P_0402_50V8J

Place closely pin 13

PCH_PLT_RST# — @ C658 0.1U_0402_16V4Z

1000P_0402_50V7K C650 — 0.1U_0402_16V4Z C651 — 0.1U_0402_16V4Z C652 — 0.1U_0402_16V4Z C653 — 0.1U_0402_16V4Z C654 — 0.1U_0402_16V4Z C655

+3VSB — R552 0_0603_5% — R441 0_0603_5%

+EC_AVCC — C656 0.1U_0402_16V4Z — ECAGND — R443 @ 0_0402_5%

VR_HOT# <57> — R447 @ 0_0402_5% — H_PROCHOT# <5>

H_PROCHOT#_EC — Q42 2N7002H_SOT23 — C860 47P_0402_50V8J

U46 KB930QF-A1_LQFP128_14X14

VCC VCC VCC VCC VCC VCC AVCC — GND GND GND GND AGND

GATEA20/GPIO00
KBRST#/GPIO01
SERIRQ#
LPC_FRAME#/LFRAME#
LPC_AD3/LAD3
LPC_AD2/LAD2
LPC_AD1/LAD1
LPC_AD0/LAD0
CLK_PCI_EC/PCICLK
PCIRST#/GPIO05
EC_RST#/ECRST#
EC_SCI#/GPIO0E
CLKRUN#/GPIO1D

LPC & MISC

<12> EC_GA20 — EC_GA20 1
<12> EC_KBRST# — EC_KBRST# 2
<12> SERIRQ — SERIRQ 3
<13> LPC_FRAME# — LPC_FRAME# 4
<13> LPC_AD3 — LPC_AD3 5
<13> LPC_AD2 — LPC_AD2 7
<13> LPC_AD1 — LPC_AD1 8
<13> LPC_AD0 — LPC_AD0 10
<17> CLK_PCI_LPC — CLK_PCI_LPC 12
<5,13,40> PCH_PLT_RST# — PCH_PLT_RST# 13
<12> EC_SCI# — EC_SCI# 20
<13> CLKRUN# — R925 @ 0_0402_5% — CLKRUN# R 38

+3VSB — R446 47K_0402_5% — C659 0.1U_0402_16V4Z

PWM Output

PWM0/GPIO0F — EC_OSD_PWM 21 — EC_OSD_PWM <48>
BEEP#/PWM1/GPIO10 — BEEP# 23 — BEEP# <41>
FANPWM0/GPIO12 — FAN_CPU_PWM 26 — FAN_CPU_PWM <48>
ACOFF/FANPWM1/GPIO13 — FAN_GPU_PWM 27 — FAN_GPU_PWM <48>

AD Input

BATT_TEMP/AD0/GPI38 — 63 — GFXVR_IMON — GFXVR_IMON <57>
BATT_OVP/AD1/GPI39 — 64
ADP_I/AD2/GPI3A — 65 — AD_BID
AD3/GPI3B — 66
AD4/GPI42 — 75 — IMVP_IMON
AD5/GPI43 — 76 — IMVP_IMON <57>

DA Output

DAC_BRIG/DA0/GPO3C — 68 — R762 — LSADC0 <34,35>
EN_DFAN1/DA1/GPO3D — 70 — R761 — LSADC1 <34,35>
IREF/DA2/GPO3E — 71 — R449 — LSADC2 <34,35>
DA3/GPO3F — 72 — R450 — LSADC3 <34,35>
(all 0_0402_5%)

PS2 Interface

EC_MUTE#/PSCLK1/GPIO4A — 83 — PS2_CLK — PS2_CLK <38>
USB_EN#/PSDAT1/GPIO4B — 84 — PS2_DATA — PS2_DATA <38>
CAP_INT#/PSCLK2/GPIO4C — 85 — VOL_SCL_1 — VOL_SCL_1 <42>
PSDAT2/GPIO4D — 86 — VOL_SDA_1 — VOL_SDA_1 <42>
TP_CLK/PSCLK3/GPIO4E — 87 — EC_3V5V_EN — EC_3V5V_EN <52>
TP_DATA/PSDAT3/GPIO4F — 88 — HP_AMP_DOWN# — HP_AMP_DOWN# <43>

SPI Device I/F

SDICS#/GPXIOA00 — 97 — VGATE_R — R453 2 1 0_0402_5% — VGATE — VGATE <13,57>
WOL_EN/SDICLK/GPXIOA01 — 98 — LAN_DISABLE#_R — LAN_DISABLE#_R <40>
ME_EN/SDIMOSI/GPXIOA02 — 99 — ME_FLASH <13>
LID_SW#/GPXIOD00 — 109 — SCALER_ON# <35>

SPI Flash ROM

SPIDI/MISO — 119 — EC_SI_SPI_SO — EC_SI_SPI_SO <46>
SPIDO/MOSI — 120 — EC_SO_SPI_SI — EC_SO_SPI_SI <46>
SPICLK/GPXIOB58 — 126 — SPI_CLK — R454 33_0402_5% — SPI_CLK_R <46>
SPICS# — 128 — SPI_CS# — SPI_CS# <46>

GPIO

GPIO40 — 73 — CIR_IN — R455 1 2 10K_0402_5% +3VSB — CIR_IN <48>
H_PECI/GPIO41 — 74 — H_PECI — H_PECI <5,12>
FSTCHG/GPIO50 — 89 — GLAN_PCIE_WAKE# — GLAN_PCIE_WAKE# <40>
BATT_CHG_LED#/GPIO52 — 90
CAPS_LED#/GPIO53 — 91 — BT_AUTOPAIR — SSD_DET# <37>
BATT_LOW_LED#/GPIO54 — 92 — WL_BLUE_LED# — BT_AUTOPAIR <48>
PWR_LED#/GPIO55 — 93 — PWR_ON_LED# — WL_BLUE_LED# <48>
SYSON/GPIO56 — 95 — SYSON — PWR_ON_LED# <48>
VR_ON/XCLK32K/GPIO57 — 121 — VR_ON — SYSON <38,49,55>
AC_IN/GPIO59 — 127 — PSU_PG# — VR_ON <57>
PSU_PG# <51>

C660 @ 100P_0402_50V8J

SM Bus

EC_SMB_CK1/SCL0/GPIO44
EC_SMB_DA1/SDA0/GPIO45
EC_SMB_CK2/SCL1/GPIO46
EC_SMB_DA2/SDA1/GPIO47

<42> VOL_SCL — VOL_SCL 77
<42> VOL_SDA — VOL_SDA 78
<13> EC_SMB_CK2_M — EC_SMB_CK2_M 79
<13> EC_SMB_DA2_M — EC_SMB_DA2_M 80

GPIO

PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
SUS_PWR_DN_ACK/GPIO0D
INVT_PWM/PWM2/GPIO11
FAN_SPEED1/FANFB0/GPIO14
FANFB1/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
ON_OFF/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A

<13> PM_SLP_S3# — PM_SLP_S3# 6
<13> PM_SLP_S5# — PM_SLP_S5# 14
<13,38> EC_SMI# — EC_SMI# 15
<48> EC_ESB_INT — EC_ESB_INT 16
<48> EC_OSD_CK — 17
<48> EC_OSD_DA — 18
<13> SUS_PWR_ACK — SUS_PWR_ACK 19
<36> INVT_PWM — INVT_PWM 25
<48> FAN_CPU_SPEED — FAN_CPU_SPEED 28
<48> FAN_GPU_SPEED — FAN_GPU_SPEED 29
<38,44> E51TXD_P80DATA — E51TXD_P80DATA 30
<44> E51RXD_P80CLK — E51RXD_P80CLK 31
<50> ON/OFF — ON/OFF 32
<48> CEN_PWR_LED — CEN_PWR_LED 34
<13> SUSWARN# — SUSWARN# 36

GPO

EC_RSMRST#/GPXIOA03 — 100 — EC_RSMRST# — EC_RSMRST# <13>
EC_LID_OUT#/GPXIOA04 — 101 — VCCSA_PG — VCCSA_PG <53>
EC_ON/GPXIOA05 — 102 — EC_ON <50>
EC_SWI#/GPXIOA06 — 103 — EC_SWI# <13>
ICH_PWROK/GPXIOA07 — 104 — EC_PWROK — EC_PWROK <13>
BKOFF#/GPXIOA08 — 105 — BKOFF# — BKOFF# <36>
RF_OFF#/GPXIOA09 — 106 — WL_OFF# <44>
GPXIOA10 — 107 — EC_ID
GPXIOA11 — 108 — POWER_KEY <35>

GPI

PM_SLP_S4#/GPXIOD01 — 110 — PM_SLP_S4# <13>
ENBKL/GPXIOD02 — 112 — R461 0_0402_5% — S_BKOFF <34,35,36>
EAPD/GPXIOD03 — 114 — EAPD_CODEC <41>
EC_THERM#/GPXIOD04 — 115 — HDMI_CABLE_DET — HDMI_CABLE_DET <38>
SUSP#/GPXIOD05 — 116 — SUSP# <24,49,53,54,56,59>
PBTN_OUT#/GPXIOD06 — 117 — PBTN_OUT# <13>
EC_PME#/GPXIOD07 — 118 — 35V_PG — 35V_PG <52>

V18R — 124 — C663 4.7U_0603_6.3V6K

XCLK1 — CRY2 — C662 15P_0402_50V8J
XCLK0 — CRY1 — C664 15P_0402_50V8J
32.768KHZ_12.5PF_Q13MC14610002 Y6 — @ R463 20M_0402_5% — R467 0_0402_5% @

<13> PCH_SUSCLK

Int. K/B Matrix

KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49

UART_TX_R — 55
EC_MUTE# — 56 — <42> EC_MUTE#
AMP_POWER_DOWN# — 57 — <42> AMP_POWER_DOWN#
CVBS_SYNC_DET — 58 — <34,35,38> CVBS_SYNC_DET
HDMI_SYNC_DET — 59 — <34,35> HDMI_SYNC_DET
HP_PLUG# — 60 — <35,41,43> HP_PLUG#
BT_RESET — 61 — <38,48> BT_RESET
J5 @ KSI7 — 62
10K_0603_5%
R451 47K_0402_5% KSO1 — 40
R452 47K_0402_5% KSO2 — 41
CODEC_CN — 42 — <41> CODEC_CN
EC_OSD_RST# — 43 — <48> EC_OSD_RST#
SOURCE_LED — 44 — <48> SOURCE_LED
EC_CAM_OFF — 45 — <36> EC_CAM_OFF
AV_AUDIO_SEL# — 46 — <43,47> AV_AUDIO_SEL#
S3_1.5VEN — 47 — <51,55> S3_1.5VEN
EC_ENVDD — 48 — <36> EC_ENVDD
3D_PWREN — 49 — <34> 3D_PWREN
PCH_ENABLE — 50 — <18> PCH_ENABLE
J8 @ 10K_0603_5% — 52 — <34,35> PANEL_STATE_OFF
UART_RX_R — 53
H_PROCHOT#_EC — 54
EC_REVPWROK — 82 — <12> EC_REVPWROK

UART_TX <15,34,35> — R474 0_0402_5% — UART_TX_R
UART_RX <15,34,35> — R485 0_0402_5% — UART_RX_R

8/15 Add

+3VSB — 4.7K_0402_5% — R968 — KSI7

10/25 Add R968

8/19 Add R884(Vendor suggest)

1K_0402_1% — R884 — PANEL_STATE_OFF

1000P_0402_50V7K C982 — EC_SMB_CK2
1000P_0402_50V7K C983 — EC_SMB_DA2

8/20 Add

EC DEBUG port

Reserve R460 for EC debug.

R460 100K_0603_5% — E51TXD_P80DATA

100P_0402_50V8J C876 — ON/OFF

+3VSB — R465 @ 10K_0402_5% — U39 @ SN74AHCT1G125GW_SOT353-5 — EC_RSMRST#
C665 @ 0.1U_0402_10V6K
R471 0_0402_5% @

+V_3.3V — R550 4.7K_0402_5% — R551 4.7K_0402_5%

EC_SMB_CK2_M — Q61A DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 <21,42>
EC_SMB_DA2_M — Q61B DMN66D0LDW-7_SOT363-6 — EC_SMB_DA2 — EC_SMB_DA2 <21,42>

11/4 Change PN of Q61 from SB00000AR00 to SB00000DH00

+3VSB — Ra — R442 100K_0402_5% AV@ — AD_BID — Rb — R445 0_0603_5% NON_AV@

LSADC0 R492 100K_0402_5%
LSADC1 R493 100K_0402_5%
LSADC2 R494 100K_0402_5%
LSADC3 R495 100K_0402_5%

10/5 Add R492~495(EC request)

9/29 Change net name from +V_5V to +5VSB

+5VSB — PS2_CLK 4.7K_0402_5% R927 — PS2_DATA 4.7K_0402_5% R928

PCH_PLT_RST# — R456 100K_0402_5%

R458 2D@ 100K_0402_5% — +3VSB
R459 3D@ 100K_0402_5%

+3VSB

VOL_SDA_1	4.7K_0402_5%		R967
VOL_SCL_1	4.7K_0402_5%		R966
EC_OSD_RST#	2.2K_0402_5%		R947
BT_RESET	4.7K_0402_5%		R941
AV_AUDIO_SEL#	4.7K_0402_5%	3D@	R936
HDMI_CABLE_DET	4.7K_0402_5%		R887
EC_OSD_CK	4.7K_0402_5%		R854
EC_OSD_DA	4.7K_0402_5%		R853
PANEL_STATE_OFF	4.7K_0402_5%	@	R497
AMP_POWER_DOWN#	4.7K_0402_5%	@	R496
EC_ESB_INT	2.2K_0402_5%		R771
GLAN_PCIE_WAKE#	100K_0402_5%		R462
ON/OFF	4.7K_0402_5%		R464
POWER_KEY	4.7K_0402_5%	@	R713
PWR_ON_LED#	8.2K_0402_5%	@	R466
VOL_SCL	4.7K_0402_5%		R468
VOL_SDA	4.7K_0402_5%		R469
WL_BLUE_LED#	8.2K_0402_5%	@	R470
EC_MUTE#	4.7K_0402_5%		R472

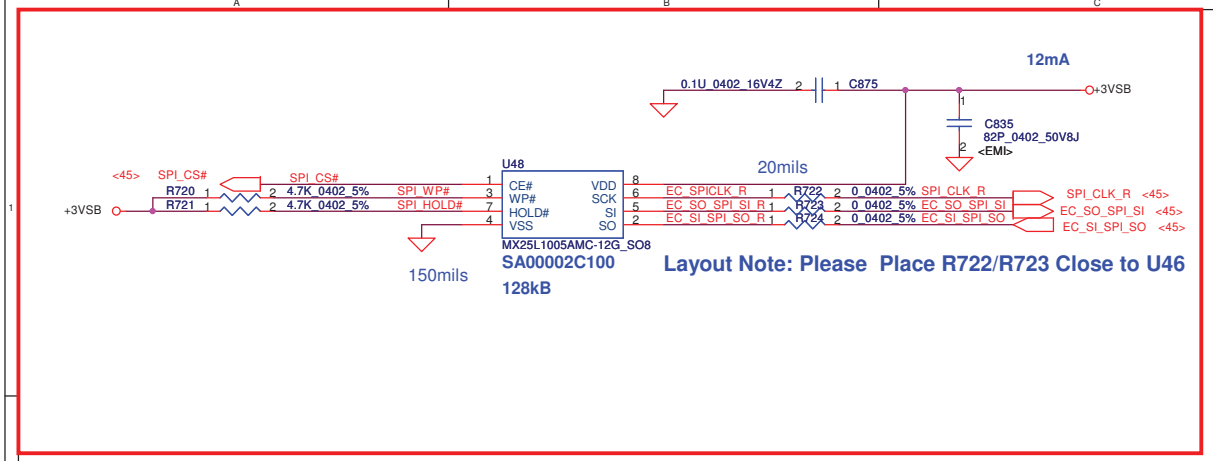
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

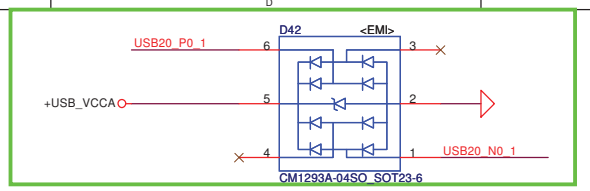
Compal Electronics, Inc.

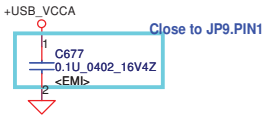
Title: EC KB930/KB conn

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

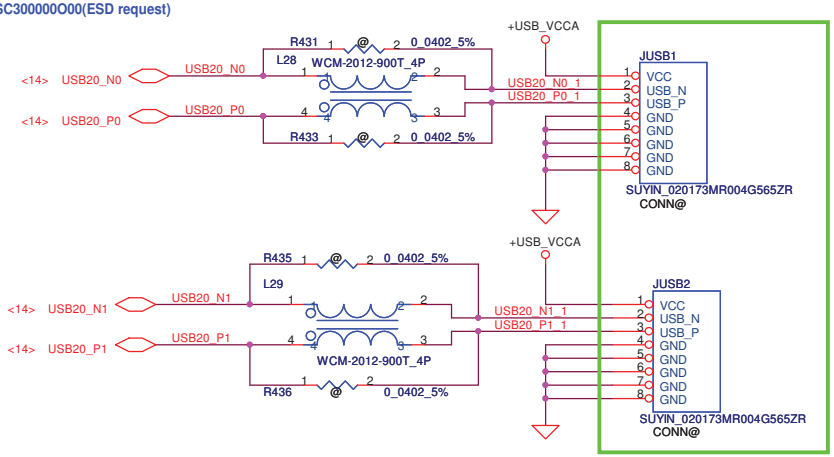
Date: Thursday, February 24, 2011 | Sheet 45 of 62





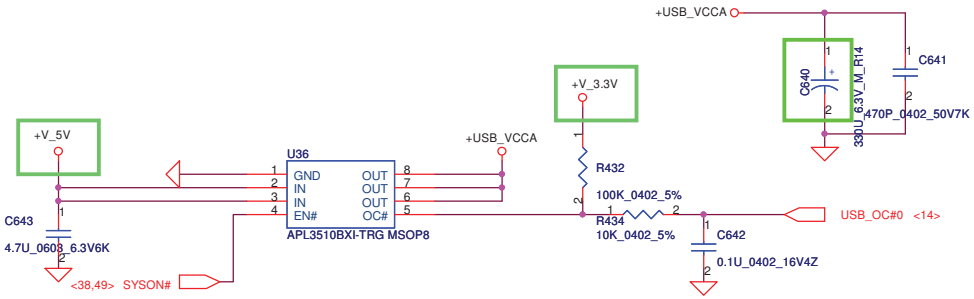


10/25 Change symbol and footprint of D42 from SC300000100 to SC300000O00(ESD request)

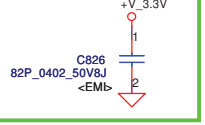


USB Conn. (SIDE)

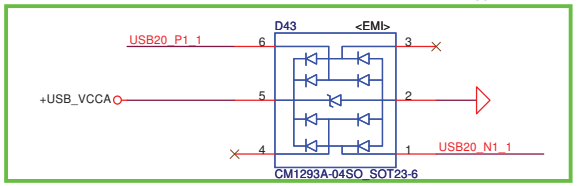
11/2 Change PN of C640 from SF000002Y00 to SF000001G00



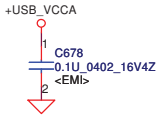
10/22 Add(EMI Request)



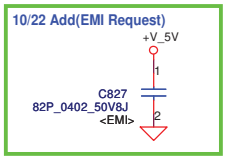
8/13 Add D43/C678(EMI Suggest)



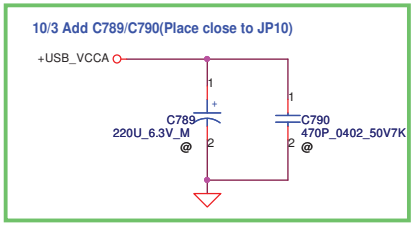
10/25 Change symbol and footprint of D43 from SC300000100 to SC300000O00(ESD request)



10/22 Add(EMI Request)



10/3 Add C789/C790(Place close to JP10)



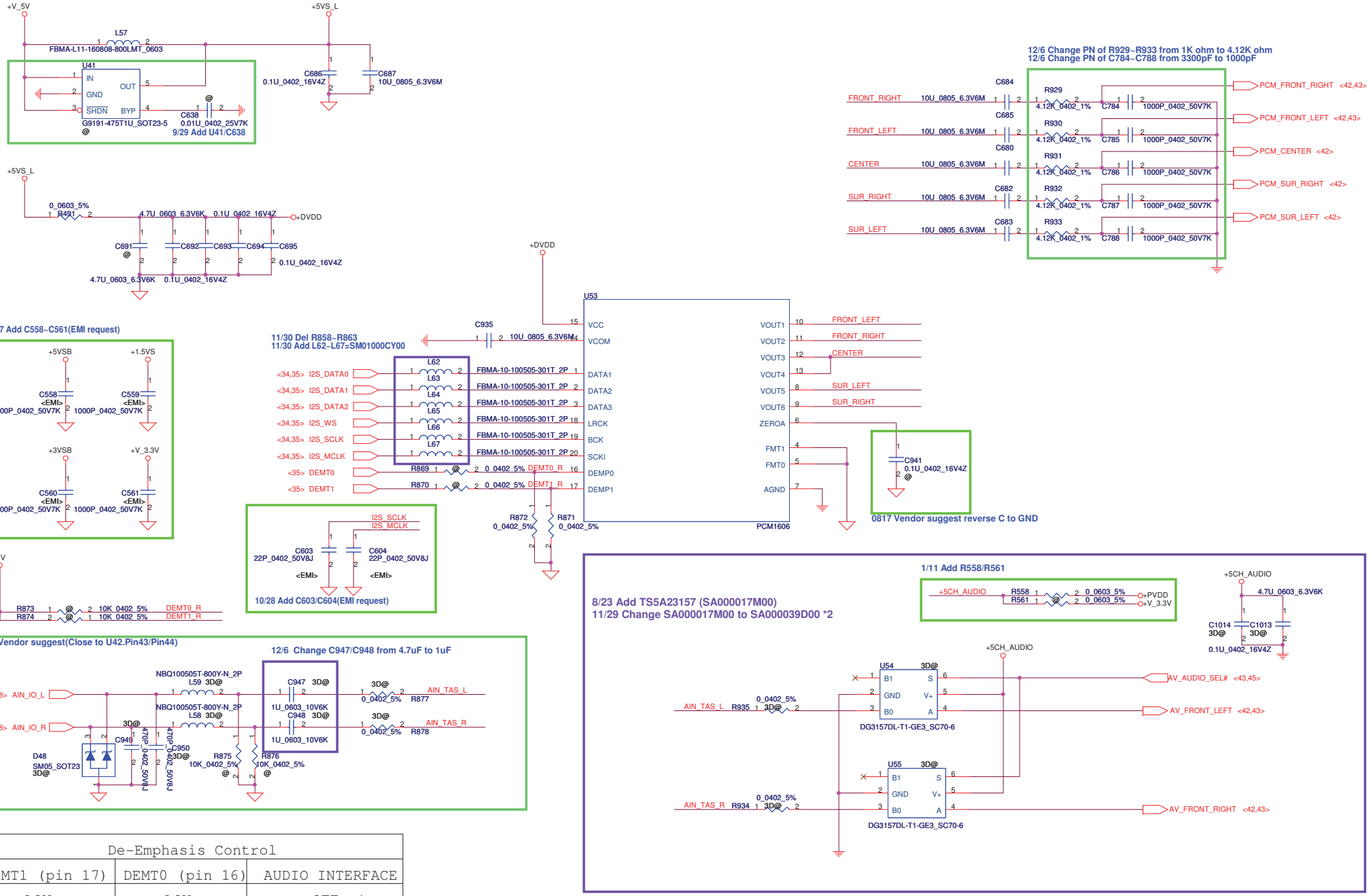
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: USB / BIOS ROM

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 46 of 62



De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

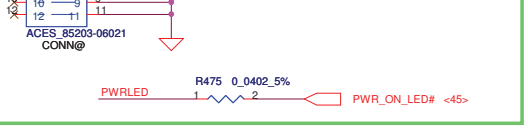
Title: 5CH AUDIO_PCM1606

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 47 of 62

Power switch board

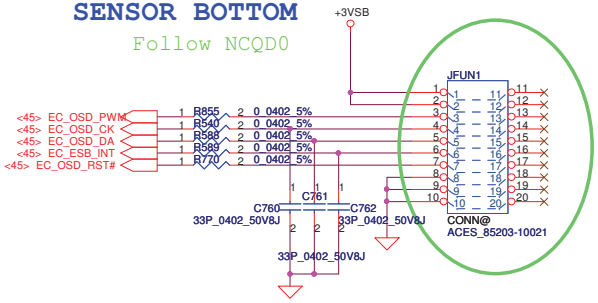
12/6 Change symbol of JPWR1 from SP02000U100 to SP01000B100



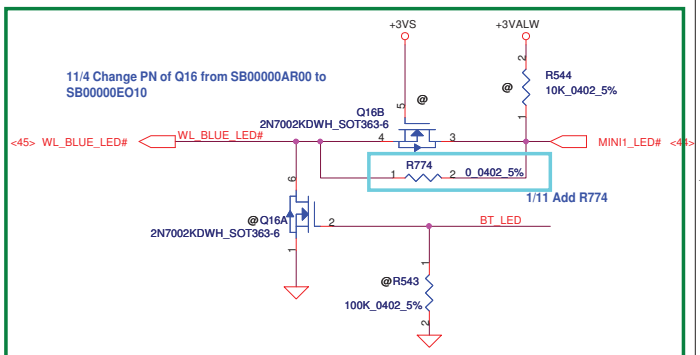
SENSOR BOTTOM

Follow NCQD0

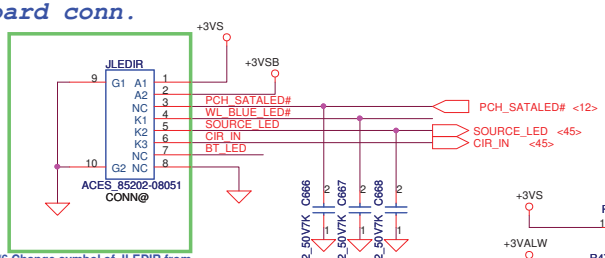
12/6 Change symbol of JFUN1 from SP02000AN00 to SP01000HE00



11/4 Change PN of Q16 from SB00000AR00 to SB00000EO10

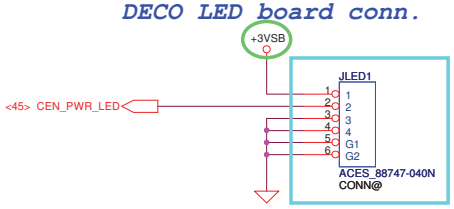


LED board conn.

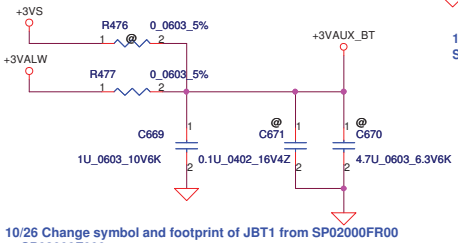


12/6 Change symbol of JLEDIR from SP020008R00 to SP01000N500

DECO LED board conn.

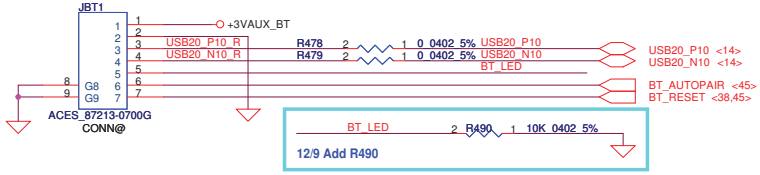


12/6 Change symbol of JLED1 from SP02000PO00 to SP010028400(3pin to 4 pin)

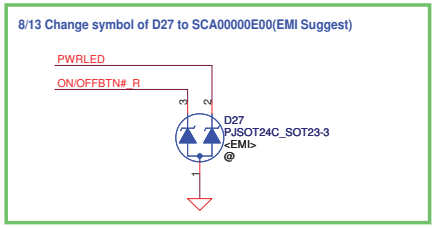


BT Connector

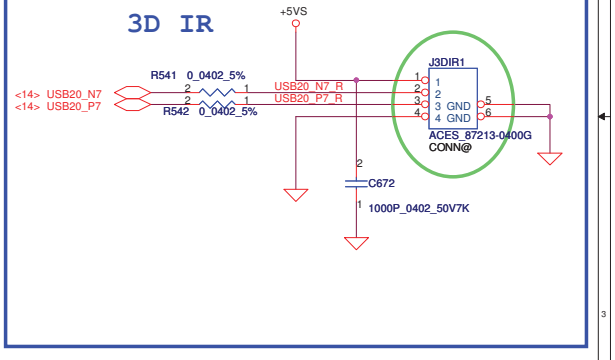
10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000



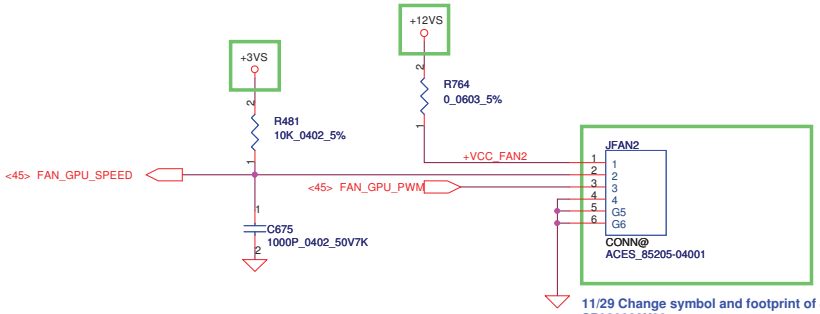
8/13 Change symbol of D27 to SCA00000E00(EMI Suggest)



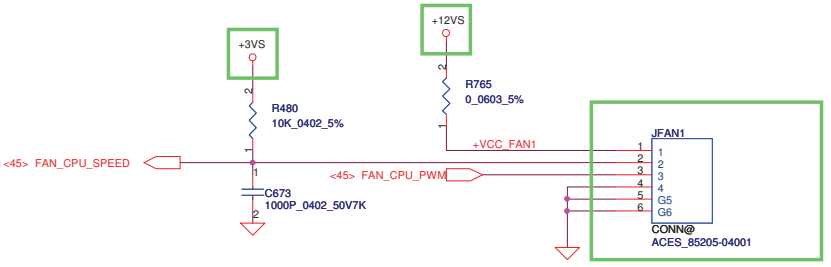
10/3 Change symbol of J3DIR1 from SP020008V00 to SP02000GC00(直立式 to R/A)



Fan Control circuit



11/29 Change symbol and footprint of JFAN2 from SP02000U900 to SP020008X00



11/29 Change symbol and footprint of JFAN1 from SP02000U900 to SP020008X00

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

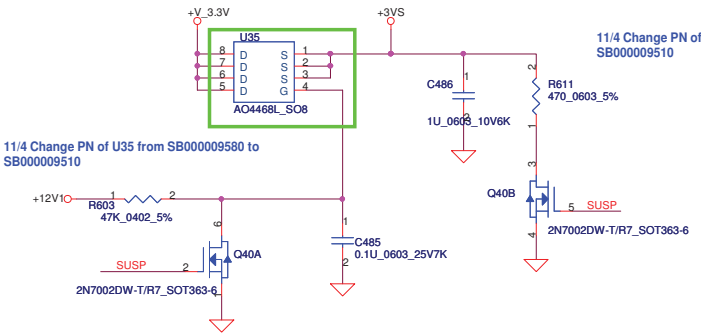
Compal Electronics, Inc.

Title: **WL/BT ON/OFF, PWR S/W, OSD**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 48 of 62

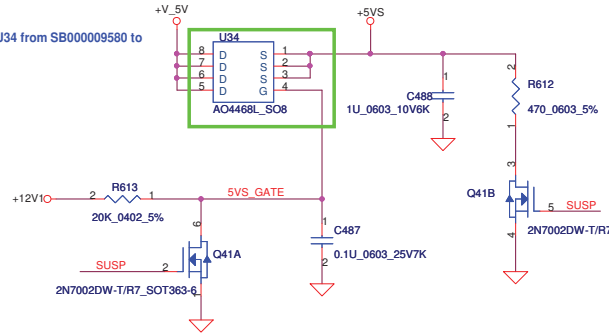
+V_3.3V TO +3VS



11/4 Change PN of U35 from SB000009580 to SB000009510

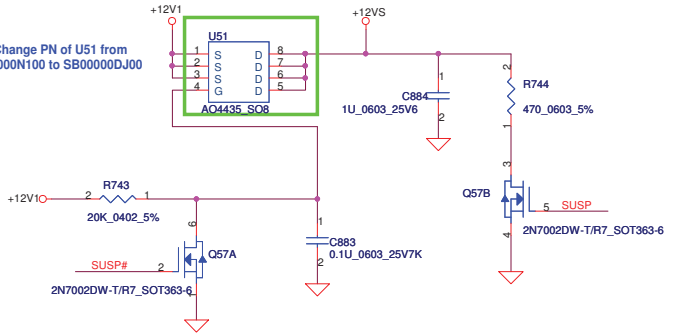
11/4 Change PN of U34 from SB000009580 to SB000009510

+V_5V TO +5VS

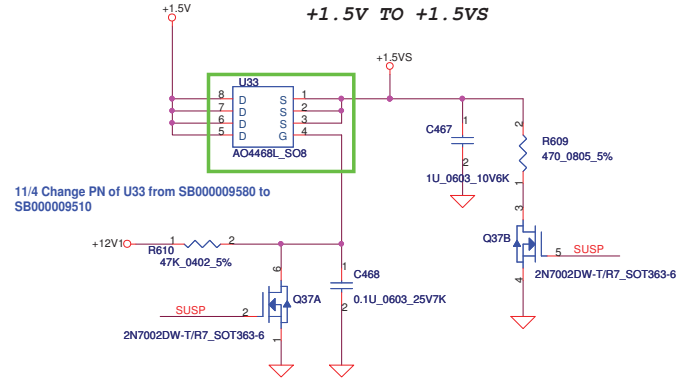


11/2 Change PN of U51 from SB00000N100 to SB00000DJ00

+12V1 TO +12VS

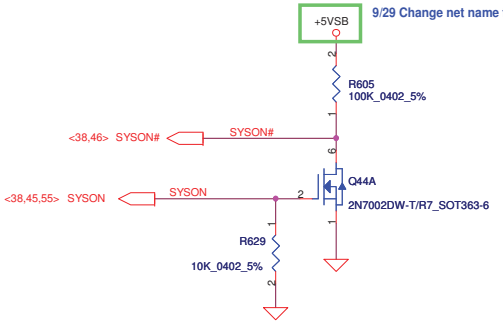


+1.5V TO +1.5VS

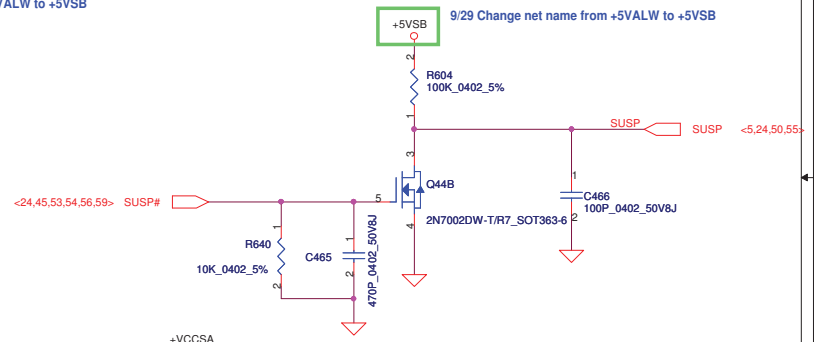


11/4 Change PN of U33 from SB000009580 to SB000009510

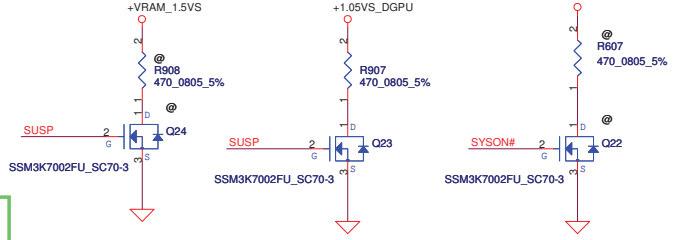
9/29 Change net name from +5VALW to +5VSB

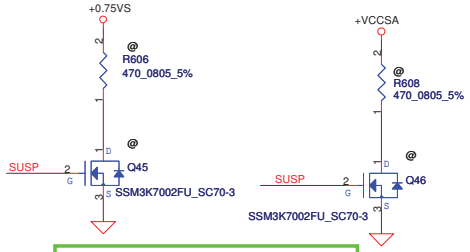


9/29 Change net name from +5VALW to +5VSB

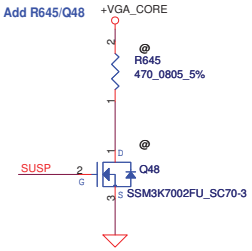


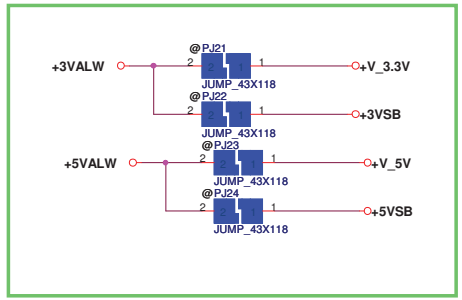
Discharge circuit



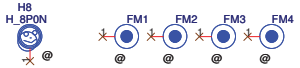


10/28 Add R645/Q48

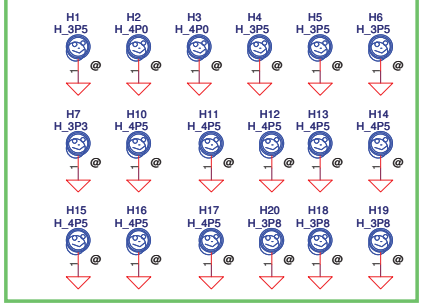




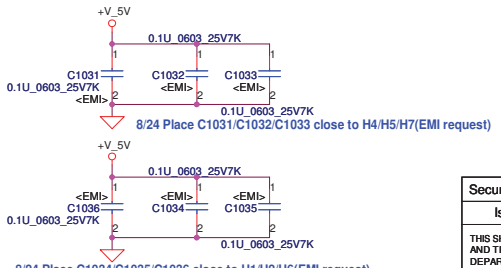
NON-PDH



Screw



8/24 Add C1031~C1036



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

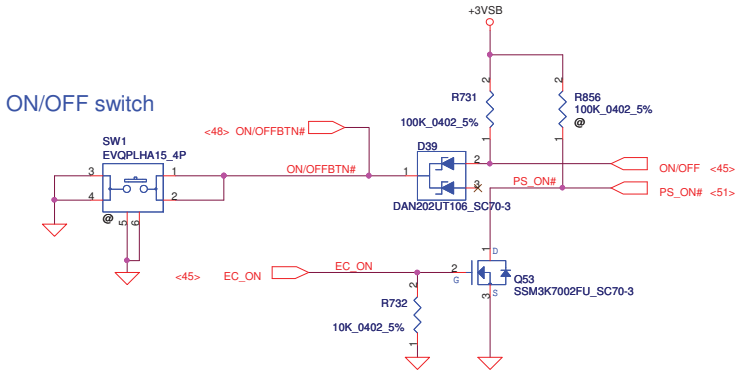
Compal Electronics, Inc.

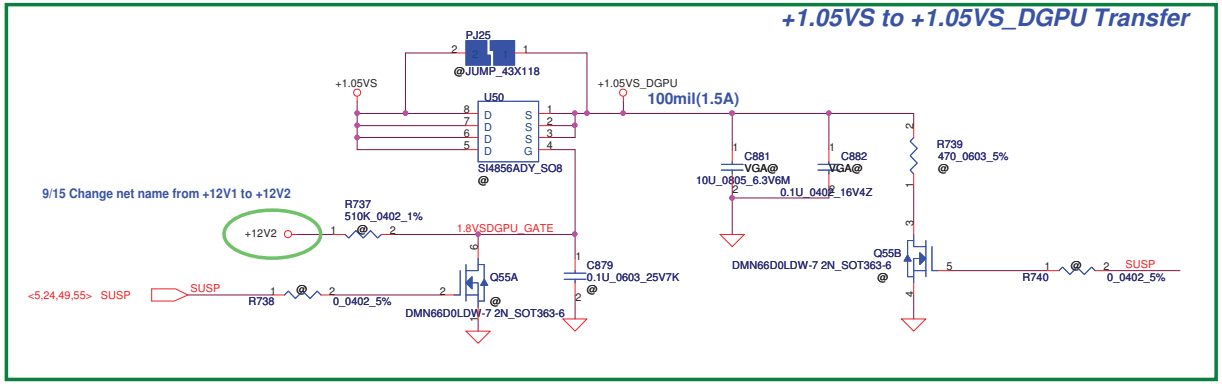
Title: DC Interface/Screw

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 49 of 62

Power Button





Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

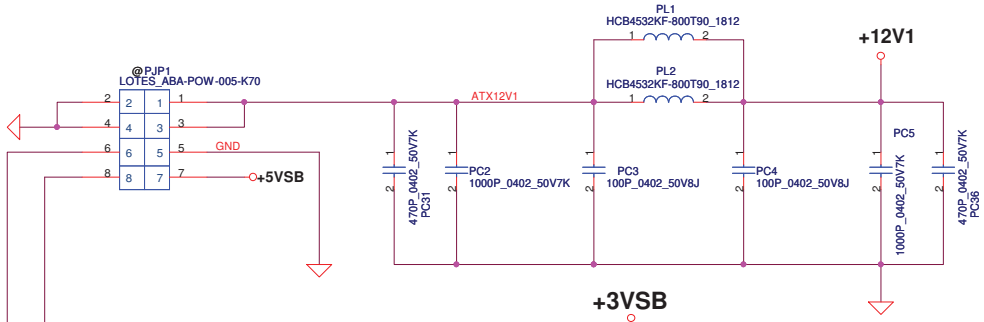
Title: Power OK/PBN

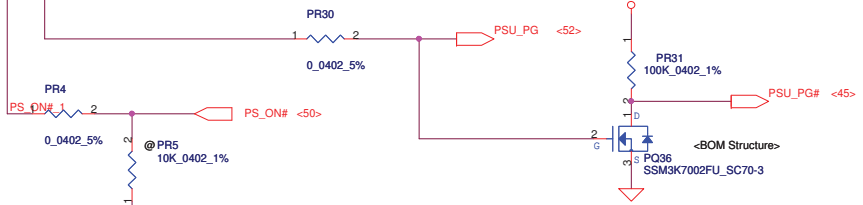
Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	1.A

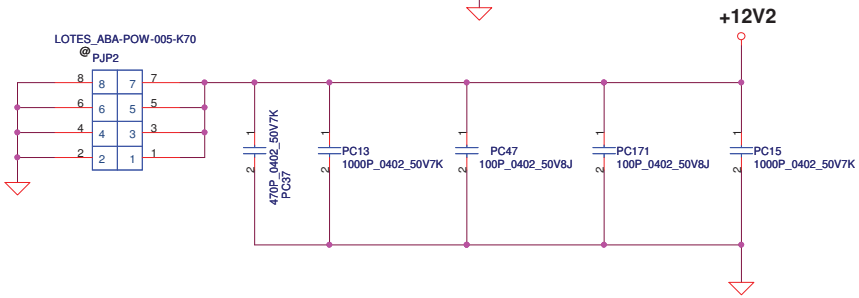
Date: Thursday, February 24, 2011 Sheet 50 of 62

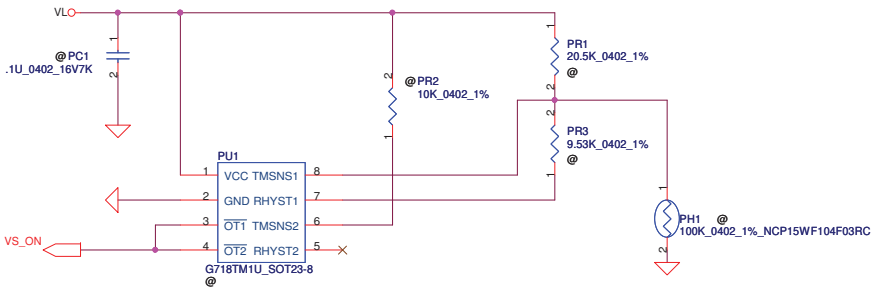
PH1 under CPU botten side :

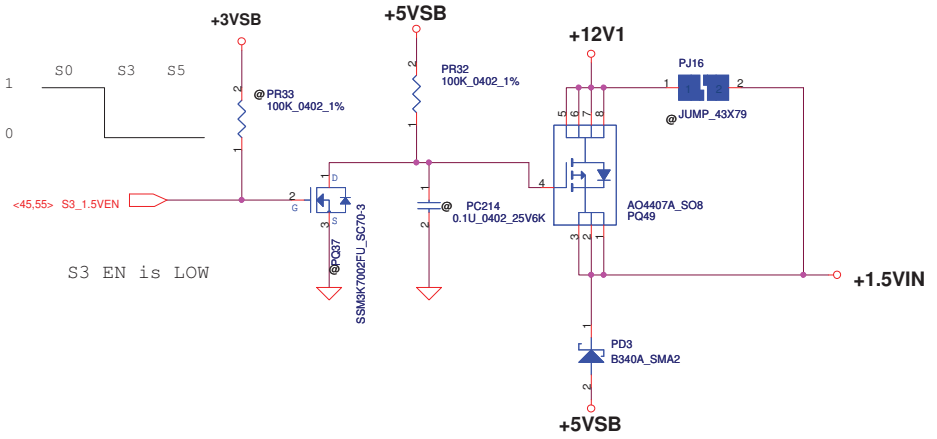
CPU thermal protection at 92 degree C
Recovery at 57 degree C

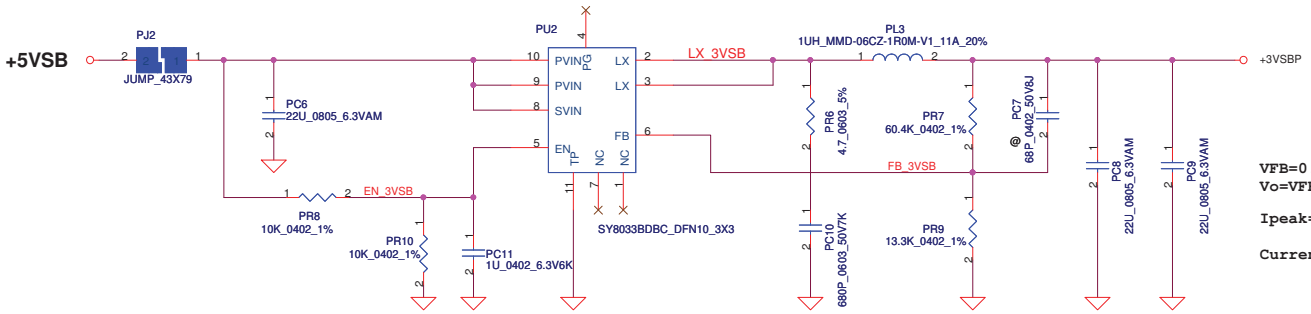










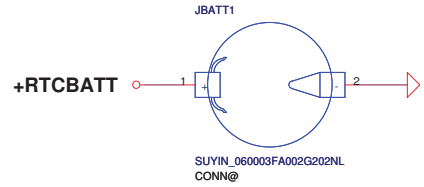


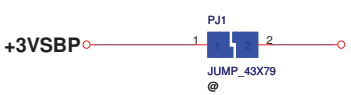
FOR EC suspend

VFB=0.6V
Vo=VFB*(1+PR7/PR9)=3.318 V

Ipeak=0.062A, Imax=0.045A

Current limit >4A





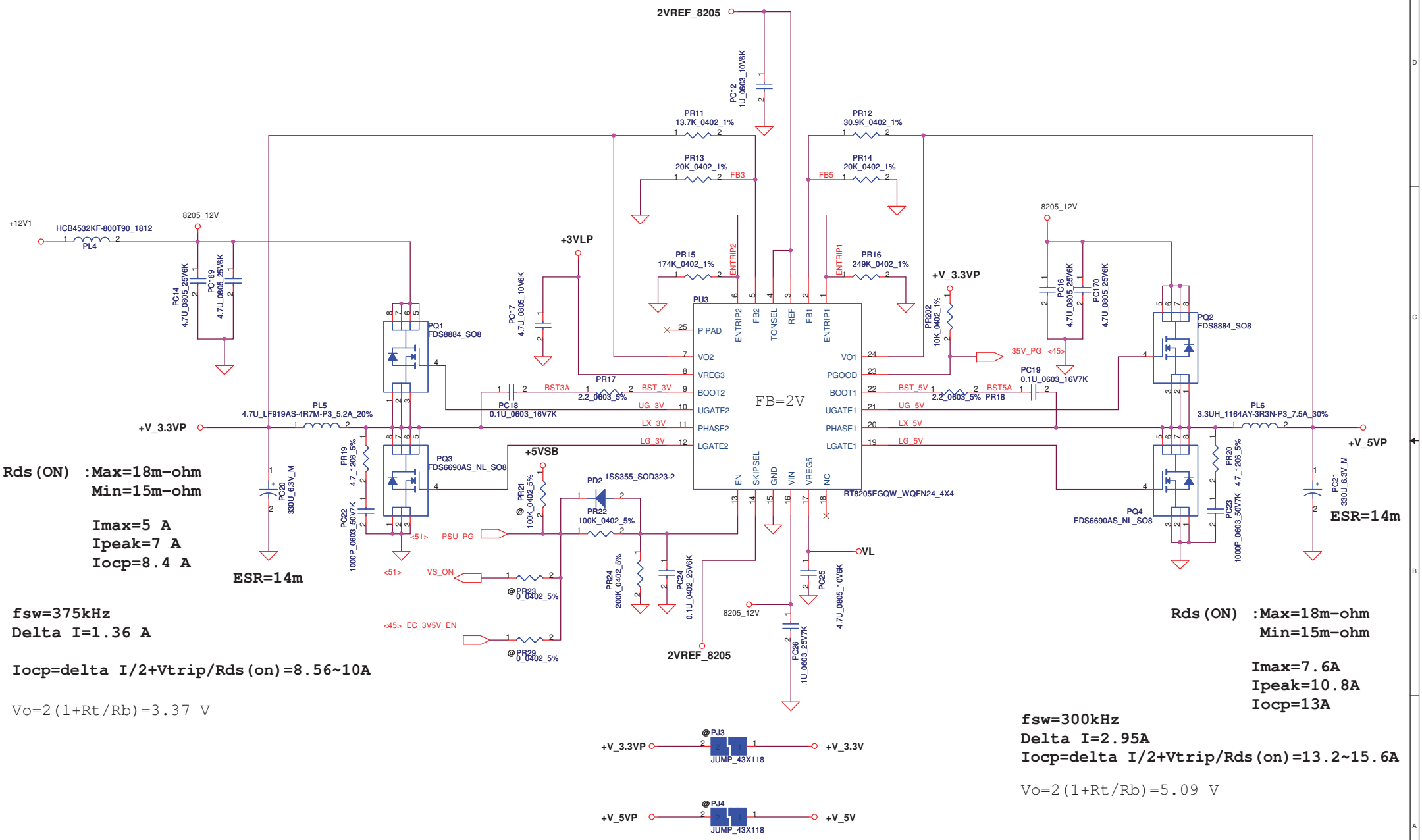
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 24, 2011 | Sheet 51 of 62



Rds(ON) :Max=18m-ohm
Min=15m-ohm

Imax=5 A
Ipeak=7 A
Iocp=8.4 A

ESR=14m

fsw=375kHz
Delta I=1.36 A

Iocp=delta I/2+Vtrip/Rds(on)=8.56~10A

Vo=2(1+Rt/Rb)=3.37 V

Rds(ON) :Max=18m-ohm
Min=15m-ohm

Imax=7.6A
Ipeak=10.8A
Iocp=13A

ESR=14m

fsw=300kHz
Delta I=2.95A
Iocp=delta I/2+Vtrip/Rds(on)=13.2~15.6A

Vo=2(1+Rt/Rb)=5.09 V

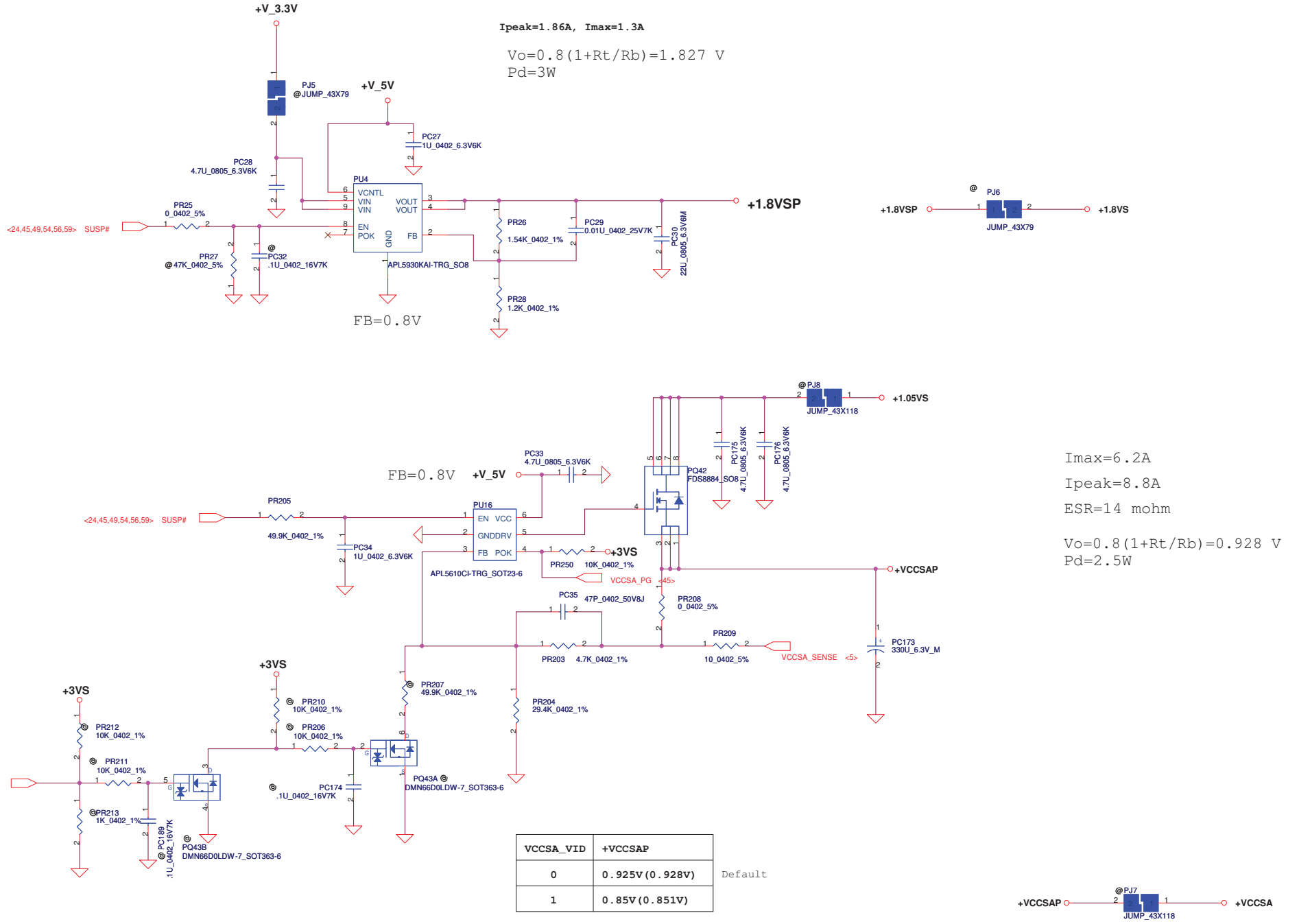
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: **+V_5VP/ +V_3VP**

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 24, 2011 | Sheet 52 of 62



VCCSA_VID	+VCCSAP	
0	0.925V(0.928V)	Default
1	0.85V(0.851V)	

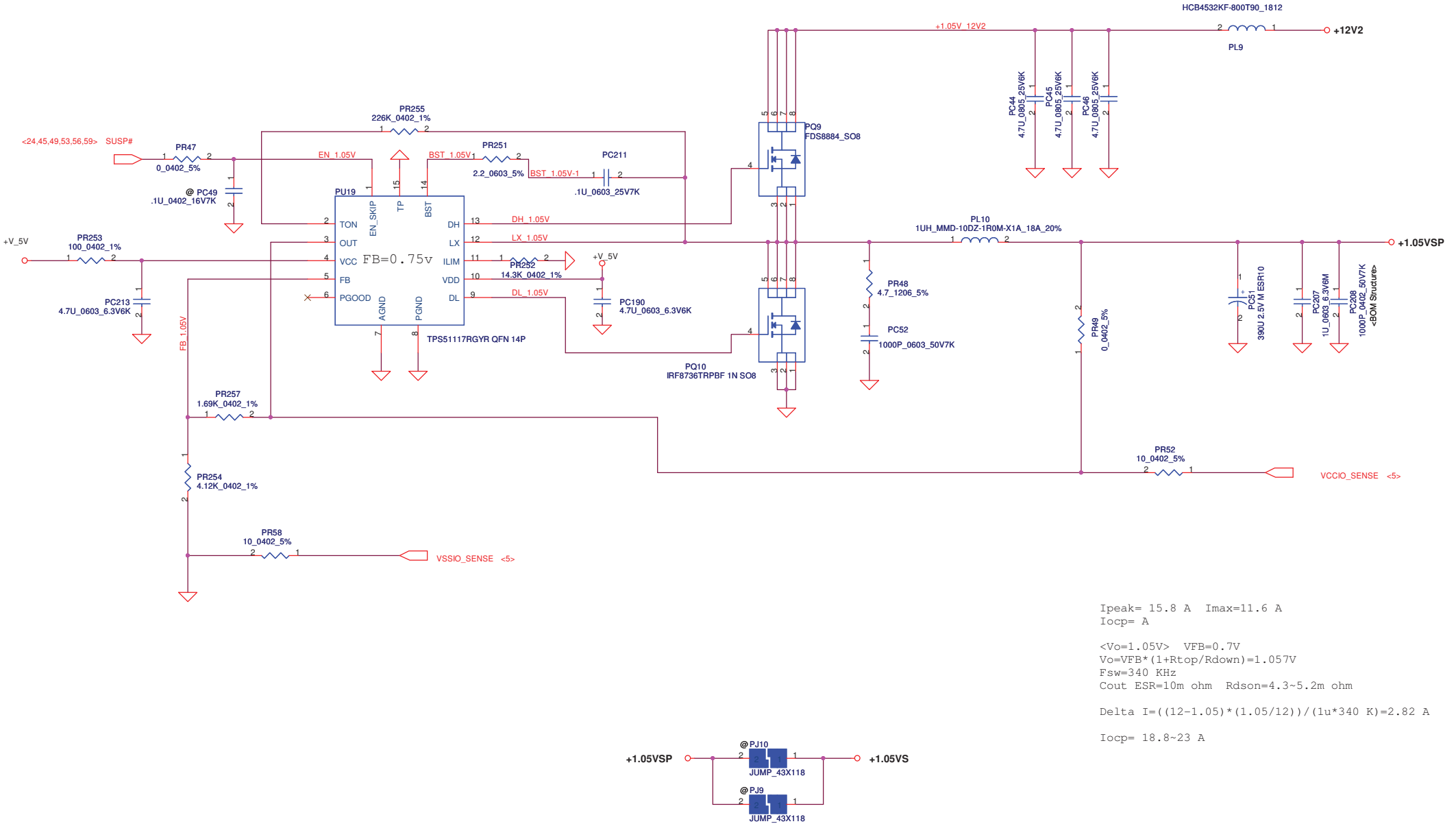
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: +VCCSA/+1.8VSP

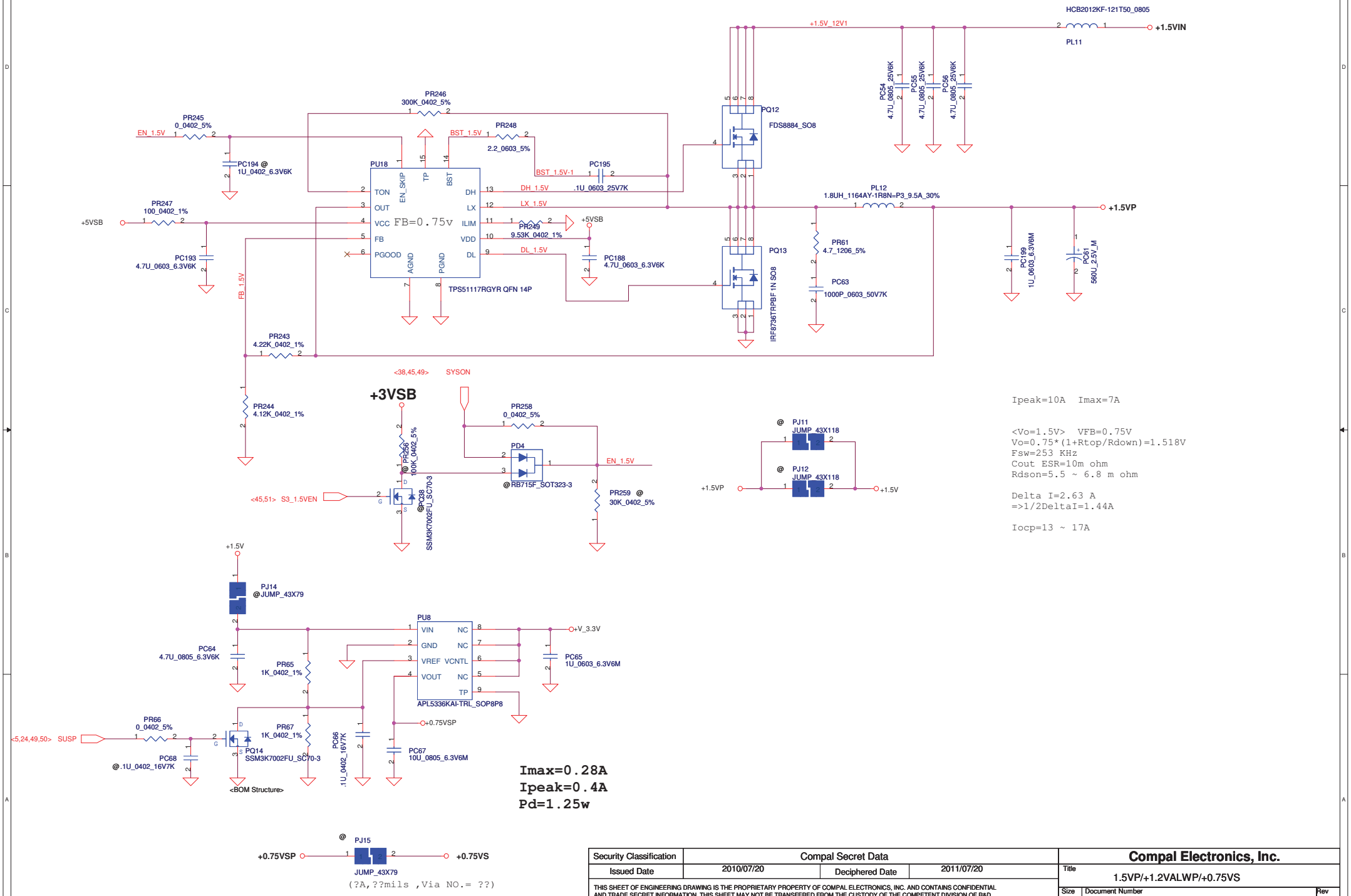
Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 24, 2011 | Sheet 53 of 62



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Title	+1.05VSP		
Size Custom	Document Number		Rev 0.1
Date: Thursday, February 24, 2011	Sheet 54 of 62		



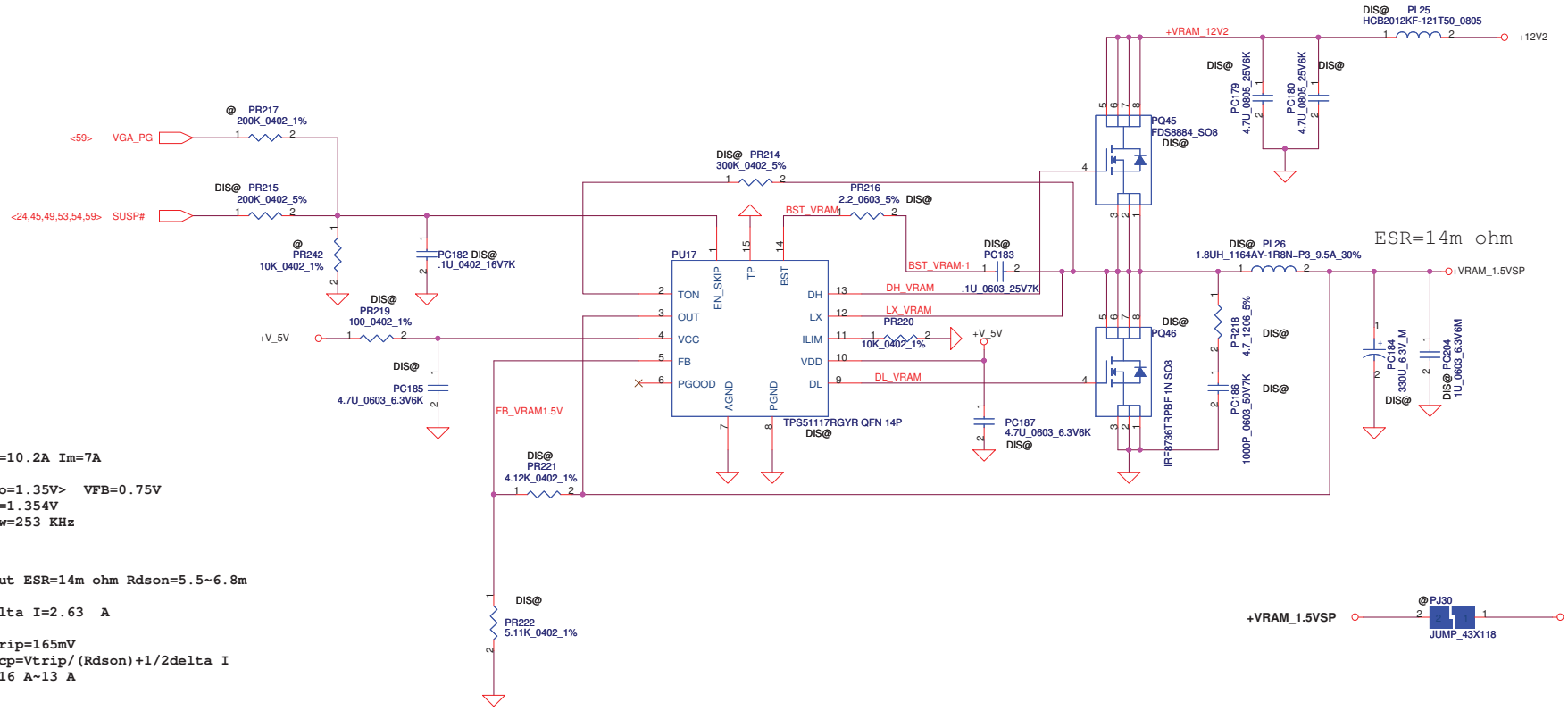
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: 1.5VP/+1.2VALWP/+0.75VS

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 24, 2011 | Sheet 55 of 62



Ip=10.2A Im=7A

<Vo=1.35V> VFB=0.75V
Vo=1.354V
Fsw=253 KHz

Cout ESR=14m ohm Rdson=5.5~6.8m

Delta I=2.63 A

Vtrip=165mV
Iocp=Vtrip/(Rdson)+1/2delta I
= 16 A~13 A

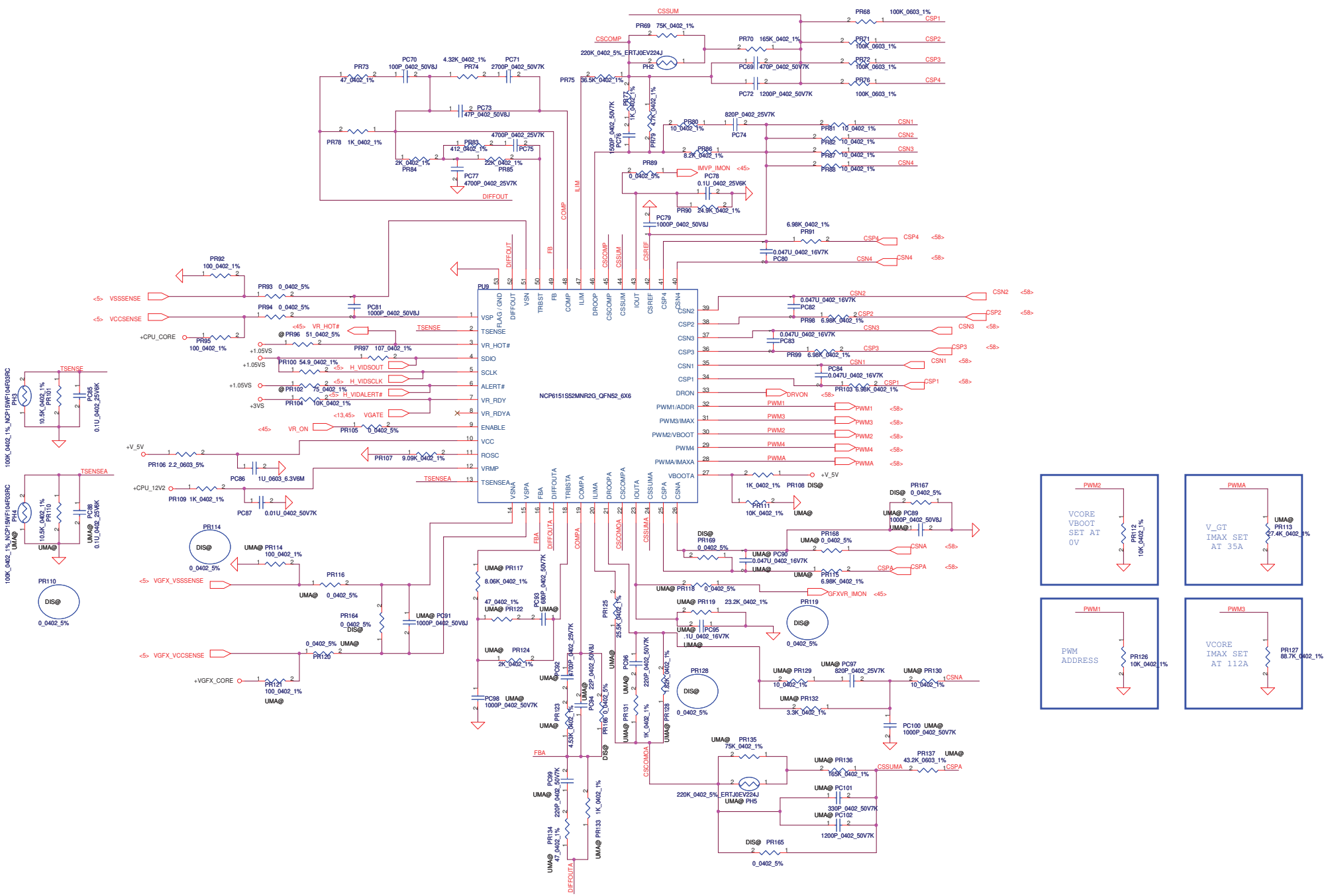
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: VCCPP/1.8VP

Size: Custom | Document Number: PLA00 M/B LA-6953P Schematic | Rev: 0.1

Date: Thursday, February 24, 2011 | Sheet 56 of 62



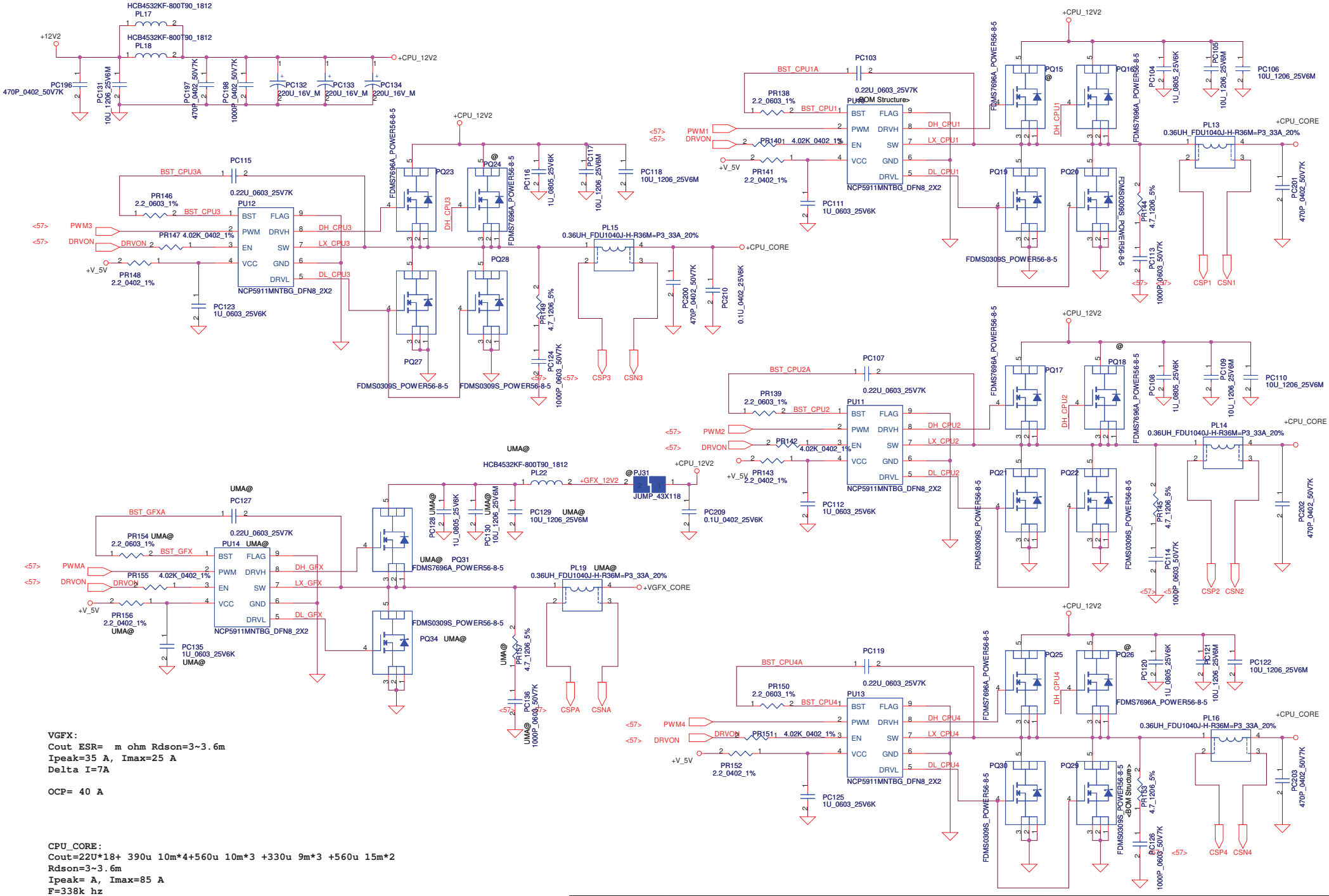
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: CPU_CORE_1

Size	Document Number	Rev
C		0.1

Date: Thursday, February 24, 2011 | Sheet 57 of 62



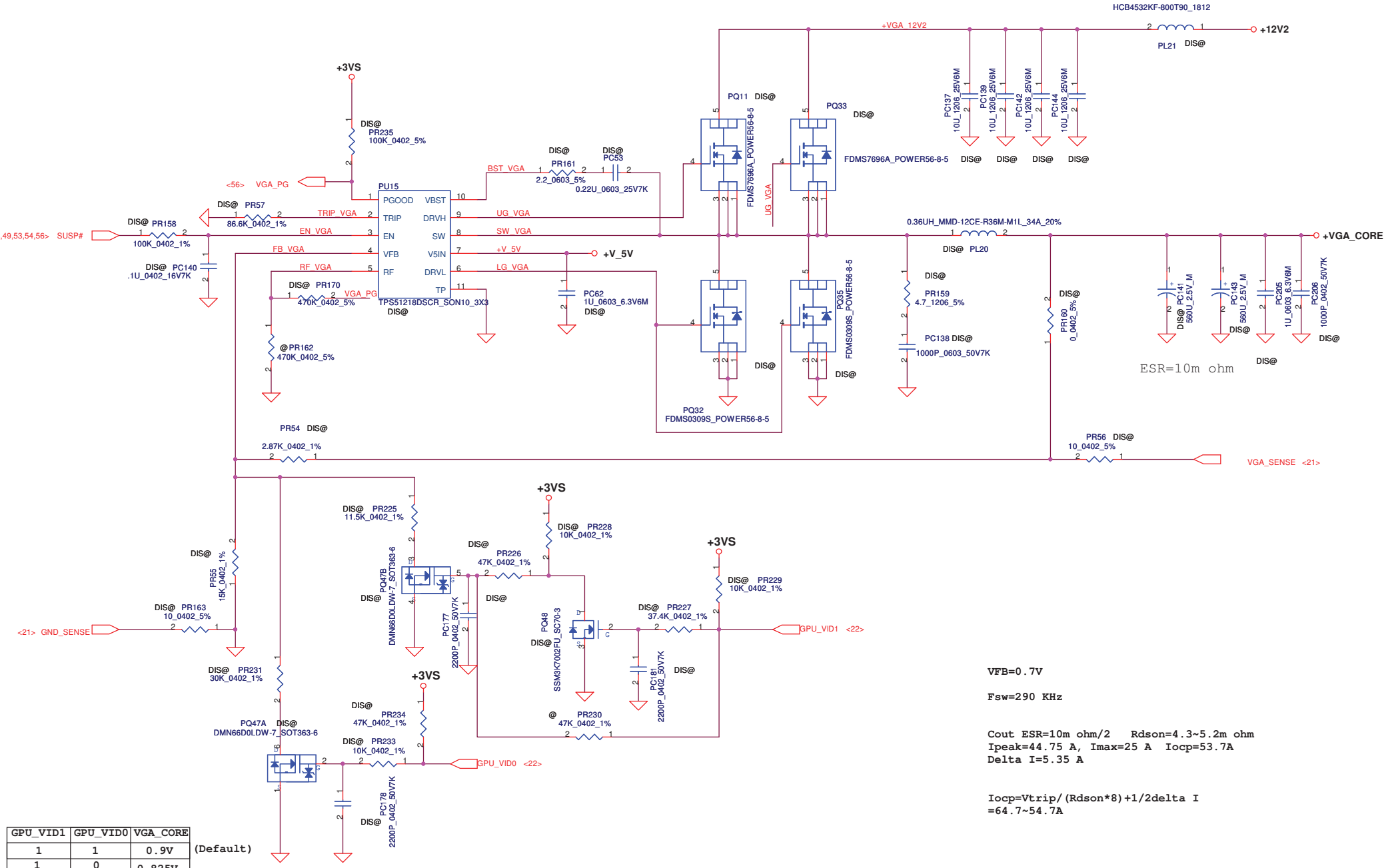
Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: CPU_CORE_2

Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 24, 2011 | Sheet 58 of 62



VFB=0.7V

Fsw=290 KHz

Cout ESR=10m ohm/2 Rdson=4.3~5.2m ohm
Ipeak=44.75 A, Imax=25 A Iocp=53.7A
Delta I=5.35 A

Iocp=Vtrip/(Rdson*8)+1/2delta I
=64.7~54.7A

GPU_VID1	GPU_VID0	VGA_CORE
1	1	0.9V (Default)
1	0	0.825V
0	1	1.075V

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

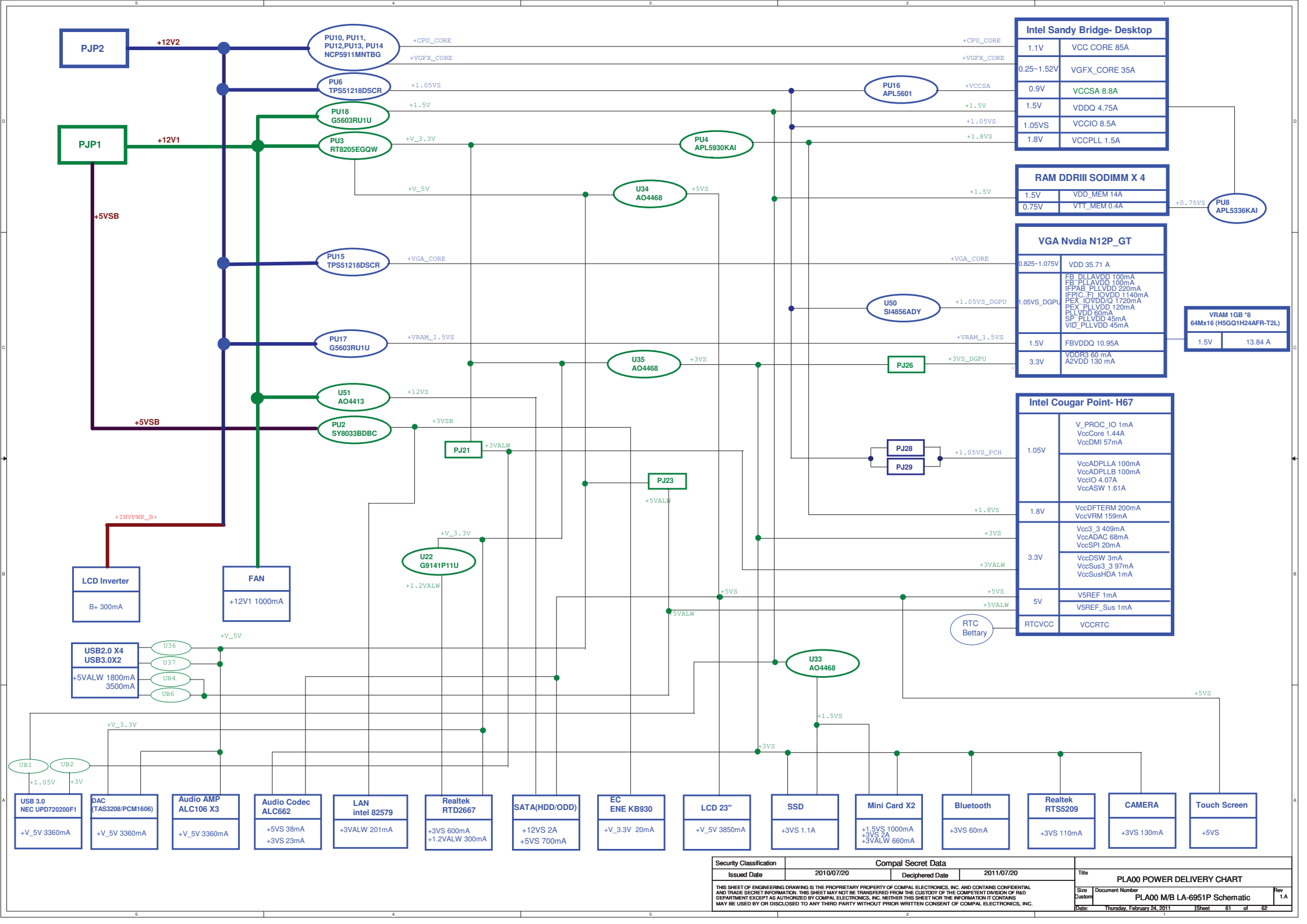
Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, February 24, 2011 | Sheet 59 of 62

Title	<Title>
Size: A	Document Number: PLA00 M/B LA-6953P Schematic
Rev: 0.1	
Date: Thursday, February 24, 2011	Sheet 60 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

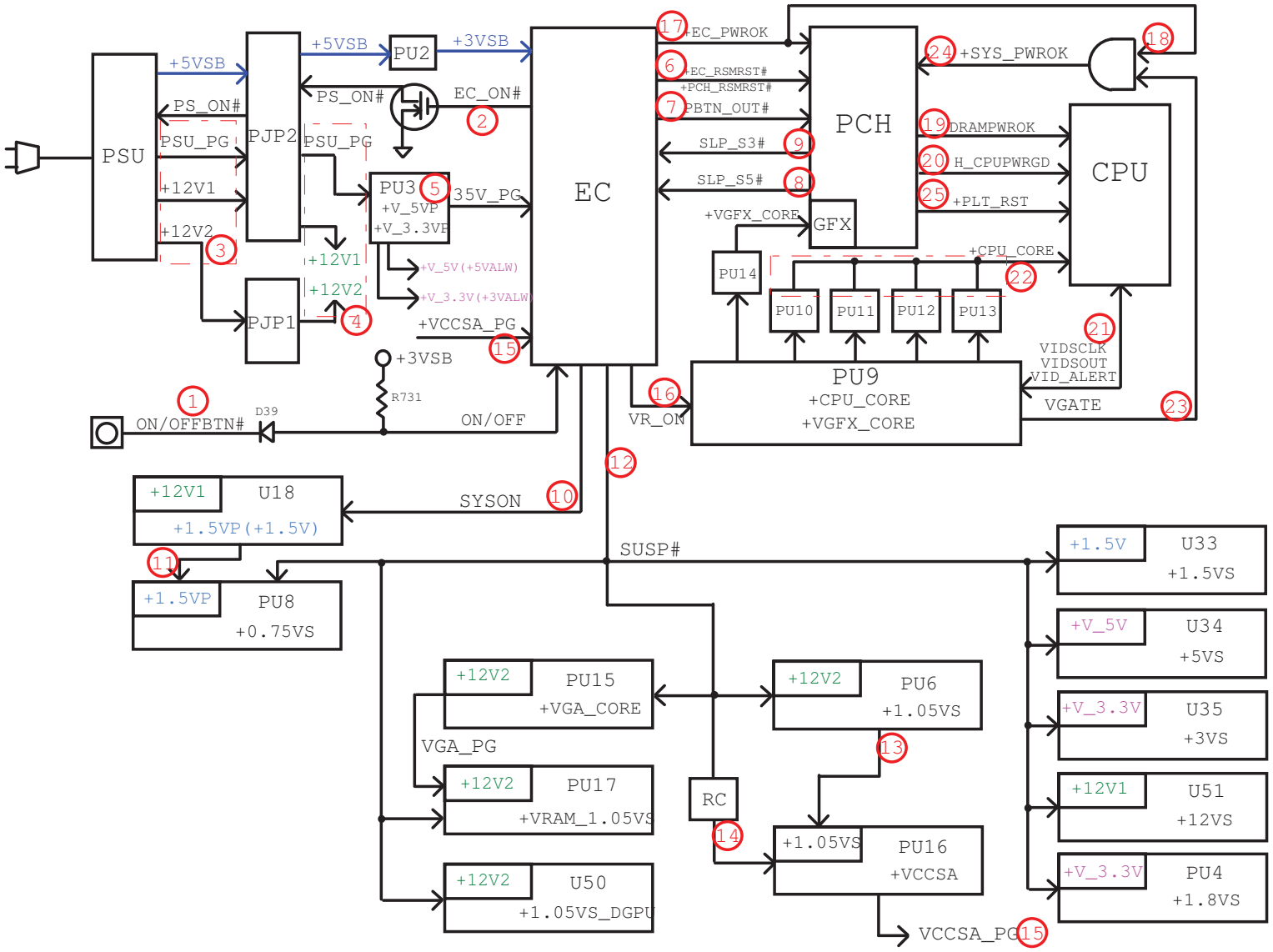
Title: PLA00 POWER DELIVERY CHART

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	1.A

Date: Thursday, February 24, 2011 | Sheet 61 of 62

COMPAL CONFIDENTIAL

MODEL NAME: *PLA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA6951P*
REVISION: *0.3*
DATE: *2010/10/26*



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.A

Date: Thursday, February 24, 2011 | Sheet 62 of 62