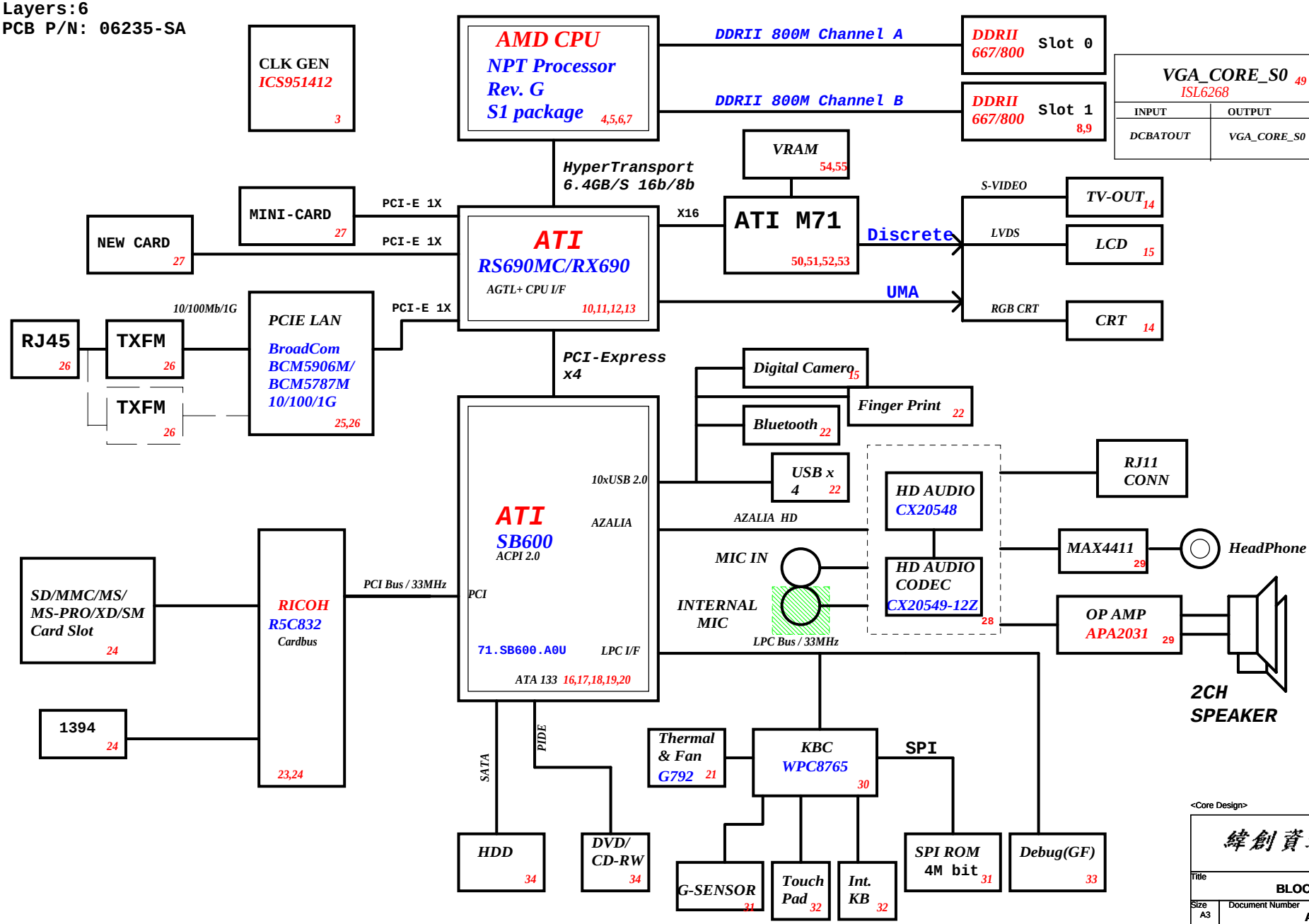
A-NOTE 2.0 Block Diagram

Project Code:91.4T001.001
Layers:6
PCB P/N: 06235-SA



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

VGA_CORE_S0 49
ISL6268

INPUT	OUTPUT
DCBATOUT	VGA_CORE_S0

Battery Charger 44
ISL6255

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 41
TPS 51120

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC 18
APL5332KAC

INPUT	OUTPUT
3D3V_S5	1D2V_S5

SYSTEM POWER 42
TPS51116

INPUT	OUTPUT
DCBATOUT	1D8V_S3 0D9V_S3

1D2V_S0 43
ISL6268

INPUT	OUTPUT
DCBATOUT	1D2V_S0

CPU V_CORE 38,39
ISL6264

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 41
TPS 51120

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA
Date: Tuesday, September 26, 2006 | Sheet 1 of 55

SA: 07/31/06 Start

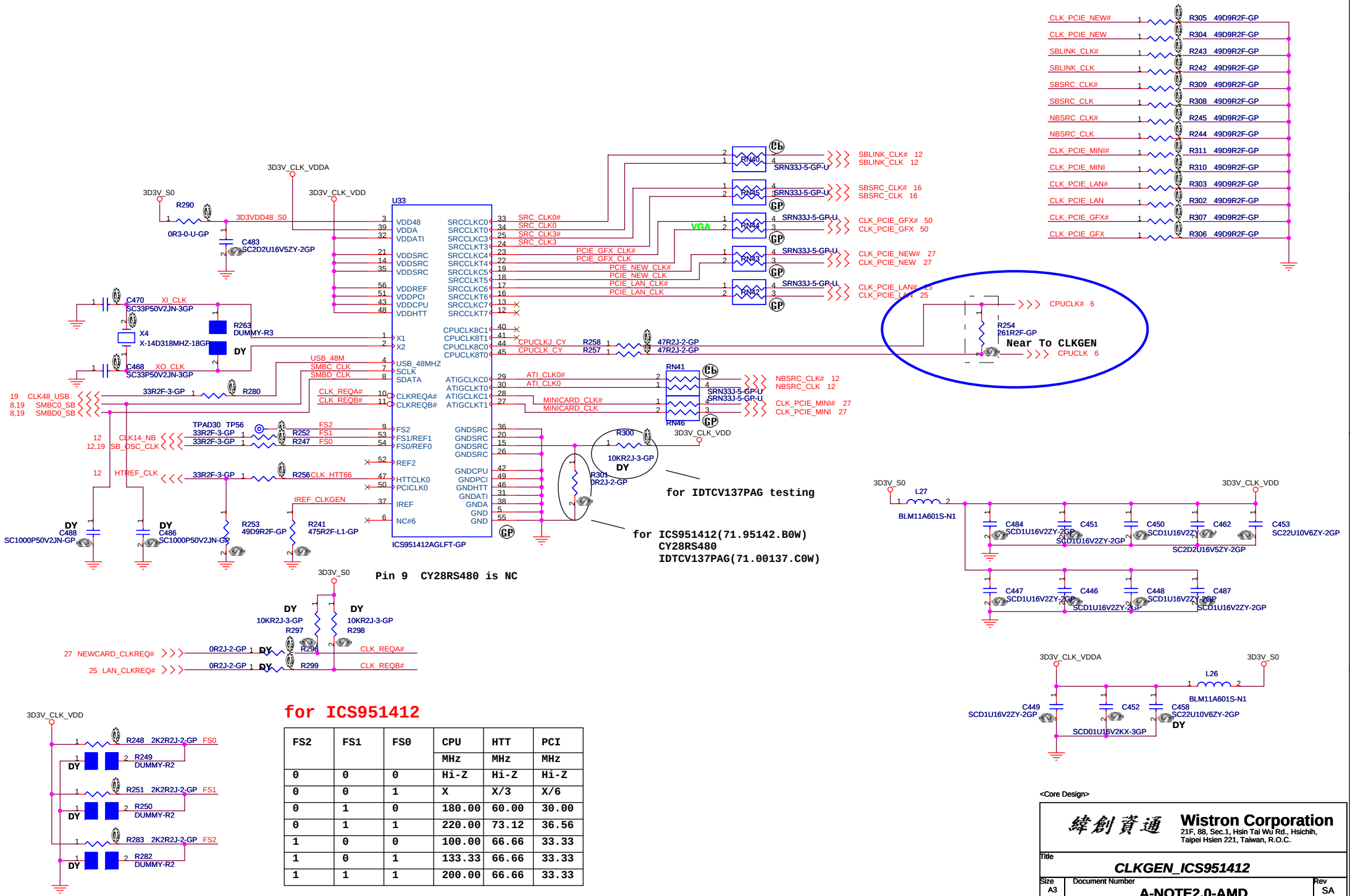
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHANGE HISTORY**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 2 of 55



for ICS951412

FS2	FS1	FS0	CPU	HTT	PCI
			MHz	MHz	MHz
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	73.12	36.56
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33

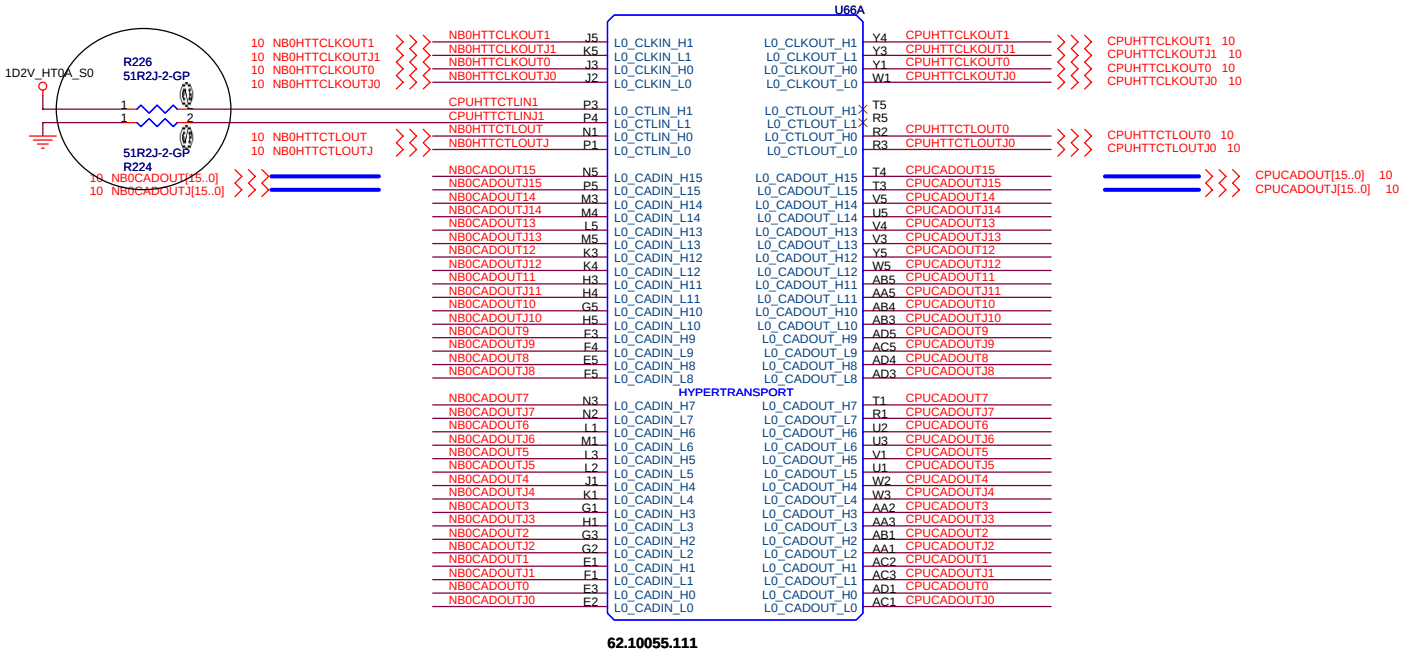
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_ICS951412**

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 3 of 55



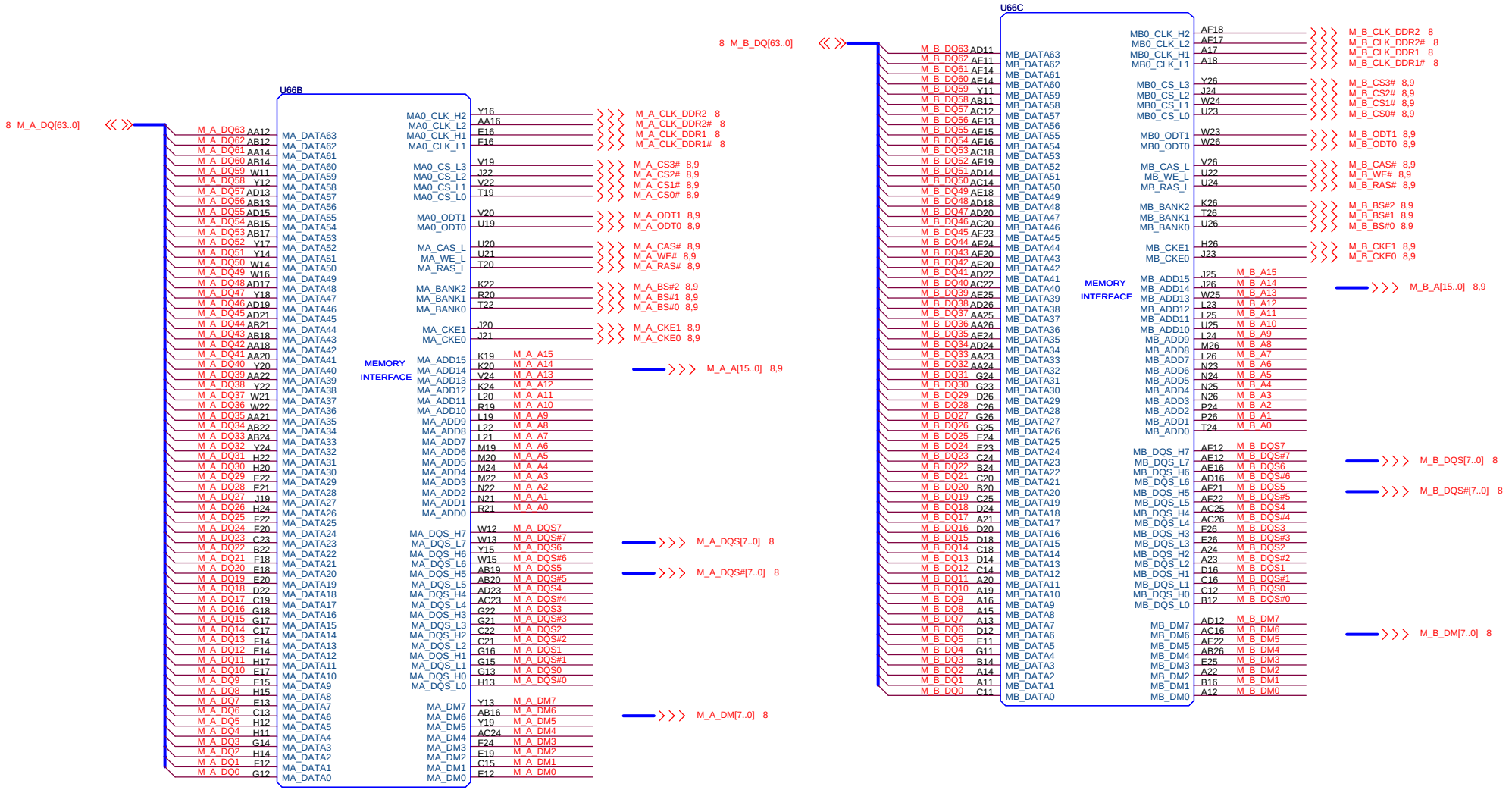
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(1/4)_HyperTransport I/F***

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 4 of 55



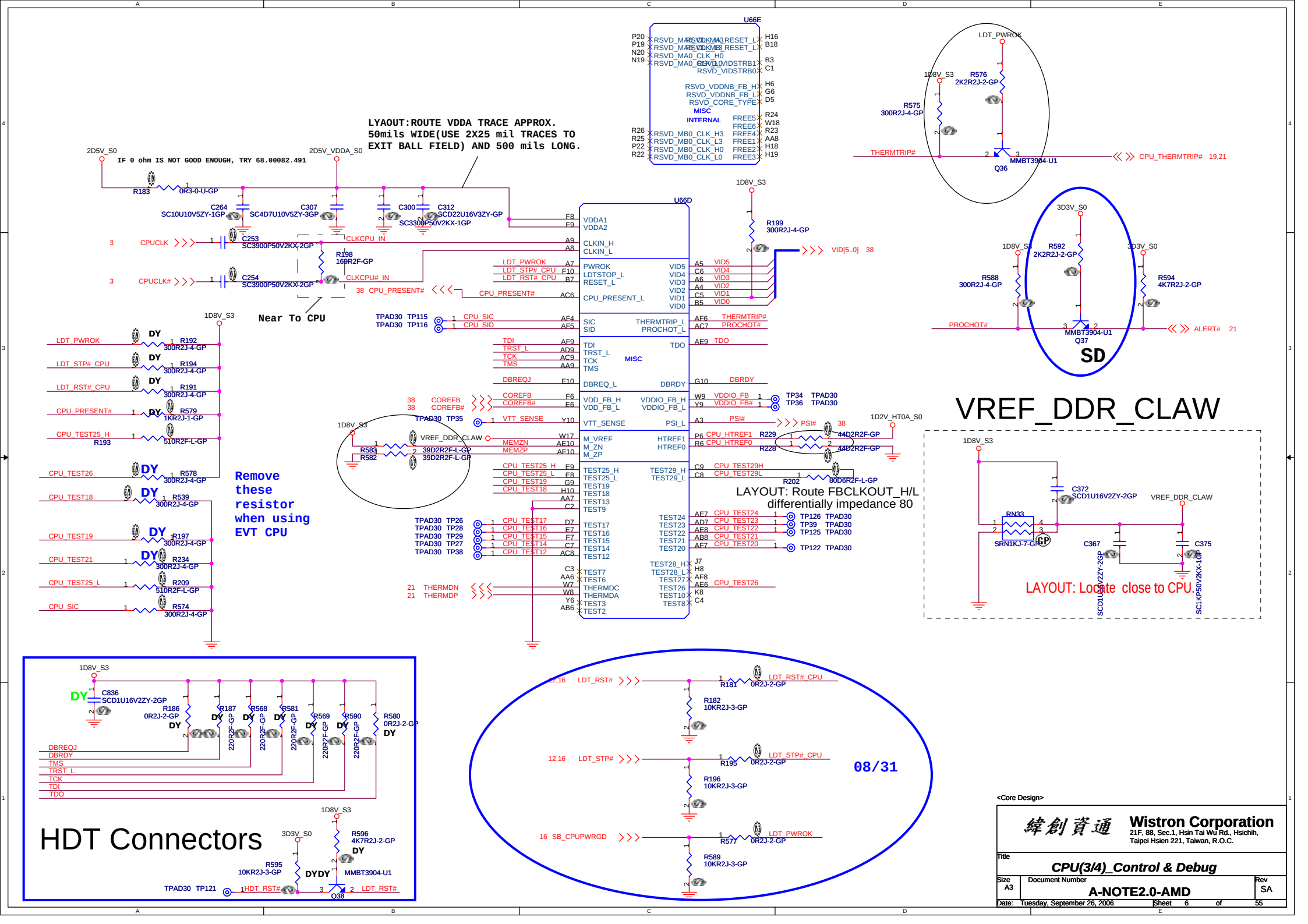
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 5 of 55



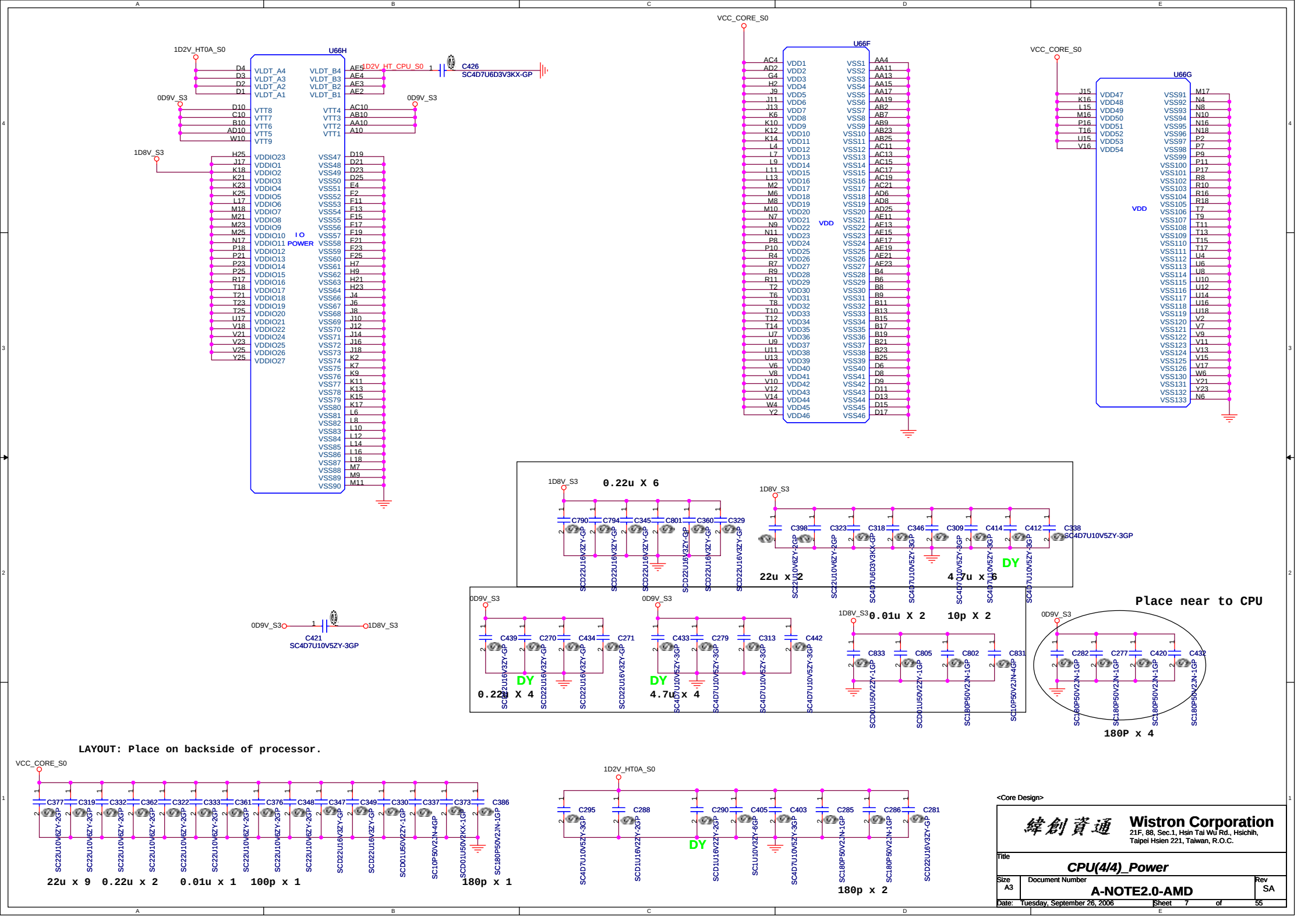
<Core Design>

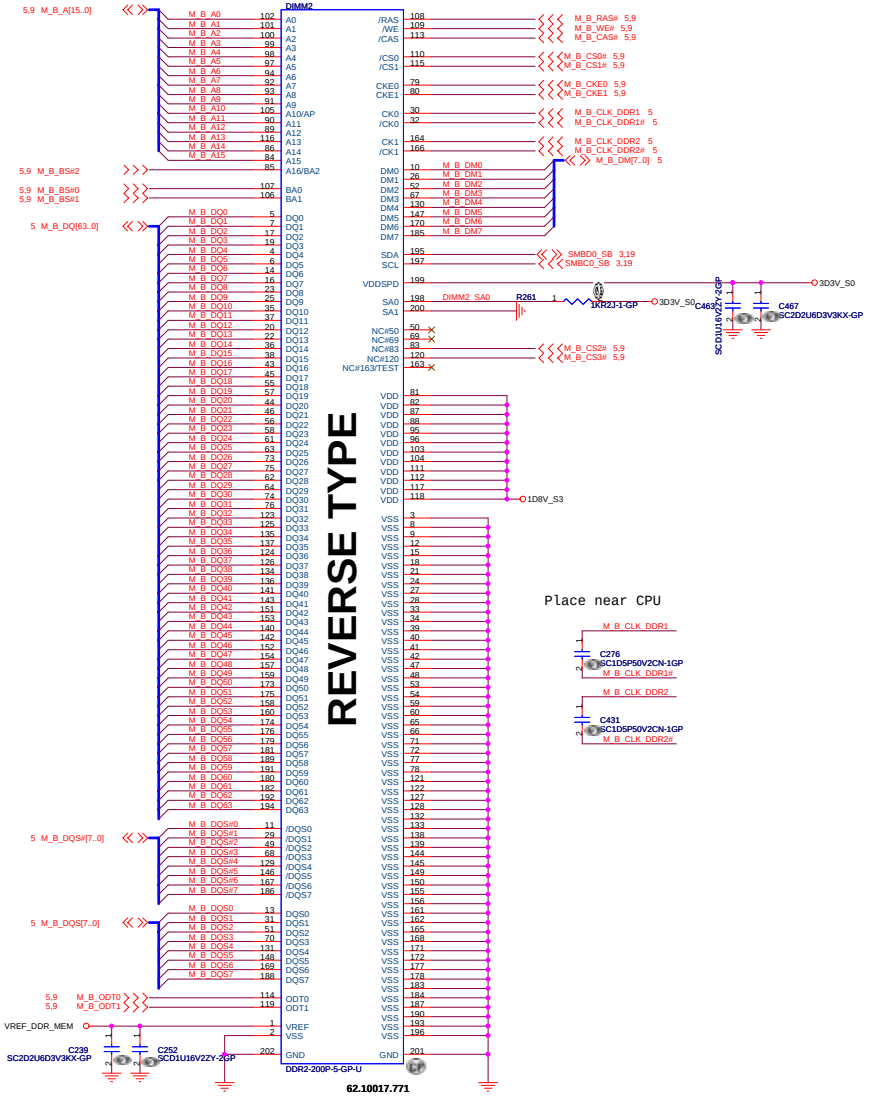
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

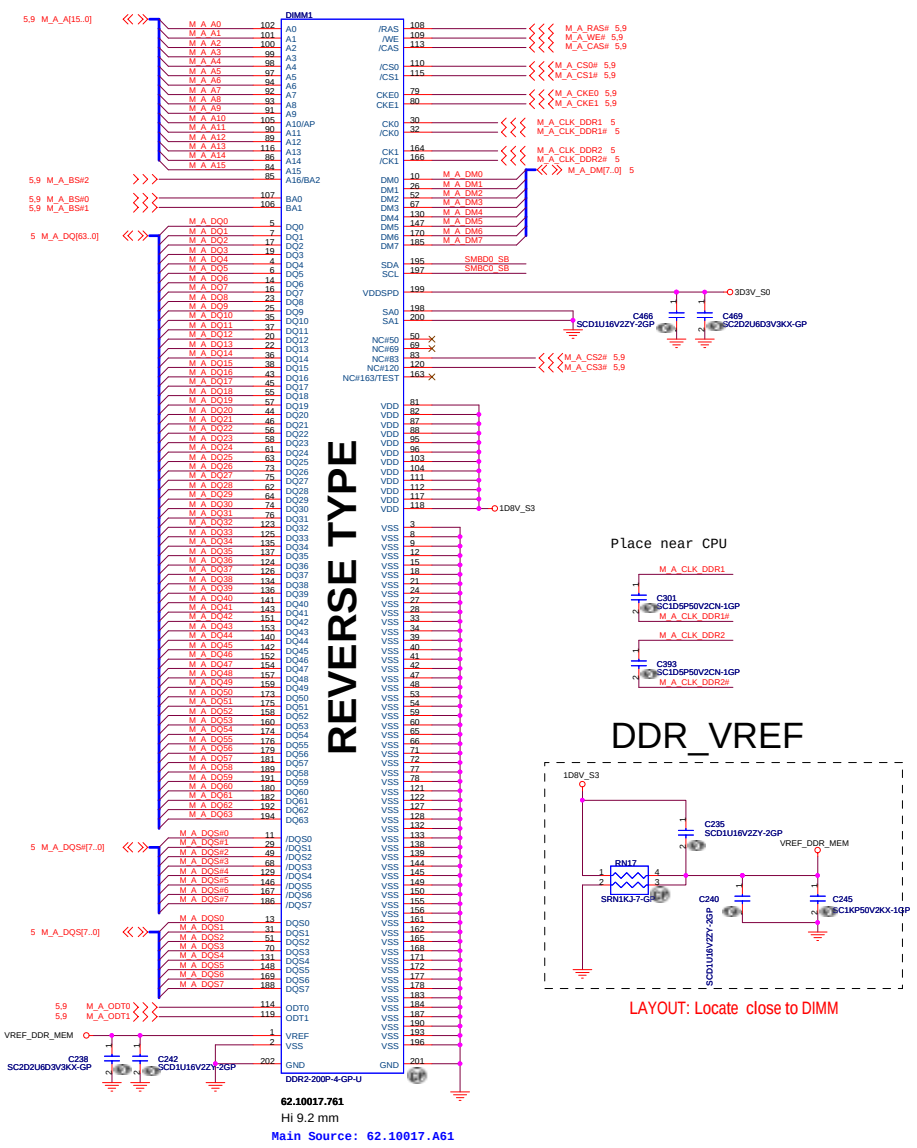
Title: CPU(3/4)_Control & Debug

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 6 of 55


U66H
1D2V_HT0A_S0
0D9V_S3
1D8V_S3
1D2V_HT_CPU_S0
C426
SC4D7U6D3V3KX-GP
VLDT_A4
VLDT_A3
VLDT_A2
VLDT_A1
VLDT_B4
VLDT_B3
VLDT_B2
VLDT_B1
VTT8
VTT7
VTT6
VTT5
VTT9
VTT4
VTT3
VTT2
VTT1
VDDIO23
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDIO12
VDDIO13
VDDIO14
VDDIO15
VDDIO16
VDDIO17
VDDIO18
VDDIO19
VDDIO20
VDDIO21
VDDIO22
VDDIO24
VDDIO25
VDDIO26
VDDIO27
I O
POWER
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
VSS60
VSS61
VSS62
VSS63
VSS64
VSS66
VSS67
VSS68
VSS69
VSS70
VSS71
VSS72
VSS73
VSS74
VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
VCC_CORE_S0
U66F
VDD
U66G
VSS
0D9V_S3
C421
SC4D7U10V5ZY-3GP
1D8V_S3
0.22u X 6
22u x 2
4.7u x 16
DY
0.22u X 4
4.7u x 4
0.01u X 2
10p X 2
Place near to CPU
180P x 4
LAYOUT: Place on backside of processor.
22u x 9
0.22u x 2
0.01u x 1
100p x 1
180p x 1
180p x 2
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
A-NOTE2.0-AMD
Rev
SA
Date: Tuesday, September 26, 2006
Sheet 7 of 55





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

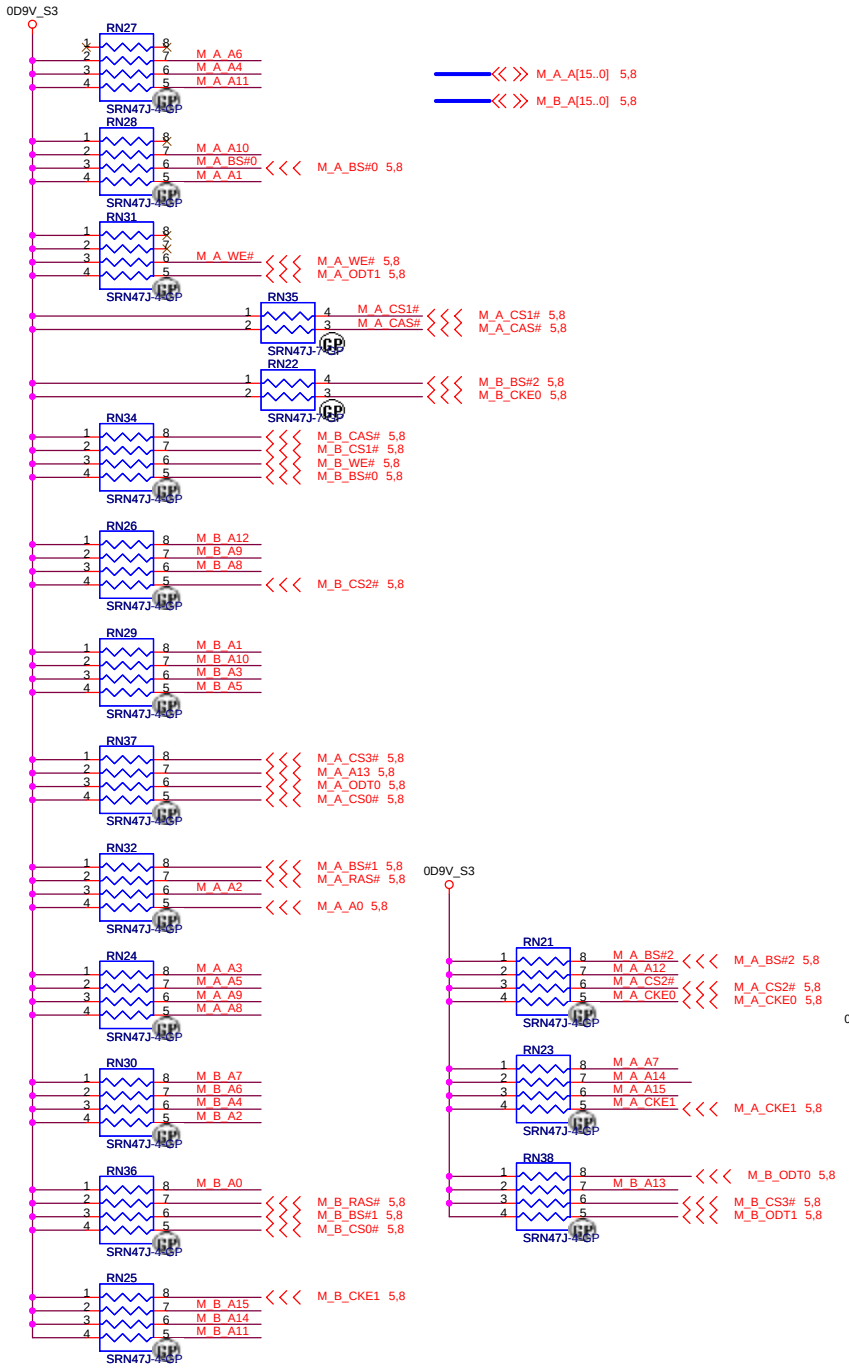
Title: ***DDR SO-DIMM SKT***

Size	Document Number	Rev
A2	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 8 of 55

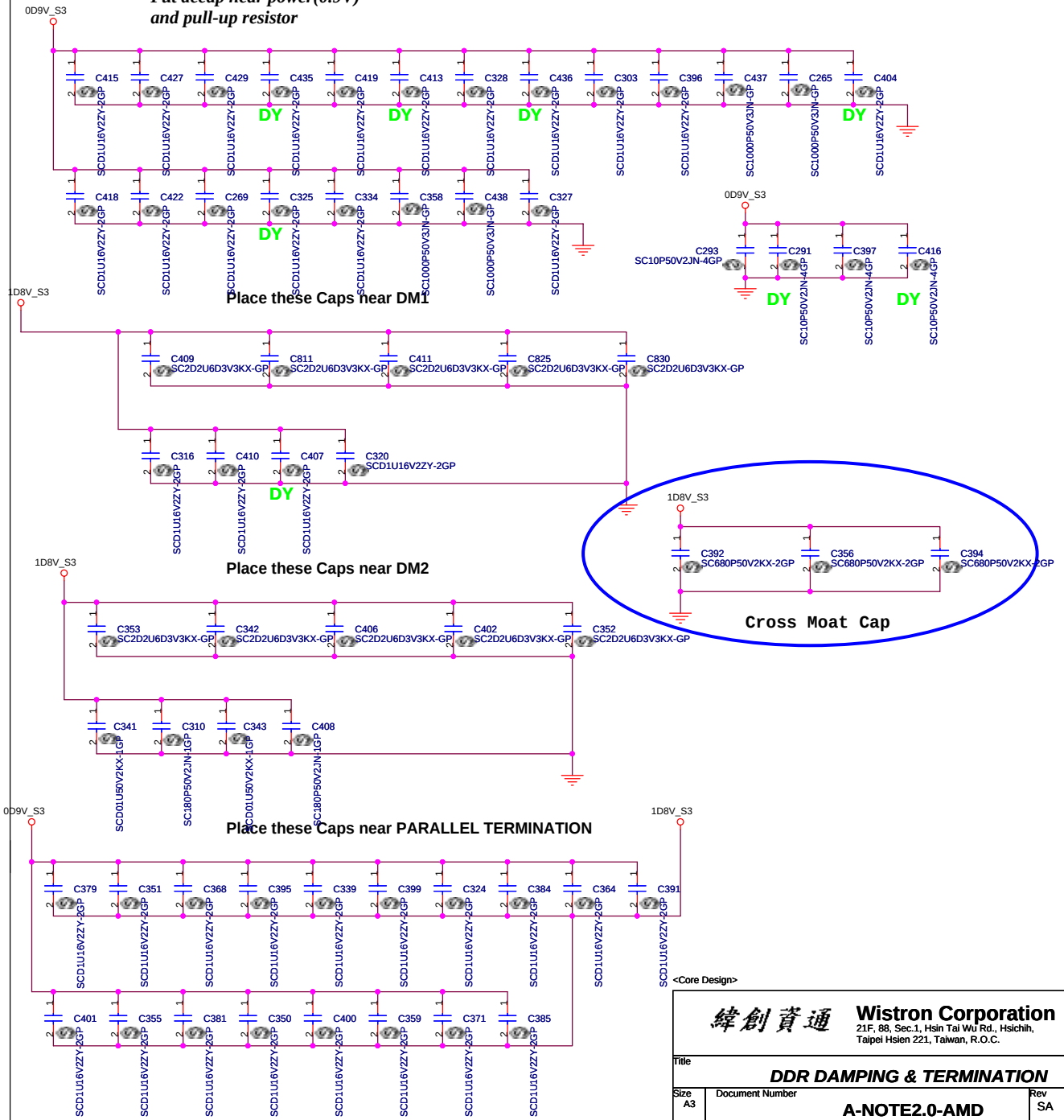
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

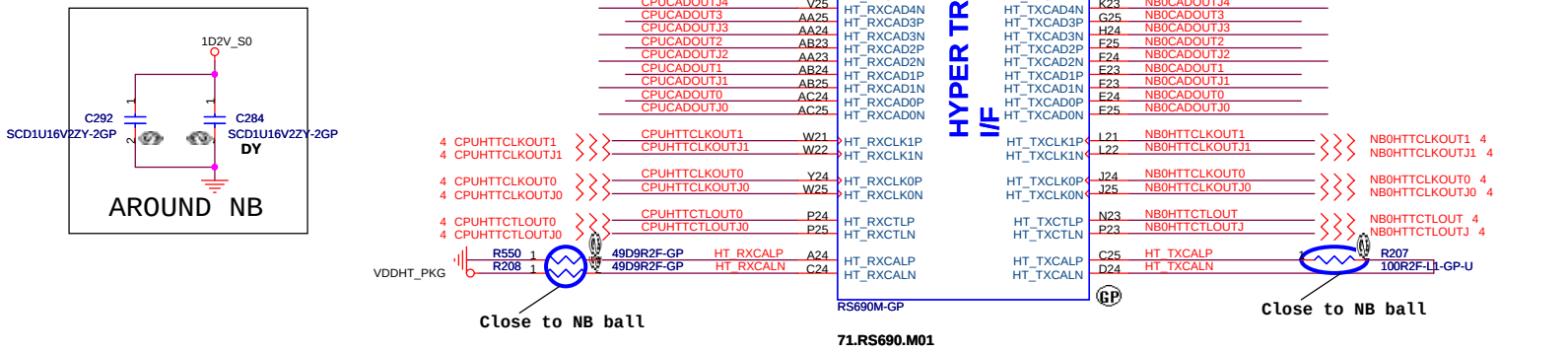
Title: ***DDR DAMPING & TERMINATION***

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 9 of 55

CLAW HAMMER TO NB

NB TO CLAW HAMMER



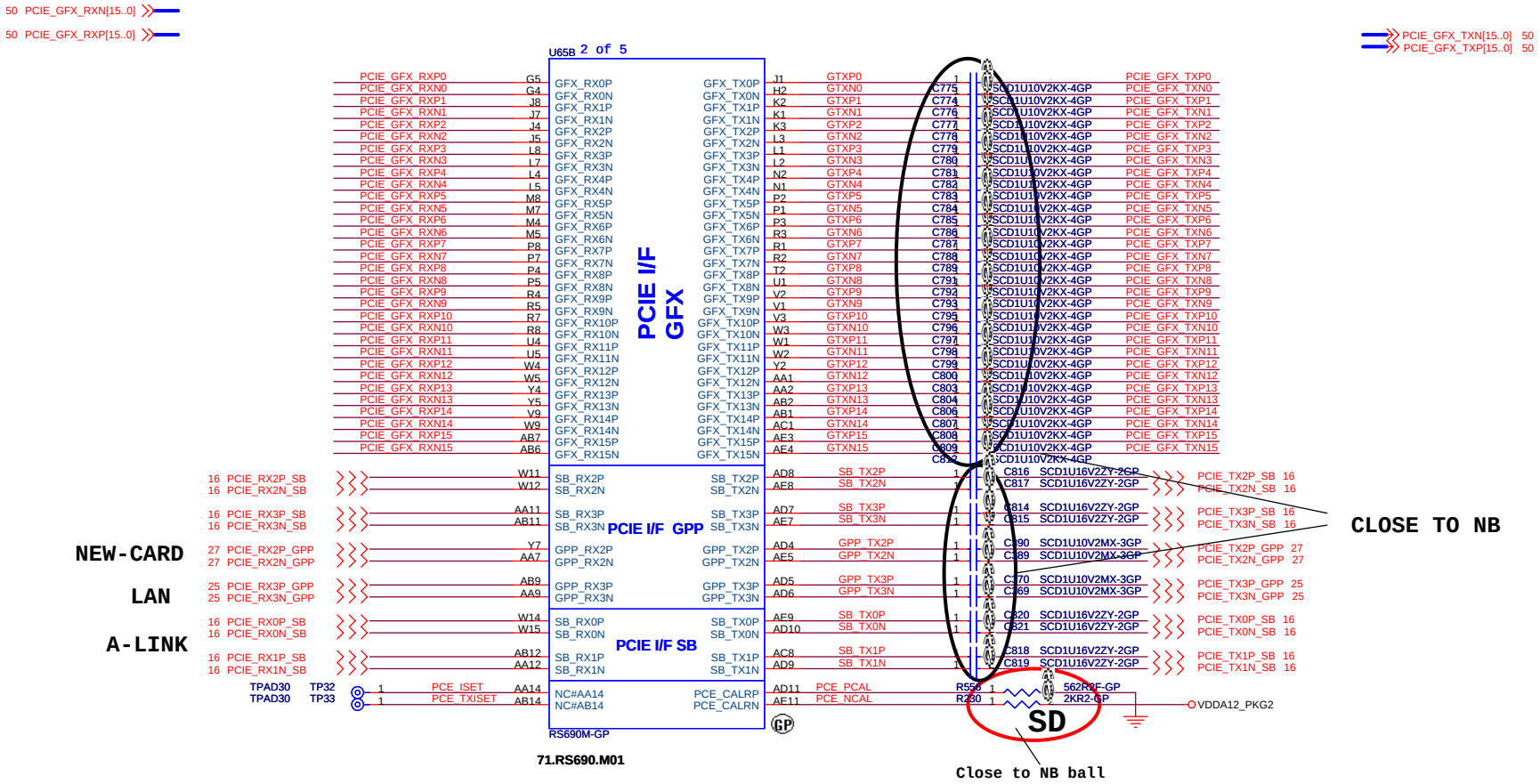
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_HT

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 10 of 55



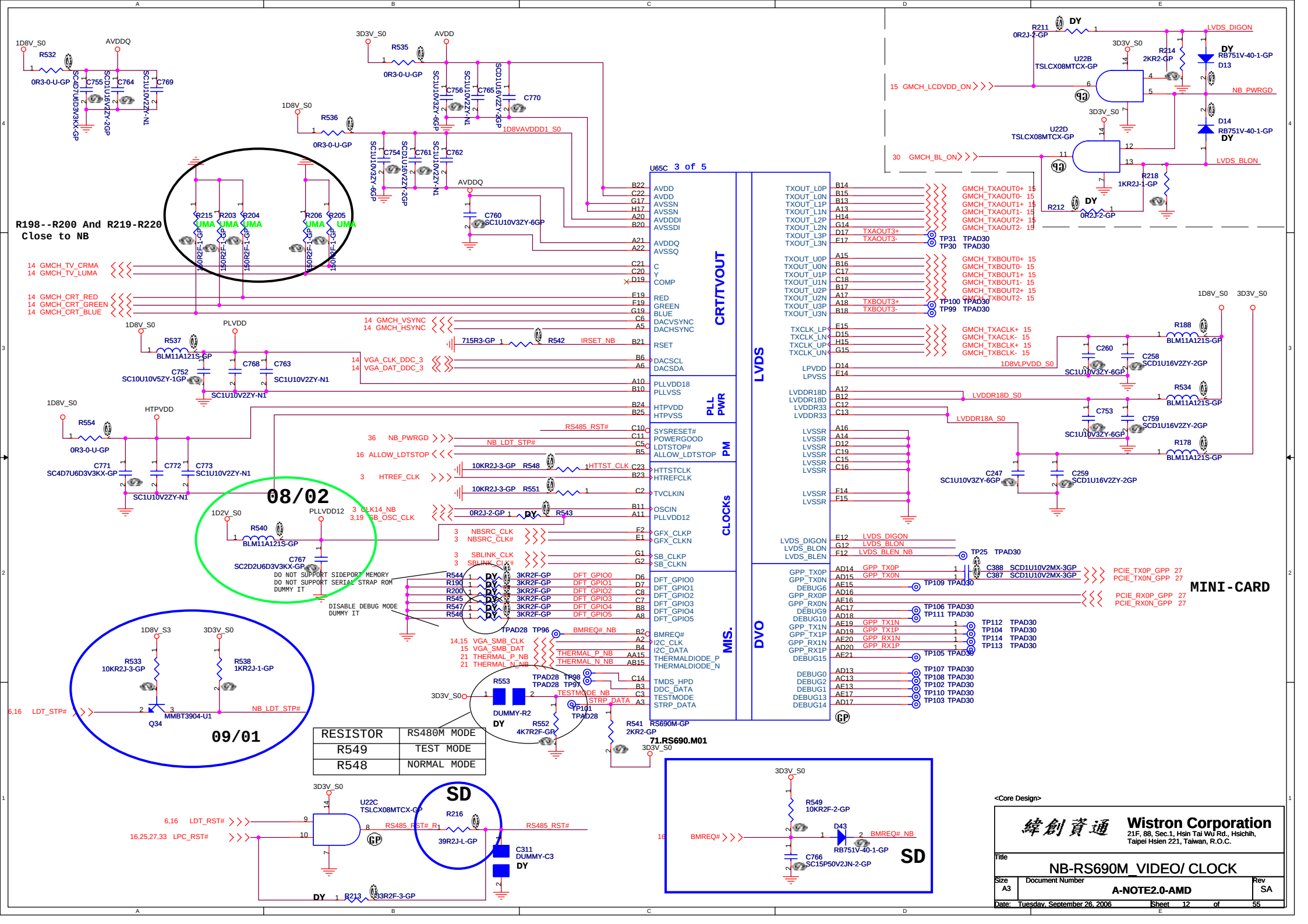
<Core Design>

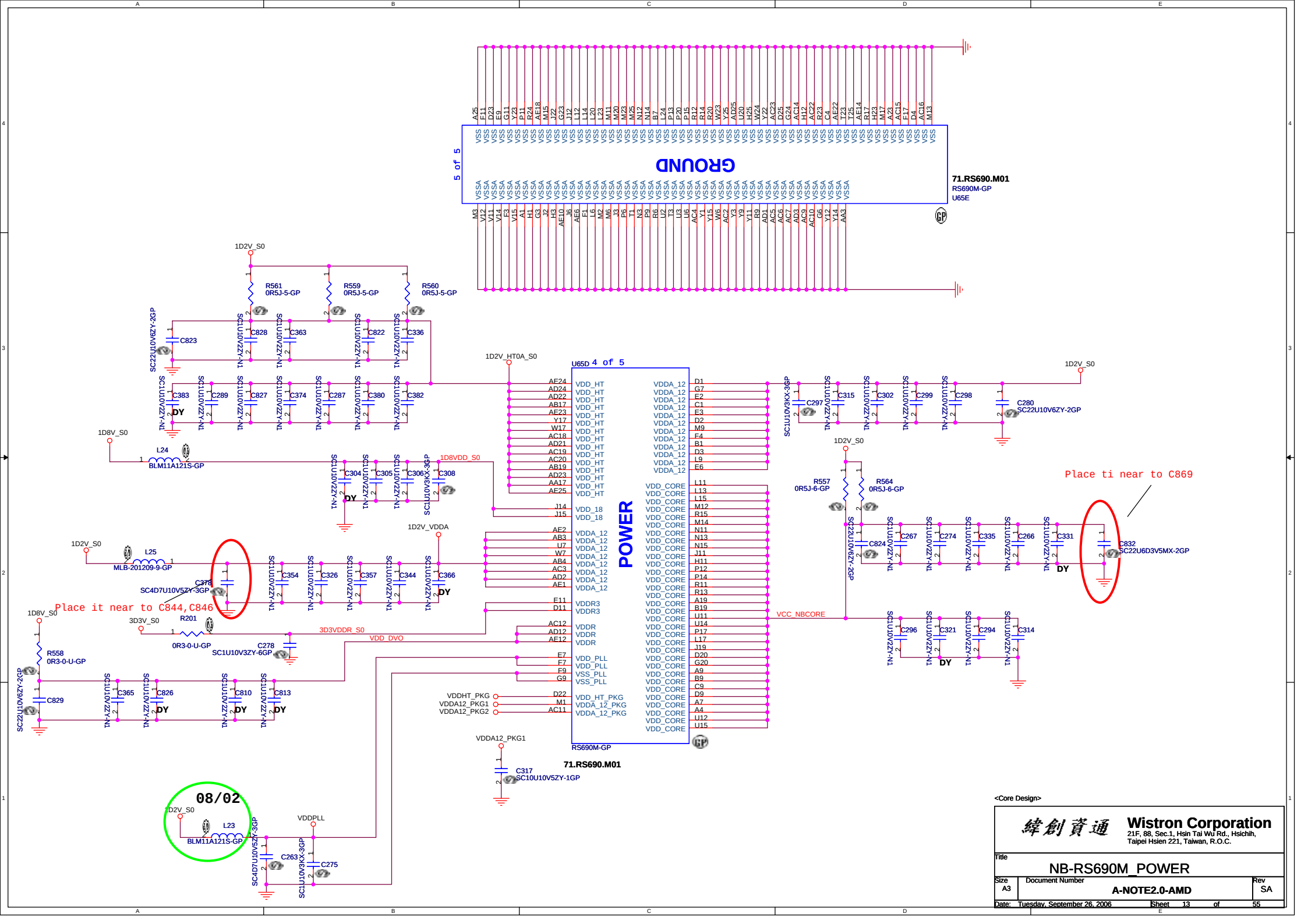
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS690M_MEM/PCIE_LINK I/F

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

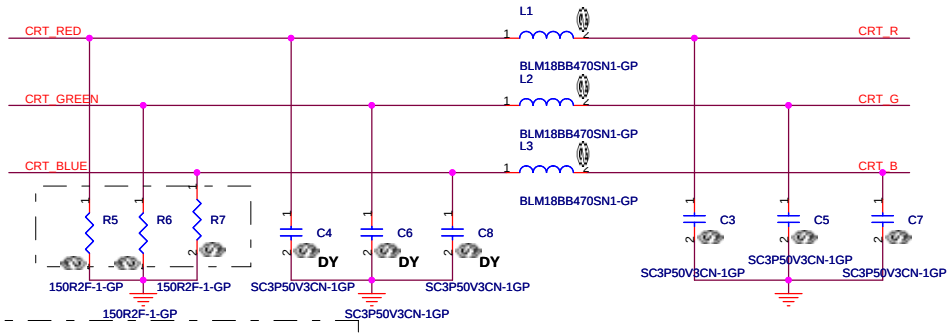
Date: Tuesday, September 26, 2006 | Sheet 11 of 55


R198--R200 And R219-R220
Close to NB
U65C 3 of 5
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
LVDS
DVO
08/02
09/01
SD
MINI-CARD
71.RS690.M01
RESISTOR | RS480M MODE
R549 | TEST MODE
R548 | NORMAL MODE
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_VIDEO/ CLOCK
Size A3
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 12 of 55

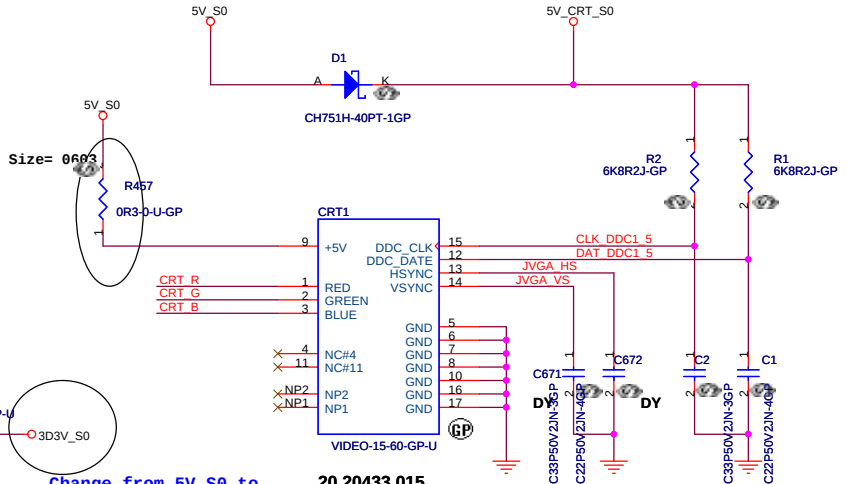

5 of 5
GROUND
71.RS690.M01
RS690M-GP
U65E
U65D 4 of 5
POWER
RS690M-GP
71.RS690.M01
1D2V_S0
1D8V_S0
3D3V_S0
1D2V_HT0A_S0
1D8VDD_S0
1D2V_VDDA
3D3VDDR_S0
VDD_DVO
VDDPLL
VDDA12_PKG1
VCC_NBCORE
Place it near to C844,C846
Place ti near to C869
08/02
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size A3
Document Number
A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 13 of 55

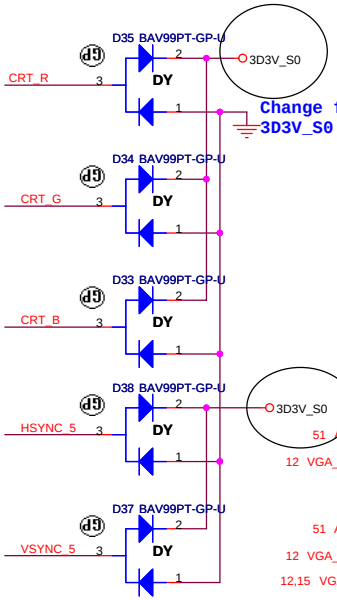
CRT I/F & CONNECTOR

Ferrite bead impedance: 47ohm@100MHz



Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
R857--R859 Close to CRT Conn,the trace impedance between NB and 150ohm resistor should be 50ohm+/-15%, the trace impedance between 150ohm resistor and conn shoulld be 75ohm+/-15%

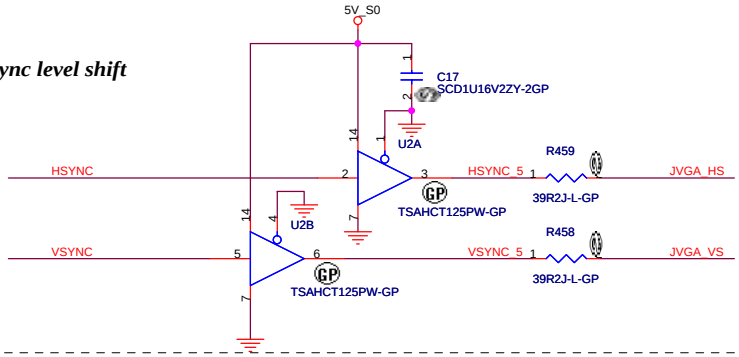




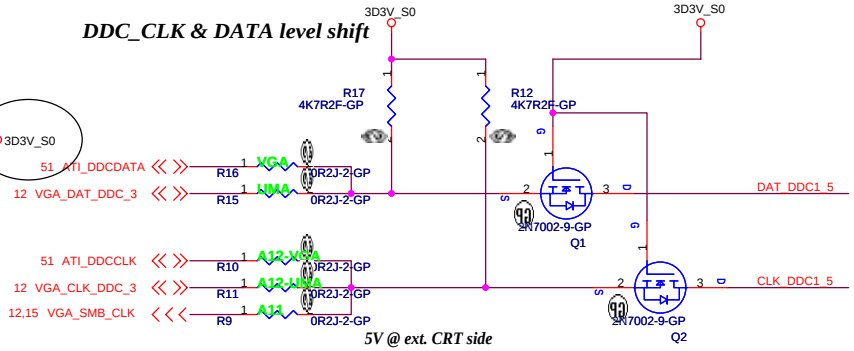
Change from 5V_S0 to 3D3V_S0 as ATI suggestion.

20.20433.015

Hsync & Vsync level shift



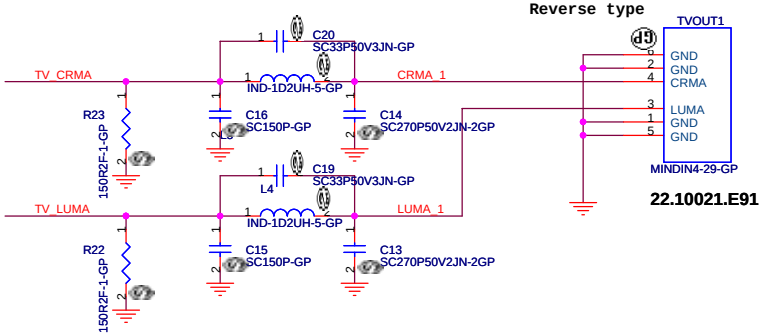
DDC_CLK & DATA level shift



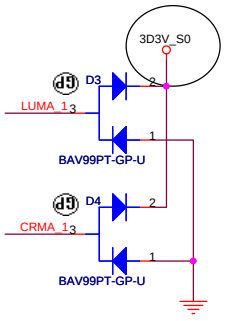
5V @ ext. CRT side

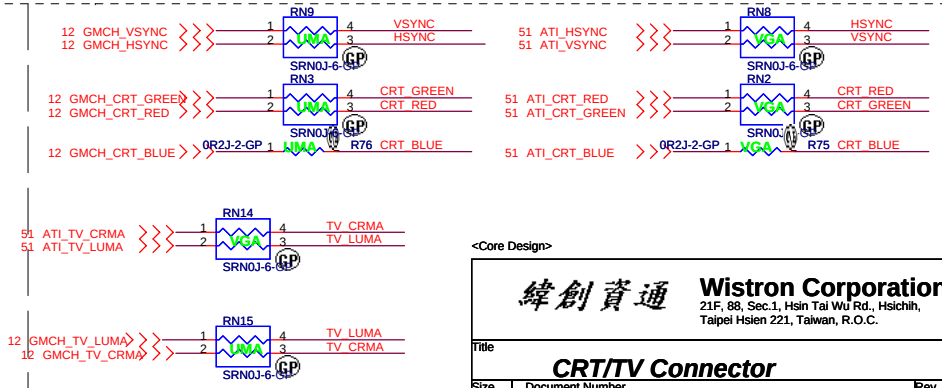
TV OUT CONN

Reverse type



22.10021.E91





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 14 of 55

LED / INVERTER INTERFACE

LCD/INVERTER/CCD CONN

TOP VIEW

LCD 40 1

CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GPIO
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

51 ATI_EDID_CLK
12,14 VGA_SMB_CLK
12 VGA_SMB_DAT
51 ATI_EDID_DATA
R51 R52 R54 R56 0R2J-2-GP
LCD_EDID_CLK
LCD_EDID_DATA

For Cross Moat
VCCGFXCORE
C57 C49 C47 SC1000P50V2JN-N1

DCBATOUT
RES 1206
R24 0R6J-3-GP
C31 SCD1U10V2KX-4GP
C28 SC10U25V0KX-3GP
C26 C25 C30 C39 C29 C38
LCDVDD_S0
3D3V_S0
5V_DC_S0

LCD1 ACES-CONN40C-GP-U
20.F0813.040
TXAOUT0- TXAOUT0+ TXAOUT1- TXAOUT1+ TXAOUT2- TXAOUT2+ TXACLK- TXACLK+ TXBOUT0- TXBOUT0+ TXBOUT1- TXBOUT1+ TXBOUT2- TXBOUT2+ TXBCLK- TXBCLK+
WEBCAM_GPIO
TP1 TPAD28
RN1 SRN4K7J-8-GP
LCD_EDID_CLK
LCD_EDID_DATA
BRIGHTNESS_CONN
FPBACK 30
R35 0R2J-2-GP
BRIGHTNESS 30
R28 100KR2J-1-GP
R36
R33 100KR2J-1-GP
DY
ATI_BRIGHTNESS 51
EC6 SC1000P50V2JN-GP
USB_PN7 19
USB_PP7 19

5V_S5
R721 100R2F-L1-GP-U
LED3 LED-G-138-GP
EC63 SC1000P50V3JN-GP
STBY_LED# 30

5V_S0
R723 150R2J-L1-GP-U
R724 100R2F-L1-GP-U
LED2 LED1 LED-G-138-GP
Q41 CHDTC124EU-1GP
EC64 SC1000P50V3JN-GP
EC65 SC1000P50V3JN-GP
BLUETOOTH_LED 24
WLAN_LED# 27

3D3V_S0
U70A TSLCX08MTCX-GP
32 MEDIA_LED#
CDROM_LED# 34
HDLED#
R321 1KR2J-1-GP
SATA_LED# 17

5V_S5
R720 150R2J-L1-GP-U
R722 100R2F-L1-GP-U
LED4 LED-GR-6-GP
Q40 Q39 CHDTC124EU-1GP
C938 C940 SC1000P50V2JN-N1
CHG_LED1 30
CHG_LED2 30

5V_DC_S0
0R3J-2-N1-GP R32
U6 G5240B2T1U-GP-U
C35 SC22U6D3V5MX-2GP
5V_S0
C34 SCD1U16V2ZY-2GP
CAMERA_EN# 30
51 ATI_LCDVDD_ON
12 GMCH_LCDVDD_ON
R40 R44 1KR3F-GP

LCD POWER

Layout 40 mil
LCDVDD_S0
3D3V_S0
U7 G5281RC1U-GP
LCDVDD_ON_1
R37 100KR2J-1-GP
C32 SCD1U16V2ZY-2GP
C37 SC10U10V2ZY-6GP

RN13 SRN0J-7-GP
12 GMCH_TXACLK+ 12 GMCH_TXACLK- 12 GMCH_TXAOUT0+ 12 GMCH_TXAOUT0-
TXACLK+ TXACLK- TXAOUT0+ TXAOUT0-
RN11
12 GMCH_TXBCLK+ 12 GMCH_TXBCLK- 12 GMCH_TXBOUT0+ 12 GMCH_TXBOUT0-
TXBCLK+ TXBCLK- TXBOUT0+ TXBOUT0-
RN12
12 GMCH_TXAOUT1+ 12 GMCH_TXAOUT1- 12 GMCH_TXAOUT2+ 12 GMCH_TXAOUT2-
TXAOUT1+ TXAOUT1- TXAOUT2+ TXAOUT2-
RN10
12 GMCH_TXBOUT1+ 12 GMCH_TXBOUT1- 12 GMCH_TXBOUT2+ 12 GMCH_TXBOUT2-
TXBOUT1+ TXBOUT1- TXBOUT2+ TXBOUT2-
RN7
51 ATI_TXAOUT0- 51 ATI_TXAOUT0+ 51 ATI_TXACLK- 51 ATI_TXACLK+
TXAOUT0- TXAOUT0+ TXACLK- TXACLK+
RN5
51 ATI_TXBOUT0- 51 ATI_TXBOUT0+ 51 ATI_TXBCLK- 51 ATI_TXBCLK+
TXBOUT0- TXBOUT0+ TXBCLK- TXBCLK+
RN6
51 ATI_TXAOUT2- 51 ATI_TXAOUT2+ 51 ATI_TXAOUT1- 51 ATI_TXAOUT1+
TXAOUT2- TXAOUT2+ TXAOUT1- TXAOUT1+
RN4
51 ATI_TXBOUT2- 51 ATI_TXBOUT2+ 51 ATI_TXBOUT1- 51 ATI_TXBOUT1+
TXBOUT2- TXBOUT2+ TXBOUT1- TXBOUT1+

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INV / LCD
Size: A3
Document Number: A-NOTE2.0-AMD
Rev: SA
Date: Tuesday, September 26, 2006
Sheet 15 of 55

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

32K suspend clock output

U71A 1 of 4

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

LPC

CPU

RTC

XTAL

SB600-GP

71.SB600.00U

PCIRST# 3V to 5V level shift for HDD & CDROM

SB600 asserts PLTRST# to reset devices on the platform.

Secondary PCI Bus reset signal.

2nd source: 20.D0198.103

08/28

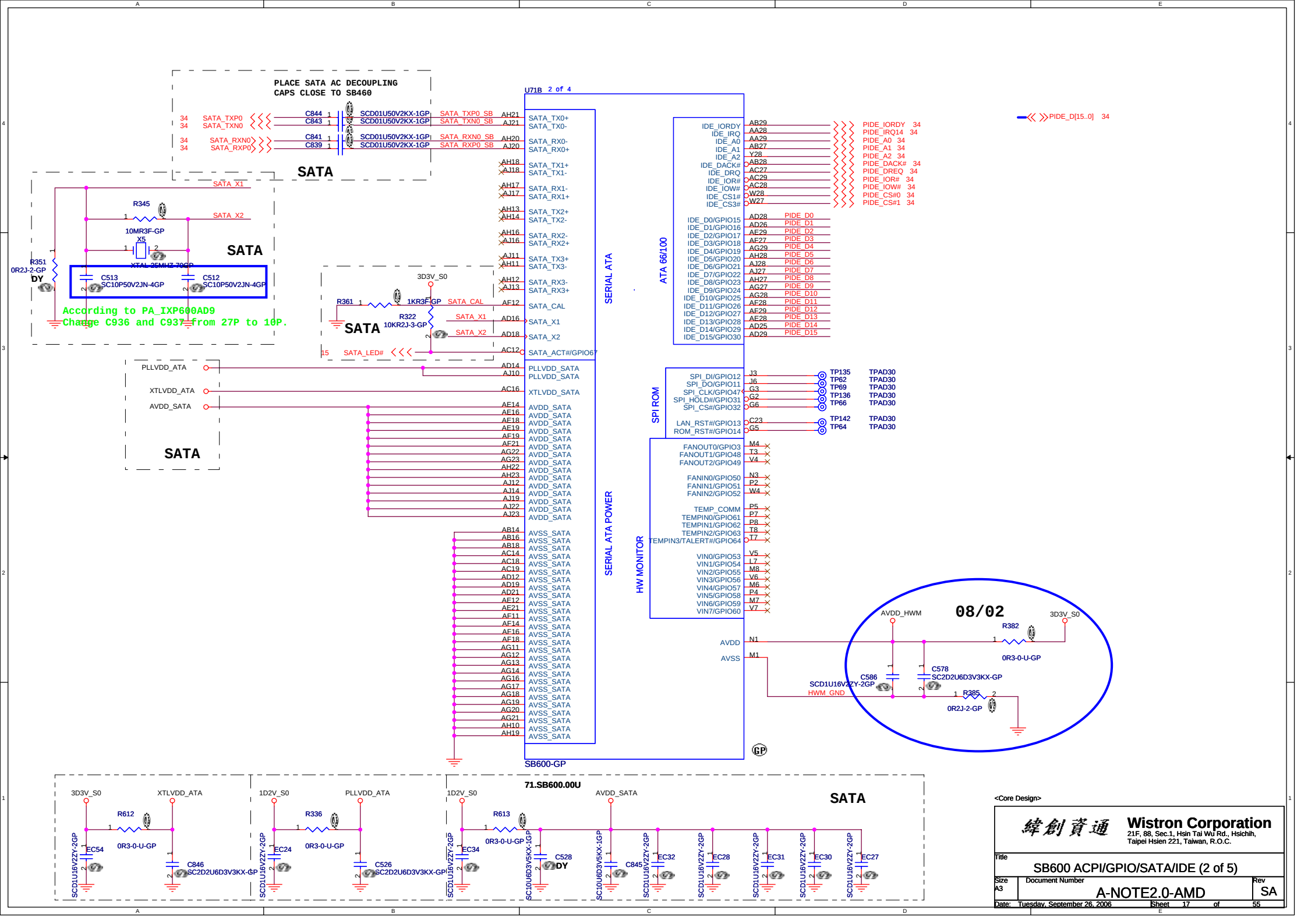
<Core Design>

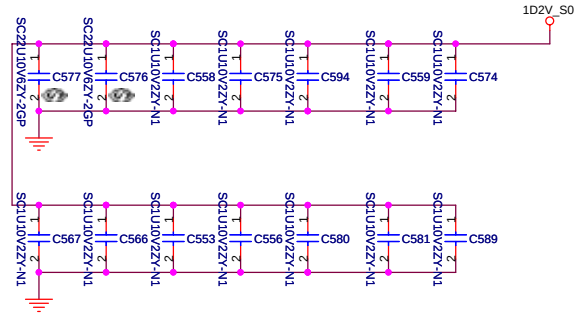
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

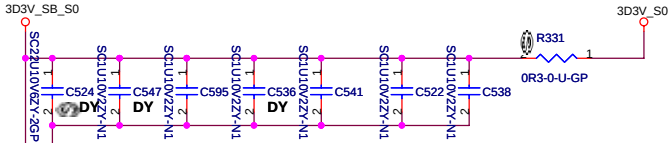
Title: SB600 PCI/CPU/LPC/RTC (1 of 5)

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

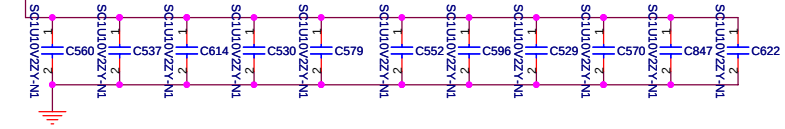
Date: Tuesday, September 26, 2006 | Sheet 16 of 55

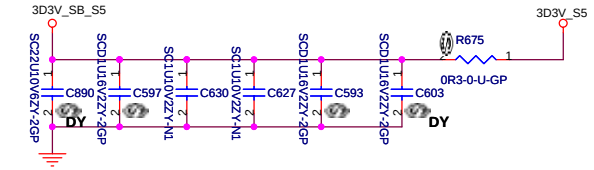

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460
SATA
SATA
SATA
SATA
SATA
U71B 2 of 4
SERIAL ATA
SERIAL ATA POWER
ATA 66/100
SPI ROM
HW MONITOR
SB600-GP
According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.
08/02
71.SB600.00U
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SB600 ACPI/GPIO/SATA/IDE (2 of 5)
A-NOTE2.0-AMD
SA
Tuesday, September 26, 2006
17
55

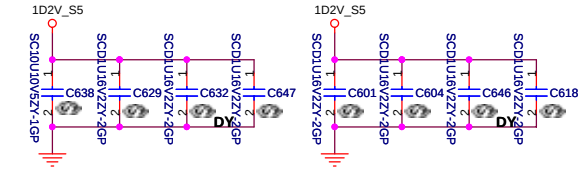


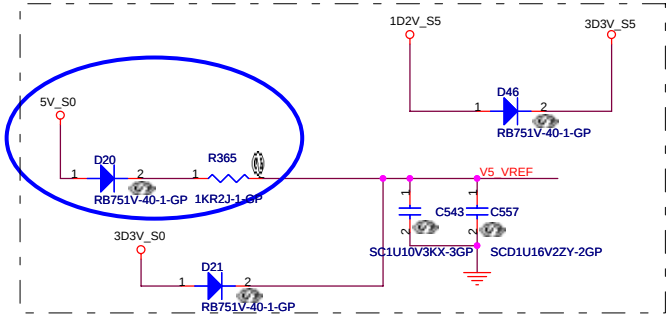


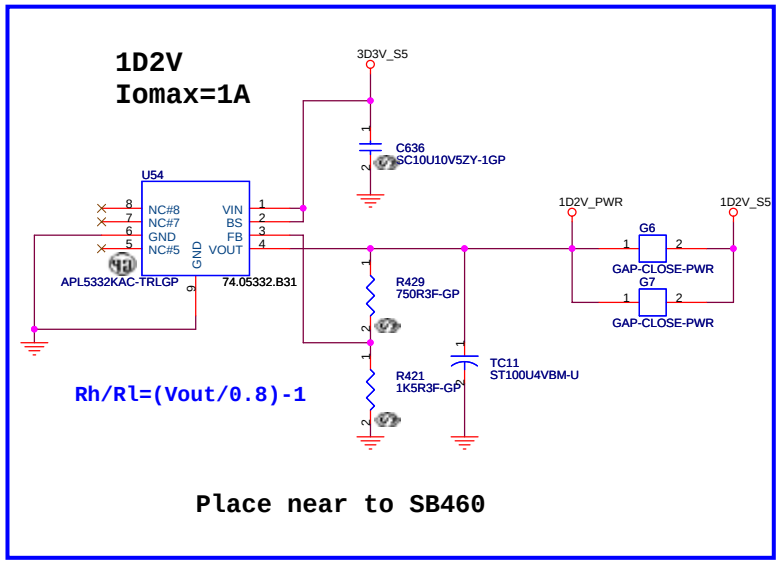
2Pin Use One Capcitance Uniformly.

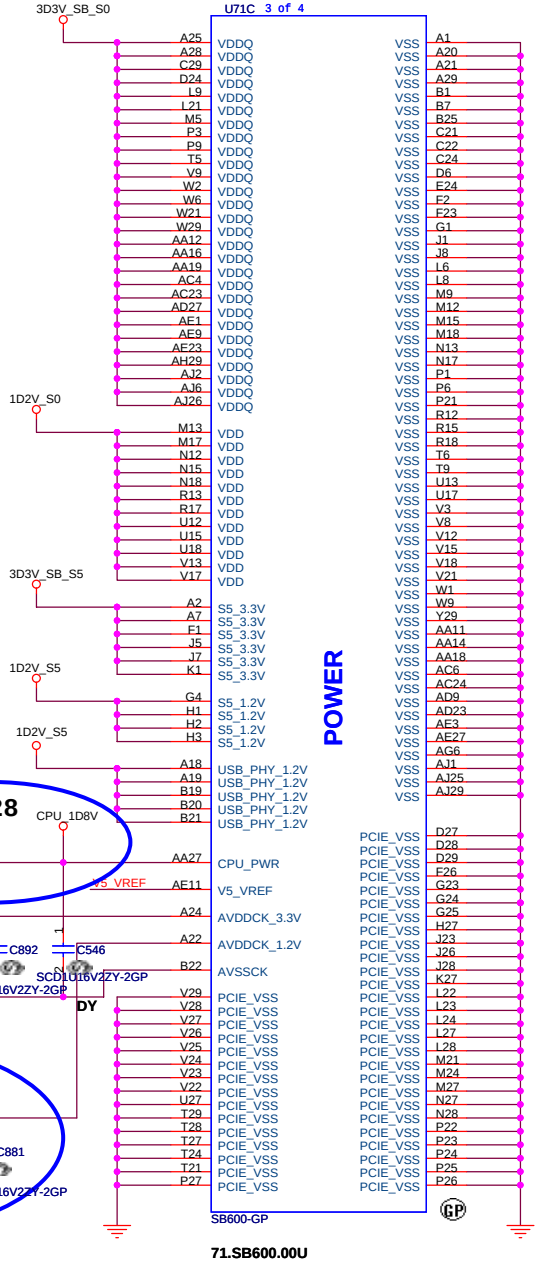












<core_design><Core Design></core_design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 POWER/DECOUPLING**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

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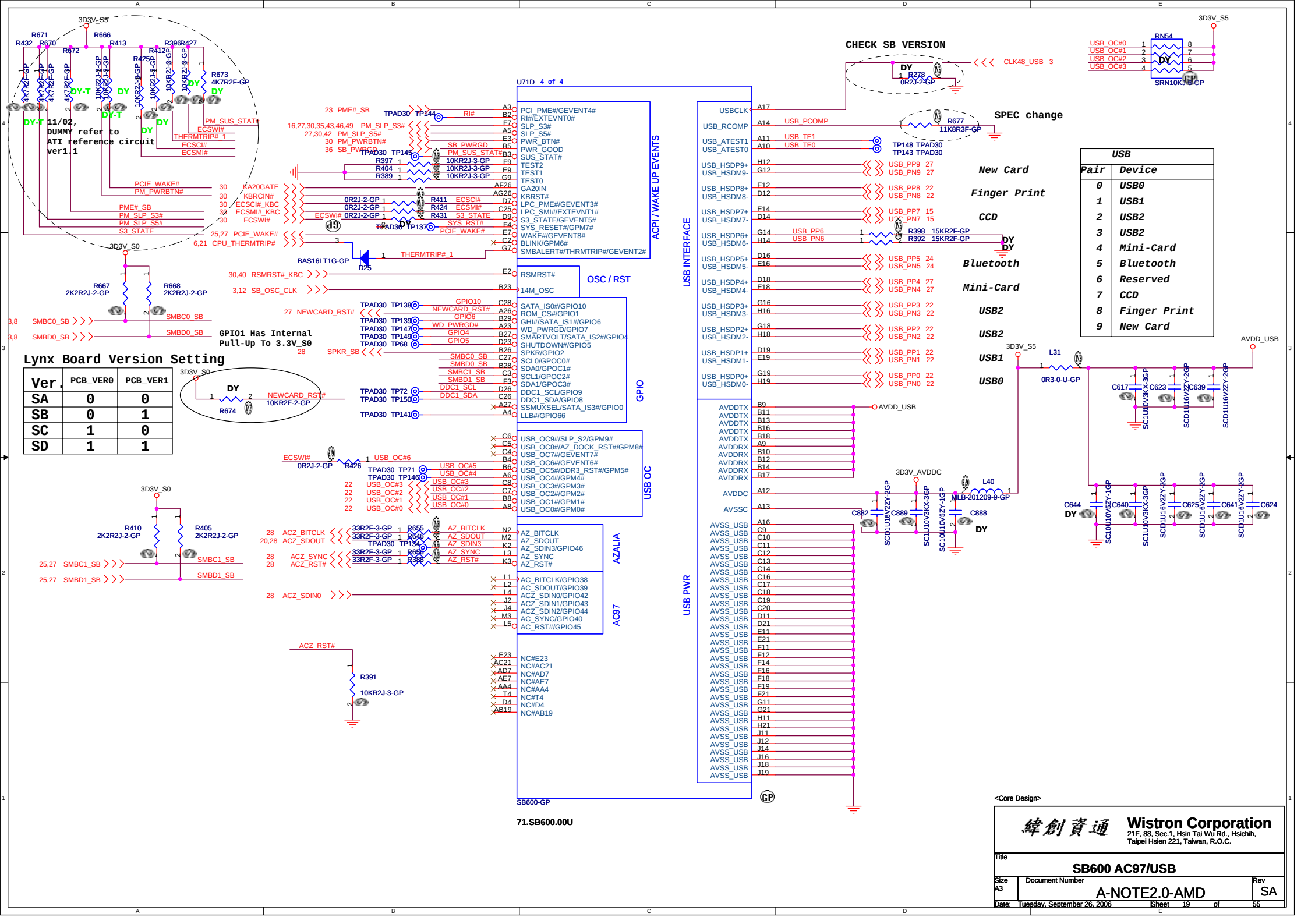
CHECK SB VERSION
SPEC change
New Card
Finger Print
CCD
Bluetooth
Mini-Card
USB2
USB2
USB1
USB0
USB
Pair Device
0 USB0
1 USB1
2 USB2
3 USB2
4 Mini-Card
5 Bluetooth
6 Reserved
7 CCD
8 Finger Print
9 New Card
Lynx Board Version Setting
Ver. PCB_VER0 PCB_VER1
SA 0 0
SB 0 1
SC 1 0
SD 1 1
GPIO1 Has Internal
Pull-Up To 3.3V_S0
DY-T 11/02,
DUMMY refer to
ATI reference circuit
ver1.1
U71D 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
SB600-GP
71.SB600.00U
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 AC97/USB
Size A3
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
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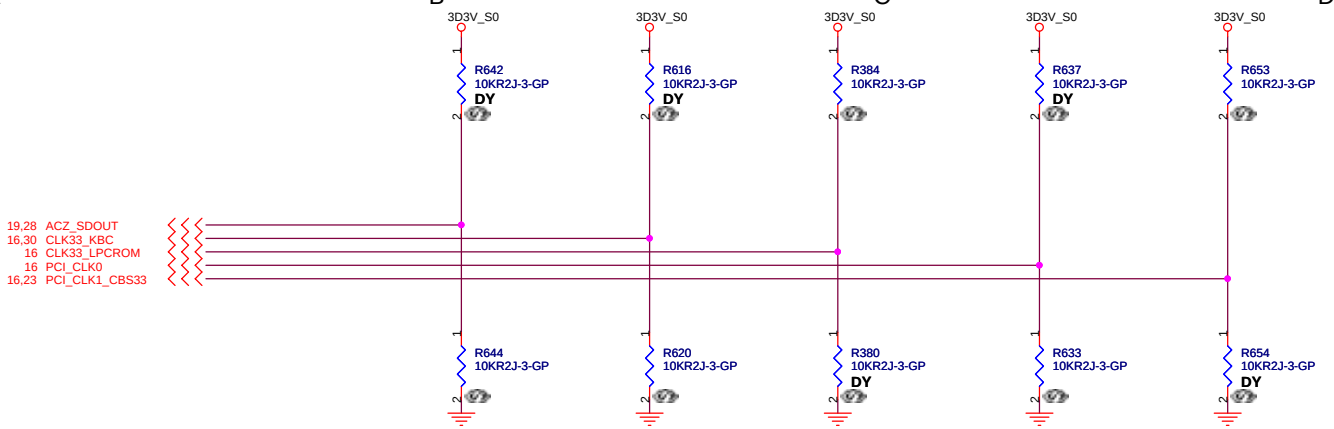
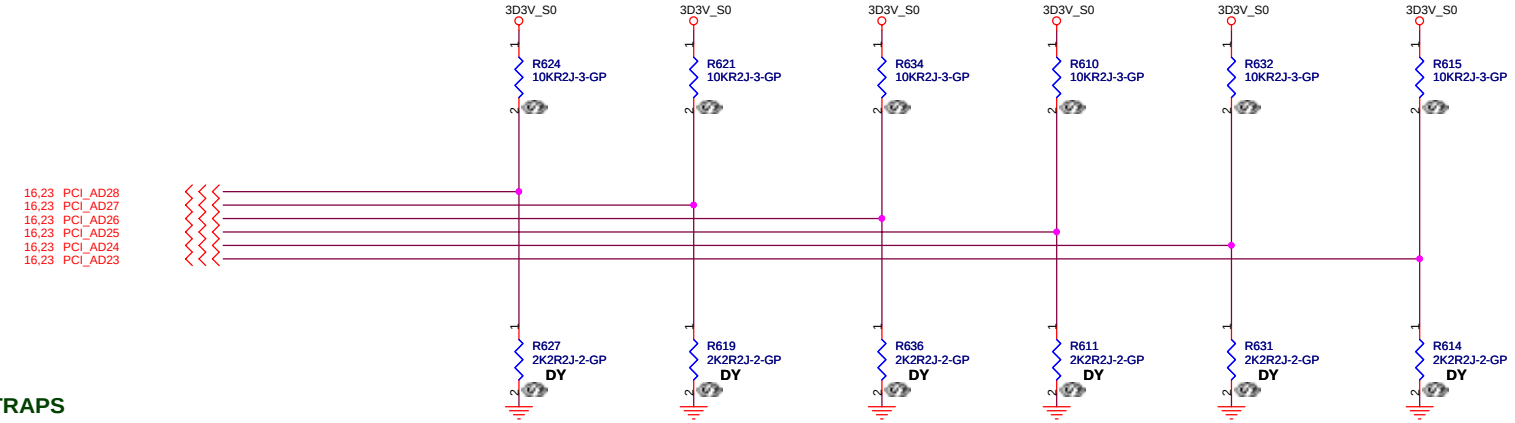


REQUIRED SYSTEM STRAPS

		AC_SDOUT	PCI_CLK0,PCI_CLK1_CBS33	PCI_CLK4	PCI_CLK6
STRAP HIGH		USE DEBUG STRAPS	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	USB INT PLL48	CPU I/F=K8 DEFAULT
STRAP LOW		IGNORE DEBUG STRAPS DEFAULT	L,H=LPC ROM II L,L=Firmware Hub ROM	USB EXT. 48MHZ DEFAULT	CPU I/F=P4

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

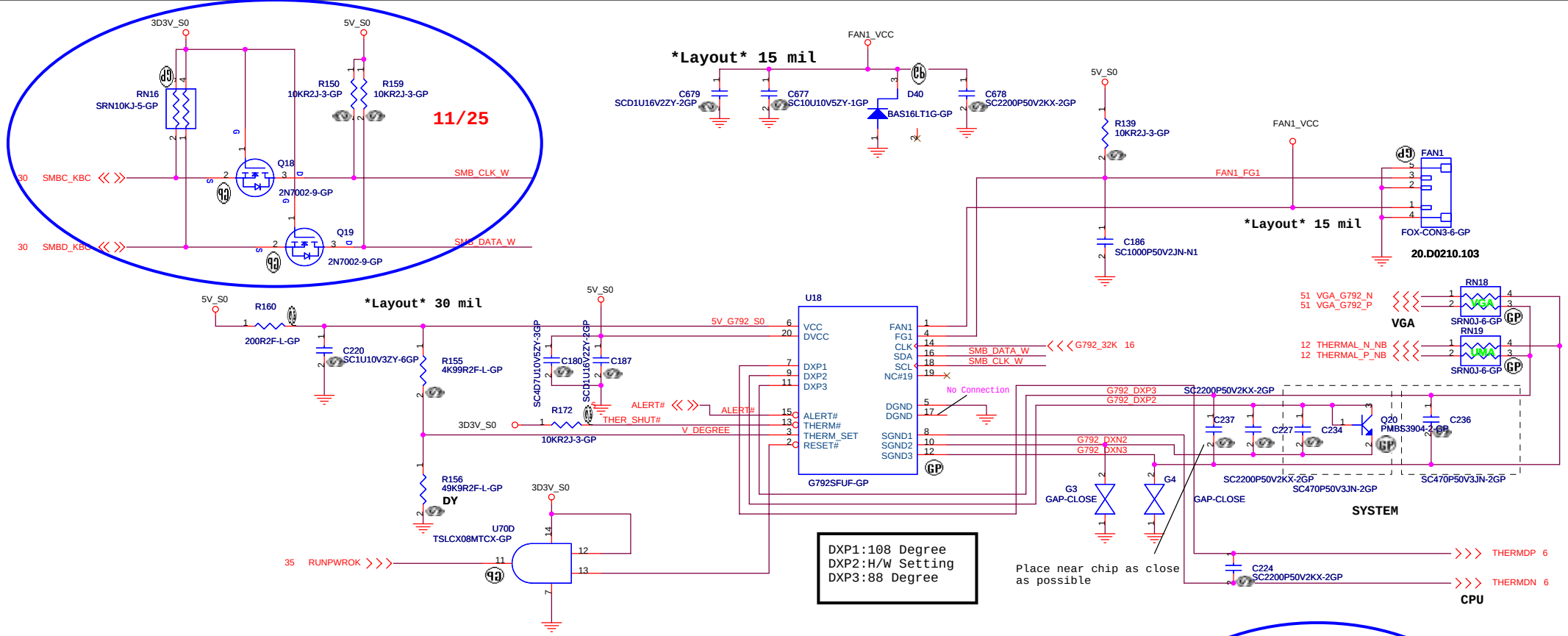
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

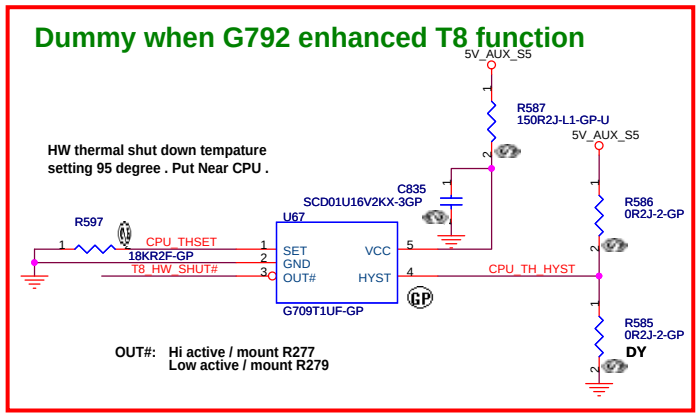
Title: SB600 STRAPPING PIN

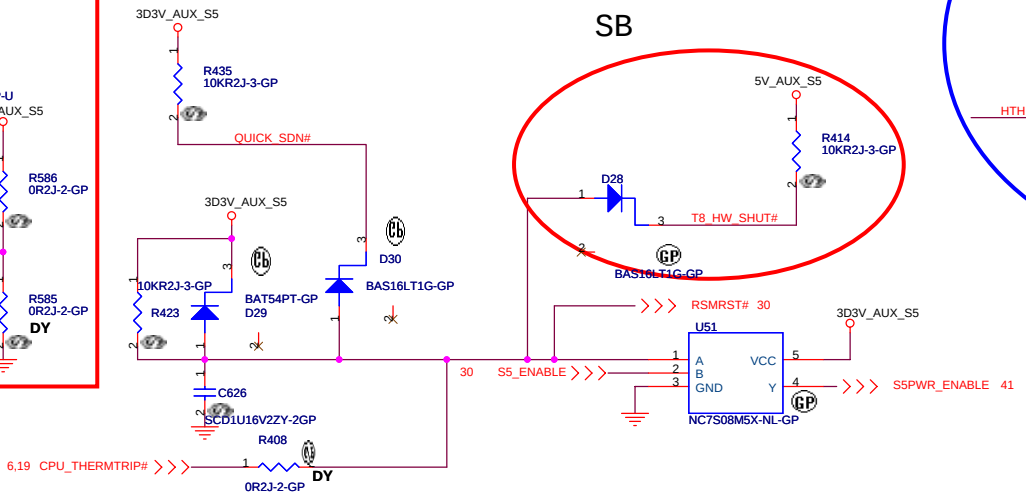
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

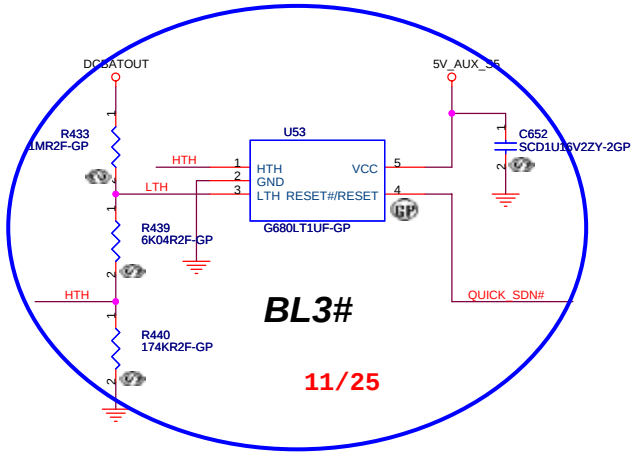
Date: Tuesday, September 26, 2006 | Sheet 20 of 55



HW Thermal Throttling







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G792

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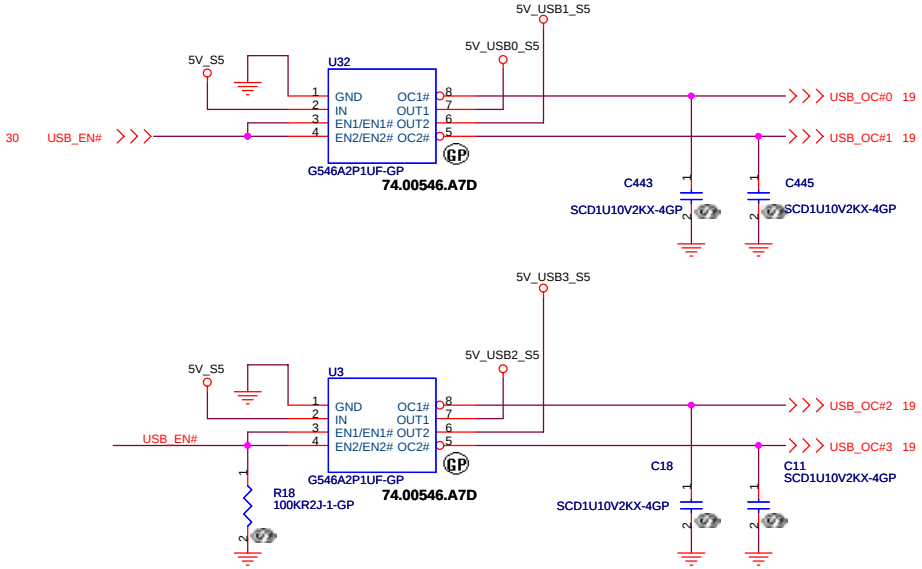
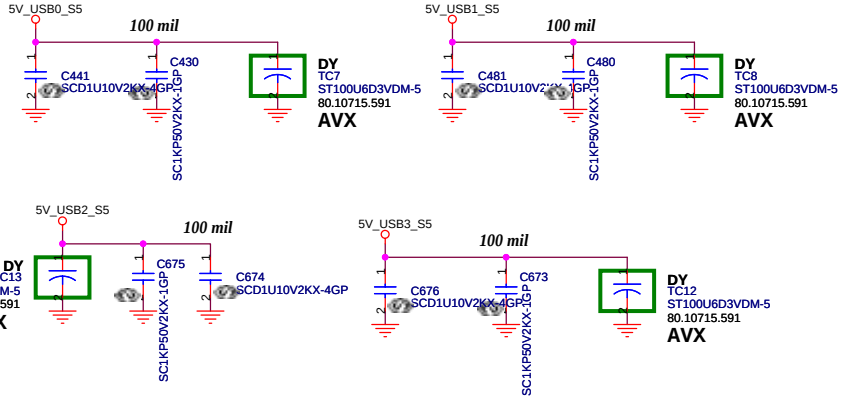
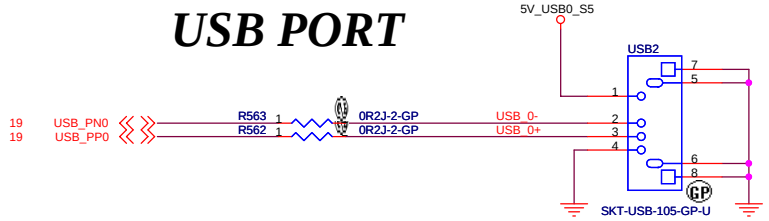
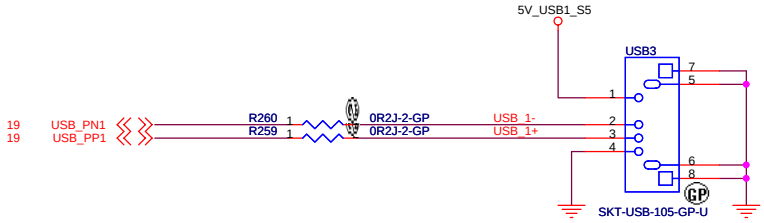


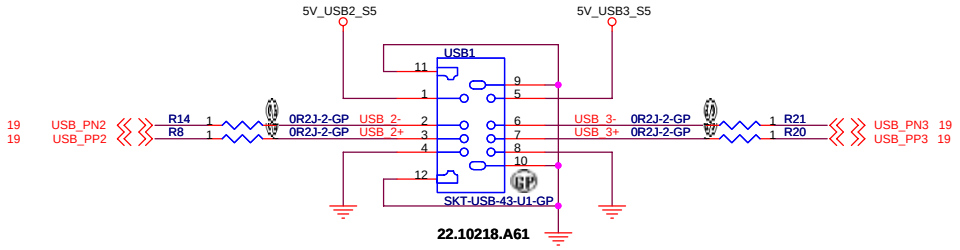


USB PORT

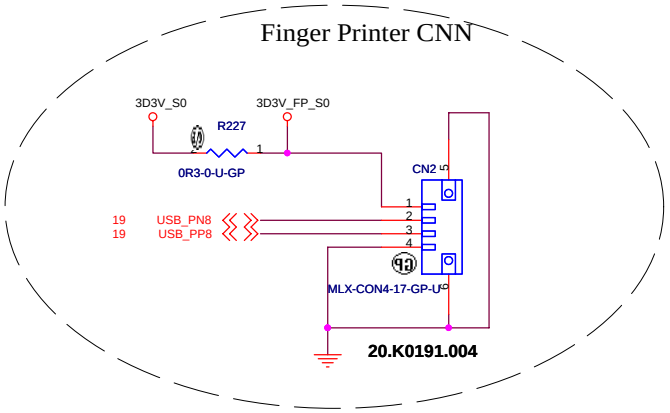


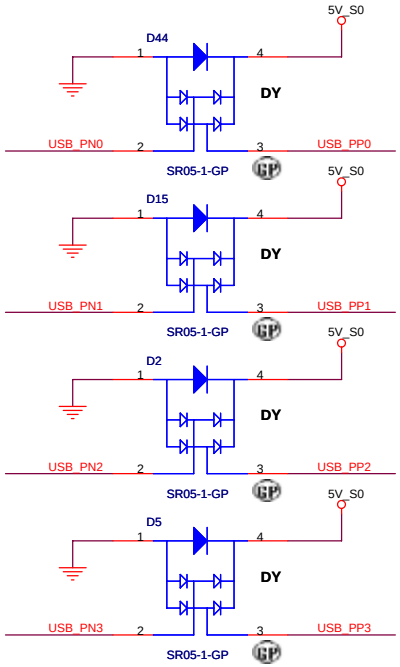


22.10218.J11



22.10218.A61





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB/MDC/BT and TV TURNER I/F

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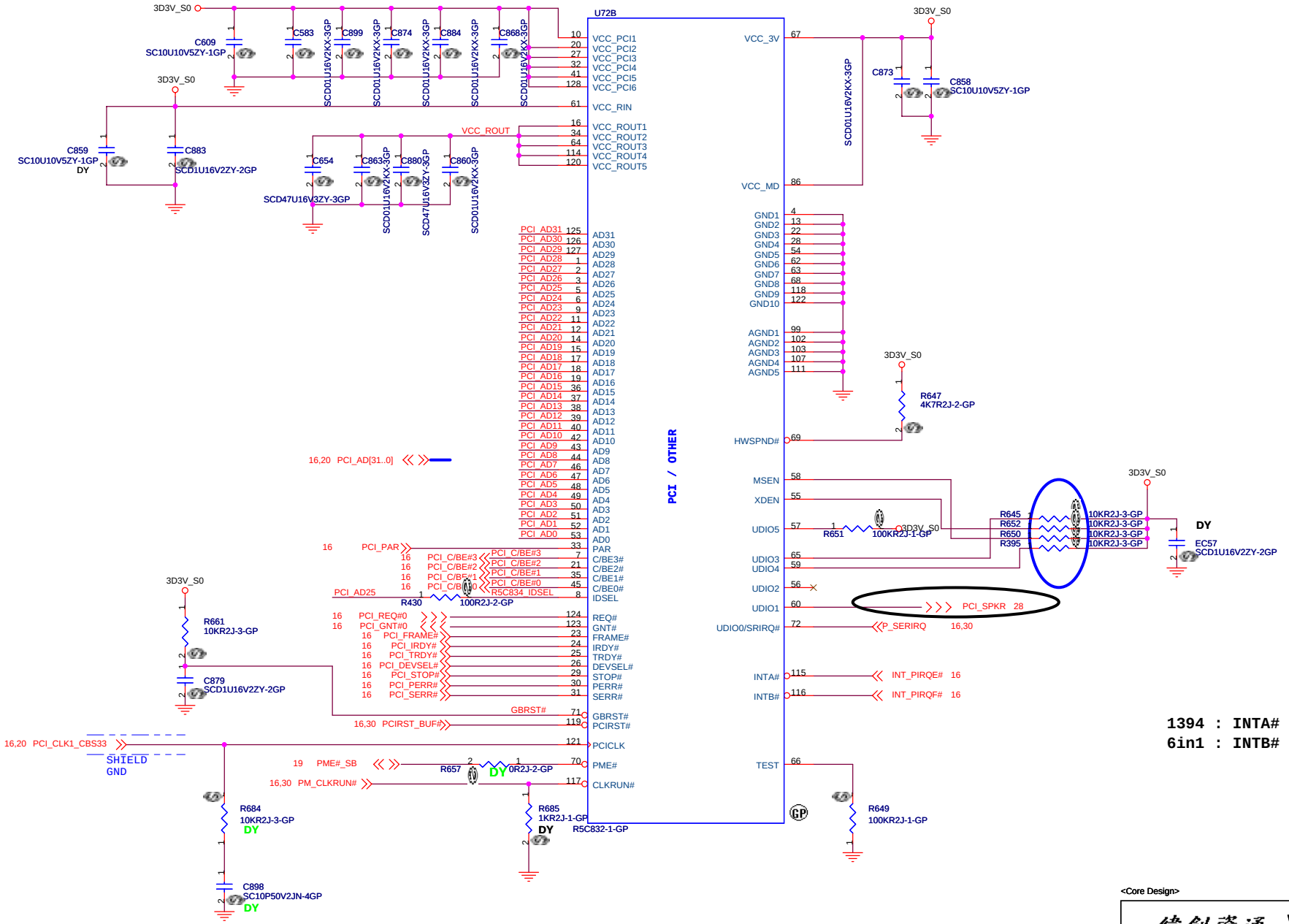

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RICOH R5C832(1/2)

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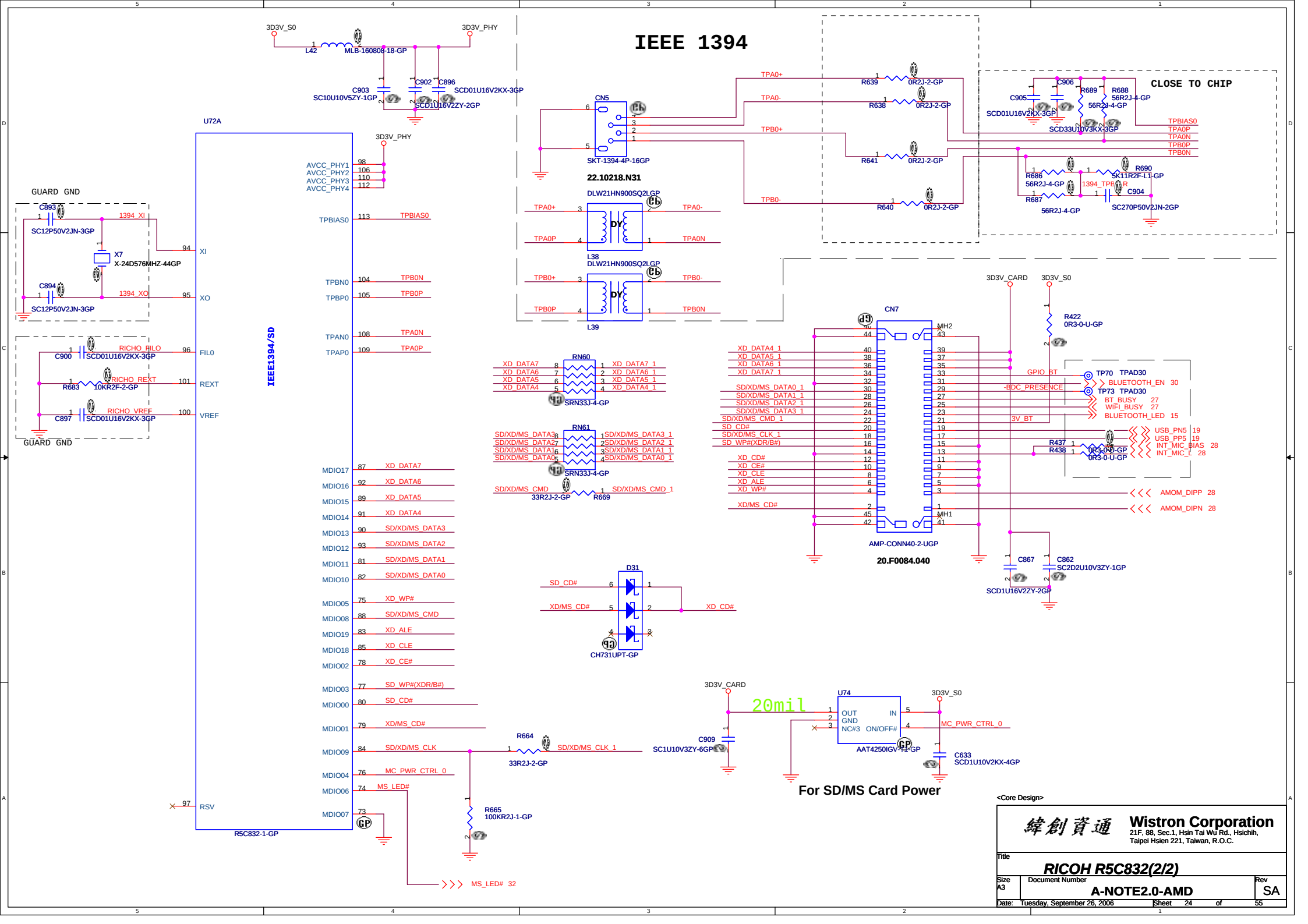
IEEE 1394



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RICOH R5C832(2/2)

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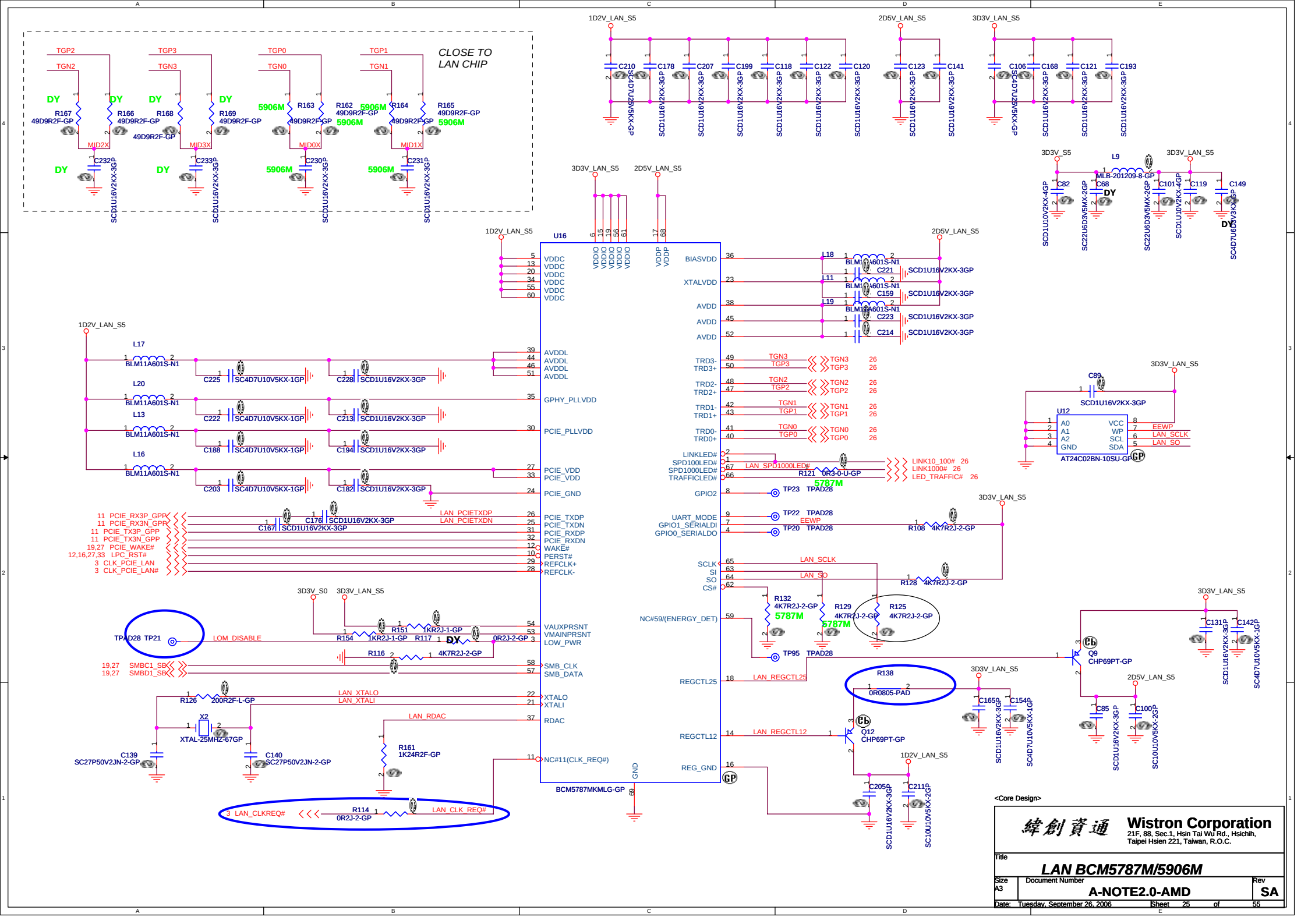
CLOSE TO LAN CHIP
TGP2
TGN2
TGP3
TGN3
TGP0
TGN0
TGP1
TGN1
DY
5906M
R167 49D9R2F-GP
R166 49D9R2F-GP
R168 49D9R2F-GP
R169 49D9R2F-GP
R163 49D9R2F-GP
R162 49D9R2F-GP
R164 49D9R2F-GP
R165 49D9R2F-GP
MID2X
MID3X
MID0X
MID1X
C232
C233
C230
C231
SCD1U16V2KX-3GP
1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
C210
C178
C207
C199
C118
C122
C120
C123
C141
C106
C168
C121
C193
SCD1U16V2KX-3GP
SCD47U25V5KX-GP
L9
MLB-201209-8-GP
C82
C68
C101
C119
C149
SCD1U10V2KX-4GP
SC22U6D3V5MX-2GP
SC22U6D3V5MX-4GP
SC4D7U6D3V3KX-GP
U16
VDDC
VDDIO
VDDP
BIASVDD
XTALVDD
AVDD
AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_VDD
PCIE_GND
PCIE_TXDP
PCIE_TXDN
PCIE_RXDP
PCIE_RXDN
WAKE#
PERST#
REFCLK+
REFCLK-
TRD3-
TRD3+
TRD2-
TRD2+
TRD1-
TRD1+
TRD0-
TRD0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
GPIO2
UART_MODE
GPIO1_SERIALDI
GPIO0_SERIALDO
SCLK
SI
SO
CS#
NC#59/(ENERGY_DET)
REGCTL25
REGCTL12
REG_GND
VAUXPRSNT
VMAINPRSNT
LOW_PWR
SMB_CLK
SMB_DATA
XTALO
XTALI
RDAC
NC#11(CLK_REQ#)
GND
BCM5787MKMLG-GP
L17
L20
L13
L16
L18
L11
L19
BLM11A601S-N1
C225
C222
C188
C203
C228
C213
C194
C182
C221
C159
C223
C214
SC4D7U10V5KX-1GP
SCD1U16V2KX-3GP
TGN3
TGP3
TGN2
TGP2
TGN1
TGP1
TGN0
TGP0
LAN_SPD1000LED#
R121 0R3-0-U-GP
LINK10_100#
LINK1000#
LED_TRAFFIC#
TP23 TPAD28
TP22 TPAD28
EEWP
TP20 TPAD28
R108 4K7R2J-2-GP
R128 4K7R2J-2-GP
LAN_SCLK
LAN_SO
R132 4K7R2J-2-GP
R129 4K7R2J-2-GP
R125 4K7R2J-2-GP
5787M
TP95 TPAD28
LAN_REGCTL25
LAN_REGCTL12
R138 0R0805-PAD
Q12 CHP69PT-GP
Q9 CHP69PT-GP
C165
C154
C85
C100
C131
C142
SCD1U16V2KX-3GP
SC4D7U10V5KX-1GP
SC10U10V5KX-2GP
C89
U12
AT24C02BN-10SU-GP
A0
A1
A2
GND
VCC
WP
SCL
SDA
EEWP
LAN_SCLK
LAN_SO
11 PCIE_RX3P_GPP
11 PCIE_RX3N_GPP
11 PCIE_TX3P_GPP
11 PCIE_TX3N_GPP
19,27 PCIE_WAKE#
12,16,27,33 LPC_RST#
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
LAN_PCIETXDP
LAN_PCIETXDN
C176 SCD1U16V2KX-3GP
C167 SCD1U16V2KX-3GP
3D3V_S0
R151 1KR2J-1-GP
R154 1KR2J-1-GP
R117 1KR2J-1-GP
0R2J-2-GP
DY
TPAD28 TP21
LOM_DISABLE
R116 4K7R2J-2-GP
19,27 SMBC1_SB
19,27 SMBD1_SB
R126 200R2F-L-GP
X2
XTAL-25MHZ-67GP
C139 SC27P50V2JN-2-GP
C140 SC27P50V2JN-2-GP
R161 1K24R2F-GP
3 LAN_CLKREQ#
R114 0R2J-2-GP
LAN_CLK_REQ#
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN BCM5787M/5906M
Size A3
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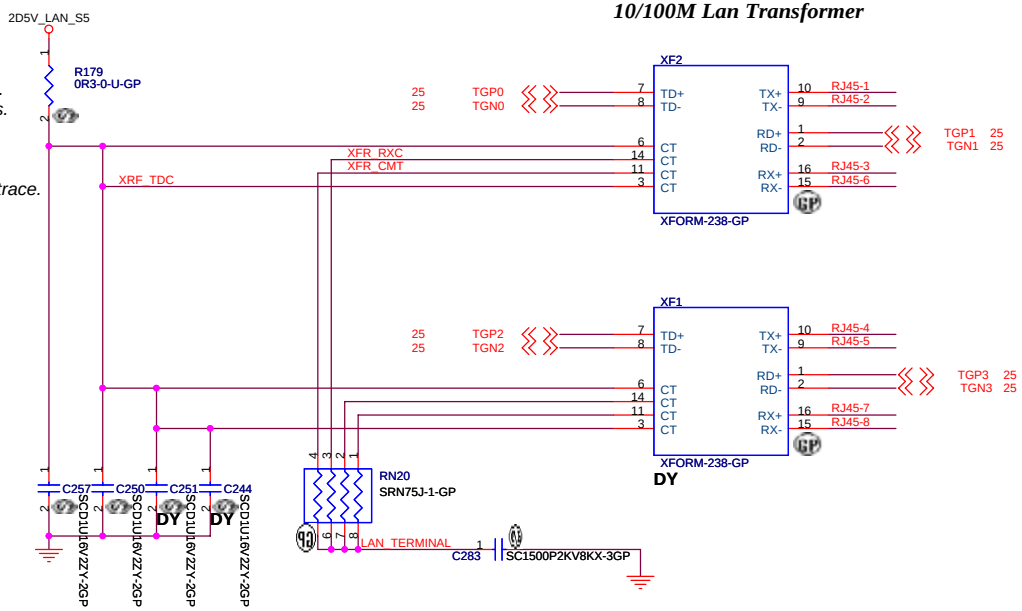
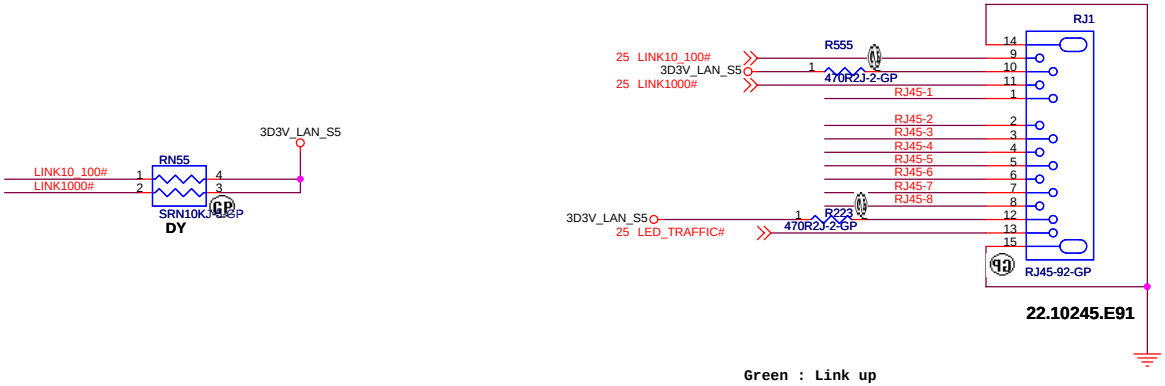
10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



PIN09 : GREEN
PIN11 : ORANGE



Green : Link up
Blinking : TX/RX activity

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LAN Connector***
Size: A3	Document Number: **A-NOTE2.0-AMD**
Rev: **SA**	
Date: Tuesday, September 26, 2006	Sheet 26 of 55

NEWCARD Connector

Place them Near to Chip

3D3V_S5 1D5V_S0

C650 DY SCD1U16V2ZY-2GP

C631 DY SCD1U16V2ZY-2GP

Place them Near to Connector

3D3V_NEW_S0 1D5V_NEW_S0 3D3V_NEW_LAN_S5

C648 SC10U10V5ZY-1GP

C651 SCD1U16V2ZY-2GP

C656 SC10U10V5ZY-1GP

C655 SCD1U16V2ZY-2GP

C653 SCD1U16V2ZY-2GP

3D3V_NEW_S0 1D5V_NEW_S0

U50

16,19,30,35,43,46,49 PM_SLP_S3#

2,16,25,33 LPC_RST#

R415 33R2J-2-GP

TPAD30 TP74

19,30,42 PM_SLP_S5#

C621 SC22P50V2JN-4GP

R5538D001-TR-FGP

PERST# CPUSB# CPPE# NEWCARD_OC#

STBY# SYSRST# PERST# CPUSB# CPPE# OC# SHDN#

3.3VOUT 3.3VOUT 1.5VOUT 1.5VOUT

3.3VIN 3.3VIN 1.5VIN 1.5VIN

GND THERMAL_PAD RCLKEN AUXIN AUXOUT NC#16

R436 DUMMY-R2

3D3V_S5 3D3V_NEW_LAN_S5

NEWCARD_RST# 19

3D3V_S0 1D5V_S0

SC4D7U10V5ZY-3GP C634 C642 SCD1U16V2ZY-2GP

SC4D7U10V5ZY-3GP C637 C649 SCD1U16V2ZY-2GP

NEW1

FCI-CON26-6-GP-U

62.10081.031

PCIE_TX2P_GPP 11 PCIE_TX2N_GPP 11

PCIE_RX2P_GPP 11 PCIE_RX2N_GPP 11

CLK_PCIE_NEW 3 CLK_PCIE_NEW# 3

CPPE# NEWCARD_CLKREQ# NEWCARD_CLKREQ# 3

3D3V_NEW_S0

PERST#

3D3V_NEW_LAN_S5

PCIE_WAKE# 19,25

1D5V_NEW_S0

SMBD1_SB 19,25 SMBC1_SB 19,25

CONN_TP2 TP75 TPAD30 CONN_TP3 TP76 TPAD30

CPUSB#

USB_PP9 19 USB_PN9 19

CN3

CARDBUS-SKT-GP

21.H0119.001

For Newcard socket

3D3V_S0 1D5V_S0 3D3V_S5

C870 SC1U10V2ZY C840 SCD1U16V2ZY-2GP

C853 SC1U10V2ZY C864 SCD1U16V2ZY-2GP

C851 SCD1U16V2ZY-2GP

Place near MINIC1

Mini Card Connector

MINIC1

R604 0R2J-2-GP

19,25 PCIE_WAKE# MINIC_WAKE#

24 BT_BUSY 24 WIFI_BUSY

TPAD30 TP129

3 CLK_PCIE_MINI# 3 CLK_PCIE_MINI

30 E51_RX 30 E51_TX

R626 0R2J-2-GP R630 0R2J-2-GP

DEBUG_RX DEBUG_TX

12 PCIE_RX0N_GPP 12 PCIE_RX0P_GPP

12 PCIE_TX0N_GPP 12 PCIE_TX0P_GPP

5V_AUX_S5

C548 SCD1U16V2ZY-2GP

SKT-MINI52P-6-GP

62.10043.261

NP1 NP2

10KR2J-3-GP R628

WIFI_RF_EN 30 LPC_RST# 12,16,25,33

SMBC1_SB 19,25 SMBD1_SB 19,25

USB_PN4 19 USB_PP4 19

LED_WWAN# TPAD28 TP132 WLAN_LED# 15

TP63 TPAD28

EC55 EC56 EC58

SCD1U10V2KX-4GP SCD1U10V2KX-4GP SCD1U10V2KX-4GP

WIRELESS SWITCH

3D3V_S0

R704 100KR2J-1-GP

WIRLESS_DISABLE# 30

CN4

SW-SLIDE57-GP

22.40048.741

C918 SCD1U16V2ZY-2GP DY

Iomax=300mA

3D3V_S0 1D5V_S0

U69

VOUT VIN GND

APL5308-15AC-GP

C838 SC10U10V5ZY-1GP

Place near to mini-card conn

<Core Design>

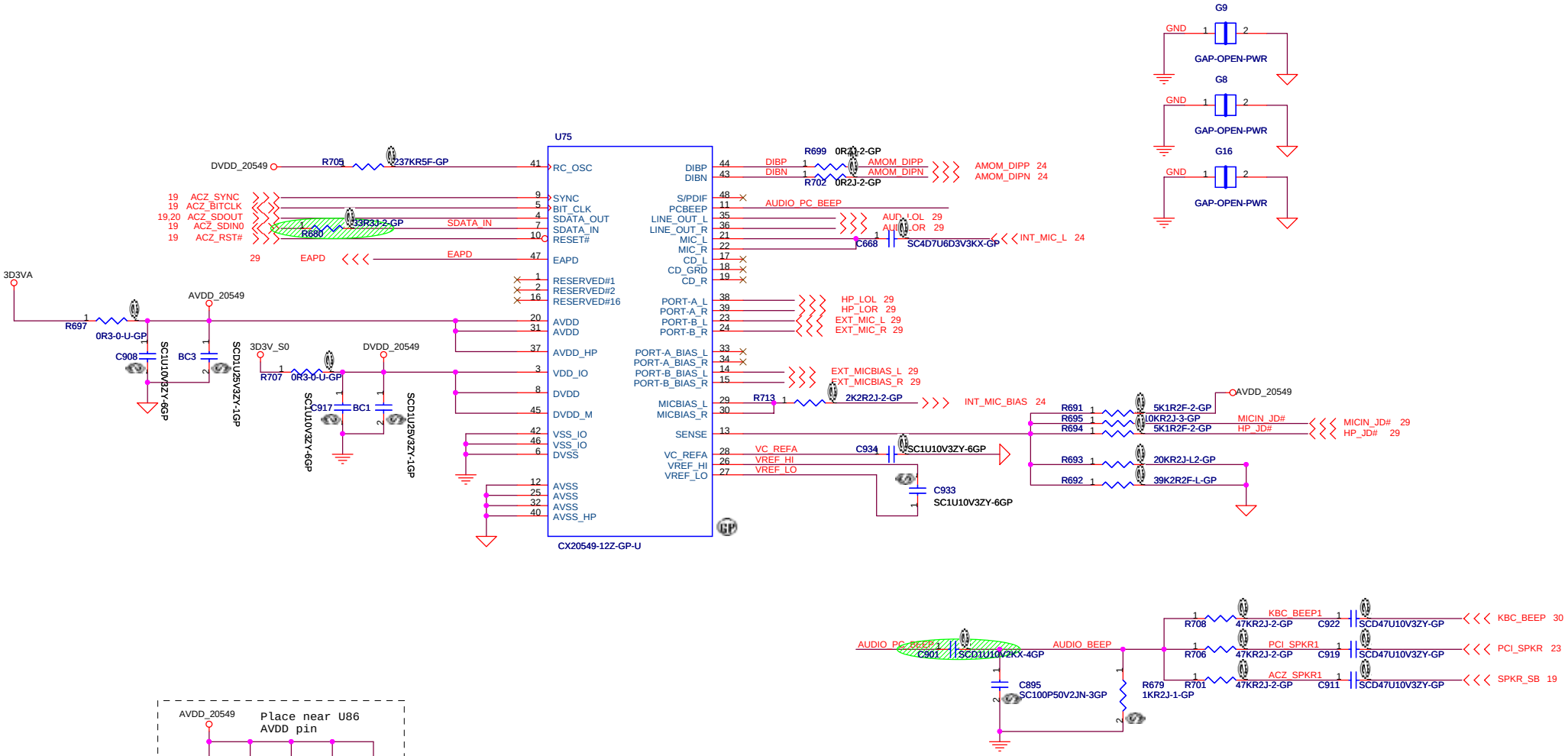
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI-PCIE

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 27 of 55



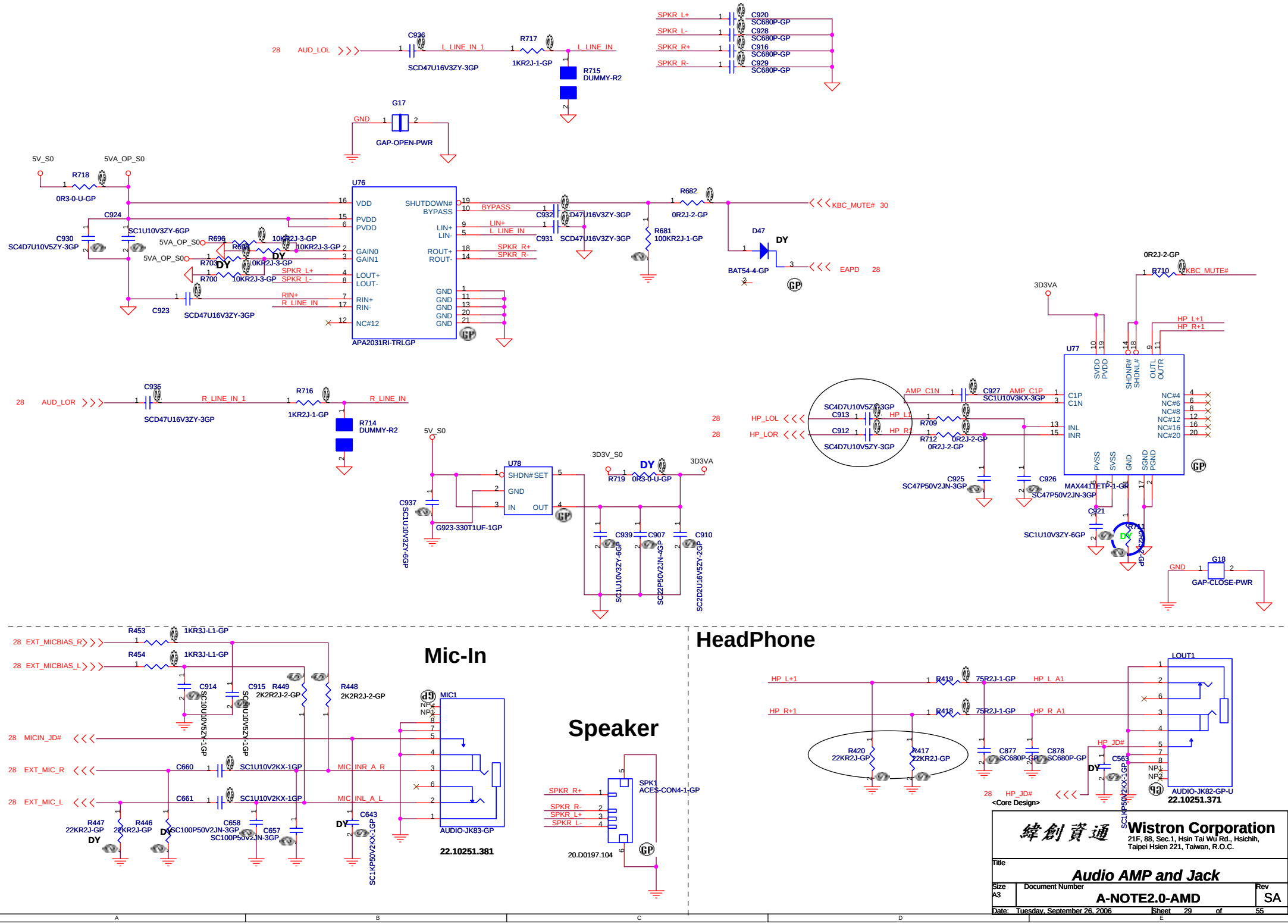
<Core Design>

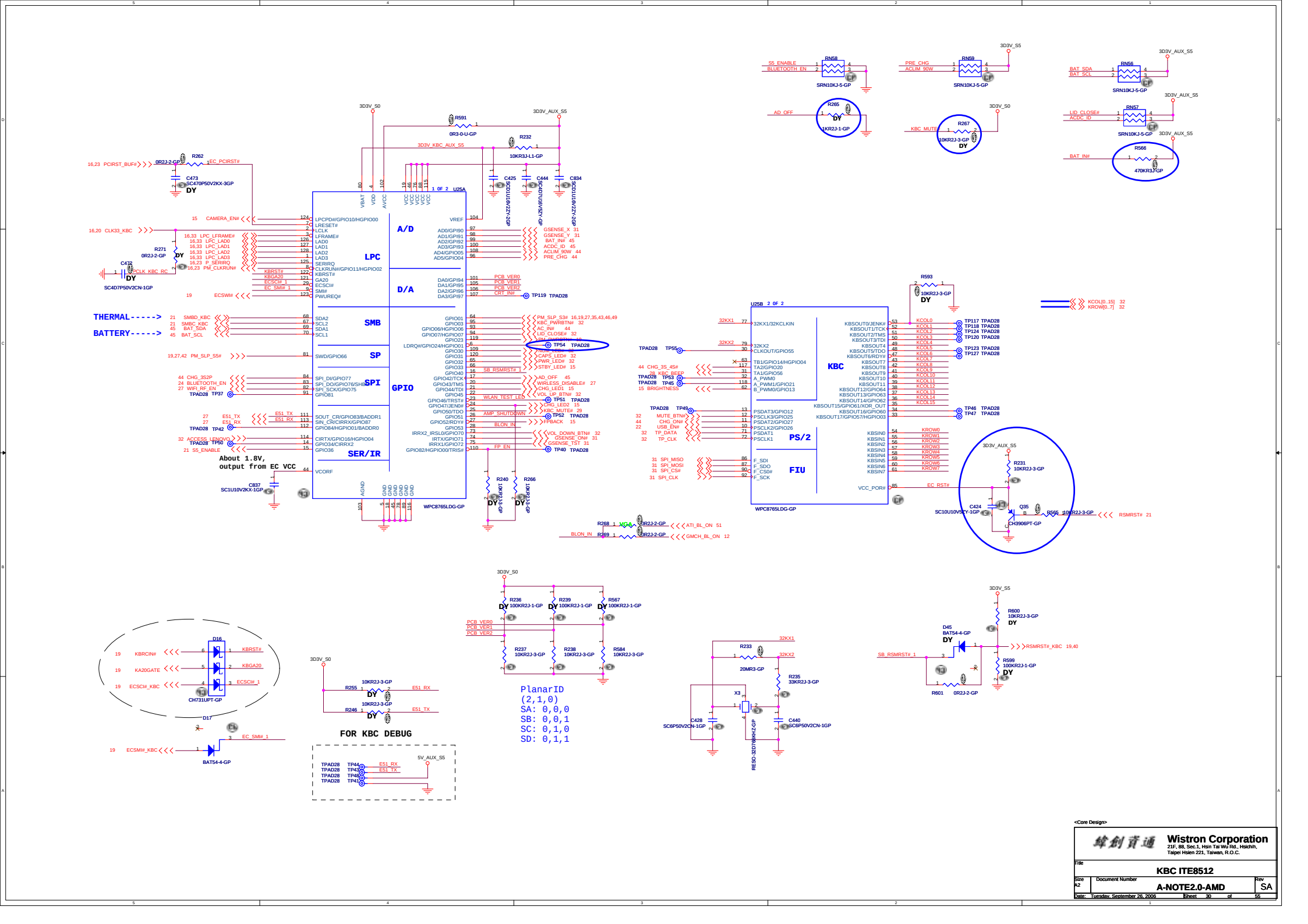
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

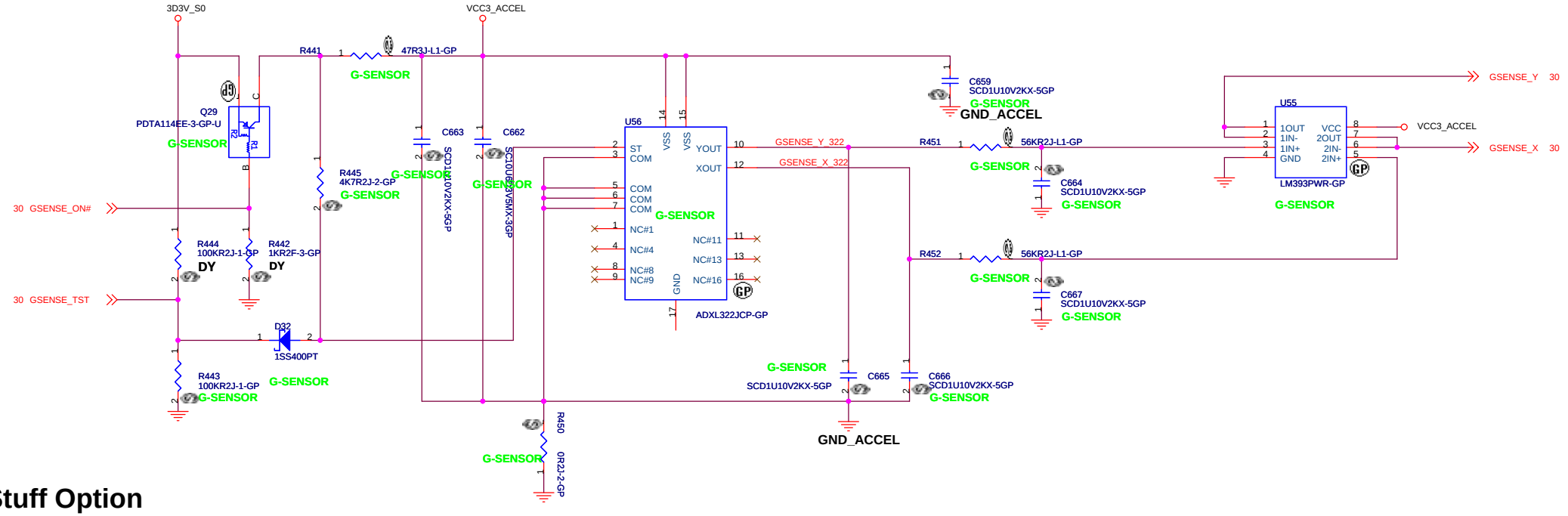
Title: ***AUDIO (1/2) -- CODEC CX20549***

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 28 of 55


AUD_LOL
C926
SCD47U16V3ZY-3GP
L_LINE_IN_1
R717
1KR2J-1-GP
L_LINE_IN
R715
DUMMY-R2
SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-
C920
C928
C916
C929
SC680P-GP
G17
GND
GAP-OPEN-PWR
5V_S0
5VA_OP_S0
R718
0R3-0-U-GP
U76
APA2031RI-TRLGP
VDD
PVDD
GAIN0
GAIN1
LOUT+
LOUT-
RIN+
RIN-
NC#12
SHUTDOWN#
BYPASS
LIN+
LIN-
ROUT+
ROUT-
GND
C924
SC1U10V3ZY-6GP
C930
SC4D7U10V5ZY-3GP
R696
R699
R703
R700
10KR2J-3-GP
DY
SPKR_L+
SPKR_L-
C923
SCD47U16V3ZY-3GP
RIN+
R_LINE_IN
C932
C931
SCD47U16V3ZY-3GP
R682
0R2J-2-GP
R681
100KR2J-1-GP
KBC_MUTE#
30
D47
BAT54-4-GP
EAPD
28
GP
AUD_LOR
C935
R_LINE_IN_1
R716
R_LINE_IN
R714
DUMMY-R2
U78
SHDN#
SET
GND
IN
OUT
3D3V_S0
3D3VA
R719
C937
G923-330T1UF-1GP
C939
C907
C910
SC1U10V3ZY-6GP
SC22P50V2JN-4GP
SC2D2U16V5ZY-2GP
HP_LOL
HP_LOR
C913
C912
SC4D7U10V5ZY-3GP
HP_L1
HP_R1
R709
R712
0R2J-2-GP
U77
MAX4411ETP-1-GP
AMP_C1N
AMP_C1P
C927
SC1U10V3KX-3GP
C1P
C1N
INL
INR
SVDD
PVDD
SHDNR#
SHDNL#
OUTL
OUTR
PVSS
SVSS
GND
SGND
PGND
NC#4
NC#6
NC#8
NC#12
NC#16
NC#20
C925
SC47P50V2JN-3GP
C926
SC47P50V2JN-3GP
C921
SC1U10V3ZY-6GP
R711
DY
SC2K-GP
HP_L+1
HP_R+1
R710
KBC_MUTE#
G18
GAP-CLOSE-PWR
Mic-In
EXT_MICBIAS_R
EXT_MICBIAS_L
R453
R454
1KR3J-L1-GP
C914
C915
SC10U10V5ZY-1GP
R449
2K2R2J-2-GP
R448
2K2R2J-2-GP
MIC1
MICIN_JD#
EXT_MIC_R
EXT_MIC_L
C660
C661
SC1U10V2KX-1GP
MIC_INR_A_R
MIC_INL_A_L
R447
R446
22KR2J-GP
SC100P50V2JN-3GP
C658
C657
C643
SC1KP50V2KX-1GP
AUDIO-JK83-GP
22.10251.381
Speaker
SPK1
ACES-CON4-1-GP
20.D0197.104
HeadPhone
HP_L+1
HP_R+1
R419
R418
75R2J-1-GP
HP_L_A1
HP_R_A1
R420
R417
22KR2J-GP
C877
C878
SC680P-GP
HP_JD#
C563
LOUT1
AUDIO-JK82-GP-U
22.10251.371
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio AMP and Jack
Size
A3
Document Number
A-NOTE2.0-AMD
Rev
SA
Date: Tuesday, September 26, 2006
Sheet 29 of 55


THERMAL------>
BATTERY------>
About 1.8V, output from EC VCC
FOR KBC DEBUG
PlanarID (2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
WPC8765LDG-GP
U25A 1 OF 2
U25B 2 OF 2
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC ITE8512
A-NOTE2.0-AMD
Tuesday, September 26, 2006

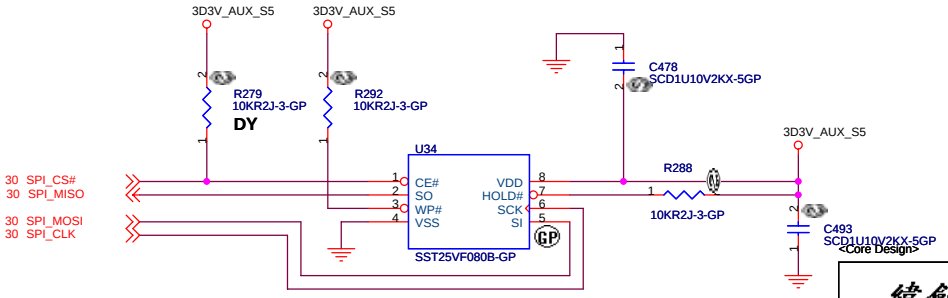


Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

SPI ROM for System & KBC



1. SST 25VF016B
2. Macronix MX25L1605A
3. SST 8Mbit 72.25080.G01

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS ROM/G-Sensor

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

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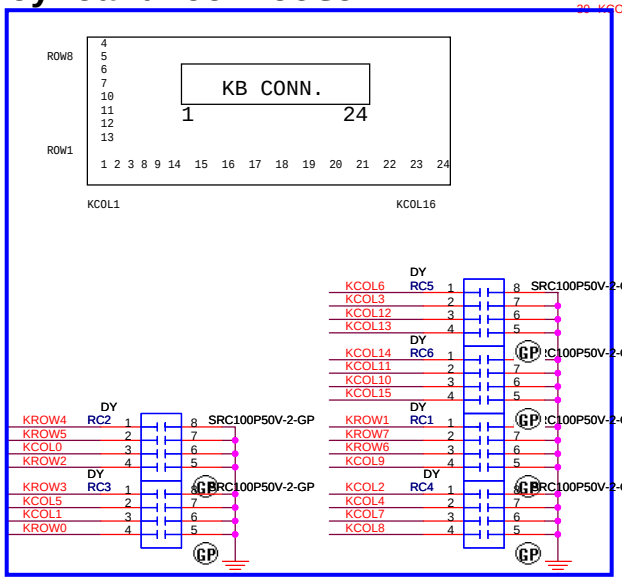
Internal KeyBoard Connector



30 KROW[0..7]
30 KCOL[0..15]
1
25
K/B

KB1
ACES-CON24-1-GP
20.K0197.024

COVER SWITCH

CVR1
COVER_SW
R13
100R2J-2-GP
LID_CLOSE# 30
C9
SC1KP50V2KX-1GP
SW-SLIDE7-GP
62.40014.071

Lanuch Board CNN

3D3V_AUX_S5
R102
R105
10KR2J-3-GP
30 KBC_PWRBTN#
30 ACCESS_LENOVO
R103
R104
470R2J-2-GP
PWRBTN#
ACCESS_SYS#
C96
C97
SCD1U16V2ZY-2GP

3D3V_S0
3D3V_S5
CN1
ACCESS_SYS#
PWRBTN#
VOL_DOWN#
MUTE#
VOL_UP#
30 PWR_LED#
24 MS_LED#
15 MEDIA_LED#
30 CAPS_LED#
30 NUM_LED#
C80
C79
ACES-CON20-3-GP
20.K0262.020

3D3V_S5
R99
R96
R100
30 MUTE_BTN#
30 VOL_UP_BTN#
30 VOL_DOWN_BTN#
R98
R97
R101
MUTE#
VOL_UP#
VOL_DOWN#
C94
C93
C95

TOUCH PAD

5V_S0
SRN10KJ-5-GP
RN39
30 TP_DATA
30 TP_CLK
C423
C417
SC33P50V2JN-3GP
TPAD1
ACES-CON6-5GP
20.K0204.006
C273
C268
SCD1U16V2ZY-2GP
SCD1U10V3ZY-6GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAUNCH / TOUCHPAD / KB CONN
Size: A3
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Sheet 32 of 55

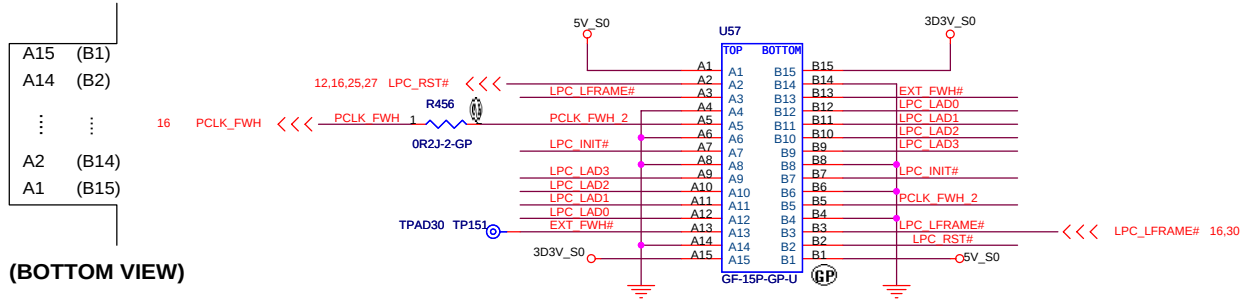
LPC_LAD[0..3] 16,30

GOLDEN FINGER FOR DEBUG BOARD

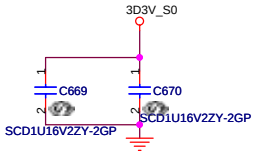
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

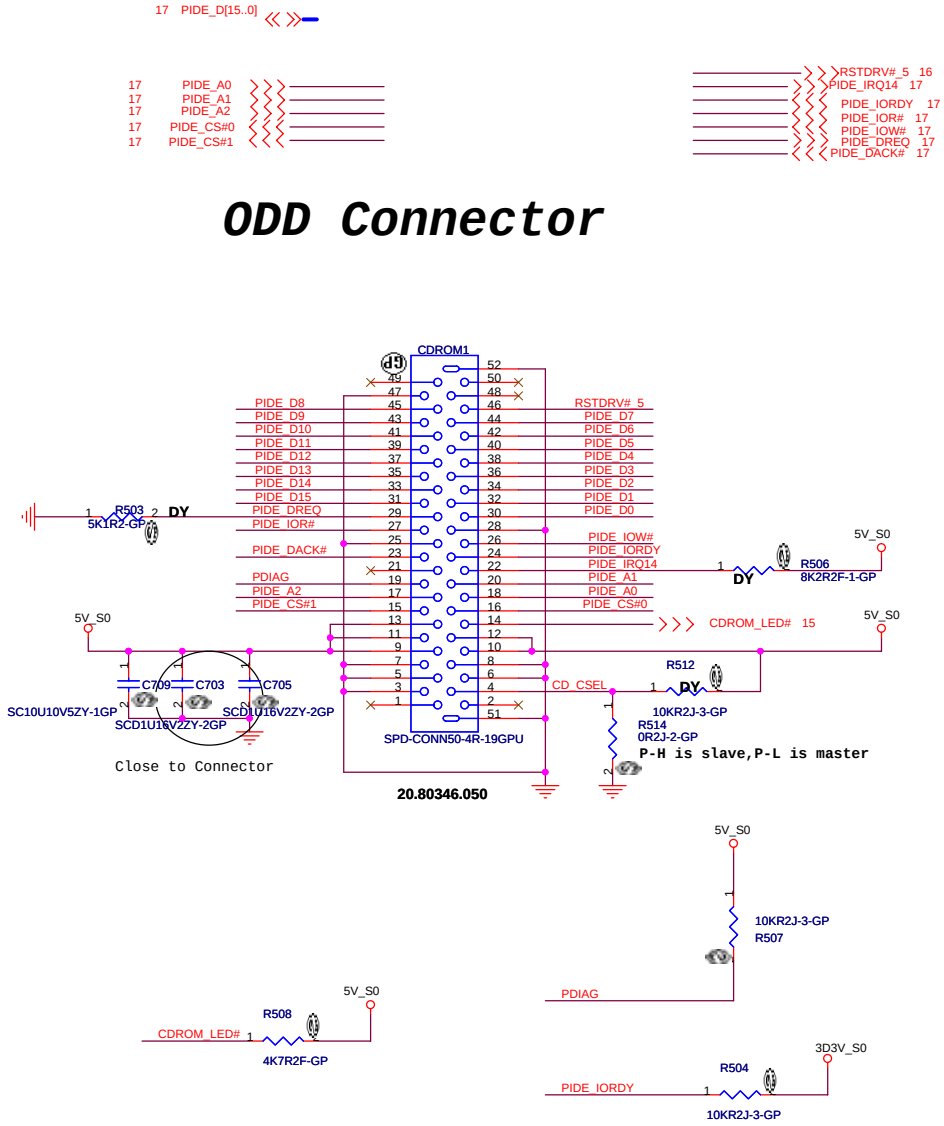


<Core Design>

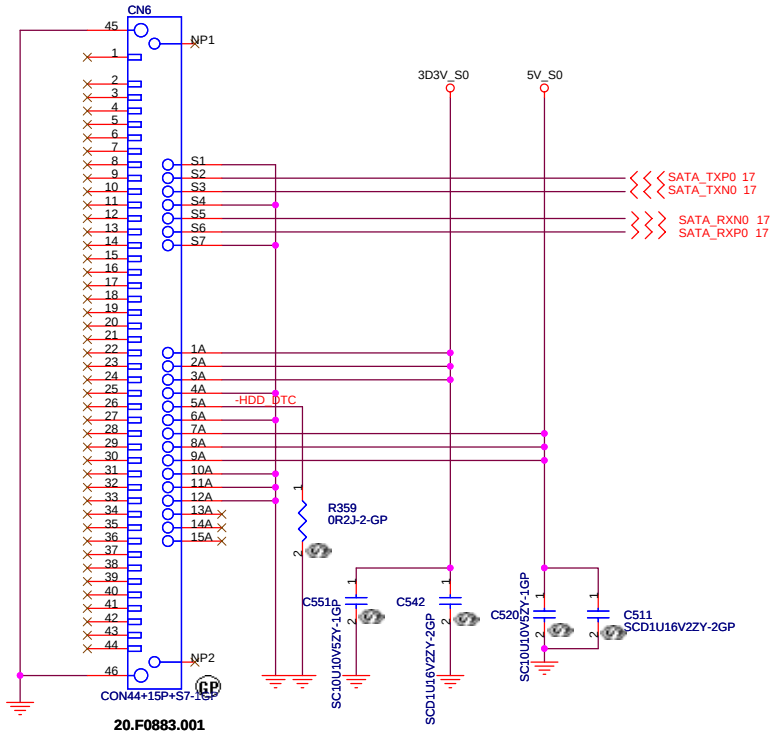
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Debug (Gold Finger)***	
Size A3	Document Number ***A-NOTE2.0-AMD***	Rev **SA**
Date: Tuesday, September 26, 2006	Sheet 33 of 55	

ODD Connector



SATA HD Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM CONN

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

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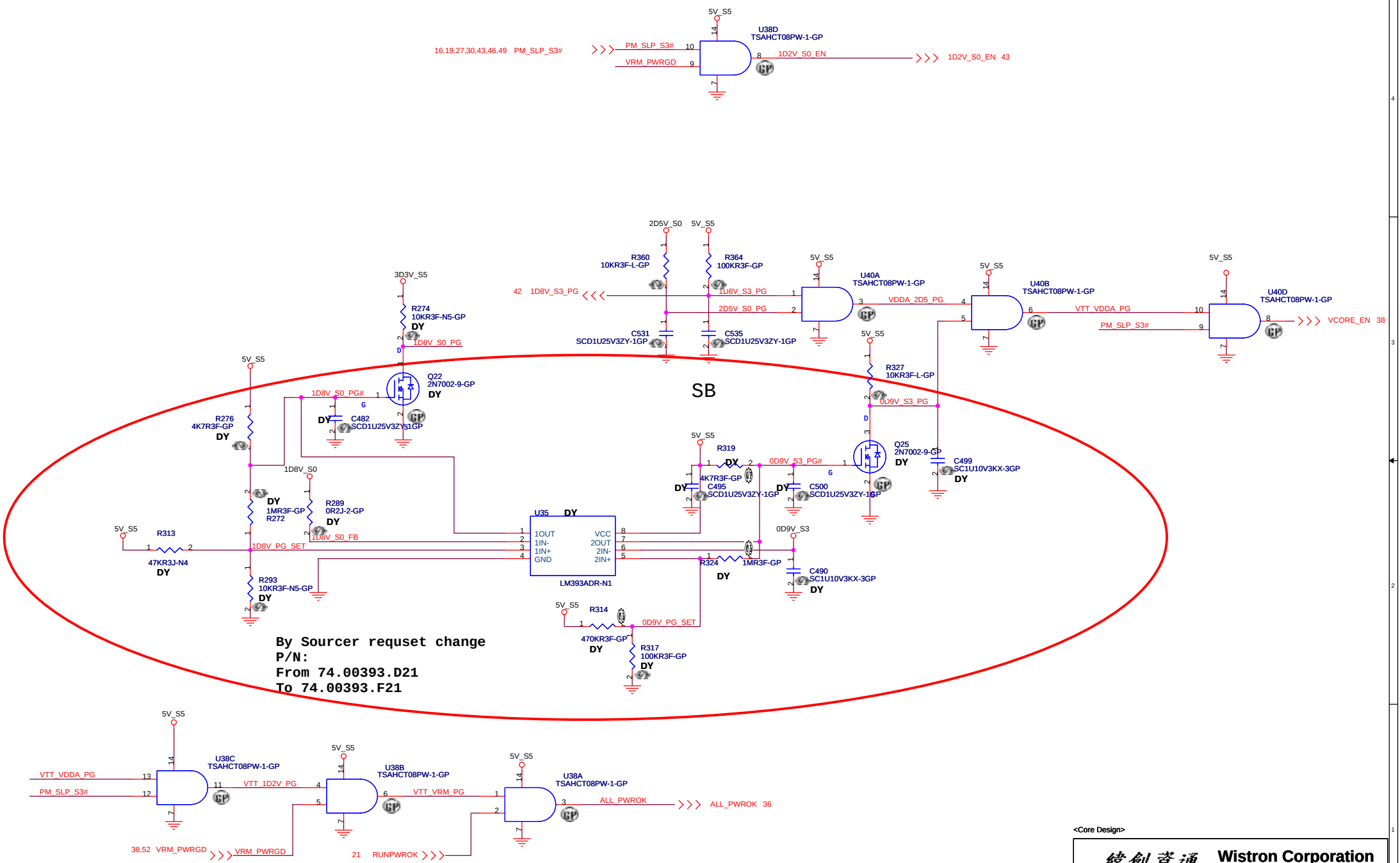


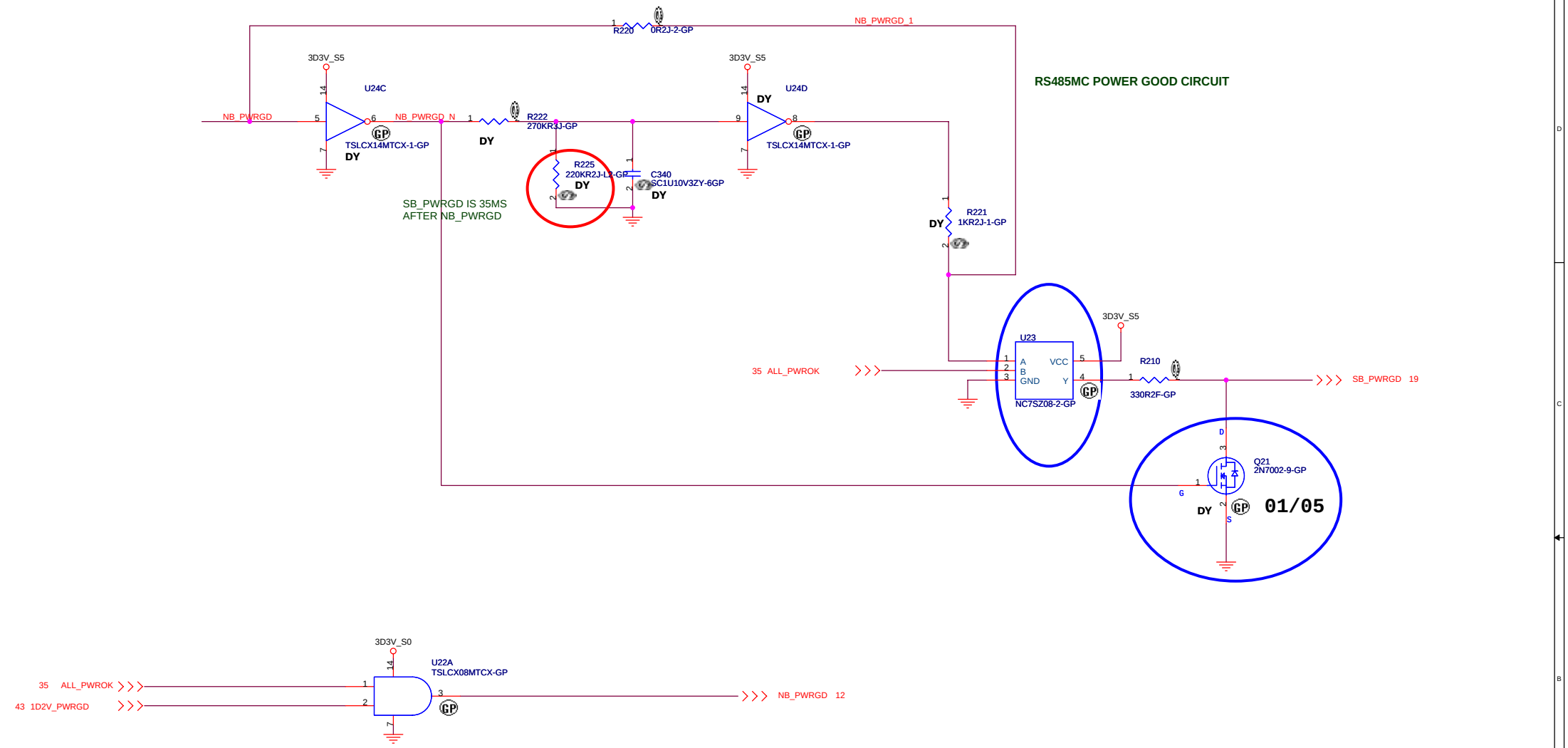
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWERGOOD&ENABLES(1/2)***

Size	Document Number	Rev
Custom	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 35 of 55



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
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CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

DCBATOUT
5V_S5

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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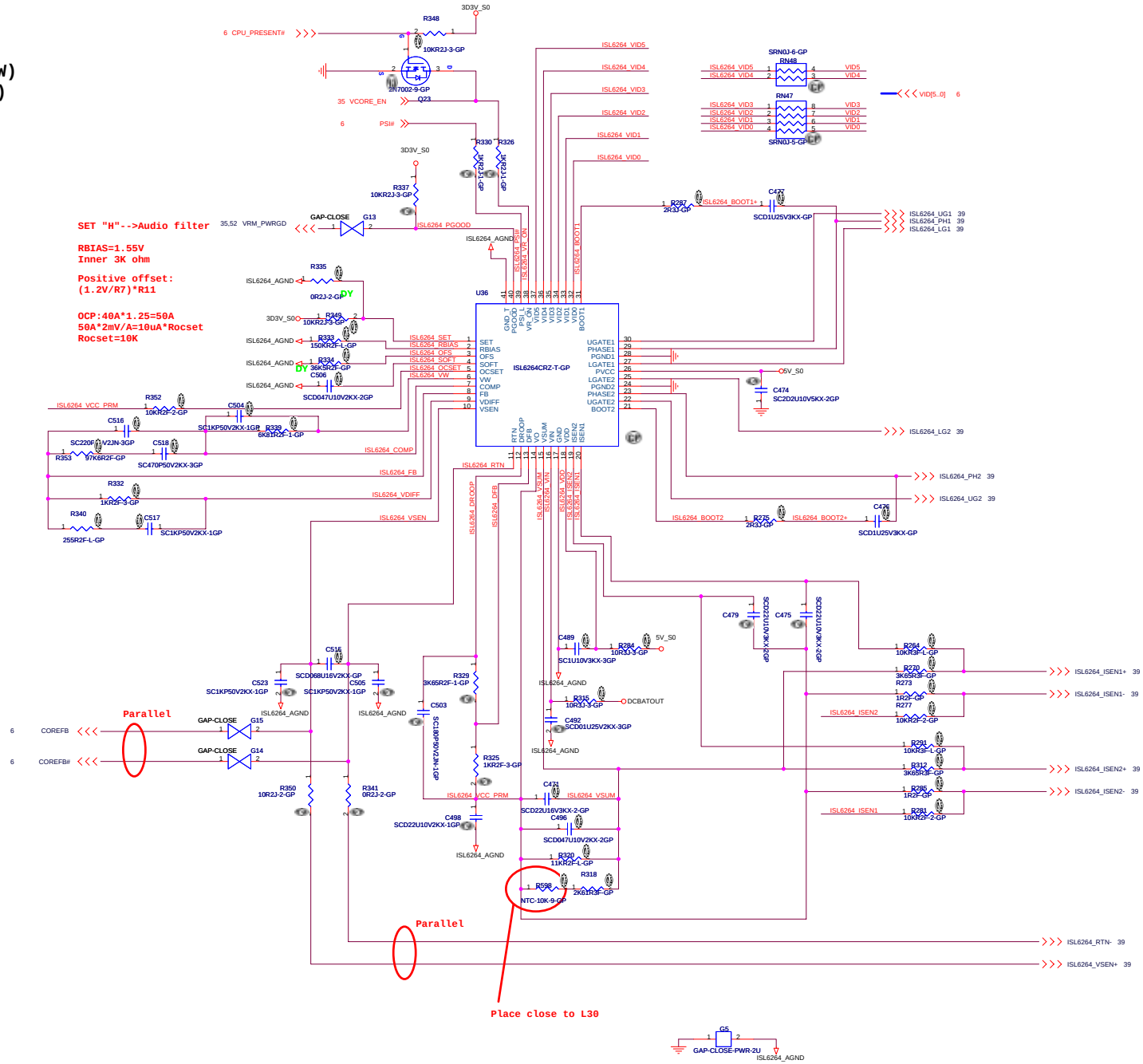
Date: Tuesday, September 26, 2006 Sheet 37 of 55

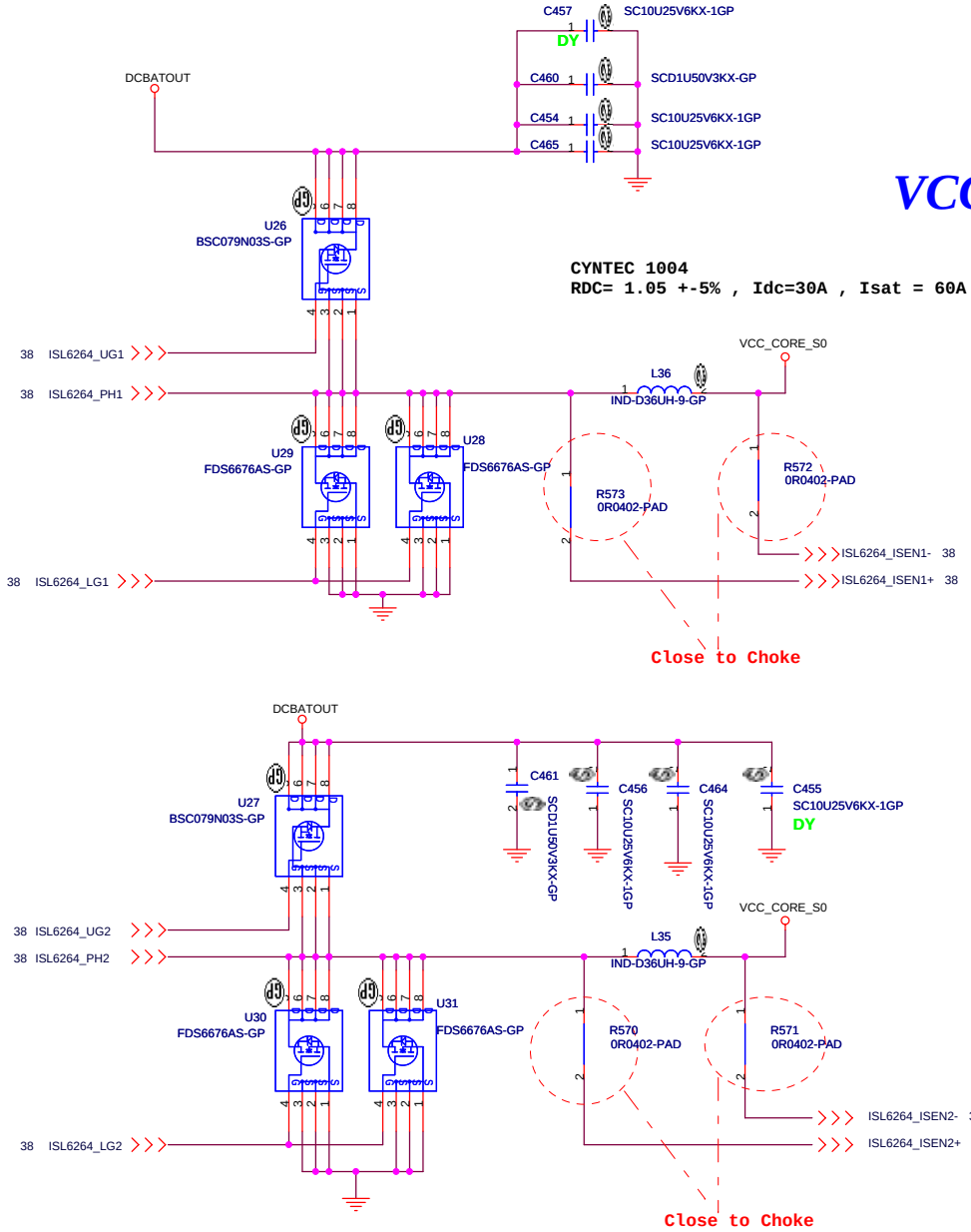
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



VCC_CORE_S0



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU Vcore Power_2		
Size: A3	Document Number: A-NOTE2.0-AMD	Rev: SA
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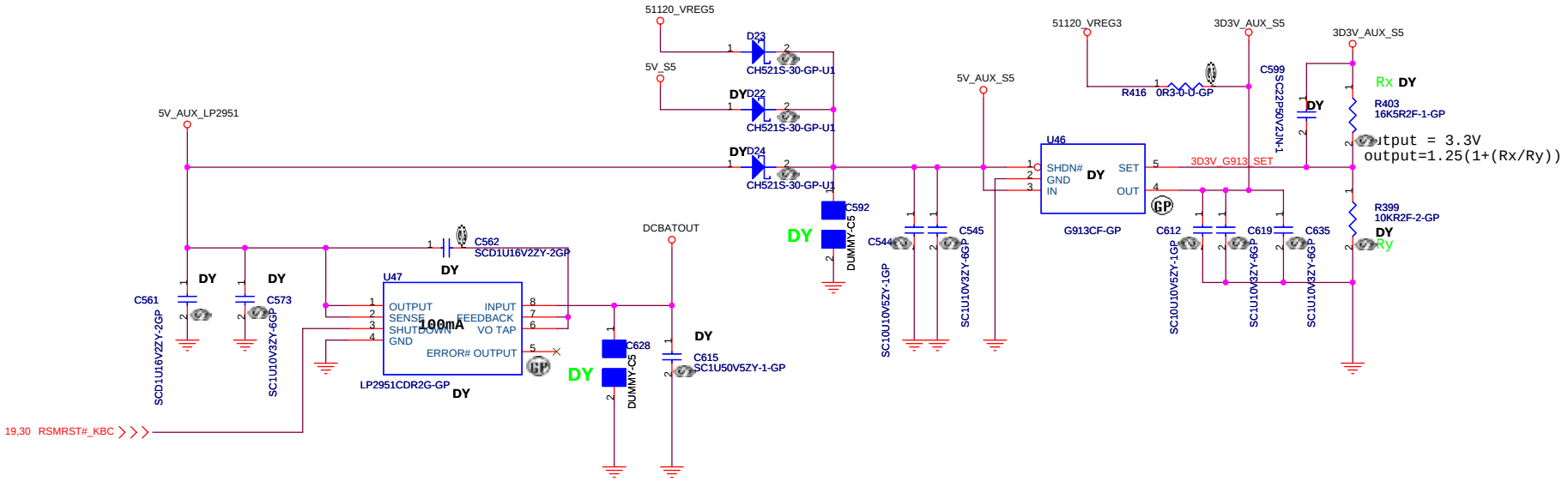
Aux Power

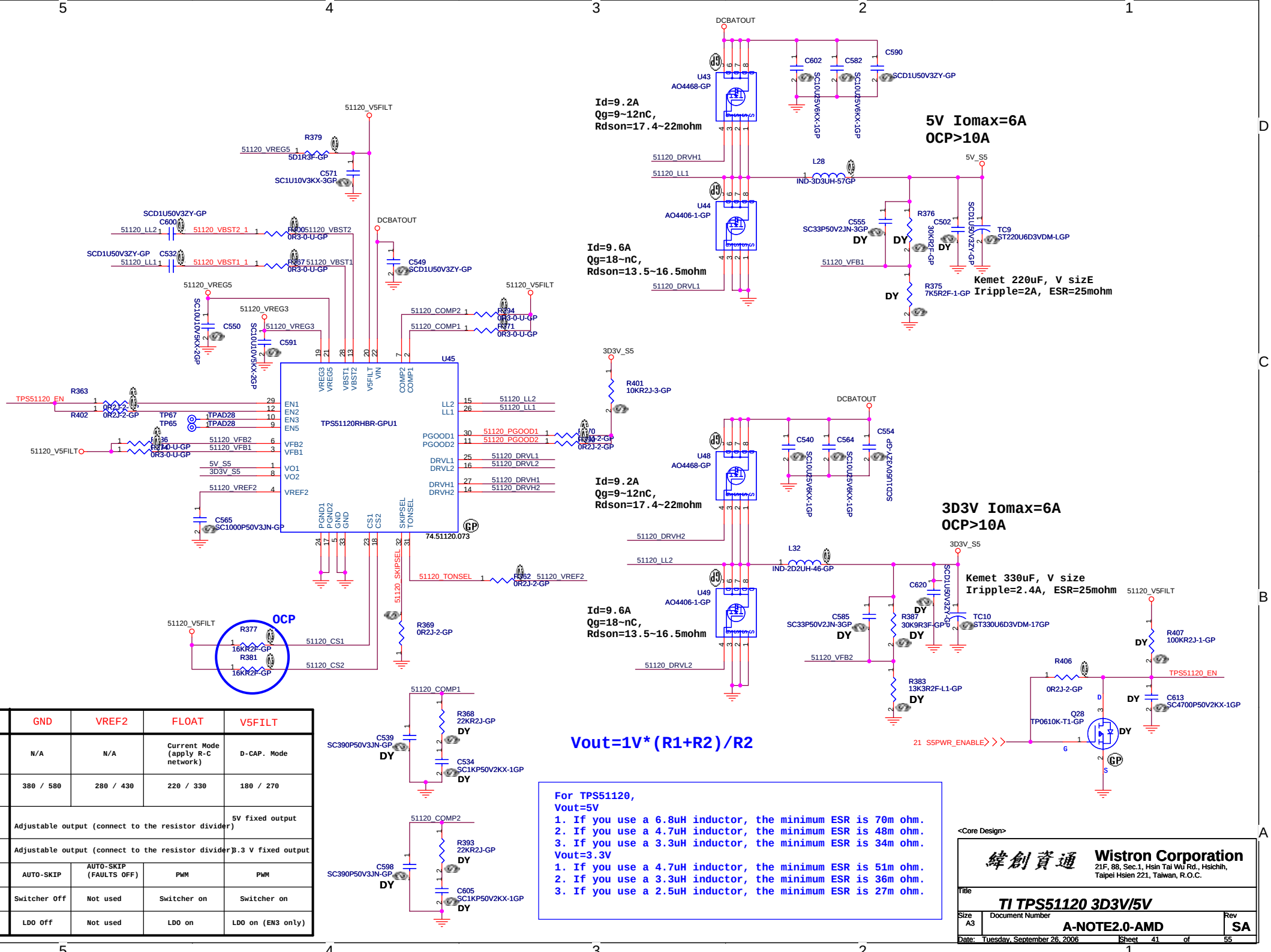
3D3V_AUX_S5



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	3D3V/ 5V_AUX	
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 40 of 55	



Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3 V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on
EN3, EN5	LDO Off	Not used	LDO on	LDO on (EN3 only)

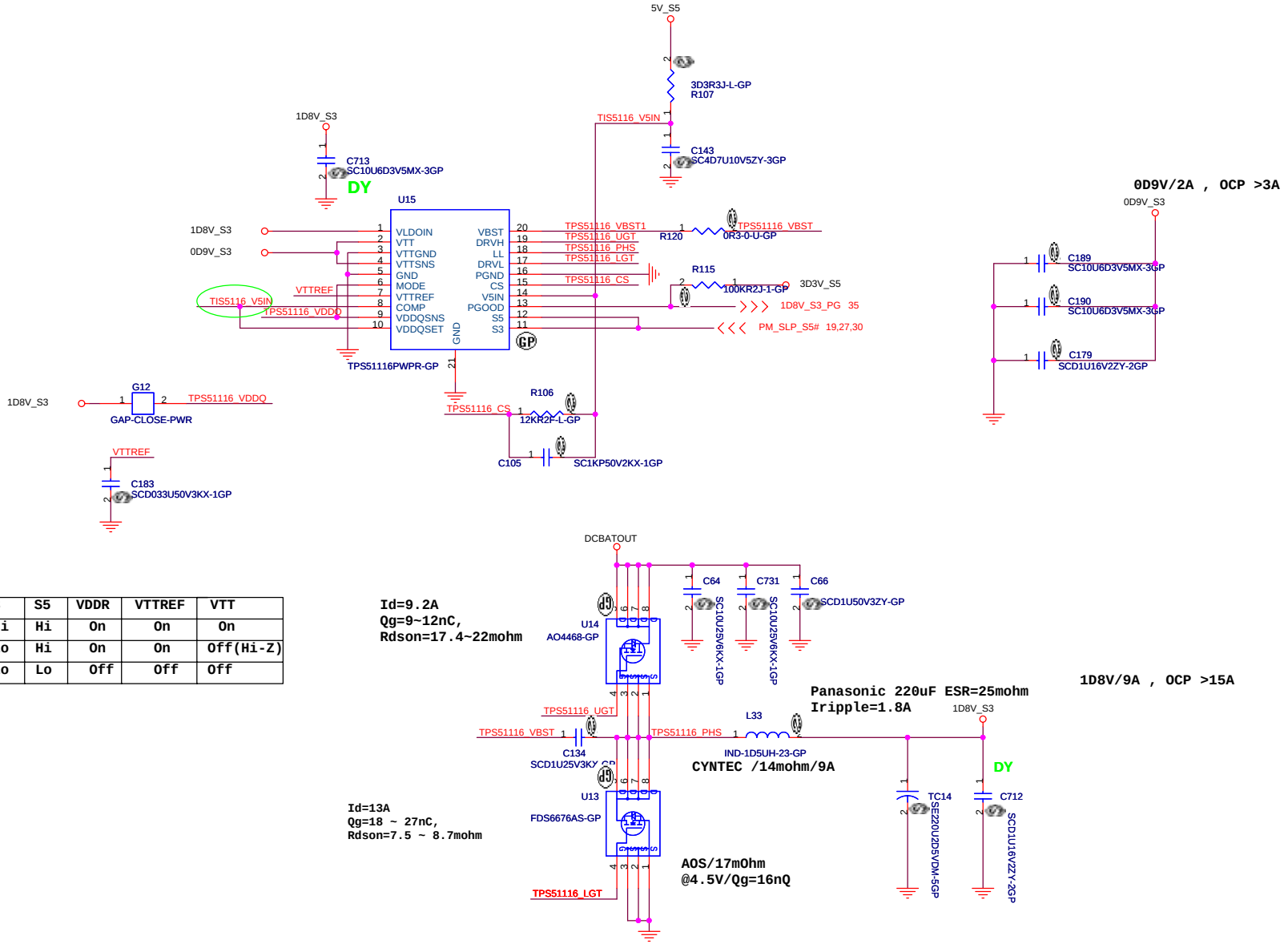
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI TPS51120 3D3V/5V

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 41 of 55

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

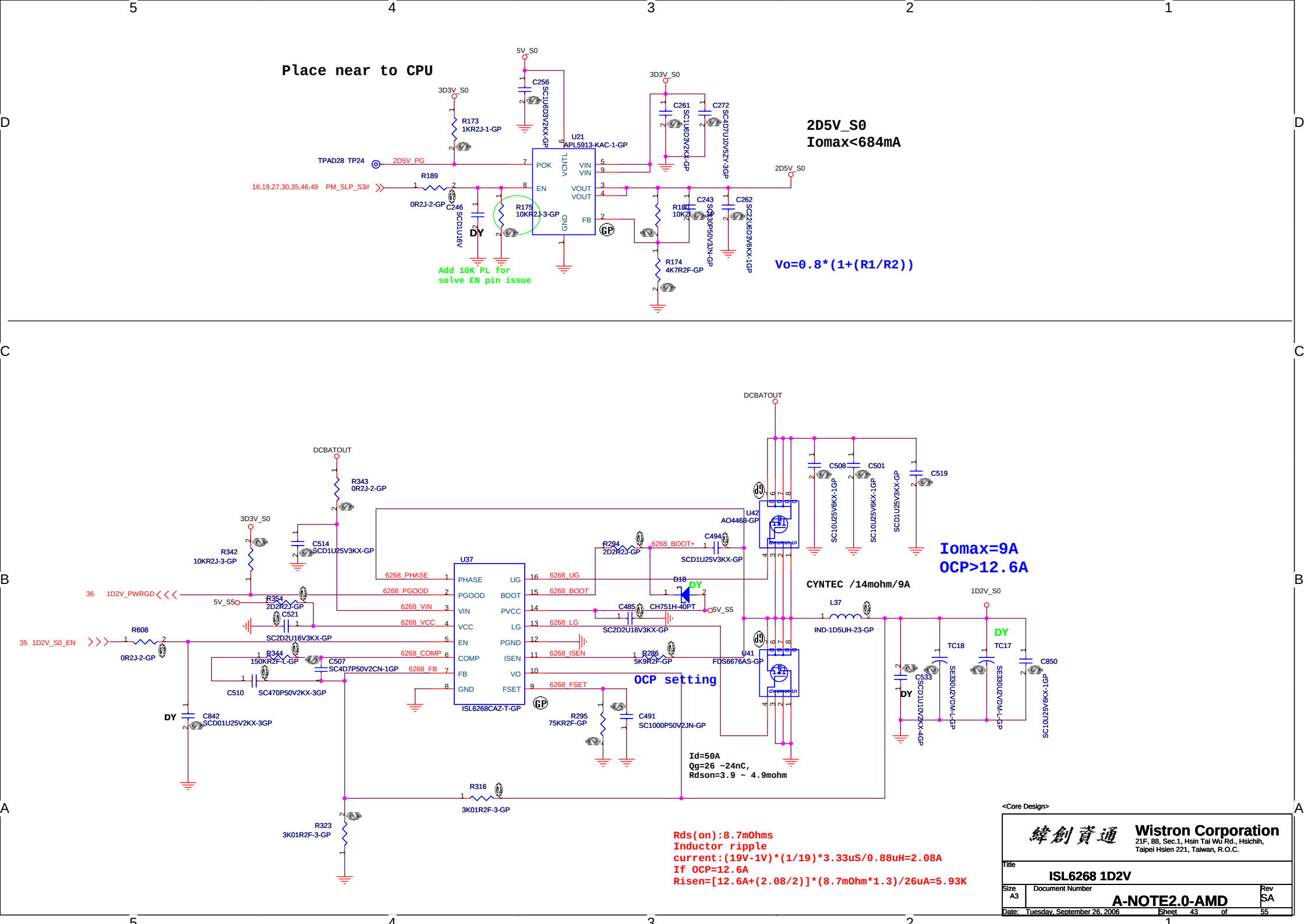
<Core Design>

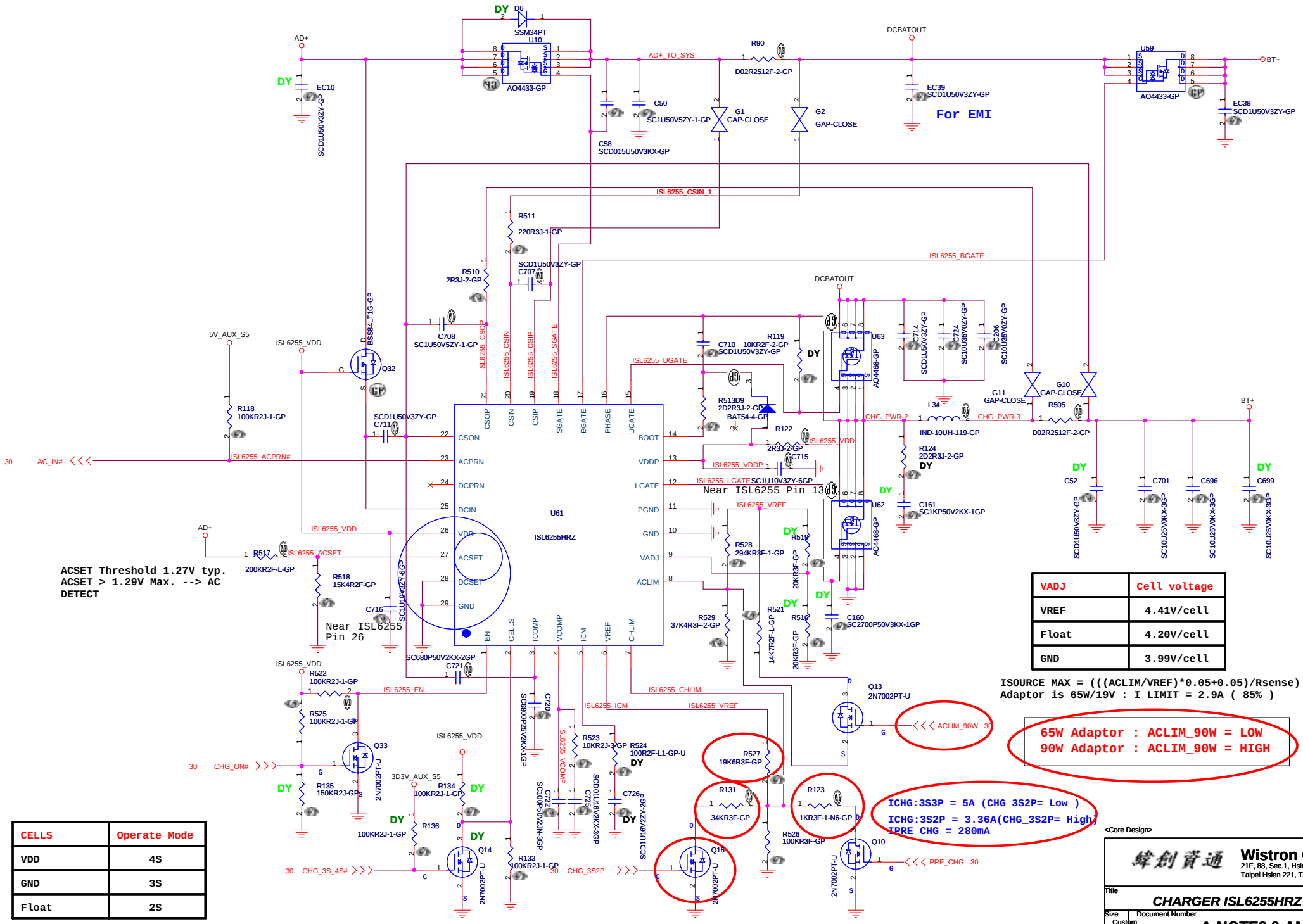
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI TPS51116 1D8V / 0D9V

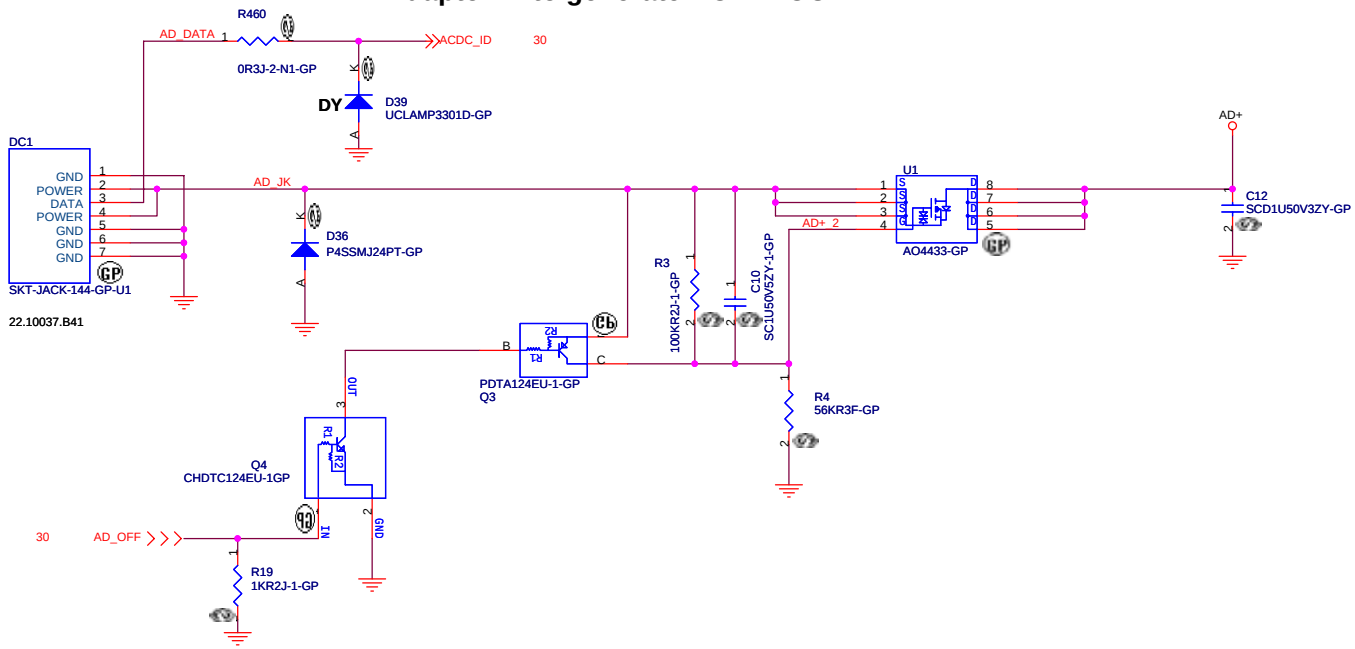
Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 42 of 55

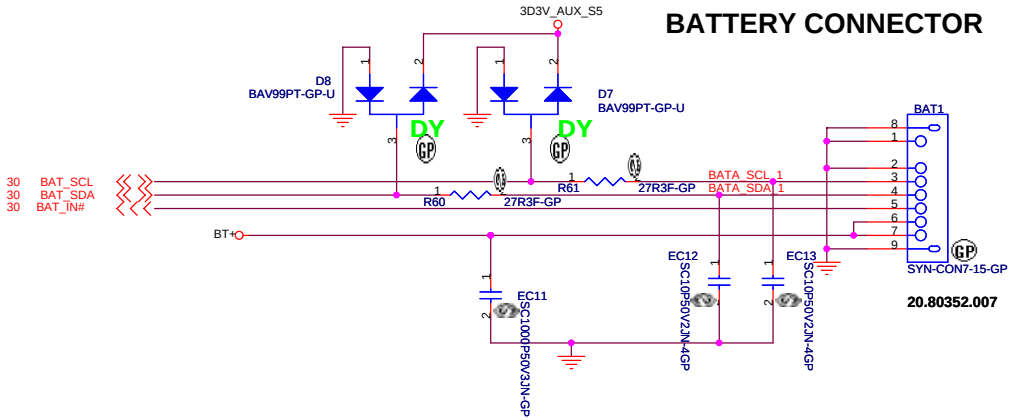

Place near to CPU
2D5V_S0
Iomax<684mA
Vo=0.8*(1+(R1/R2))
Add 10K PL for solve EN pin issue
Iomax=9A
OCP>12.6A
CYNTEC /14mohm/9A
OCP setting
Id=50A
Qg=26 ~24nC,
Rdson=3.9 ~ 4.9mohm
Rds(on):8.7mOhms
Inductor ripple current:(19V-1V)*(1/19)*3.33uS/0.88uH=2.08A
If OCP=12.6A
Risen=[12.6A+(2.08/2)]*(8.7mOhm*1.3)/26uA=5.93K
U21 APL5913-KAC-1-GP
U37 ISL6268CAZ-T-GP
U42 AO4468-GP
U41 FDS6676AS-GP
D18 CH751H-40PT
L37 IND-1D5UH-23-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ISL6268 1D2V
A-NOTE2.0-AMD
Tuesday, September 26, 2006
Sheet 43 of 55


ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC DETECT
Near ISL6255 Pin 26
Near ISL6255 Pin 13
ISL6255HRZ
U61
For EMI
DCBATOUT
AD+
BT+
5V_AUX_S5
3D3V_AUX_S5
ISL6255_VDD
ISL6255_ACSET
ISL6255_ACPRN#
ISL6255_EN
ISL6255_CHLIM
ISL6255_ICM
ISL6255_VREF
ISL6255_UGATE
ISL6255_BGATE
ISL6255_CSIN_1
ISL6255_VDDP
ISL6255_LGATE
CHG_PWR_2
CHG_PWR_3
AD+_TO_SYS
AC_IN#
CHG_ON#
CHG_3S_4S#
CHG_3S2P
ACLIM_90W
PRE_CHG
ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)
65W Adaptor : ACLIM_90W = LOW
90W Adaptor : ACLIM_90W = HIGH
ICHG:3S3P = 5A (CHG_3S2P= Low)
ICHG:3S2P = 3.36A(CHG_3S2P= High)
IPRE_CHG = 280mA
VADJ Cell voltage
VREF 4.41V/cell
Float 4.20V/cell
GND 3.99V/cell
CELLS Operate Mode
VDD 4S
GND 3S
Float 2S
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER ISL6255HRZ
A-NOTE2.0-AMD
Tuesday, September 26, 2006
Sheet 44 of 55

Adaptor in to generate DCBATOUT



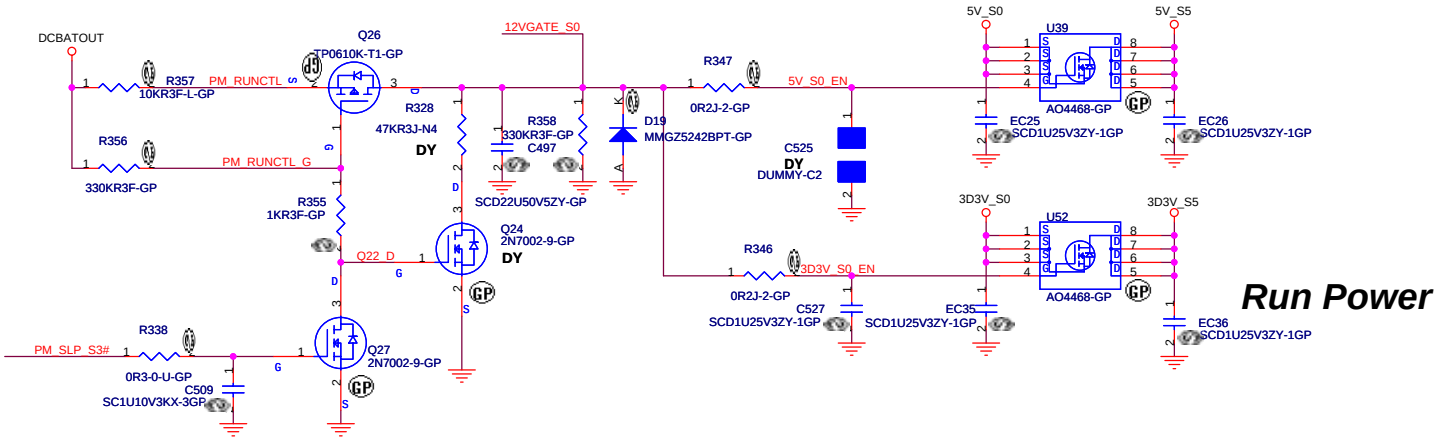
BATTERY CONNECTOR



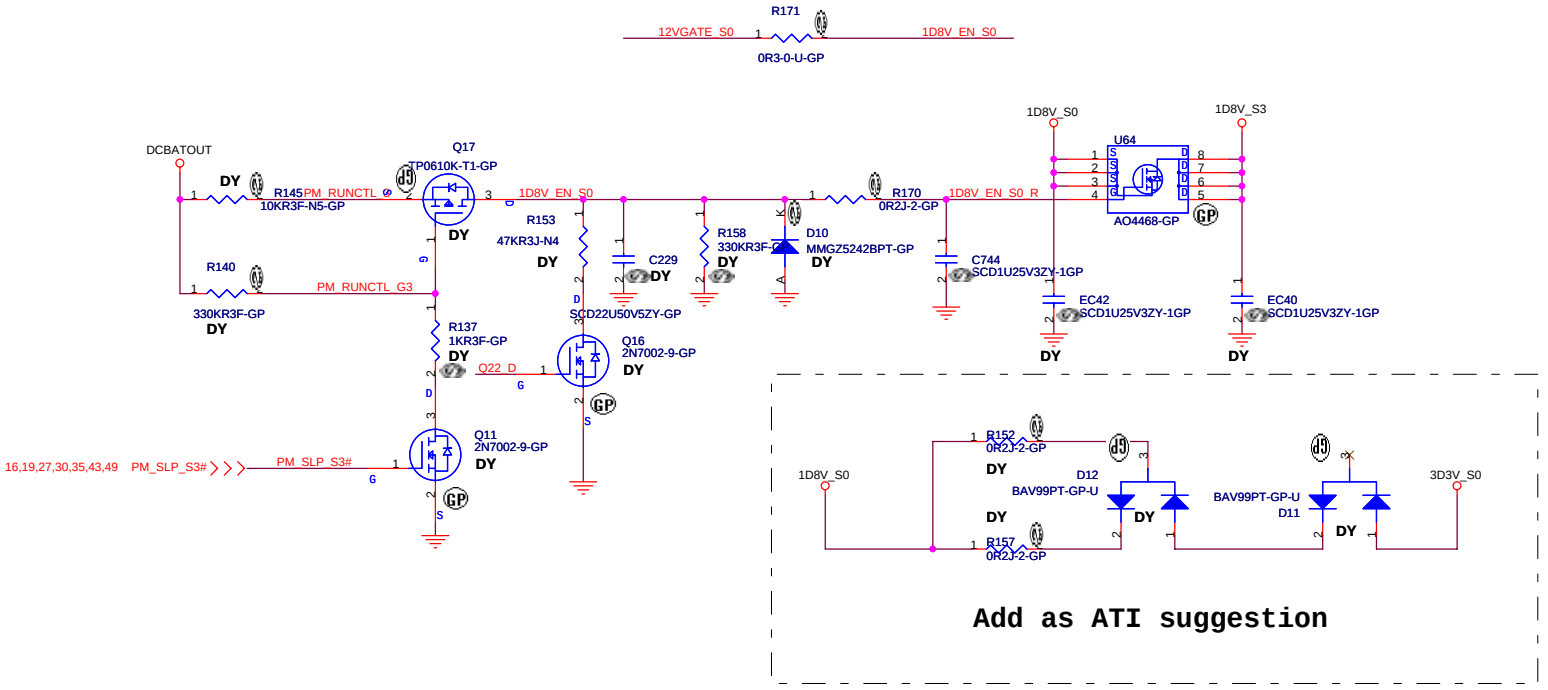
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BAT CONN***	
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 45 of 55	



Run Power



Add as ATI suggestion

Power On Logic

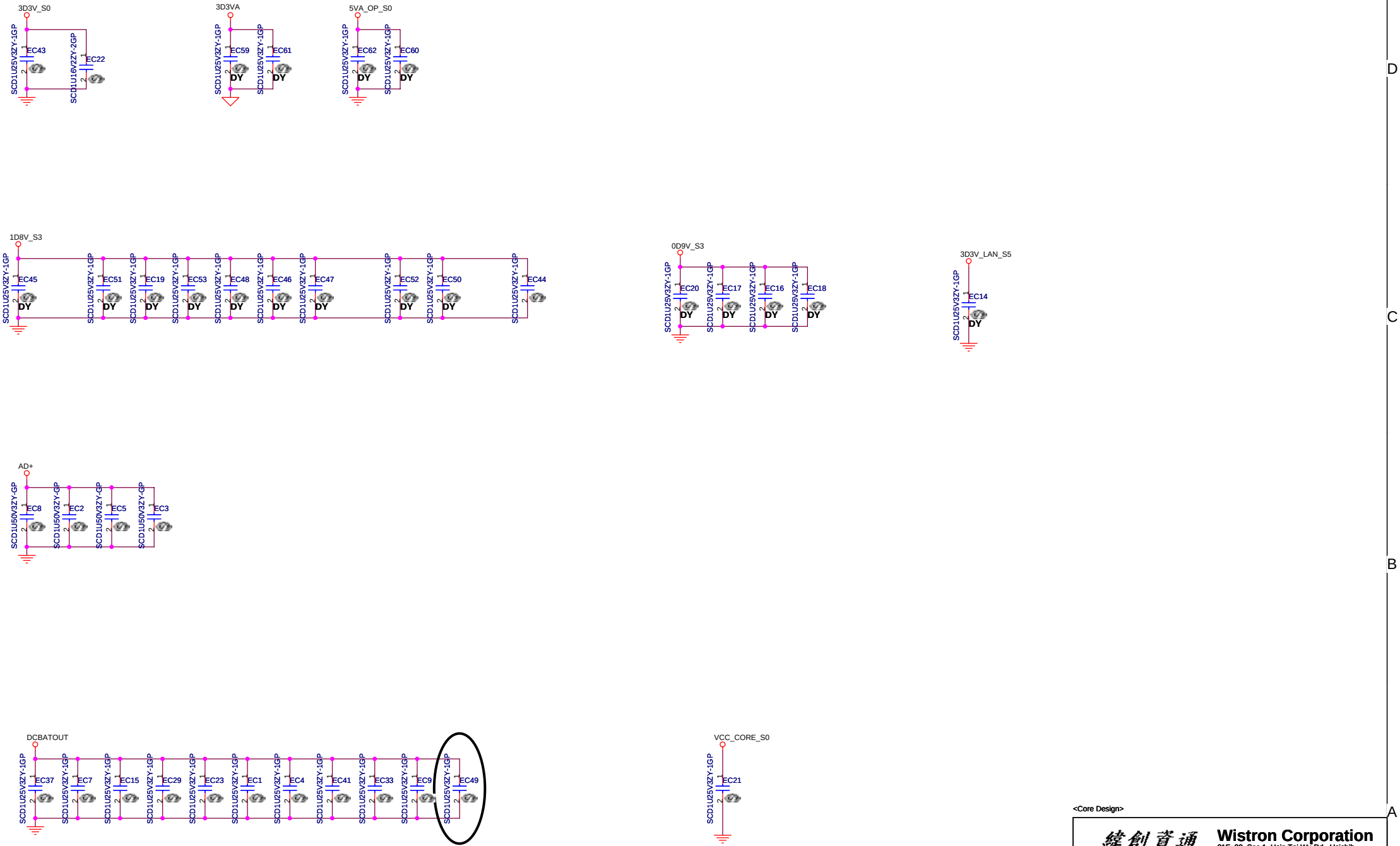
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWR CTL LOGIC / PWR PLANE

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 46 of 55



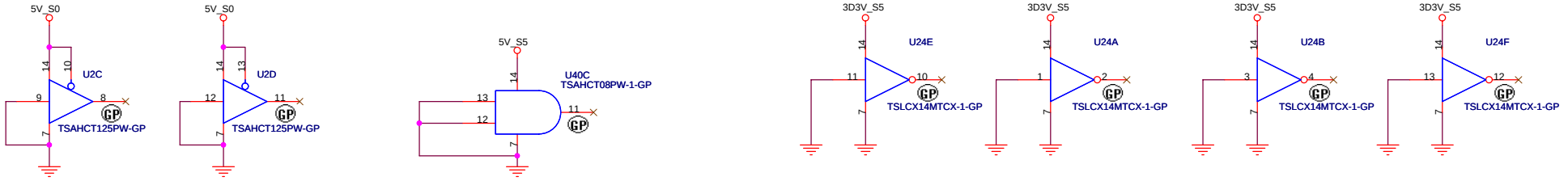
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai WU Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI COMPONENTS**

Size	Document Number	Rev
A3	A-NOTE2.0-AMD	SA

Date: Tuesday, September 26, 2006 Sheet 47 of 55



34.4T003.001 x 2

HOLE1 HTE8BE8R28-D-4
HOLE2 HOLE295X354R110-S

34.4T002.001 x 1

HOLE19 HOLET217B79R71

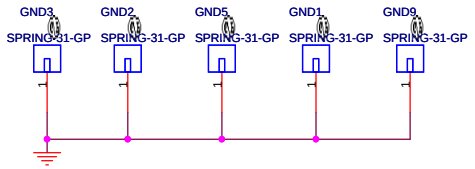
34.41Q08.011 x 3

HOLE4 HTE7BE7R28-D-33
HOLE3 HOLE315R110
HOLE5 HTE8BE8R28-D-65

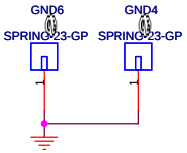
HOLE20 HOLET217B79R71
HOLE21 HOLE315R102
HOLE6 HOLE354X354R110-S1
HOLE23 HOLE315R102
HOLE24 HOLE315R102
HOLE16 HOLE354X315R110-S8

HOLE7 HOLE315R110
HOLE8 HTE8BE8R28-D-65
HOLE9 HTE8BE8R28-D-65
HOLE12 HT217X185B197R118-S
HOLE11 HTE6BE6R28-L-37
HOLE18 HOLE354X315R110-S9
HOLE14 HT205X217B197R118-S
HOLE22 HOLE

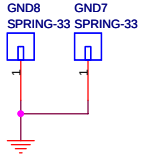
HOLE10 HTE8BE8R24-D-413
HOLE25 HOLE276R94
HOLE26 HOLE276R94
HOLE27 HOLE276R94
HOLE13 HT205X217B197R118-S
HOLE28 HOLE276R94
HOLE15 HT217X185B197R118-S
HOLE17 HOLE354X315R110-S10



34.49U24.001 x 5



34.39S07.001 x 2



34.4B312.001 x 2

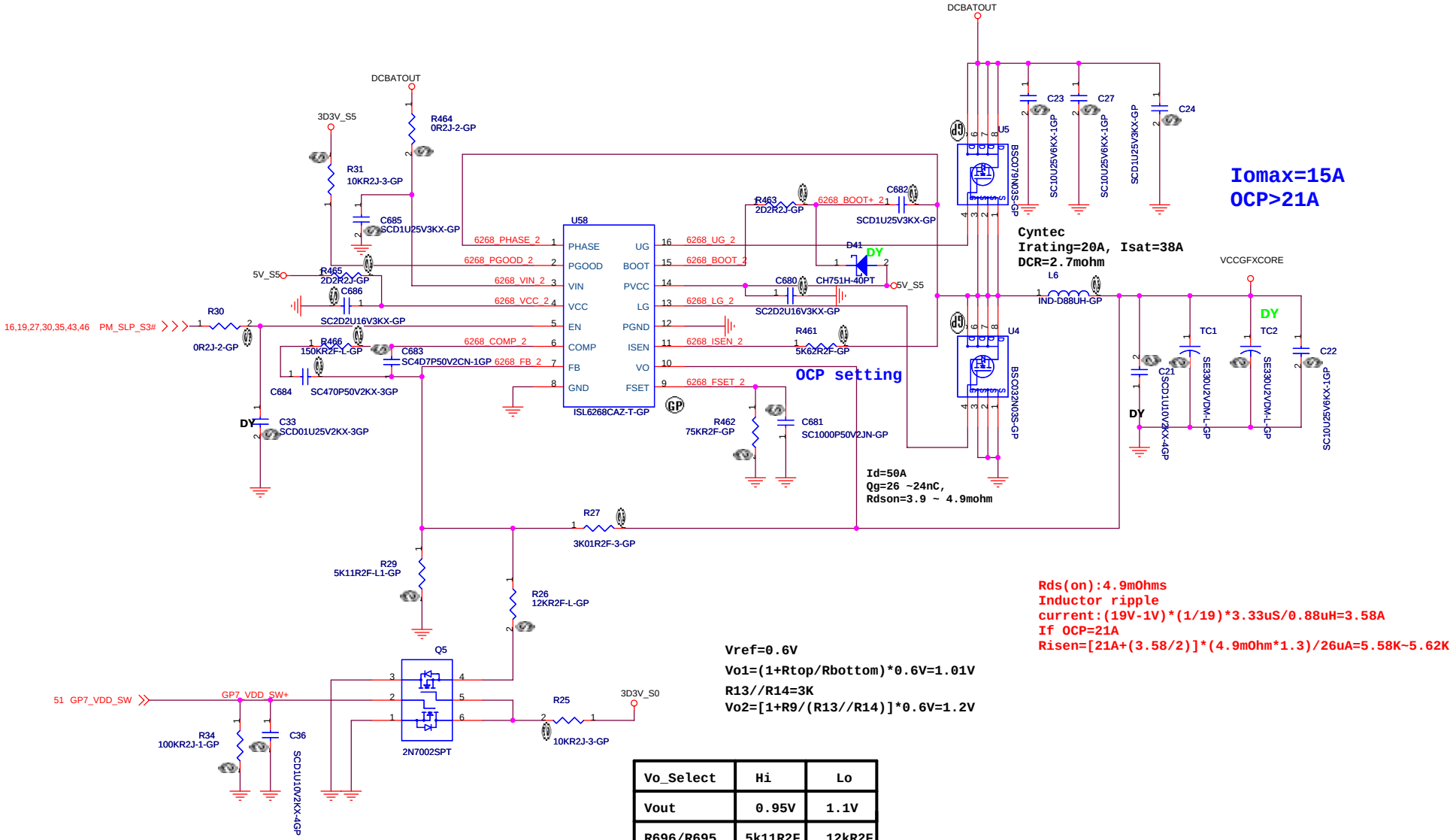
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MISC***

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 48 of 55



Vo_Select	Hi	Lo
Vout	0.95V	1.1V
R696/R695	5k11R2F	12kR2F

Vo_Select	Hi	Lo
Vout	0.95V	1.2V
R696/R695	5k11R2F	7k15R2F

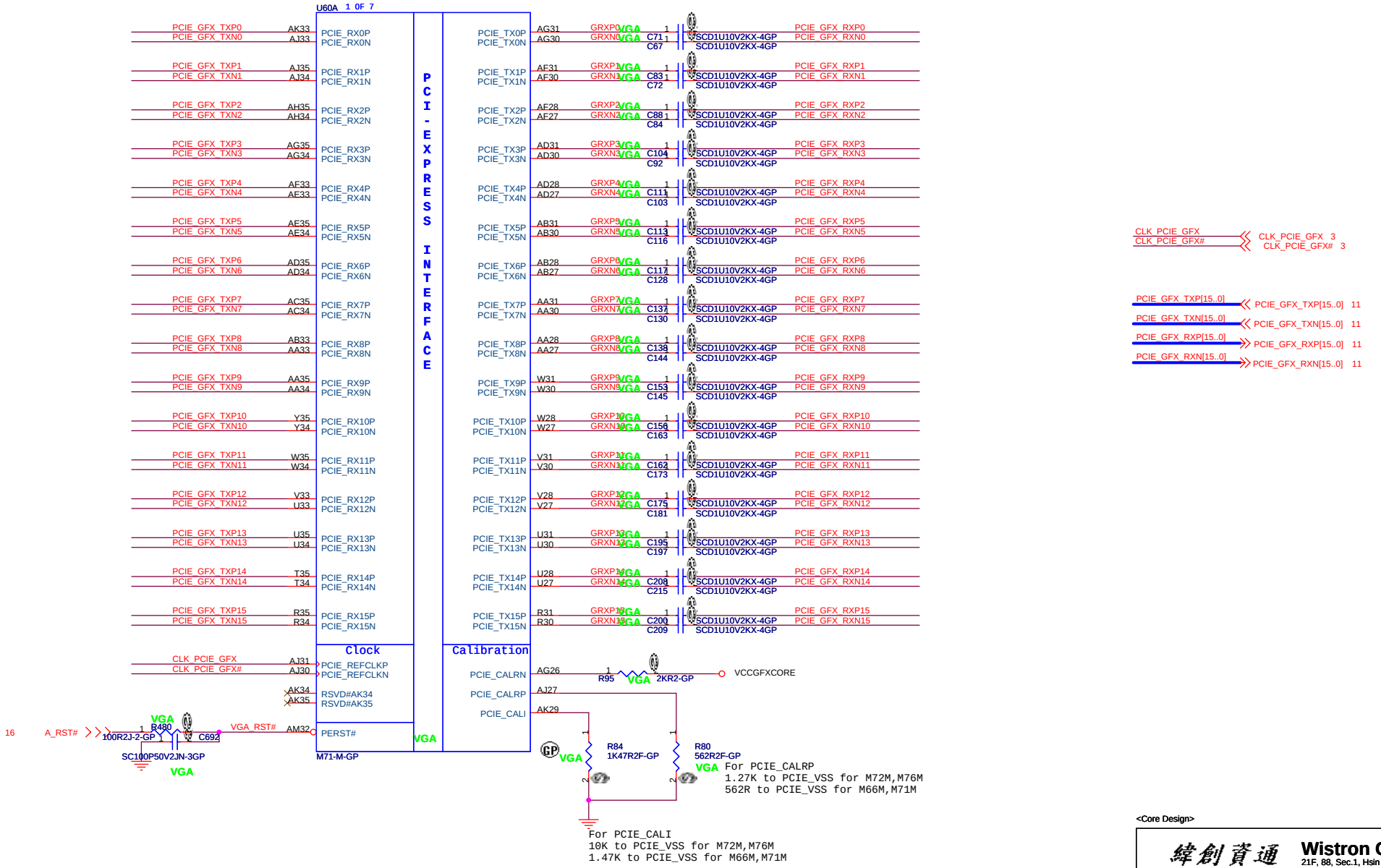
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: A3 | Document Number: A-NOTE2.0-AMD | Rev: SA

Date: Tuesday, September 26, 2006 | Sheet 49 of 55


U60A 1 OF 7
PCI-EXPRESS INTERFACE
PCIE_GFX_TXP0
PCIE_GFX_TXN0
PCIE_GFX_TXP1
PCIE_GFX_TXN1
PCIE_GFX_TXP2
PCIE_GFX_TXN2
PCIE_GFX_TXP3
PCIE_GFX_TXN3
PCIE_GFX_TXP4
PCIE_GFX_TXN4
PCIE_GFX_TXP5
PCIE_GFX_TXN5
PCIE_GFX_TXP6
PCIE_GFX_TXN6
PCIE_GFX_TXP7
PCIE_GFX_TXN7
PCIE_GFX_TXP8
PCIE_GFX_TXN8
PCIE_GFX_TXP9
PCIE_GFX_TXN9
PCIE_GFX_TXP10
PCIE_GFX_TXN10
PCIE_GFX_TXP11
PCIE_GFX_TXN11
PCIE_GFX_TXP12
PCIE_GFX_TXN12
PCIE_GFX_TXP13
PCIE_GFX_TXN13
PCIE_GFX_TXP14
PCIE_GFX_TXN14
PCIE_GFX_TXP15
PCIE_GFX_TXN15
AK33
AJ33
AJ35
AJ34
AH35
AH34
AG35
AG34
AF33
AE33
AE35
AE34
AD35
AD34
AC35
AC34
AB33
AA33
AA35
AA34
Y35
Y34
W35
W34
V33
U33
U35
U34
T35
T34
R35
R34
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
Clock
CLK_PCIE_GFX
CLK_PCIE_GFX#
AJ31
AJ30
PCIE_REFCLKP
PCIE_REFCLKN
AK34
AK35
RSVD#AK34
RSVD#AK35
PERST#
VGA_RST#
AM32
M71-M-GP
VGA
Calibration
PCIE_CALRN
PCIE_CALRP
PCIE_CALI
AG26
AJ27
AK29
R95
2KR2-GP
VCCGFXCORE
For PCIE_CALRP
1.27K to PCIE_VSS for M72M,M76M
562R to PCIE_VSS for M66M,M71M
R84
1K47R2F-GP
R80
562R2F-GP
For PCIE_CALI
10K to PCIE_VSS for M72M,M76M
1.47K to PCIE_VSS for M66M,M71M
16
A_RST#
R480
100R2J-2-GP
C692
SC100P50V2JN-3GP
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
AG31
AG30
AF31
AF30
AF28
AF27
AD31
AD30
AD28
AD27
AB31
AB30
AB28
AB27
AA31
AA30
AA28
AA27
W31
W30
W28
W27
V31
V30
V28
V27
U31
U30
U28
U27
R31
R30
GRXP0
GRXN0
GRXP1
GRXN1
GRXP2
GRXN2
GRXP3
GRXN3
GRXP4
GRXN4
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GRXN5
GRXP6
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GRXN15
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C116
C117
C128
C137
C130
C138
C144
C153
C145
C156
C163
C162
C173
C175
C181
C195
C197
C208
C215
C200
C209
SCD1U10V2KK-4GP
PCIE_GFX_RXP0
PCIE_GFX_RXN0
PCIE_GFX_RXP1
PCIE_GFX_RXN1
PCIE_GFX_RXP2
PCIE_GFX_RXN2
PCIE_GFX_RXP3
PCIE_GFX_RXN3
PCIE_GFX_RXP4
PCIE_GFX_RXN4
PCIE_GFX_RXP5
PCIE_GFX_RXN5
PCIE_GFX_RXP6
PCIE_GFX_RXN6
PCIE_GFX_RXP7
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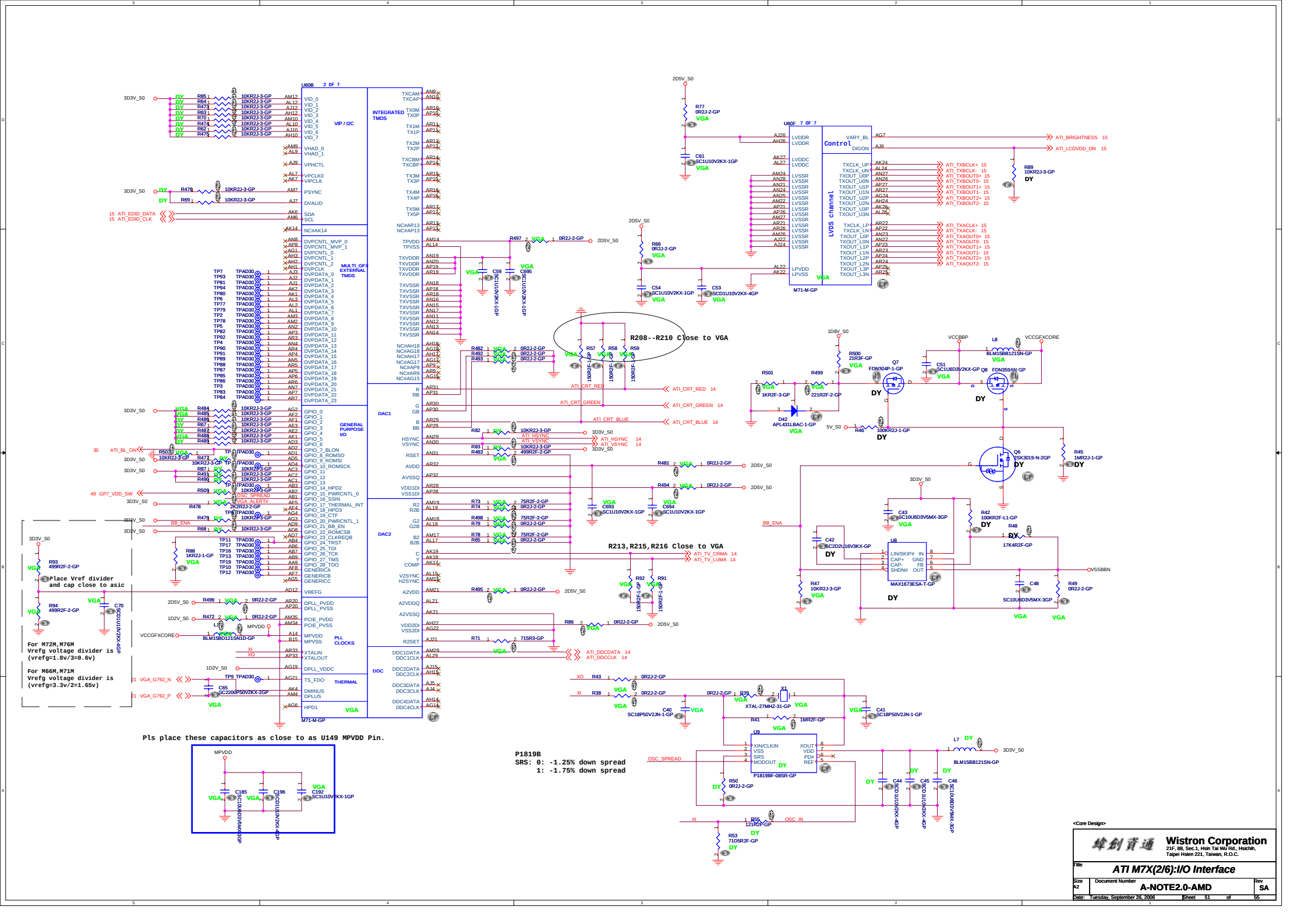
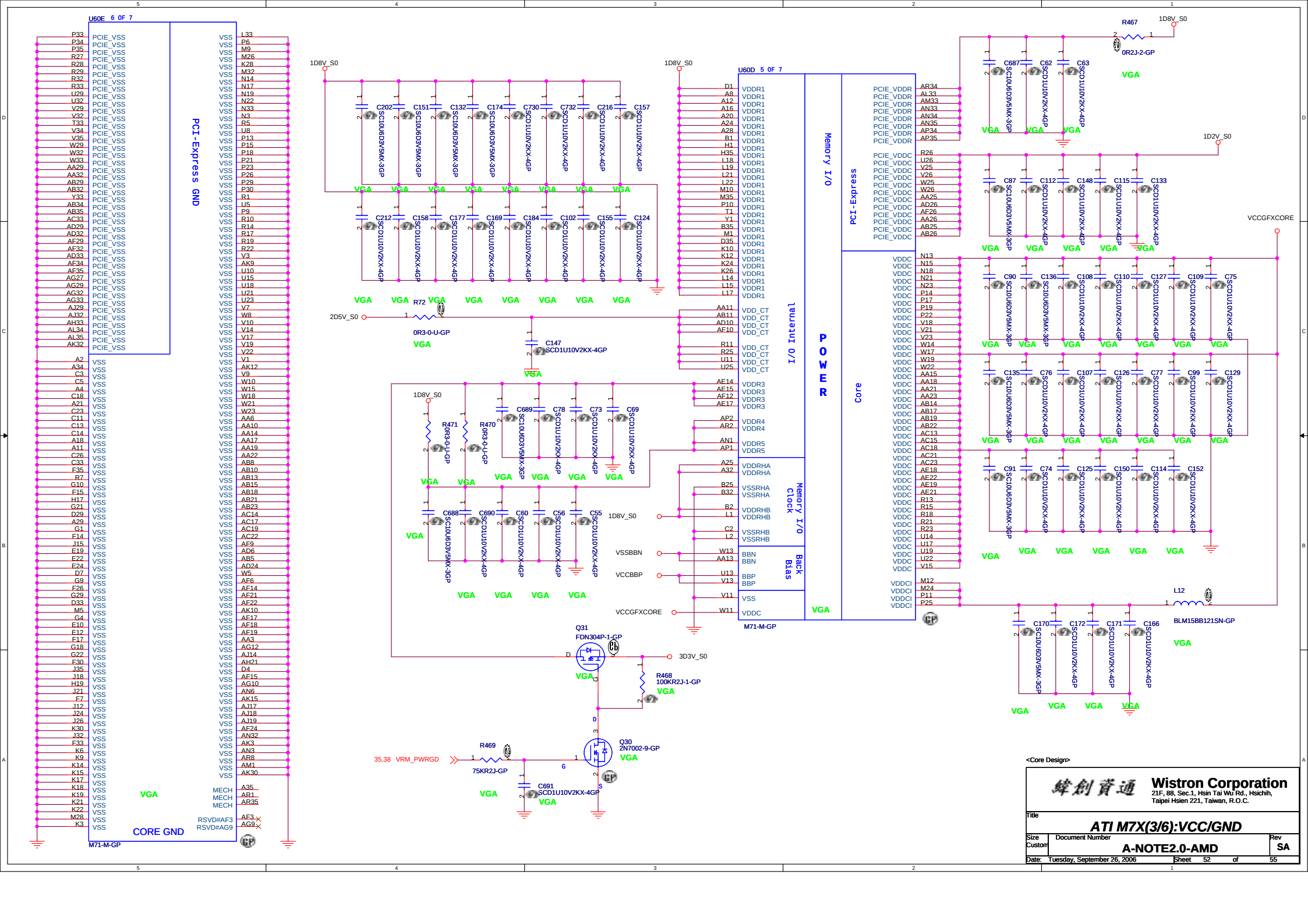
PCIE_GFX_RXP8
PCIE_GFX_RXN8
PCIE_GFX_RXP9
PCIE_GFX_RXN9
PCIE_GFX_RXP10
PCIE_GFX_RXN10
PCIE_GFX_RXP11
PCIE_GFX_RXN11
PCIE_GFX_RXP12
PCIE_GFX_RXN12
PCIE_GFX_RXP13
PCIE_GFX_RXN13
PCIE_GFX_RXP14
PCIE_GFX_RXN14
PCIE_GFX_RXP15
PCIE_GFX_RXN15
CLK_PCIE_GFX 3
CLK_PCIE_GFX# 3
PCIE_GFX_TXP[15..0] 11
PCIE_GFX_TXN[15..0] 11
PCIE_GFX_RXP[15..0] 11
PCIE_GFX_RXN[15..0] 11
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M7X(1/6):PCIE Interface
Size A3
Document Number A-NOTE2.0-AMD
Rev SA
Date: Tuesday, September 26, 2006
Sheet 50 of 55


U60B 2 0F 7
INTEGRATED TMDS
VIP / I2C
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
DAC1
DAC2
DDC
PLL CLOCKS
THERMAL
M71-M-GP
U60F 7 0F 7
Control
LVDS channel
M71-M-GP
R208--R210 Close to VGA
R213,R215,R216 Close to VGA
Pls place these capacitors as close to as U149 MPVDD Pin.
Place Vref divider and cap close to asic
For M72M,M76M
Vrefg voltage divider is
(vrefg=1.8v/3=0.6v)
For M66M,M71M
Vrefg voltage divider is
(vrefg=3.3v/2=1.65v)
P1819B
SRS: 0: -1.25% down spread
1: -1.75% down spread
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI M7X(2/6):I/O Interface
A-NOTE2.0-AMD
Size A2
Rev SA
Date: Tuesday, September 26, 2006
Sheet 51 of 55


U60E 6 OF 7
PCIE_VSS
PCI-Express GND
VSS
CORE GND
MECH
RSVD#AF3
RSVD#AG9
M71-M-GP
U60D 5 OF 7
VDDR1
VDD_CT
VDDR3
VDDR4
VDDR5
VDDRHA
VSSRHA
VDDRHB
VSSRHB
BBN
BBP
VDDC
VDDCI
I/O Internal
Memory I/O
Memory I/O Clock
Back Bias
PCI-Express
Core
POWER
M71-M-GP
1D8V_S0
1D2V_S0
2D5V_S0
3D3V_S0
VCCGFXCORE
VSSBBN
VCCBBP
VRM_PWRGD
35,38
R72
0R3-0-U-GP
R467
0R2J-2-GP
R471
R470
R468
100KR2J-1-GP
R469
75KR2J-GP
L12
BLM15BB121SN-GP
Q31
FDN304P-1-GP
Q30
2N7002-9-GP
VGA
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M7X(3/6):VCC/GND
Size
Custom
Document Number
A-NOTE2.0-AMD
Rev
SA
Date: Tuesday, September 26, 2006
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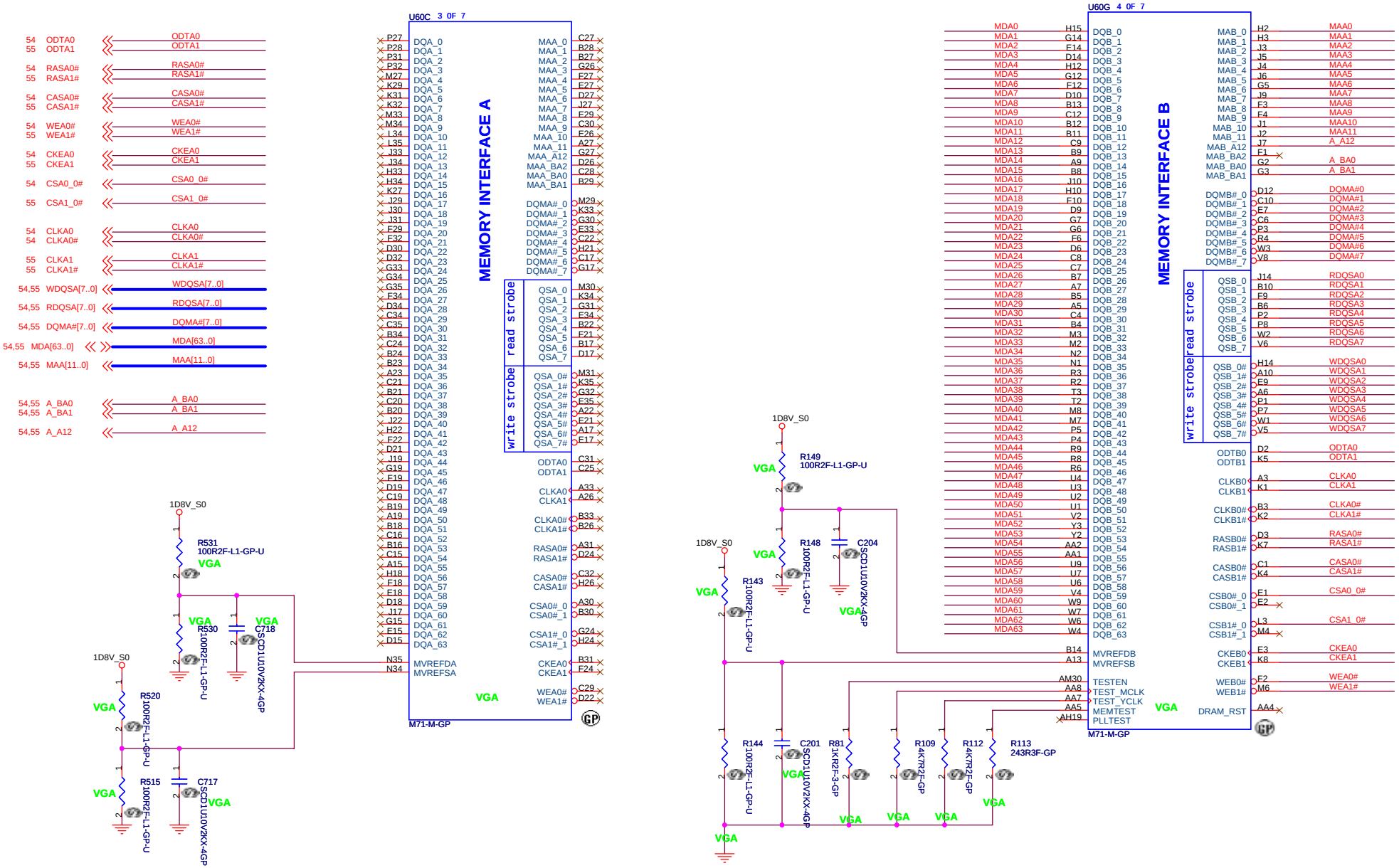

<Core Design>

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Title: **ATI M7X(4/6):Memory Interface**

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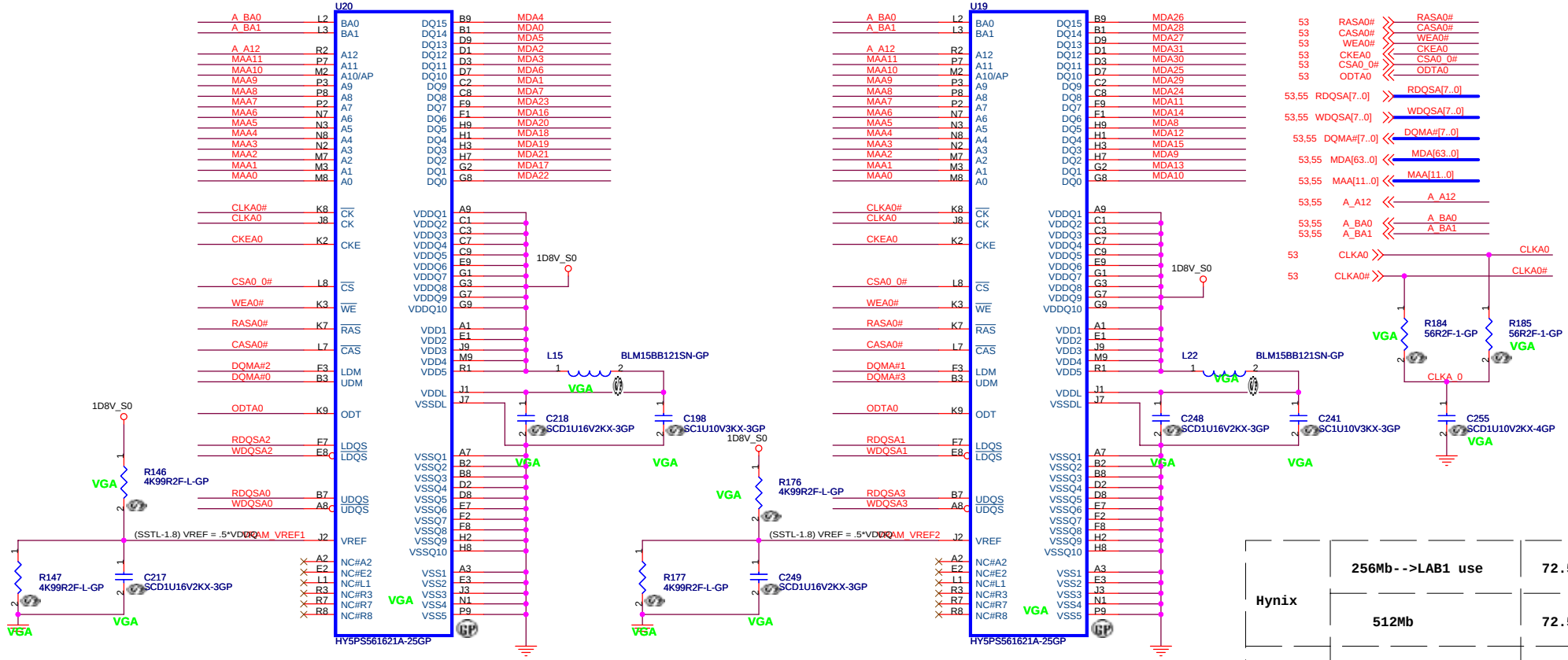
DDR2 BGA MEMORY



Hynix	256Mb-->LAB1 use	72.55616.C0U
	512Mb	72.51216.D0U
Second Source Qimonda	256Mb-->LAB1 use	72.18256.B0U
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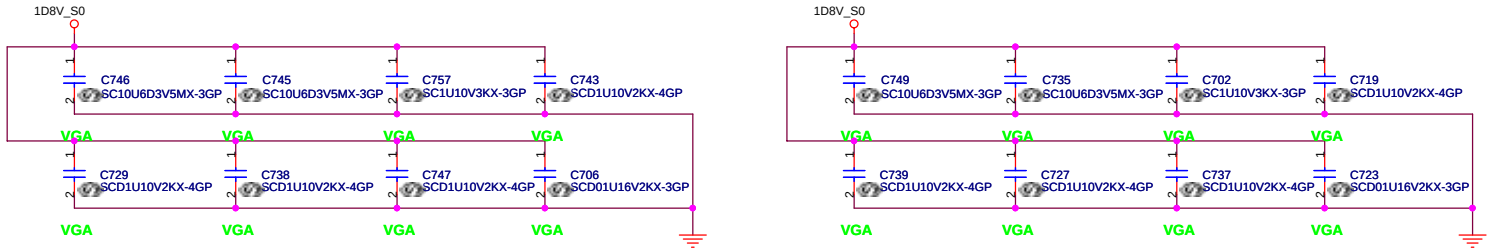

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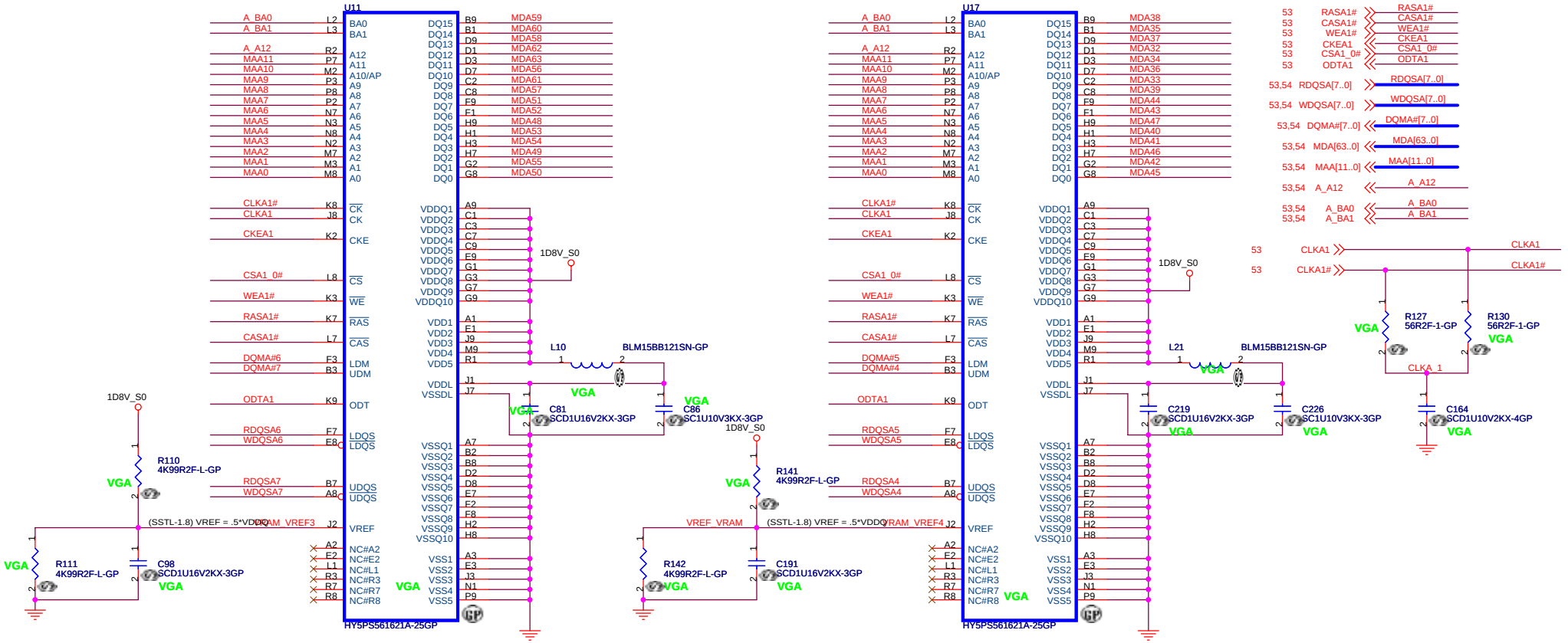
DDR2 BGA MEMORY



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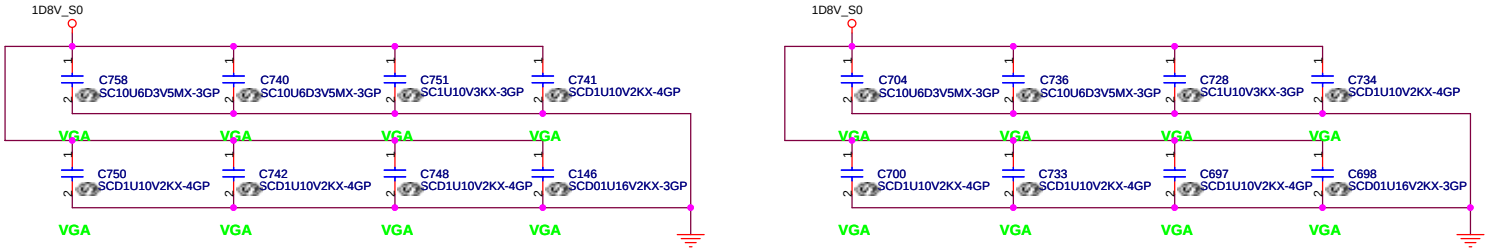

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Title	***VRAM***	
Size: A3	Document Number: **A-NOTE2.0-AMD**	Rev: SA
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