

## Schematics Page Index (Title / Revision / Change Date)

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40	ICH7-M( POWER) 4/5	1.1	2006/08/10	80		1.1	2006/08/10

P. Leader	Check by	Design by

Project Code &amp; Schematics Subject: MS21 MP Main Board

(TYPE 2)

PCB P/N: 1P-0068100-8011 (FUBAI)  
1P-0068500-8011 (Hannstar)

FOXCONN

HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

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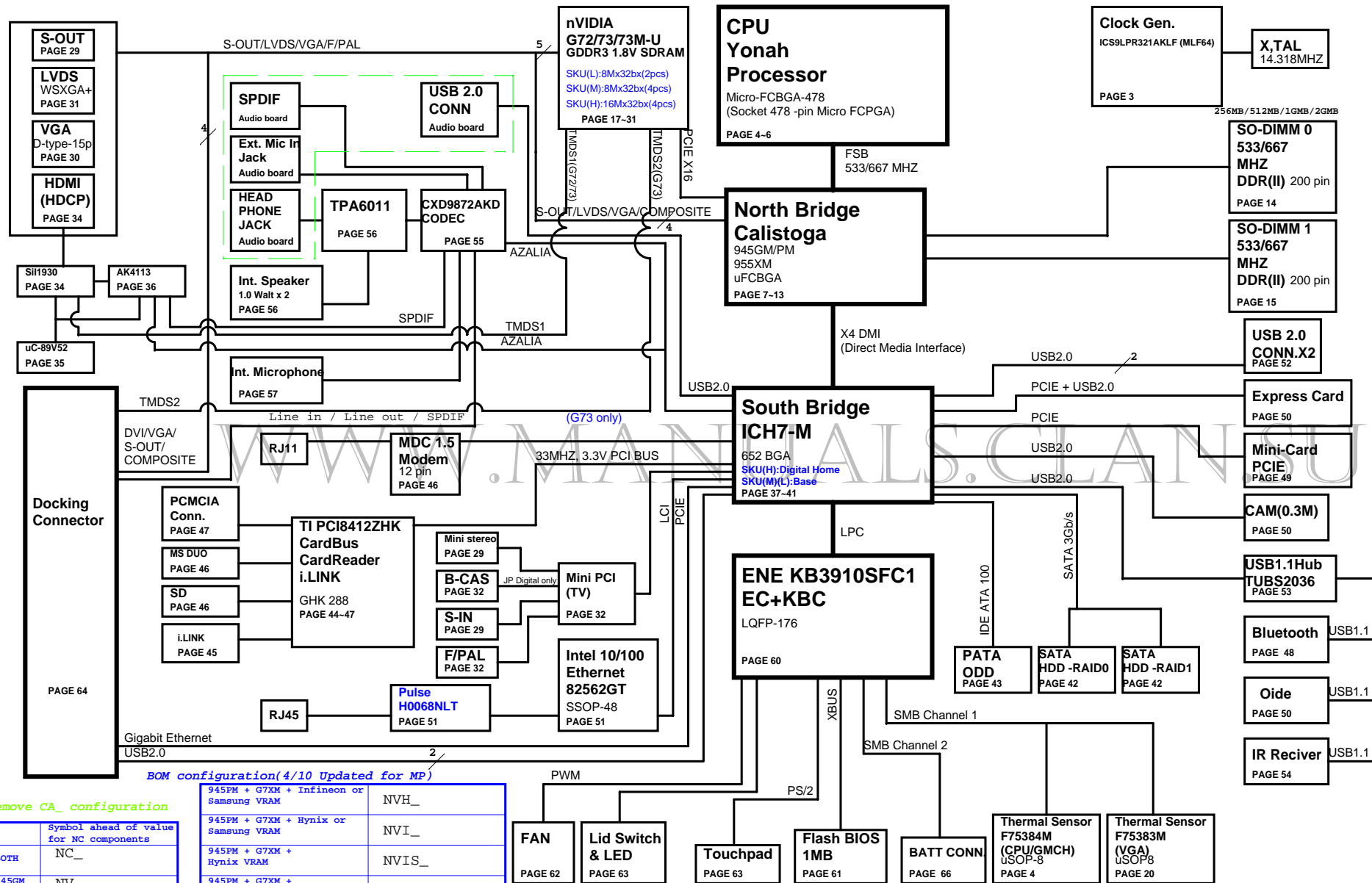
Size A3	Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2	Rev 1.1
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# MS21(CALISTOGA PM+Gfx Block Diagram)

Red texts:  
New modified



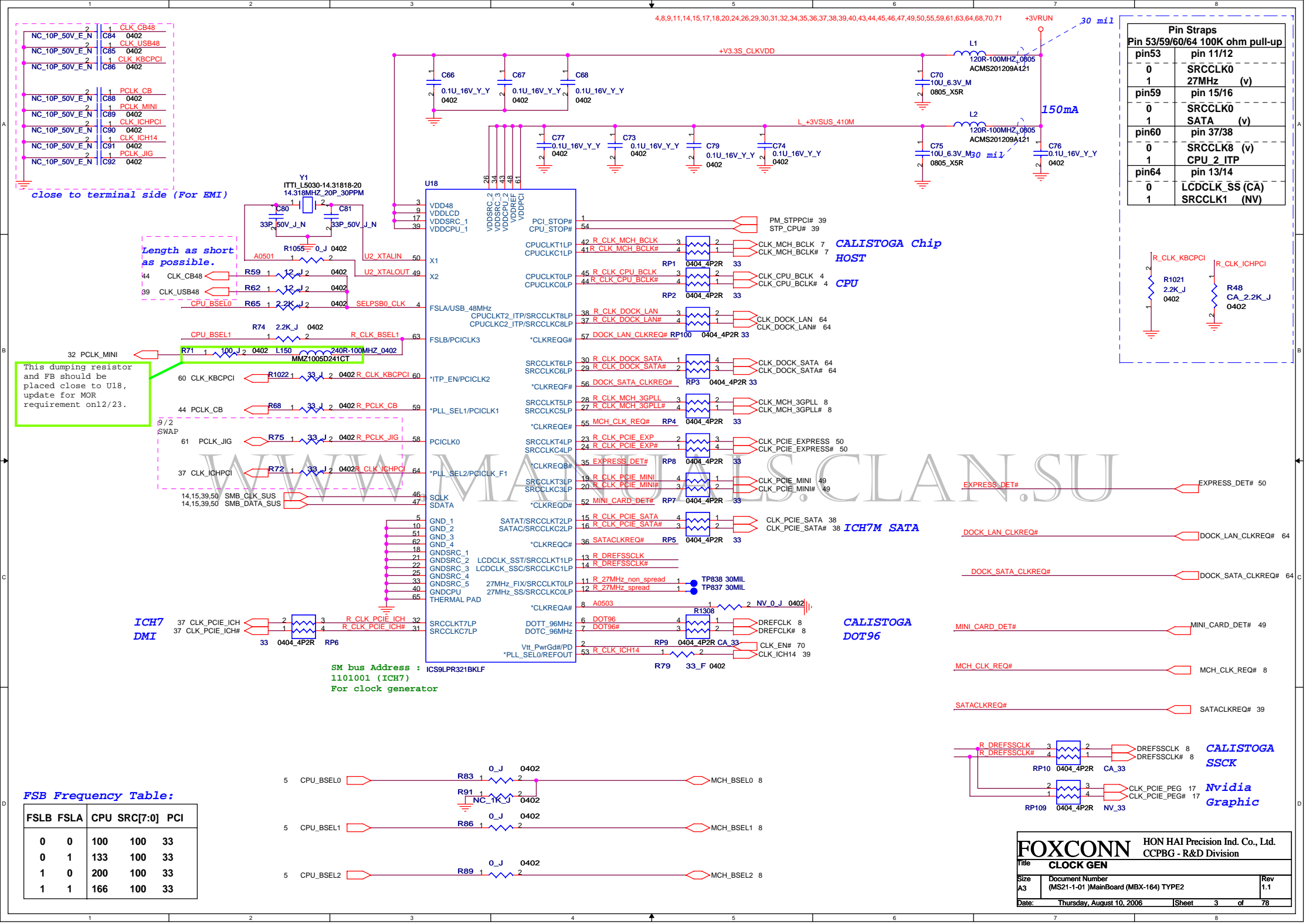
BOM configuration(4/10 Updated for MP)

Remove CA configuration

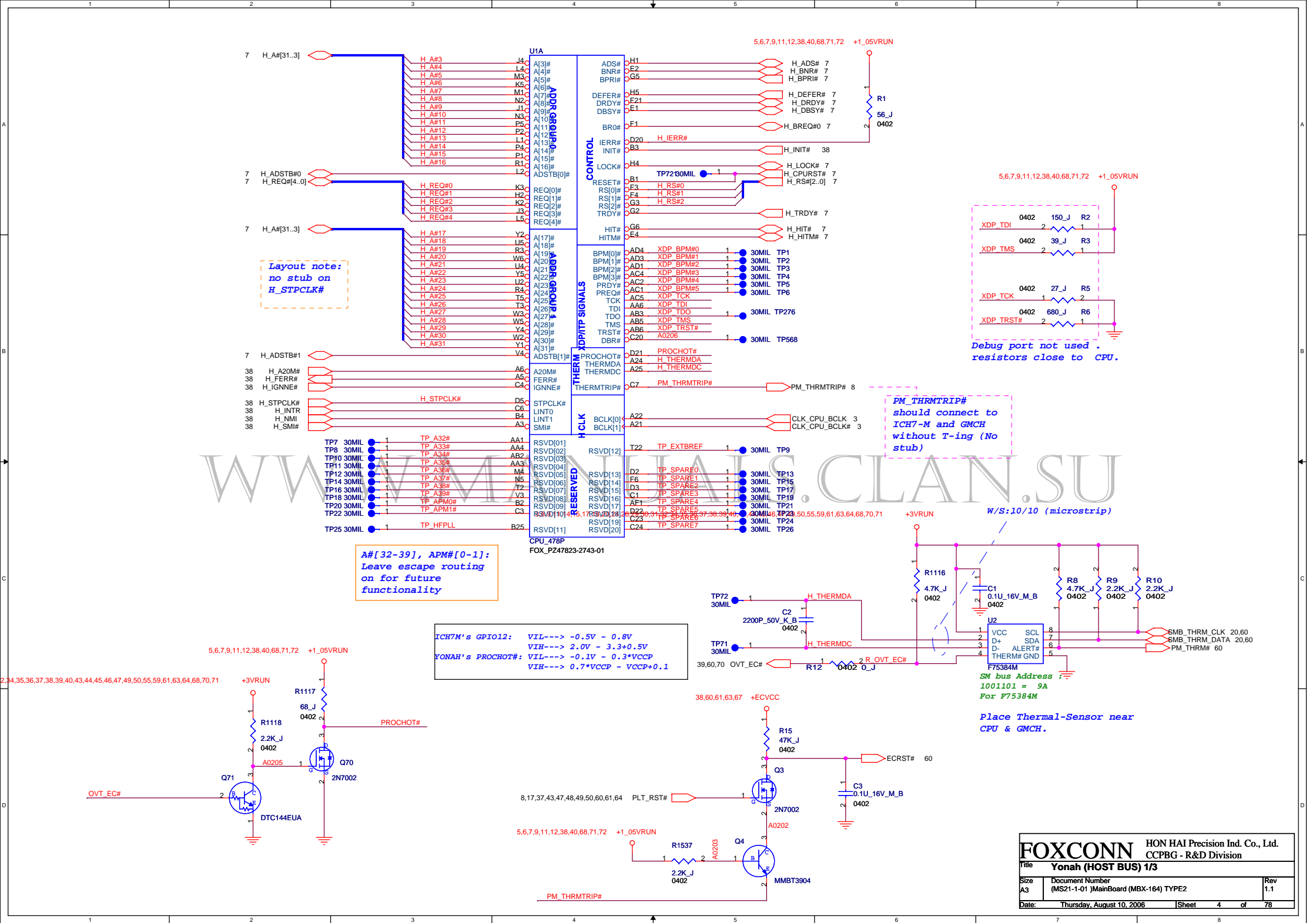
Symbol	ahead of value for NC components
BOTH	NC_
945GM	NV_
945PM + G72M	NV73_
945PM + G73M	NV72_
945PM + G72M or G73M-U	NV73Only_

945PM + G7XM + Infineon or Samsung VRAM	NVH_
945PM + G7XM + Hynix or Samsung VRAM	NVI_
945PM + G7XM + Hynix VRAM	NVIS_
945PM + G7XM + Infineon VRAM	NVHS_
945PM + G72M or G73M	NV16M_, NV73U_
945PM + G73M-U	NV8M_, NV7273_
*JP Digital TV Tuner SKU & No Tuner SKU not stick	JDTVNC_





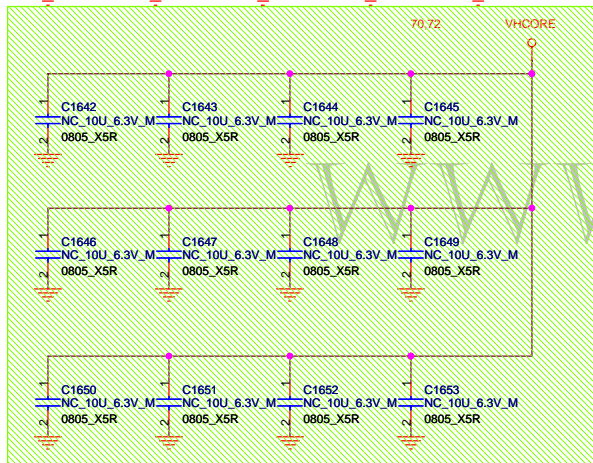
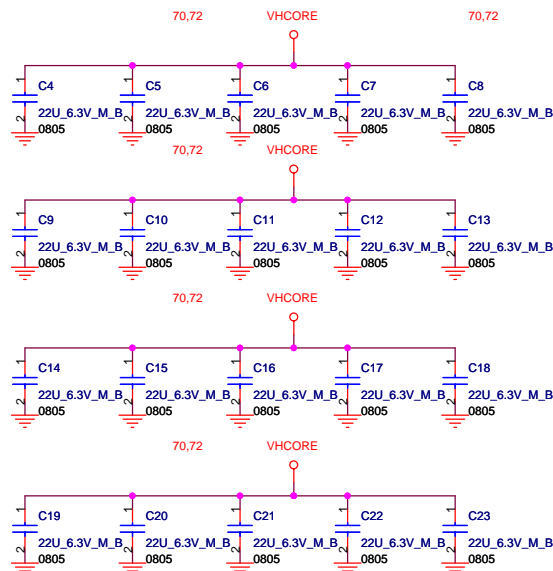




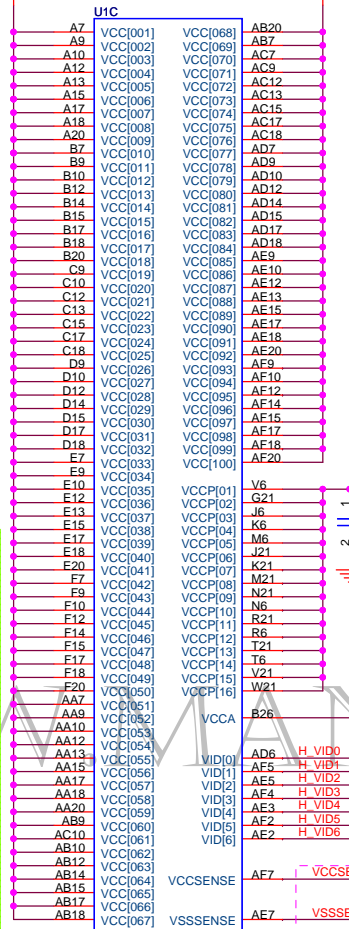
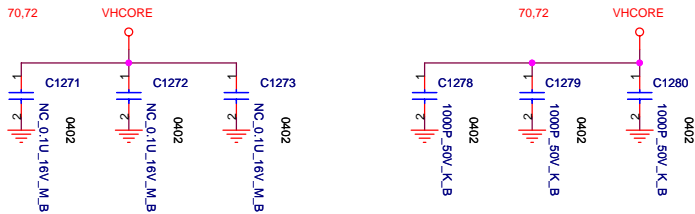






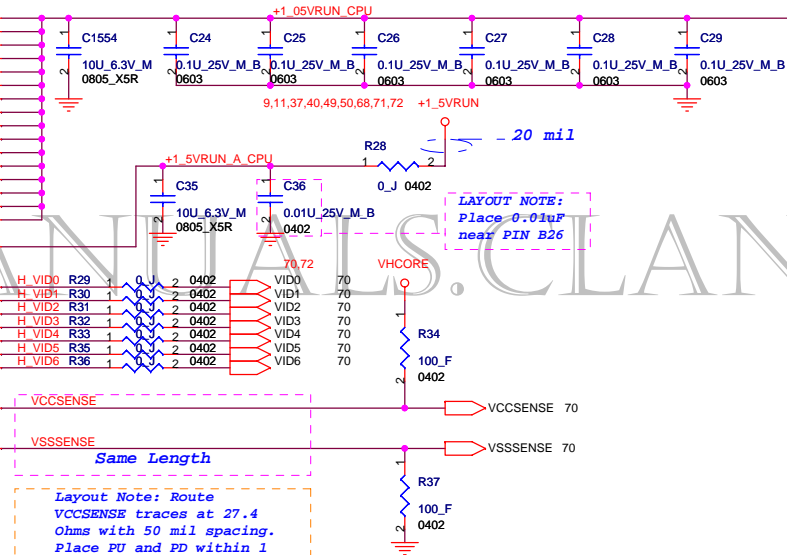


Backup 10uF capacitors for 22uF shortage.



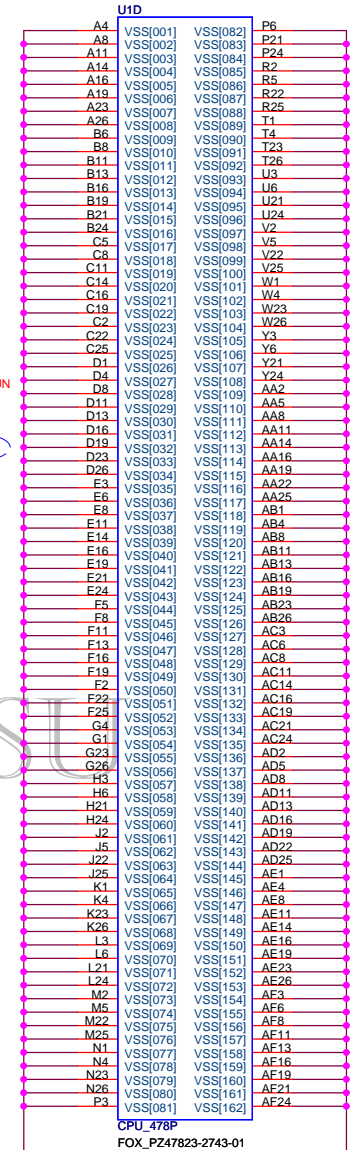
CPU\_478P  
FOX\_P247823-2743-01

CPU\_VCCA----->120mA  
CPU\_VCCP----->2.5A  
CPU\_VCC----->44A



Layout Note: Route  
VCCSENSE traces at 27.4  
Ohms with 50 mil spacing.  
Place PU and PD within 1  
inch of cpu.

width=18 mil  
spacing=7 mil

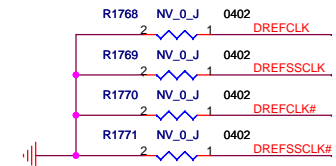


CPU\_478P  
FOX\_P247823-2743-01





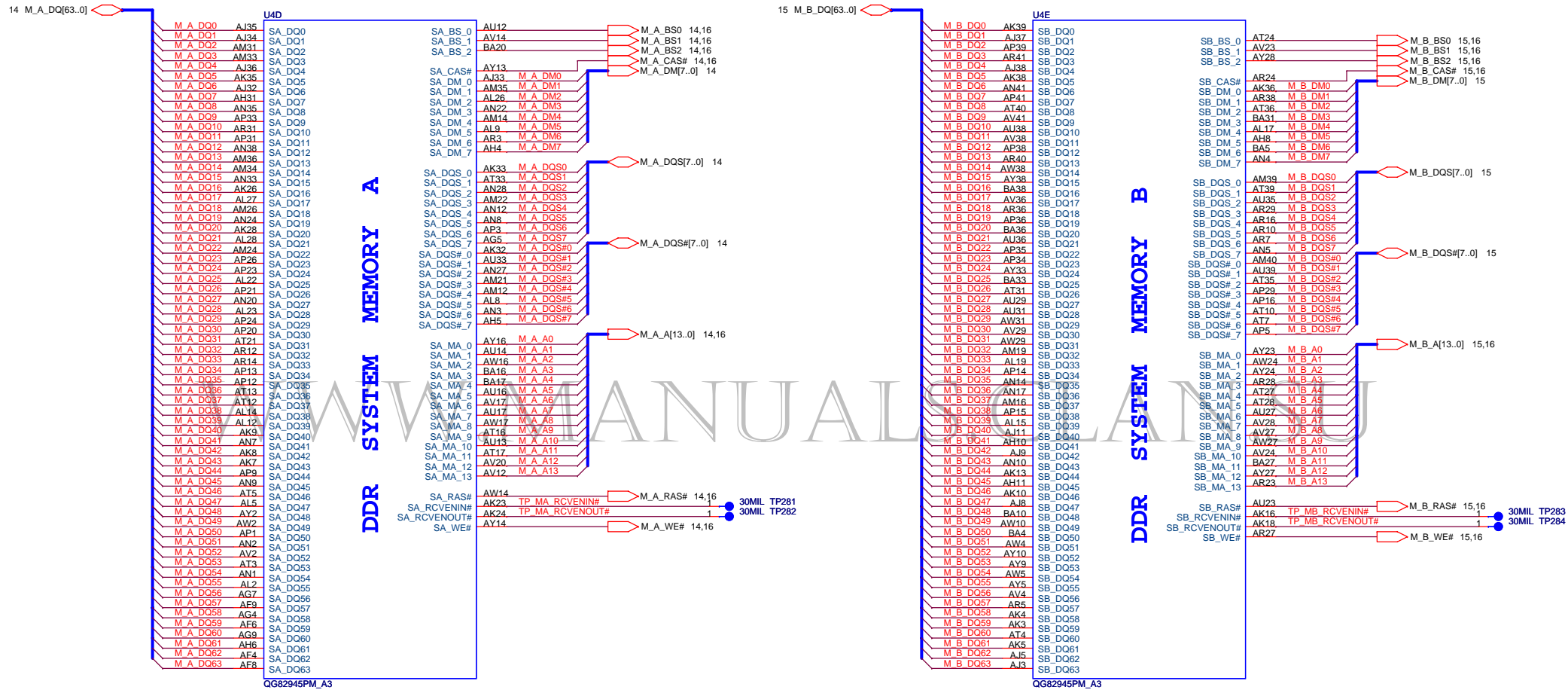




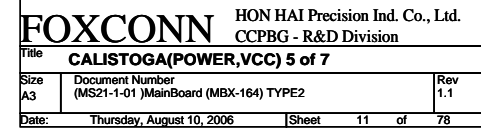




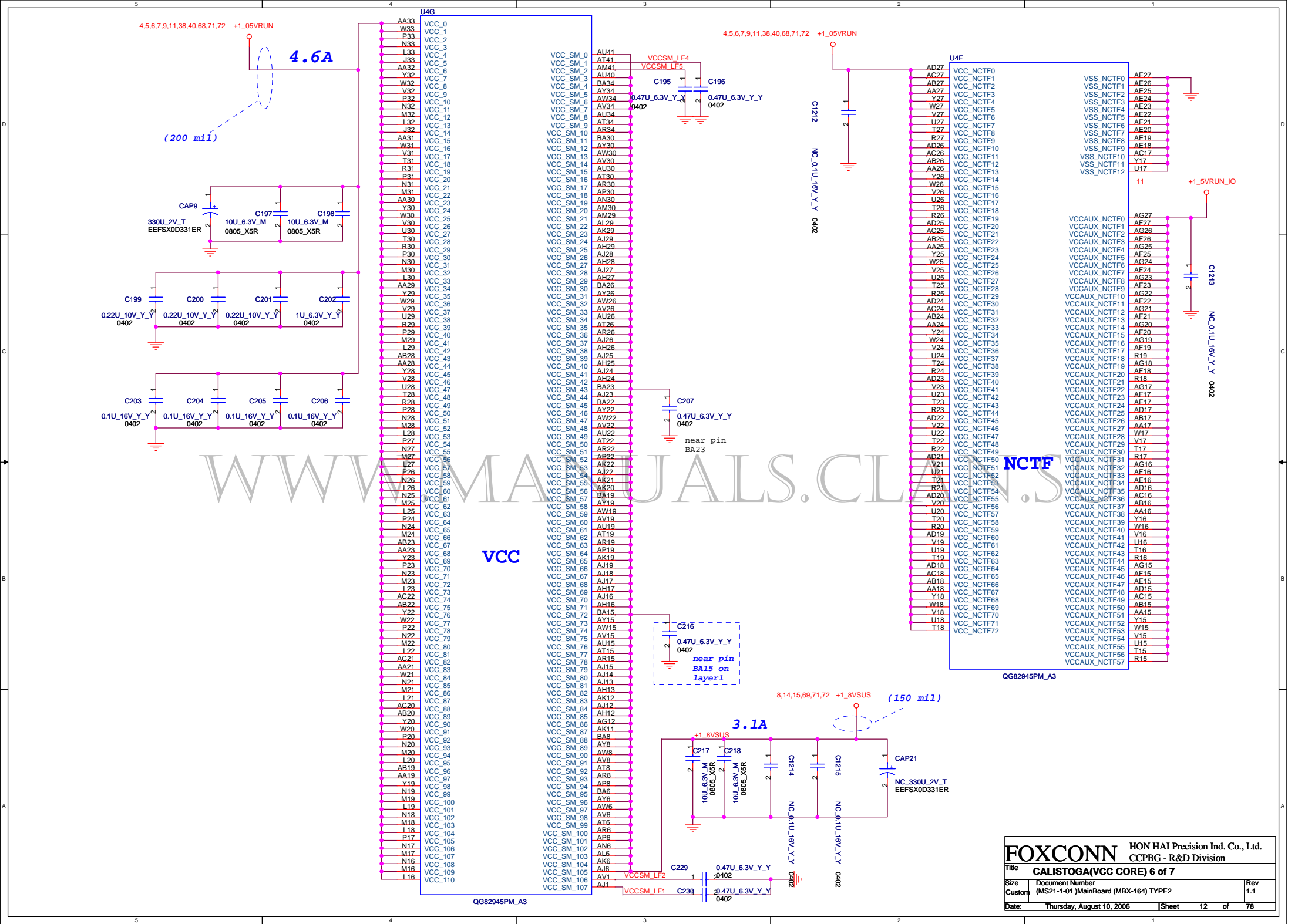














8 MCH\_CFG\_5 1 30MIL TP554

MCH\_CFG\_5 Low = DMIX2 High = DMIX4

8 MCH\_CFG\_6 1 30MIL TP556

MCH\_CFG\_6 Low = Moby Dick High = Calistoga DDR2 select (default high)

8 TP\_MCH\_CFG\_7 TP\_MCH\_CFG\_7

MCH\_CFG\_7 (CPU Strap) Low = RSVD High = Mobile Yonah processor

8 MCH\_CFG\_9 1 30MIL TP559

MCH\_CFG\_9 (PCIe Graphics Lane) Low = Reverse Lane High = Normal operation For layout convenience

8 MCH\_CFG\_10 1 30MIL TP560

MCH\_CFG\_10 (HOST PLL VCC SELECT) Low = RESERVED High = MOBILITY

8 MCH\_CFG\_11 1 R162 NC 2.2K $\Omega$  0402

MCH\_CFG\_11 (PSB 4x CLK ENABLE) Low = Calistoga High = Reserved

8 MCH\_CFG\_12 1 30MIL TP562

8 MCH\_CFG\_13 1 30MIL TP563

MCH\_CFG\_13:12 00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

8 MCH\_CFG\_16 1 30MIL TP564

MCH\_CFG\_16 (FSB Dynamic ODT) Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH\_CFG\_18 Low = 1.05V(default) High = 1.5V (VCC\_CORE Select)

8 MCH\_CFG\_18 1 30MIL TP555

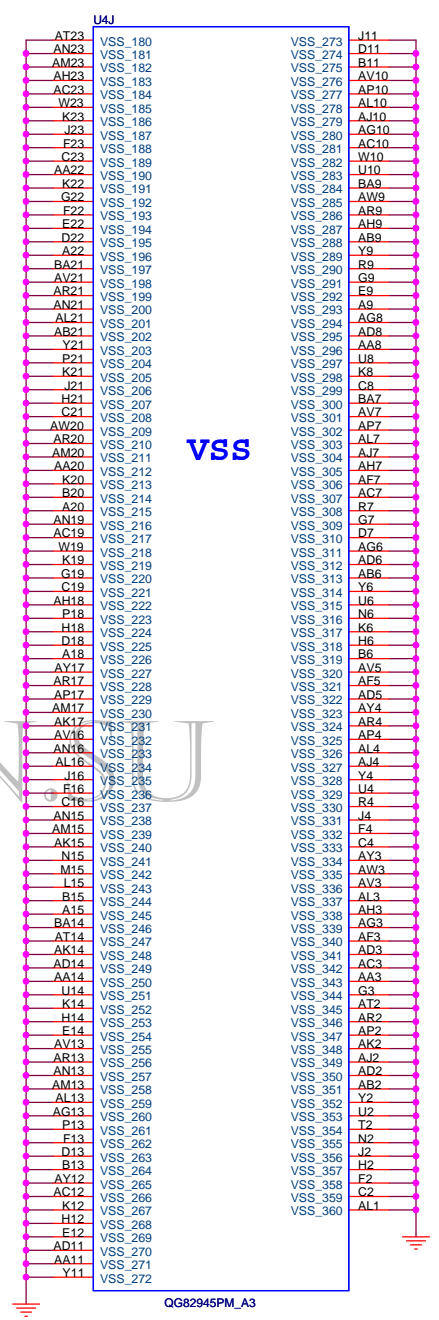
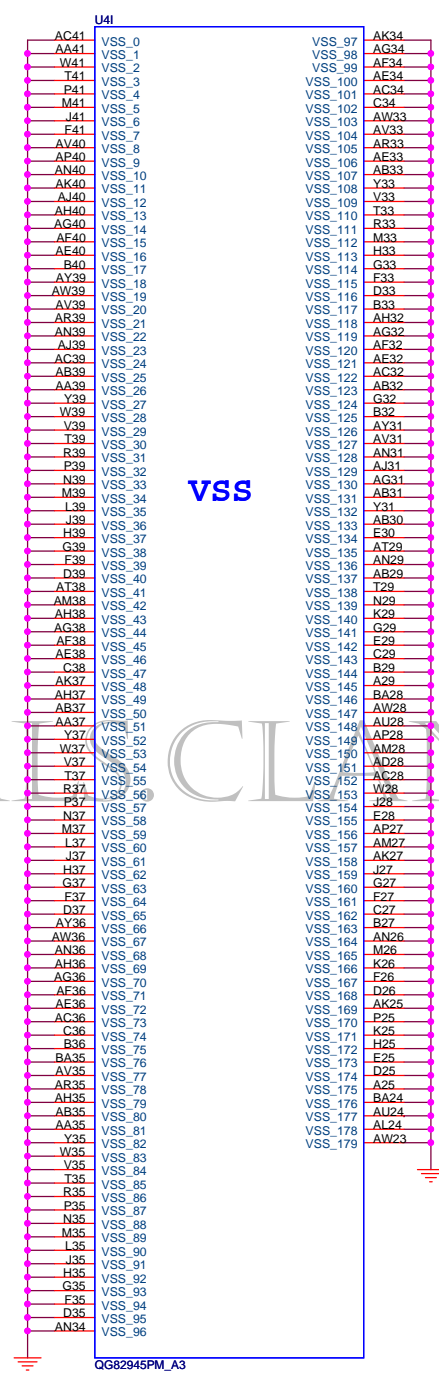
MCH\_CFG\_19 (DMI LANE REVERSAL) Low = Normal(default) High = LANES REVERSED

8 MCH\_CFG\_19 1 30MIL TP558

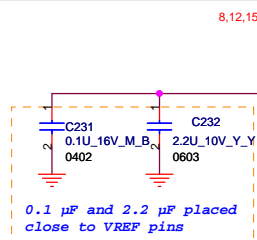
MCH\_CFG\_20 Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

8 MCH\_CFG\_20 1 30MIL TP561

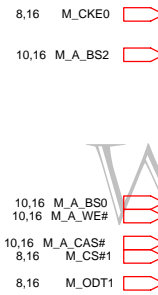
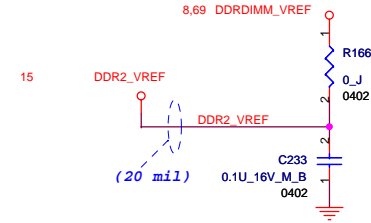
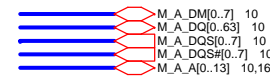
Layout Note: Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub



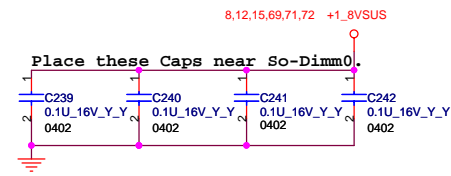
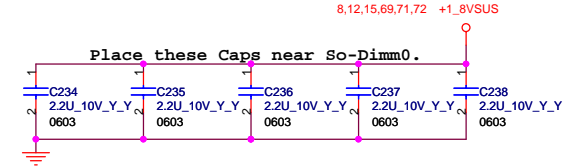
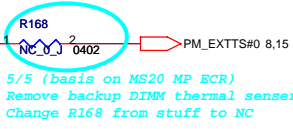




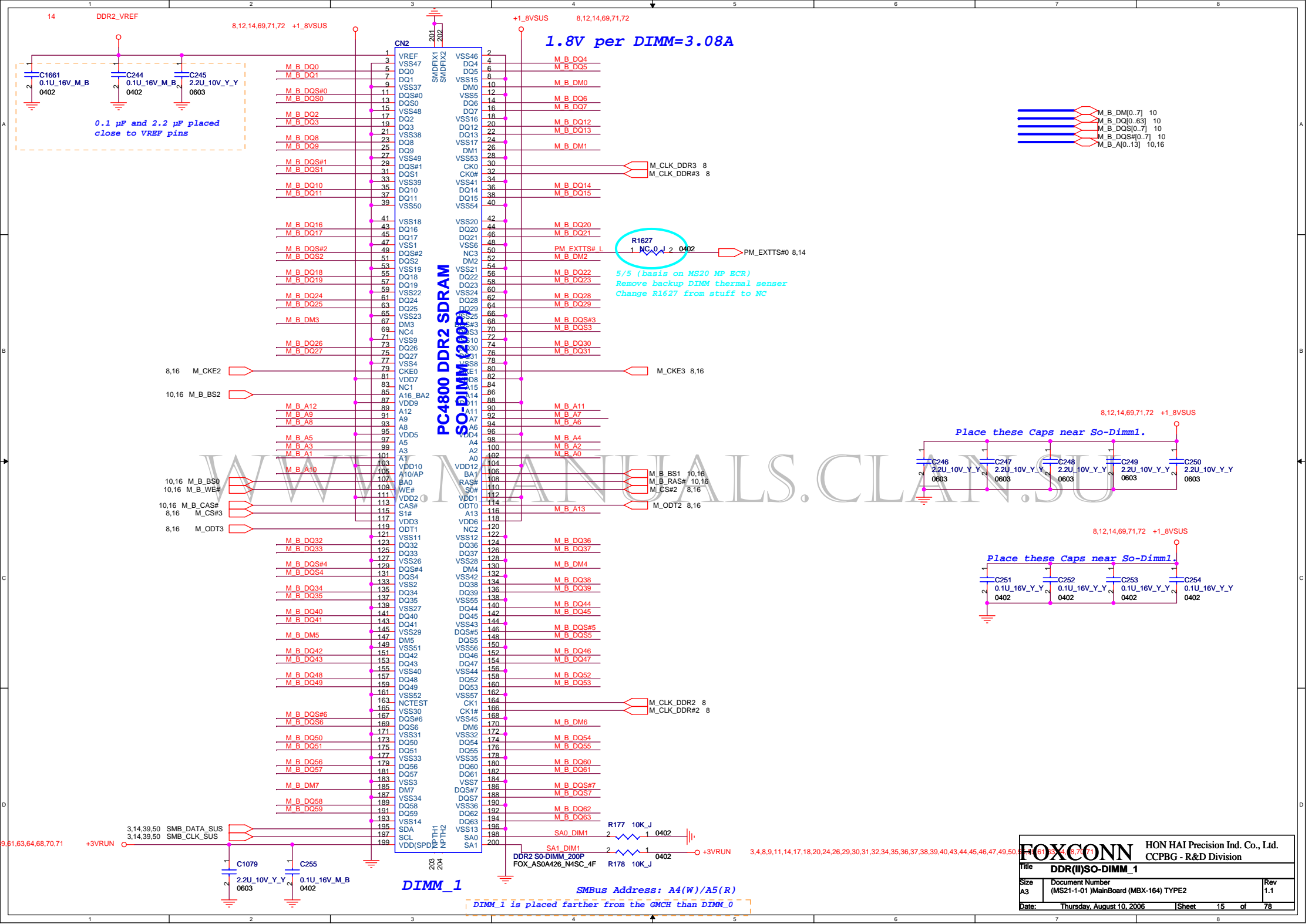
1.8V per DIMM=3.08A



PC4800 DDR2 SDRAM  
SO-DIMM (200P)







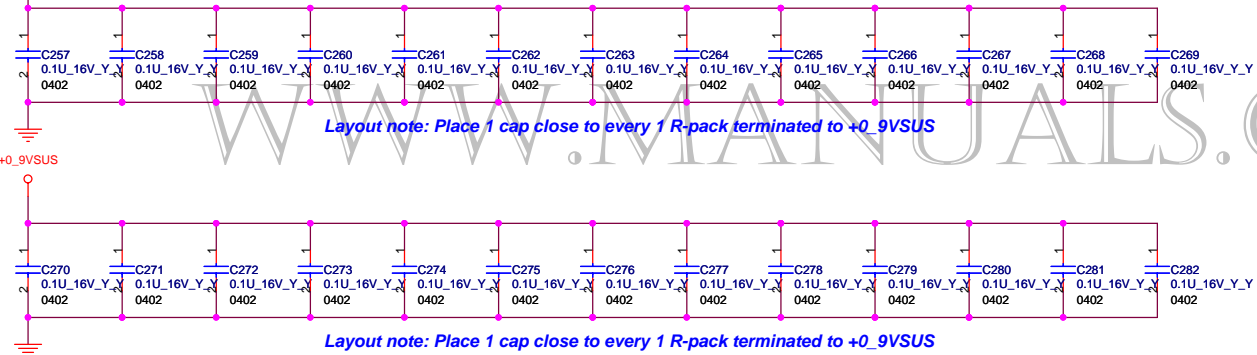


69,72

+0\_9VSUS

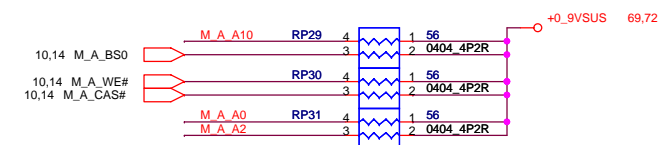
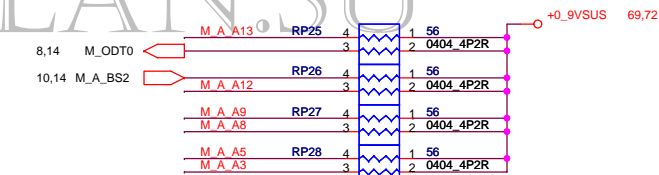
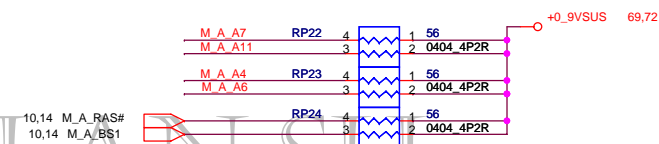
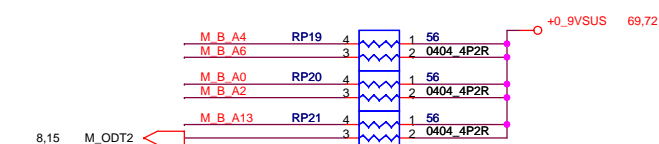
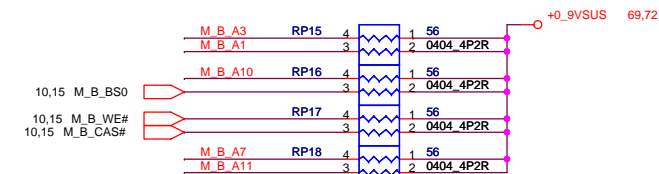
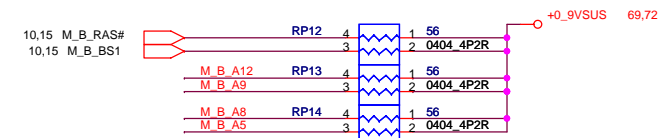
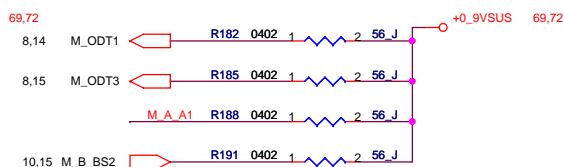
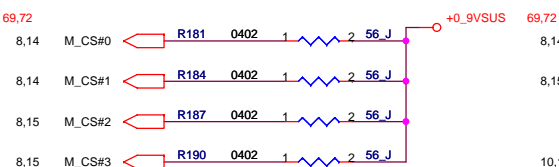
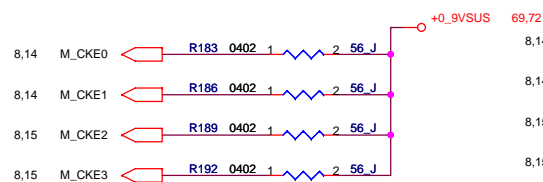
69,72

+0\_9VSUS



Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VSUS

Layout note: Place 1 cap close to every 1 R-pack terminated to +0\_9VSUS



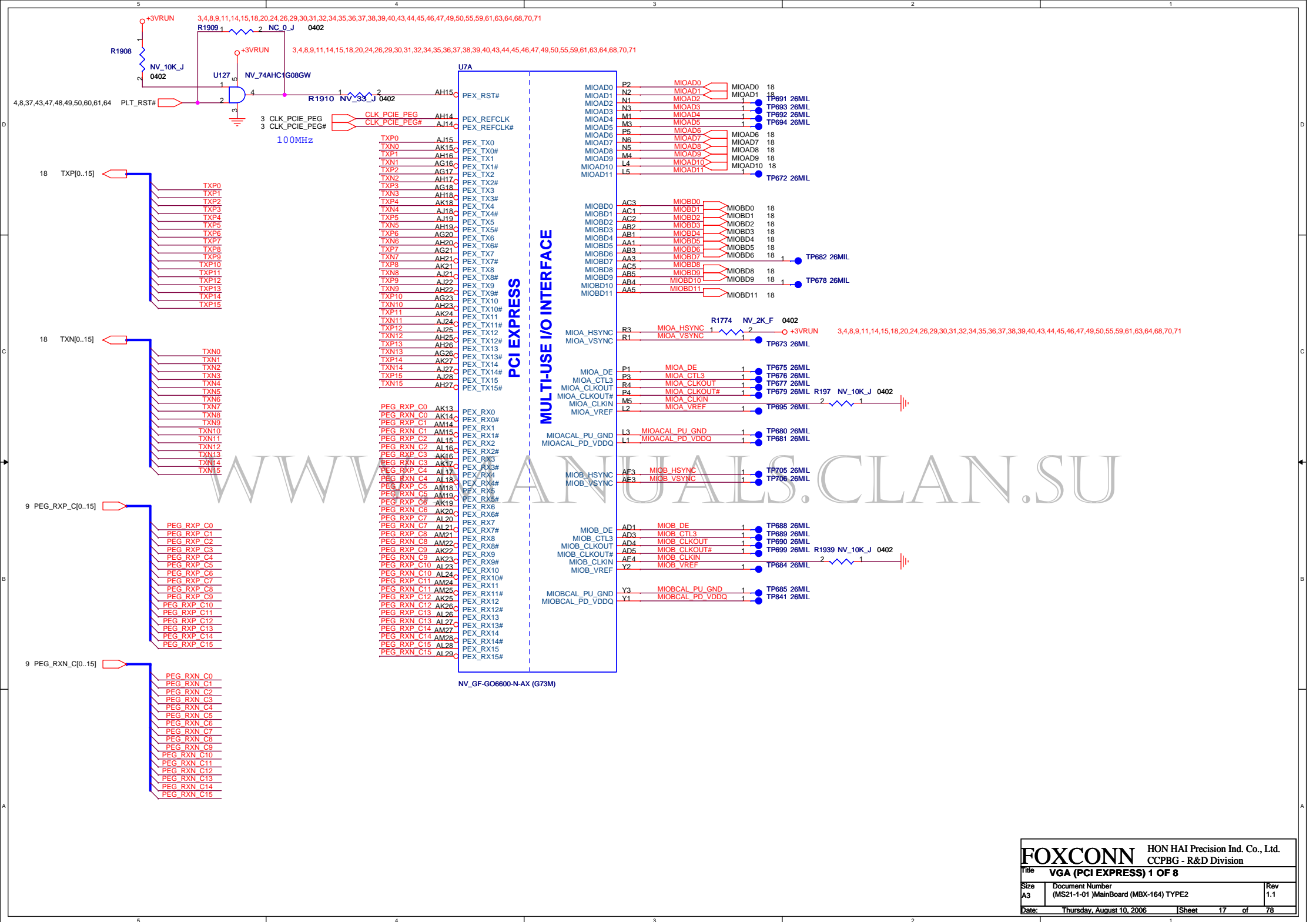
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

File **DDR(II)Termination**

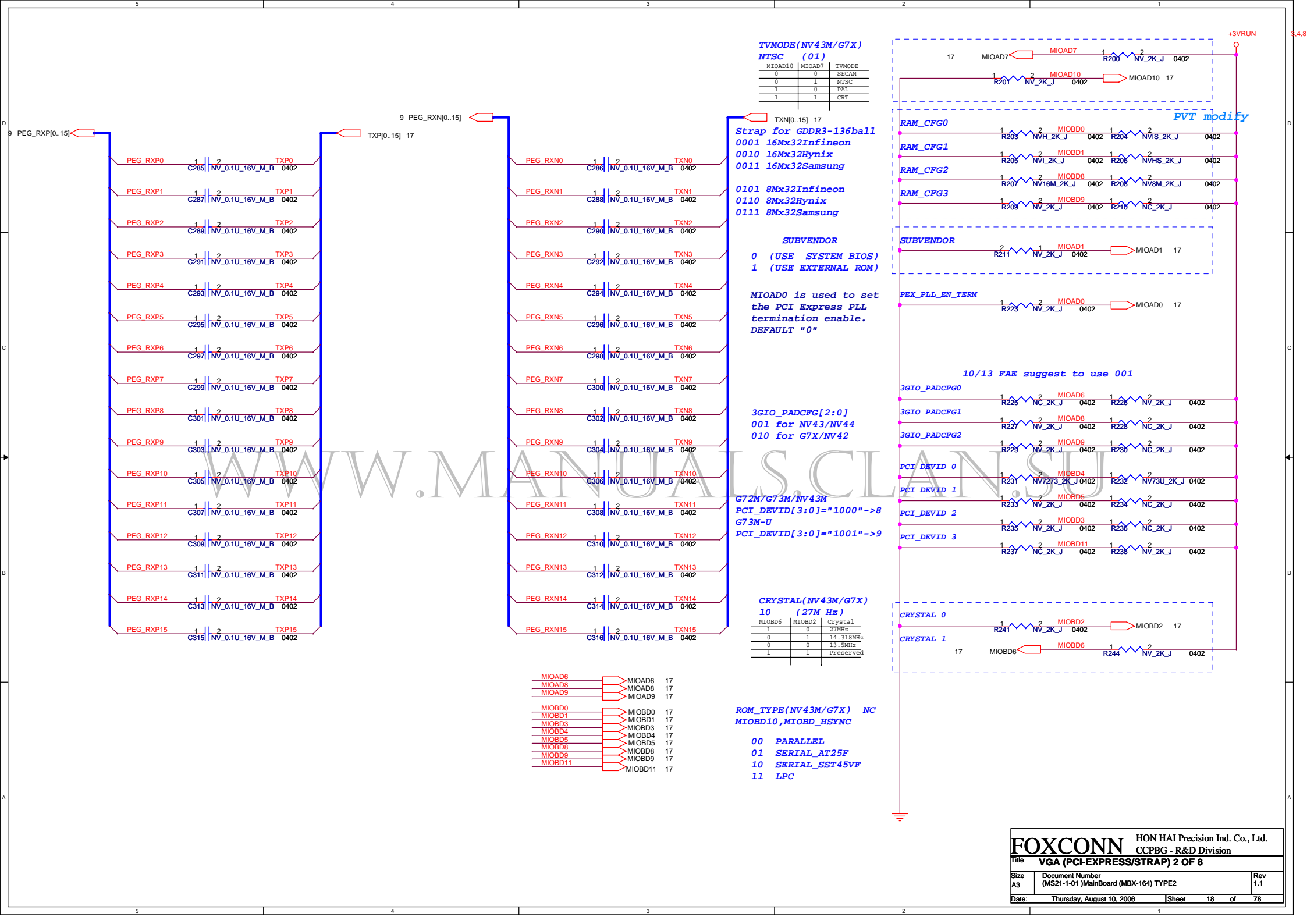
Size **A3** Document Number (MS21-1-01) MainBoard (MBX-164) TYPE2 Rev 1.1

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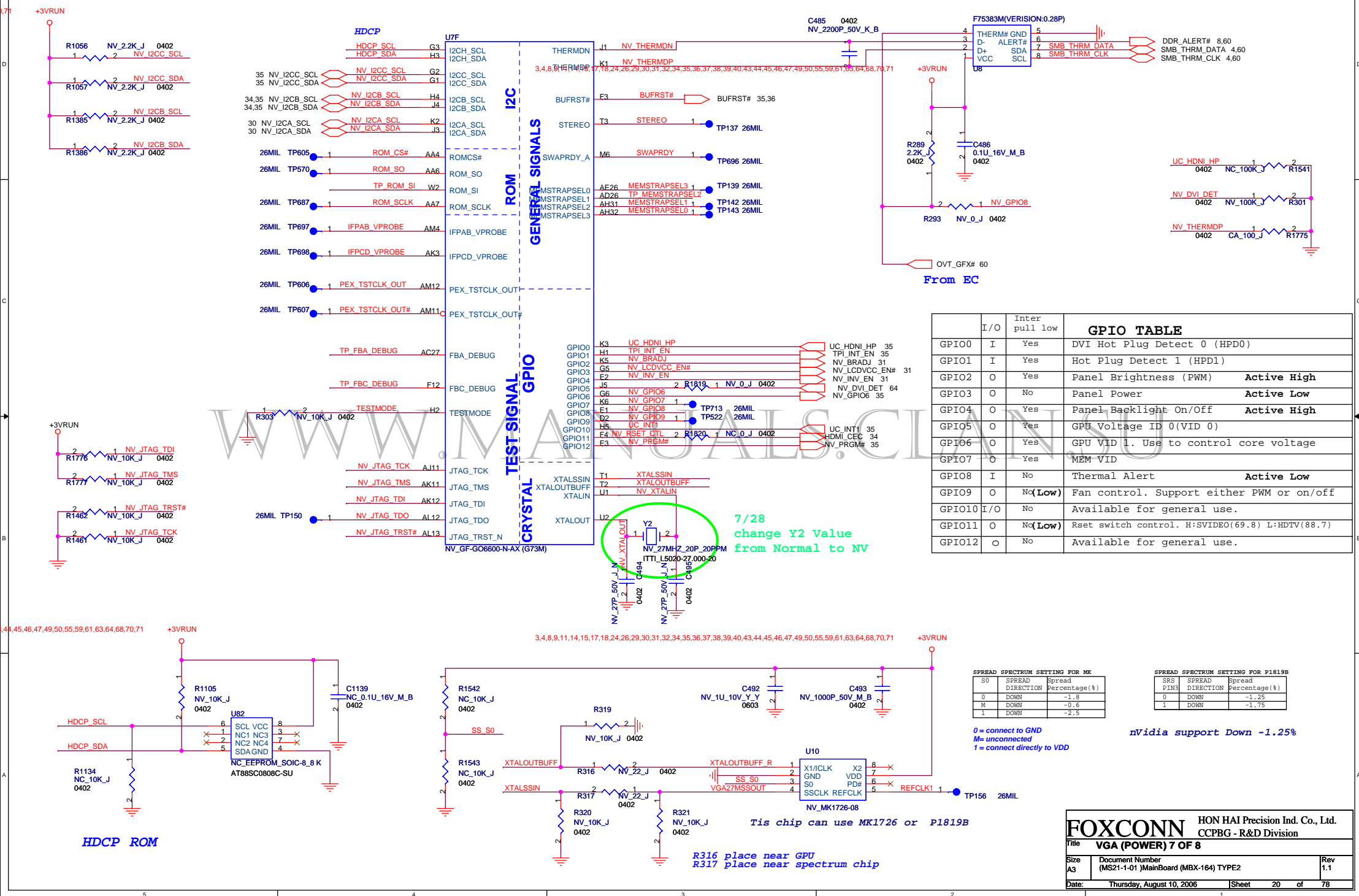












	I/O	Inter pull low	GPIO TABLE	
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)	
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)	
GPIO2	O	Yes	Panel Brightness (PWM)	Active High
GPIO3	O	No	Panel Power	Active Low
GPIO4	O	Yes	Panel Backlight On/Off	Active High
GPIO5	O	Yes	GPU Voltage ID 0 (VID 0)	
GPIO6	O	Yes	GPU VID 1. Use to control core voltage	
GPIO7	O	Yes	MEM VID	
GPIO8	I	No	Thermal Alert	Active Low
GPIO9	O	No (Low)	Fan control. Support either PWM or on/off	
GPIO10	I/O	No	Available for general use.	
GPIO11	O	No (Low)	Reset switch control. H: SVIDEO(69.8) L: HDTV(88.7)	
GPIO12	O	No	Available for general use.	

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

0 = connect to GND  
M= unconnected  
1 = connect directly to VDD

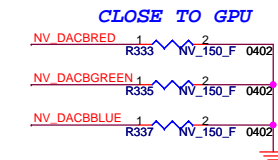
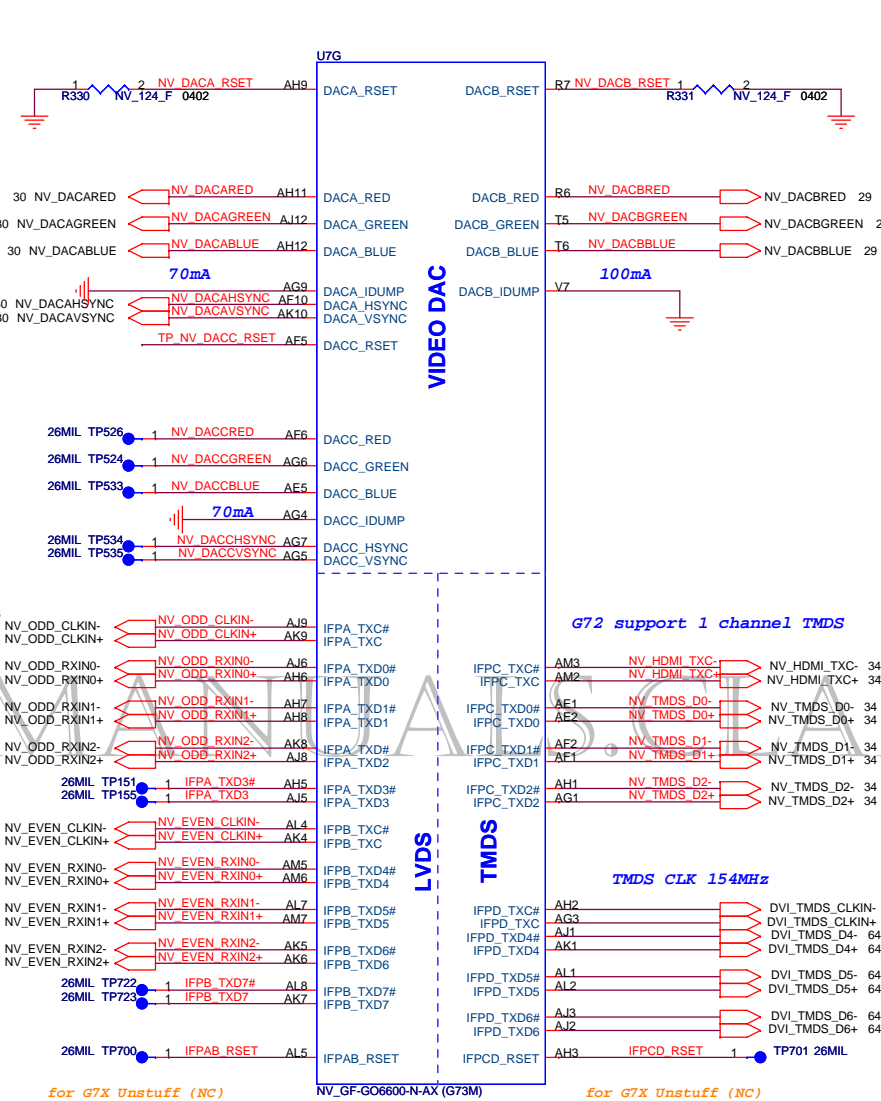
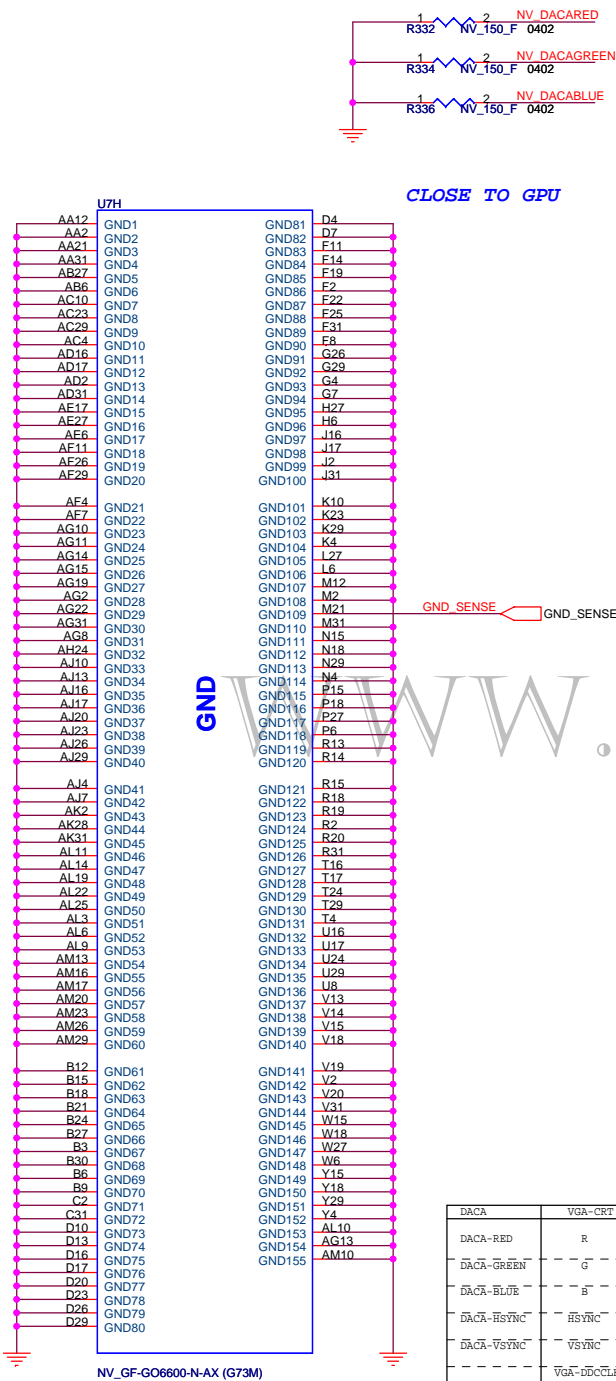
SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

nVidia support Down -1.25%

Tis chip can use MK1726 or P1819B

```
R316 place near GPU
R317 place near spectrum chip
```



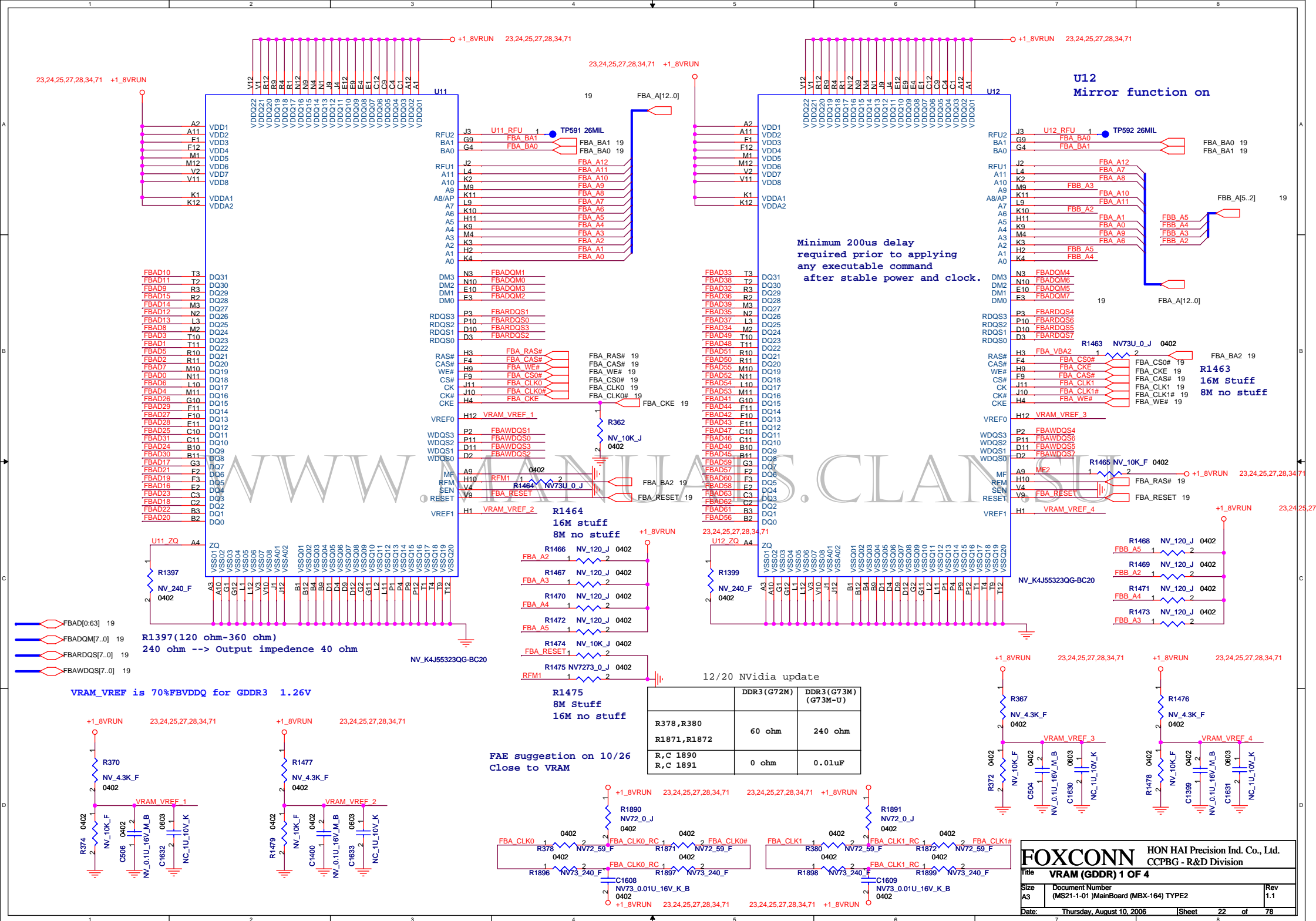


DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

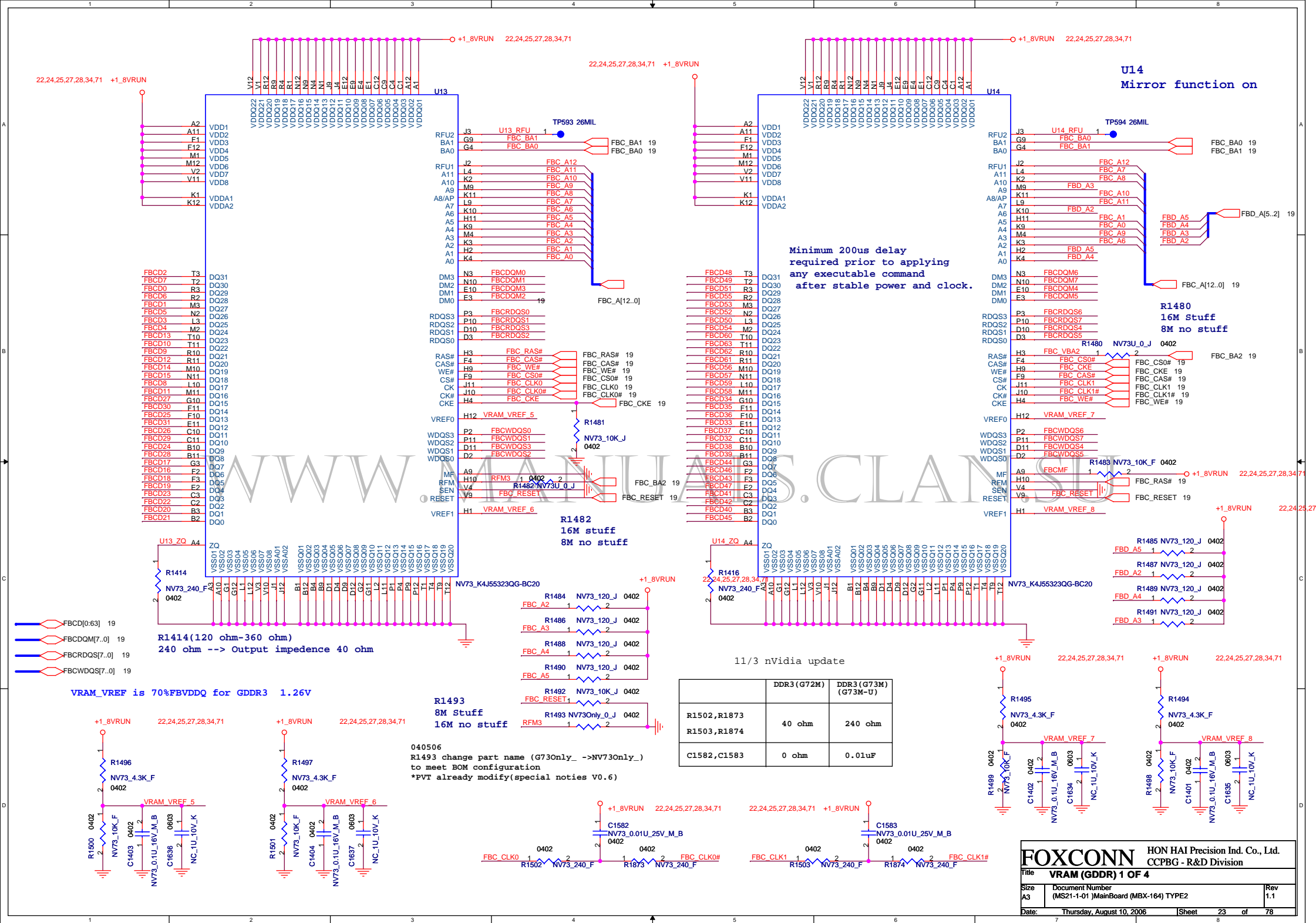
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DDCCLK	SCL
	DVI-DDCDATA	SDA

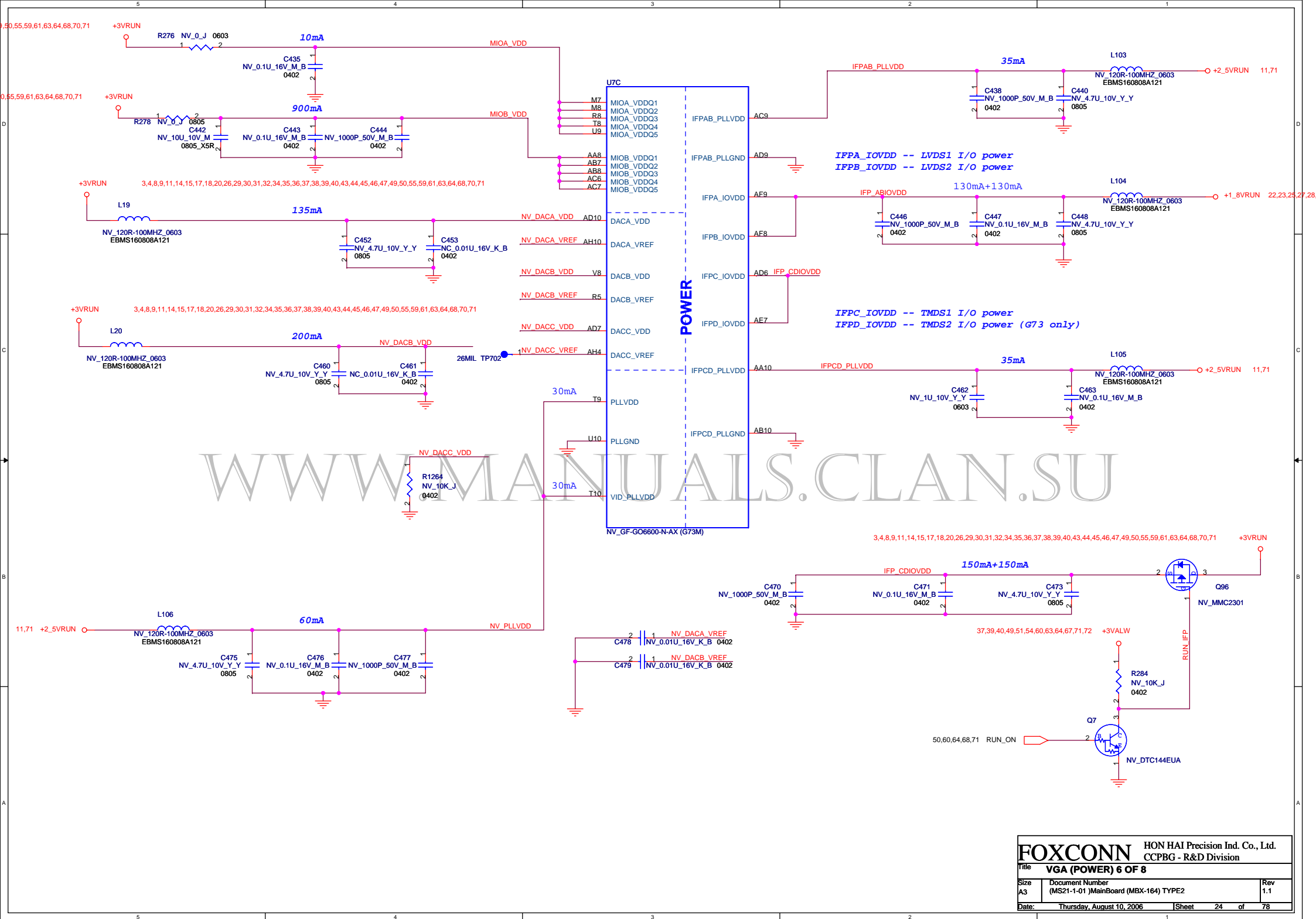






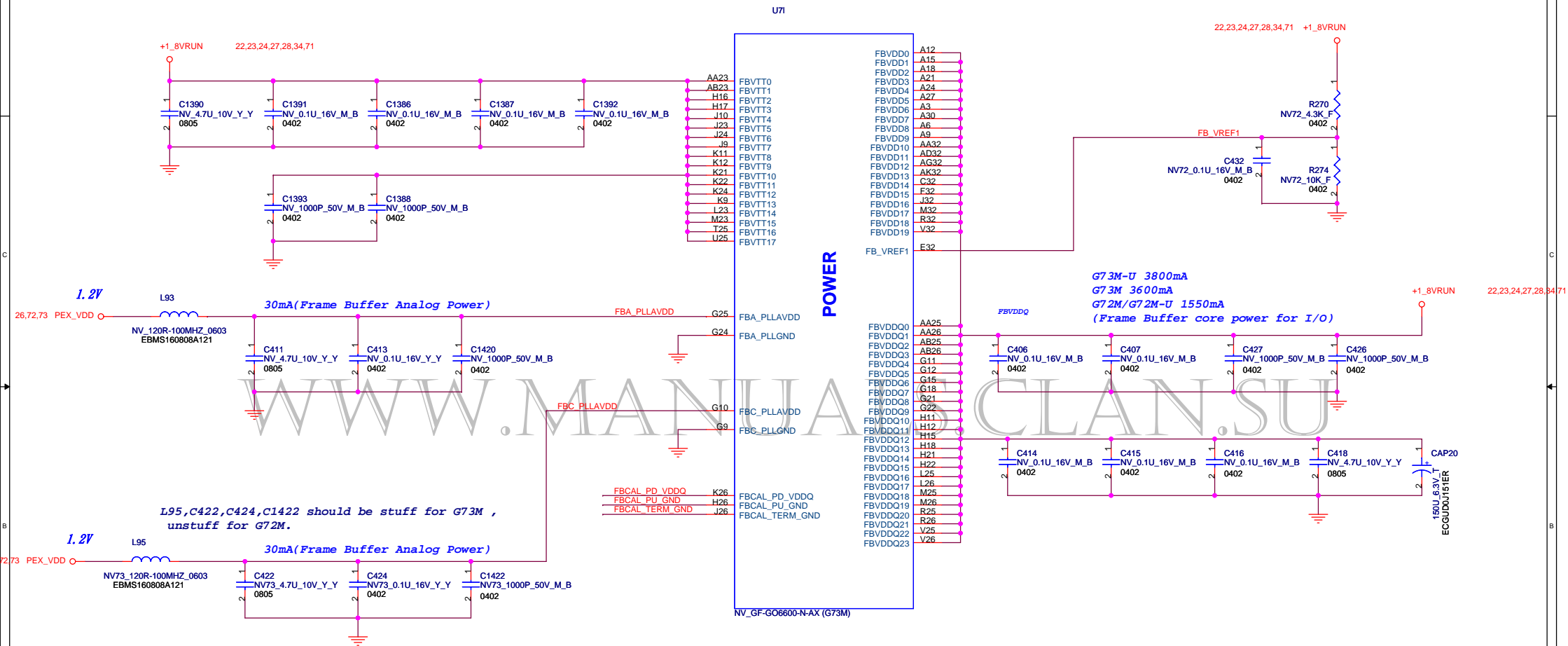








For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.



	DDR1	DDR3(G72M)	DDR3(G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

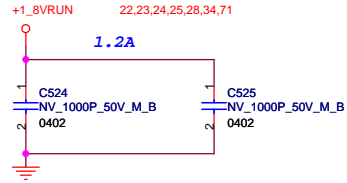
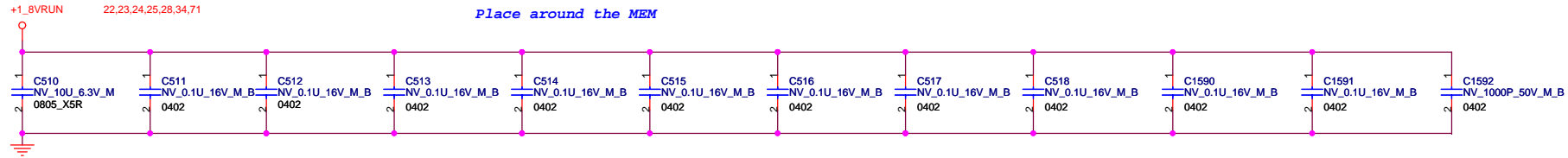






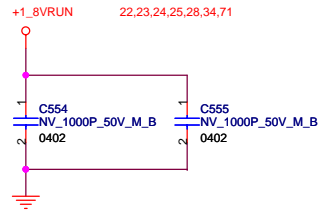
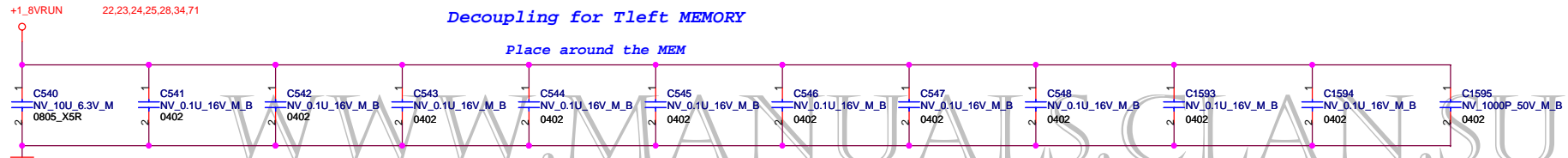
### Decoupling for Tright MEMORY

Place around the MEM



### Decoupling for Tleft MEMORY

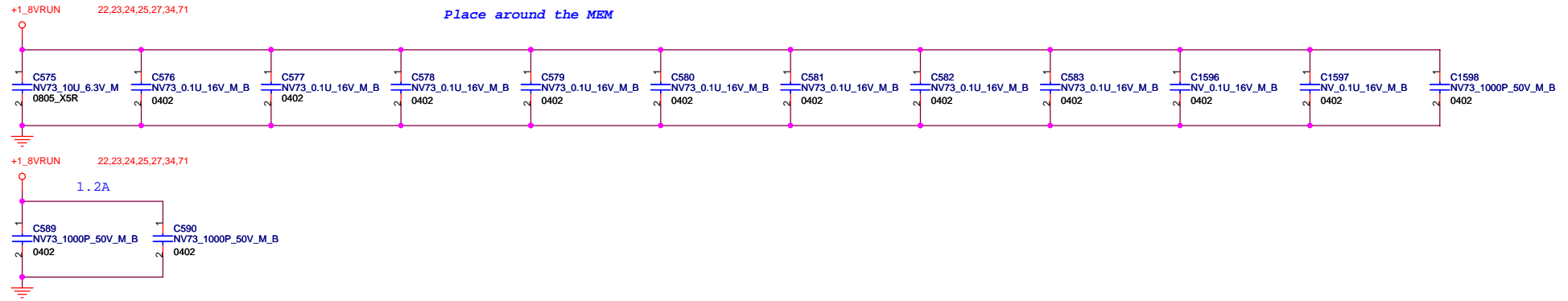
Place around the MEM





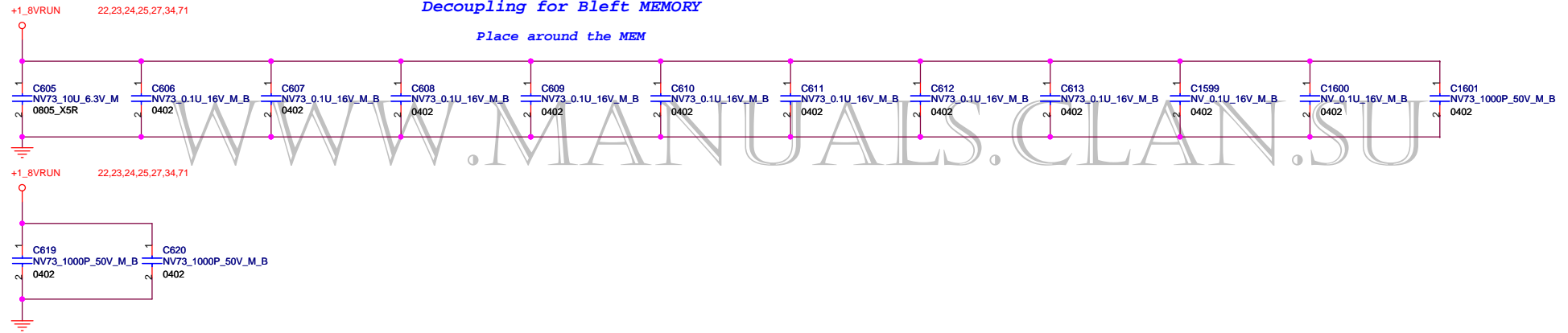
### Decoupling for Bright MEMORY

Place around the MEM



### Decoupling for Bleft MEMORY

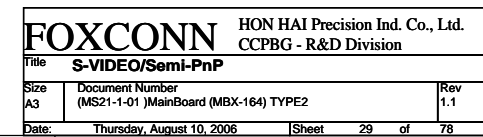
Place around the MEM





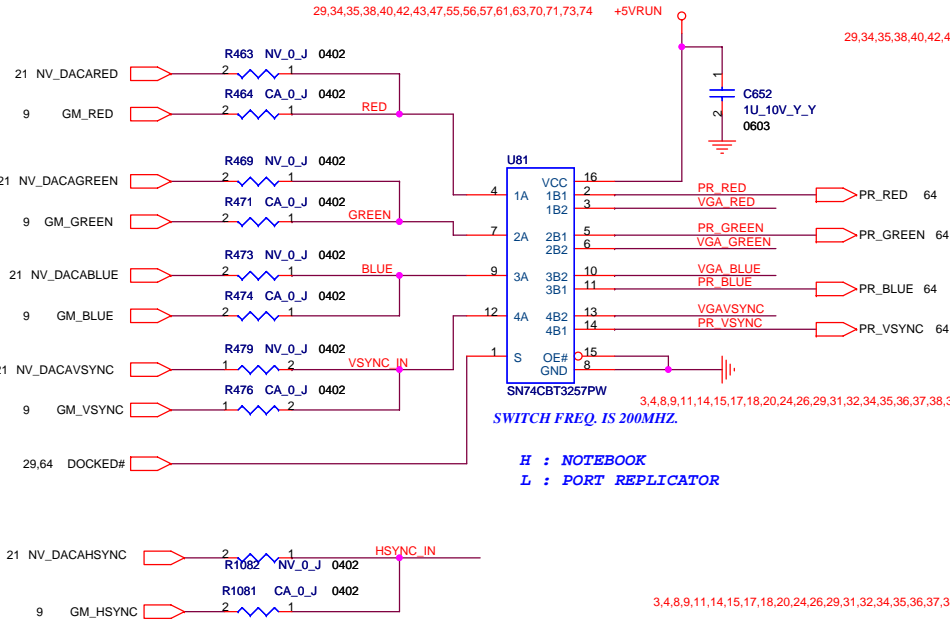
## S-VIDEO

These component close to S-Video connector within 700 mil



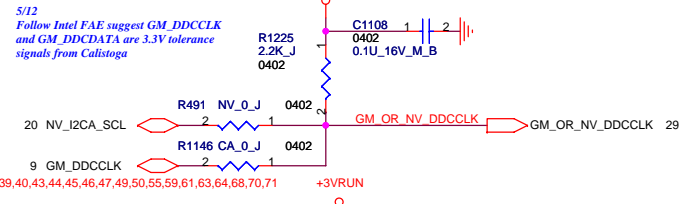


## CRT ANALOG SWITCH

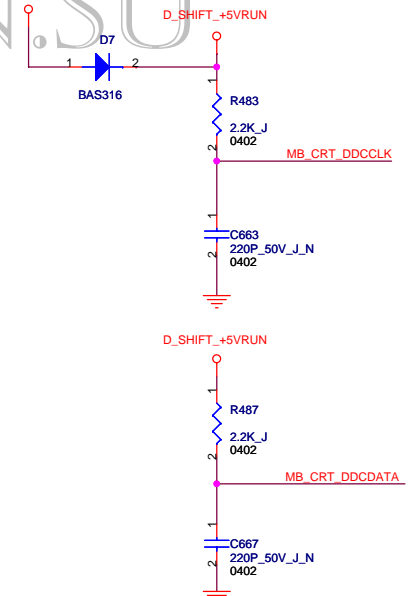
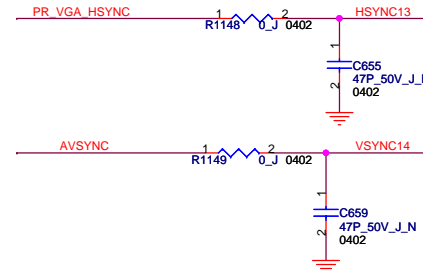
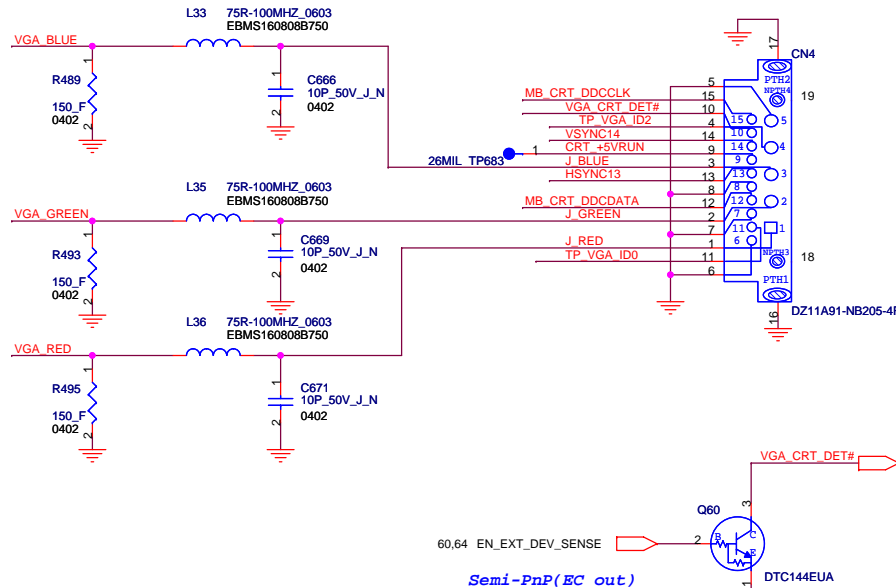


3,4,8,9,11,14,15,17,18,20,24,26,29,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71

5/12  
Follow Intel FAE suggest GM\_DDCCLK  
and GM\_DDCDATA are 3.3V tolerance  
signals from Calistoga



## CRT CONNECTOR



FOXCONN			HON HAI Precision Ind. Co., Ltd.	
Title			CCPBG - R&D Division	
Size			Document Number	
A3			(MS21-1-01) MainBoard (MBX-164) TYPE2	
Date:			Rev	
Thursday, August 10, 2006			1.1	
Sheet			30 of 78	



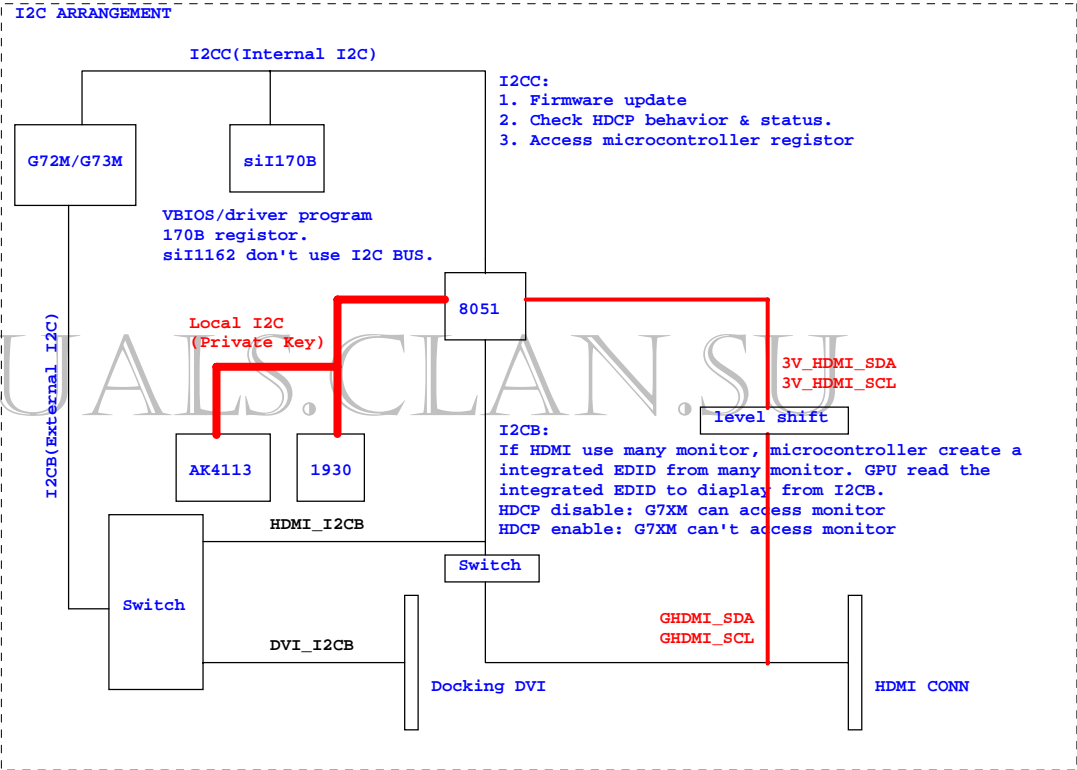
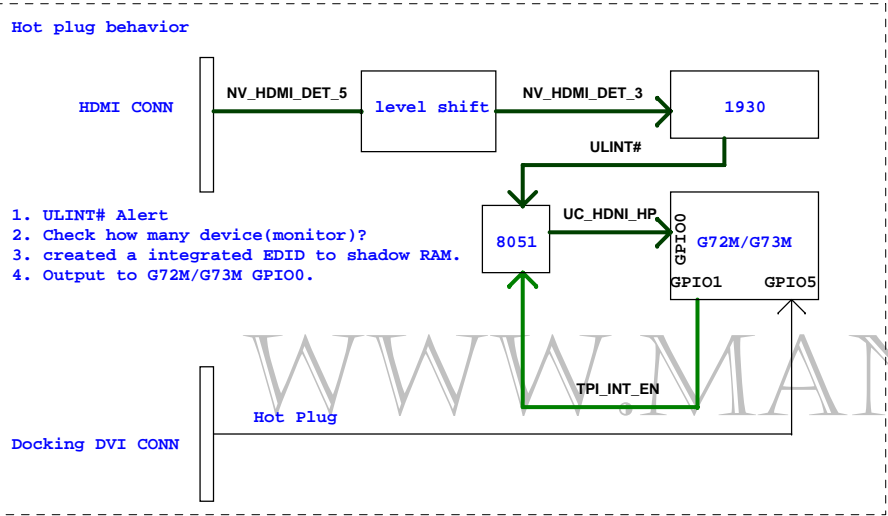




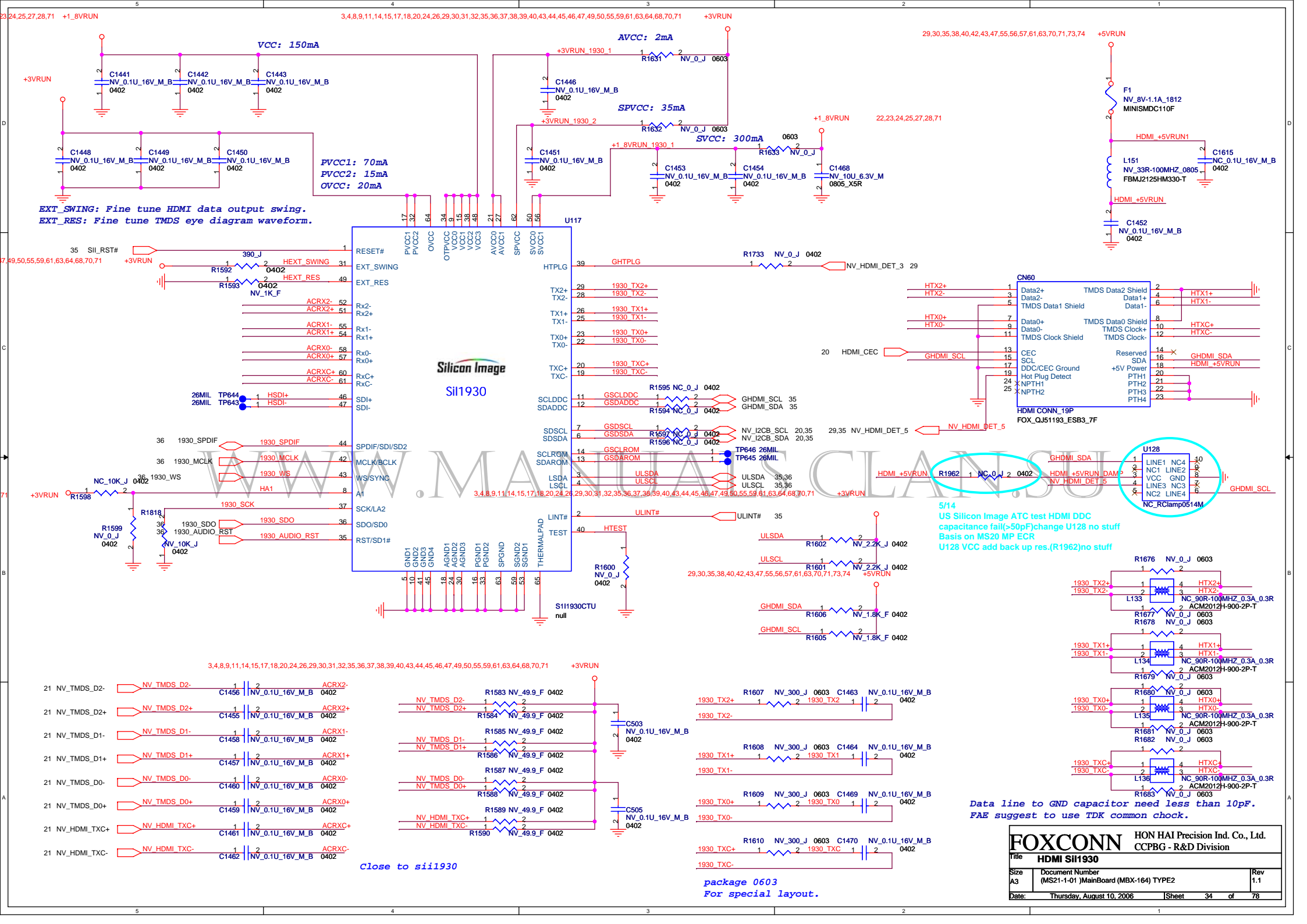




# Hot plug behavior & I2C ARRANGEMENT block diagram







EXT\_SWING: Fine tune HDMI data output swing.  
EXT\_RES: Fine tune TMDs eye diagram waveform.

PVCC1: 70mA  
PVCC2: 15mA  
OVCC: 20mA

AVCC: 2mA

SPVCC: 35mA

SVCC: 300mA

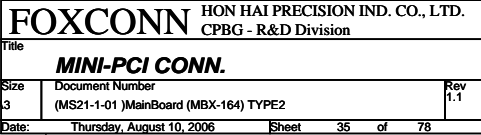
Silicon Image  
SII1930

5/14  
US Silicon Image ATC test HDMI DDC  
capacitance fail(>50pF)change U128 no stuff  
Basis on MS20 MP ECR  
U128 VCC add back up res.(R1962)no stuff

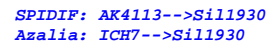
Data line to GND capacitor need less than 10pF.  
FAE suggest to use TDK common choock.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	HDMI SII1930		
Size	Document Number	Rev	
A3	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1	
Date:	Thursday, August 10, 2006	Sheet	34 of 78

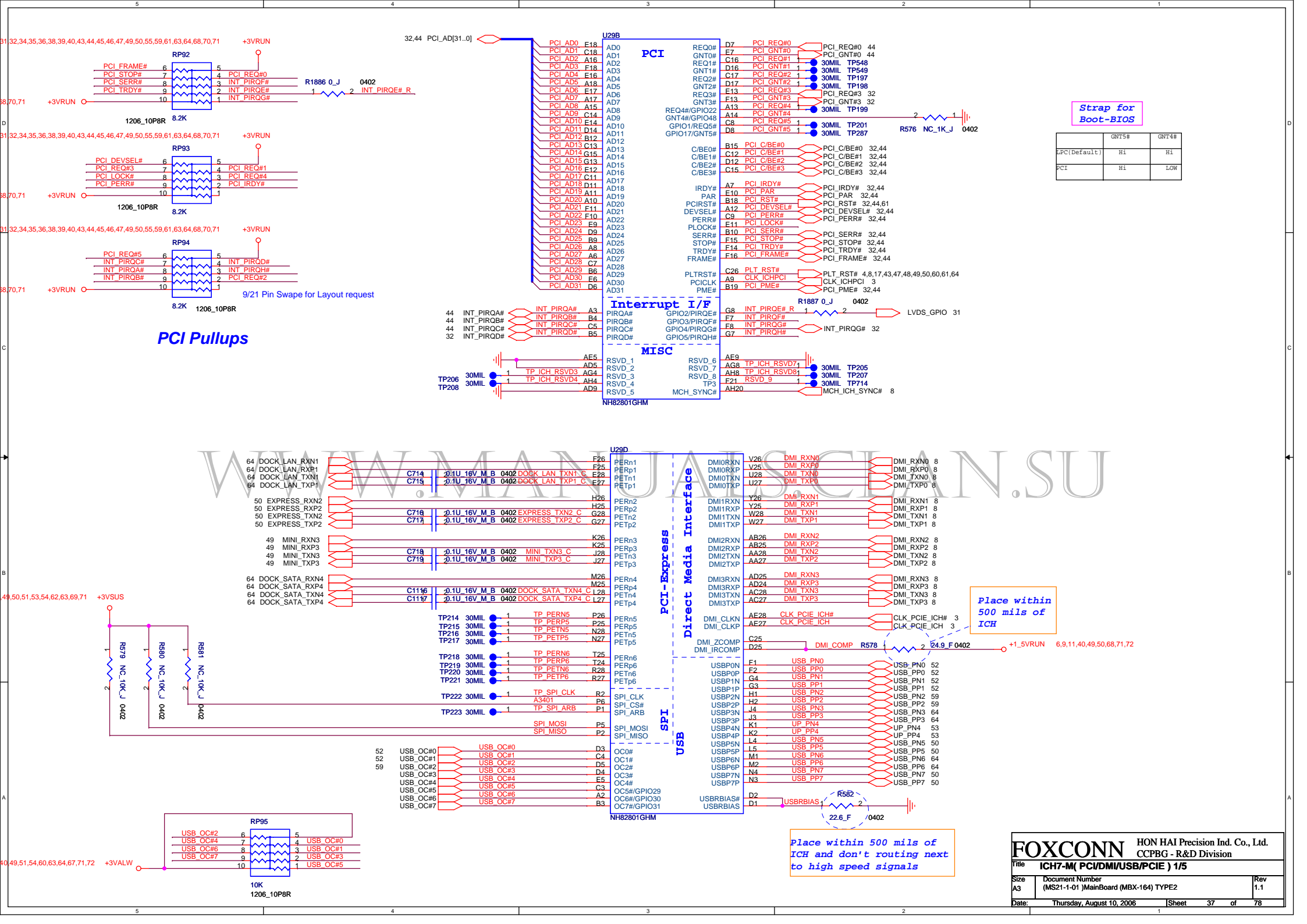












PCI Pullups

Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	H1	H1
PCI	H1	LOW

Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals

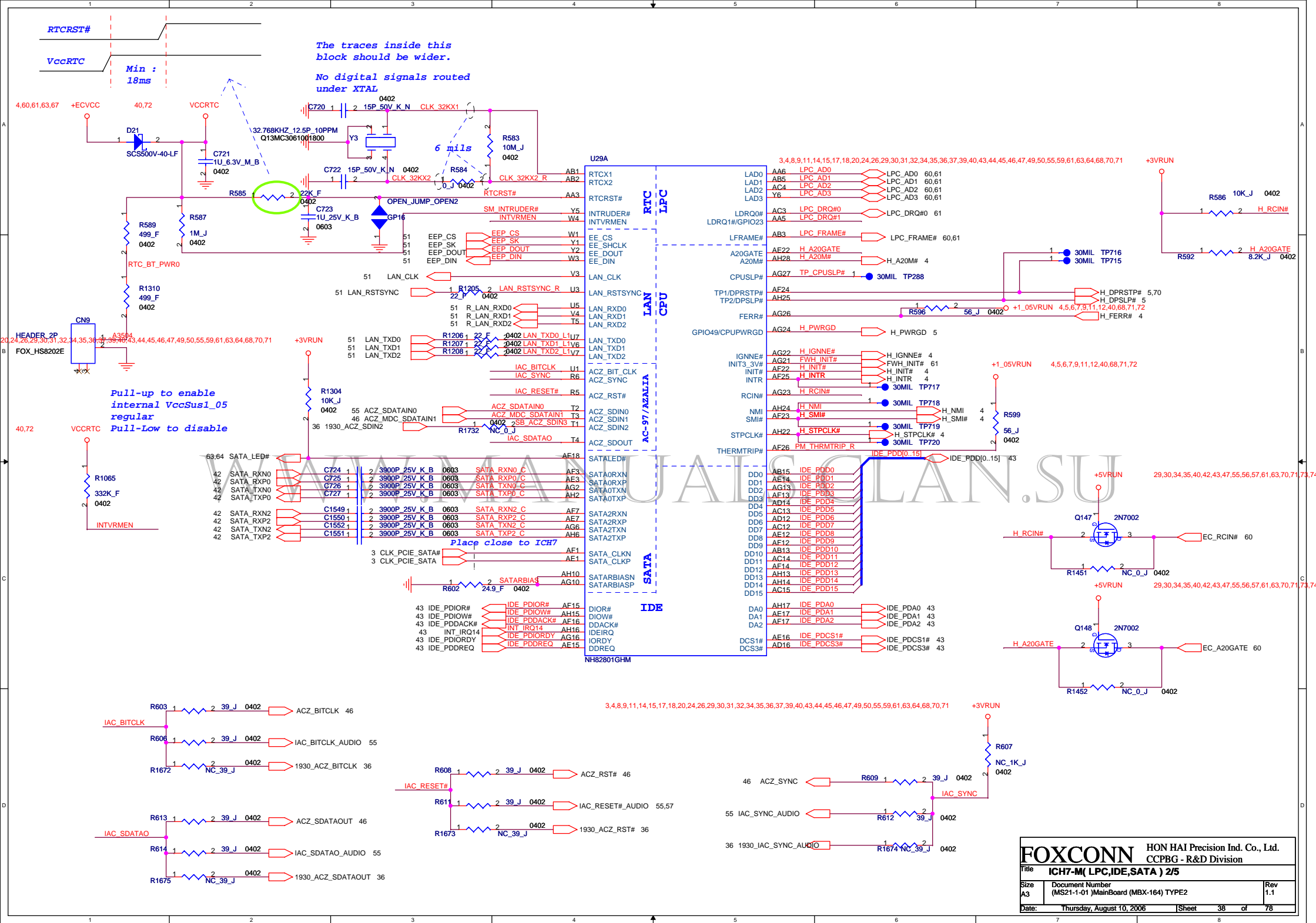
FOXCONN HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title ICH7-M( PC/DMI/USB/PCIE ) 1/5

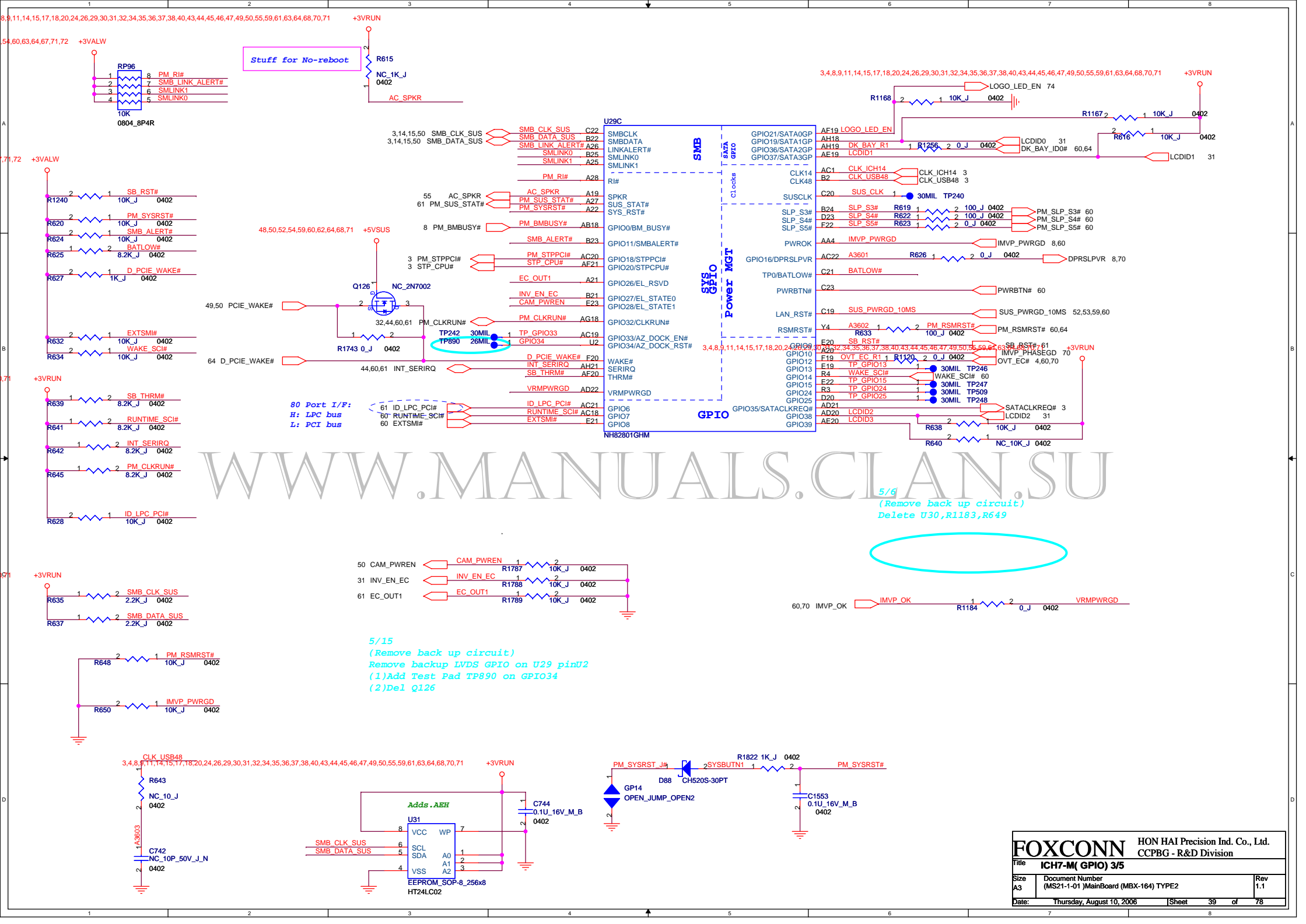
Size A3 Document Number (MS21-1-01 )MainBoard (MBX-164) TYPE2 Rev 1.1

Date: Thursday, August 10, 2006 Sheet 37 of 78

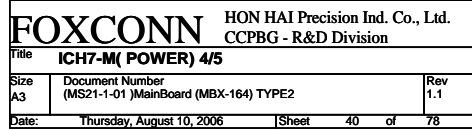




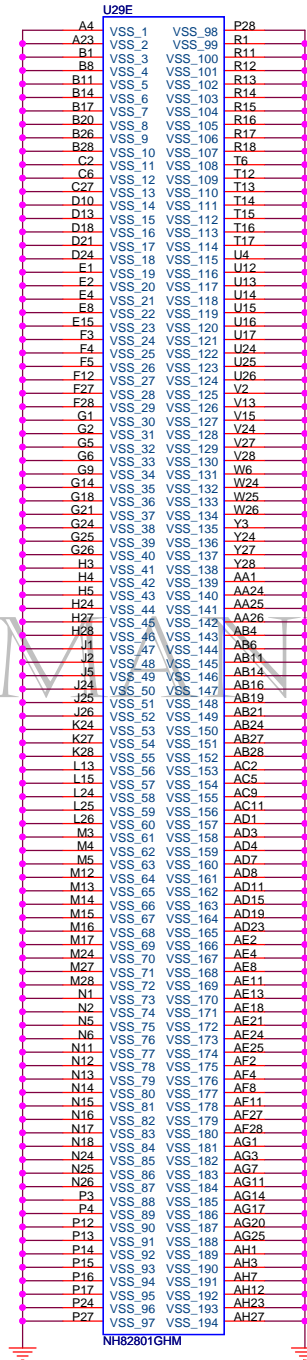








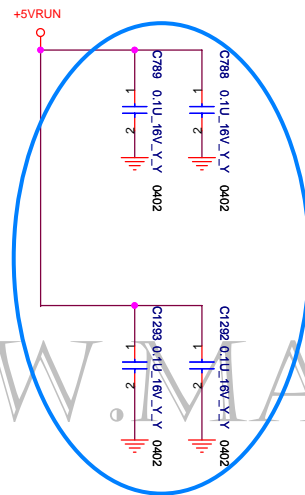






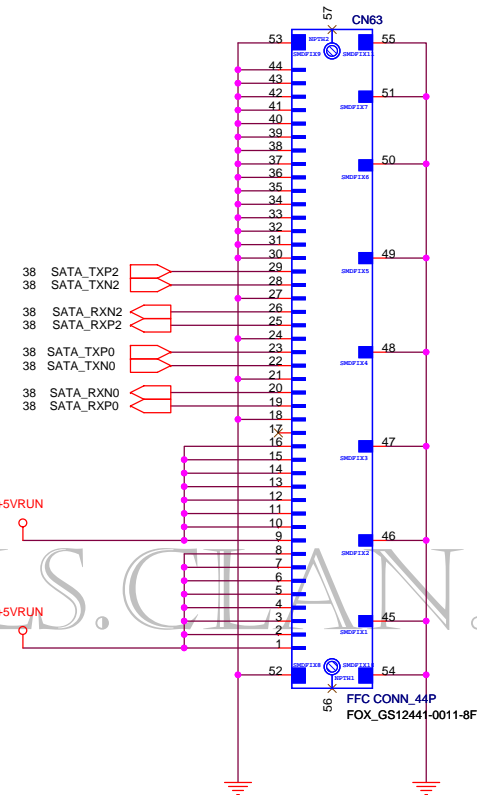
5/6  
 For power droup cause 0.16V voltage loss Issue  
 (1)F7,F8,F19,F20 no stuff  
 (2)Co-layout normal open gap GP17~GP18 with fuse  
 5/27 Delete SATA HDD Fuse backup circuit  
 (1)Remove F7,F8,F19,F20 Pad  
 (2)Remove GP17~GP18 open gap

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74



29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74

29,30,34,35,38,40,43,47,55,56,57,61,63,70,71,73,74



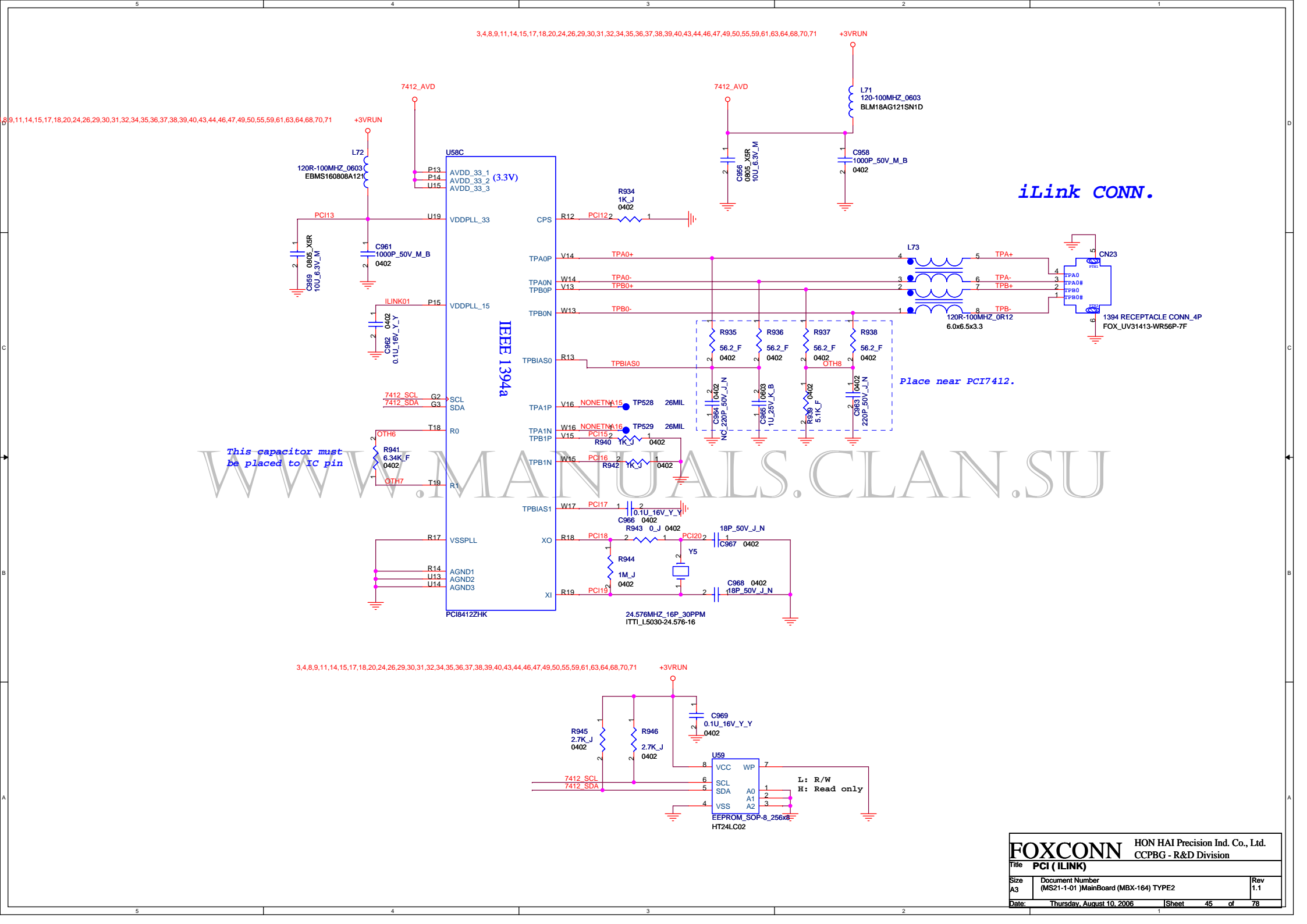




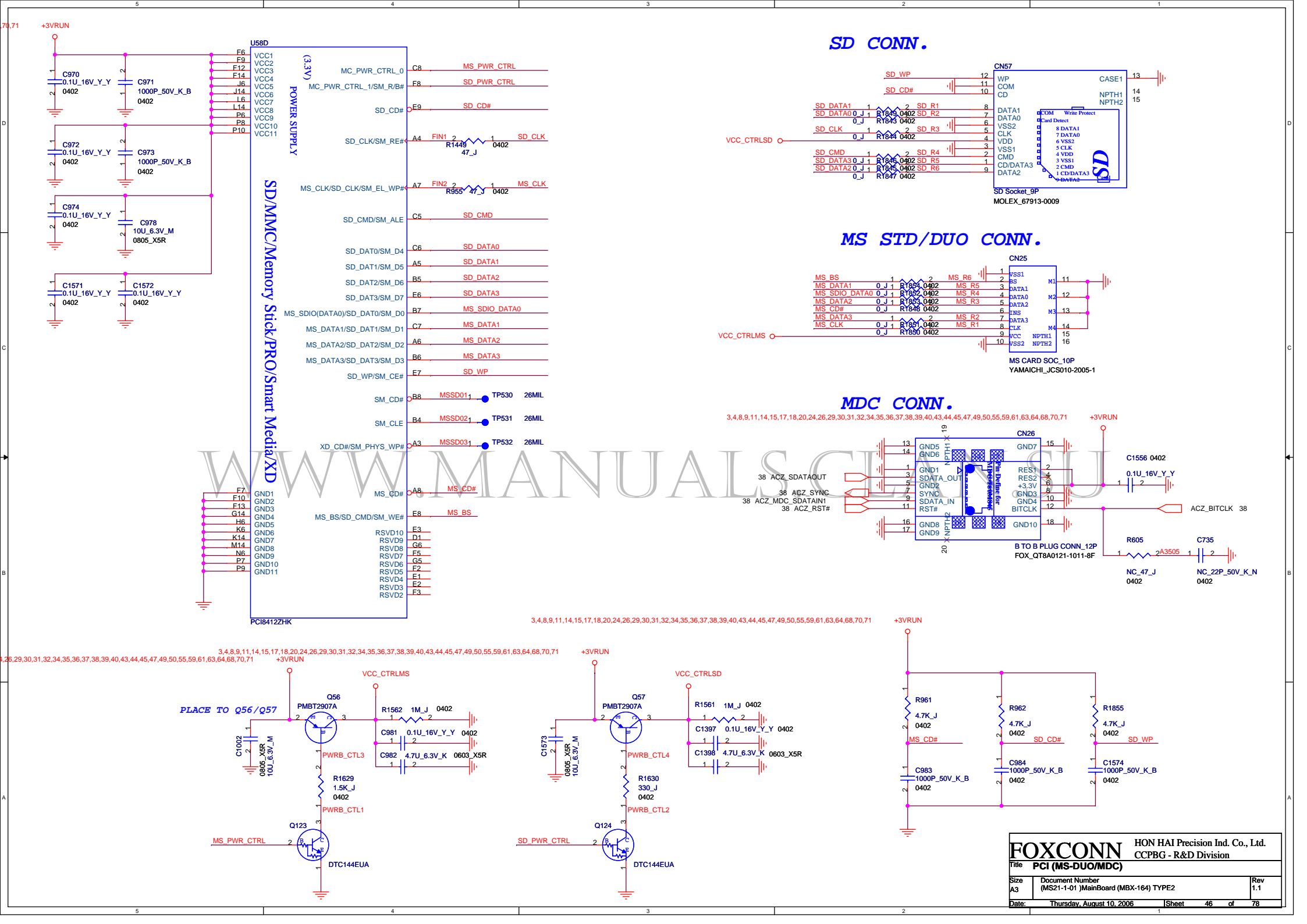




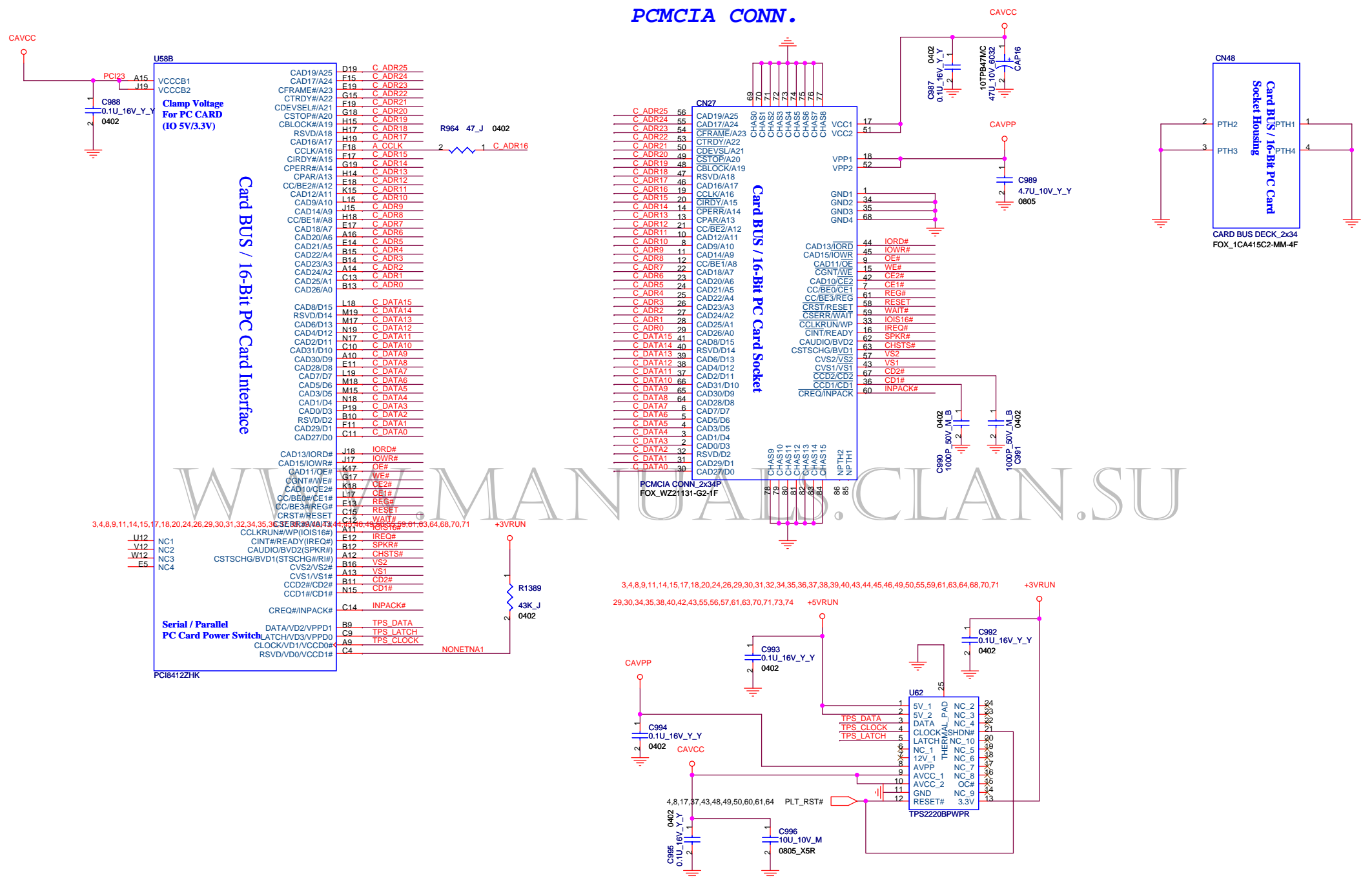




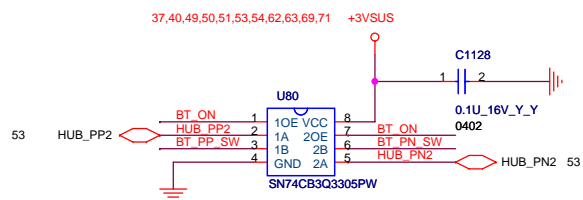
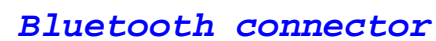




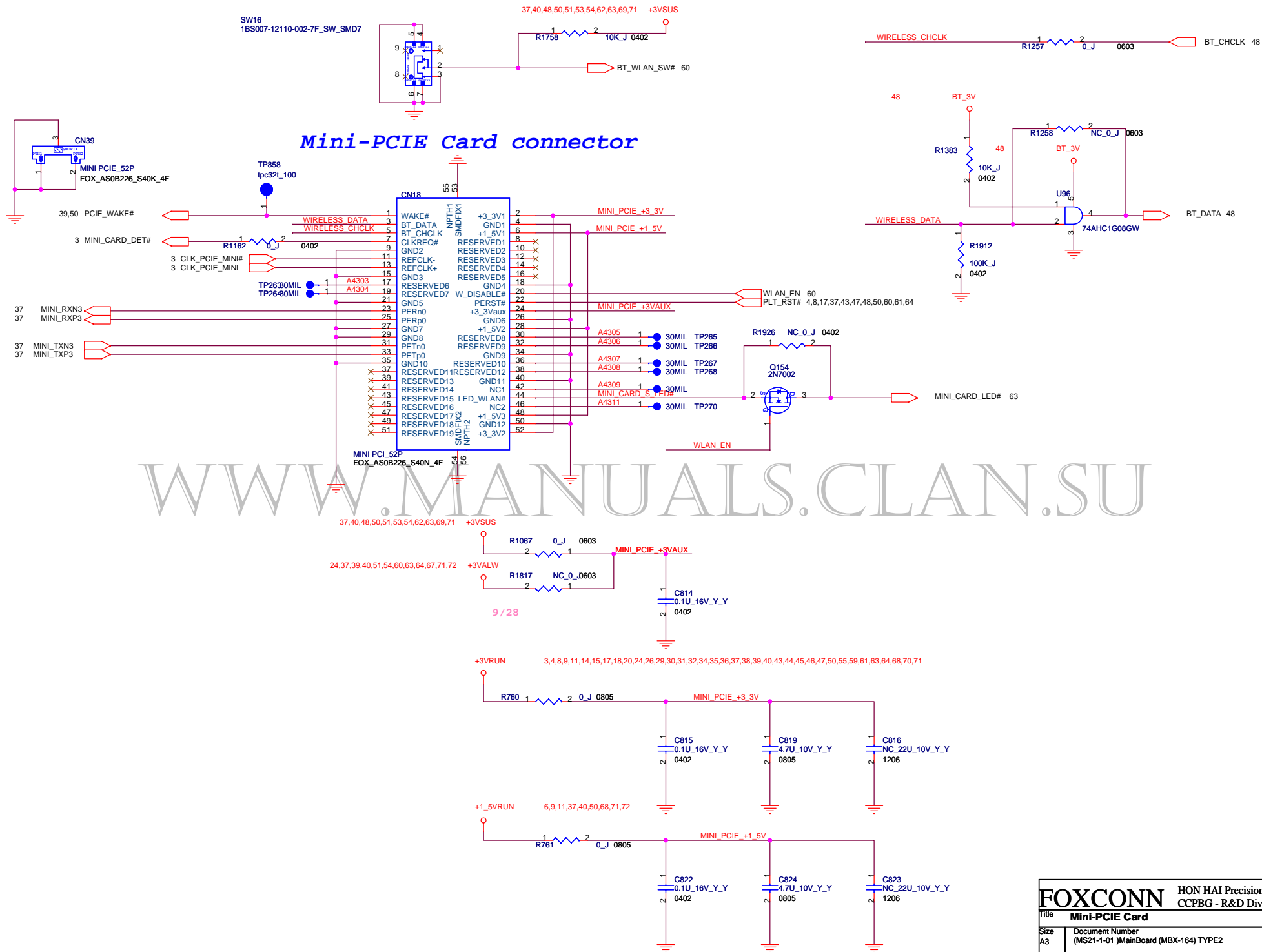






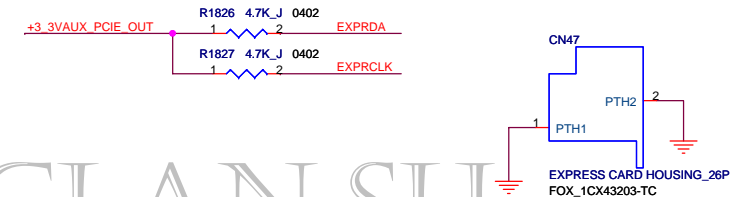
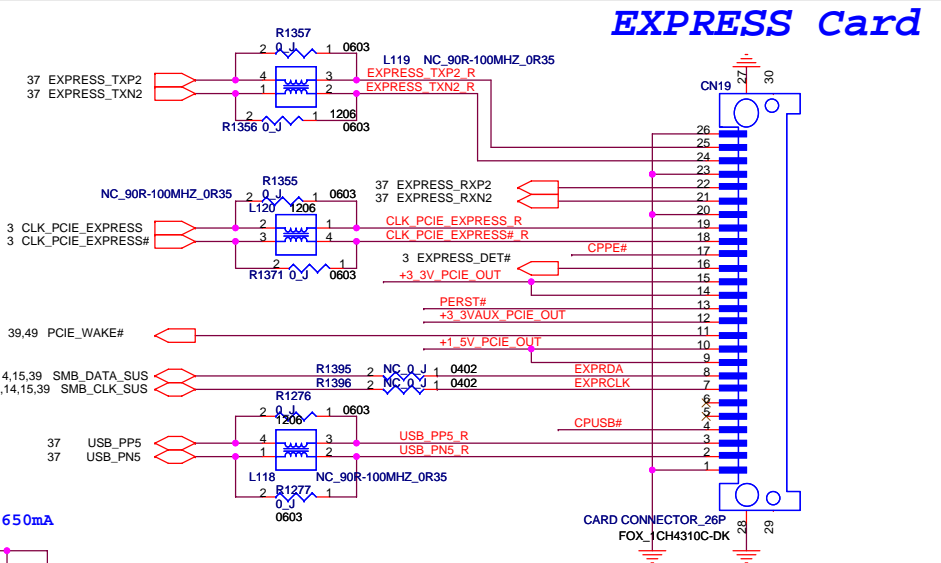
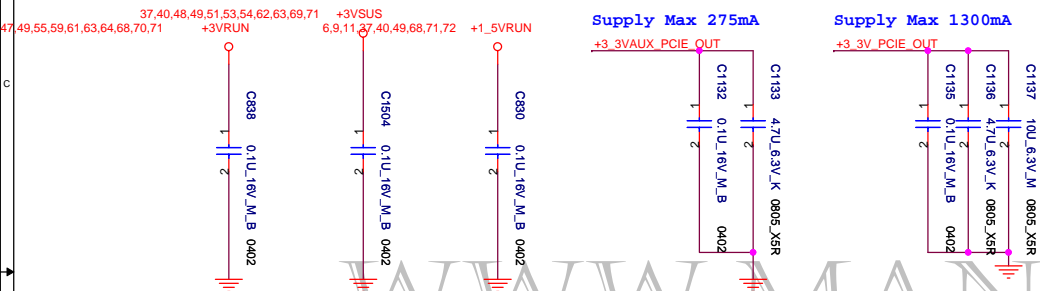
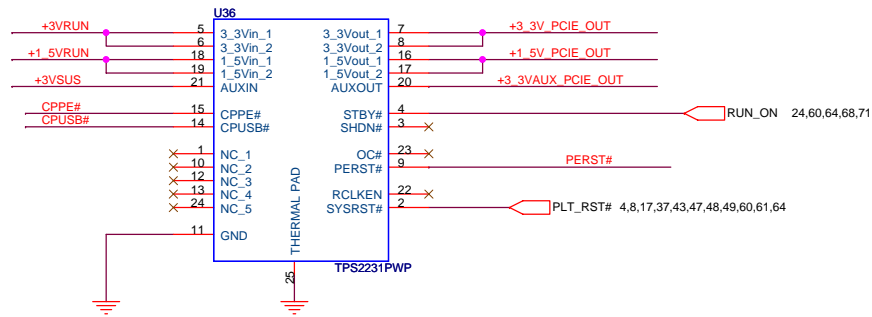




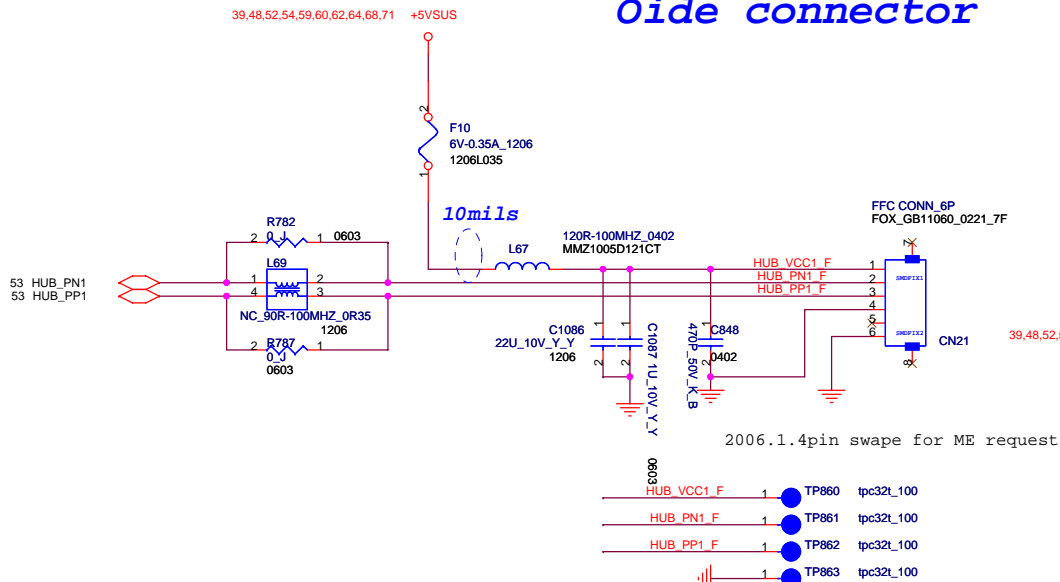




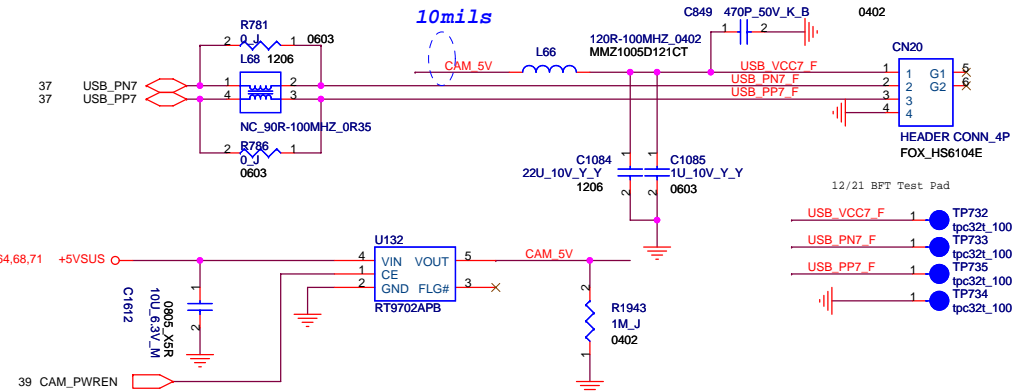
VOLTAGE INPUTS <sup>(1)</sup>			LOGIC INPUTS			VOLTAGE OUTPUTS <sup>(2)</sup>			MODE <sup>(3)</sup>
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP <sup>(4)</sup>	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted



*Oide connector*



## CAMERA connector

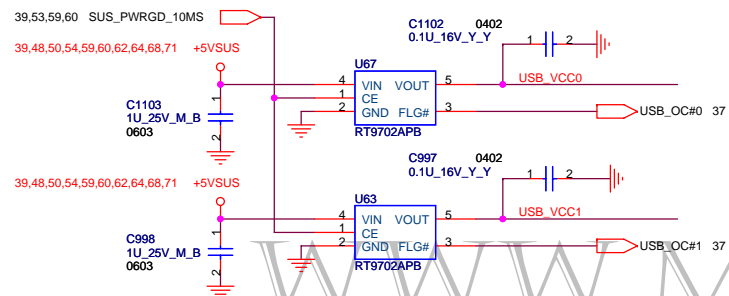
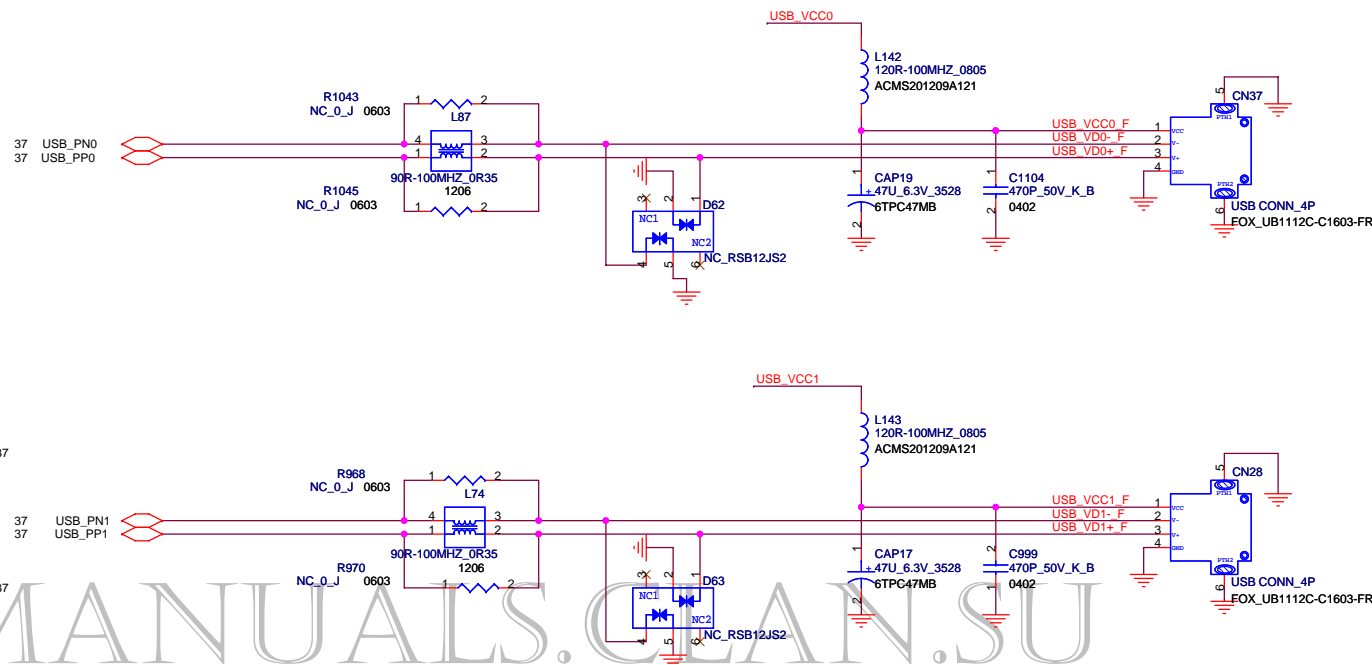






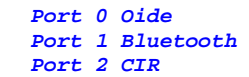


## USB connector #2



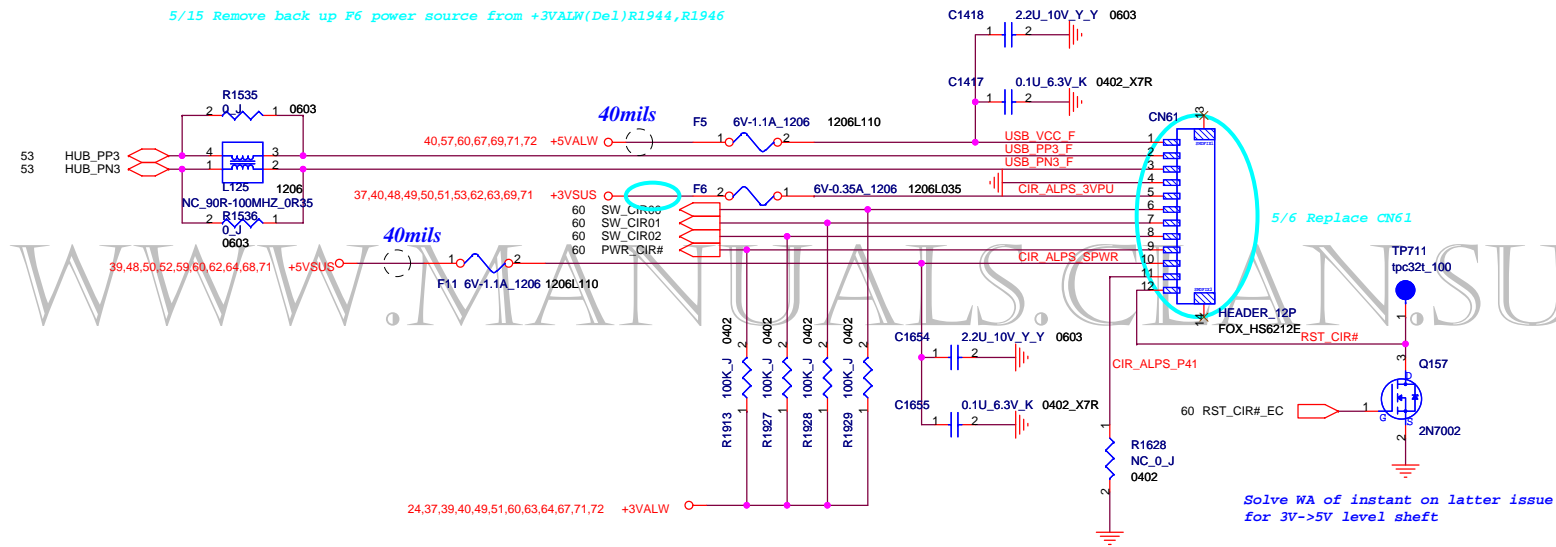


## USB 1.1 HUB



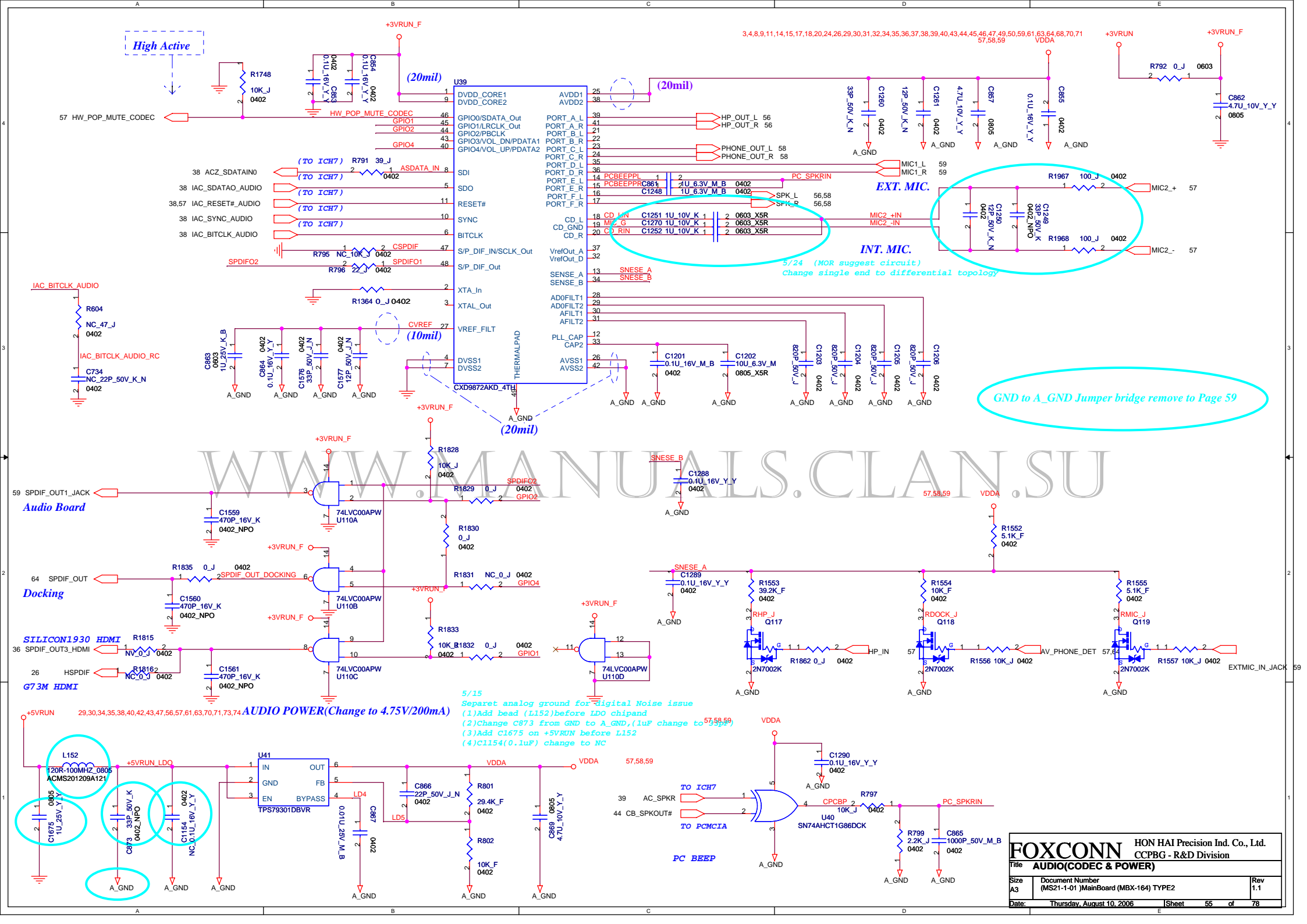


## IR Rreceiver connector



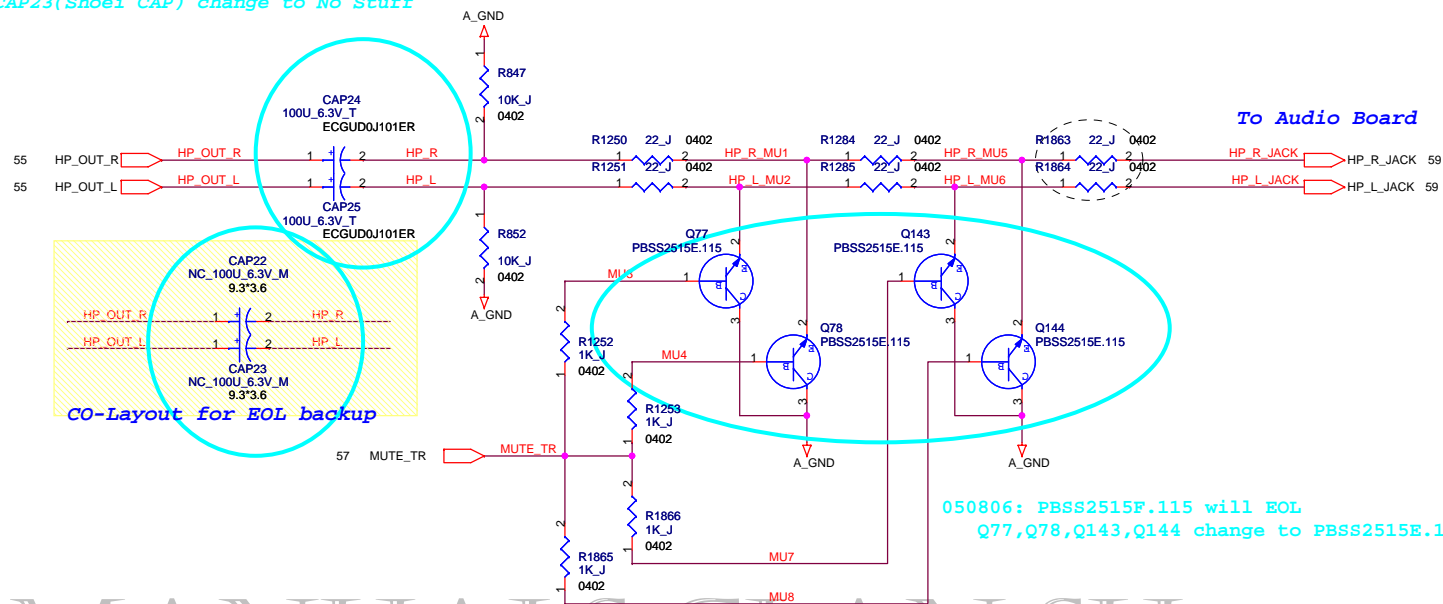
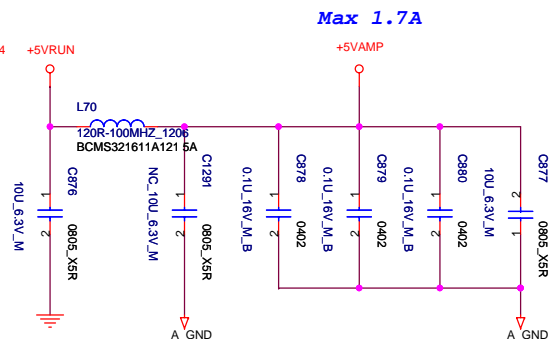
USB VCC F	1	TP847
USB PP3 F	1	tpc32t_100
USB PN3 F	1	TP848
	1	tpc32t_100
	1	TP849
	1	tpc32t_100
	1	TP850
	1	tpc32t_100
CIR_ALPS_3VPU	1	TP851
	1	tpc32t_100
SW_CIR00	1	TP852
	1	tpc32t_100
SW_CIR01	1	TP853
	1	tpc32t_100
SW_CIR02	1	TP854
	1	tpc32t_100
PWR_CIR#	1	TP855
	1	tpc32t_100
CIR_ALPS_SPWR	1	TP856
	1	tpc32t_100







```
050806: Shoei CAP will EOL
CAP24,CAP25(SP CAP) change to Stuff
CAP22,CAP23(Shoei CAP) change to No Stuff
```



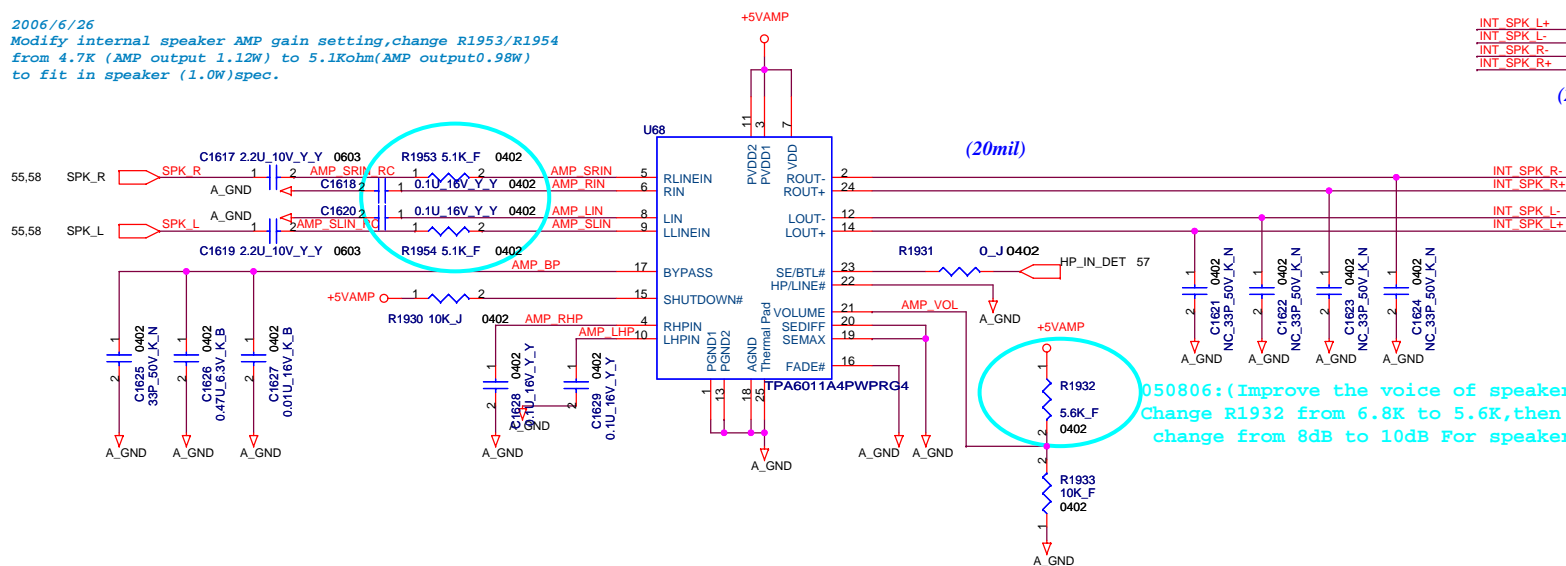
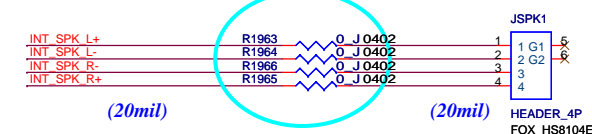
050806: PBSS2515F.115 will EOL  
Q77,Q78,Q143,Q144 change to PBSS2515E.115

WWW.MANUALS.CLANSII **INTERNAL SPEAKER**

050806:(Improve the voice of speaker up to 0.94W).  
Add damping Resistors R1953 on AMP\_STIN,R1954 on AMP\_SLIN  
then speaker amp output won't be distorted.  
For speaker loudness issue.

2006/6/26  
Modify internal speaker AMP gain setting,change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W) to fit in speaker (1.0W)spec.

```
050806:(Improve the voice of speaker up to 0.94W).
EMI team confirm whether
it is ok to use 0ohm resistor replacing bead
```



050806:(Improve the voice of speaker up to 0.94W).  
Change R1932 from 6.8K to 5.6K,then amp gain  
change from 8dB to 10dB For speaker loudness issue

*BFT Test Pad*

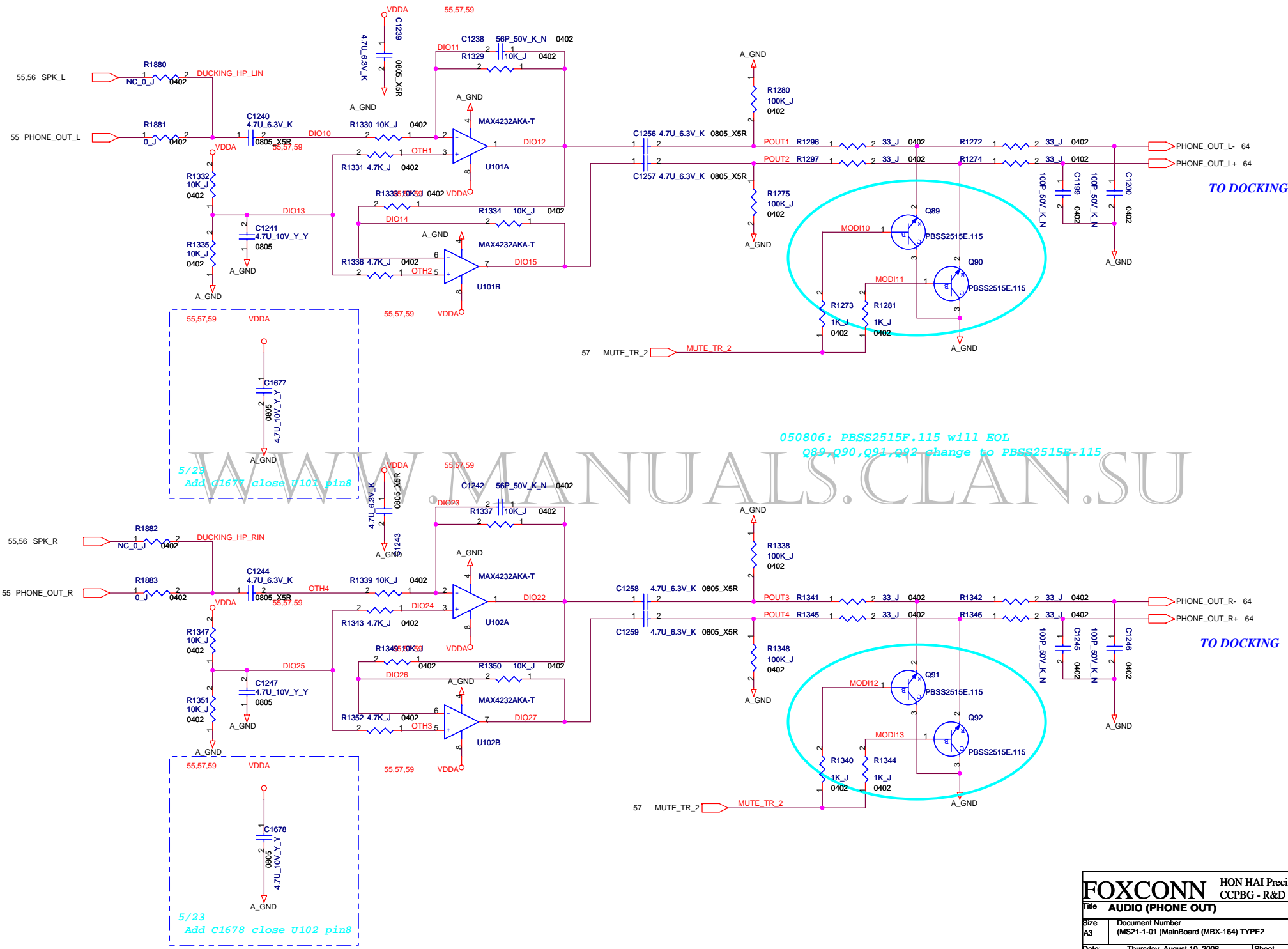
- |            |   |            |
|------------|---|------------|
| INT_SPK L+ | 1 | TP742      |
| INT_SPK L- | 1 | tpc32t_100 |
| INT_SPK R- | 1 | TP743      |
| INT_SPK R+ | 1 | tpc32t_100 |
| INT_SPK R- | 1 | TP744      |
| INT_SPK R+ | 1 | tpc32t_100 |
| INT_SPK R- | 1 | TP745      |
| INT_SPK R+ | 1 | tpc32t_100 |







# PHONE OUT

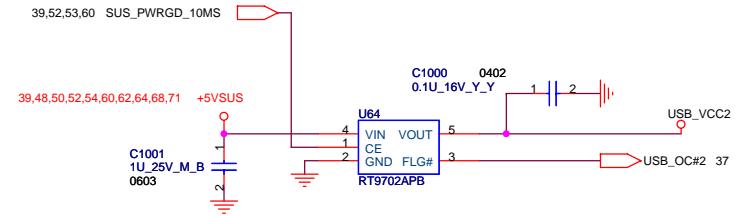
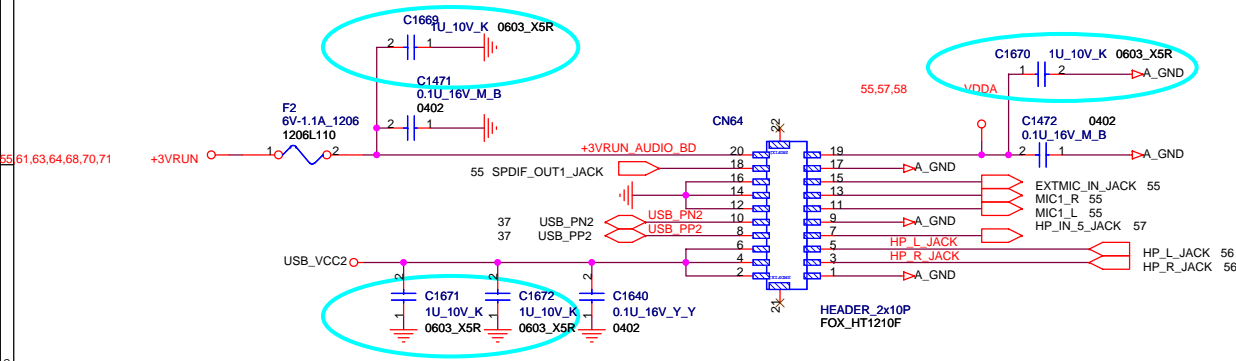




# Audio Board connector

050806: (To improve SNR issue)

Add 1uF capacitors close CN64 :C1671,C1672 on USB\_VCC2,  
C1669 on +3VRUN\_AUDIO\_BD, and C1670 on VDDA .



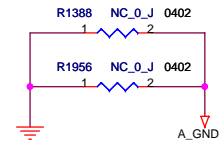
5/6

Separate analog ground for digital Noise issue:

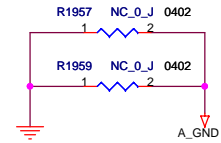
- (1) Remove GP3 (Close Jumper) not bridge between GND and A\_GND
- (2) Backup two jumper resistors for bridge between GND and A\_GND  
(C1388, C1966 on Screw hole H3, C1957, C1959 on screw hole H5)
- (3) Isolate screw hole H4, add 100pF capacitors C1673, C1674 for EMI, Zener diode D100 for ESD
- (4) Add jumper resistor for Return patch R1955 close L70 (+5VAMP) & R1958 close U41 (+3VRUN) & R1960 close codec.

Backup two jumper resistors for bridge between GND and A\_GND

Close screw hole H3

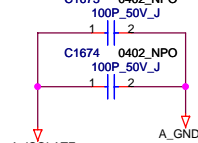


Close screw hole H5

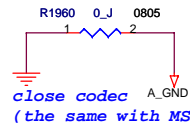
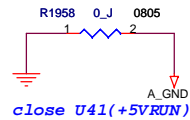
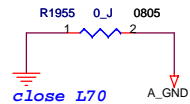


Isolate screw hole H4, and add EMI/ESD solution

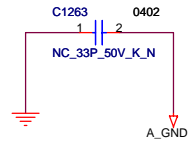
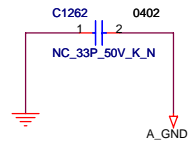
EMI



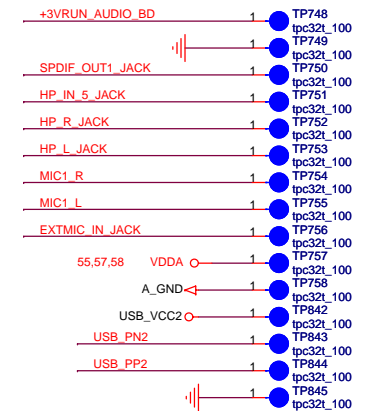
Add jumper resistor for Return patch



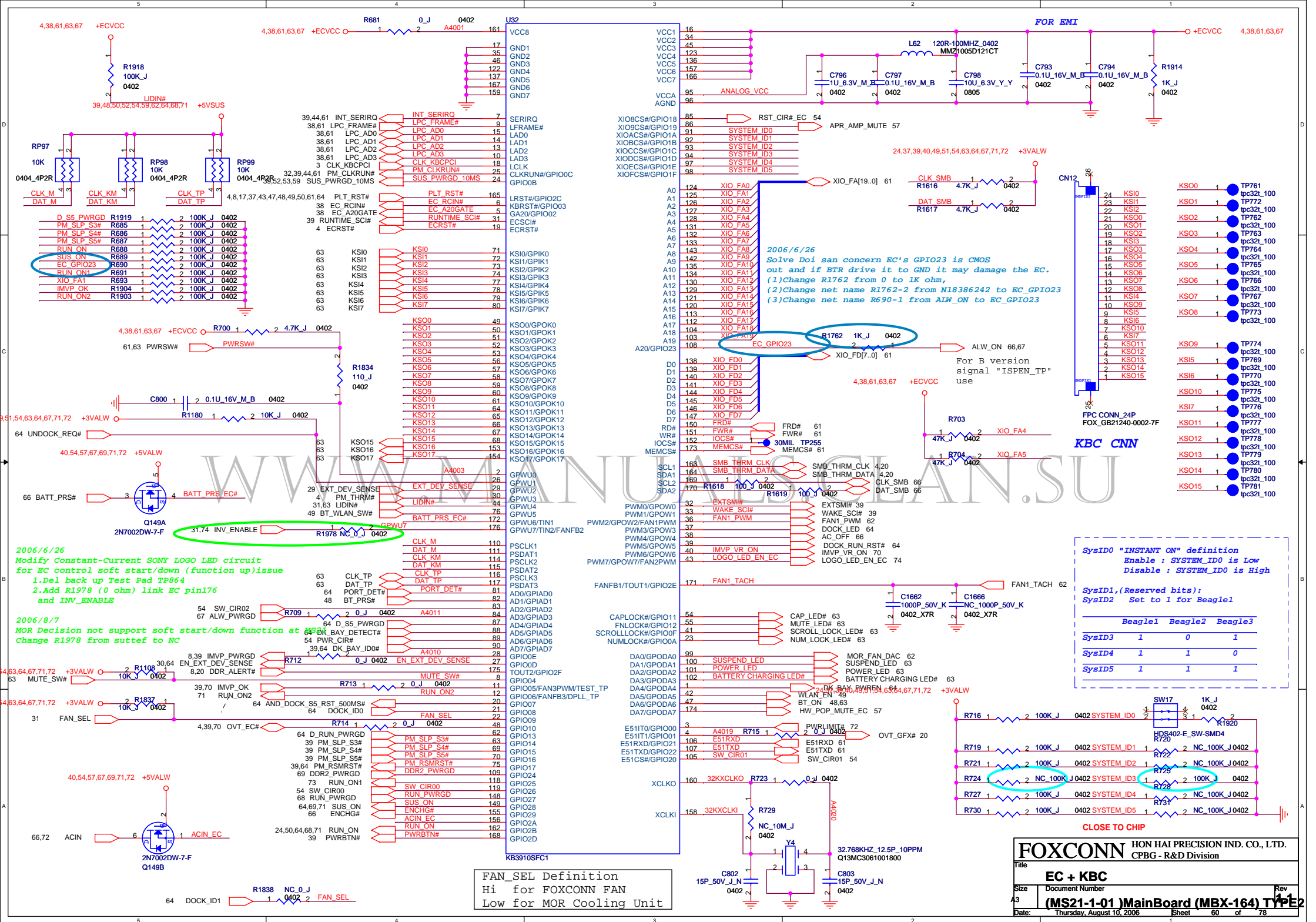
Original EMI back up solution to continue with MS20 (bridge between GND and A\_GND)



BFT Test Pad



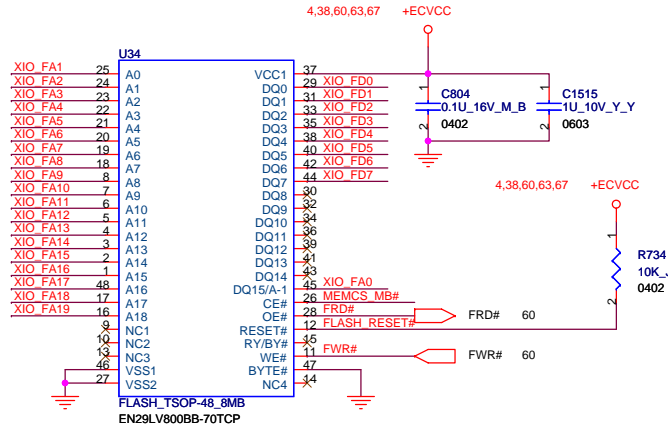




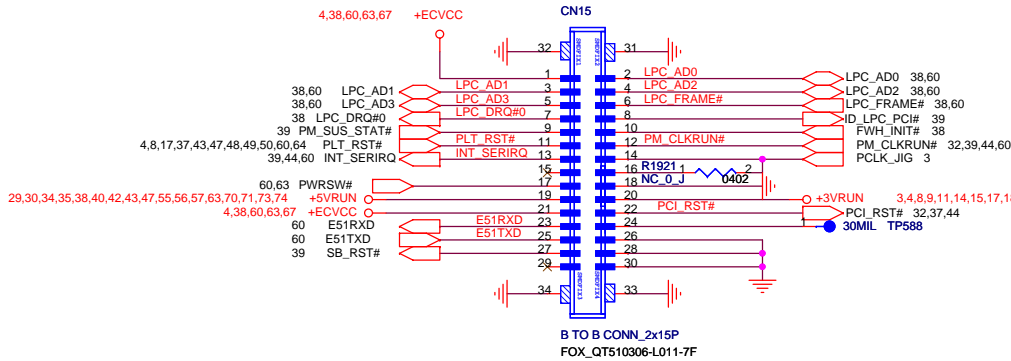


# FLASH BIOS

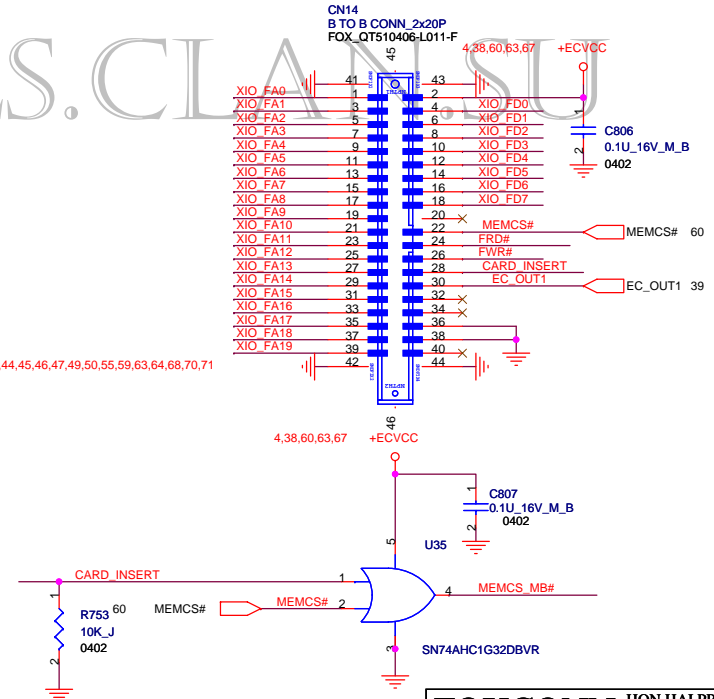
60 XIO\_FA[19..0]  
60 XIO\_FD[7..0]



# JIG-120

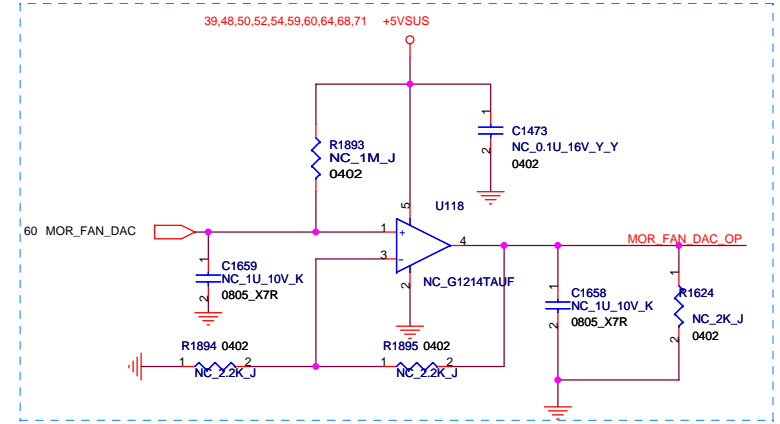
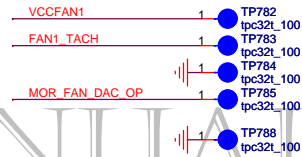
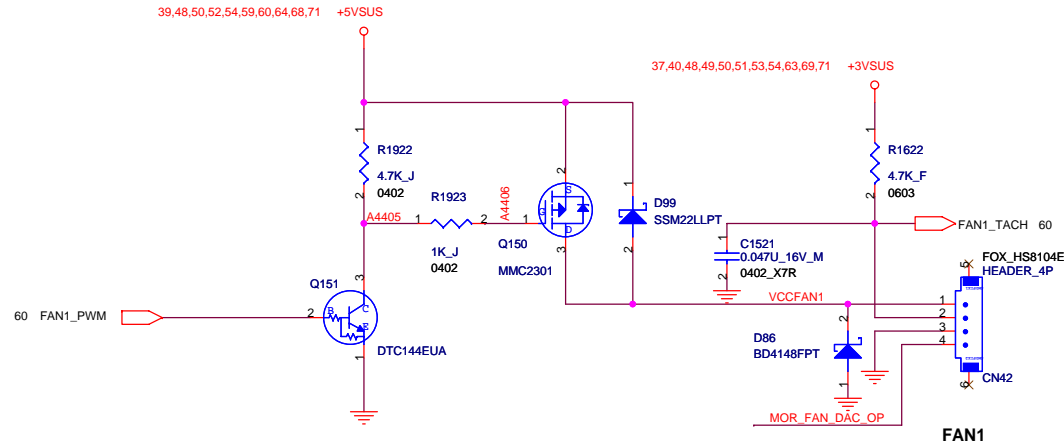


# X-BUS





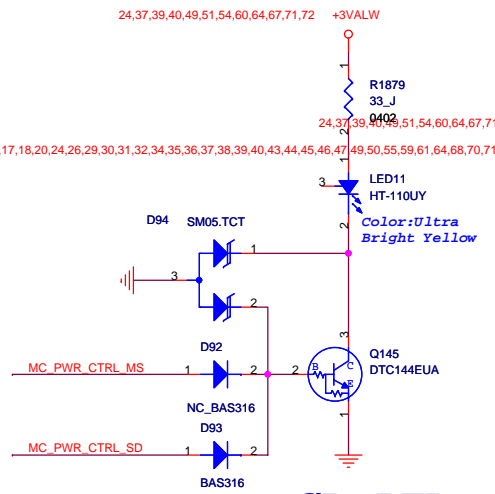
# FAN(FAN1+MOR FAN)



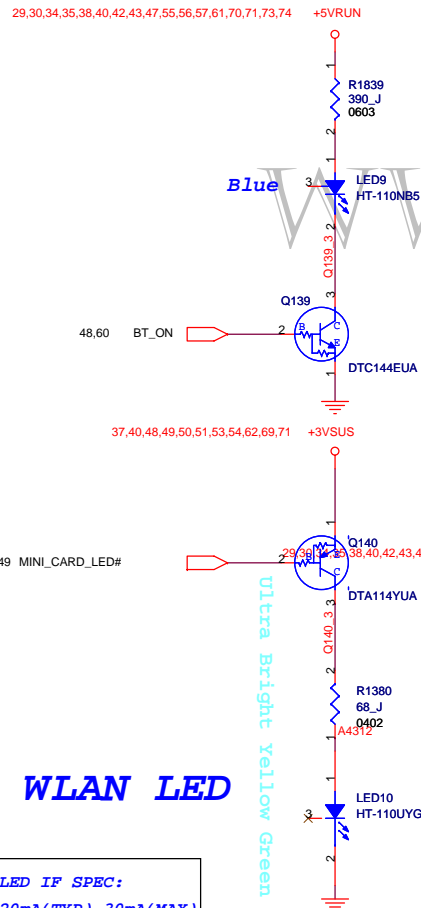
6/28 MOR fan circuit modify to backup  
(NC)U118  
(NC)R1893  
(NC)R1894  
(NC)R1895  
(NC)R1624  
(NC)C1473

WWW.MANUALS.CLAN.SU



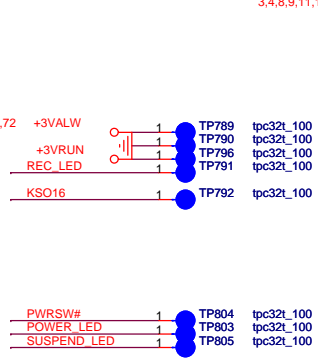


## SD LED BLUETOOTH LED

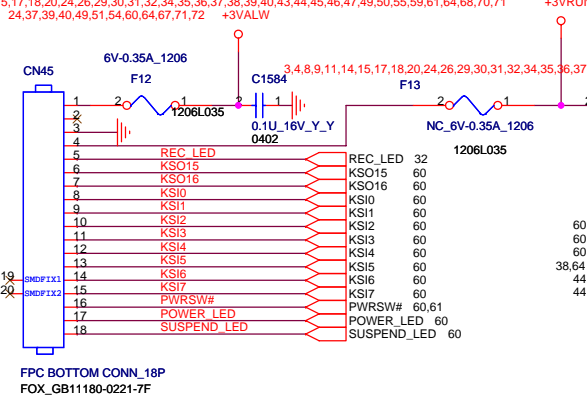


## WLAN LED

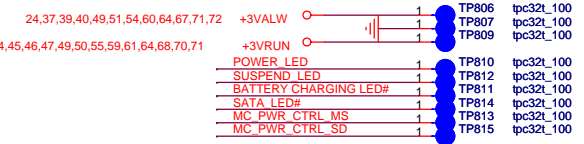
LED IF SPEC:  
20mA(TYP), 30mA(MAX)



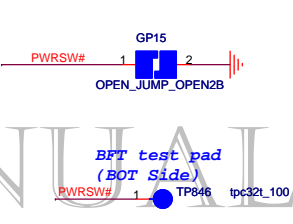
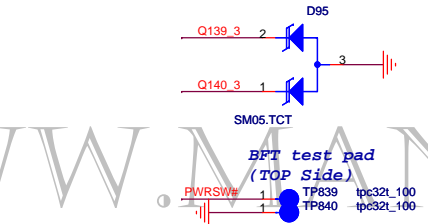
## To Power Button Board Connector



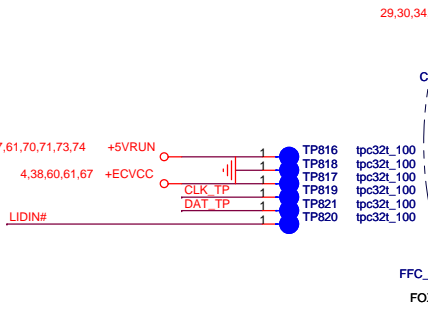
## To LED Board Connector



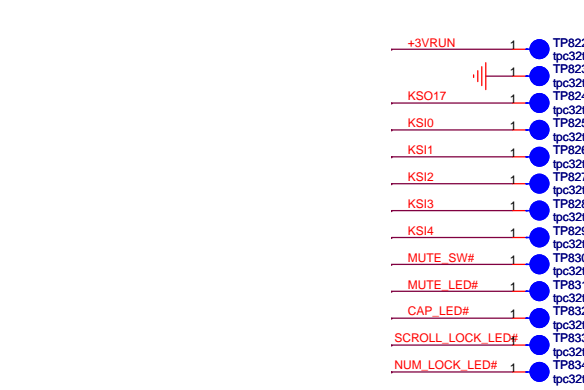
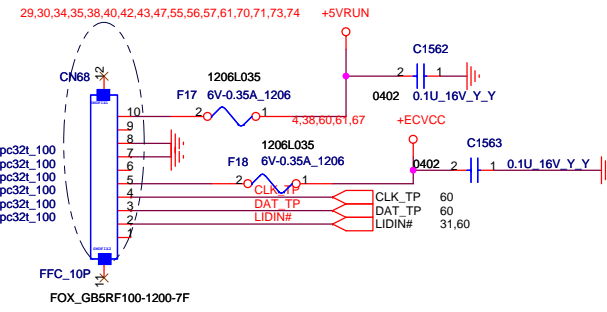
## To AV Function Board Connector



CN68 Change from MOLEX to FOXCONN By kain 0517

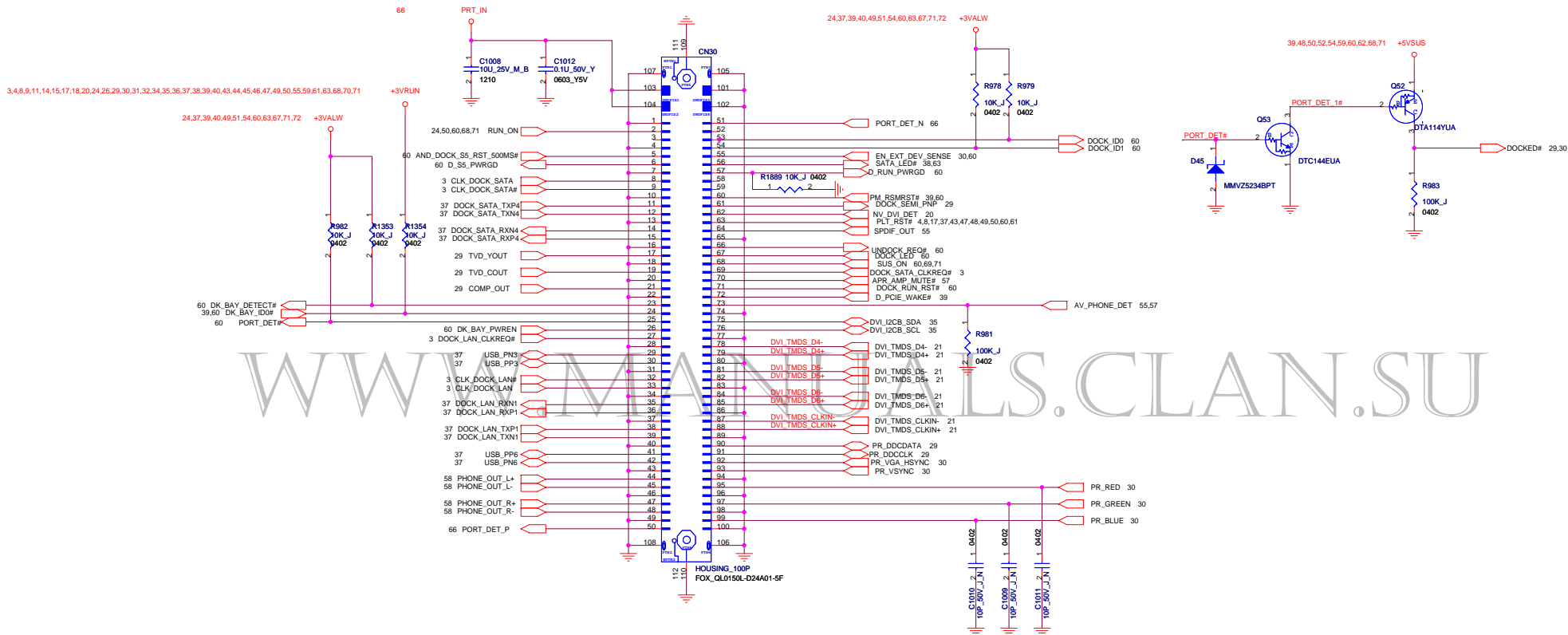


## To Touch Pad Board Connector

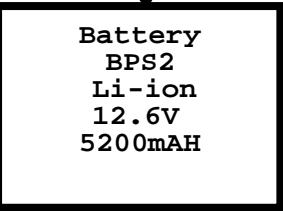
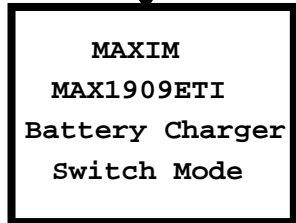
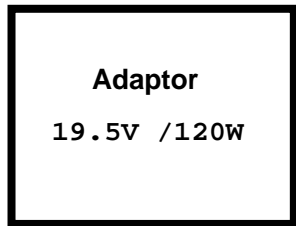


062606: Move Logo Led Circuit module to page 74.

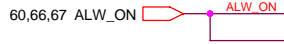
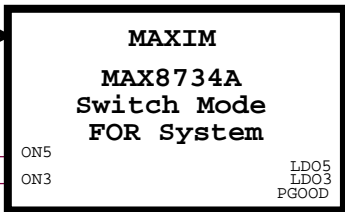






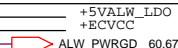


DCBATOUT

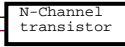


System  
+5VALW/9A

System  
+3VALW/8A

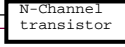


60,64,69,71 SUS\_ON



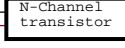
+5VSUS/3.1A

24,50,60,64,68,71 RUN\_ON



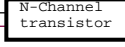
+5VRUN/4.5A

60,64,69,71 SUS\_ON



+3VSUS/1.5A

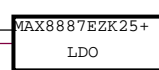
24,50,60,64,68,71 RUN\_ON



+3VRUN/7A

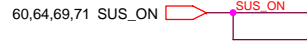
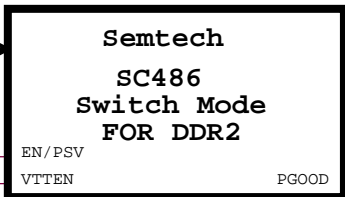
+3VSUS

24,50,60,64,68,71 RUN\_ON



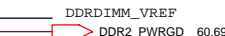
+2\_5VRUN/300mA

DCBATOUT

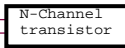


+1\_8VSUS/15.5A

+0\_9VSUS/2A

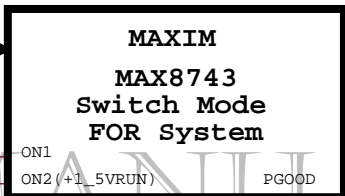


60,71 RUN\_ON2



+1\_8VRUN/6A

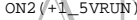
DCBATOUT



24,50,60,64,68,71 RUN\_ON



24,50,60,64,68,71 RUN\_ON



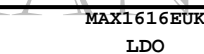
+1\_05VRUN/9.5A

+1\_5VRUN/7A

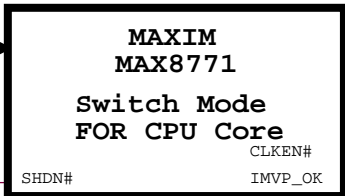


+8V For Load switch

60,64,69,71 SUS\_ON



DCBATOUT



60,70 IMVP\_VR\_ON

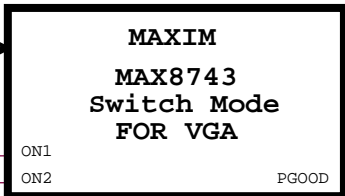


VHORE/44A

CLK\_EN# 3,70

IMVP\_OK 39,60,70

DCBATOUT



60,73 RUN\_ON1



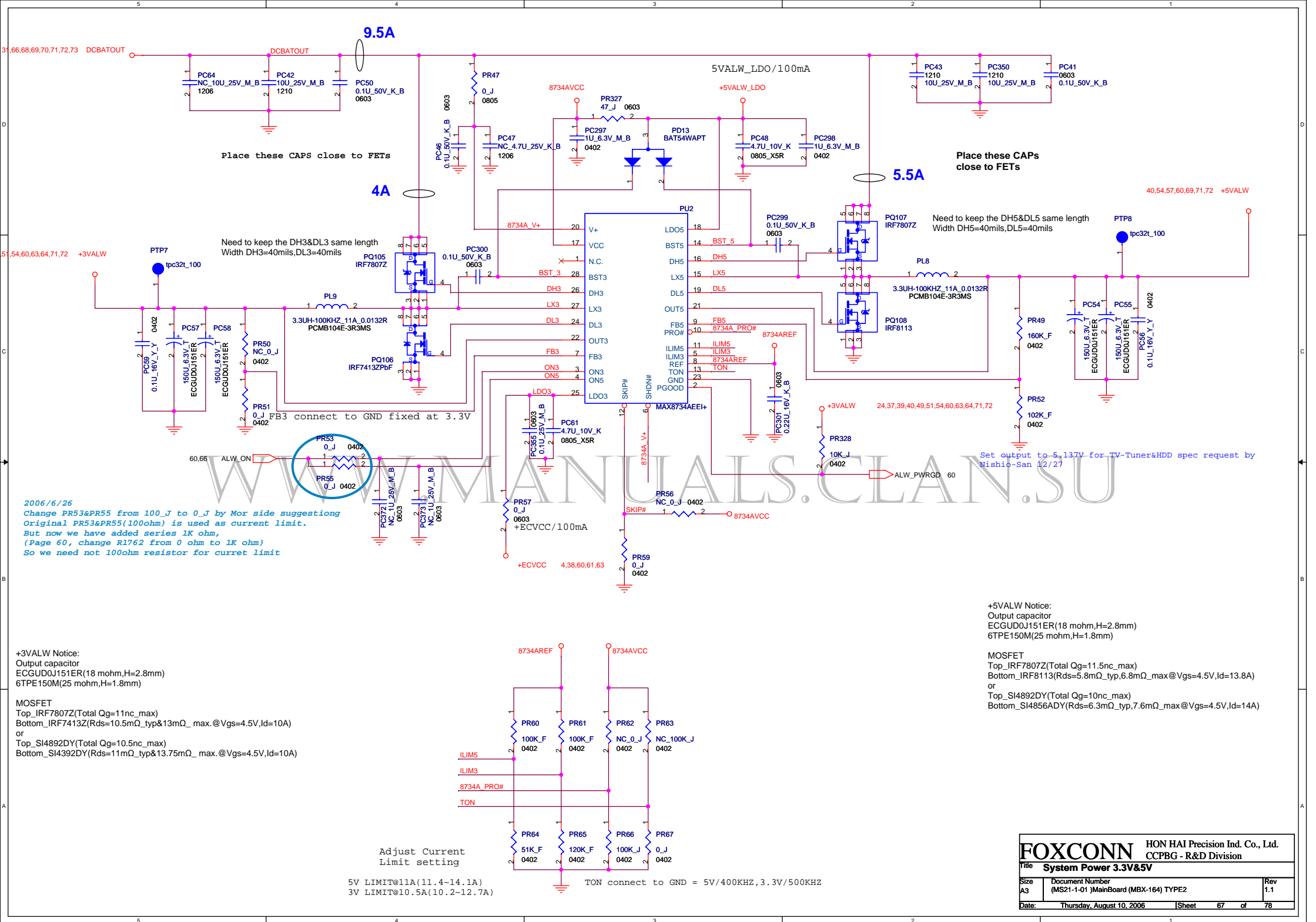
PEX\_VDD(1.2V)/2A

NV\_VDD(1.025V)/16.5A









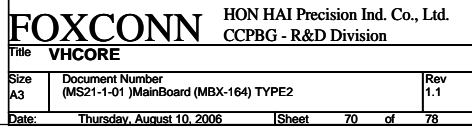








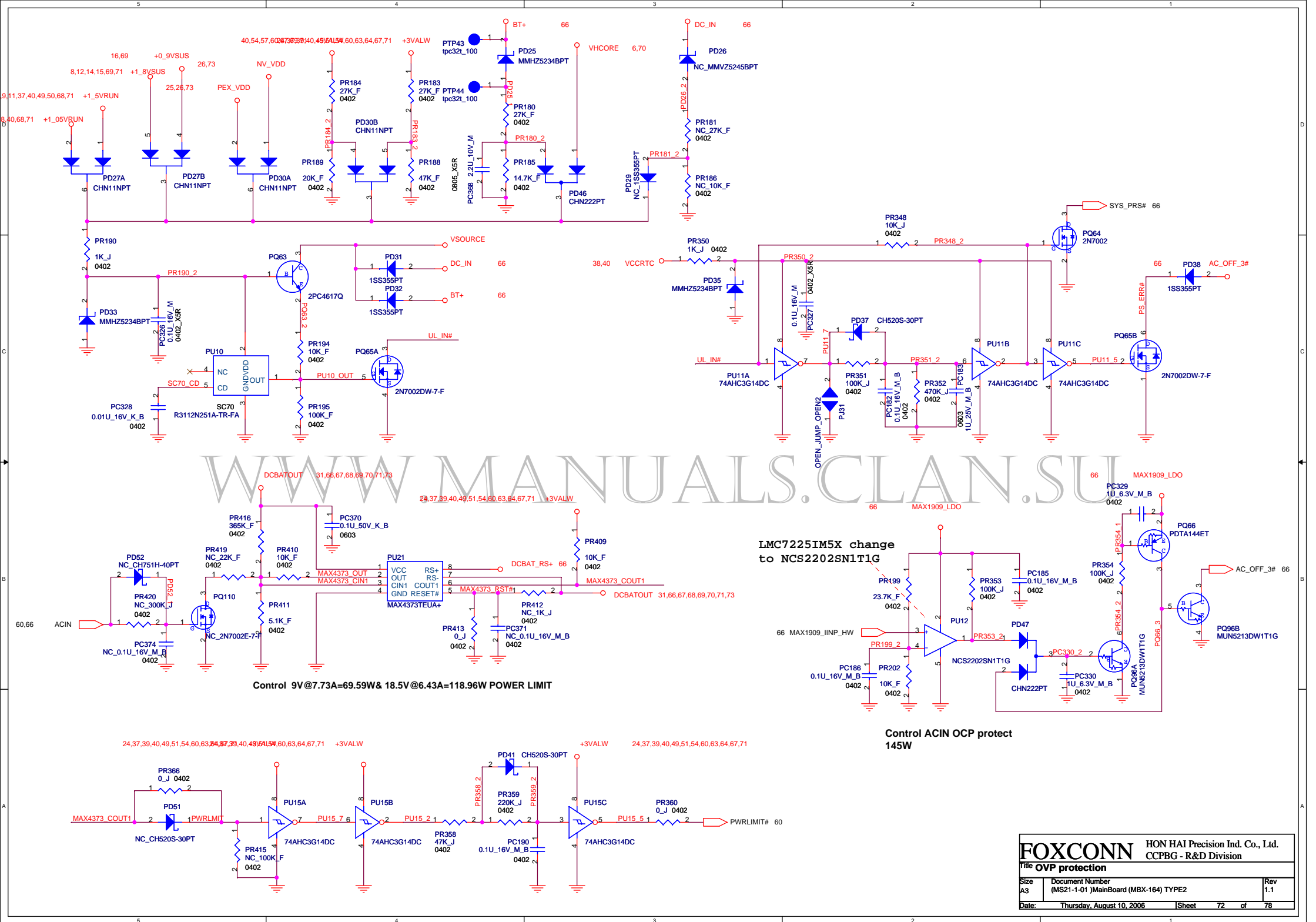














31,66,67,68,69,70,71,72 DCBATOUT

3A

Place these CAPS  
close to FETs

PL17

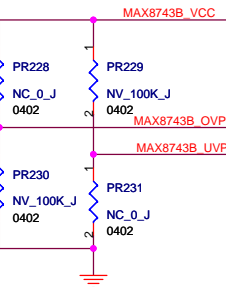
NV\_0.68UH-100KHZ\_28A\_0.025R  
PCMC133E-R68MF

(041006)

NV\_VDD on G73M-U power noise issue,  
change PR417 (PU16-FB2) from 2K to 2.1K  
(to setting NV\_VDD voltage on G73M-U from 1.2V to 1.21V)

NV\_VDD Notice:  
Output capacitor  
EEFUD0D471LG(ESR=9mohm,H=2.8mm,Arms=3.4A)  
2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET  
Top\_Si7392DP(Total Qg=15nc\_max)  
Bottom\_Si7336ADP(Rds=3.1mΩ\_typ,4 mΩ\_max@Vgs=4.5V,Id=19A)  
or  
Top\_NTMFS4707N(Total Qg=15nc\_max)  
Bottom\_NTMFS4119N(Rds=3.1mΩ\_typ,4.8 mΩ\_max@Vgs=4.5V,Id=25A)

PR361  
NV\_0\_J 0603

+5VRUN

29,30,34,35,38,40,42,43,47,55,56,57,61,63,70,71,74

1A

DCBATOUT 31,66,67,68,69,70,71,72

Place these CAPS  
close to FETs

25,26,72 PEX\_VDD

Need to keep the  
1\_2V\_DH & 1\_2V\_DL same length  
Width DH1=40mils,DL=40mils

Adjust Current  
Limit setting

1\_2V LIMIT@2.8A(2.7~3.2A)  
1\_025V LIMIT@22A(20.5~25.7A)

PEX\_VDD Notice:  
Output capacitor  
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)  
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)  
SI4914DY(Rds=22mΩ\_typ,27mΩ\_max@Vgs=4.5V,Id=6.4A)

FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title	+1_2VRUN&+1_025VRUN	
Size	Document Number	Rev
A3	(MS21-1-01) MainBoard (MBX-164) TYPE2	1.1
Date:	Thursday, August 10, 2006	Sheet 73 of 78



2006/6/26

Modify Constant-Current SONY LOGO LED circuit

for U138 cost issue

- 1.Back up:U138(MAX1916EZT),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)
  - 2.Remove back up solution U139(GMT,G5920TB1UF),C1660(0.1u)
  - 3.Add new Constant-Current circuit (OP + MOS)
- 51K ohm: R1972 ,  
 1.2K ohm: R1973 ,  
 1k ohm:R1974 ,  
 10 ohm: R1975  
 (NC)0 ohm: R1976(for back up U138 MAX1916)  
 0.1uF,16V: C1679  
 (NC)22uF,6.3V: C1680  
 OP LM358 ADR : U139  
 N-MOS 2N7002: Q158  
 N-MOS DTA114YUA:Q159  
 P-MOS DTC144EUA:Q160

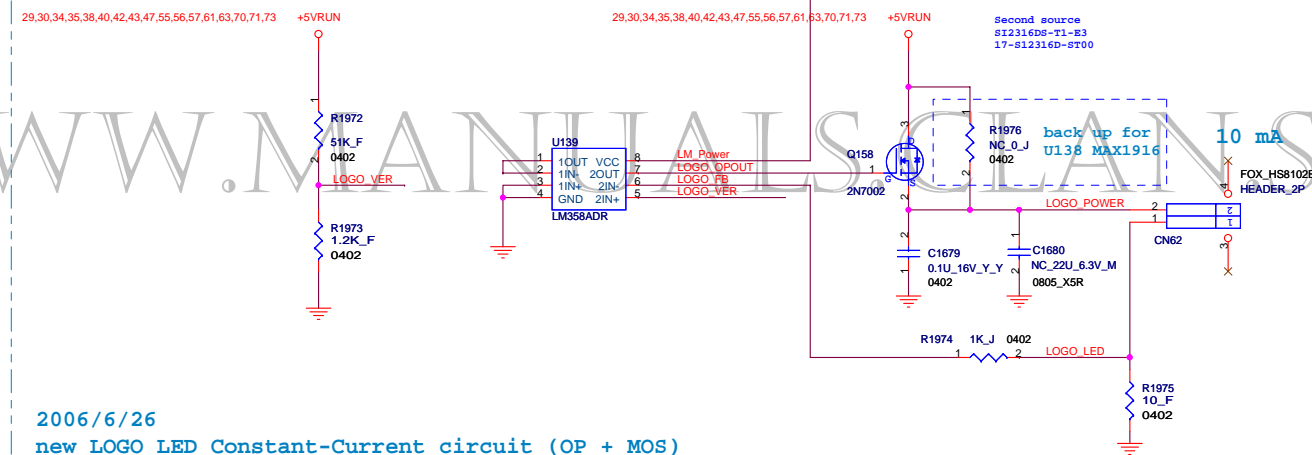
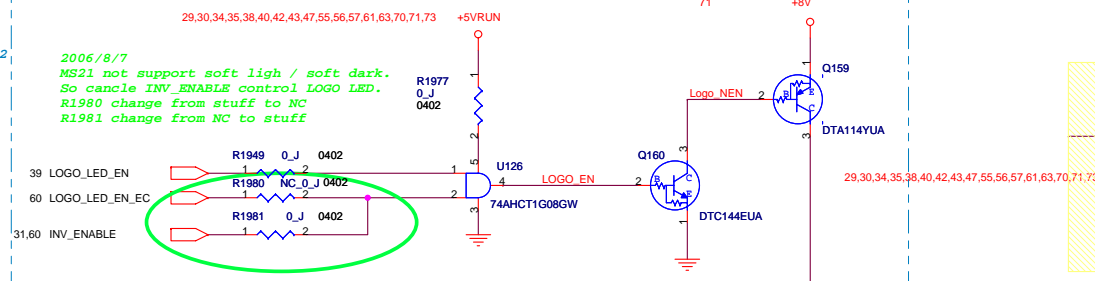
for EC control soft start/down (function up)issue

- 1.Del R1948(back up LOGO\_LED\_EN\_EC to U126 pin1)
- 2.Serial (Back up) R1981 between INV\_ENABLE to U126 pin2
- 3.Move net LOGO\_LED\_EN\_EC from R1948 pin1 to R1980 pin1
- 4.Add R1977 between +5VRUN to U126 pin5(VCC)
- 5.Add R1980 between Logo\_led\_en\_ec to U126 pin2

## Constant-Current SONY LOGO LED

2006/6/26

EC &amp; SB control soft start/down



2006/6/26  
 (1)remove TP835(GND Test Pad)  
 (2)add TP857(LOGO\_POWER)

2006/6/26

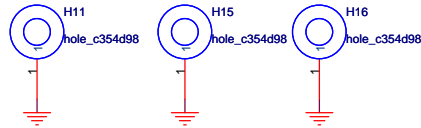
(Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP)  
 Detail location

10U\_25V\_M\*9pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),  
 0.01U\_25V\_K\*1pcs(PC387),1U\_25V\_M\*1pcs(PC388),0.22U\_16V\_M\*1pcs(PC391),  
 220P\_50V\_K\*1pcs(PC392),SKS30-04AT-G\*1pcs(PD53),8UH-100KHZ\_2.5A\_0.07R\*1pcs(PL22),  
 2N7002\*2pcs(PQ9114,PQ116),FDS6680A\*1pcs(PQ117),120K\_F\*1pcs(PR432),  
 0.03\_F\*1pcs(PR434)95.3K\_F\*1pcs(PR435),10K\_F\*1pcs(PR436),MAX668EUB+T\*1pcs(PU22),



# HOLE

## Type 1



## Type 2

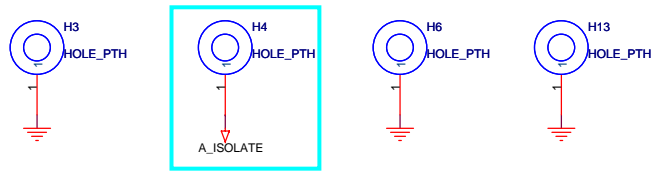
2005/10/24  
Remove Screw Hole H2 P/N 1X-HOLE000-0108  
because the Hole overlay with CN32 and layout will  
modify component screw shipe

## Type 3

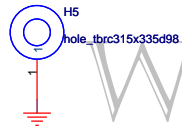
2005/10/24  
Remove Screw Hole H1 P/N 1X-HOLE000-0110  
because the Hole overlay with CN32 and layout will  
modify component screw shipe

2006/5/6  
Separet analog ground for digital Noise issue:  
Isolate screw hole H4 Change H4 net name from  
A\_GND to A\_ISOLATE

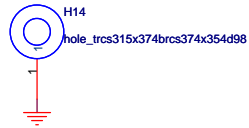
## Type 4



## Type 5



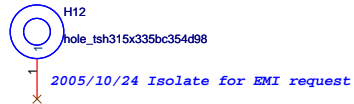
## Type 6



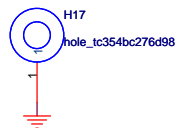
## Type 7



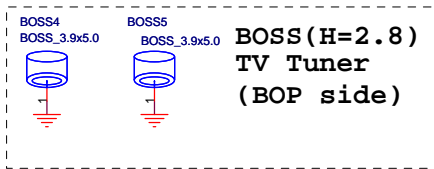
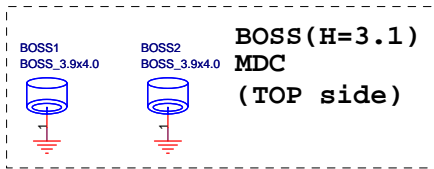
## Type 8



## Type 9



## Type CPU



## Type NPTH Guide (spherical)HOLD



## Type NPTH Guide (oval-shaped)HOLD





MS20 MP to MS21 DVT Change History

(2006/5/23)

- (川) 01.(Page08) Remove R110 for PM\_EXTTS#1 back up pull up res.ICH7 (DPRSLPVR)already have internal pull up
- (川) 02.(Page14) Remove backup DIMM thermal senser Change R168 from stuff to NC(basis on MS20 MP ECR)
- (川) 03.(Page15) Remove backup DIMM thermal senser Change R1627 from stuff to NC(basis on MS20 MP ECR)
- (蘭) 04.(Page34) US Silicon Image ATC test HDMI DDC capacitance fail(>50pF)change U128 no stuff Basis on MS20 MP ECR add back up res.(R1962)no stuff for U128 VCC
- (才) 05.(Page39) Delete U30,R1183,R649 (backup circuit)
- (賣) 06.(Page42) For power droup cause 0.16V voltage loss Issue(1)F7,F8,F19,F20 no stuff(2)Co-layout GP17-GP20 with fuse
- (業) 07.(Page55) Separet analog ground for digital Noise issue  
(1)Add bead (L152)before LDO chipand  
(2)Change C873 from GND to A\_GND  
(3)Add C1675 on +5VRUN before L152
- (業) 08.(Page56) Shoei CAP will EOL. CAP24,CAP25(SP CAP) change to Stuff: CAP22,CAP23(Shoei CAP) change to No Stuff
- (業) 09.(Page56) PBSS2515F.115 will EOL ,Q77,Q78,Q143,Q144 change to PBSS2515E.115
- (業) 10.(Page56) Improve the voice of speaker up to 0.94W  
(1)Add damping Resistors R1953 on SRIN,R1954 on AMP\_SLIN then speaker amp output won't be distorted.  
(2)Change R1932 from 6.8K to 5.6K, then amp gain change from 8dB to 10dB.
- (業) 11.(Page57) PBSS2515F.115 will EOL Q89,Q90,Q91,Q92 change to PBSS2515E.115
- (業) 12.(Page59) Improve SNR issue,Add 1uF capacitors close CN64 :C1671,C1672 on USB\_VCC2,C1669 on +3VRUN\_AUDIO\_BD, and C1670 on VDDA .
- (業) 13.(Page59) Separet analog ground for digital Noise issue:  
(1)Remove GP3 (Close Jumper)not bridge between GND and A\_GND  
(2)Backup two jumper resistors for bridge between GND and A\_GND (C1388,C1966 on Screw hole H3,C1957,C1959 on screw hole H5)  
(3)Isolate screw hole H4,add 100pF capacitors C1673,C1674 for EMI,Zener diode D100 for ESD  
(4)Add jumper resistor for Return patch R1955 close L70(+5VAMP) & R1958 close U41(+5VRUN) & R1960 close codec
- (才) 14.(Page39) Remove back up circuit LVDS GPIO on U29 pinU2(1)Add Test Pad TP890 on GPIO34(2)Del Q126
- (賣) 15.(Page54) Remove back up F6 power source from +3VALW (Del)R1944,R1946
- (青) 16.(Page67) Reserve PC64(10U\_25V\_M\_B 1206) for 1210 size shortage. Change PR57 from 0805 size to 0603 size for 0603 size rated current is also enough.
- (青) 17.(Page70) Add PC375 (0.1uF) to avoid IMVP\_OK signal 700mV pulse when power on. Change PC107/PC108 from 2.2u\_16V\_M to 2.2u\_10V\_M for 2.2u\_16V\_M shortage.
- (青) 18.(Page71) Change PC164/PC165 from 2.2u\_16V\_M to 2.2u\_10V\_M for 2.2u\_16V\_M shortage.
- (青) 19.(Page71) Change PC368 from 2.2u\_16V\_M to 2.2u\_10V\_M for 2.2u\_16V\_M shortage. Change PU12 from LMC7225IM5X to NCS2202SNI1TG1 for LMC7225IM5X shortage.
- (才) 20.(Page60) Modify system ID setting. R725 from stuff change to NC,R726 from NC change to stuff
- (蘭) 21.(Page32) CN66,CN67 Change from MOLEX(IN-0010000-MWG0) to FOXCONN(IN-0010000-F0T0)
- (賣) 22.(Page63) CN68 Change from MOLEX(IN-0010000-MWG0) to FOXCONN(IN-0010000-F0T0)
- (業) 23.(Page57) Add C1676 (4.7 uF/bupass cap) close A\_ U99 pin8
- (業) 24.(Page58) Add C1677,C1678 (4.7 uF/bupass cap) close A\_ U101,U102 pin8
- (青) 25.(Page74) Add Inverter Boost Circuit

(2006/5/24)

- (業) 1.(Page55) According to MOR suggest Change Int MIC topology from single end to differential  
(1) C1251 change from 33pF 0402 to 1uF 0603  
(2) C1252 change from 12pF 0402 to 1uF 0603  
(3) C1270 change from 0.1F 0402 to 1uF 0603  
(4) Add R1967, R1968 100 ohm 0402
- 2.(Page57) According to MOR suggest Change Int MIC topology from single end to differential  
(1) C1231 change from 4.7uF 0805 to 220pF 0402  
(2) C1232 change from 1uF 0805 to 4.7uF 0805  
(3) C1233 change from 4.7uF 0805 to NC\_33pF 0402  
(4) C1234 change from 100pF 0402 to NC\_33pF 0402  
(5) C1237 change from 100pF 0402 to 33pF 0402  
(6) R1318 change from 10Kohm 0402 to 5.1Kohm 0402  
(7) R1319 change from 1Kohm 0402 to 4.7Kohm 0402  
(8) R1320 change from 33ohm 0402 to 100ohm 0402  
(9) R1321 change from NC\_0ohm 0402 to 4.7Kohm 0402  
(10) R1325 change from 47Kohm 0402 to 4.7Kohm 0402  
(11) R1326 change from 7.5Kohm 0402 to 2.2Kohm 0402  
(12) R1327 change from 100ohm 0402 to 1Kohm 0402  
(13) Add R1970, R1971 100 ohm 0402  
(14) Add R1969 4.7 Kohm 0402  
(15) R1236 change from 4.7u to 1u

(2006/5/26)

- (業) (1) C1230 change from 2200pF to 4700 pF by MOR request

MS21 DVT to MS21 PVT Change History

(2006/6/26)

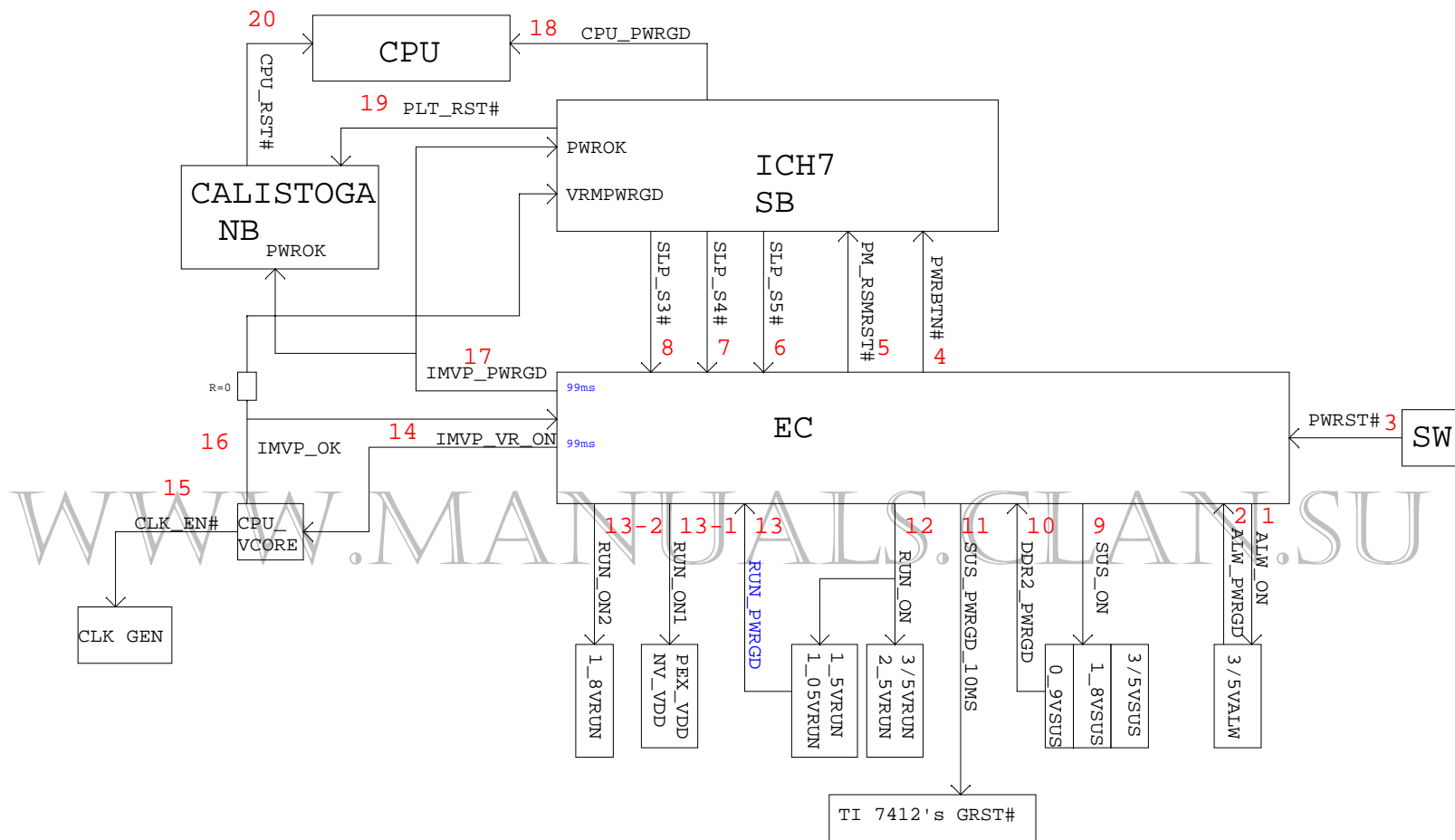
- (才) 01.(Page60) Solve Doi san concern EC's GPIO23 is CMOS out and if BTR drive it to GND it may damage the EC.  
(1)Change R1762 from 0 to 1K ohm,  
(2)Change net name R1762-2 from N18386242 to EC\_GPIO23  
(3)Change net name R690-1 from ALW\_ON to EC\_GPIO23
- (蘭) 02.(Page31) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP  
(1)Delete PR426&PR427  
(2)change C604-1,C1557-1,C1558-1,CN49 pin1,pin2 net name INVERTER\_VCC to net DCBATOUT.
- (賣) 03.(Page74) Del inverter boost circuit , after change ,the inverter circuit is the same with MS20 MP  
Delete 10U\_25V\_M\*1pcs(PC380,PC381,PC382,PC383,PC384,PC385,PC386,PC389,PC390),  
0.01U\_25V\_K\*1pcs (PC387),1U\_25V\_M\*1pcs(PC388),0.22U\_16V\_M\*1pcs(PC391),  
220P\_50V\_K\*1pcs(PC392),SKS30-04AT-G\*1pcs(PD53),8UH-100KH2\_2.5A\_0.07R\*1pcs(PL22),  
2H7002\*2pcs(PQ114,PQ116),FDS6680A\*1pcs(PQ117),120K\_F\*1pcs(PR432),  
0.03\_F\*1pcs(PR434)95.3K\_F\*1pcs(PR435),10K\_F\*1pcs(PR436),MAX668EUB+T\*1pcs(PU22),  
100K\_J\*1pcs (PR428) 100K\_J\*1pcs (PR429)
- (青) 04.(Page67)Change PR53&PR55 from 100\_J to 0\_J by Mor side suggestion  
Original PR53&PR55(100ohm) is used as current limit.But now we have added series 1K ohm,  
(Page 60, change R1762 from 0 ohm to 1K ohm) So we need not 100ohm resistor for curret limit
- (業) 05.(Page56) Modify internal speaker AMP gain setting,change R1953/R1954 from 4.7K (AMP output 1.12W) to 5.1Kohm(AMP output0.98W) to fit in speaker (1.0W)spec.
- (業) 06.(Page57) Modify internal MIC AMP gain setting,change R1318 from 5.1K to 5.9K ohm, To lead TYPE2 board gain (differential type MIC)the same with TYPE1 board single end MIC) (Gain=9.2)
- (才) 07.(Page60) Modify Constant-Current SONY LOGO LED circuit for EC control soft start/down (function up)issue  
(1).Del back up Test Pad TP864  
(2).Add R1978 (0 ohm) link EC pin176 and INV\_ENABLE
- (賣) 08.(Page74) Modify Constant-Current SONY LOGO LED circuit  
A.for U138 cost issue  
1.Back up:U138(MAXI1916E2T),R1936 (91K ohm,0402),R1982(0R,NC),R1983(0R,NC)  
2.Remove back up solution U139(GMT,G5920TBIUF),C1660(0.1u)  
3.Add new Constant-Current resistor circuit (OP + MOS)  
51K ohm: R1972 ,  
1.2K ohm: R1973 ,  
1k ohm:R1974  
10 ohm: R1975  
(NC)0 ohm: R1976(for back up U138 MAXI1916)  
0.1uF,16V: C1679  
(NC)22uF,6.3V: C1680  
OP 1258 ADR : U139  
N-MOS 2N7002: Q158  
N-MOS DTA114YUA:Q159  
P-MOS DTC144SUA:Q160  
B.for EC control soft start/down (function up)issue  
1.Del R1948(back up LOGO\_LED\_EN\_EC to U126 pin1)  
2.Serial (Back up) R1981 between INV\_ENABLE to U126 pin2  
3.Move net LOGO\_LED\_EN\_EC from R1948 pin1 to R1980 pin1  
4.Add R1977 between +5VRUN to U126 pin5(VCC)  
5.Add R1980 between Logo\_led\_en\_ec to U126 pin2
- (賣) 09.(Page 42) Delete SATA HDD Fuse backup circuit  
(1)Remove F7,F8,F19,F20 Pad  
(2)Remove GP17-GP18 open gap
- (才) 10. (Page 62) MOR fan circuit modify to backup  
(NC)U118 (NC)R1893  
(NC)R1624 (NC)C1473  
(NC)R1894 (NC)R1895

MS21 PVT to MS21 MP Change History

- (賣) 01.(Page74) MS21 not support soft ligh / soft dark. So cancle INV\_ENABLE control LOGO LED.  
R1980 change from stuff to NC  
R1981 change from NC to stuff
- (才) 02.(Page60) MS21 not support soft ligh / soft dark. So cancle INV\_ENABLE control LOGO LED.  
R1978 Change from stuff to NC
- (業) 03.(Page57) Change C1676 from stuff to NC for MOR suggestion Cost down request.
- (青) 04.(Page66) At MS21 PCN1 used FOXCONN connector, Change PCN1 Vendor from molex to NWING
- (良) 05.(Page29) Change D60,D61,D81 Value from NV to Normal
- (良) 06.(Page20) Change Y2 Value from Normal to NV

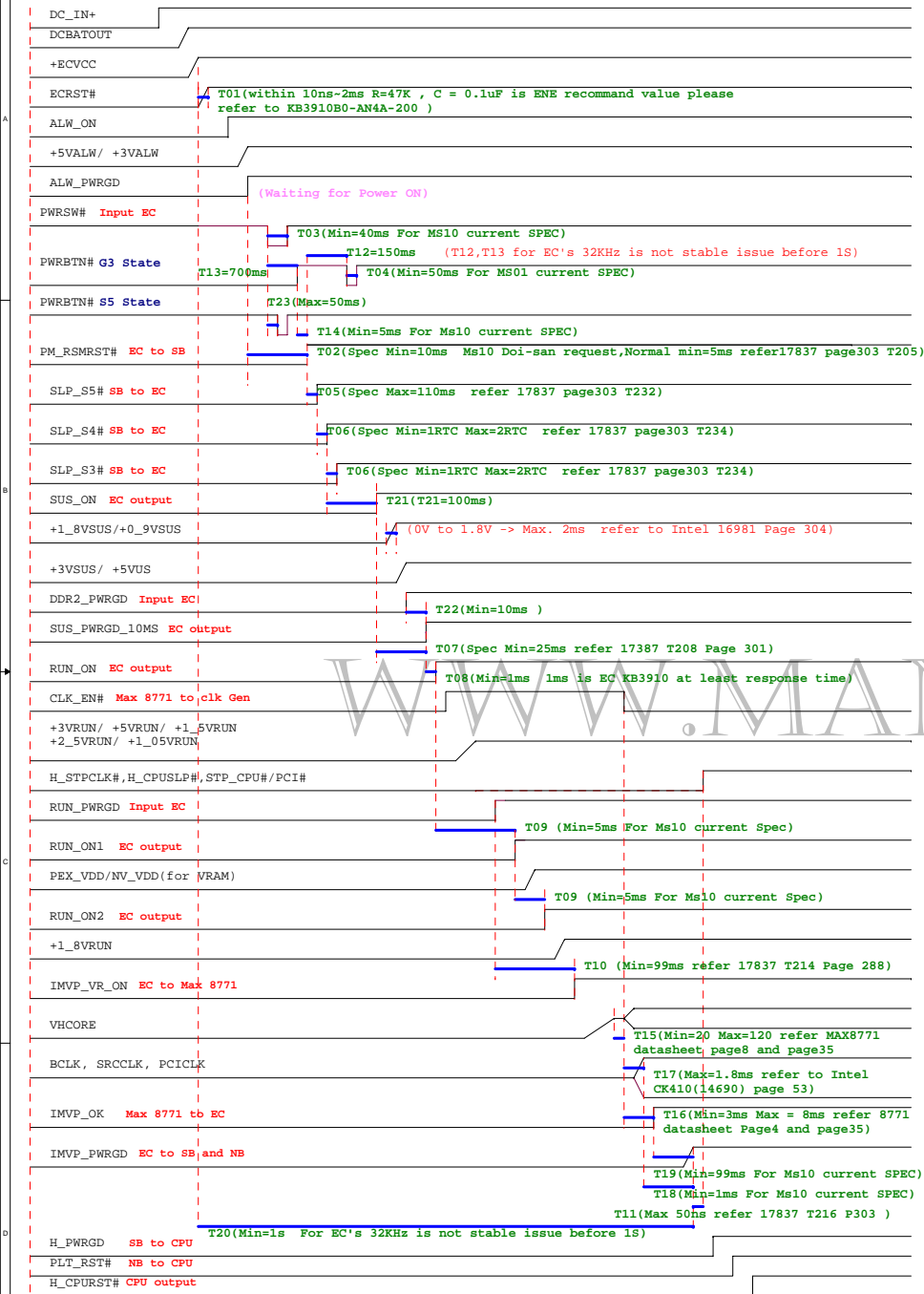


# MS21 Power On Sequence Block Diagram

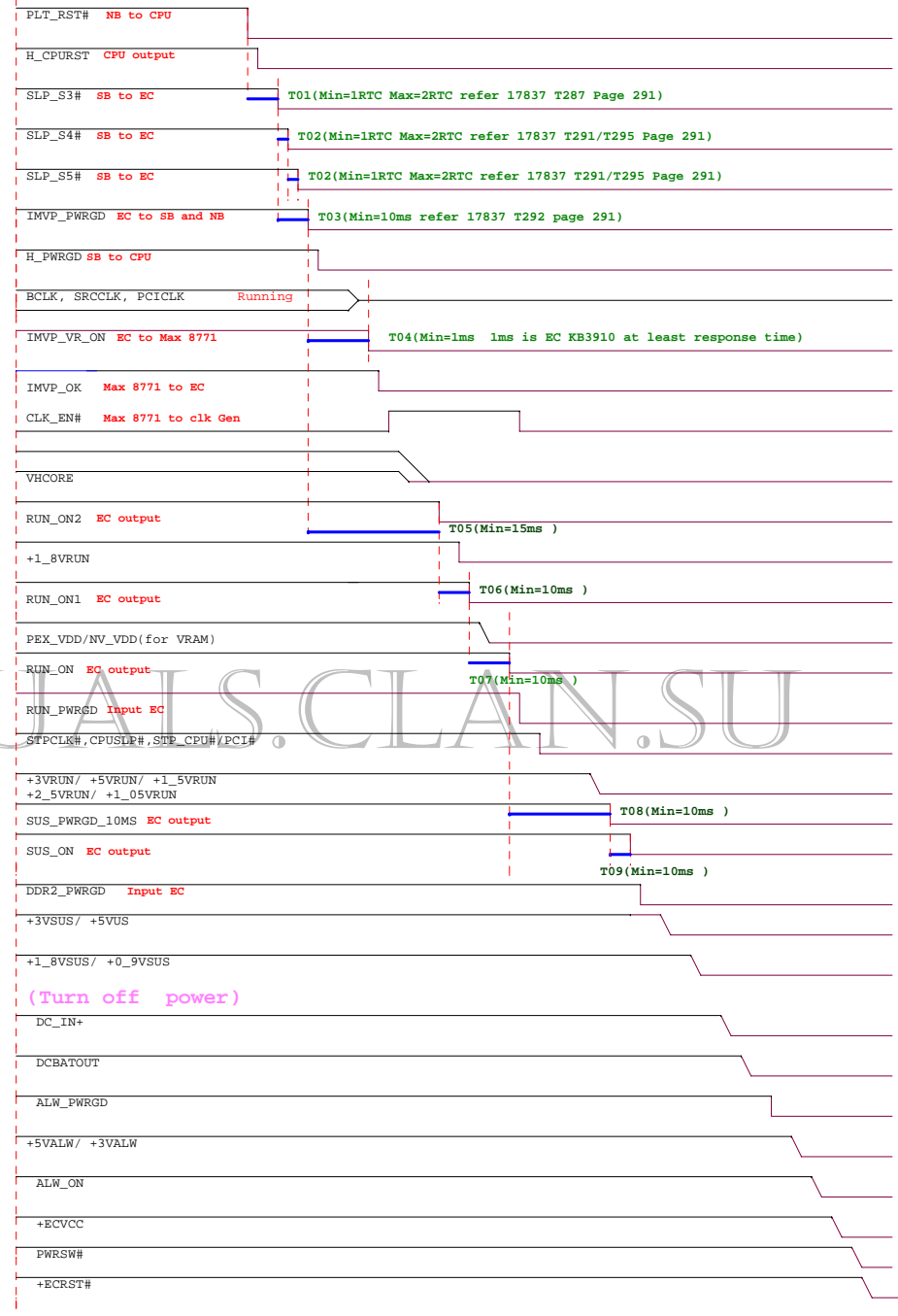




# Power On/Off Sequence Specification



T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	
within 10ns-2ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCLK	Min. 25 ms	Min. 1ms	Min. 10ms	Min. 99ms	Max. 50ms	
T12	T13	T14	T15	T16	T17	T18	T19	T20	T21	T22	T23
Min. 150ms	Min 700ms	Min 5ms	Min : 20us Max : 120us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min. 99ms	Min. 1s	100ms	Min. 10ms	Max 50ms



T01	T02	T03	T04	T05	T06	T07	T08	T09
1 - 2 RTCLK	1 - 2 RTCLK	Min. 10ms	Min. 1ms	Min. 15ms	Min. 10ms	Min. 10ms	Min. 10ms	Min. 10ms