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BOM Control Table

Value / Prefix	CA_	AT_	DS_	ND_	LND_	HD_
UMA (W/ Dock)	V		V			
UMA (W/O Dock)	V			V	V	
M82 (W/ Dock)		V	V			
M82 (W/O Dock HDMI)		V		V		
M82 (w/dock W/ HDMI)		V	V			V

Project Code & Schematics Subject: M750 Main Board

PCB P/N:

FOXCONN HON HAI Precision Ind. Co., Ltd.
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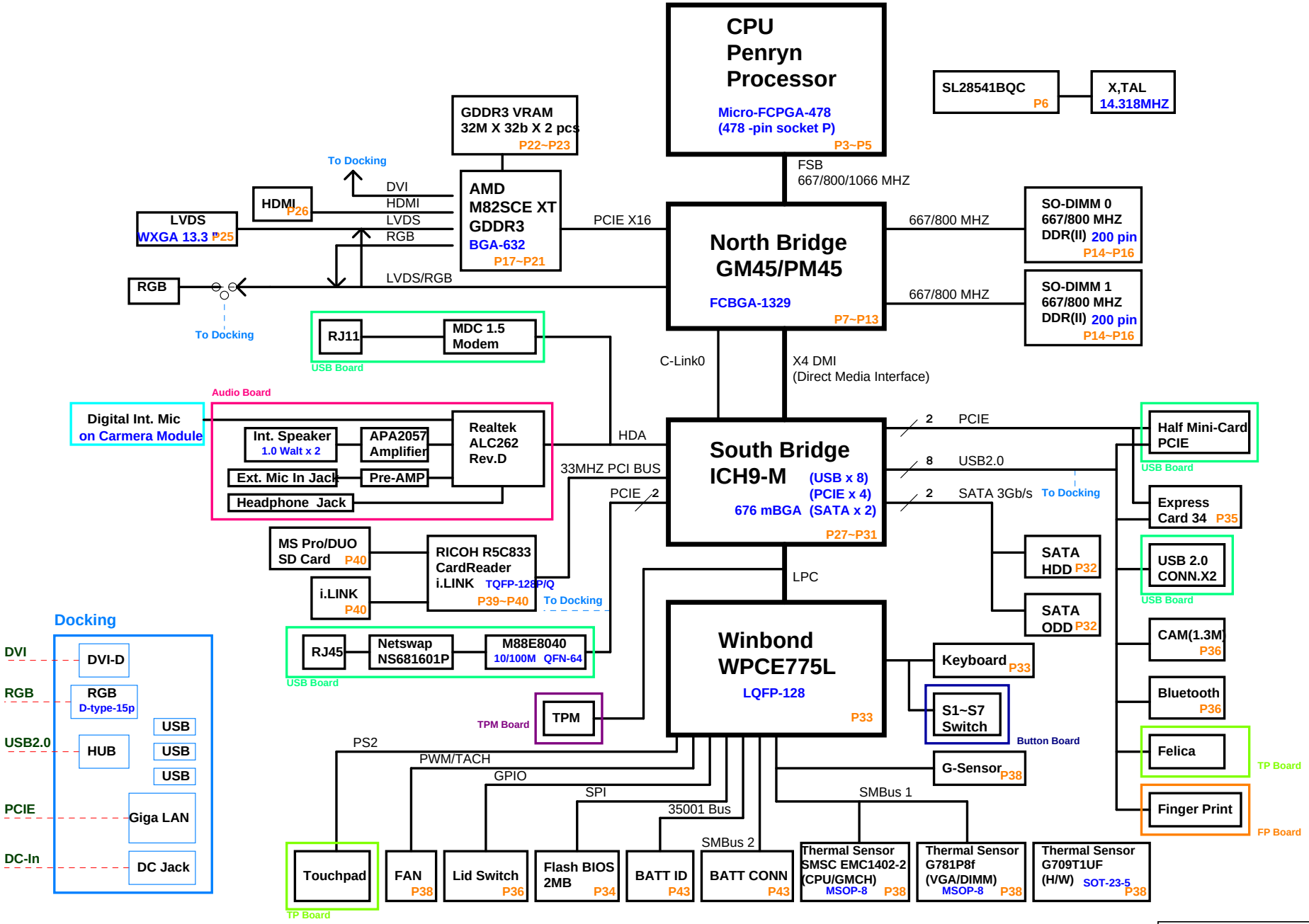
M750 (Montevina + M82SCE XT)



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Block Diagram	
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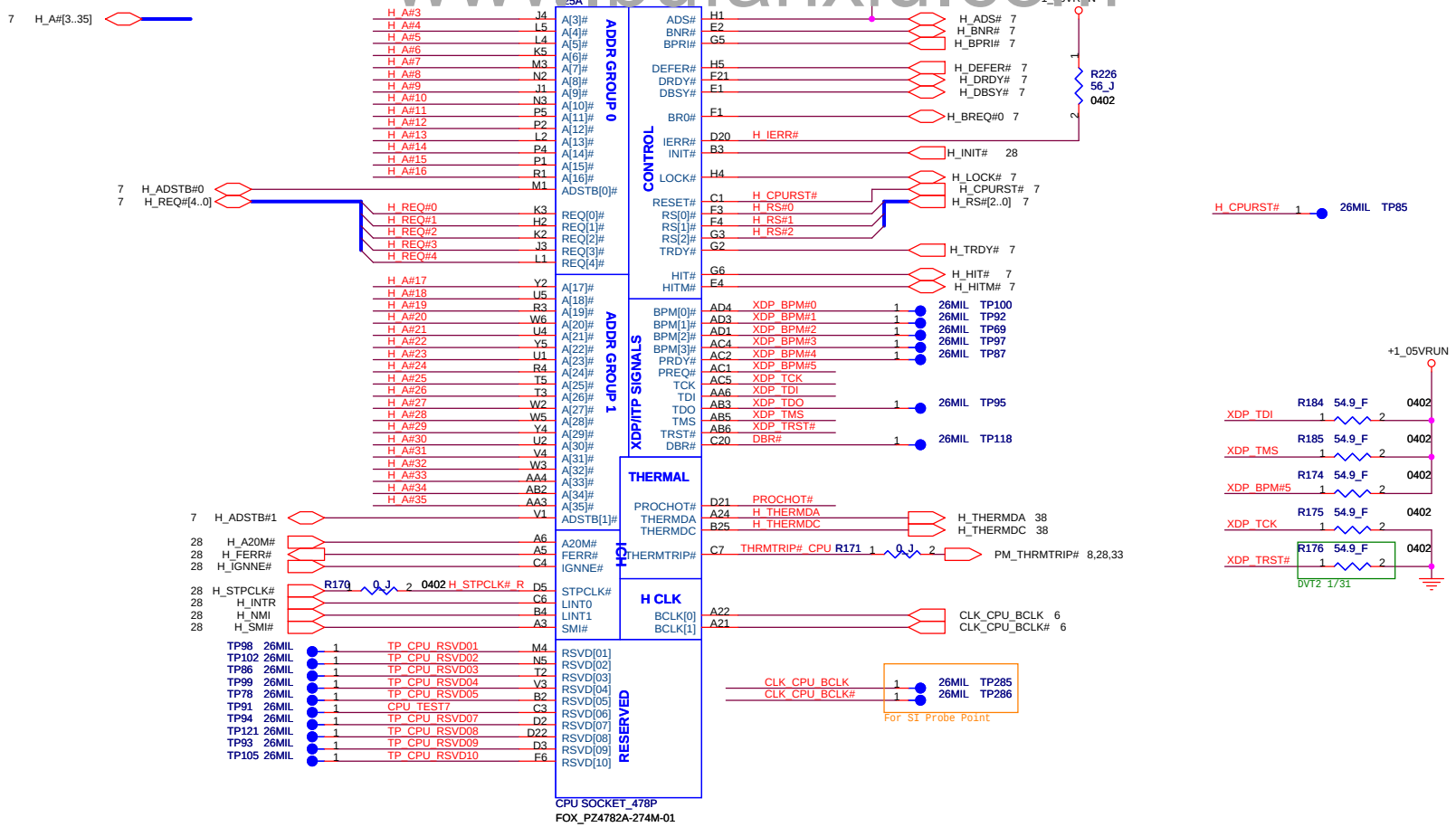

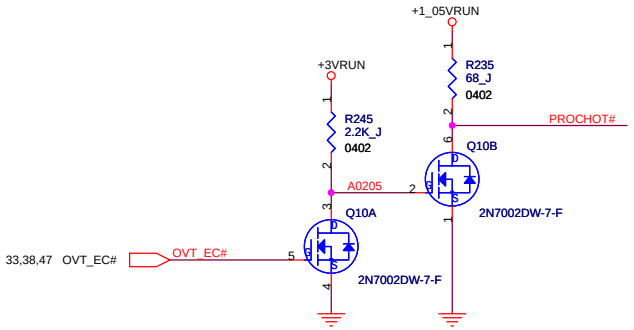

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Penryn (HOST BUS) 1/3	
Size A3	Document Number M750-1-01	Rev 1.0
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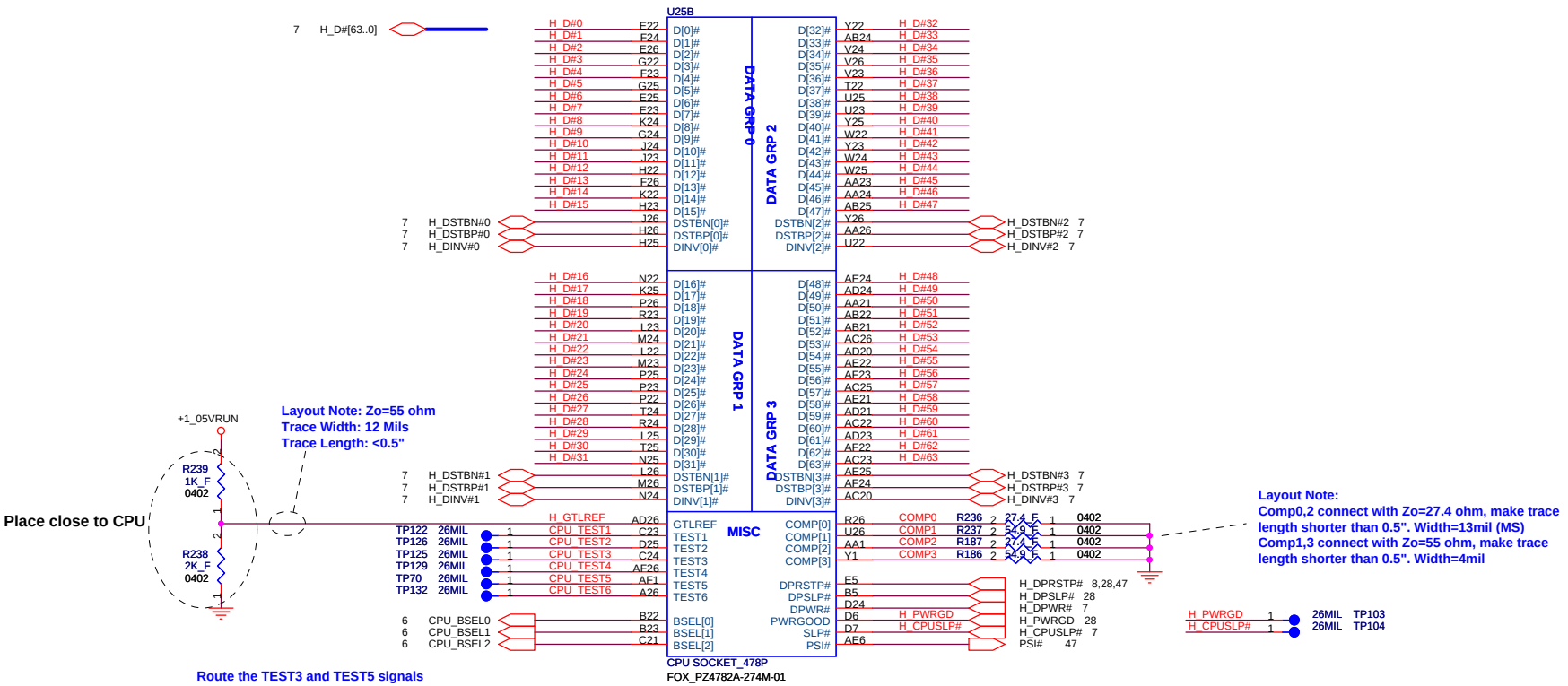

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Title	Penryn (HOST BUS) 2/3	
Size A3	Document Number M750-1-01	Rev 1.0
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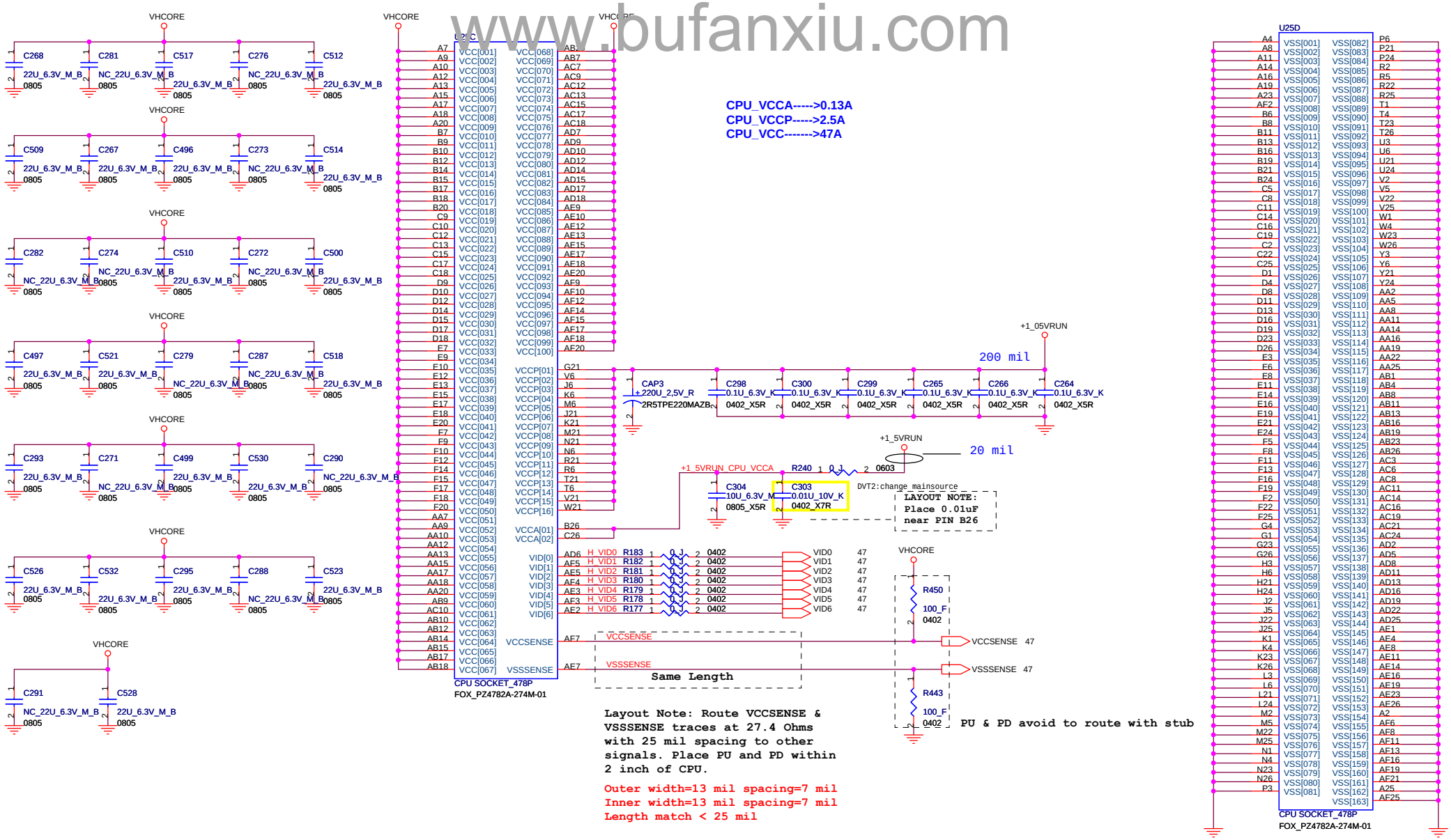

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Title	Penryn (POWER/GROUND) 3/3		
Size A3	Document Number M750-1-01		Rev 1.0
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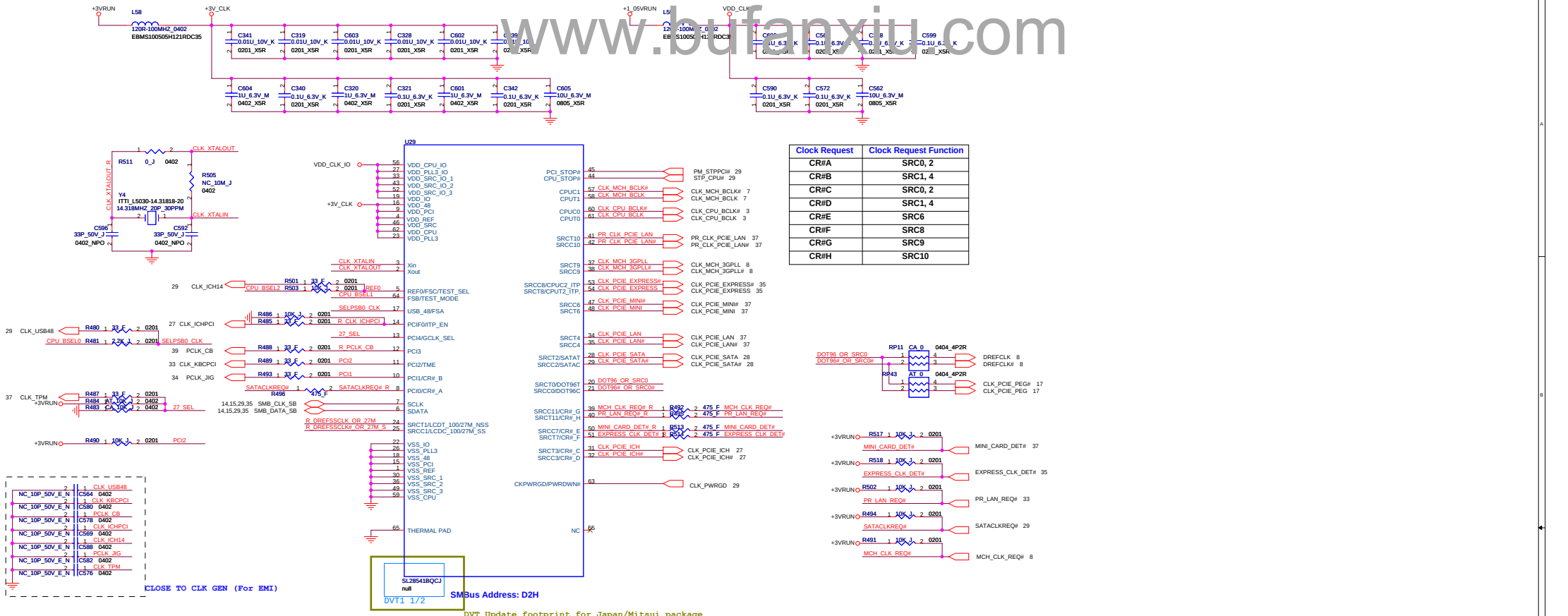

Clock Request	Clock Request Function
CR#A	SRC0, 2
CR#B	SRC1, 4
CR#C	SRC0, 2
CR#D	SRC1, 4
CR#E	SRC6
CR#F	SRC8
CR#G	SRC9
CR#H	SRC10

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: CLOCK GEN		
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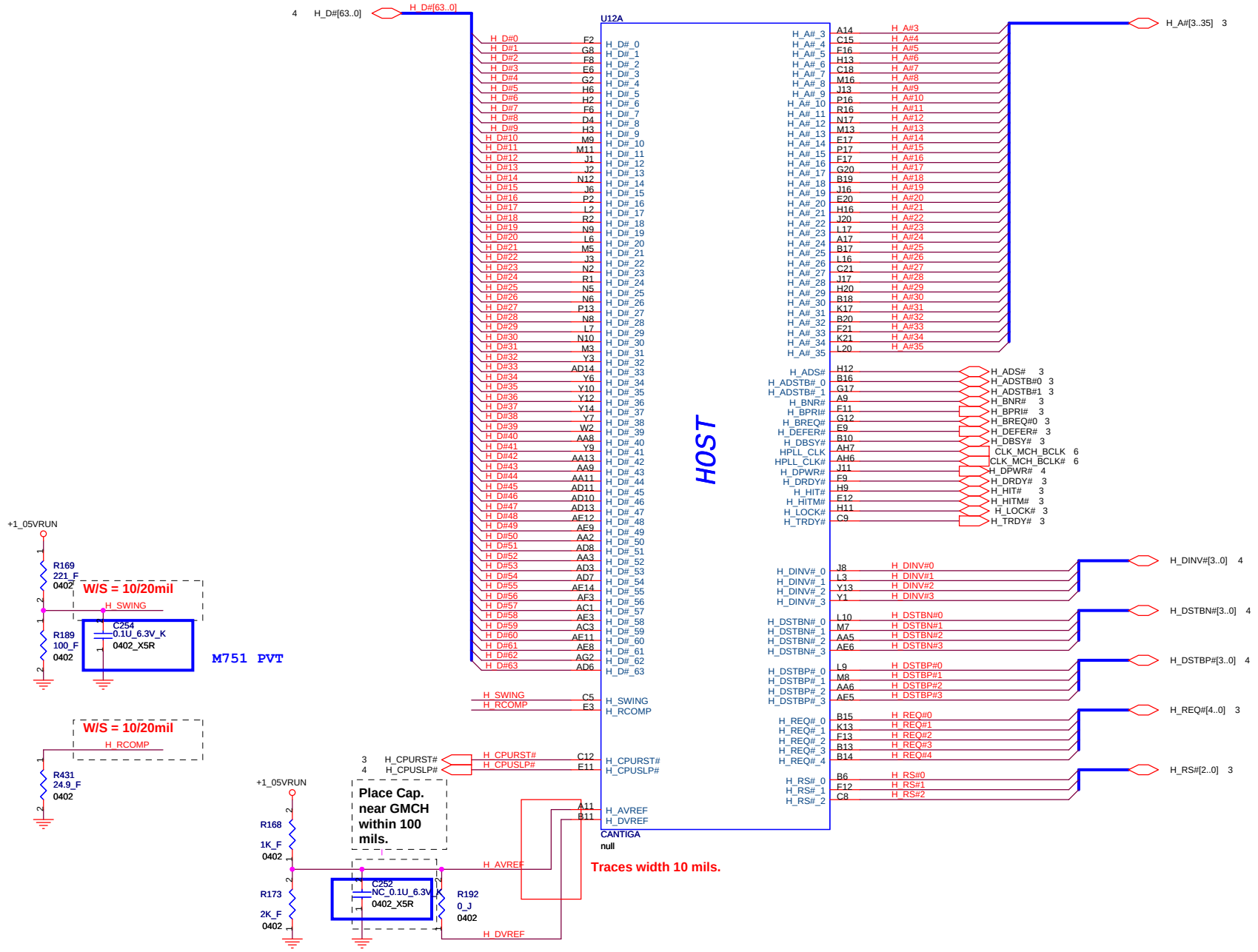

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Cantiga (HOST) 1/7		
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MCH_CFG_0~2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3~4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIE Graphics Lane	Low = Lane Reversed High = Normal operation
MCH_CFG_10 PCIE Loopback enable	Low = Enabled High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled High = Disabled (default)
MCH_CFG_14~15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17~18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

U12B

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
GRAPHICS VID
NC
MISC
HDA

CFG[17:3] internal pull-up
CFG[20:18] internal pull-down

CANTIGA
null

FOXCONN
HON HAI Precision Ind. Co., Ltd.
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Title	Cantiga (DMI) 2/7	
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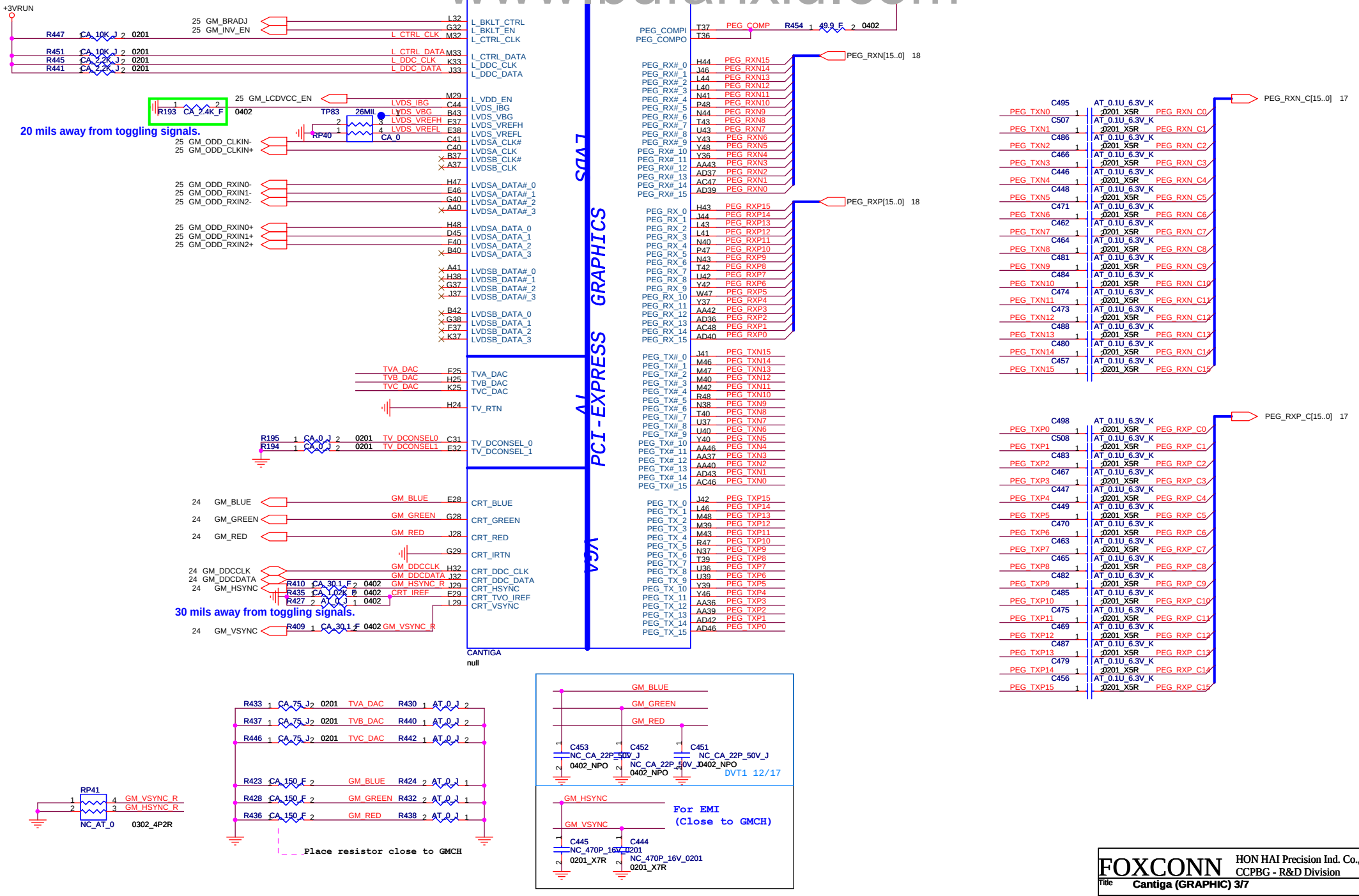

FOXCONN	HON HAI Precision Ind. Co., Ltd.
	CCPBG - R&D Division
Title	Cantiga (GRAPHIC) 3/7
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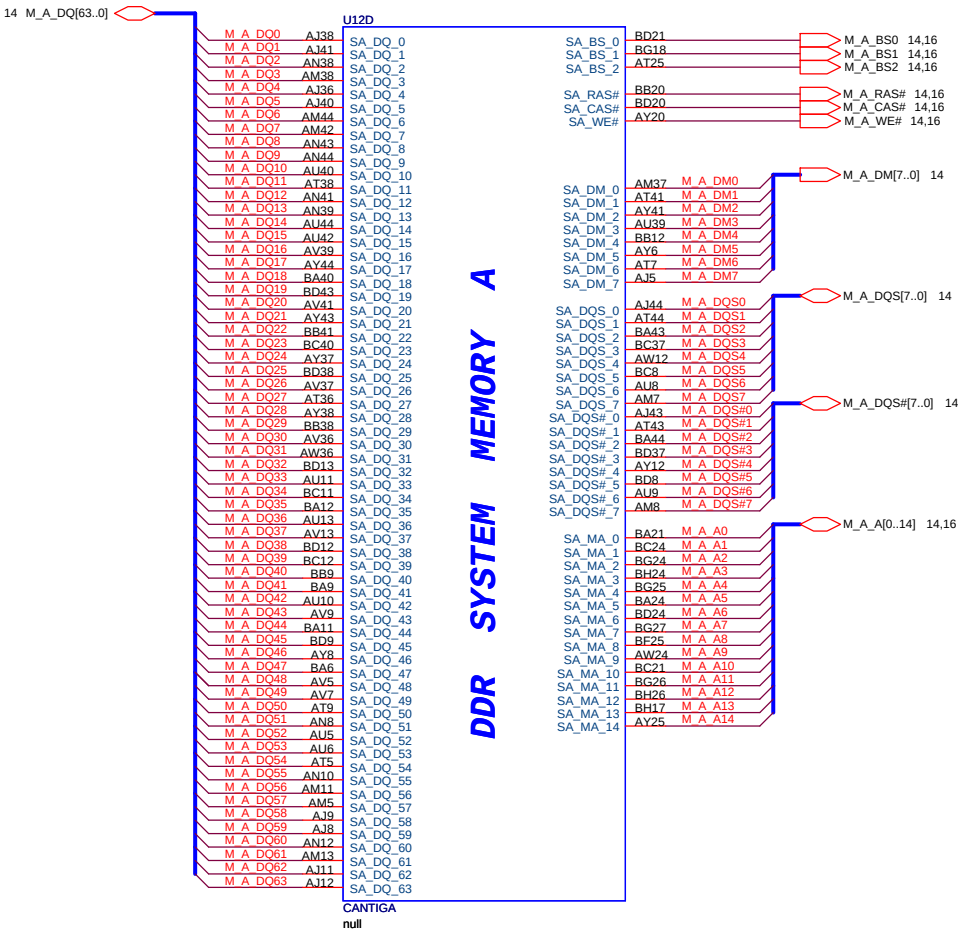

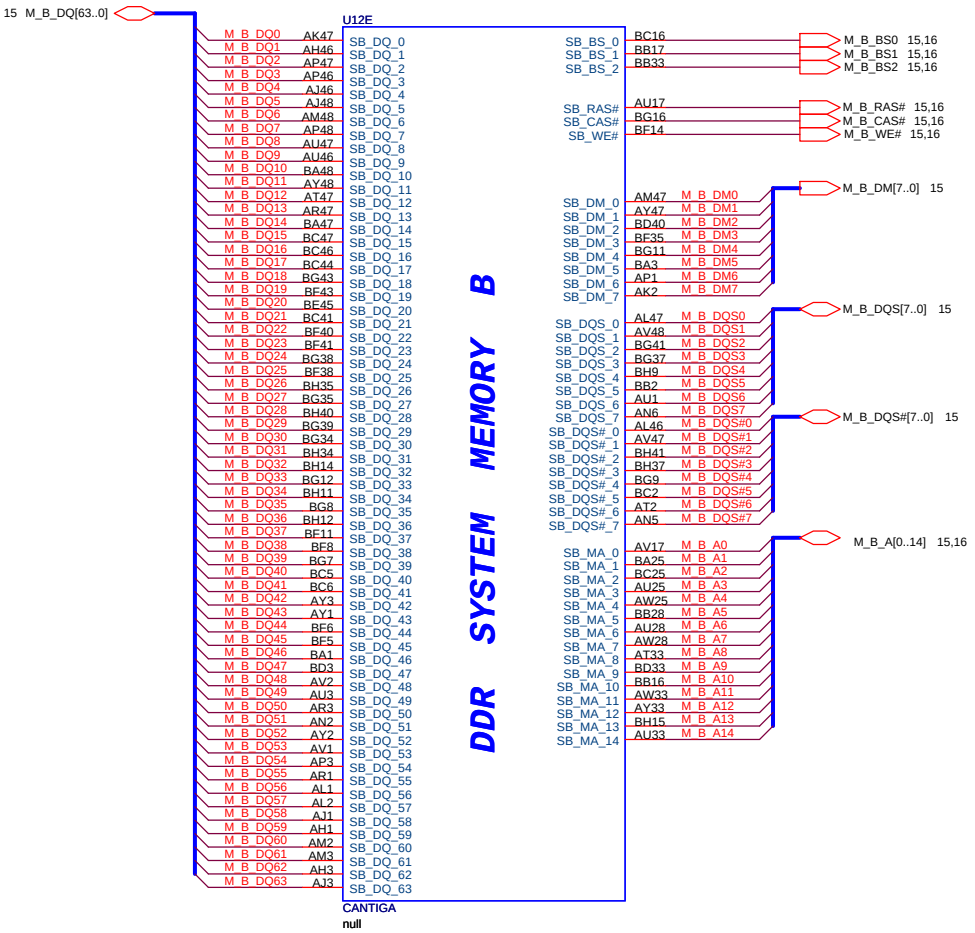

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Title	Cantiga (DDRII) 4/7	
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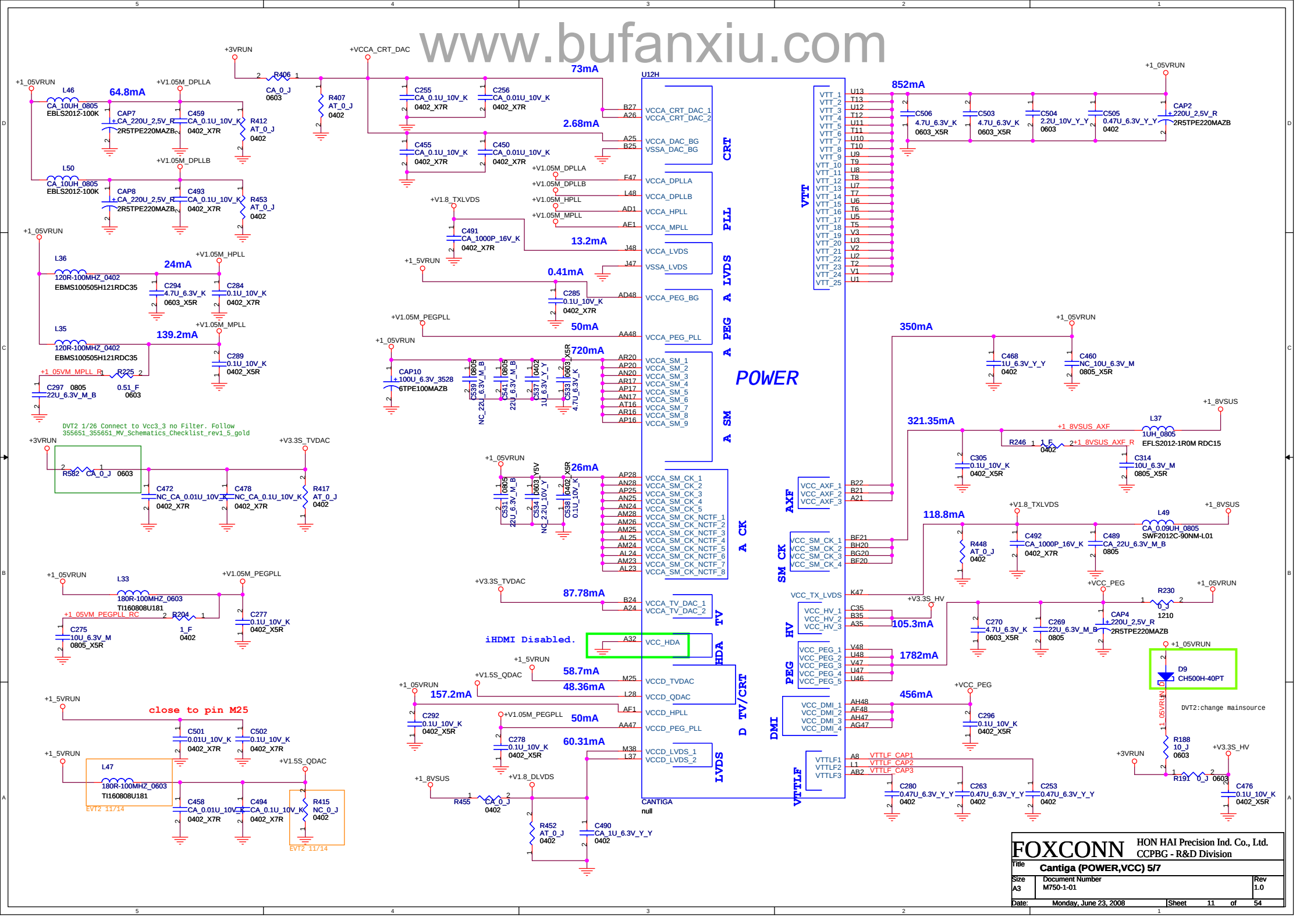

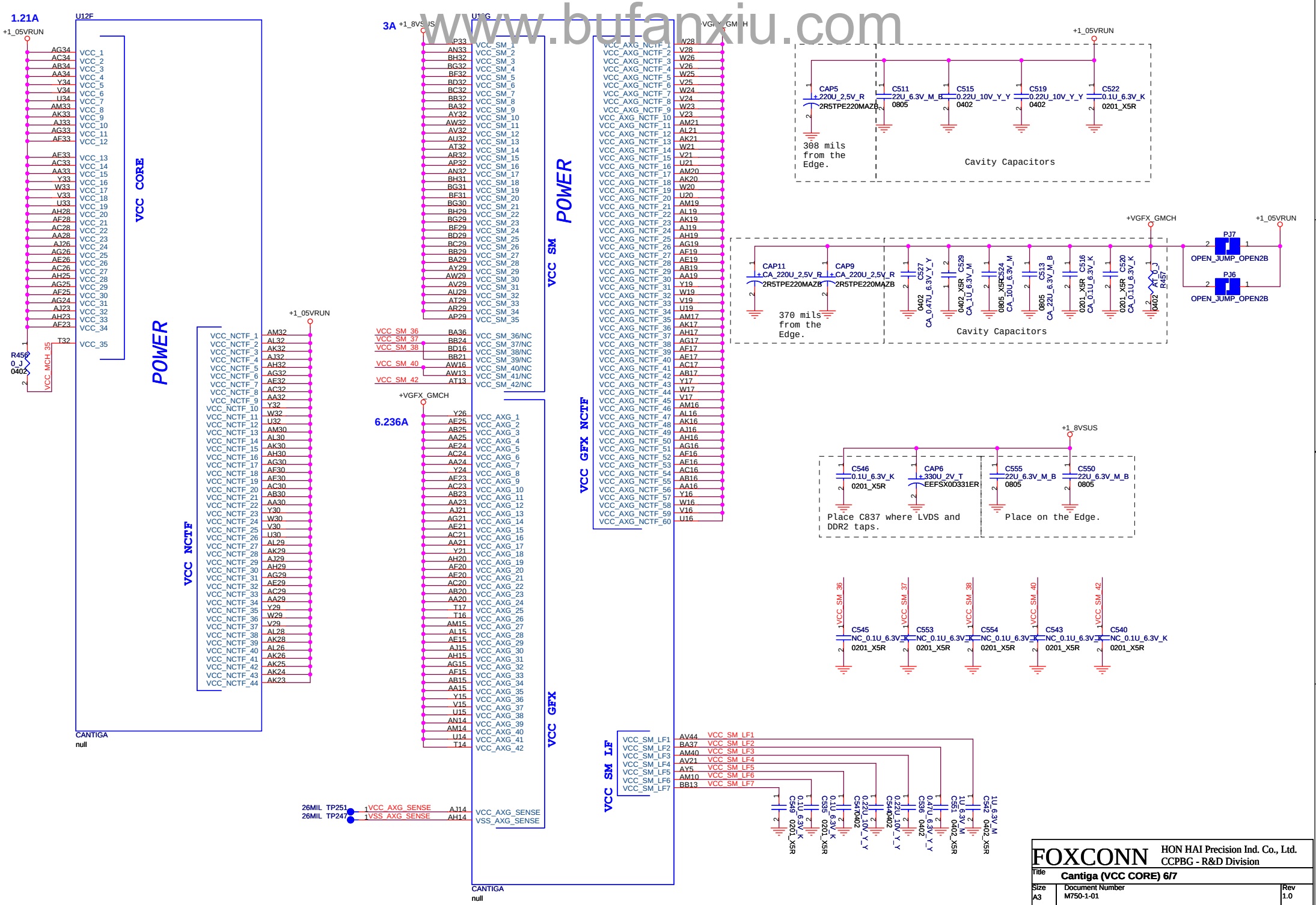

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Title	Cantiga (VCC CORE) 6/7	
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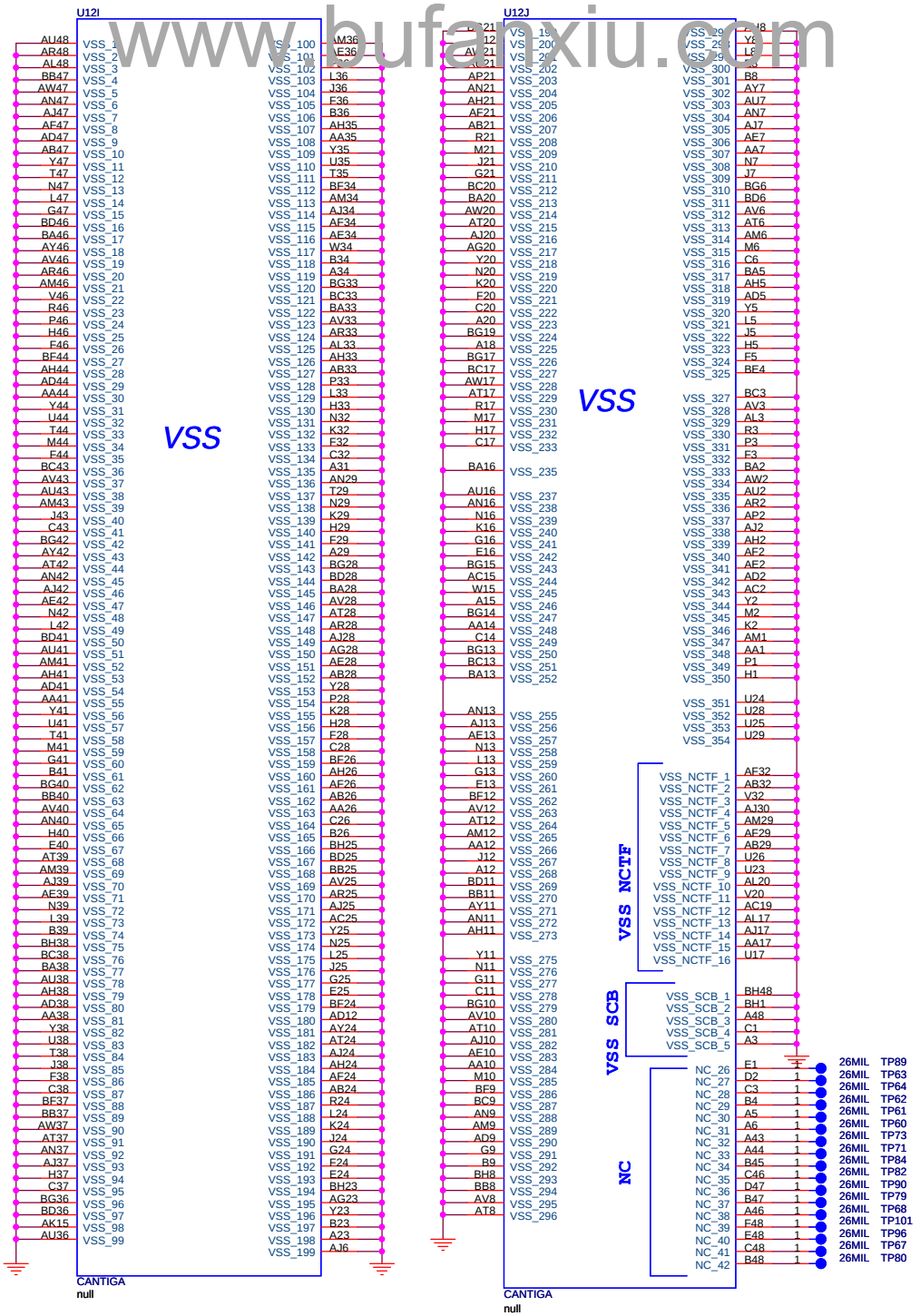

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Cantiga (VSS) 7/7	
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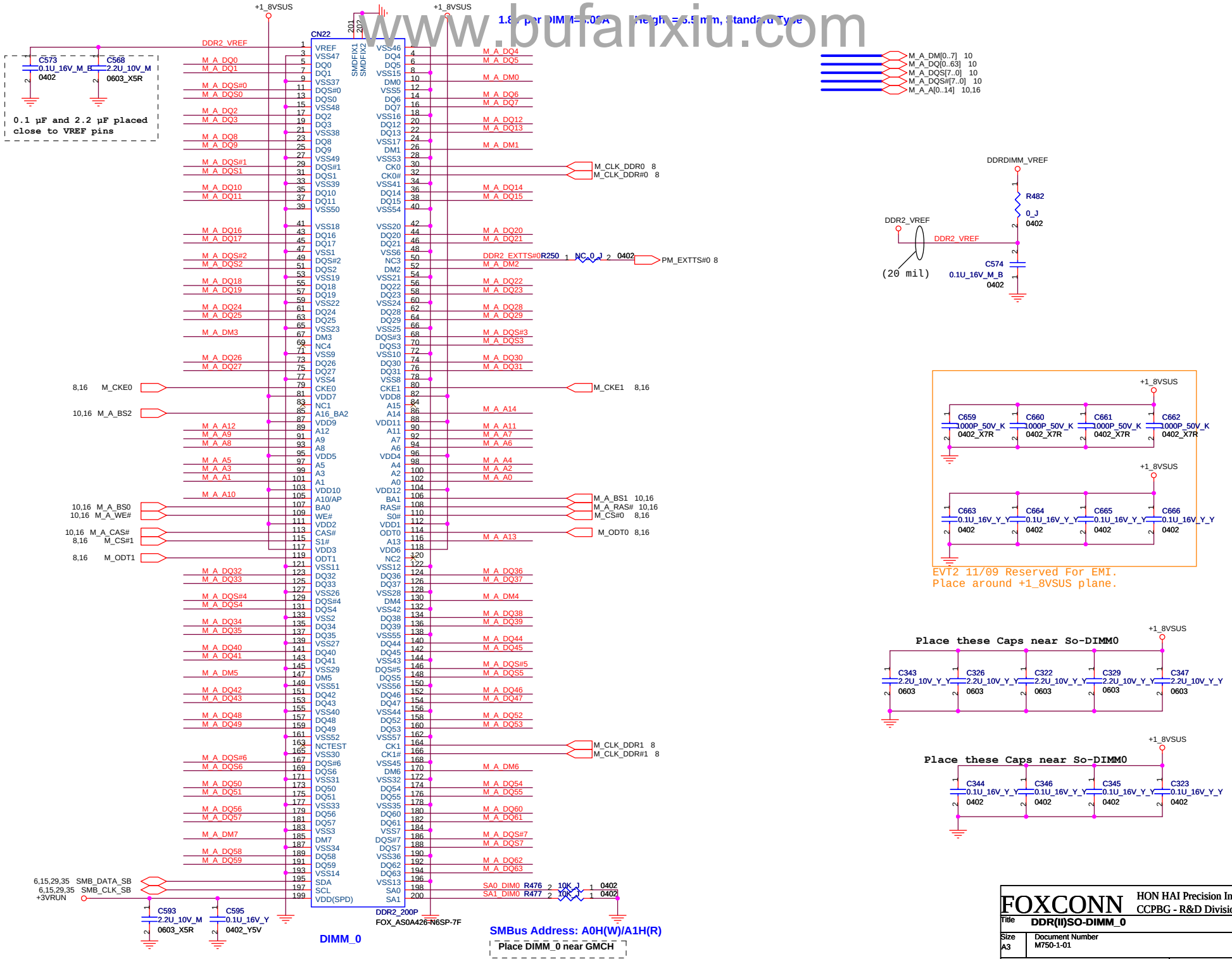

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Title	DDR(II)SO-DIMM_0	
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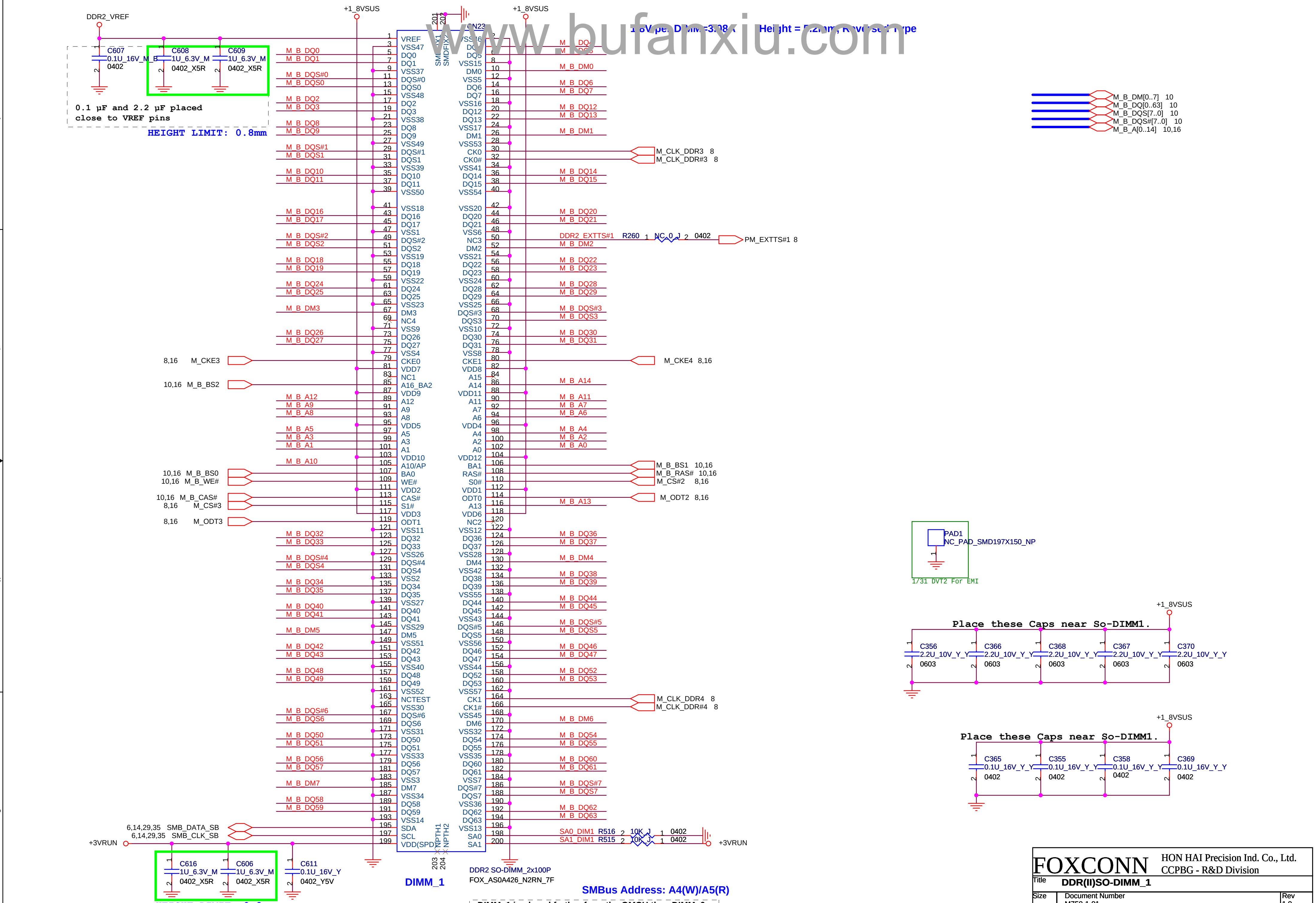

SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title	DDR(II)SO-DIMM_1	
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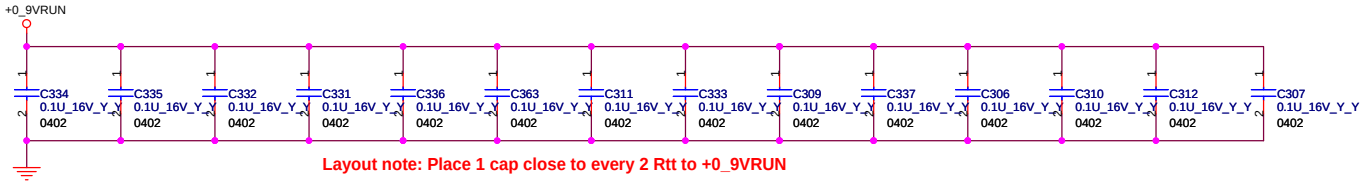
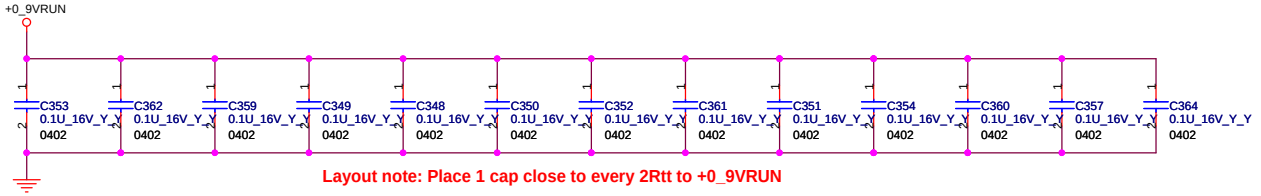


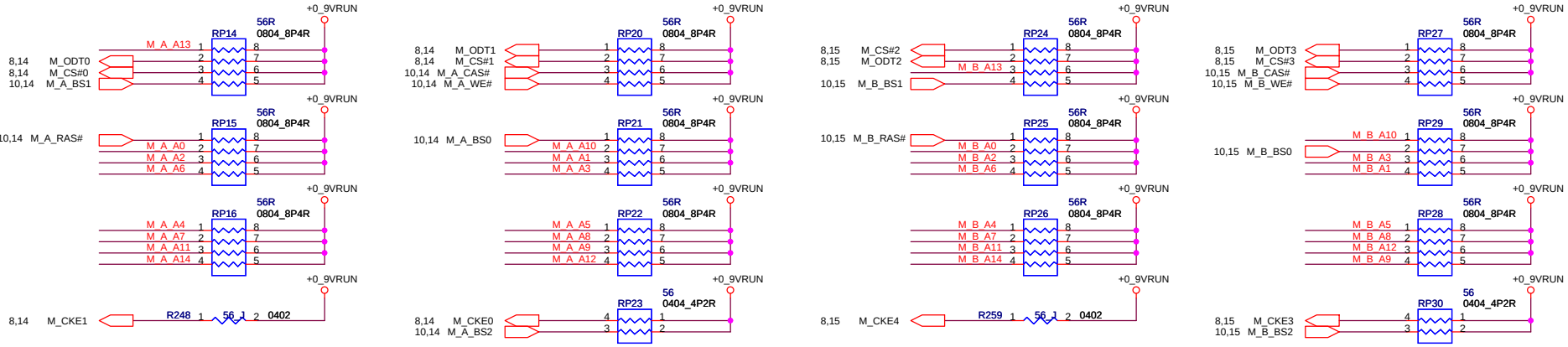
Layout note: Place 1 cap close to every 2 Rtt to +0_9VRUN



Layout note: Place 1 cap close to every 2Rtt to +0_9VRUN

10,14 M_A_A[0..14]

10,15 M_B_A[0..14]



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR(II)Termination	
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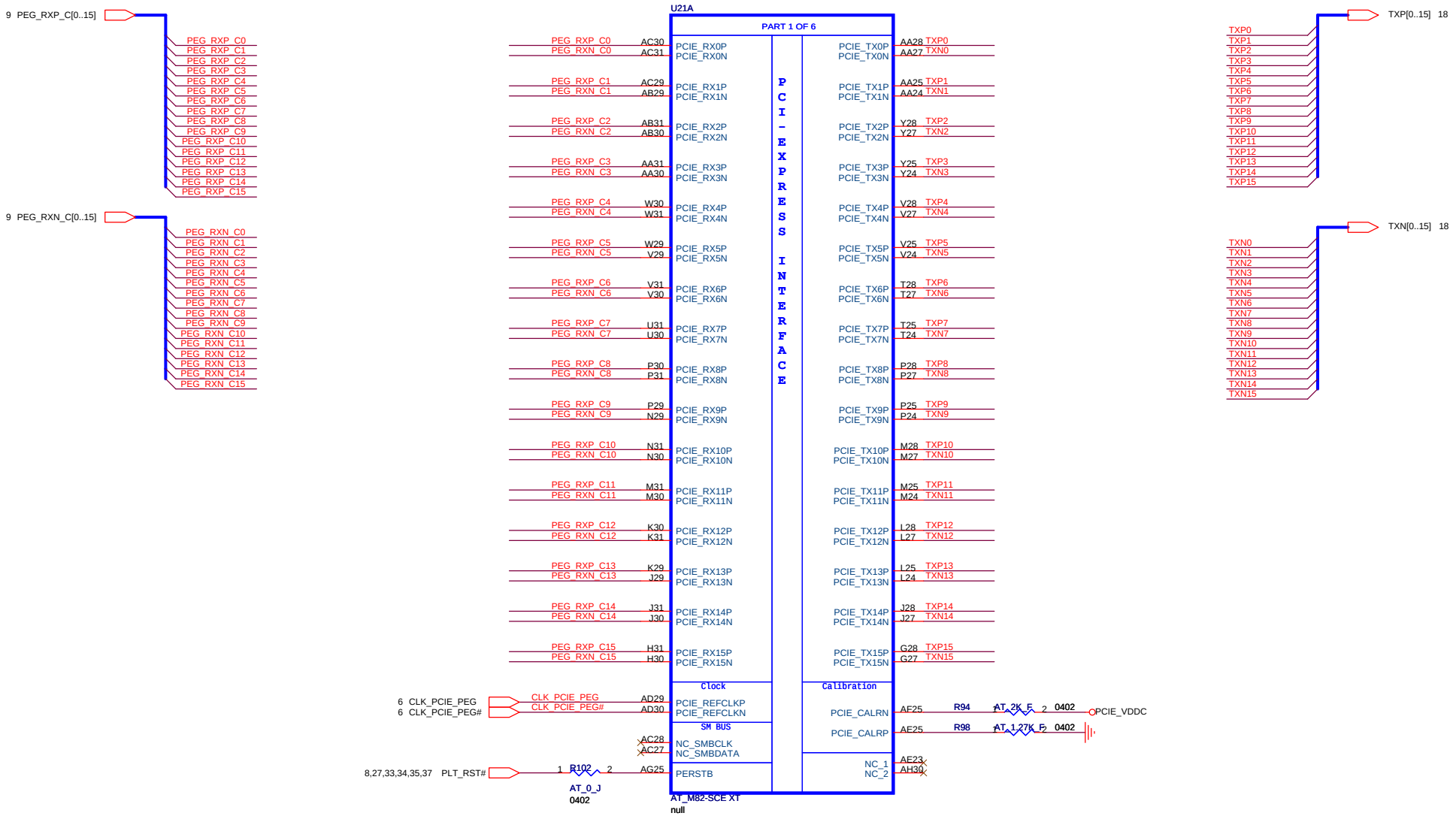

FOXCONN
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CCPBG - R&D Division

Title	VGA (PCI-E) 1/5	
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9 PEG_RXP[0..15]

PEG_RXP0	C206	AT_0.1U_6.3V_K	0201_X5R	TXP0	
PEG_RXP1	C224	AT_0.1U_6.3V_K	0201_X5R	TXP1	
PEG_RXP2	C204	AT_0.1U_6.3V_K	0201_X5R	TXP2	
PEG_RXP3	C230	AT_0.1U_6.3V_K	0201_X5R	TXP3	
PEG_RXP4	C215	AT_0.1U_6.3V_K	0201_X5R	TXP4	
PEG_RXP5	C226	AT_0.1U_6.3V_K	0201_X5R	TXP5	
PEG_RXP6	C202	AT_0.1U_6.3V_K	0201_X5R	TXP6	
PEG_RXP7	C232	AT_0.1U_6.3V_K	0201_X5R	TXP7	
PEG_RXP8	C199	AT_0.1U_6.3V_K	0201_X5R	TXP8	
PEG_RXP9	C220	AT_0.1U_6.3V_K	0201_X5R	TXP9	
PEG_RXP10	C235	AT_0.1U_6.3V_K	0201_X5R	TXP10	
PEG_RXP11	C213	AT_0.1U_6.3V_K	0201_X5R	TXP11	
PEG_RXP12	C229	AT_0.1U_6.3V_K	0201_X5R	TXP12	
PEG_RXP13	C209	AT_0.1U_6.3V_K	0201_X5R	TXP13	
PEG_RXP14	C211	AT_0.1U_6.3V_K	0201_X5R	TXP14	
PEG_RXP15	C237	AT_0.1U_6.3V_K	0201_X5R	TXP15	

TXP[0..15] 17

9 PEG_RXN[0..15]

PEG_RXN0	C207	AT_0.1U_6.3V_K	0201_X5R	TXN0	
PEG_RXN1	C225	AT_0.1U_6.3V_K	0201_X5R	TXN1	
PEG_RXN2	C205	AT_0.1U_6.3V_K	0201_X5R	TXN2	
PEG_RXN3	C231	AT_0.1U_6.3V_K	0201_X5R	TXN3	
PEG_RXN4	C214	AT_0.1U_6.3V_K	0201_X5R	TXN4	
PEG_RXN5	C227	AT_0.1U_6.3V_K	0201_X5R	TXN5	
PEG_RXN6	C203	AT_0.1U_6.3V_K	0201_X5R	TXN6	
PEG_RXN7	C233	AT_0.1U_6.3V_K	0201_X5R	TXN7	
PEG_RXN8	C198	AT_0.1U_6.3V_K	0201_X5R	TXN8	
PEG_RXN9	C221	AT_0.1U_6.3V_K	0201_X5R	TXN9	
PEG_RXN10	C234	AT_0.1U_6.3V_K	0201_X5R	TXN10	
PEG_RXN11	C212	AT_0.1U_6.3V_K	0201_X5R	TXN11	
PEG_RXN12	C228	AT_0.1U_6.3V_K	0201_X5R	TXN12	
PEG_RXN13	C208	AT_0.1U_6.3V_K	0201_X5R	TXN13	
PEG_RXN14	C210	AT_0.1U_6.3V_K	0201_X5R	TXN14	
PEG_RXN15	C236	AT_0.1U_6.3V_K	0201_X5R	TXN15	

TXN[0..15] 17

Strap for GDDR3-136ball
ATI_DVPDATA[23 : 20]

0001 16Mx32 Qimonda
0010 16Mx32 Hynix
0011 16Mx32 Samsung
0101 32Mx32 Qimonda
0110 32Mx32 Hynix
0111 32Mx32 Samsung

If no ROM attached, GPIO[9:13:12:11]
CONFIG{3:0}
controls the memory aperture size.

128MB	X000
256MB	X001
64MB	X010
32MB	X011
512MB	X100
1GB	X101
2GB	X110
4GB	X111

+1_8VRUN

MEM_ID0	R351	NC_AT_10K_J	0402	AT_MEM_ID0	R341	AT_10K_J	0402
MEM_ID1	R342	AT_10K_J	0402	AT_MEM_ID1	R343	NC_AT_10K_J	0402
MEM_ID2	R350	AT_10K_J	0402	AT_MEM_ID2	R340	NC_AT_10K_J	0402
MEM_ID3	R349	AT_10K_J	0402	AT_MEM_ID3	R339	NC_AT_10K_J	0402

N.C R350, MOUNT R340 FOR 32X32Mb Qimonda VRAM

+3V_DELAY

MEM_SIZE3	R30	AT_10K_J	0402	AT_GPIO9	R31	NC_AT_10K_J	0402
MEM_SIZE2	R354	AT_10K_J	0402	AT_GPIO13	R347	NC_AT_10K_J	0402
MEM_SIZE1	R28	AT_10K_J	0402	AT_GPIO12	R46	NC_AT_10K_J	0402
MEM_SIZE0	R353	AT_10K_J	0402	AT_GPIO11	R346	NC_AT_10K_J	0402

N.C R353, MOUNT R346 FOR 256MB VRAM

19	AT_MEM_ID0	AT_MEM_ID0
19	AT_MEM_ID1	AT_MEM_ID1
19	AT_MEM_ID2	AT_MEM_ID2
19	AT_MEM_ID3	AT_MEM_ID3
19	AT_GPIO9	AT_GPIO9
19	AT_GPIO11	AT_GPIO11
19	AT_GPIO12	AT_GPIO12
19	AT_GPIO13	AT_GPIO13

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: VGA (STRAP) 2/5

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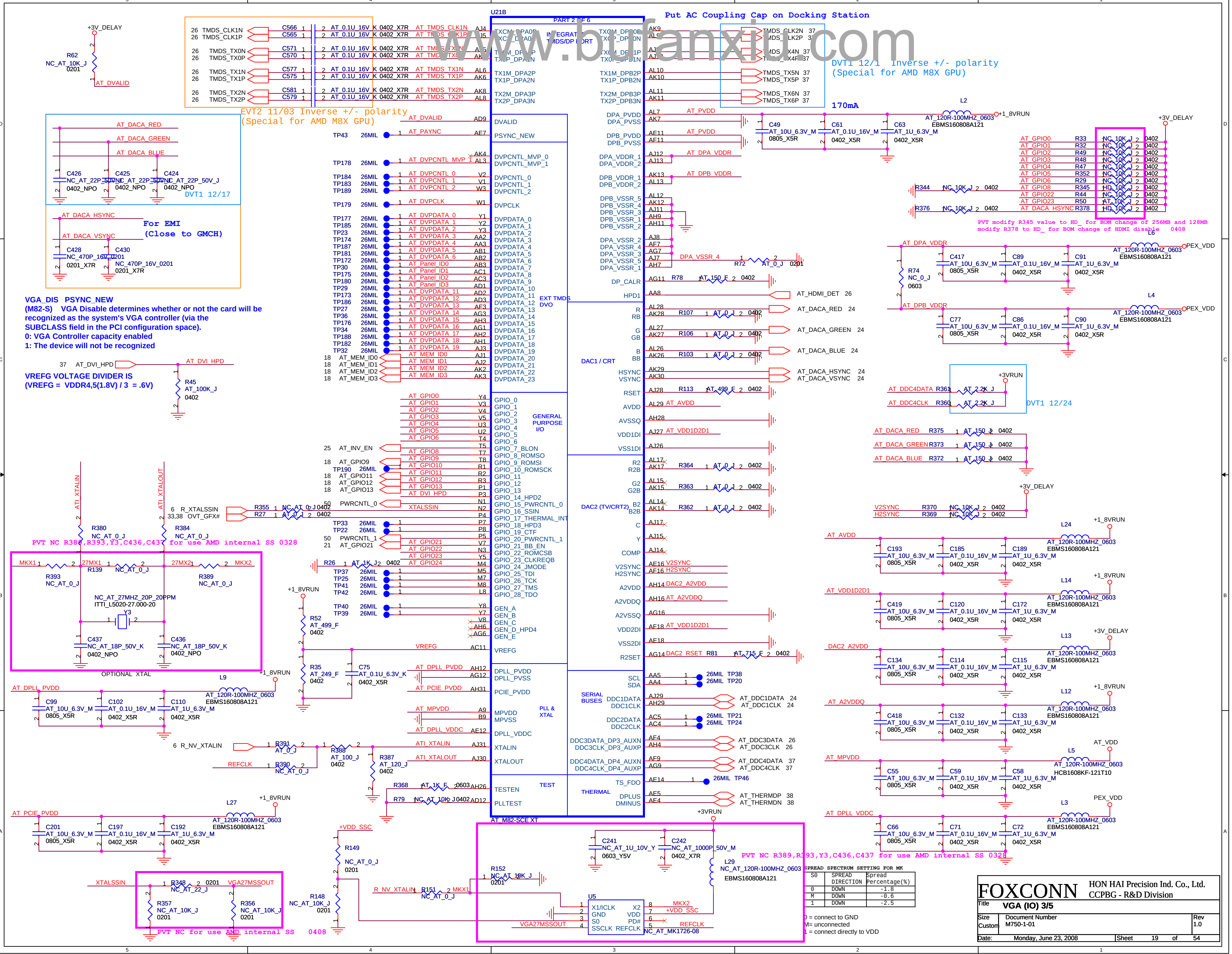

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	VGA (IO) 3/5	
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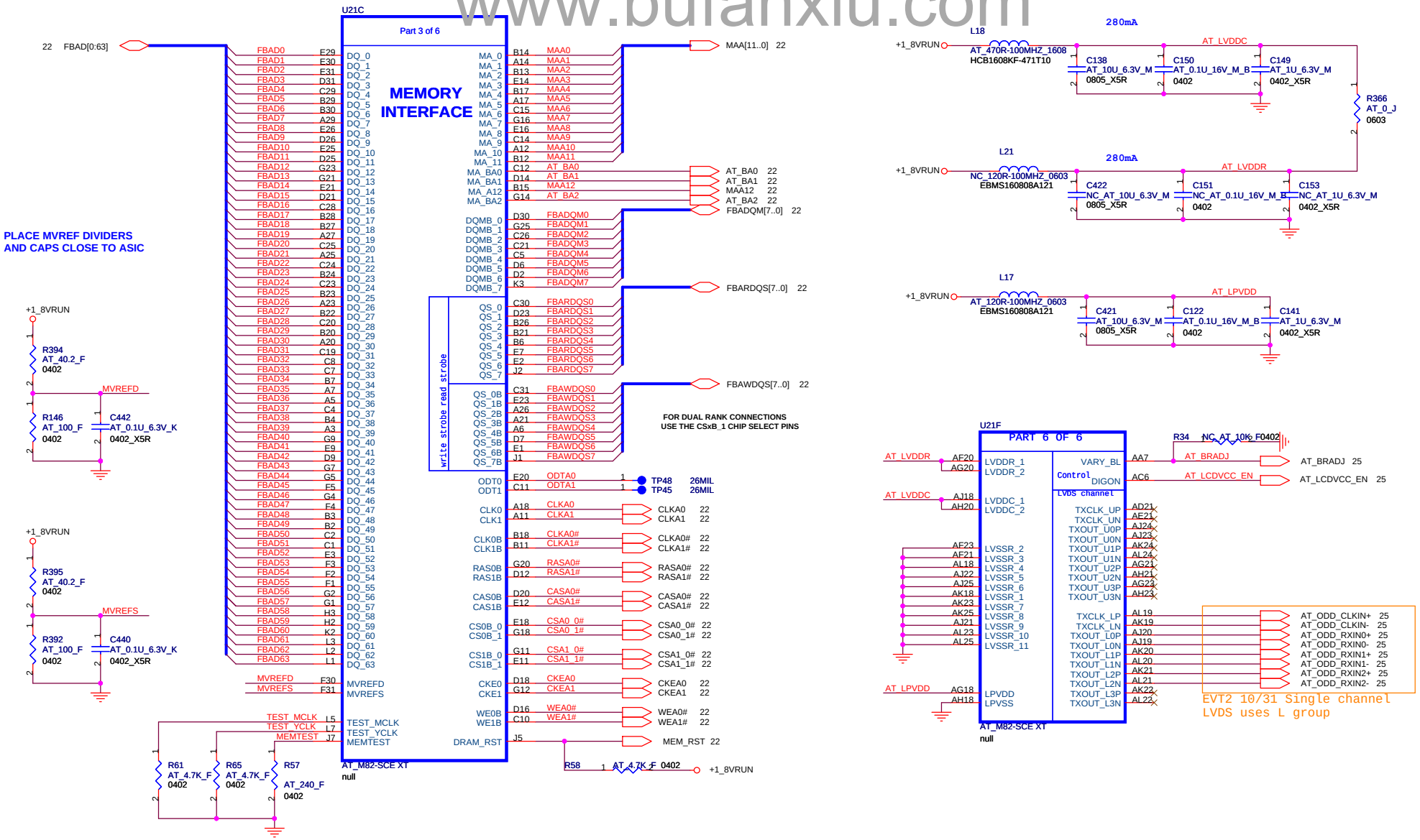

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA (GDDR) 4/5	
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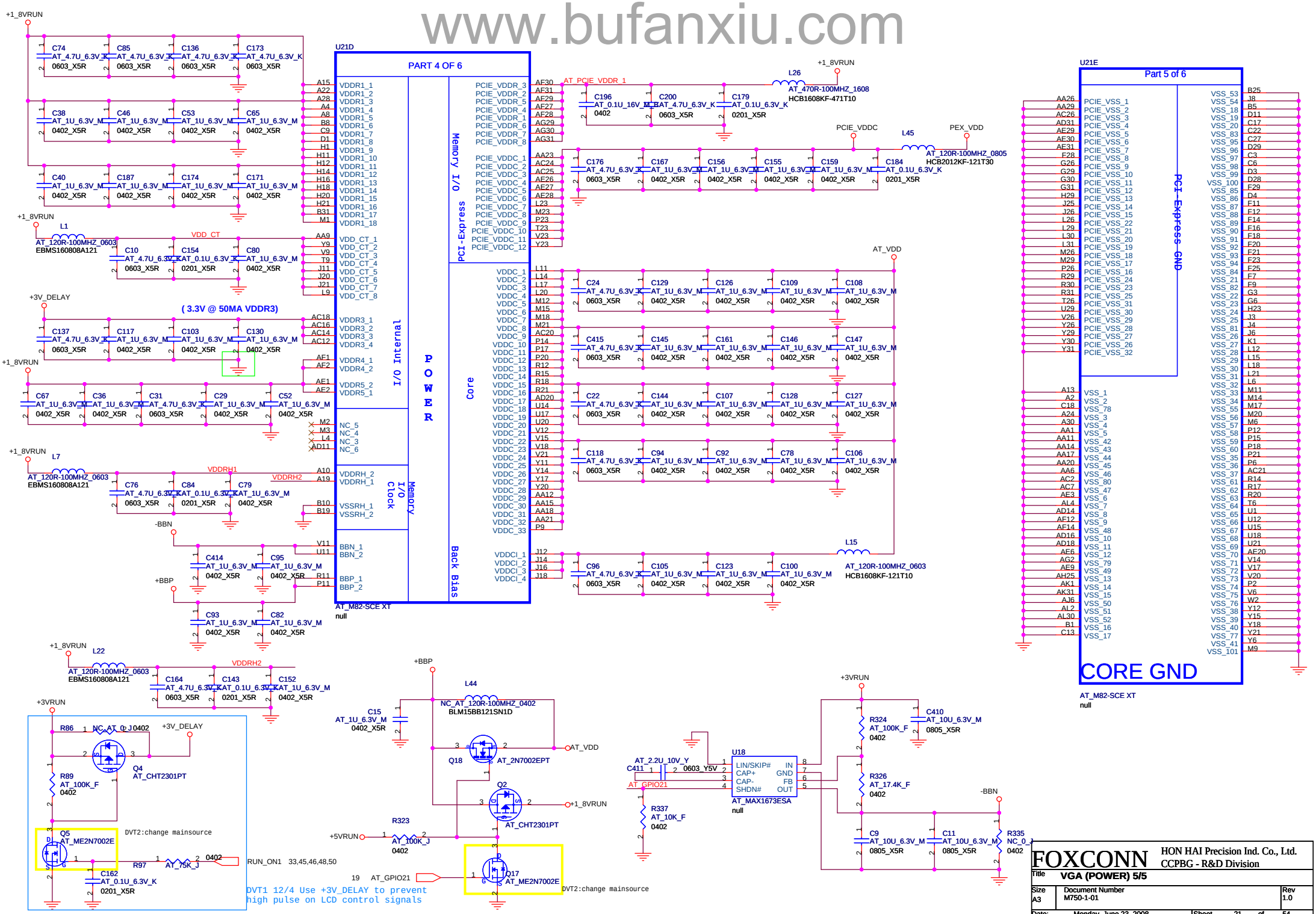

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	CCPBG - R&D Division	
Title	VGA (POWER) 5/5	
Size A3	Document Number M750-1-01	Rev 1.0
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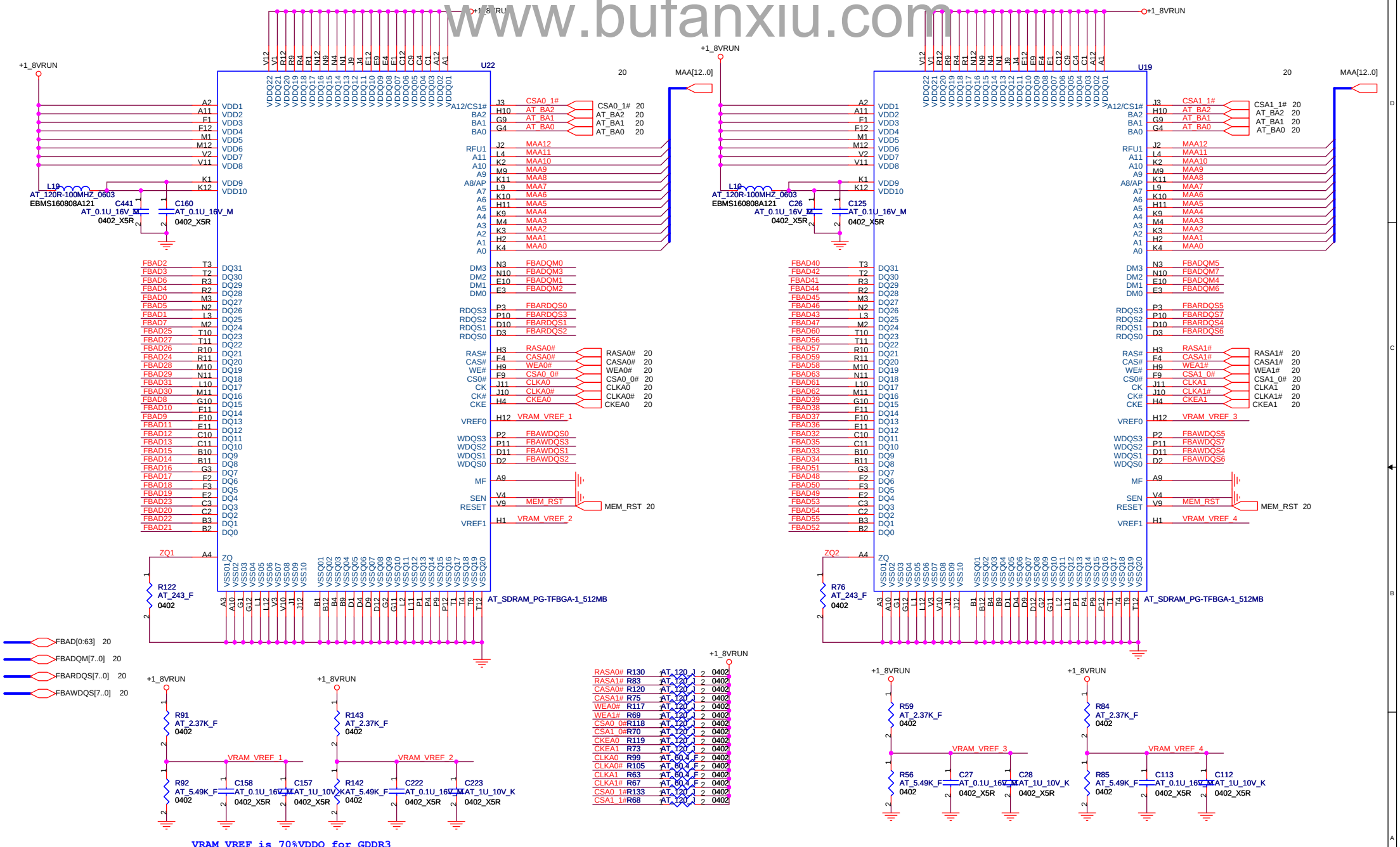

FOXCONN	HON HAI Precision Ind. Co., Ltd.
	CCPBG - R&D Division
Title	VRAM (GDDR3) 1/2
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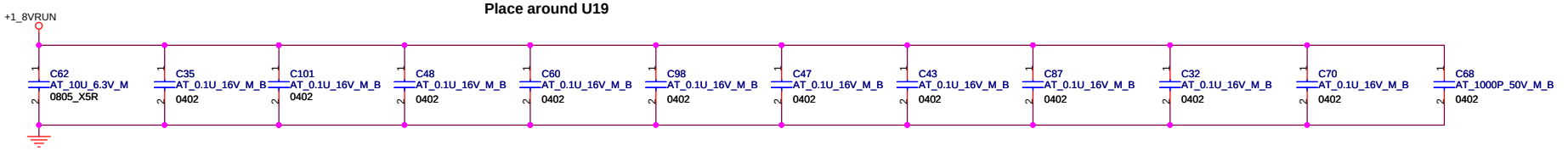
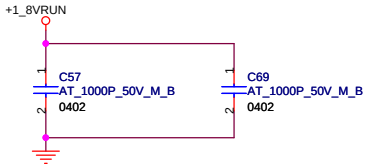
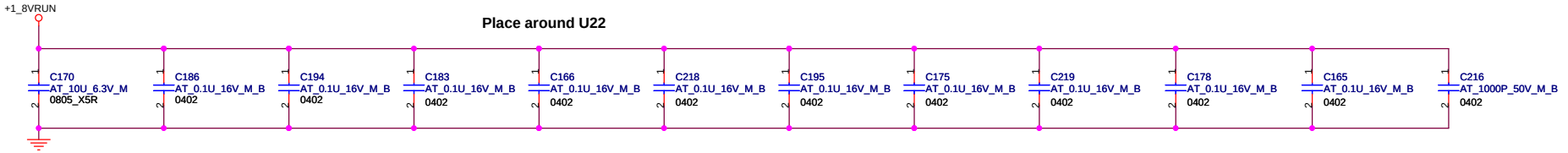
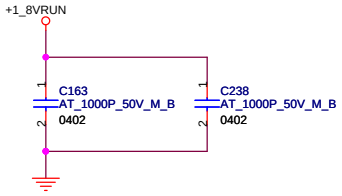
Place around U19



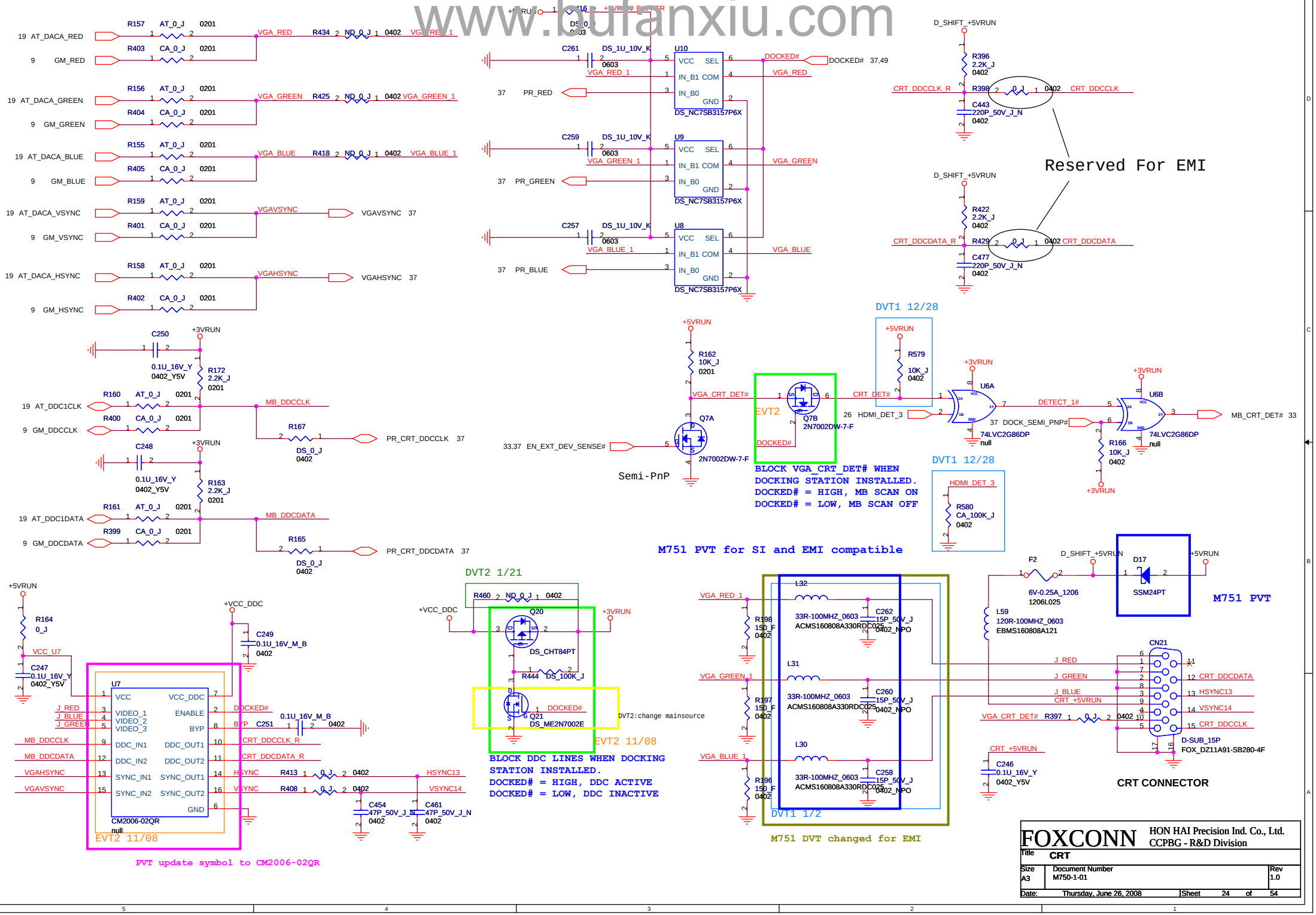


Place around U22



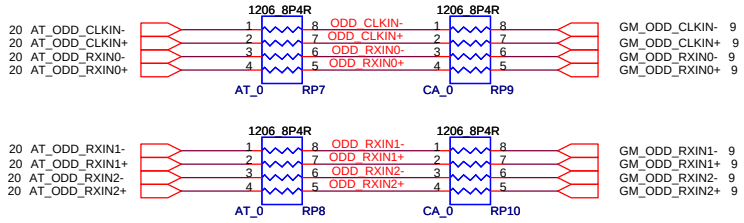


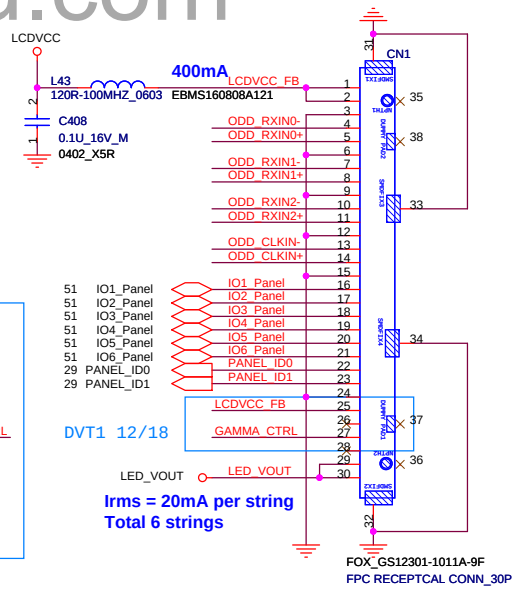
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VRAM (BYPASS) 2/2	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 23 of 54	

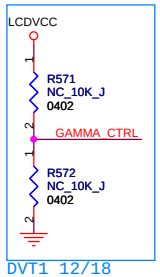


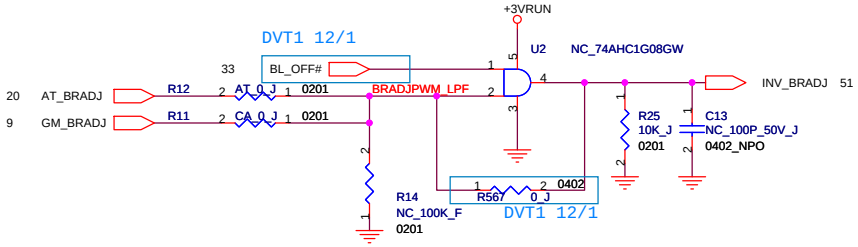
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CRT	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Thursday, June 26, 2008	Sheet 24 of 54	

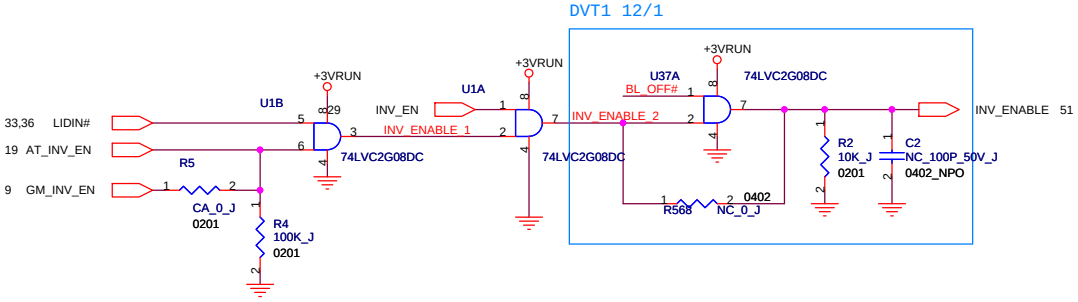
LVDS

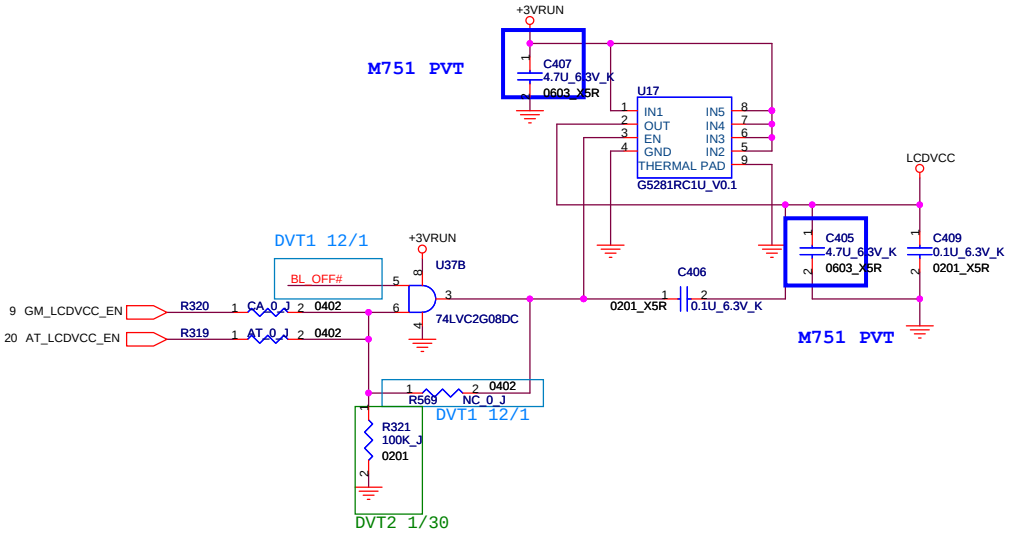




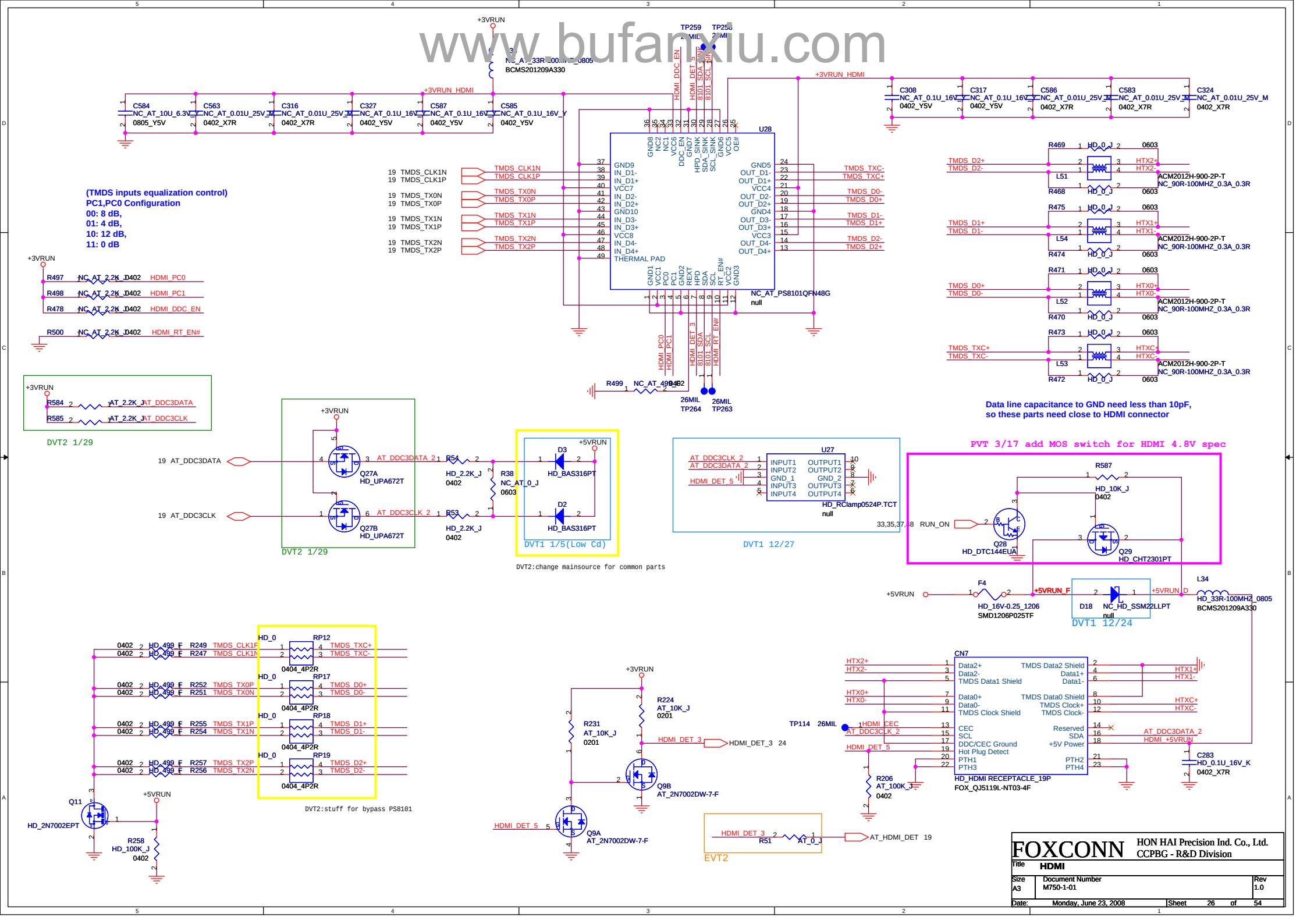




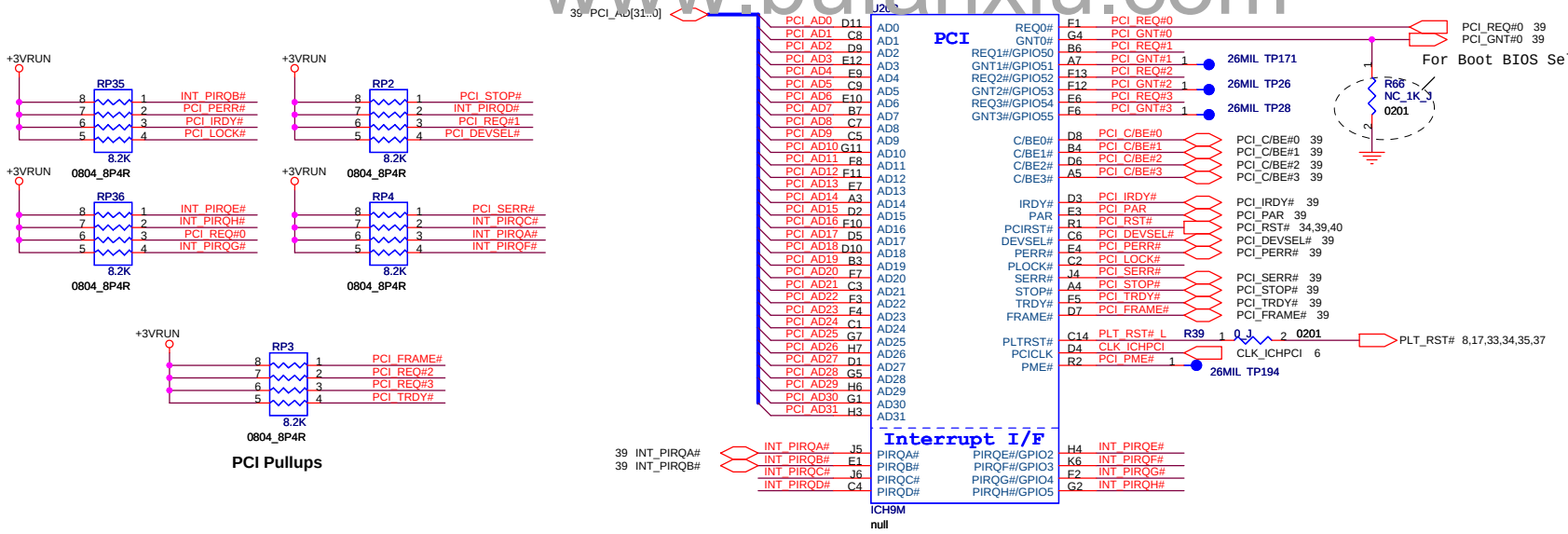




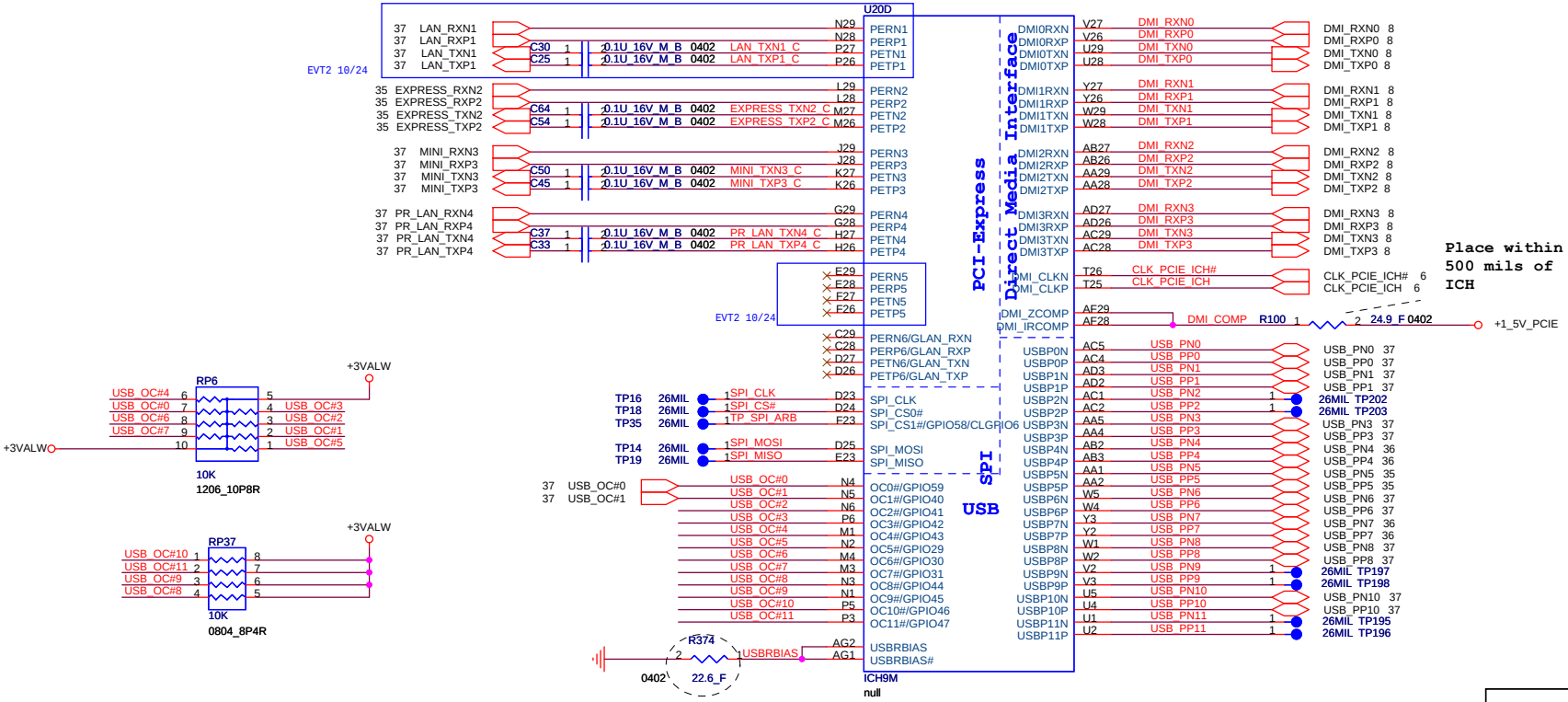
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LVDS	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 25 of 54	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 26 of 54	



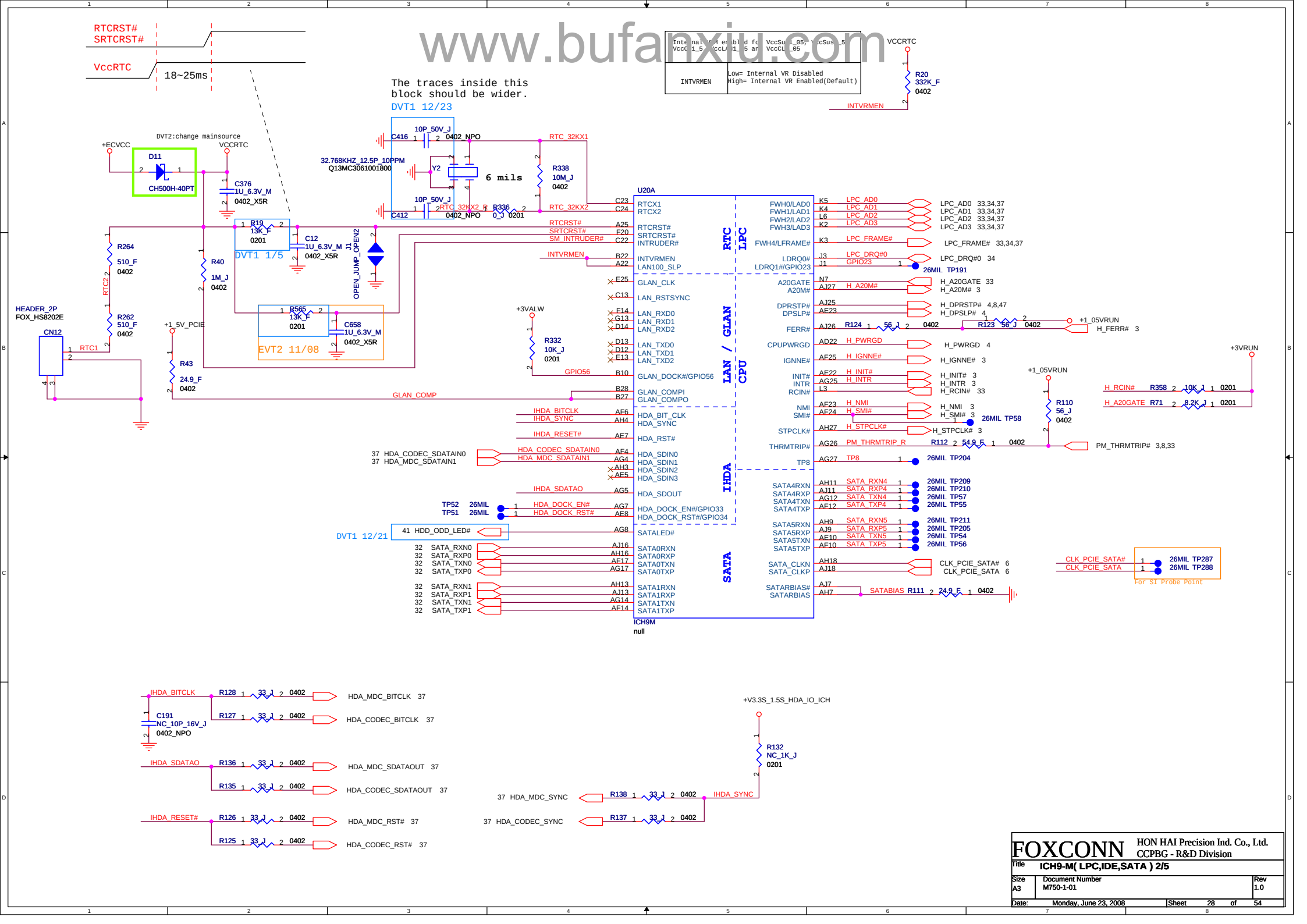
	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi



USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	x
PORT-3	Docking Hub
PORT-4	Bluetooth
PORT-5	ExpressCard
PORT-6	FingerPrint
PORT-7	Camera
PORT-8	Felica
PORT-9	x
PORT-10	Wimax
PORT-11	x

FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ICH9-M(PCI/DMI/USB/PCIE) 1/5	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 27 of 54	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ICH9-M(LPC,IDE,SATA) 2/5		
Size A3	Document Number M750-1-01		Rev 1.0
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SW1: DISPLAY OUTOUT SELECTION
(FOR DEBUG ONLY)

DISPLAY_SEL	
0	CRT
1	LVDS

Dock Support Selection

	Dock Support
0	Not Support
1	Support

RP1 10K 1206_10P8R

R104 NC_1K_J 0201

R140 100K_J 0201 DISPLAY_SEL
R144 100K_J 0201 GPIO37
NC_HDS402-E_SW-SMD4
12/27 DVT1

CLK_ICH14 — 26MIL TP289
CLK_USB48 — 26MIL TP290
For SI Probe Point

R327 100K_J 0201 GPIO57
R329 100K_J 0201 MB_FLASH_EN
R17 10K_J 0201 PM_RSMRST#
R77 10K_J 0201 IMVP_PWRGD
R328 10K_J 0201 INV_EN
R334 10K_J 0201 GPIO13

U20C ICH9M null

SMB: SMB_CLK_SB G16, SMB_DATA_SB A13, SMB_LINK_ALERT# E17, SMLINK0 C17, SMLINK1 B18
SATA GPIO: SATA0GP/GPIO21 AH23, SATA1GP/GPIO19 AE19, SATA4GP/GPIO36 AE21, SATA5GP/GPIO37 AD20
CLOCKS: CLK14 H1, CLK48 AF3, SUSCLK P1
SYS GPIO: PM_RI# F19, PM_SUS_STAT# R4, SB_RST# G19, PM_SYNC# M6, WAKE_SCI# A17, PM_STPPCI# A14, PM_STP_CPU# E19, PM_CLKRUN# L4, WAKE# E20, SERIRQ M5, THRM# AJ23, VRMPWRGD D21, TP12 A20
Power MGT: SLP_S3# C16, SLP_S4# E16, SLP_S5# G17, S4_STATE#/GPIO26 C10, PWROK G20, DPRSLPVR/GPIO16 M2, BATLOW# B13, PWRBTN# R3, LAN_RST# D20, RSMRST# D22, CK_PWRGD R5, CLPWROK R6, SLP_M# B16
GPIO: GPIO1 AG19, GPIO6 AH21, GPIO7 AG21, GPIO8 A21, LAN_PHY_PWR_CTRL/GPIO12 C12, ENERGY_DETECT/GPIO13 C21, GPIO17 AE18, GPIO18 K1, GPIO20 AF8, SCLOCK/GPIO22 AJ22, GPIO27 A9, GPIO28 D19, SATACLKREQ#/GPIO35 L1, SLOAD/GPIO38 AE19, SDATAOUT0/GPIO39 AG22, SDATAOUT1/GPIO48 AF21, GPIO49 AH24, GPIO57/CLGPIO5 A8
Controller Link: CL_CLK0 F24, CL_CLK1 B19, CL_DATA0 F22, CL_DATA1 C19, CL_VREF0 C25, CL_VREF1 A19, CL_RST0# F21, CL_RST1# D18
MISC: SPKR M7, MCH_SYNC# AJ24, TP3 B21, TP9 AH20, TP10 AJ20, TP11 AJ21, MEM_LED/GPIO24 A16, GPIO10/SUS_PWR_ACK C18, GPIO14/AC_PRESENT C11, WOL_EN/GPIO9 C20

PANEL_ID1 AH23 — PANEL_ID1 25
PANEL_ID0 AE19 — PANEL_ID0 25
DISPLAY_SEL AE21
GPIO37 AD20
CLK_ICH14 H1 — CLK_ICH14 6
CLK_USB48 AF3 — CLK_USB48 6
SUS_CLK P1 — 26MIL TP193
PM_SLP_S3# C16 — PM_SLP_S3# 33
PM_SLP_S4# E16 — PM_SLP_S4# 33
PM_SLP_S5# G17 — PM_SLP_S5# 33
PM_S4_STATE# C10 — 26MIL TP162
IMVP_PWRGD_SB R64 2.2K_J 0201 — IMVP_PWRGD 8,33
DPRSLPVR_R R359 0_J 0201 — DPRSLPVR 8,47
BATLOW#
PWRBTN# R3 — PWRBTN# 33
LAN_RST# D20 R42 10K_J 0201
PM_RSMRST#_SB R18 2.2K_J 0201 — PM_RSMRST# 33
CK_PWRGD R5 — CK_PWRGD 6
MPWROK R6
PM_SLP_M# B16 — 26MIL TP163
CL_CLK0 F24 — CL_CLK0 8
CL_CLK1 B19 — 26MIL TP170
CL_DATA0 F22 — CL_DATA0 8
CL_DATA1 C19 — 26MIL TP165
CL_VREF0_ICH C25
CL_VREF1_ICH A19
CL_RST0# F21 — CL_RST0# 8
CL_RST1# D18 — 26MIL TP15
TP_GPIO24 A16 — 26MIL TP167
GPIO10 C18
GPIO14 C11
TP_GPIO9 C20 — 26MIL TP168

6,14,15,35 SMB_CLK_SB
6,14,15,35 SMB_DATA_SB
SMB_LINK_ALERT#
SMLINK0
SMLINK1
34,37 PM_SUS_STAT#
34 SB_RST#
8 PM_SYNC#
33 WAKE_SCI#
6 PM_STPPCI#
6 PM_STP_CPU#
33,34,37,39 PM_CLKRUN#
35 PCIE_EXPRESS_WAKE# — R24 0_J 0201
37 PCIE_WAKE#
33,34,37,39 INT_SERIRQ
VRMPWRGD
TP164 26MIL — TP12
37 FP_DET#
34 ID_LPC_PCI#
33 RUNTIME_SCI#
33 EXTSMI#
34 MB_FLASH_EN
GPIO13
ODD_DP#
TP192 26MIL — TP_GPIO18
TP53 26MIL — TP_GPIO20
GPIO22
25 INV_EN
48 ODD_ON
6 SATACLKREQ#
GPIO38
DOCK_SUPPORT
GPIO48
TP207 26MIL — TP_GPIO49
GPIO57
37 HDA_SPKR
8 MCH_ICH_SYNC#
TP166 26MIL — TP3
TP212 26MIL — TP9
TP206 26MIL — TP10
TP208 26MIL — TP11

ID_LPC_PCI#
80 Port I/F:
H: LPC bus
L: PCI bus

+3VRUN
RP38 8.2K RUNTIME_SCI# / ID_LPC_PCI# 0302_4P2R
R382 8.2K_J 0201 SB_THRM#
RP5 8.2K PM_CLKRUN# / INT_SERIRQ 0302_4P2R
R114 10K_J 0201 GPIO48
R381 10K_J 0201 GPIO22
R96 10K_J 0201 ODD_DP#
R60 2.2K_J 0201 SMB_CLK_SB
R331 2.2K_J 0201 SMB_DATA_SB
R116 10K_J 0201 FP_DET#
R583 NC_10K_J 0201 TP_GPIO9
DVT2 1/26 If G3 -> S5 WOL is not supported, GPIO9/WOL_EN can be connected to ground.

+3VRUN
U3 EEPROM_SOP-8_256x8 HT24LC02
VCC WP SCL SDA A0 A1 A2 VSS
C21 0.1U_16V_Y 0402_Y5V
SMB_CLK_SB
SMB_DATA_SB
SMBus Address: AEH

33,47 IMVP_OK — R22 0_J 0201 — VRMPWRGD
R21 100K_J 0201

+3VALW
R15 NC_3.24K_F 0201
CL_VREF1_ICH
C14 NC_0.1U_16V_M_B 0402
R16 NC_453_F 0201

+3VRUN
R37 3.24K_F 0201
CL_VREF0_ICH
C20 0.1U_16V_M_B 0402
R36 453_F 0201

+3VALW
SMB_LINK_ALERT# R55 10K_J 0201
BATLOW# R330 8.2K_J 0201
PCIE_WAKE# R23 1K_J 0201
GPIO10 R333 10K_J 0201
GPIO14 R41 10K_J 0201

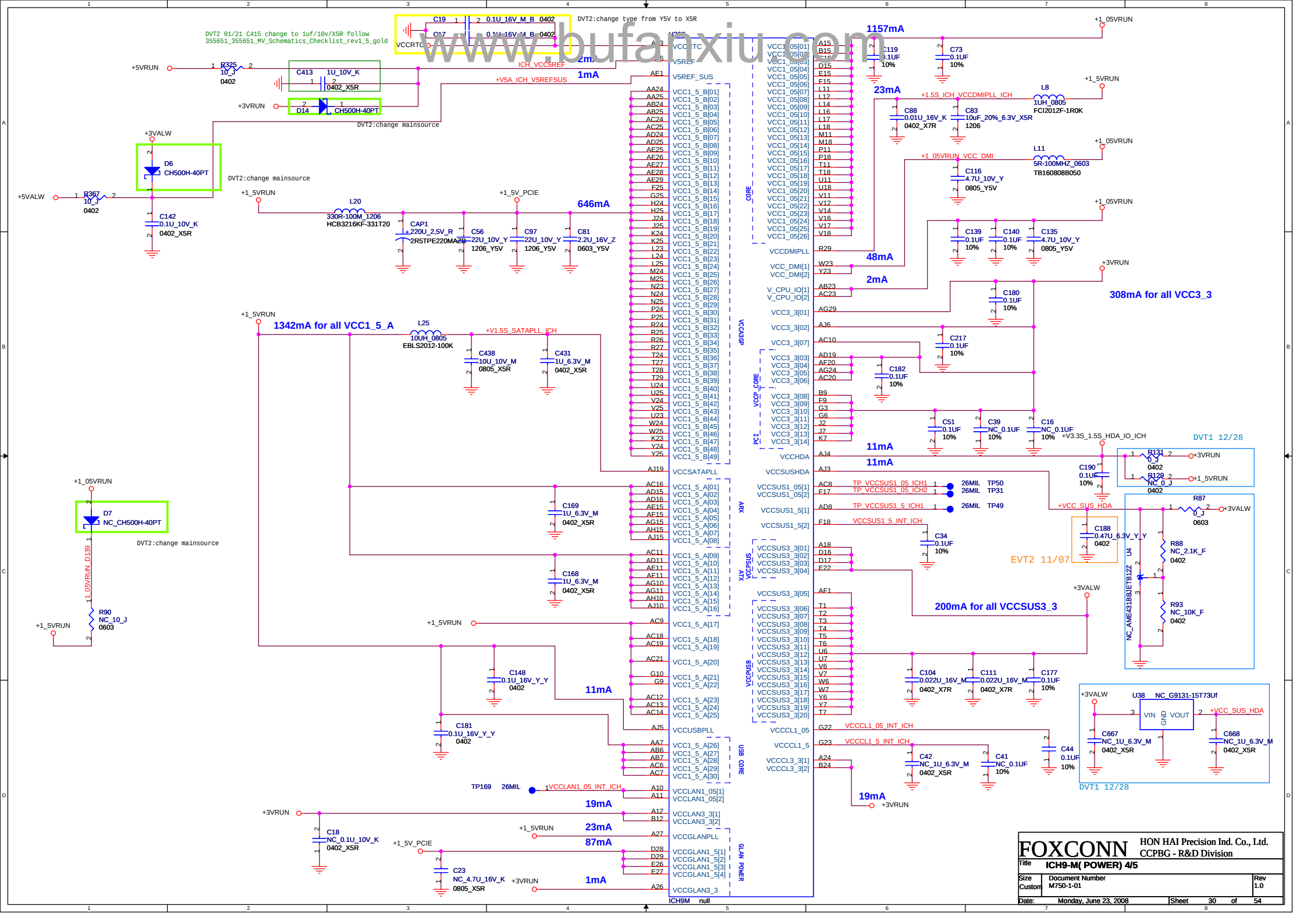
D5 BAS316PT
PM_RSMRST#_SB 2 — 1 — ALW_PWRGD 33,44
D4 BAS316PT
IMVP_PWRGD_SB 2 — 1

+3VRUN
PANEL_ID0 R95 10K_J 0201
PANEL_ID1 R383 10K_J 0201
ID0_PU R134 NC_10K_J 0201
ID1_PU R141 NC_10K_J 0201
GPIO38 R115 10K_J 0201
DOCK_SUPPORT R121 DS_10K_J 0201
R586 ND_10K_J 0201
12/27 DVT1

1/29 DVT2
CLK_USB48
R371 NC_10_J 0402
1 CLK_USB48_R 2
C423 NC_10P_50V_J_N 0402

MPWROK 8
MPWROK — R82 0_J 0201 — IMVP_PWRGD

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ICH9-M(GPIO) 3/5		
Size A3	Document Number M750-1-01		Rev 1.0
Date: Monday, June 23, 2008		Sheet 29 of 54	


www.bufanxiu.com
DVT2 01/21 C415 change to 1uf/10v/X5R follow 355651_355651_MV_Schematics_Checklist_rev1_5_gold
DVT2:change type from Y5V to X5R
DVT2:change mainsource
1157mA
23mA
48mA
2mA
646mA
1342mA for all VCC1_5_A
308mA for all VCC3_3
200mA for all VCCSUS3_3
11mA
19mA
87mA
1mA
EVT2 11/07
DVT1 12/28
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
ICH9-M(POWER) 4/5
Document Number M750-1-01
Rev 1.0
Monday, June 23, 2008
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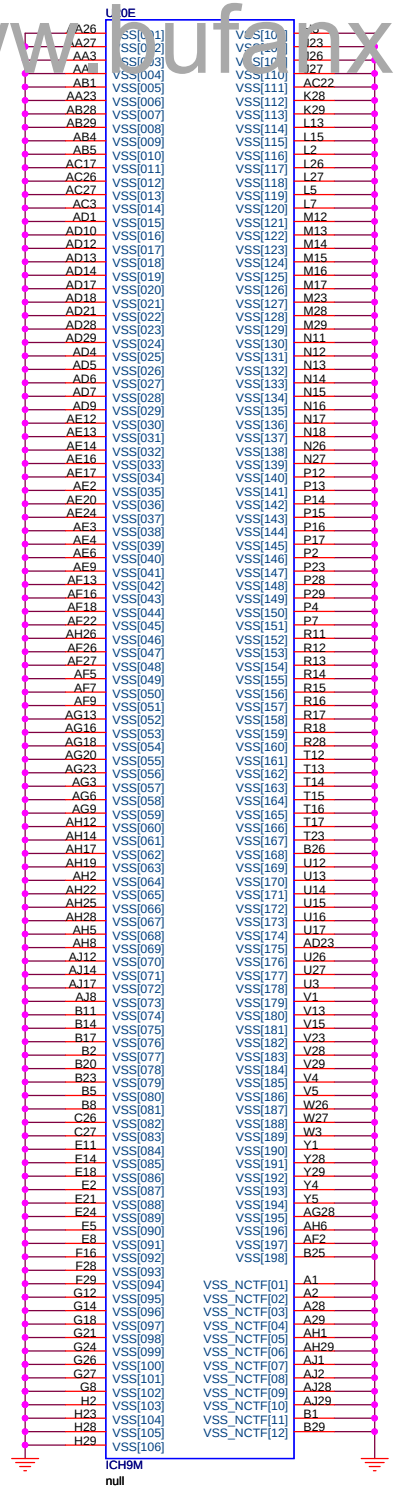
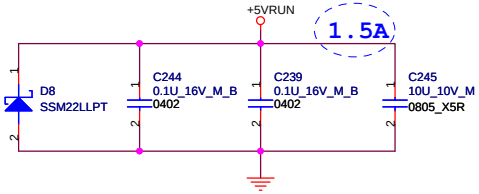
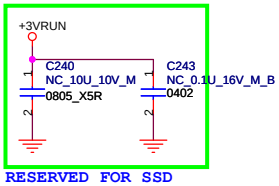
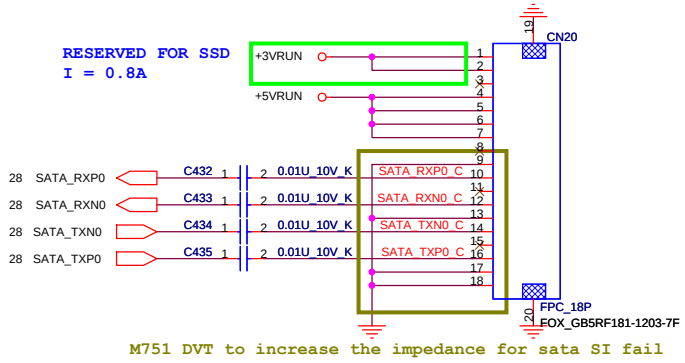


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ICH9-M(GND) 5/5	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 31 of 54	

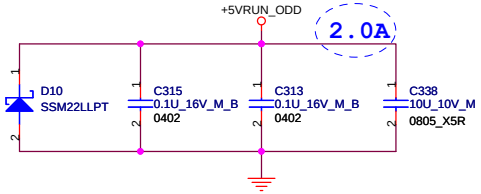


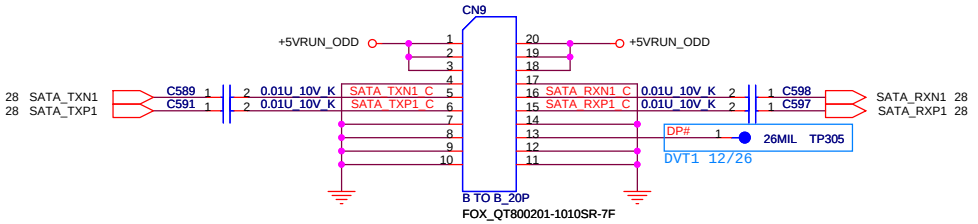




M751 DVT to increase the impedance for sata SI fail

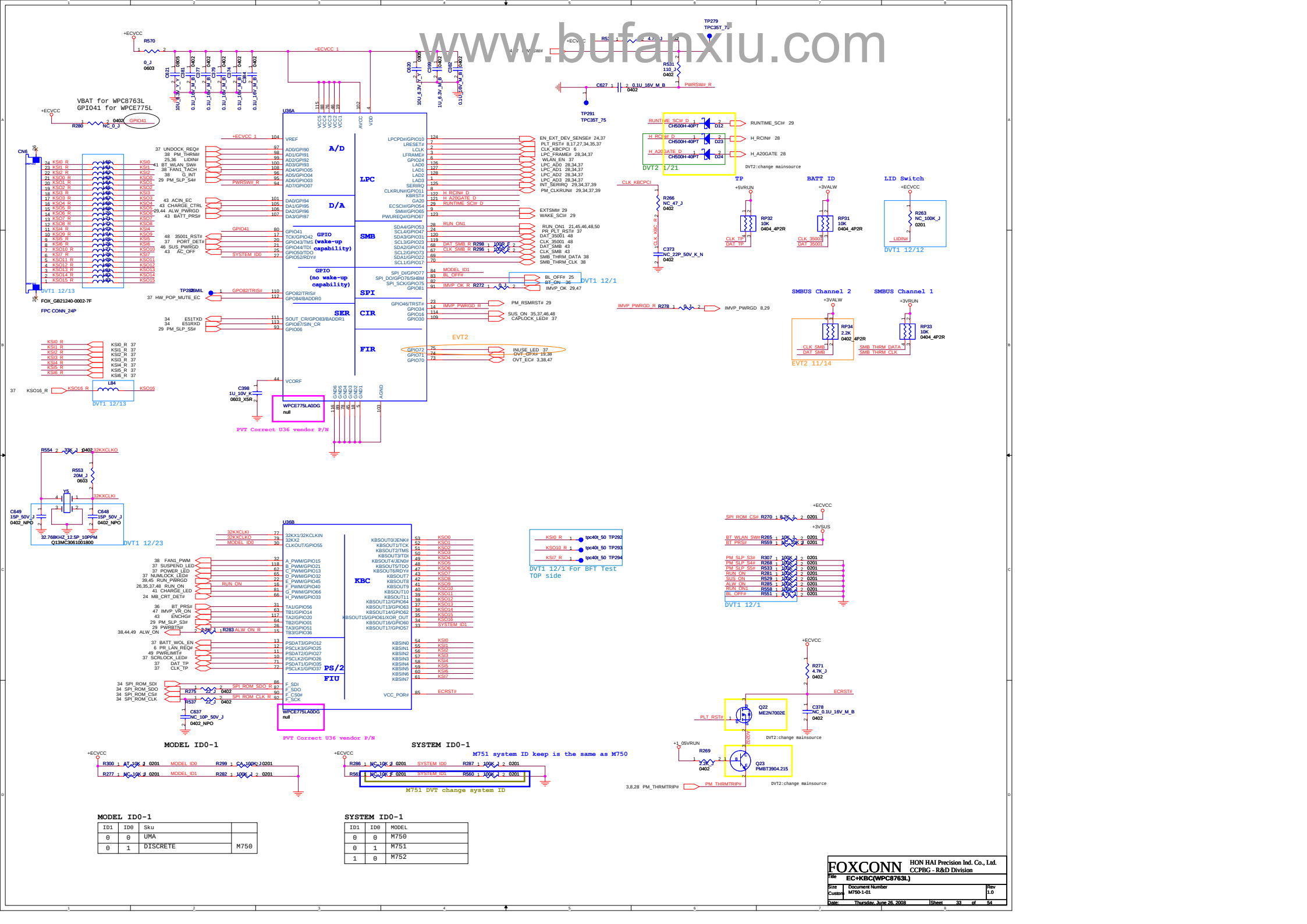
SATA HDD CONN





SATA ODD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD/ODD		
Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet 32 of 54	



MODEL ID0-1

ID1	ID0	Sku	
0	0	UMA	M750
0	1	DISCRETE	

SYSTEM ID0-1

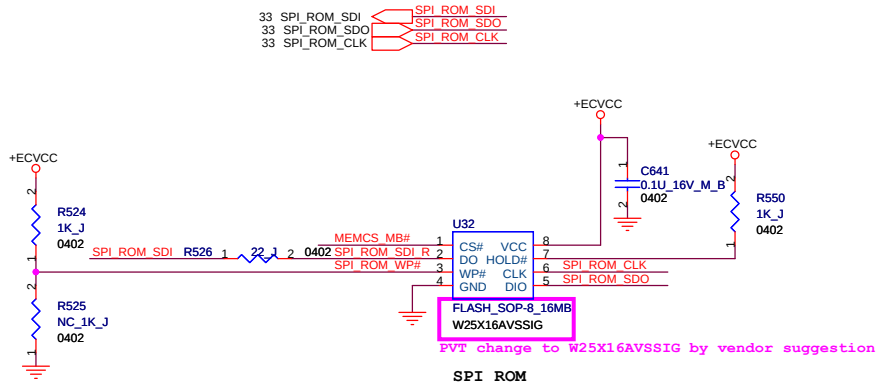
ID1	ID0	MODEL
0	0	M750
0	1	M751
1	0	M752

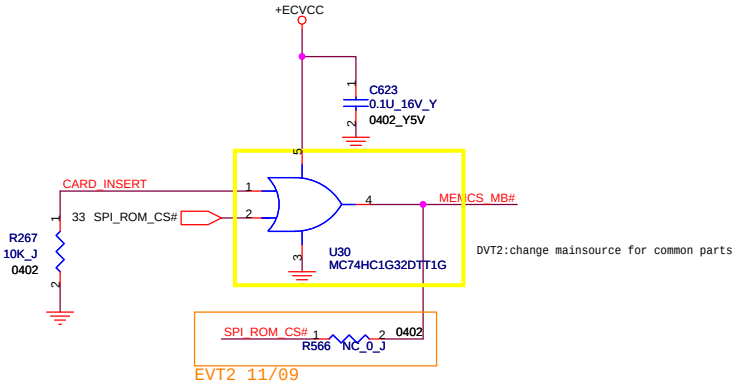
FOXCONN — HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

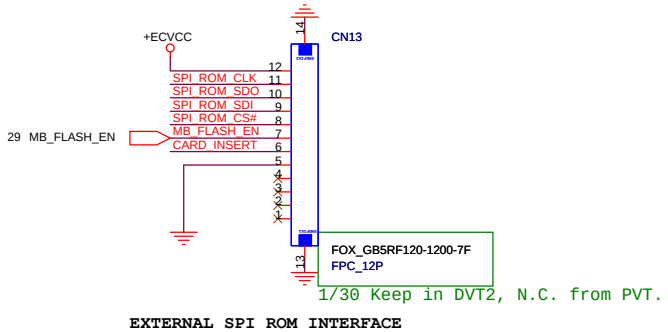
File: EC+KBC(WPC8763L)

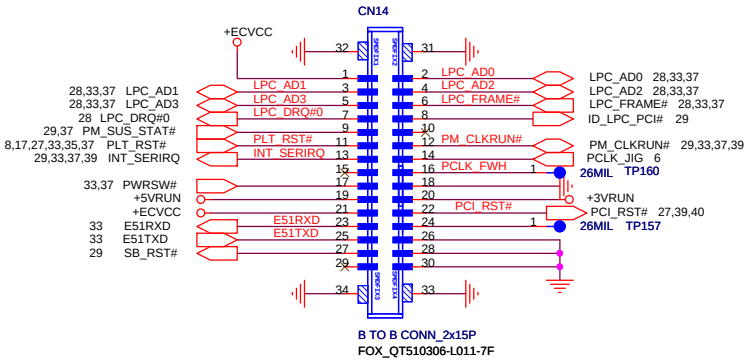
Size: Custom | Document Number: M750-1-01 | Rev: 1.0

Date: Thursday, June 26, 2008 | Sheet 33 of 54





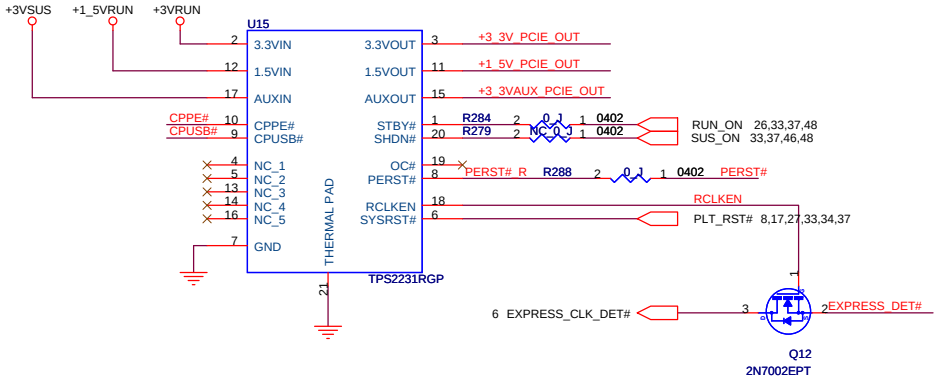


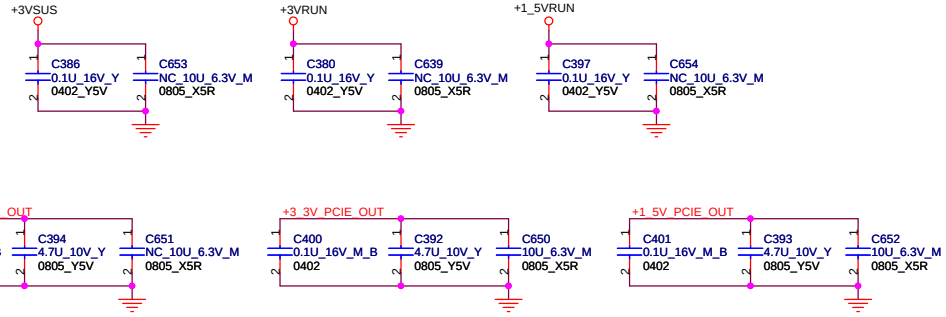


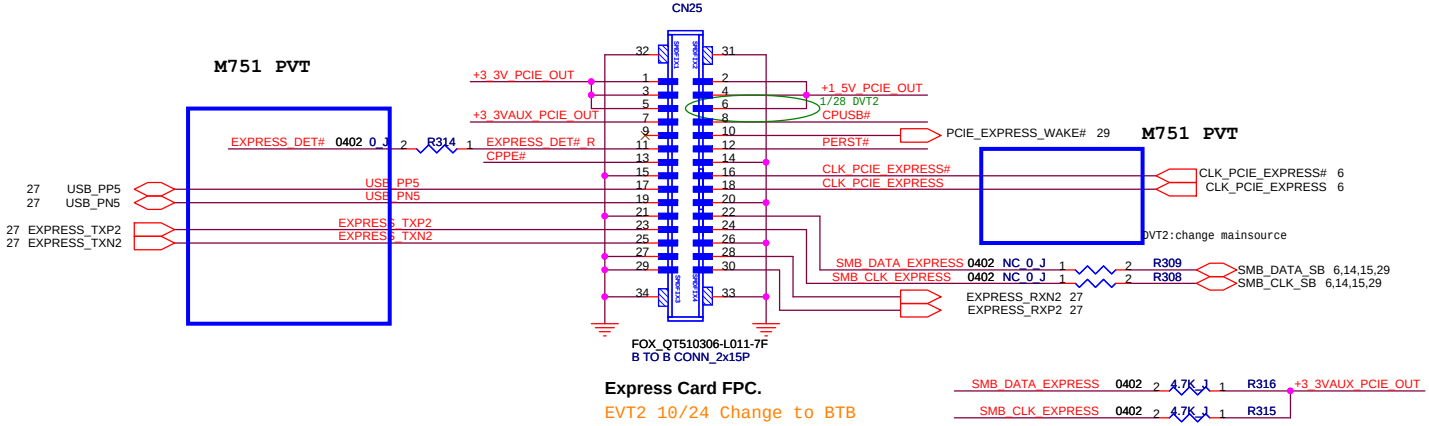
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	BIOS ROM/DEBUG PORT	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 34 of 54	

+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A

Express Card Power Switch



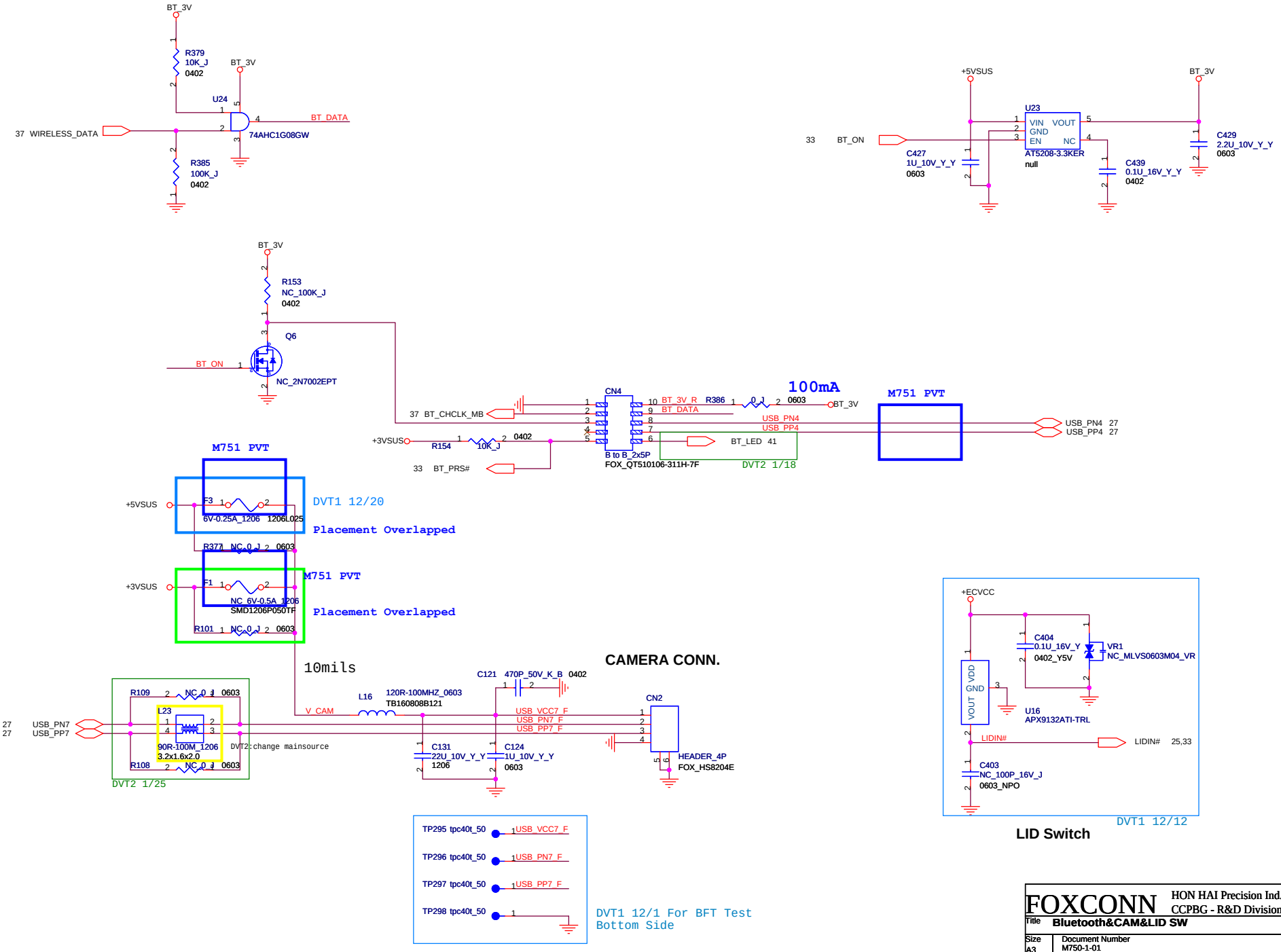




Express Card FPC.

EVT2 10/24 Change to BTB

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EXPRESS CARD	
Size A3	Document Number M750-1-01	Rev 0.1
Date: Monday, June 23, 2008	Sheet 35 of 54	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Bluetooth&CAM&LID SW	
Size A3	Document Number M750-1-01	Rev 1.0
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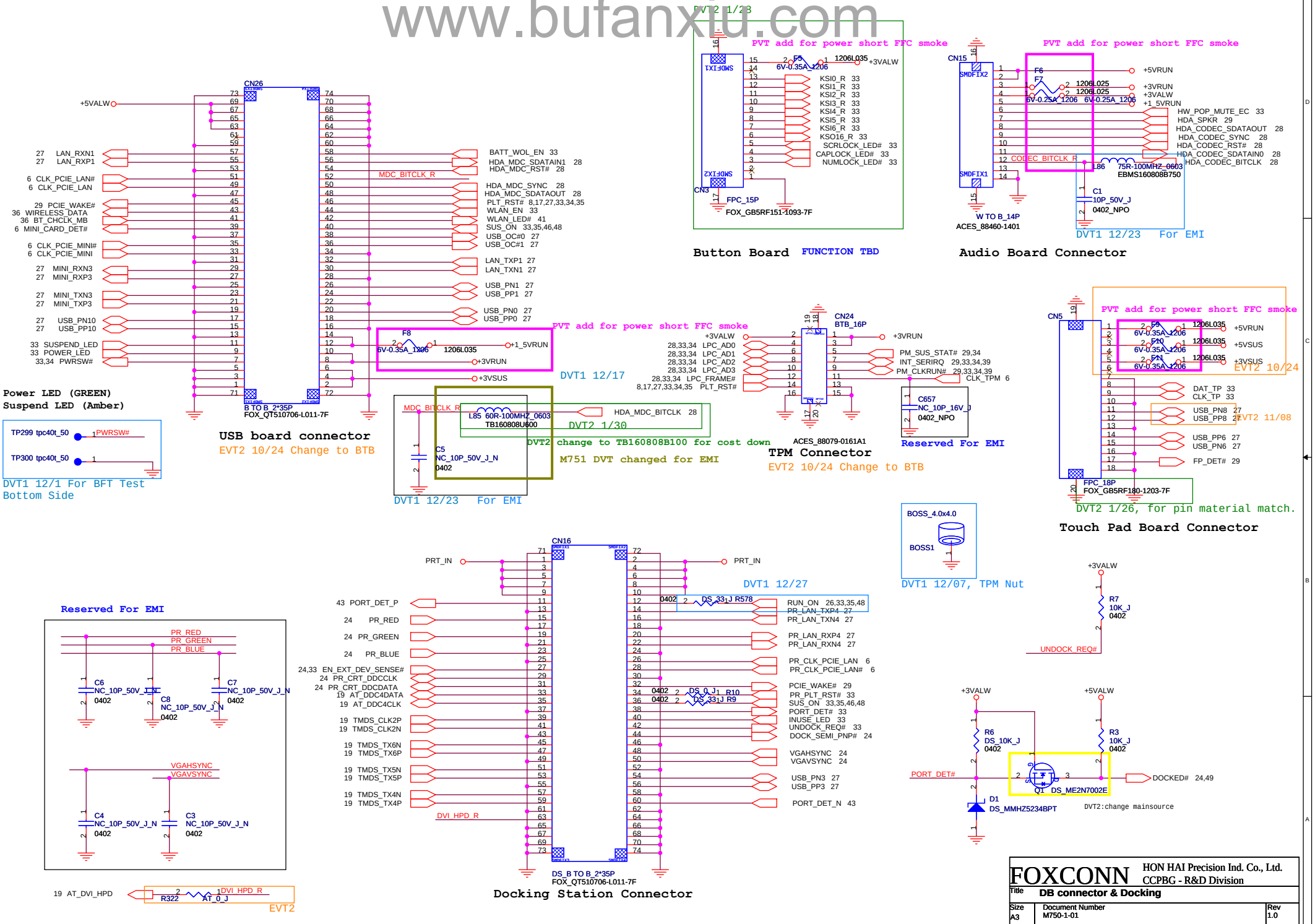
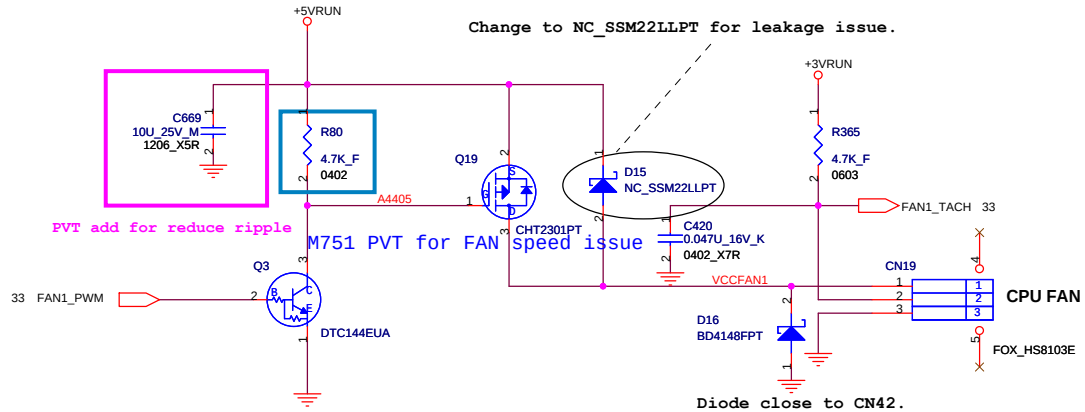
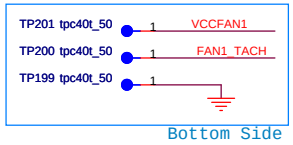
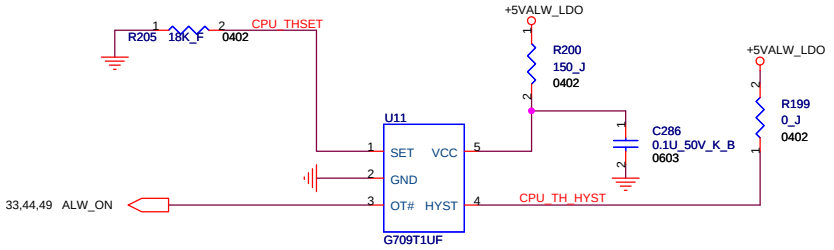


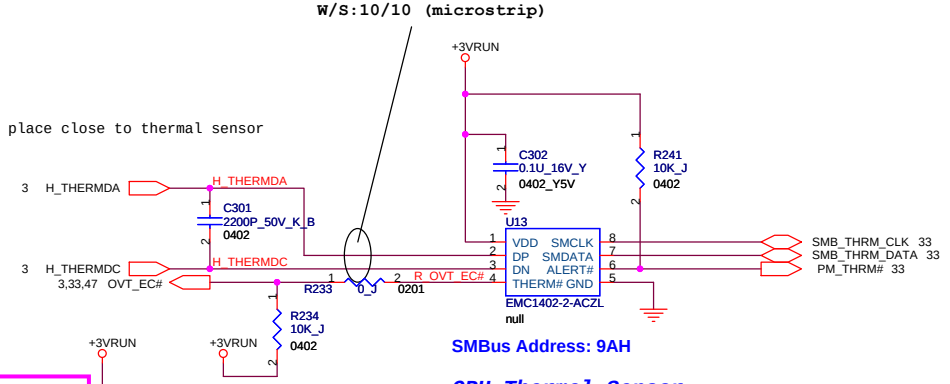
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DB connector & Docking	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 37 of 54	

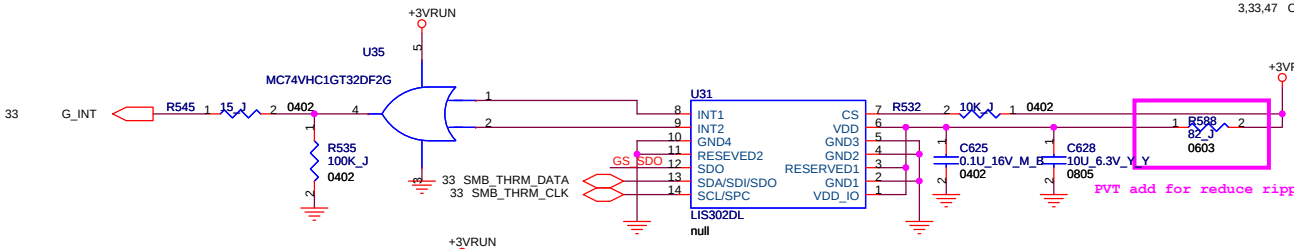
HW THERMAL PROTECTION

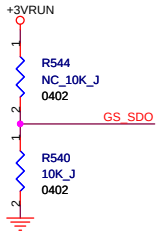


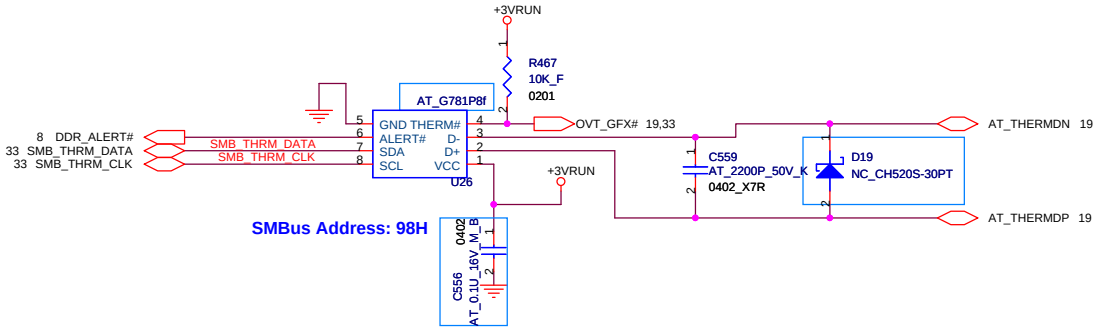












FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN/Thermal & G-Sensor	
Size A3	Document Number M750-1-01	Rev 1.0
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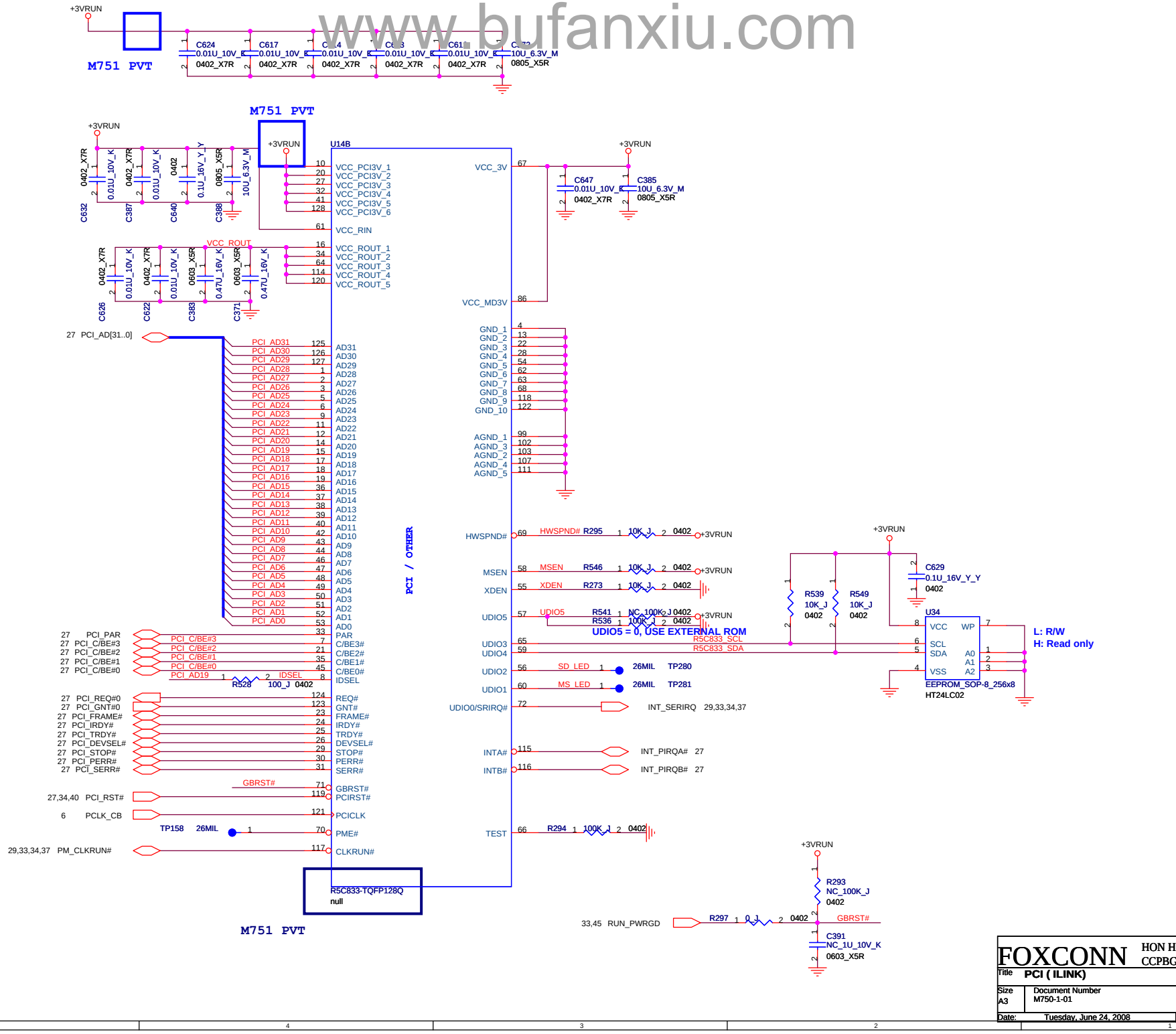

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	PCI (ILINK)	
Size A3	Document Number M750-1-01	Rev 1.0
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M751 PVT

U14A

IEEE1394/SD

XOUT R
R290 0_J 0402
XOUT
R289 NC_10M_J 0402
Y1
XIN
24.576MHZ_16P_30PPM
ITTI_L5030-24.576-16
C390 0402_NPO 22P_50V_J
C389 0402_NPO 22P_50V_J
EVT2 11/14
XIN 94 XI
XOUT 95 XO
96 FIL0
R548 10K_F 0402 833_REXT 101 REXT
C645 0.01U_10V_K 0402_X7R 833_VREF 100 VREF
Add net name
97 RSV
R5C833-TQFP128Q
null
M751 PVT

AVCC_833
C375 10U_6.3V_M 0805_X5R
C634 0.1U_16V_Y_Y 0402
C630 1000P_50V_M_B 0402
C646 0.01U_10V_K 0402_X7R
L39 120R-100MHZ_0603 EBMS160808A121
AVCC_PHY3V_1 98
AVCC_PHY3V_2 106
AVCC_PHY3V_3 110
AVCC_PHY3V 112
TPBIAS0 113
C631 0.22U_6.3V_K 0402_X5R
C633 0.1U_10V_K 0402_X7R
HEIGHT LIMIT: 0.8mm
R538 56.2_F 0402
R534 56.2_F 0402
TPBN0 104 TPB0-
TPBP0 105 TPB0+
TPAN0 108 TPA0-
TPAP0 109 TPA0+
L57 90R-100M_1206 3.2x1.6x2.0
L56 90R-100M_1206 3.2x1.6x2.0
TPB- TPB+ TPA- TPA+
R542 56.2_F 0402
R547 56.2_F 0402
C638 270P_50V_K 0402_NPO
R543 5.1K_F 0402
AS CLOSE AS POSSIBLE TO R5C833

1394_AGND
CN8 1394_4P FOX_UV31413-WU92P-7F
L87 600R-100MHZ_0603 EBMS160808A601
L88 NC_600R-100MHZ_0603 EBMS160808A601
iLink CONN.
PVT add for EMI

+3VRUN
C636 NC_10U_6.3V_M 0805_X5R
C635 10U_6.3V_M 0805_X5R
U33 BD2056AFJ
MSPWR_EN
SDPWR_EN
MS/SD POWER

VCC_CTRLMS
C325 2.2U_10V_M 0603_X5R
C330 0.1U_16V_Y_Y 0402
R253 150K_J 0402
VCC_CTRLSD
C610 1U_6.3V_M 0402_X5R
C615 1U_6.3V_M 0402_X5R
C619 0.1U_16V_Y_Y 0402
R527 150K_J 0402
HEIGHT LIMIT: 0.8mm

MDIO17(MMC)(SD/MS)(xD) 87 MS_DATA3 R574 68_J 0402 MS_DATA3_R
MDIO16(MMC)(SD/MS)(xD) 92 MS_DATA2 R573 68_J 0402 MS_DATA2_R
MDIO15(MMC)(SD/MS)(xD) 89 MS_DATA1 R575 68_J 0402 MS_DATA1_R
MDIO14(MMC)(SD/MS)(xD) 91 MS_DATA0 R576 68_J 0402 MS_DATA0_R
DVT1 1/2 (Close to U14)
MDIO13(SD/MMC)(MS)(xD) 90 SD_DATA3
MDIO12(SD/MMC)(MS)(xD) 93 SD_DATA2
MDIO11(SD/MMC)(MS)(xD) 81 SD_DATA1
MDIO10(SD/MMC)(MS)(xD) 82 SD_DATA0
MS_BS R577 68_J 0402 MS_BS_R
DVT1 1/2 (Close to U14)
MDIO05(SD/MMC)(MS)(xD) 75 MSPWR_EN
MDIO08(SD/MMC)(MS)(xD) 88 SD_CMD
MDIO19(MMC/SD/MS)(xD) 83 R291 33_J 0402 MS_CLK
MDIO18(MMC/SD/MS)(xD) 85 MS_BS
MDIO02(MMC/SD/MS)(xD) 78
C395 NC_10P_16V_J 0402_NPO
MDIO03 77 SD_WP
MDIO00 80 SD_CD#
MDIO01 79 MS_INS#
MDIO09(SD/MMC/MS)(xD) 84 R292 33_J 0402 SD_CLK
C396 NC_10P_16V_J 0402_NPO
MDIO04 76 SDPWR_EN
MDIO06 74 MEDIA_LED
MDIO07 73

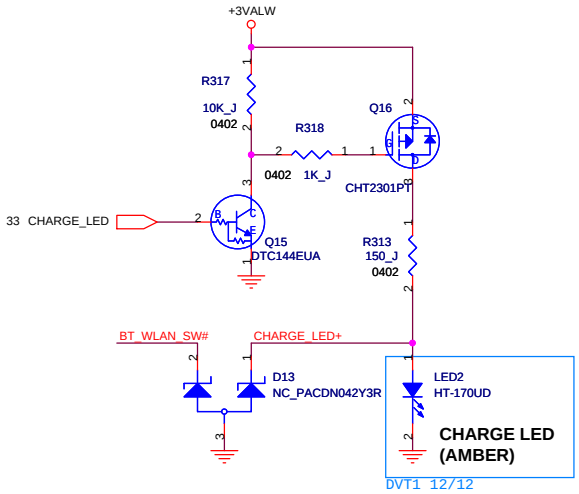
+3VRUN
R556 4.7K_J 0402 MS_INS#
R555 4.7K_J 0402 SD_CD#
R557 4.7K_J 0402 SD_WP
C643 1000P_50V_M_B 0402
C642 1000P_50V_M_B 0402
C644 1000P_50V_M_B 0402
DVT1 12/20

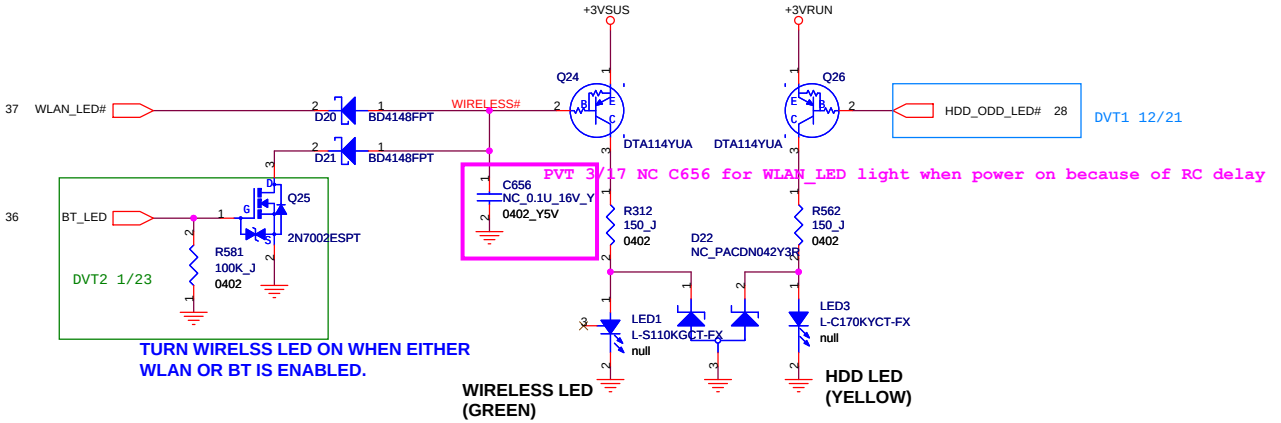
DVT1 1/2
MS_BS_R R510 0_J 0402
MS_DATA1_R R509 0_J 0402
MS_DATA0_R R508 0_J 0402
MS_DATA2_R R507 0_J 0402
MS_INS# MS_DATA3_R R506 0_J 0402
MS_CLK
VCC_CTRLMS
C594 NC_22P_50V_K 0402_NPO
CN10 SOCKET_10P YAMAICHI_JCS010-2300-0
MS STD/DUO CONN.
EVT2

SD_WP SD_CD# SD_DATA1 R523 33_J 0402 SD_DATA0 R522 33_J 0402
SD_CLK
C618 NC_22P_50V_K 0402_NPO
VCC_CTRLSD
SD_CMD R521 33_J 0402 SD_DATA3 R520 33_J 0402 SD_DATA2 R519 33_J 0402
CN11 SD SOCKET_9P FOX_WK21923-S6P-7F
SD CONN.

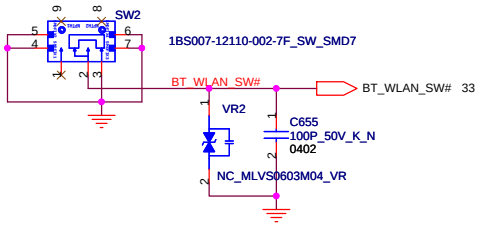
+3VRUN
R310 150_J 0402
LED4 HT-110UY null
MS/SD LED (YELLOW)
EVT2 11/08
DVT add Q30 for cost down
need change EEPROM
Q30 NC_DTA114YUA
Q13 DTC144EUA
MEDIA_LED
MEDIA_LED_1
R589 20K_F 0402
27,34,39 PCI_RST#
C672 4.7U_6.3V_K 0603_X5R
C670 0.1U_16V_Y_Y 0402
U39 74AHC1G08GW
PVT add for MEDIA_LED have high pulse cause the MS/SD LED light when power on 0328

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title PCI (ILINK&MS&SD)
Size A3 Document Number M750-1-01 Rev 1.0
Date: Thursday, June 26, 2008 Sheet 40 of 54

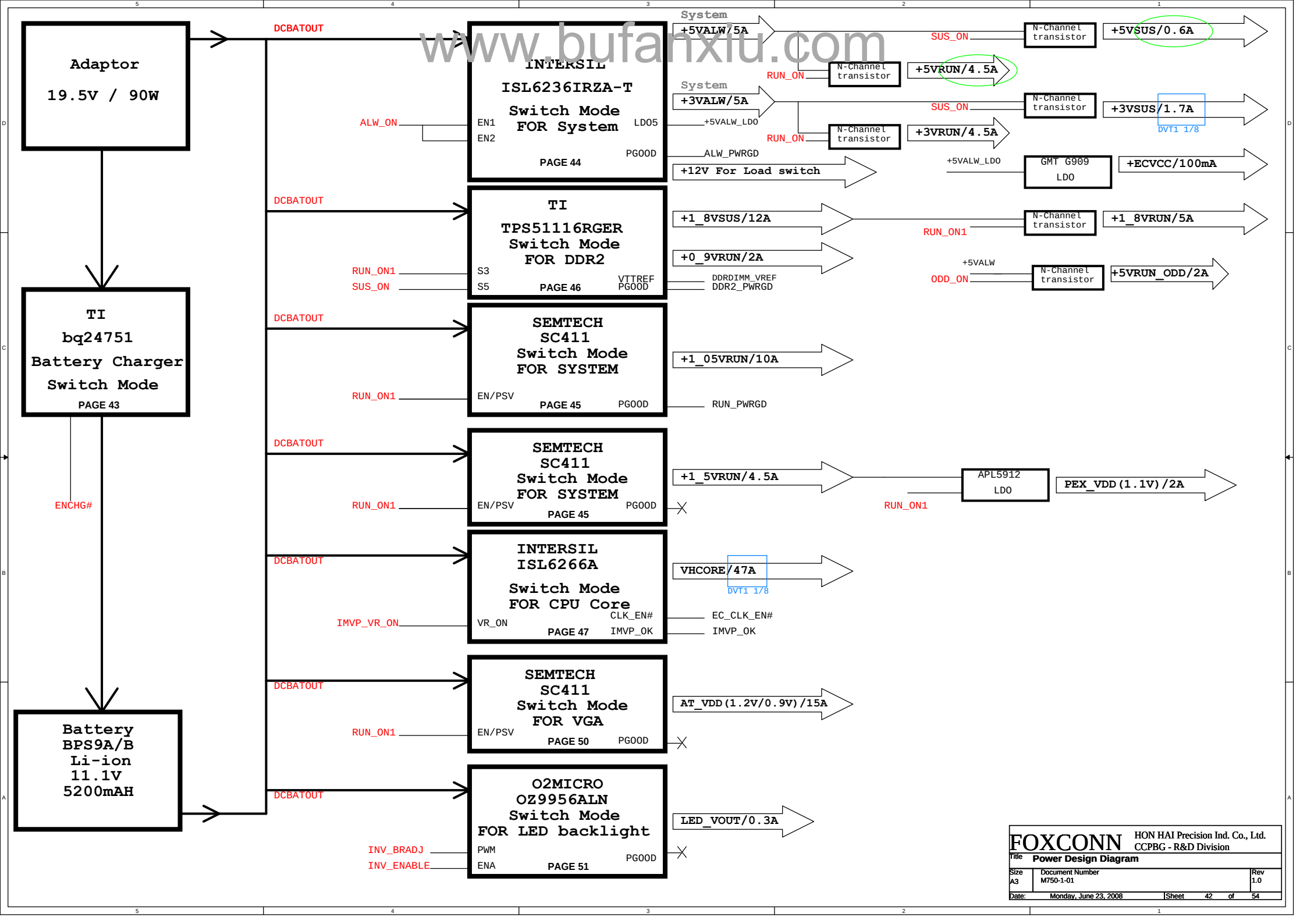




WLAN/BT ON/OFF SWITCH



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: LED & Switch		
Size: A3	Document Number: M750-1-01	Rev: 1.0
Date: Monday, June 23, 2008	Sheet 41 of 54	



FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Power Design Diagram	
Size A3	Document Number M750-1-01	Rev 1.0
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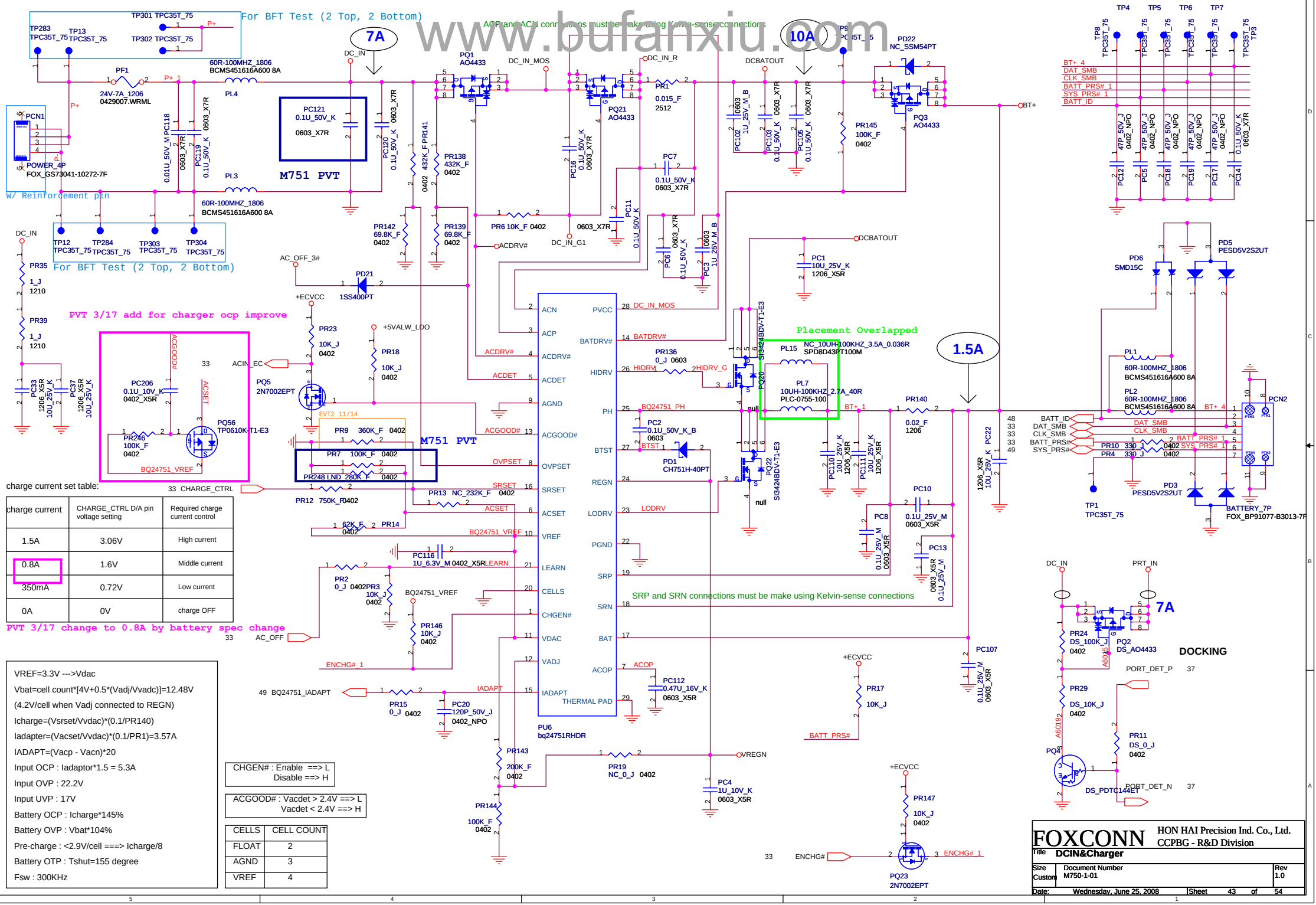


charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

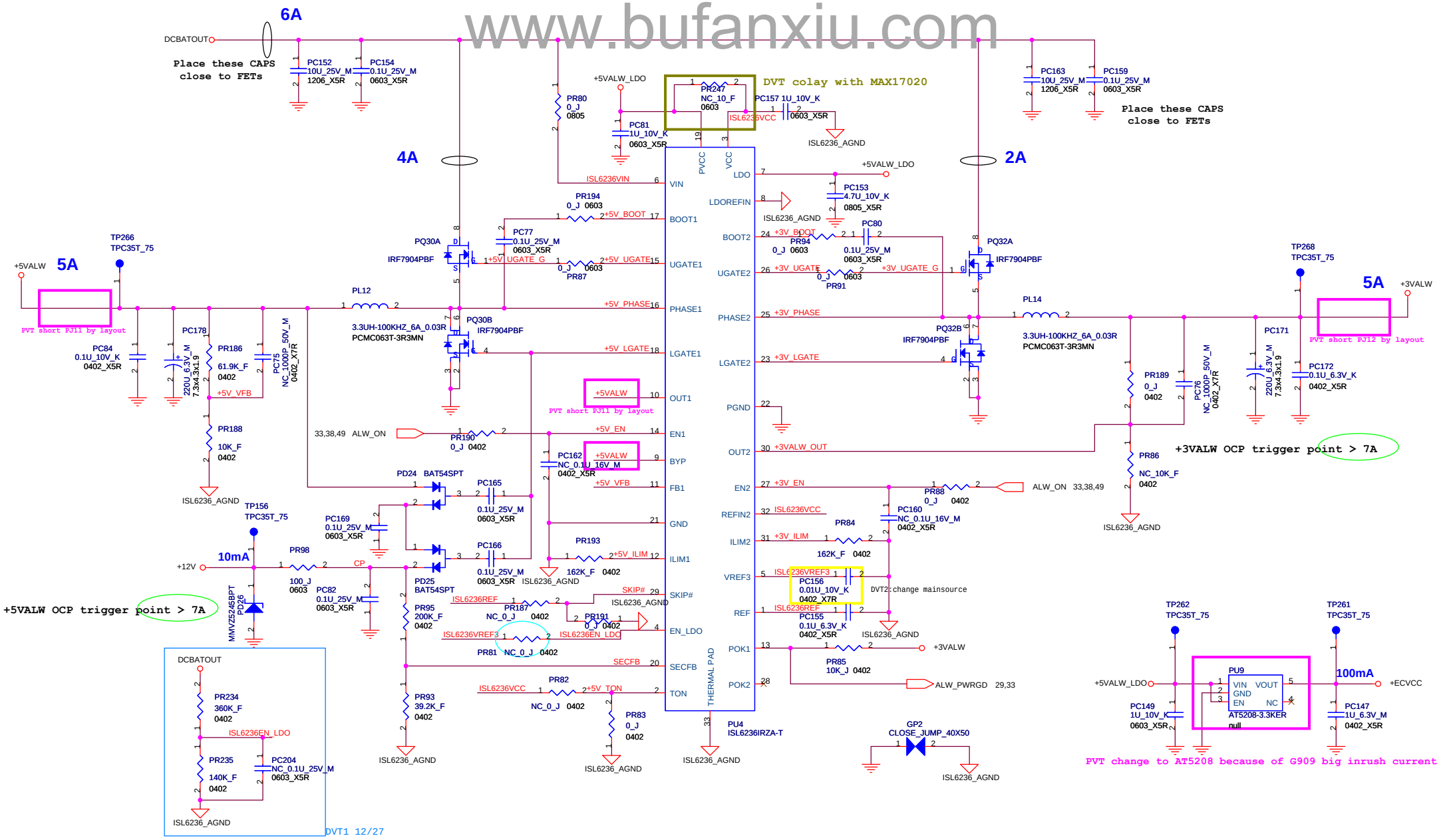
VREF=3.3V --->Vdac
Vbat=cell count*[4V+0.5*(Vadj/Vvadc)]=12.48V
(4.2V/cell when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR140)
Iadapter=(Vacset/Vvdac)*(0.1/PR1)=3.57A
IADAPT=(Vacp - Vacn)*20
Input OCP : Iadaptor*1.5 = 5.3A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz

CHGEN# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

Title	DCIN&Charger		
Size	Document Number		Rev
Custom	M750-1-01		1.0
Date:	Wednesday, June 25, 2008	Sheet 43 of 54	



TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR186/PR188)+1)*VFB1

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: SYS Power (+3_3V/+5V)

Size	Document Number	Rev
A3	M750-1-01	1.0

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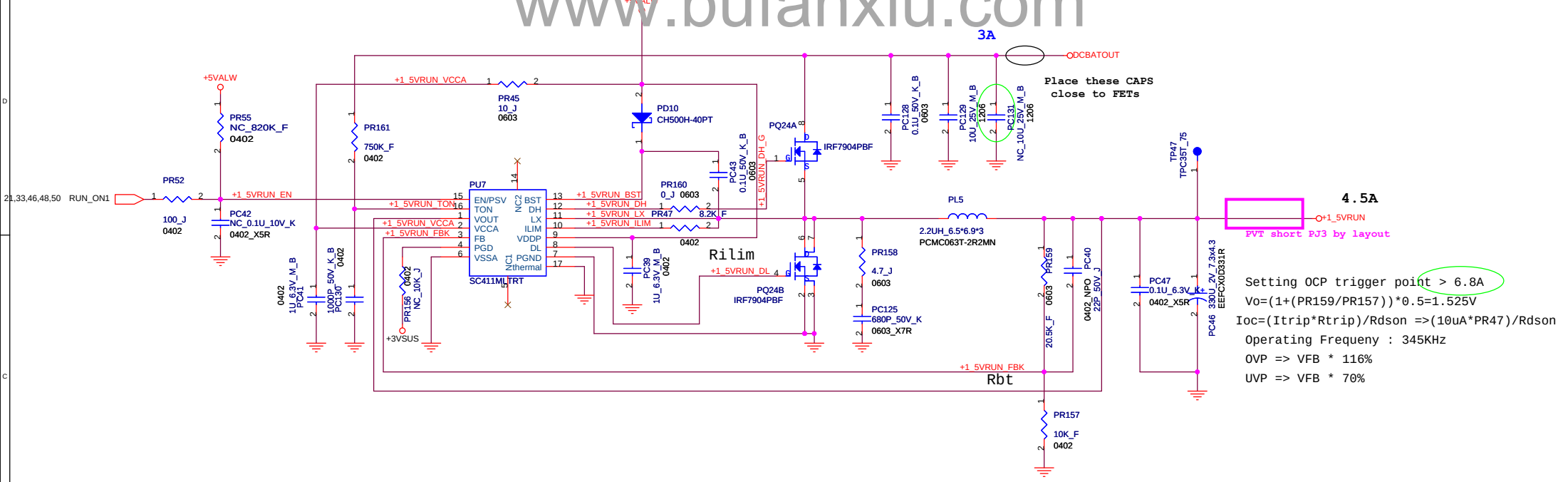
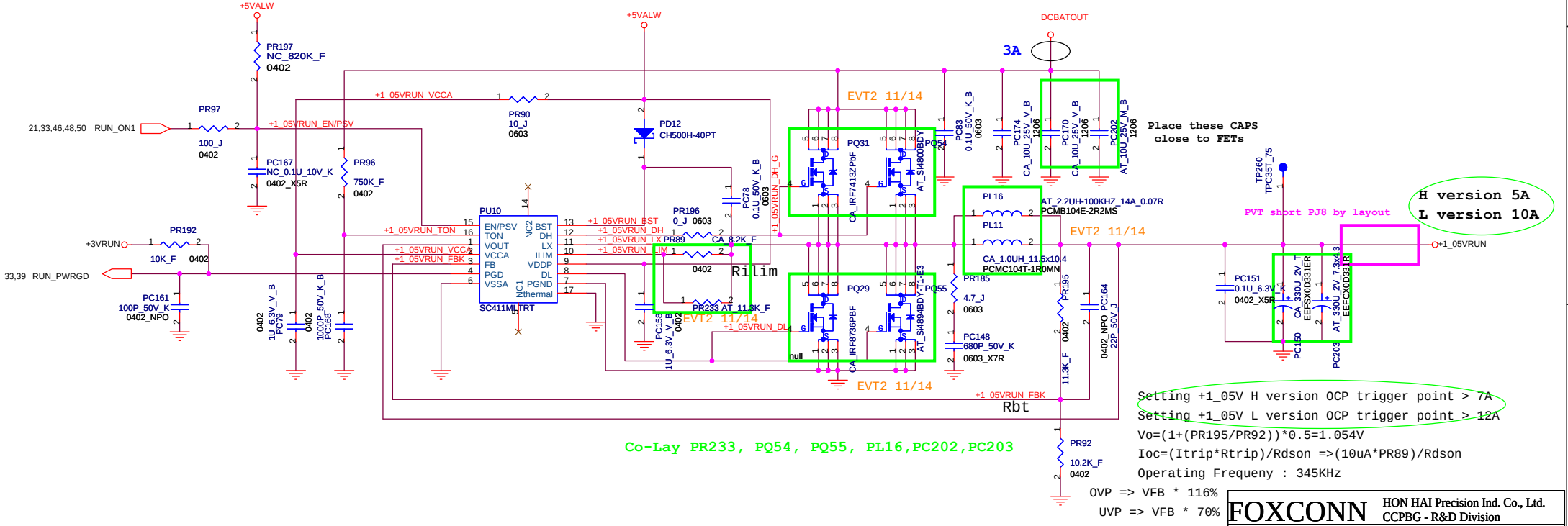
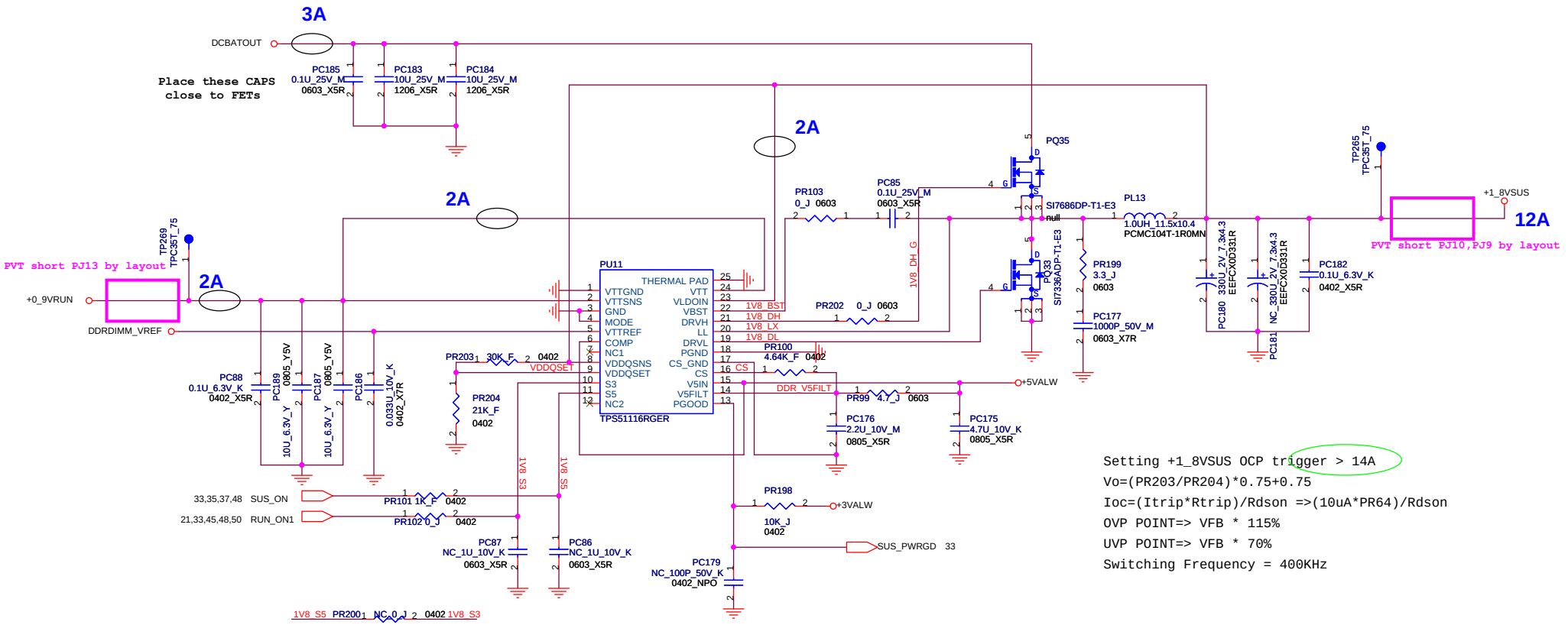




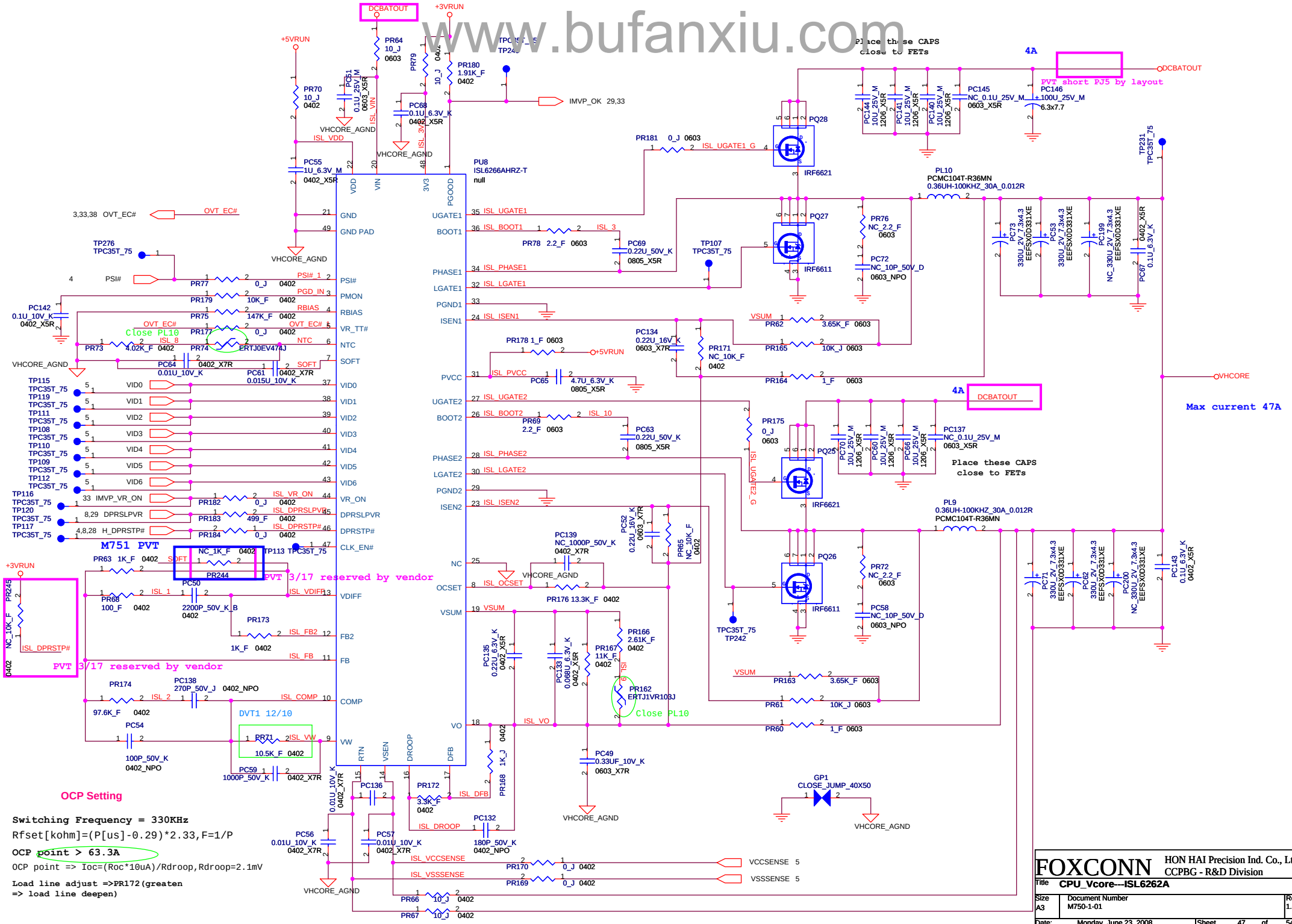
FOXCONN — HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title	SYS Power(+1_5V/+1_05V)	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 45 of 54	



Setting +1_8VSUS OCP trigger > 14A
Vo=(PR203/PR204)*0.75+0.75
Ioc=(Itrip*Rtrip)/Rdson =>(10uA*PR64)/Rdson
OVP POINT=> VFB * 115%
UVP POINT=> VFB * 70%
Switching Frequency = 400KHz

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR2 Power(+1_8V/+0_9V)	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 46 of 54	



OCP Setting

Switching Frequency = 330KHz

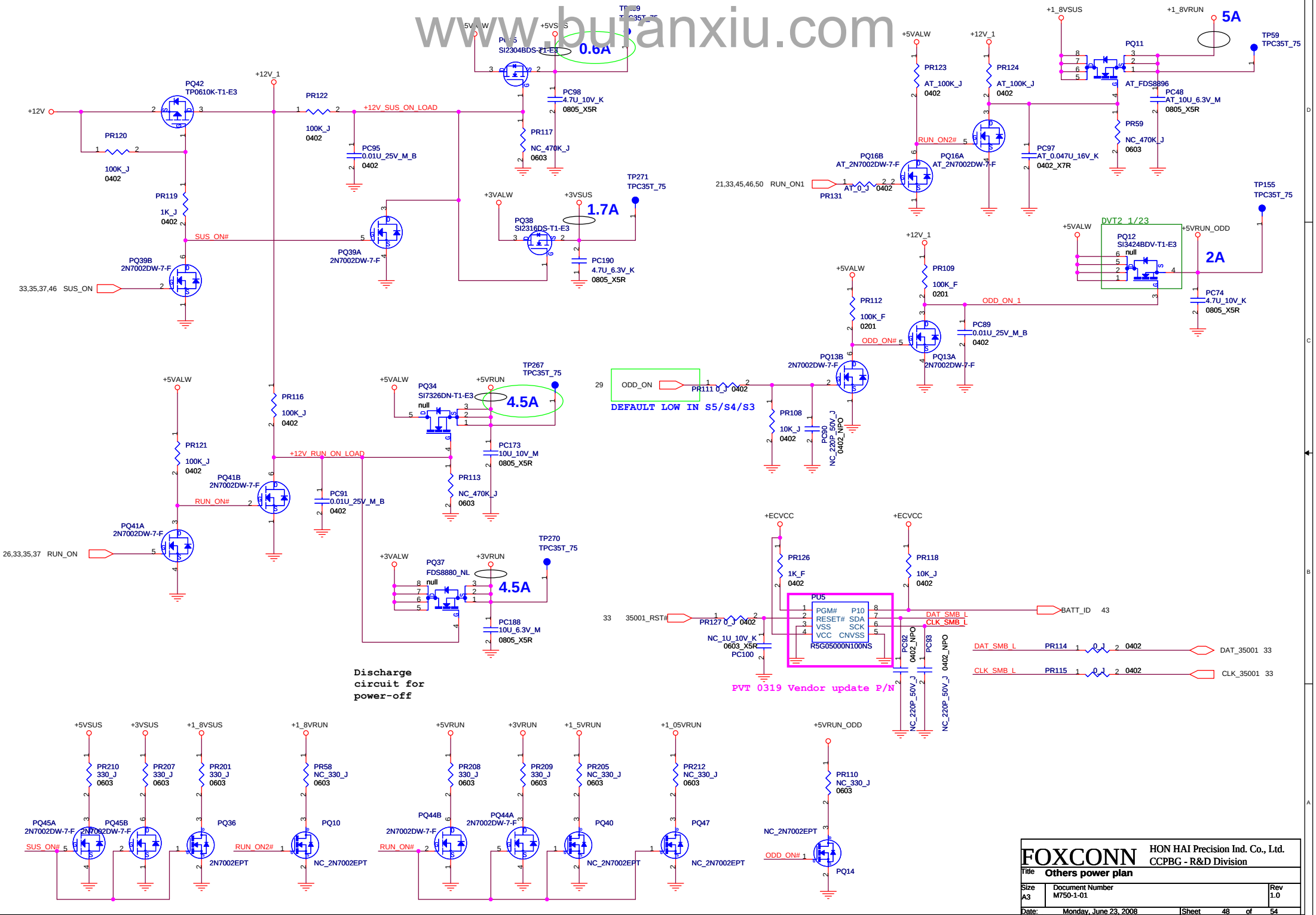
Rfset[kohm]=(P[us]-0.29)*2.33,F=1/P

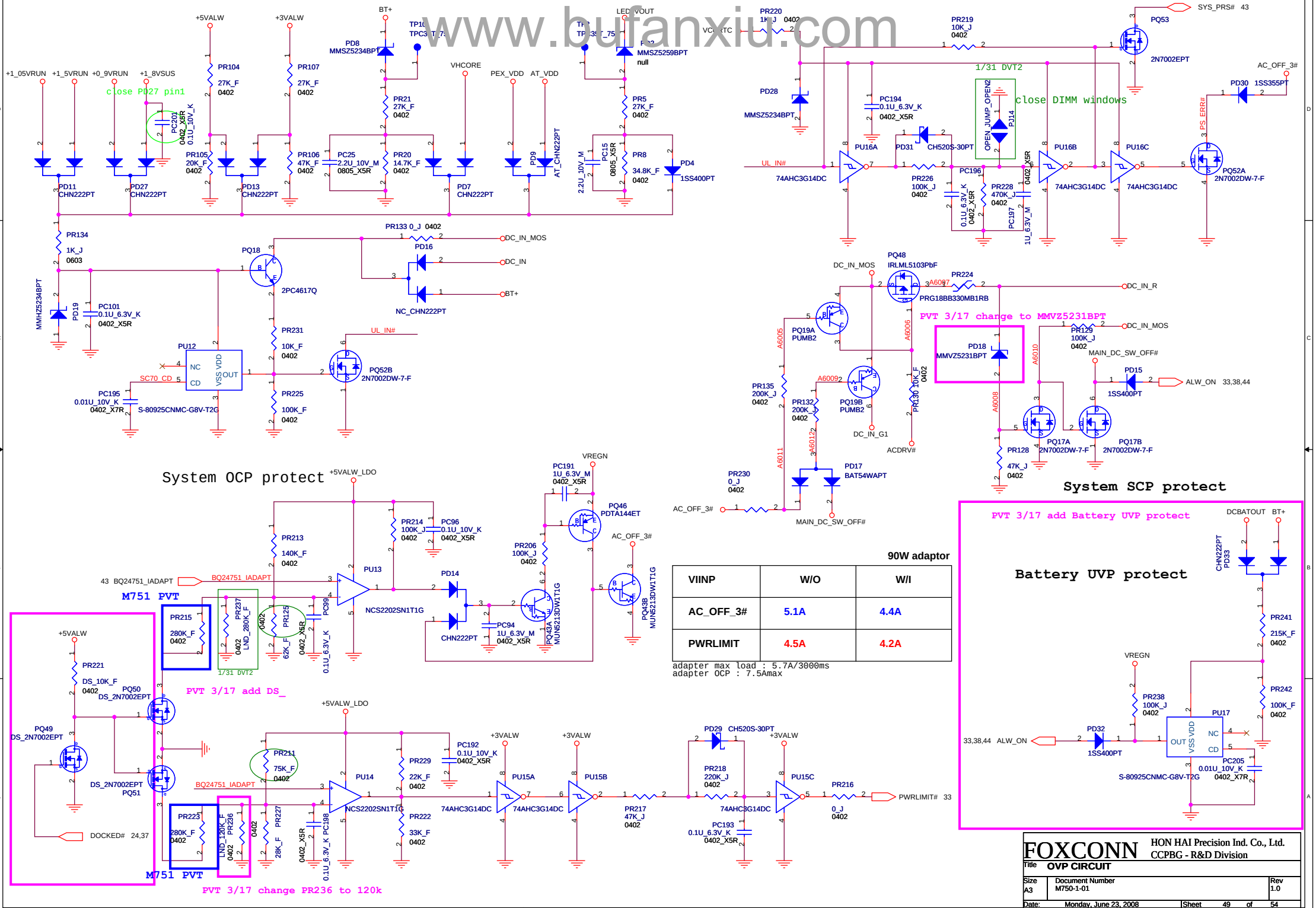
OCP point > 63.3A

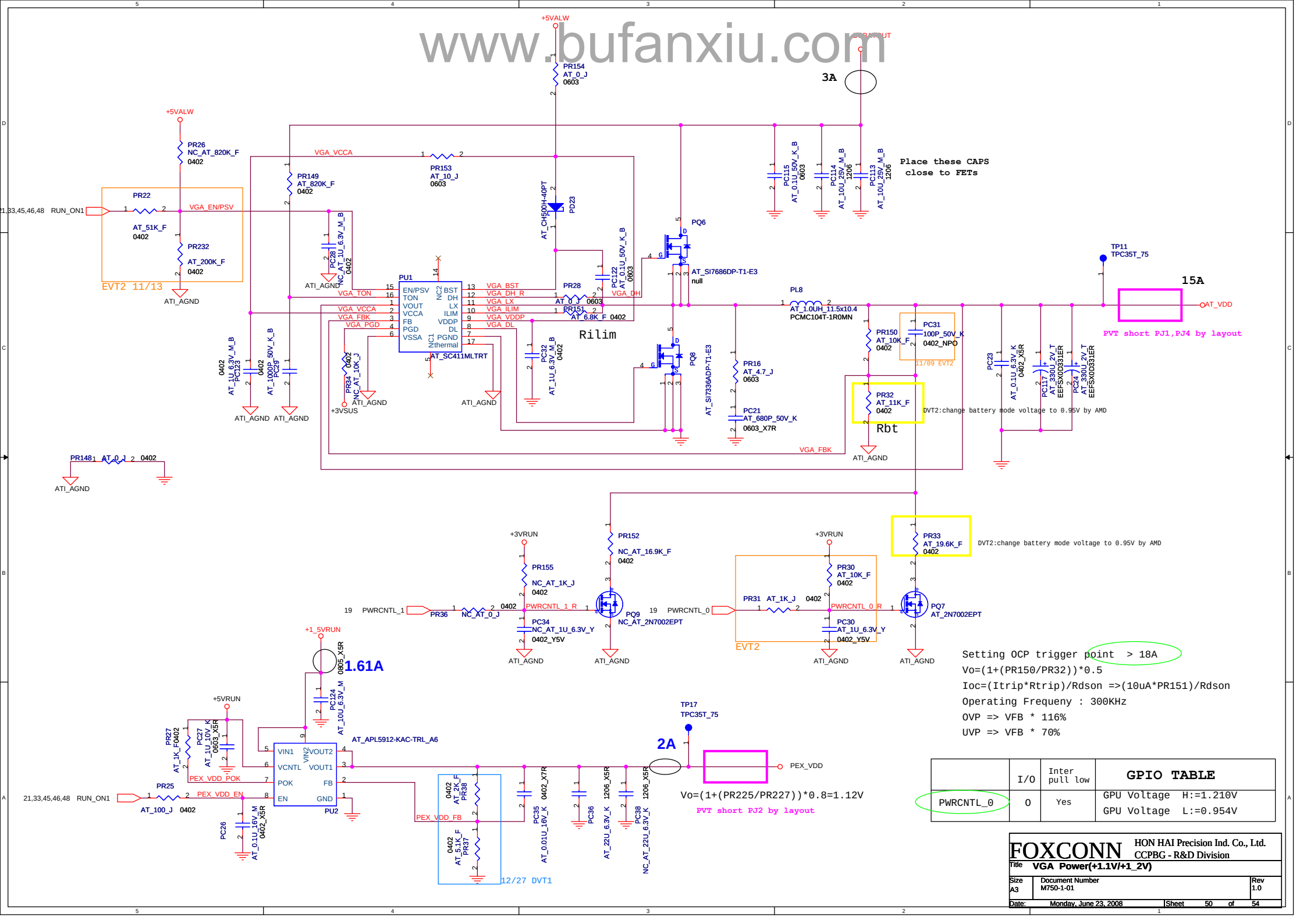
OCP point => Ioc=(Roc*10uA)/Rdroop,Rdroop=2.1mV

Load line adjust =>PR172(greaten => load line deepen)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CPU_Vcore---ISL6262A	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 47 of 54	



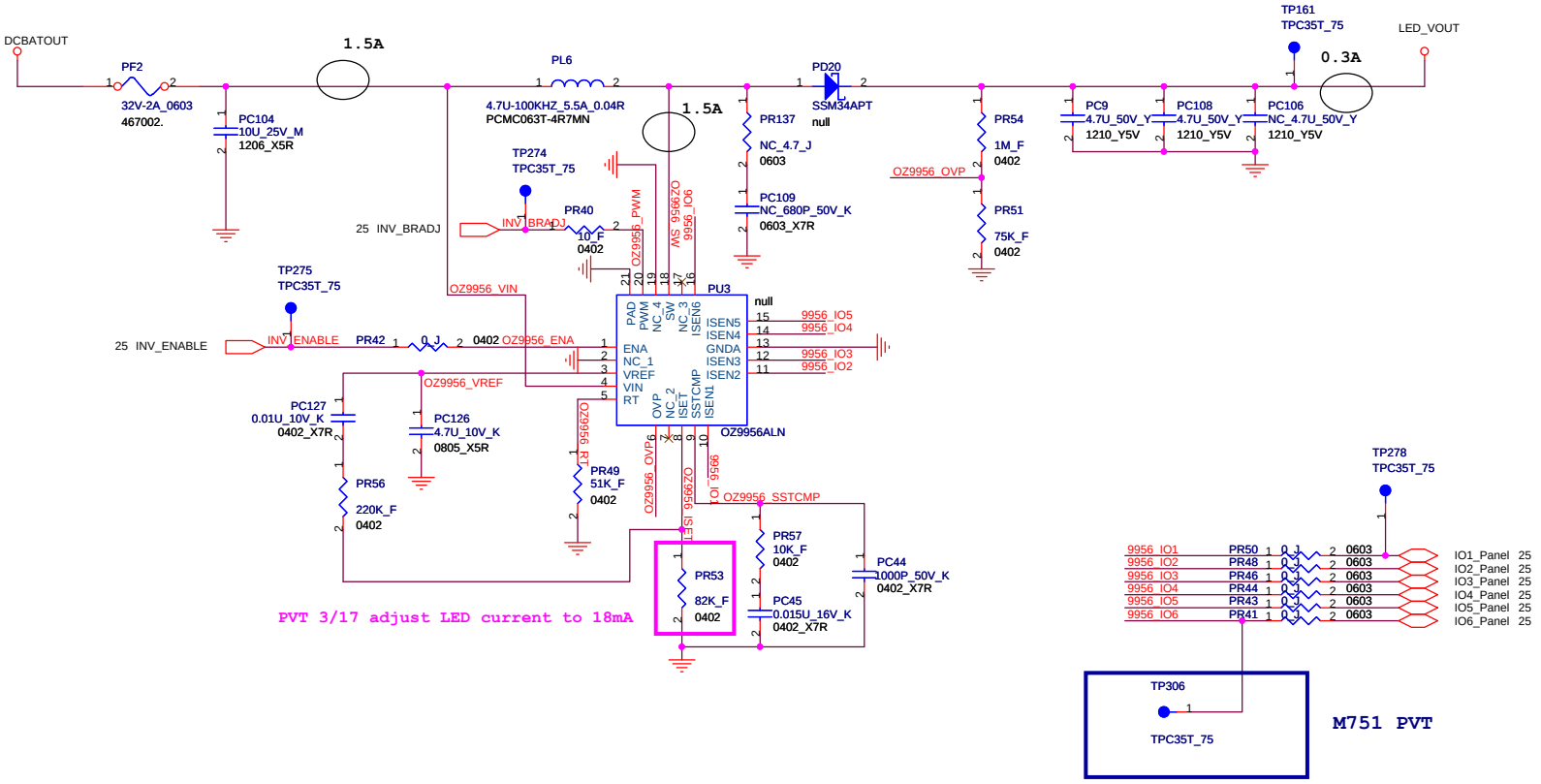




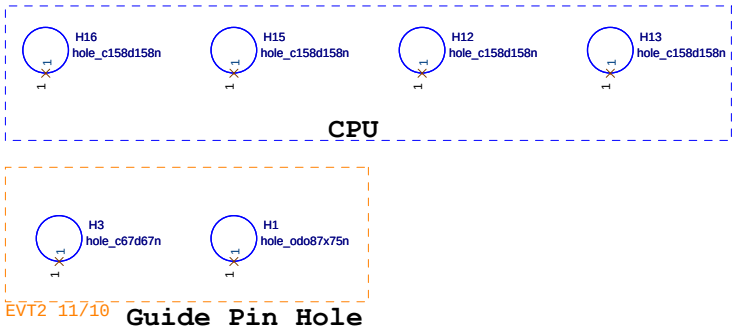
	I/O	Inter pull low	GPIO TABLE
PWRCNTL_0	O	Yes	GPU Voltage H:=1.210V GPU Voltage L:=0.954V

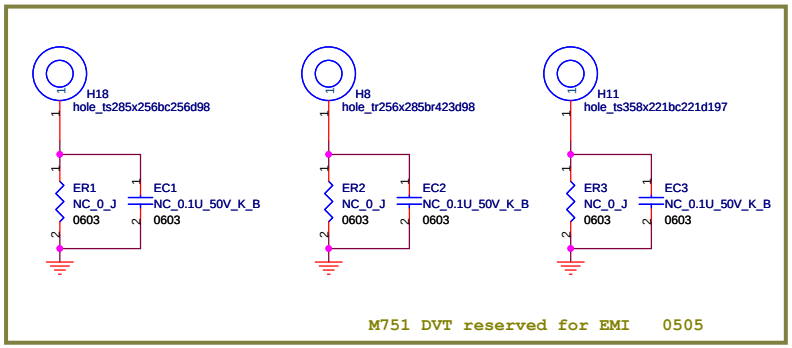
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

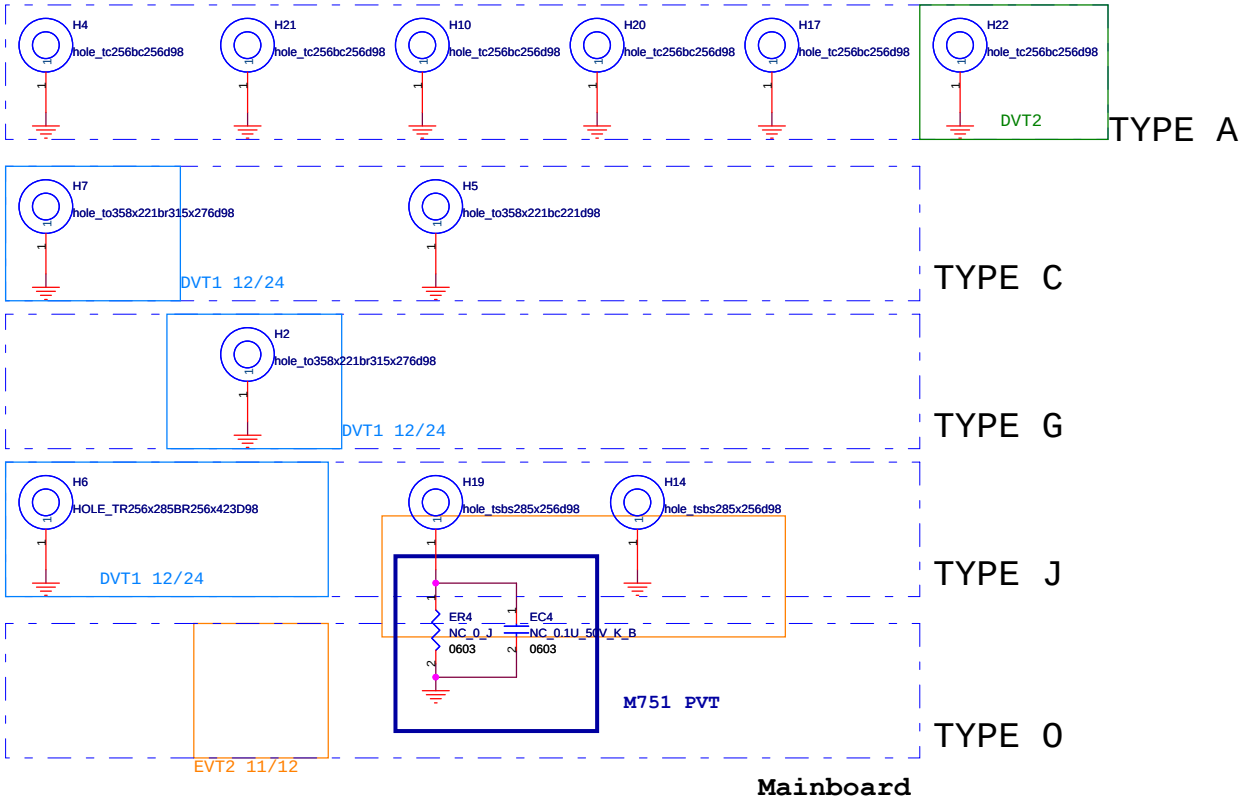
Title	VGA Power(+1.1V/+1_2V)	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Monday, June 23, 2008	Sheet 50 of 54	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED Backlight Power	
Size A3	Document Number M750-1-01	Rev 1.0
Date: Thursday, June 26, 2008	Sheet 51 of 54	







FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
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10/12
Change color of MS/SD/HDD LED.
Mount R419, R414, R420, R421.
10/13
SYSTEM_ID, MODEL_ID definition update.
10/20
CPU 22uF CAP N.C. parts location change.
N.C. R101 For EVT2 (Use +5V type camera module)
10/24
Move PCI Express pair of LAN from port5 to port1.
10/29
Change PR9 to 422K.
Add PL15 and PL7 co-lay.
Modify charge current setting table.
Mount PR83.
PL11 change to 1uH.
Add TP276 test point.
Add PC201 0.1uF and close to PD27 pin1.
Change PL6 to 4.7uH and add TP274,TP275 test points.
10/30
Refer to PUR sugguestoin to change component source.
Add NC_PR232
Change PR30 to 10K and PR31 to 1K.
Mount PC30
Add TP278 test point.
10/31
Refer to PUR sugguestoin to change component source.
Swap LVDS group of ATI M82.
11/02
Change "#" to net "EN_EXT_DEV_SENSE" for low active.
Modify MB Semi-PNP circuit.
11/03
Inverse HDMI pairs polarity(DVI pairs inversed on docking side).
11/04
Change USB board connector.
Combine MS/SD LED to one(MEDIA_LED).
11/05
N.C. R377, Mount F3.
Change INUSE_LED to GPIO72.
Change MS slot to YAMAICHI JCS010-2300-0.
11/06
Change part of CN16/CN26.(Height Change)
Change netname of "SD_WP#" to "SD_WP".
Change PR143 to 200Kohm.
Update charge current setting table.
Reserve BATT_WOL_EN for LAN wake up enable/disable in battery mode.
11/07
C453, C452, C451,C426, C425, C424 change size to 0402.
Mount PR158, PC125 and PR185, PC148 and PR199, PC177 and PR16, PC21.
N.C. PR36.
Change C188 from 0.1uF to 0.47uF.
11/08
Swap USB_PP8/PN8 for ease of routing.
Change button board connector to WBF31326-F04TR.
Change MS/SD LED to side view, yellow color.
Change U7 from CM2009 to CM2006.
Update VCC_DDC power isolation circuit.
Add R565,C658 for SRTCRST#.
11/09
Change PC31 from 22p to 100p.
Reserve R566 for removal of Ext. SPI Conn on DVT.
Reverse Button Brd CN pin assignment.
Add EMI Cap C659~C666 on +1_8VSUS.
11/10
Delete guide pin hole H9, H22.
N.C. F3, mount F1. (Use +3VSUS for camera power on EVT2).
11/11
Change pin assignment of Express CN.

11/12
Change PTH hole size. (H11)
Add TP283,TP284.
Change net name "ISL_VSSSENSE_" to "ISL_VSSSENSE".
11/13
Add TP285~290 for SI probe point.
Change type of H14,H19.
Change PR22=51K, PR232=200k.
11/14
Tune crystal accuracy, change C390/C389/C416/C412 to 22PF,C648/C649 to 18PF.
Change PR6=360K.(Charge Current Control)
Co-Lay PR233, PQ54, PQ55, PL16.
Change RP34 to 2.2K for SI.
N.C. R415, mount L47 on H model.
11/19
N.C. R559 (Double pull up on BT_PRS#)
11/23
Change camera power to +5VSUS.
DVT1 12/01
Swap DVI bus polarity.
Route RUN_ON to docking station CN.
Add logic gate(U37) to prevent panel flash when boot up.
Add R567, bypass brightness control signal.
Use +3V_DELAY(Q4) to prevent M82 high pulse on LCD control signals.
12/07
Change DC-IN CN(PCN1, With Reinforcement Pin).
Add TPM Nut (BOSS1).
Change Button Board CN (CN3) to 15 pin.
Add R570 for power consumption measurement.
12/12
Change U6 from Quad to Dual XOR gate.
Change EMI Caps C424~C426, C451~453 to 10pF.
Change color of LED2(Charge LED) to Amber.
Change U16 from MR-sensor to Hall-sensor. (N.C. R263)
12/13
Change damping resistors of keyboard matrix to 120ohm ferrite bead.(For EMI)
12/17
Change C451,C452,C453,C424,C425,C451 to 22pF. (For EMI)
Add one more +3VSUS (CN26) for WLAN module to cover 1500mA(peak)/1100mA(normal) requirement.
12/18
Add one more LCDVCC pin (CN1) for panel to improve voltage drop.
Add optional resistors(R571,R572) for gamma control.
Reduce LED_VOUT from 6 pins to 2 pins.
12/20
Change net "BL_OFF" to "BL_OFF#".
Add R573-577 to improve MS signal overshoot/undershoot.
Mount C642-644.
Change F3 to 0.25A.
12/21
Change Net "HDD_LED#" to "HDD_ODD_LED#"
12/23
Change C412/C416 from 22pF to 10pF.
Change C648,C649 from 18pF to 15pF.
Mount U26(VGA Thermal Sensor) on H model only.
Add 75 ohm bead, 10pF capacitor on HDA_MDC_BITCLK/HDA_CODEC_BITCLK for EMI.
12/24
Update H2/H6/H7/H8 footprint.
Delete R563, R564 (CRT_GND).
Change D17, D18 to SSM22 to reduce voltage drop.
Change pull up voltage of R360/R361 to +3VRUN. (Only Strap/GPIO pin connected to +3V_DELAY)
N.C. C403 (Not necessary for ESD)
12/26
Delete ODD_DP# connection to ICH9M.

12/27
Add PC204 for noise filtering.
Add R578 for protection.
Change U27 from RClamp0514 to RClamp0524.
N.C. SW1, R[illegible]34,R[illegible]41
Change P[illegible]38 to 2[illegible], [illegible]R37 [illegible] 1K
12/2[illegible]
N.C. [illegible] shunt regulator to reduce S4 consumption.
Mount R131, N.C. R129.
Reserve LDO (U38) for 1.5V type VCCSUSHDA.
Add R579,R580 to avoid floating on input pin.
1/2
N.C. C451~453, C424~426.
N.C. PC204.
Add prefix AT_ on R322, R51.
Change damping resistor value of MS card.
(R573~577 from 33 to 68 ohm)
(R506~510 from 33 to 0 ohm)
Change L30~32 to 27nH inductor.
Change C258,260,262 to 2.2pF.
Change revision of clock generator(U29) to Rev.B
1/5
Change D2/D3 to low capacitance type.
Fine tune delay timiing. Change R19/R565 to 13K.
1/8
Update power design spec.
VCore: 47A, +3VSUS: 1.7A.
DVT2
1/15
Update power budget of VCCHDA,VCCSUSHDA,VCCDMI,VCC1_5_A
Add GND pin on C130.2
1/18
Add BT_LED on CN4.6
Update WIRELESS LED circuit. Page41.
1/21
Add screw hole H22.
Add D23, D24 for leakage issue when EC initialization.
Add R460 for Non-Dock Sku.
1/23
PQ12 change to SI3424BDV-T1-E3.
PR125 change to 62Kohm
PR215 change to 205Kohm
PR211 change to 75Kohm
PR223 change to 154Kohm
Add PR237 ND_280Kohm , PR236 ND_154Kohm for Non-Dock sku.
Add pull down resistor (R581) on BT_LED.
1/25
Mount L23, N.C. R108, R109 for EMI.
Change L86 from 75R to 10R for SI.
For Docking sku, add prefix DS_ on value of C257,C259,C261,CN16 D1,PQ2,PQ4,PR11,PR24,PR29,Q1,Q20,Q21,R6,R9,R10,R165,R167,R416 R444,R578,U8,U9,U10.
1/26
Change R176 from 54.9 to 649 Ohm.
Del L48, Add R582. R583 (N.C.)
Change C413 from 0.1uf to 1uF.
Change CN5 from Gold plated to TIN plated.
1/28
Mount R555, R556, R557.
Add +1_5V_PCIE_OUT on CN25.6 to reduce voltage drop.
Change CN3 from WBF31526-F04TR to GB5RF151-1093-7F.
(Vender naming rule change, same part.
layout footprint pin reversed)
1/29
Add R584, R585, Q27 to solve DDC capacitance issue.
Add R586 for identification of Dock support.
1/30
Change L86 back to 75R, change L85 from 75R to 10R.
Mount CN13 for software debug on DVT2.
N.C. R572.
Move R321 to U37B.6
1/31
Move PJ14 to PR226.2
Change R176 back to 54.9 ohm.
Add prefix LND on PR236,PR237 for Non-Dock skue for LOW model.
Add PAD1 for EMI Grounding.

0218
M750

change U30 from N[illegible]S32M5X(14-NC7S32M-5X00) to MC74HC1G32DTT1G(14-MC74HC1-G300)
change D2,[illegible]3 from BAS3[illegible]6(16-BAS3160-0000) to BAS316PT(16-BAS316P-T000) for common parts
change D6,D[illegible],D[illegible],D1[illegible],D12 D14,D23,D24 from 16-SCS500V-4000 to CH500H-40PT(16-CH500H4-0P00) for common parts
change Q1.Q5,Q17,Q21,Q22 from 17-2N7002P-T000 to ME2N7002E(17-ME2N700-2E00) for common parts
change Q23 from 17-MMBT390-4001 to PMBT3904.215(17-PMBT390-4200) for commonn parts
change C303,PC156 from 0.01U_6.3V_K(1C-2B20103-K100) to 0.01U_10V_K(1C-2B20103-K200) for commonn parts
change L23,L28,L40,L41,L42 from 90R-100MHZ_0R35(1L-FDLW31S-N900) to 90R-100M_1206(1L-FWCM321-6F00) for commonn parts

change C19,C17 from Y5V to X5R tolerence
change PR32 to 11K, PR33 to 19.6k to set the battery mode voltage to 0.95V by AMD for battery mode dual display

0318 PVT

NC C656 for WLAN_LED light when power on because of RC delay
update battery identify IC(PU5) P/N to R5G05000N100NS by vendor
update U7 symbol to CM2006-02QR
modify R345 value to HD_ for BOM change of disable HDaudio in 128MB SKU
remove PJ11,PJ12,PJ3,PJ8,PJ10,PJ9,PJ13,PJ5 and short by layout
correct U36 vendor P/N to WPCE775LA0DG
change U32 to W25X16AVSSIG by vendor suggestion
add PQ56,PC206,PR246 for charger ocp improve by M760 battery OCP issue
modify P43 charge current table ,middle current change from 1A to 0.8A
add PR244 and PR245(dummy directly) for intersil ISL6266A found C4 hang at the other company
change PD18 to MMVZ5231BPT for SCP circuit
add UVP circuit (PU17,PR238,PD32,PC205,PR242,PR241,PD33)
change PR236 to 120Kohm for power limit point improved
change PQ50,PQ51,PQ49,PR221 value title to DS_
change PR53 to 82Kohm for LED backlight current modify
add R587,Q28,Q29 for improve HDMI voltage drop

0326
Short PJ1,PJ2,PJ4 by layout
add C669 for reduce fan power source ripple
add L87,L88 for EMI
add U39,C670 for MS/SD abnormal behavior

0327
change PU9 to AT5208 because of G909 big inrush current

0328
NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS
add R589,C672 for MS/SD led abnormal when power on

NC R389,R393,Y3,C436,C437,C241,C242,L29,U5,R152 for use AMD internal SS
add R589,C672 for MS/SD led abnormal when power on
reserve R588 for reduce G-sensor power ripple

0402
add F5~F11 for power short

0403
change PR241 from 232K to 215K for UVP circuit improve

0408
NC R348,R356,R357 for using AMD internal SS
change R378 value to HD_ for HDMI disable

M751 DVT

0505
Reserve EC1,EC2,EC3, ER1,ER2,ER3 for Hynix 1GB EMI
change HDD sata CN20 pin define to increase the impedance for SATA SI

0506
reserve PR247 for colay with MAX17020
Update U29 footprint for Japan/Mitsui package
change L85 to 60ohm for EMI
NC C5 for EMI

0508
add Q30 for MS/SD LED cost down

M751 PVT

0618
Page 24:Change L30,L31,L32 to 33ohm and change C258,C260,C262 to 15PF for SI issue
Page 25:chang C405 C407 to 1C-2B30475-K100 for PUR request
Page 33:NC R561,Mount R560 ,keep system ID the same as M750
Page 36:NC F1 ,mount F3,for 5v Camera moudle
Page 38:Change R80 to 4.7k from 10k , for FAN speed issue
Page 40 :NC Q30 ,Mount U39 Q13 C672 C670 R589 for mor Request
Page 47:NC PR244 ,Vendor suggestion and it is related with DC4
Page 43,49:1.PR14 change to 62Kohm , co-lay PR248 LND_86.6Kohm with PR7.
2.PR215 205Kohm change to 280Kohm
3.PR223 154Kohm change to 280Kohm
Page 24: change D17 to 16-SSM24AP-T000' for leakage issue
Page 7;Change C254,C252 rating to 6.3v for cost down
Page 35:del R301,R302,R303,R304,R305,R306,L40,L41,L42 for cost down
Page36:del R147 R150 L28 for cost down
Page 39:del R261 for cost down,change U14 version
Page 33:Change CN6 to 1N-0024000-F1T0 for pur request
Page 52:add ER4 EC4 for EMI Issue

0625

Page 43:.PC121 change from 0.1uF/25V to 0.1uF/50V(1C-2B30104-K000)
Page 52 : change ER4 EC4 to 0603 for EMI request
Page 40:modify the U33 P/N to 15-BD2056A-FJ00 for CE update component library
Page 35:resume CN6 main source 1N-0024000-M1T0,for 2nd source layout issue
Page 24:change D17 to 16-SSM24PT-0000 For design change
Page 51:add one test point in PR41 pin1.

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