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PJ Leader	Appr. by	Check by	Design by
			Alex

Project Code & Schematics Subject:	MS03 M/B-FUBAI	PCB P/N:	1P-0055100-80SB
Project Code & Schematics Subject:	MS03 M/B-HANNSTAR	PCB P/N:	1P-0055500-80SB
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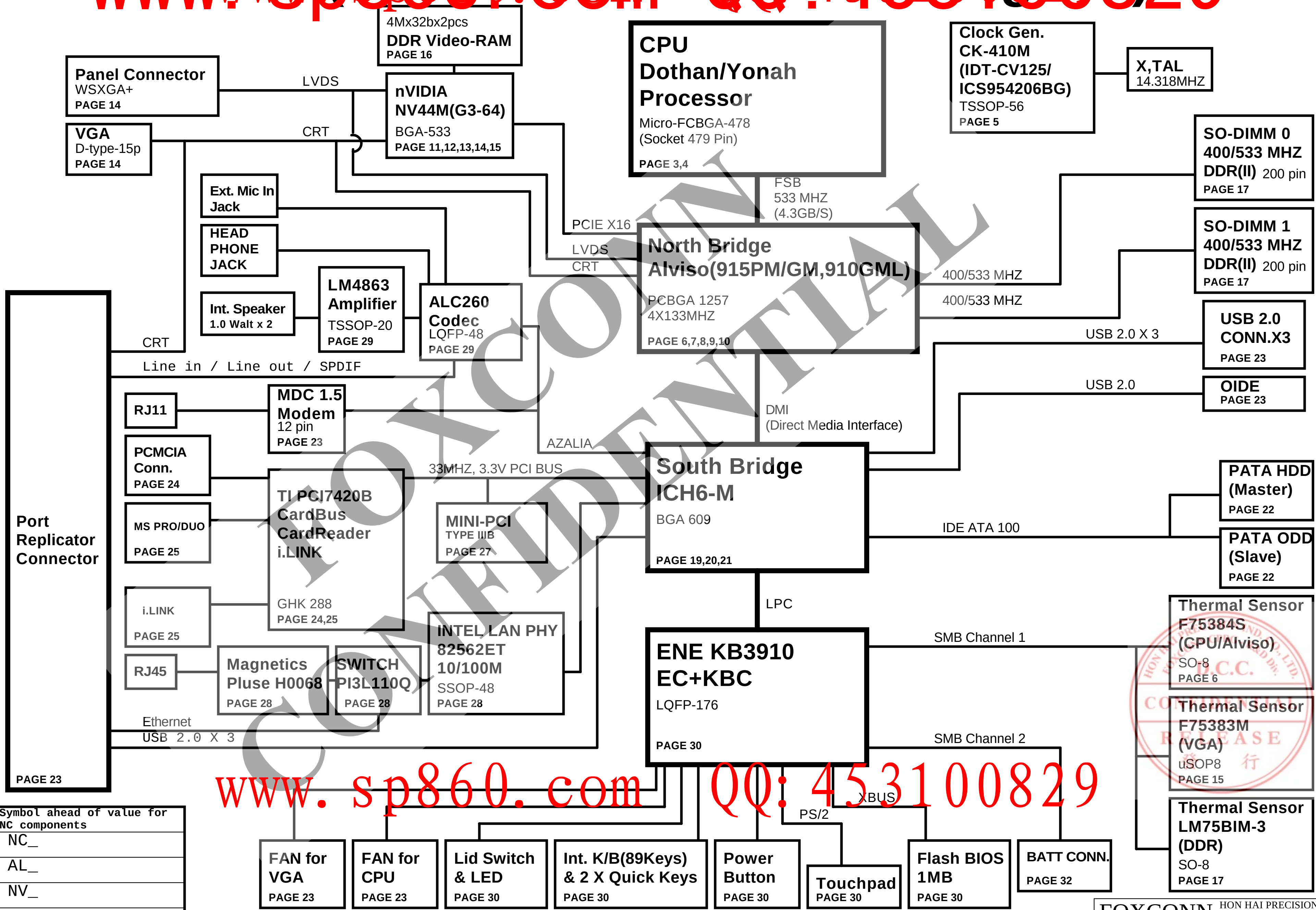
MS03(915PM/GM) Block Diagram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DDR(II) 200 pin
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(4.3GB/S)
Ext. Mic In
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HEAD
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JACK
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LVDS
CRT
North Bridge
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PCBGA 1257
4X133MHZ
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400/533 MHZ
400/533 MHZ
Int. Speaker
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LM4863
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INTEL LAN PHY
82562ET
10/100M
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F75384S
(CPU/Alviso)
SO-8
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Pluse H0068
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SWITCH
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ENE KB3910
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Ethernet
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LM75BIM-3
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FAN for
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FAN for
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Int. K/B(89Keys)
& 2 X Quick Keys
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Power
Button
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Touchpad
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Flash BIOS
1MB
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BATT CONN.
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	Symbol ahead of value for NC components
ALL	NC_
915PM + NV44M	AL_
915GM or 910GML	NV_
910GML	LNC_
915PM + NV44M or 915GM	HMNC_

BOM configuration

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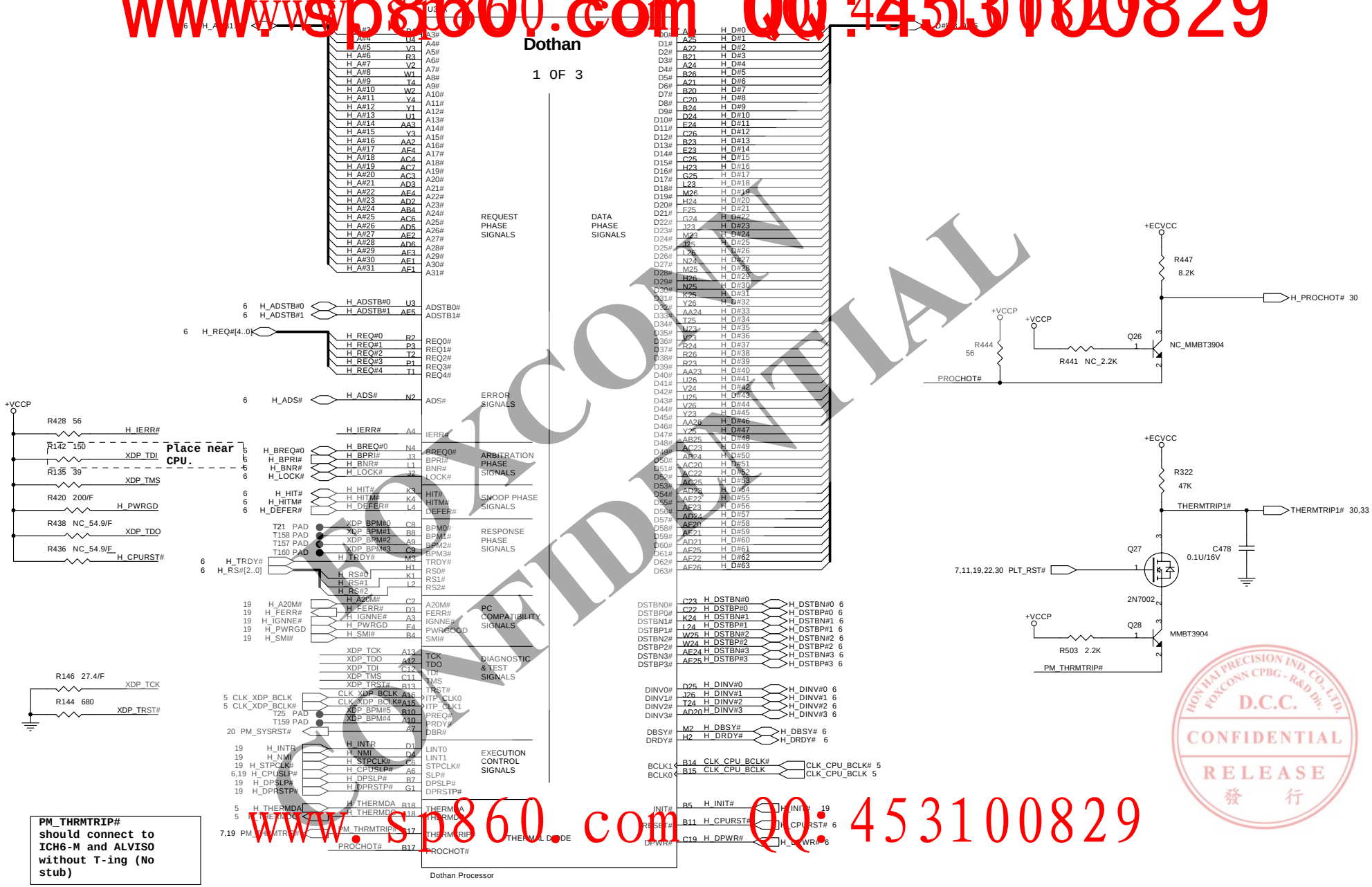

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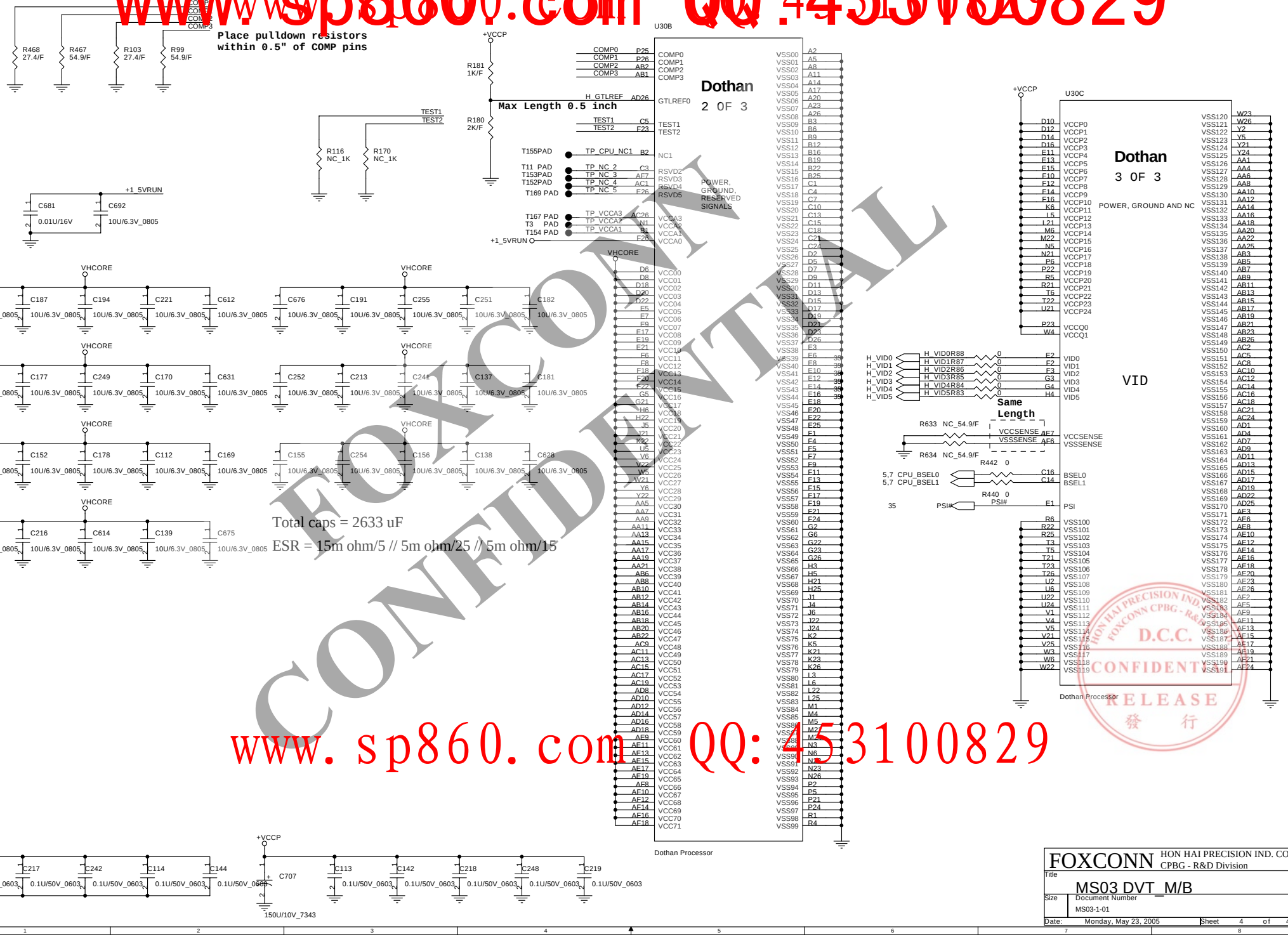

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Length as short as possible.

Placed within 500mils of Y1

L5030-14.318MHZ/+-30ppm/20pF

U33

IDTCV125 / ICS954206BG

SM bus Address : 1101001 (ICH6) For clock generator

SM bus Address : 1001101(EC) For F75384S

Place Thermal-Sensor near CPU & GMCH.

Alviso Chip HOST

CPU

Alviso Chip

For NV44M & Alviso option

ICH6 DMI

Graphic NV44M

ALVISO SSCK

U32 F75384S

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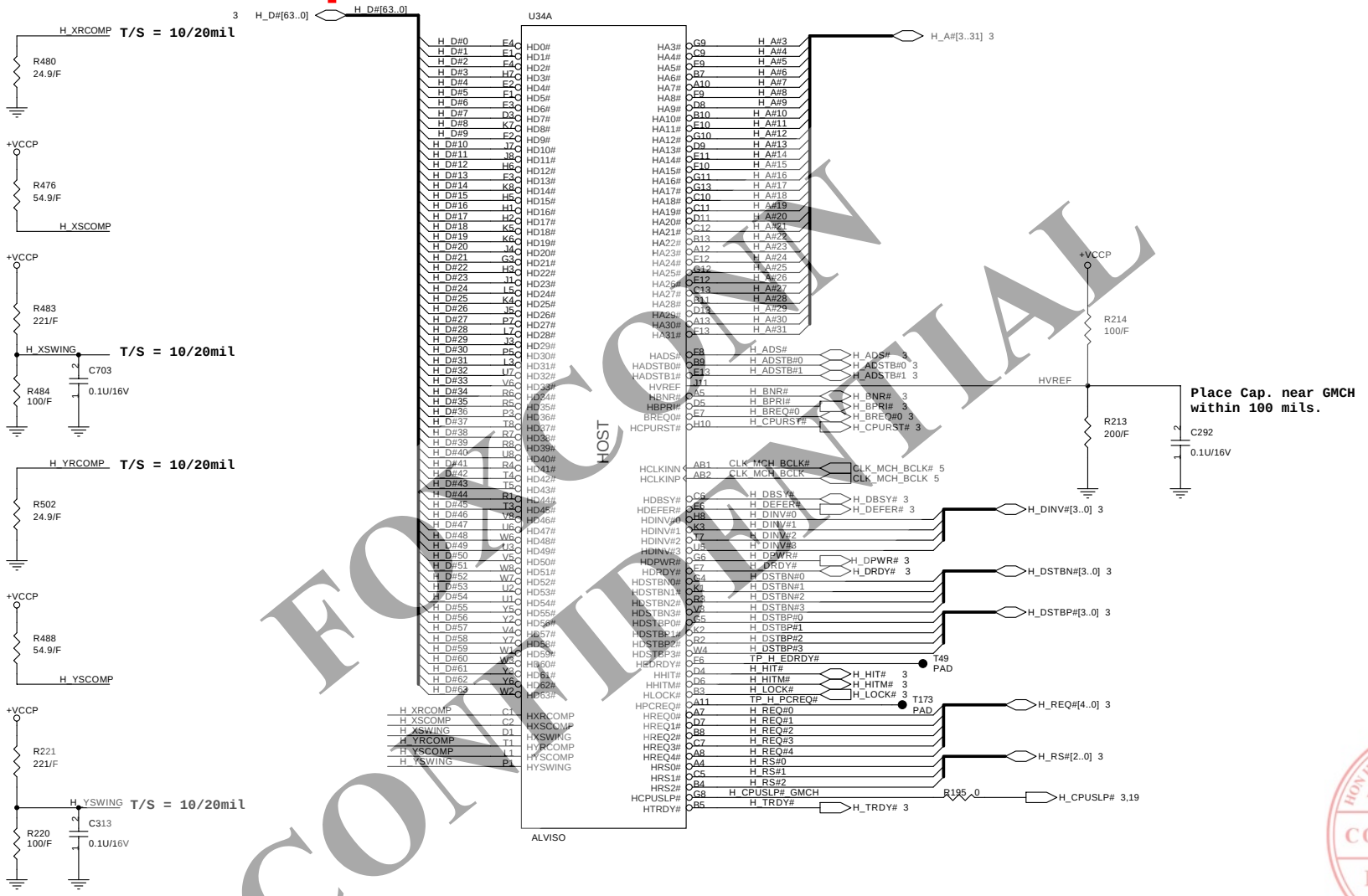

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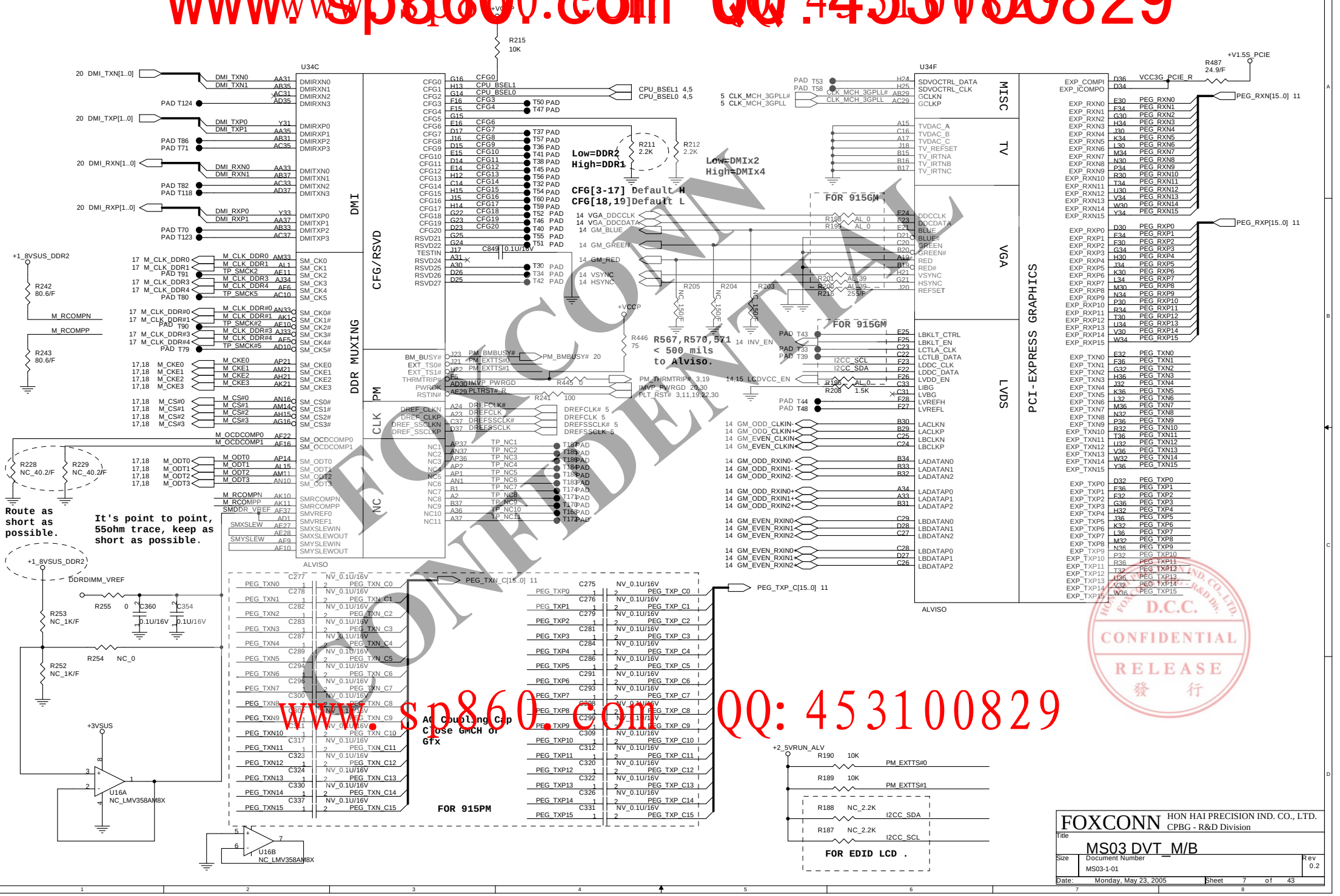

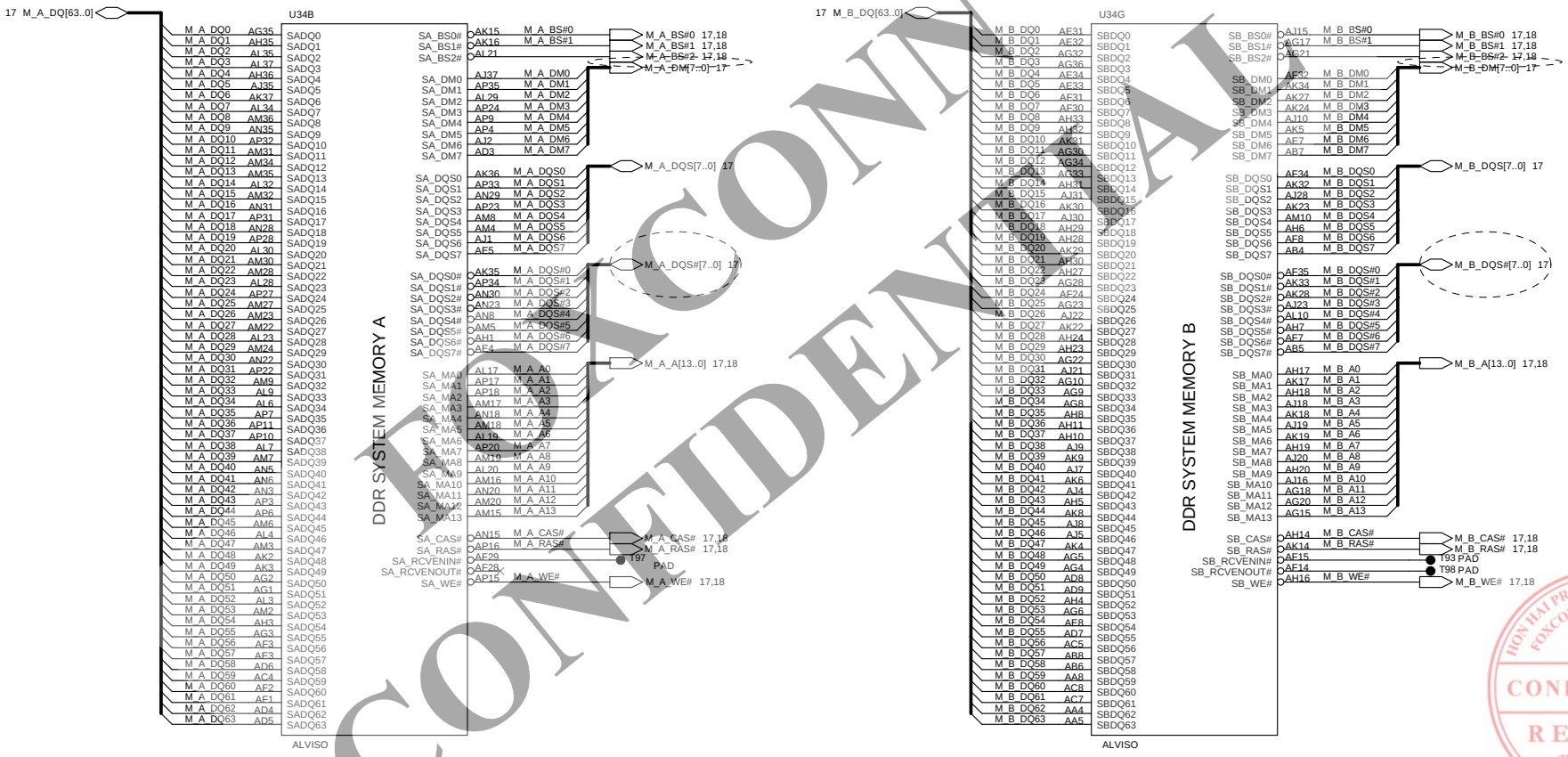

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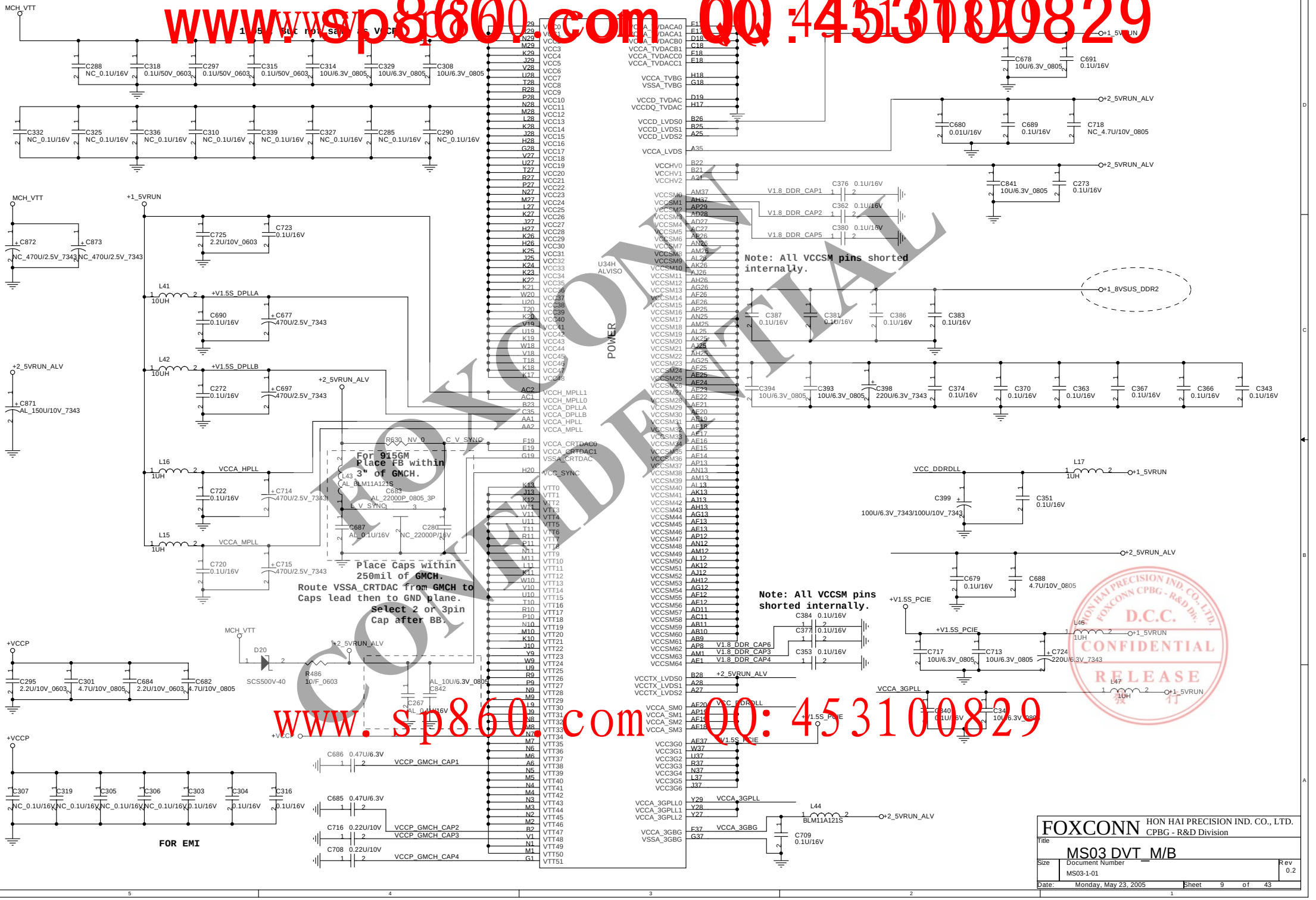

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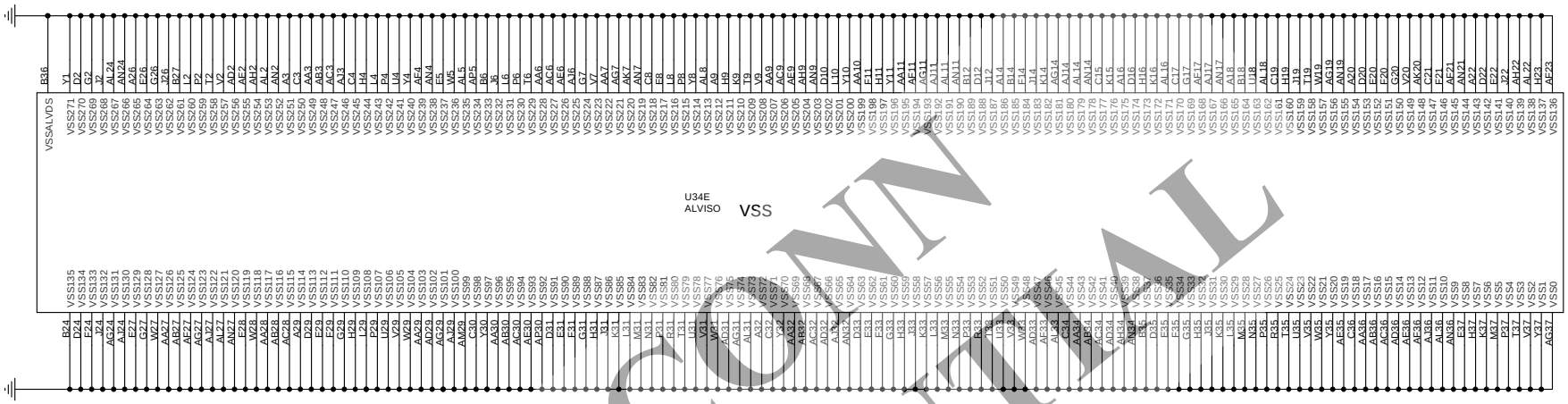

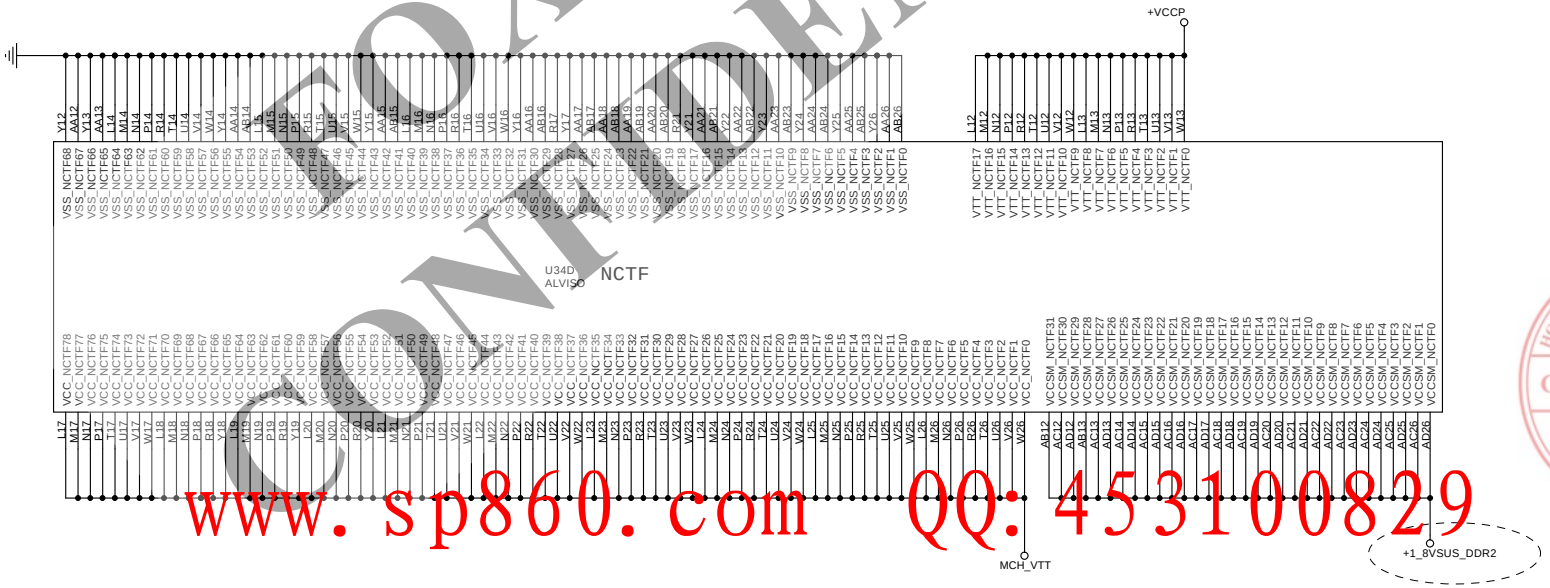

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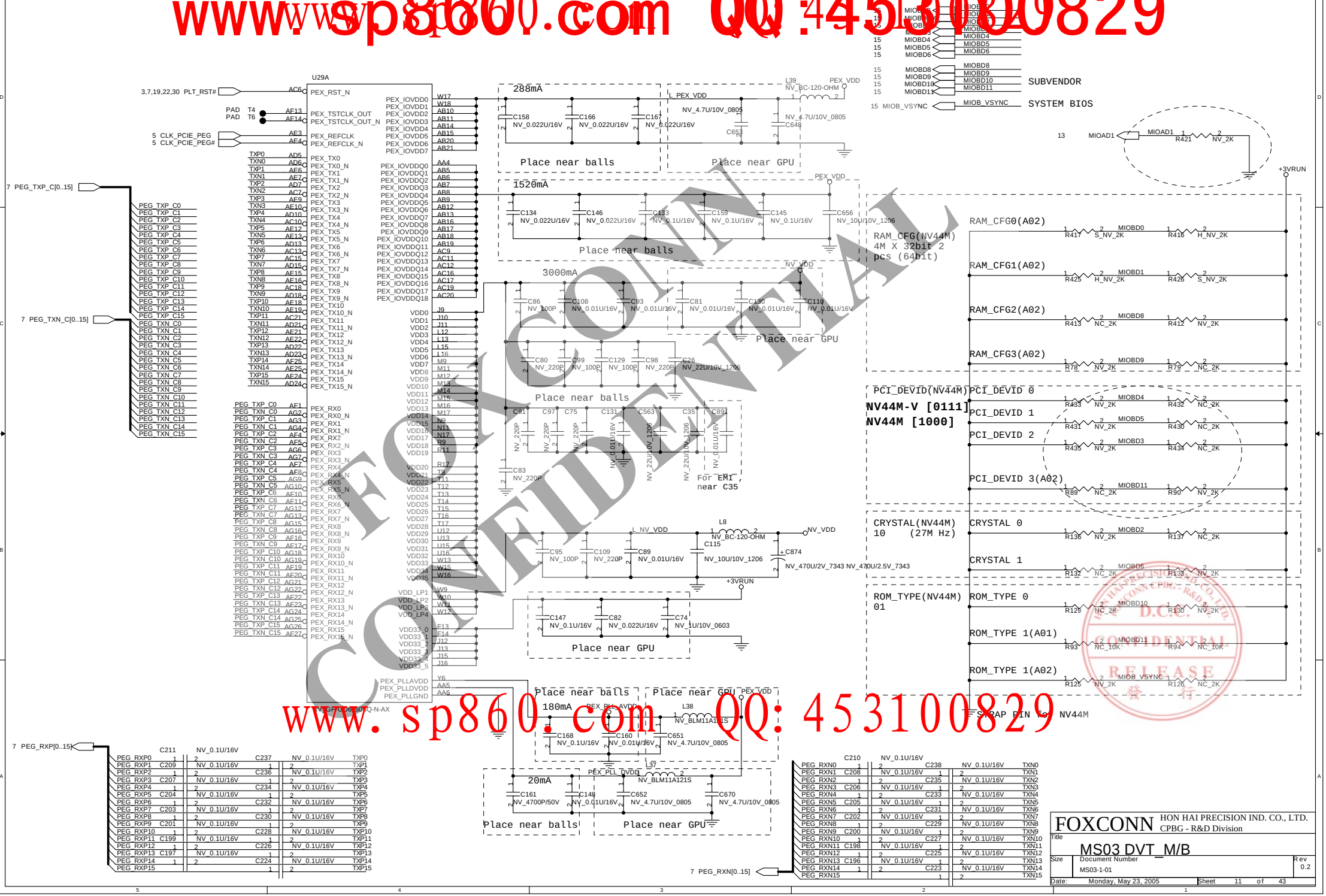

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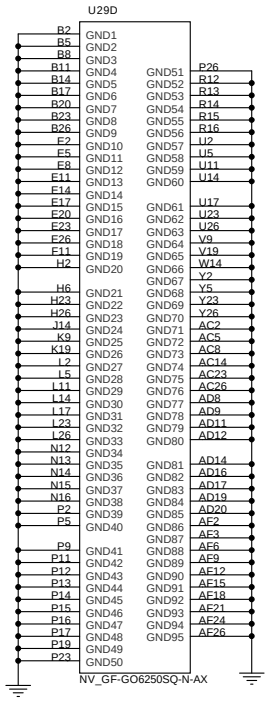

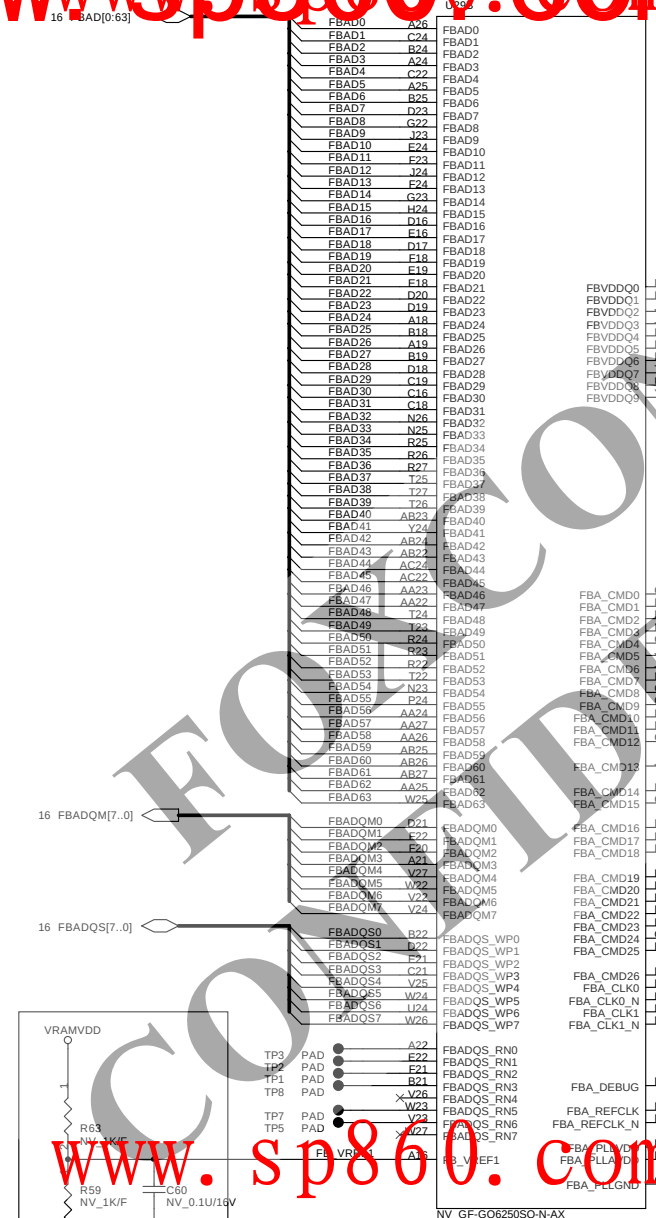

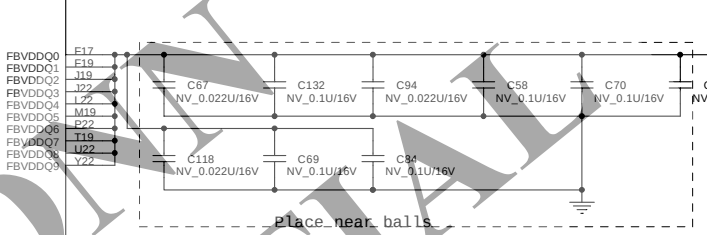

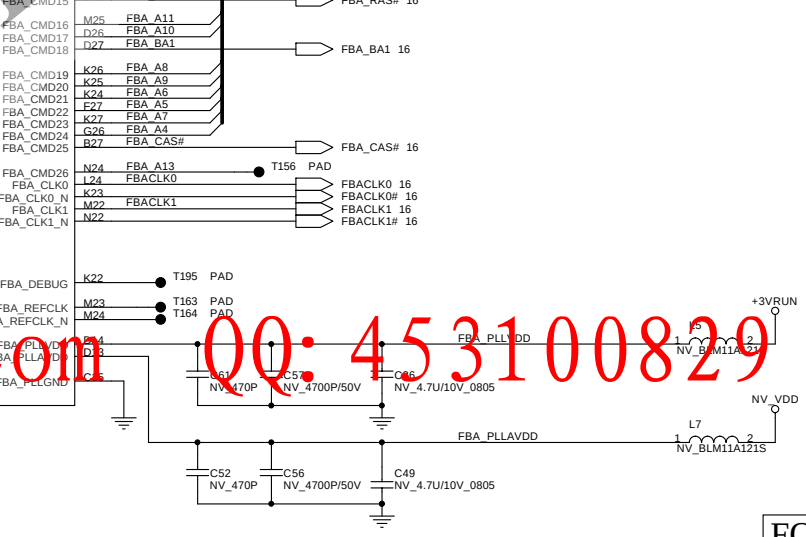

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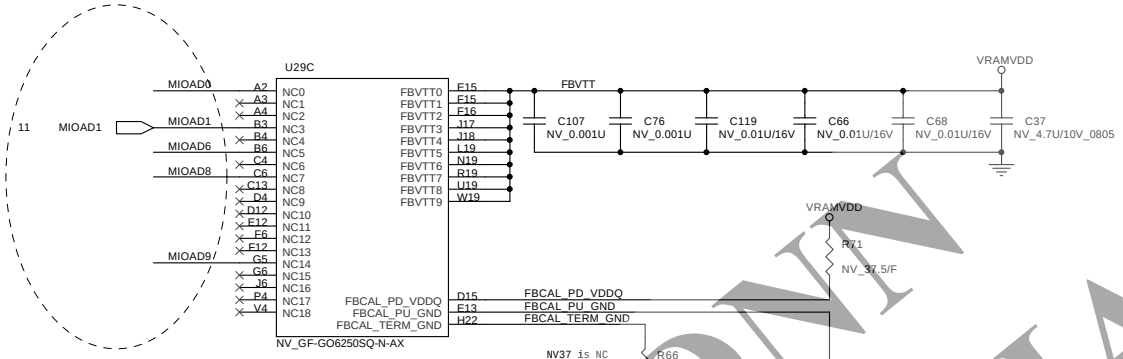

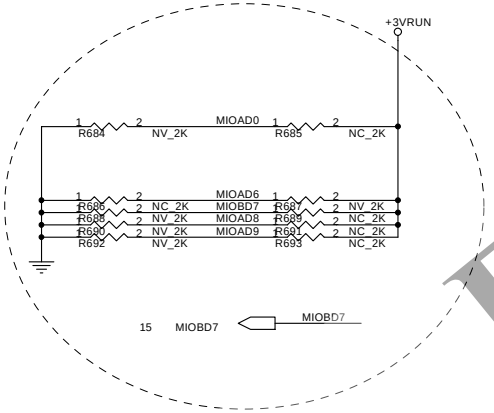

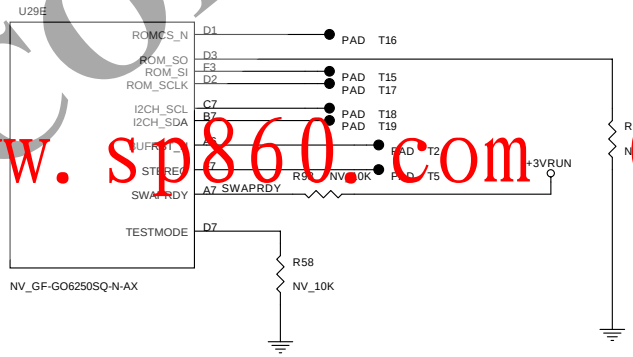

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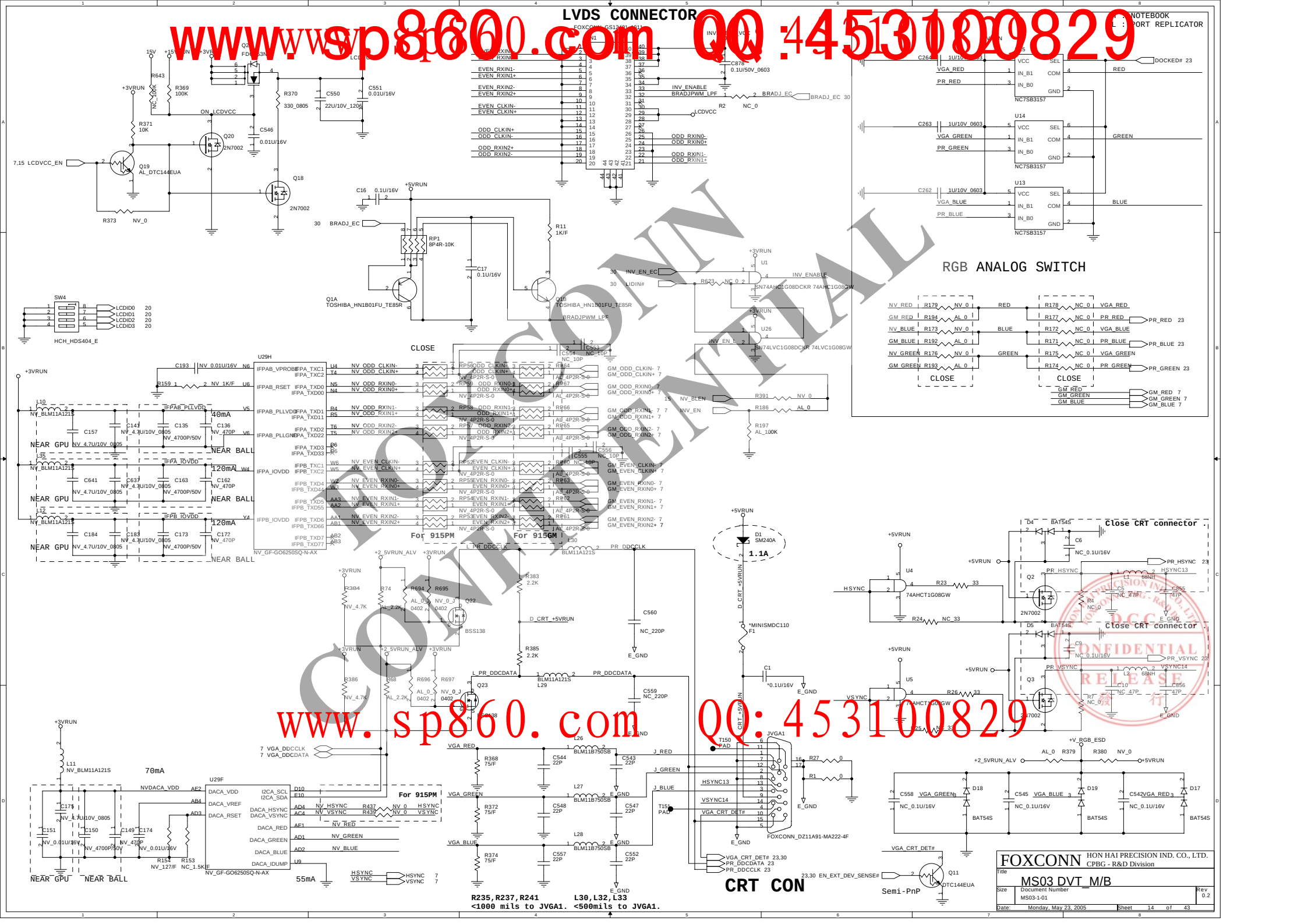

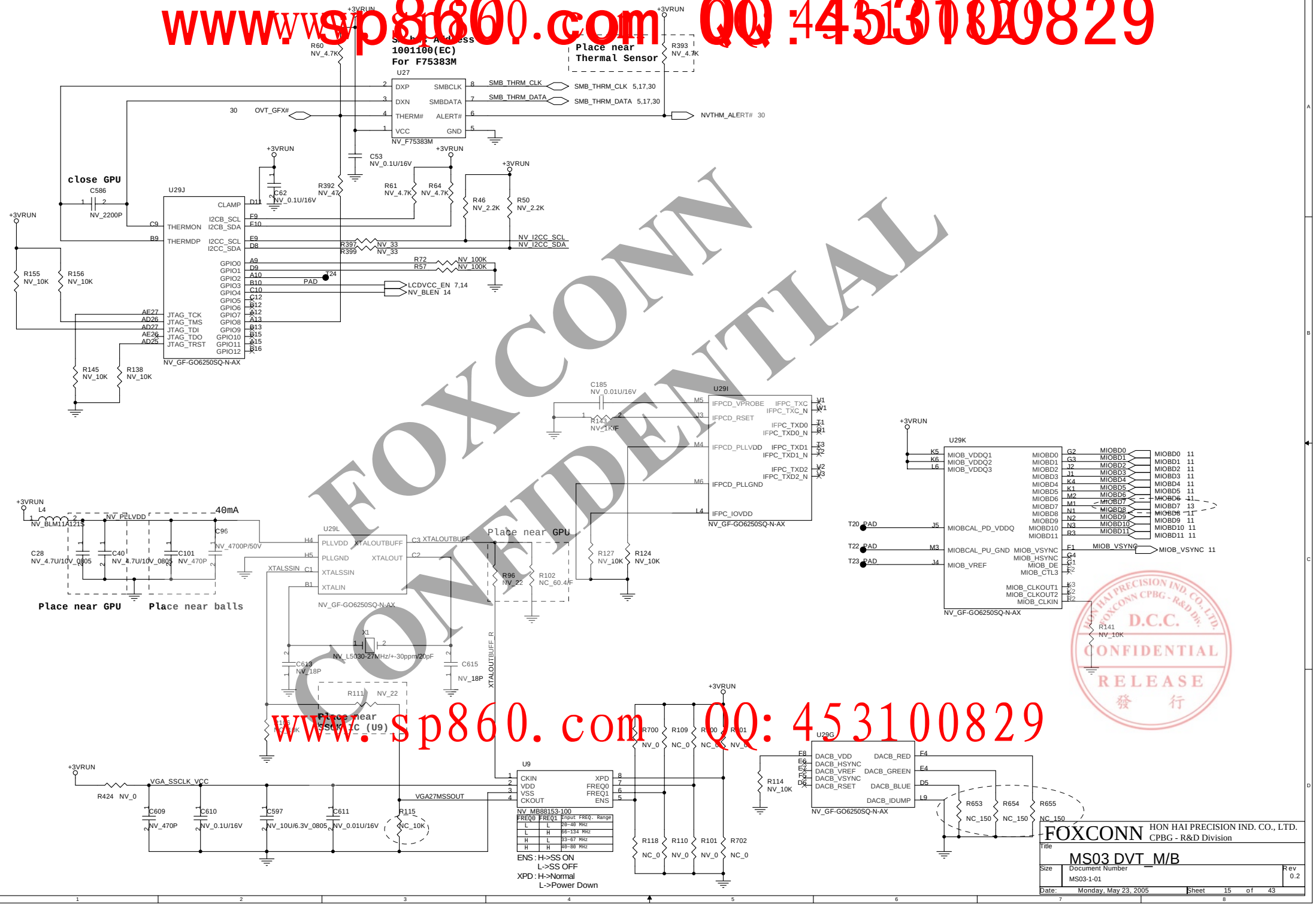

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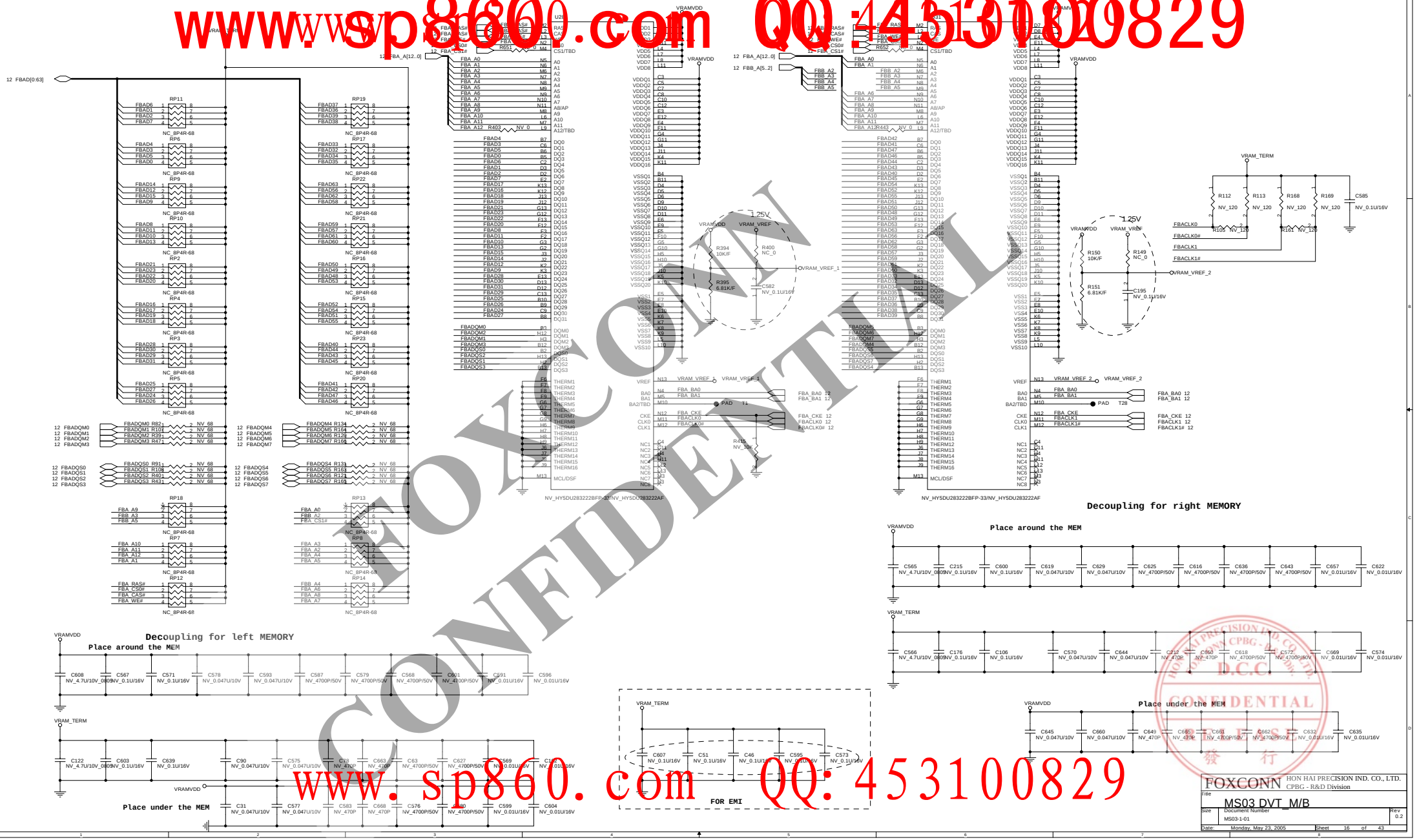

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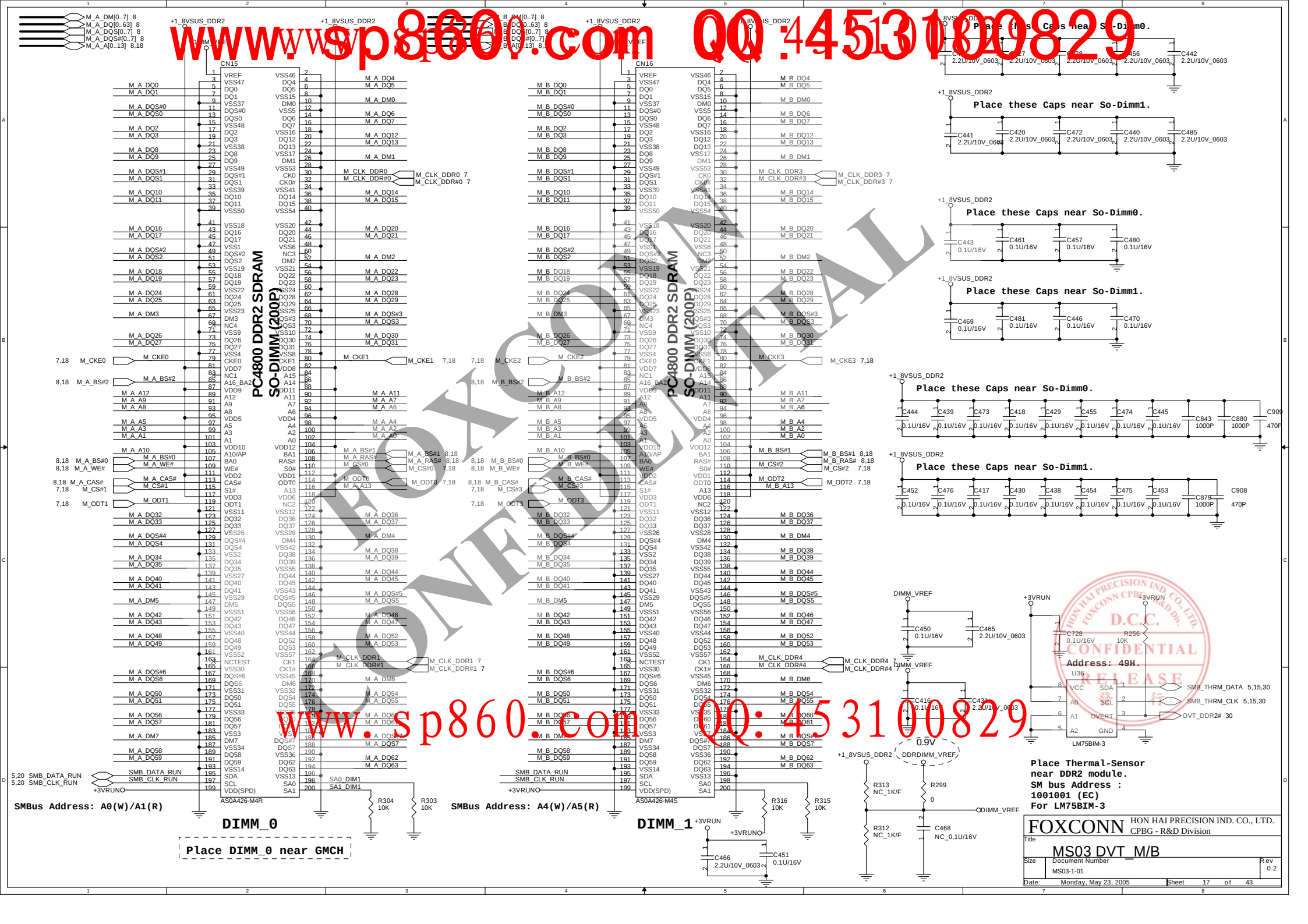

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M_A_A[0..13] 8,17

M_B_A[0..13] 8,17

SMDDR_VTERM

C484 0.1U/16V
C482 0.1U/16V
C462 0.1U/16V
C483 0.1U/16V
C435 0.1U/16V
C460 0.1U/16V
C426 0.1U/16V
C424 0.1U/16V
C464 0.1U/16V
C423 0.1U/16V
C437 0.1U/16V
C434 0.1U/16V
C425 0.1U/16V

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

SMDDR_VTERM

C436 0.1U/16V
C433 0.1U/16V
C479 0.1U/16V
C421 0.1U/16V
C486 0.1U/16V
C463 0.1U/16V
C487 0.1U/16V
C422 0.1U/16V
C458 0.1U/16V
C459 0.1U/16V
C432 0.1U/16V

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

8,17 M_A_BS#1
8,17 M_A_RAS#
RP35 4P2R-S-56
M_A_A6
M_A_A4 RP36 4P2R-S-56
M_A_A11
M_A_A7 RP38 4P2R-S-56
SMDDR_VTERM

M_A_A12
M_A_A9 RP34 4P2R-S-56
M_A_A8
M_A_A5 RP29 4P2R-S-56
M_A_A3
M_A_A1 RP30 4P2R-S-56
SMDDR_VTERM

8,17 M_A_WE#
8,17 M_A_BS#0
M_A_A10 RP31 4P2R-S-56
8,17 M_A_CAS# RP32 4P2R-S-56
M_A_A0
M_A_A2 RP37 4P2R-S-56
SMDDR_VTERM

7,17 M_CKE1
7,17 M_CKE0 RP39 4P2R-S-56
7,17 M_CS#3 R317 56
7,17 M_CS#1 R301 56
M_A_A13
7,17 M_CS#0 RP33 4P2R-S-56
SMDDR_VTERM

8,17 M_B_BS#1
8,17 M_B_RAS# RP49 4P2R-S-56
M_B_A5
M_B_A8 RP40 4P2R-S-56
M_B_A9
M_B_A12 RP41 4P2R-S-56
SMDDR_VTERM

8,17 M_B_WE#
8,17 M_B_CAS# RP42 4P2R-S-56
M_B_A3
M_B_A1 RP43 4P2R-S-56
M_B_A10
8,17 M_B_BS#0 RP44 4P2R-S-56
7,17 M_CKE2
M_B_A11 RP46 4P2R-S-56
SMDDR_VTERM

M_B_A4
M_B_A6 RP47 4P2R-S-56
M_B_A2
M_B_A0 RP48 4P2R-S-56
SMDDR_VTERM

7,17 M_CKE3
M_B_A7 RP45 4P2R-S-56
7,17 M_CS#2
M_B_A13 RP50 4P2R-S-56
SMDDR_VTERM

8,17 M_A_BS#2 R388 56
8,17 M_B_BS#2 R389 56
SMDDR_VTERM

7,17 M_ODT0 R429 56
7,17 M_ODT1 R610 56
7,17 M_ODT2 R451 56
7,17 M_ODT3 R452 56
SMDDR_VTERM

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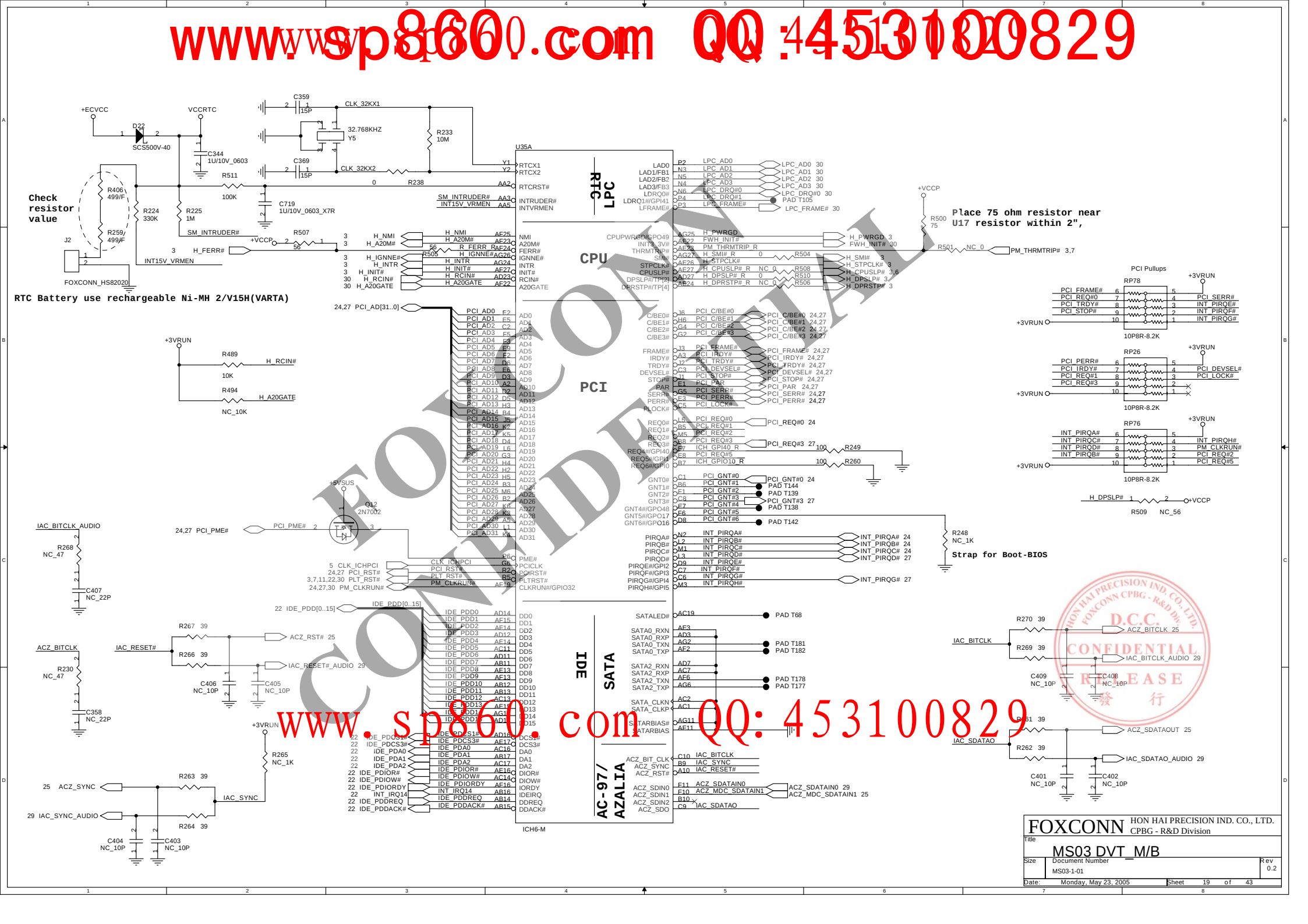

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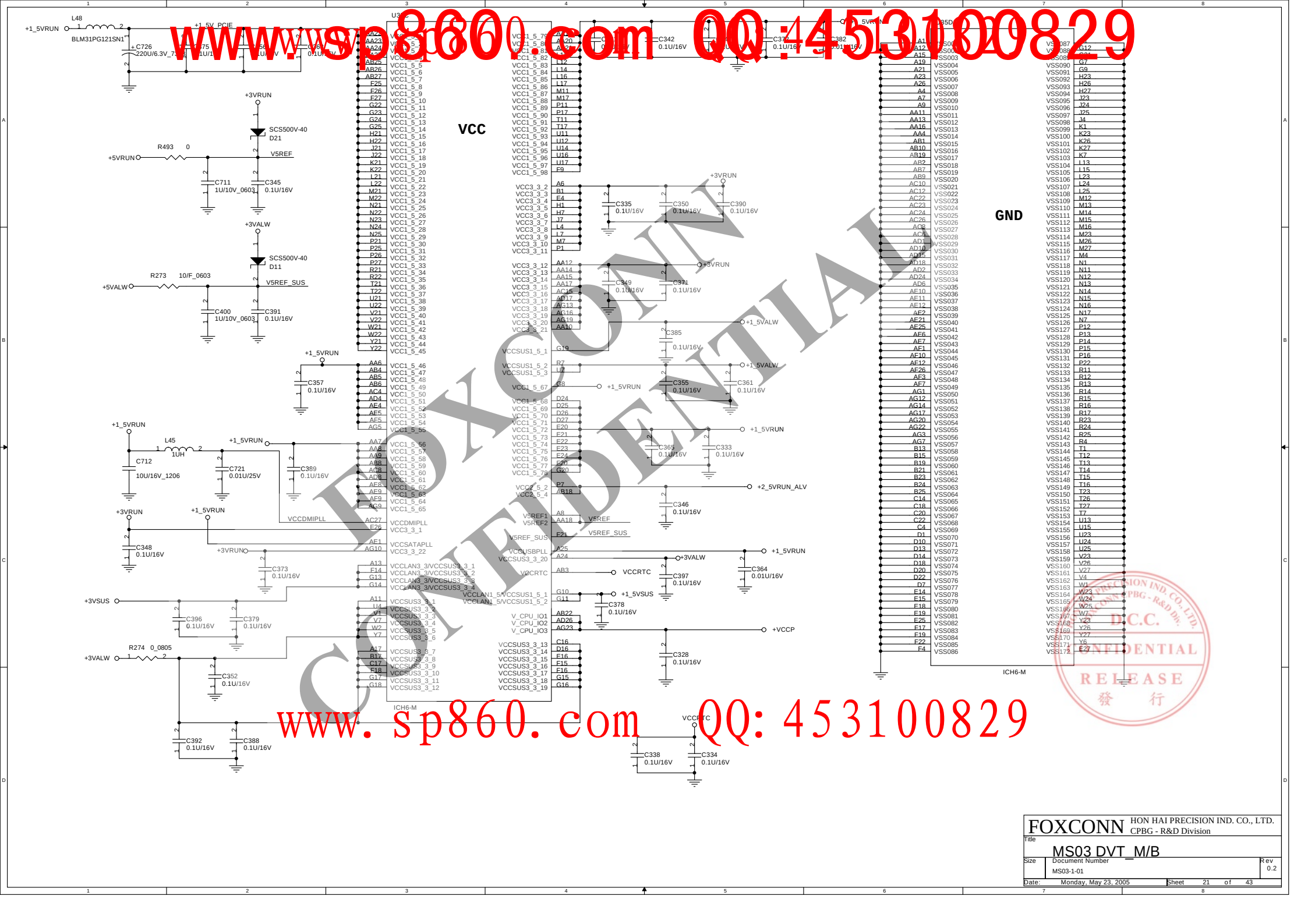

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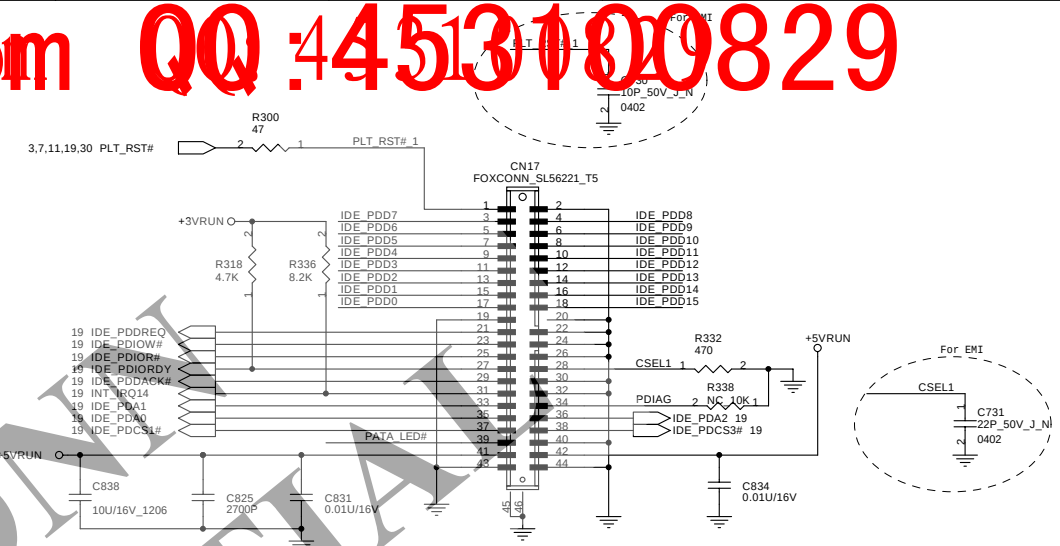
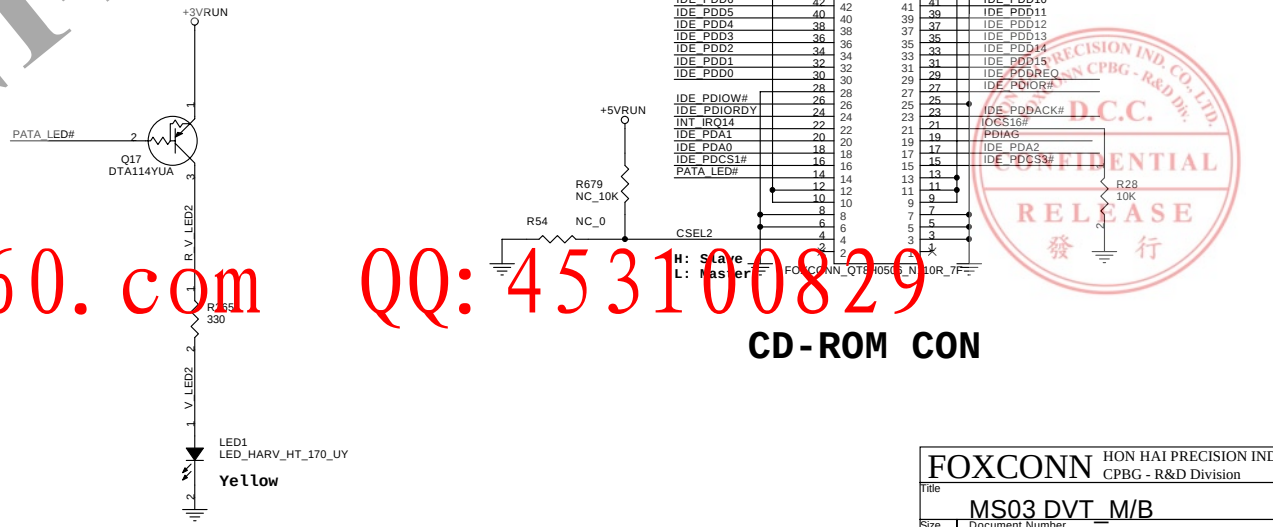


HDD CON



CD-ROM CON

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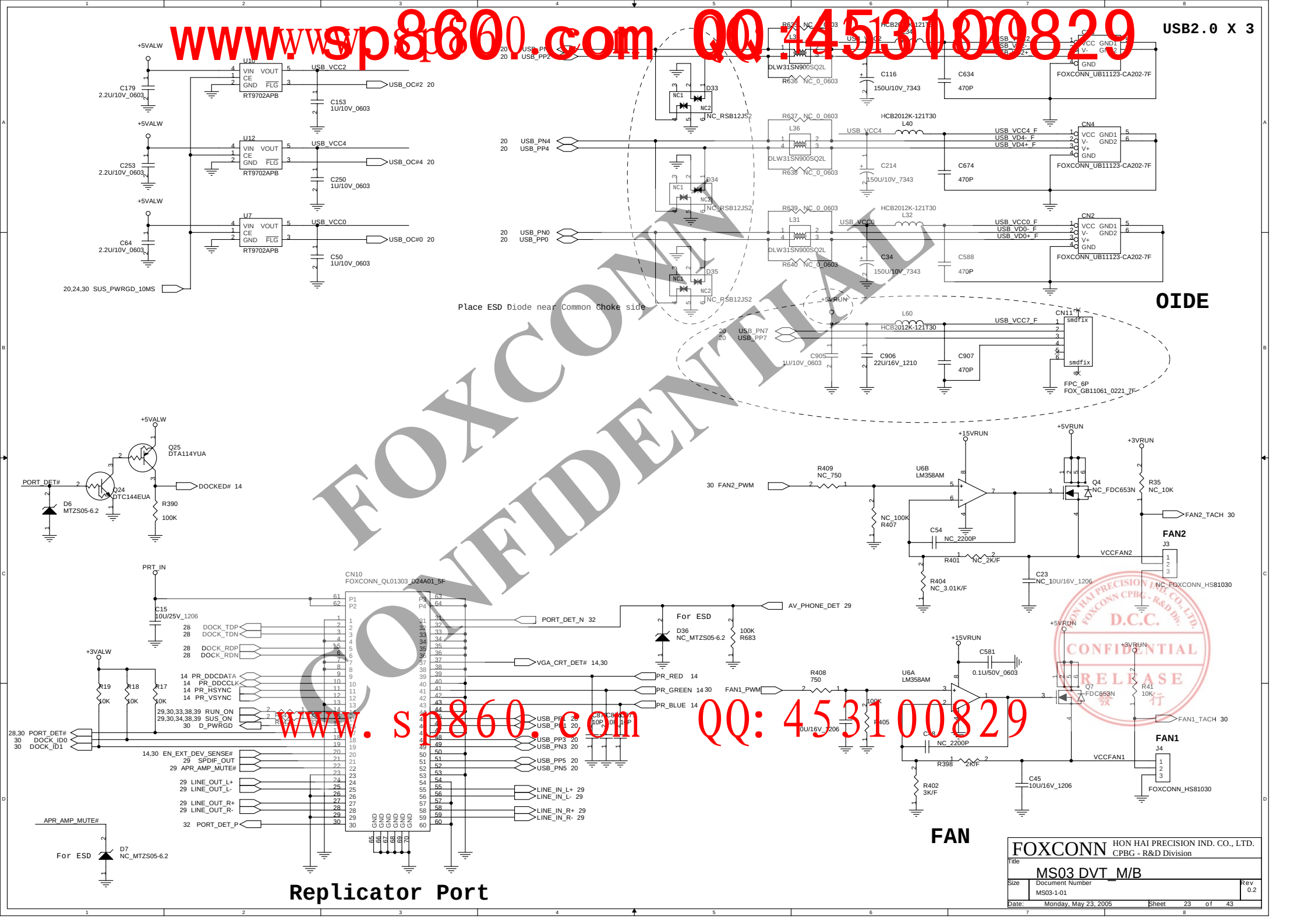

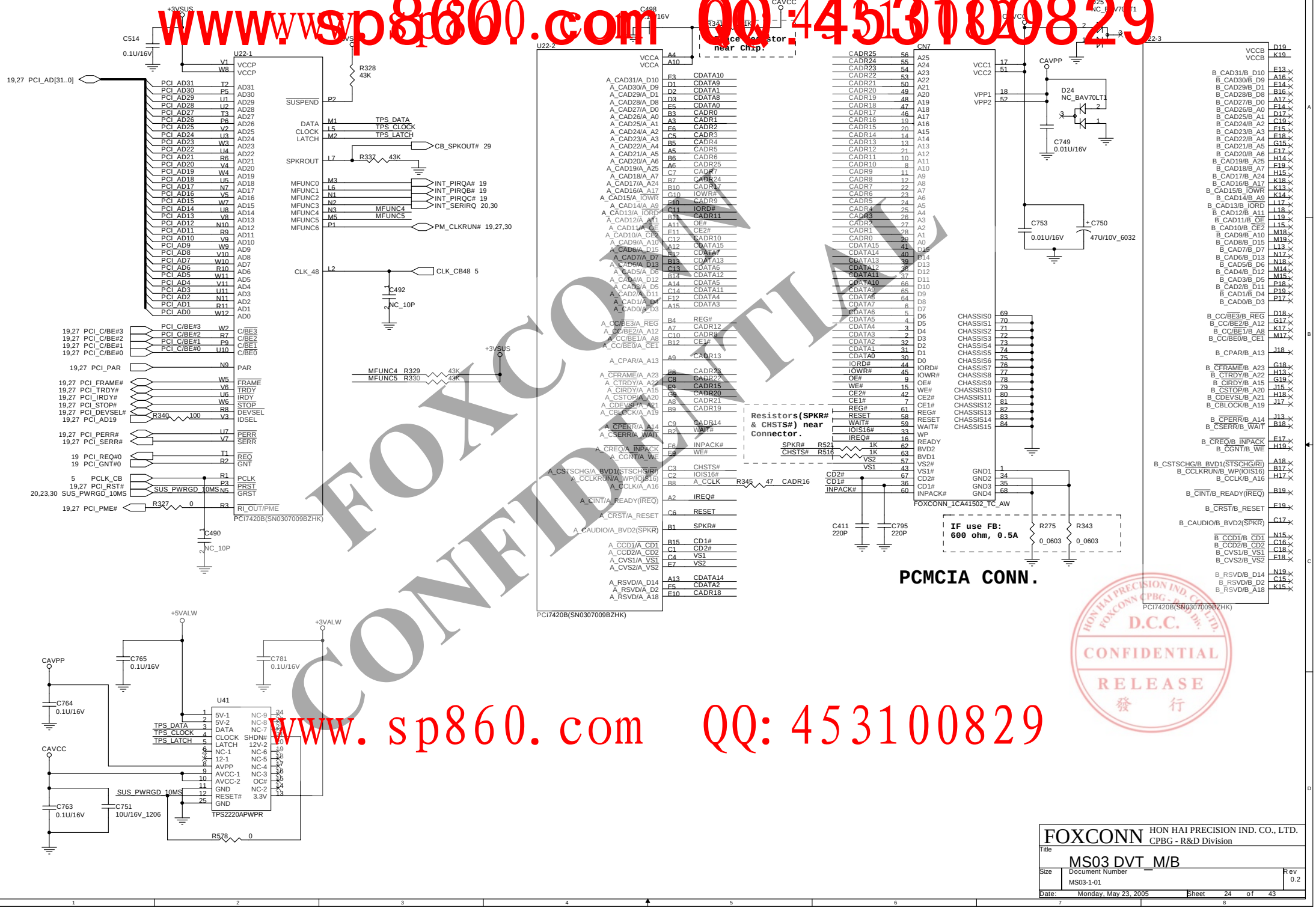

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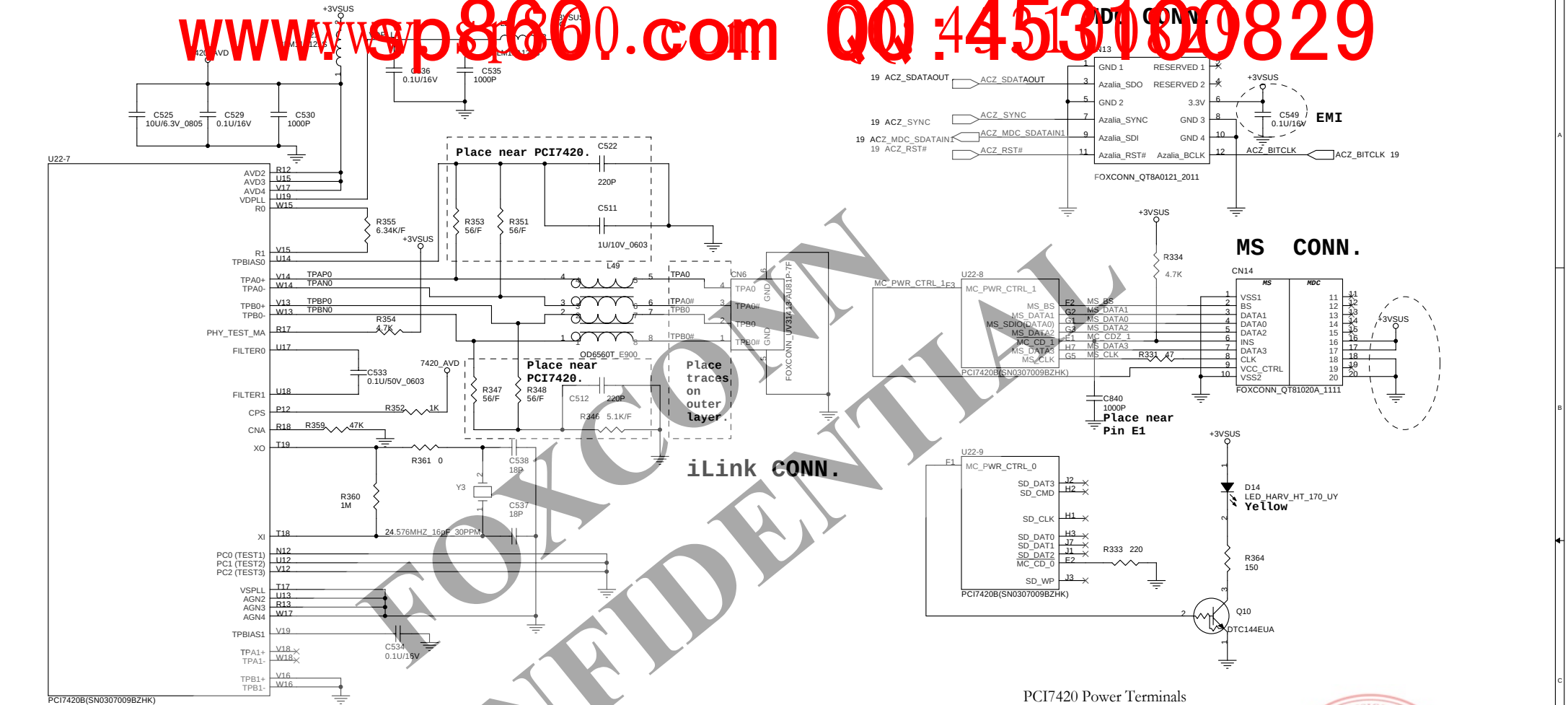
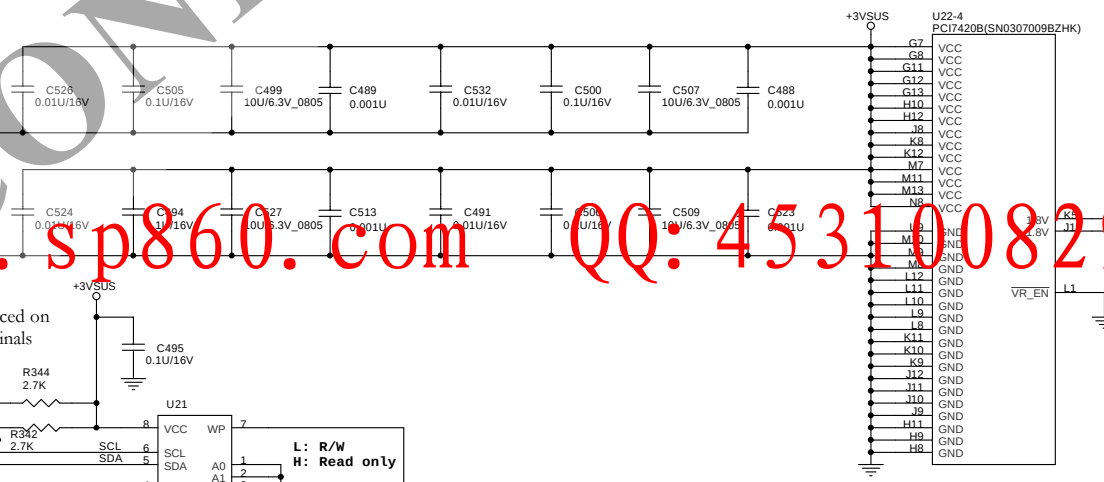
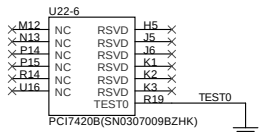


PCI7420 Power Terminals



PCI7420 UNUSED TERMINALS



Resistors should be placed on the SCL and SDA terminals

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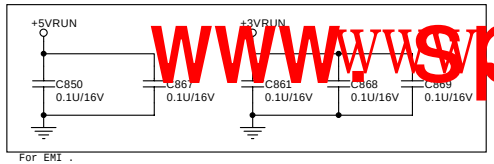

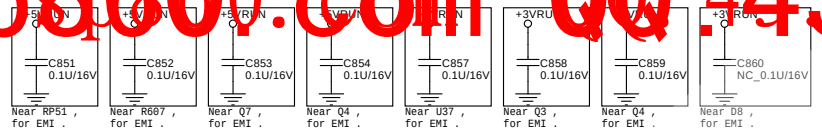

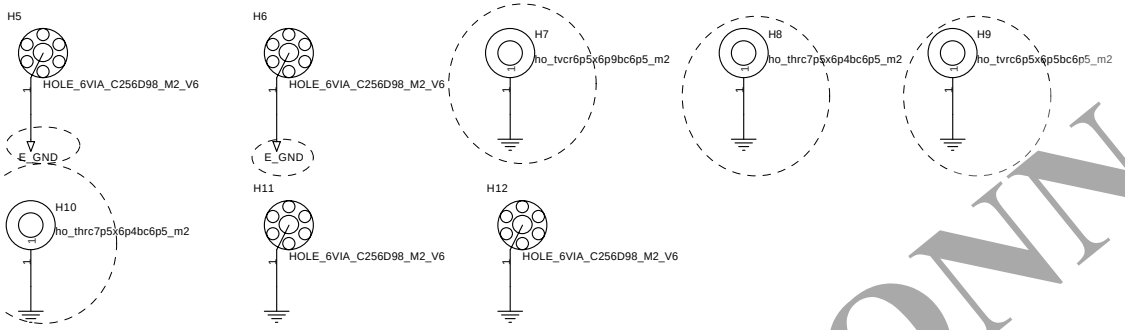

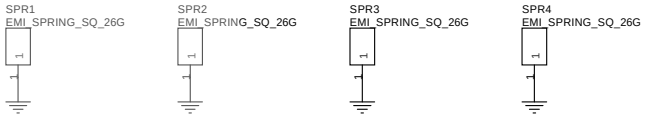

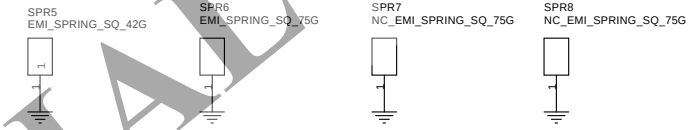

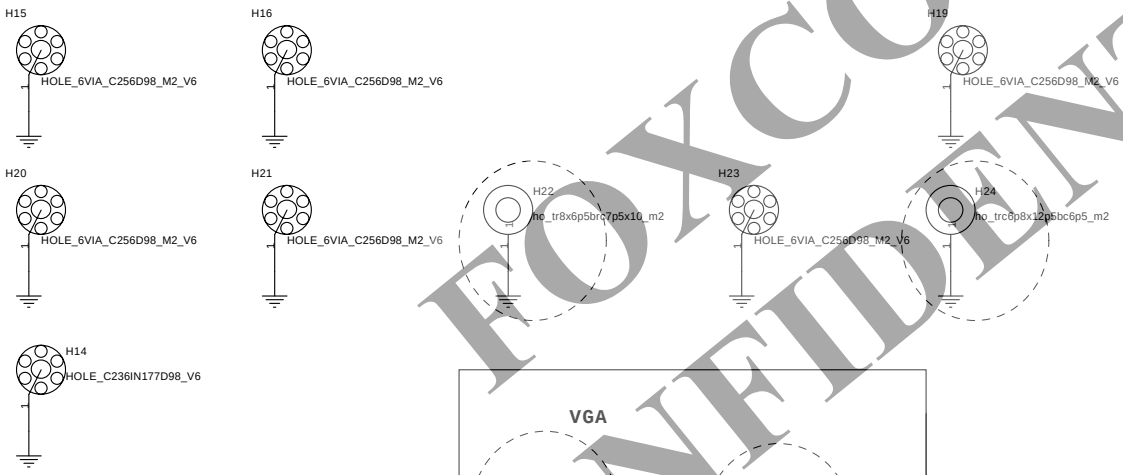

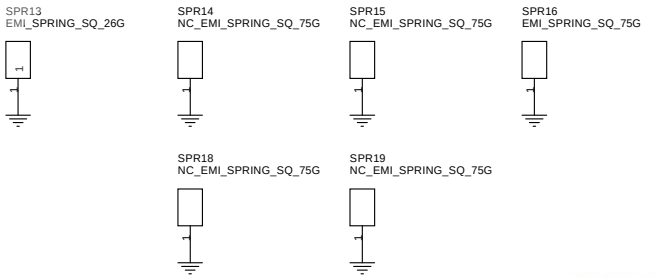

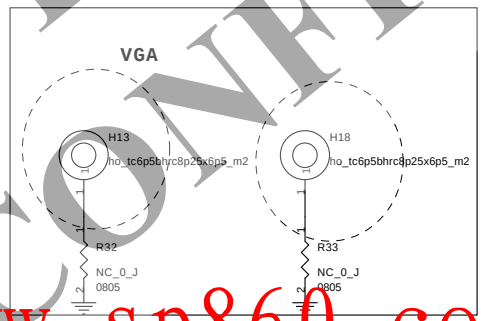

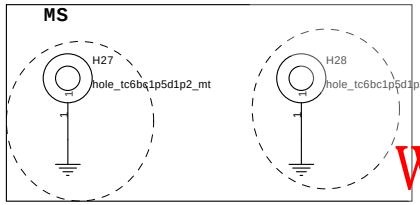

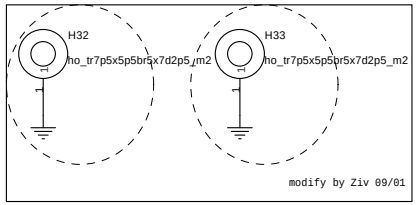

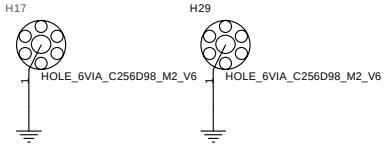

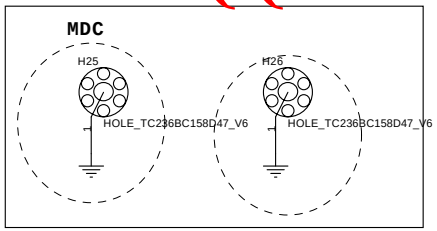

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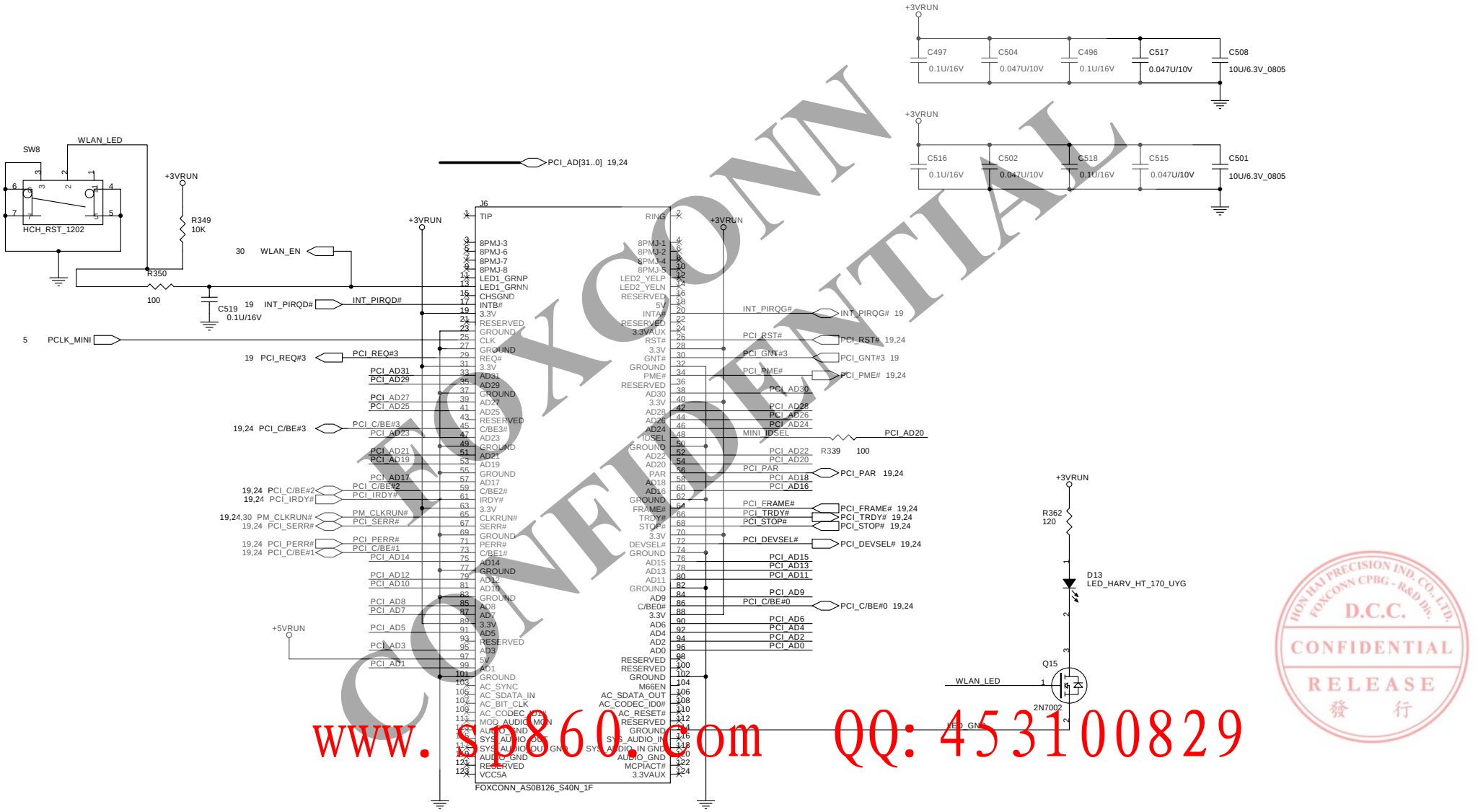

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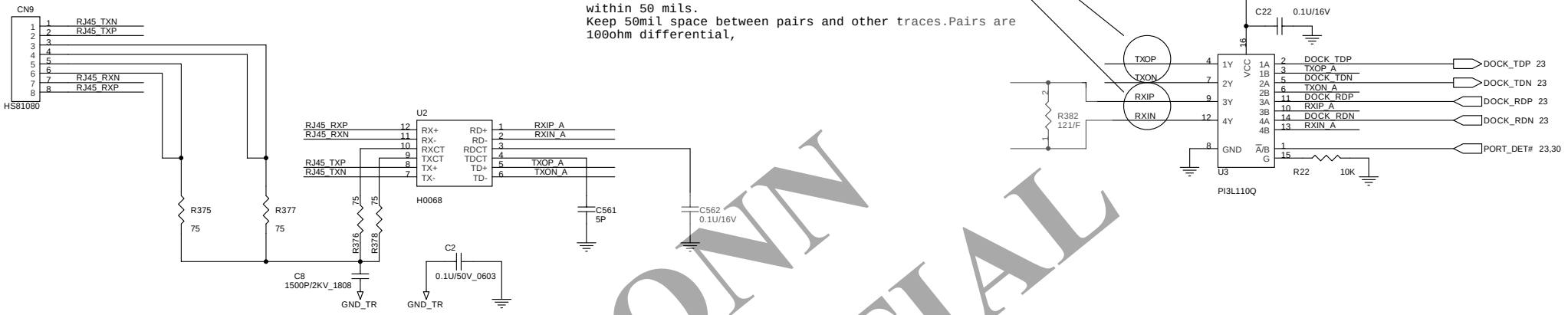
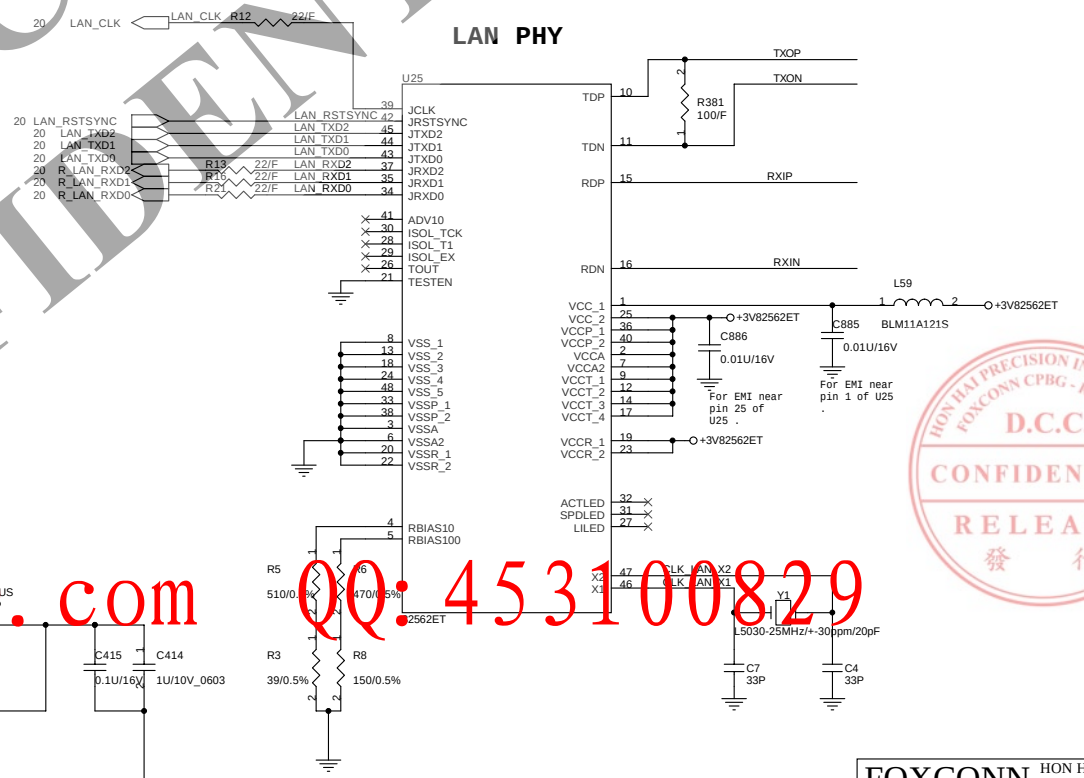
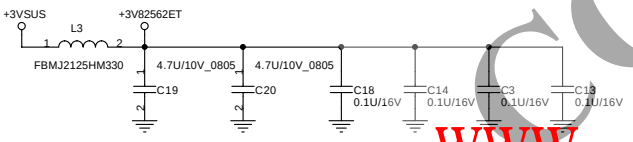
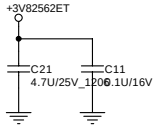
Match length of cable side Rx and Tx pair traces +/- 50 mil
LAYOUT NOTES:
Match total length of chip side Tx and Rx pair traces +/- 50mil
Match length of cable side Rx and Tx pair traces +/- 50 mil
Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,

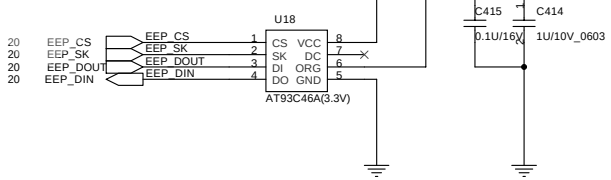


LAN PHY









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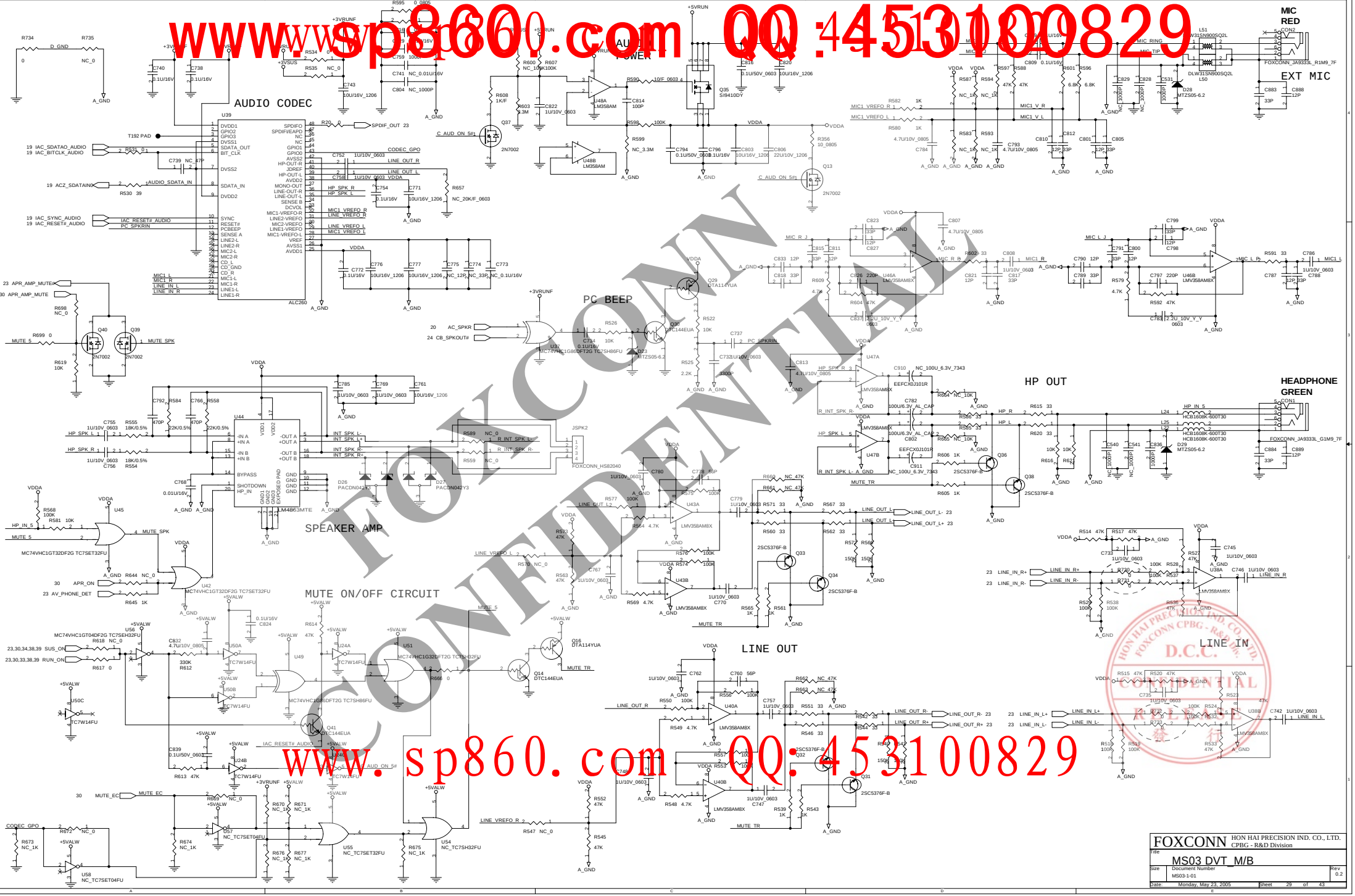

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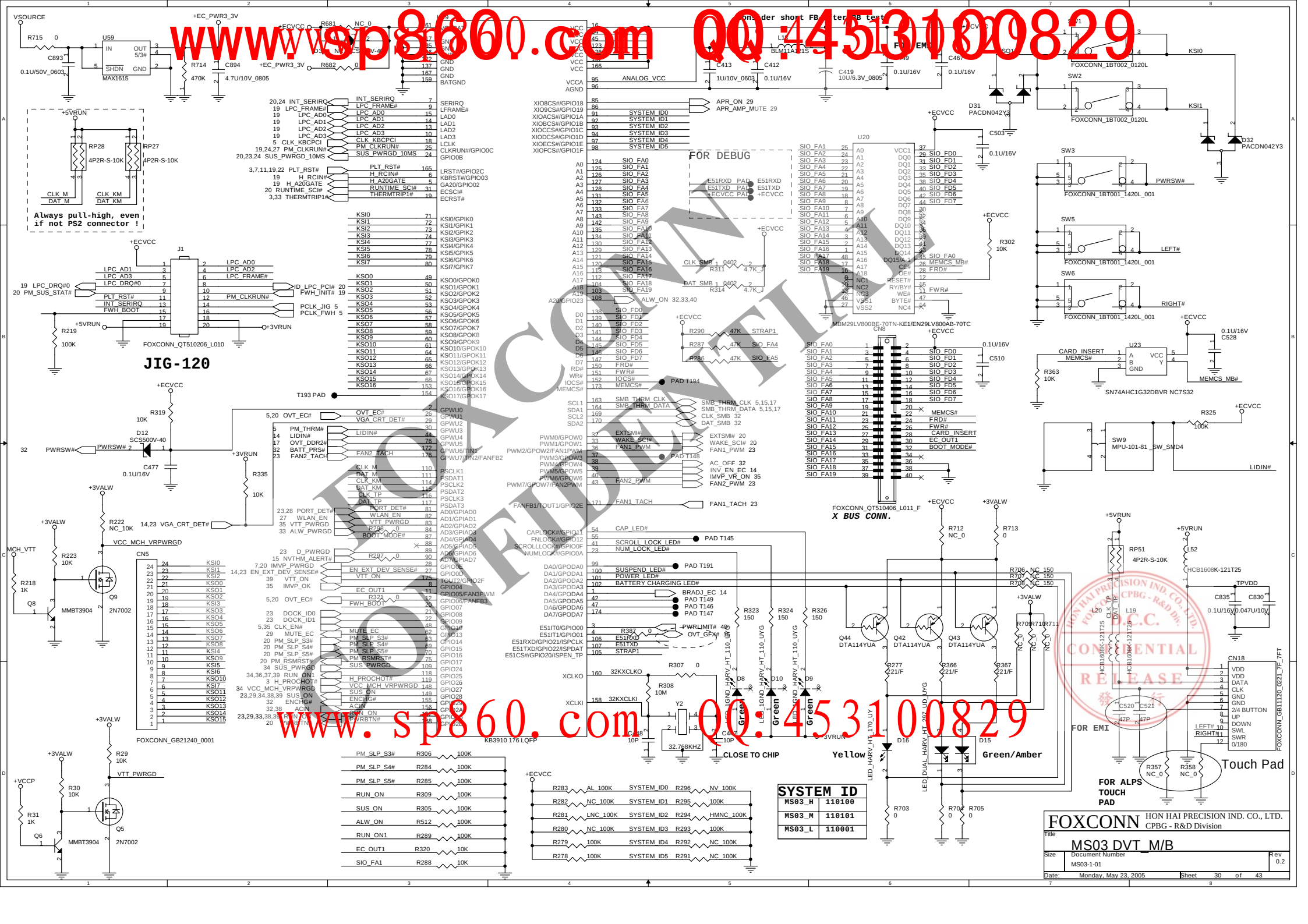

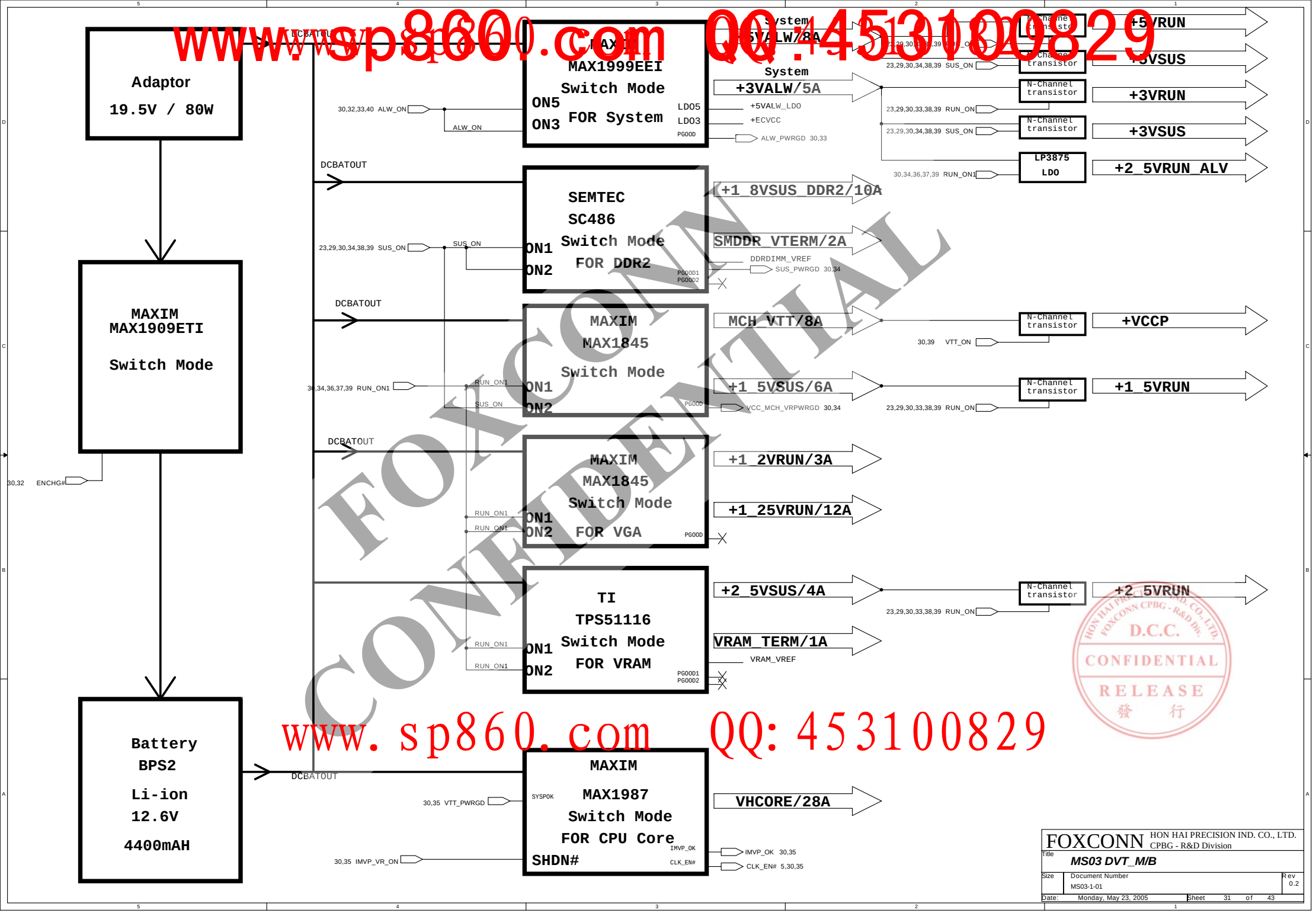

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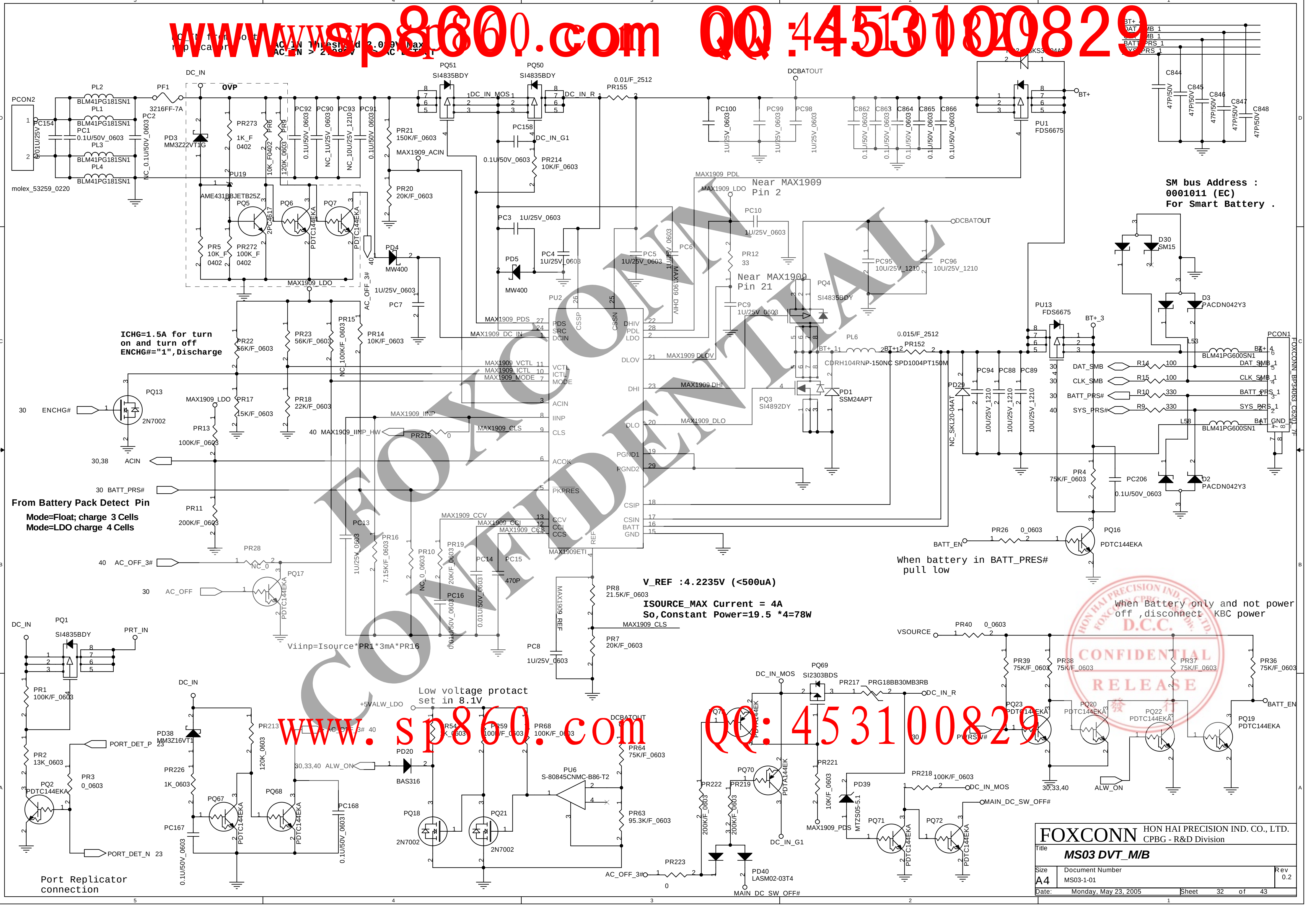

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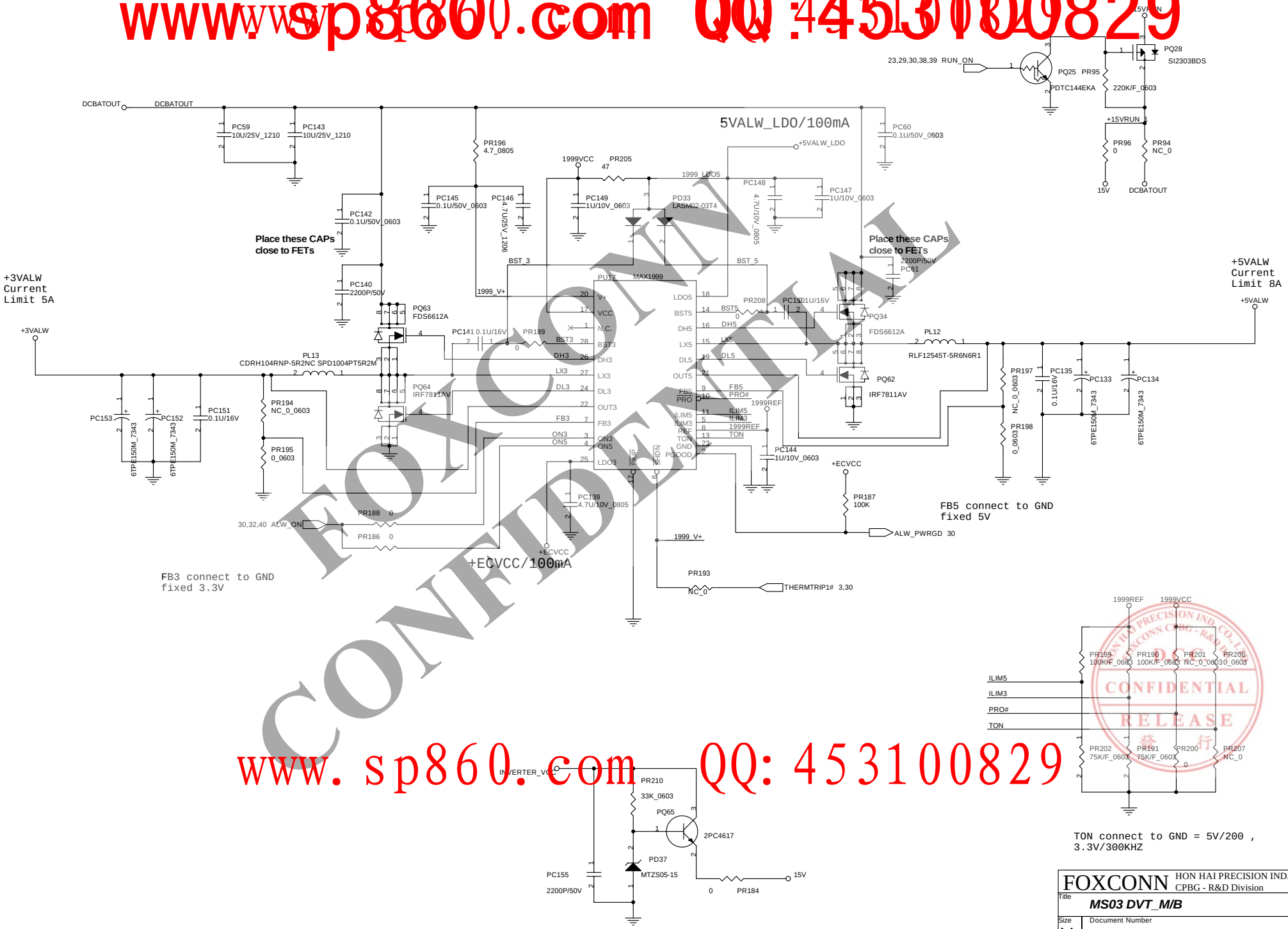

TON connect to GND = 5V/200 , 3.3V/300KHZ

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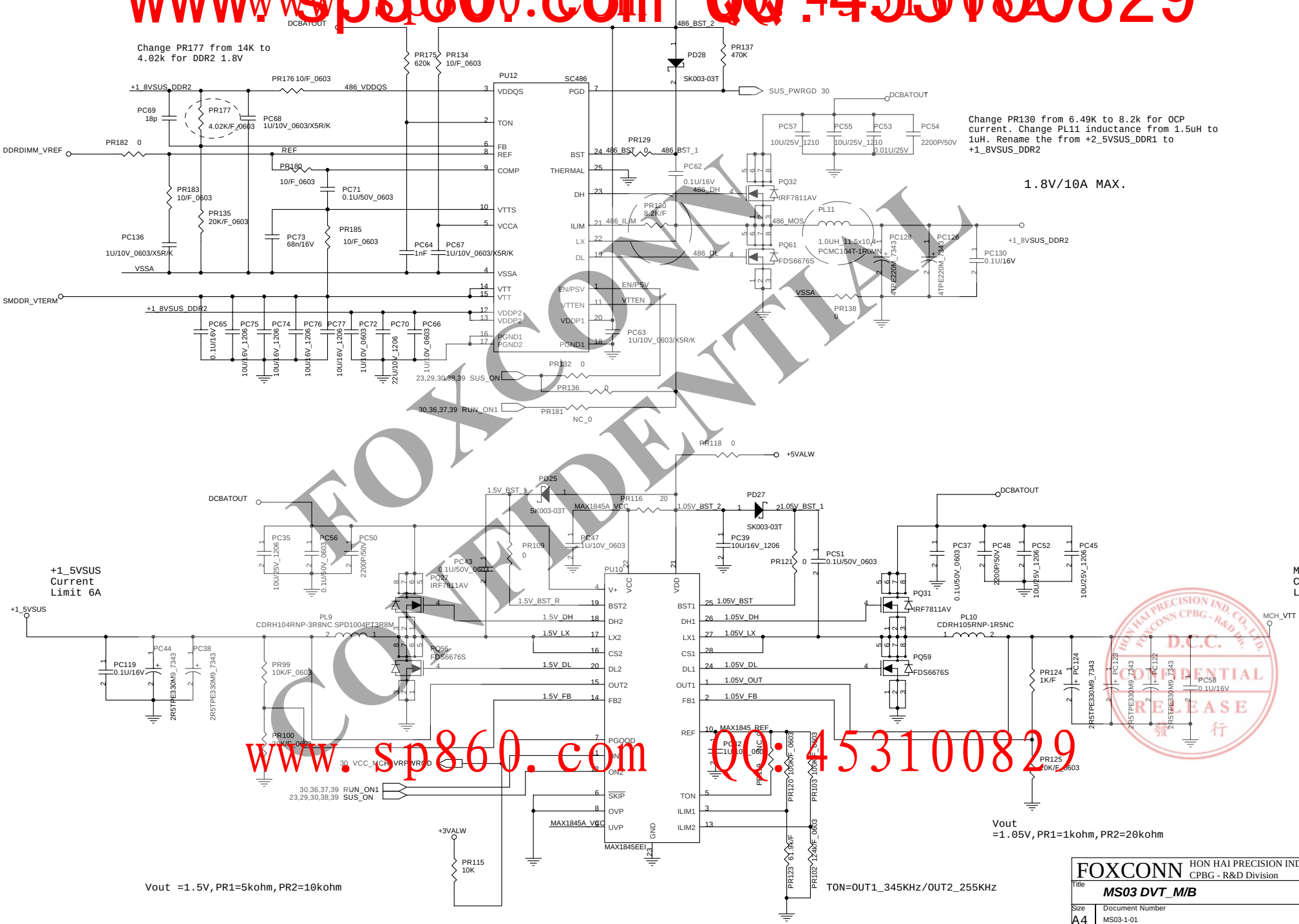

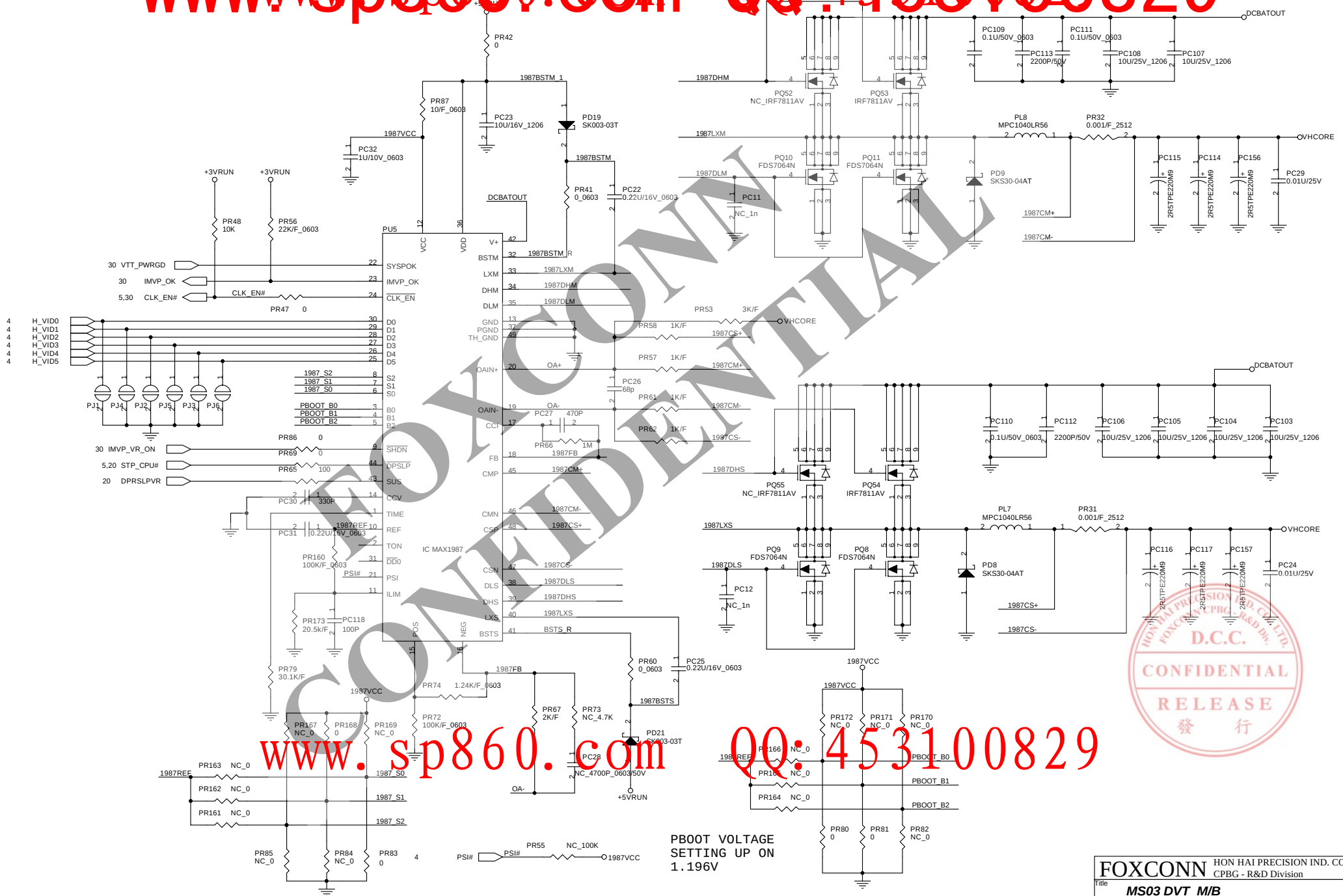

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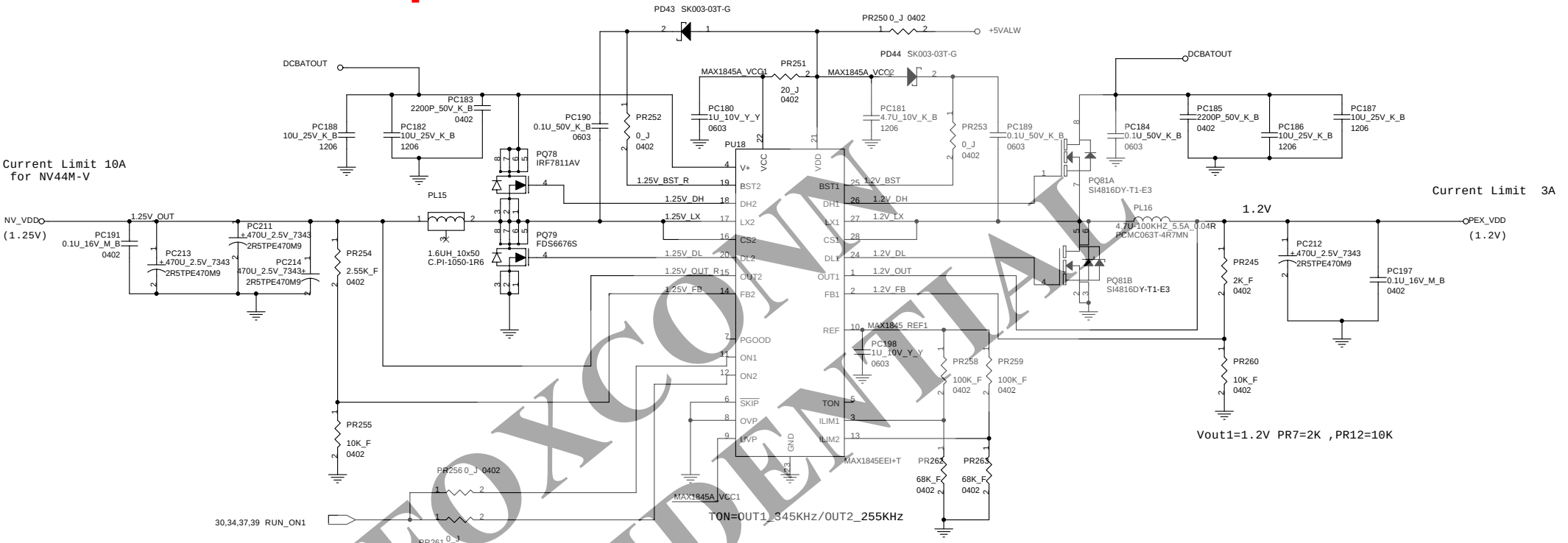

Power daughter board for VGA

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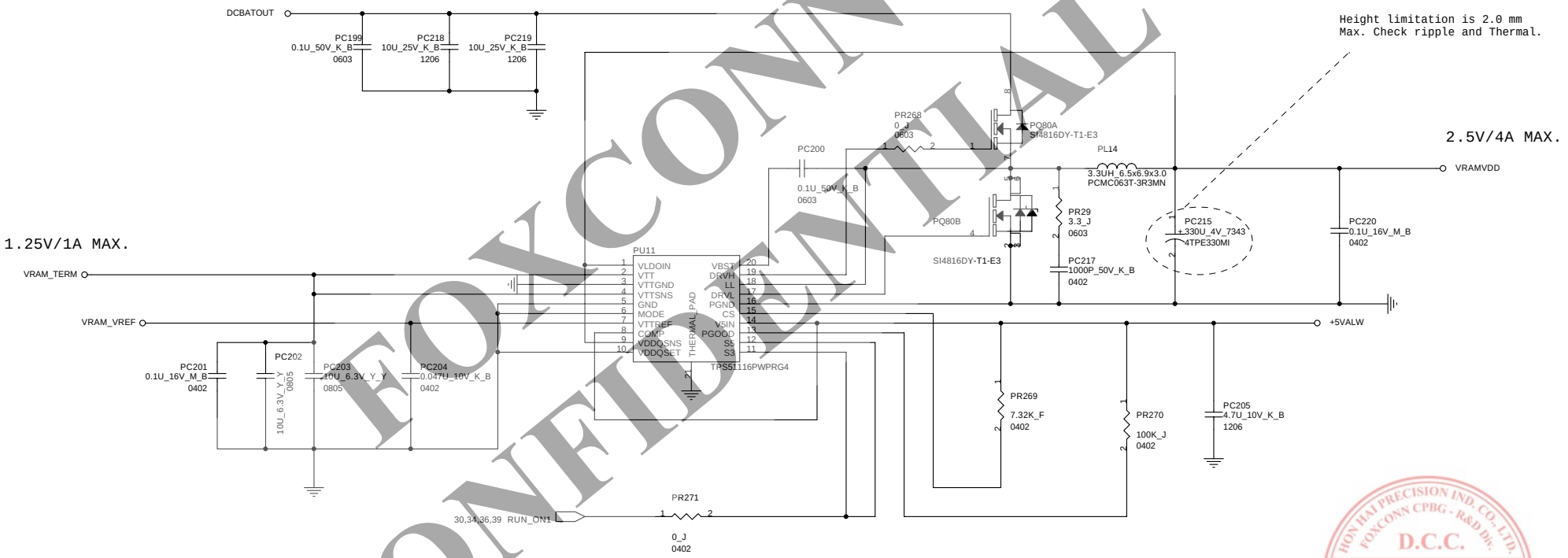

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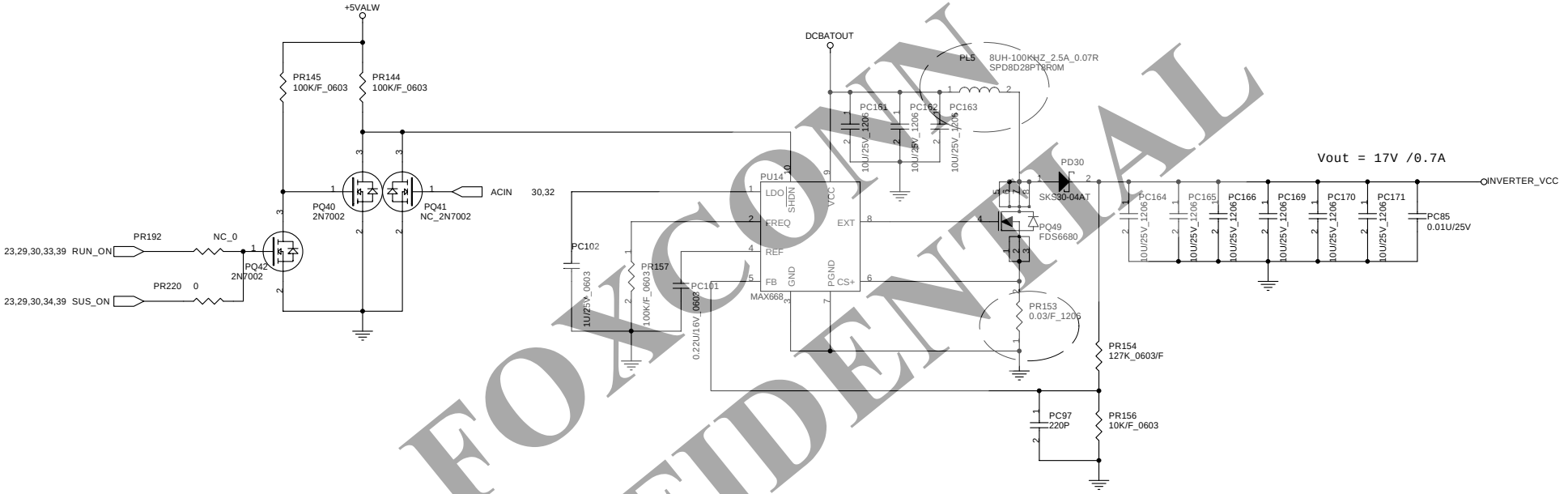
Change PL5 and PR153 for improving the step-up circuit



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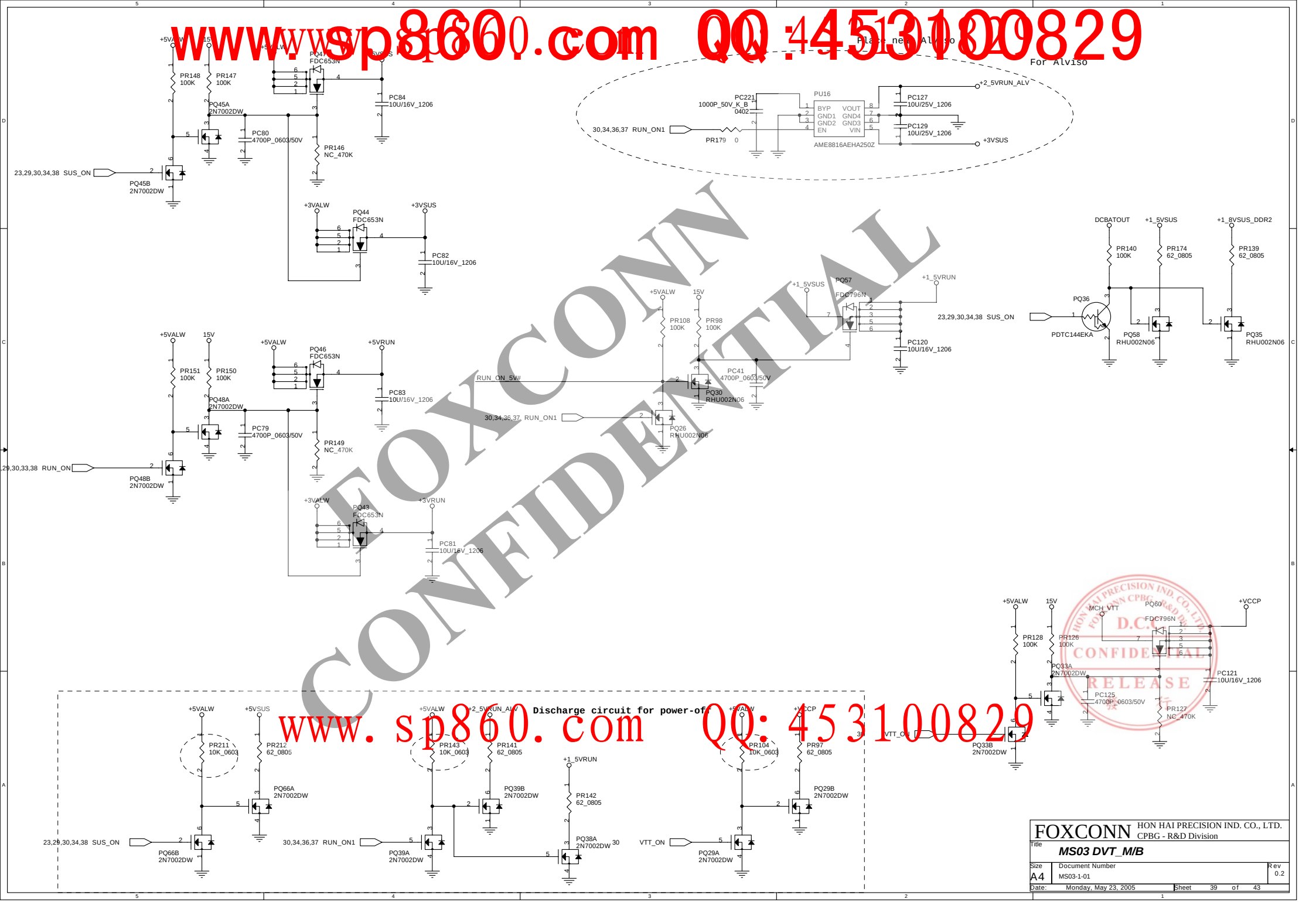

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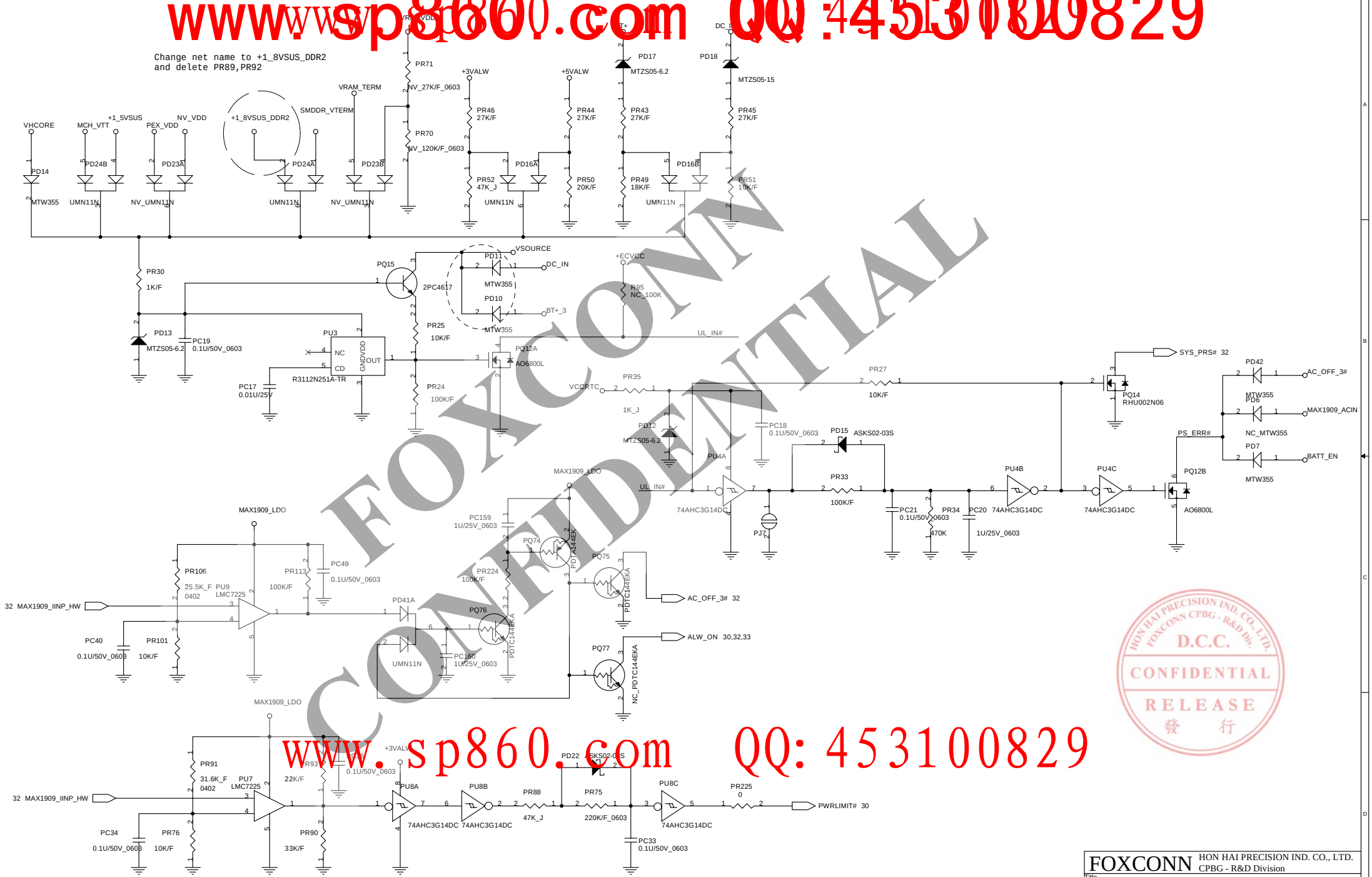

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HISTORY

EVT board start.

(2005/03/31)

P14: Change D1 from NC to mount.

P15: Change R115 from mount to NC.

(2005/04/01)

P40: Rotate PD10, PD11.

(2005/04/12)

P14: Correct LVDS Bus relative of connection (swap Data+/Data-, CLK+/CLK-).

P25: Change CN14 pin16, pin17 from NC to +3VSUS, change CN14 pin18, pin20 from NC to GND.

P30: Delete SW7, Q46, R396, R721.

(2005/04/25)

P12: Add T195 for measure VRAM Timing.

(2005/04/26)

P14: Delete the right side dot of L1.

(2005/04/29)

P14: Change Q22, Q23 from 2N7002 to BSS138.

(2005/05/04)

P14: Change R694, R695, R696, R697 from 2.2K to 0 ohm.

(2005/05/09)

P26: Change H14 part from HOLE_6VIA_C256IN177D98_M2_V6(6.5mm) to HOLE_C236IN177D98_V6(6.0mm).

P15: Change R701 from NC to mount, change R702 from mount to NC.

(2005/05/10)

P32: Change PD3 from P4SSMJ24APT to MM3Z22VT1G.

P32: Change PQ5 from PDTC144EKA to 2PC4617.

P32: Change PR5 from 75K/F_0603 to 10K/F_0402.

P32: Change PR6 from 120K_0603 to 10K/F_0402.

P32: Add PU19 AME, AME431BBJETB25Z.

P32: Add PR272 100K/F_0402.

P32: Add PR273 1K/F_0402.

P36: Change PR262 from 15.8K/F_0402 to 68K/F_0402.

P36: Change PR263 from 40.2K/F_0402 to 68K/F_0402.

P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to CHOKE_3P_315_394X394_2.

P36: Delete PJ11, PJ12.

P37: Delete PJ13, PJ14.

P39: Delete PJ8, PR178.

P39: Add PC221 1000P_50V_0402.

P39: Change PU16 from LP3875 to AME8816AEHA250Z.

P05: Change R478, R481 from 33ohm to 56ohm for rising edge rate and falling edge rate.

P05: Change C696, C698, C700, C701, C702, C706 from NC to 18pF (EMI solution).

P22: Add C730, C731 (EMI solution).

P22: Connect CN17.20, CN17.32, CN17.44 to GND.

P26: Change SPR7, SPR15 from mount to NC (EMI solution).

(2005/05/11)

P23: Add D33,D34 and D35 for ESD(Not mount).

P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to L_3P_315_394X394.

(2005/05/13)

P26: Change H25, H26 footprint from ho_tc236bc158d17_v6 to ho_tc236bc158d17_h7.

P26: Change H27, H28 footprint from ho_tc1p5bc6d1p2_v2 to ho_tc1p5bc6d1p2_hb.

(2005/05/16)

P02: Update symbol ahead table, add LNC_ and HMNC_.

P30: Change R280 from mount to NC.

P30: Change R281 from AL_100K to LNC_100K.

P30: Change R293 from NC to mount.

P30: Change R294 from NV_100K to HMNC_100K.

(2005/05/17)

P26: Add R32, R33 NC_0_J (EMI solution).

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HISTORY

(2005/05/18)

P29: Change C783, C837 from [illegible] to [illegible]

P26: Change H27, H28 from ho_tc1p5bc6d1p2_m2(ho_tc1p5bc6d1p2_mb) to hole_tc6bc1p5d1p2_mt(ho_tc6bc1p5d1p2_mt).

P40: Change PR91 from 31.6K to 25.5K, change PR109 from 49.9K to 31.6K.

P29: Delete R611, R622, R628, R629, R647, R648, R649, R650, JSPK1.

P29: Add C910, C911 NC_100U_6.3V_7343.

(2005/05/19)

P29: Add R734,R735 for anti-digital noise interference.

(2005/05/20)

P30: Change R311, R314 from 10K to 4.7K_J.

P29: Change R735 from mount to NC.

P05: Change R481 from 56ohm to 47ohm.

P05: Change R478 from 56ohm to 47ohm.

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Revision History

Doc. Rev.	ECN No.:	Sch. Page	Rev Change From	Rev Change To	Description of Change

Doc. Rev.	ECN No.:	Sch. Page	Rev Change From	Rev Change To	Description of Change

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