Page	Title of schematic page	Rev.	Date
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02	Block Diagram	1A	
03	Change List	1A	
04	ICS9LR3197	1A	
05	PROCESSOR 1/4(DMI&HOST&PCI)	1A	
06	PROCESSOR 2/4(DDR)	1A	
07	PROCESSOR 3/4(POWER)	1A	
08	PROCESSOR 4/4(GND)	1A	
09	PCH 1/5 (DMI&VIDEO)	1A	
10	PCH 2/5 (SATA/LPC/Azalia)	1A	
11	PCH 3/5 (PCI/PCIE/CLK/USB)	1A	
12	PCH 4/5 (GPIO)	1A	
13	PCH 5/5 (POWER)	1A	
14	DDR3 DIMM	1A	
15	CRT/LVDS	1A	
16	WWAN/Light Sensor	1A	
17	WPCE775L & FLASH	1A	
18	Docking/35001/TP/S1	1A	
19	HDD/ODD/SSD	1A	
20	KB/USB/FAN/Reset	1A	
21	HDMI	1A	
22	POWER CPU CORE (ISL62882)	1A	
23	POWER 3VPCU&5VPCU(PM6686)	1A	
24	POWER 1.5VSUS/VTT_MEM	1A	
25	POWER VCC1.05(OZ8111LN)-26A	1A	
26	POWER VCC_CFXCORE(MAX17028)	1A	
27	POWER(ADAPTER IN / CONN)	1A	
28	POWER VCC1.8	1A	
29	NVIDIA N11M-GE1 PCIE&PW 1/3	1A	
30	NVIDIA N11M-GE1 TMDS&DAC 2/3	1A	
31	NVIDIA N11M-GE1 VRAM 3/4	1A	
32	NVIDIA N11M-GE1 VRAM 4/4	1A	
33	R5U231	1A	

QUANTA COMPUTER

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GD3 Block Diagram

VRAM gDDR3 P31,P32 — 64Mx16 4PCS

NVIDIA/AMD N11M-GE1 23x23mm P29-P30

PCIE 16Lanes

CPU Arrandale 989 PIN (micro FC-PGA) P5-P8

DDR3 800/1066 1.5V — UNBUFFERED DDR3 SODIMM P14

DDR3 800/1066 1.5V — UNBUFFERED DDR3 SODIMM P14

14.318MHz — CLOCK GEN ICS9LRS3105 P4

TMDS — HDMI P21

LVDS — LCD P15

R/G/B — CRT P15

TMDS — Docking DVI P18

FDI interface

DMI(4X)

Puma Peak 2x2 AGN(Intel WiFi Link 6200)
Kilmer Peak 2x2 AGN(Imtel WiMAX/WiFi Link 6250)

WLAN Module Puma peak/Kilmer Peak
Intel : HB91 or 97
Atheros : HB91 or 97 P16

MS/SD R5U231 P33

LAN Giga Atheros AR8131M P16

Docking LAN Atheros AR8131M P18

ExpressCard/34 P18

SD

MS_HG

1394

RJ45

PCIE #1 #2 #3 #4 #5 #6 #7 #8

PCH
Ibex Peak-M
B-3 Step
676 BGA
31mm x 31mm
P9-P13

INT. HM57 + SPI rom 8MB
INT. HM55 + SPI rom 4MB
HM55 + SPI rom 4MB(Hynix)
HM55 + SPI rom 4MB(Samsung)

ME BIOS 4M P19

Azalia Link

ALC275
ALC262 for back up Plan P19

MIC. Jack P19 — Audio Jack P19 — INT.SPKR. P19 — Digital MIC Knowles SPM0405HE4H P19

USB 1.1/2.0 — USB Slot *3 P23; Finger Print TCS5B P18; ExpressCard *1 P18; Blue Tooth T77M114.11 P18; Camera P23; Felica P18; WiMAX P16; WWAN Gobi2000; Docking USB HUB

SATA Port 0 — SATA HDD *1 P16

SATA Port 1 — SATA ODD *1 P10

3.3V LPC,33MHZ

PCU
WPC775
P17

TOUCH PAD — T/P SWITCH

INT.K/B P20

SPI BIOS 2M P10

LED
CAPS/NUM/SCRL
Wireless/WWAN/BT
Power/Speep
HDD
MS/SD
Charge

Button
POWER
Wireless SW
B1/B2/B3/ODD

Light Sensor TAOS TSL2561FN P16

SM BUS G Sensor LIS331DL

ExpressCard
USB CON*1
PCI-E *1

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DVT change list

0708:
-P4 Delete R518 0 ohm.
-P4 Delete R1
-P4 Y1 change pin assignment.
-P4 Add R621
-P4 R6 change PU to PD and mount 10K.
-P5 Add Q67 2N7002.(For GFX PROCHOT)
-P5 U2.AN15 add GFX_PROHOT Net.(For GFX_PROCHOT)
-P9 R567 no mount(Driver from EC)
-P10 R152 change from 33 to SBK160808T-121Y-N.(For EMI)
-P10 C156 mount 22PF.(For EMI)
-P10 R133 change from 4.7K to 51 ohm
-P10 Swap U54 pin2 & pin5.
-P10 Add R619 2.37K/F.
-P10 R126 change from 4.7K to 2.37K/F
-P11 Add R622 10K(For PCIE_REQ_WLAN)
-P11 RP8 mount for Ext. only
-P11 Add Q66 2N7002(For PCIE_REQ_WLAN)
-P11 Add Y3 25MHz for Int. only.
-P11 Add R179 1M (For Int. only).
-P11 Add C168,C169 6.8PF (For Int. only)
-P11 R584 mount 0 ohm(for N11 only)
-P11 D1 change to SW1010CPT.(For 3VPCU leakage)
-P11 Add R624 10k for N11 SKU only.
-P11 R186 mount 10k.(For Int. only)
-P13 Delete R218,R220 0 ohm.(save cost)
-P13 Delete R215 0_25.(save cost)
-P13 Mount C214,C188 1uF.
-P14 Swap SMDDR_VREF_DQ0 & SMDDR_VREF_DQ1
-P14 R227,R232 mount 470 ohm.
-P15 L12,L13,L14 change to BK1608H680.
-P15 CON4 pin assignment reverse.(ME request)
-P17 Add R620 2.2K
-P17 R314 value change from 39K to 100K.
-P17 Delete D55
-P17 Add Q65 PDTA124EU.
-P17 D58 mount
-P17 Add R623 100K .(For EC idle mode save power)
-P17 D9,D10,D12,D13,D14,D15,D16,D17, D18,D19 change from SW1010CPT to RB501V-40.
-P17 Add D59 RB501V-40.(For SCI# leakage current)
-P18 R330 change Pull-up from RVCC3 to VCC3.
-P19 CON44 change to "掀蓋式".
-P19 CON17 pin assignment reverse.
-P19 R588 change from 37.2K/F to 36K/F.(For ODD current limit)
-P19 CON10 change footprint.(add Lock pin)
-P20 Q48 change footprint to "SOT23_213-3_3-2"
-P20 Q57 change from PDTC144EU to 2N7002E.
-P20 R573 change from 5.2K to 3.01K.
-P21 CON32 change pin assignment.
-P22 PC23,PC24 no mount.
-P22 Add PR311 68 ohm.(for Prochot# in IMVP6.5)
-P22 PC19 & PC25 modify net
-P23 Delete PG1,PG2
-P23 PR93 change net from"+VCC_CFXCORE-1" to "+VGA_CORE"
-P23 PC59 1000P delete (For VCC3 timing)
-P23 PC61 1000P delete (For VCC5 timing)
-P24 PR280 change to 820K(For VCC1.5 timing)
-P24 PC212 change to 2200P(For VCC1.5 timing)
-P24 PR119 change to 0 ohm
-P24 PC94 no mount
-P24 Add PD40 RB501V-40.(for N11 powerr off time)
-P24 Delete PG16.
-P24 Delete PG13,PG14
-P24 PR214 no mount
-P25 Delete PG7,PG8
-P26 PR178 change from 7.5K/F to 6.04K/F.(VGA OCP)
-P26 Add PR312 10K ohm.(For GFX PROCHOT)
-P26 Add PR313 0 ohm.(For GFX PROCHOT)
-P26 Add PD39 RB501V-40.
-P26 Delete PG9,PG10
-P26 PC141 change to E@0.1UF (Ext. only)(+VGA_CORE timing)
-P26 PR202 change to 47K(For +VGA_CORE timing)
-P26 VID For External VGA_CORE circuit modify
-P28 Delete PG11
-P28 PC225 change to 0.1UF.(For VCC1.8 timing)
-P30 R4045 change from GND to VCC3
-P30 R4047 change from VCC3 to GND
-P30 Add R4108 Pull-high,(PU-ES sample,PD QS sample)
-P31 CON32 reverse pin assignment
-P33 C322,C323 change from 27PF to 22PF.

0804
-P5 Add Q68,R628,R630,R629,R633 for DRAMRST#
-P5 R22 change power from +1.5VCU to VCC1.5_CPU
-P7 C108,C110 change height to lower.
-P7 VDDQ power change to VCC1.5_CPU
-P10 Y2 change footprint
-P12 U4.C38 change to BT_PRS#
-P12 U4.AA4 change to CRIT_TEMP_REP#
-P12 U4.F1 change to DRAMRST_CNTRL_PCH.
-P12 R577 change from GND to RVCC3
-P13 C178 change from 1U to 10uF.(For CRT wave noise)
-P15 Delete L15.(save cost)
-P17 R615 mount 0 ohm
-P17 U18.106 change to CRIT_TEMP_REP#.
-P17 Add R625 100K.(For RSMRST# abnormal shutdown)
-P17 D11 change to SW1010CPT
-P17 Add R626,R627 0 ohm.
-P18 Add C752,C753 1000P.(For EMI)
-P19 U30.9 delete net.
-P19 C392 change to 10UF.(reduce ripple)
-P19 CON44.14 change to GND
-P19 CON44.42 change to HDA_BCLK0
-P19 CON44.44 change to GND
-P24 Add Pq74,PR314,PD41,PC242,PR315,PR316,PQ75
-P29 L4001 change to PBY160808T-221Y-N(220,2A).
-P33 CON8 change footprint.
-P33 R298 change from 68 to 22 ohm

0805
-P5 Add C756 470PF.
-P5 R22 change value from 1.1K/F to 1.5K/F(For S3 power)
-P5 R23 change value from 3K/F to 750/F.(For S3)
-P5 Add U64,C755,R634. (For S3 power)
-P5 U2.F6 change to DRAMRST_CPU#
-P7 C688 mount 330UF(Reduce ripple)
-P8 U2.J17 U2.H17 delete net "DDR_VREF_DQ0""DDR_VREF_DQ1"
-P10 Delete R583
-P10 R152 change from 0603 to 0402
-P13 Add C754 0.01uF(Reduce ripple)
-P13 L6,L7 change to TDK MKG1608B10NJ
-P13 C190 change from 0.1U to 1uF.
-P14 Delete U7.(thermal don't use)
-P14 Delete R228,R230,R231,R233
-P14 CON1.1 CON2.2 change net to "SMDDR_VREF_DQ0"
-P15 R241,R242 change to 33 ohm.
-P15 R237,R238 change to 4.7K
-P15 delete L10,L11
-P15 Add R631 100K.
-P15 Add F17.
-P16 Delete F10
-P17 R321 no mount
-P17 Add 5V_RESET net
-P17 U63.6 add DRAMRST_CNTRL net
-P17 Add R632 10K
-P17 U22.1 add net"5V_RESET#"
-P18 P373,C374,C375 mount 10P.
-P18 CON15 change to Foxconn,(EMI solution)
-P18 Add D60
-P20 U57 change input voltage from VCC5 to 5VPCU.
-P22 PR1 change to 2.2/F_6
-P23 PQ10,PQ13 change to AON7406.(Reduce ripple)
-P23 Add PU16,PR317,PR318,PR319,PD42,PC243,PC244,PC245
-P24 PU4.11 add net "VCC1.5_CPU_VCC105_PWRGD"
-P24 PR120 delete
-P24 PR124 value change to 8.06K/F
-P24 Add PU17,PR320,PC246,PR321,PR323,PC247,PR322,PR324
-P24 Add PR110,PQ30
-P24 Add PQ77
-P24 Delete PR120,PR130
-P24 PR314 change to 100K/F
-P24 PC242 change to 2200PF.
-P24 Add PQ74 NTMFS4935
-P24 Add PQ75 2N7002E
-P24 Add PR316 220_6 ohm
-P28 PR137 mount 24.9K/F
-P28 PR141 mount 470K/NTC/THINKING_4
-P29 Delete R4002

QUANTA COMPUTER

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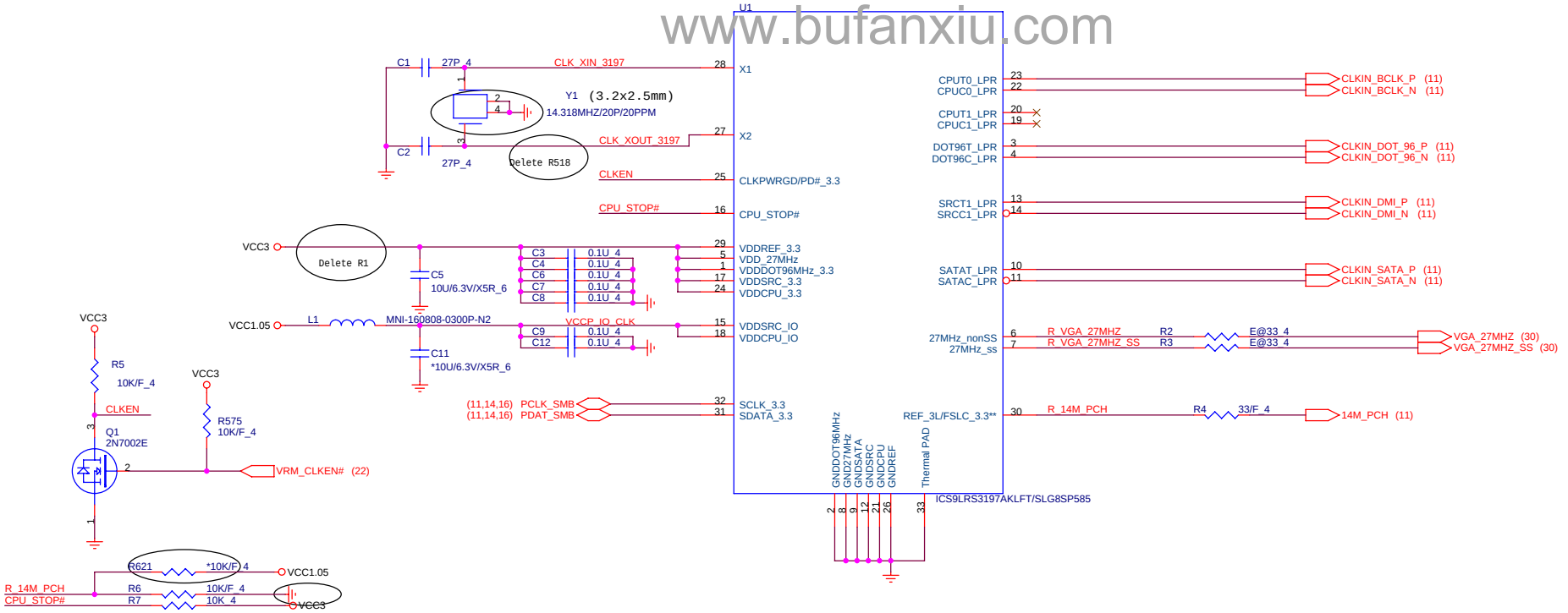

CPU Frequency Select Table

FSLC	CPU MHz	SRC MHz	REF MHz	USB MHz	DOT MHz
0(default)	133.33	100.00	14.318	48.00	96.00
1	100.00				

Table 2: pin 6, 7 Configuration

B1b4	B1b3	B1b2	B1b1	Pin 6 MHz	Pin 7 MHz	Spread %	Comment
0	0	0	0	N/A	N/A	N/A	N/A
0	0	0	1	N/A	N/A	N/A	N/A
0	0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	
0	0	1	1	27MHz_nonSS	27MHz_SS	-1%	
0	1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
0	1	0	1	27MHz_nonSS	27MHz_SS	-2%	
0	1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
0	1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	
1	0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
1	0	0	1	27MHz_nonSS	27MHz_SS	+-0.5%	
1	0	1	0	27MHz_nonSS	27MHz_SS	+-0.75%	
1	0	1	1	N/A	N/A	N/A	N/A
1	1	0	0	N/A	N/A	N/A	N/A
1	1	0	1	N/A	N/A	N/A	N/A
1	1	1	0	N/A	N/A	N/A	N/A
1	1	1	1	N/A	N/A	N/A	N/A

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	0	0	0	56 pin TSSOP
0	0	0	1	64 pin TSSOP
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	72 pin QFN
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	32 pin QFN
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 3: IO_Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

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QUANTA COMPUTER

Title	CLOCK GENERATOR	
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ARRANDALE PROCESSOR (DMI,PEG,FDI)

ARRANDALE PROCESSOR (CLK,MISC,JTAG)

U2A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

Arrandale

U2B

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

Arrandale

XDP Signal

JTAG MAPPING

Scan Chain (Default)	STUFF -> R27, R30, R37 NO STUFF -> R29, R34
CPU Only	STUFF -> R27, R29 NO STUFF -> R30, R34, R37
GMCH Only	STUFF -> R34, R37 NO STUFF -> R27, R29, R30

Processor Pullups

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QUANTA COMPUTER

Title	PROCESSOR 1/4(HOST&PCI)	
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ARRANDALE PROCESSOR (DDR3)

U2C

DDR SYSTEM MEMORY A

(14) M_A_DQ[63:0]

M_A_DQ0	A10	SA_DQ[0]
M_A_DQ1	C10	SA_DQ[1]
M_A_DQ2	C7	SA_DQ[2]
M_A_DQ3	A7	SA_DQ[3]
M_A_DQ4	B10	SA_DQ[4]
M_A_DQ5	D10	SA_DQ[5]
M_A_DQ6	E10	SA_DQ[6]
M_A_DQ7	A8	SA_DQ[7]
M_A_DQ8	D8	SA_DQ[8]
M_A_DQ9	F10	SA_DQ[9]
M_A_DQ10	F6	SA_DQ[10]
M_A_DQ11	F7	SA_DQ[11]
M_A_DQ12	E9	SA_DQ[12]
M_A_DQ13	B7	SA_DQ[13]
M_A_DQ14	E7	SA_DQ[14]
M_A_DQ15	C6	SA_DQ[15]
M_A_DQ16	H10	SA_DQ[16]
M_A_DQ17	G8	SA_DQ[17]
M_A_DQ18	K7	SA_DQ[18]
M_A_DQ19	J8	SA_DQ[19]
M_A_DQ20	G7	SA_DQ[20]
M_A_DQ21	G10	SA_DQ[21]
M_A_DQ22	J7	SA_DQ[22]
M_A_DQ23	J10	SA_DQ[23]
M_A_DQ24	L7	SA_DQ[24]
M_A_DQ25	M6	SA_DQ[25]
M_A_DQ26	M8	SA_DQ[26]
M_A_DQ27	L9	SA_DQ[27]
M_A_DQ28	L6	SA_DQ[28]
M_A_DQ29	K8	SA_DQ[29]
M_A_DQ30	N8	SA_DQ[30]
M_A_DQ31	P9	SA_DQ[31]
M_A_DQ32	AH5	SA_DQ[32]
M_A_DQ33	AF5	SA_DQ[33]
M_A_DQ34	AK6	SA_DQ[34]
M_A_DQ35	AK7	SA_DQ[35]
M_A_DQ36	AF6	SA_DQ[36]
M_A_DQ37	AG5	SA_DQ[37]
M_A_DQ38	AJ7	SA_DQ[38]
M_A_DQ39	AJ6	SA_DQ[39]
M_A_DQ40	AJ10	SA_DQ[40]
M_A_DQ41	AJ9	SA_DQ[41]
M_A_DQ42	AL10	SA_DQ[42]
M_A_DQ43	AK12	SA_DQ[43]
M_A_DQ44	AK8	SA_DQ[44]
M_A_DQ45	AL7	SA_DQ[45]
M_A_DQ46	AK11	SA_DQ[46]
M_A_DQ47	AL8	SA_DQ[47]
M_A_DQ48	AN8	SA_DQ[48]
M_A_DQ49	AM10	SA_DQ[49]
M_A_DQ50	AR11	SA_DQ[50]
M_A_DQ51	AL11	SA_DQ[51]
M_A_DQ52	AM9	SA_DQ[52]
M_A_DQ53	AN9	SA_DQ[53]
M_A_DQ54	AT11	SA_DQ[54]
M_A_DQ55	AP12	SA_DQ[55]
M_A_DQ56	AM12	SA_DQ[56]
M_A_DQ57	AN12	SA_DQ[57]
M_A_DQ58	AM13	SA_DQ[58]
M_A_DQ59	AT14	SA_DQ[59]
M_A_DQ60	AT12	SA_DQ[60]
M_A_DQ61	AL13	SA_DQ[61]
M_A_DQ62	AR14	SA_DQ[62]
M_A_DQ63	AP14	SA_DQ[63]

(14) M_A_BS#0	AC3	SA_BS[0]
(14) M_A_BS#1	AB2	SA_BS[1]
(14) M_A_BS#2	U7	SA_BS[2]
(14) M_A_CAS#	AE1	SA_CAS#
(14) M_A_RAS#	AB3	SA_RAS#
(14) M_A_WE#	AE9	SA_WE#

SA_CK[0]	AA6	M_A_CLK0 (14)
SA_CK#[0]	AA7	M_A_CLK0# (14)
SA_CKE[0]	P7	M_A_CKE0 (14)
SA_CK[1]	Y6	M_A_CLK1 (14)
SA_CK#[1]	Y5	M_A_CLK1# (14)
SA_CKE[1]	P6	M_A_CKE1 (14)
SA_CS#[0]	AE2	M_A_CS#0 (14)
SA_CS#[1]	AE8	M_A_CS#1 (14)
SA_ODT[0]	AD8	M_A_ODT0 (14)
SA_ODT[1]	AF9	M_A_ODT1 (14)

SA_DM[0]	B9	M_A_DM0
SA_DM[1]	D7	M_A_DM1
SA_DM[2]	H7	M_A_DM2
SA_DM[3]	M7	M_A_DM3
SA_DM[4]	AG6	M_A_DM4
SA_DM[5]	AM7	M_A_DM5
SA_DM[6]	AN10	M_A_DM6
SA_DM[7]	AN13	M_A_DM7

M_A_DM[7:0] (14)

SA_DQS#[0]	C9	M_A_DQS#0
SA_DQS#[1]	F8	M_A_DQS#1
SA_DQS#[2]	J9	M_A_DQS#2
SA_DQS#[3]	N9	M_A_DQS#3
SA_DQS#[4]	AH7	M_A_DQS#4
SA_DQS#[5]	AK9	M_A_DQS#5
SA_DQS#[6]	AP11	M_A_DQS#6
SA_DQS#[7]	AT13	M_A_DQS#7

M_A_DQS#[7:0] (14)

SA_DQS[0]	C8	M_A_DQS0
SA_DQS[1]	F9	M_A_DQS1
SA_DQS[2]	H9	M_A_DQS2
SA_DQS[3]	M9	M_A_DQS3
SA_DQS[4]	AH8	M_A_DQS4
SA_DQS[5]	AK10	M_A_DQS5
SA_DQS[6]	AN11	M_A_DQS6
SA_DQS[7]	AR13	M_A_DQS7

M_A_DQS[7:0] (14)

SA_MA[0]	Y3	M_A_A0
SA_MA[1]	W1	M_A_A1
SA_MA[2]	AA8	M_A_A2
SA_MA[3]	AA3	M_A_A3
SA_MA[4]	V1	M_A_A4
SA_MA[5]	AA9	M_A_A5
SA_MA[6]	V8	M_A_A6
SA_MA[7]	T1	M_A_A7
SA_MA[8]	Y9	M_A_A8
SA_MA[9]	U6	M_A_A9
SA_MA[10]	AD4	M_A_A10
SA_MA[11]	T2	M_A_A11
SA_MA[12]	U3	M_A_A12
SA_MA[13]	AG8	M_A_A13
SA_MA[14]	T3	M_A_A14
SA_MA[15]	V9	M_A_A15

M_A_A[15:0] (14)

Arrandale

U2D

DDR SYSTEM MEMORY - B

(14) M_B_DQ[63:0]

M_B_DQ0	B5	SB_DQ[0]
M_B_DQ1	A5	SB_DQ[1]
M_B_DQ2	C3	SB_DQ[2]
M_B_DQ3	B3	SB_DQ[3]
M_B_DQ4	E4	SB_DQ[4]
M_B_DQ5	A6	SB_DQ[5]
M_B_DQ6	A4	SB_DQ[6]
M_B_DQ7	C4	SB_DQ[7]
M_B_DQ8	D1	SB_DQ[8]
M_B_DQ9	D2	SB_DQ[9]
M_B_DQ10	F2	SB_DQ[10]
M_B_DQ11	F1	SB_DQ[11]
M_B_DQ12	C2	SB_DQ[12]
M_B_DQ13	F5	SB_DQ[13]
M_B_DQ14	F3	SB_DQ[14]
M_B_DQ15	G4	SB_DQ[15]
M_B_DQ16	H6	SB_DQ[16]
M_B_DQ17	G2	SB_DQ[17]
M_B_DQ18	J6	SB_DQ[18]
M_B_DQ19	J3	SB_DQ[19]
M_B_DQ20	G1	SB_DQ[20]
M_B_DQ21	G5	SB_DQ[21]
M_B_DQ22	J2	SB_DQ[22]
M_B_DQ23	J1	SB_DQ[23]
M_B_DQ24	J5	SB_DQ[24]
M_B_DQ25	K2	SB_DQ[25]
M_B_DQ26	L3	SB_DQ[26]
M_B_DQ27	M1	SB_DQ[27]
M_B_DQ28	K5	SB_DQ[28]
M_B_DQ29	K4	SB_DQ[29]
M_B_DQ30	M4	SB_DQ[30]
M_B_DQ31	N5	SB_DQ[31]
M_B_DQ32	AF3	SB_DQ[32]
M_B_DQ33	AG1	SB_DQ[33]
M_B_DQ34	AJ3	SB_DQ[34]
M_B_DQ35	AK1	SB_DQ[35]
M_B_DQ36	AG4	SB_DQ[36]
M_B_DQ37	AG3	SB_DQ[37]
M_B_DQ38	AJ4	SB_DQ[38]
M_B_DQ39	AH4	SB_DQ[39]
M_B_DQ40	AK3	SB_DQ[40]
M_B_DQ41	AK4	SB_DQ[41]
M_B_DQ42	AM6	SB_DQ[42]
M_B_DQ43	AN2	SB_DQ[43]
M_B_DQ44	AK5	SB_DQ[44]
M_B_DQ45	AK2	SB_DQ[45]
M_B_DQ46	AM4	SB_DQ[46]
M_B_DQ47	AM3	SB_DQ[47]
M_B_DQ48	AP3	SB_DQ[48]
M_B_DQ49	AN5	SB_DQ[49]
M_B_DQ50	AT4	SB_DQ[50]
M_B_DQ51	AN6	SB_DQ[51]
M_B_DQ52	AN4	SB_DQ[52]
M_B_DQ53	AN3	SB_DQ[53]
M_B_DQ54	AT5	SB_DQ[54]
M_B_DQ55	AT6	SB_DQ[55]
M_B_DQ56	AN7	SB_DQ[56]
M_B_DQ57	AP6	SB_DQ[57]
M_B_DQ58	AP8	SB_DQ[58]
M_B_DQ59	AT9	SB_DQ[59]
M_B_DQ60	AT7	SB_DQ[60]
M_B_DQ61	AP9	SB_DQ[61]
M_B_DQ62	AR10	SB_DQ[62]
M_B_DQ63	AT10	SB_DQ[63]

(14) M_B_BS#0	AB1	SB_BS[0]
(14) M_B_BS#1	W5	SB_BS[1]
(14) M_B_BS#2	R7	SB_BS[2]
(14) M_B_CAS#	AC5	SB_CAS#
(14) M_B_RAS#	Y7	SB_RAS#
(14) M_B_WE#	AC6	SB_WE#

SB_CK[0]	W8	M_B_CLK0 (14)
SB_CK#[0]	W9	M_B_CLK0# (14)
SB_CKE[0]	M3	M_B_CKE0 (14)
SB_CK[1]	V7	M_B_CLK1 (14)
SB_CK#[1]	V6	M_B_CLK1# (14)
SB_CKE[1]	M2	M_B_CKE1 (14)
SB_CS#[0]	AB8	M_B_CS#0 (14)
SB_CS#[1]	AD6	M_B_CS#1 (14)
SB_ODT[0]	AC7	M_B_ODT0 (14)
SB_ODT[1]	AD1	M_B_ODT1 (14)

SB_DM[0]	D4	M_B_DM0
SB_DM[1]	E1	M_B_DM1
SB_DM[2]	H3	M_B_DM2
SB_DM[3]	K1	M_B_DM3
SB_DM[4]	AH1	M_B_DM4
SB_DM[5]	AL2	M_B_DM5
SB_DM[6]	AR4	M_B_DM6
SB_DM[7]	AT8	M_B_DM7

M_B_DM[7:0] (14)

SB_DQS#[0]	D5	M_B_DQS#0
SB_DQS#[1]	E4	M_B_DQS#1
SB_DQS#[2]	J4	M_B_DQS#2
SB_DQS#[3]	L4	M_B_DQS#3
SB_DQS#[4]	AH2	M_B_DQS#4
SB_DQS#[5]	AL4	M_B_DQS#5
SB_DQS#[6]	AR5	M_B_DQS#6
SB_DQS#[7]	AR8	M_B_DQS#7

M_B_DQS#[7:0] (14)

SB_DQS[0]	C5	M_B_DQS0
SB_DQS[1]	E3	M_B_DQS1
SB_DQS[2]	H4	M_B_DQS2
SB_DQS[3]	M5	M_B_DQS3
SB_DQS[4]	AG2	M_B_DQS4
SB_DQS[5]	AL5	M_B_DQS5
SB_DQS[6]	AP5	M_B_DQS6
SB_DQS[7]	AR7	M_B_DQS7

M_B_DQS[7:0] (14)

SB_MA[0]	U5	M_B_A0
SB_MA[1]	V2	M_B_A1
SB_MA[2]	T5	M_B_A2
SB_MA[3]	V3	M_B_A3
SB_MA[4]	R1	M_B_A4
SB_MA[5]	T8	M_B_A5
SB_MA[6]	R2	M_B_A6
SB_MA[7]	R6	M_B_A7
SB_MA[8]	R4	M_B_A8
SB_MA[9]	R5	M_B_A9
SB_MA[10]	AB5	M_B_A10
SB_MA[11]	P3	M_B_A11
SB_MA[12]	R3	M_B_A12
SB_MA[13]	AF7	M_B_A13
SB_MA[14]	P5	M_B_A14
SB_MA[15]	N1	M_B_A15

M_B_A[15:0] (14)

Arrandale

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	PROCESSOR 2/4(DDR)	
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Date: Monday, August 31, 2009	Sheet 6 of 33	

ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU:
ARRANDALE 1.05V
(18A)

Please note that +VCC_GFX_CORE
should be 1.05V in Auburndale

change height to lower.

Clarksfiled VTT=1.1 VTT_Select=Low
Arrandale VTT=1.05 VTT_Select=High

For Turbo Mode

CRB default VID[6:0]=0100100
PSI# default=0
DPRSLPVR default=1

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QUANTA COMPUTER

Title	PROCESSOR 3/4(POWER)	
Size: Custom	Document Number: GD3 Main Board	Rev: 2A
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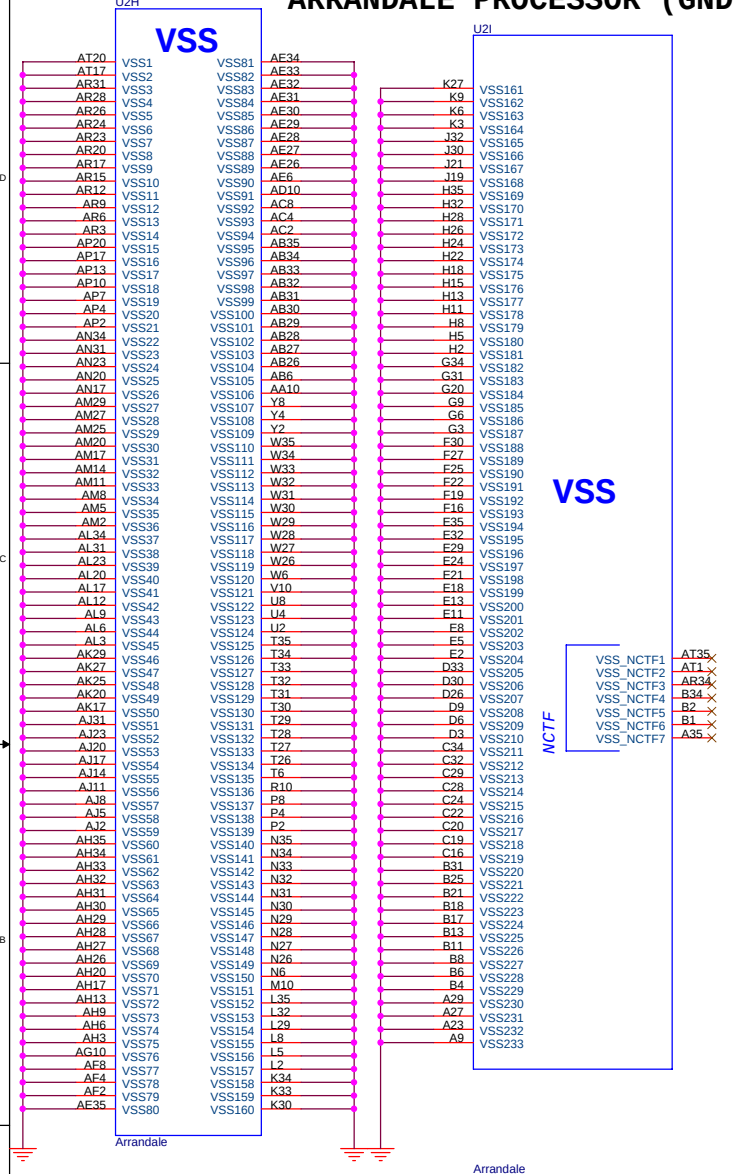
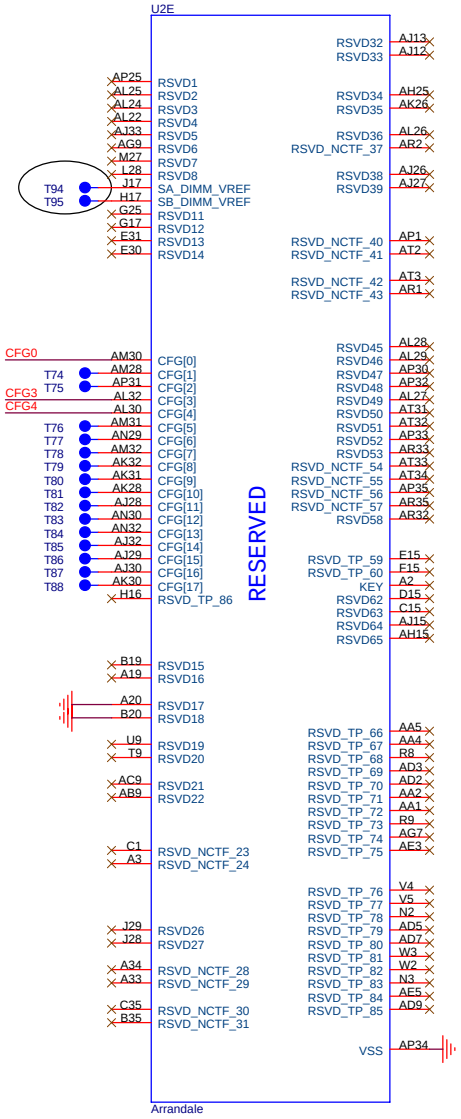
ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR(RESERVED, CFG)



CFG0 R73 *3.01K_4

Not applicable for Clarksfield Processor

PCI-Epress Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enabled

CFG3 R74 3.01K_4

PCI-Epress Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Diplay Port 0 : Enabled; An external Display port device is connected to the Embedded Display port

CFG4 R75 *3.01K_4

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QUANTA COMPUTER

Title: PROCESSOR 4/4(GND)

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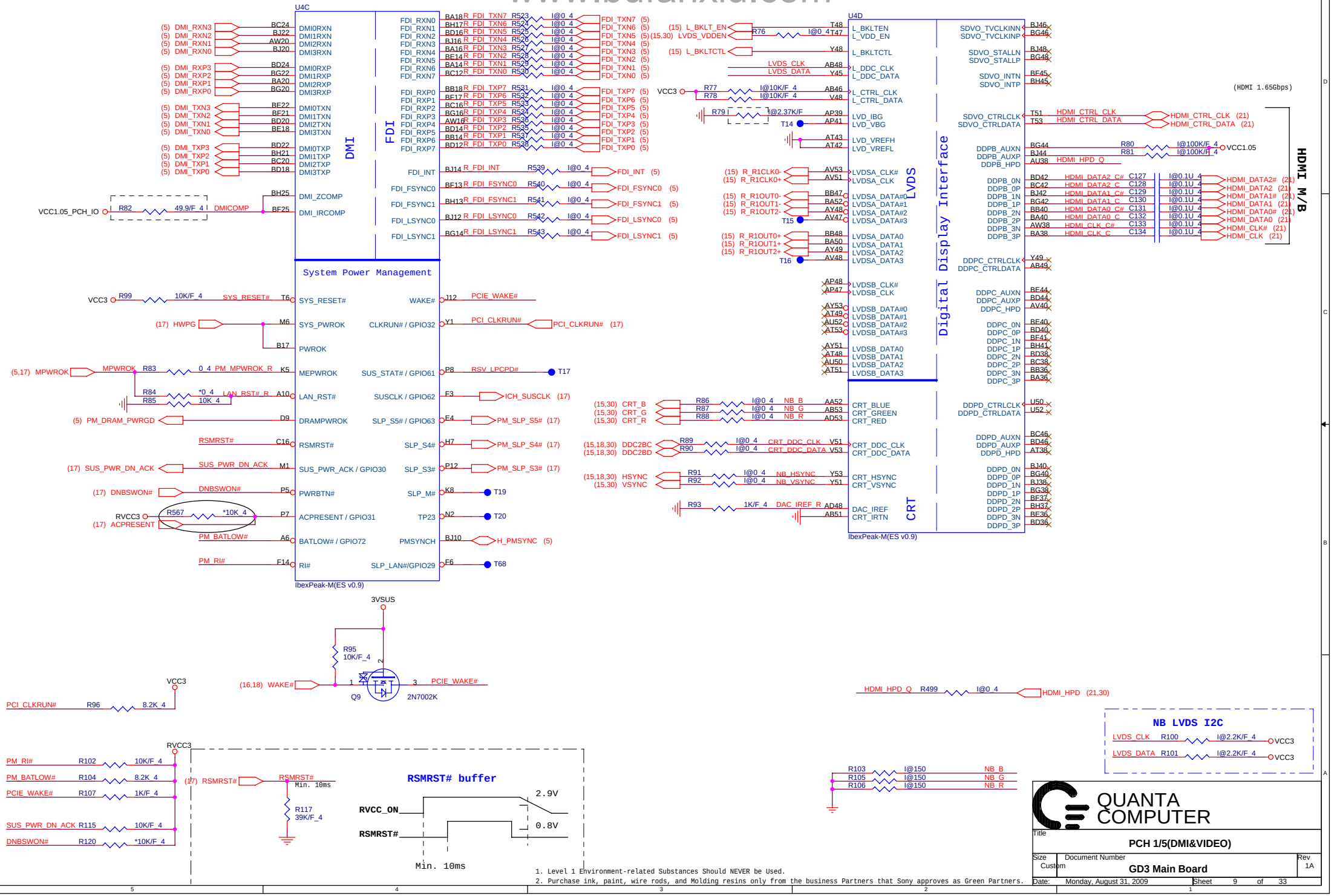
IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (LVDS,DDI)



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QUANTA COMPUTER

Title	PCH 1/5(DMI&VIDEO)
Size: Custom	Document Number: GD3 Main Board
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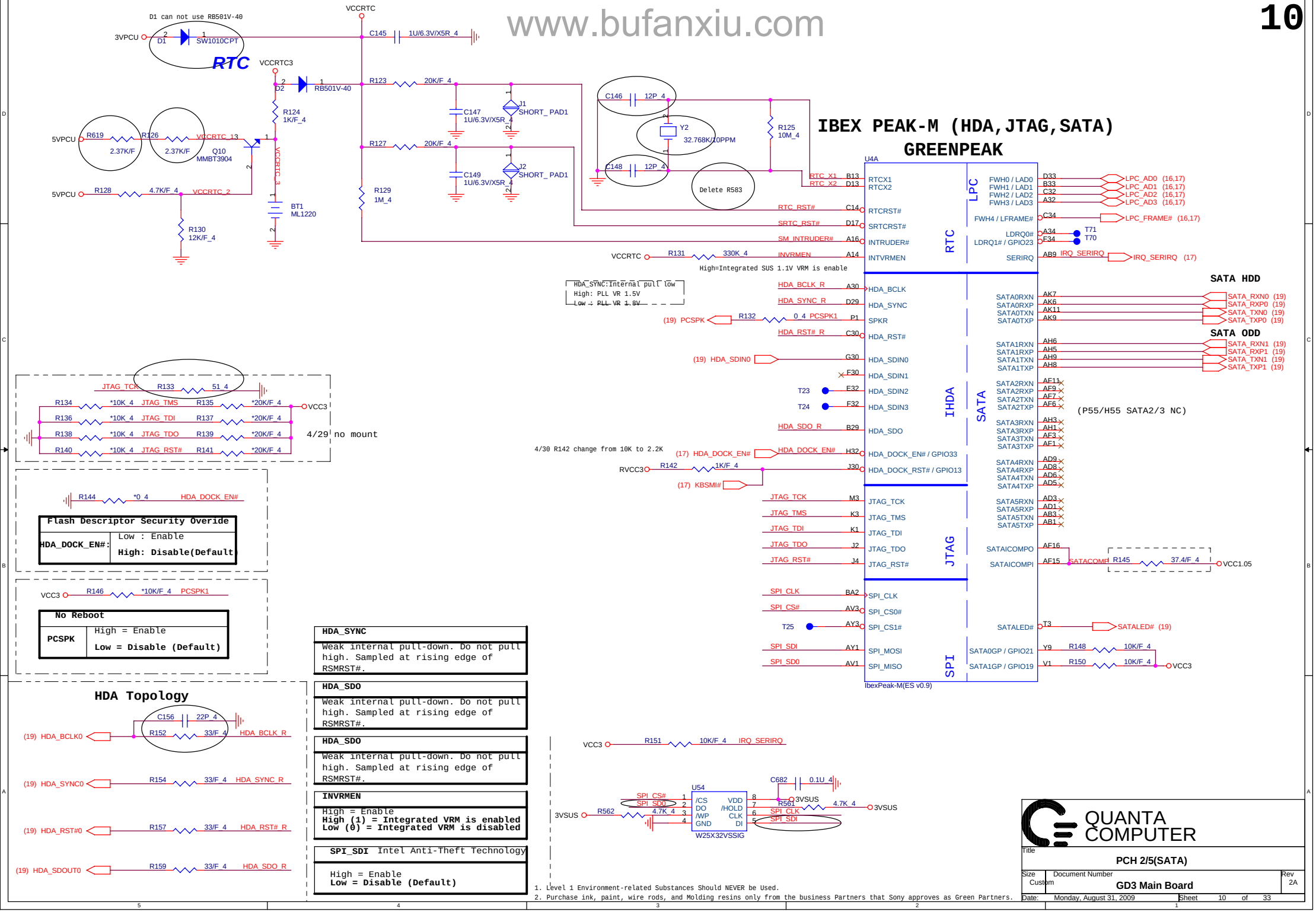
Date: Monday, August 31, 2009	Sheet 9 of 33

IBEX PEAK-M (HDA,JTAG,SATA) GREENPEAK



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	PCH 2/5(SATA)	
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

NV_CLE:DMI termination voltage. Weak internal pull-up. Do not pull low

BT

USB Port0
USB Port1
Docking USB
Express Card
USB Port2

Finger Printer
Camera
WWAN
Felica
WIMAX
BT

GNT2#/GPIO53 :

High : Internal pull-up

Low : Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops)

SM BUS for C0 (CLOCK/DRAM)

PCLK_SMB/PDAT_SMB	Address
SO-DIMM0	1010 000X A0h
SO-DIMM1	1010 010X A4h
ICS9LRS3105	1101 0010 D2h
Express Card	

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 Swap override/Top-Block Swap Override enabled **High = Default**

Anti-Theft Technology

NV_ALE	High = Enable **Low = Disable**

Boot BIOS Strap

GNT0#	GNT#1	Boot BIOS Location
0	0	* **LPC**
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GPIO56

If not used, 8.2-k? to 10-k? pull-up to +V3.3A

QUANTA COMPUTER

Title: PCH 3/5(PCI)

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1. Level 1 Environment-related Substances Should NEVER be Used.
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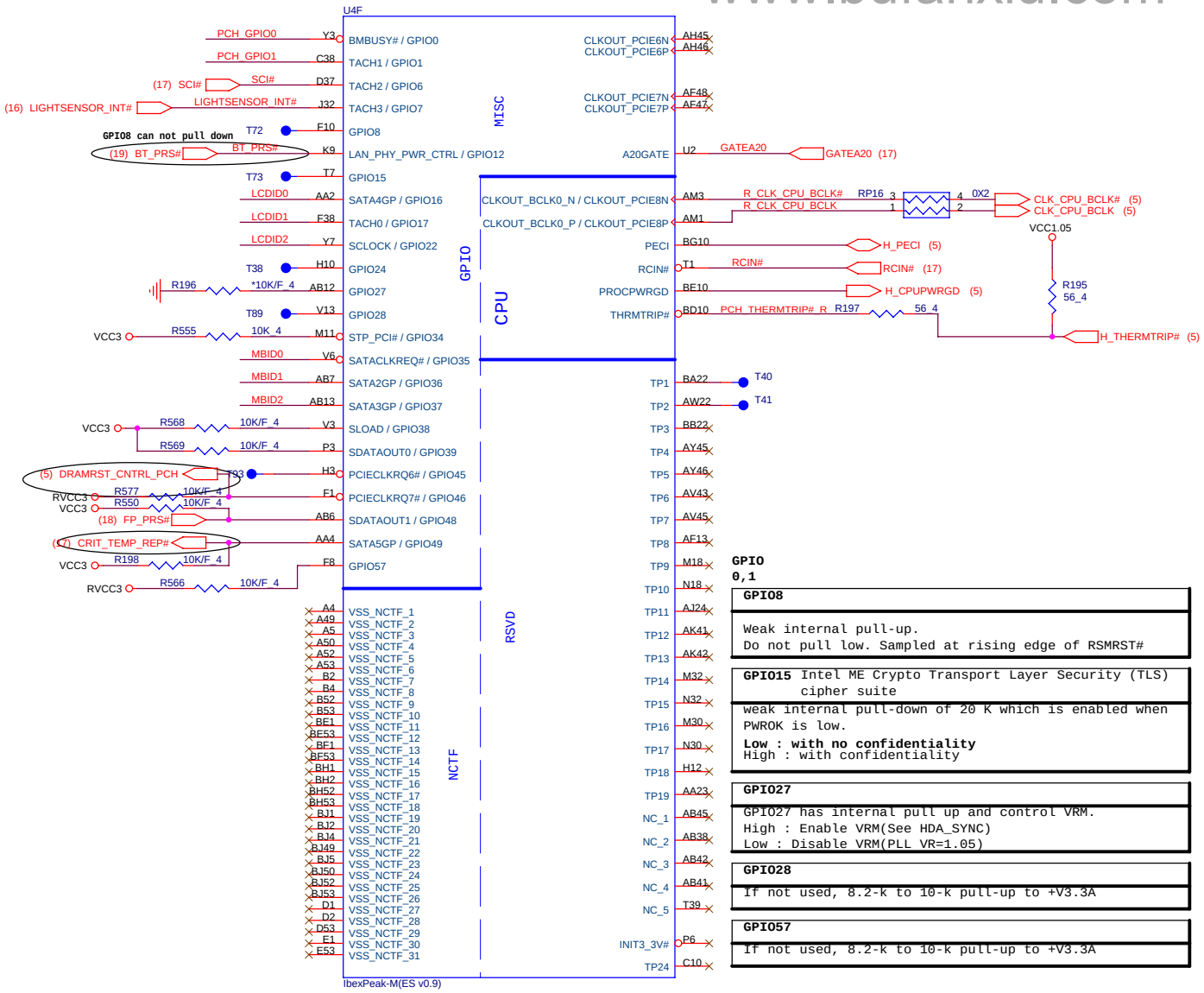
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPIO 0,1

GPIO8

Weak internal pull-up.
Do not pull low. Sampled at rising edge of RSMRST#

GPIO15 Intel ME Crypto Transport Layer Security (TLS) cipher suite

weak internal pull-down of 20 K which is enabled when PWROK is low.

Low : with no confidentiality
High : with confidentiality

GPIO27

GPIO27 has internal pull up and control VRM.
High : Enable VRM(See HDA_SYNC)
Low : Disable VRM(PLL VR=1.05)

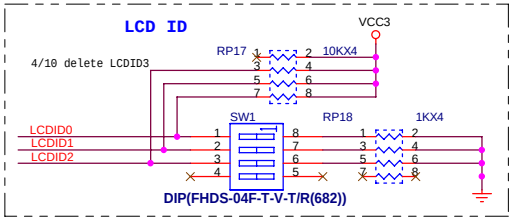
GPIO28

If not used, 8.2-k to 10-k pull-up to +V3.3A

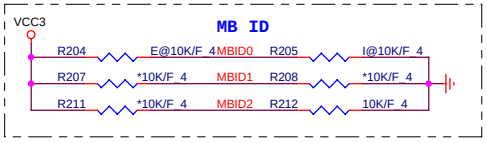
GPIO57

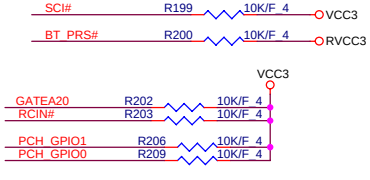
If not used, 8.2-k to 10-k pull-up to +V3.3A

SV_SET_UP	High = Strong (Default)



	MBID0	MBID1	MBID2	QCI P/N
INT. HM57 + SPI rom 8MB	0	0	0	31GD3MB0030
INT. HM55 + SPI rom 4MB	0	0	1	31GD3MB0000
HM55 + SPI rom 4MB(Hynix)	1	0	0	31GD3MB0010
HM55 + SPI rom 4MB(Samsung)	1	0	1	31GD3MB0020





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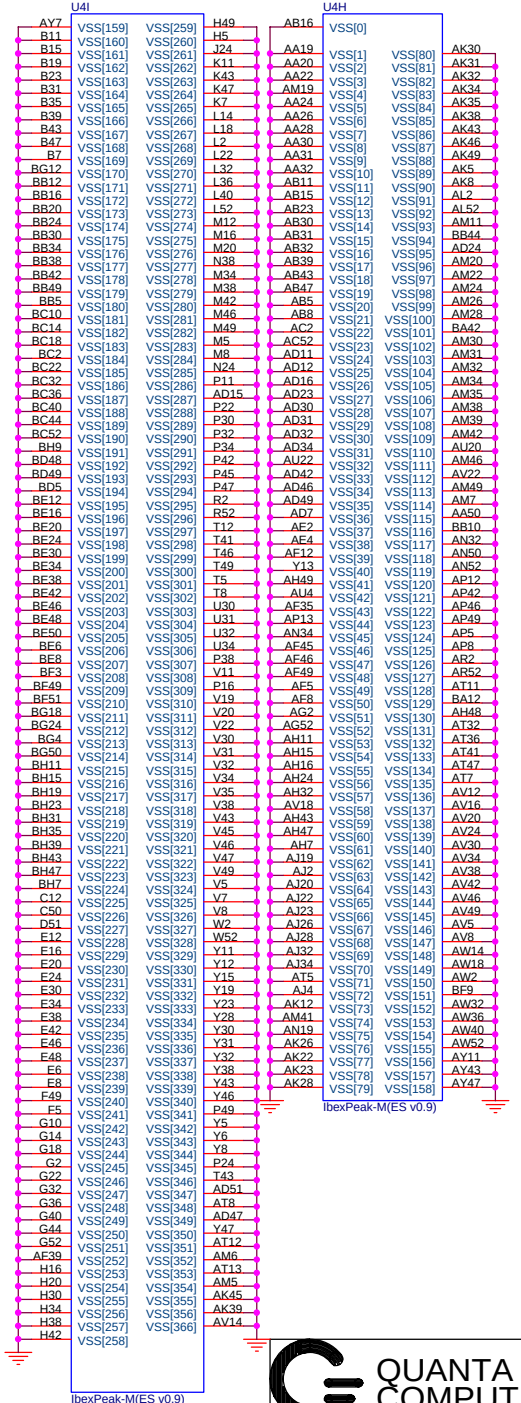

QUANTA COMPUTER

Title	PCH 4/5(GPIO)	
Size: Custom	Document Number: GD3 Main Board	Rev: 1A
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IBEX PEAK-M (POWER)

POWER

U4J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | PCI/GPIO/LPC | CPU | RTC | HDA

C172 *1U/6.3V/X5R_4 PCH_VCCACLK (52mA) AP51 VCCACLK[1]
AP53 VCCACLK[2]
R580 0_4 (320mA) AF23 VCCLAN[1]
AF24 VCCLAN[2]
C181 0.1U_4 Y20 DCPSUSBYP
VCC1.05 (1.849A) AD38 VCCME[1]
C182 22U/6.3V_8 AD39 VCCME[2]
C184 1U/6.3V/X5R_4 AD41 VCCME[3]
Place near AD38,V39
AF43 VCCME[4]
AF41 VCCME[5]
AF42 VCCME[6]
V39 VCCME[7]
V41 VCCME[8]
V42 VCCME[9]
Y39 VCCME[10]
Y41 VCCME[11]
Y42 VCCME[12]
C191 0.1U_4 (1.57V) V9 DCPRTC
C716 220U/2.5V/3528/ESR=15/H1.9
C194 10U/6.3V/X5R_6
C198 1U/6.3V/X5R_4
VCC1.8 (196mA) AU24 VCCVRM[3]
VCC1.05 L6 MLG1608B10NJ(10uH/600mA/0.11) VCC1.05_PCH_VCCADPLLA (68mA) BB51 VCCADPLLA[1] BB53 VCCADPLLA[2]
R219 *0_4
VCC1.05 L7 MLG1608B10NJ(10uH/600mA/0.11) VCC1.05_PCH_VCCADPLLB (69mA) BD51 VCCADPLLB[1] BD53 VCCADPLLB[2]
VCC1.05 AH23 VCCIO[21]
C202 10U/6.3V/X5R_6 AJ35 VCCIO[22]
C203 1U/6.3V/X5R_4 AH35 VCCIO[23]
C717 220U/2.5V/3528/ESR=15/H1.9 AF34 VCCIO[2]
C204 1U/6.3V/X5R_4 AH34 VCCIO[3]
C205 1U/6.3V/X5R_4
C207 1U/6.3V/X5R_4 AF32 VCCIO[4]
C209 0.1U_4 VCC_PCH_DCPSST (1.536V) V12 DCPSST
C212 0.1U_4 VCC_PCH_DCPSUS (1.05V) Y22 DCPSUS
RVCC3 (163mA) P18 VCCSUS3_3[29]
U19 VCCSUS3_3[30]
C215 0.1U_4 U20 VCCSUS3_3[31]
U22 VCCSUS3_3[32]
VCC3 V15 VCC3_3[5]
C217 0.1U_4 V16 VCC3_3[6]
Y16 VCC3_3[7]
VCC1.05 (<1mA) AT18 V_CPU_IO[1]
C219 0.1U_4 AU18 V_CPU_IO[2]
C221 1U/6.3V/X5R_4
VCCRTC (2mA) A12 VCCRTC
C222 0.1U_4
C224 0.1U_4
C225 1U/6.3V/X5R_4

VCCIO[5] V24 VCC1.05
VCCIO[6] V26
VCCIO[7] Y24 C173 1U/6.3V/X5R_4
VCCIO[8] Y26
VCCSUS3_3[1] V28 (163mA) RVCC3
VCCSUS3_3[2] U28
VCCSUS3_3[3] U26
VCCSUS3_3[4] U24 C179 0.1U_4
VCCSUS3_3[5] P28 C180 0.1U_4
VCCSUS3_3[6] P26 C673 0.1U_4
VCCSUS3_3[7] N28 C674 0.1U_4
VCCSUS3_3[8] N26 C675 0.1U_4
VCCSUS3_3[9] M28
VCCSUS3_3[10] M26
VCCSUS3_3[11] L28
VCCSUS3_3[12] L26
VCCSUS3_3[13] J28
VCCSUS3_3[14] J26
VCCSUS3_3[15] H28
VCCSUS3_3[16] H26
VCCSUS3_3[17] G28
VCCSUS3_3[18] G26
VCCSUS3_3[19] F28
VCCSUS3_3[20] F26
VCCSUS3_3[21] E28
VCCSUS3_3[22] E26
VCCSUS3_3[23] C28
VCCSUS3_3[24] C26
VCCSUS3_3[25] B27
VCCSUS3_3[26] A28
VCCSUS3_3[27] A26
VCCSUS3_3[28] U23
VCCIO[56] V23 VCC1.05
V5REF_SUS F24 (<1mA) RVCC5_V5REFSUS C190 1U/6.3V/X5R_4
V5REF K49 (<1mA) VCC5_V5REF C196 0.1U_4 R217 10_4 VCC5
D4 RB501V-40 VCC3
VCC3_3[8] J38
VCC3_3[9] L38
VCC3_3[10] M36 (0.357mA) VCC3
VCC3_3[11] N36 C201 0.1U_4 C676 0.1U_4
VCC3_3[12] P36
VCC3_3[13] U35
VCC3_3[14] AD13 C208 0.1U_4 VCC3
VCCSATAPLL[1] AK3 (31mA) PCH_VCCSATAPLL C210 *1U/6.3V/X5R_4
VCCSATAPLL[2] AK1 (0.78V)
VCCIO[9] AH22 VCC1.05
VCCVRM[4] AT20 (196mA) VCC1.8
VCCIO[10] AH19 VCC1.05
VCCIO[11] AD20
VCCIO[12] AF22
VCCIO[13] AD19
VCCIO[14] AE20 C216 1U/6.3V/X5R_4
VCCIO[15] AF19 C672 0.1U_4
VCCIO[16] AH20
VCCIO[17] AB19
VCCIO[18] AB20
VCCIO[19] AB22
VCCIO[20] AD22
VCCME[13] AA34 VCC1.05
VCCME[14] Y34
VCCME[15] Y35 C220 10U/6.3V/X5R_6
VCCME[16] AA35
VCCSUSHDA L30 (6mA) RVCC3
C223 1U/6.3V/X5R_4

5VPCU R579 10K/F_4 Q46 2N7002K-T1-E3 R578 1M_4 15VPCU
(17,23) RVCC_ON Q52 DTC144EU Q51 2N7002E RVCC5 R216 10_4
Q58 2N7002E R603 100/F_4
D3 RB501V-40 RVCC3
VCC1.05_PCH_IO (3.062A) Delete R215
VCC1.05

U4G

VCC1.05 (1.432A) VCCCORE[1] AB24
VCCCORE[2] AB26
VCCCORE[3] AB28
VCCCORE[4] AD26
VCCCORE[5] AD28
VCCCORE[6] AE26
VCCCORE[7] AE28
VCCCORE[8] AF30
VCCCORE[9] AF31
VCCCORE[10] AH26
VCCCORE[11] AH28
VCCCORE[12] AH30
VCCCORE[13] AH31
VCCCORE[14] AJ30
VCCCORE[15] AJ31
C175 10U/6.3V/X5R_6 C177 0.1U_4
VCC1.05 AK24 VCCIO[24]
(40mA) B24 VCCAPLLEXP
C188 1U/6.3V/X5R_4 PCH_VCCAPLLEXP
AN20 VCCIO[25]
AN22 VCCIO[26]
AN23 VCCIO[27]
AN24 VCCIO[28]
AN26 VCCIO[29]
AN28 VCCIO[30]
BJ26 VCCIO[31]
BJ28 VCCIO[32]
AT26 VCCIO[33]
AT28 VCCIO[34]
AU26 VCCIO[35]
AU28 VCCIO[36]
AV26 VCCIO[37]
AV28 VCCIO[38]
AW26 VCCIO[39]
AW28 VCCIO[40]
BA26 VCCIO[41]
BA28 VCCIO[42]
BB26 VCCIO[43]
BB28 VCCIO[44]
BC26 VCCIO[45]
BC28 VCCIO[46]
BD26 VCCIO[47]
BD28 VCCIO[48]
BE26 VCCIO[49]
BE28 VCCIO[50]
BG26 VCCIO[51]
BG28 VCCIO[52]
BH27 VCCIO[53]
AN30 VCCIO[54]
AN31 VCCIO[55]
C199 10U/6.3V/X5R_6
C192 1U/6.3V/X5R_4
C193 1U/6.3V/X5R_4
C195 1U/6.3V/X5R_4
C197 1U/6.3V/X5R_4
C663 0.1U_4
C664 0.1U_4
VCC3 AN35 VCC3_3[1]
VCC1.8 (196mA) AT22 VCCVRM[1]
C214 1U/6.3V/X5R_4 PCH_VCCFDIPLL BJ18 VCCFDIPLL (37mA)
VCC1.05 AM23 VCCIO[1]

VCCADAC[1] AE50 VCC3_VCCADAC L3 BLM18PG181SN1D (69mA) VCC3
VCCADAC[2] AE52 C174 0.1U_4 C178 10U/6.3V/X5R_6 C754 0.01u_4
VSSA_DAC[1] AE53
VSSA_DAC[2] AE51
VCCALVDS AH38 VCC3_VCCALVDS R214 I@0_4 (<1mA) VCC3
C183 I@0.1U_4/E@0_4
VSSA_LVDS AH39
VCCTX_LVDS[1] AP43 VCC1.8_VCCTX_LVDS L4 I@0.1uH_8 (59mA) VCC1.8
VCCTX_LVDS[2] AP45
VCCTX_LVDS[3] AT46 C185 I@0.01u_4/E@0_4
VCCTX_LVDS[4] AT45 C186 I@0.01u_4
C187 I@10U/6.3V/X5R_6
VCC3_3[2] AB34 VCC3
VCC3_3[3] AB35 C189 0.1U_4
VCC3_3[4] AD35
VCCVRM[2] AT24 (196mA) C690 1U/6.3V/X5R_4 VCC1.8
VCCDMI[1] AT16 (61mA) VCC1.05
VCCDMI[2] AU16 C200 1U/6.3V/X5R_4 Delete R218
VCCPNAND[1] AM16 (156mA) VCC1.8
VCCPNAND[2] AK16
VCCPNAND[3] AK20 Delete R220
VCCPNAND[4] AK19 C206 0.1U_4
VCCPNAND[5] AK15 C671 0.1U_4
VCCPNAND[6] AK13
VCCPNAND[7] AM12
VCCPNAND[8] AM13
VCCPNAND[9] AM15
VCCME3_3[1] AM8 (85mA) VCC3
VCCME3_3[2] AM9
VCCME3_3[3] AP11 C213 0.1U_4
VCCME3_3[4] AP9

VCC CORE | CRT | LVDS | HVCMOS | PCI E* | DMI | SPI | NAND | FDI

IbexPeak-M(ES v0.9)

Enable/Disable internal VRM VCCVRM[1..4].
GPIO27: High : Enable (Internal pull High) VCCACLK[1..2], VCCSATAPLL[1..2], VCCAPLLEXP, VCCFDIPLL can remove
Low : Disable

Straping VCC1.5 or VCC1.8
HDA_SYNC: High : VCC1.5
Low : VCC1.8 (Internal pull Low)

QUANTA COMPUTER

Title: PCH 5/5(POWER)
Size: | Document Number: GD3 Main Board | Rev: 2A
Date: Tuesday, September 01, 2009 | Sheet 13 of 33

(H=8mm)

CON2

PC3-XXXX DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

(H=4mm)

CON1

PC3-XXXX DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1

Place these Caps near So-Dimm1.

VTT_MEM

C226 10U/6.3V/X5R_6
C227 10U/6.3V/X5R_6
C228 10U/6.3V/X5R_6
C229 1U/6.3V/X5R_4
C230 1U/6.3V/X5R_4
C231 1U/6.3V/X5R_4
C232 1U/6.3V/X5R_4

Place these Caps near So-Dimm0.

VTT_MEM

C233 10U/6.3V/X5R_6
C234 10U/6.3V/X5R_6
C235 10U/6.3V/X5R_6
C236 1U/6.3V/X5R_4
C237 1U/6.3V/X5R_4
C238 1U/6.3V/X5R_4
C239 1U/6.3V/X5R_4

1.5VSUS

R227 470/F_4
R232 470/F_4
C240 470P_4

SMVREF_GMCH — SMVREF_GMCH (24)

Delete R228,R230,R231,R233

MBDATA/MBCLK:	Address
WWAN Thermal (G751)	100 1001
DRAM Thermal (G751)	100 1000
HDD G-Sensor	001 1101
Ext.Graphics Thermal (LM89-1)	100 1101
Nvidia Graphics Thermal	1001 1110
PCH SMBUS	
TPA2016D2 Write	1011 0000
TPA2016D2 Read	1011 0001
TAOS TSL2561FN(W52H/R53H)	0101 001X
TAOS TSL2561FN(Alert)	0001 100X
Philips PCA9557	001 1011

MEMORY THRM SENSOR

Thermal I2C

VCC3

(11,17) MBDATA — Q15 2N7002E — R234 10K/F_4 — KBSMDATA (16,19,30)

(11,17) MBCLK — Q16 2N7002E — R235 10K/F_4 — KBSMCLK (16,19,30)

U7 *G751-2P-8F

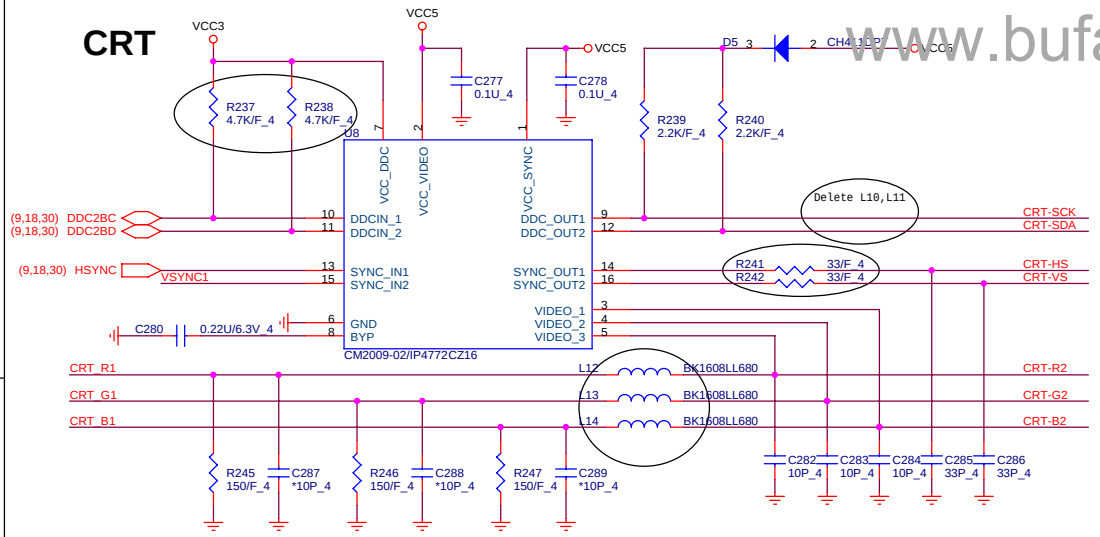
(16,19,30) KBSMDATA — SMBDATA — +Vs
(16,19,30) KBSMCLK — SMBCLK — A0
O.S. — A1
GND — A2

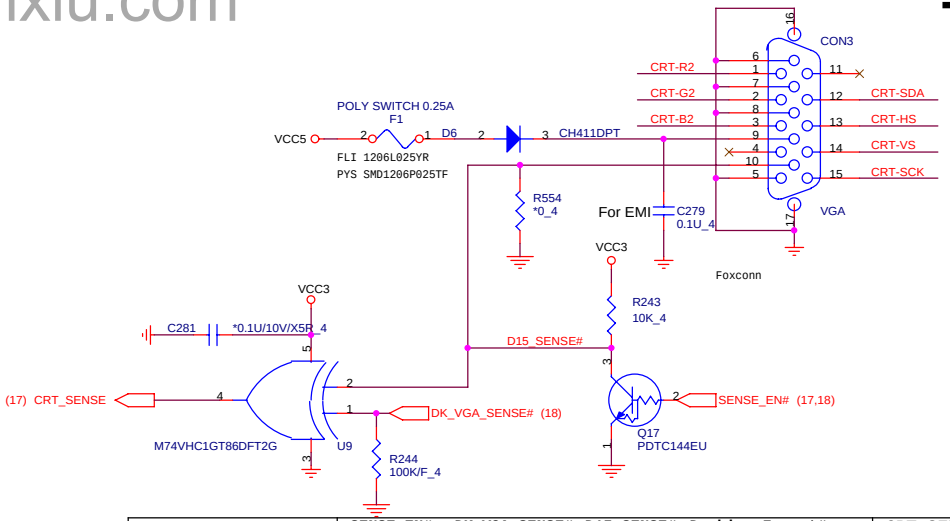
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

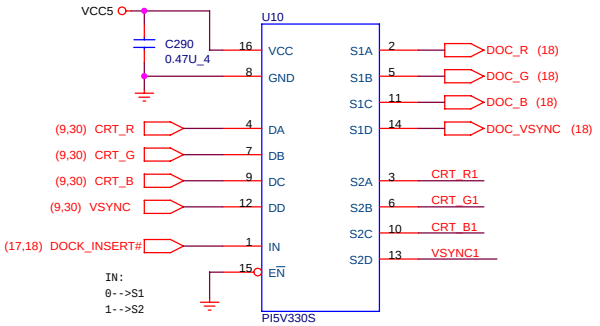
QUANTA COMPUTER

Title	DDR3 DIMM-0	
Size: Custom	Document Number: Main Board	Rev: 2A
Date: Monday, August 31, 2009	Sheet 14 of 33	

CRT



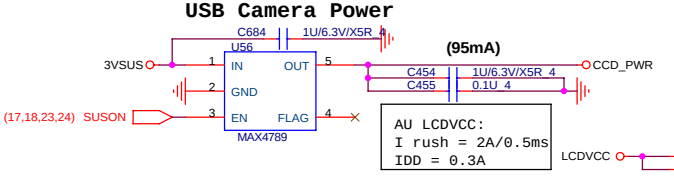




[EC Behavior]
CRT_SENSE: H=>L or L=>H detect which one is inserting
Docking_Insert#: H=>L detect which one is inserting
[CRT SW]
When Docking_Insert# is low switching RGB to Docking CRT
[SENSE_EN#]
Input for CRT pin10, EC assert to high when CRT insert[NEO Request]

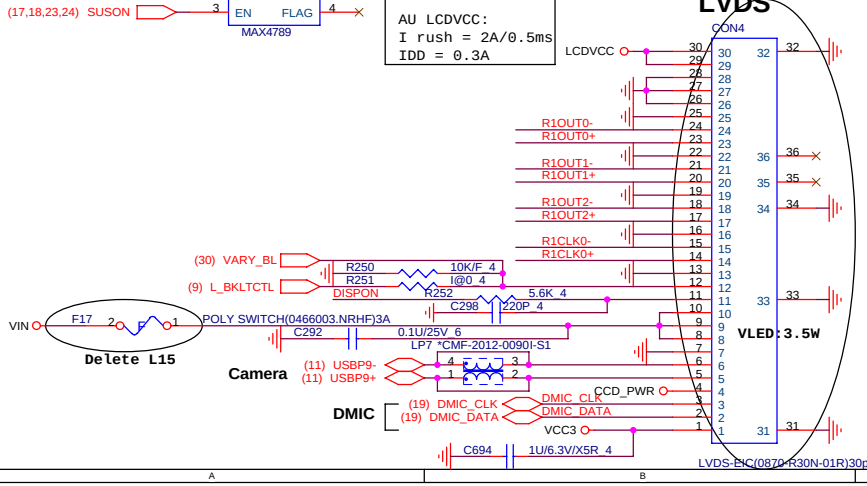
	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	H => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H

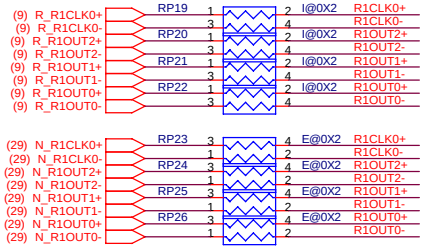
USB Camera Power



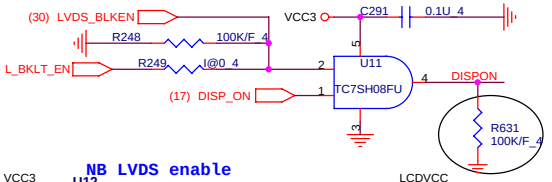
AU LCDVCC:
I rush = 2A/0.5ms
IDD = 0.3A

LVDS

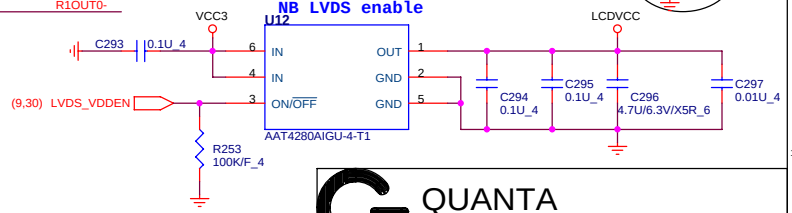




Display On



NB LVDS enable



1.Level 1 Environment-related Substances Should NEVER be Used.
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QUANTA COMPUTER

Title	CRT/LVDS	
Size: Custom	Document Number: Main Board	Rev: 1A
Date: Thursday, September 03, 2009	Sheet 15 of 33	

LAN Board BTB

WLAN PCIE

LAN PCIE

Express Card

CON38

(11) PCIE_TXP1
(11) PCIE_TXN1
(11) PCIE_RXP1
(11) PCIE_RXN1
(11) CLK_PCIE_WLAN
(11) CLK_PCIE_WLAN#
(11) PCIE_TXP3
(11) PCIE_TXN3
(11) PCIE_RXP3
(11) PCIE_RXN3
(11) CLK_PCIE_LAN
(11) CLK_PCIE_LAN#
(11) PCIE_RXN5
(11) PCIE_RXP5
(11) PCIE_TXN5
(11) PCIE_TXP5

USBP10+ (11)
USBP10- (11)
USBP12+ (11)
USBP12- (11)
USBP0+
USBP0-
USBP0+ (11)
USBP0- (11)
USBP1+
USBP1-
USBP1+ (11)
USBP1- (11)
USBP3- (11)
USBP3+ (11)
KBSMDATA (14,19,30)
KBSMCLK (14,19,30)
PRS#0 (17)
PRS#1 (17)
PRS#2 (17)
CLK_PCIE_EXPRESS_CARD (11)
CLK_PCIE_EXPRESS_CARD# (11)
USBOC1# (11)
PCLK_MP (11)
RF_LED# (19)
WWAN_EN (17)
WWAN_USB (17)
PLTRST# (5,11,29,33)
USBOC0#
USBOC0# (11)
PCIE_REQ_LAN# (11)
LPC_AD0 (10,17)
LPC_AD1 (10,17)
LPC_AD2 (10,17)
LPC_AD3 (10,17)
SLEEPLED#
PWRLED#
SLEEPLED# (17)
PWRLED# (17)
NBSWON#
NBSWON# (17)
SCROLED
CAPSLED
NUMLED
SCROLED (17)
CAPSLED (17)
NUMLED (17)
PCIE_REQ_EXPRESSCARD# (11)

(17) WLAN_RF_ON#
(10,17) LPC_FRAME#

3VSUS F13 (1.2A) POLY SWITCH(1206L110WR)1.1A
5VSUS F9 POLY SWITCH 2.6A (3A)
VCC3 (3A)
C695 10U/6.3V/X5R_6
C704 10U/6.3V/X5R_6
C701 10U/6.3V/X5R_6
C702 10U/6.3V/X5R_6
5VPCU
3VPCU

Debug Port

WWAN(AXK5S00037YG)

M/B to Function Board

(FFC Type)

FLI 1206L025YR
PYS SMD1206P025TF
POLY SWITCH 0.25A
F7 (0.6mA)
VCC3
VCC3_LIGHTSENSOR
C689 10U/6.3V/X5R_6
CON34
Function

(17) B1#
(17) B2#
(17) B3#
R548 1K/F_4
R549 1K/F_4
R556 1K/F_4
VCC3
3VPCU
R547 10K_4
R546 10K_4
VCC3
R618 *10K_4
VCC3
R557 10K_4

(14,19,30) KBSMDATA
(14,19,30) KBSMCLK
(12) LIGHTSENSOR_INT#

KBSMDATA C713 *10P_4
KBSMCLK C714 *10P_4

Q50 PDTC144EU
Q49 PDTC144EU
RF_LED#
WWAN_EN
BT_LED (19)

4/27 : Add Q50 for WWAN LED

Delete F10
VCC1.5
C703 10U/6.3V/X5R_6 (1.3A)
3VWAN
C709 10U/6.3V/X5R_6 (2.75A)
RVCC3_AUX
C696 10U/6.3V/X5R_6 (1A)
C697 10U/6.3V/X5R_6
CON46
WWAN(C17448-114A8-L)

WWAN Power

(2.75A Peak, 1.5A normal)

5VPCU
15VPCU
RVCC3
Q62 NTMFS4921
3VWAN
R590 10K/F_4
R610 470K_4
WWAN3V
R611 100/F_4
(17) WWAN_USB
Q54 PDTC144EU
Q63 2N7002E
C737 *0.01U_4
Q64 2N7002E

WLAN Power

(1A Peak, 0.75A normal)

5VPCU
15VPCU
RVCC3
Q59 NTMFS4921
RVCC3_AUX
R593 10K/F_4
R608 470K_4
WLAN3V
R609 100/F_4
(17) WLAN_PWEN
Q56 PDTC144EU
Q60 2N7002E
C736 *0.01U_4
Q61 2N7002E

QUANTA COMPUTER

Title	LAN Board/ Function Board	
Size	Document Number: Main Board	Rev 1A
Date: Thursday, September 03, 2009	Sheet 16 of 33	

I/O Address

	BADDR1-0	Index	Data
*	1 0	2E	2F
	1 1	4E	4F
	0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
	0 1	XOR-TREE TEST	

SHMB: SHBM(If = 0 Enable share host BIOS memory)
DOCK_RST# : BADDR0
T?: BADDR1

U18 WPC775L

LPC: LAD0 LAD1 LAD2 LAD3 LRESET# LCLK LFRAME# SERIRQ SMI#/GPIO65 ECSCI#/GPIO54 KBRST# GPIO67/PWUREQ#
A/D: AD0/GPI90 AD1/GPI91 AD2/GPI92 AD3/GPI93 AD5/GPIO04 AD4/GPIO05
D/A: DA0/GPI94 DA1/GPI95 DA2/GPI96 DA3/GPI97
PWM: A_PWM0/GPIO15 B_PWM/GPIO21 C_PWM/GPIO13 D_PWM/GPIO32 H_PWM/GPIO33 G_PWM/GPIO66 E_PWM/GPIO45 F_PWM/GPIO40 GPIO06 GPIO30 GPIO16 SCL3/GPIO23 SDA3/GPIO31
SPI: F_SDI F_SD0 F_SCK F_CS0#
K/B: KBSIN0..KBSIN7 KBSOUT0/JENK# KBSOUT1/TCK KBSOUT2/TMS KBSOUT3/TDI KBSOUT4/JENO# KBSOUT5/TDO KBSOUT6/RDY# KBSOUT7..KBSOUT15/GPIO61/XOR_OUT KBSOUT16/GPIO60
GPIO: AD7/GPIO07 LPCPD#/GPIO10 CLKRUN#/GPIO11 SCL1/GPIO17 SDA1/GPIO22 GPIO24/HGPIO01 GPIO34 GPIO36 TA1/GPIO56 TCK/GPIO42 TMS/GPIO43 GPIO41 TDI/GPIO44 TRST#/GPIO46 SCL4/GPIO47 TA3/GPIO51 TDO/GPIO50 RDY#/GPIO52 SDA4/GPIO53 KBSOUT17/GPIO57 GPIO70 GPIO71 GPIO72 GPIO82/TRIS# SOUT_CR/GPIO83/BADDR1 GPIO84/BADDR0 SIN_CR/GPIO87 SPI_DI/GPIO77 SPI_DO/GPIO76/SHBM SPI_CLK/GPIO75 GPIO81 GPIO74/SDA2 GPIO73/SCL2 VREF VCC_POR# VCORF
PS/2: PSDAT3/GPIO12 PSCLK3/GPIO25 PSDAT2/GPIO27 PSCLK2/GPIO26 PSDAT1/GPIO35 PSCLK1/GPIO37
TA2/GPIO20 CLKOUT/GPIO55 TB1/GPIO14 TB2/GPIO01 AD6/GPIO03
32KX1/32KCLKIN 32KX2

VCC_POR# RESET: R324 4.7K_4 3VPCU; C361 0.1U_4
Y5 32.768K/10PPM; C363 15P_4; C364 15P_4; R322 20M_4; R323 33K_4; R617 *100K_4; R558 *0_4; (9) ICH_SUSCLK

Winbond W25Q16BVSSIG 2MB
U23 W25Q16BVSSIG: /CS DO /WP GND VDD /HOLD CLK DI
F_CS0# F_SDI F_SCK F_SD0; C366 0.1U_4; R623 100K/F_4

U63 PCA9557PW: VDD SCL SDA A0 A1 A2 GND OD_I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 RESET
MBCLK MBDATA; R595 10K/F_4; R596 10K/F_4; R632 10K/F_4; R594 10K/F_4
DRAMRST_CNTRL (5) PRS#0 (16) PRS#1 (16) PRS#2 (16) NUMLED (16) CAPSLED (16) SCROLED (16) SENSE_EN# (15,18)

U22 G923-330: VIN VOUT SHDN GND SET
5VPCU 3VPCU; C359 1U/6.3V/X5R_4; C360 10U/6.3V/X5R_6; C362 0.1U/10V/X5R_4; R321 *10K/F_4
(73) 5V_RESET#; (300mA)
4/29 add R576

U19 NC7SZ58; U20 NC7SZ04P5X; U21 TC7SH08FU
R306 0_4 ISENS_DOCK (18); C356 *0.01u_4; R626 0_4 MPWROK; R627 0_4; R563 10K/F_4; R625 100K/F_4
D56 *RB501V-40 HWPG; D57 *RB501V-40 MPWROK; D58 RB501V-40 RSMRST#
PM_SYS_PWRGD; (9) HWPG; C358 0.1U_4; R309 10K/F_4 VCC5; C357 0.22U/10V/X5R_4; R308 1M_4; R304 15K/F_4
D11 can not use SW1010CPT
(23,28) LS_PGOOD D9 RB501V-40; (25,28) 8743_PWRGD D10 RB501V-40; (23) PM_SYS_PWRGD D11 SW1010CPT; (24) DDR_PWRGD D12 RB501V-40; (26) EXT_INT_VGA_PWRGD D13 RB501V-40

Q22 PDTA124EU; NBSWON#; ACIN D18 RB501V-40 HOLD#; PM_SLP_S3# D19 RB501V-40; Q65 PDTA124EU; R314 100K/F_4; B2#

(S3~G3 support : Q65 ,R546 mount,R618 no mount)
(S0 suppoert : Q65 ,R546 mount,R618 mount)

If ODD support MD,Need Mount R615
R615 0_4 AZ_GPIO0; ODD_MD# (19); D17 RB501V-40 DNBSWON# (9)

DOCK_INSERT# DOCK_PWRON DOCK_PWROK 150ms DOCK_RST#

INT/EXT# R500 39K/F_4; PM_SLP_S4# R315 39K/F_4; VRON R317 39K/F_4; PM_SLP_S3# R318 39K/F_4; AZ_GPIO0 R319 4.7K_4; PM_SLP_S5# R576 39K/F_4; ODD_EJECT R604 100K_4
5/10 AddR604

TBCLK R300 4.7K_4; TBDATA R301 4.7K_4; R302 3.3K_4 MBCLK; R303 3.3K_4 MBDATA; R571 3.3K_4 MBCLK_BAT; R572 3.3K_4 MBDATA_BAT

MBATV C345 10U/6.3V/X5R_6; C346 0.1U_4; C349 0.1U_4; C352 0.1U_4; C353 0.1U_4; C354 0.1U_4; C355 0.1U_4; MNB-201209-000 L16; C350 10U/6.3V/X5R_6; C351 0.1U_4
ISENS_IN C347 0.01U_4

R307 10K/F_4; R313 4.7K_4; R620 2.2K/F_4
(12) GATEA20 D14 RB501V-40; (10) KBSMI# D15 RB501V-40; (12) SCI# D59 RB501V-40; (12) RCIN# D16 RB501V-40; (9) RSMRST#
(10) IRQ_SERIRQ; (11) PCLK_EC; (10,16) LPC_FRAME#; (10,16) LPC_AD0..AD3
F_SDI F_SD0 F_SCK F_CS0#
R316 10K/F_4; (16) B1# (16) B2# (13,23) RVCC_ON; (19) LID#; (18) TBDATA TBCLK
(18) DOCK_EJECT (18) DOCK_PWRON (16) B3# HOLD# (27) ACIN

(5,9) MPWROK; PM_SLP_S4# (9); MBATV (27); ISENS_IN (27); BAT_PRS# (27); VFAN (20); HDD_INTERRUPT (19); CRIT_TEMP_REP# (12); I_SET (27); WLAN_PWEN (16); KB_BACKLIGHT (20); DOCK_INSERT# (15,18); ACPRESENT (9); DISP_ON (15); SLEEPLED# (16); BATLED1 (19); PWRLED# (16); MAINON (23,25,26,27,28); ODD_EJECT (19); ODD_PWEN (19); MBCLK (11,14); MBDATA (11,14); DOCK_RST# (18); DOCK_INUSE# (18); PCI_CLKRUN# (9); MBCLK_BAT (27); MBDATA_BAT (27); FAN-SIG (20); DOCK_PWROK (18); NBSWON# (16); BATT_RST# (18); HDA_DOCK_EN# (10); SUSON (15,18,23,24); SUS_PWR_DN_ACK (9); PM_SLP_S3# (9); PM_SLP_S5# (9); VRON (22); CRT_SENSE (15); WWAN_USB (16); WIRELESS_SW# (19); WWAN_EN (16); VOL_MUTE (19); CHGEN# (27); INT/EXT# (27); WLAN_RF_ON# (16); BT_PEN# (19); DC/-C (27); HDD_UNLOAD (19); 35001_SDA (18); 35001_SCK (18); R320 10K/F_4; R612 0_4; C365 1U/6.3V/X5R_4; R558 *0_4

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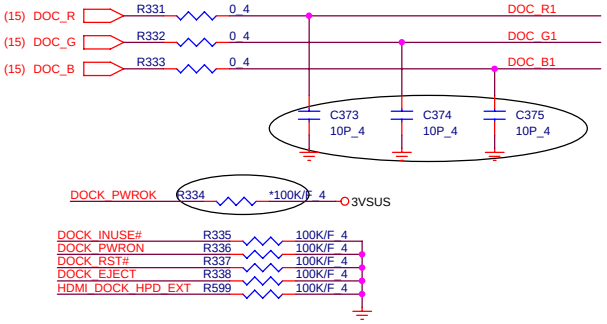
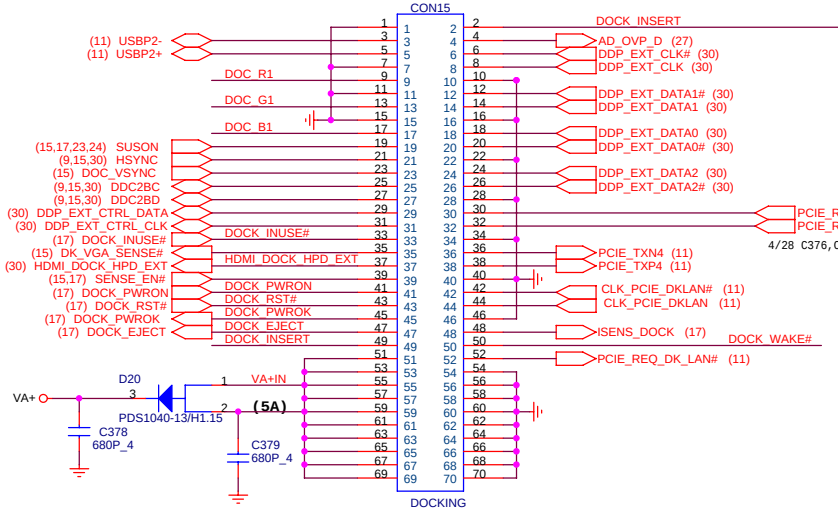
4/18 change BIOS to 2MB 2MBYTE W25X16AVSSIG AKE38ZP0N01

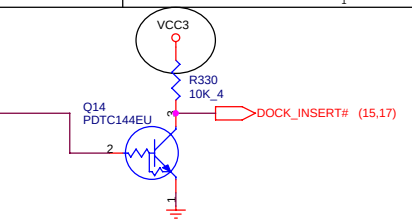
QUANTA COMPUTER

Title	WPCE775L & FLASH	
Size	Document Number: Main Board	Rev: 2A
Date: Wednesday, September 02, 2009	Sheet 17 of 33	

Docking

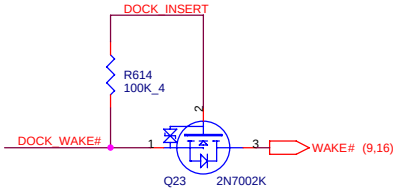




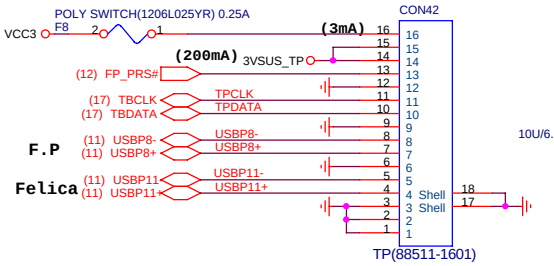


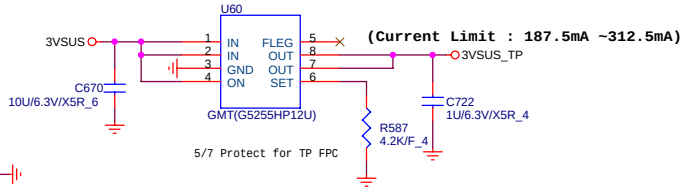
DOCK_INSERT#:
1 No Docking station insert
0: Docking station insert

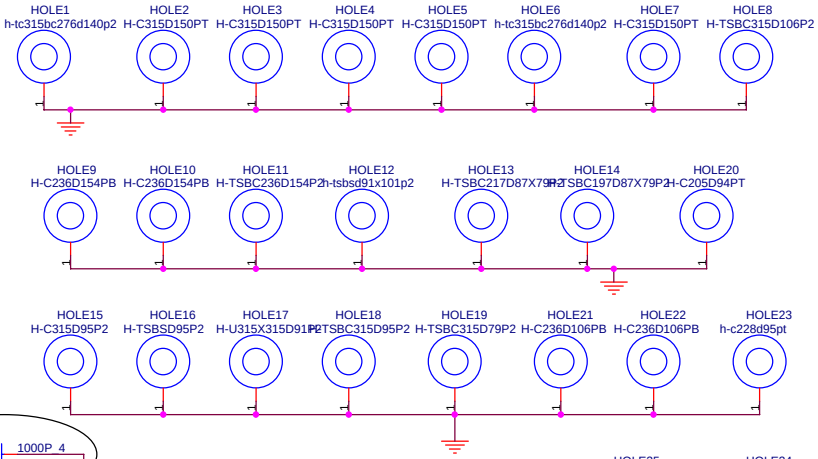
4/28 C376,C377 delete



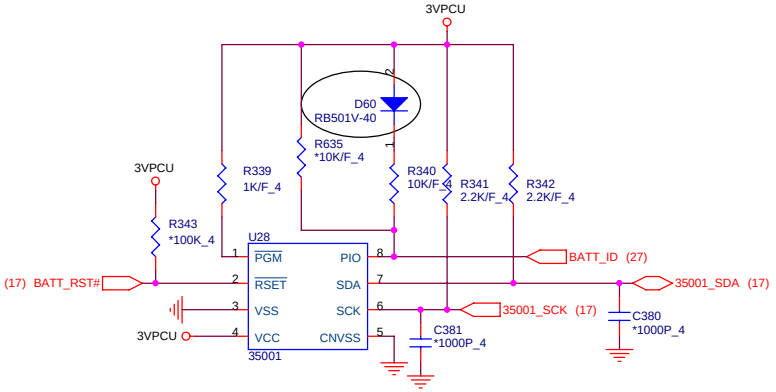
T/P to M/B (FPC)



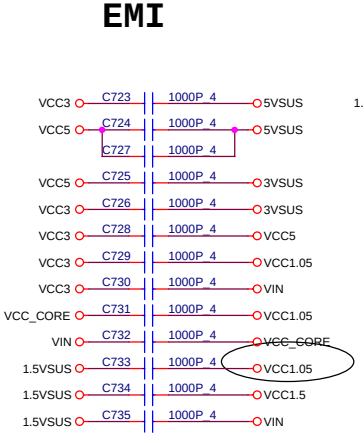


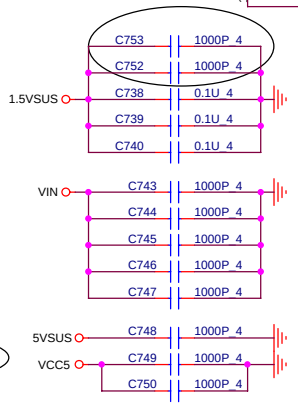


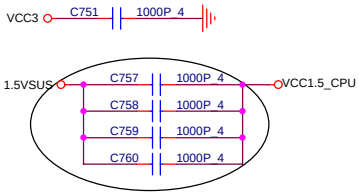
35001



EMI







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QUANTA COMPUTER

Title	Docking/TPM/35001	
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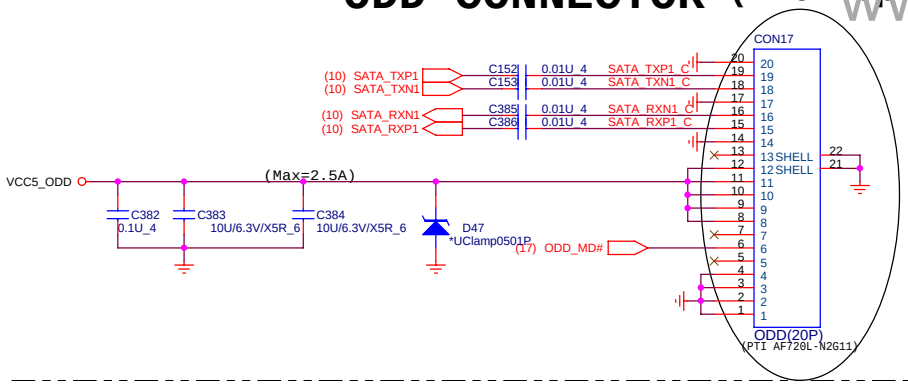
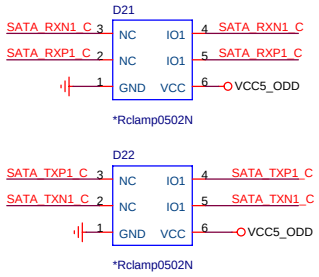
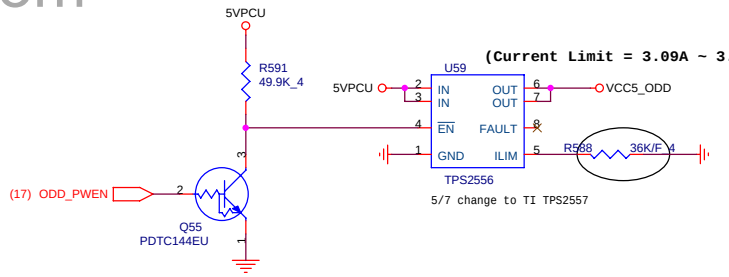
ODD CONNECTOR (FPC 20pin)

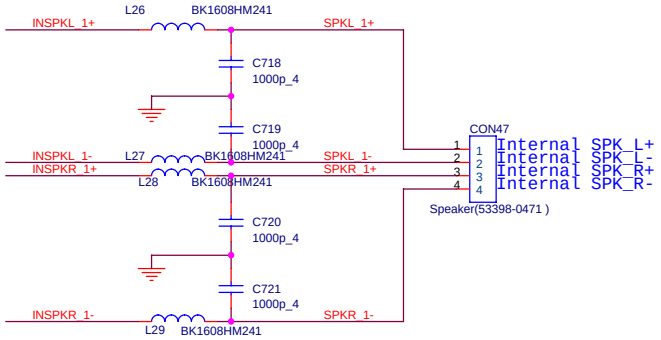




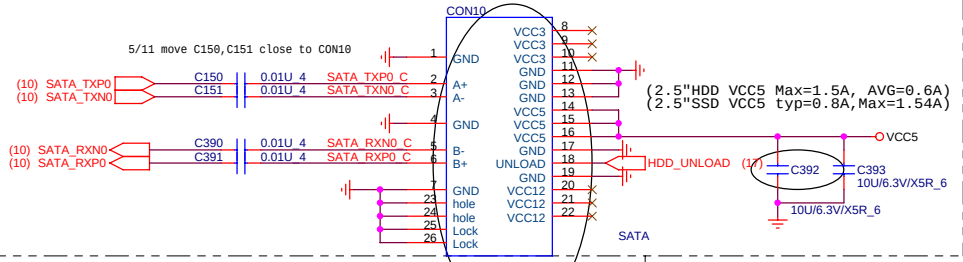


5/1 Delete Q27,R346,Q25,R344,Q26,Q24; Add U59

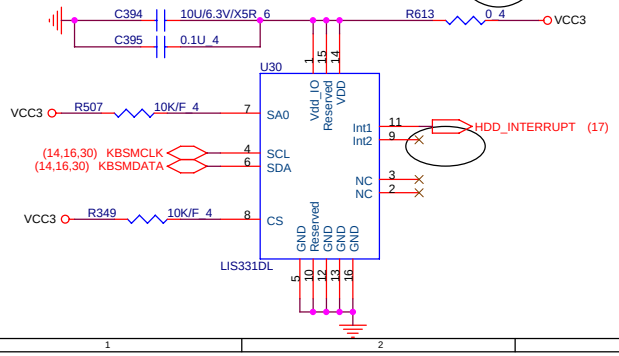
SPEAKER CONNECTOR



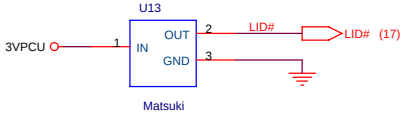
HDD CONNECTOR



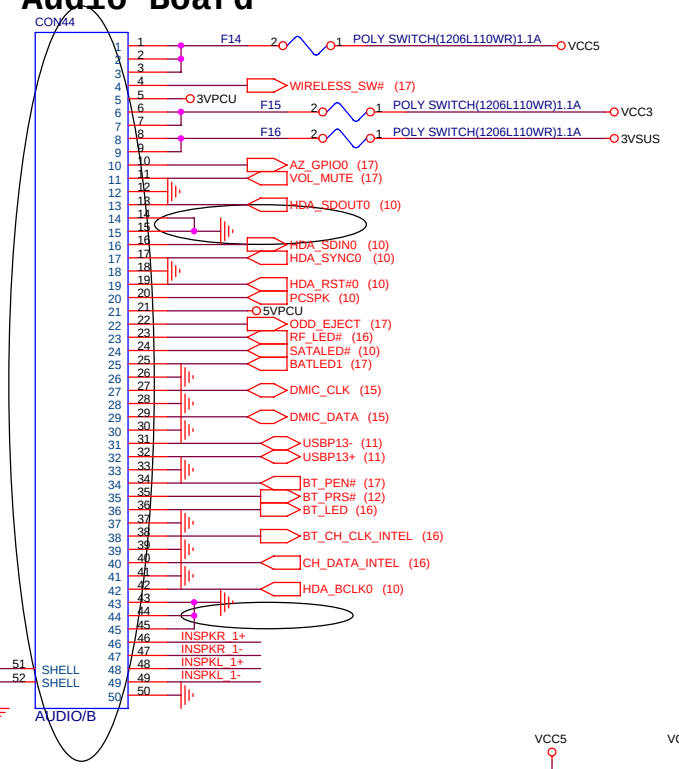
HDD PROTECT

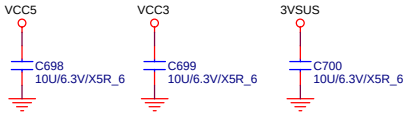


Magnetic Lid Switch



Audio Board





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QUANTA COMPUTER

Title	HDD/ODD/SSD	
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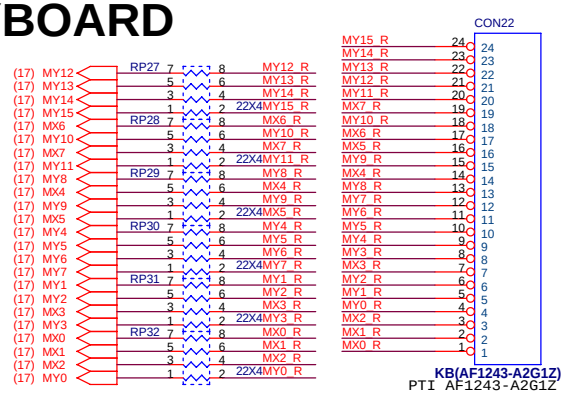
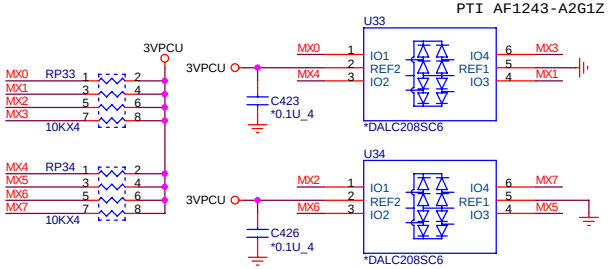
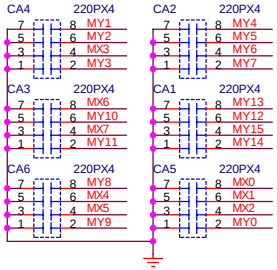
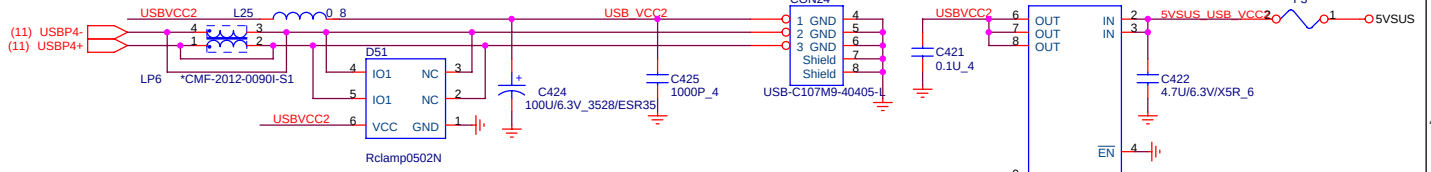
KEYBOARD

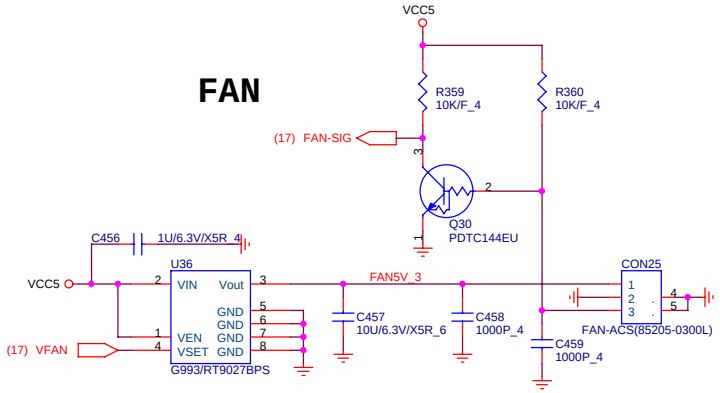




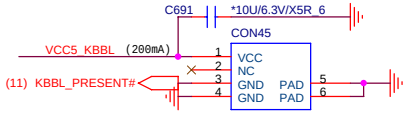


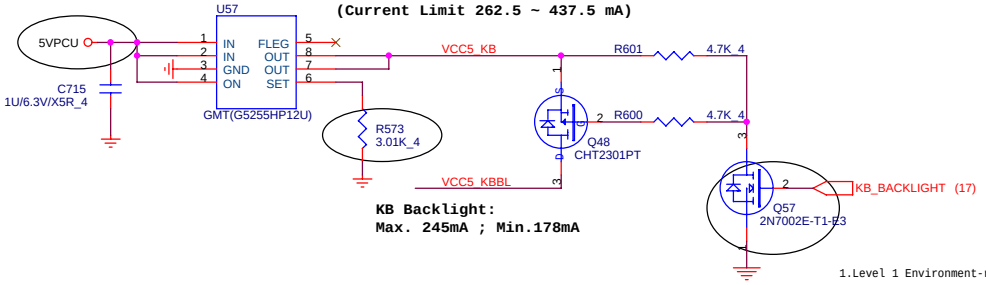


FAN



KB BACKLIGHT





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QUANTA COMPUTER

Title	KB/USB/FAN	
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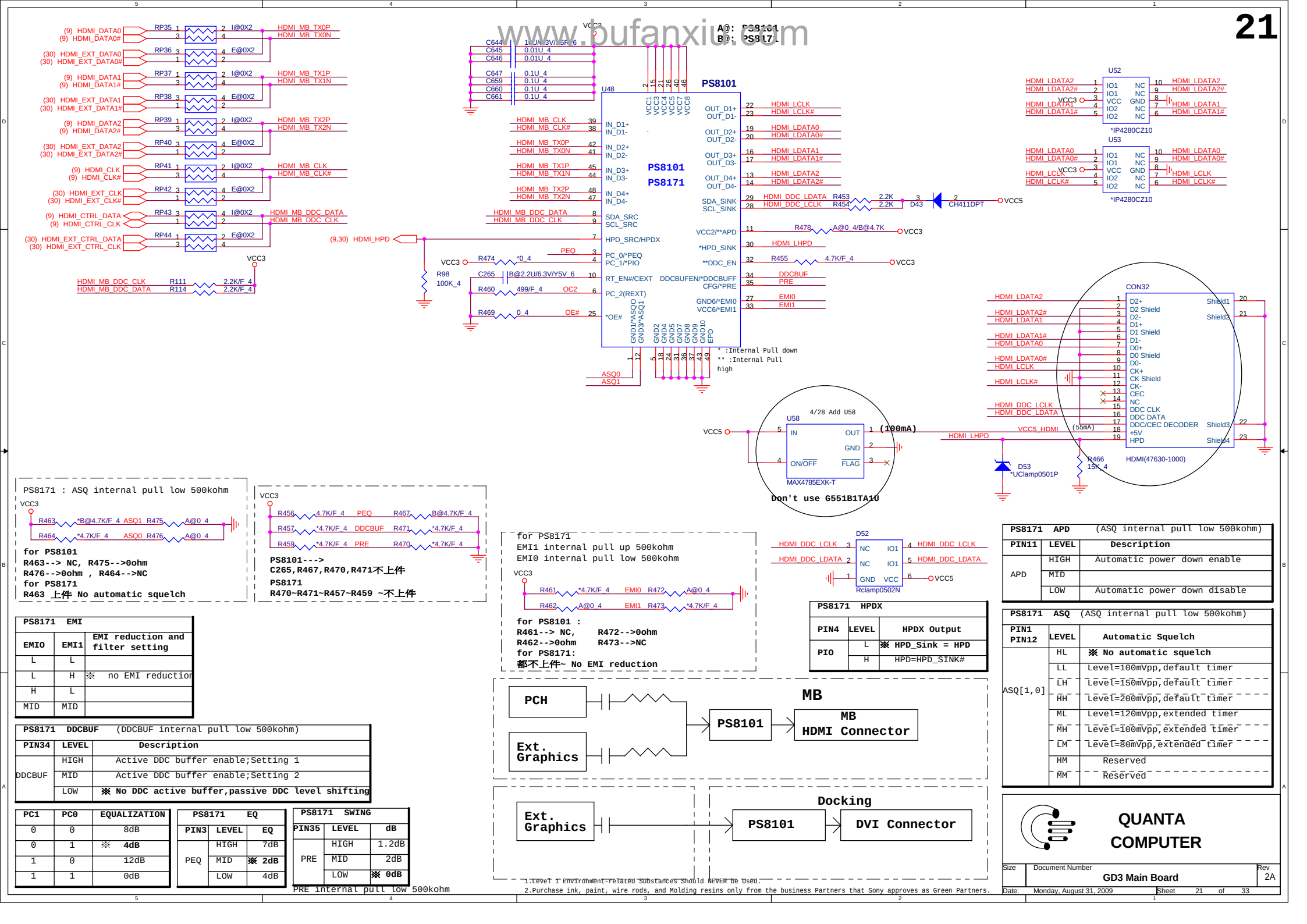

PS8171 : ASQ internal pull low 500kohm

for PS8101
R463--> NC, R475-->0ohm
R476-->0ohm , R464-->NC
for PS8171
R463 上件 No automatic squelch

PS8101--->
C265,R467,R470,R471不上件
PS8171
R470~R471~R457~R459 ~不上件

for PS8171
EMI1 internal pull up 500kohm
EMI0 internal pull low 500kohm

for PS8101 :
R461--> NC, R472-->0ohm
R462-->0ohm R473-->NC
for PS8171:
都不上件~ No EMI reduction

PS8171 EMI		
EMIO	EMI1	EMI reduction and filter setting
L	L	
L	H	※ no EMI reduction
H	L	
MID	MID	

PS8171 DDCBUF (DDCBUF internal pull low 500kohm)		
PIN34	LEVEL	Description
DDCBUF	HIGH	Active DDC buffer enable;Setting 1
	MID	Active DDC buffer enable;Setting 2
	LOW	**※ No DDC active buffer,passive DDC level shifting**

PC1	PC0	EQUALIZATION
0	0	8dB
0	1	※ **4dB**
1	0	12dB
1	1	0dB

PS8171 EQ		
PIN3	LEVEL	EQ
PEQ	HIGH	7dB
	MID	**※ 2dB**
	LOW	4dB

PS8171 SWING		
PIN35	LEVEL	dB
PRE	HIGH	1.2dB
	MID	2dB
	LOW	**※ 0dB**

PRE internal pull low 500kohm

PS8171 HPDX		
PIN4	LEVEL	HPDX Output
PIO	L	**※ HPD_Sink = HPD**
	H	HPD=HPD_SINK#

PS8171 APD (ASQ internal pull low 500kohm)		
PIN11	LEVEL	Description
APD	HIGH	Automatic power down enable
	MID	
	LOW	Automatic power down disable

PS8171 ASQ (ASQ internal pull low 500kohm)		
PIN1 PIN12	LEVEL	Automatic Squelch
ASQ[1,0]	HL	**※ No automatic squelch**
	LL	Level=100mVpp,default timer
	LH	Level=150mVpp,default timer
	HH	Level=200mVpp,default timer
	ML	Level=120mVpp,extended timer
	MH	Level=100mVpp,extended timer
	LM	Level=80mVpp,extended timer
	HM	Reserved
	MM	Reserved

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QUANTA COMPUTER

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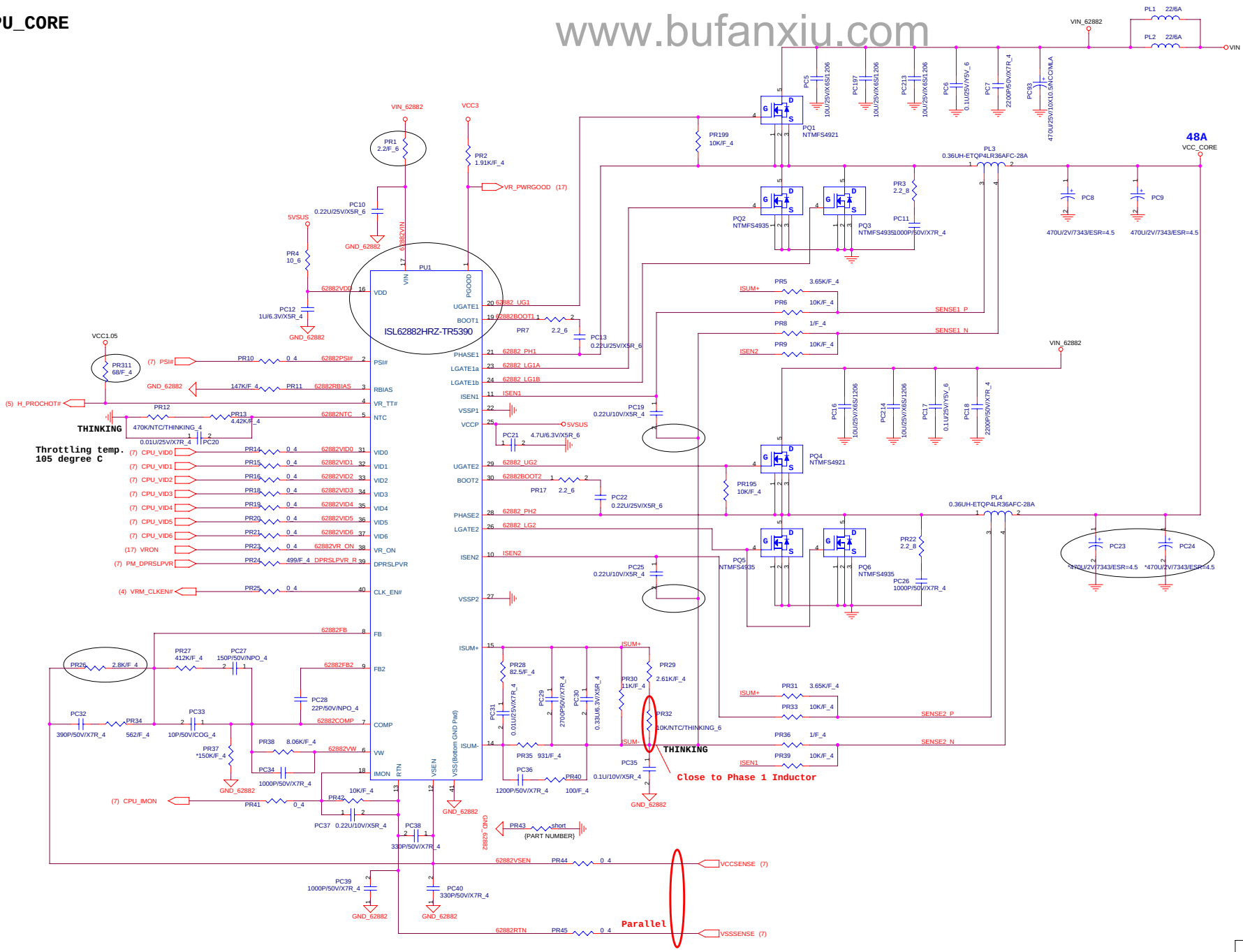

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QUANTA COMPUTER

Size	Document Number	Rev
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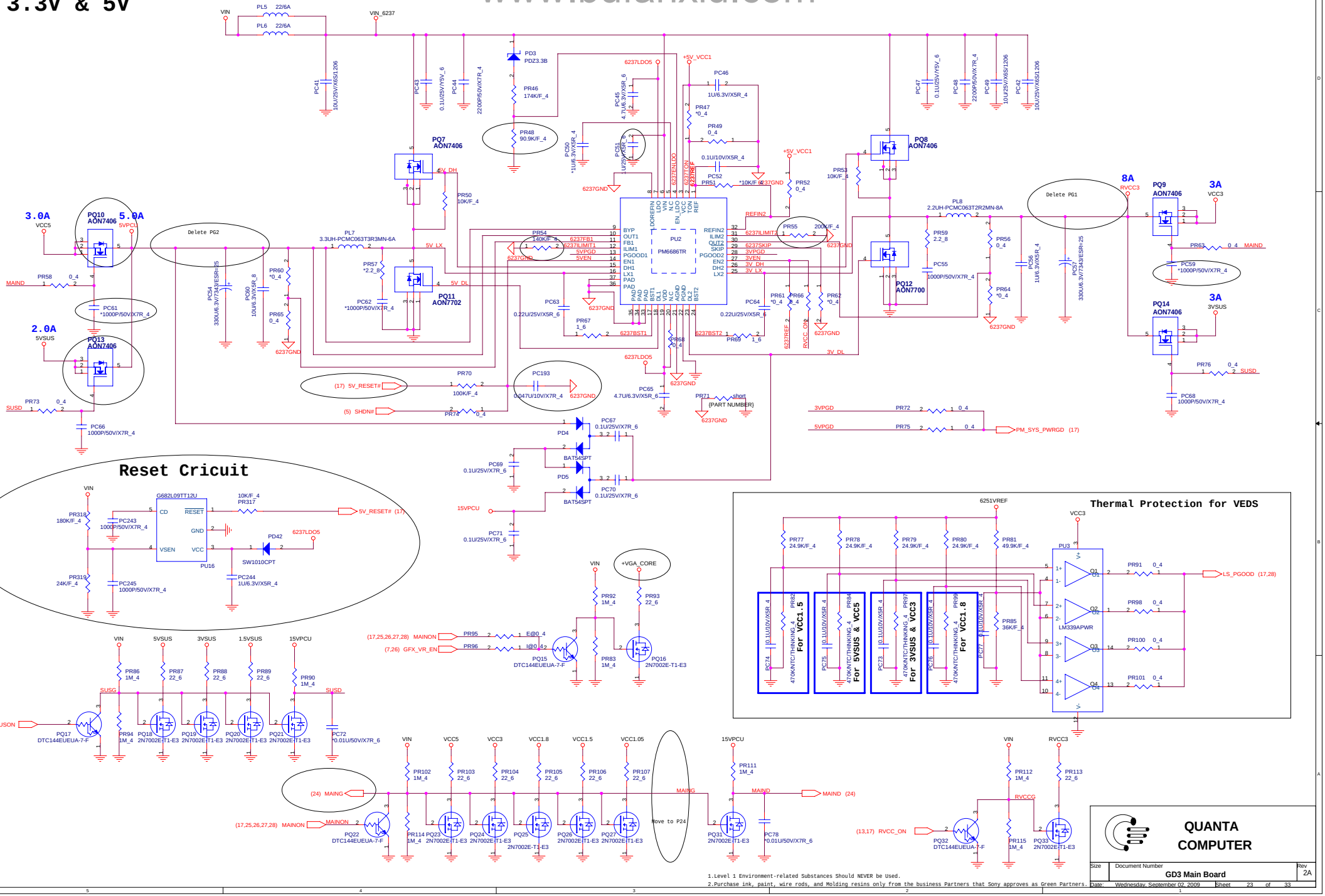
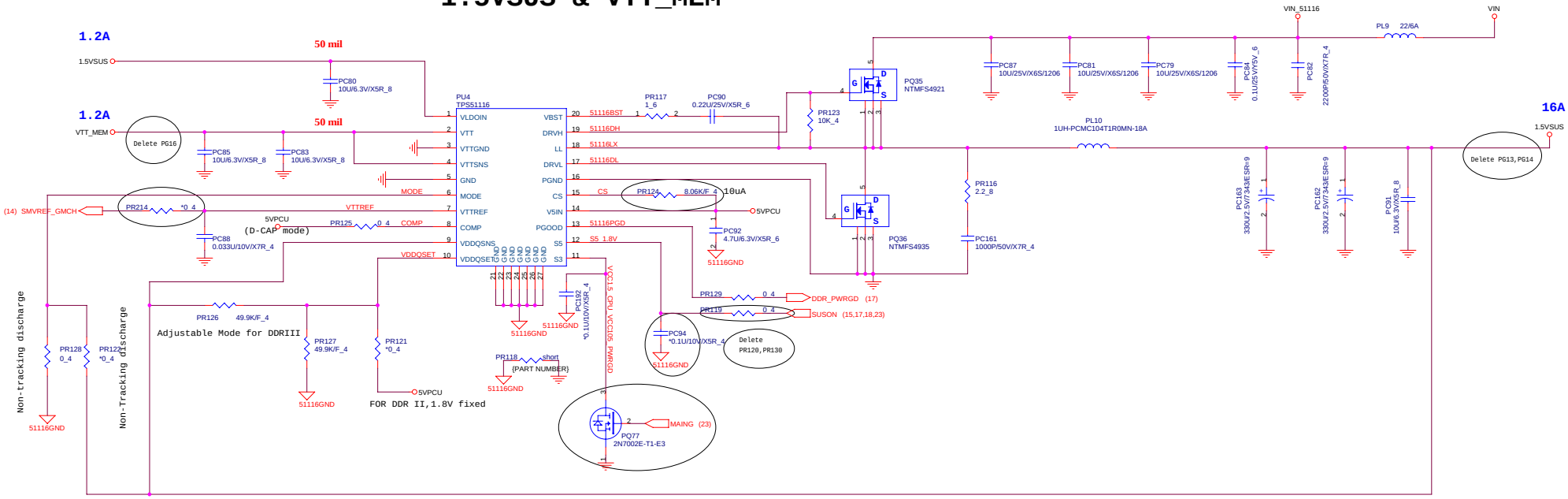
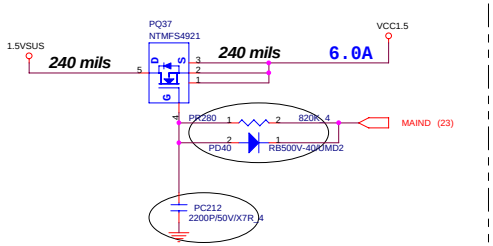
3.3V & 5V



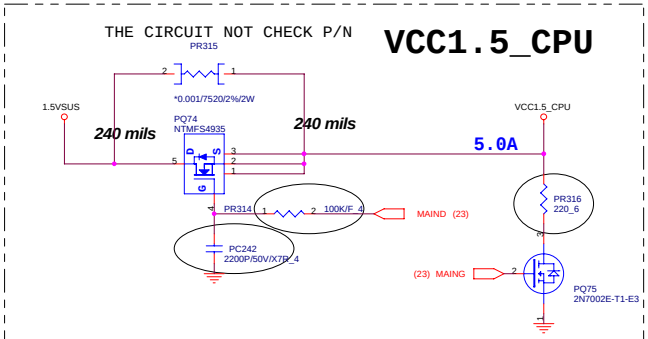
1.5VSUS & VTT_MEM



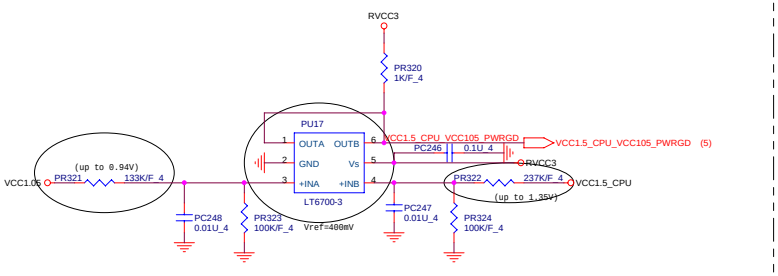
VCC1.5



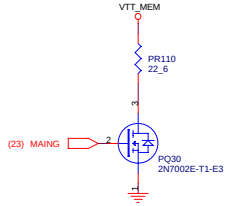
VCC1.5_CPU



VCC1.5_CPU_VCC105_PWRGD



VTT_MEM Discharge

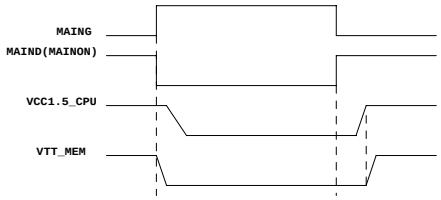


MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

VTT = VTTREF = VDDQSNS/2 = 0.9V

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



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QUANTA COMPUTER

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	GD3 Main Board	2A

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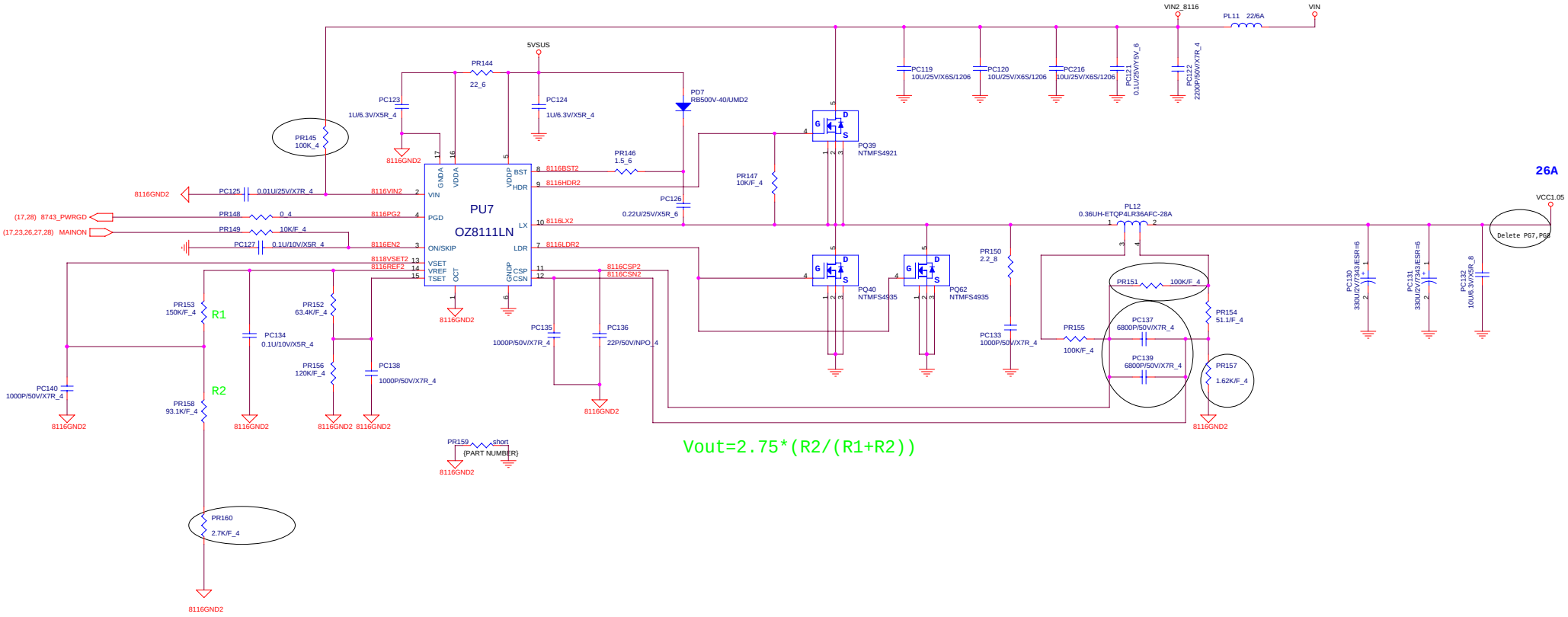

(Ext. Graphice Plaes NDI PQ41,PR161)

VTT_SEL	VCC1.05-1
High	1.05V
Low	1.10V

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QUANTA COMPUTER

Size	Document Number	Rev
	GD3 Main Board	1A

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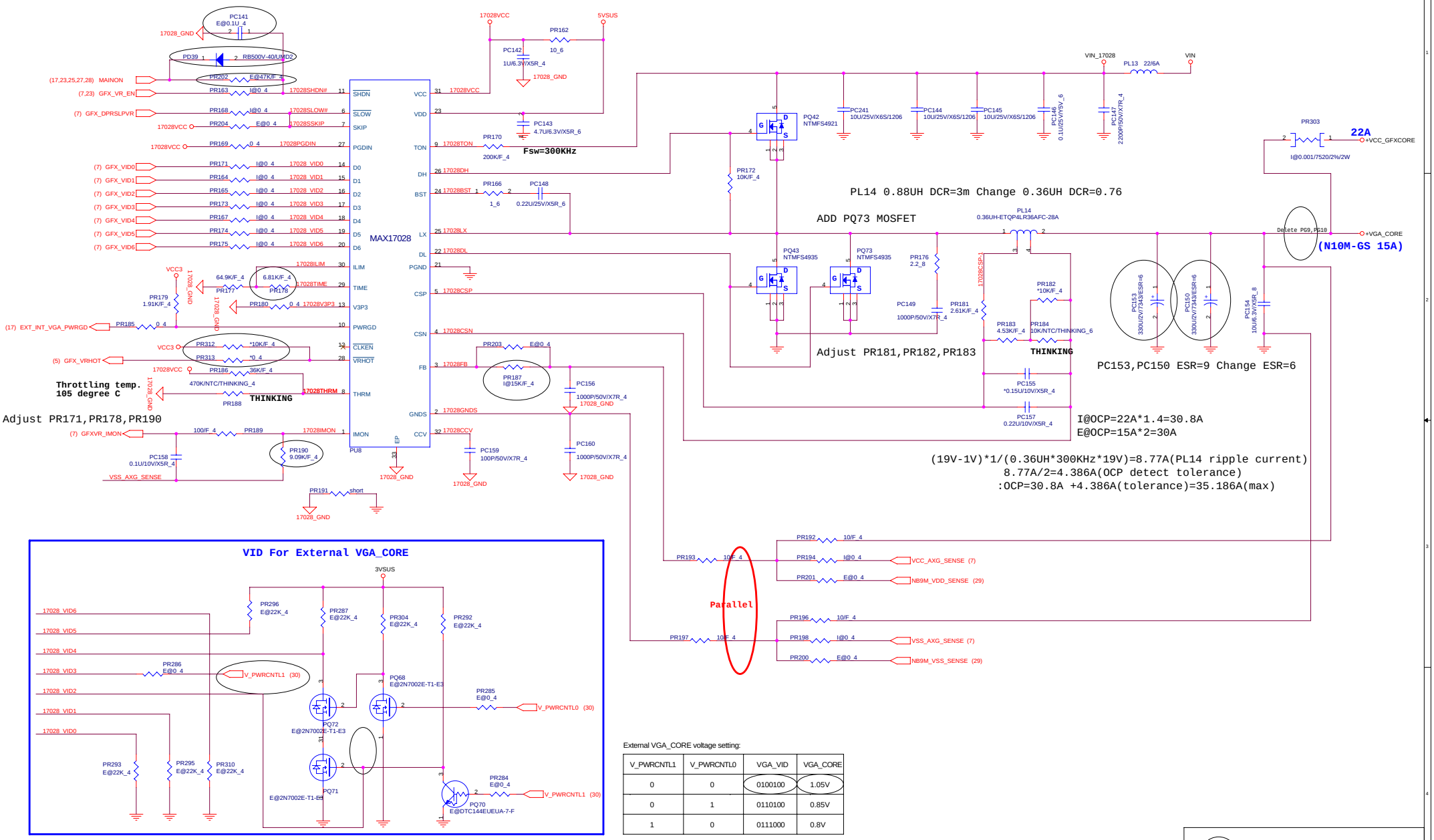

External VGA_CORE voltage setting:

V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0100100	1.05V
0	1	0110100	0.85V
1	0	0111000	0.8V

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QUANTA COMPUTER

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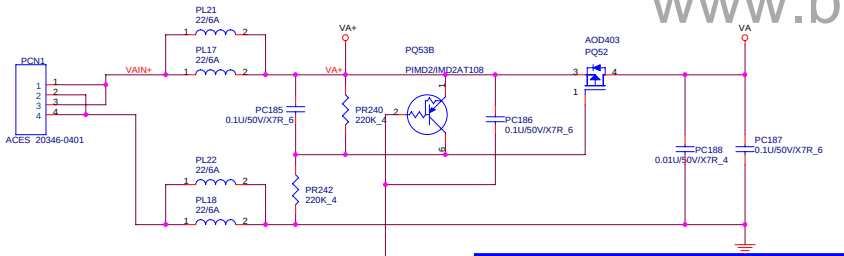

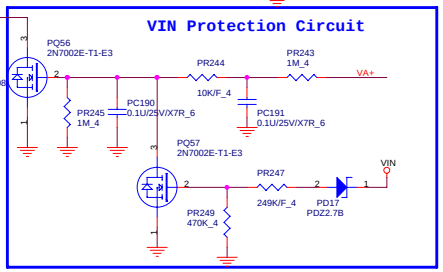

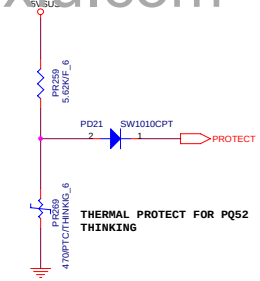

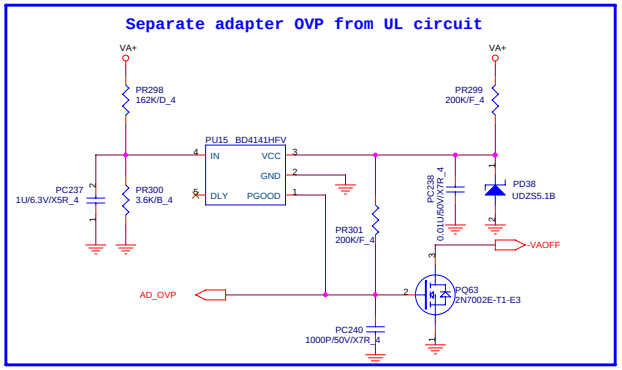

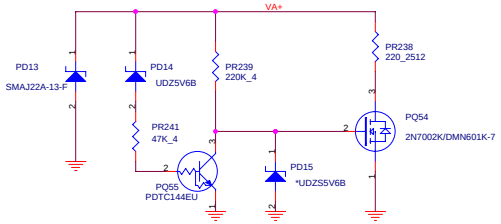

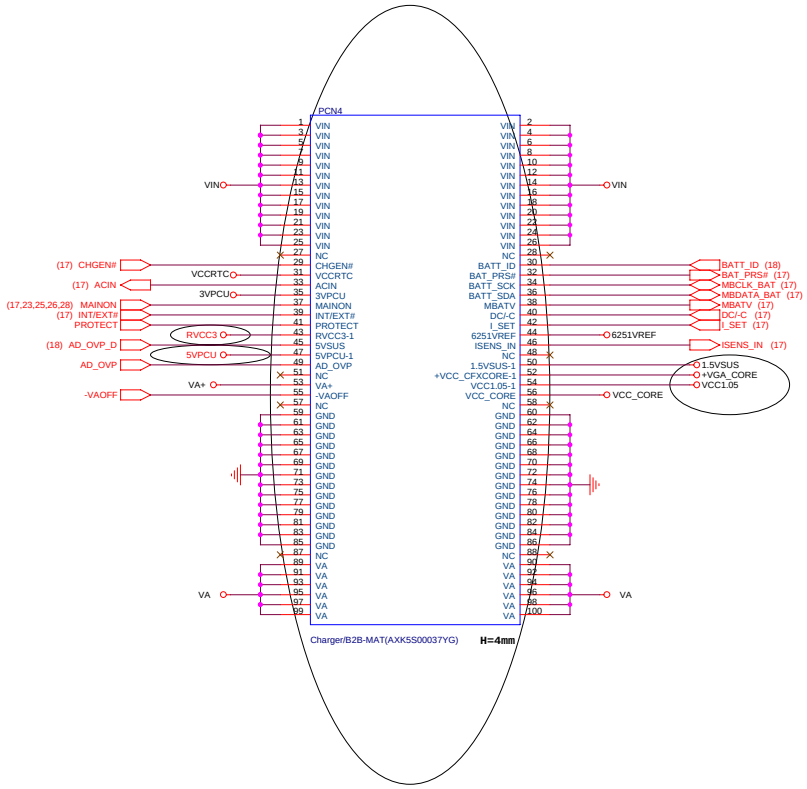

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QUANTA COMPUTER

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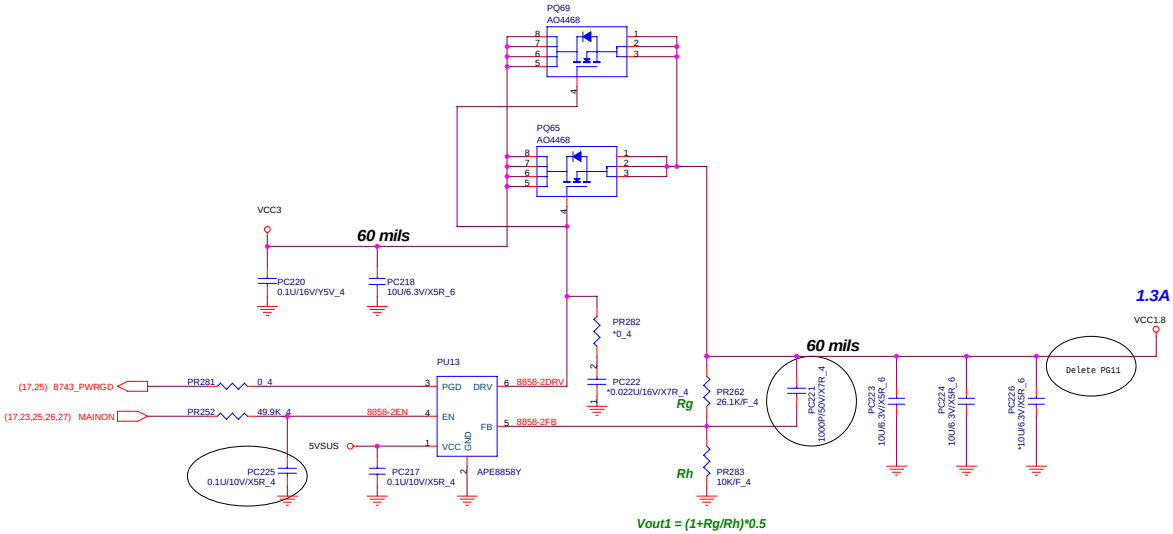
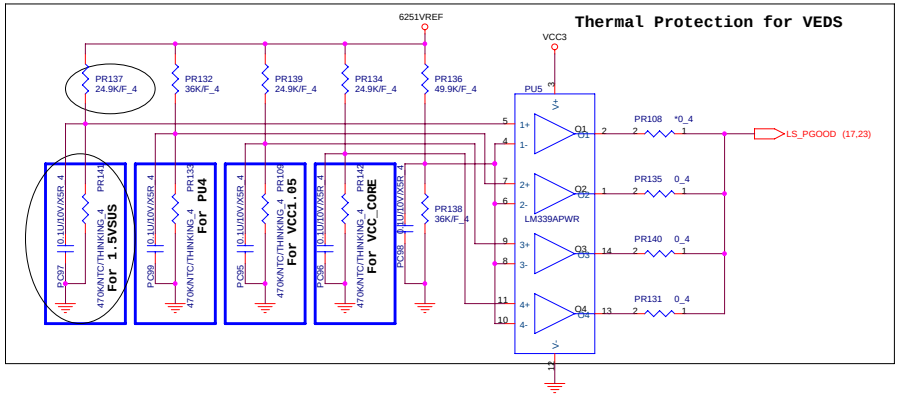
VCC1.8





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QUANTA COMPUTER

Size	Document Number	Rev
	GD3 Main Board	4A
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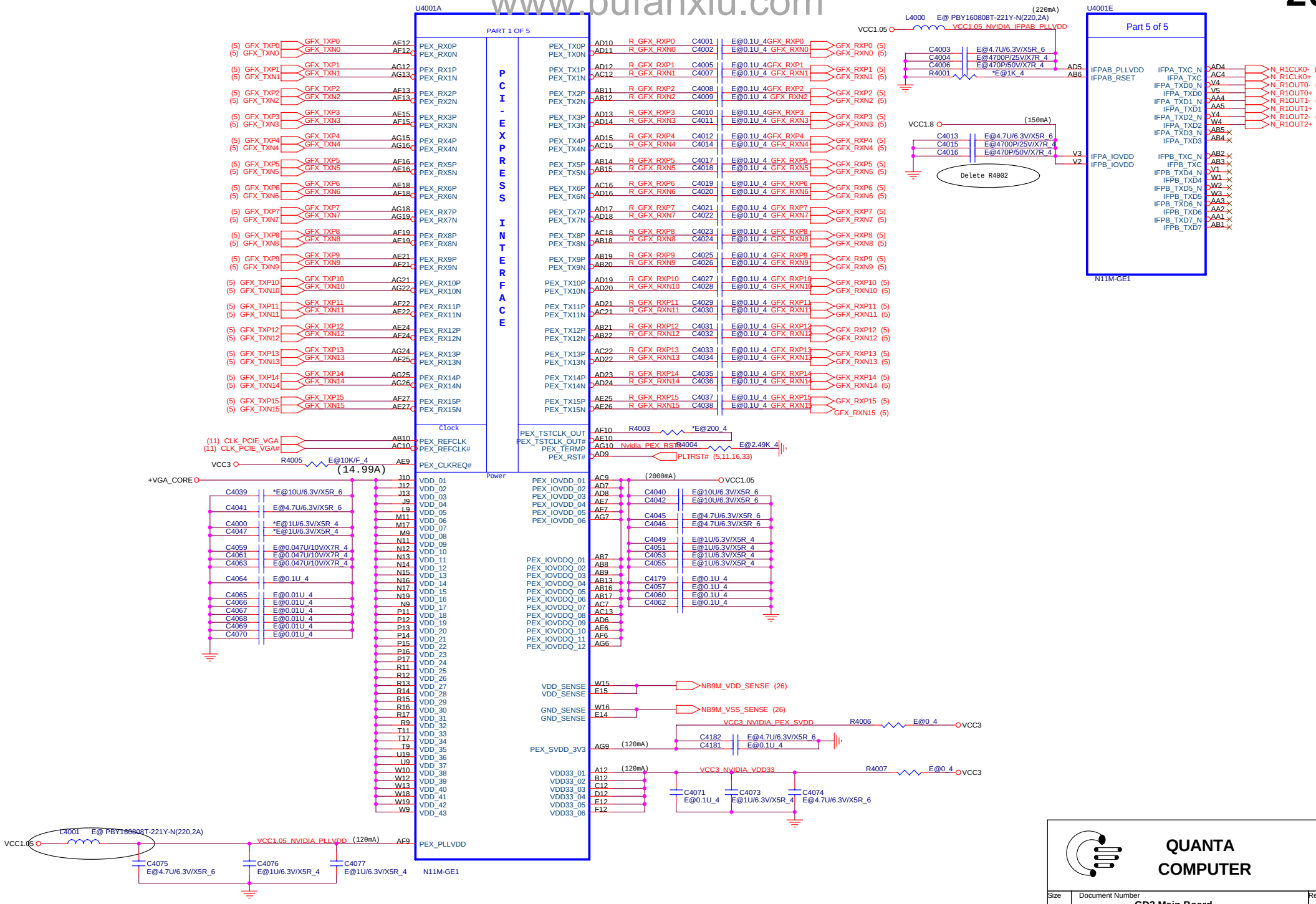

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QUANTA COMPUTER

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nVidia VGA_CORE voltage setting:

V_PWRCNTL1	V_PWRCNTL0	VGA_VID	VGA_CORE
0	0	0101000	1.0V
0	1	0110100	0.85V
1	0	0111000	0.8V

Logical Strap Bit Mapping

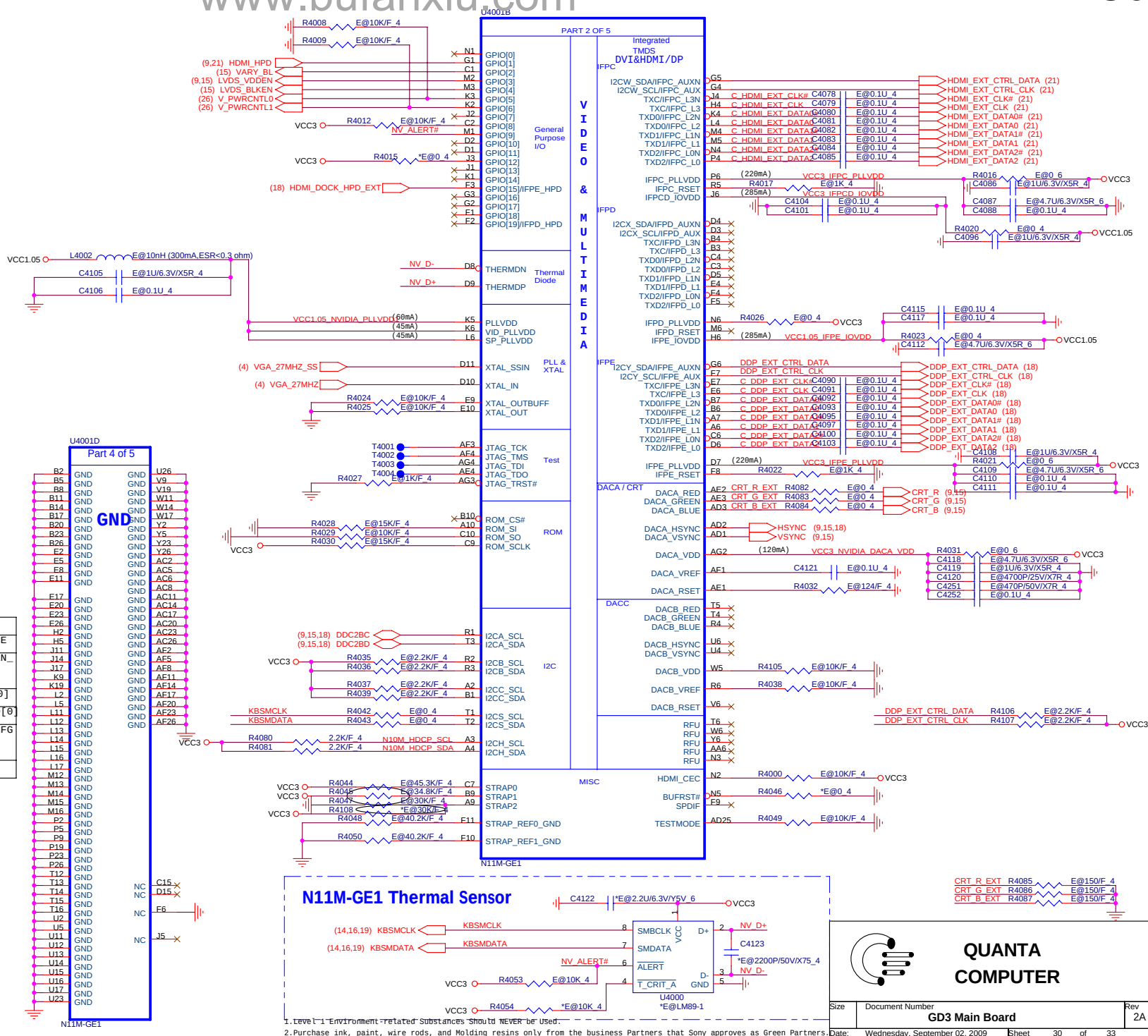
Resister Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG [3]	3GIO_PADCFG [2]	3GIO_PADCFG [1]	3GIO_PADCFG [0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

VRAM Strap:ROM_SI ; RAMCFG[x]

VRAM Capacity	VRAM Vender	ID	R4028
DDR3 64Mx16	Samsung	0011	PD20K
	Hynix	0010	PD15K



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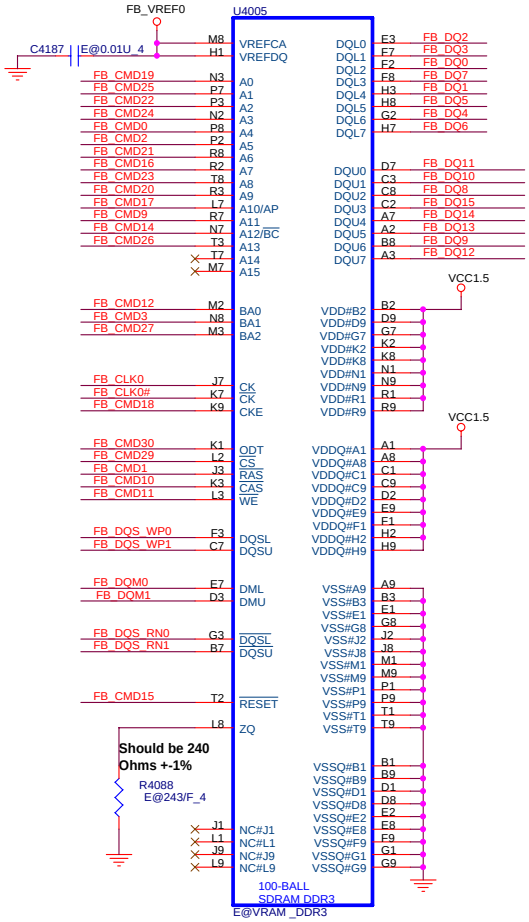
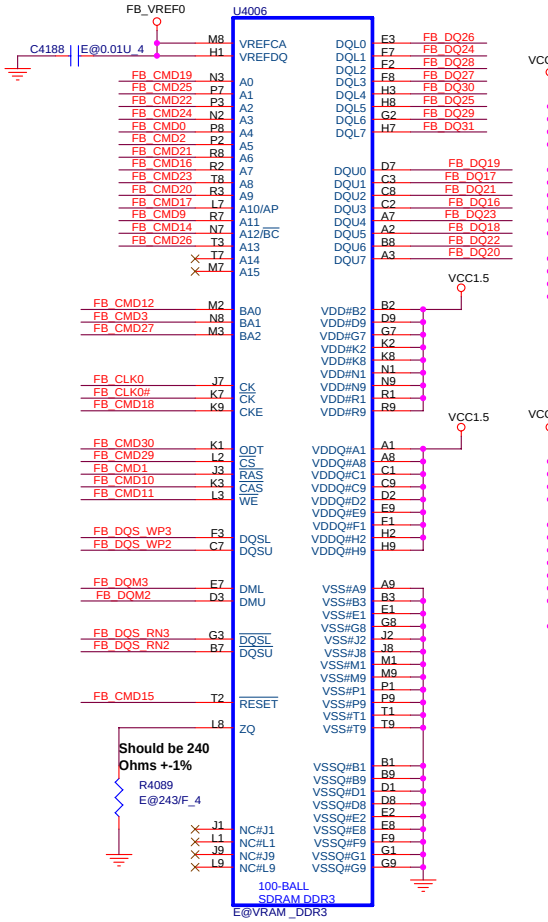
Down Side VRAM TOP/BOT

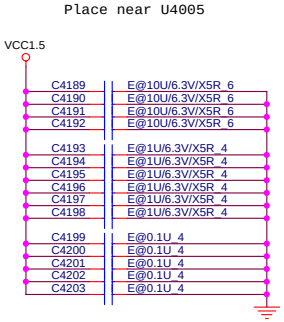
TOP



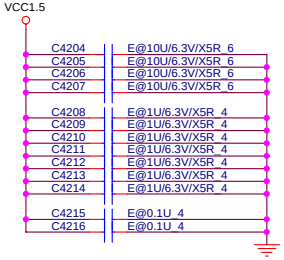
BOT



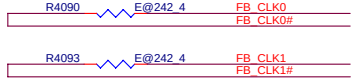
Place near U4005

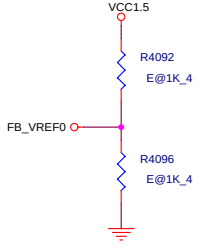


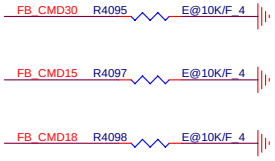
Place near U4006

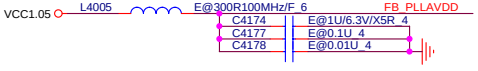


Place near VRAM side









1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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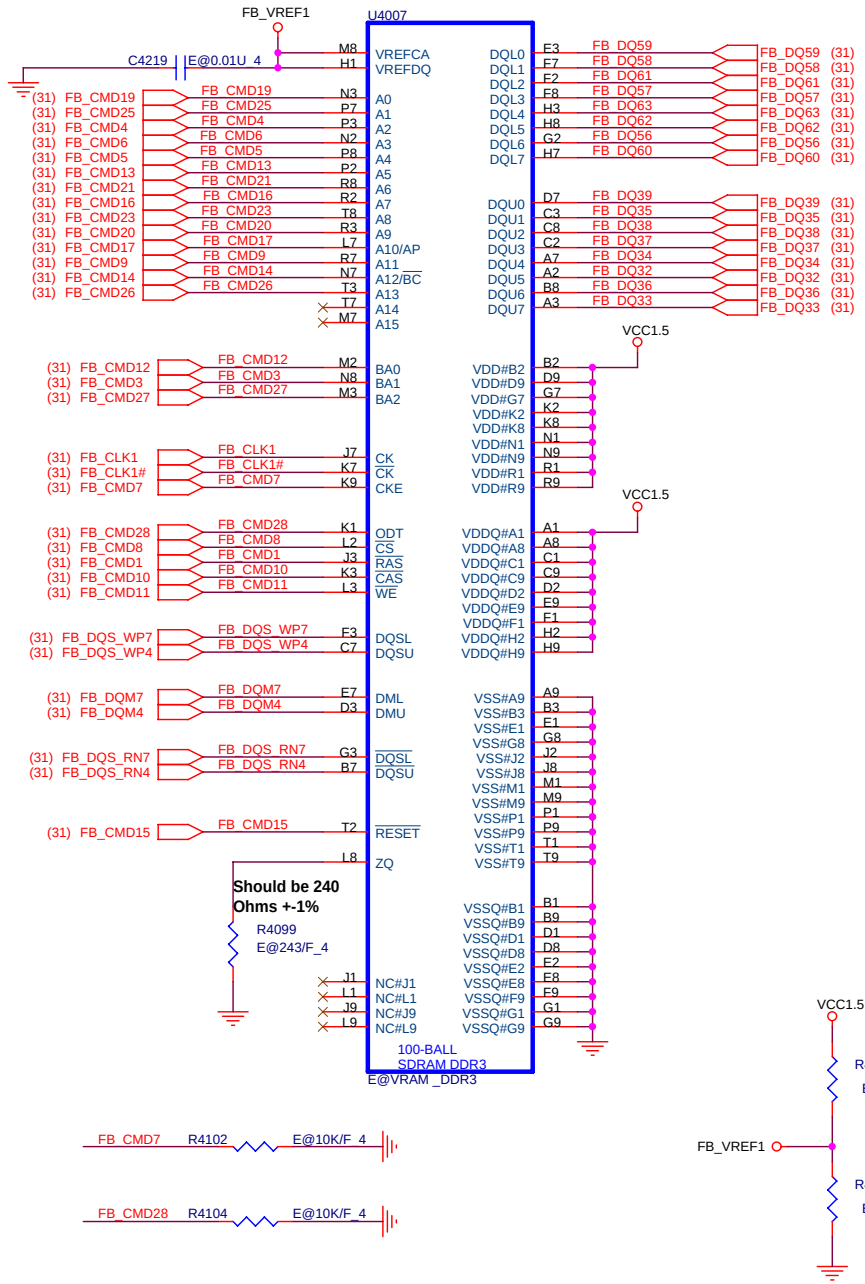
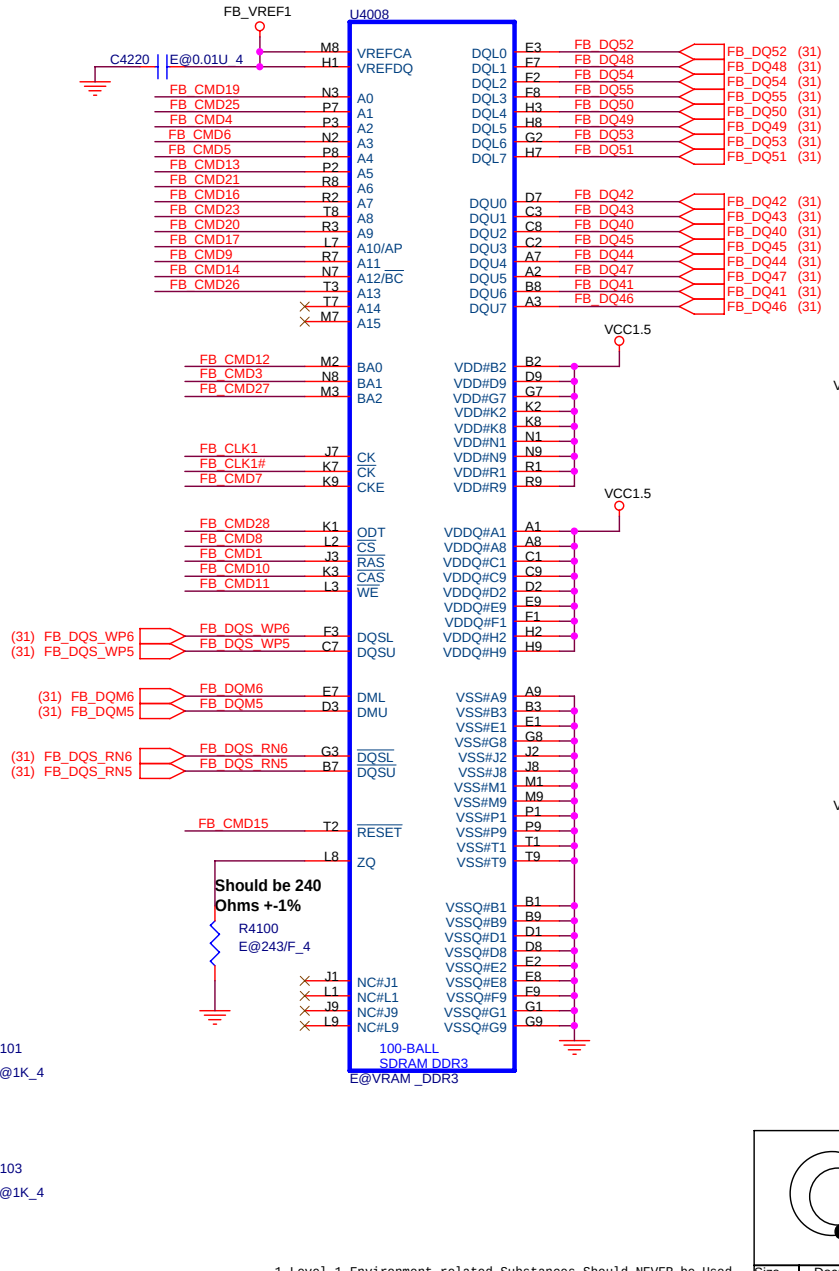
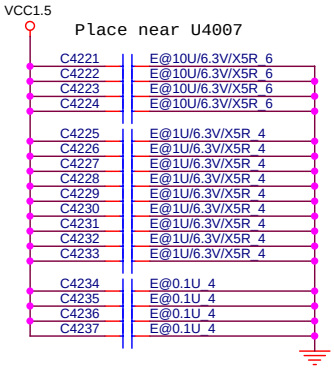
Up Side VRAM TOP/BOT

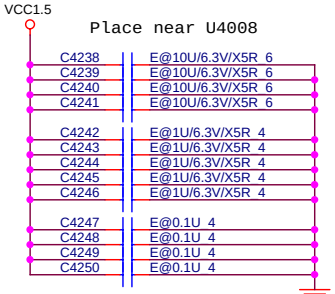
TOP



BOT







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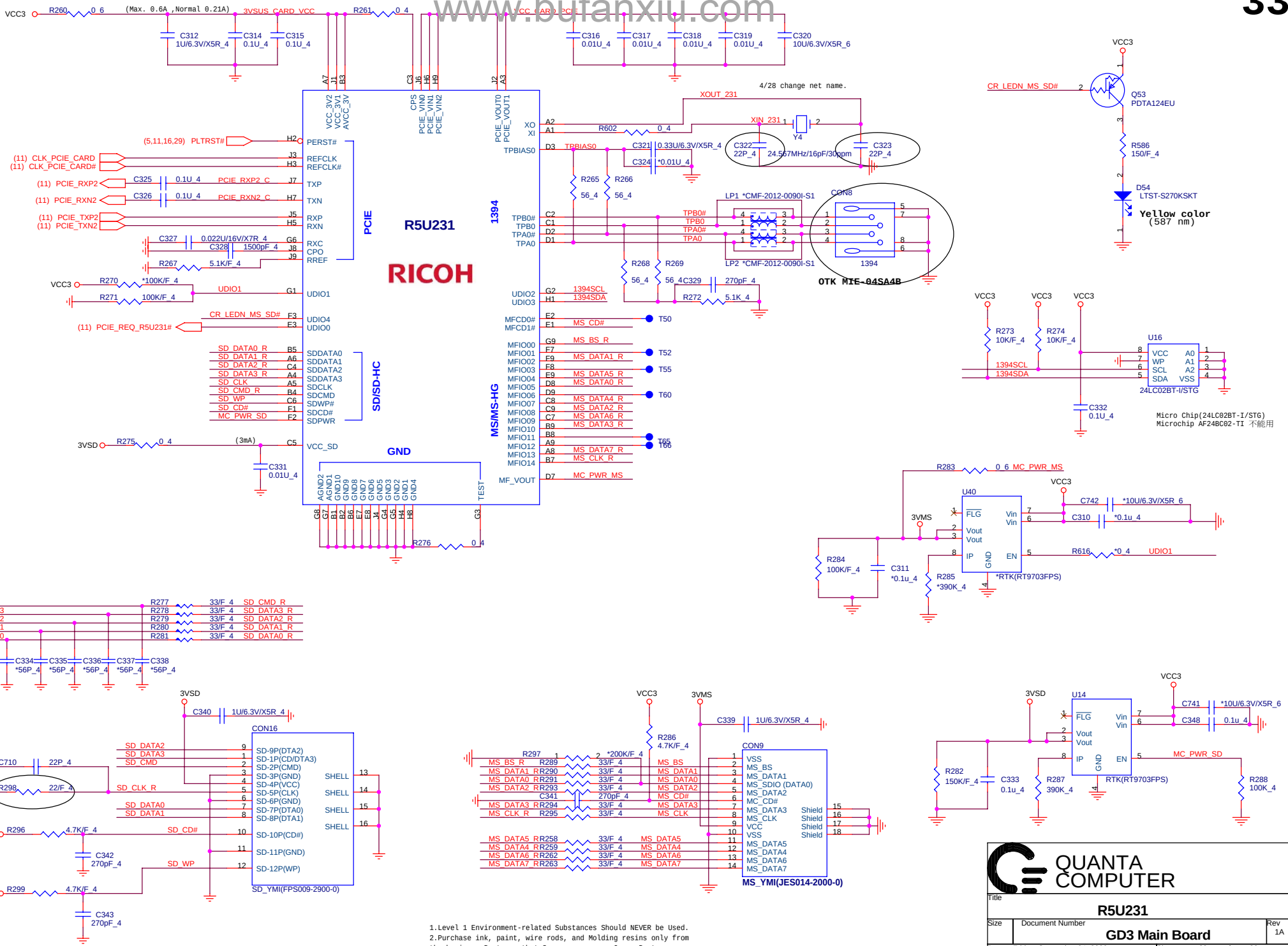

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QUANTA COMPUTER

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