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MONACO

CPU : AMD SEMPRON
Chip Set : NVIDIA C51MV & MCP51
Remarks : 17"LCD

Model Name : MONACO
PBA Name : MAIN
PCB Code : BA41-00687A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2006.07.05

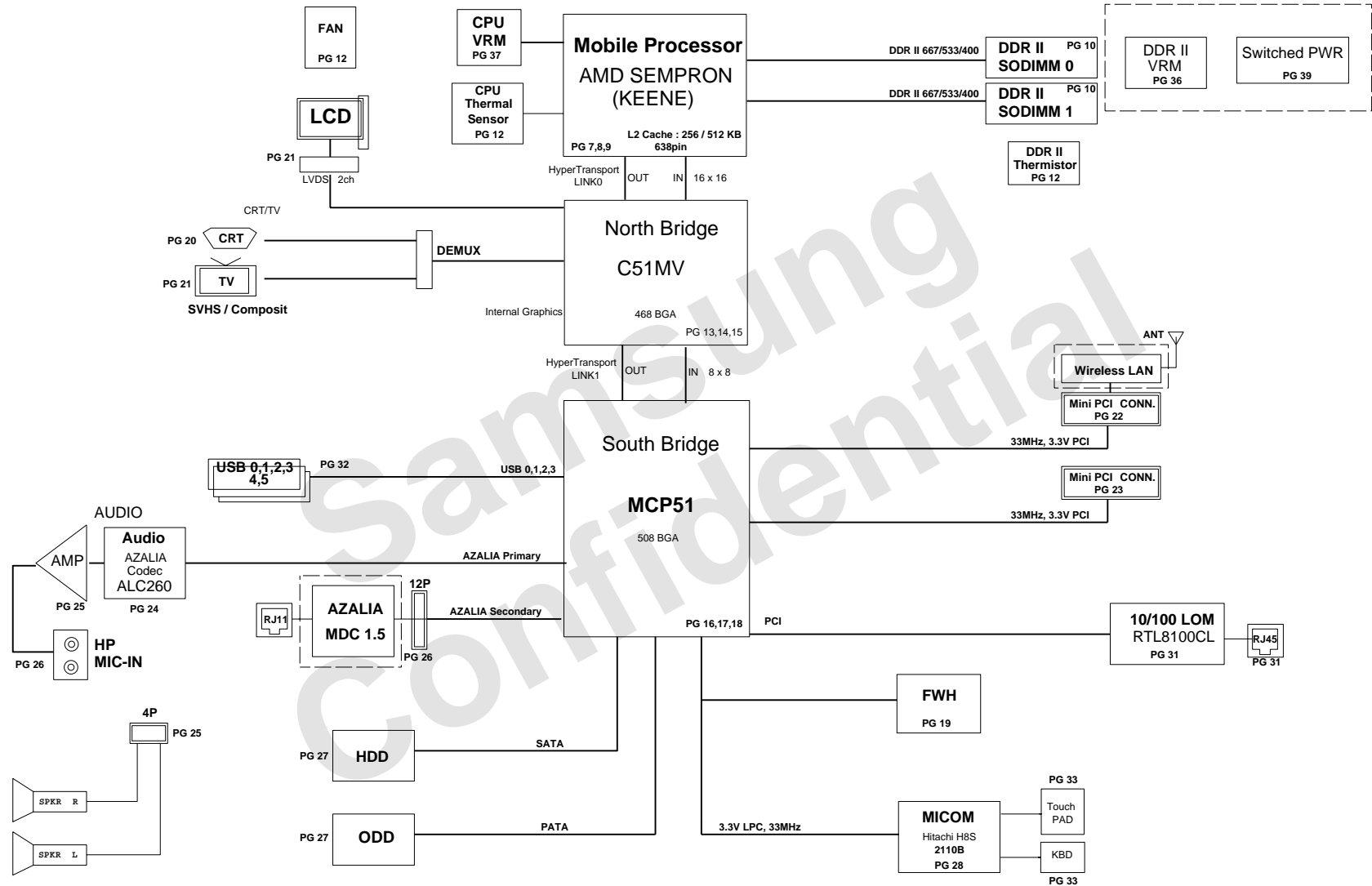
DRAW	CHECK	APPROVAL
SON, C.W	LEE, S.P	LIM, J.G

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DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN COVER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	PART NO.		
APPROVAL	LIM, J.G	REV	1.0	BA41-00687A		
MODULE CODE	LAST EDIT		July 5, 2006 3:50:07 PM	PAGE 1 OF 42		

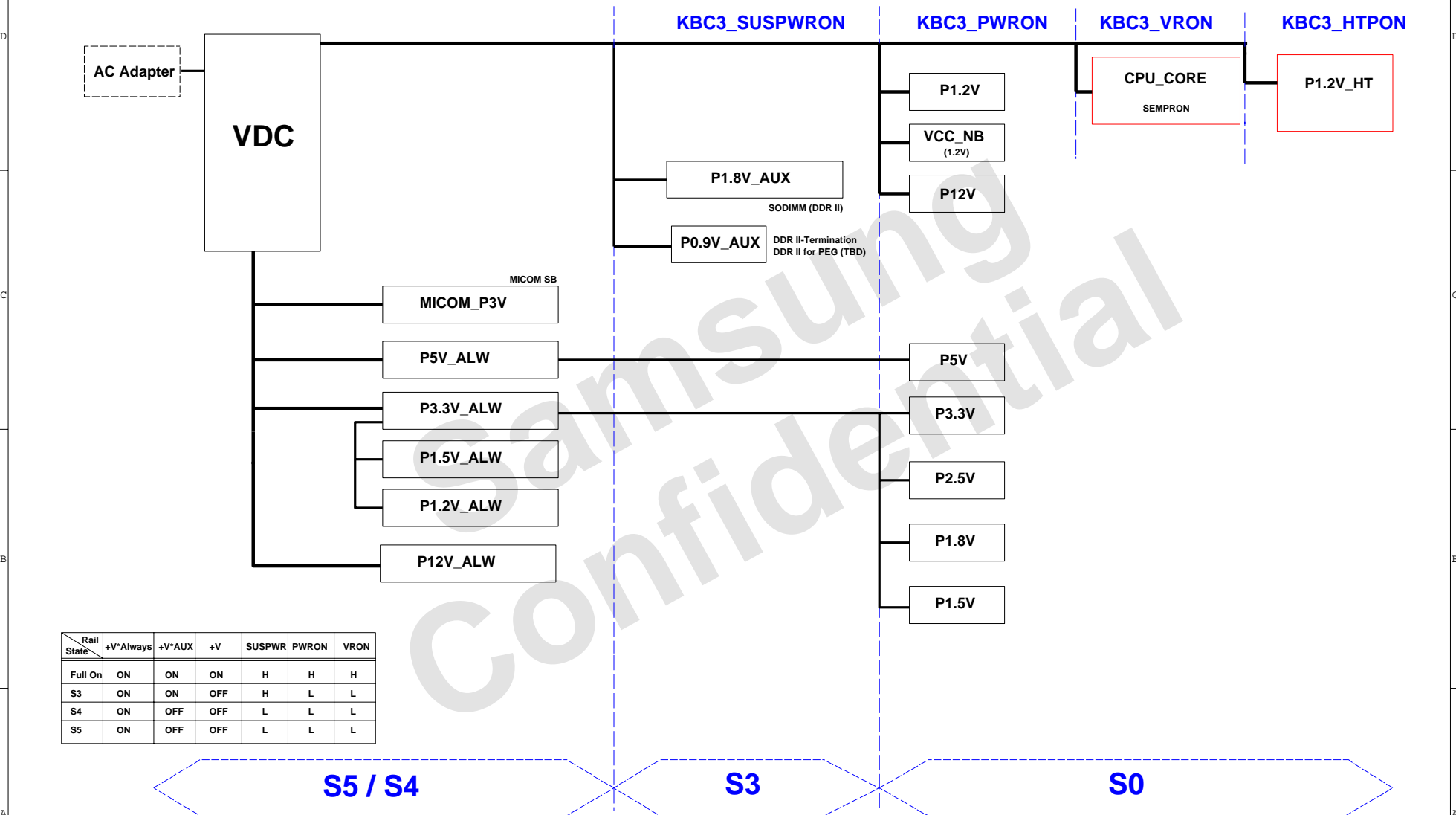
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DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
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Power Diagram



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
MINIPCI A	AD21	0	A,B
MINIPCI B	AD22	1	C,D
LAN	AD23	2	D
5-IN-1	AD24	3	B
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	25MHz	MCP51	MCP51 REF CLOCK
Crystal	32.768KHz	MCP51	Real Time Clock
Crystal	10MHz	MICOM	H8S-2110B
Crystal	27MHz	C51MV	TV OUT
Crystal	25MHz	LAN	RTL8110CL

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core voltage for AMD SEMPRON (1.308-1.068V)
VCC_NB	SEMPRON Processor Hyper Transport (1.2V) North Bridge Core Voltage
P0.9V_AUX	0.9V switched power rail (off in S4-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWS	5V power rail (Always On)
P3.3V_ALWS	3.3V power rail (Always On)
P1.5V_ALWS	1.5V power rail (Always On)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.5500 V	1 0 0 0 0 0	0.7625 V
0 0 0 0 0 1	1.5250 V	1 0 0 0 0 1	0.7500 V
0 0 0 0 1 0	1.5000 V	1 0 0 0 1 0	0.7375 V
0 0 0 0 1 1	1.4750 V	1 0 0 0 1 1	0.7250 V
0 0 0 1 0 0	1.4500 V	1 0 0 1 0 0	0.7125 V
0 0 0 1 0 1	1.4250 V	1 0 0 1 0 1	0.7000 V
0 0 0 1 1 0	1.4000 V	1 0 0 1 1 0	0.6875 V
0 0 0 1 1 1	1.3750 V	1 0 0 1 1 1	0.6750 V
0 0 1 0 0 0	1.3500 V	1 0 1 0 0 0	0.6625 V
0 0 1 0 0 1	1.3250 V	1 0 1 0 0 1	0.6500 V
0 0 1 0 1 0	1.3000 V	1 0 1 0 1 0	0.6375 V
0 0 1 0 1 1	1.2750 V	1 0 1 0 1 1	0.6250 V
0 0 1 1 0 0	1.2500 V	1 0 1 1 0 0	0.6125 V
0 0 1 1 0 1	1.2250 V	1 0 1 1 0 1	0.6000 V
0 0 1 1 1 0	1.2000 V	1 0 1 1 1 0	0.5875 V
0 0 1 1 1 1	1.1750 V	1 0 1 1 1 1	0.5750 V
0 1 0 0 0 0	1.1500 V	1 1 0 0 0 0	0.5625 V
0 1 0 0 0 1	1.1250 V	1 1 0 0 0 1	0.5500 V
0 1 0 0 1 0	1.1000 V	1 1 0 0 1 0	0.5375 V
0 1 0 0 1 1	1.0750 V	1 1 0 0 1 1	0.5250 V
0 1 0 1 0 0	1.0500 V	1 1 0 1 0 0	0.5125 V
0 1 0 1 0 1	1.0250 V	1 1 0 1 0 1	0.5000 V
0 1 0 1 1 0	1.0000 V	1 1 0 1 1 0	0.4875 V
0 1 0 1 1 1	0.9750 V	1 1 0 1 1 1	0.4750 V
0 1 1 0 0 0	0.9500 V	1 1 1 0 0 0	0.4625 V
0 1 1 0 0 1	0.9250 V	1 1 1 0 0 1	0.4500 V
0 1 1 0 1 0	0.9000 V	1 1 1 0 1 0	0.4375 V
0 1 1 0 1 1	0.8750 V	1 1 1 0 1 1	0.4250 V
0 1 1 1 0 0	0.8500 V	1 1 1 1 0 0	0.4125 V
0 1 1 1 0 1	0.8250 V	1 1 1 1 0 1	0.4000 V
0 1 1 1 1 0	0.8000 V	1 1 1 1 1 0	0.3875 V
0 1 1 1 1 1	0.7750 V	1 1 1 1 1 1	0.3750 V

IC / SMB Address

Devices	Address	Hex	Bus
MCP51	Master	-	SMBUS Master
W83L786NG(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor

USB PORT Assign

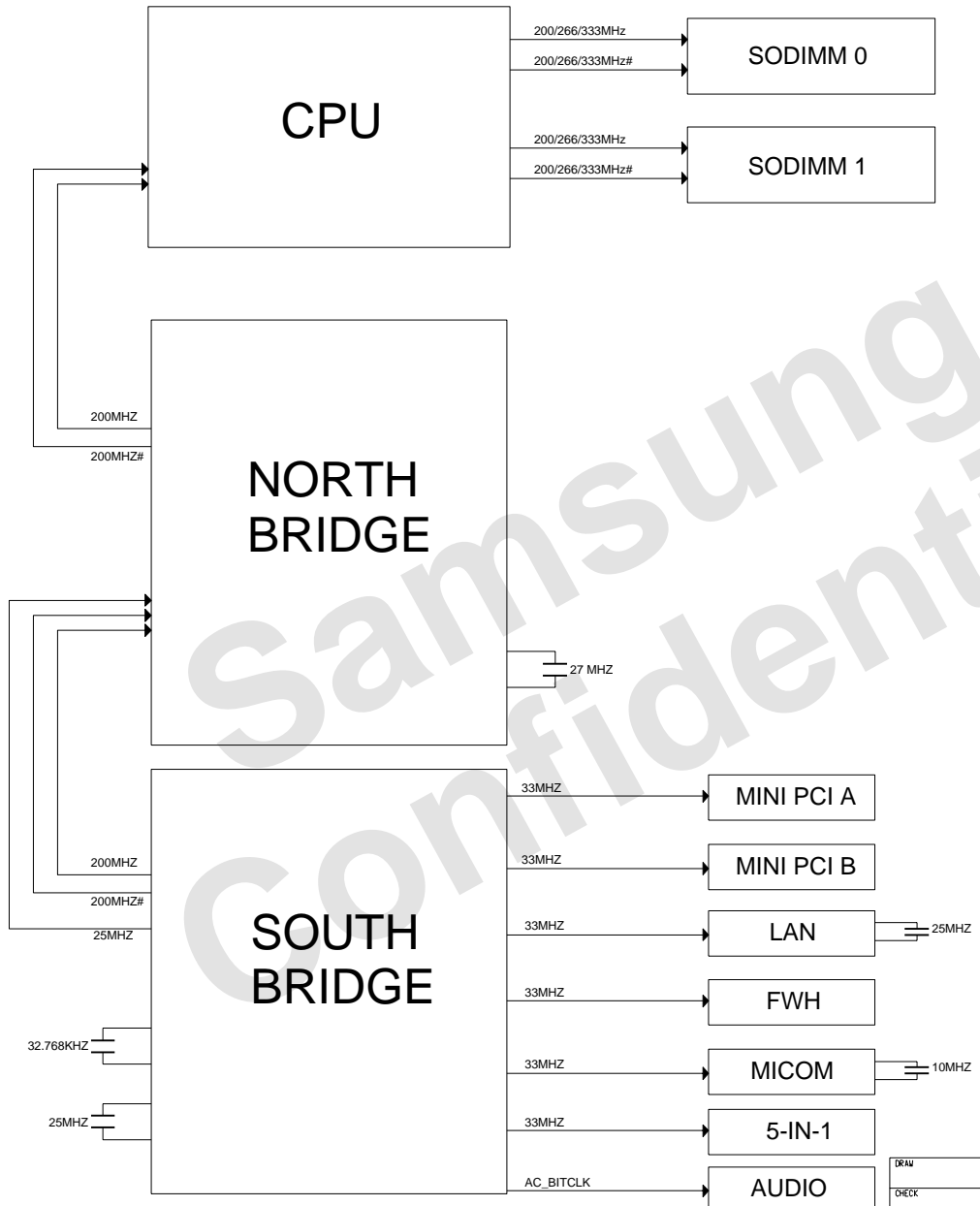
PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2,3	SYSTEM PORT B
4,5	SYSTEM PORT C
6	DMB

System Power States

- CHP3_SLP5* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLP3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLP4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLP5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

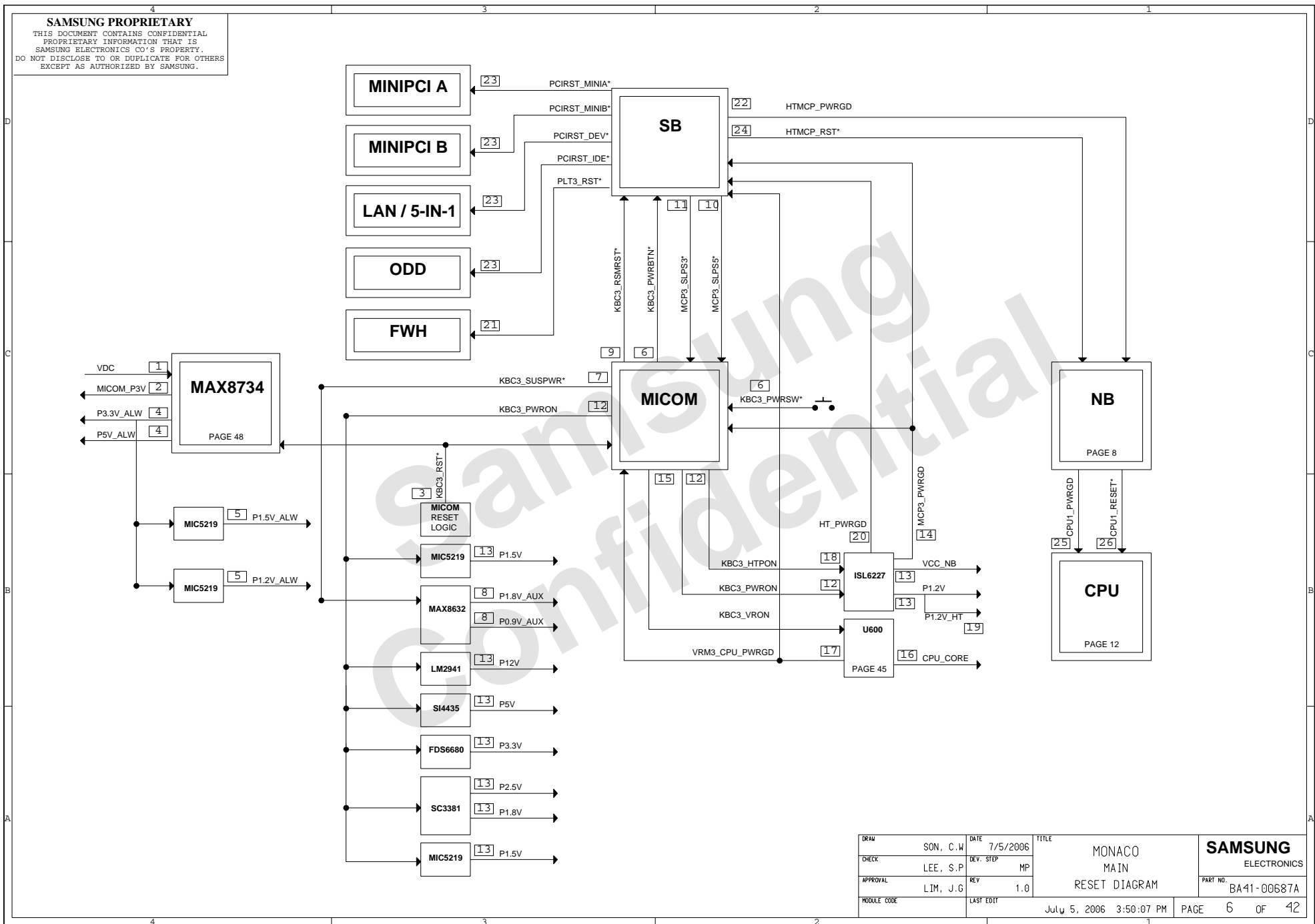
DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP		MAIN	
APPROVAL	LIM, J.G	REV	1.0		BOARD INFORMATION	PART NO. BA41-00687A
MODULE CODE		LAST EDIT		July 5, 2006 3:50:07 PM	PAGE	4 OF 42

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APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
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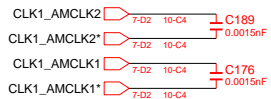
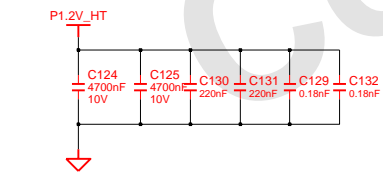
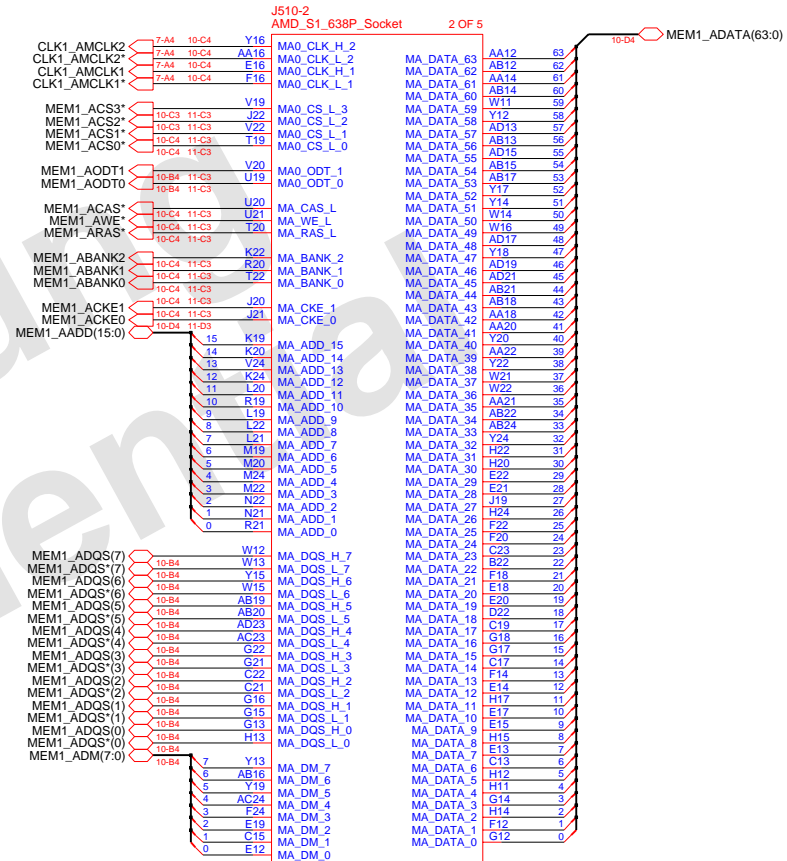
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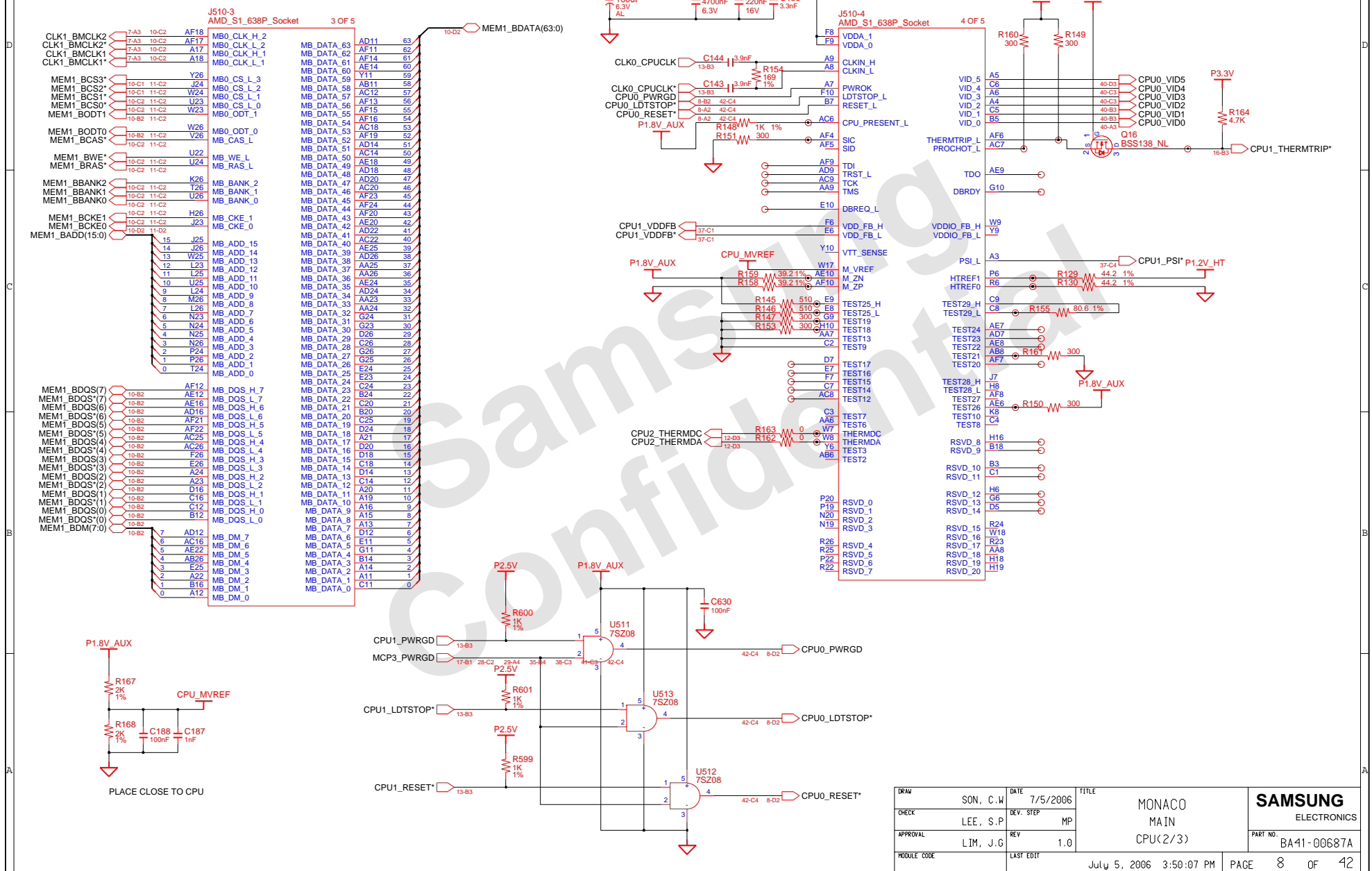
PLACE CLOSE TO PROCESSOR WITHIN 1.5INCH

PLACE CLOSE TO PROCESSOR WITHIN 1.5INCH

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN CPU(1/3)	SAMSUNG ELECTRONICS PART NO. BA41-00687A
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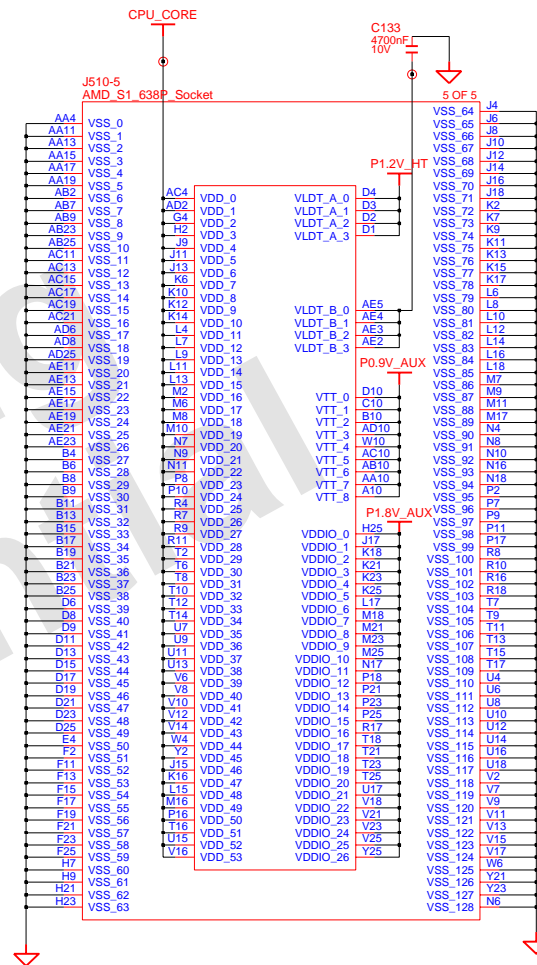
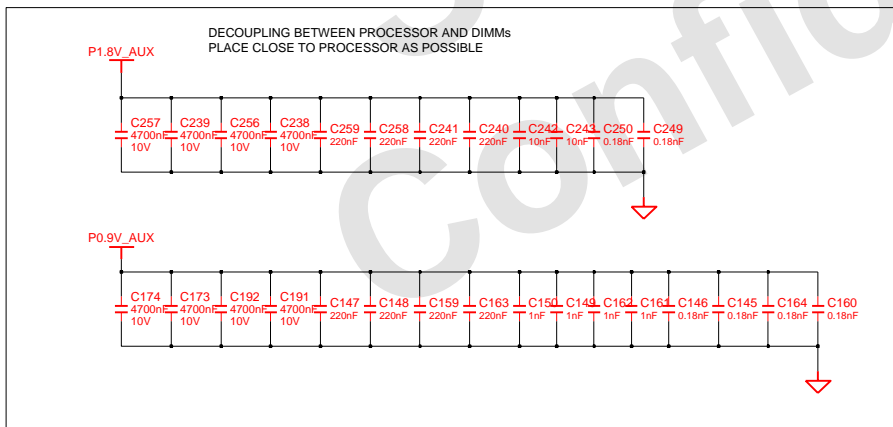
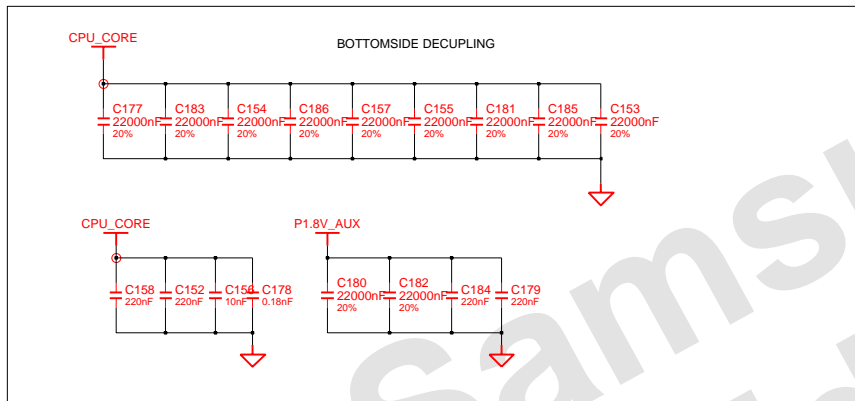
J510-3 AMD_S1_638P_Socket 3 OF 5		MEM1_BDATA(63.0)	
CLK1_BMCLK2	7-A3 10-C2 AF18	MB_DATA_63	AD11 63
CLK1_BMCLK2*	7-A3 10-C2 AF17	MB_DATA_62	AF11 62
CLK1_BMCLK1	7-A3 10-C2 A17	MB_DATA_61	AF14 61
CLK1_BMCLK1*	7-A3 10-C2 A18	MB_DATA_60	AE14 60
MEM1_BCS2*	Y26	MB_DATA_59	Y11 59
MEM1_BCS1*	10-C1 11-C2 J24	MB_DATA_58	AB11 58
MEM1_BCS0*	10-C1 11-C2 W24	MB_DATA_57	AC12 57
MEM1_BODT1	10-C2 11-C2 U23	MB_DATA_56	AF13 56
MEM1_BODT0	10-C2 11-C2 W23	MB_DATA_55	AF15 55
MEM1_BODT0*	10-B2 11-C2	MB_DATA_54	AF16 54
MEM1_BODT0*	10-B2 11-C2	MB_DATA_53	AC18 53
MEM1_BODT0*	10-B2 11-C2	MB_DATA_52	AF19 52
MEM1_BODT0*	10-C2 11-C2	MB_DATA_51	AD14 51
MEM1_BODT0*	10-C2 11-C2	MB_DATA_50	AC14 50
MEM1_BODT0*	10-C2 11-C2	MB_DATA_49	MB_DATA_49
MEM1_BODT0*	10-C2 11-C2	MB_DATA_48	AD18 48
MEM1_BODT0*	10-C2 11-C2	MB_DATA_47	AD20 47
MEM1_BODT0*	10-C2 11-C2	MB_DATA_46	AC20 46
MEM1_BODT0*	10-C2 11-C2	MB_DATA_45	AF23 45
MEM1_BODT0*	10-C2 11-C2	MB_DATA_44	AF24 44
MEM1_BODT0*	10-C2 11-C2	MB_DATA_43	AF20 43
MEM1_BODT0*	10-C2 11-C2	MB_DATA_42	AE20 42
MEM1_BODT0*	10-C2 11-C2	MB_DATA_41	AD22 41
MEM1_BODT0*	10-C2 11-C2	MB_DATA_40	AC22 40
MEM1_BODT0*	10-C2 11-C2	MB_DATA_39	AE25 39
MEM1_BODT0*	10-C2 11-C2	MB_DATA_38	AD26 38
MEM1_BODT0*	10-C2 11-C2	MB_DATA_37	AA25 37
MEM1_BODT0*	10-C2 11-C2	MB_DATA_36	AE24 36
MEM1_BODT0*	10-C2 11-C2	MB_DATA_35	AD24 34
MEM1_BODT0*	10-C2 11-C2	MB_DATA_34	AA23 33
MEM1_BODT0*	10-C2 11-C2	MB_DATA_33	AA24 32
MEM1_BODT0*	10-C2 11-C2	MB_DATA_32	G24 31
MEM1_BODT0*	10-C2 11-C2	MB_DATA_31	G23 30
MEM1_BODT0*	10-C2 11-C2	MB_DATA_30	D26 29
MEM1_BODT0*	10-C2 11-C2	MB_DATA_29	C26 28
MEM1_BODT0*	10-C2 11-C2	MB_DATA_28	G25 27
MEM1_BODT0*	10-C2 11-C2	MB_DATA_27	E24 26
MEM1_BODT0*	10-C2 11-C2	MB_DATA_26	E23 24
MEM1_BODT0*	10-C2 11-C2	MB_DATA_25	C24 23
MEM1_BODT0*	10-C2 11-C2	MB_DATA_24	B24 22
MEM1_BODT0*	10-C2 11-C2	MB_DATA_23	C20 21
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MEM1_BODT0*	10-C2 11-C2	MB_DATA_17	D18 15
MEM1_BODT0*	10-C2 11-C2	MB_DATA_16	C18 14
MEM1_BODT0*	10-C2 11-C2	MB_DATA_15	D14 13
MEM1_BODT0*	10-C2 11-C2	MB_DATA_14	C14 12
MEM1_BODT0*	10-C2 11-C2	MB_DATA_13	A20 11
MEM1_BODT0*	10-C2 11-C2	MB_DATA_12	A19 10
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MEM1_BODT0*	10-C2 11-C2	MB_DATA_7	E11 5
MEM1_BODT0*	10-C2 11-C2	MB_DATA_6	G11 4
MEM1_BODT0*	10-C2 11-C2	MB_DATA_5	B14 3
MEM1_BODT0*	10-C2 11-C2	MB_DATA_4	B14 3
MEM1_BODT0*	10-C2 11-C2	MB_DATA_3	A14 2
MEM1_BODT0*	10-C2 11-C2	MB_DATA_2	A11 1
MEM1_BODT0*	10-C2 11-C2	MB_DATA_1	A11 1
MEM1_BODT0*	10-C2 11-C2	MB_DATA_0	C11 0
MEM1_BDQS(7)	10-B2 AE12	MB_DOS_H_7	AD12
MEM1_BDQS(7)*	10-B2 AE12	MB_DOS_L_7	AC16
MEM1_BDQS(6)	10-B2 AE16	MB_DOS_H_6	AE22
MEM1_BDQS(6)*	10-B2 AD16	MB_DOS_L_6	AB26
MEM1_BDQS(5)	10-B2 AF21	MB_DOS_H_5	E25
MEM1_BDQS(5)*	10-B2 AF22	MB_DOS_L_5	A22
MEM1_BDQS(4)	10-B2 AC25	MB_DOS_H_4	B16
MEM1_BDQS(4)*	10-B2 AC26	MB_DOS_L_4	B12
MEM1_BDQS(3)	10-B2 F26	MB_DOS_H_3	AD12
MEM1_BDQS(3)*	10-B2 E26	MB_DOS_L_3	AC16
MEM1_BDQS(2)	10-B2 AE16	MB_DOS_H_2	AE22
MEM1_BDQS(2)*	10-B2 AD16	MB_DOS_L_2	AB26
MEM1_BDQS(1)	10-B2 AF21	MB_DOS_H_1	E25
MEM1_BDQS(1)*	10-B2 AF22	MB_DOS_L_1	A22
MEM1_BDQS(0)	10-B2 AC25	MB_DOS_H_0	B16
MEM1_BDQS(0)*	10-B2 AC26	MB_DOS_L_0	B12
MEM1_BDQS(0)	10-B2 F26	MB_DOS_L_0	AD12
MEM1_BDQS(0)*	10-B2 E26	MB_DOS_L_0	AC16
MEM1_BDQS(0)	10-B2 AE16	MB_DM_7	AE22
MEM1_BDQS(0)*	10-B2 AD16	MB_DM_6	AB26
MEM1_BDQS(0)	10-B2 AF21	MB_DM_5	E25
MEM1_BDQS(0)*	10-B2 AF22	MB_DM_4	A22
MEM1_BDQS(0)	10-B2 AC25	MB_DM_3	B16
MEM1_BDQS(0)*	10-B2 AC26	MB_DM_2	B12
MEM1_BDQS(0)	10-B2 F26	MB_DM_1	AD12
MEM1_BDQS(0)*	10-B2 E26	MB_DM_0	AC16

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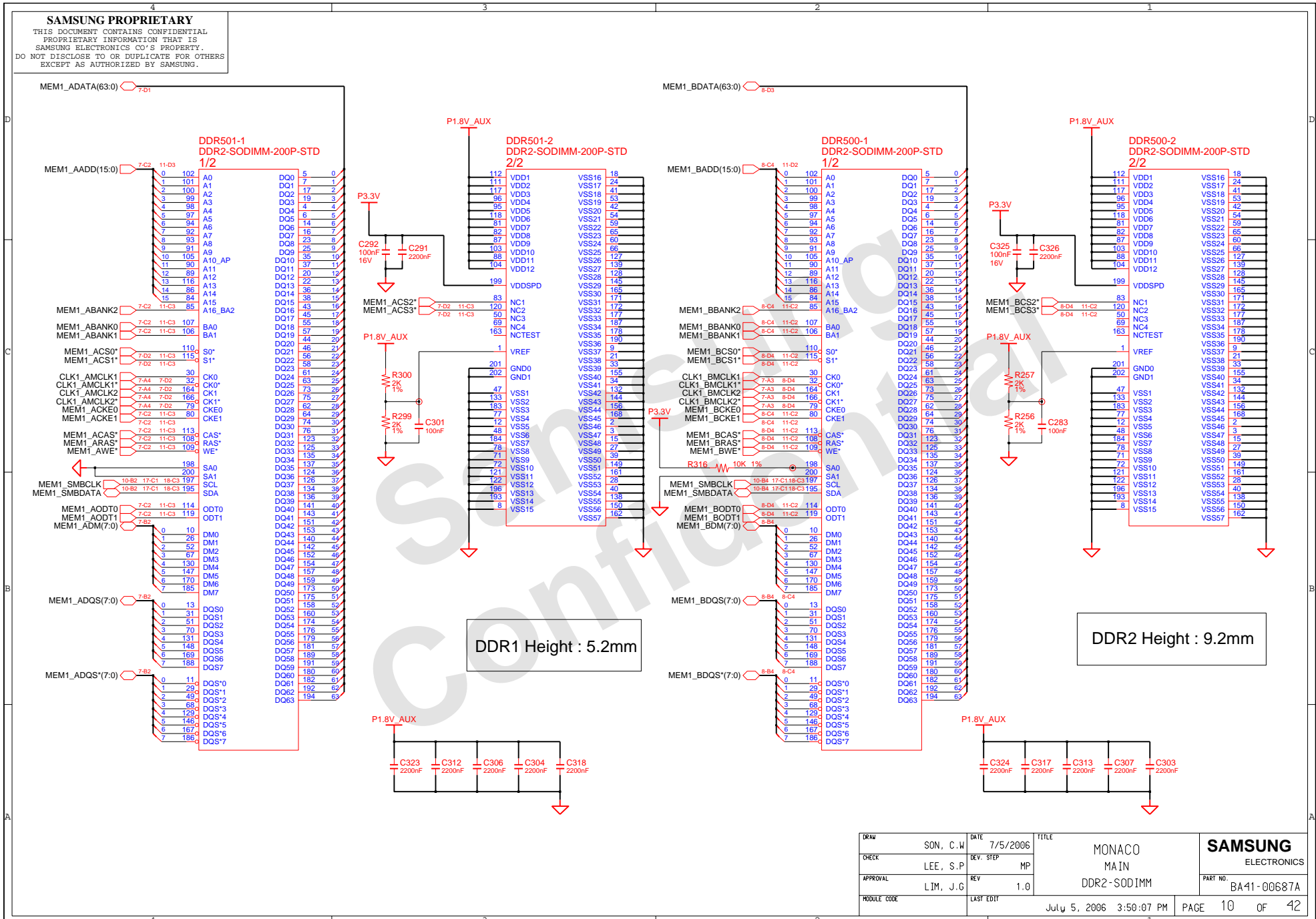
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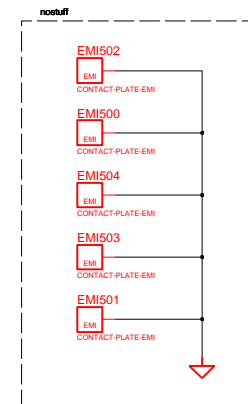
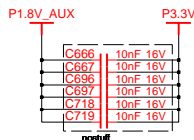
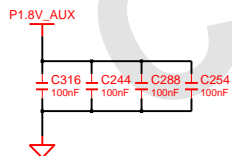
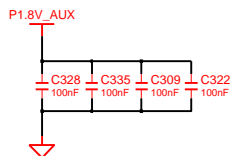
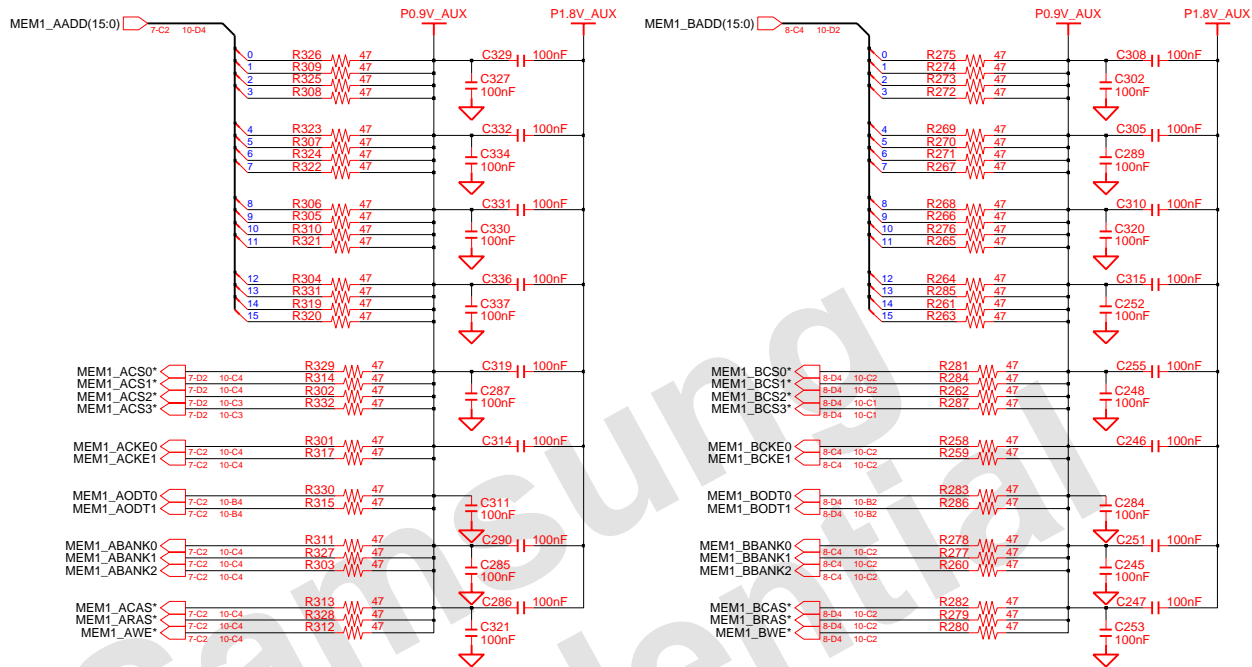
DDR1 Height : 5.2mm

DDR2 Height : 9.2mm

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	DDR2-SODIMM		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	LAST EDIT			July 5, 2006 3:50:07 PM	PAGE 10 OF 42	

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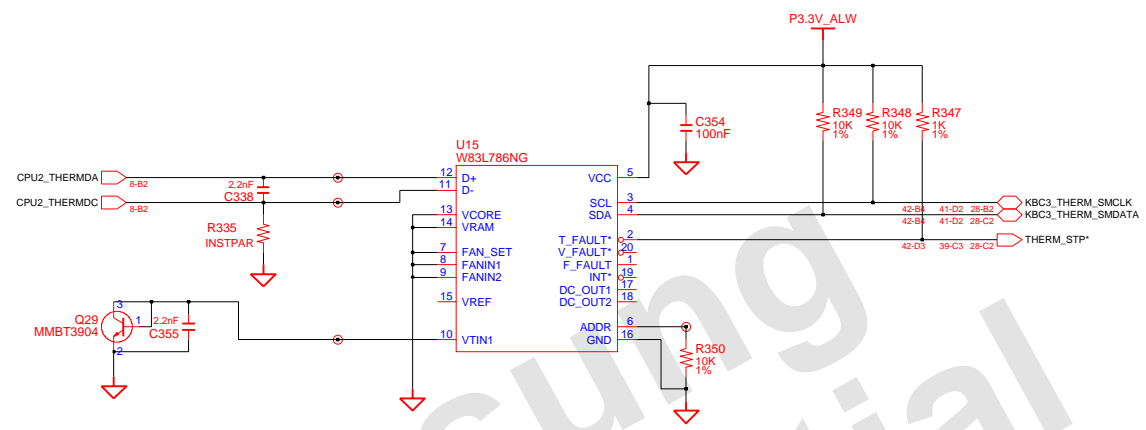
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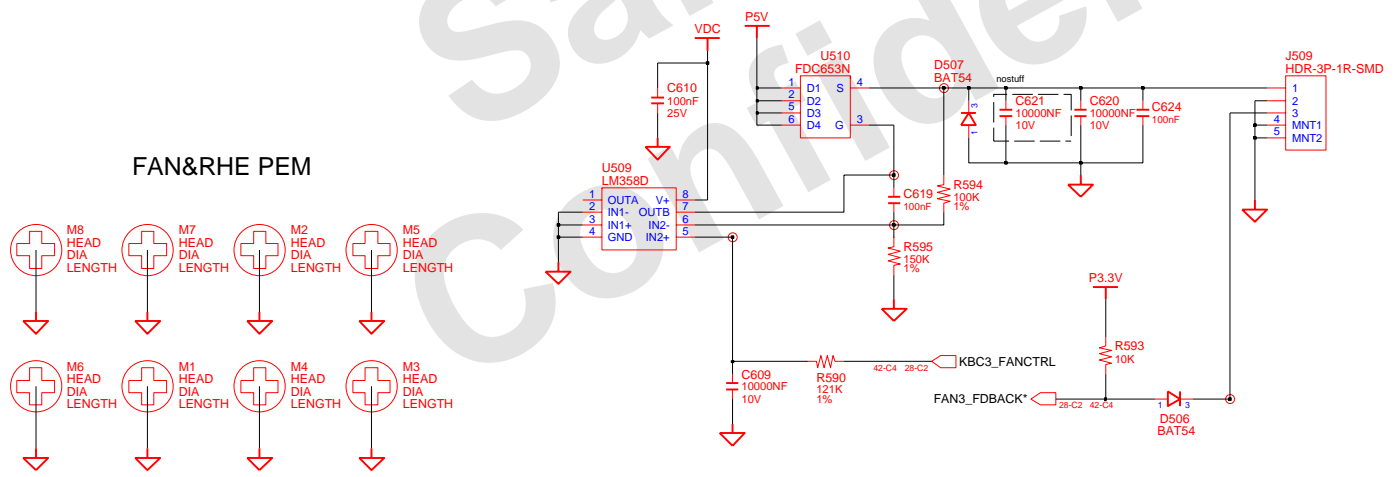
DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN DDR2 - TERMINATION	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE 11 OF 42

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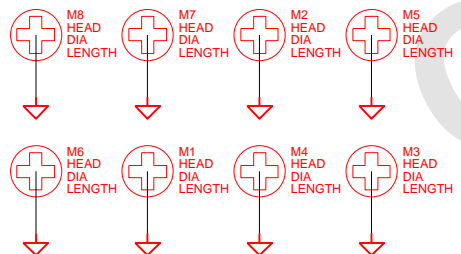
CPU/MEMORY Thermal Sensor



FAN CONTROL



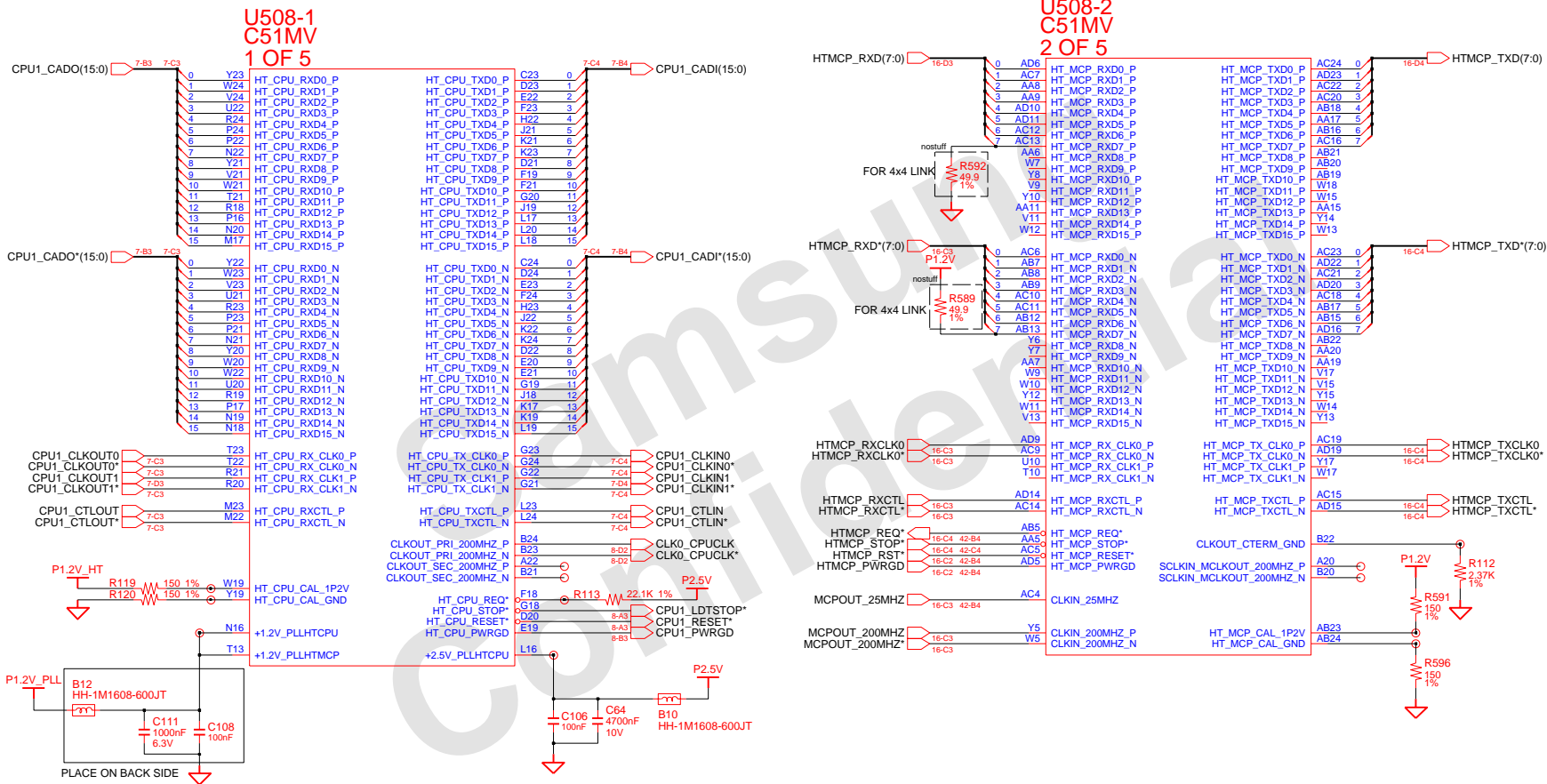
FAN&RHE PEM



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	REV	1.0	THERMAL SENSOR/FAN CTRL	PART NO.	BA41-00687A
MODULE CODE		LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	12	OF 42

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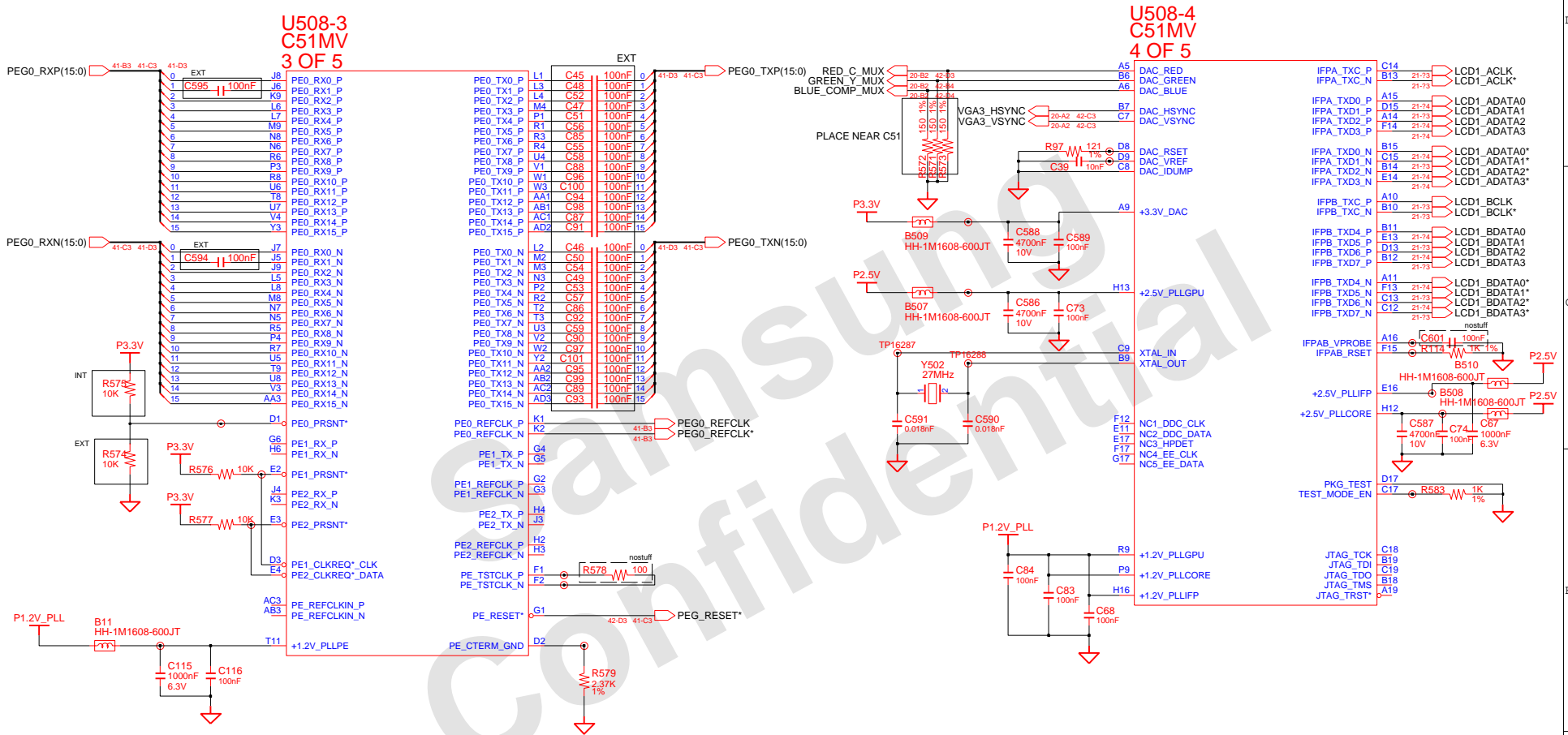
U508-1
C51MV
1 OF 5

U508-2
C51MV
2 OF 5

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN NORTH BRIDGE(1/3)	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT				July 5, 2006 3:50:07 PM PAGE 13 OF 42

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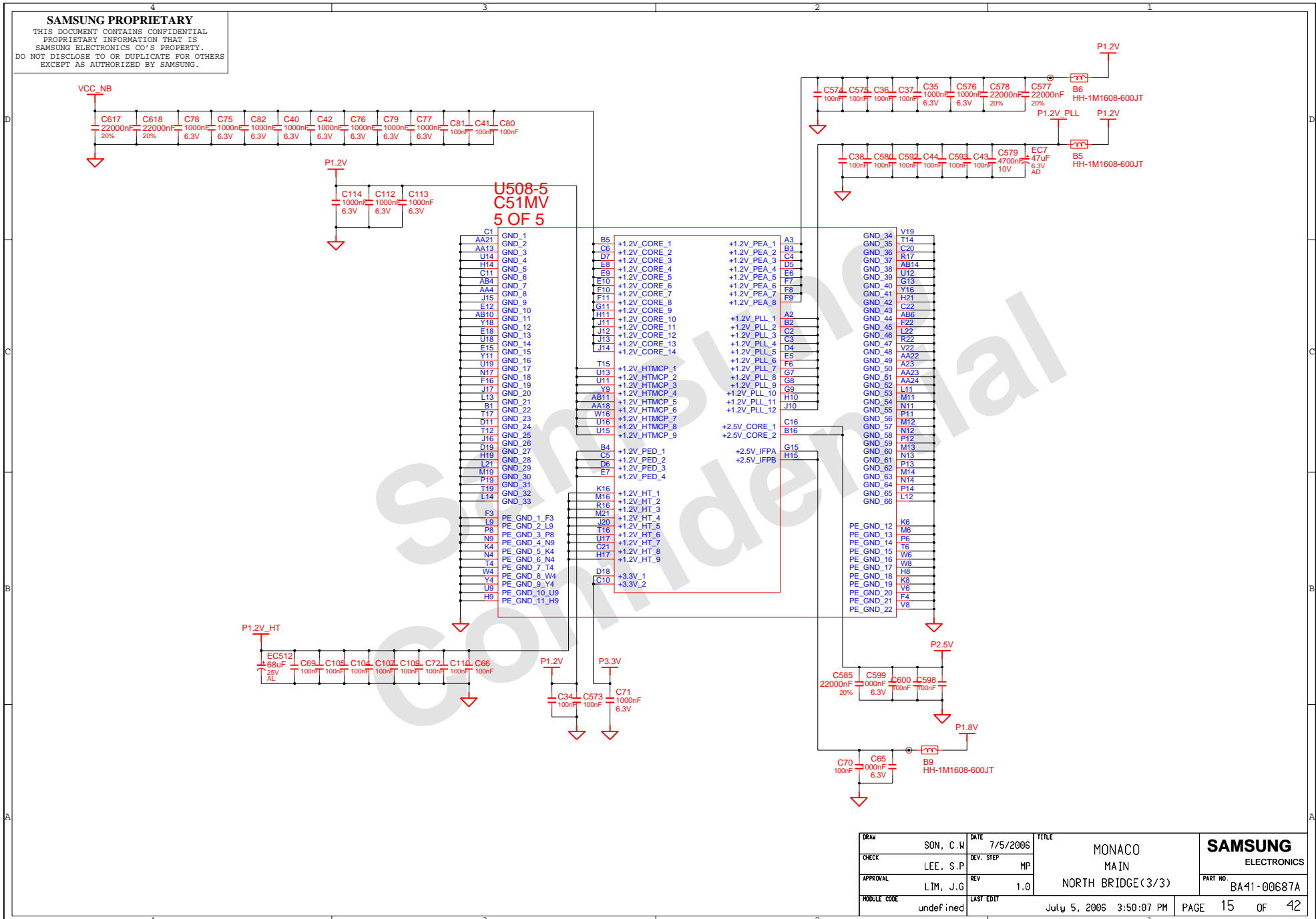
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DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	NORTH BRIDGE(2/3)	PART NO.	BA41-00687A
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	14	OF 42

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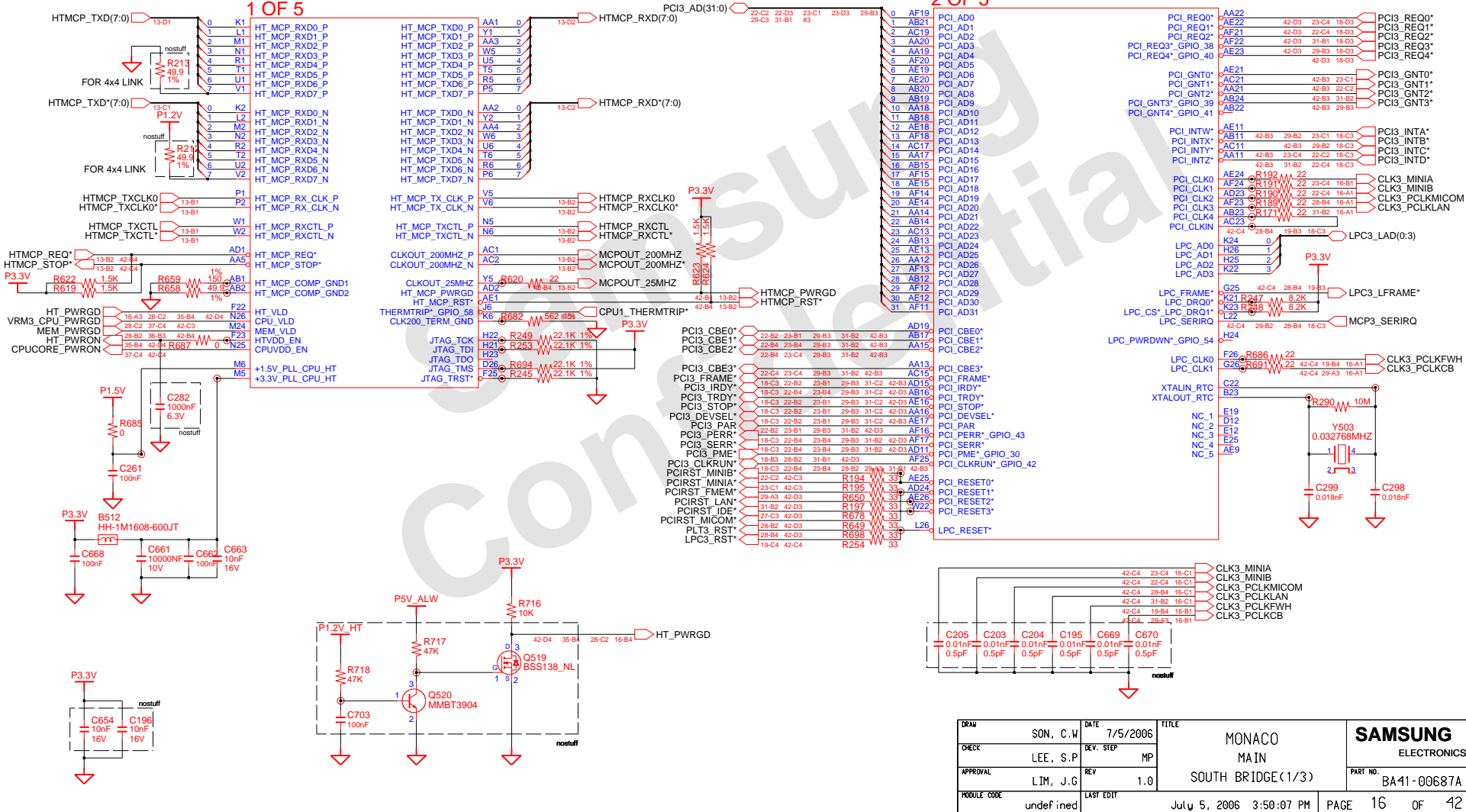
DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN NORTH BRIDGE(3/3)	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	15	OF 42

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**U517-1
MCP51M
1 OF 5**

**U517-2
MCP51M
2 OF 5**



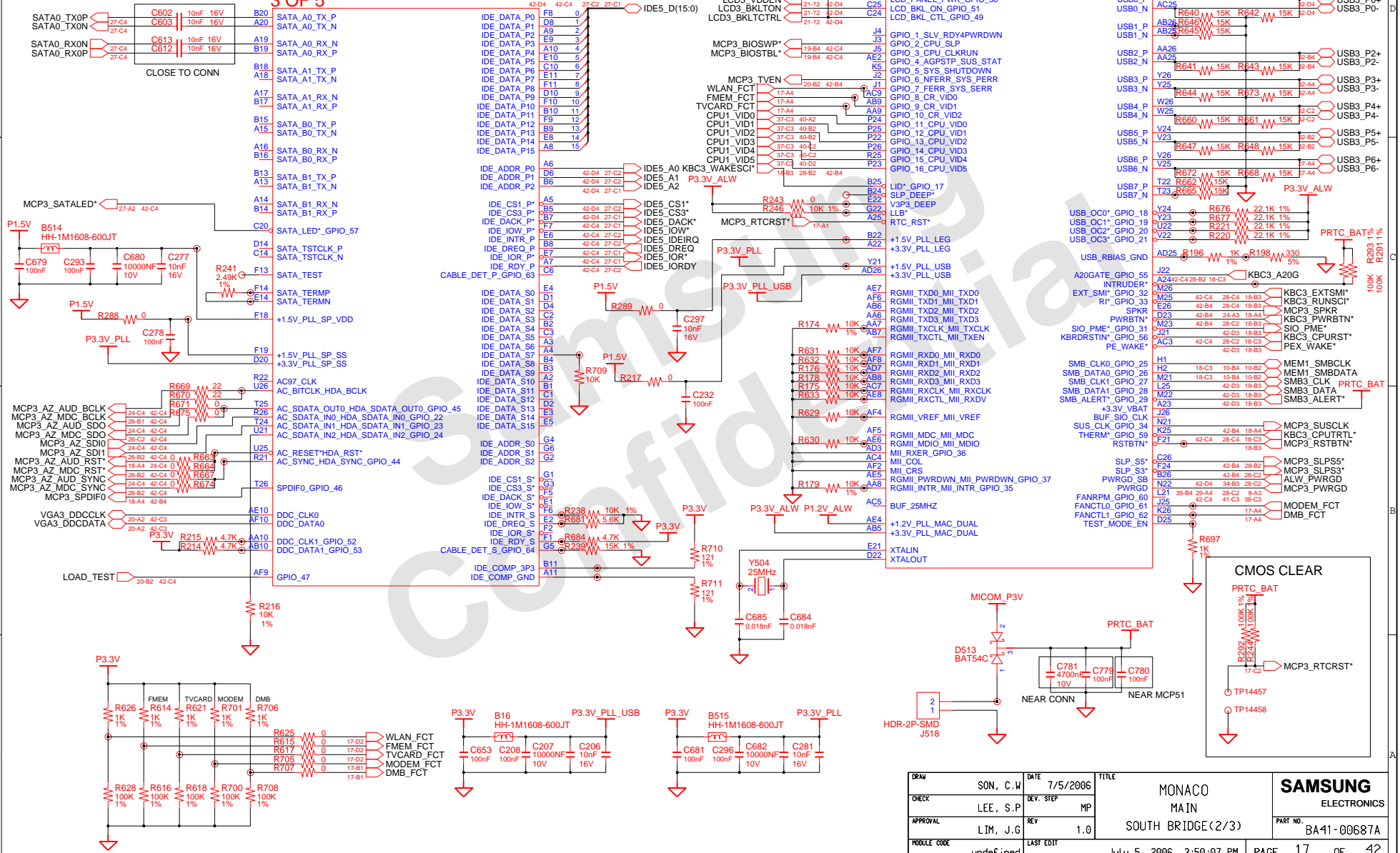
DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN SOUTH BRIDGE(1/3)	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT				
				July 5, 2006 3:50:07 PM	PAGE 16 OF 42	

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U517-3 MCP51M 3 OF 5

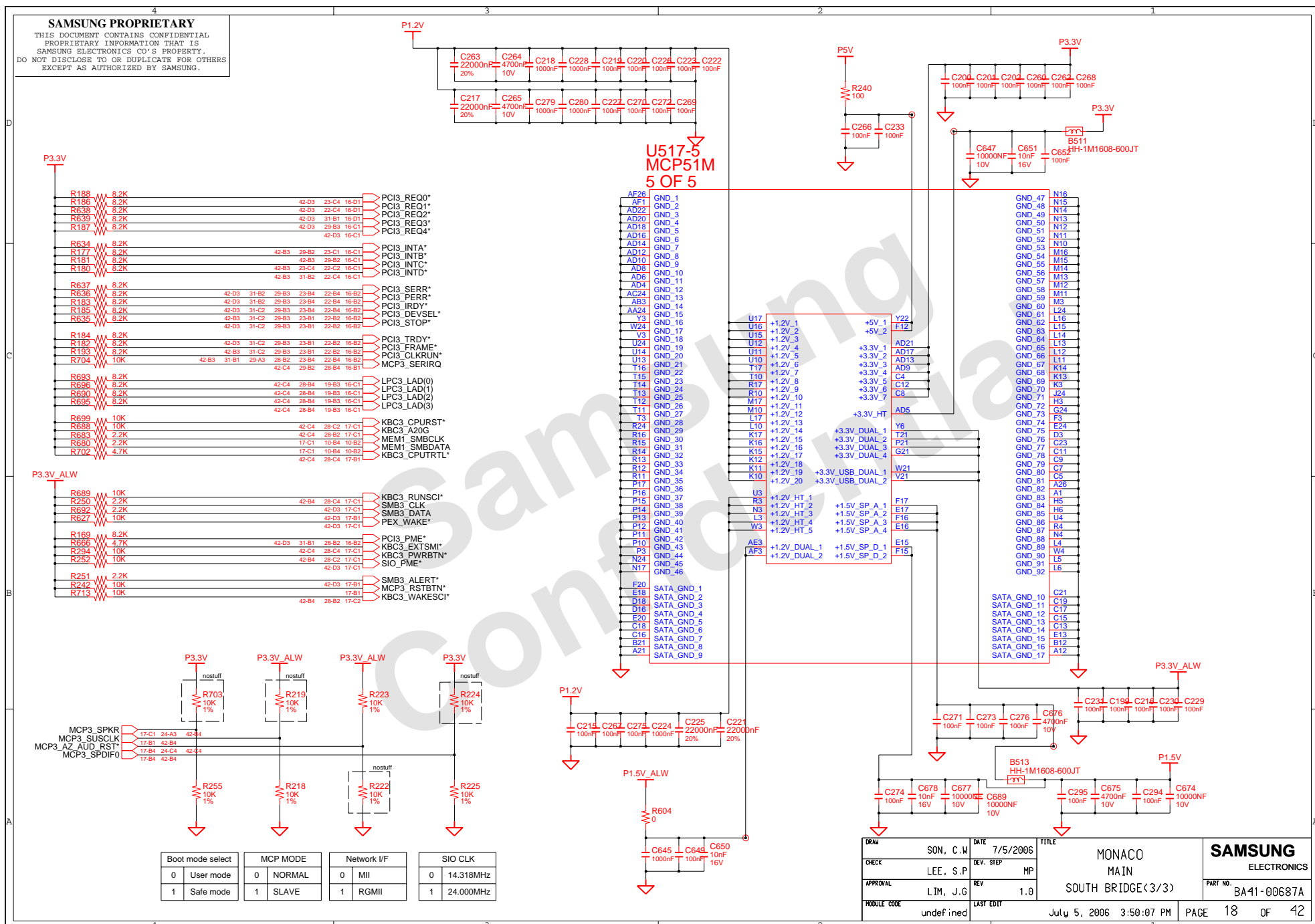
U517-4 MCP51M 4 OF 5



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN SOUTH BRIDGE(2/3)	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	17 OF 42	

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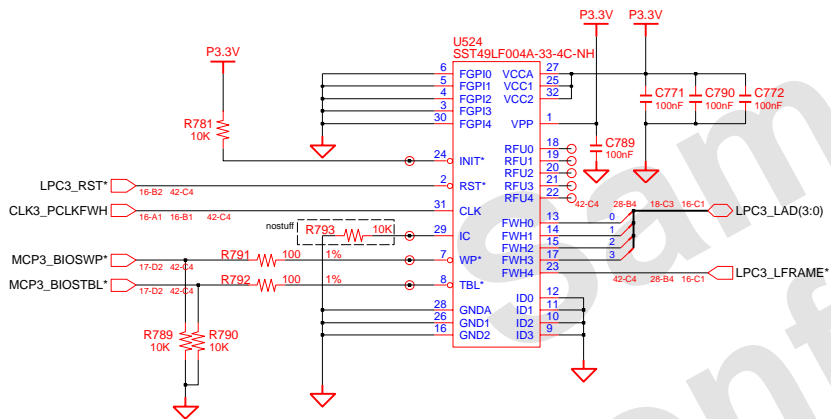


Boot mode select	MCP MODE	Network I/F	SIO CLK
0 User mode	0 NORMAL	0 MII	0 14.318MHz
1 Safe mode	1 SLAVE	1 RGMII	1 24.000MHz

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	SOUTH BRIDGE(3/3)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	18	OF 42

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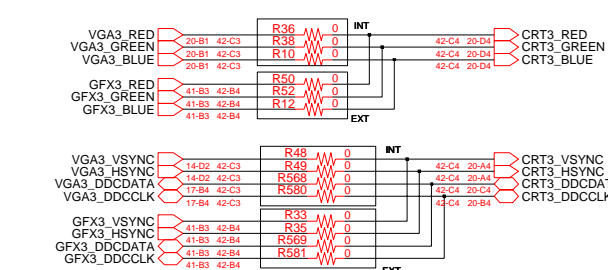
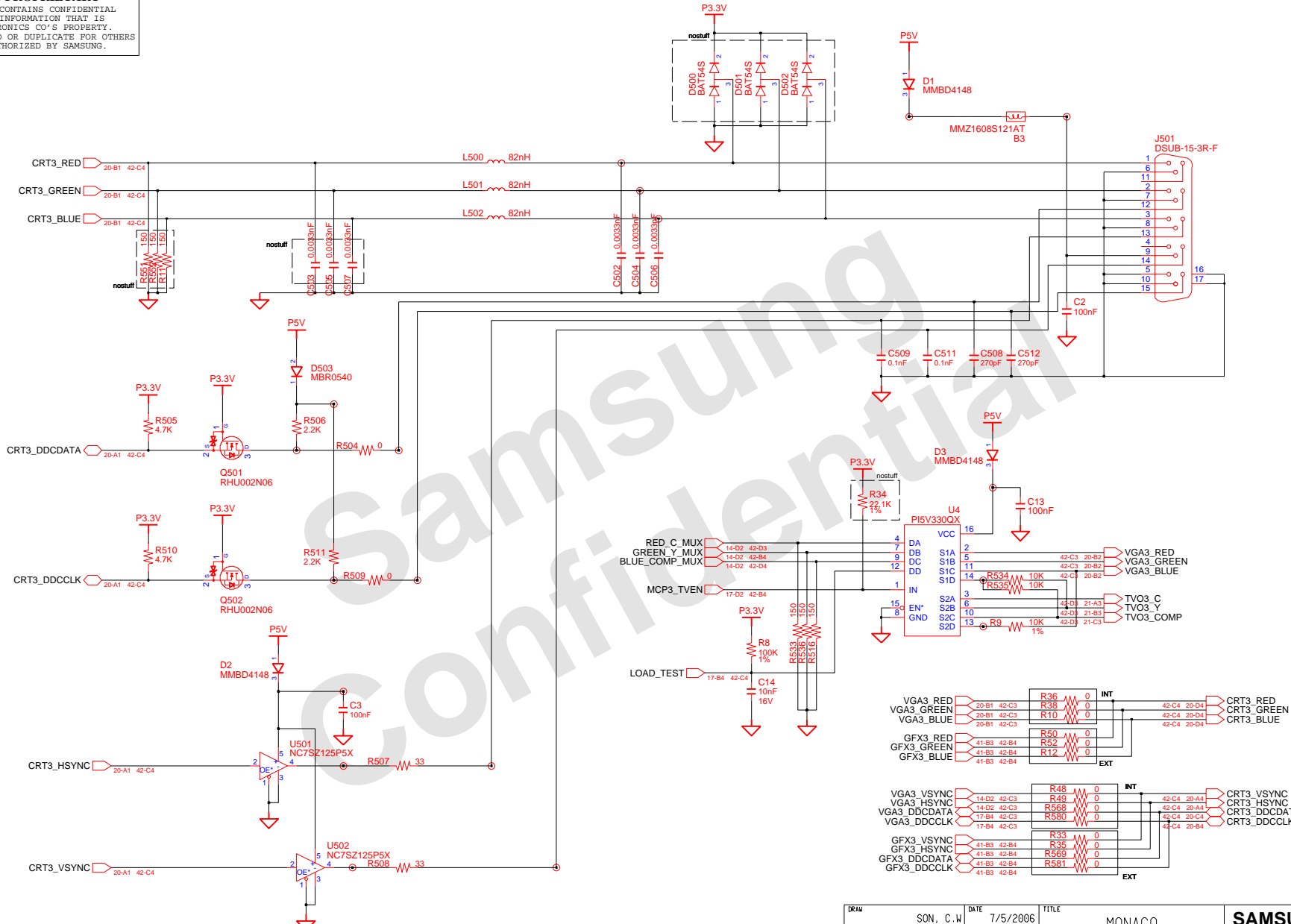


- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INITIALIZE SYSTEM H/W
- 08 INITIALIZE CHIPSET REGISTERS
- 09 SET IN POST FLAG
- 0A INIT CPU REGISTERS
- 0B CPU CACHE ON
- 0C INITIALIZE CACHE TO POST
- 0E INITIALIZE I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INITIALIZE POWER MANAGER
- 11 LOAD ALTERNATE REGISTERS
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INITIALIZE KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 INITIALIZE 8254 TIMER
- 1A INITIALIZE 8237 DMA CONTROLLER
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REGISTERS TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TEST CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REGISTERS
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INITIALIZE INTERRUPT VECTOR
- 44 INITIALIZE BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INITIALIZE I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INITIALIZE PCI BUS AND DEVICE
- 4A INITIALIZE ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY * PRESS SETUP*
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1
- 66 CONFIGURE ADVANCE CACHE REGISTERS
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD ERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT. RS232C
- 84 DETECT AND INSTALL EXT. PARALLEL
- 86 RE-INITIALIZE ON-BOARD I/O PORT
- 88 INITIALIZE BIOS DATA ROM
- 8A INITIALIZE EXTENDED BIOS DATA AREA
- 8C INITIALIZE FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INITIALIZE TYPEMATRIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INITIALIZE HDD CONTROLLER
- 91 INITIALIZE LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	MAIN		
APPROVAL	LIM, J.G	REV	1.0	FWH		PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	19	OF 42

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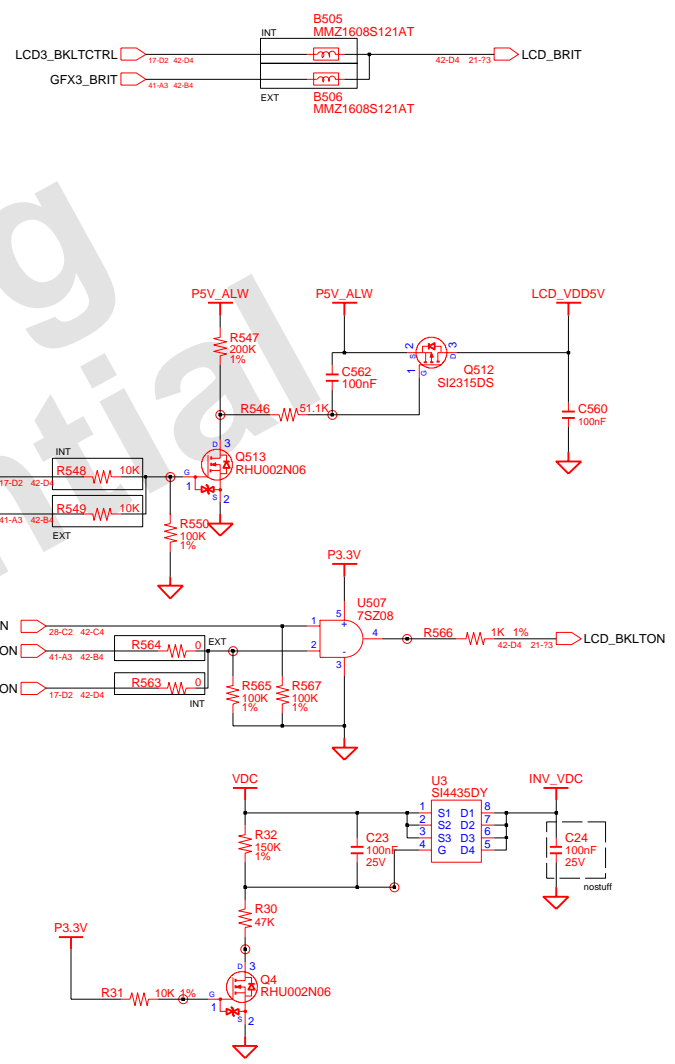
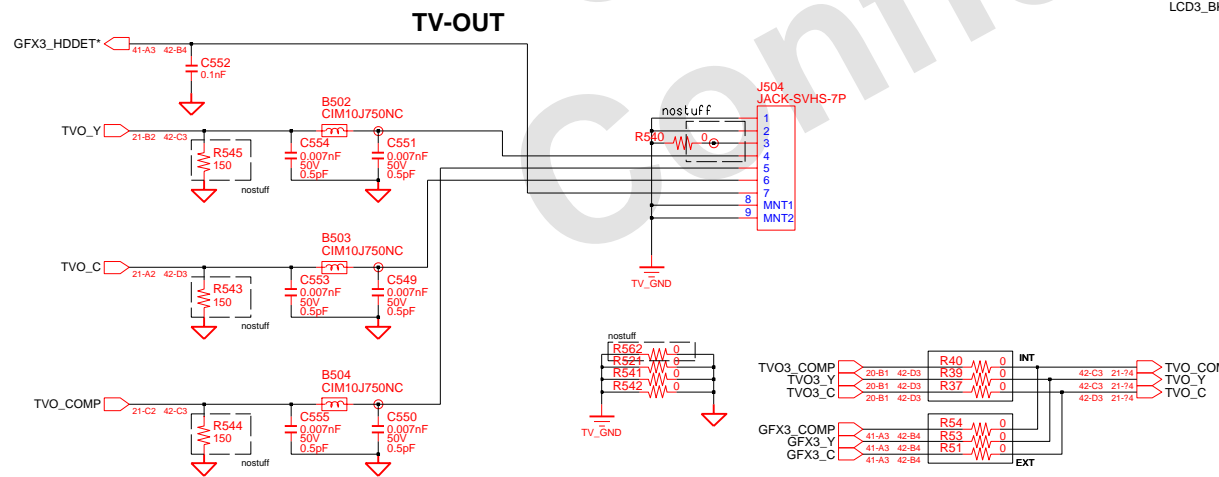
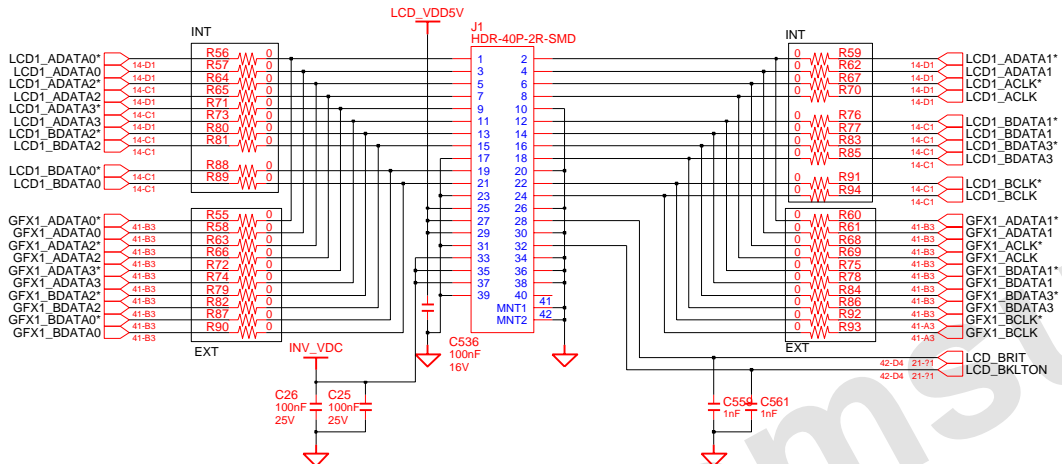


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	20	OF 42

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LCD CONNECTOR

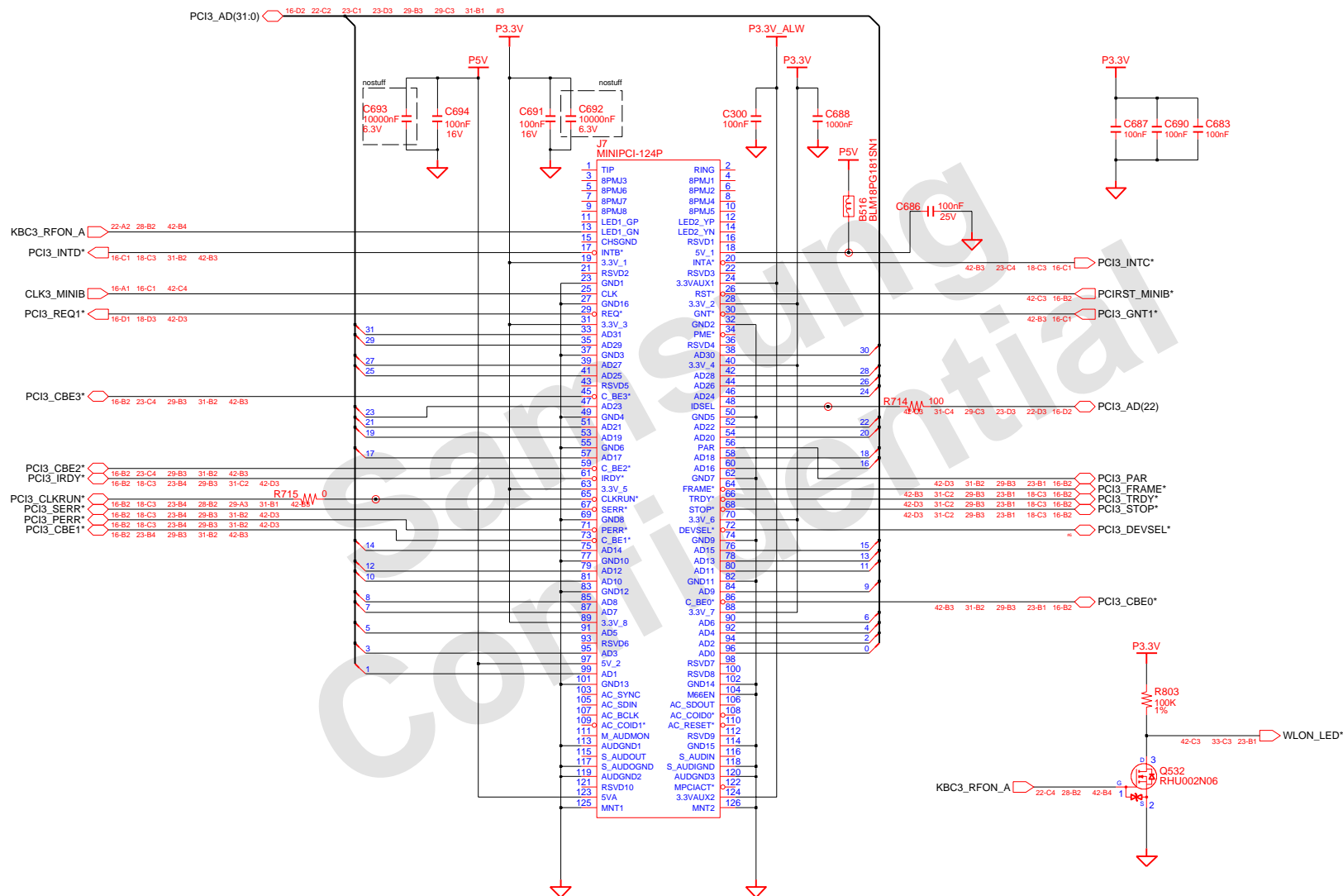


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN LCD / TV-OUT	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	21 OF 42	

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FOR WIRELESS LAN

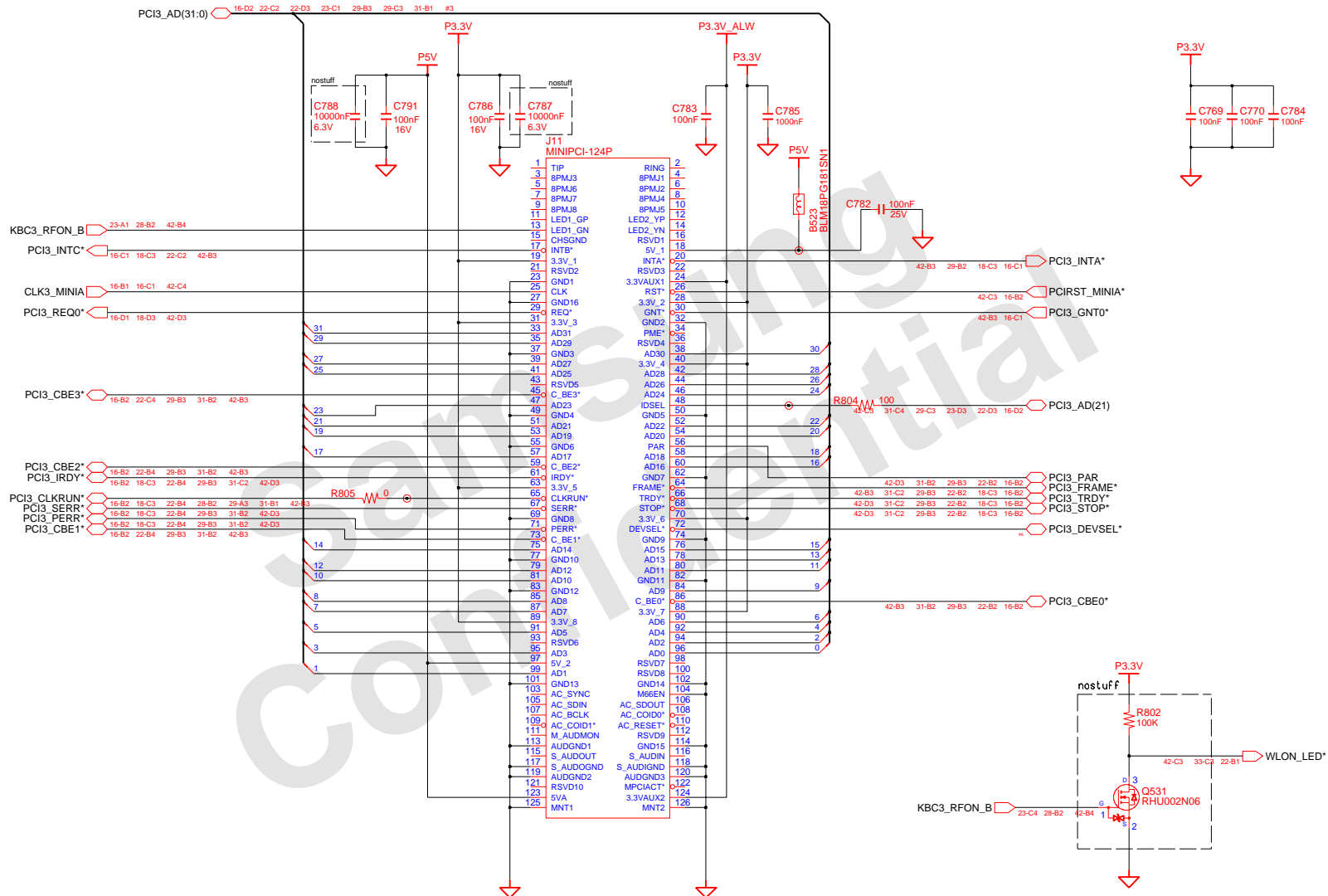


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN MINI PCI A	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	22	OF 42

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FOR TV CARD(OPTION)



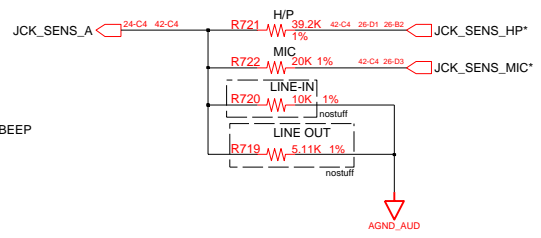
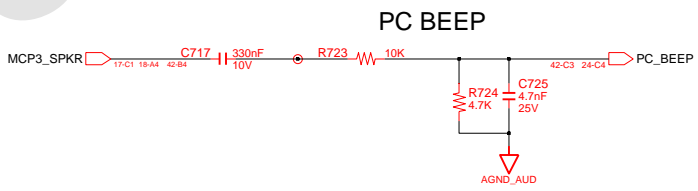
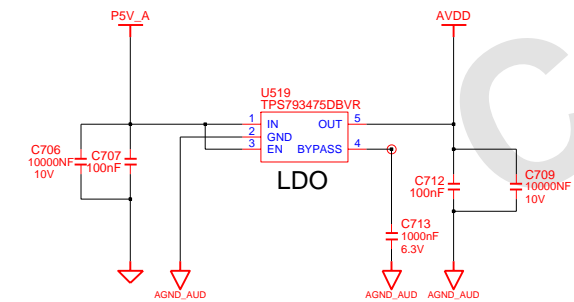
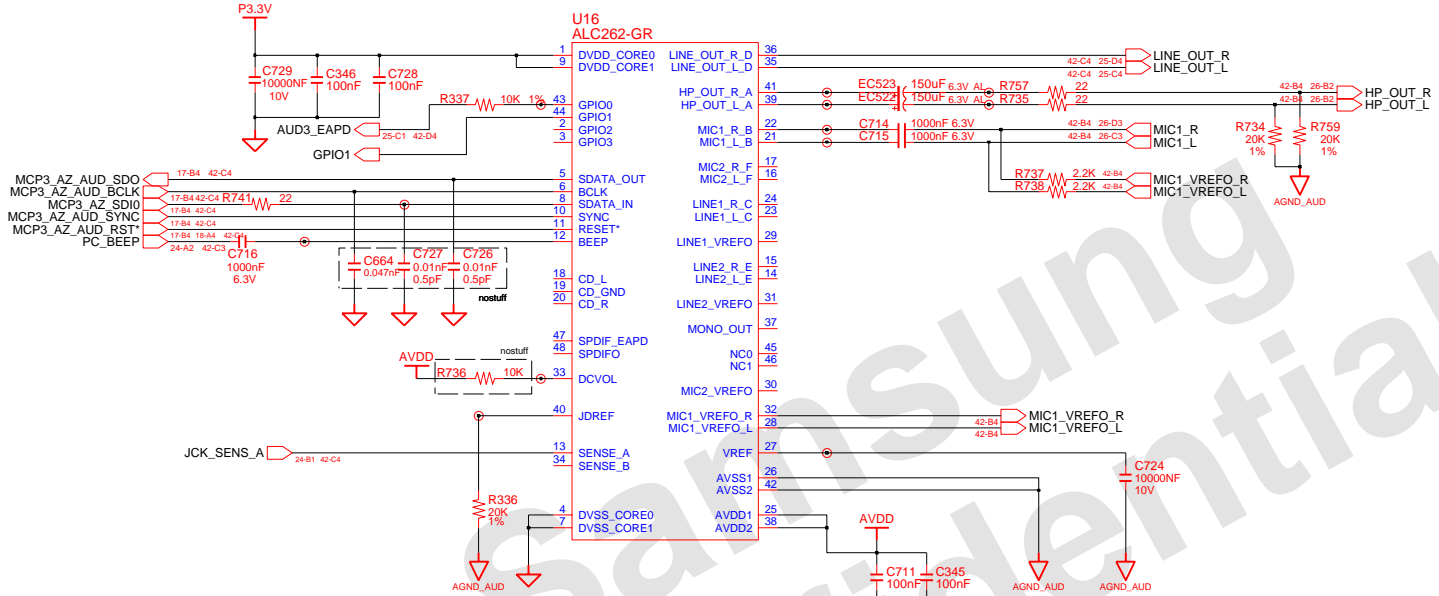
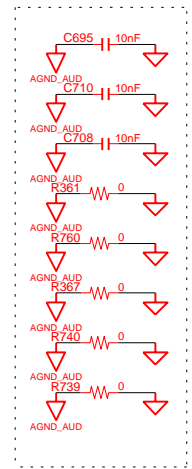
DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN MINI PCI B	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	23	OF 42

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- 1. AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3. AGND_MIC IS MIC GROUND
- 4. AGND_CHS IS CHASSIS GROUND

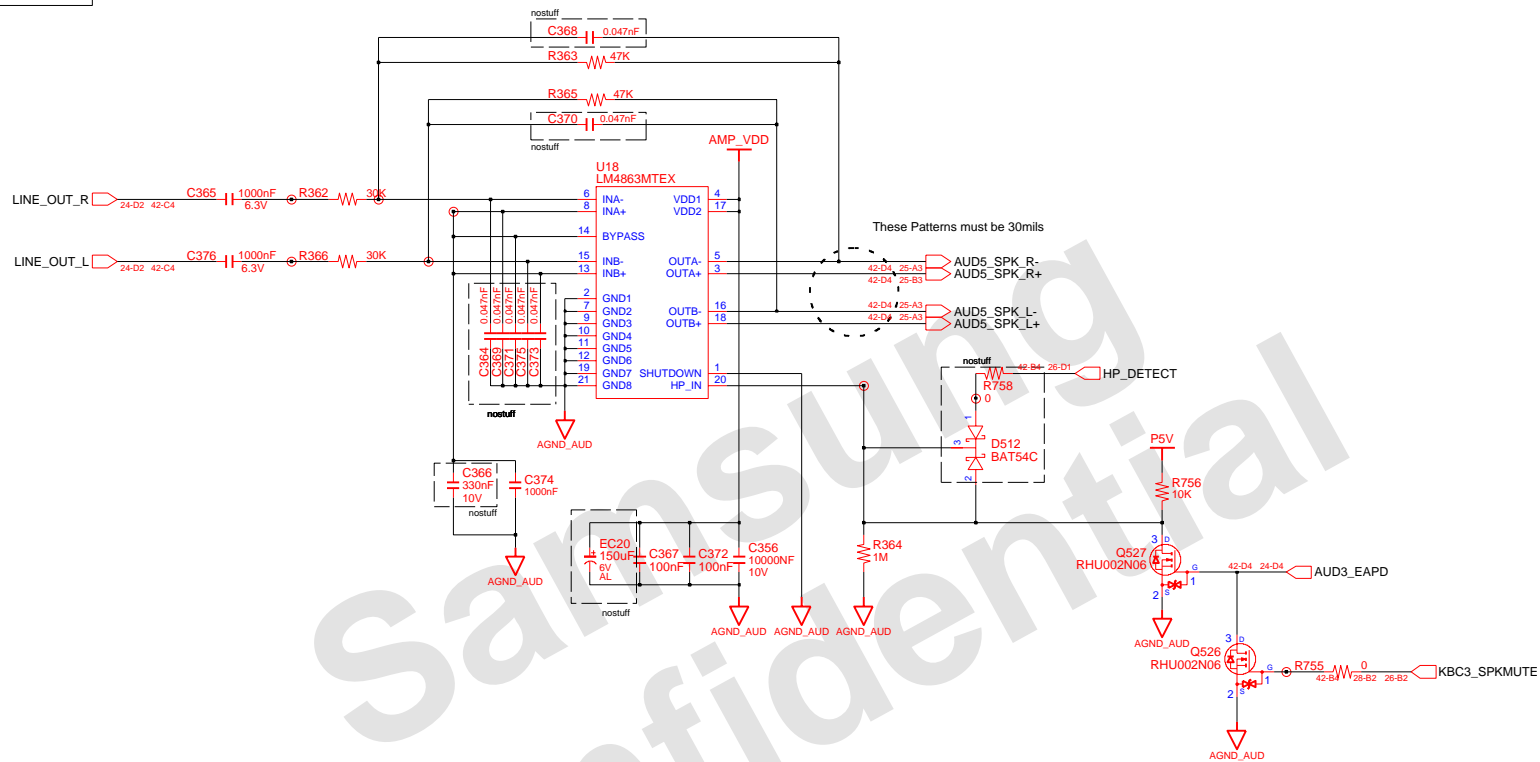
ALL TYPE IS 1608



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	24 OF 42	

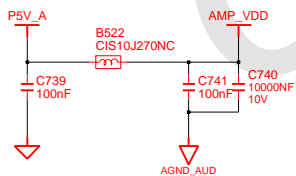
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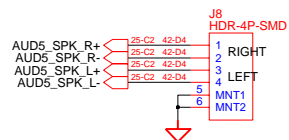


These Patterns must be 30mils

AMP_VDD



INTERNAL STEREO SPEAKERS



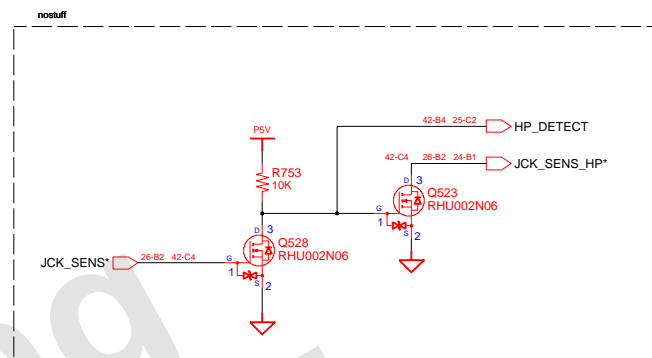
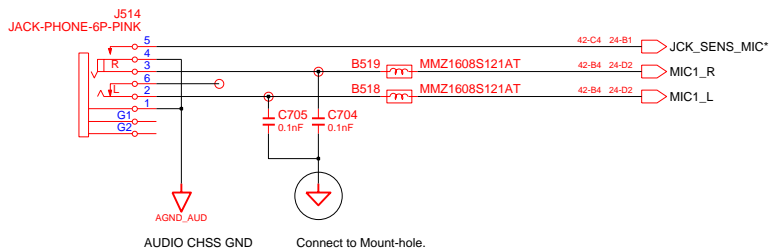
Should be written sign "L", "R" on the PCB

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN AUDIO AMP	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	25 OF 42	

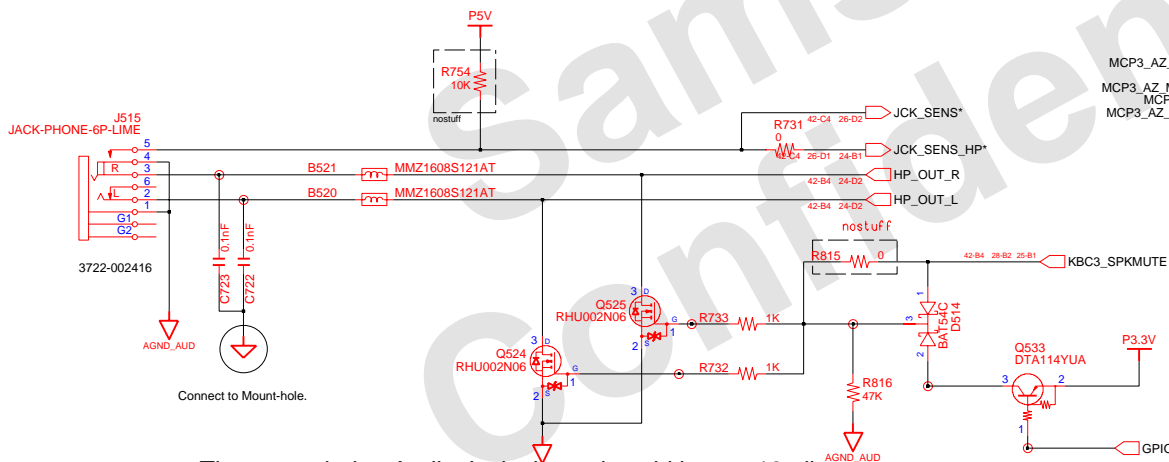
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MIC JACK

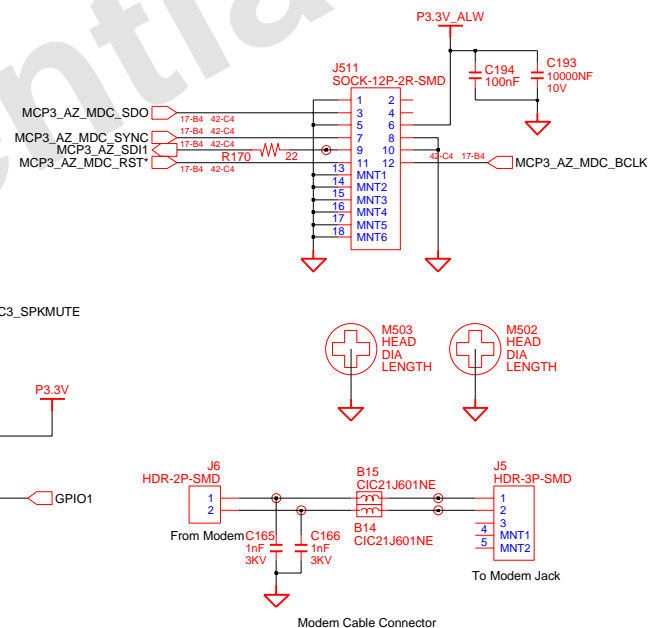


HEADPHONE



The traces led to Audio Jacks have the width over 10mil

MDC Connector

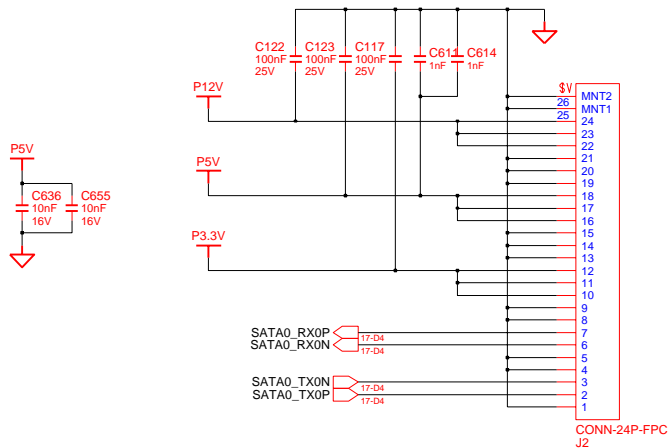


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN AUDIO / MDC CONN	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	26 OF 42	

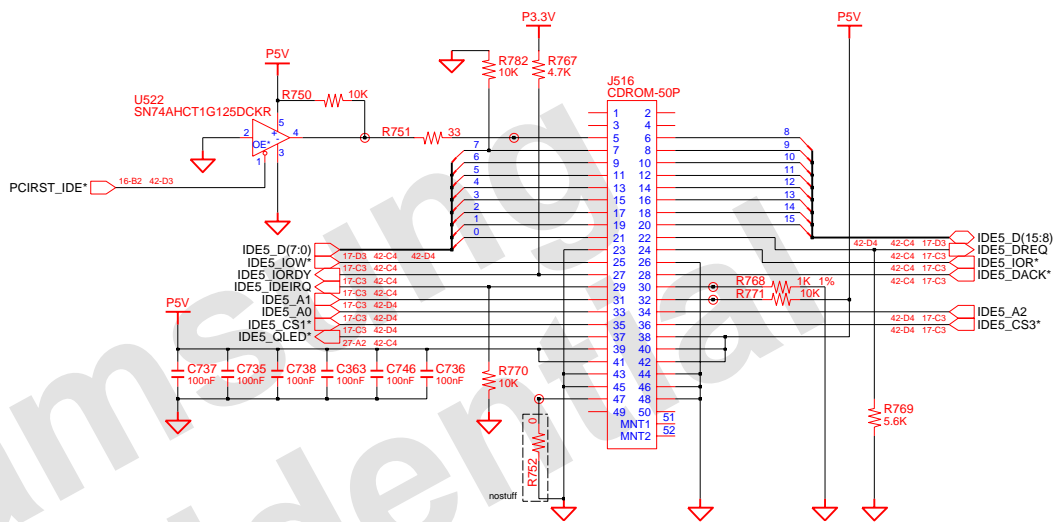
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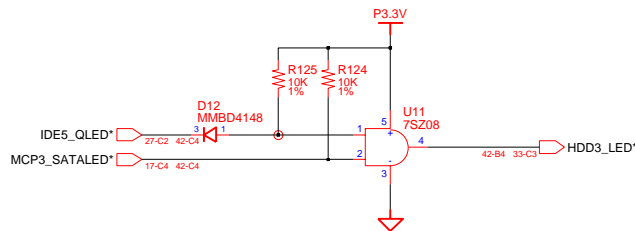
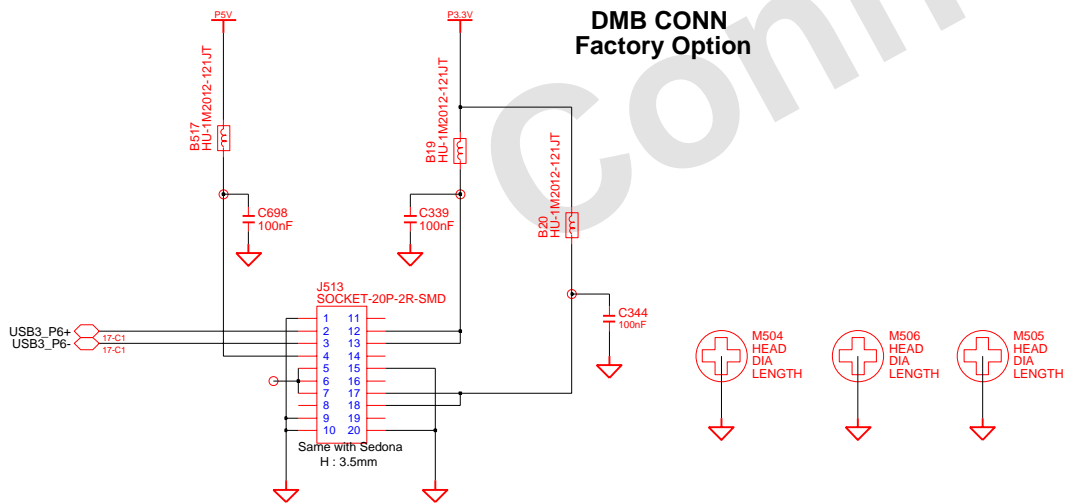
HDD CONN



CD CONN



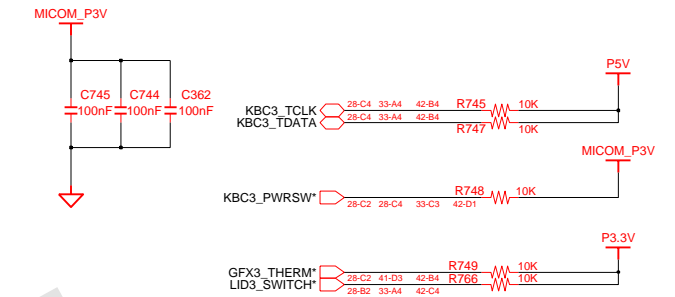
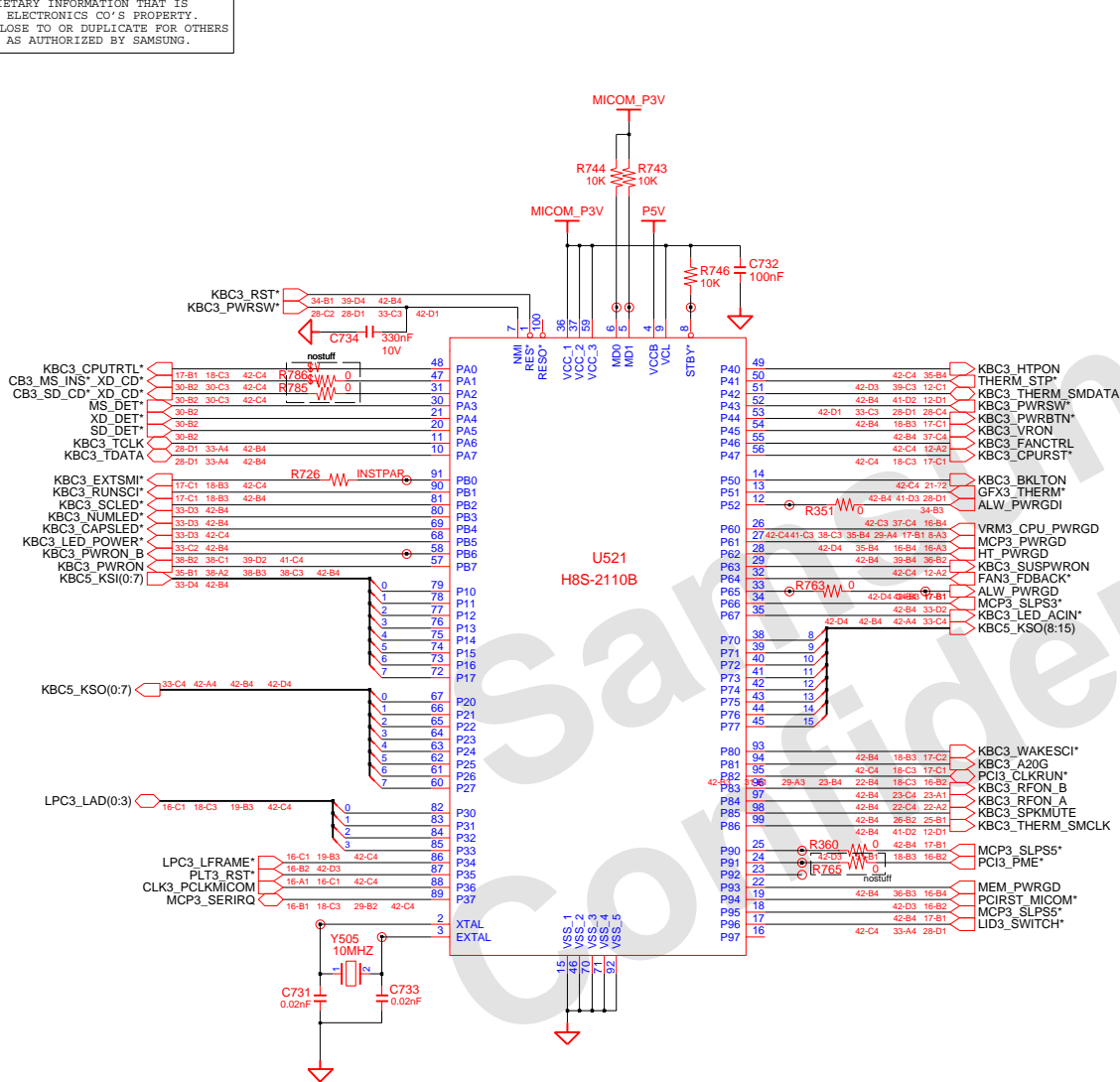
**DMB CONN
Factory Option**



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	HDD / ODD / DMB		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	27	OF 42

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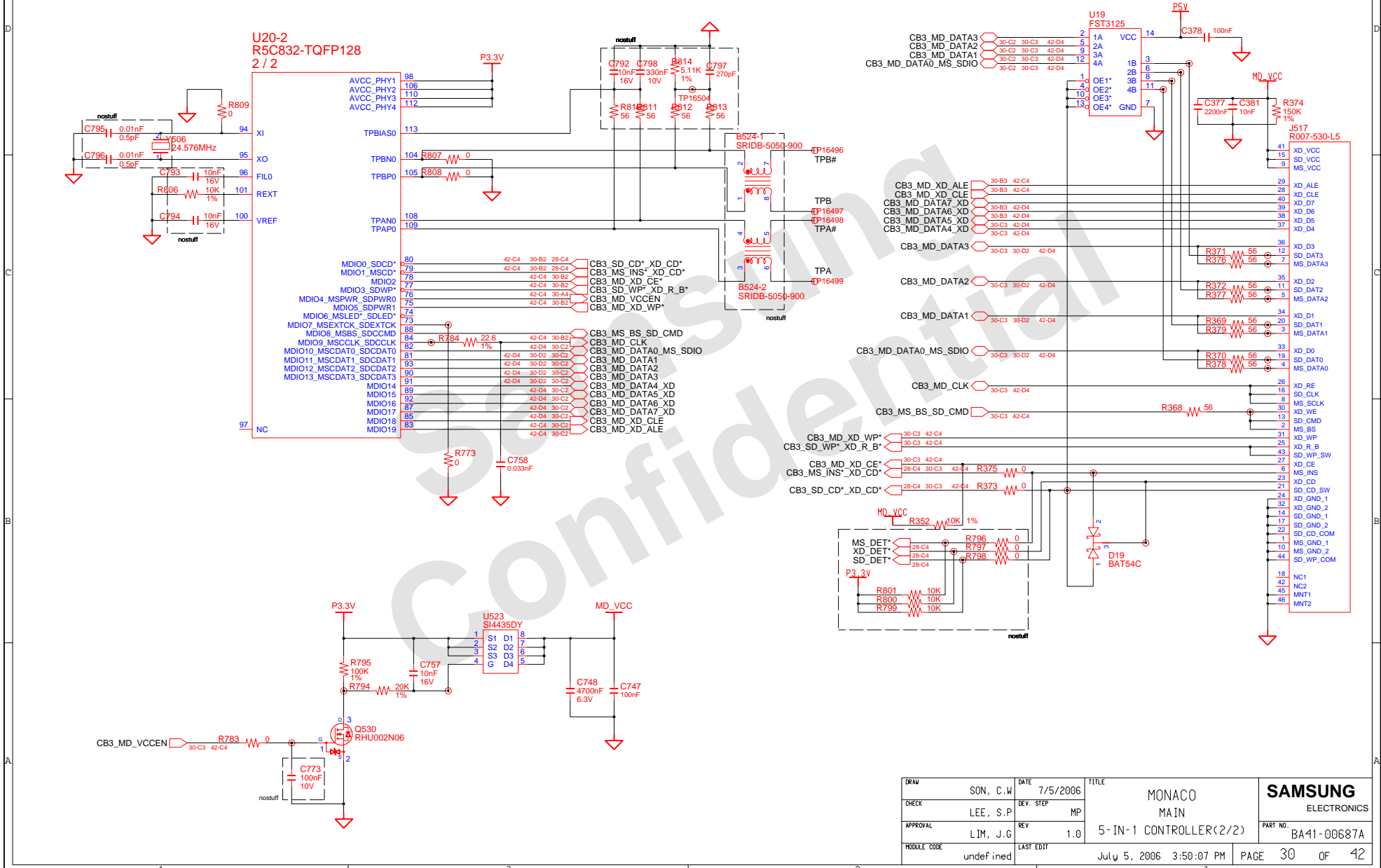
MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN MICOM	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			PART NO. BA41-00687A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	28	OF 42

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OPTION

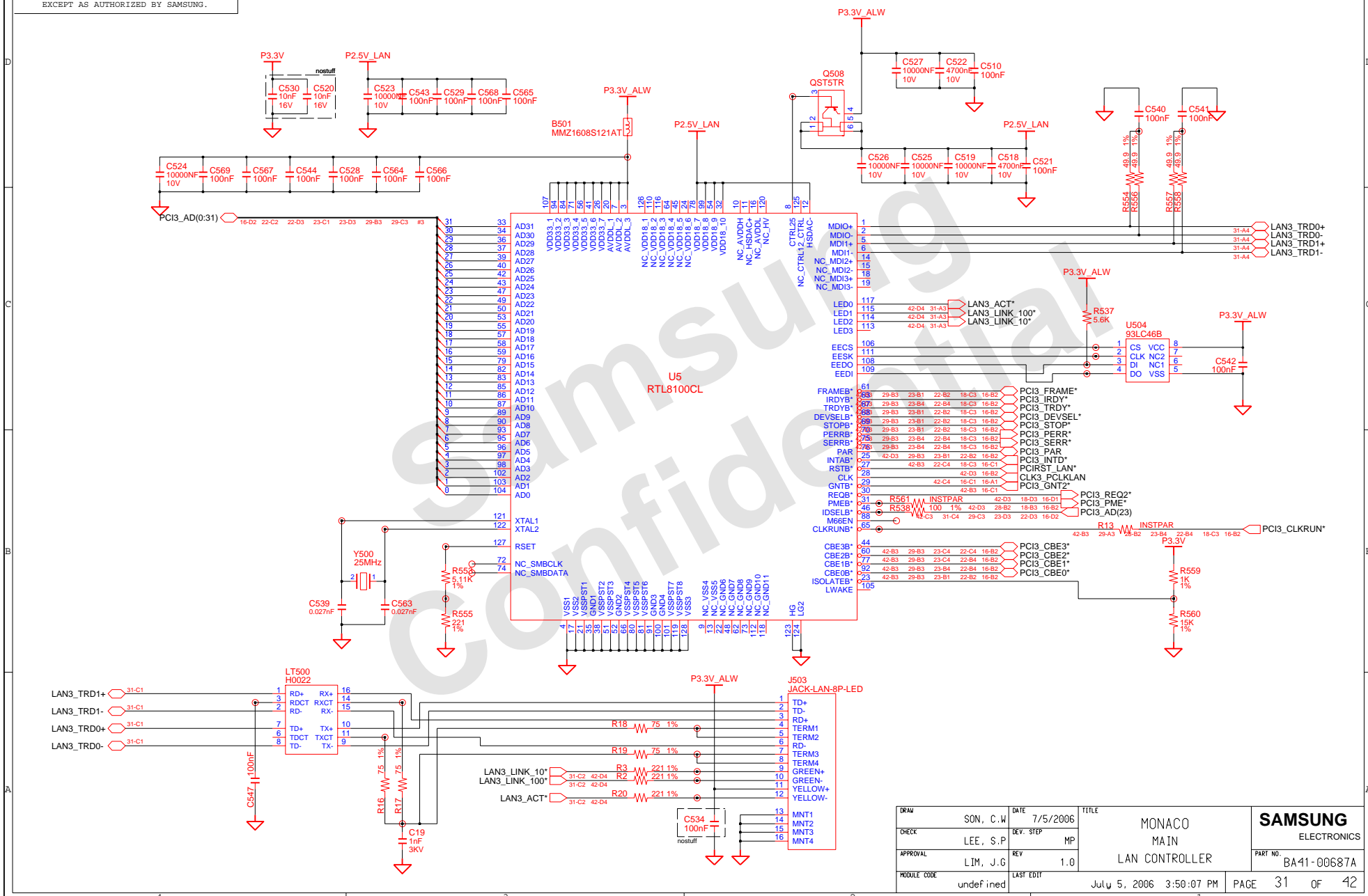


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	5-IN-1 CONTROLLER(2/2)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	30	OF 42

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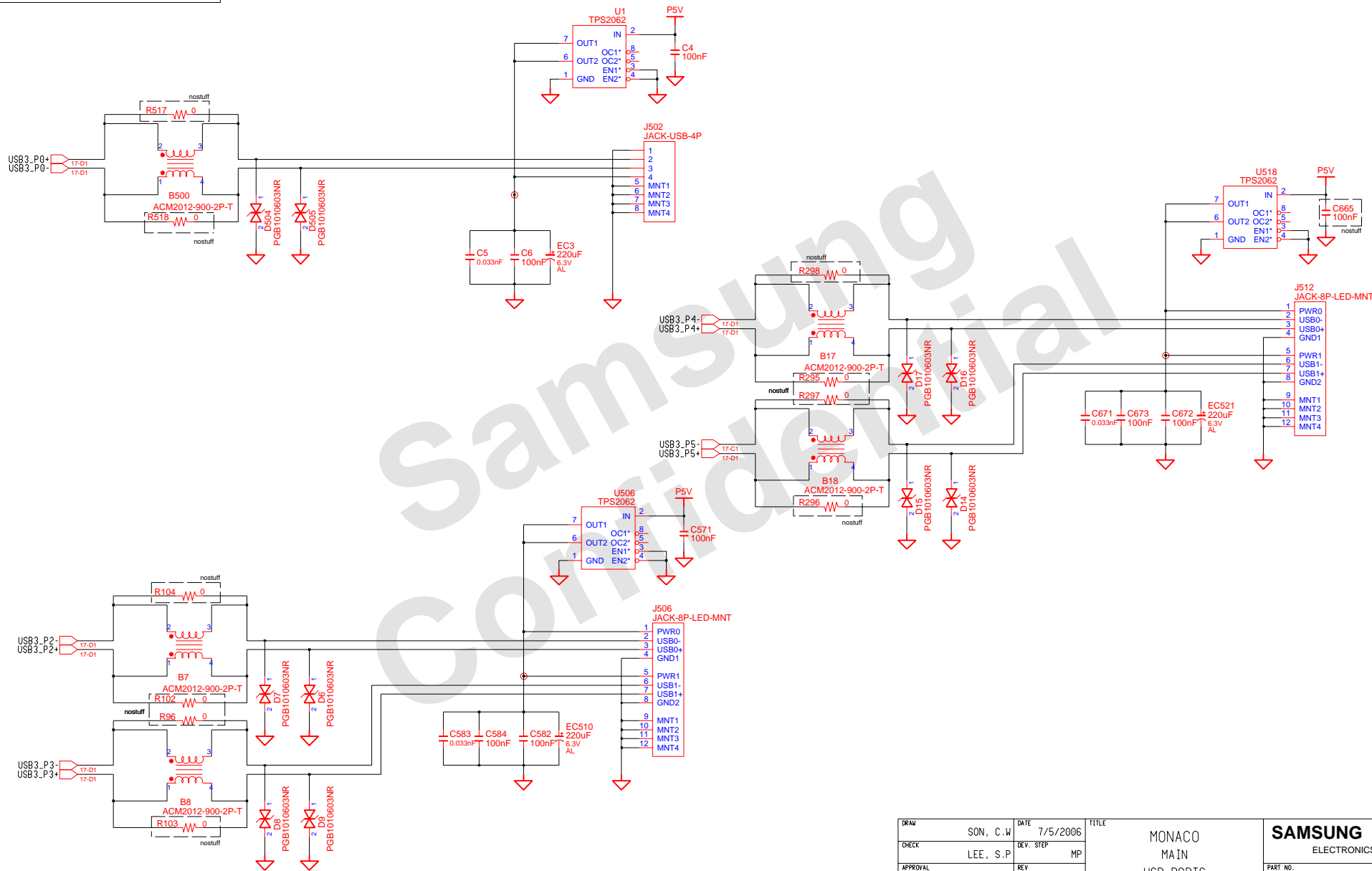
LAN Controller (Only 10/100M)



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			PART NO. BA41-00687A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	31	OF 42

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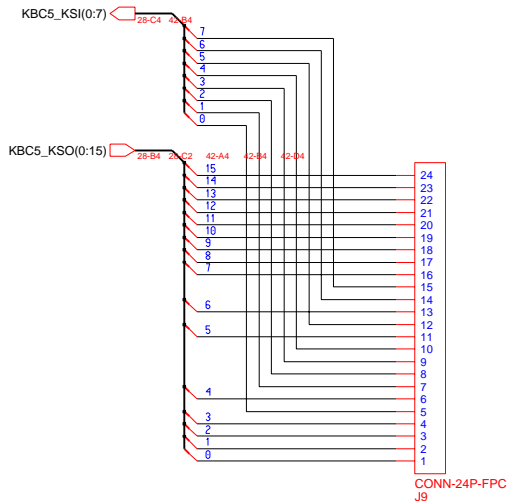


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN USB PORTS	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	32 OF 42	

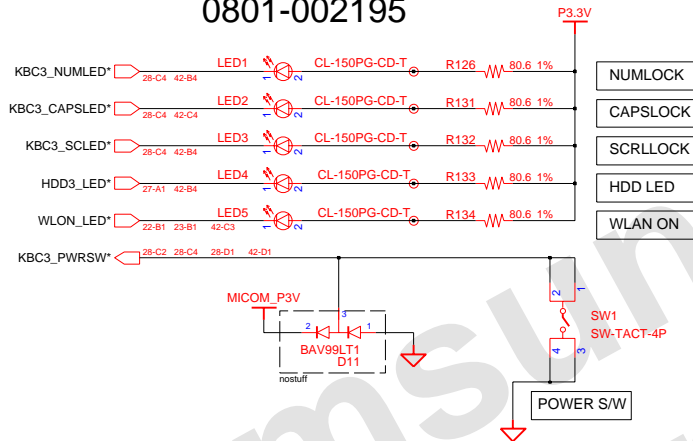
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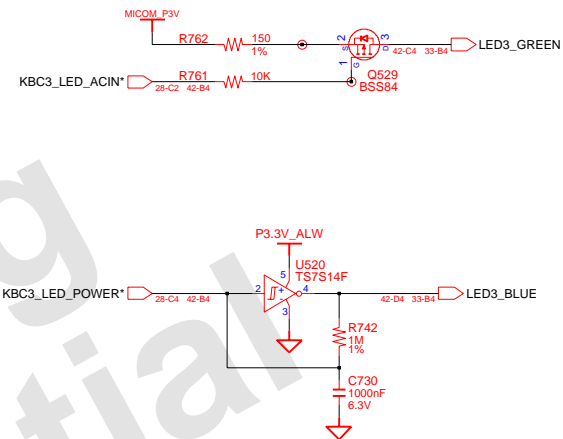
KEYBOARD



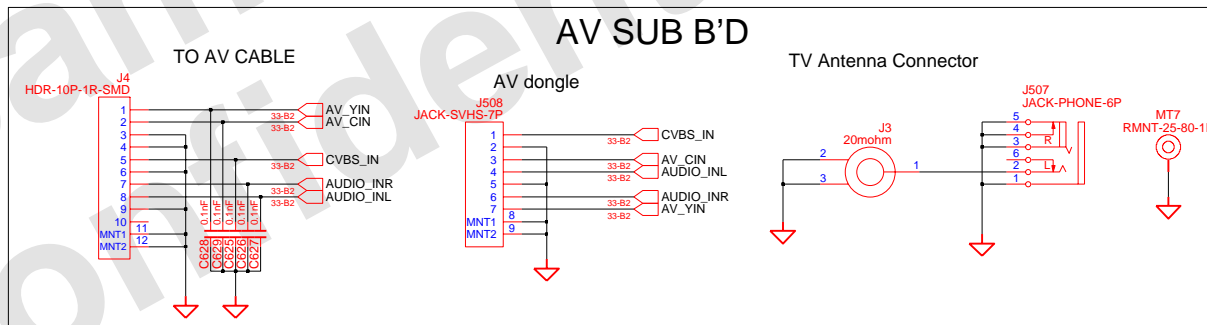
LED
0801-002195



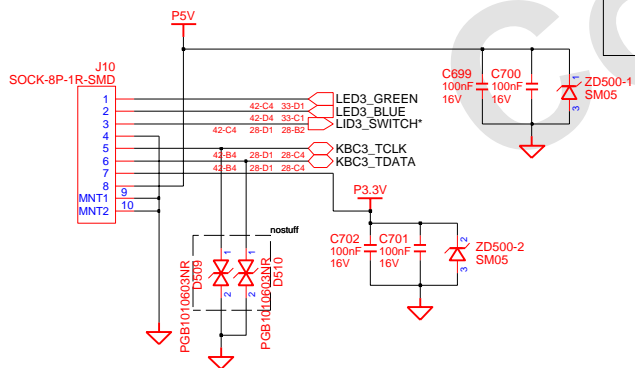
ADAPTERIN/CHARGING LED



AV SUB B'D



TOUCH PAD

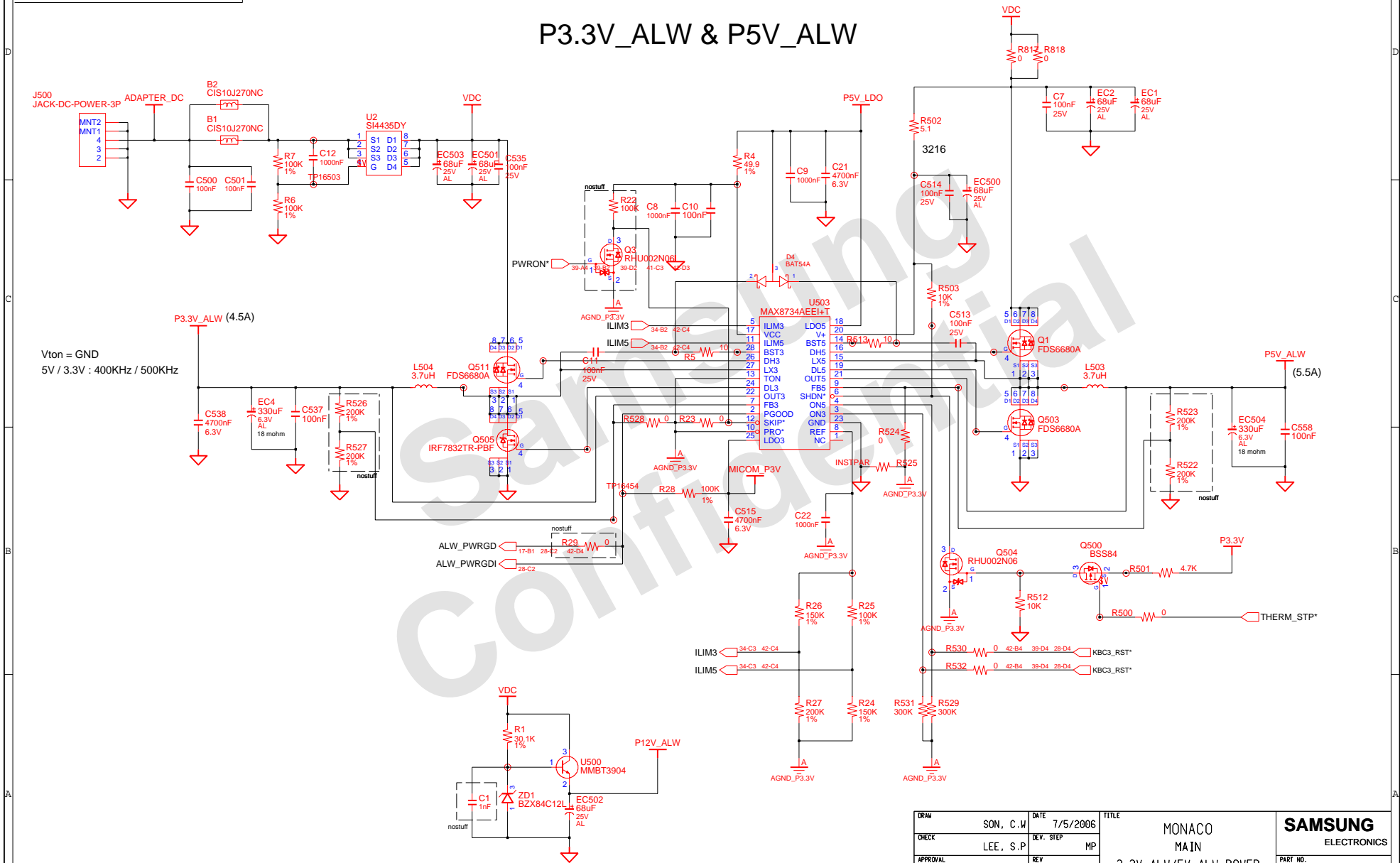


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	KBD/TPAD/LED/SW		
APPROVAL	LIM, J.G	REV	1.0	PART NO.		BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	33	OF 42

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P3.3V_ALW & P5V_ALW

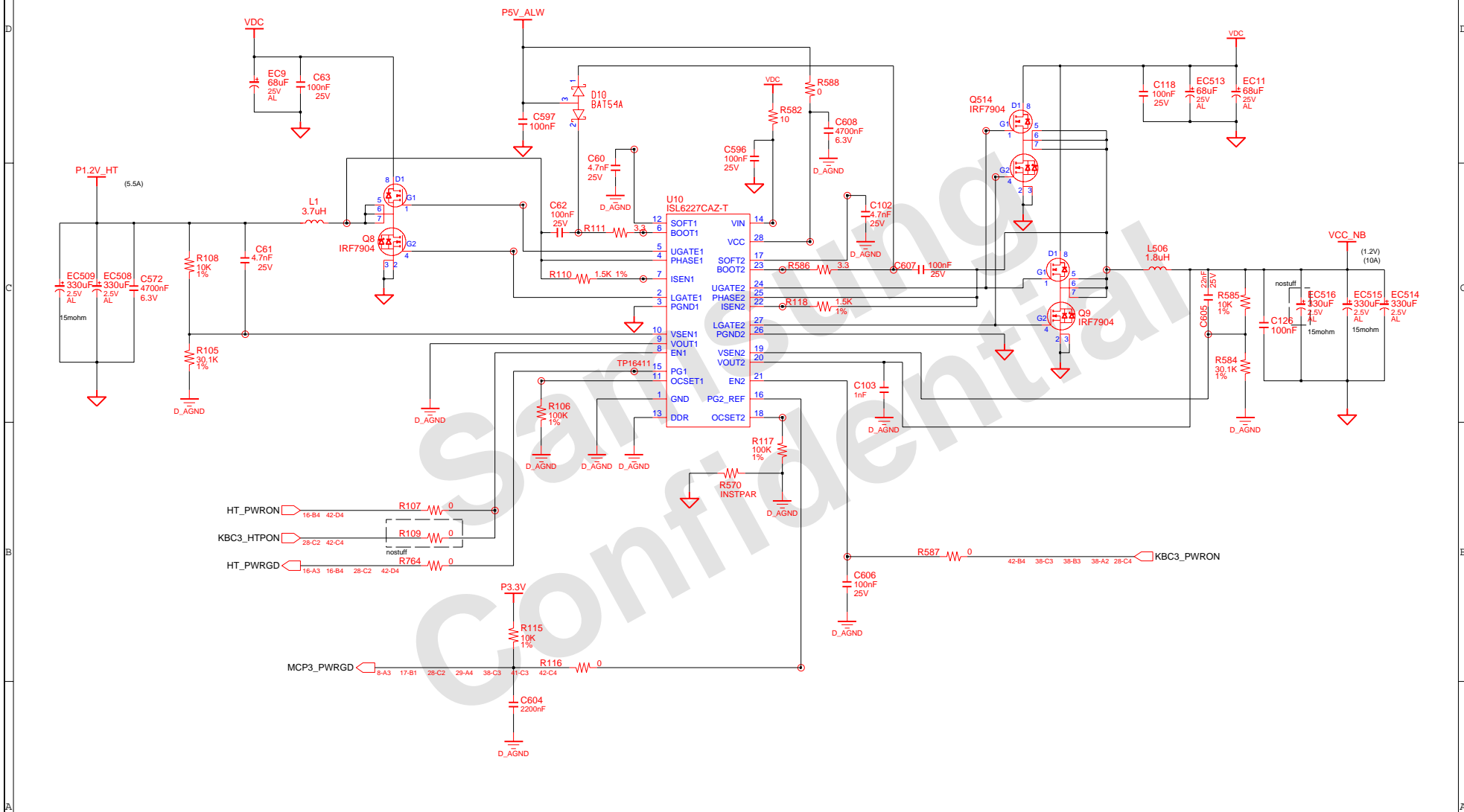


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	3.3V_ALW/5V_ALW POWER		
APPROVAL	LIM, J.G	REV	1.0	PART NO. BA41-00687A		PAGE 34 OF 42
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM			

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VCC_NB & P1.2V_HT

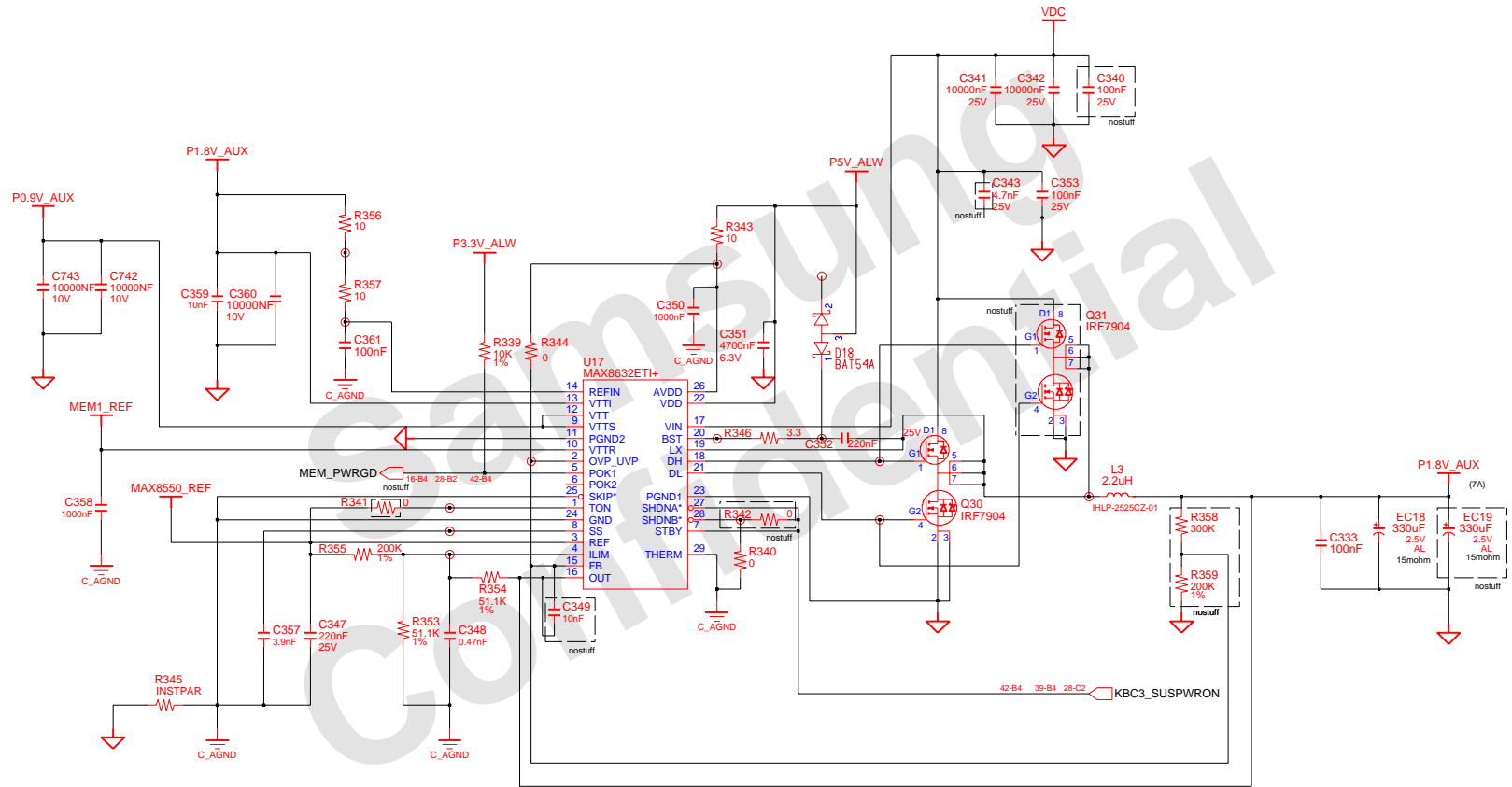


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	VCC_NB / 1.2V_HT POWER	PART NO. BA41-00687A	
APPROVAL	LIM, J.G	REV	1.0	July 5, 2006 3:50:07 PM	PAGE	35 OF 42
MODULE CODE	undef ined	LAST EDIT				

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DDR2 Power

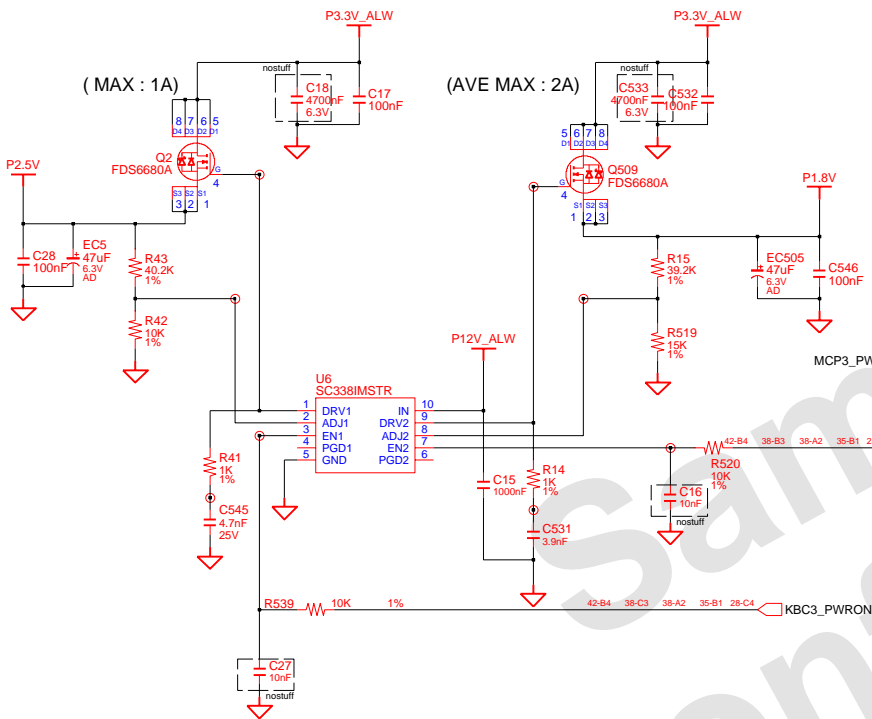


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN DDR2 POWER	SAMSUNG ELECTRONICS PART NO. BA41-00687A
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	36	OF 42

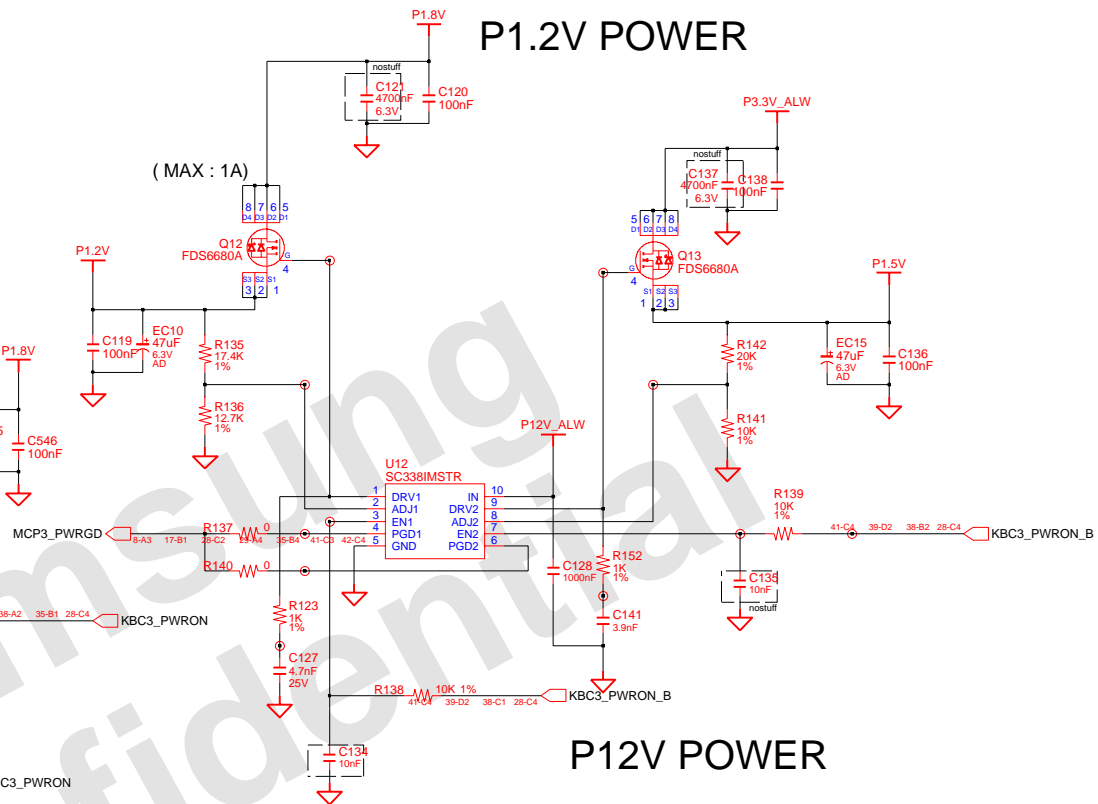
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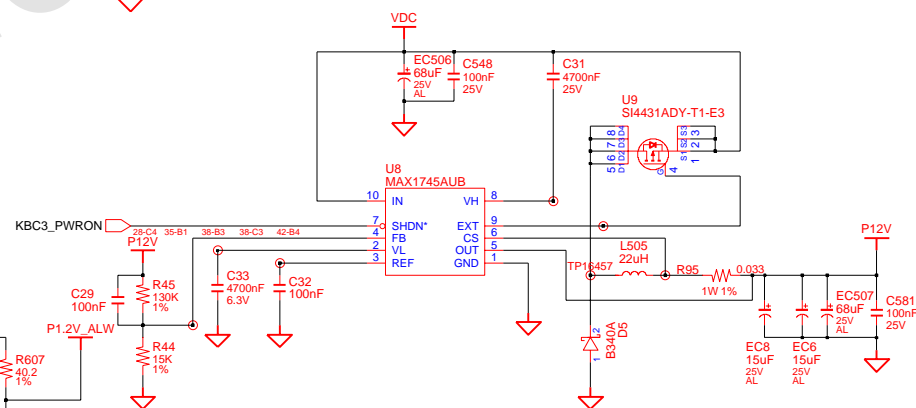
P1.8V / P2.5V POWER



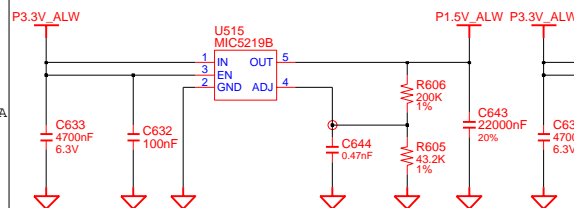
P1.2V POWER



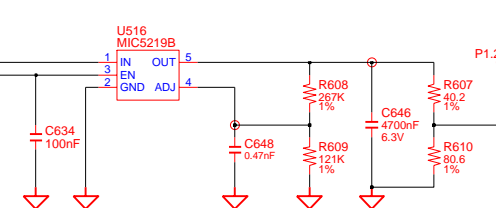
P12V POWER



P1.5V_ALW



P1.2V_ALW

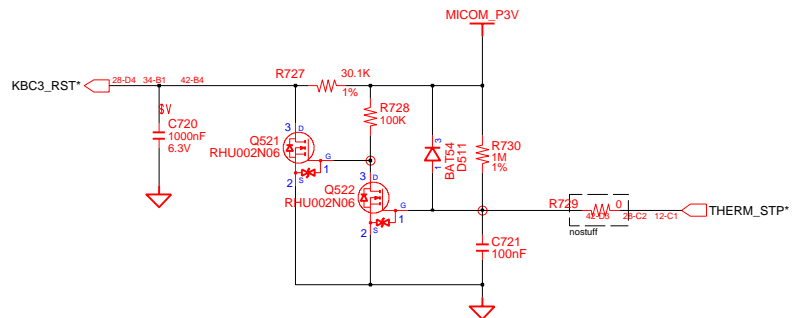


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0	1.2VA/1.5VA/1.8V/2.5V/12V		PART NO. BA41-00687A
MODULE CODE	undef:ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	38	OF 42

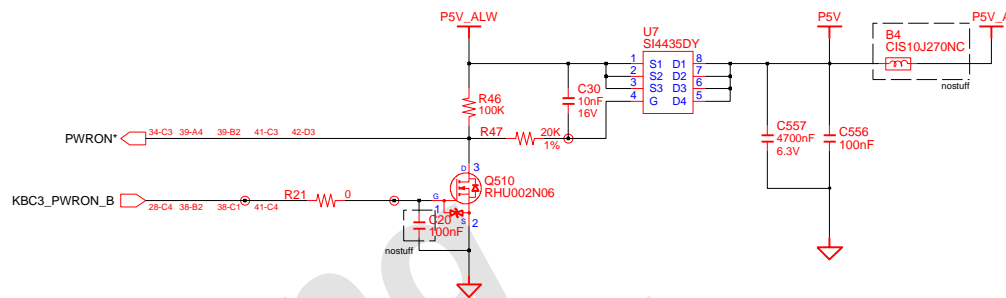
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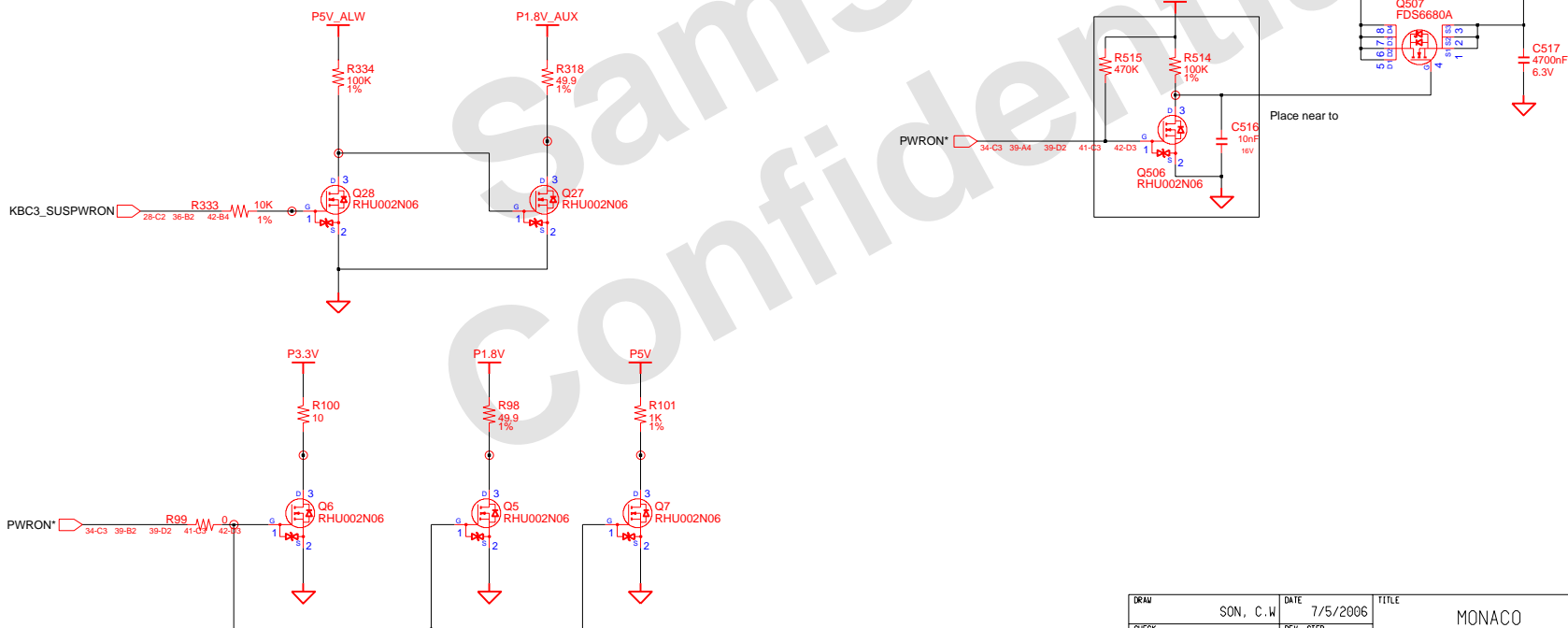
MICOM RESET



Switched Power On (P5V)



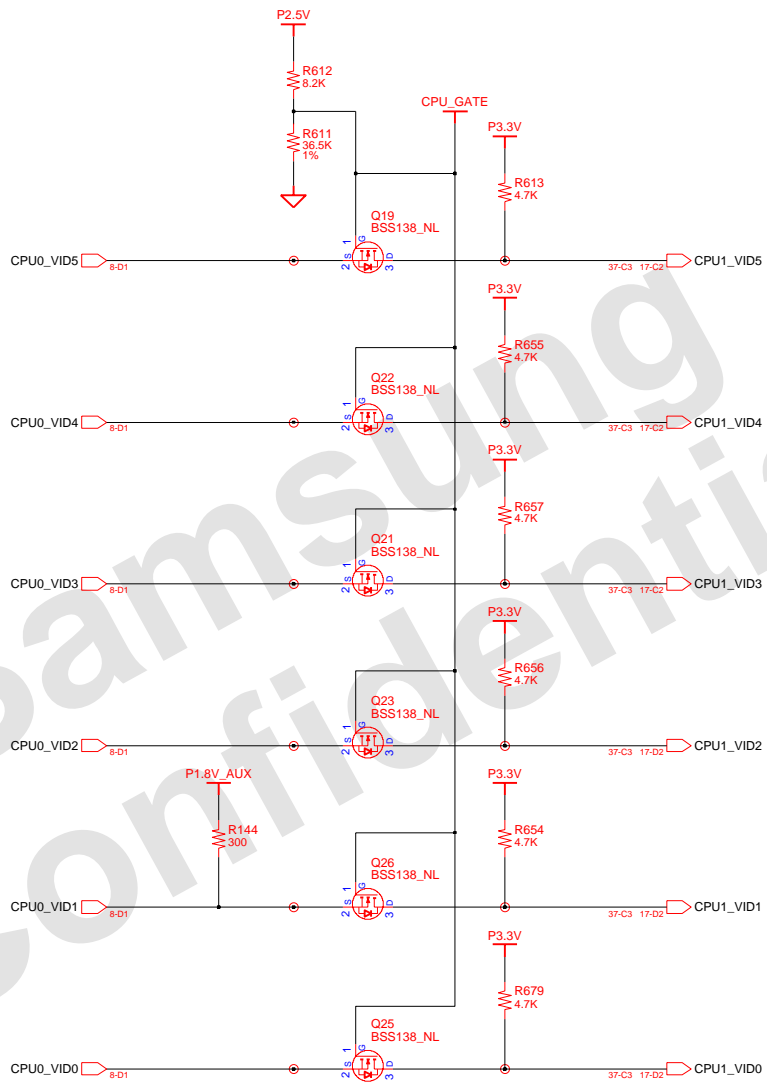
Switched Power On (P3.3V)



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP	MICOM / SWITCHED POWER	PART NO. BA41-00687A	
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	39	OF 42

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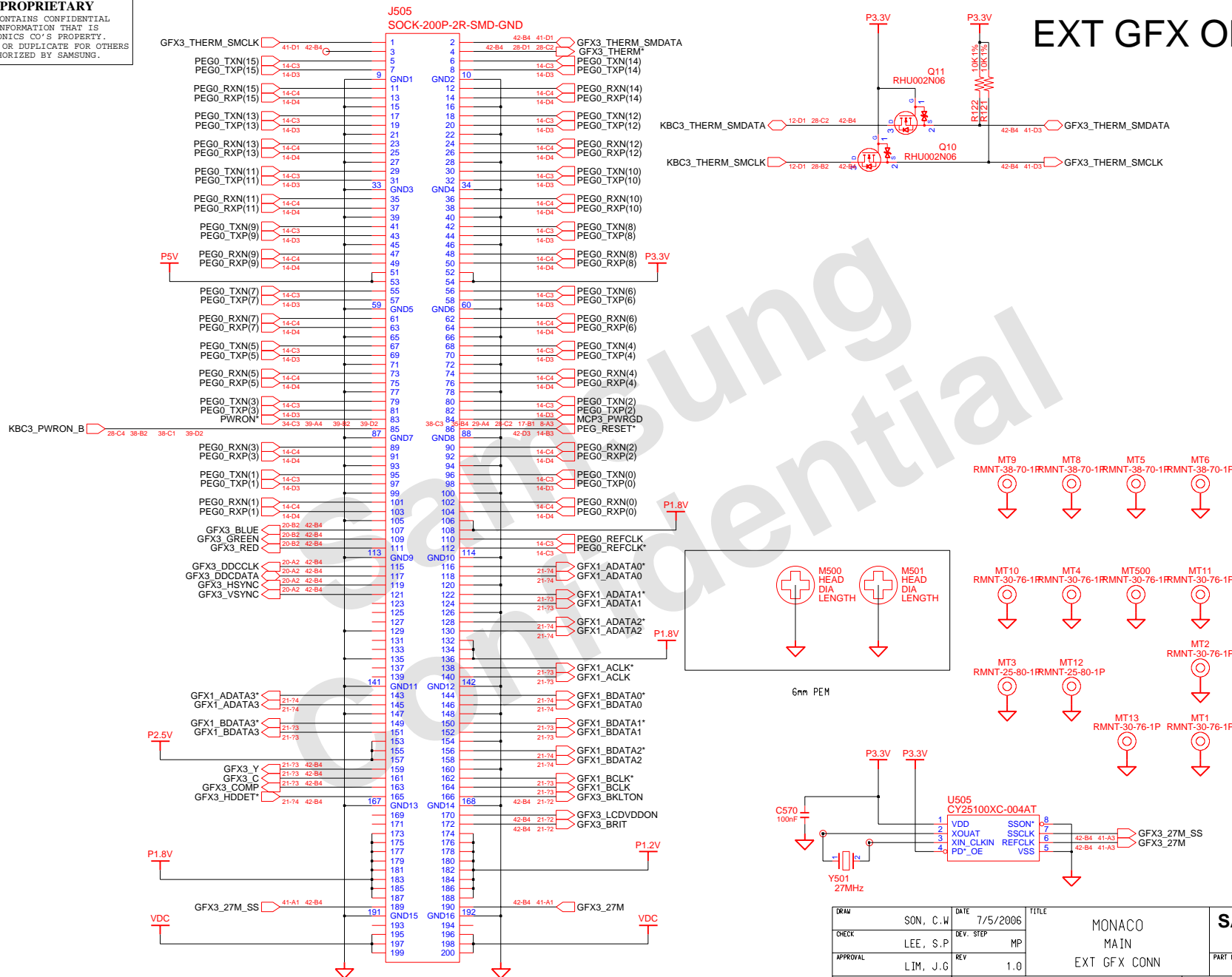


DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN CPU VID TRANSLATION	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP			
APPROVAL	LIM, J.G	REV	1.0		PART NO.	BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	40	OF 42

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EXT GFX ONLY



DRAW	SON, C.W	DATE	7/5/2006	TITLE	MONACO MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	MP		EXT GFX CONN	
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00687A
MODULE CODE	undef ined	LAST EDIT	July 5, 2006 3:50:07 PM	PAGE	41	OF 42

