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ACCORDION-R

CPU : SANTAROSA
 Chip Set : ATI RS600ME & SB600
 Remarks : DESKNOTE

Model Name : ACCORDION-R
 PBA Name : MAIN
 PCB Code : BA41-00777B
 Dev. Step : PR
 Revision : 1.0
 T.R. Date : 2007.7.11

DRAW	CHECK	APPROVAL
SON, C.W	LEE, S.P	LIM, J.G

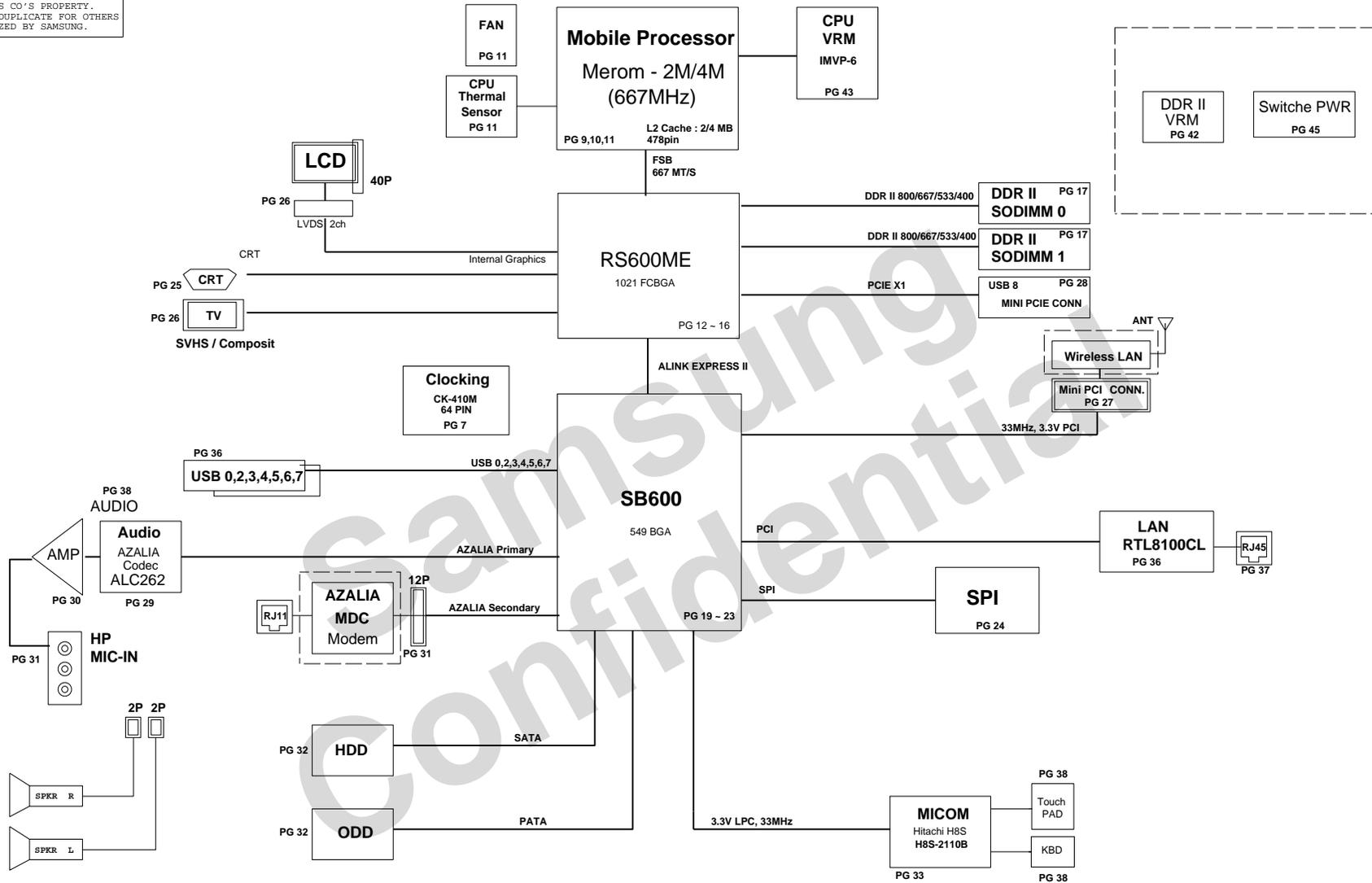
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DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN COVER	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 11, 2007 16:55:42 PM			
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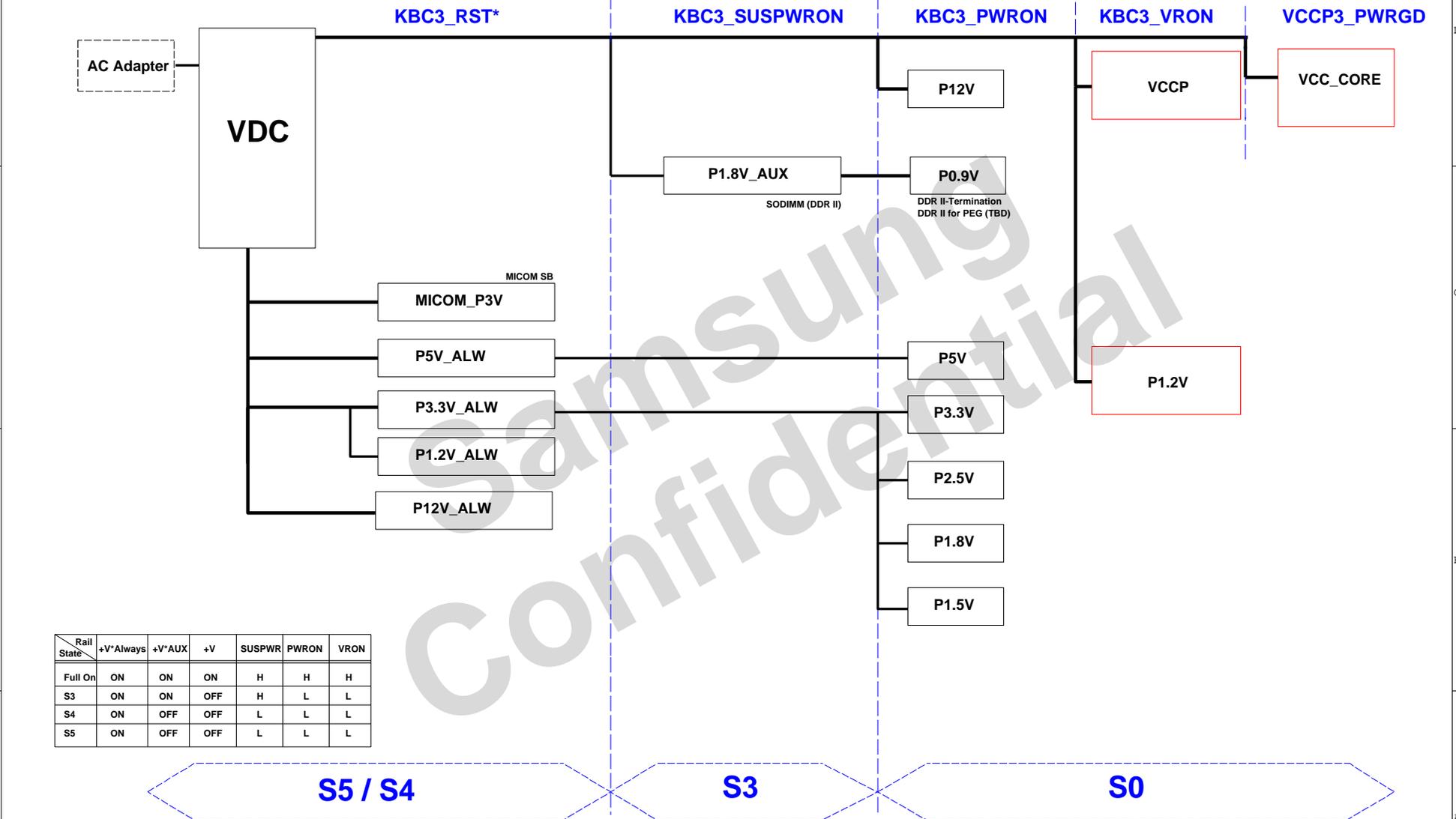


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APPROVAL	LIM, J.G	REV	1.0			
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Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	L	L	L
S5	ON	OFF	OFF	L	L	L

S5 / S4

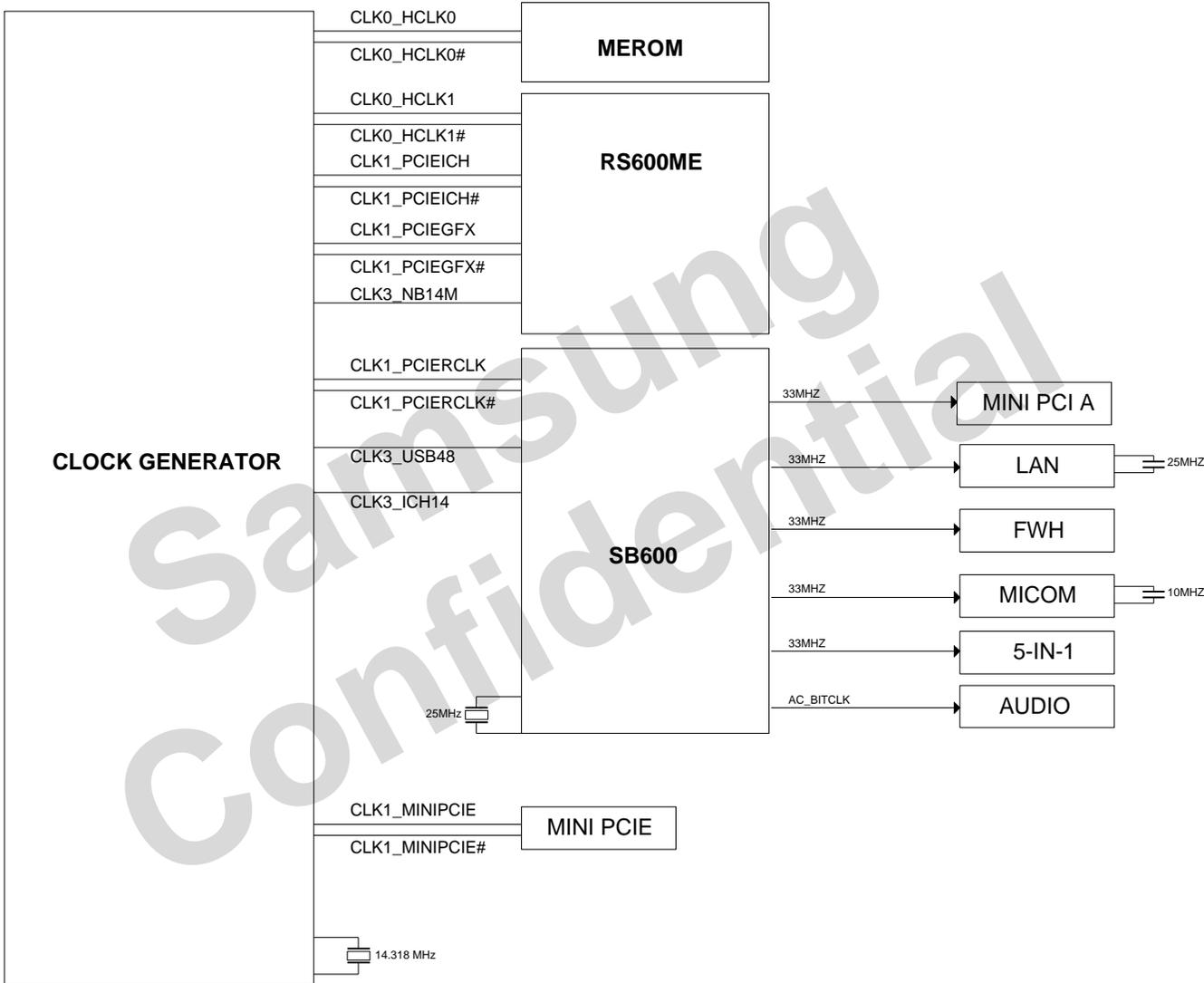
S3

S0

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00777B
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APPROVAL	LIM, J.G	REV	1.0			
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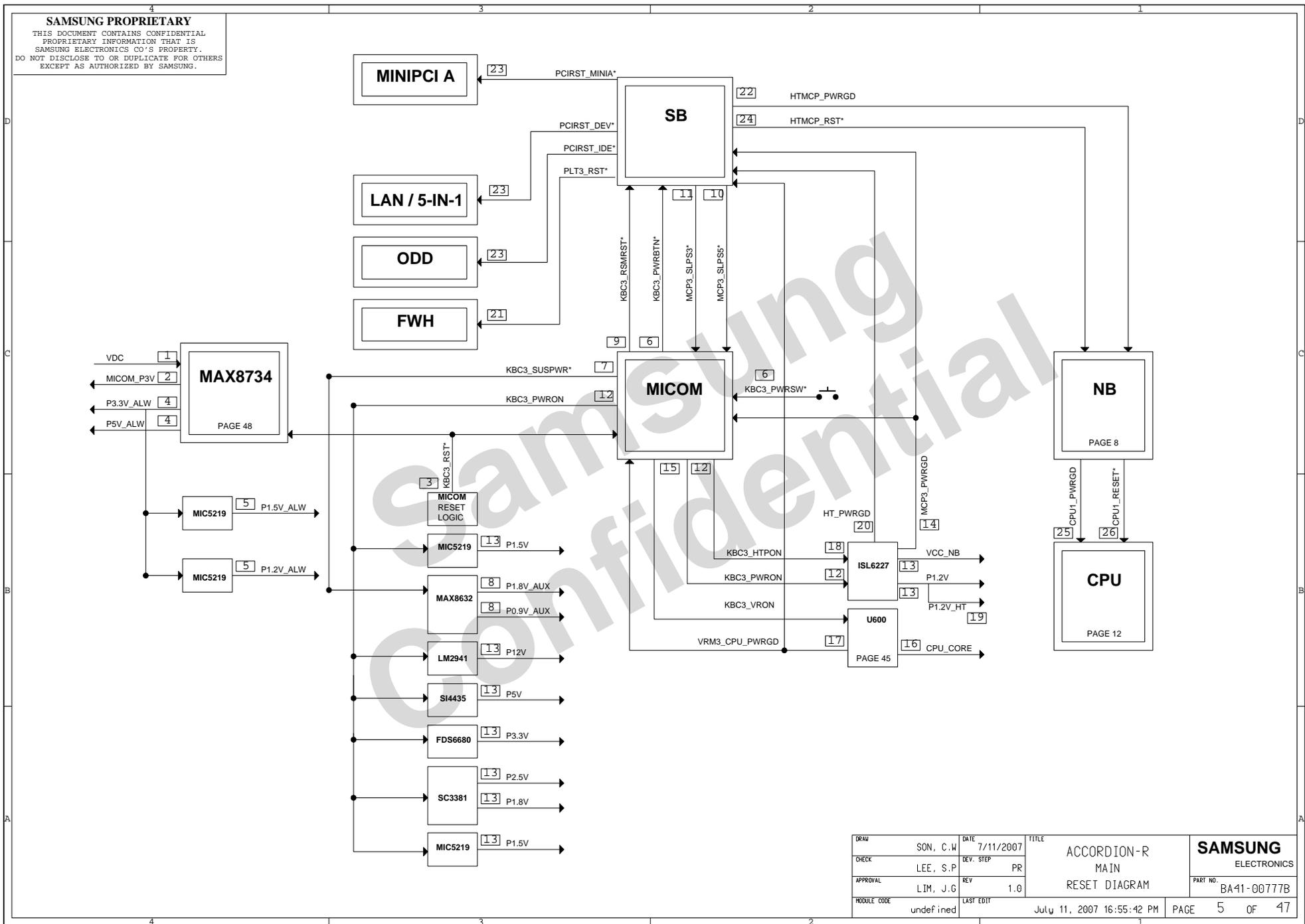
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DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN CLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
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CHECK	LEE, S.P	DEV. STEP	PR	REV	1.0		
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 5 OF 47	
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
MINIPCI A	AD21	0	A,B
LAN	AD23	2	D
S-IN-1	AD24	3	B
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	14.318MHz	CLOCK	ICS951461
Crystal	10MHz	MICOM	H8S-2110B
Crystal	25MHz	LAN	RTL8110CL

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU CORE	Core voltage for AMD SEMPRON (1.308-1.068V)
VCC_NB	SEMPRON Processor Hyper Transport (1.2V) North Bridge Core Voltage
P0.9V_AUX	0.9V switched power rail (off in S4-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWS	5V power rail (Always On)
P3.3V_ALWS	3.3V power rail (Always On)
P1.5V_ALWS	1.5V power rail (Always On)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.5500 V	1 0 0 0 0 0	0.7625 V
0 0 0 0 0 1	1.5250 V	1 0 0 0 0 1	0.7500 V
0 0 0 0 1 0	1.5000 V	1 0 0 0 1 0	0.7375 V
0 0 0 0 1 1	1.4750 V	1 0 0 0 1 1	0.7250 V
0 0 0 1 0 0	1.4500 V	1 0 0 1 0 0	0.7125 V
0 0 0 1 0 1	1.4250 V	1 0 0 1 0 1	0.7000 V
0 0 0 1 1 0	1.4000 V	1 0 0 1 1 0	0.6875 V
0 0 0 1 1 1	1.3750 V	1 0 0 1 1 1	0.6750 V
0 0 1 0 0 0	1.3500 V	1 0 1 0 0 0	0.6625 V
0 0 1 0 0 1	1.3250 V	1 0 1 0 0 1	0.6500 V
0 0 1 0 1 0	1.3000 V	1 0 1 0 1 0	0.6375 V
0 0 1 0 1 1	1.2750 V	1 0 1 0 1 1	0.6250 V
0 0 1 1 0 0	1.2500 V	1 0 1 1 0 0	0.6125 V
0 0 1 1 0 1	1.2250 V	1 0 1 1 0 1	0.6000 V
0 0 1 1 1 0	1.2000 V	1 0 1 1 1 0	0.5875 V
0 0 1 1 1 1	1.1750 V	1 0 1 1 1 1	0.5750 V
0 1 0 0 0 0	1.1500 V	1 1 0 0 0 0	0.5625 V
0 1 0 0 0 1	1.1250 V	1 1 0 0 0 1	0.5500 V
0 1 0 0 1 0	1.1000 V	1 1 0 0 1 0	0.5375 V
0 1 0 0 1 1	1.0750 V	1 1 0 0 1 1	0.5250 V
0 1 0 1 0 0	1.0500 V	1 1 0 1 0 0	0.5125 V
0 1 0 1 0 1	1.0250 V	1 1 0 1 0 1	0.5000 V
0 1 0 1 1 0	1.0000 V	1 1 0 1 1 0	0.4875 V
0 1 0 1 1 1	0.9750 V	1 1 0 1 1 1	0.4750 V
0 1 1 0 0 0	0.9500 V	1 1 1 0 0 0	0.4625 V
0 1 1 0 0 1	0.9250 V	1 1 1 0 0 1	0.4500 V
0 1 1 0 1 0	0.9000 V	1 1 1 0 1 0	0.4375 V
0 1 1 0 1 1	0.8750 V	1 1 1 0 1 1	0.4250 V
0 1 1 1 0 0	0.8500 V	1 1 1 1 0 0	0.4125 V
0 1 1 1 0 1	0.8250 V	1 1 1 1 0 1	0.4000 V
0 1 1 1 1 0	0.8000 V	1 1 1 1 1 0	0.3875 V
0 1 1 1 1 1	0.7750 V	1 1 1 1 1 1	0.3750 V

I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
W83L786NG(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2, 3	SYSTEM PORT B
4, 5	SYSTEM PORT C
1	DMB
6, 7	SYSTEM PORT D
8	MINI POE

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

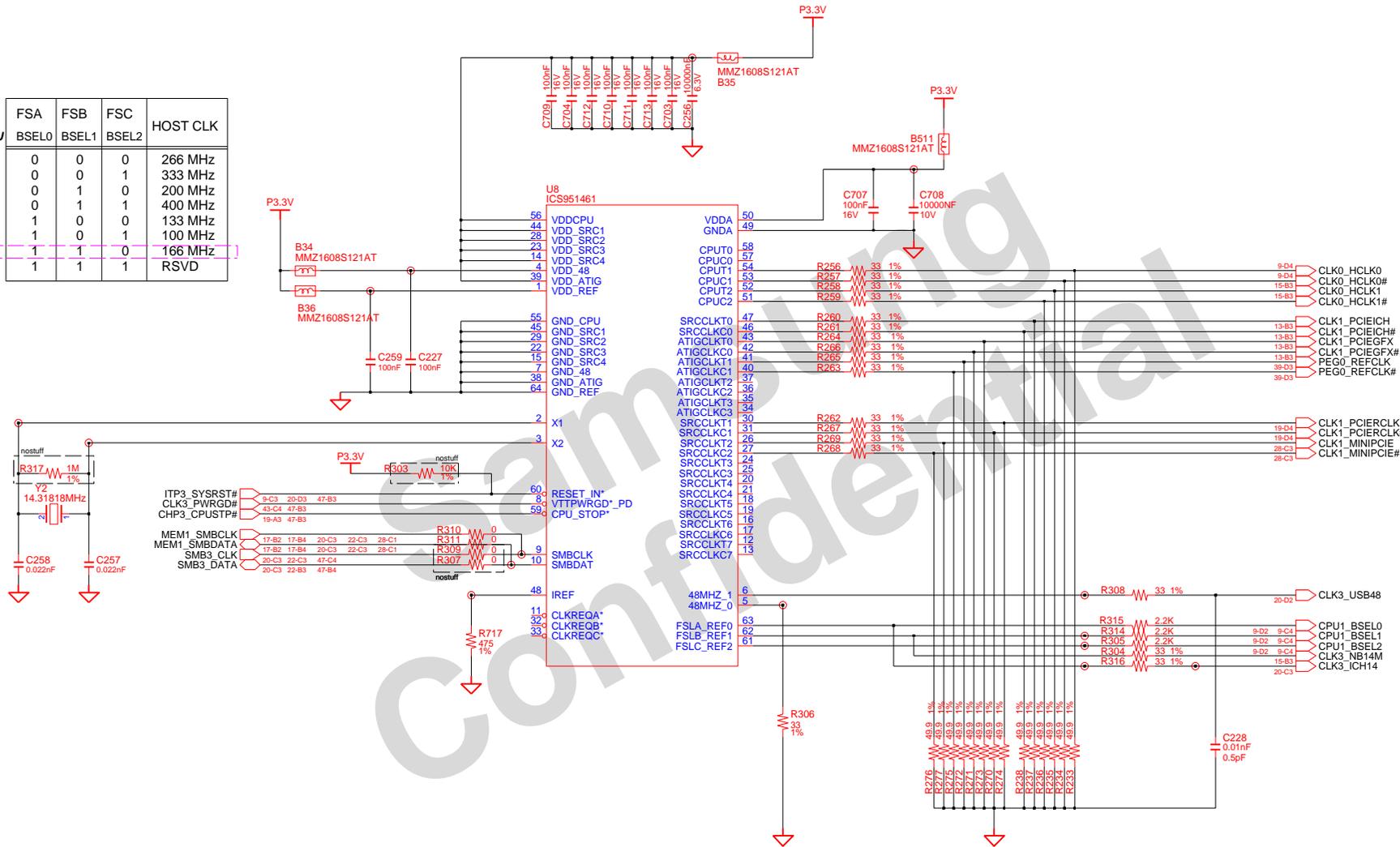
CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

DRAW	SON, C.W.	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P.	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G.	REV	1.0		BOARD INFORMATION	PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	6	OF 47

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CPU			
FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

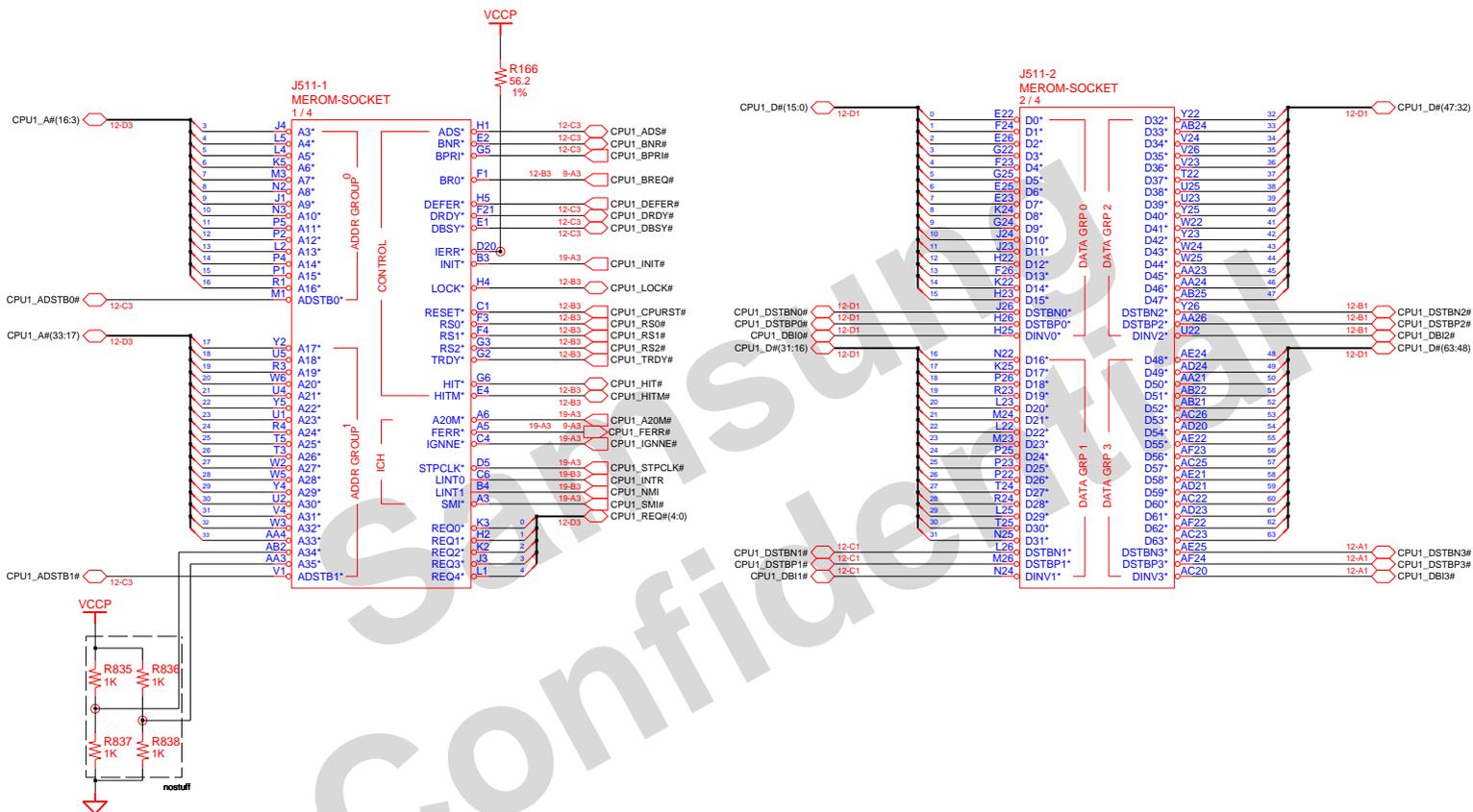


ITP3_SYSRST#	9-C3	20-D3	47-B3
CLK3_PWRGD#	33-C4	47-B3	
CHP3_CPUSTP#	19-A3	47-B3	
MEM1_SMBCLK	17-B2	17-B4	20-C3 22-C3 28-C1
MEM1_SMBDATA	17-B2	17-B4	20-C3 22-C3 28-C1
SMB3_CLK	20-C3	22-C3	47-C4
SMB3_DATA	20-C3	22-B3	47-B4

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	7	OF 47

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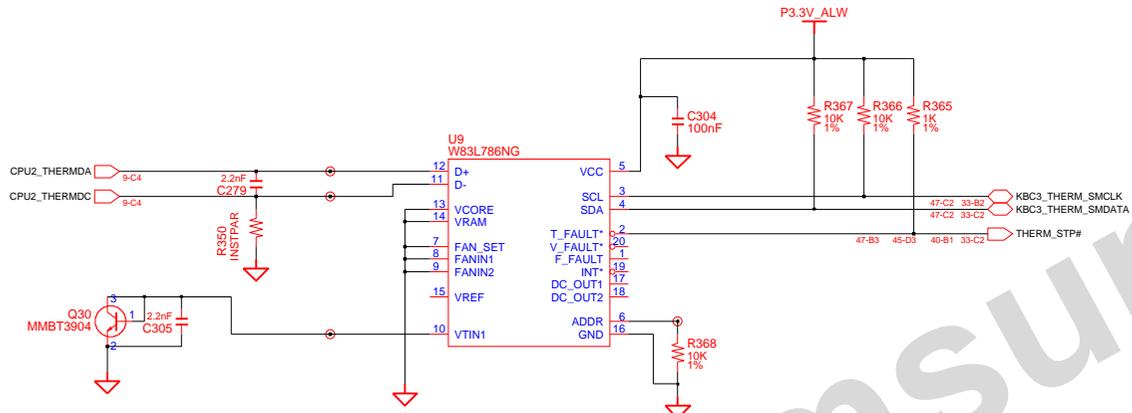


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN CPU(1/3)	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE		

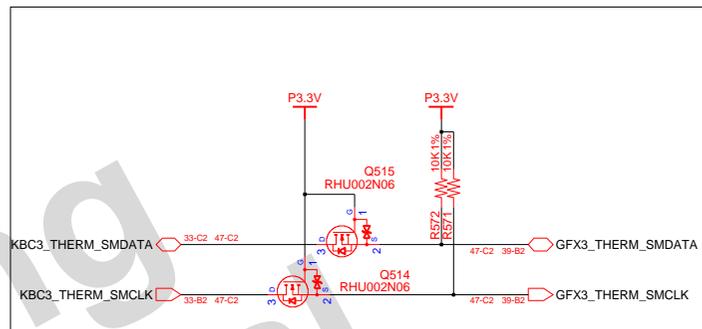
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CPU/MEMORY Thermal Sensor

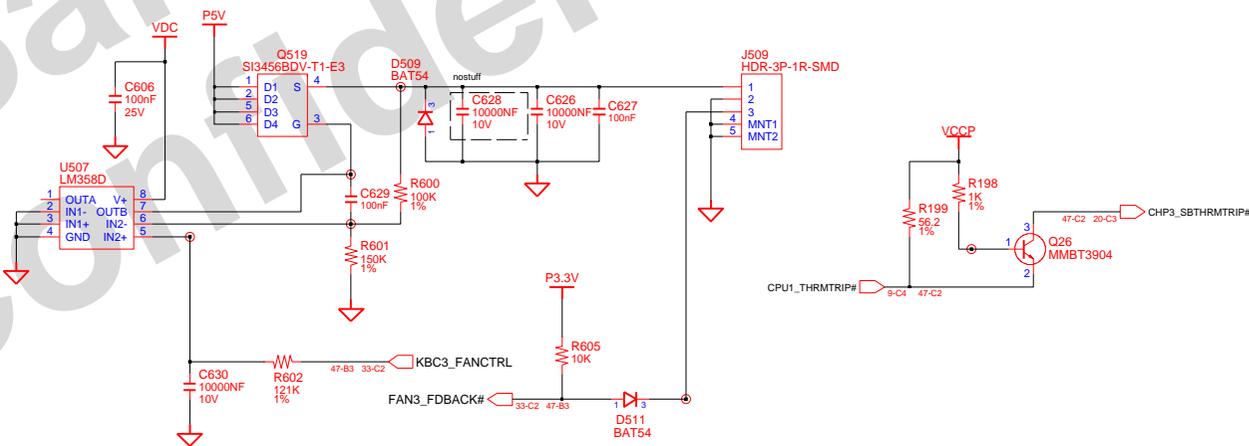
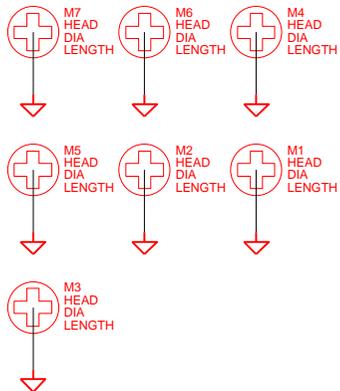


EXT



FAN CONTROL

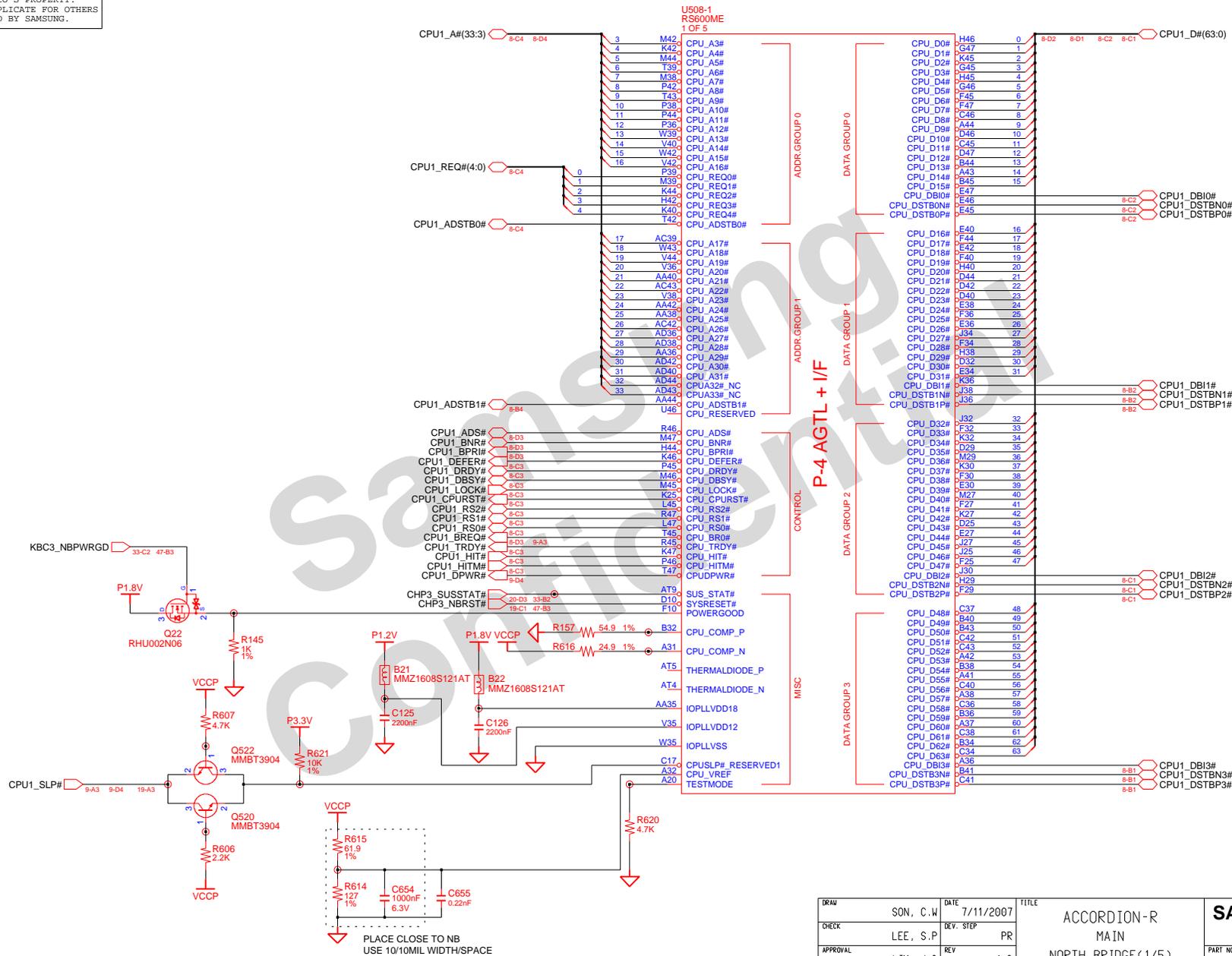
FAN&RHE PEM



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	LIM, J.G	REV	1.0	THERMAL SENSOR/FAN CTRL	BA41-00777B	
MODULE CODE	undefined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	11 OF 47	

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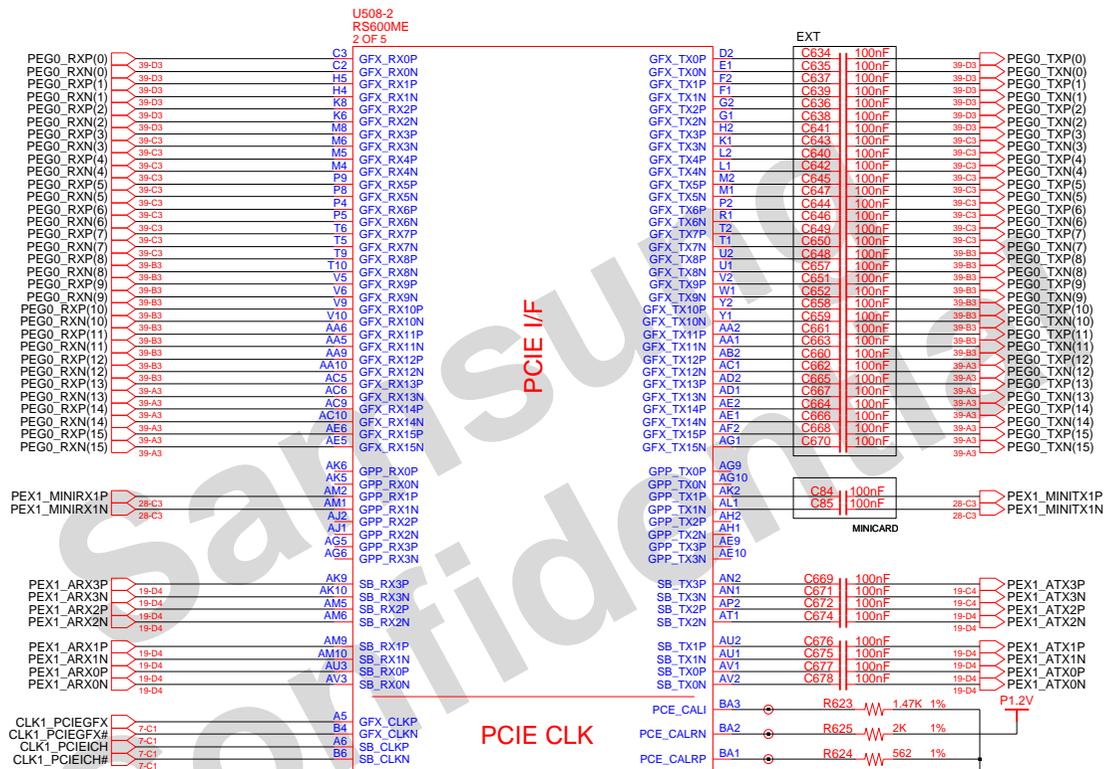


PLACE CLOSE TO NB
USE 10/10ML WIDTH/SPACE

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN NORTH BRIDGE(1/5)	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
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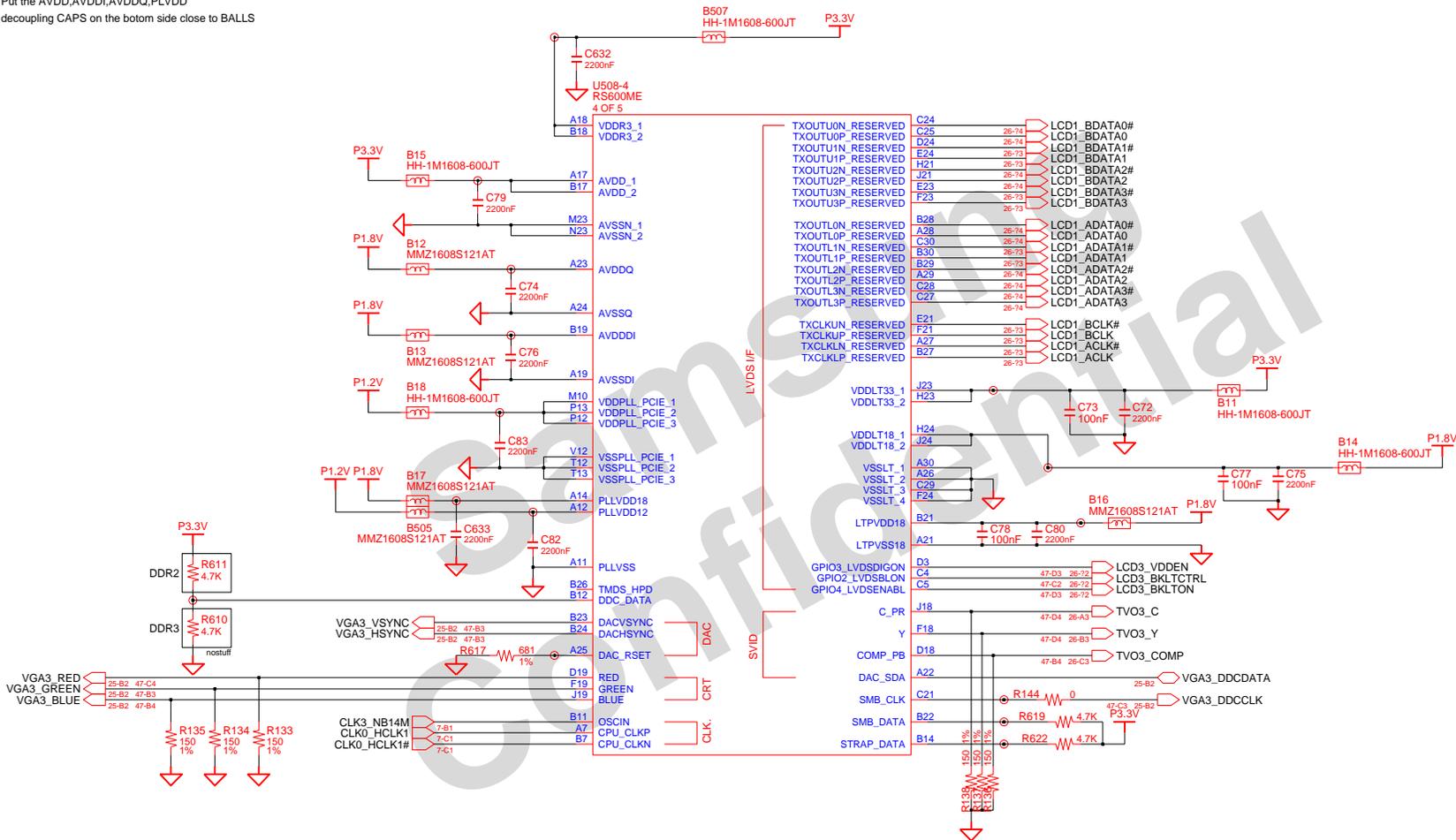


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CHECK	LEE, S.P	DEV. STEP	PR	REV	1.0	
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 13 OF 47
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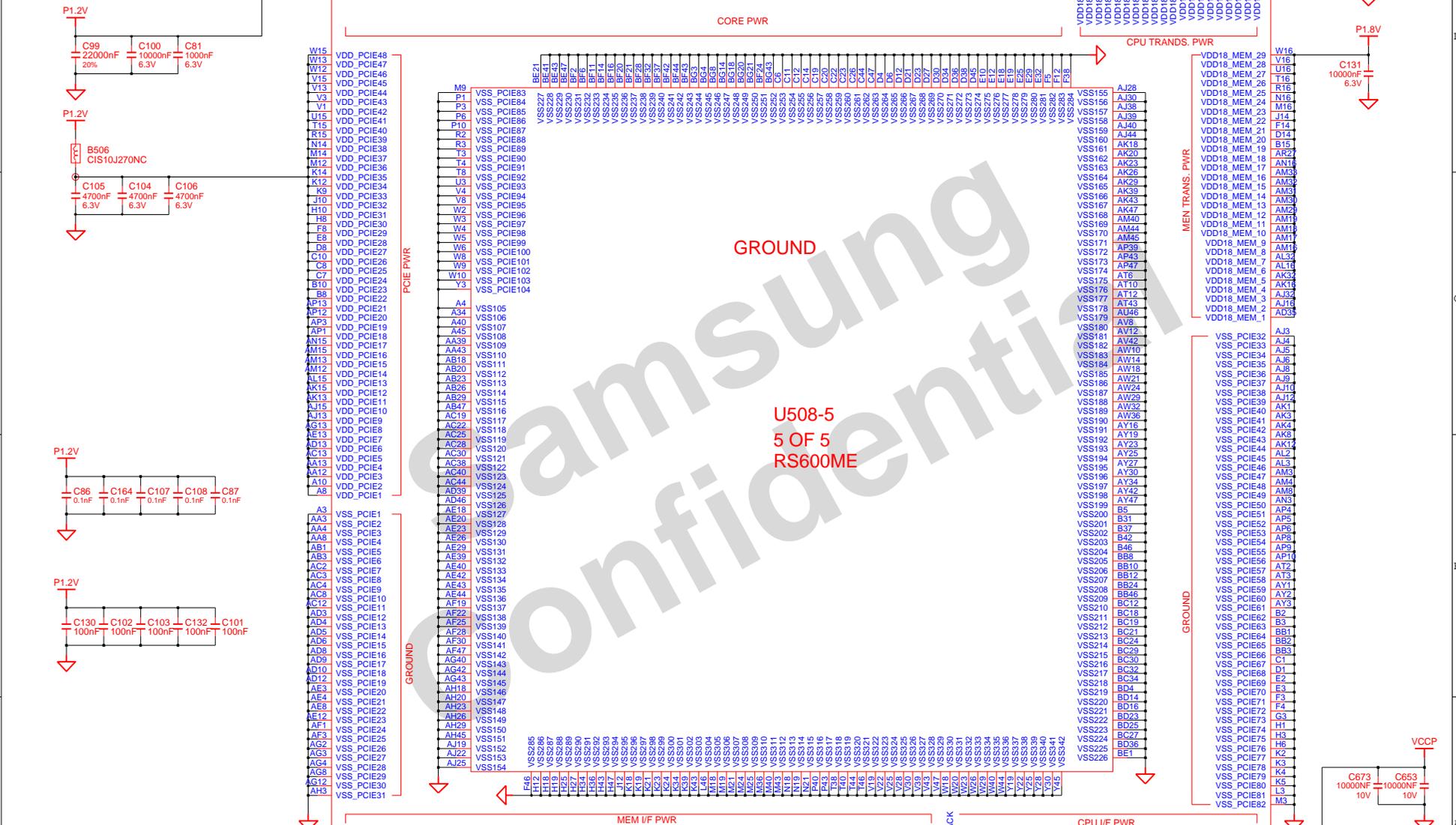
Put the AVDD,AVDDI,AVDDQ,PLVDD decoupling CAPS on the botom side close to BALLS



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN NORTH BRIDGE(4/5)	SAMSUNG ELECTRONICS
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APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00777B
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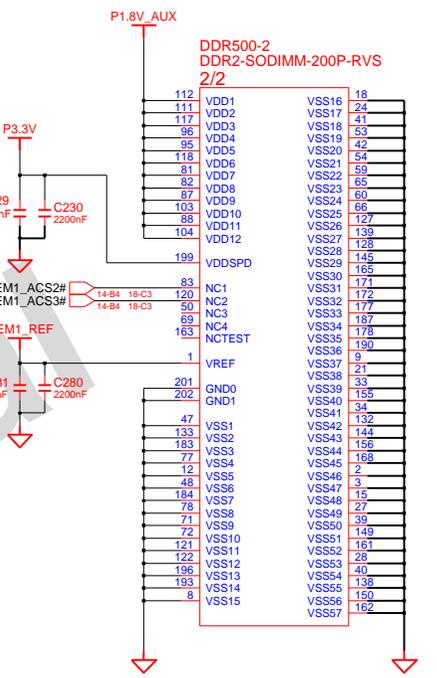
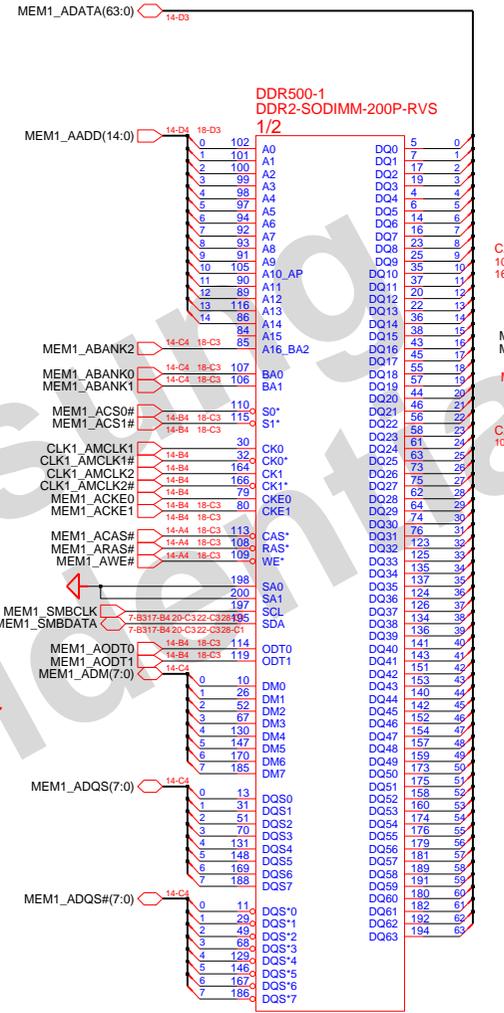
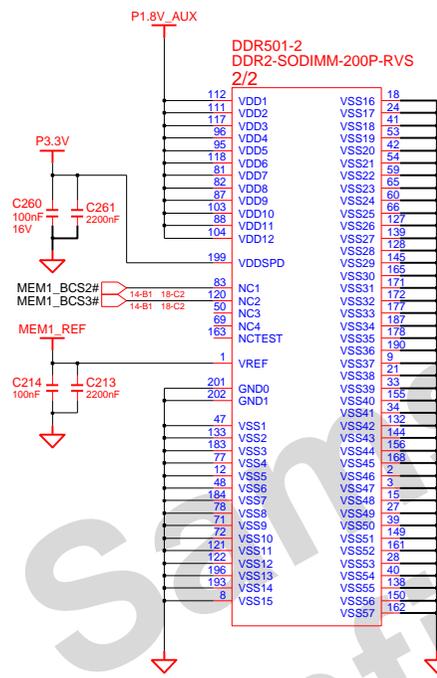
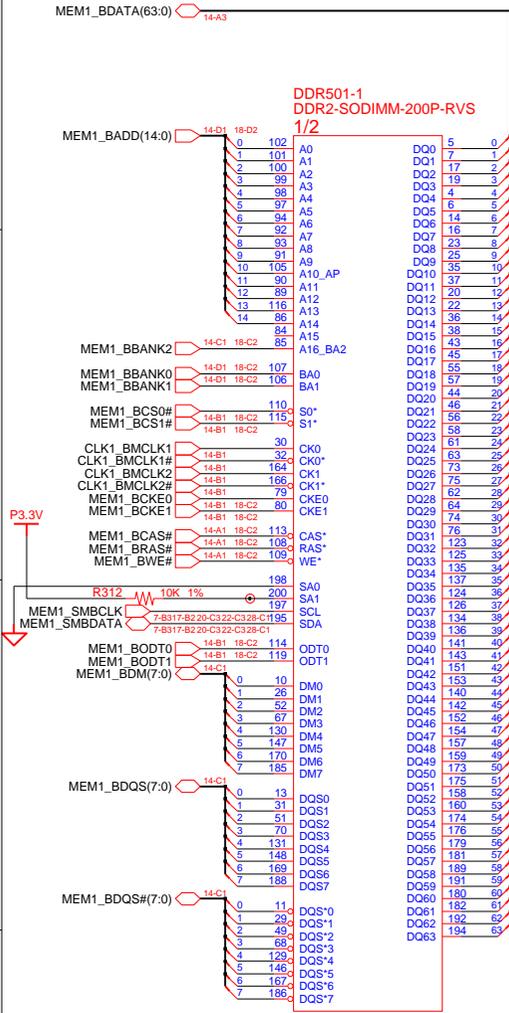
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PART NO. BA41-00777B

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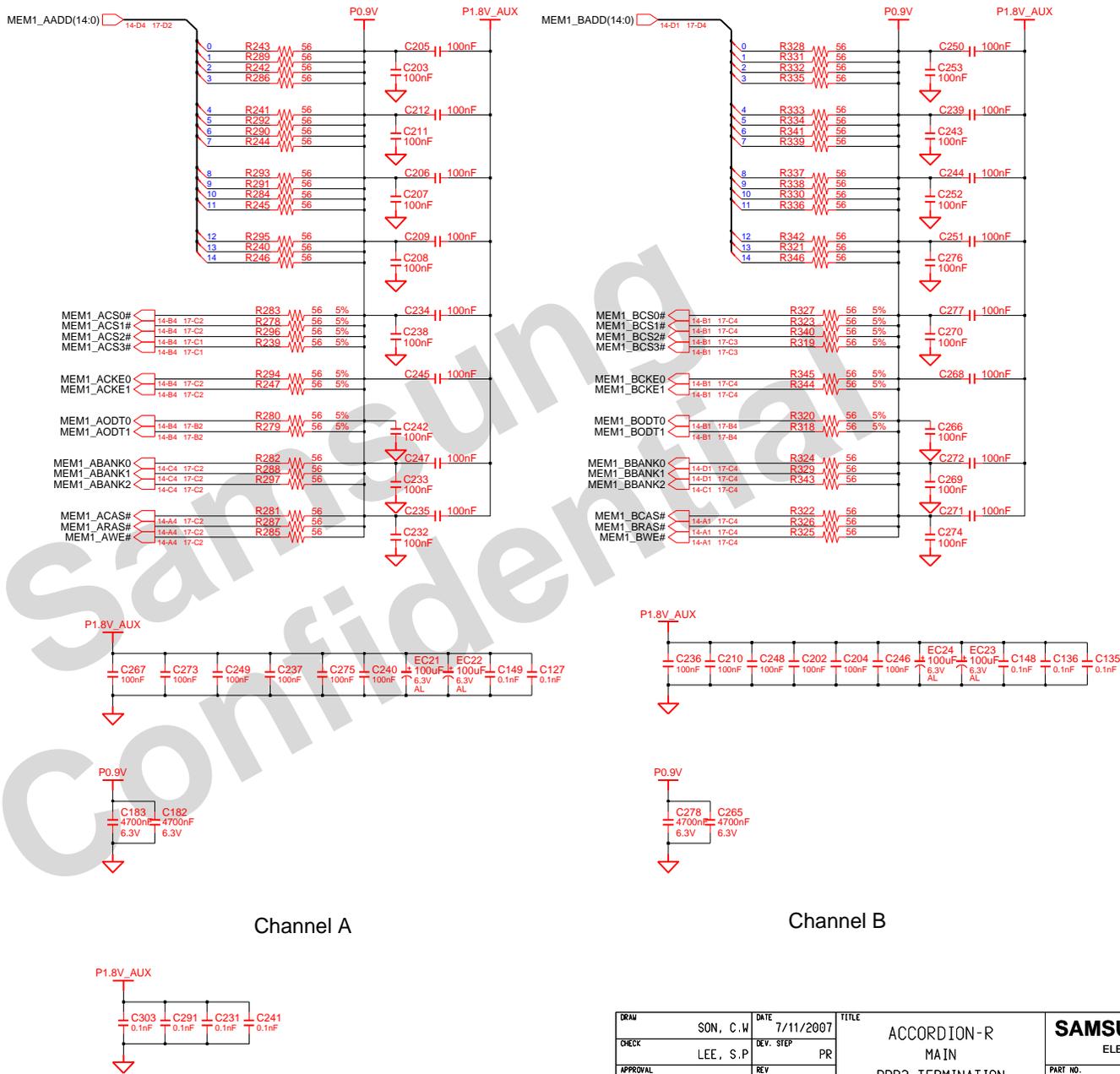
DDR1 Height : 5.2mm

DDR2 Height : 9.2mm

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	DDR2-SODIMM	PART NO.	BA41-00777B
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Channel A

Channel B

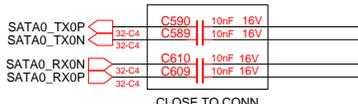
DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN DDR2- TERMINATION	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 18 OF 47		

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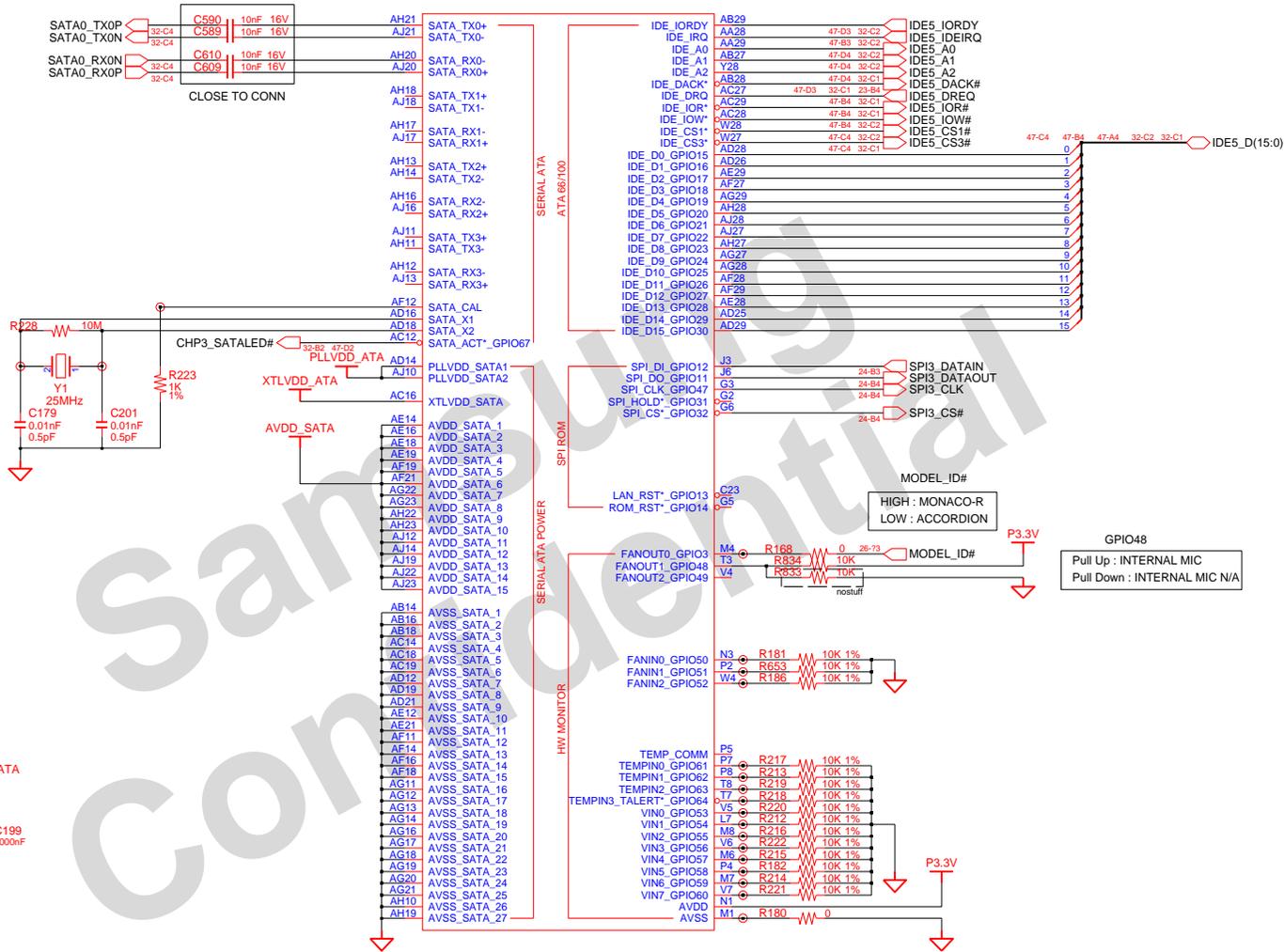
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**U510-3
218S6ECLA21FG**

3 / 4



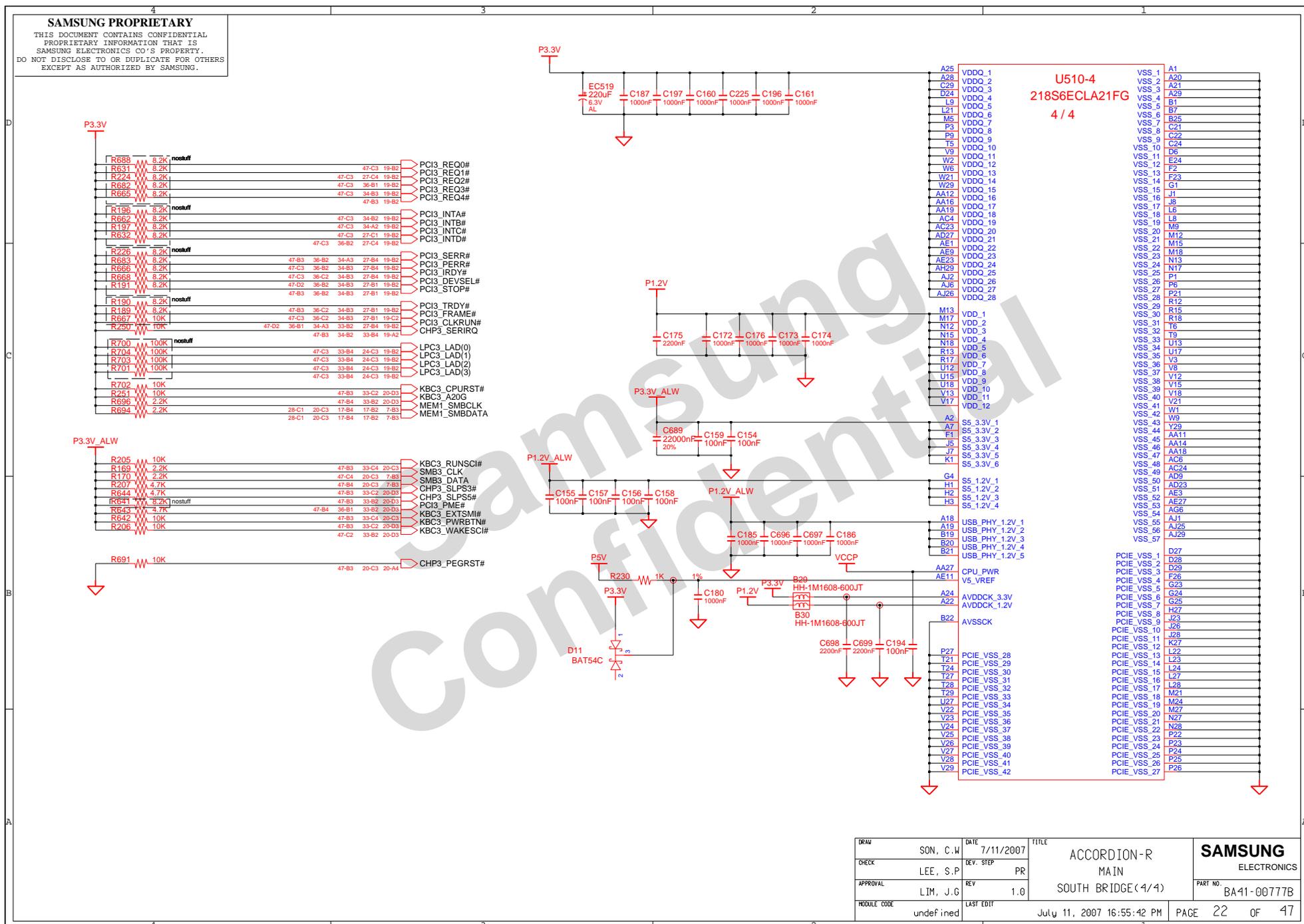
CLOSE TO CONN



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN SOUTH BRIDGE(3/4)	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
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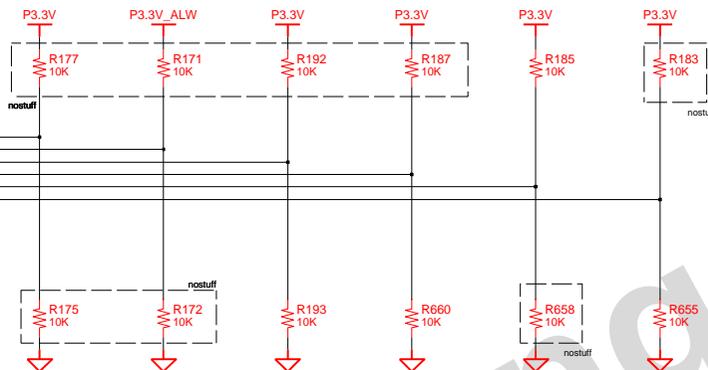


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN SOUTH BRIDGE(4/4)	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	22 OF 47	

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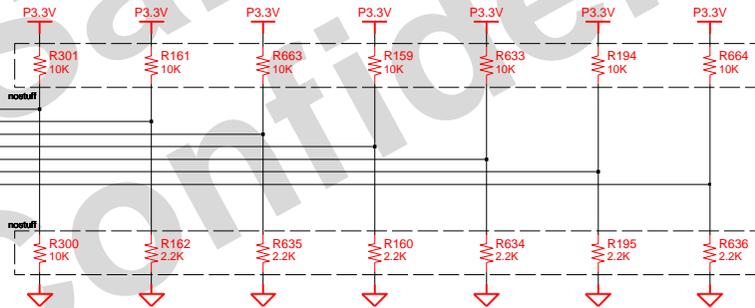
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REQUIRED SYSTE STRAPS



PULL HIGH	AC_SDOUT USE DEBUG STRAPS	RTC_CLK INTERNAL RTC DEFAULT	PCI_CLK4 USE INT. PLL48	PCI_CLK6 CPU IF = K8	PCI_CLK0 ROM TYPE: H,H = PCI ROM H,H = SPI ROM L,H = LPC ROM L,L = FWH ROM	PCI_CLK1 DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXT.RTC	USE EXT. 48MHZ DEFAULT	CPU IF = P4		

DEBUS STRAPS



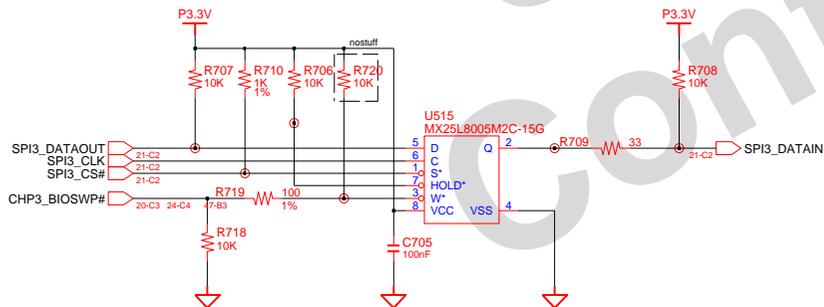
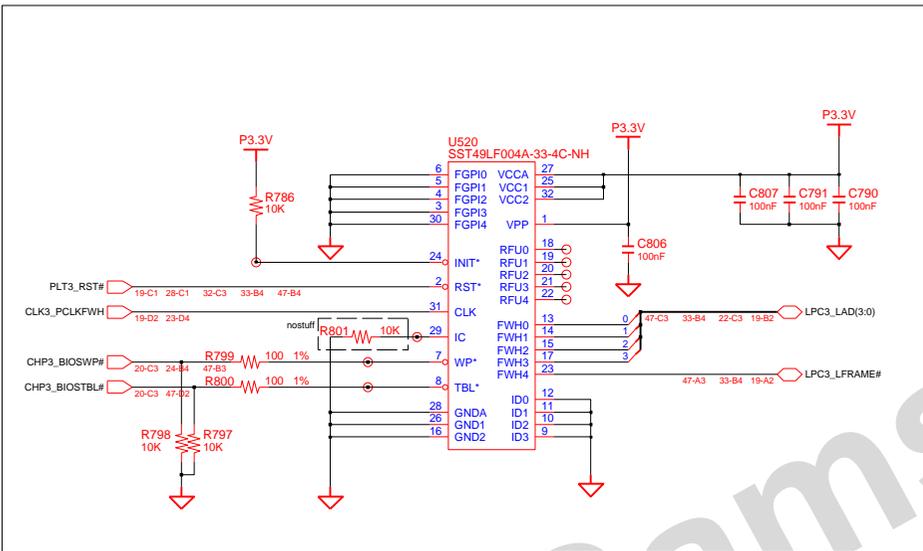
STRAP HIGH	IDE5_DACK* USE LONG RESET DEFAULT	PCI3_AD(28) USE LONG RESET DEFAULT	PCI3_AD(27) USE PCI PLL DEFAULT	PCI3_AD(26) USE ACPI BCLK DEFAULT	PCI3_AD(25) USE IDE PLL DEFAULT	PCI3_AD(24) USE DEFAULT PCIE STRAPS DEFAULT	PCI3_AD(23) BOOTFAIL TIMER DISABLED DEFAULT
STRAP LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN STRAPS OPTION	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 23 OF 47		

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nostuff

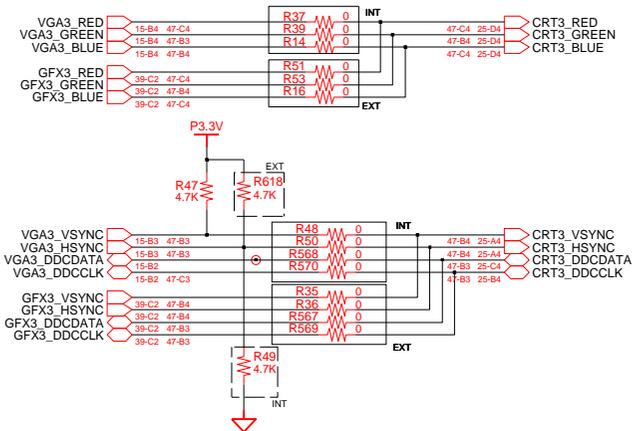
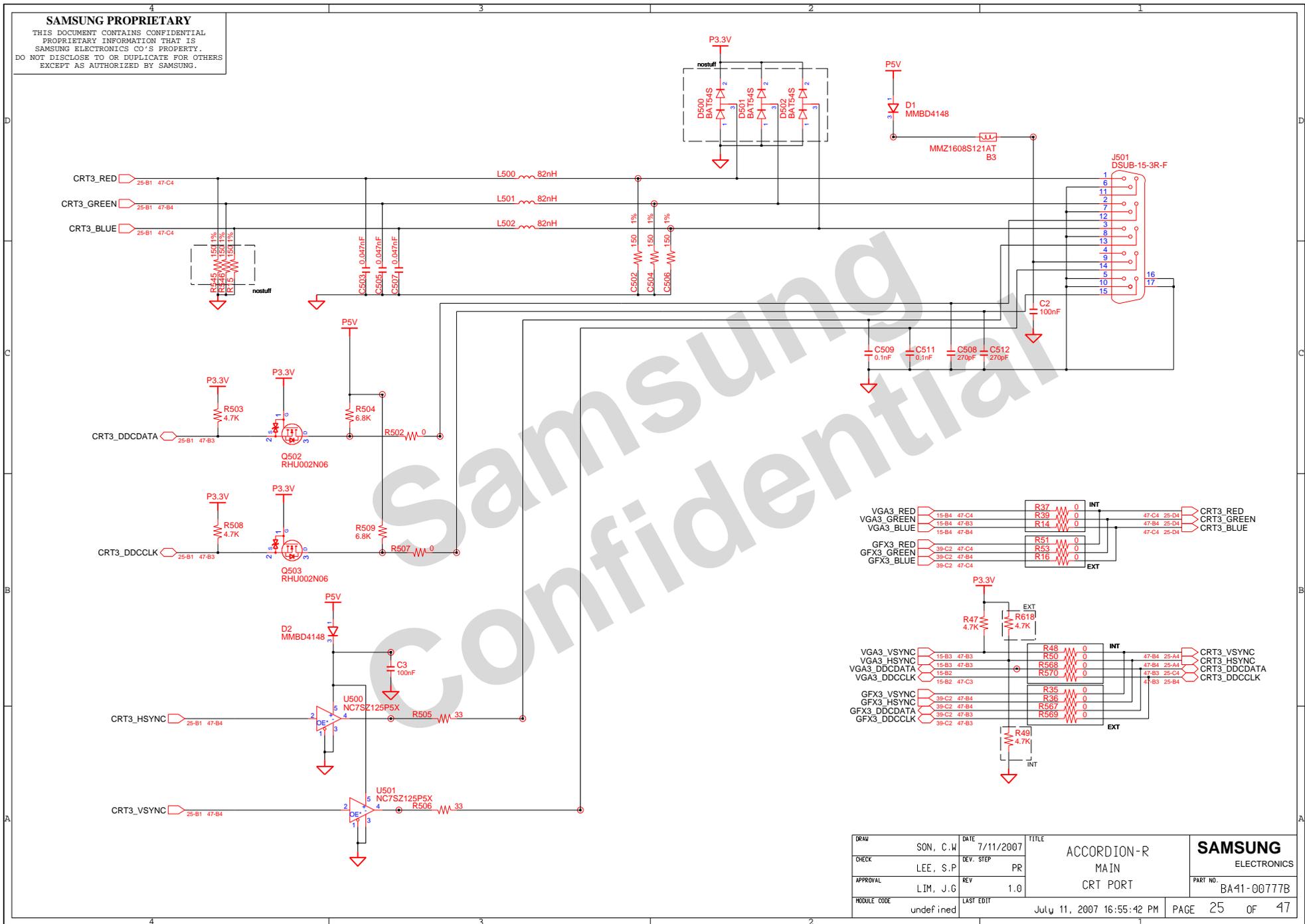


- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INITIALIZE SYSTEM H/W
- 08 INITIALIZE CHIPSET REGISTERS
- 09 SET IN POST FLAG
- 0A INIT CPU REGISTERS
- 0B CPU CACHE ON
- 0C INITIALIZE CACHE TO POST
- 0E INITIALIZE I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INITIALIZE POWER MANAGER
- 11 LOAD ALTERNATE REGISTERS
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INITIALIZE KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 INITIALIZE 8254 TIMER
- 1A INITIALIZE 8237 DMA CONTROLLER
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REGISTERS TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TEST CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REGISTERS
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INITIALIZE INTERRUPT VECTOR
- 44 INITIALIZE BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INITIALIZE I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INITIALIZE PCI BUS AND DEVICE
- 4A INITIALIZE ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY "PRESS SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1
- 66 CONFIGURE ADVANCE CACHE REGISTERS
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD EERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT. RS232C
- 84 DETECT AND INSTALL EXT. PARALLEL
- 86 RE-INITIALIZE ON-BOARD I/O PORT
- 88 INITIALIZE BIOS DATA ROM
- 8A INITIALIZE EXTENDED BIOS DATA AREA
- 8C INITIALIZE FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INITIALIZE TYPOMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INITIALIZE HDD CONTROLLER
- 91 INITIALIZE LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		FWH	
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	24 OF 47	

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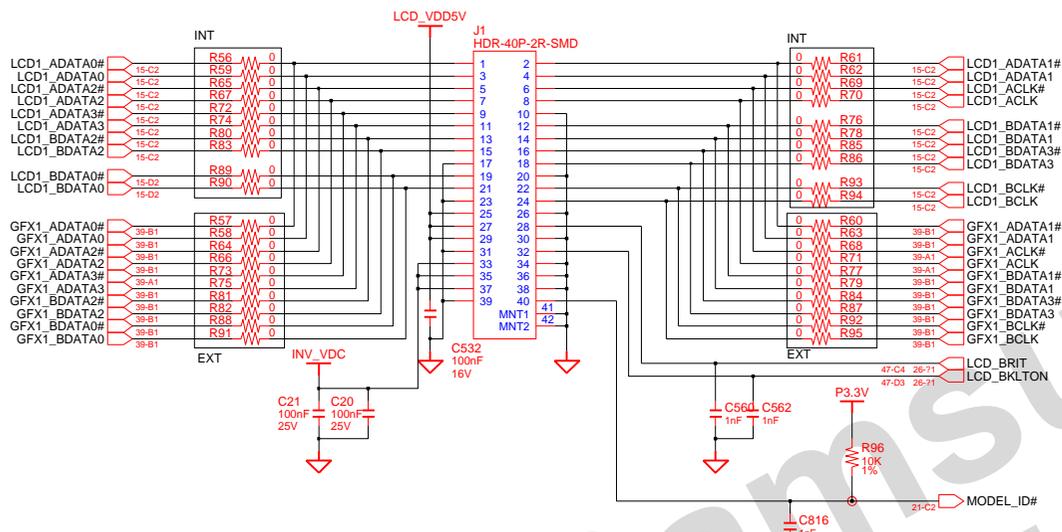


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN CRT PORT	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR	REV	1.0	
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 25 OF 47
MODULE CODE	undef:ined					

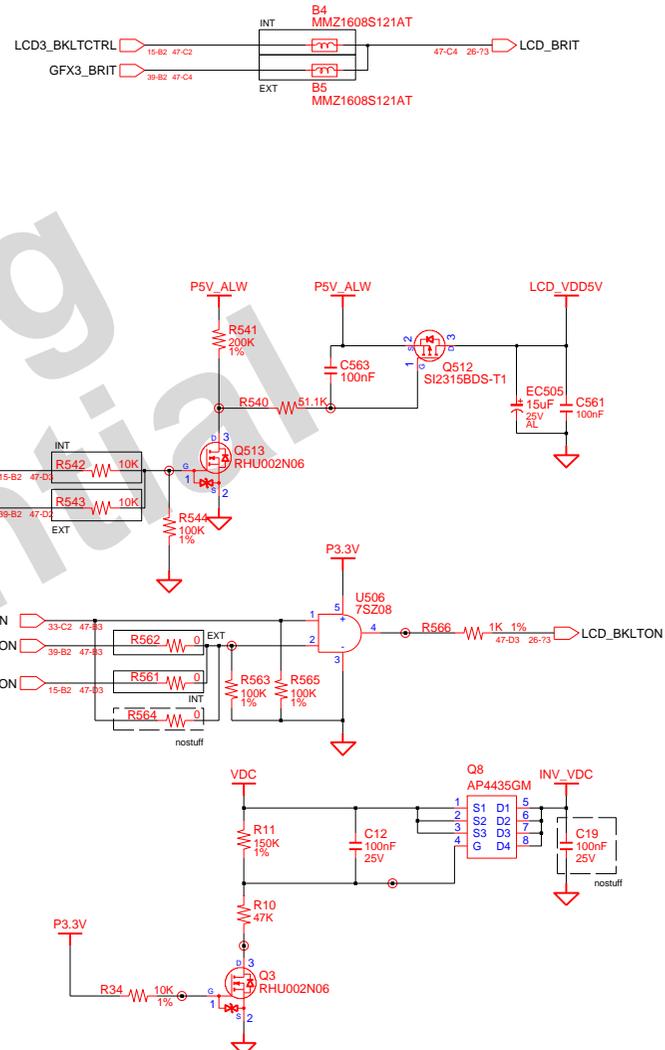
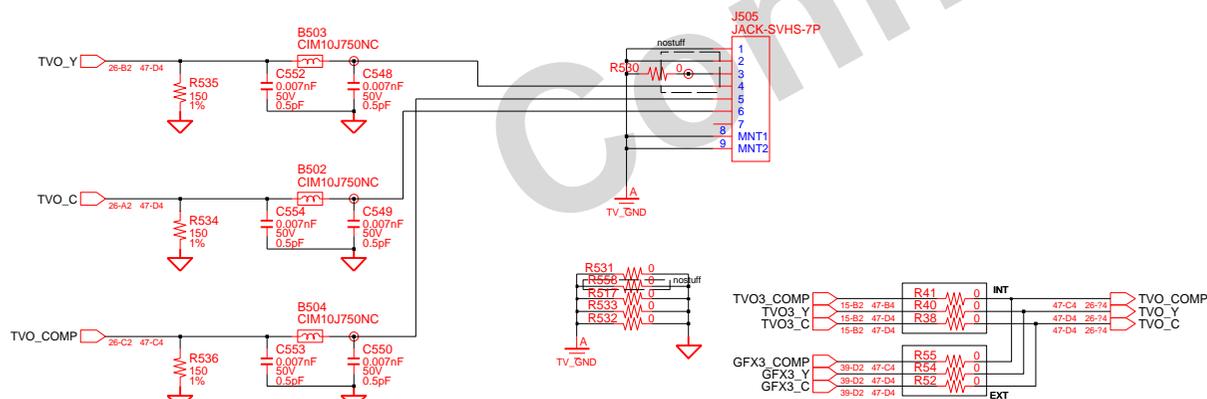
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LCD CONNECTOR



TV-OUT

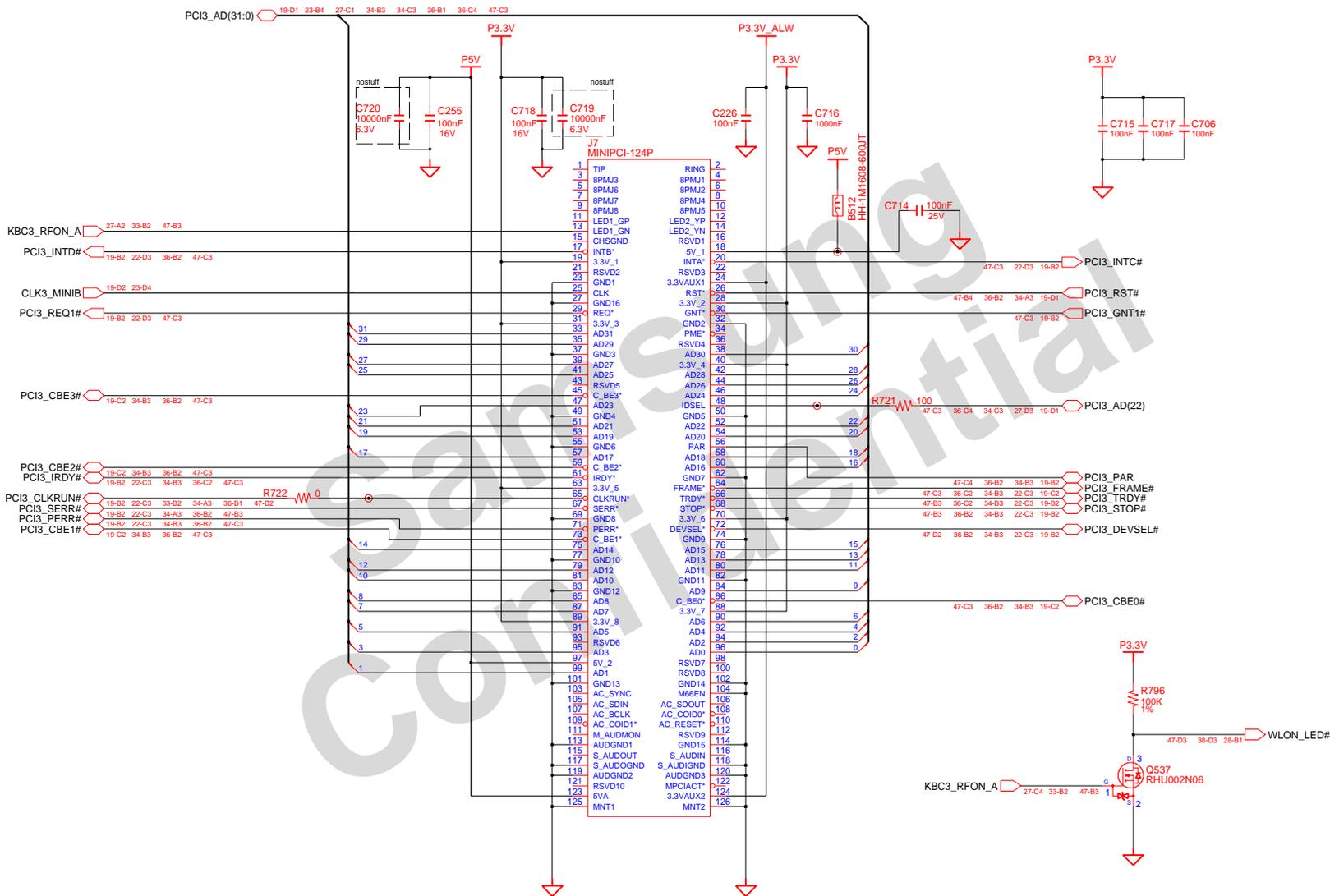


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	LCD / TV-OUT		PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	26	OF 47

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FOR WIRELESS LAN

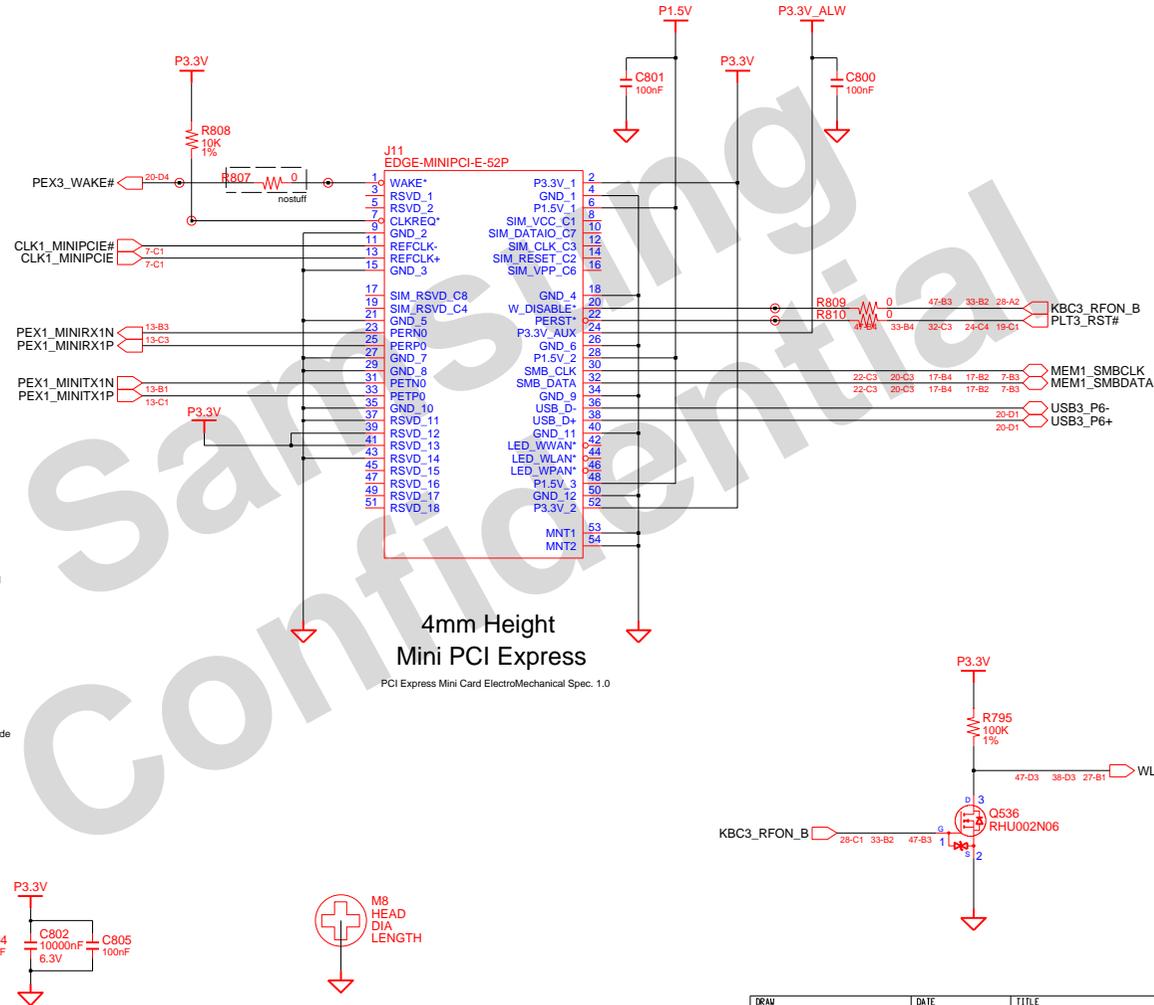


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN MINI PCI	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE		

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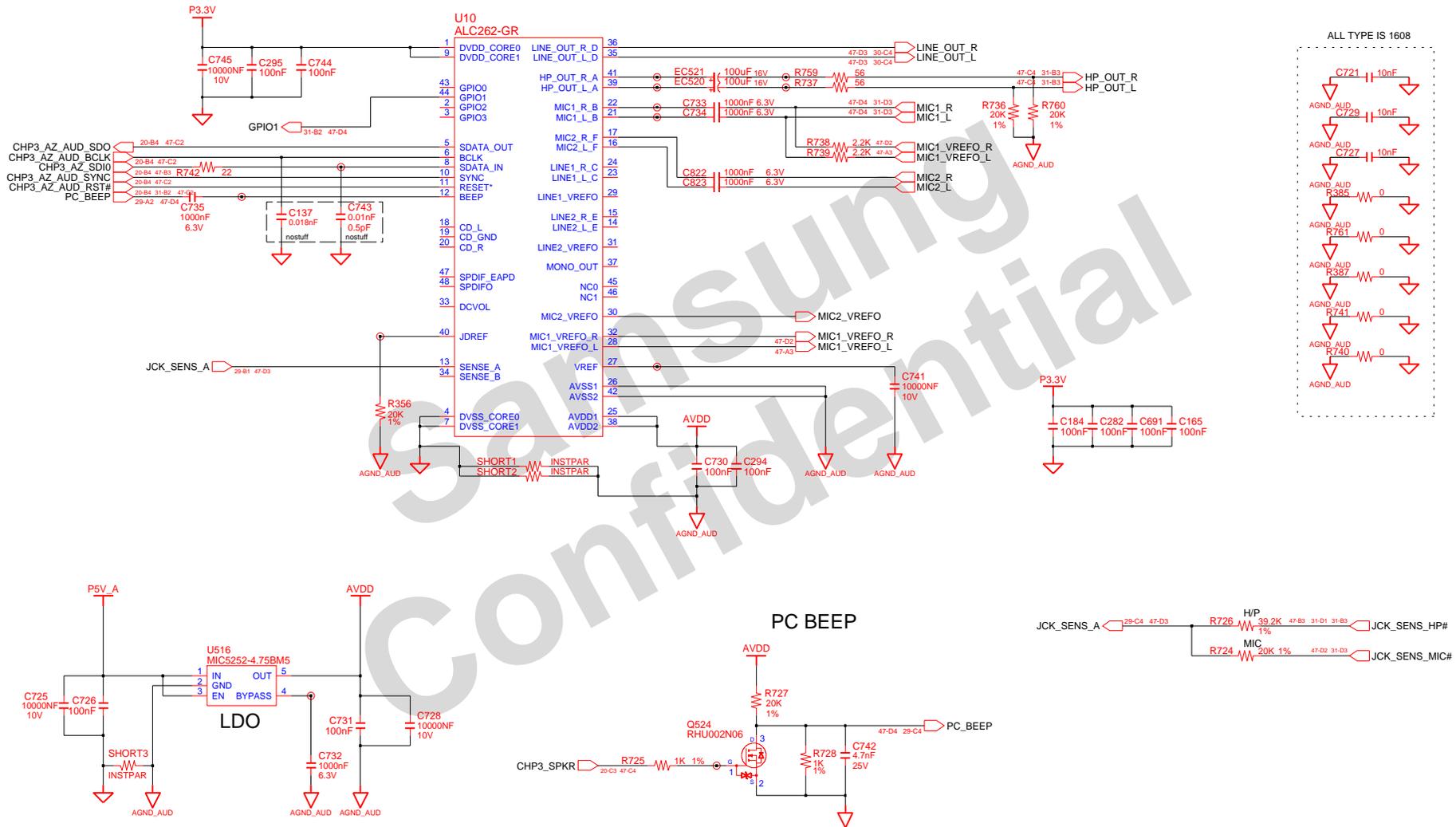
FOR MINICARD(OPTION)



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN MINI CARD	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE		LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 28 OF 47		

SAMSUNG PROPRIETARY

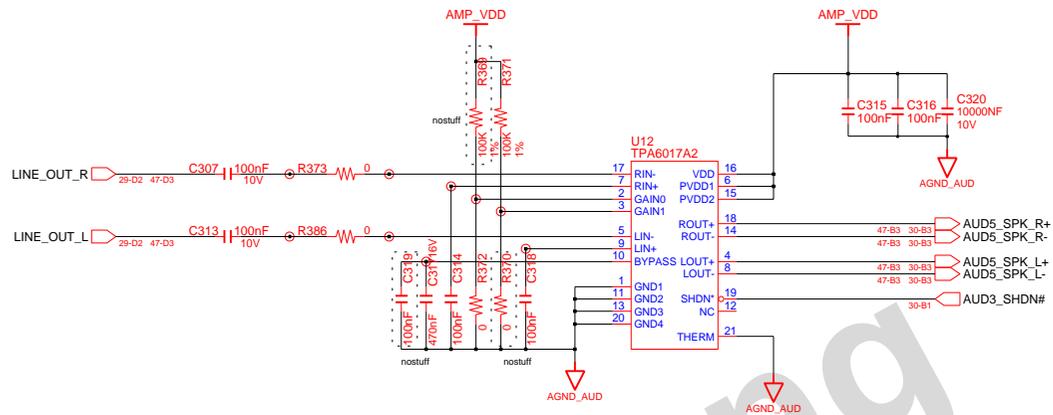
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DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	29	OF 47

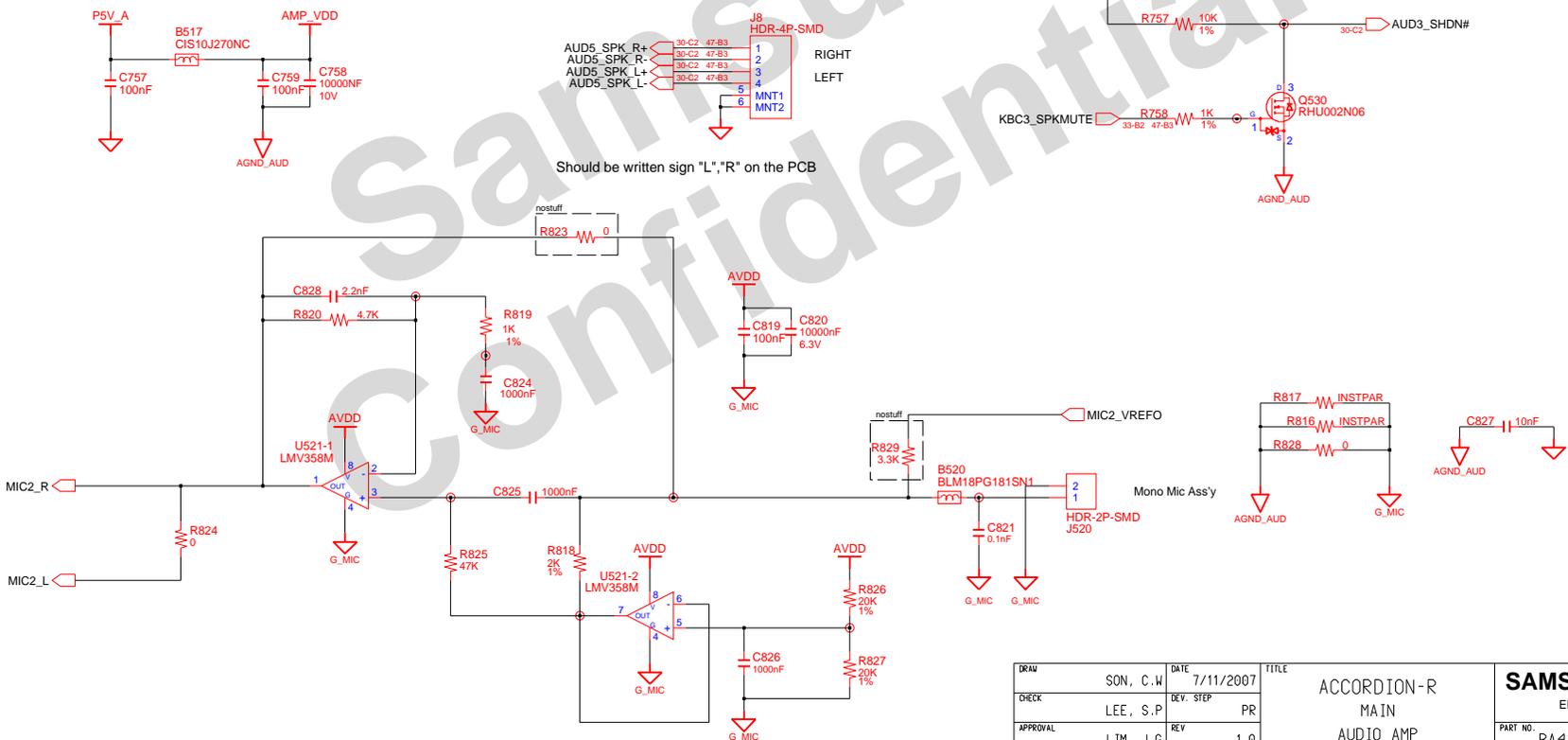
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AMP_VDD

INTERNAL STEREO SPEAKERS



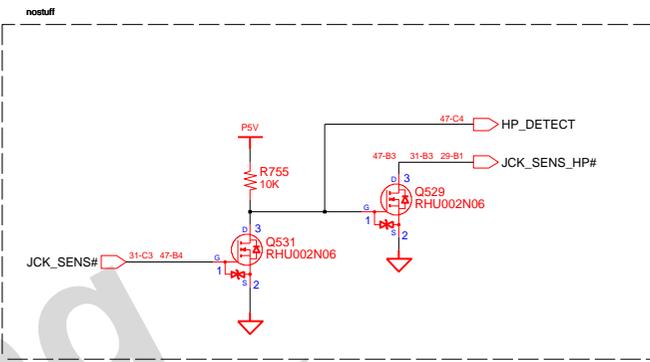
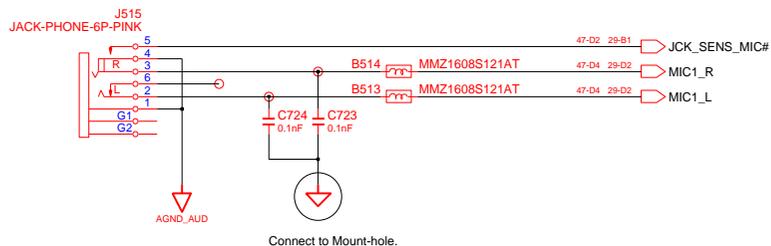
Should be written sign "L","R" on the PCB

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN AUDIO AMP	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 30 OF 47		

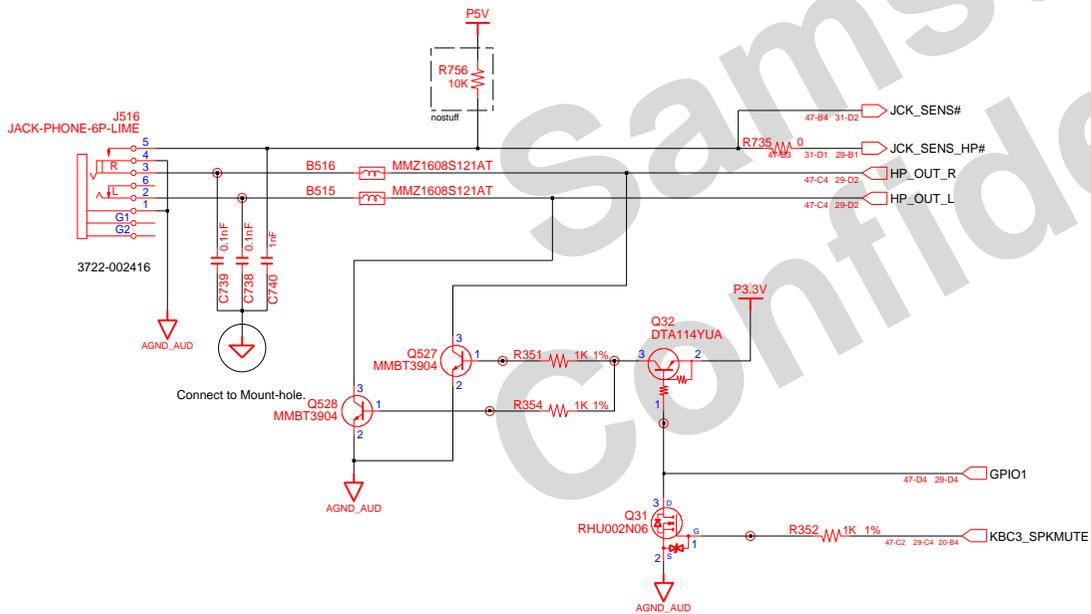
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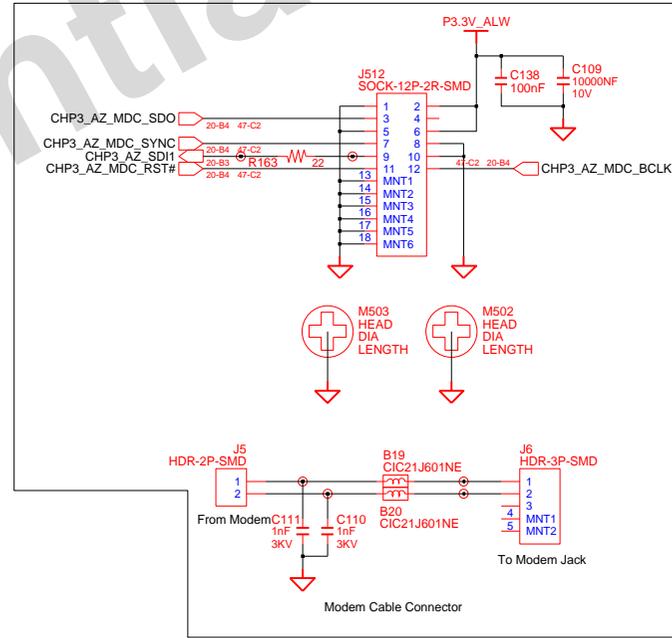
MIC JACK



HEADPHONE



MDC Connector (OPTION)

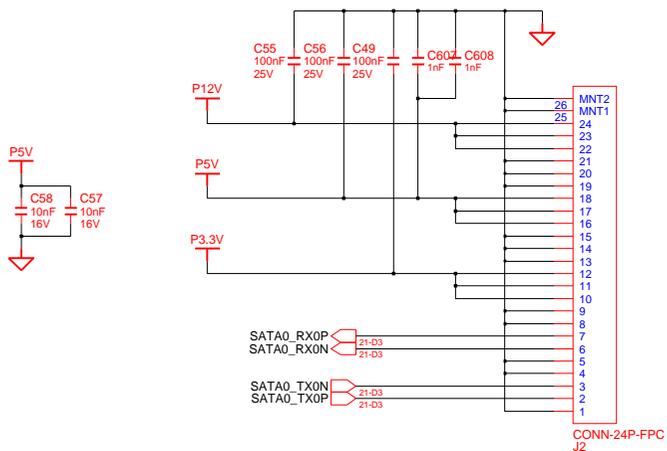


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	AUDIO / MDC CONN		PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	31	OF 47

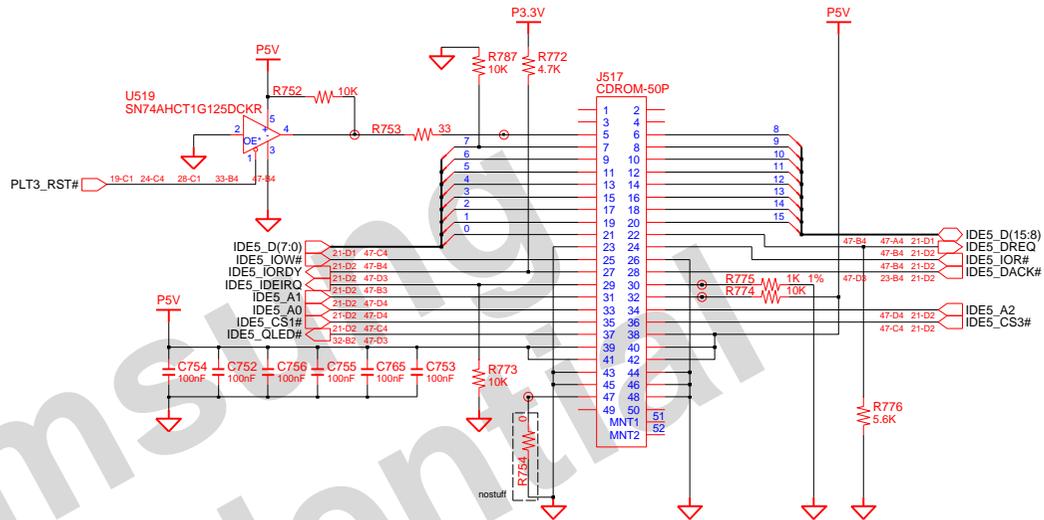
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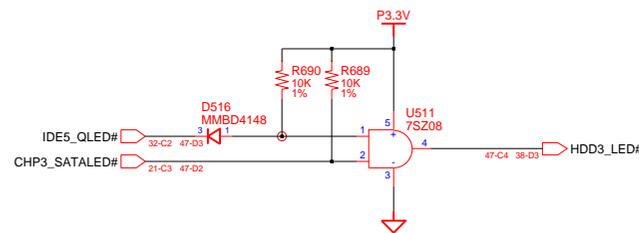
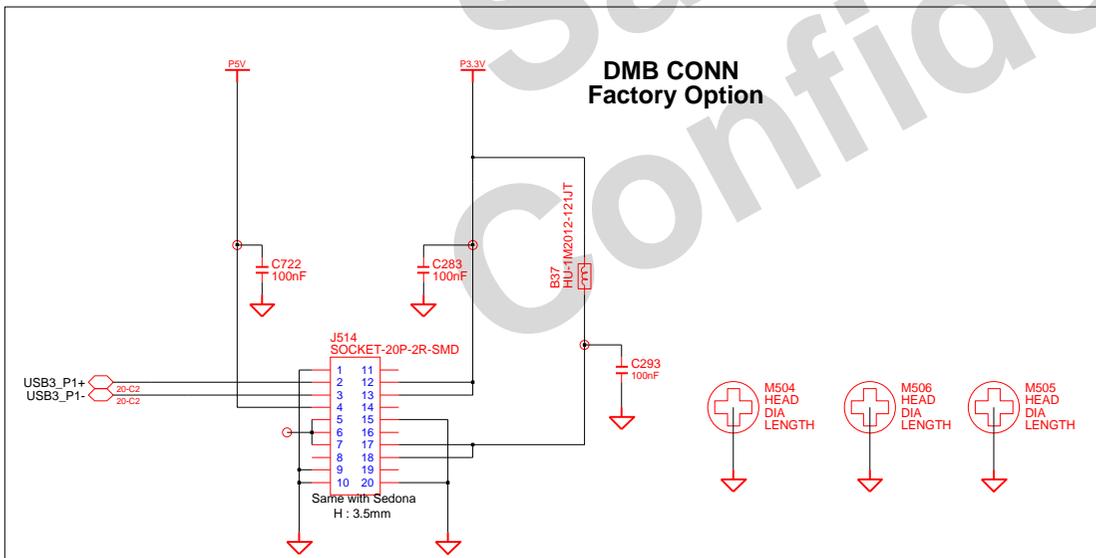
HDD CONN



CD CONN



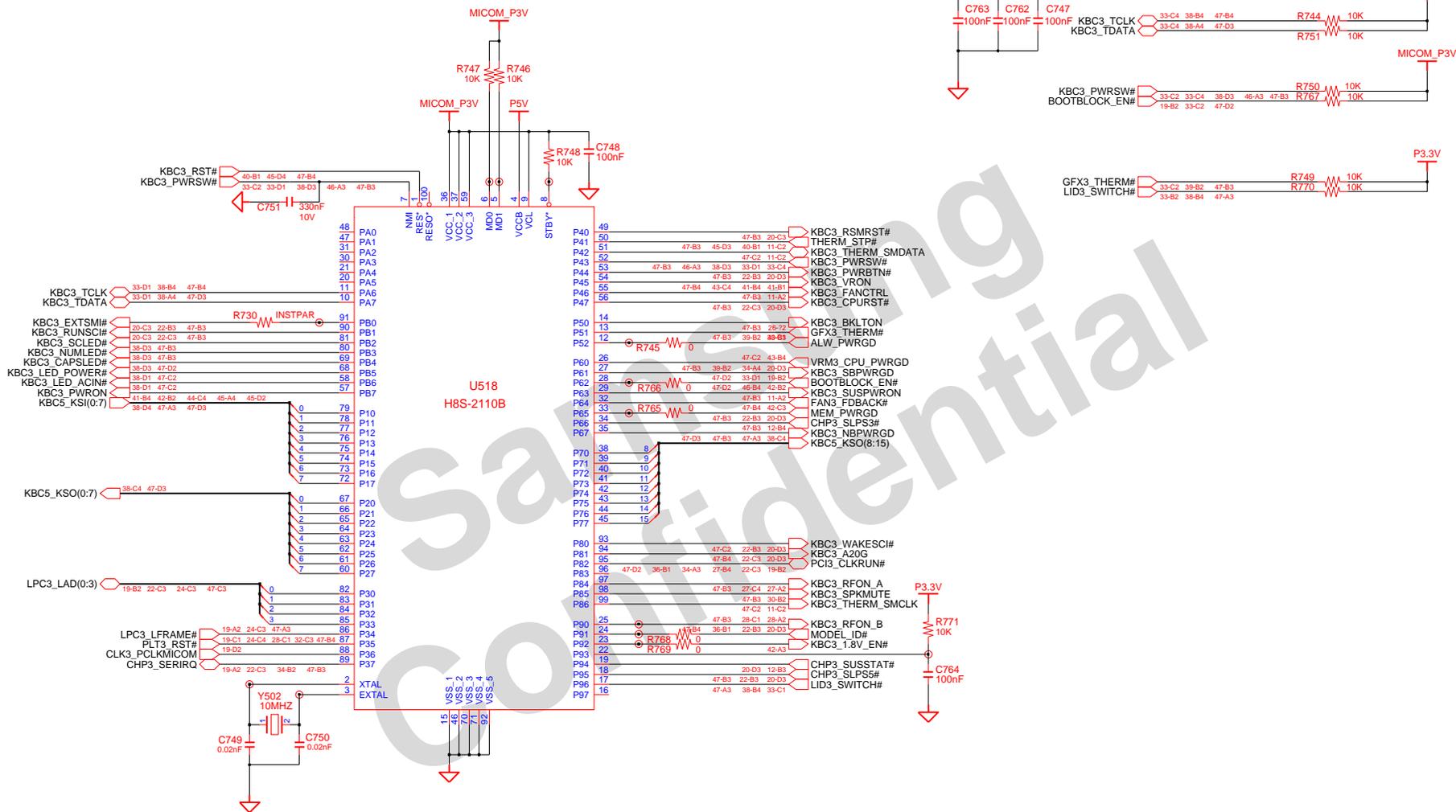
**DMB CONN
Factory Option**



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN HDD/ODD/DMB	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	32	OF 47

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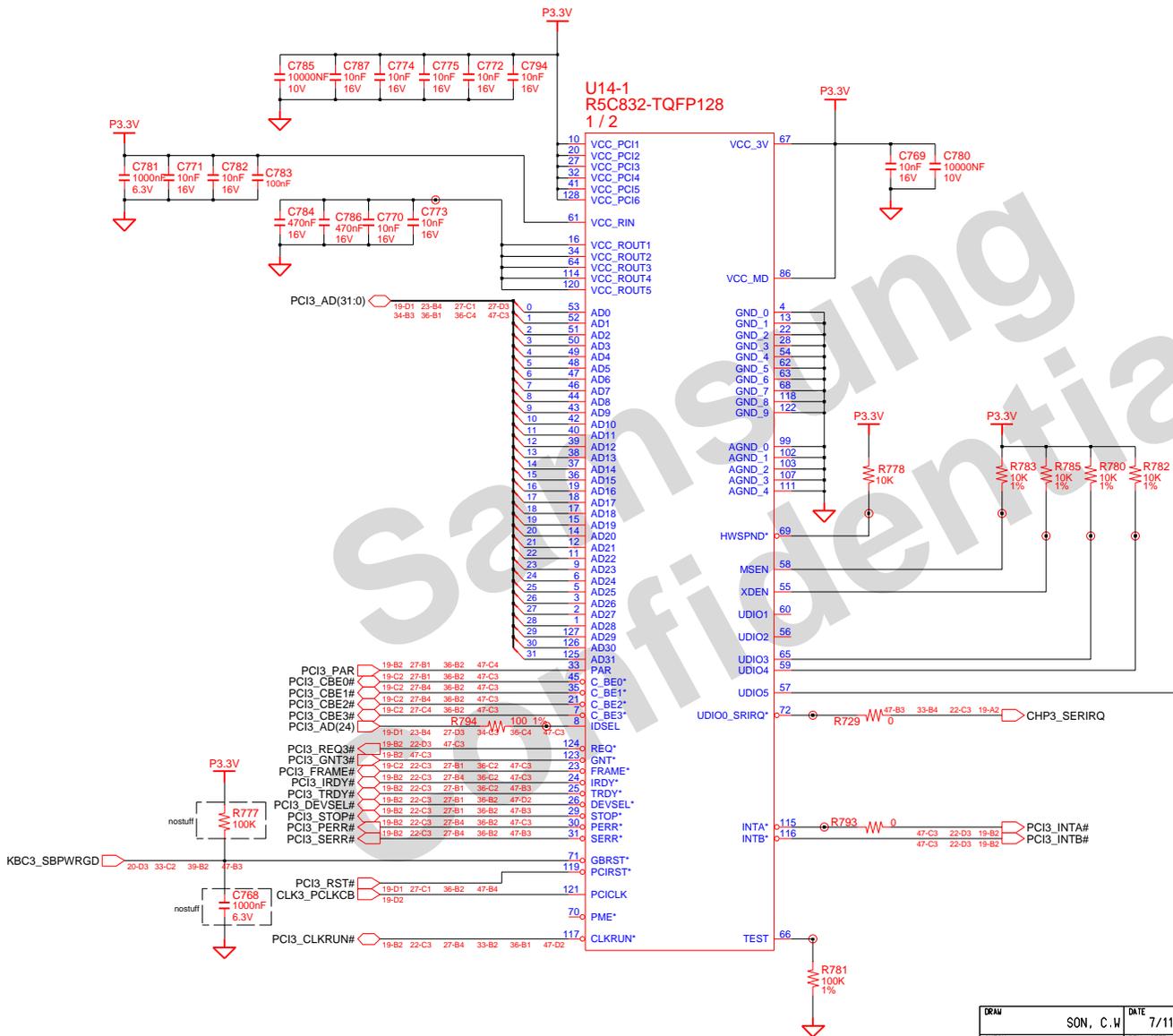
MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		MICOM	
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	33	OF 47

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OPTION

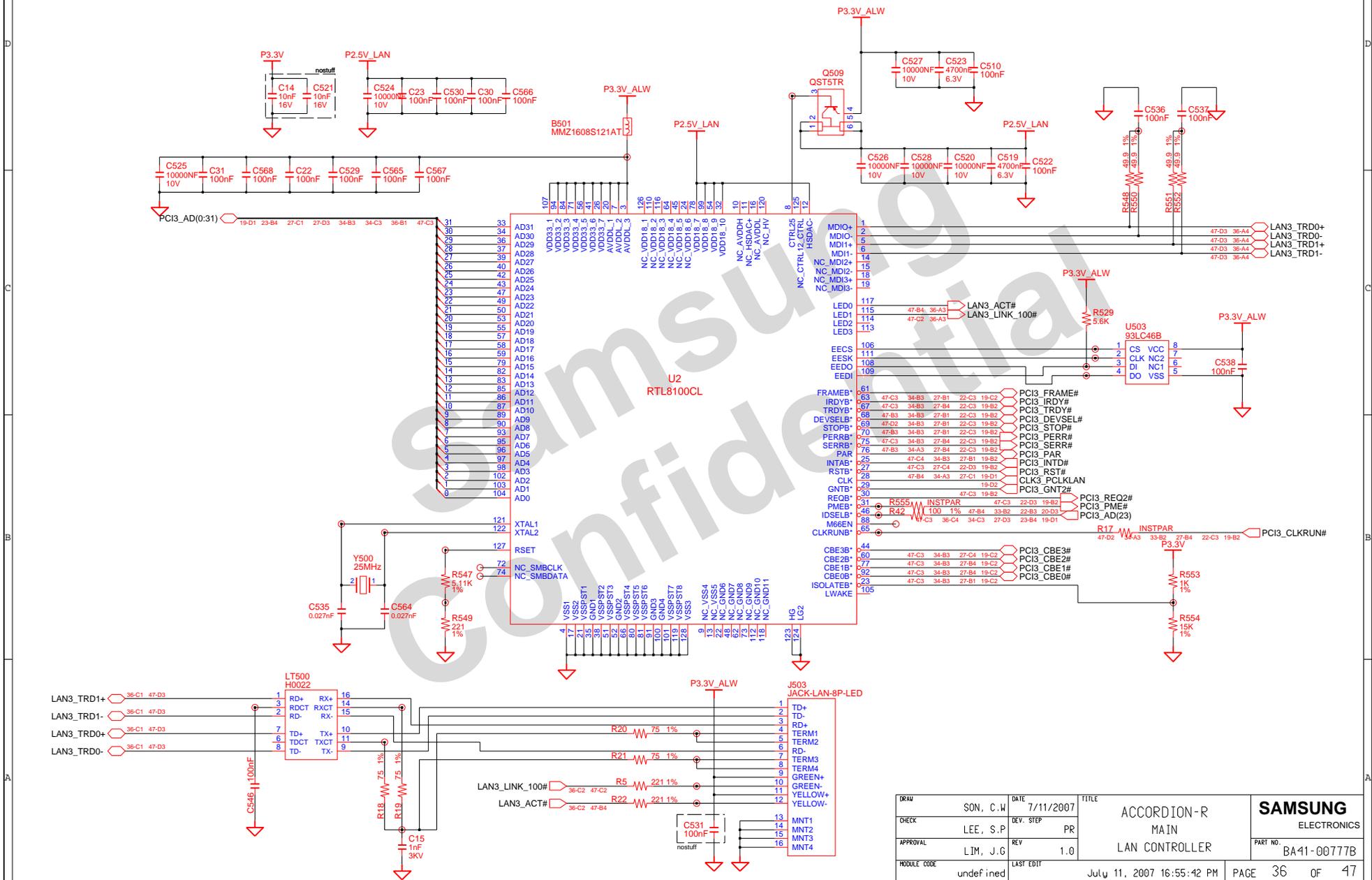


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	5-IN-1 CONTROLLER(1/2)	PART NO.	
APPROVAL	LIM, J.G	REV	1.0		BA41-00777B	
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	34	OF 47

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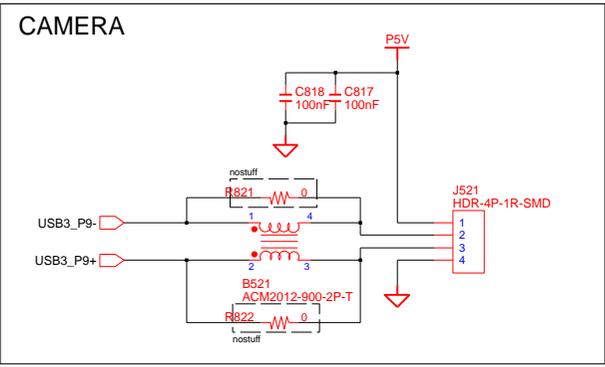
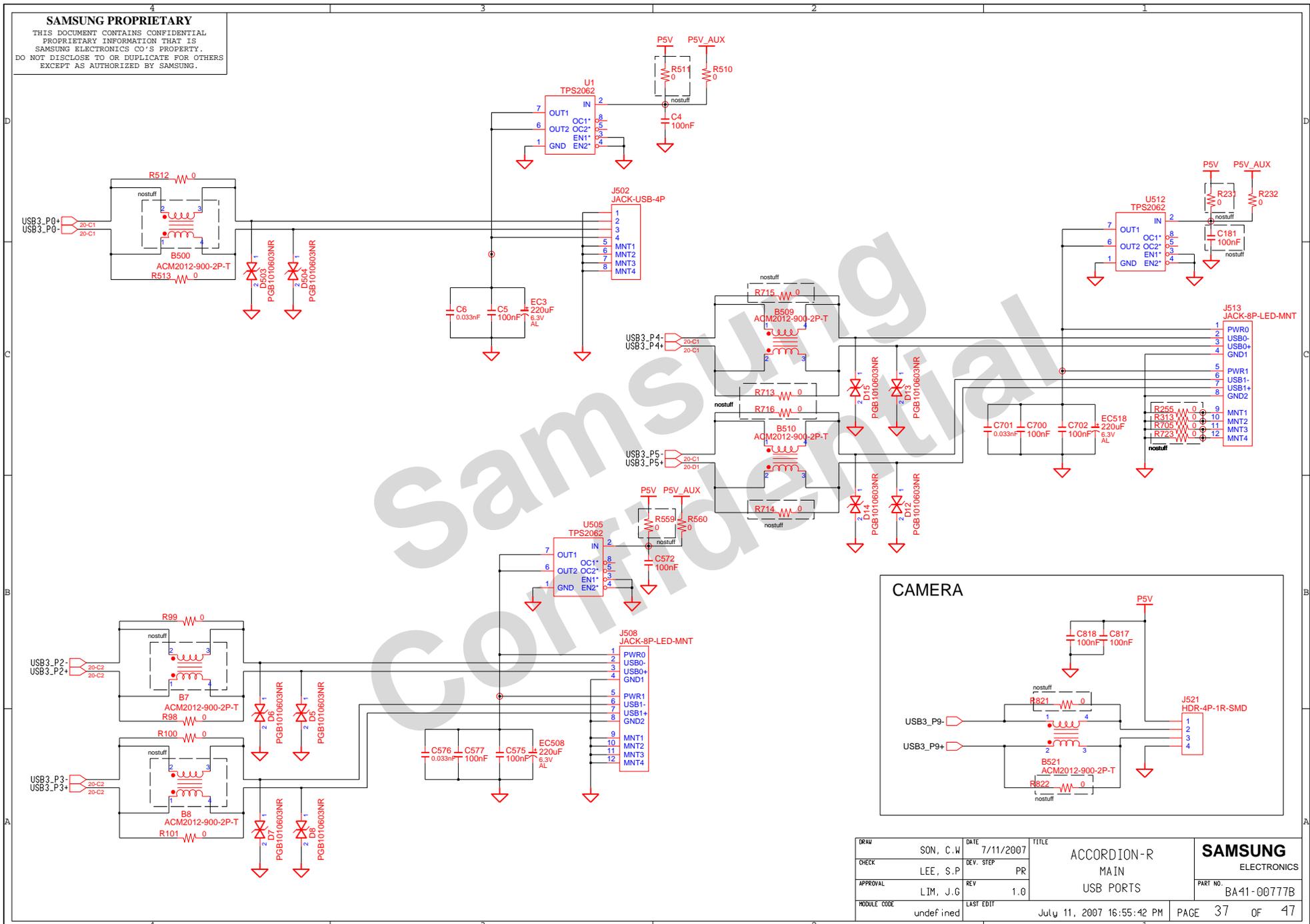
LAN Controller (Only 10/100M)



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	36 OF 47	

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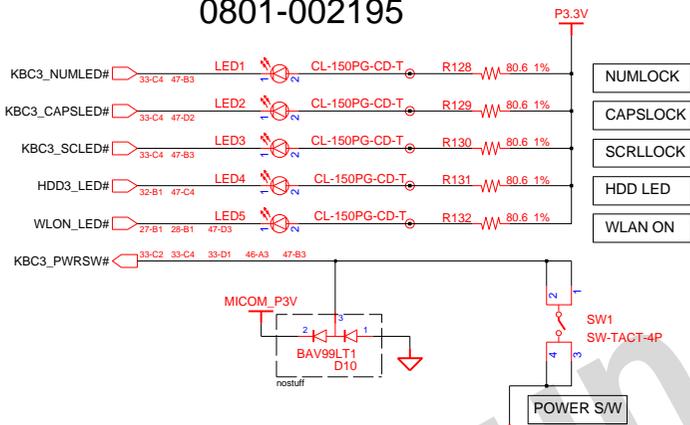
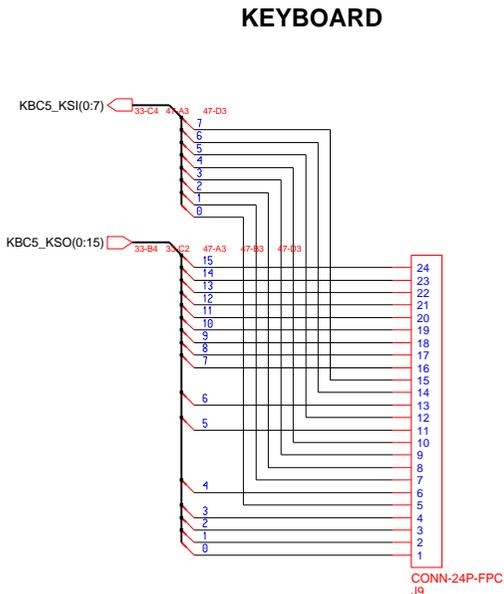
DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN USB PORTS	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	37 OF 47	

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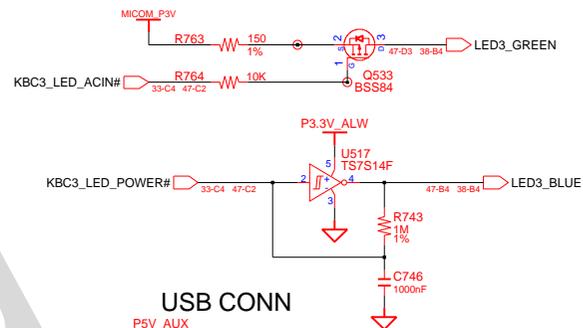
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**LED
0801-002195**

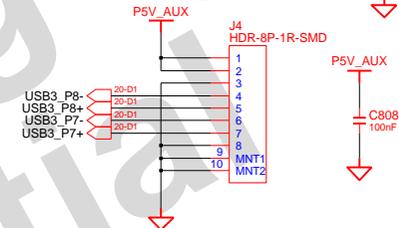
KEYBOARD



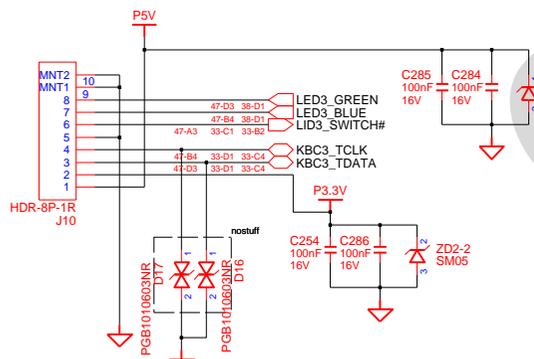
ADAPTERIN/CHARGING LED



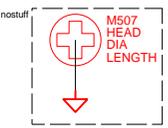
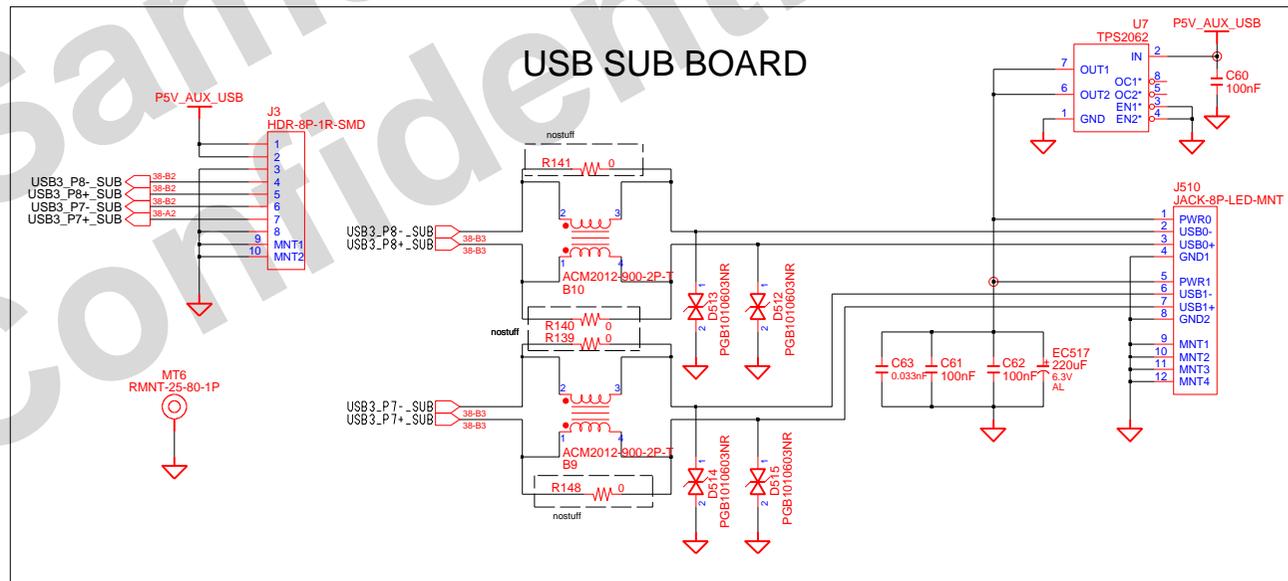
USB CONN



TOUCH PAD



USB SUB BOARD

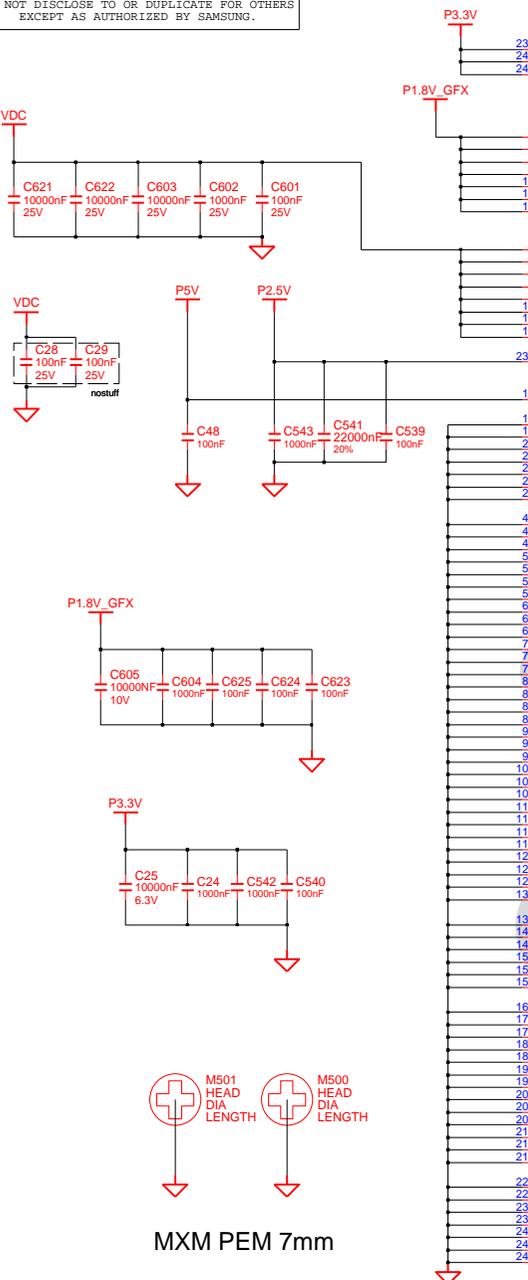


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	REV	KBD/TPAD/LED/SW	
APPROVAL	LIM, J.G	REV	1.0	LAST EDIT	July 11, 2007 16:55:42 PM	PART NO. BA41-00777B
MODULE CODE	undef ined	PAGE	38	OF	47	

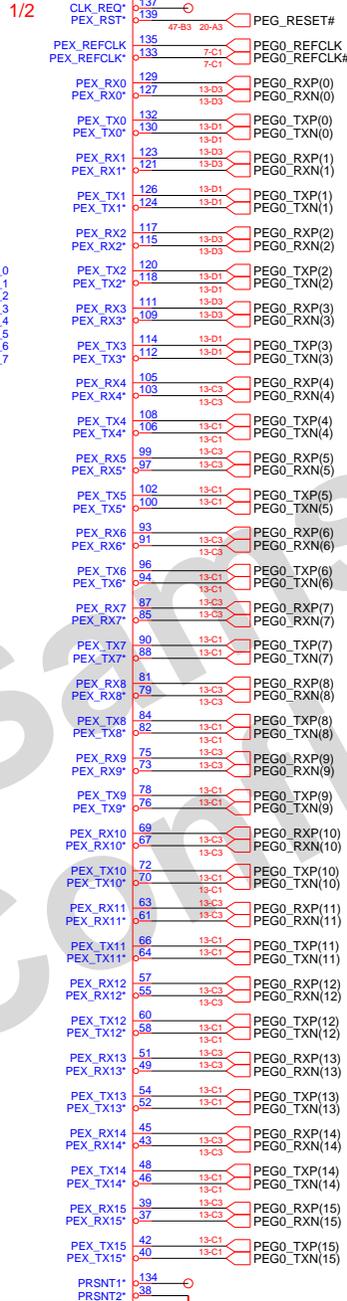
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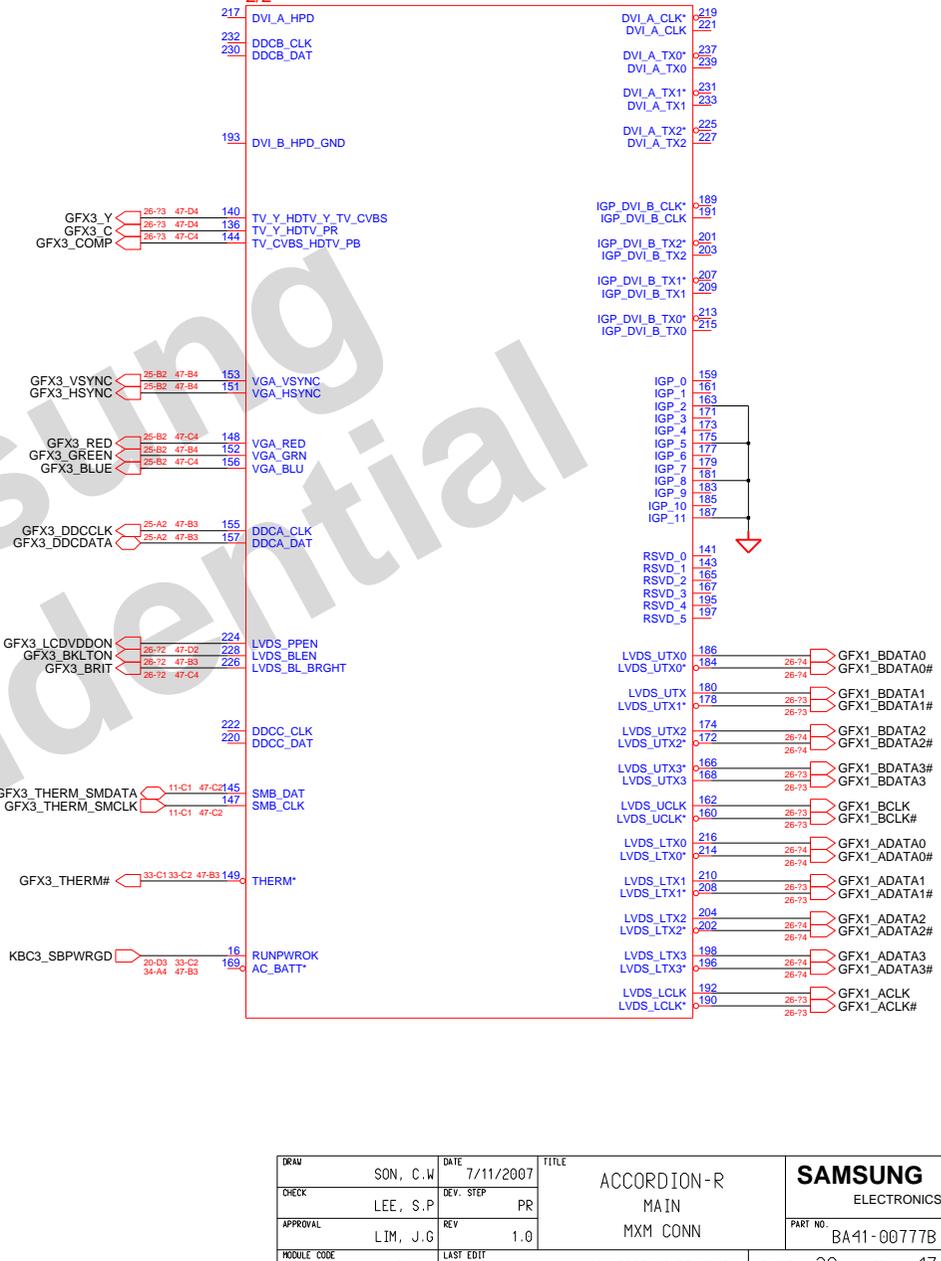
J506-1 SOCKET-242P-2R-SMD



MXM PEM 7mm



J506-2 SOCKET-242P-2R-SMD 2/2



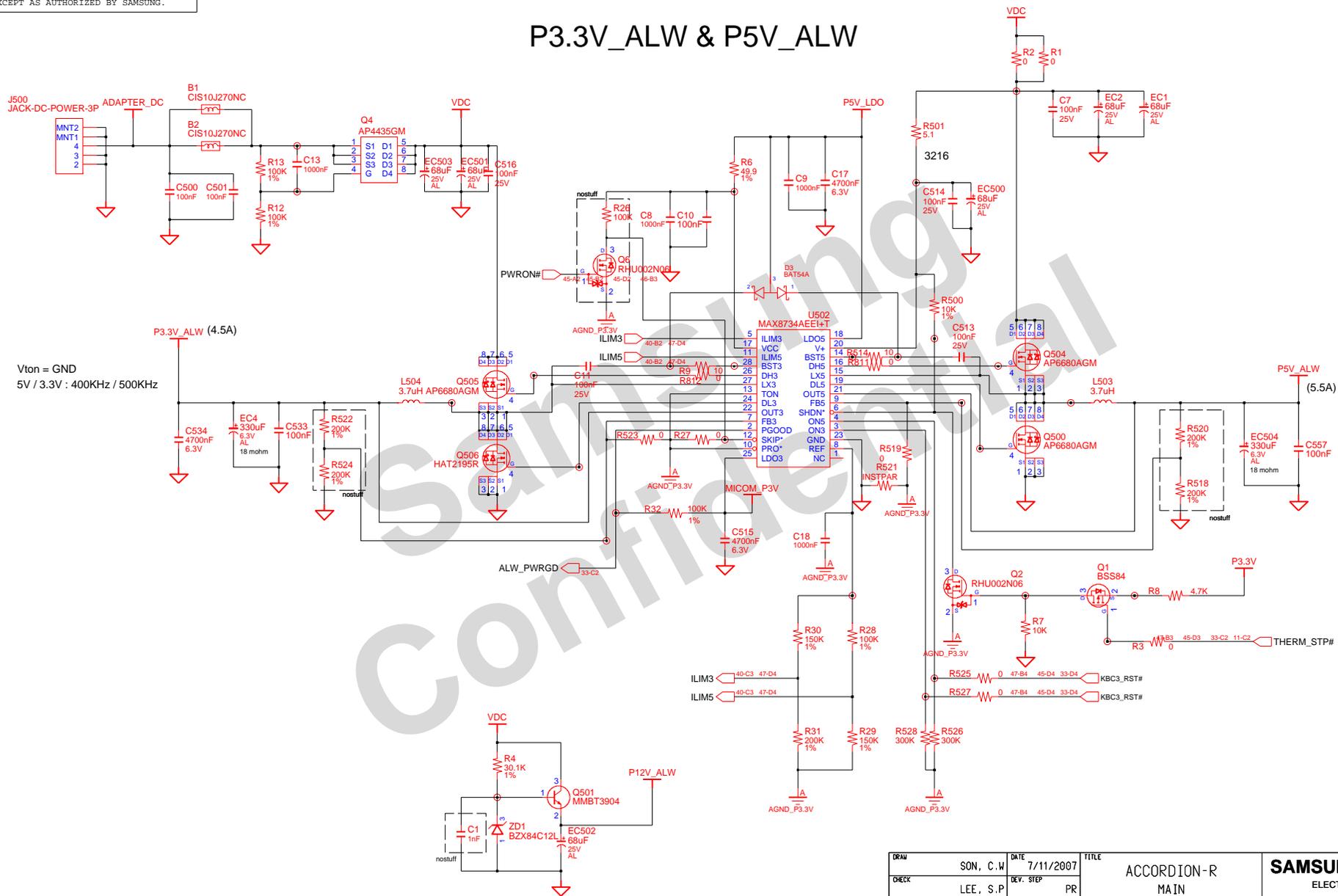
EXT GFX ONLY

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN MXM CONN	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	39 OF 47	

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P3.3V_ALW & P5V_ALW

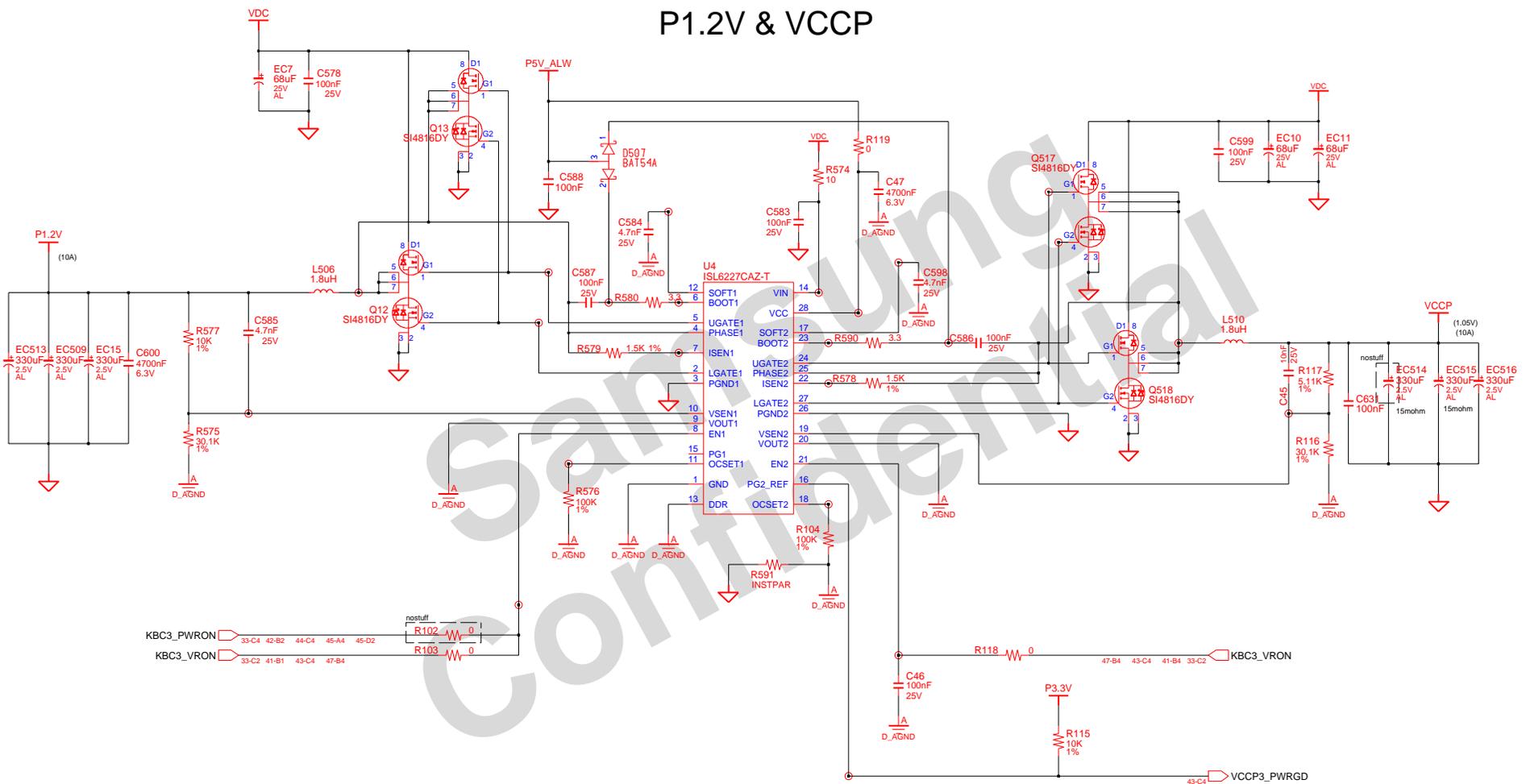


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	40	OF 47
MODULE CODE	undef:ined					

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P1.2V & VCCP

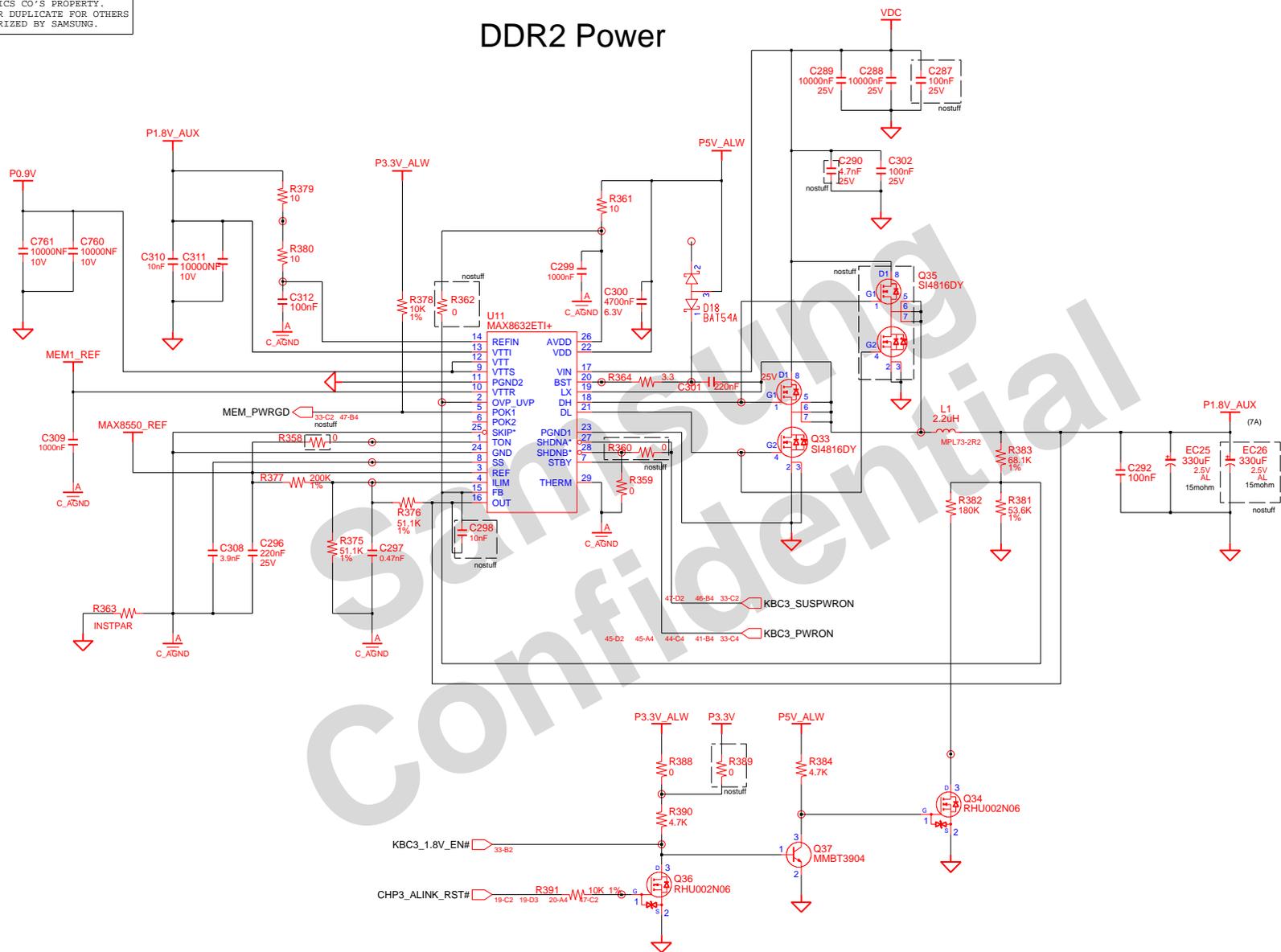


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN 1.2V/VCCP POWER	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 41 OF 47		

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DDR2 Power

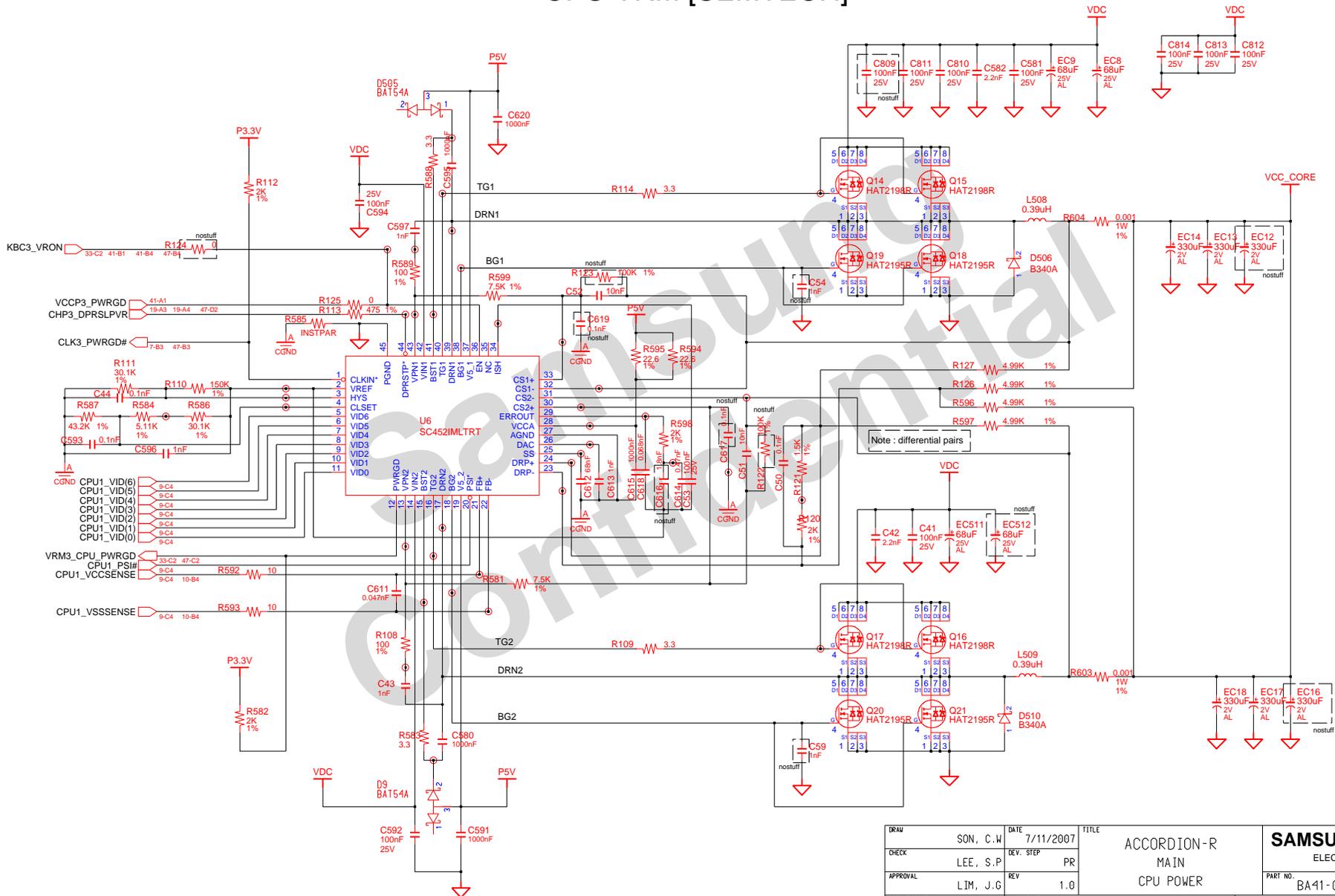


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN DDR2 POWER	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	42 OF 47	

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CPU VRM [SEMTECH]

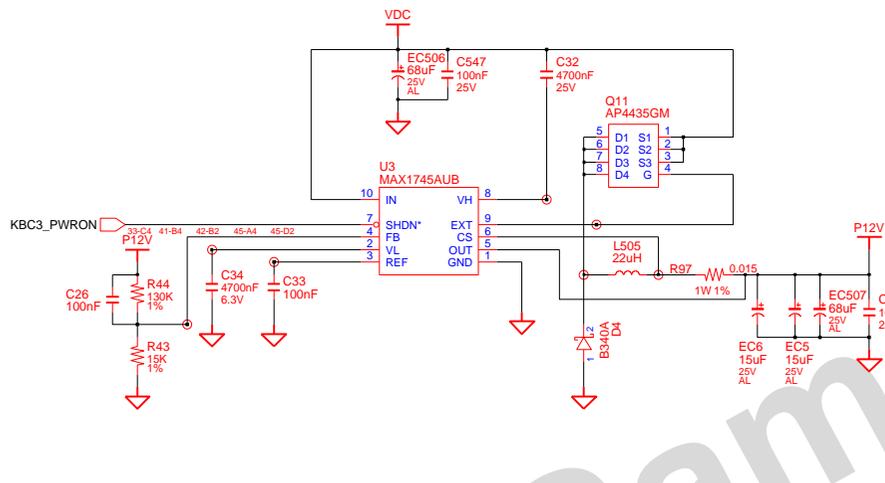


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00777B	
CHECK	LEE, S.P	DEV. STEP	PR				
APPROVAL	LIM, J.G	REV	1.0				
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE			43 OF 47

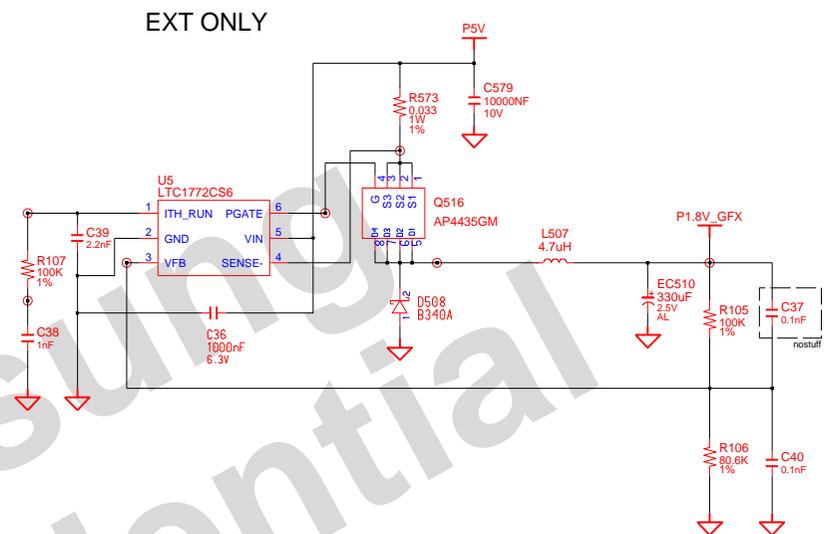
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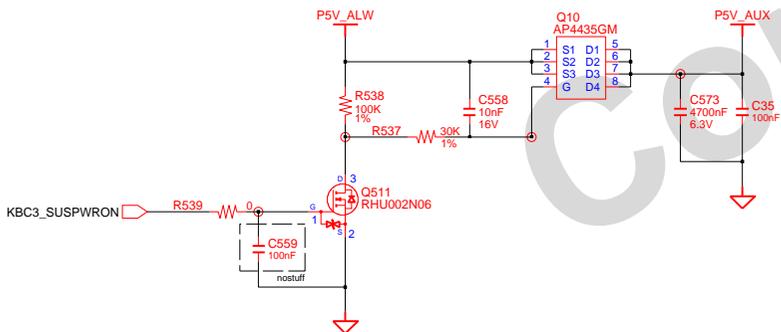
P12V POWER



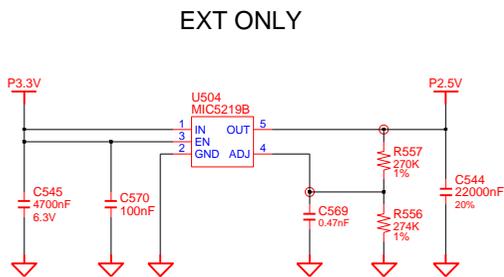
P1.8V POWER FOR MXM CARD



P5V_AUX POWER



P2.5V POWER

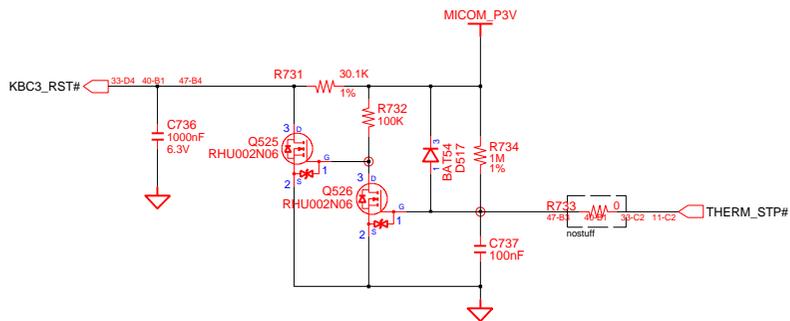


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN P12V / MXM 1.8V POWER	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE 44 OF 47		

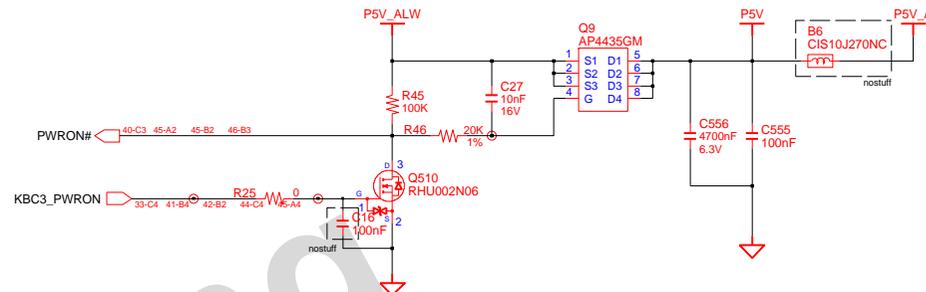
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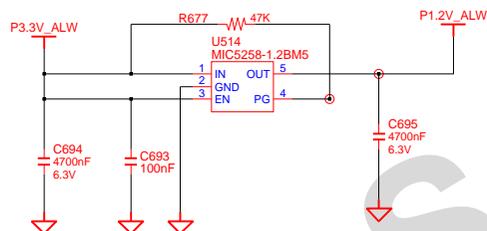
MICOM RESET



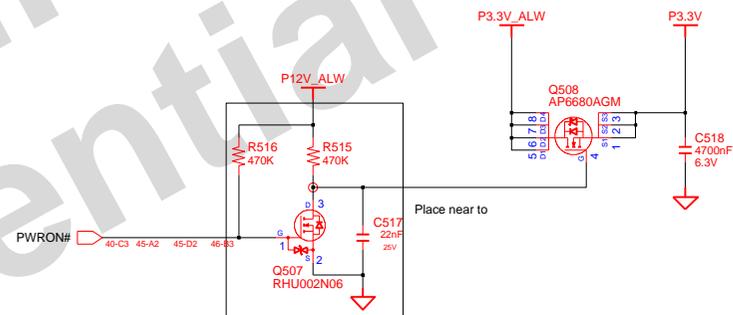
Switched Power On (P5V)



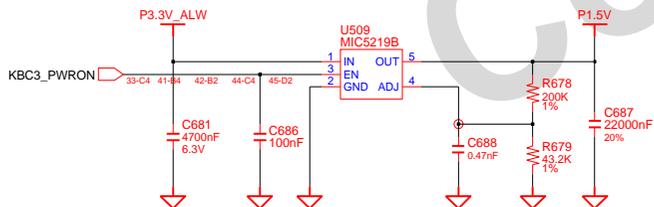
P1.2V_ALW



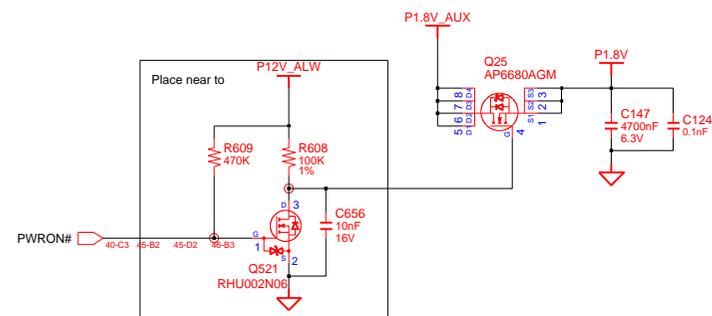
Switched Power On (P3.3V)



P1.5V POWER



Switched Power On (P1.8V)

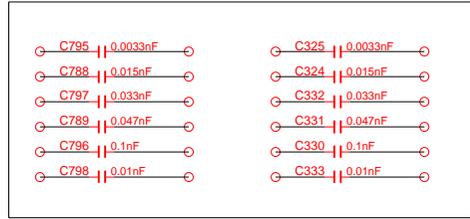
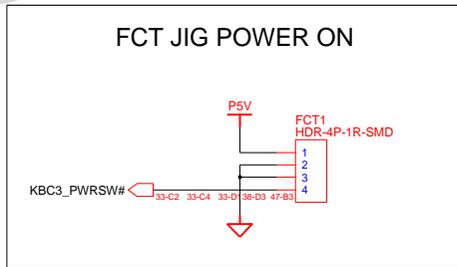
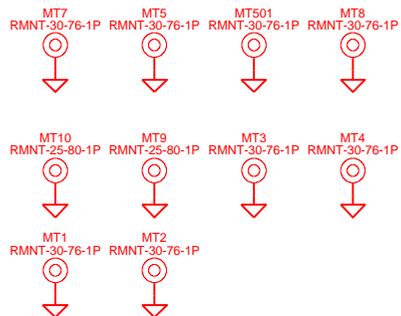
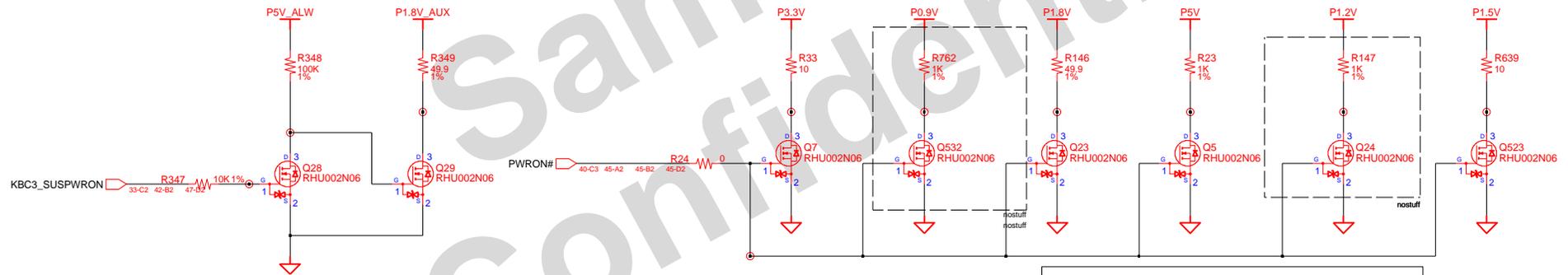
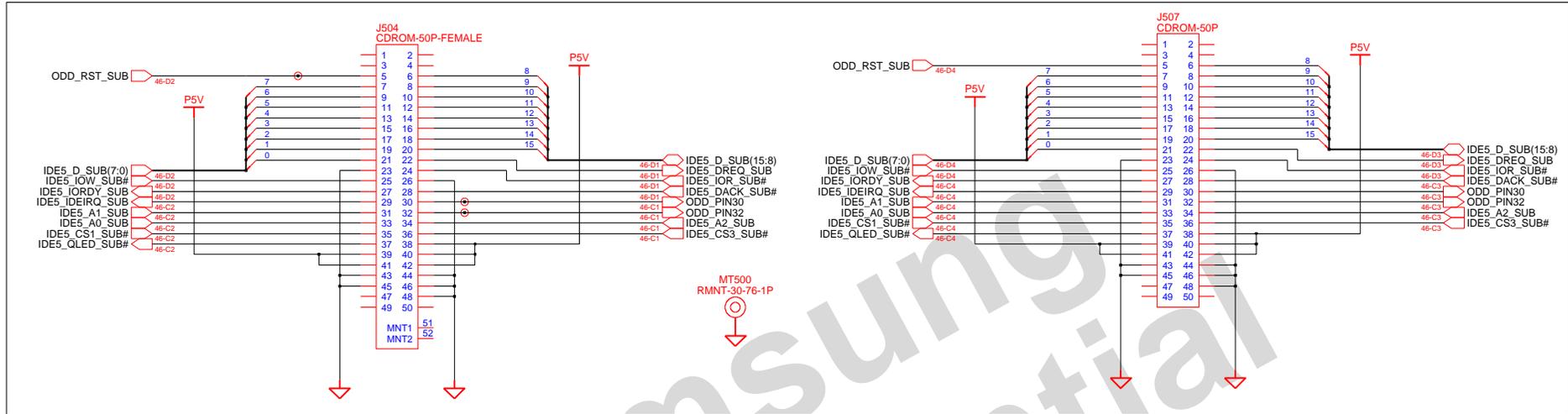


DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	45	OF 47

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ODD IF SUB BOARD



These are for ICT using.

DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	POWER STRAPS/ODD SUB B'D		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-00777B
MODULE CODE	undef ined	LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	46	OF 47

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TP16758OILIM3
TP16759OILIM5
TP16760OTV0_C
TP16761OTV0_Y
TP16762OCFX3_X
TP16763OCFX3_Y
TP16764CMIC1_L
TP16765CMIC1_R
TP16766OIV03_C
TP16767OIV03_Y
TP16768OIDE5_A0
TP16769OIDE5_A1
TP16770OIDE5_A2
TP16754OCPC_BEEP
TP16755OCASDOUT
TP16756OCRT3_RED
TP16747OCFX3_RED
TP16748OHP_OUT_B
TP16749OHP_OUT_P
TP16750OCD_BRIT
TP16751OCPC3_PAR
TP16752OSMB3_CLK
TP16753OIV0_COMP
TP16737OVGA3_RED

TP16739OCHP3_SPKR
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TP16837OHP3_SA1LED#
TP16838OCFX3_LCVDVDDON
TP16839OJCK_SENS_MIC#
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TP16849OCB3_MD_DATA5_XD
TP16850OCB3_MD_DATA6_XD
TP16851OCB3_MD_DATA7_XD
TP16852OHP3_ALINK_RST#
TP16853OHP3_AZ_AUD_SDO
TP16854OHP3_AZ_MDC_SDO
TP16855OKBC3_LED_P0HER#
TP16856OCB3_MS_BS_SD_CMD
TP16857OHP3_AZ_AUD_BCLK
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TP16868OKBC3_THERM_SMDATA
TP16869OCB3_MS_IN#_XD_CD#
TP16870OCB3_SD_WP#_XD_R_B#
TP16871OCB3_MD_DATA0_MS_SDIO
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TP16876OAMP_VDD

TP16883OAGND_AUD
TP16884OAVDD_SATA

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TP16892OADAPTER_DC
TP16893OADAPTER_DC
TP16894OADAPTER_DC
TP16895OADAPTER_DC
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TP16897OAGND

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TP16907OGROUND
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TP16915OCD_VDD5V
TP16916OCD_VCC
TP16920ONEM1_REF
TP16927OMICOM_P3V
TP16928OAX8550_REF
TP16932OP12V
TP16933OP12V
TP16936OP0_3V
TP16937OP0_3V
TP16940OP1_2V
TP16941OP1_2V
TP16944OP1_5V
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TP16951OP1_8V
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TP16953OP2_5V
TP16956OP5V_A
TP16957OP5V_A
TP16960OP5V_ALW
TP16961OP5V_ALW
TP16964OP5V_LDO
TP16968OP12V_ALW
TP16969OP12V_ALW
TP16972OPRTC_BAT

TP16976OP1_2V_ALW
TP16977OP1_2V_ALW
TP16980OP1_8V_AUX
TP16981OP1_8V_AUX
TP16984OP2_5V_LAN
TP16985OP2_5V_LAN
TP16988OP3_3V_ALW
TP16989OP3_3V_ALW
TP16993OCPIE_VDDOR
TP16999OPLL_VDD_ATA
TP17000OTV_GND
TP17004OVDC
TP17008OVCCP
TP17012OVCC_CORE
TP17016OXTL_VDD_ATA
TP17017OXTL_VDD_ATA
TP17019OXTL_VDD_ATA

PCB REVISION CONTROL (ICT)				
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2	1-2	2007.04.06	1.0	PV
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



DRAW	SON, C.W	DATE	7/11/2007	TITLE	ACCORDION-R MAIN TEST POINTS	SAMSUNG ELECTRONICS PART NO. BA41-00777B
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE		LAST EDIT	July 11, 2007 16:55:42 PM	PAGE	47 OF 47	