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SuZhou

CPU : Intel Arrandale
 Chip Set : Intel Ixex Peak(PM55)
 GFX : N11P / M-GE1(40nm)
 Remarks : Calpella Platform

Model Name : SuZhou-MH
 PBA Name : MAIN
 PCB Code : BA41-01190A
 Dev. Step : PR
 Revision : 1.0
 T.R. Date : 2009.11.16

Design	CHECK	APPROVAL
Xiaohong Zhang	Rujin Zheng	BC Lee

■ **Owner : SEC Mobile R & D** **Signature :** **X**

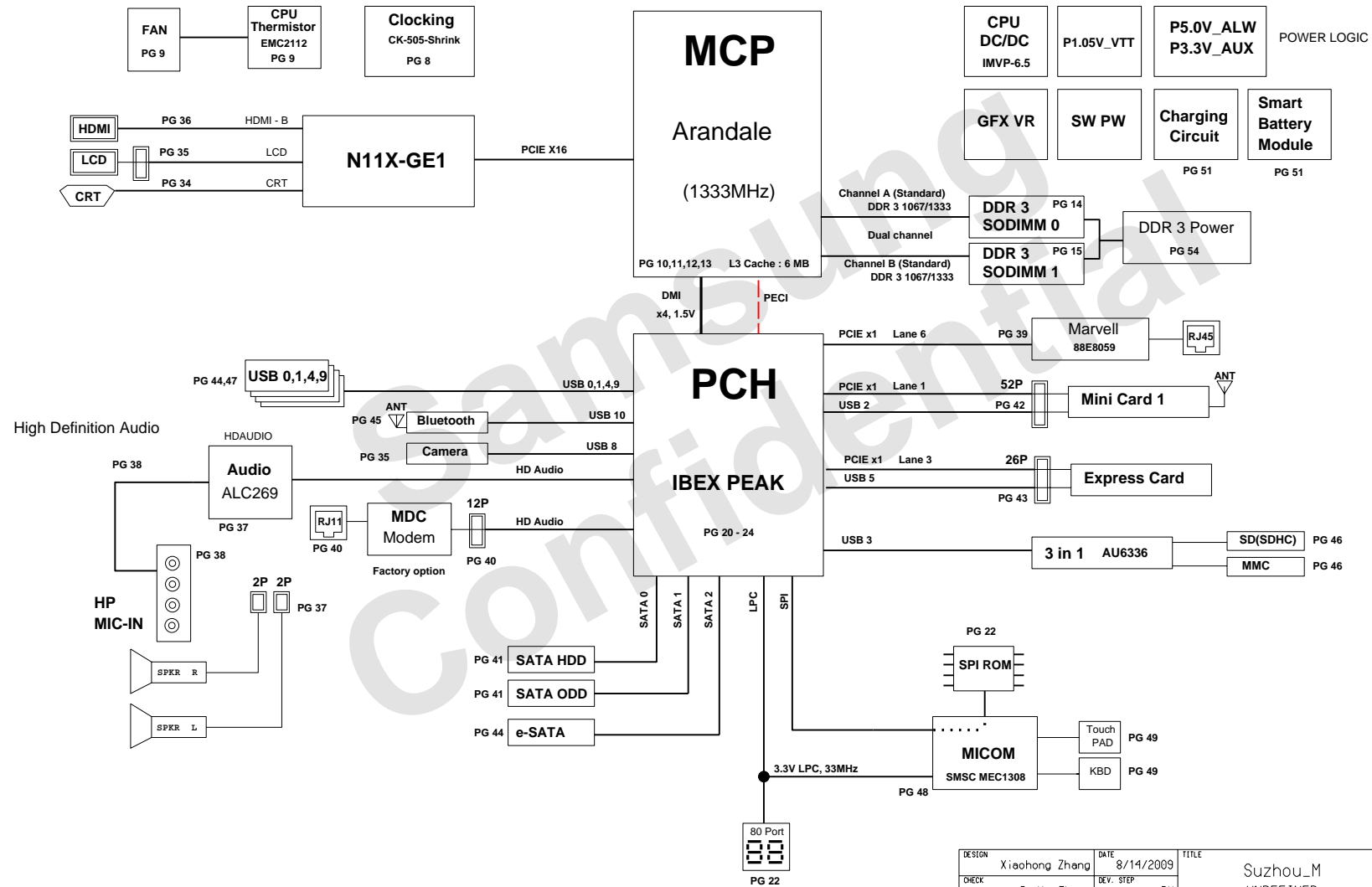
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DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	1 OF 62	

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BLOCK DIAGRAM



DESIGN	Xiaohong Zheng	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A	
CHECK	Rujin Zheng	DEV. STEP	PV	UNDEF INED			
APPROVAL	BC LEE	REV	1.0	UNDEF INED			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM				
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5) S3
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5) S0
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarkfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak S0

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	IBEX PEAK	

LCD Panel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I ² C / SMB Address			
Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

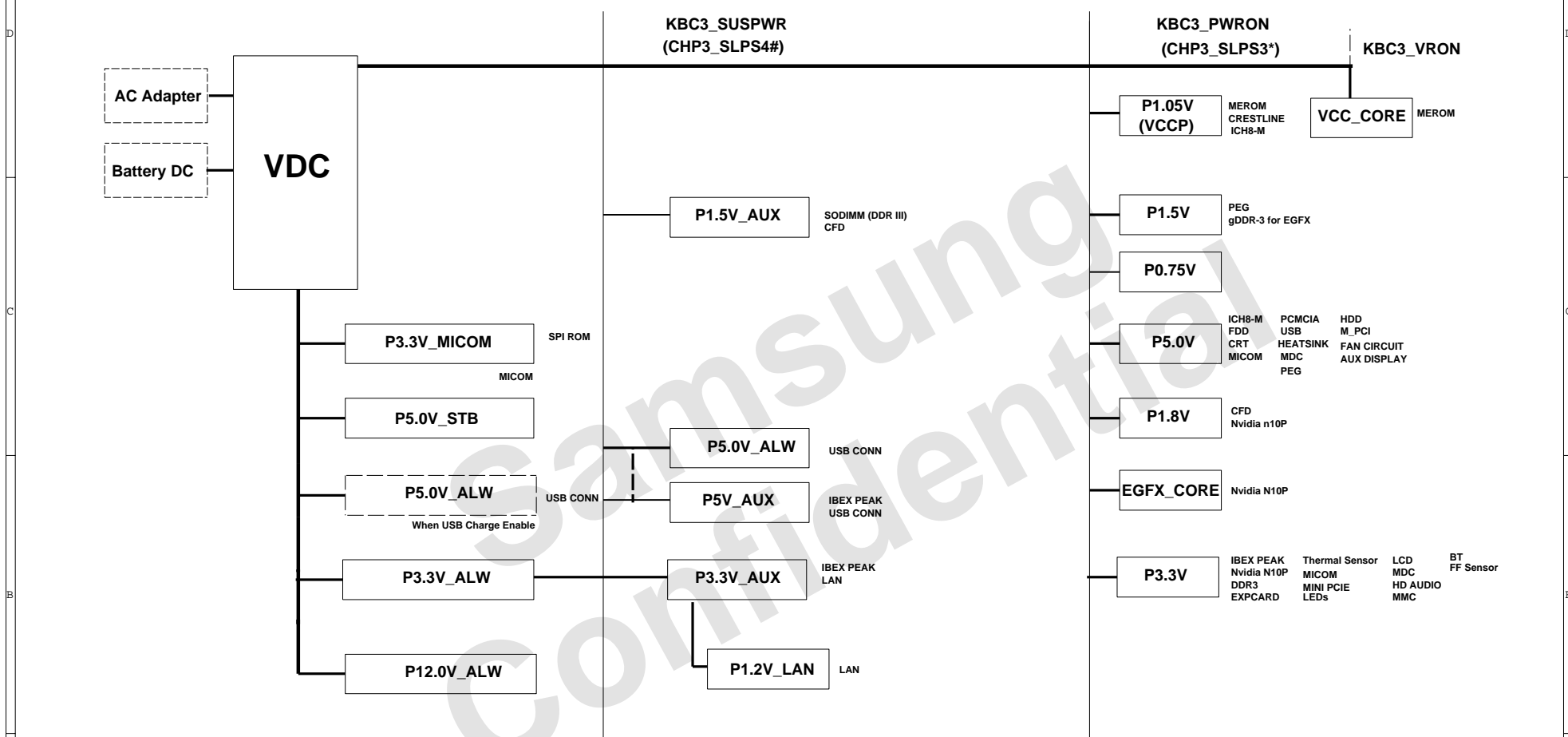
USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Mini PCI Express 1	3	EXPRESS CARD
3	NC	4	NC
4	SYSTEM PORT 4	5	NC
5	EXPRESS CARD	6	NC
6	NC (N/A WITH HM55)	7	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)	8	NC (N/A WITH HM55)
8	Multi Memory Card Controller		
9	SYSTEM PORT 9		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA

DESIGN	Xiaohong Zhang	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEF INED	
APPROVAL	BC LEE	REV	1.0		UNDEF INED	PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	3	OF 62

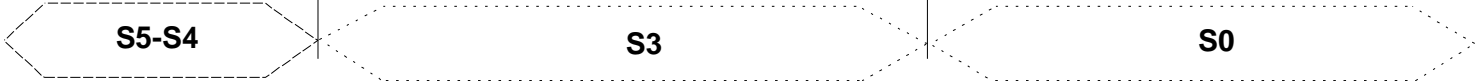
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POWER DIAGRAM Rev 0.1



Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---



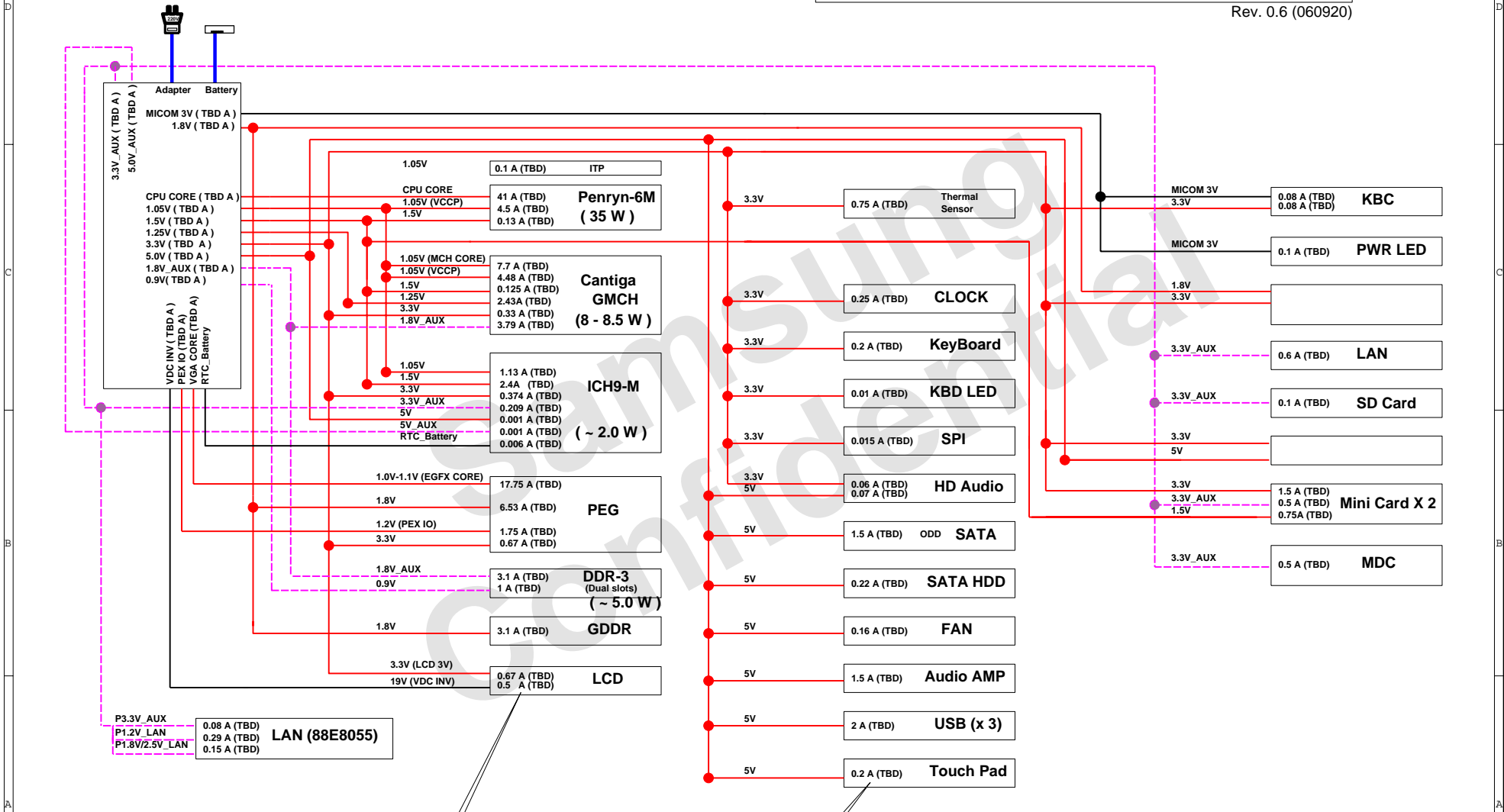
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APPROVAL	BC LEE	REV	1.0	UNDEFINED	PART NO. BA41-01190/1/2A	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	4 OF 62	

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



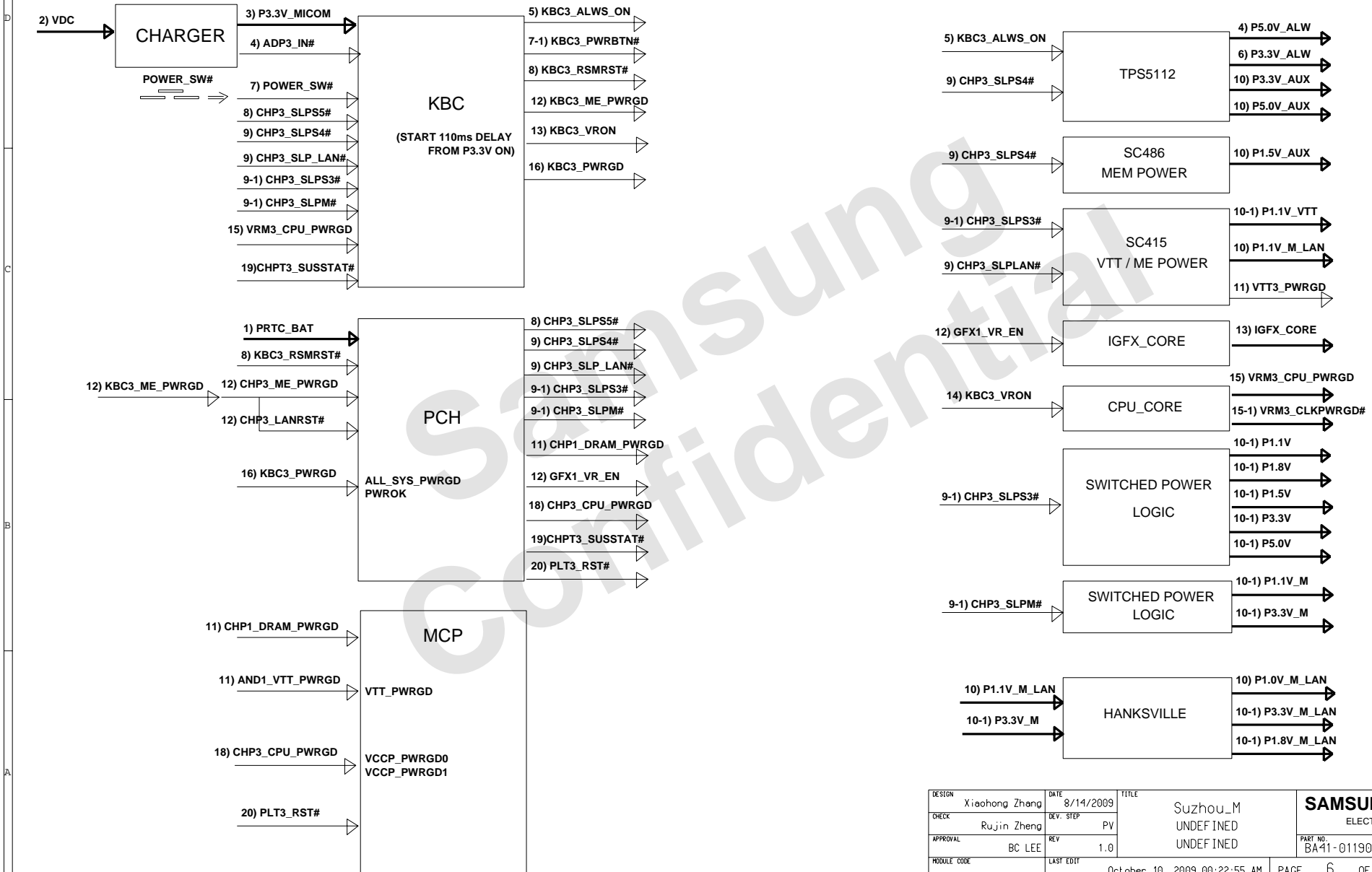
Value by Datasheet/Application notes (Value by measurement)

DESIGN	Xiaohong Zheng	DATE	8/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		UNDEFINED	
APPROVAL	BC LEE	REV	1.0		UNDEFINED	
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PRELIMINARY

POWER SEQUENCE Rev. 0.5



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CHECK	Rujin Zheng	DEV. STEP	PV	UNDEF INED		
APPROVAL	BC LEE	REV	1.0	UNDEF INED	PART NO. BA41-01190/1/2A	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	6 OF 62	

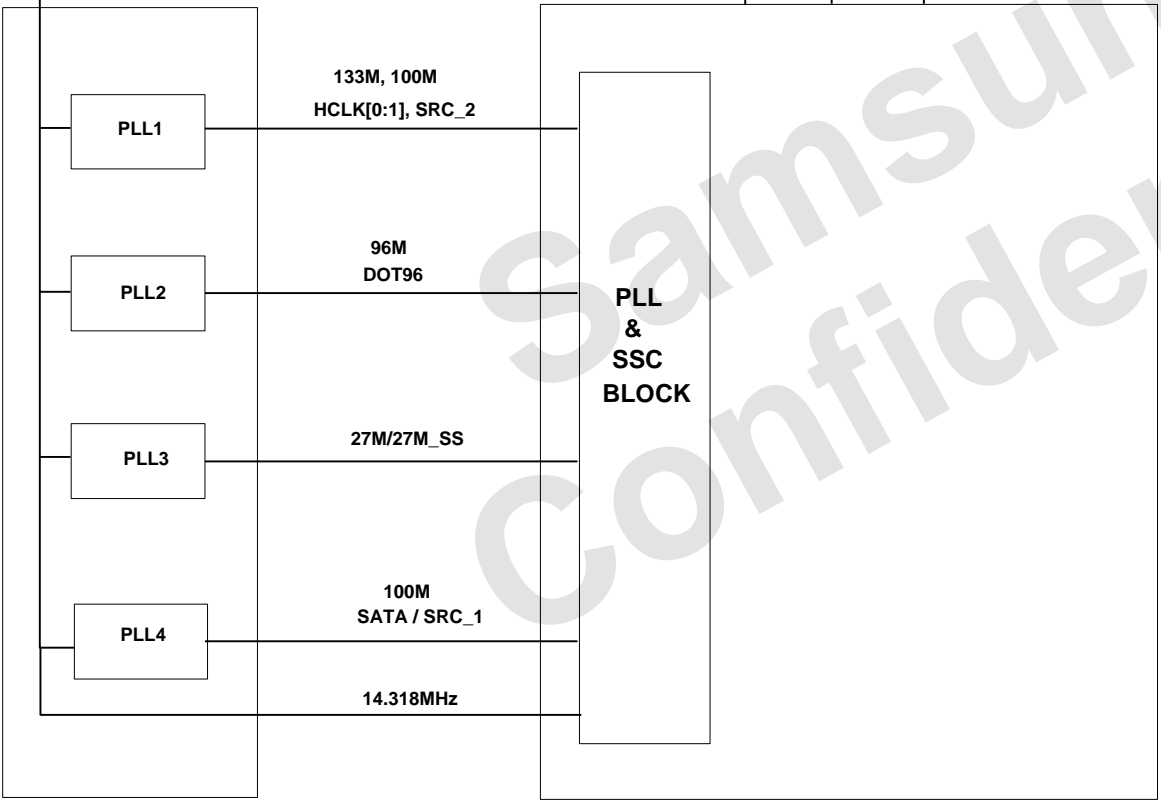
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CLOCK DISTRIBUTION Rev. 0.1

Arandale

BCLK 133M
 DMI 100M
 DP 120M

XTAL



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CHECK	Rujin Zheng	DEV. STEP	PV	UNDEF INED		
APPROVAL	BC LEE	REV	1.0	UNDEF INED		
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	7 OF 62	

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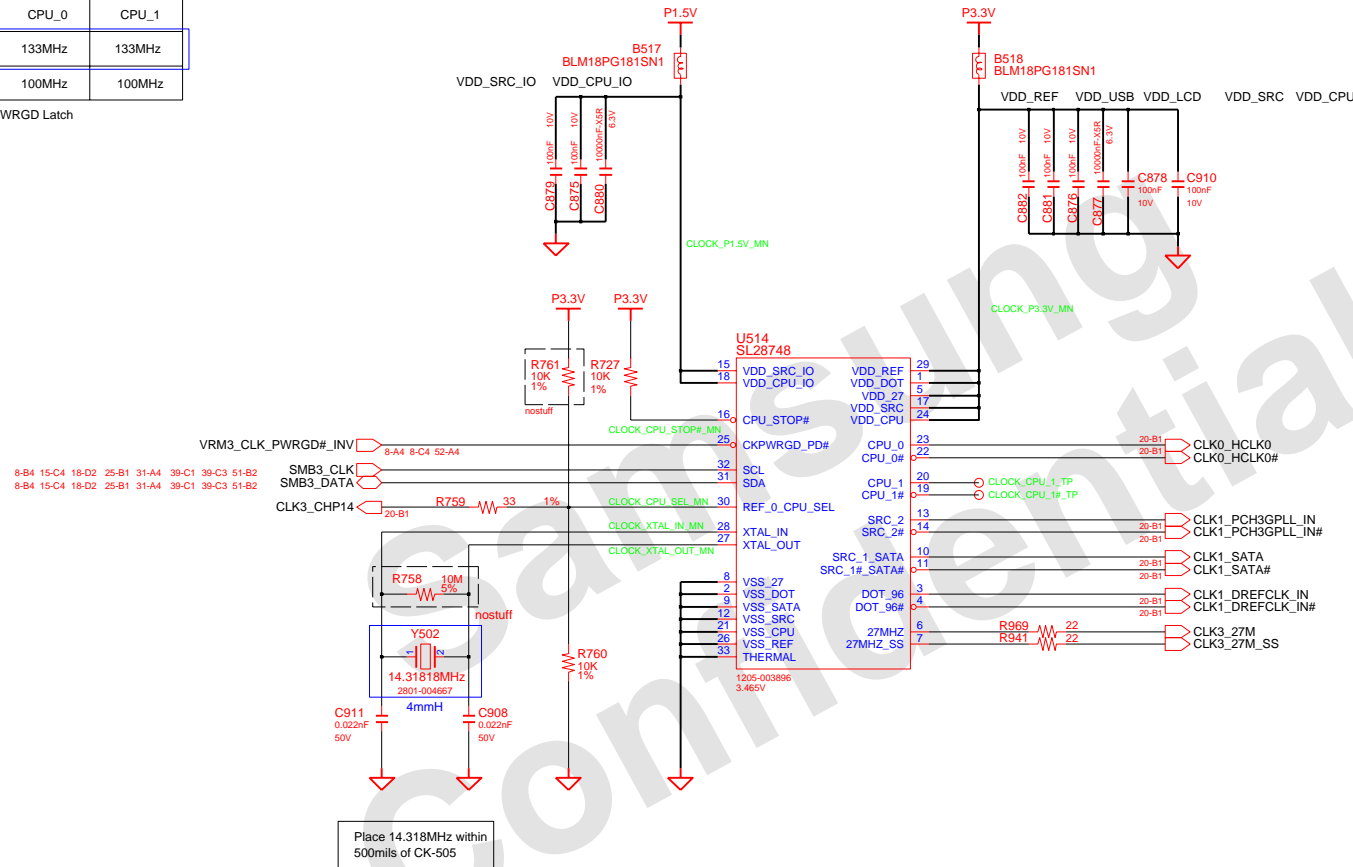
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CK505M SHRINK VERSION

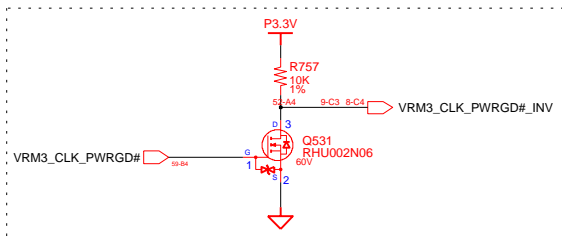
CPU_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

*CPU_SEL During CK_PWRGD Latch



Place 14.318MHz within 500mils of CK-505



DRAW	Xiaohong Zheng	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	Main_Clock_Circuit		
APPROVAL	BC LEE	REV	1.0	CK_Clock_505M		PART NO. BA41-01190/1/2A
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	8	OF 62

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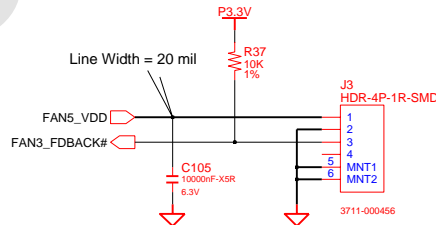
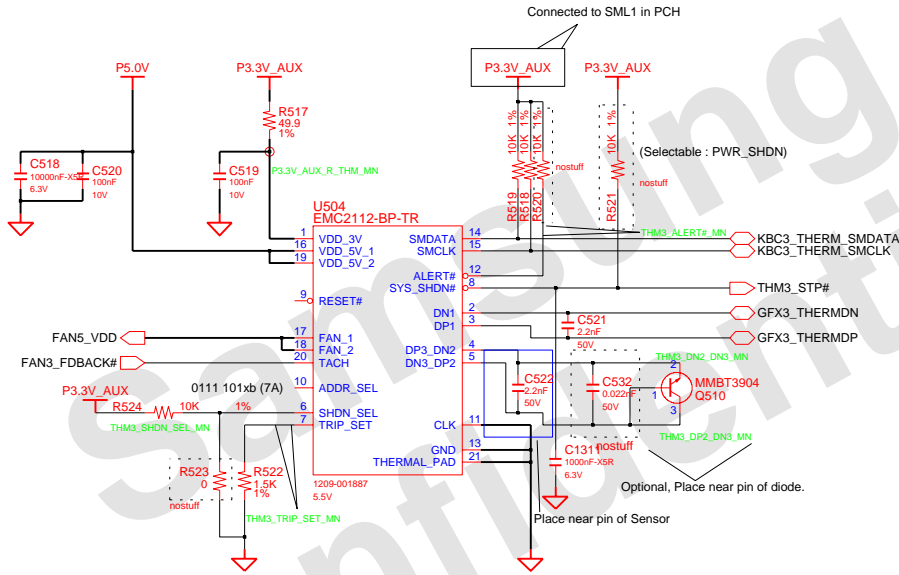
THERMAL SENSOR & FAN CONTROL

ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDNSEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

TRIP_SET Resistor Setting (60 ~ 122 C)	
60	0.0
95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
✓ 103	2550
104	2740
105	2940
122	49900

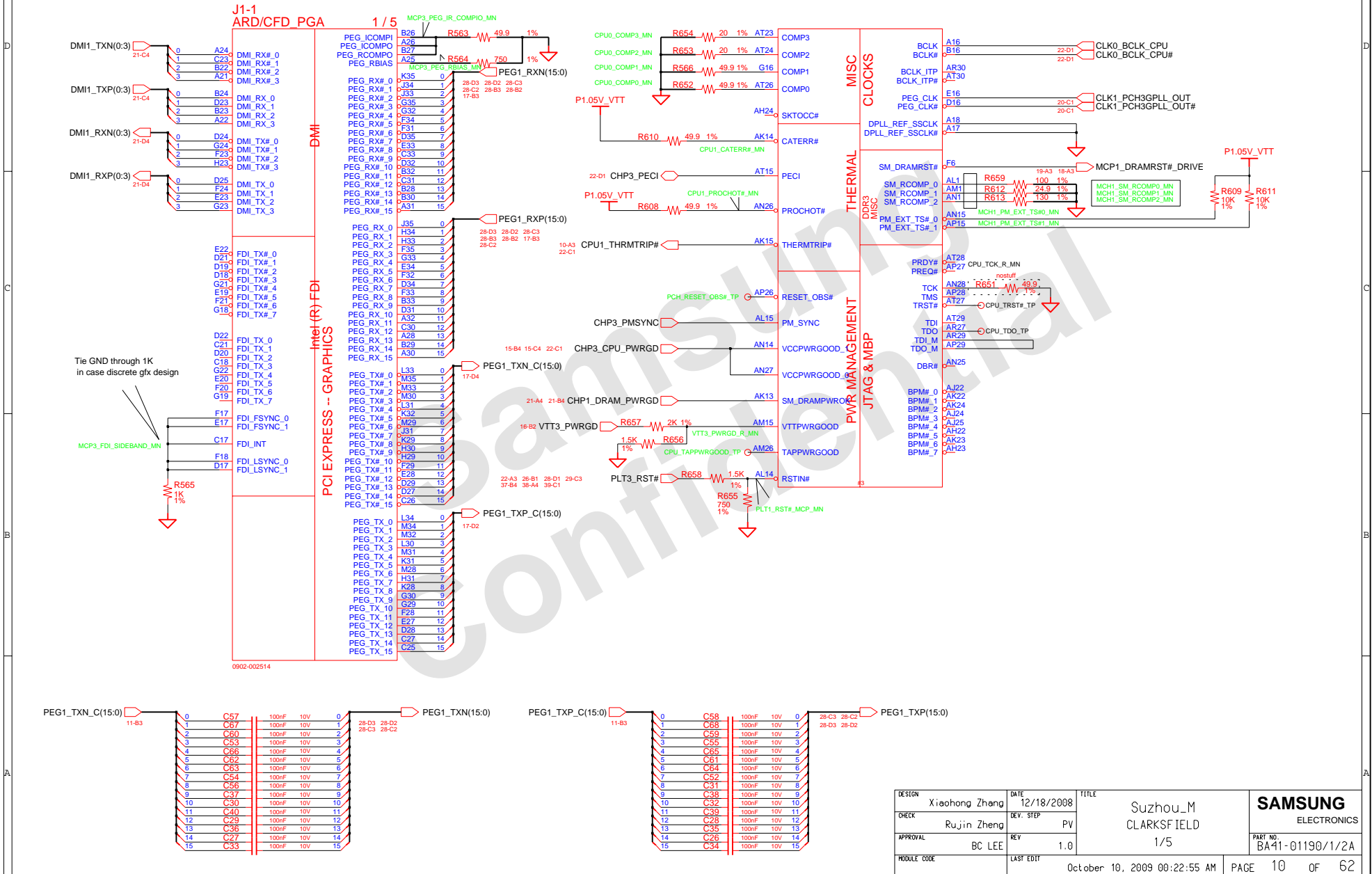
$V_Trip = (T_Trip - T_Min) / 80$
 V_TRIP : TRIP_SET Voltage
 T_Min : Minimum Temperature



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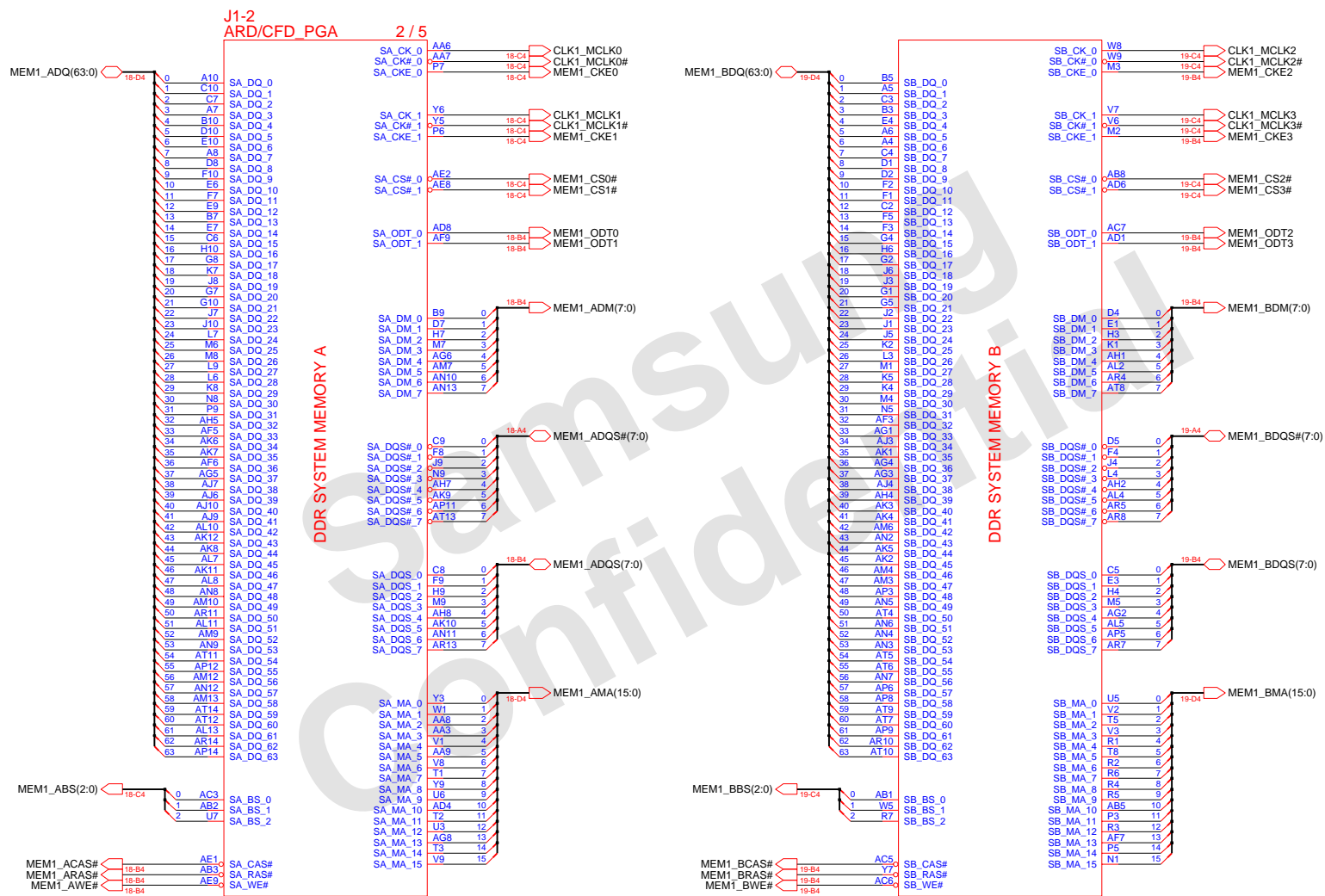
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ARRANDALE PROCESSOR (DMI,PEG, FDI)



DESIGN	Xiaohong Zheng	DATE	12/18/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	CLARKSFIELD		
APPROVAL	BC LEE	REV	1.0	1/5		PART NO. BA41-01190/1/2A
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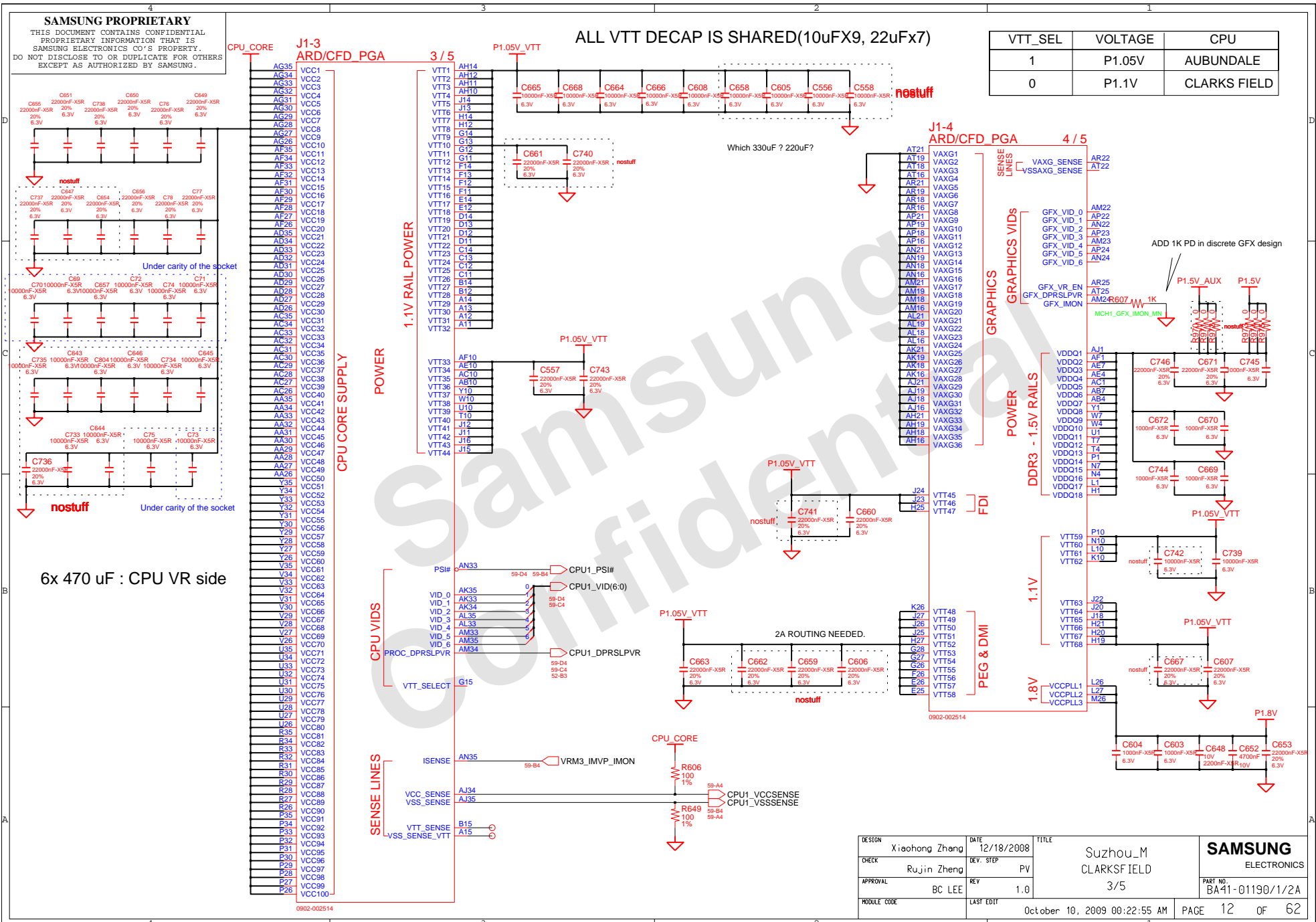
0902-002514

DESIGN	Xiaohong Zheng	DATE	12/18/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	CLARKSFIELD	2/5	
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	11	OF 62

ALL VTT DECAP IS SHARED(10uF-X9, 22uF-X7)

VTT_SEL	VOLTAGE	CPU
1	P1.05V	AUBUNDALE
0	P1.1V	CLARKS FIELD

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DESIGN	Xiaohong Zheng	DATE	12/18/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		CLARKS FIELD	
APPROVAL	BC LEE	REV	1.0		3/5	PART NO. BA41-01190/1/2A
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**J1-5
 ARD/CFD PGA5 / 5**

VSS4720	VSS1	VSS81	AE34
AT17	VSS2	VSS82	AE35
AR31	VSS3	VSS83	AE36
AR28	VSS4	VSS84	AE37
AR26	VSS5	VSS85	AE38
AR24	VSS6	VSS86	AE39
AR23	VSS7	VSS87	AE28
AR20	VSS8	VSS88	AE27
AR17	VSS9	VSS89	AE26
AR16	VSS10	VSS90	AE5
AR12	VSS11	VSS91	AC8
AR9	VSS12	VSS92	AC4
AR6	VSS13	VSS93	AC2
AR3	VSS14	VSS94	AC2
AP20	VSS15	VSS95	AB35
AP17	VSS16	VSS96	AB34
AP13	VSS17	VSS97	AB33
AP10	VSS18	VSS98	AB32
AP7	VSS19	VSS99	AB31
AP4	VSS20	VSS100	AB30
AP2	VSS21	VSS101	AB29
AN34	VSS22	VSS102	AB28
AN31	VSS23	VSS103	AB27
AN23	VSS24	VSS104	AB26
AN20	VSS25	VSS105	AB25
AN17	VSS26	VSS106	AA10
AM29	VSS27	VSS107	Y8
AM27	VSS28	VSS108	Y2
AM25	VSS29	VSS109	W35
AM20	VSS30	VSS110	W34
AM17	VSS31	VSS111	W33
AM14	VSS32	VSS112	W32
AM11	VSS33	VSS113	W31
AM8	VSS34	VSS114	W30
AM5	VSS35	VSS115	W29
AM2	VSS36	VSS116	W28
AL34	VSS37	VSS117	W27
AL31	VSS38	VSS118	W26
AL23	VSS39	VSS119	W6
AL20	VSS40	VSS120	V10
AL17	VSS41	VSS121	U8
AL12	VSS42	VSS122	U4
AL9	VSS43	VSS123	U2
AL6	VSS44	VSS124	T35
AL3	VSS45	VSS125	T35
AK29	VSS46	VSS126	T34
AK27	VSS47	VSS127	T33
AK25	VSS48	VSS128	T32
AK20	VSS49	VSS129	T31
AK17	VSS50	VSS130	T30
AK31	VSS51	VSS131	T29
AK23	VSS52	VSS132	T28
AK20	VSS53	VSS133	T26
AJ23	VSS54	VSS134	T25
AJ17	VSS55	VSS135	T6
AJ14	VSS56	VSS136	R10
AJ11	VSS57	VSS137	P9
AJ8	VSS58	VSS138	P4
AJ5	VSS59	VSS139	P2
AJ2	VSS60	VSS140	N35
AH35	VSS61	VSS141	N34
AH34	VSS62	VSS142	N33
AH33	VSS63	VSS143	N32
AH31	VSS64	VSS144	N31
AH30	VSS65	VSS145	N30
AH29	VSS66	VSS146	N29
AH28	VSS67	VSS147	N28
AH27	VSS68	VSS148	N27
AH26	VSS69	VSS149	N26
AH20	VSS70	VSS150	M10
AH17	VSS71	VSS151	L35
AH13	VSS72	VSS152	L32
AH9	VSS73	VSS153	L29
AH6	VSS74	VSS154	L5
AH3	VSS75	VSS155	L5
AG10	VSS76	VSS156	L2
AF8	VSS77	VSS157	K34
AF4	VSS78	VSS158	K33
AF2	VSS79	VSS159	K30
AE35	VSS80	VSS160	K30

K27	VSS161
K9	VSS162
K6	VSS163
K3	VSS164
J32	VSS165
J21	VSS166
J19	VSS167
H35	VSS168
H32	VSS169
H28	VSS170
H26	VSS171
H24	VSS172
H22	VSS173
H19	VSS174
H15	VSS175
H13	VSS176
H11	VSS177
H8	VSS178
H5	VSS179
H2	VSS180
G34	VSS181
G31	VSS182
G20	VSS183
G9	VSS184
G6	VSS185
G3	VSS186
F30	VSS187
F27	VSS188
F25	VSS189
F22	VSS190
F19	VSS191
F16	VSS192
F15	VSS193
E32	VSS194
E29	VSS195
E24	VSS196
E21	VSS197
E18	VSS198
E13	VSS199
E11	VSS200
E8	VSS201
E5	VSS202
E2	VSS203
D33	VSS204
D30	VSS205
D26	VSS206
D9	VSS207
D6	VSS208
D3	VSS209
C34	VSS210
C32	VSS211
C29	VSS212
C28	VSS213
C22	VSS214
C24	VSS215
C20	VSS216
C19	VSS217
C16	VSS218
B31	VSS219
B25	VSS220
B21	VSS221
B18	VSS222
B17	VSS223
B13	VSS224
B11	VSS225
B8	VSS226
B6	VSS227
B4	VSS228
B29	VSS229
A27	VSS230
A23	VSS231
A9	VSS232
A9	VSS233

R650
 3.01K 1%
 CPU_CFG_7,R,MN

AT35 CPU_VSS_NCTF1
 AT1 CPU_VSS_NCTF2
 AR34 CPU_VSS_NCTF3
 B34 CPU_VSS_NCTF4
 B2 CPU_VSS_NCTF5
 B1 CPU_VSS_NCTF6
 A35 CPU_VSS_NCTF7

AP25	RSVD1	RSVD32	AJ13
AL25	RSVD2	RSVD33	AJ12
AL24	RSVD3		
AL22	RSVD4	RSVD34	AH25
AJ33	RSVD5	RSVD35	AK26
AG9	RSVD6	RSVD36	AL26
M27	RSVD7	RSVD_NCTF_37	AR2
L26	RSVD8		
J17	SA_DIMM_VREFDQ	RSVD38	AJ26
H17	SB_DIMM_VREFDQ	RSVD39	AJ27
G25	RSVD11		
C17	RSVD12	RSVD_NCTF_40	AP1
E31	RSVD13	RSVD_NCTF_41	AT2
E30	RSVD14	RSVD_NCTF_42	AT3
		RSVD_NCTF_43	AR1
AM30	CFG_0	RSVD45	AL28
AM28	CFG_1	RSVD46	AL29
AP31	CFG_2	RSVD47	AP30
AL32	CFG_3	RSVD48	AP32
AL30	CFG_4	RSVD49	AL27
AM31	CFG_5	RSVD50	AT31
AN29	CFG_6	RSVD51	AP33
AM32	CFG_7	RSVD52	AR33
AK32	CFG_8	RSVD53	AR33
AK28	CFG_9	RSVD_NCTF_54	AT34
AJ28	CFG_10	RSVD_NCTF_55	AT34
AN30	CFG_11	RSVD_NCTF_56	AP35
AK32	CFG_12	RSVD_NCTF_57	AR35
AJ32	CFG_13	RSVD58	AR32
AJ29	CFG_14	RSVD_TP_59	E15
AK30	CFG_15	RSVD_TP_60	F15
AK30	CFG_16	KEY	A2
H16	CFG_17	RSVD_TP_86	D15
			C15
			AJ15
			AH15
B19	RSVD15		AA5
A18	RSVD16		AA4
			R8
A20	RSVD17	RSVD_TP_86	AD3
B20	RSVD18	RSVD_TP_87	AD2
			AA2
U9	RSVD19	RSVD_TP_69	AA1
T9	RSVD20	RSVD_TP_70	R9
		RSVD_TP_71	AC7
AC9	RSVD21	RSVD_TP_72	AE3
AB9	RSVD22	RSVD_TP_73	
		RSVD_TP_74	
		RSVD_TP_75	
C1	RSVD_NCTF_23		V4
A3	RSVD_NCTF_24		V5
			N2
		RSVD_TP_76	AD5
		RSVD_TP_77	AD7
		RSVD_TP_78	W2
		RSVD_TP_79	W2
J29	RSVD26	RSVD_TP_80	N3
J28	RSVD27	RSVD_TP_81	AE5
		RSVD_TP_82	AD9
A34	RSVD_NCTF_28	RSVD_TP_83	
A33	RSVD_NCTF_29	RSVD_TP_84	
		RSVD_TP_85	
C35	RSVD_NCTF_30		
B35	RSVD_NCTF_31		
	(VSS) RSVD86		AP34

(VSS) RSVD86

CFG Straps for Processor

PCI Express Configuration Select		ALL nostuff
CFG0	1 : Single PEG 0 : Bifunction enabled	
PCI Express Static Lane Reversal		
CFG3	1 : Normal operation 0 : Lane Reversed	
Display Port Presence		
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP	
PCIe 2.0 SUPPORT		
CFG7	1 : Normal operation 0 : PCIe2.0 Jitter support	

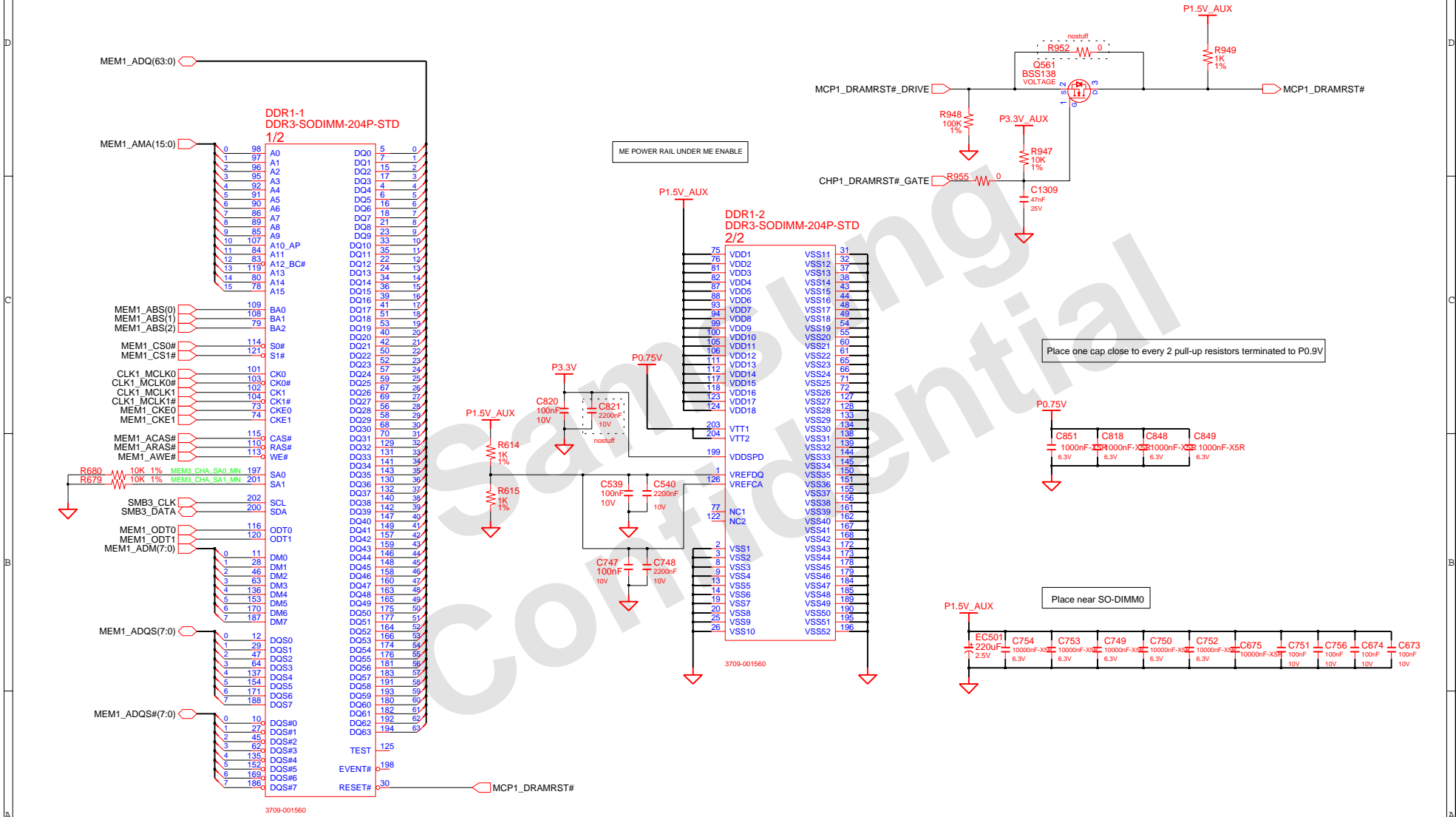
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CHECK	Rujin Zheng	DEV. STEP	PV		CLARKSFIELD	
APPROVAL	BC LEE	REV	1.0		4/5	PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	13	OF 62

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DDR SO-DIMM #0

Height : 5.2mm (Reverse)



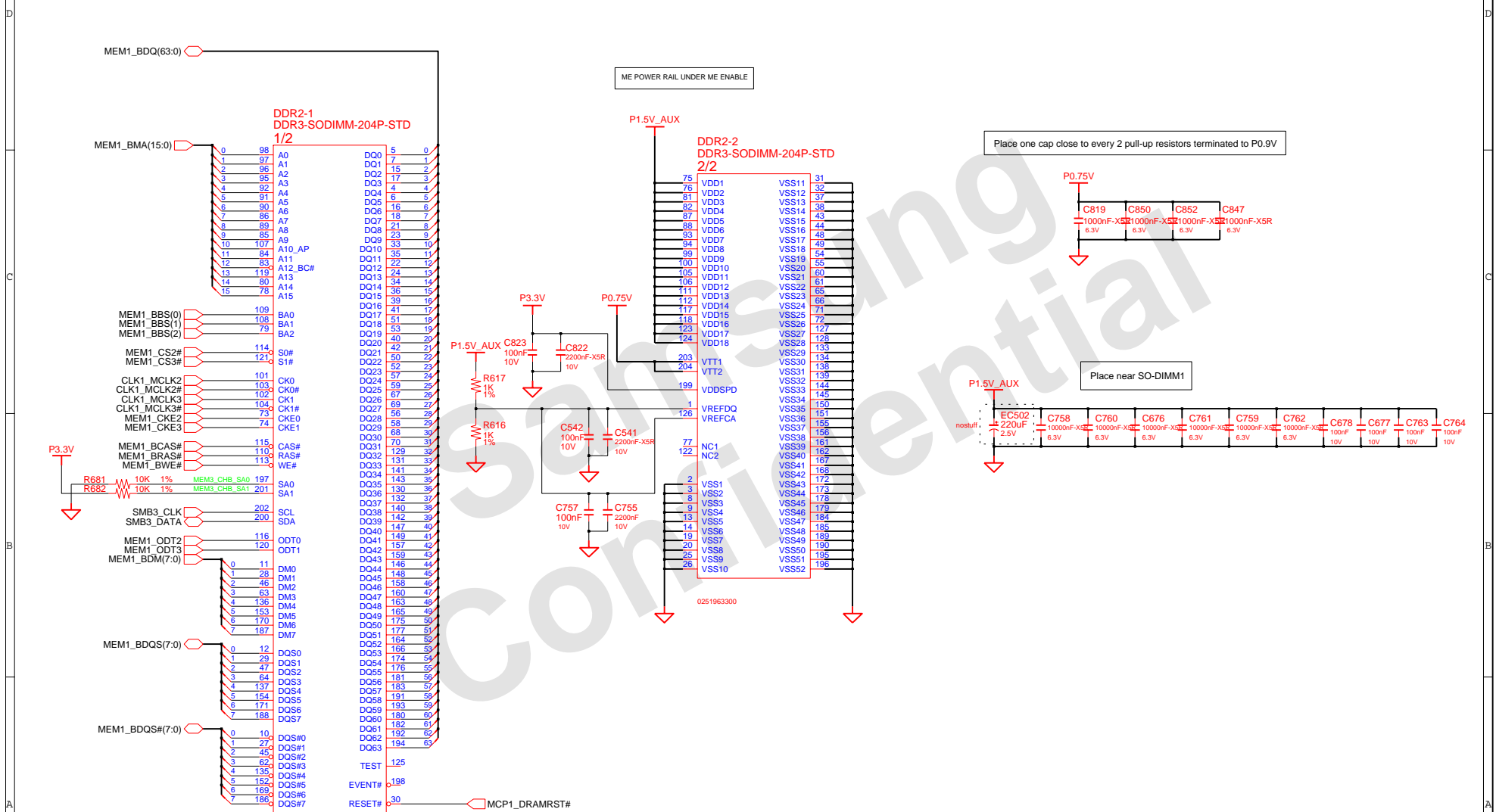
DRAW	Xiaohong Zheng	DATE	11/8/2006	TITLE	Suzhou_M SODIMM_REV DDR3 CH A	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	14 OF 62	

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DDR SO-DIMM #1

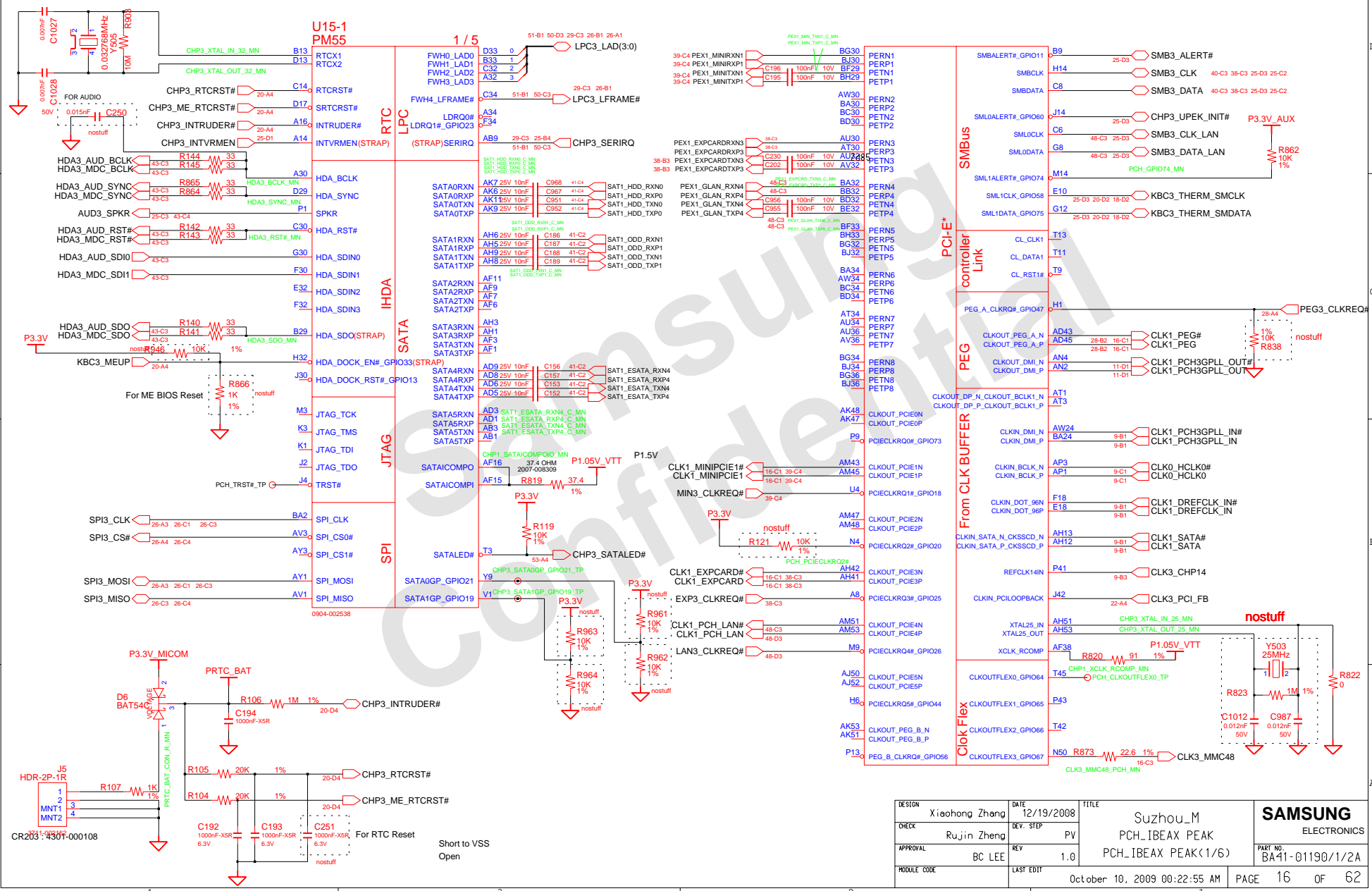
Height : 9.2mm (Reverse)



0251963300

DRAW	Xiaohong Zheng	DATE	11/8/2006	TITLE	Suzhou_M SODIMM_REV DDR3 CH B	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		PART NO. BA41-01190/1/2A	
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	15	OF 62

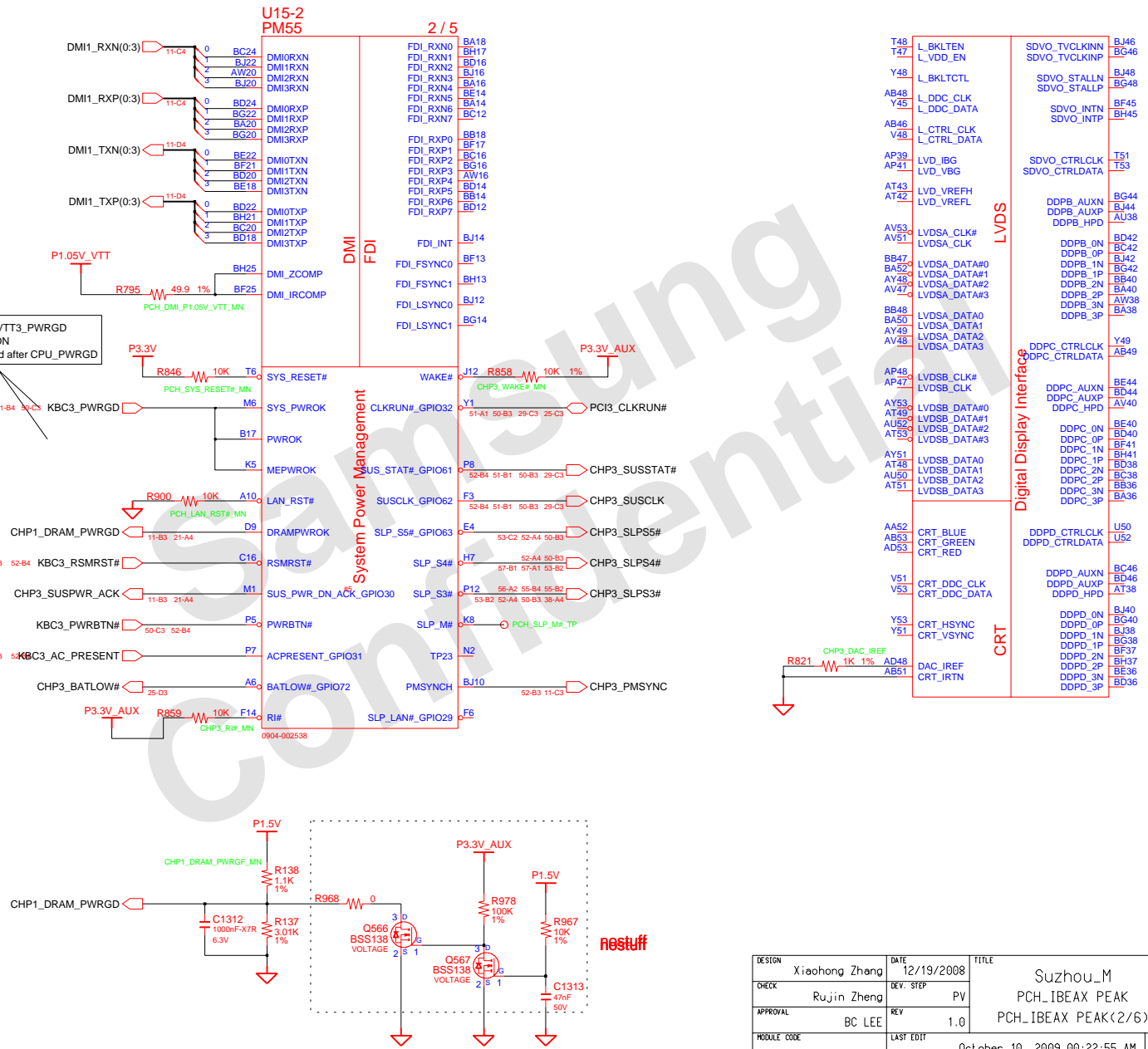
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DESIGN	Xiaohong Zheng	DATE	12/19/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV		PCH_IBEAX PEAK	
APPROVAL	BC LEE	REV	1.0		PCH_IBEAX PEAK(1/6)	
MODULE CODE		LAST EDIT				
				October 10, 2009 00:22:55 AM	PAGE 16 OF 62	

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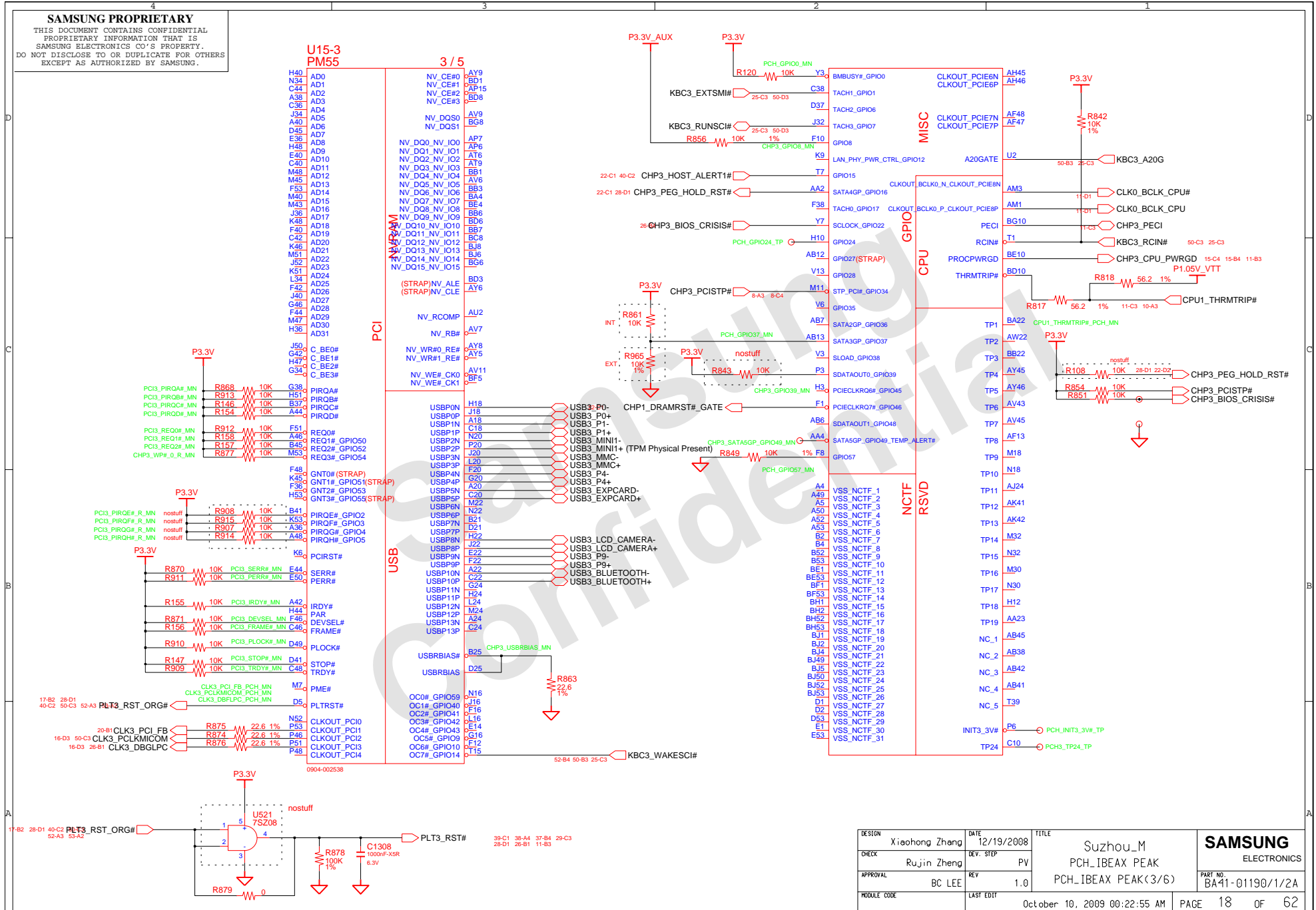
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DESIGN	Xiaohong Zheng	DATE	12/19/2008	TITLE	Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(2/6)	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV	REV	1.0	
APPROVAL	BC LEE	REV	1.0	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE 17 OF 62
MODULE CODE						

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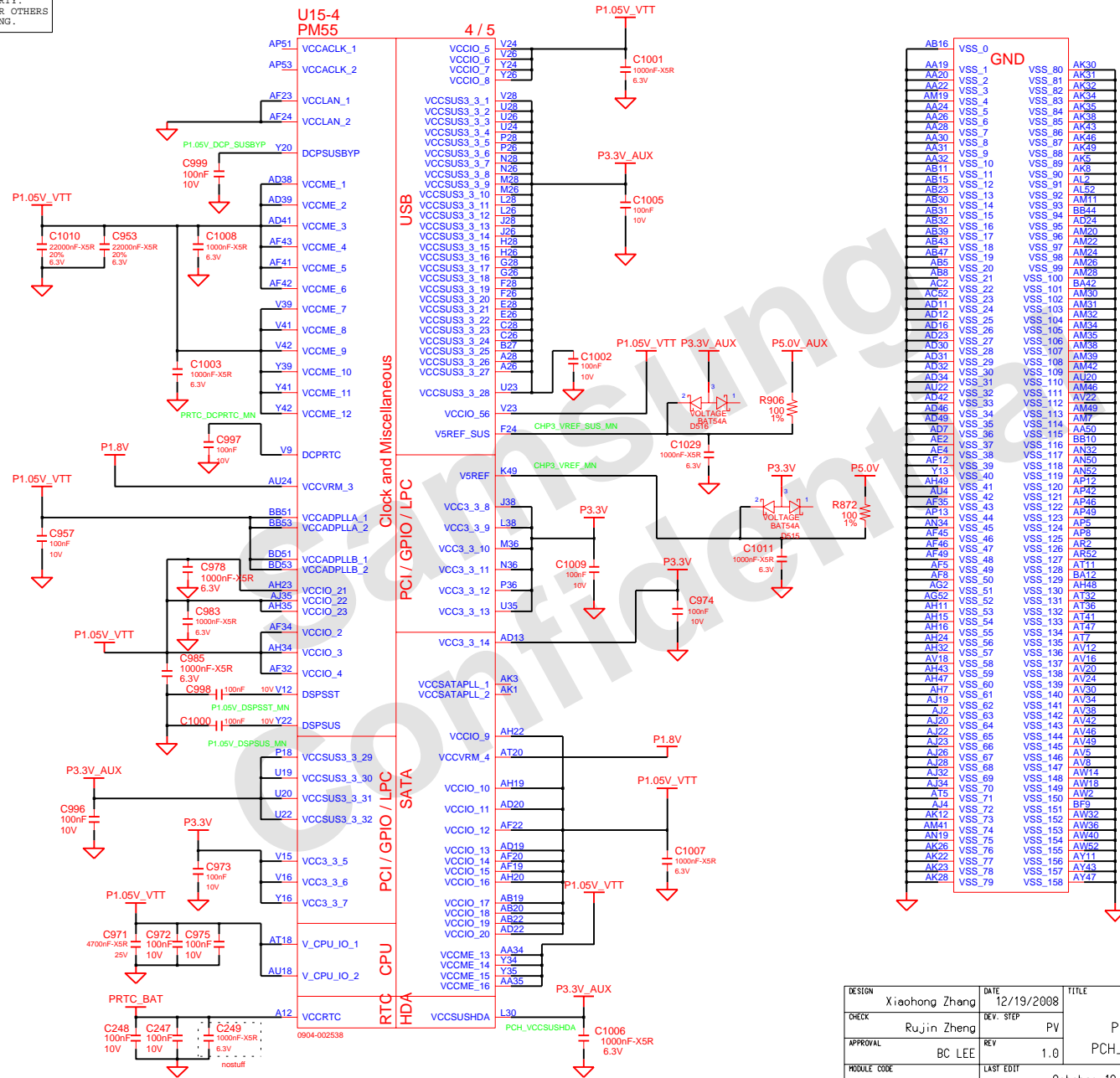


DESIGN	Xiaohong Zheng	DATE	12/19/2008	TITLE	Suzhou_M PCH_IBEAX PEAK PCH_IBEAX PEAK(3/6)	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PART NO.	BA41-01190/1/2A	
APPROVAL	BC LEE	REV	1.0	October 10, 2009 00:22:55 AM	PAGE	18 OF 62
MODULE CODE		LAST EDIT				

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P1.1V,P1.1V_M is P1.05V & P1.05V_M ACTUALLY



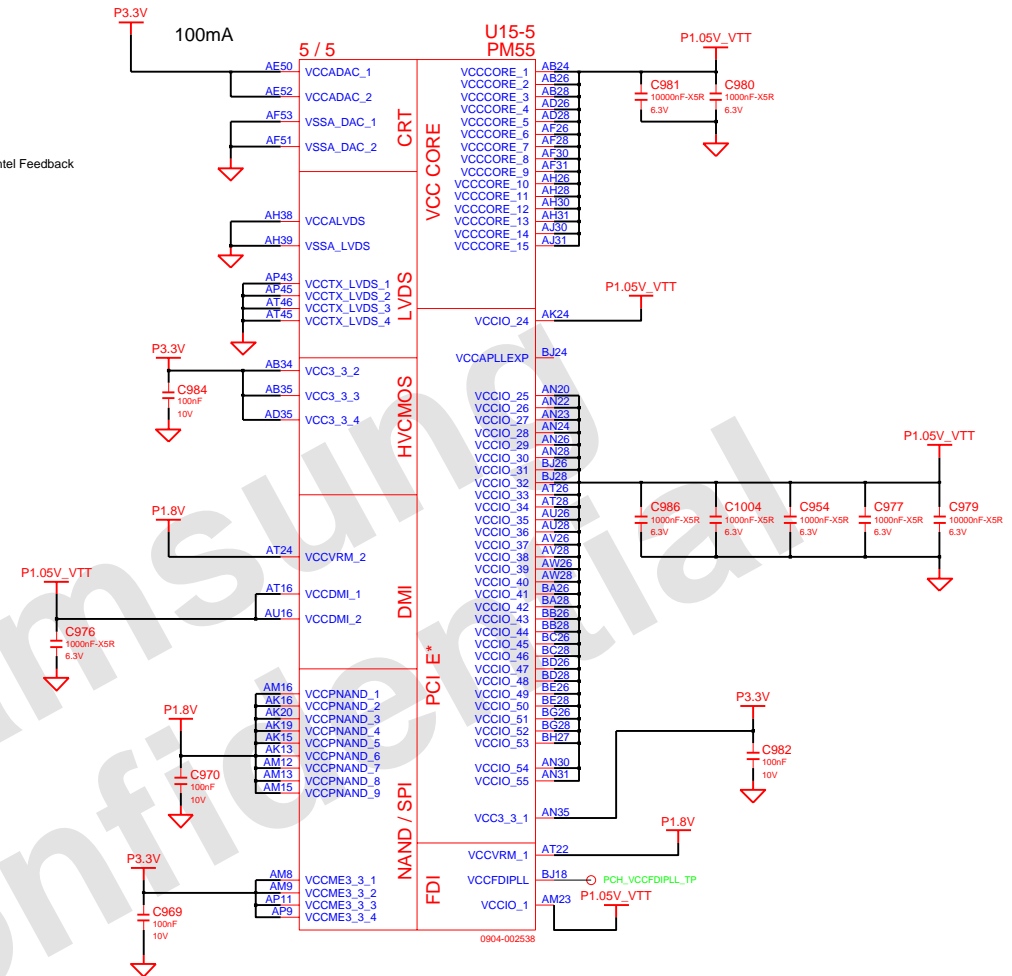
DESIGN	Xiaohong Zheng	DATE	12/19/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PCH_IBEAX PEAK		
APPROVAL	BC LEE	REV	1.0	PCH_IBEAX PEAK(4/6)		PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	19	OF 62

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H49	VSS_259	VSS_159	AY7
H5	VSS_260	VSS_160	B11
J24	VSS_261	VSS_161	B15
K11	VSS_262	VSS_162	B19
K43	VSS_263	VSS_163	B23
K47	VSS_264	VSS_164	B31
K7	VSS_265	VSS_165	B35
L14	VSS_266	VSS_166	B39
L18	VSS_267	VSS_167	B43
L2	VSS_268	VSS_168	B47
L22	VSS_269	VSS_169	B7
L32	VSS_270	VSS_170	BG12
L36	VSS_271	VSS_171	BB12
L40	VSS_272	VSS_172	BB16
L52	VSS_273	VSS_173	BB20
M12	VSS_274	VSS_174	BB24
M16	VSS_275	VSS_175	BB30
M20	VSS_276	VSS_176	BB34
M34	VSS_277	VSS_177	BB38
M38	VSS_278	VSS_178	BB42
M42	VSS_279	VSS_179	BB46
M46	VSS_280	VSS_180	BB50
M49	VSS_281	VSS_181	BC10
M5	VSS_282	VSS_182	BC14
M8	VSS_283	VSS_183	BC2
N24	VSS_284	VSS_184	BC22
N38	VSS_285	VSS_185	BC32
P11	VSS_286	VSS_186	BC40
P22	VSS_287	VSS_187	BC44
P30	VSS_288	VSS_188	BC52
P32	VSS_289	VSS_189	BH9
P34	VSS_290	VSS_190	BH9
P42	VSS_291	VSS_191	BD48
P45	VSS_292	VSS_192	BD48
P47	VSS_293	VSS_193	BD5
R2	VSS_294	VSS_194	BE12
R52	VSS_295	VSS_195	BE16
T12	VSS_296	VSS_196	BE20
T41	VSS_297	VSS_197	BE24
T46	VSS_298	VSS_198	BE38
T49	VSS_299	VSS_199	BE42
T8	VSS_300	VSS_200	BE34
T8	VSS_301	VSS_201	BE38
U30	VSS_302	VSS_202	BE46
U31	VSS_303	VSS_203	BE48
U32	VSS_304	VSS_204	BE50
U34	VSS_305	VSS_205	BE5
P38	VSS_306	VSS_206	BE8
V11	VSS_307	VSS_207	BF3
V16	VSS_308	VSS_208	BF49
V19	VSS_309	VSS_209	BF51
V20	VSS_310	VSS_210	BG18
V22	VSS_311	VSS_211	BG24
V30	VSS_312	VSS_212	BG4
V31	VSS_313	VSS_213	BG4
V32	VSS_314	VSS_214	BG50
V34	VSS_315	VSS_215	BH11
V35	VSS_316	VSS_216	BH15
V38	VSS_317	VSS_217	BH19
V43	VSS_318	VSS_218	BH23
V44	VSS_319	VSS_219	BH31
V45	VSS_320	VSS_220	BH35
V46	VSS_321	VSS_221	BH39
V47	VSS_322	VSS_222	BH43
V49	VSS_323	VSS_223	BH47
V5	VSS_324	VSS_224	BH7
V7	VSS_325	VSS_225	C12
V8	VSS_326	VSS_226	C50
W2	VSS_327	VSS_227	D51
W52	VSS_328	VSS_228	E12
Y11	VSS_329	VSS_229	E16
Y12	VSS_330	VSS_230	E20
Y15	VSS_331	VSS_231	E24
Y19	VSS_332	VSS_232	E30
Y23	VSS_333	VSS_233	E34
Y28	VSS_334	VSS_234	E38
Y30	VSS_335	VSS_235	E42
Y31	VSS_336	VSS_236	E46
Y32	VSS_337	VSS_237	E48
Y38	VSS_338	VSS_238	E8
Y43	VSS_339	VSS_239	F9
Y46	VSS_340	VSS_240	F49
P49	VSS_341	VSS_241	F5
V5	VSS_342	VSS_242	G10
V6	VSS_343	VSS_243	G14
Y8	VSS_344	VSS_244	G18
P24	VSS_345	VSS_245	G2
T43	VSS_346	VSS_246	G22
AD51	VSS_347	VSS_247	G32
AT8	VSS_348	VSS_248	G36
AD47	VSS_349	VSS_249	G40
Y47	VSS_350	VSS_250	G44
AT12	VSS_351	VSS_251	G52
AM6	VSS_352	VSS_252	AF38
AT13	VSS_353	VSS_253	H16
AM5	VSS_354	VSS_254	H20
AK45	VSS_355	VSS_255	H30
AK39	VSS_356	VSS_256	H34
AV14	VSS_357	VSS_257	H38
	VSS_358	VSS_258	H42

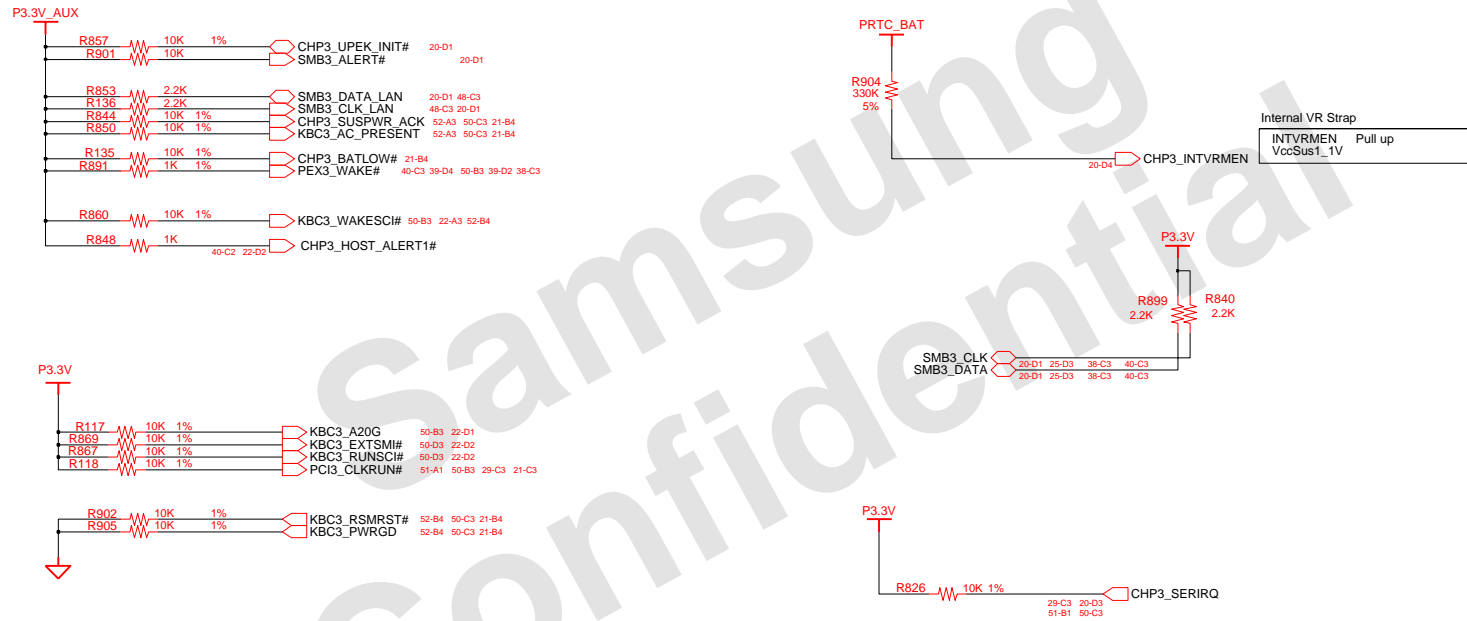
By desig guide rev0.8 & Intel Feedback



DESIGN	Xiaohong Zheng	DATE	12/19/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PCH_IBEAX PEAK		
APPROVAL	BC LEE	REV	1.0	PCH_IBEAX PEAK(5/6)		PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	20	OF 62

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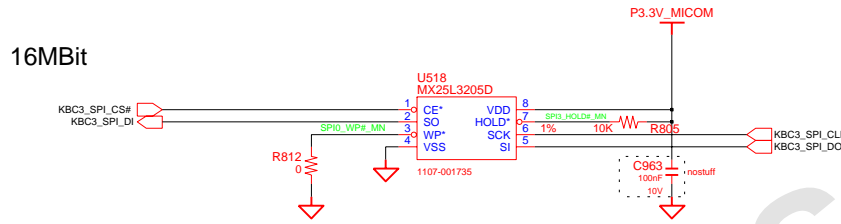
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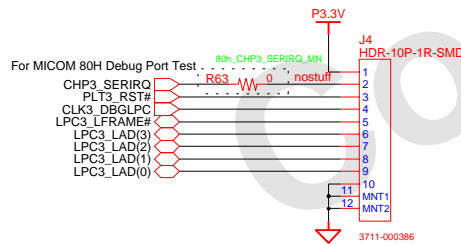
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SPI_BIOS_ROM



80H DECODER CONNECTOR

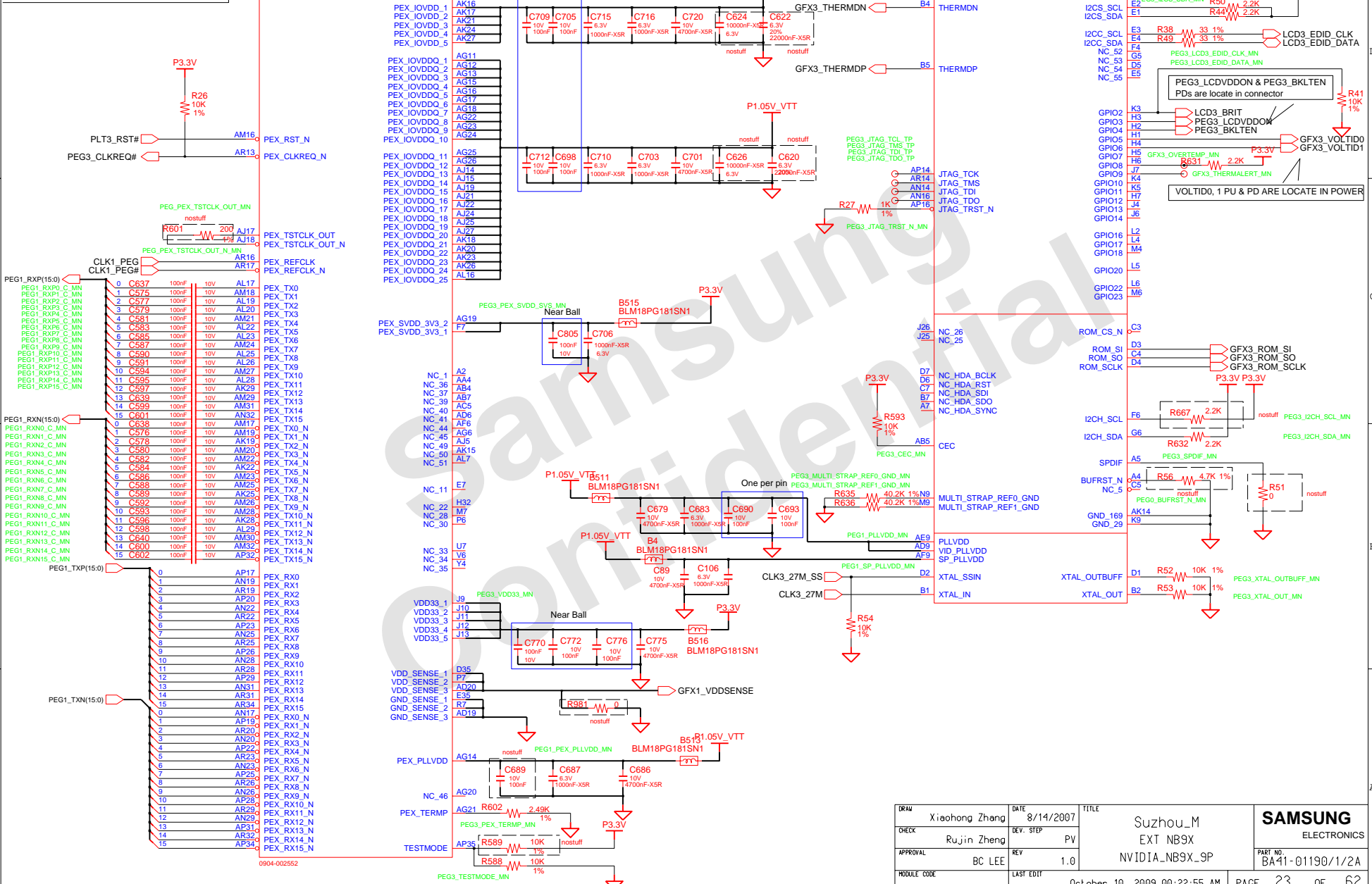


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. CPU SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	8E	SHADOW OPTION ROMS
18	8254 TIMER INIT	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	D9	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5A	DISPLAY FRESH SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 812K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV	SPI_BIOS_ROM		
APPROVAL	BC LEE	REV	1.0	SPI_BIOS_ROM		
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM		PAGE 22 OF 62	

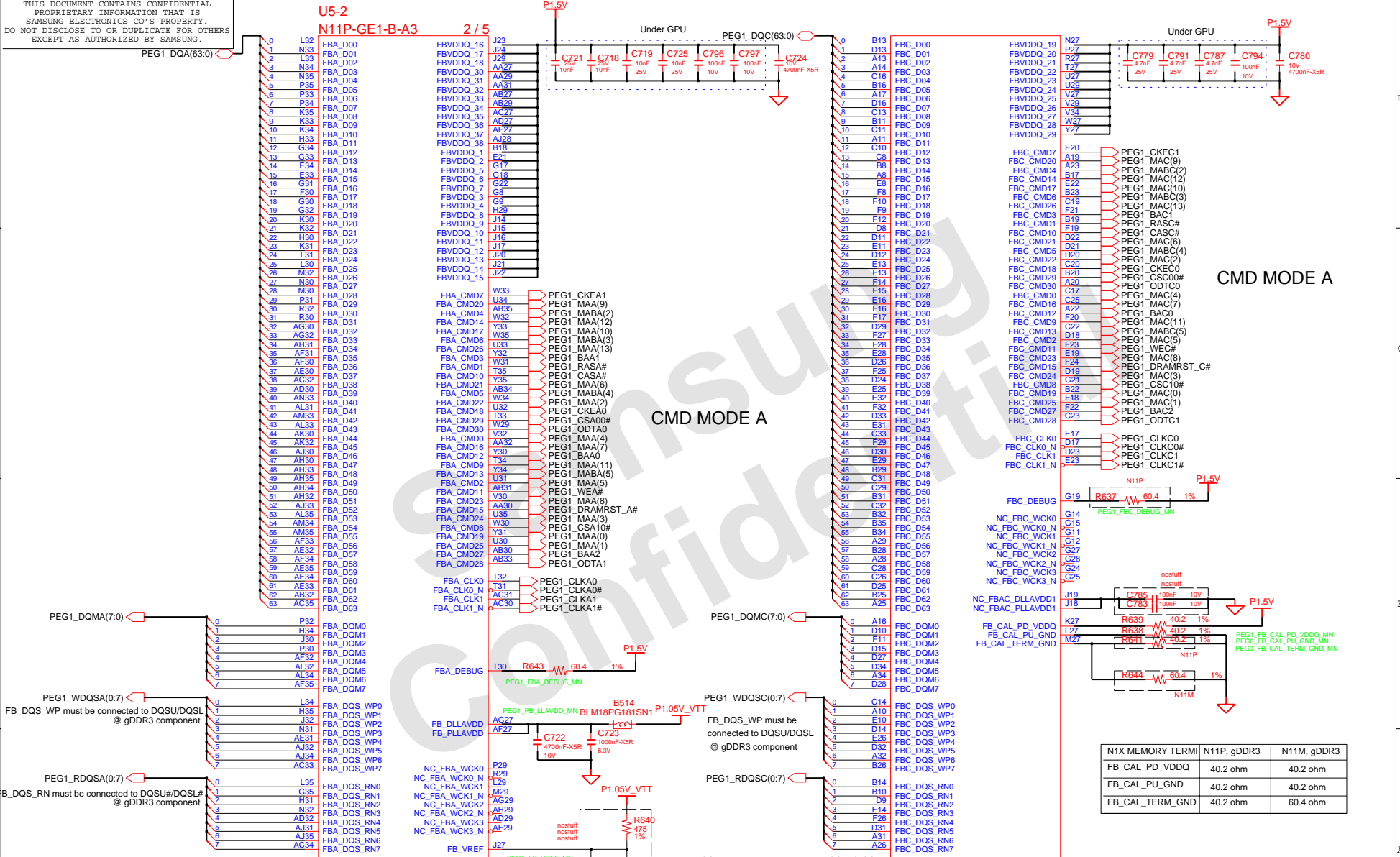
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U5-1
 N11P-GE1-B-A3 1 / 5



DRAW	Xiaohong Zheng	DATE	8/14/2007	TITLE	Suzhou_M EXT NB9X	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	REV	NVIDIA_NB9X_9P	
APPROVAL	BC LEE	REV	1.0	LAST EDIT	October 10, 2009 00:22:55 AM	PART NO. BA41-01190/1/2A
MODULE CODE						PAGE 23 OF 62

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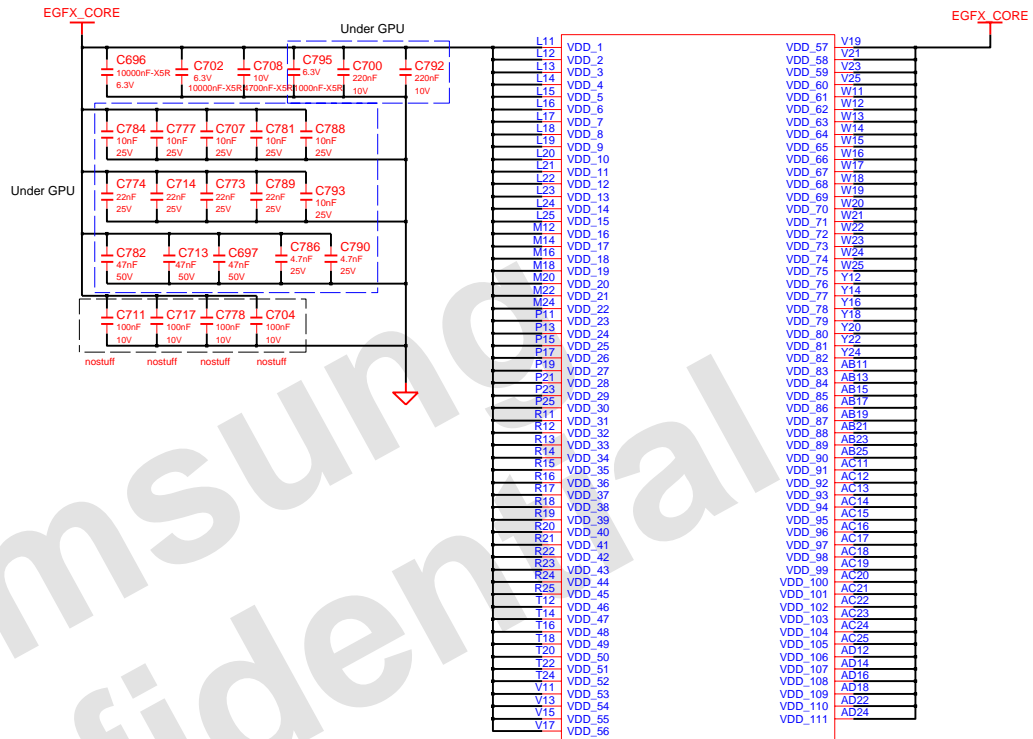
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FB_CAL_PD_VDDQ	40.2 ohm	40.2 ohm
FB_CAL_PU_GND	40.2 ohm	40.2 ohm
FB_CAL_TERM_GND	40.2 ohm	60.4 ohm

DRAW	Xiaohong Zheng	DATE	8/14/2007	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV	EXT	NB9X	
APPROVAL	BC LEE	REV	1.0	NVIDIA	NB9X_9P	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	24 OF 62	

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U5-3
 N11P-GE1-B-A3 3/5

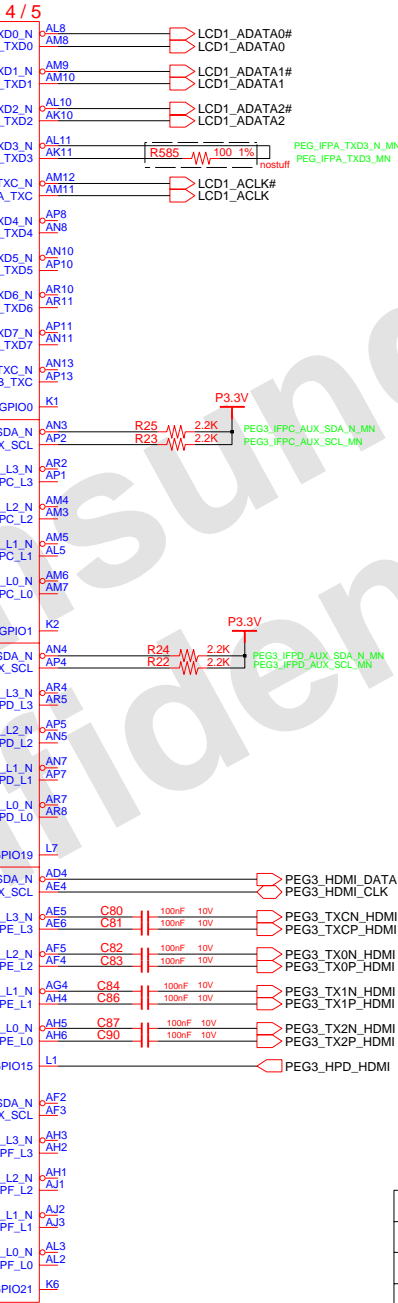
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B6	GND_2	GND_98	V18
B9	GND_3	GND_99	V20
B12	GND_4	GND_100	V22
B15	GND_5	GND_101	V24
B21	GND_6	GND_102	V31
B24	GND_7	GND_103	Y11
B27	GND_8	GND_104	Y13
B30	GND_9	GND_105	Y15
B33	GND_10	GND_106	Y17
G2	GND_11	GND_107	Y19
C4	GND_12	GND_108	Y21
E6	GND_13	GND_109	Y23
E9	GND_14	GND_110	Y25
E12	GND_15	GND_111	AA2
E15	GND_16	GND_112	AA5
E18	GND_17	GND_113	AA11
E24	GND_18	GND_114	AA12
E27	GND_19	GND_115	AA13
E30	GND_20	GND_116	AA14
F2	GND_21	GND_117	AA15
F5	GND_22	GND_118	AA16
F9	GND_23	GND_119	AA17
F34	GND_24	GND_120	AA18
J2	GND_25	GND_121	AA19
J5	GND_26	GND_122	AA20
J31	GND_27	GND_123	AA21
J34	GND_28	GND_124	AA22
L9	GND_29	GND_125	AA23
M2	GND_30	GND_126	AA24
M5	GND_31	GND_127	AA25
M11	GND_32	GND_128	AA34
M13	GND_33	GND_129	AB12
M15	GND_35	GND_130	AB14
M17	GND_36	GND_131	AB16
M19	GND_37	GND_132	AB18
M21	GND_38	GND_133	AB20
M23	GND_39	GND_134	AB22
M25	GND_40	GND_135	AB24
M31	GND_41	GND_136	AC5
M34	GND_42	GND_137	AD2
N11	GND_43	GND_138	AD5
N12	GND_44	GND_139	AD11
N13	GND_45	GND_140	AD13
N14	GND_46	GND_141	AD15
N15	GND_47	GND_142	AD17
N16	GND_48	GND_143	AD21
N17	GND_49	GND_144	AD23
N18	GND_50	GND_145	AD25
N19	GND_51	GND_146	AD31
N20	GND_52	GND_147	AD34
N21	GND_53	GND_148	AE11
N22	GND_54	GND_149	AE12
N23	GND_55	GND_150	AE14
N24	GND_56	GND_151	AE15
N25	GND_57	GND_152	AE16
P12	GND_58	GND_153	AE17
P14	GND_59	GND_154	AE18
P18	GND_60	GND_155	AE19
P20	GND_61	GND_156	AE20
P22	GND_62	GND_157	AE21
P24	GND_63	GND_158	AE22
R2	GND_64	GND_159	AE23
R5	GND_65	GND_160	AE24
R6	GND_66	GND_161	AE25
R31	GND_67	GND_162	AG2
R34	GND_68	GND_163	AG31
T11	GND_69	GND_164	AG34
T13	GND_70	GND_166	AK2
T15	GND_71	GND_167	AK5
T17	GND_72	GND_168	AK31
T19	GND_73	GND_170	AK34
T21	GND_74	GND_171	AL6
T23	GND_75	GND_172	AL9
T25	GND_76	GND_173	AL12
U11	GND_77	GND_174	AL15
U12	GND_78	GND_175	AL18
U13	GND_79	GND_176	AL21
U14	GND_80	GND_177	AL24
U15	GND_81	GND_178	AL27
U16	GND_82	GND_179	AL30
U17	GND_83	GND_180	AN2
U18	GND_84	GND_181	AN34
U19	GND_85	GND_182	AP3
U20	GND_86	GND_183	AP6
U21	GND_87	GND_184	AP9
U22	GND_88	GND_185	AP12
U23	GND_89	GND_186	AP15
U24	GND_90	GND_187	AP18
U25	GND_91	GND_188	AP21
V2	GND_92	GND_189	AP24
V5	GND_93	GND_190	AP27
V9	GND_94	GND_191	AP30
V12	GND_95	GND_192	AP33
V14	GND_96	GND_193	



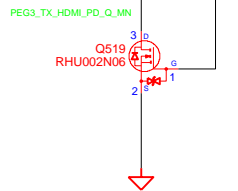
DRAW	Xiaohong Zheng	DATE	8/14/2007	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	EXT NB9X	PART NO.	
APPROVAL	BC LEE	REV	1.0	NB9X CHIP (3/4)	BA41-01190/1/2A	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	25 OF 62	

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U5-4
N11P-GE1-B-A3

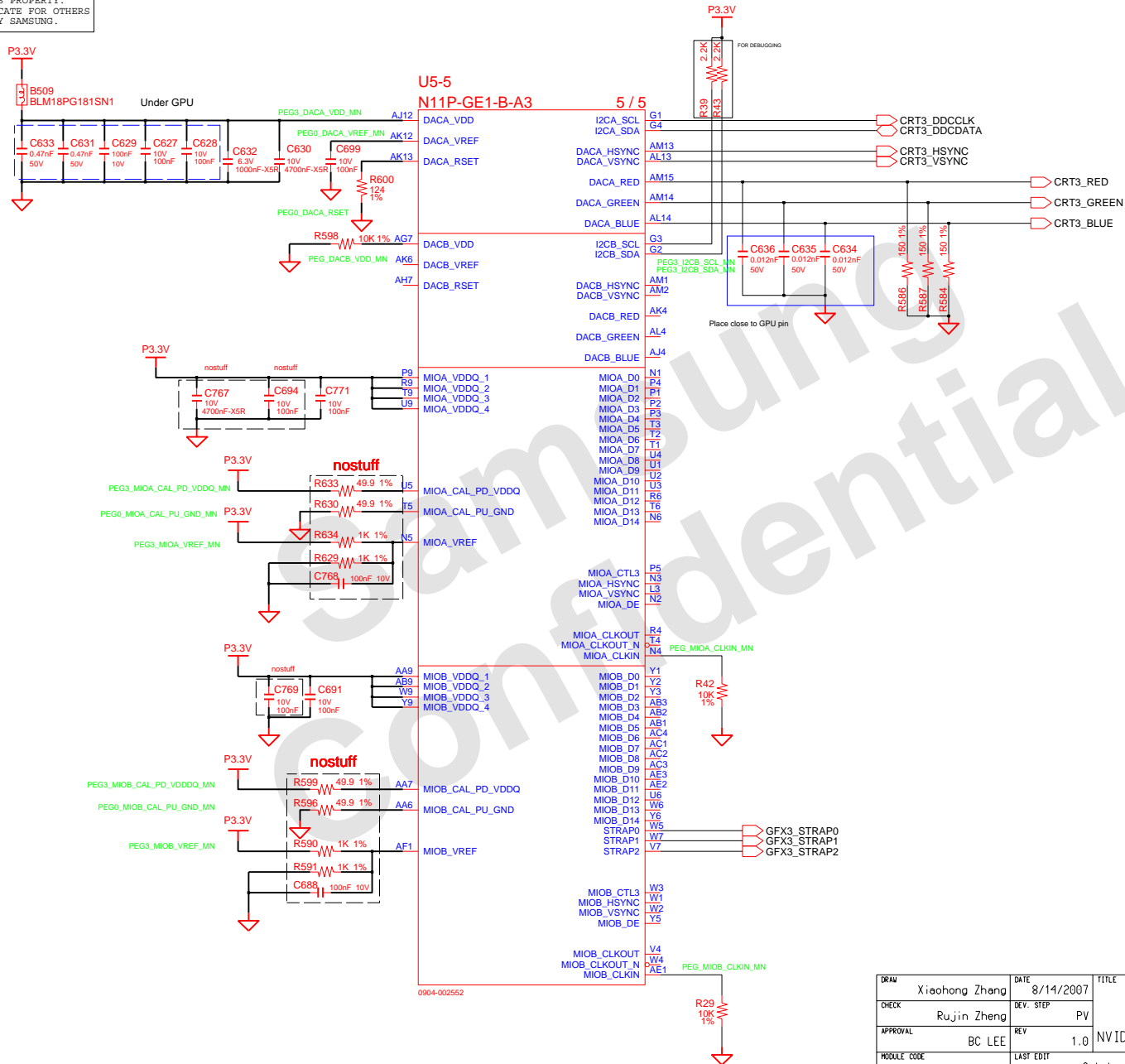


PEG3_TX2P_HDMI	R663	499	1%
PEG3_TX2N_HDMI	R662	499	1%
PEG3_TX1P_HDMI	R661	499	1%
PEG3_TX1N_HDMI	R660	499	1%
PEG3_TX0P_HDMI	R620	499	1%
PEG3_TX0N_HDMI	R621	499	1%
PEG3_TXCP_HDMI	R618	499	1%
PEG3_TXCN_HDMI	R619	499	1%



DRAW	Xiaohong Zheng	DATE	8/14/2007	TITLE	Suzhou_M EXT NB9X	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	NVIDIA_NB9X_9P		
APPROVAL	BC LEE	REV	1.0	October 10, 2009 00:22:55 AM	PAGE	26 OF 62
MODULE CODE	LAST EDIT				PART NO. BA41-01190/1/2A	

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0904-002552

DRAW	Xiaohong Zheng	DATE	8/14/2007	TITLE	Suzhou_M EXT NB9X	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	NVIDIA_NB9X_SP POWER RAIL		
APPROVAL	BC LEE	REV	1.0	PART NO. BA41-01190/1/2A		PAGE 27 OF 62
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM			

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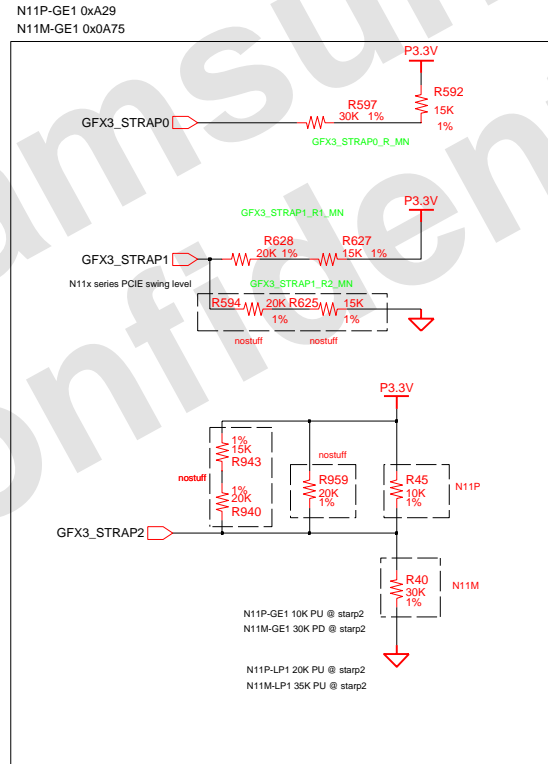
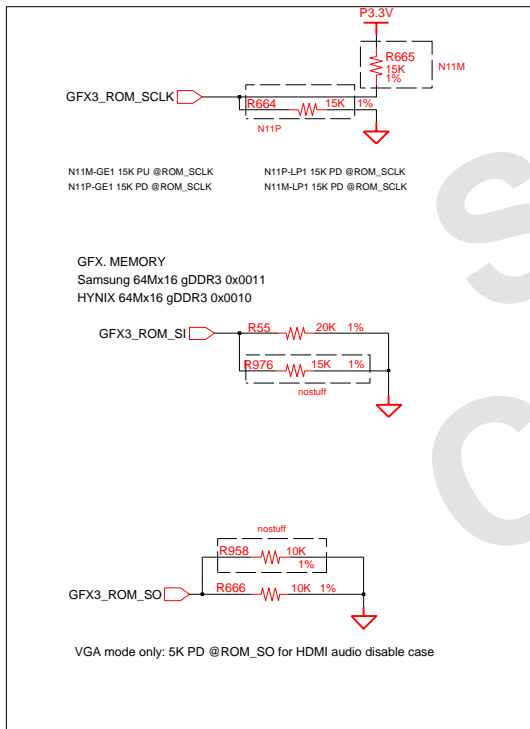
N11x_40nm STRAP

Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8v 10 0.95v
GPIO(6)	GPU VID1	01 0.85v 11 1.03v
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC

Pin	Description	Activate
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



N11P-GE1

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIe swing level
Strap0	1	1	1	1	EDID_EN

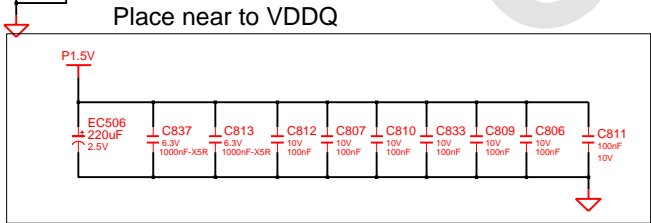
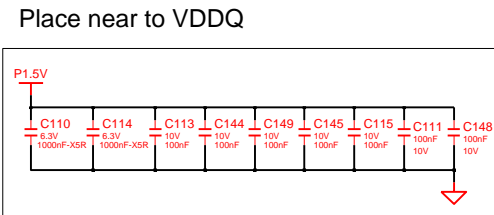
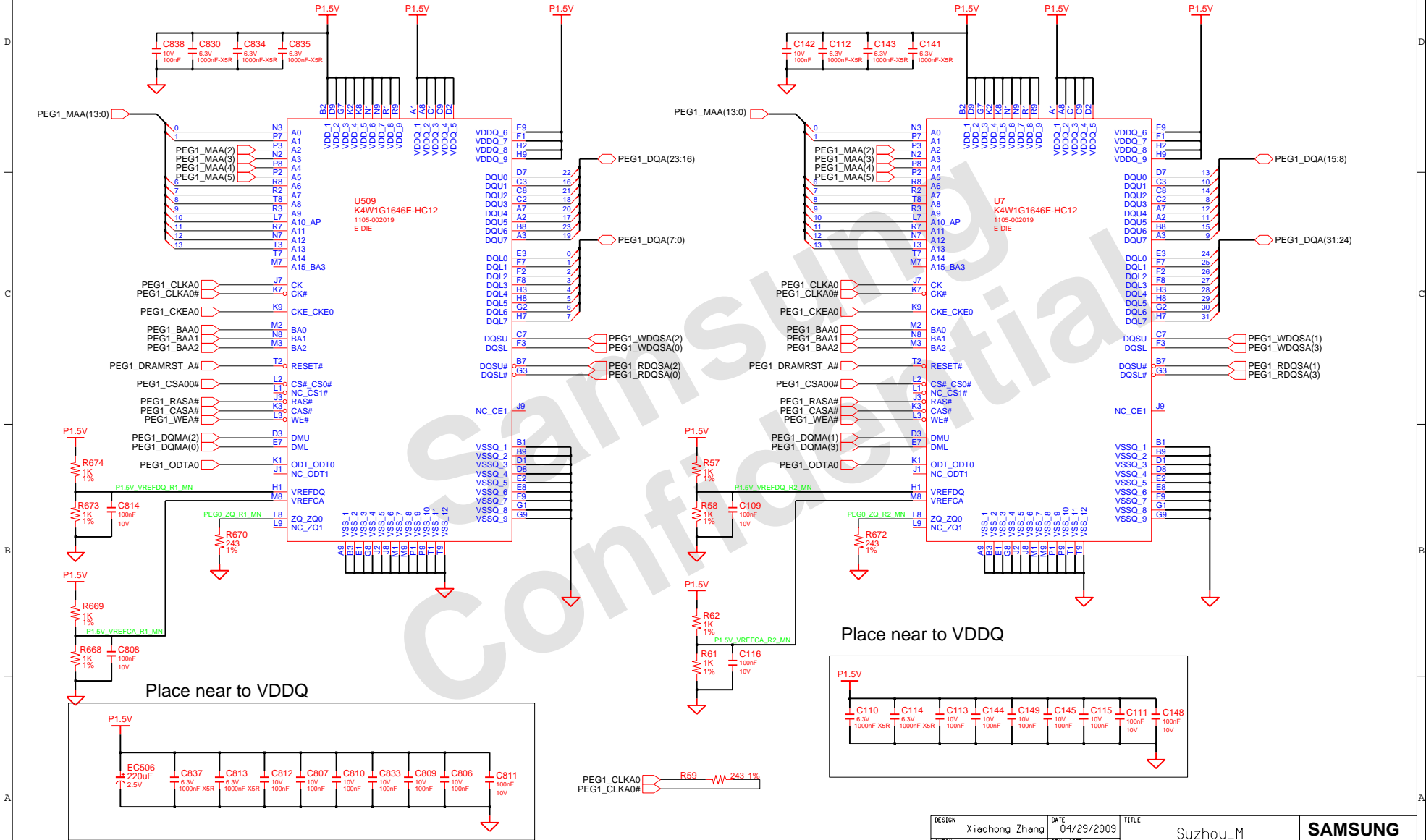
N11M-GE1

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIe swing level
Strap0	1	1	1	1	EDID_EN

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A-Channel #0



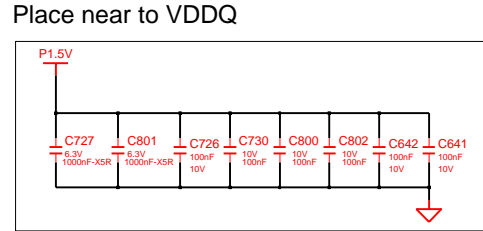
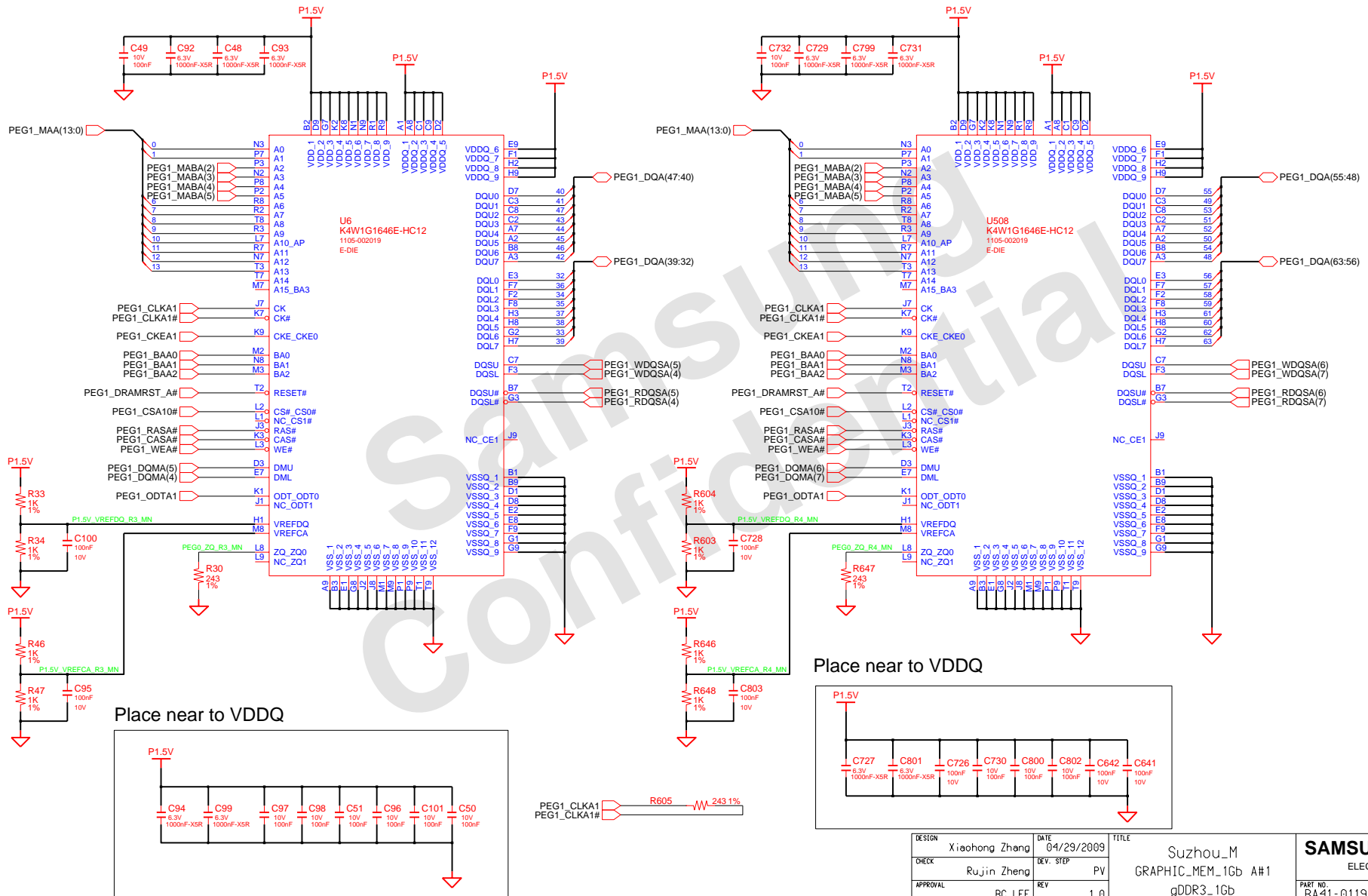
DESIGN	Xiaohong Zheng	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb A#0	
APPROVAL	BC LEE	REV	1.0	gDDR3-1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	29 OF 62

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A-Channel #1



DESIGN	Xiaohong Zheng	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb AH1	
APPROVAL	BC LEE	REV	1.0	gDDR3-1Gb	
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	30 OF 62

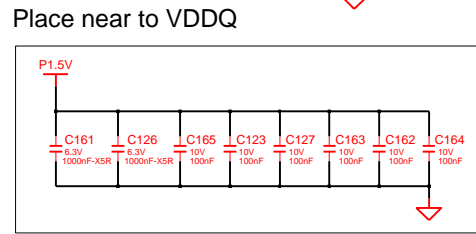
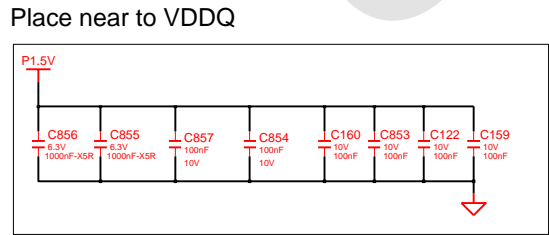
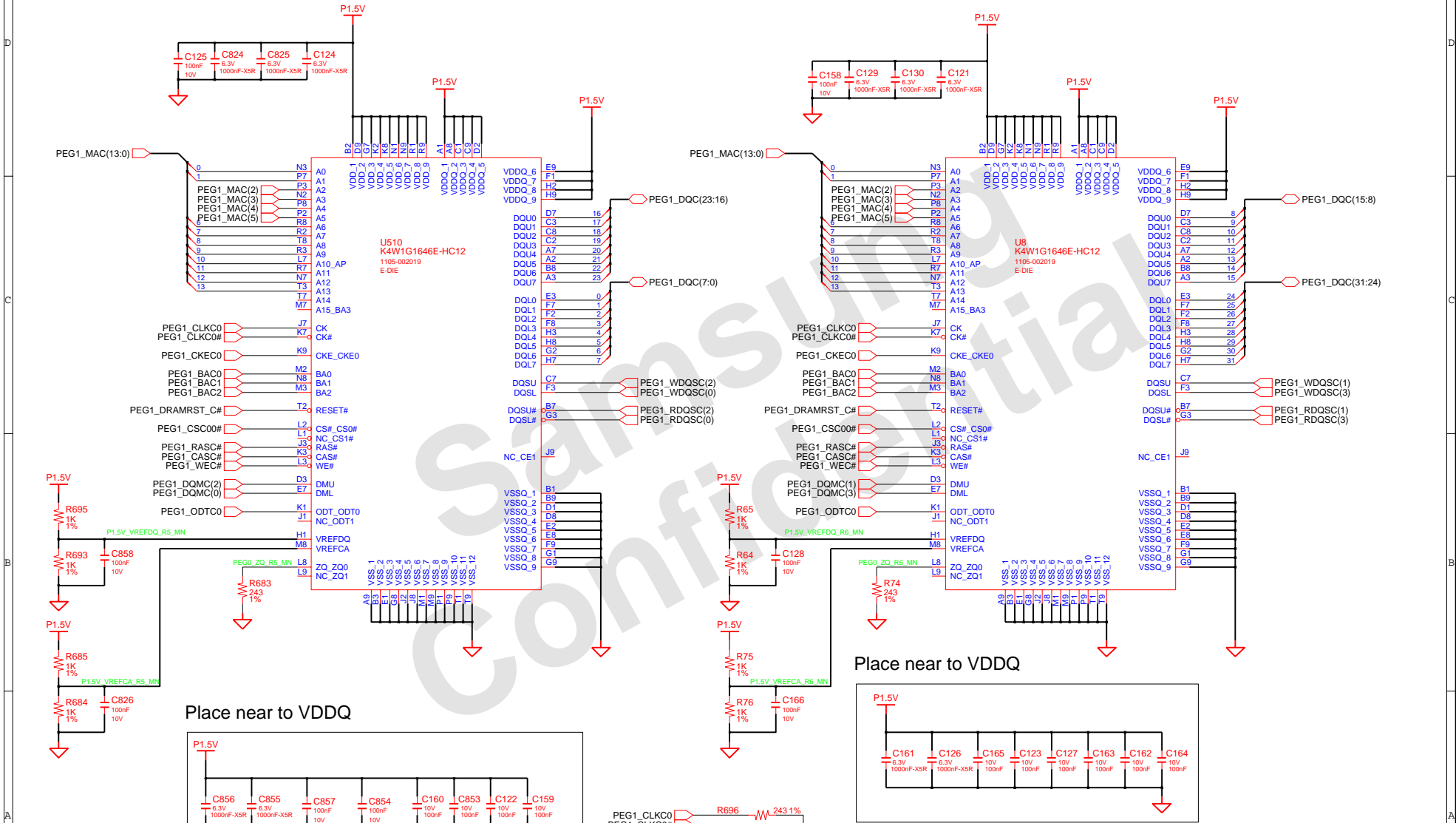
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C-Channel #0

N11P



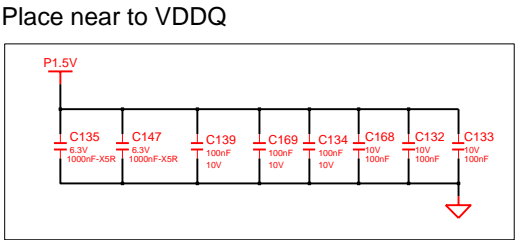
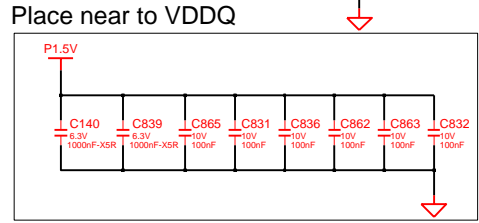
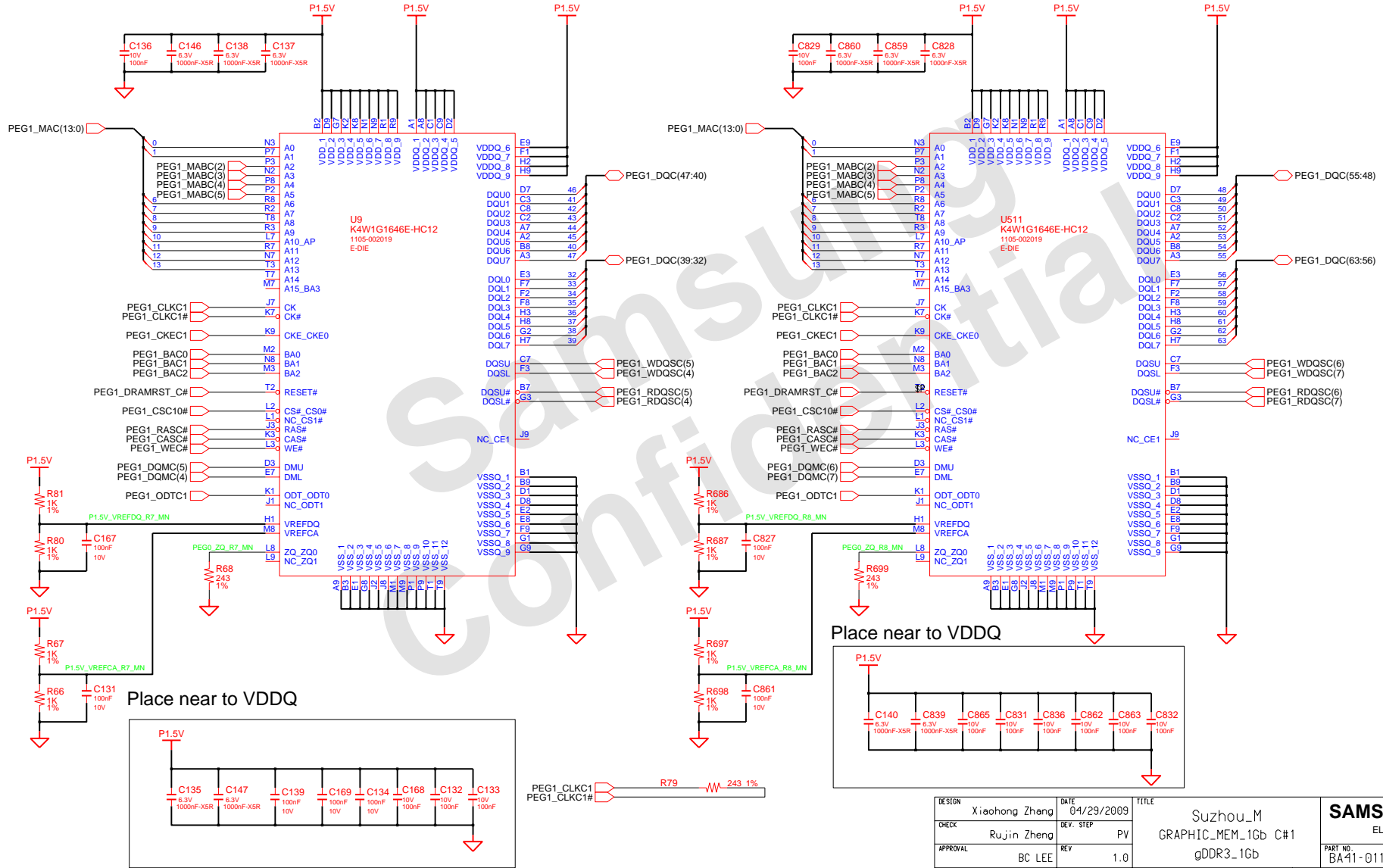
DESIGN	Xiaohong Zheng	DATE	04/29/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb C#0		
APPROVAL	BC LEE	REV	1.0	gDDR3-1Gb		PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	31	OF 62

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C-Channel #1

N11P



DESIGN	Xiaohong Zheng	DATE	04/29/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV	GRAPHIC_MEM_1Gb C#1		
APPROVAL	BC LEE	REV	1.0	gDDR3-1Gb		
MODULE CODE		LAST EDIT		October 10, 2009 00:22:55 AM		
			PAGE	32 OF 62		

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gDDR3 Memory PULL UP & PULL DOWN

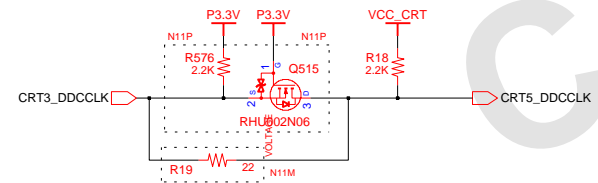
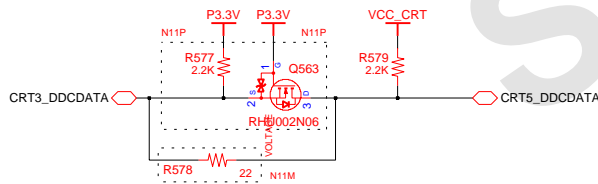
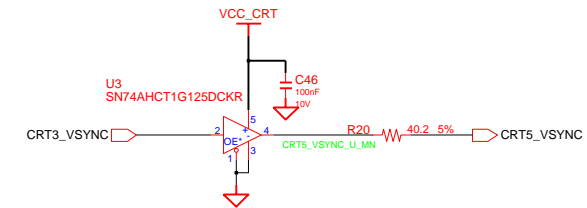
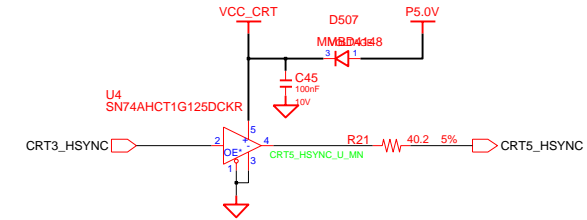


DESIGN	Xiaohong Zheng	DATE	03/14/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PULL-UP&PULL-DOWN		
APPROVAL	BC LEE	REV	1.0	gDDR3_1Gb		PART NO. BA41-01190/1/2A
MODULE CODE	LAST EDIT			October 10, 2009 00:22:55 AM	PAGE	33 OF 62

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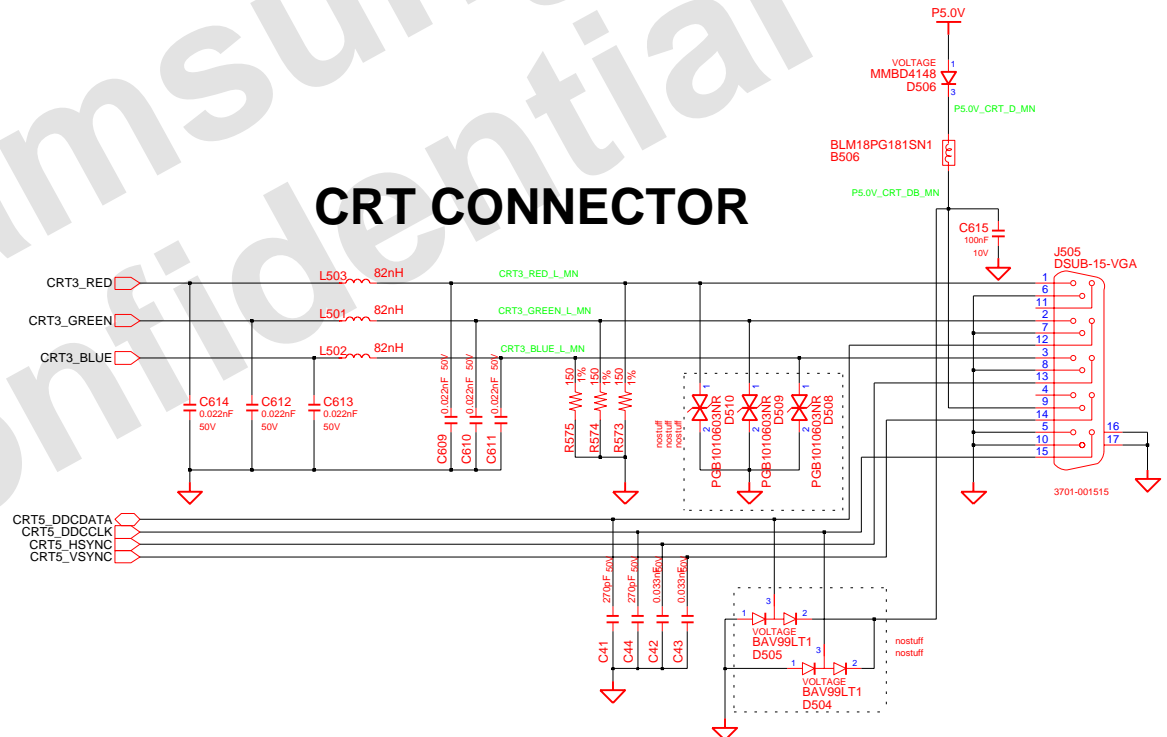
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CRT



Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

CRT CONNECTOR



DESIGN	Xiaohong Zheng	DATE	01/08/2009	TITLE	Suzhou_M GRAPHICS_IF CRT	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	34 OF 62	

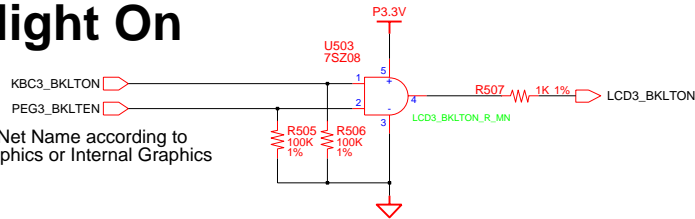
LVDS

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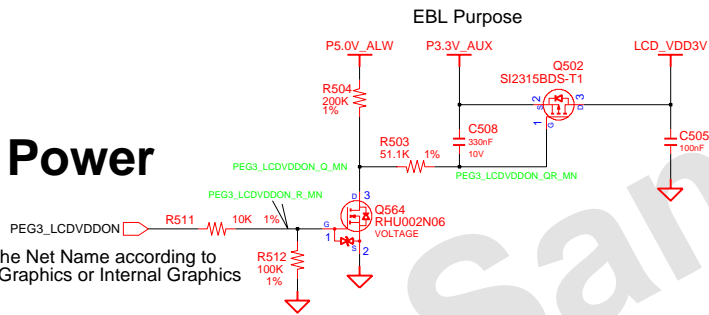
Backlight On

Change the Net Name according to External Graphics or Internal Graphics

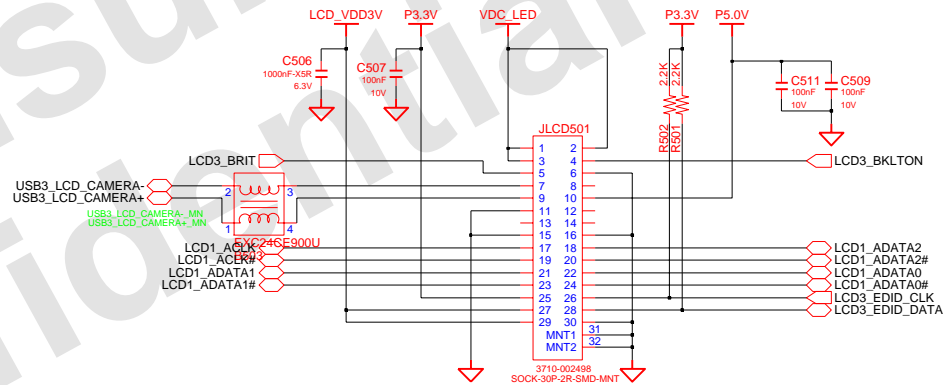


LCD Power

Change the Net Name according to External Graphics or Internal Graphics

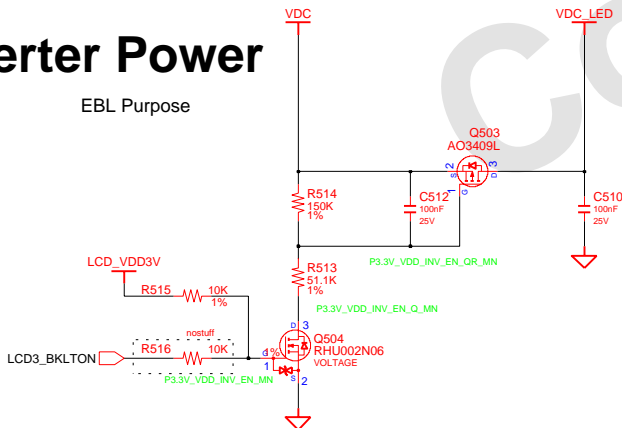


1Ch. LCD Connector



Inverter Power

EBL Purpose



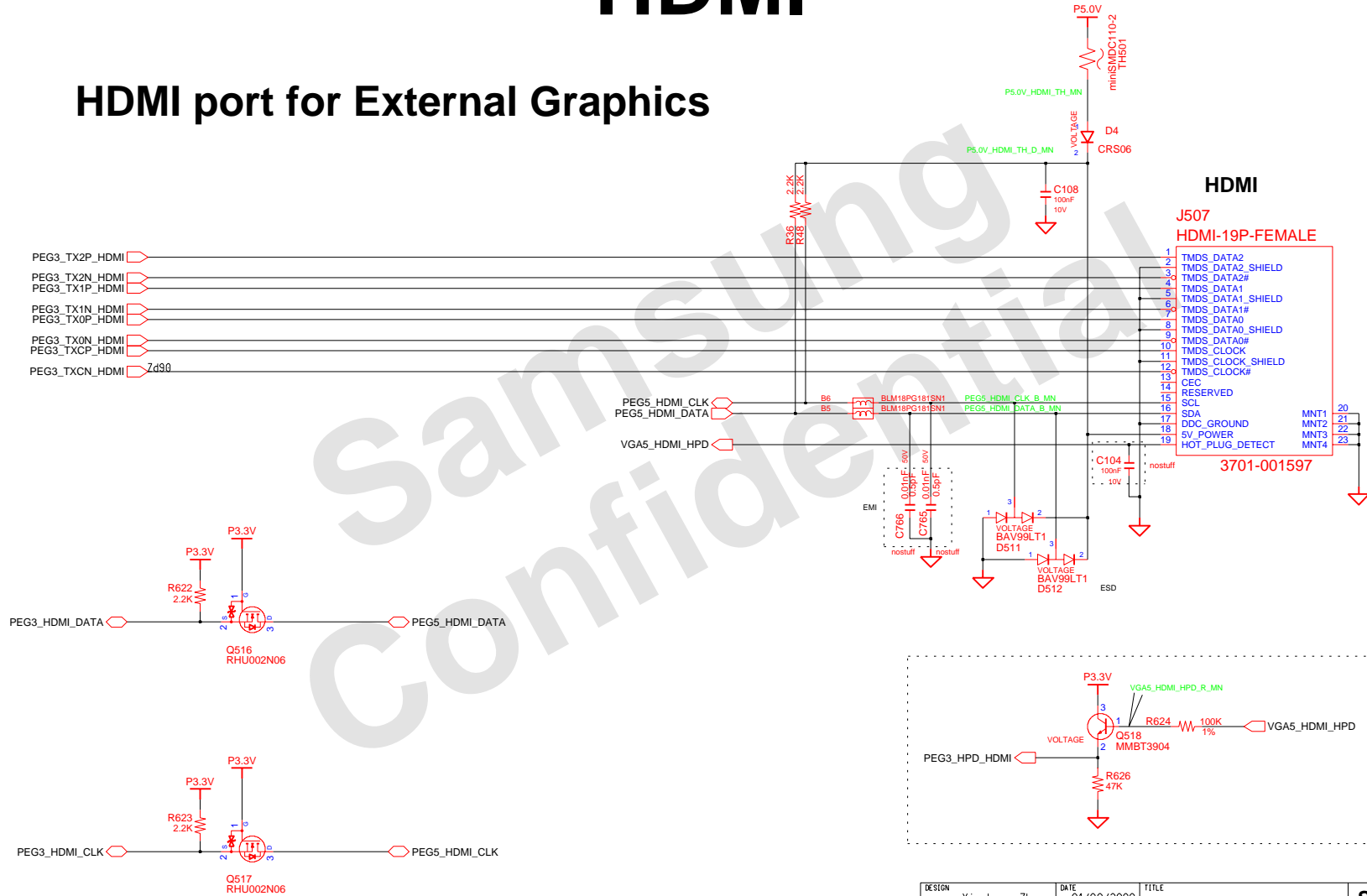
DESIGN	Xiaohong Zheng	DATE	01/08/2009	TITLE	Suzhou_M GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	35	OF 62

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HDMI

HDMI port for External Graphics

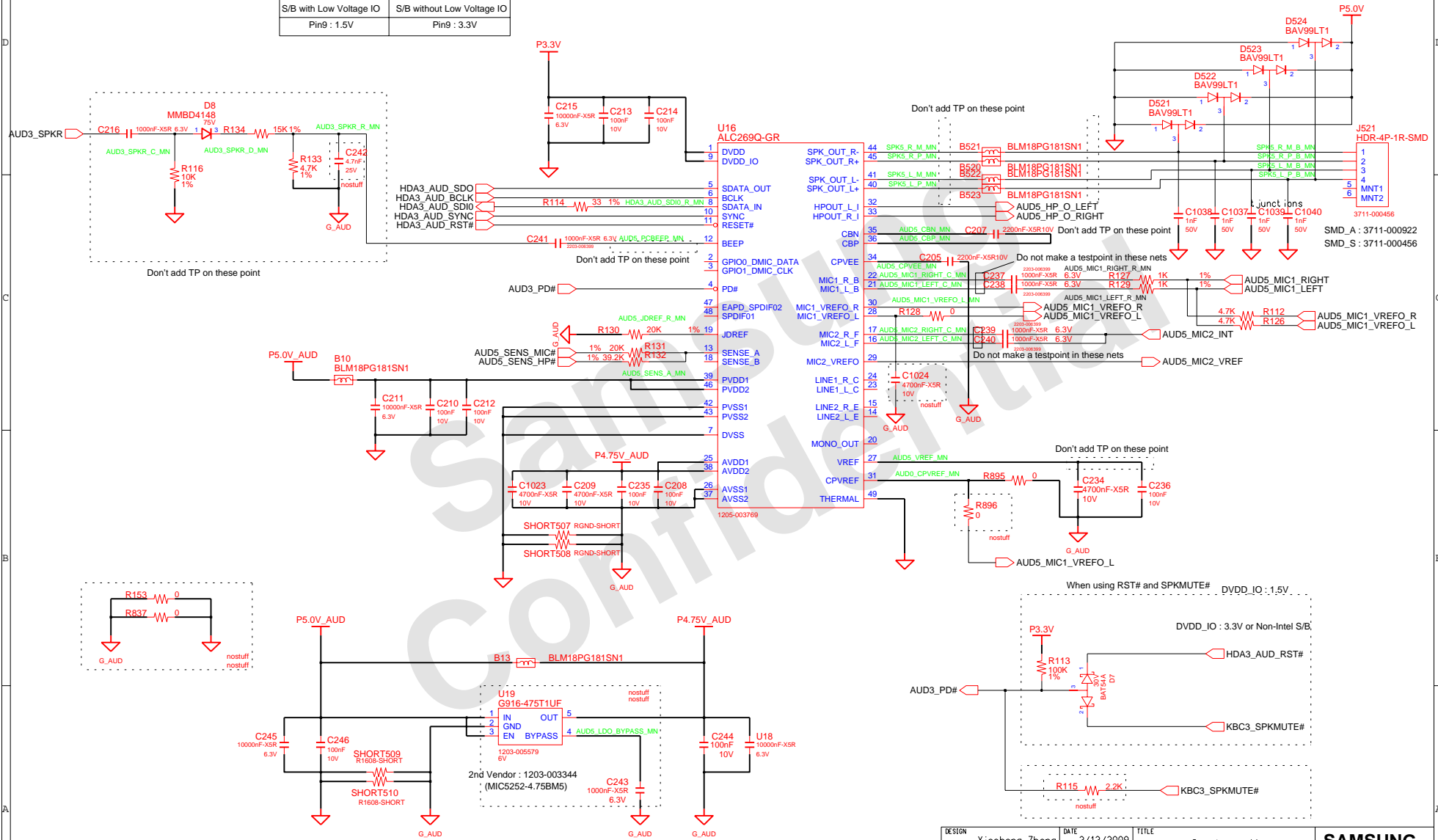


DESIGN	Xiaohong Zheng	DATE	01/08/2009	TITLE	Suzhou_M GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	36 OF 62	

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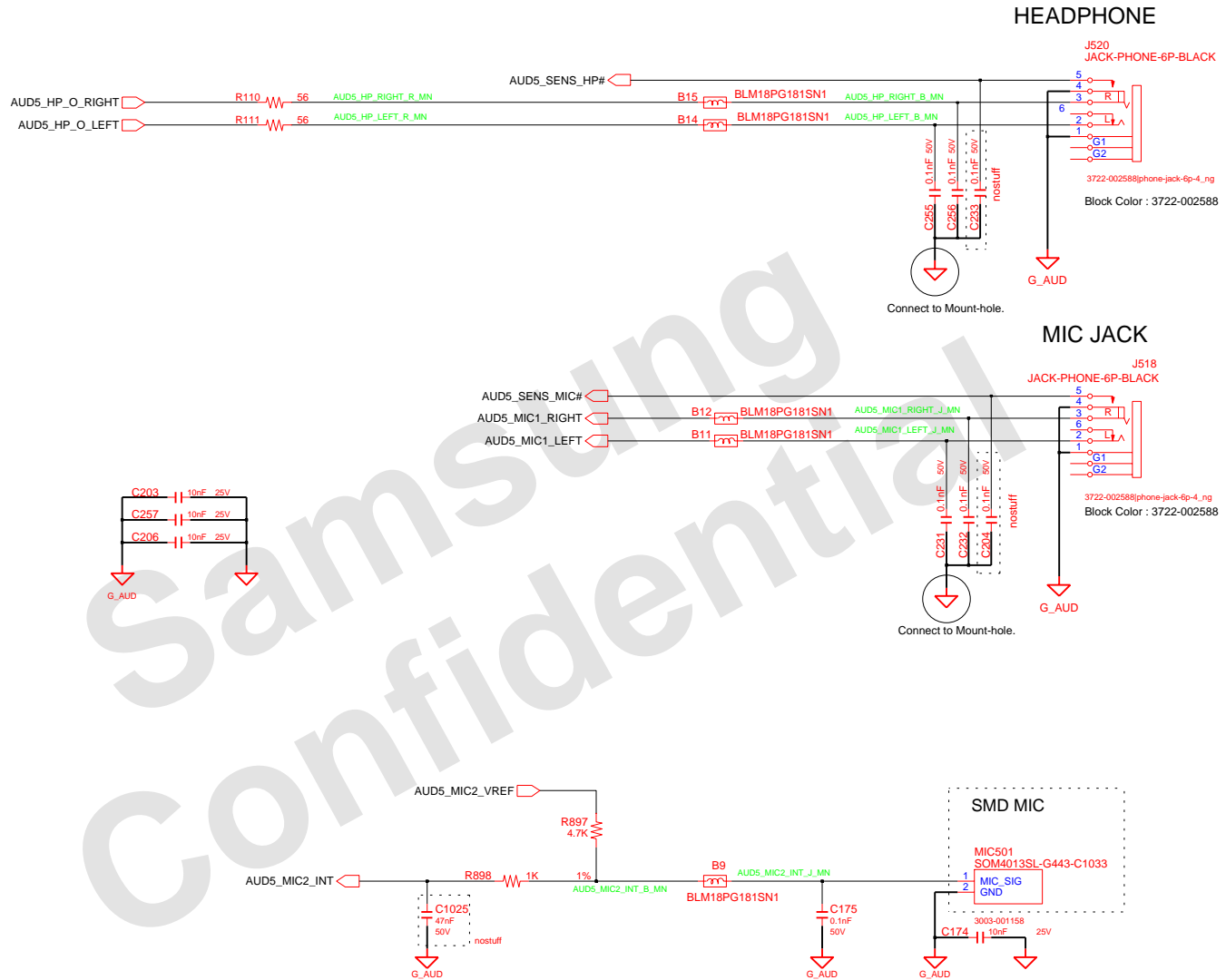
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	Xiaohong Zheng	DATE	3/13/2009	TITLE	Suzhou_M HDA_ALC269_GR AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	37 OF 62	

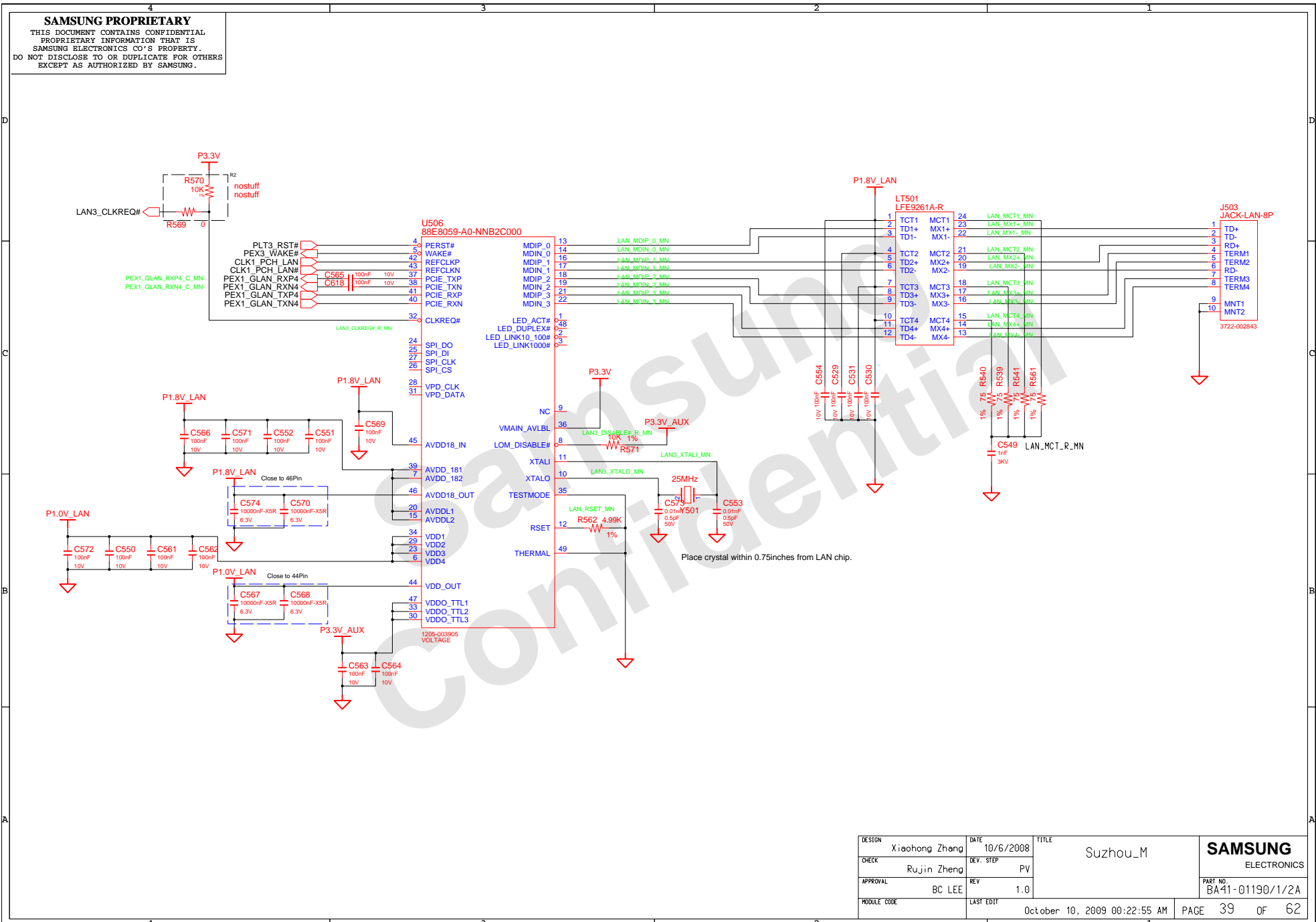
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DESIGN	Xiaohong Zheng	DATE	3/13/2009	TITLE	Suzhou_M HDA_ALC269_GR AUDIO INPUT/OUTPUT	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	38 OF 62	

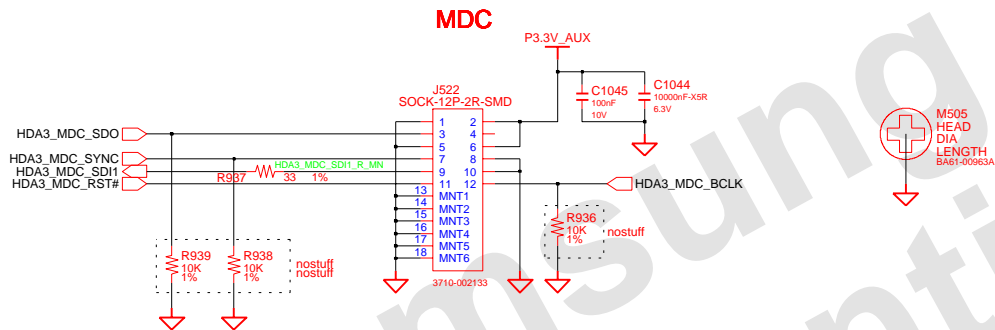
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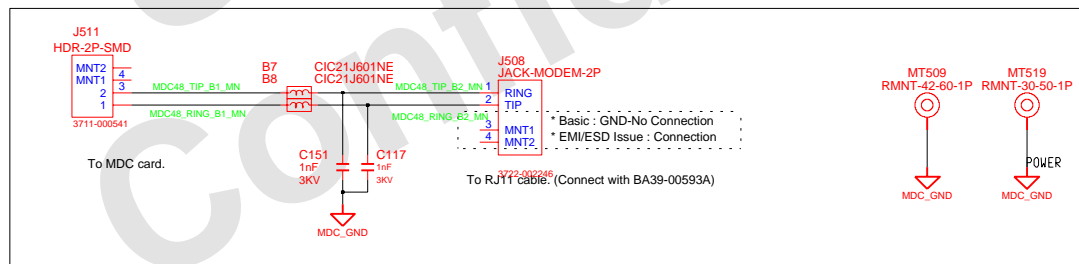
DESIGN	Xiaohong Zheng	DATE	10/6/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	39	OF 62

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MDC Connector



MDC SUB

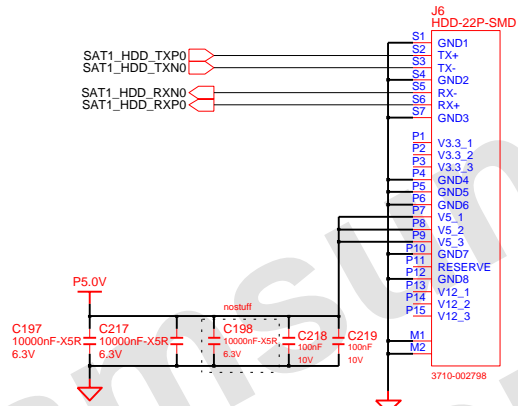


DESIGN	Xiaohong Zheng	DATE	8/20/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	UNDEF INED	UNDEF INED	
APPROVAL	BC LEE	REV	1.0	UNDEF INED	UNDEF INED	PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	40	OF 62

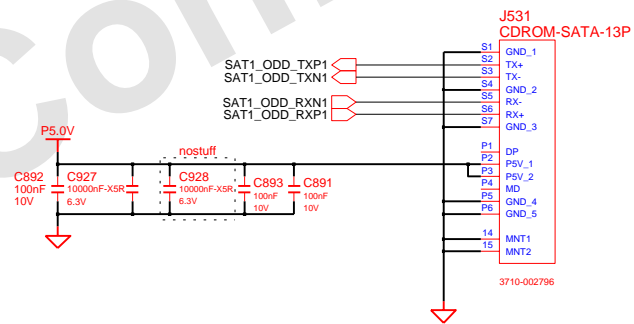
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SATA I/F CONN

SATA HDD CONN



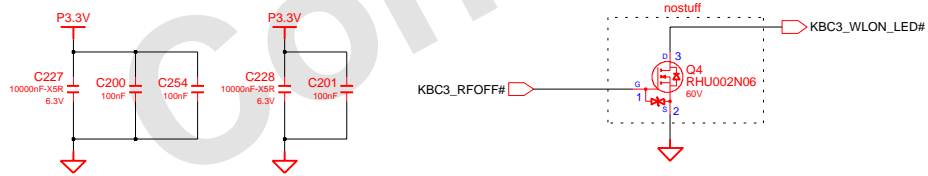
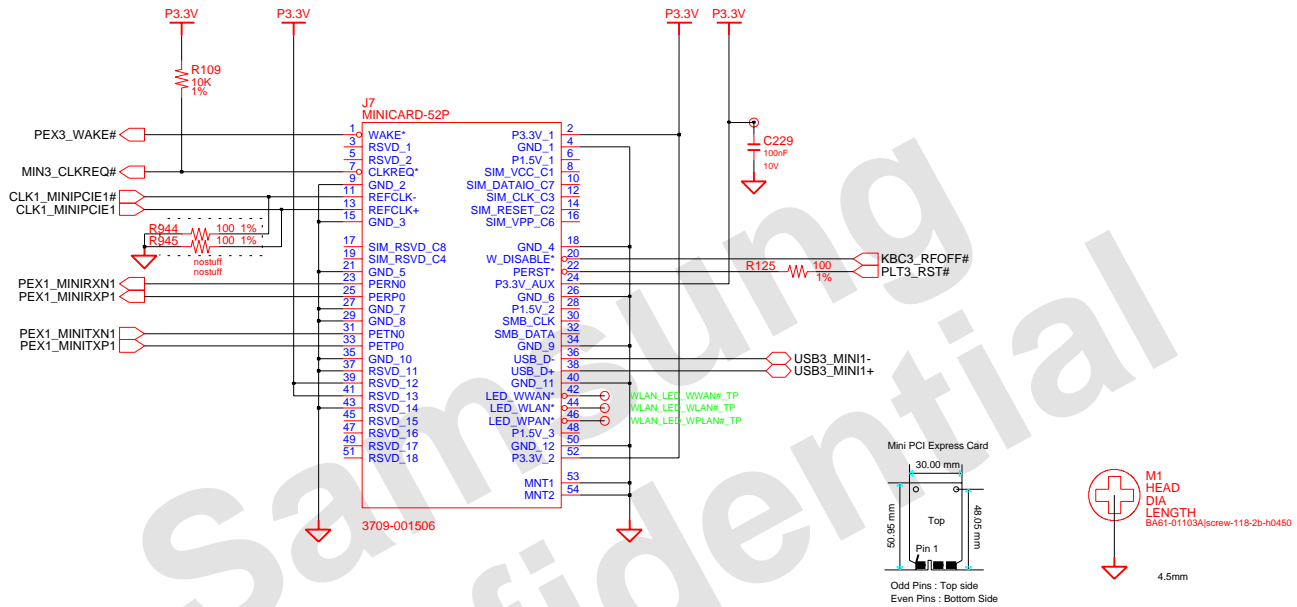
SATA ODD CONN



DESIGN	Xiaohong Zheng	DATE	6/6/2008	TITLE	Suzhou_M SATA_DEVICES	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	41	OF 62

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WLAN, 7mm

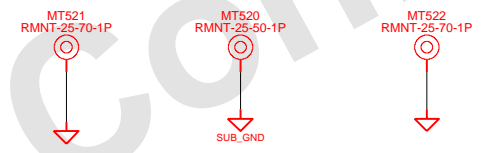
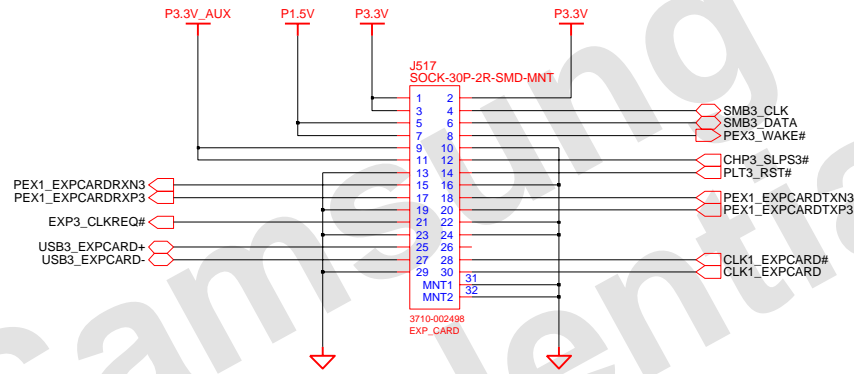


DESIGN	Xiaohong Zheng	DATE	6/6/2008	TITLE	Suzhou_M MINI_PCIE_CONN	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	42	OF 62

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Express Card

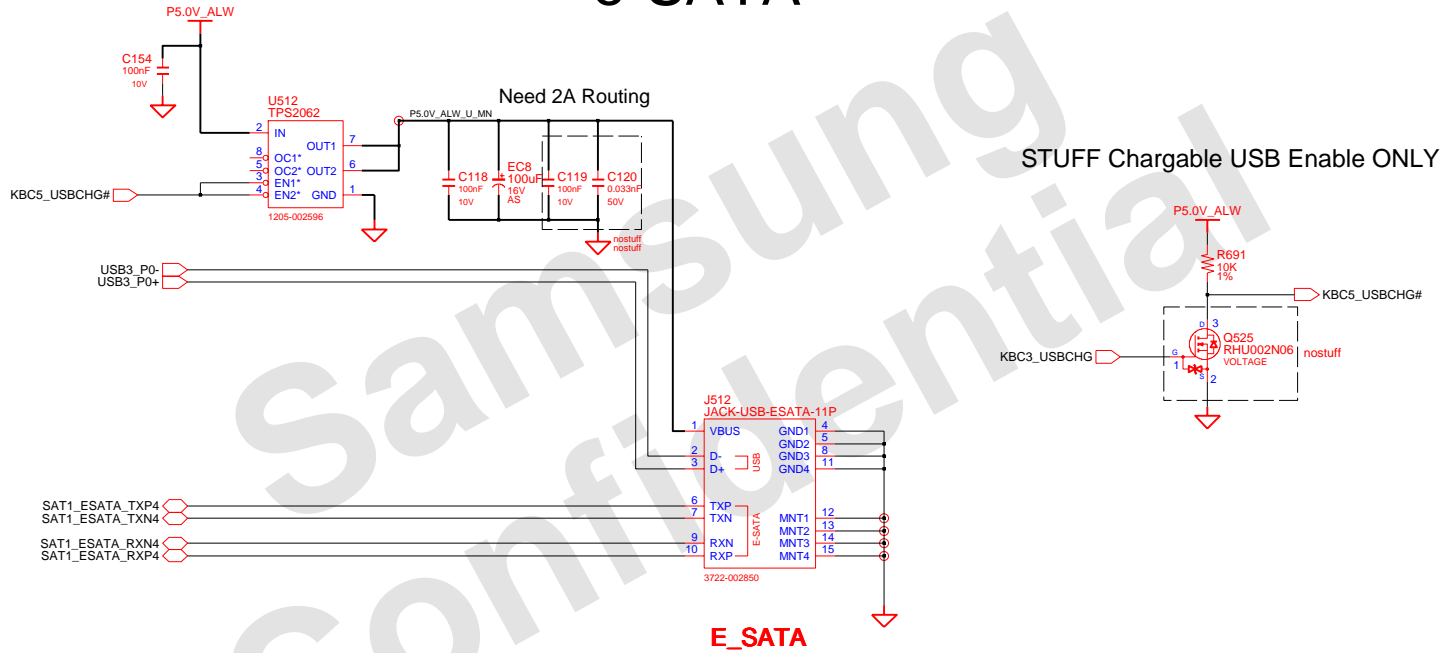


DESIGN	Xiaohong Zheng	DATE	7/7/2008	TITLE	Suzhou_M EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0		PART NO.	BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	43	OF 62

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e-SATA



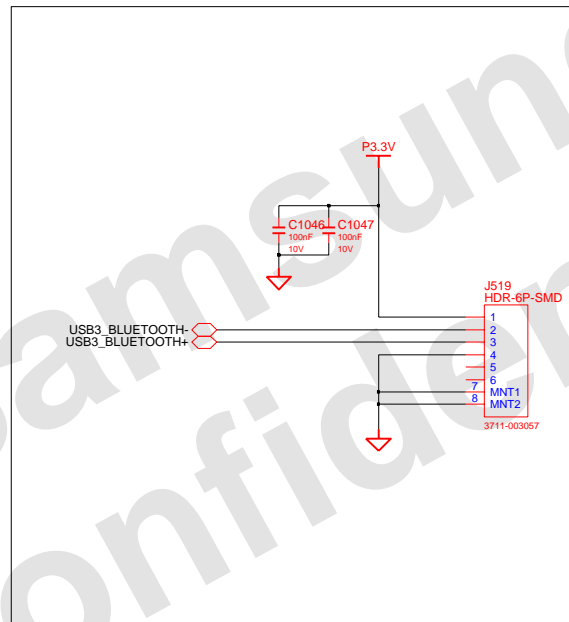
STUFF Chargeable USB Enable ONLY

E_SATA

DRAW	Xiaohong Zheng	DATE	11/8/2006	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MINI CARD		
APPROVAL	BC LEE	REV	1.0	SILOH & EBRO	PART NO.	BA41-01190/1/2A
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	44	OF 62

USB I/F Devices

Bluetooth Interface



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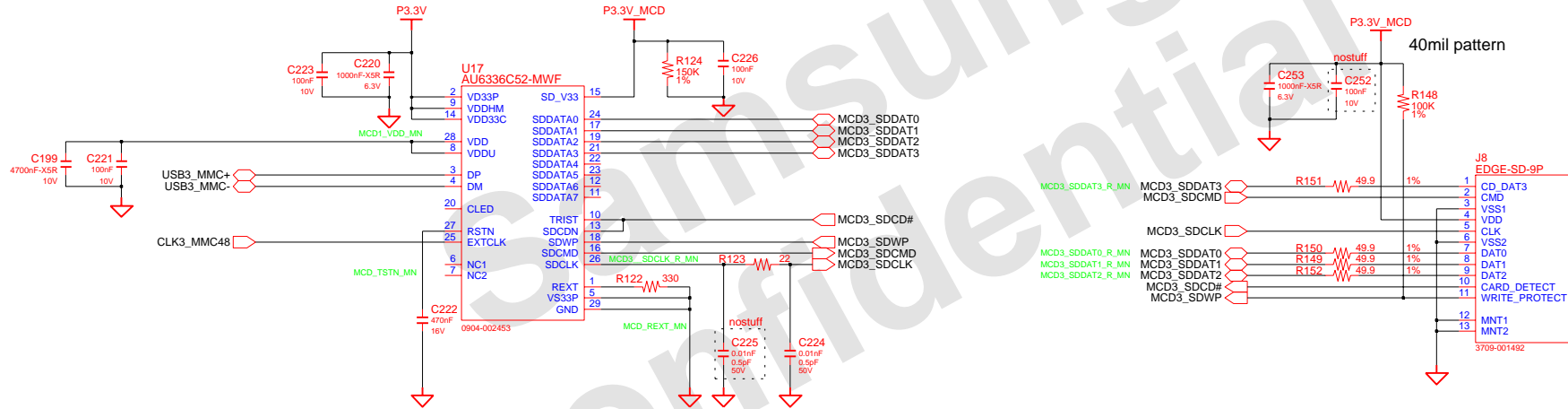
DESIGN	Xiaohong Zheng	DATE	6/6/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	USB_DEVICES		
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	45	OF 62

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3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches



40 mil trace for medica card socket ground

MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

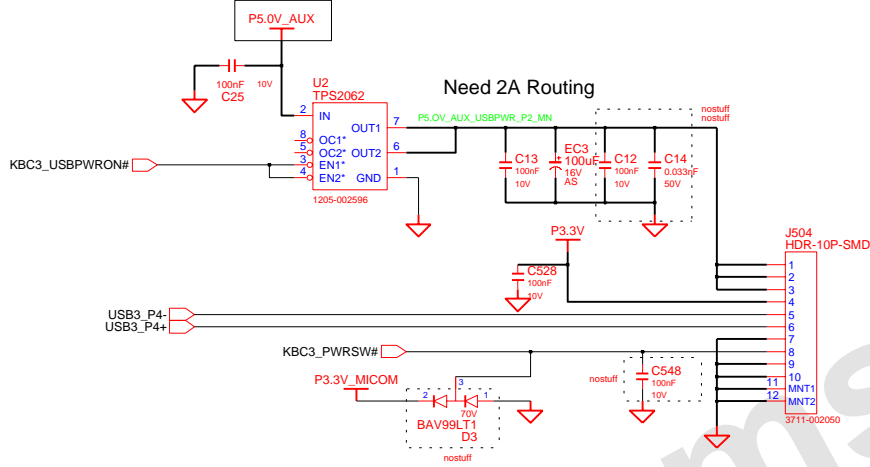
DESIGN	Xiaohong Zheng	DATE	10/15/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV		MMC	
APPROVAL	BC LEE	REV	1.0		AU6336	PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	46	OF 62

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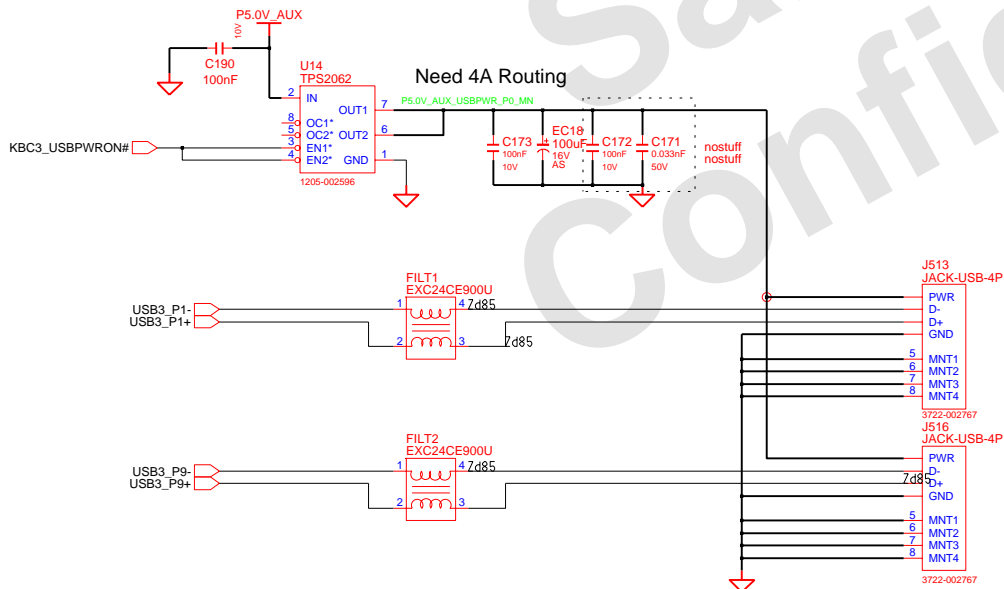
Main board

1 PORT USB CONNECTOR

Adopt P5.0V_ALW when enable chargeable USB.

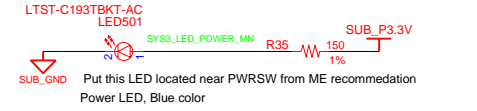


1*2 PORT USB CONNECTOR

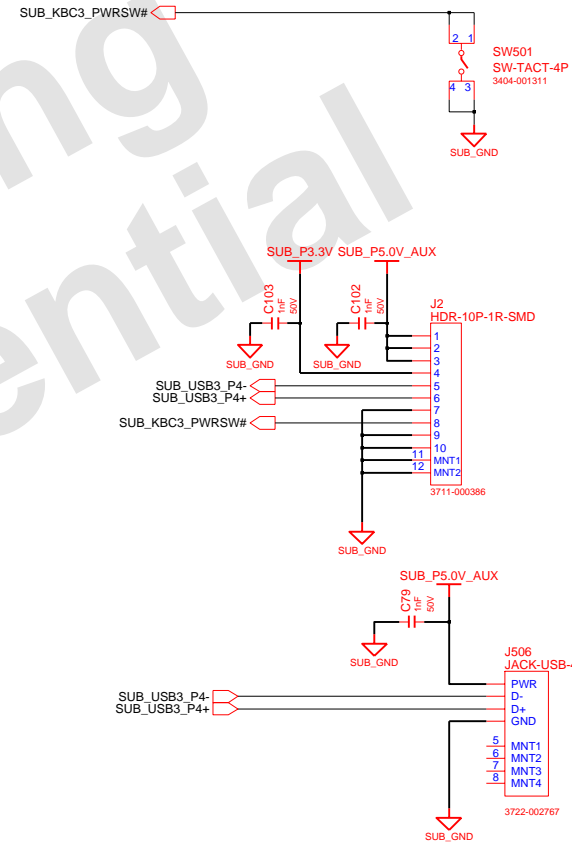


Sub board

Power Switch Button



PU TO P3.3V_MICOM IS at micom logic side.

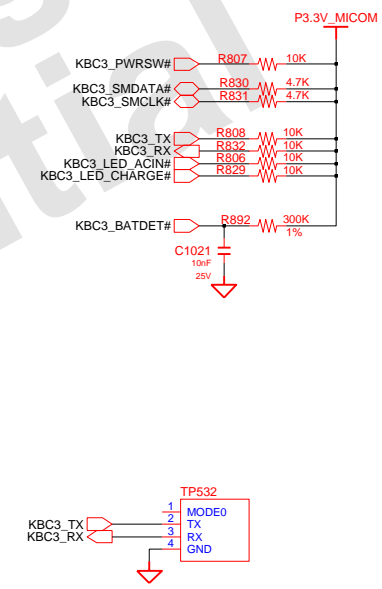
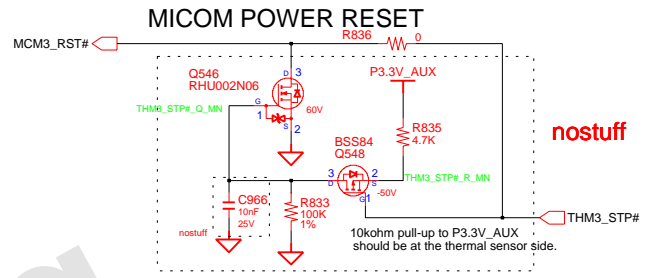
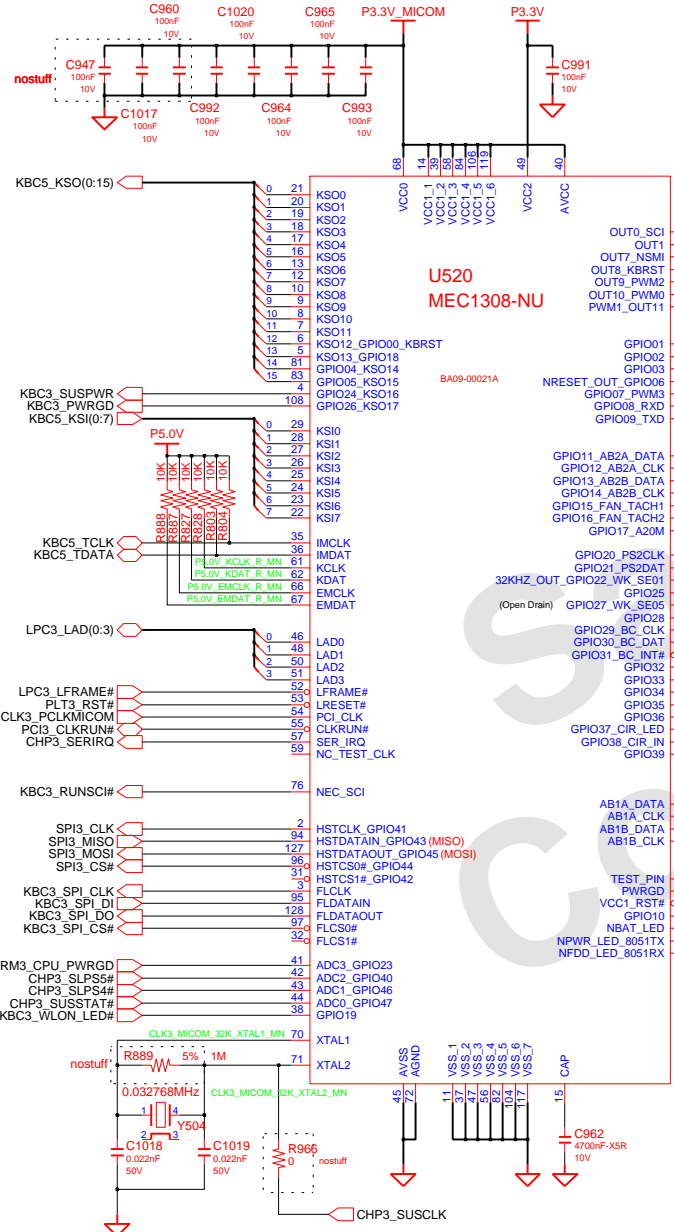


DESIGN	Xiaohong Zheng	DATE	6/6/2008	TITLE	Suzhou_M USB_CONN	SAMSUNG ELECTRONICS PART NO. BA41-01190/1/2A
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	47 OF 62	

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MAIN BOARD (MICOM)

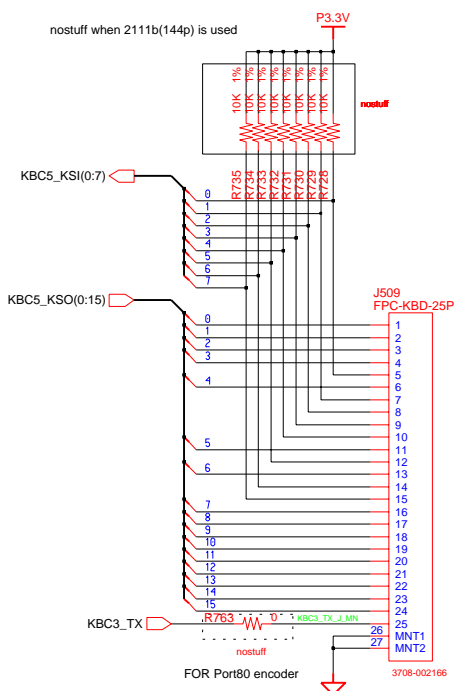


DRAW	Xiaohong Zheng	DATE	05/20/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	MICOM_SMSC_MEC1308	PART NO.	
APPROVAL	BC LEE	REV	1.0	MICOM_SMSC_MEC1308	PAGE	48 OF 62
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM			

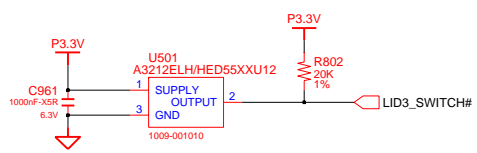
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Micom Glue Logic

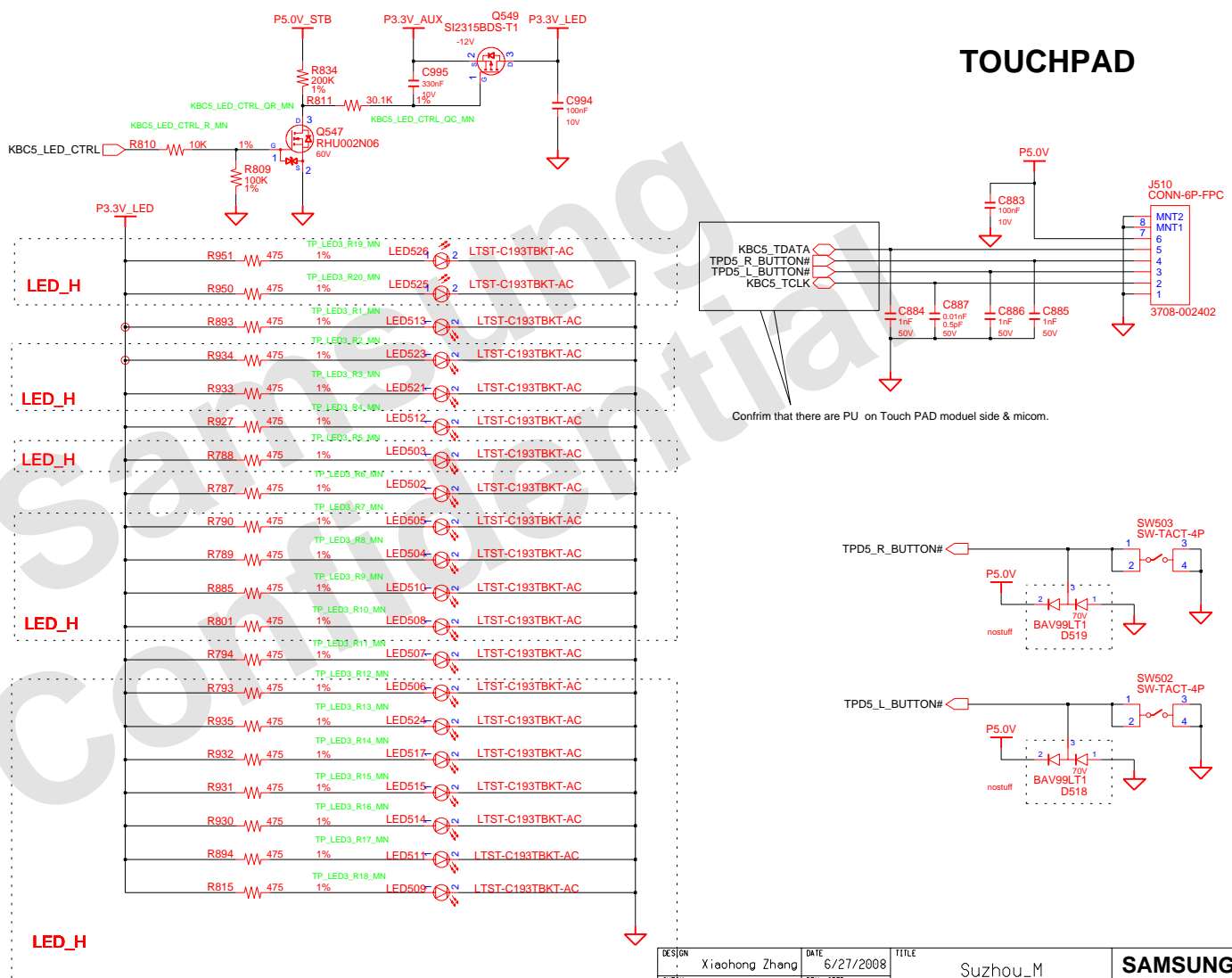
KEYBOARD



LID_SWITCH



TOUCHPAD



DESIGN	Xiaohong Zhang	DATE	6/27/2008	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	49	OF 62

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LED SWITCH LOGIC

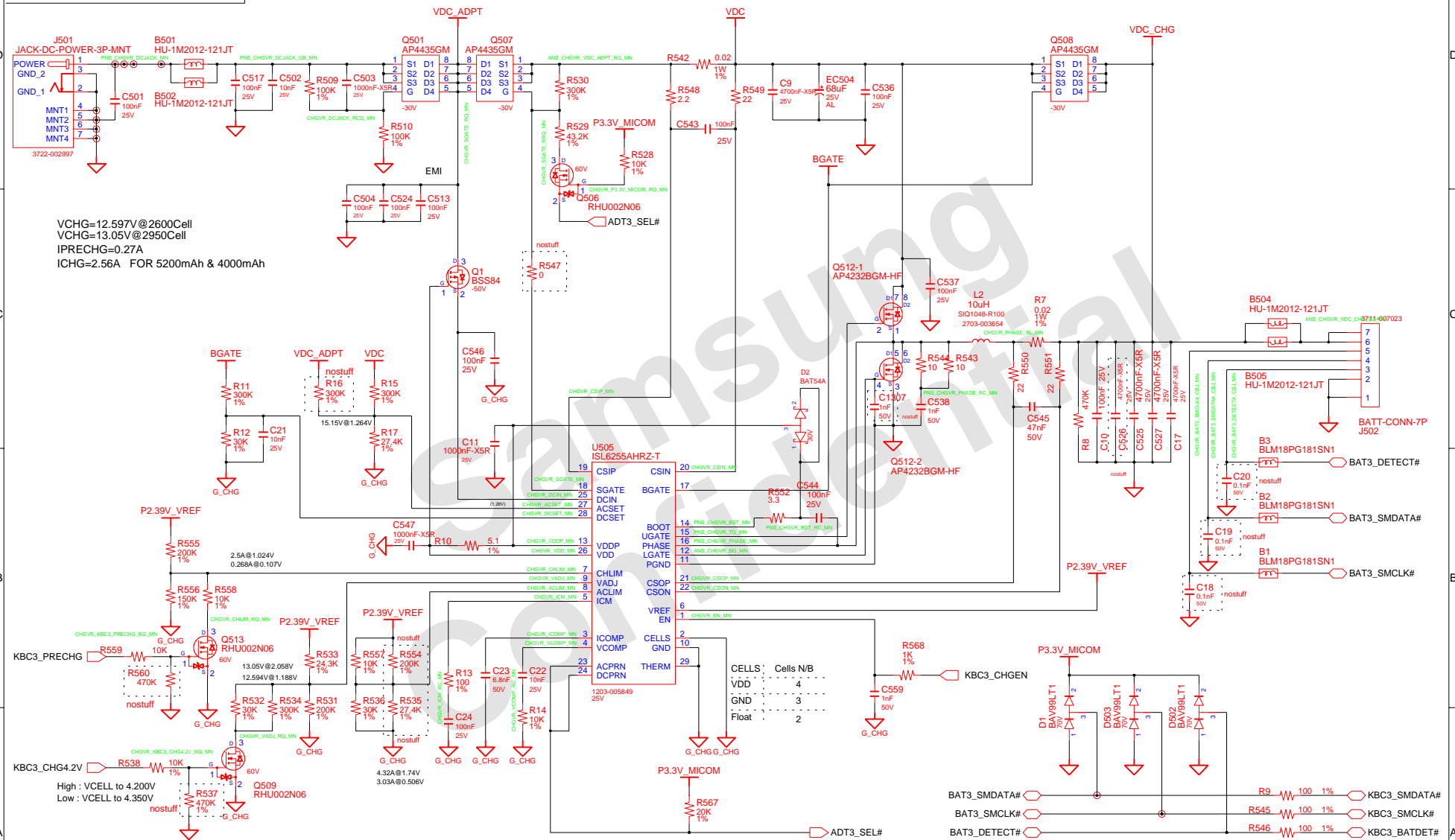
Function Key LEDs



DRAW	Xiaohong Zhang	DATE	8/12/2006	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	LED_Switch	LED_Switch	
APPROVAL	BC LEE	REV	1.0	LED_Switch	LED_Switch	PART NO. BA41-01190/1/2A
MODULE CODE		LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	50	OF 62

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CHARGER & POWER MANAGEMENT



VCHG=12.597V@2600Cell
 VCHG=13.05V@2950Cell
 IPRECHG=0.27A
 ICHG=2.56A FOR 5200mAh & 4000mAh

Adapter configuration				
60W / 3.03A / 96%		90W / 4.32A / 91.2%		
Value	SEC Code	Value	SEC Code	
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30K	2007-008275

CELLS: Cells NB	
VDD	4
GND	3
Float	2

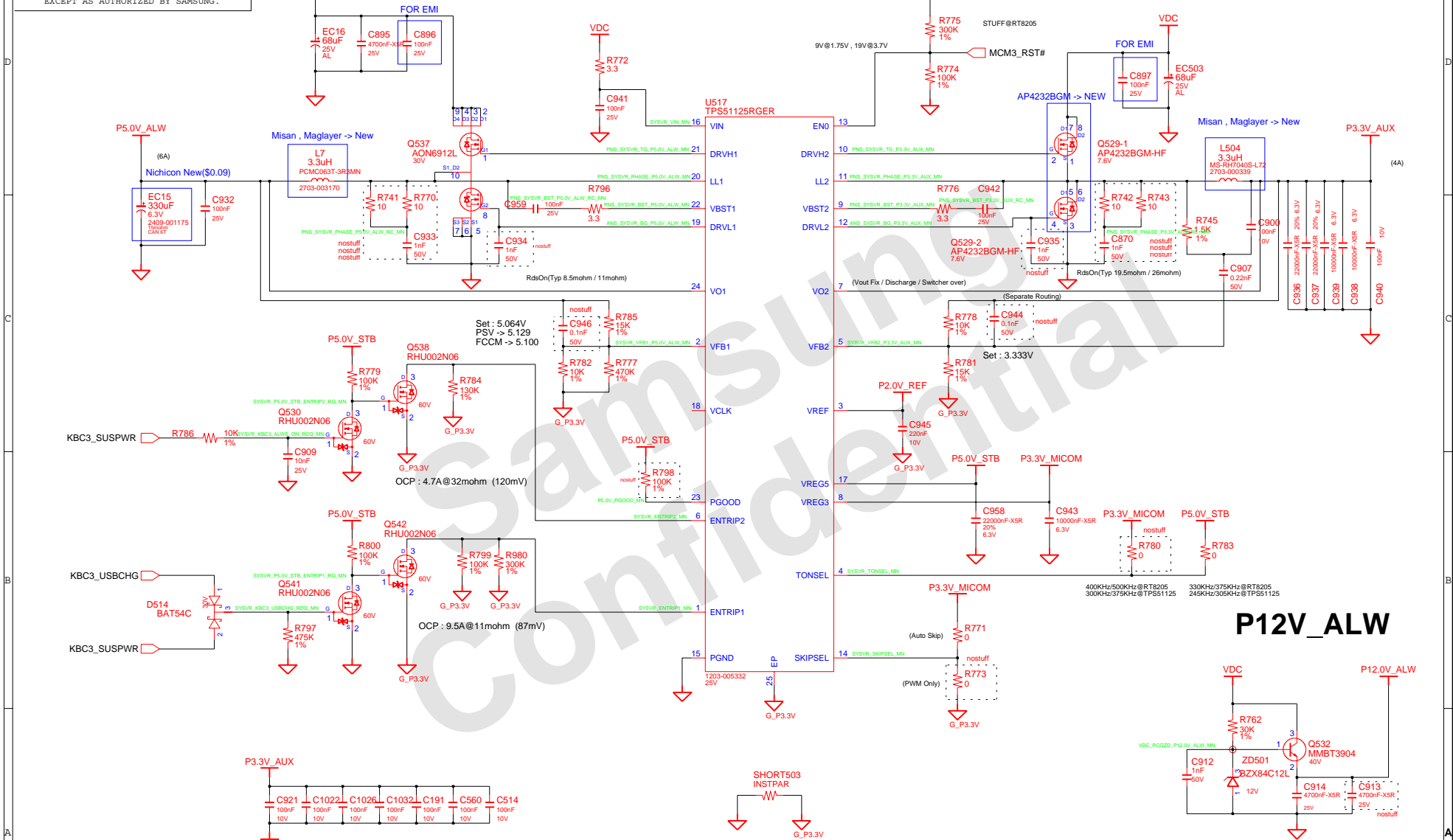
DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_MV_Charger_Isi6256a
APPROVAL	BC LEE	REV	1.0		CHARGER (ISL6256A)
MODULE CODE	undefined	LAST ENT	October 10, 2009 00:22:55 AM	PAGE	51 OF 62

SAMSUNG ELECTRONICS
PART NO. BA41-01190/1/2A

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P3.3V_AUX & P5.0V_ALW

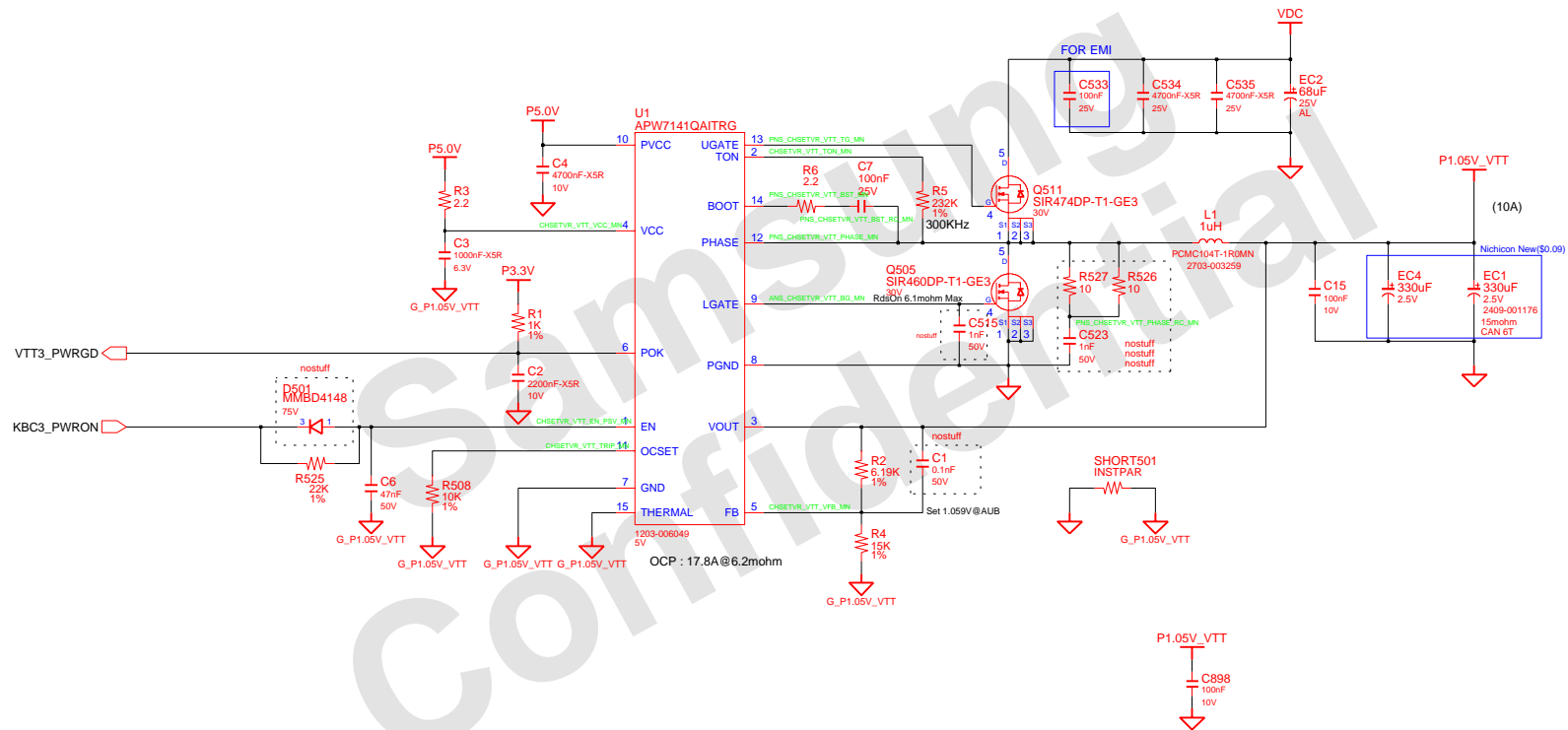


P12V_ALW

DRAW	Xiaohong Zhang	DATE	04/01/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_3V_5V_Rt8205a	PART NO.	
APPROVAL	BC LEE	REV	1.0	P3.3V_AUX / P5.0V_AUX	BA41-01190/1/2A	
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	52	OF 62

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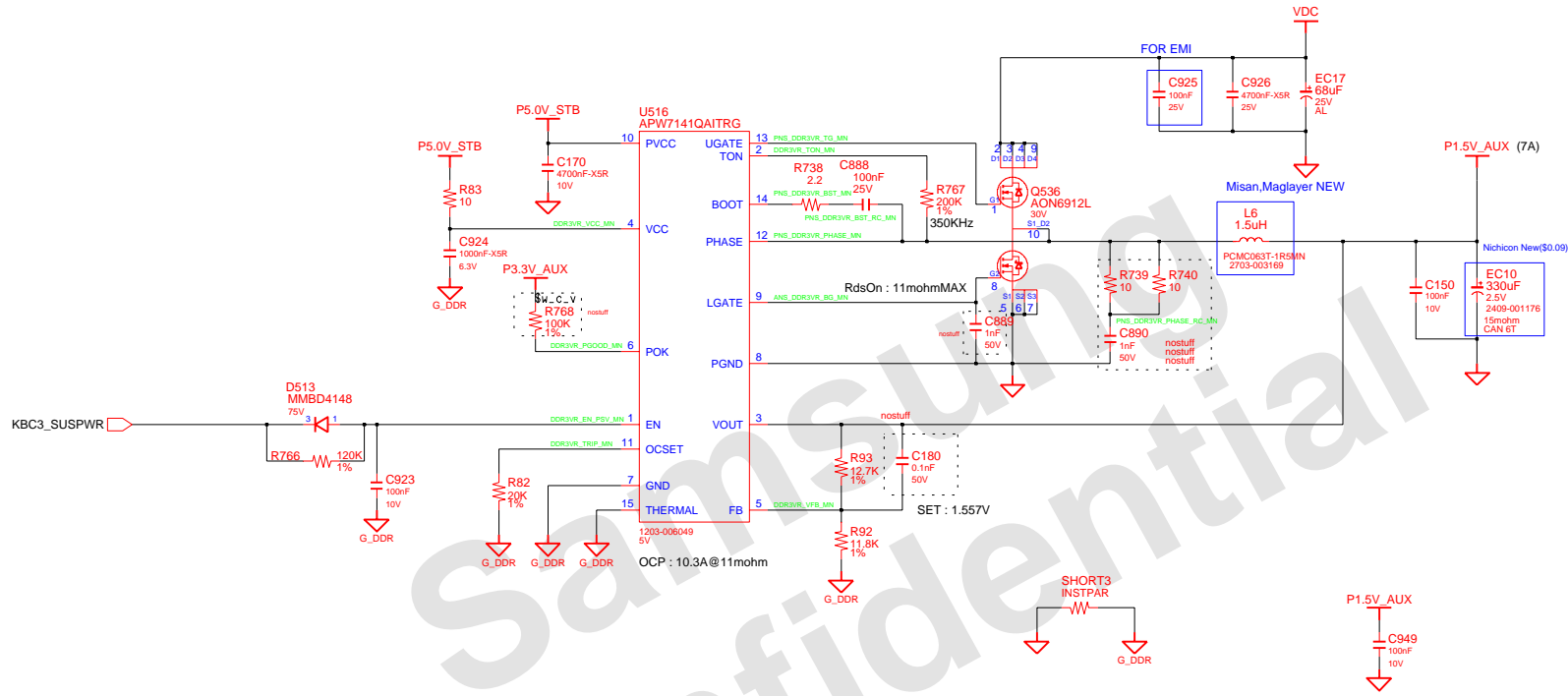
CHIPSET POWER(P1.05V_VTT & P1.05V)



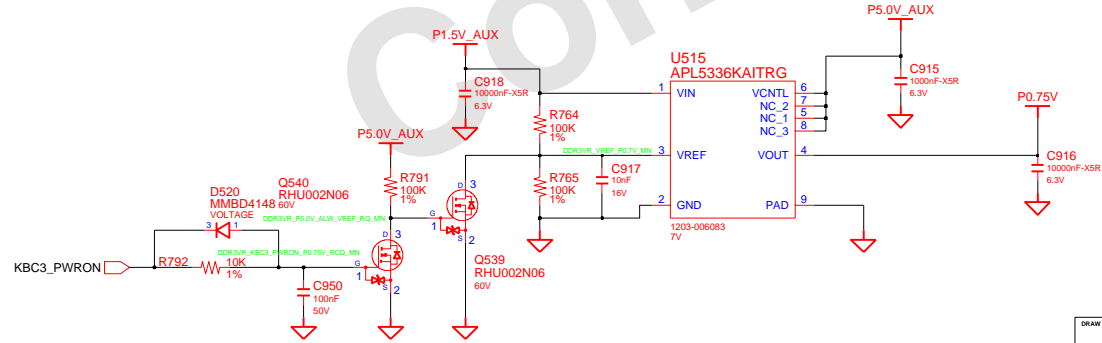
DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Cantiga		
APPROVAL	BC LEE	REV	1.0	Chipset Power (P1.05V_M,P1.2V)	PART NO.	BA41-01190/1/2A
MODULE CODE	undefined	LAST ENT	October 10, 2009 00:22:55 AM	PAGE	53	OF 62

DDR3 Power

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DDR3 VTT(0.75V)

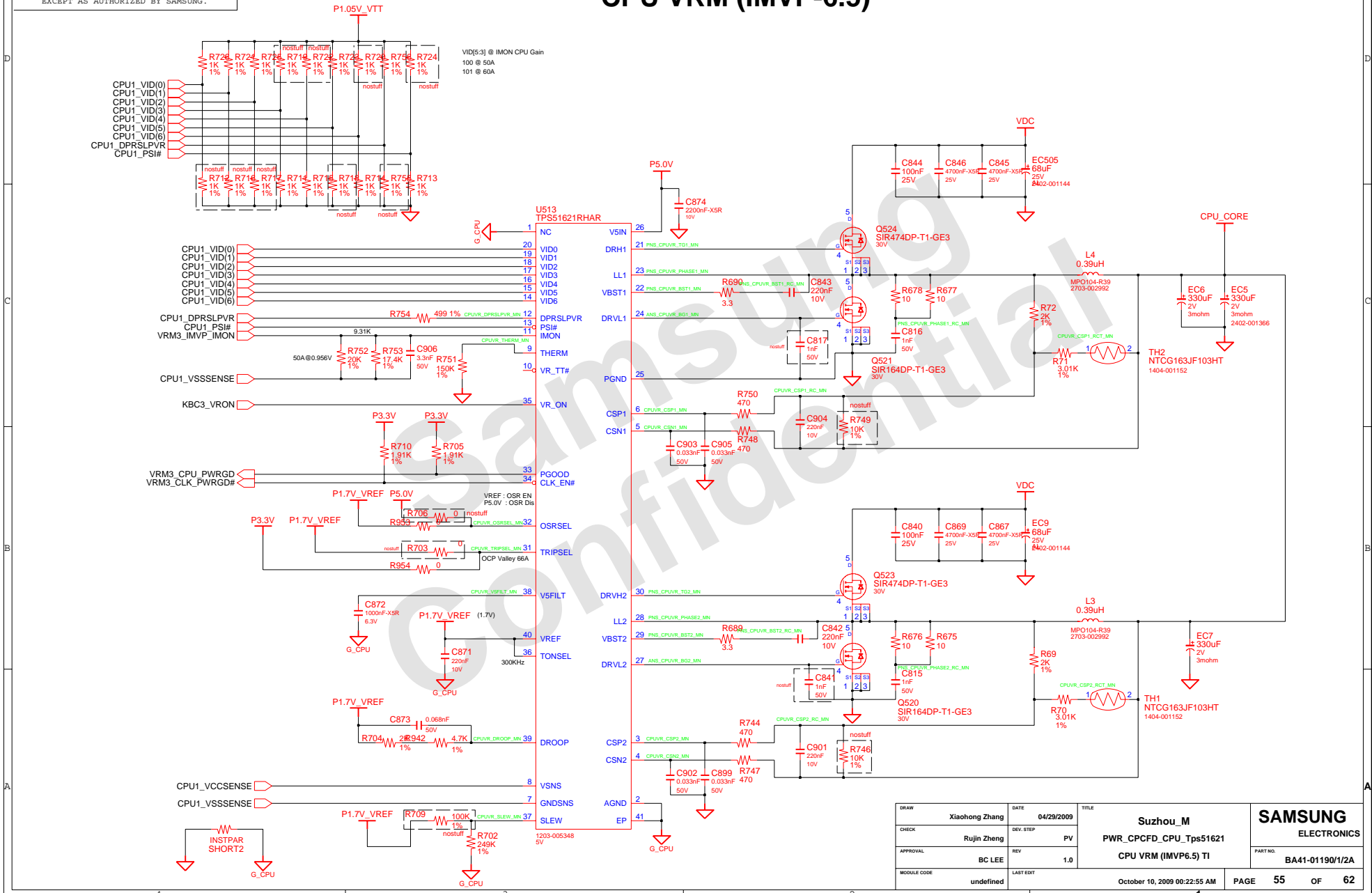


DRAW	Xiaohong Zhang	DATE	03/13/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Memory_Rt8207	PART NO.	
APPROVAL	BC LEE	REV	1.0	DDR3 POWER (P1.5V_AUX)	BA41-01190/1/2A	
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	54	OF 62

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CPU VRM (IMVP-6.5)



DRAW	Xiaohong Zhang	DATE	04/29/2009	TITLE	Suzhou_M
CHECK	Rujin Zheng	DEV. STEP	PV		PWR_CPCFD_CPU_Tps51621
APPROVAL	BC LEE	REV	1.0		CPU VRM (IMVP6.5) T1
MODULE CODE	undefined	LAST EDT	October 10, 2009 00:22:55 AM	PAGE	55 OF 62

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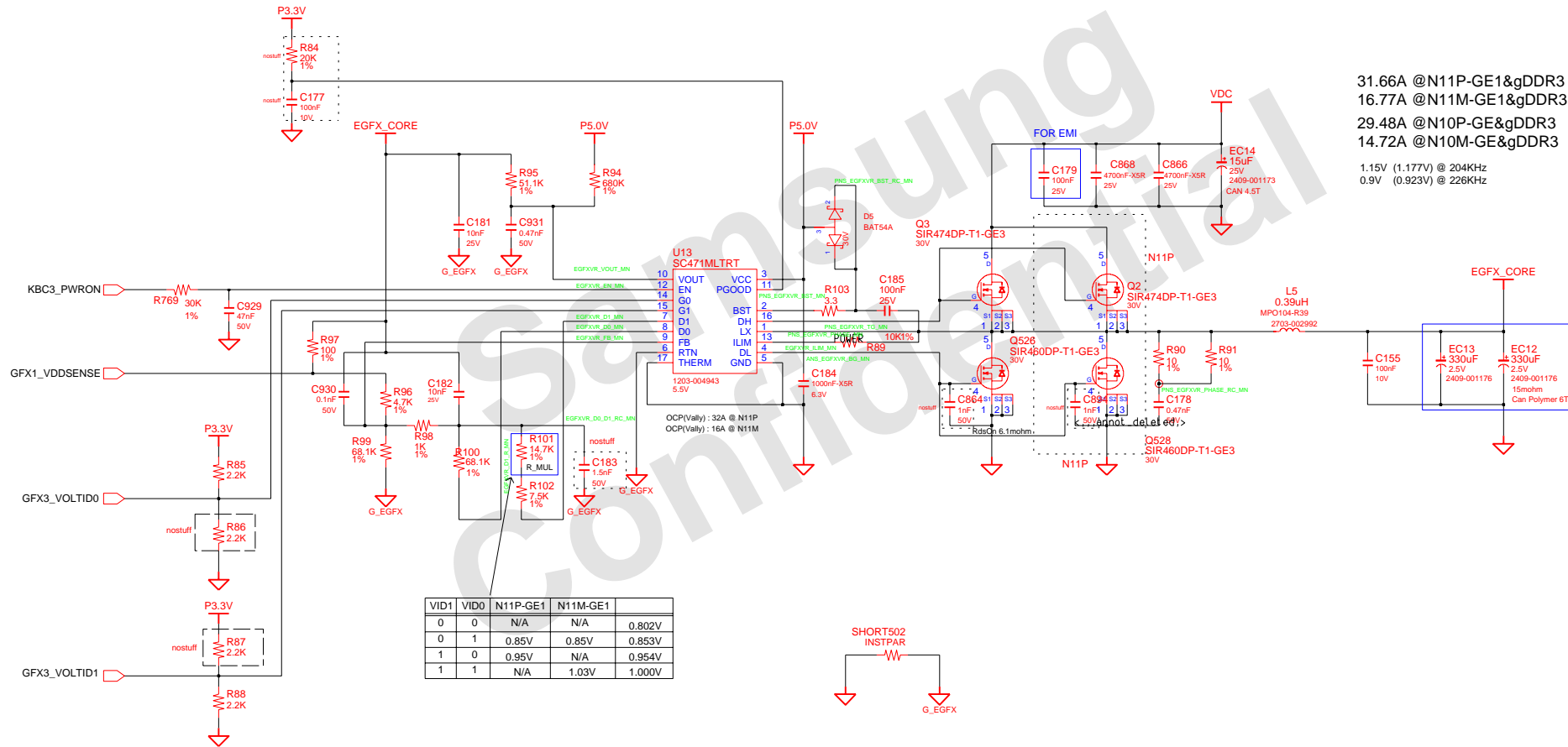
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External Graphic Core Power

N11P-GE1@23.04W N10P-GE@20.97W
 N11M-GE1@14.21W N10M-GE@13.36W

31.66A @N11P-GE1&gDDR3
 16.77A @N11M-GE1&gDDR3
 29.48A @N10P-GE&gDDR3
 14.72A @N10M-GE&gDDR3

1.15V (1.177V) @ 204KHz
 0.9V (0.923V) @ 226KHz

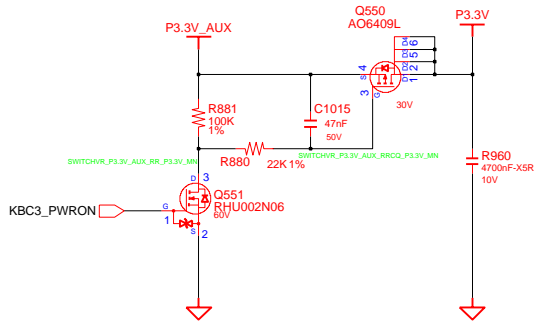


DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_Gfx_MV_Ext		
APPROVAL	BC LEE	REV	1.0	Ext Gfx Memory(TPSS1117)		PART NO. BA41-01190/1/2A
MODULE CODE		LAST EXT		October 10, 2009 00:22:55 AM	PAGE	56 OF 62

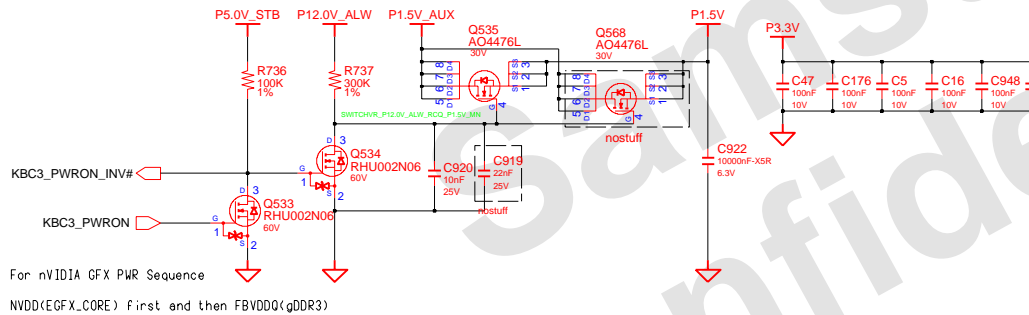
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Switched Power

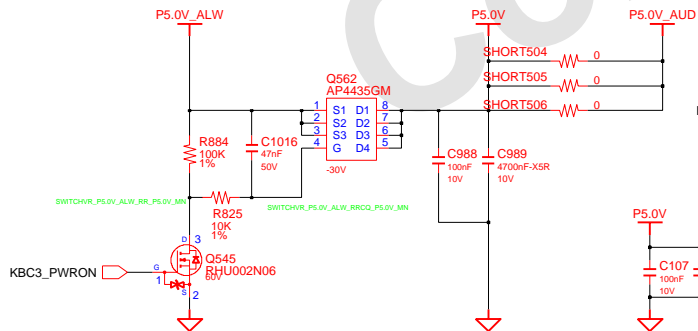
Switched Power On (P3.3V)



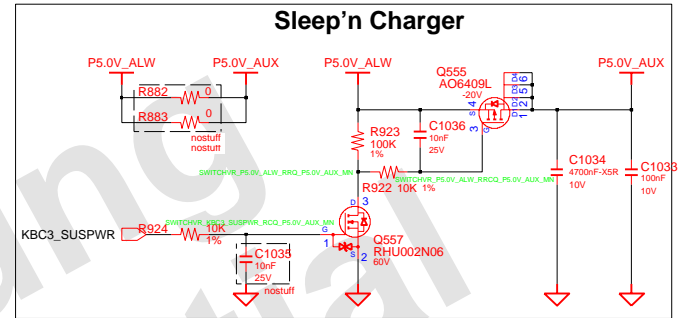
Switched Power On (P1.5V)



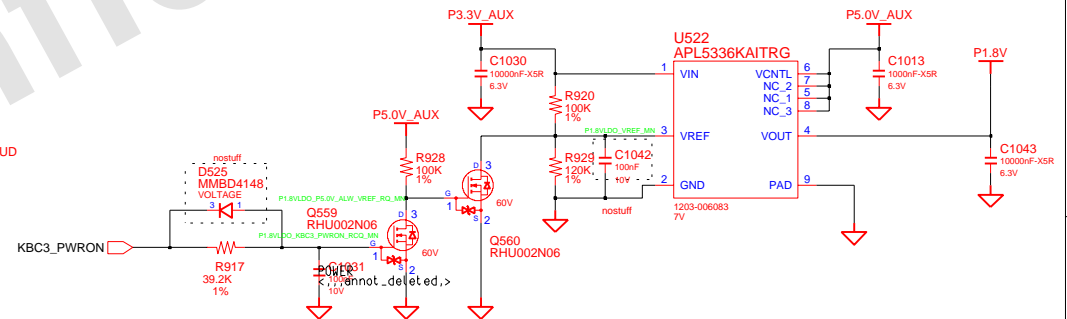
Switched Power On (P5.0V)



Sleep'n Charger



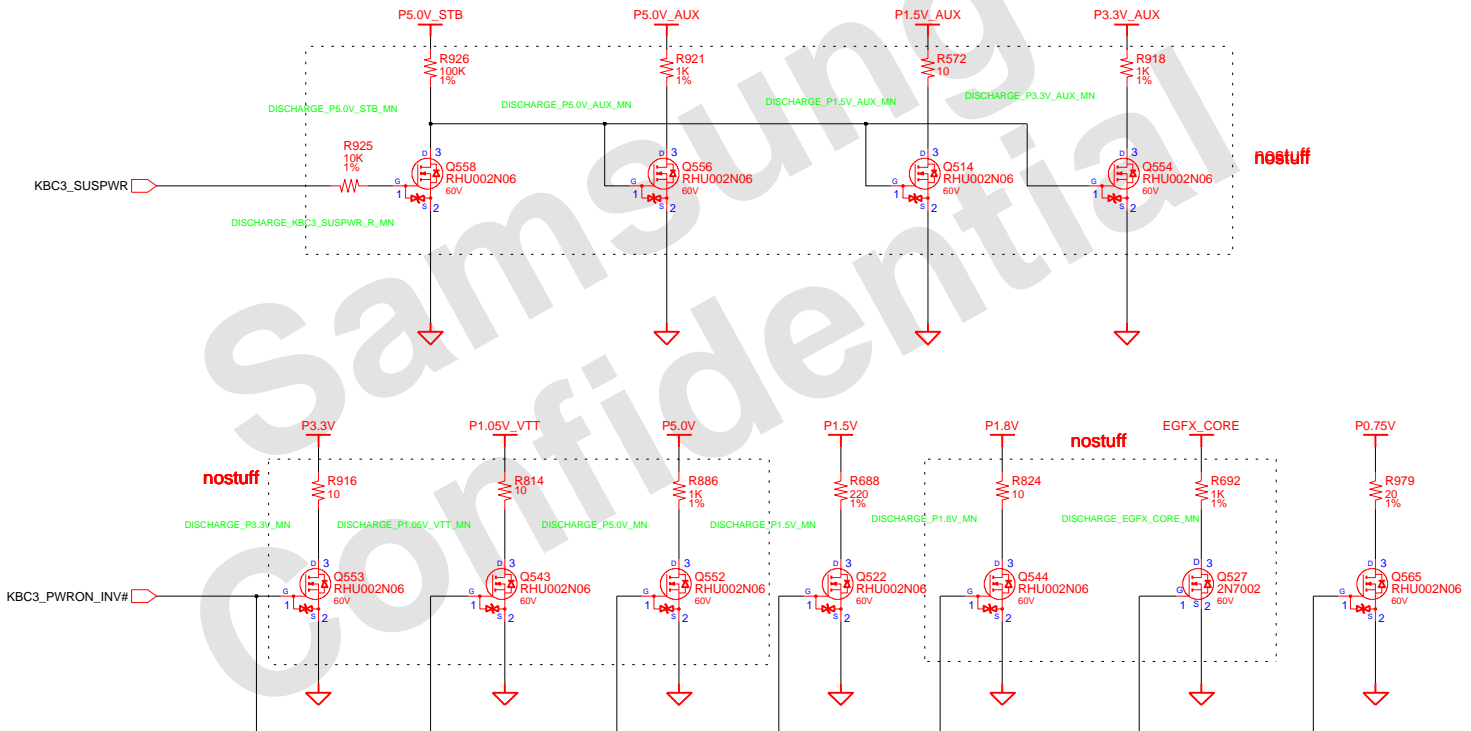
P1.8V(LDO)



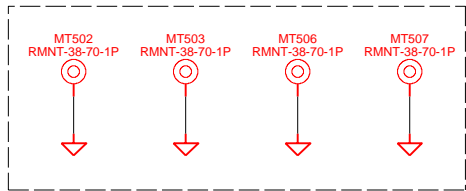
DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_Switched	PART NO.	
APPROVAL	BC LEE	REV	1.0	SWITCHED POWER	BA41-01190/1/2A	
MODULE CODE		LAST EXT				
				October 10, 2009 00:22:55 AM	PAGE	57 OF 62

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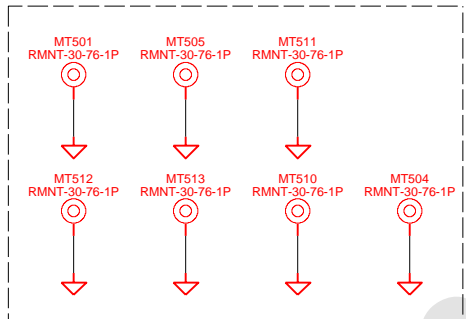
POWER DISCHARGER



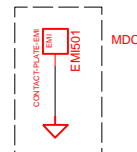
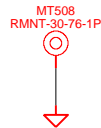
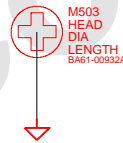
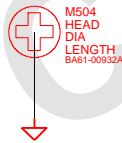
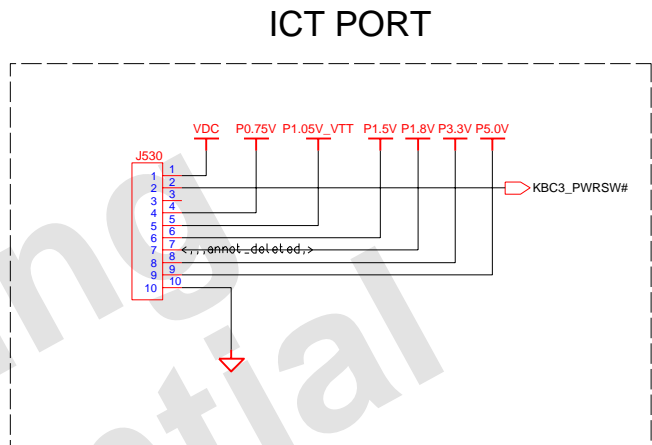
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CPU BRKT MNT



PCB TOP BOTTOM



DRAW	Xiaohong Zhang	DATE	03/11/2009	TITLE	Suzhou_M	SAMSUNG ELECTRONICS
CHECK	Rujin Zheng	DEV. STEP	PV	PWR_MV_DisCharger		
APPROVAL	BC LEE	REV	1.0	DISCHARGING LOGIC		PART NO. BA41-01190/1/2A
MODULE CODE	undefined	LAST EDIT	October 10, 2009 00:22:55 AM	PAGE	59	OF 62

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- AUD3_PD#
- FANS_VDD
- SMB3_CLK
- SPI3_CLK
- SPI3_CS#
- ADT3_SEL#
- AUD3_SPKR
- CHP3_PECI
- CPU1_PSI#

- KBC3_A20G
- KBC3_VRON
- KBC3_TCLK
- LCD3_BRIT
- MCD3_SDWP#
- MCM3_RST#
- PLT3_RST#
- SMB3_DATA
- SPI3_MISO
- SPI3_MOSI

- CLK3_CHP14
- CLK3_MMCA48
- CRT3_GREEN
- CRT3_HSYNC
- CRT3_VSYNC
- KBC3_CHGEN
- KBC3_PWRGD
- KBC3_PWRON
- KBC3_RCIN#
- KBC3_TDATA
- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD
- PEX3_WAKE#
- VTT3_PWRGD

- CHP3_PMSYNC

- CHP3_SERIRQ
- CHP3_SLPS3#
- CHP3_SLPS4#
- CHP3_SLPS5#
- CLK3_DBG_LPC
- CLK3_PCL_FB
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CRT3_DDCCLK
- GFX3_ROM_SI
- GFX3_ROM_SO

- GFX3_STRAP2

- KBC3_BKLTON
- KBC3_PWRSW#
- KBC3_RFOFF#
- KBC3_SMCLK#
- KBC3_SPL_DI
- KBC3_SPL_DO
- KBC3_SUSPWR
- KBC3_USBCHG
- KBC5_KSI(0)
- KBC5_KSI(1)
- KBC5_KSI(2)
- KBC5_KSI(3)
- KBC5_KSI(4)
- KBC5_KSI(5)
- KBC5_KSI(6)
- KBC5_KSI(7)
- KBC5_KSO(0)
- KBC5_KSO(1)

- KBC5_KSO(2)
- KBC5_KSO(3)
- KBC5_KSO(4)
- KBC5_KSO(5)
- KBC5_KSO(6)
- KBC5_KSO(7)
- KBC5_KSO(8)
- KBC5_KSO(9)

- LAN_RSET_MN
- LCD3_BKLTON
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- MCD3_SDDAT0
- MCD3_SDDAT1
- MCD3_SDDAT2
- MCD3_SDDAT3
- PEG3_BKLTEN

- SMB3_ALERT#
- SPI0_WP#_MN
- BATS_DETECT#
- CHP3_BATLOW#

- CHP3_RTORST#
- CHP3_VREF_MN
- CPU_TCK_R_MN
- CRT3_DDCDATA

- EGFXR_EN_MN
- EGFXR_FB_MN
- EXP3_CLKREQ#
- FAN3_FDBACK#
- GFX3_THERMON
- GFX3_THERMDP
- GFX3_VOLTID0
- GFX3_VOLTID1
- HDA3_AUD_SDO
- HDA3_BCLK_MN
- HDA3_MDC_SDO

- KBC3_BATDET#
- KBC3_CHG4.2V
- KBC3_EXTSMI#
- KBC3_PWRBTTN#
- KBC3_RSMRST#
- KBC3_RUNSC#
- KBC3_SMDATA#
- KBC3_SPI_CLK
- KBC3_SPI_CS#

- KBC3_TX_J_MN
- KBC5_KSO(10)
- KBC5_KSO(11)
- KBC5_KSO(12)
- KBC5_KSO(13)
- KBC5_KSO(14)
- KBC5_KSO(15)
- KBC5_USBCHG#
- LAN3_CLKREQ#

- LID3_SWITCH#
- LPC3_LFRAME#
- MEM3_CHB_SA0
- MEM3_CHB_SA1
- MNG3_CLKREQ#
- PCH_GPIO0_MN
- PCI3_CLKRUN#

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- AUD5_CPVEE_MN
- CHP3_SATALED#
- CHP3_SUSSTAT#
- CPU0_COMP0_MN
- CPU0_COMP1_MN
- CPU0_COMP2_MN
- CPU0_COMP3_MN
- CPU1_DPRSLPVR
- CPU1_VCCSENSE
- CPU1_VSSSENSE
- CPUVR_CS#1_MN
- CPUVR_CS#2_MN
- CPUVR_CS#1_MN
- CPUVR_CS#2_MN
- DDR3V_TON_MN
- GFX1_VDDSENSE
- GFX3_ROM_SCLK
- HDA3_AUD_SDIO
- HDA3_MDC_BCLK
- HDA3_MDC_RST#
- HDA3_MDC_SD1
- HDA3_MDC_SYNC
- KBC3_CAPSLED#
- KBC3_SPKMUTE#
- KBC3_WAKESCIF#
- KBC5_LED_CTRL
- LDC3_EDID_CLK
- MCP1_DRAMRST#
- PCI3_IRDY#_MN
- PCI3_PERR#_MN
- PCI3_REO1#_MN
- PCI3_REO2#_MN
- PEG0_ZQ_R1_MN
- PEG0_ZQ_R2_MN
- PEG0_ZQ_R3_MN
- PEG0_ZQ_R4_MN
- PEG0_ZQ_R5_MN
- PEG0_ZQ_R7_MN
- VGA5_HDMI_HPD
- AUD5_SENS_MIC#
- CHP3_CPU_PWRGD
- CHP3_GPIO39_MN
- CHP3_INTRUDER#
- CLK3_PCLMKCOM
- CLOCK_P1_5V_MN
- CLOCK_P3_3V_MN
- CPU1_THRMTRIP#
- PEG3_HDMI_CLK
- PEG3_HP0_HDMI
- PEG3_LCDVDD0N
- PEG3_SPDIF_MN
- PEG3_VDD33_MN
- PEG5_HDMI_CLK
- PLT3_RST_ORG#
- SPI3_HOLD#_MN
- TP_LED3_R1_MN
- TP_LED3_R2_MN
- TP_LED3_R3_MN
- TP_LED3_R4_MN
- TP_LED3_R5_MN
- TP_LED3_R6_MN
- TP_LED3_R7_MN
- TP_LED3_R8_MN
- TP_LED3_R9_MN
- CPUVR_DR0OP_MN
- CPUVR_THERM1_MN
- CPU_CFG_7_R_MN
- DDR3V_TRIP_MN
- EGFXVR_D1_R_MN
- EGFXVR_ILIM_MN
- EGFXVR_VOUT_MN
- KBC3_LED_ACIN#
- KBC3_USBPWRON#
- KBC3_WLON_LED#
- LDC3_EDID_DATA
- PCI3_FRAME#_MN
- PCI3_PIRQA#_MN
- PCI3_PIRQB#_MN
- PCI3_PIROC#_MN
- PCI3_PIROD#_MN
- PEG1_PLLVDD_MN
- PEG3_HDMI_DATA
- PEG5_HDMI_DATA
- THM3_STP#_Q_MN
- THM3_STP#_R_MN
- TPD5_L_BUTTON#
- TPD5_R_BUTTON#
- TP_LED3_R10_MN
- TP_LED3_R11_MN
- TP_LED3_R12_MN
- TP_LED3_R13_MN
- TP_LED3_R14_MN
- TP_LED3_R15_MN
- TP_LED3_R16_MN
- TP_LED3_R17_MN
- TP_LED3_R18_MN
- VRM3_CPU_PWRGD
- VRM3_IMVP_IMON
- ANS_CHGVR_BG_MN
- AUD5_JDREF_R_MN
- CHP1_DRAM_PWRGD
- CHP3_ME_RTCSRST#
- CHP3_SUSPWR_ACK
- CHP3_WPW#_0_R_MN
- CPUVR_VSFILT_MN
- DDR3V_PGOOD_MN
- KBC3_LED_POWER#
- KBC3_PWRGD_R_MN
- KBC3_PWRON_INV#
- MDC48_TIP_B1_MN
- MDC48_TIP_B2_MN
- MEM3_CHA_SA0_MN
- MEM3_CHA_SA1_MN
- PEG1_FBA_DEBUG_MN
- PEG1_FBC_DEBUG_MN
- PEG1_IFPEF_PLLVDD
- PEG1_PB_LLAVDD_MN
- PEG1_SP_PLLVDD_MN
- THM3_DN2_DN3_MN
- THM3_DP2_DN3_MN
- VRM3_CLK_PWRGD#
- VTT3_PWRGD_R_MN
- ANS_CPUVR_BG1_MN
- ANS_CPUVR_BG2_MN
- ANS_DDR3V_BG_MN
- ANS_EGFXVR_BG_MN
- CHP3_VREF_SUS_MN
- CLOCK_CPU_SEL_MN
- CLOCK_XTAL_IN_MN
- CPUVR_CSP1_RC_MN
- CPUVR_CSP2_RC_MN
- CPUVR_TRIPSEL_MN
- DDR3V_EN_PSV_MN
- HDD3_LED#_LED_MN
- KBC3_LED_CHARGE#
- KBC3_THERM_SMCLK
- MDC48_RING_B1_MN
- MDC48_RING_B2_MN
- PEG0_BUFIRST_N_MN
- PEG3_TESTMODE_MN
- PEG3_XTAL_OUT_MN
- PLT1_RST#_MCP_MN
- PNS_CPUVR_TG1_MN
- PNS_CPUVR_TG2_MN
- PNS_DDR3V_TG_MN
- PNS_EGFXVR_TG_MN
- SYSVR_ENTRIP1_MN
- SYSVR_ENTRIP2_MN
- SYSVR_SKIPSEL_MN
- THM3_SHDN_SEL_MN
- THM3_TRIP_SET_MN
- AUD5_HP_LEFT_B_MN
- CLK3_MM48_PCH_MN
- CLOCK_CPU_STOP#_MN
- CLOCK_XTAL_OUT_MN
- LAN3_CLKREQ#_R_MN
- MCH1_SM_RCOMP0_MN
- MCH1_SM_RCOMP1_MN
- MCH1_SM_RCOMP2_MN
- MCP3_PEG_RBIAS_MN
- PEG1_FBA_DEBUG_MN
- PEG1_FBC_DEBUG_MN
- PEG1_IFPEF_PLLVDD
- PEG1_PB_LLAVDD_MN
- PEG1_SP_PLLVDD_MN
- PNS_CPUVR_BST1_MN
- PNS_DDR3V_BST_MN
- PNS_EGFXVR_BST_MN
- PRTC_BAT_CON_R_MN
- SYS3_LED_POWER_MN
- 80H_CHP3_SERIRQ_MN
- AUD5_HP_RIGHT_B_MN
- AUD5_MIC2_INT_B_MN
- CHGVR_SGATE_RRQ_MN
- CHP1_DRAM_PWRGF_MN
- CHP3_PEG_HOLD_RST#
- CHP3_XTAL_IN_25_MN
- CHSETVR_VTT_TON_MN
- CHSETVR_VTT_VCC_MN
- CHSETVR_VTT_VFB_MN
- CLK3_DBFLPC_PCH_MN
- CLK3_PCI_FB_PCH_MN
- EGFXVR_D0_D1_RC_MN
- HDA3_MDC_SDH1_R_MN
- KBC5_LED_CTRL_R_MN
- LAN3_DISABLE#_R_MN
- P1_5V_VREFCA_R1_MN
- P1_5V_VREFCA_R2_MN
- P1_5V_VREFCA_R3_MN
- P1_5V_VREFCA_R4_MN
- P1_5V_VREFCA_R5_MN
- P1_5V_VREFCA_R6_MN
- P1_5V_VREFCA_R7_MN
- P1_5V_VREFCA_R8_MN
- P1_5V_VREFCA_R9_MN
- P1_5V_VREFCA_R10_MN
- P1_5V_VREFDQ_R1_MN
- P1_5V_VREFDQ_R2_MN
- P1_5V_VREFDQ_R3_MN
- P1_5V_VREFDQ_R4_MN
- P1_5V_VREFDQ_R5_MN
- P1_5V_VREFDQ_R6_MN
- P1_5V_VREFDQ_R8_MN
- PEG5_HDMI_CLK_B_MN
- PEG_IFPC_PLLVDD_MN
- VGA5_HDMI_HPD_R_MN
- AUD5_MIC1_LEFT_C_MN
- AUD5_MIC1_LEFT_R_MN
- CHP3_XTAL_OUT_25_MN
- CHSETVR_VTT_TRIP_MN
- KBC5_LED_CTRL_OC_MN
- KBC5_LED_CTRL_OR_MN
- PEG1_IFPAB_IOVDD_MN
- PEG1_IFPEF_IOVDD_MN
- PEG3_ITAG_TRST_N_MN

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- PNS_CPLVVR_PHASE1_MN
- PNS_CPLVVR_PHASE2_MN
- PNS_DDR3VR_PHASE_MN
- PNS_EGFXVR_PHASE_MN
- VRM3_CLK_PWRGDI_INV

- CHP1_SATAICOMPPIO_MN

- DDR3VR_VREF_P0_7V_MN
- KBC3_CAPSLED0_LED_MN
- MCP3_FDI_SIDE BAND_MN

- PEG3_PEX_SVDD_SVS_MN
- PEG3_TX_HDMI_PD_Q_MN
- PEG3_XTAL_OUTBUFF_MN
- PNS_CPLVVR_BST1_RC_MN

- PNS_DDR3VR_BST_RC_MN
- PNS_EGFXVR_BST_RC_MN
- ANS_CHSETVR_VTT_BG_MN
- CHSETVR_VTT_EN_PSV_MN

- CPU1_THRMTRIP#_PCH_MN

- KBC3_WLON_LED#_LED_MN
- MCP3_PEG_IR_COMPIO_MN
- PCH_DMI_P1_05V_VTT_MN

- PEG3_LCD3_EDID_CLK_MN

- PEX1_EXPCRD_TXN3_C_MN
- PEX1_EXPCRD_TXP3_C_MN
- PNS_CHSETVR_VTT_TG_MN
- P5_0V_AUX_USBPWR_P2_MN

- PEG3_LCD3_EDID_DATA_MN
- PNS_CHSETVR_VTT_BST_MN
- PNS_CPLVVR_PHASE1_RC_MN
- PNS_CPLVVR_PHASE2_RC_MN
- PNS_DDR3VR_PHASE_RC_MN
- CLK3_MICOM_32K_XTAL1_MN
- CLK3_MICOM_32K_XTAL2_MN

- SYSVR_VFB1_P5_0V_ALW_MN
- SYSVR_VFB2_P3_3V_AUX_MN

- PNS_CHSETVR_VTT_PHASE_MN
- SYSVR_KBC3_USBCHG_RDQ_MN

- ANS_SYSVR_BG_P3_3V_AUX_MN
- ANS_SYSVR_BG_P5_0V_ALW_MN

- PNS_CHSETVR_VTT_BST_RC_MN
- PNS_SYSVR_TG_P3_3V_AUX_MN
- PNS_SYSVR_TG_P5_0V_ALW_MN
- SYSVR_KBC3_ALWS_ON_RCQ_MN
- P1_8V_LDO_KBC3_PWRON_RCQ_MN
- PNS_SYSVR_BST_P3_3V_AUX_MN
- PNS_SYSVR_BST_P5_0V_ALW_MN

- DDR3VR_P5_0V_ALW_VREF_RQ_MN
- PNS_CHSETVR_VTT_PHASE_RC_MN

- PNS_SYSVR_PHASE_P3_3V_AUX_MN
- PNS_SYSVR_PHASE_P5_0V_ALW_MN
- P1_8V_LDO_P5_0V_ALW_VREF_RQ_MN
- PNS_SYSVR_BST_P3_3V_AUX_RC_MN
- PNS_SYSVR_BST_P5_0V_ALW_RC_MN
- SYSVR_P5_0V_STB_ENTRIP1_RQ_MN
- SYSVR_P5_0V_STB_ENTRIP2_RQ_MN
- SWTCHVR_P5_0V_ALW_RR_P5_0V_MN
- DDR3VR_KBC3_PWRON_P0_75V_RCQ_MN
- PNS_SYSVR_PHASE_P3_3V_AUX_RC_MN
- PNS_SYSVR_PHASE_P5_0V_ALW_RC_MN
- SWTCHVR_P3_3V_AUX_RRQ_P3_3V_MN
- SWTCHVR_P5_0V_ALW_RRQ_P5_0V_AUX_MN

- SWTCHVR_KBC3_SUSPWR_RCQ_P5_0V_AUX_MN

- BGATE
- CPU_CORE
- CPU_CORE
- CPU_CORE
- EGFX_CORE
- EGFX_CORE
- EGFX_CORE
- G_AUD
- G_AUD
- G_CHG
- G_CHG
- G_CPU

- G_DDR
- G_DDR
- G_EGFX
- G_EGFX
- G_P3_3V
- G_P3_3V
- G_P1_05V_VTT
- G_P1_05V_VTT
- LCD_VDD3V
- LCD_VDD3V
- MDC_GND
- MDC_GND
- P1_5V
- P1_5V
- P1_5V
- P1_8V
- P1_8V
- P1_8V
- P3_3V
- P3_3V
- P3_3V
- P3_3V
- P5_0V
- P5_0V
- P5_0V
- P0_75V
- P0_75V
- P1_0V_LAN
- P1_0V_LAN
- P1_5V_AUX
- P1_5V_AUX

- P1_8V_LAN
- P2_0V_REF

- P5_0V_ALW
- P5_0V_ALW
- P5_0V_AUD
- P5_0V_AUD
- P5_0V_AUX
- P5_0V_AUX
- P5_0V_STB
- P5_0V_STB
- P1_05V_VTT
- P1_05V_VTT
- P1_05V_VTT
- P1_05V_VTT

- P12_0V_ALW
- P12_0V_ALW
- P4_75V_AUD

- P2_39V_VREF

- P3_3V_MICOM
- P3_3V_MICOM
- SUB_GND
- SUB_GND
- SUB_P3_3V
- SUB_P3_3V
- SUB_P5_0V_AUX
- SUB_P5_0V_AUX
- VDC
- VDC
- VDC
- VDC
- VCC_CRT
- VCC_CRT
- VCC_LED
- VCC_LED
- VDC_ADPT
- VDC_ADPT

