QingDao_ULCPC

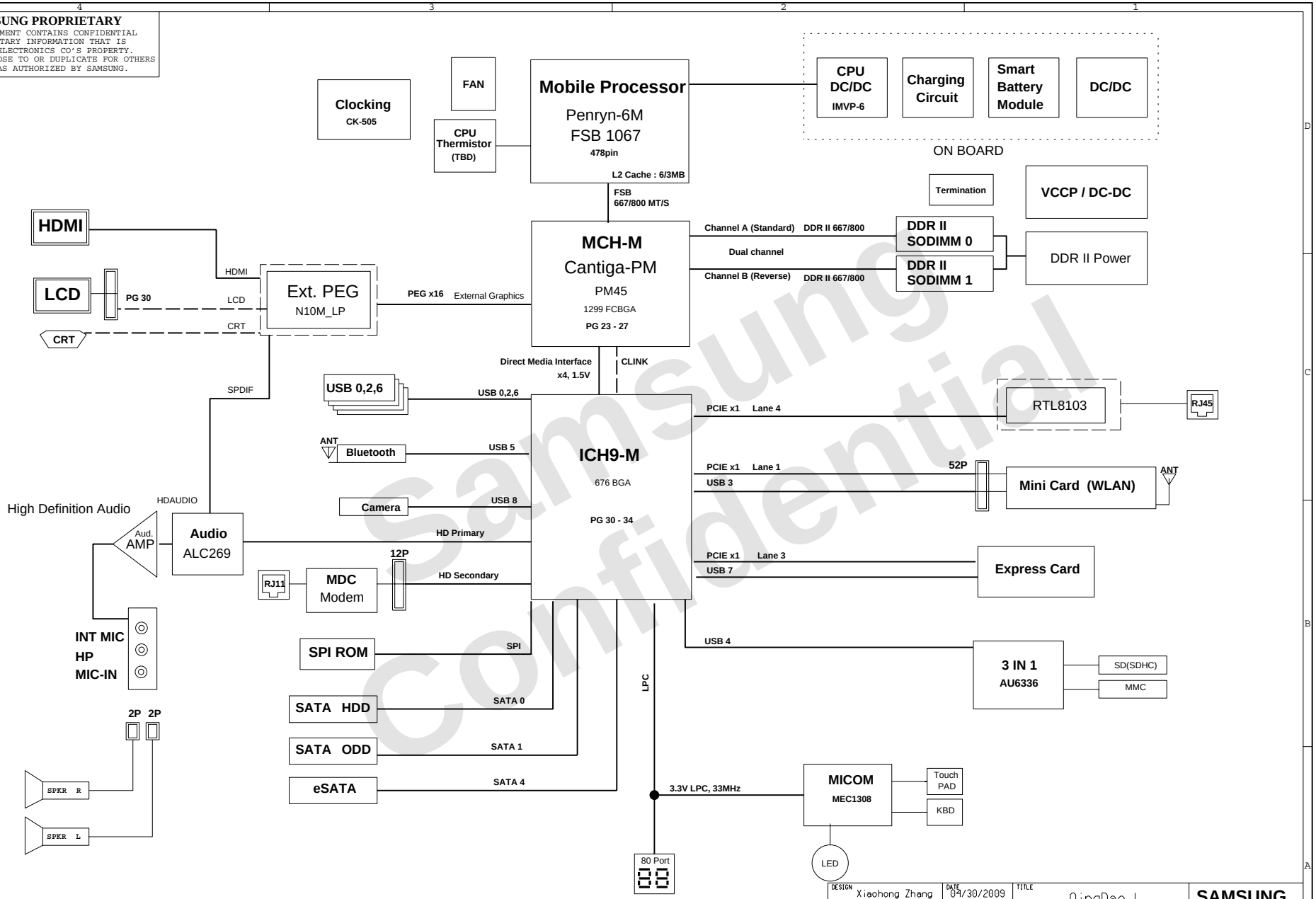
CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : QingDao_ULCPC
PBA Name : MAIN
PCB Code : BA41-01100A NANYA
BA41-01097A HANNST
BA41-01098A GCE
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.04.30

Design	CHECK	APPROVAL
XIAOHONG ZHANG	RUJIN ZHENG	BC LEE

■ ***Owner : SESC Mobile R & D*** ***Signature :*** ***X***

BLOCK DESIGN



DESIGN Xiaohong Zhang	DATE 09/30/2009	TITLE QingDao_L MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK Rujin Zheng	DEV. STEP PV		
APPROVAL BC LEE	REV 1.0		PART NO. BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT April 29, 2009 21:47:17 PM	PAGE 2 OF 15	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.05V	VTT for CPU, Cantiga & ICH9-M
P1.1	VTT for N10M_GE1
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	Mini PCI Express
2	SYSTEM PORT 1
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	EXPRESS CARD
8	Camera
9	NC
10	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	NC
3	EXPRESS CARD
4	LOM
5	NC
6	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)

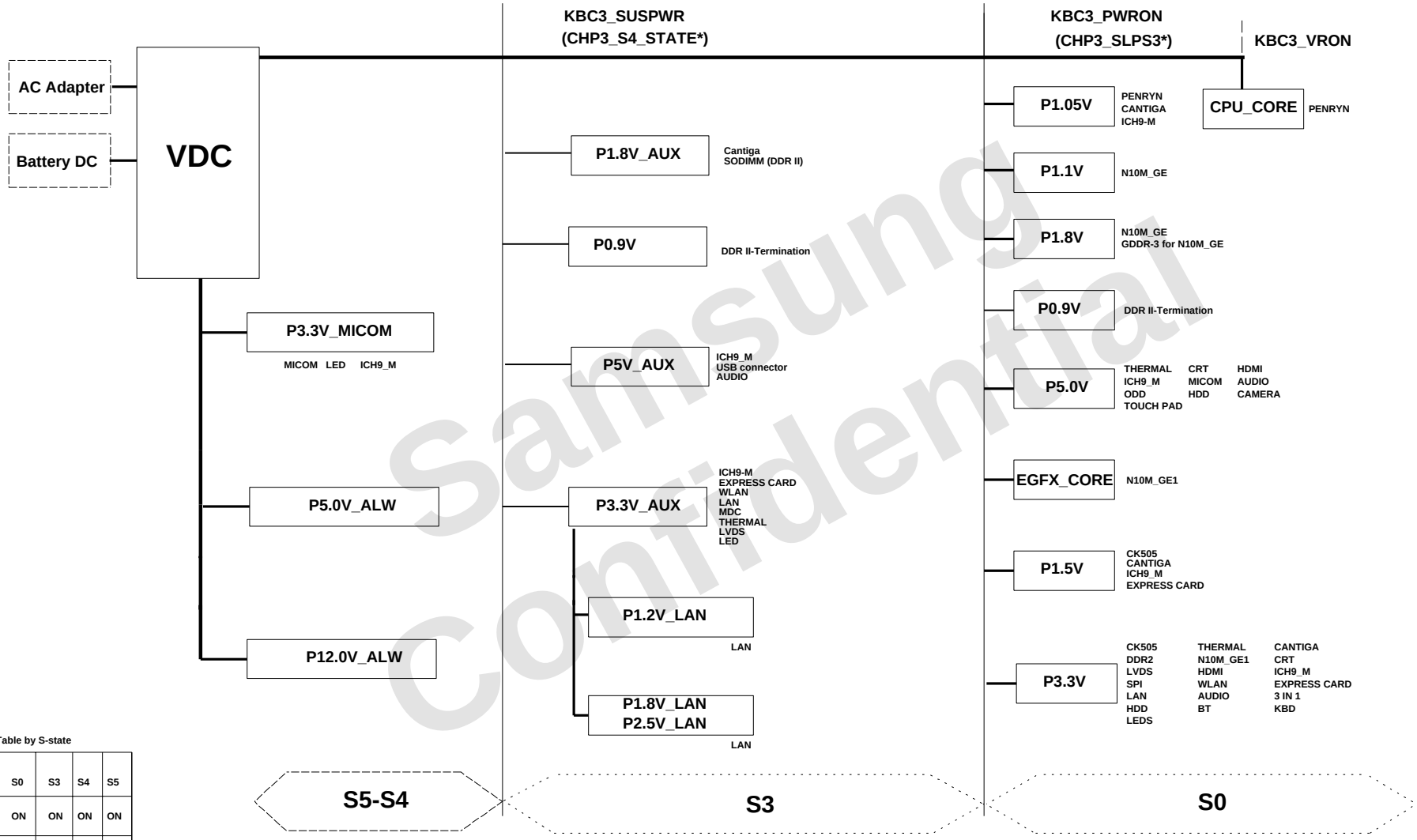
REVISION HISTORY

See rev notes for more information.

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 3 OF 15

POWER DIAGRAM

Rev 0.1



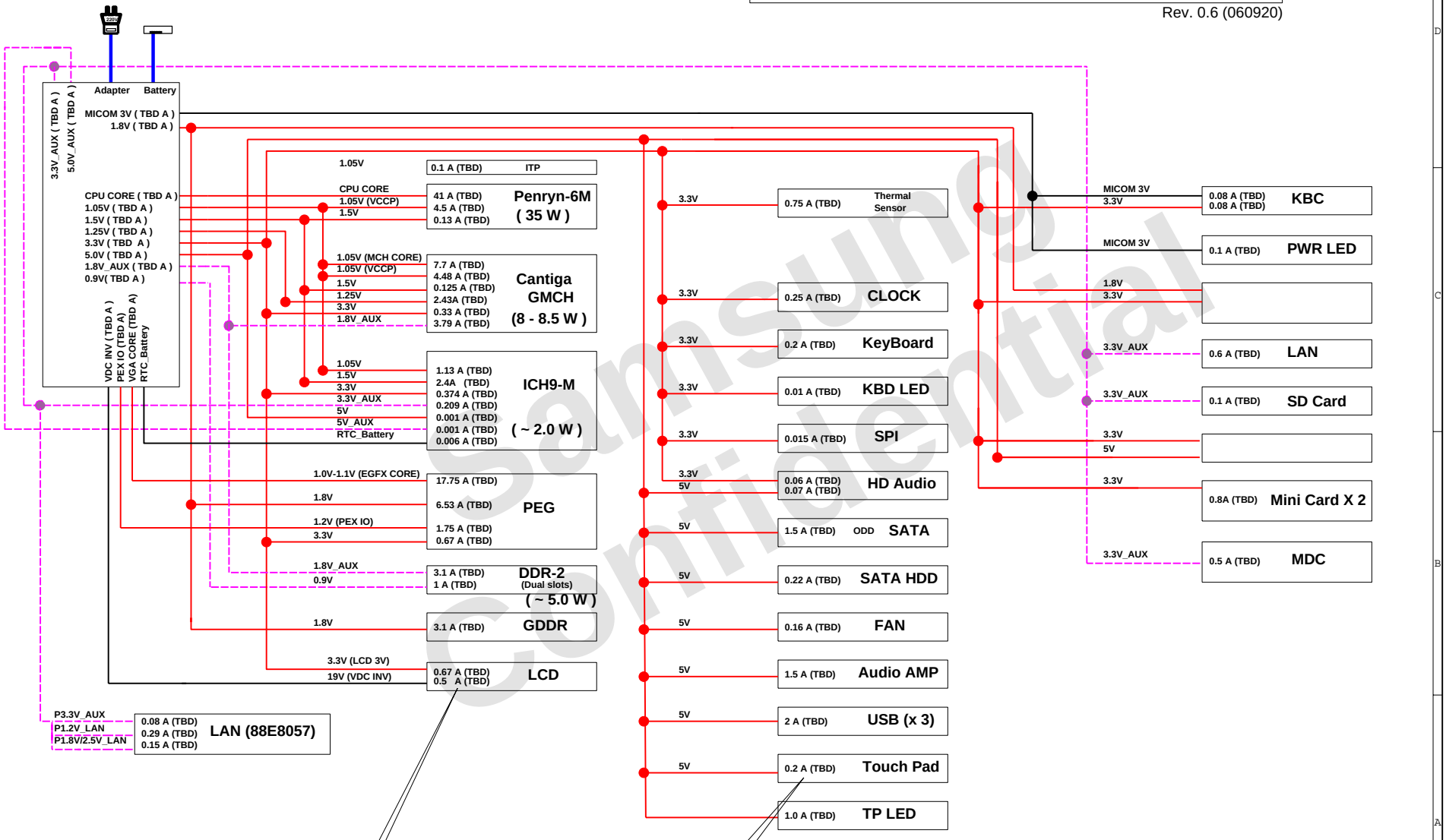
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L / MAIN / POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 4 OF 15	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L / MAIN / POWER RAILS	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 5 OF 15	

POWER SEQUENCE

Rev. 0.7

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

RTC Battery — PRTC_BAT — 1
CHP3_RTCRST#
CHP3_ME_RTCRST#

6) P3.3V_AUX

PRTC PRTC — 16

POWER S/W — 8

10-1) P1.05V
8) CHP3_SLPS5#/4#/3#

4) KBC3_PWRSW# — 4

KBC — 7
7) KBC3_RSMRST#
17) KBC3_PWRGD
15)VRM3_CPU_PWRGD
110ms Delay — 17
5) KBC3_SUSPWR — 5
9) KBC3_PWRON — 9
13) KBC3_VRON — 13

ICH9-M
LAN100_SLP
INTVRMEN
7) P1.05V_AUX
7) P1.5V_AUX
VRMPWRGD
PWROK
CL_PWROK
16) CLK3_PWRGD
15)VRM3_CPU_PWRGD
17) KBC3_PWRGD
18) CPU1_PWRGDCPU
19) PLT3_RST* — 19

CK-505 — 16-1) Clock Running

15) VRM3_CPU_PWRGD — 15

11) VCCP3_PWRGD (GM-model)
12)GCORE3_PWRGD (PM-model)
13) KBC3_VRON (Back-up)
CPU VRM

(Test Option) — 18
CPU — 20
14) CPU_CORE — 14
10-1) P1.5V
10-1) P1.05V
20) CPU1_CPURST*

3) P3.3V_MICOM — 3

AC_DC / Battery
MAX17006ETP+T

8) KBC3_SUSPWR
9) KBC3_PWRON

10) P5.0V
2) VDC
5) KBC3_SUSPWR
DDR2 POWER
RT8207GQW\
6) P1.8V_AUX
6) MEM1_VREF
10-2) 0.9V — 6

17) KBC3_PWRGD
17) KBC3_PWRGD
PWROK
CL_PWROK
GMCH
19) PLT3_RST*
6) P1.8V_AUX
10-1) P3.3V

10) P1.05V
PM-model only

SC486IMLTRT
Sheet 53
10) P1.5V — 10

2) VDC — 2
2-1) P12.0V_ALW

9-1 — 9-1
9-1) KBC3_PWRON_INV#

2) VDC
MAX17020ETJ+
10) P1.05V
9) KBC3_PWRON
11) VCCP3_PWRGD — 11

MAX8792ETD+T
11-1) EGFX_CORE
12)GCORE_PWRGD — 12

3) P5.0V_ALW — 3
P3.3V_AUX & P5V_AUX
MAX17020ETJ+
6) P5.0V_AUX
9-1

P3.3V_MICOM — 6
6) P3.3V_AUX

10-1) P3.3V
10) P1.5V
10) P1.05V
ICH9_M PCIe Devices — 19

10-1) P1.1V
11-1) EGFX_CORE
10-1) P3.3V
PEG

6) P3.3V_AUX
9-1) KBC3_PWRON
AP6680AGM
10-1) P3.3V

6) P1.8V_AUX
AP6680AGM
10-1) P1.8V

10-1) P5.0V
AP4435GM
10-1) P5.0V

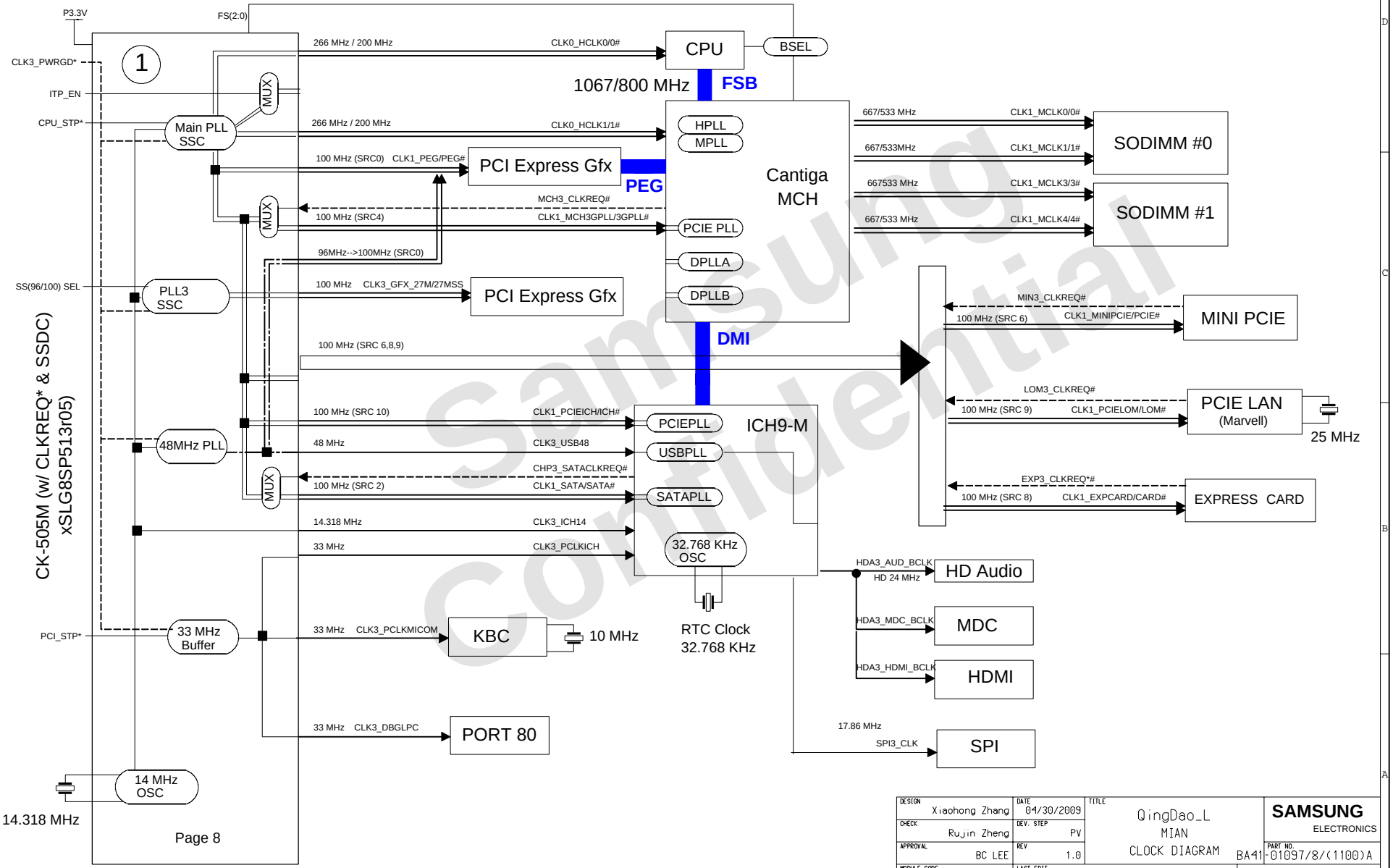
ISL8014IRZ-T
10) P1.1V

6) P1.8V_AUX
10-2) P0.9V
DDR2 Memory

LOM Marvell
6-1) P1.2V_LAN
6-1) P1.8VLAN
BCP69

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 6 OF 15

CLOCK DISTRIBUTION Rev. 0.1



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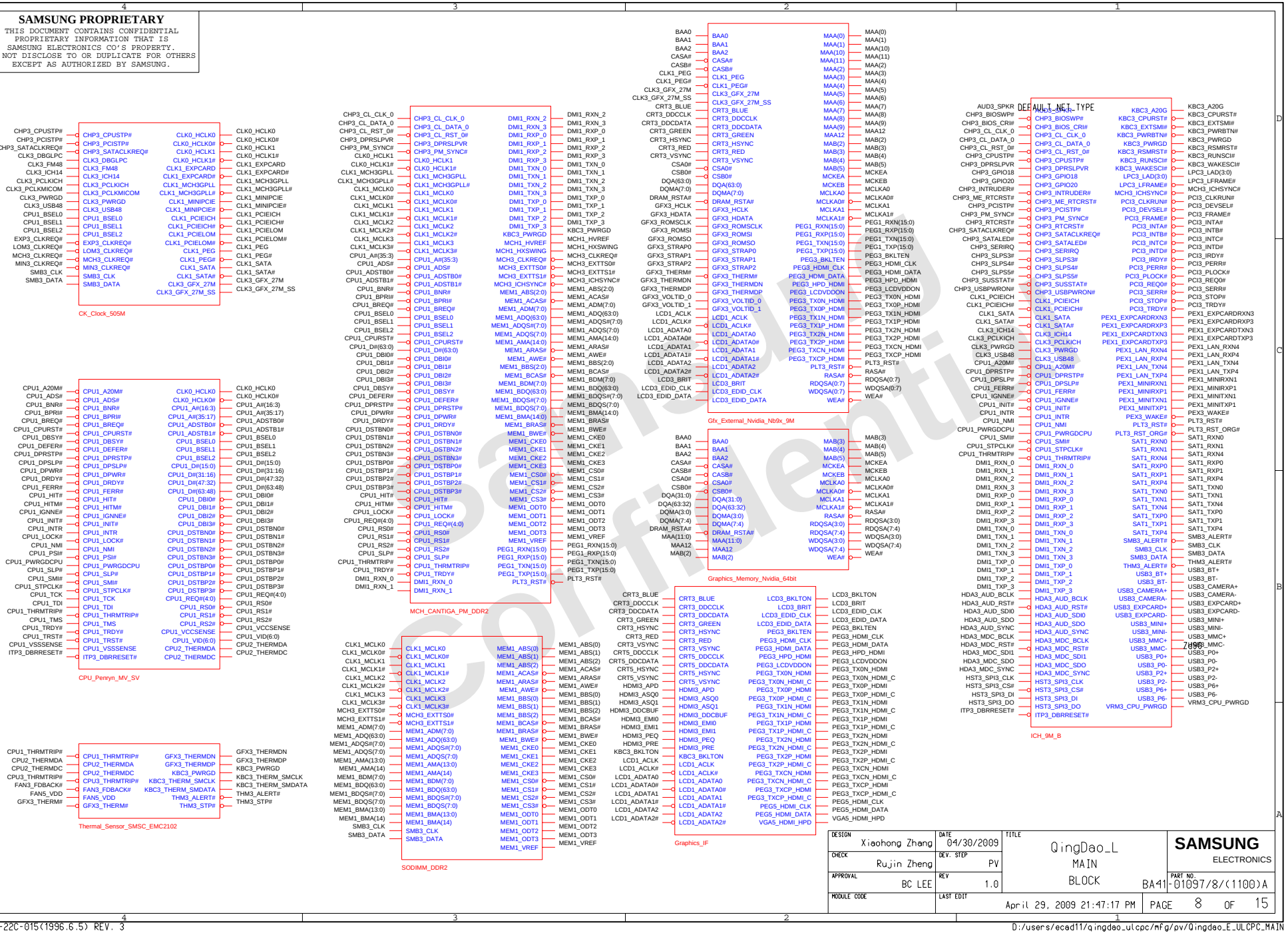
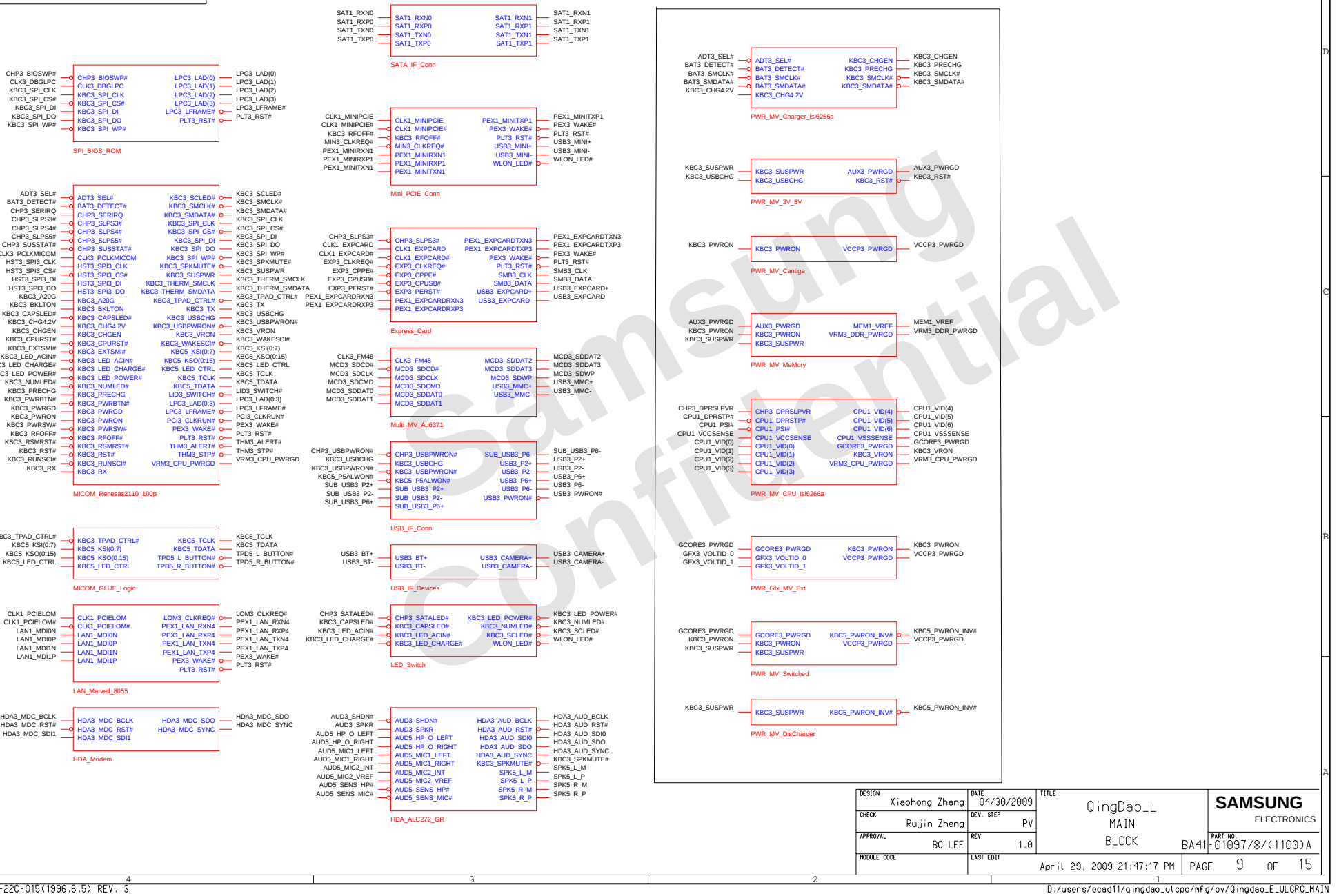
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MIAN CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 7 OF 15	



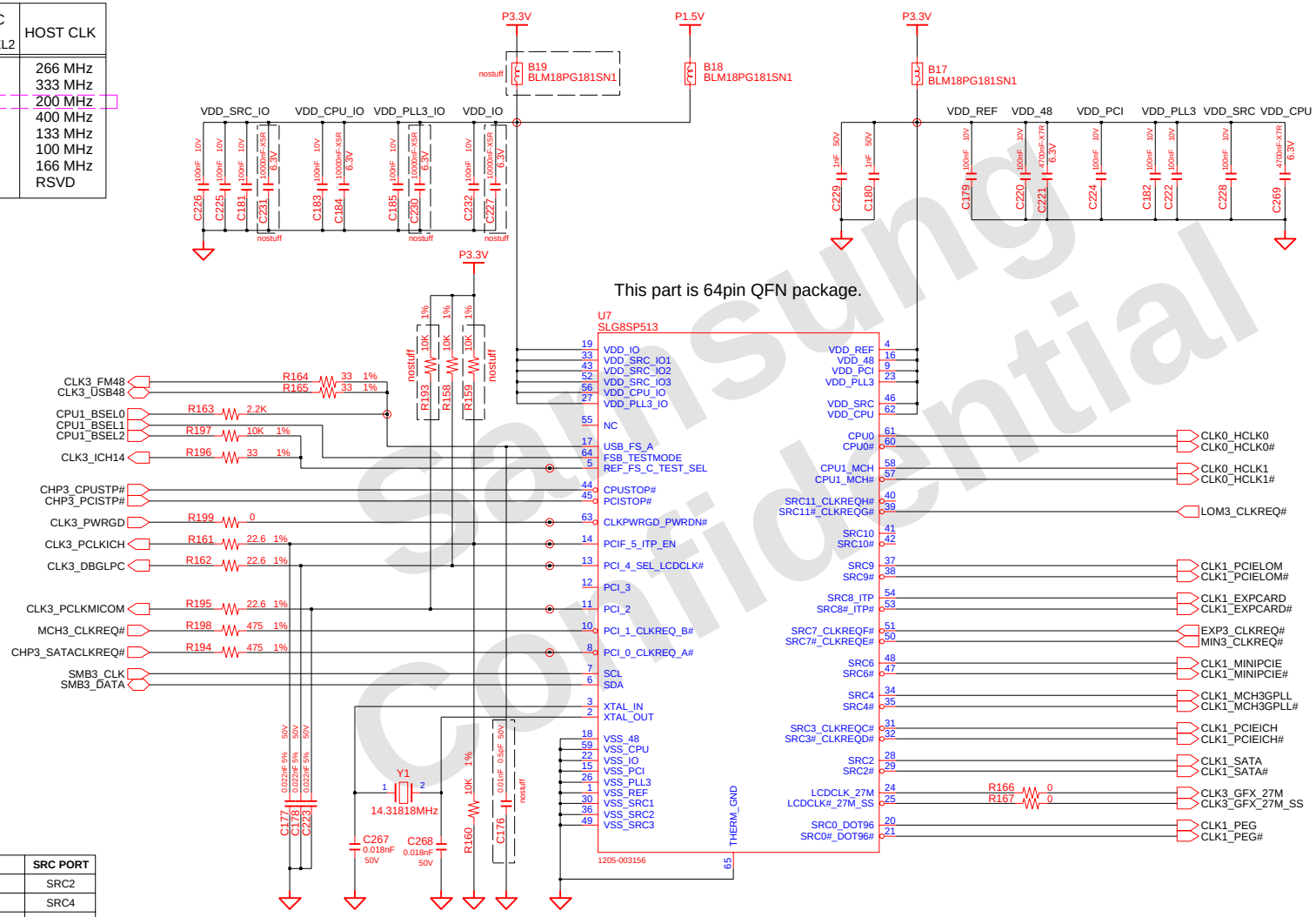
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN BLOCK	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 8 OF 15	



DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN BLOCK	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 9 OF 15	

CK505M

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

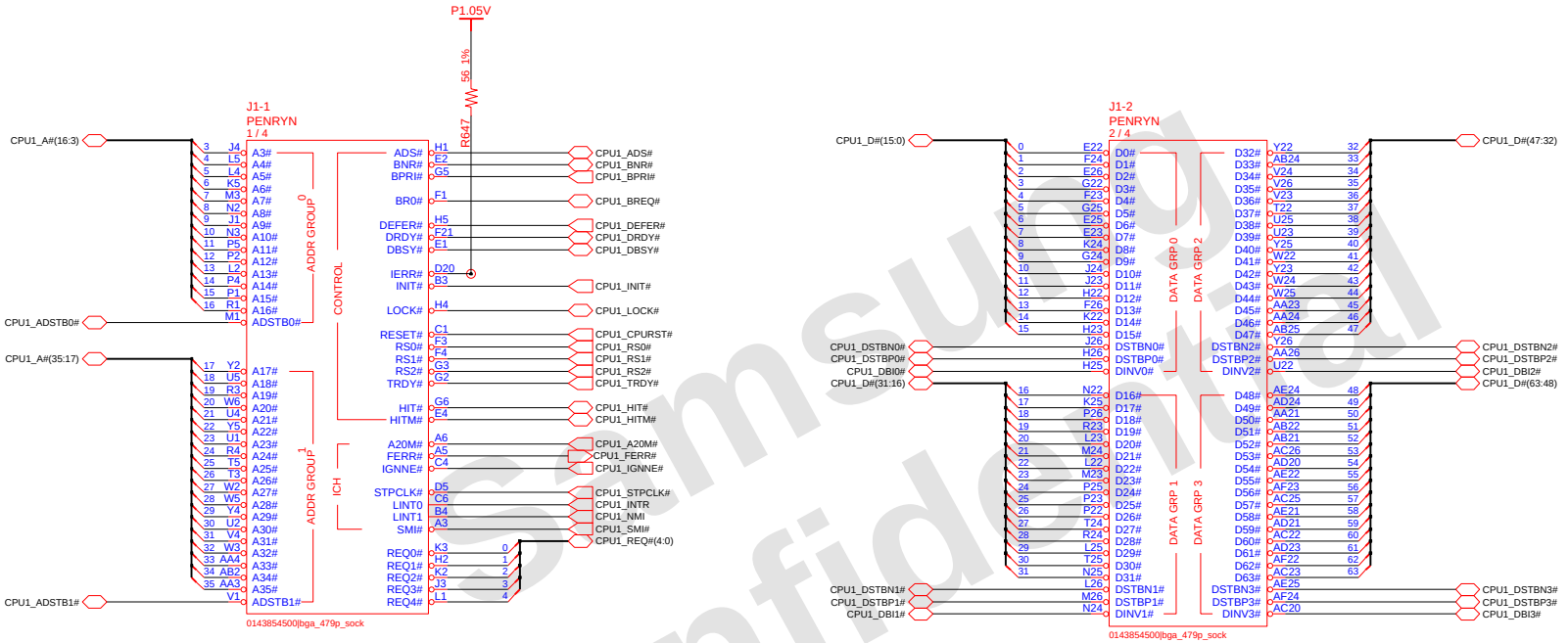


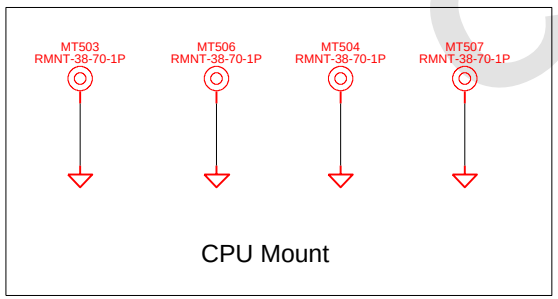
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

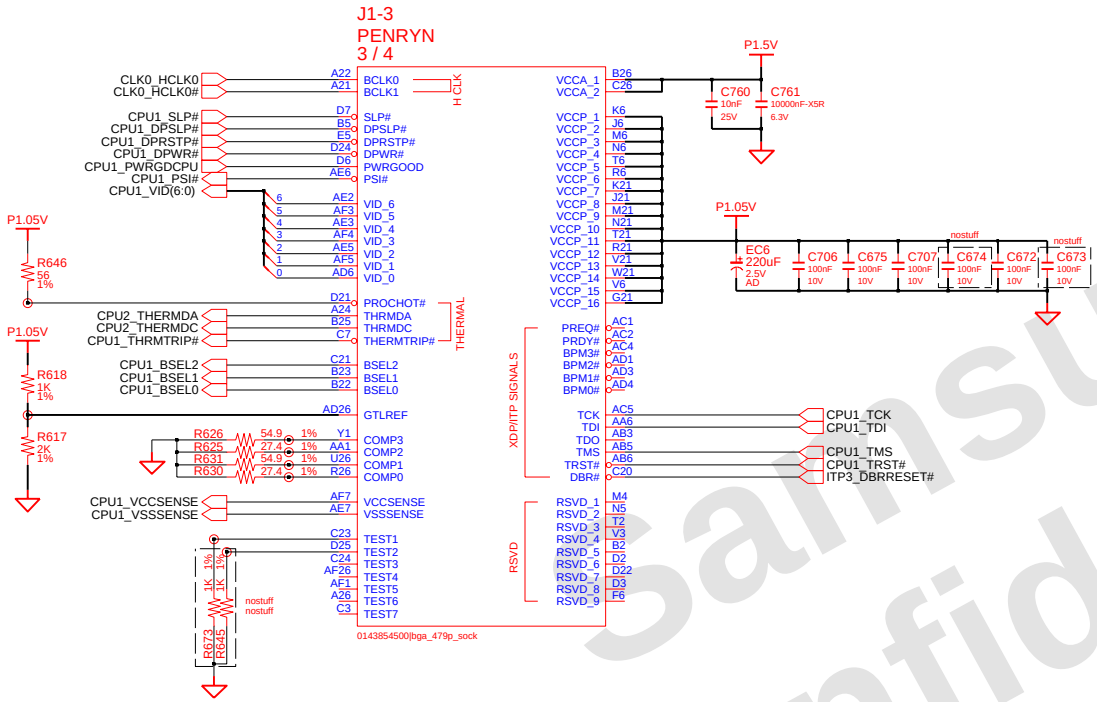
Place 14.318MHz within 500mils of CK-505

DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	





DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L CPU PENRYN (1/3)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 1 OF 3



CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 0	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp

DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

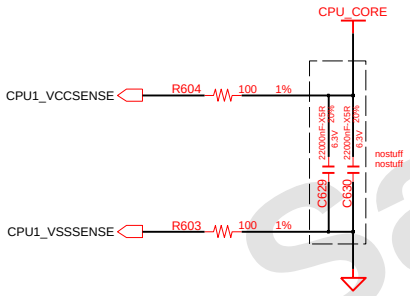
COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

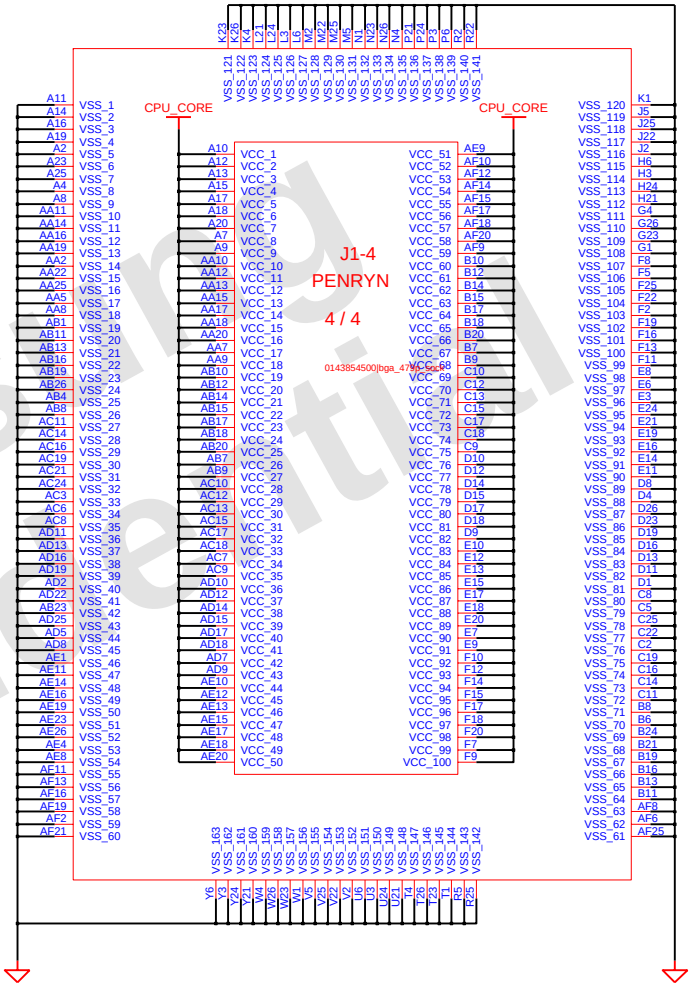
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

BSEL

		Pull-down
FSB 1067 MHz FSB 800 MHz		BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

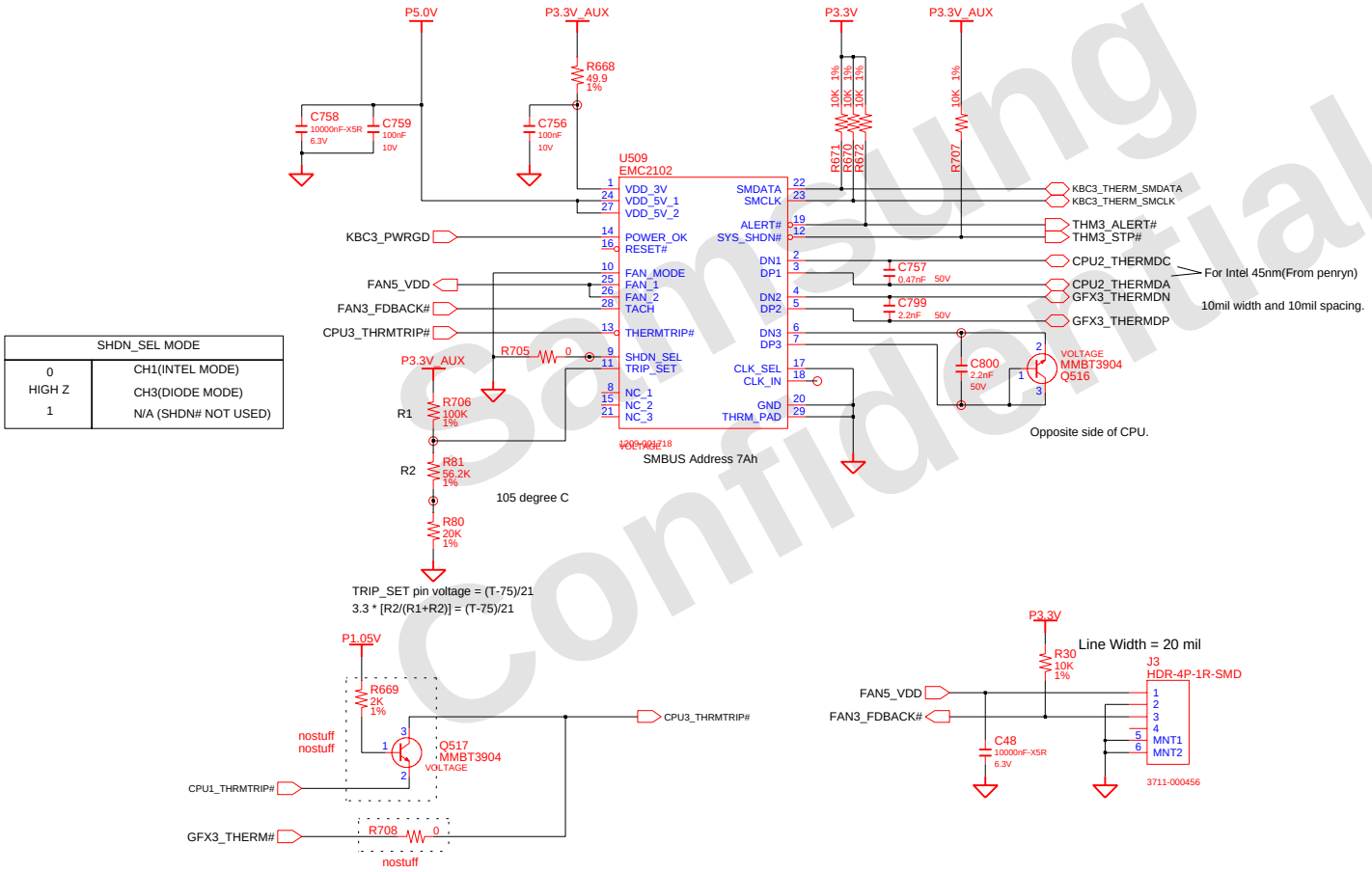
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L CPU PENRYN (2/3)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 2 OF 3	





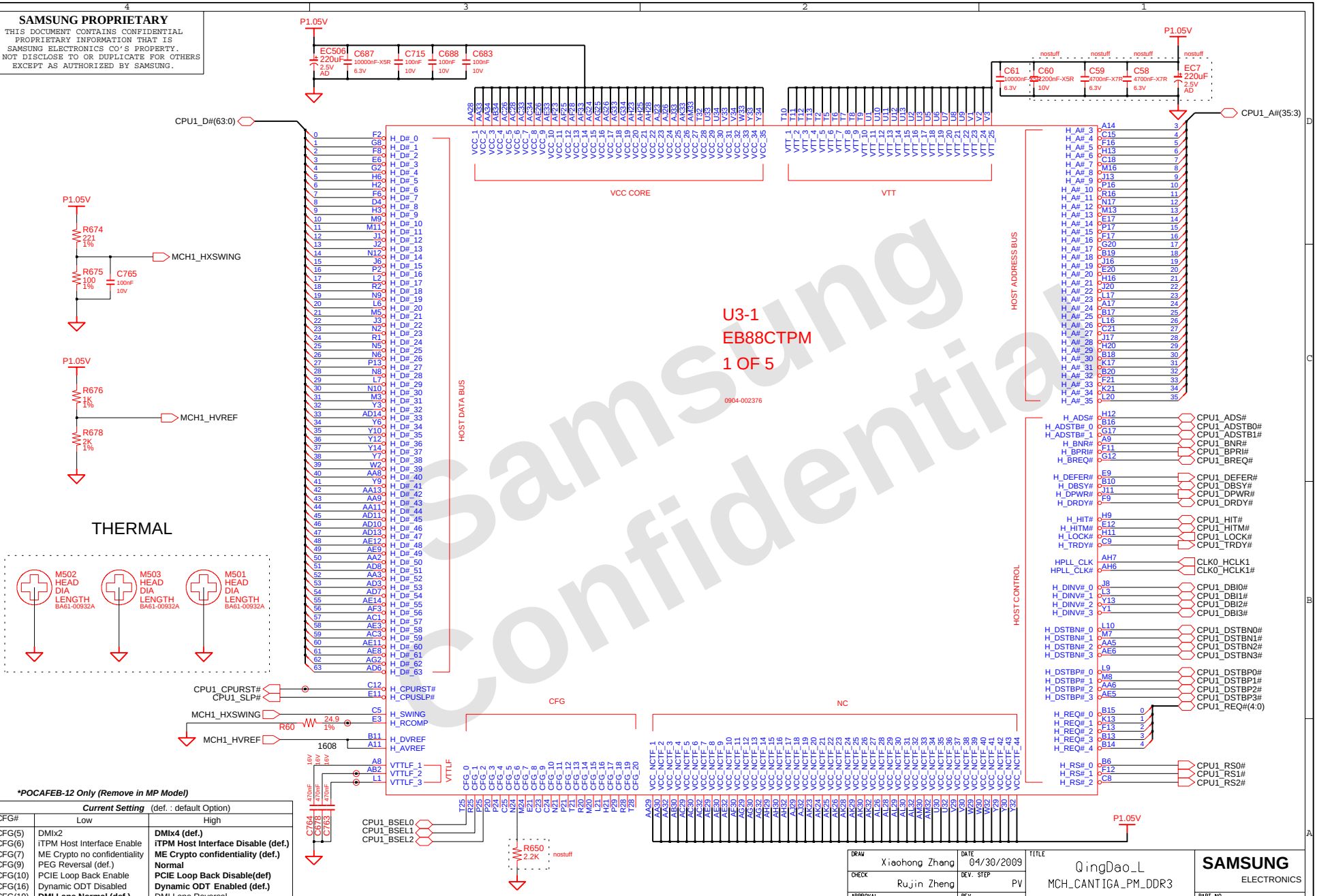
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 3 OF 3	

THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

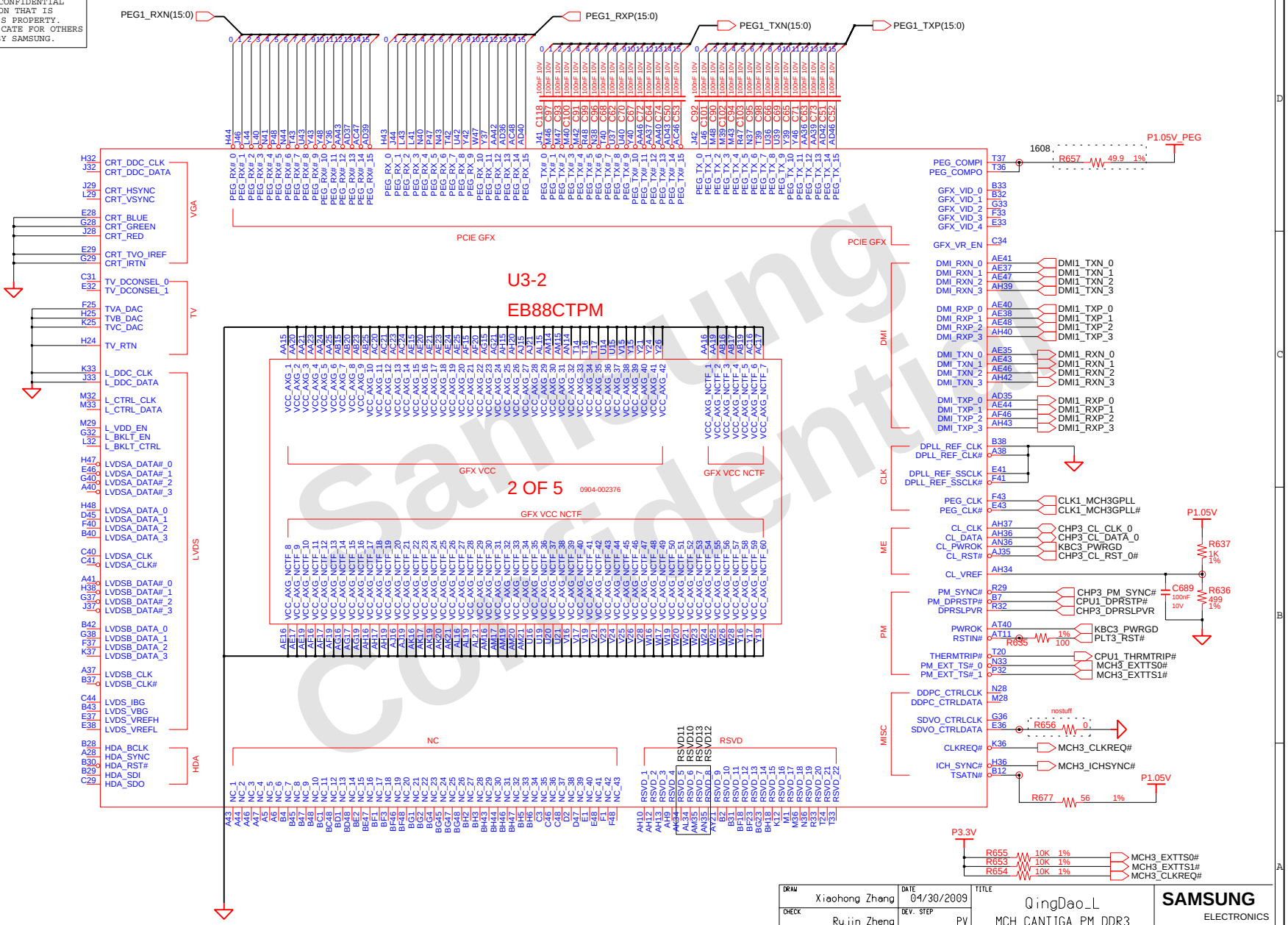
DESIGN: XIAOHONG, ZHANG	DATE: 12/3/2008	TITLE: QingDao_Ext THERMAL SENSOR EMC2102	SAMSUNG ELECTRONICS
CHECK: RUJIN, ZHENG	DEV. STEP: ADV1		PART NO.: BA41-xxxxxA
APPROVAL: BC, LEE	REV: 1.0		
MODULE CODE:	LAST EDIT: December, 3, 2008 12:55:11 PM	PAGE 1 OF 1	



POCAFEB-12 Only (Remove in MP Model)

CFG#	*Current Setting* (def. : default Option) Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	iTPM Host Interface Enable	**iTPM Host Interface Disable (def.)**
CFG(7)	ME Crypto no confidentiality	**ME Crypto confidentiality (def.)**
CFG(9)	PEG Reversal (def.)	**Normal**
CFG(10)	PCIE Loop Back Enable	**PCIE Loop Back Disable(def)**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(19)	**DMI Lane Normal (def.)**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	**SAMSUNG** ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	MCH_CANTIGA_PM_DDR3	
APPROVAL: BC LEE	REV: 1.0	CANTIGA (1/5)	PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 5	



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	MCH_CANTIGA_PM_DDR3	
APPROVAL: BC LEE	REV: 1.0	CANTIGA (2/5)	PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 2 OF 5	

PLACE EACH CAP NEAR AV42 PIN

MEM1_ADQ(63:0)

MEM1_VREF — C661 100nF 10V, C660 100nF 10V (nostuff)

R619 499 1%

MEM1_ABS(2:0) → SA_BS_0, SA_BS_1, SA_BS_2

MEM1_ADM(7:0) → SA_DM_0 … SA_DM_7

MEM1_ADQS#(7:0) → SA_DQS#_0 … SA_DQS#_7

MEM1_ADQS(7:0) → SA_DQS_0 … SA_DQS_7

MEM1_AMA(14:0) → SA_MA_0 … SA_MA_14

MEM1_ACAS#, MEM1_ARAS#, MEM1_AWE# → SA_CAS#, SA_RAS#, SA_WE#

MEM1_CS0#, MEM1_CS1# → SA_CS#_0, SA_CS#_1

MEM1_ODT0, MEM1_ODT1 → SA_ODT_0, SA_ODT_1

MEM1_CKE0, MEM1_CKE1 → SA_CKE_0, SA_CKE_1

CLK1_MCLK0, CLK1_MCLK0#, CLK1_MCLK1, CLK1_MCLK1# → SA_CK_0, SA_CK#_0, SA_CK_1, SA_CK#_1

P1.8V_AUX — R621 80.6 1%, R620 80.6 1%

SM_RCOMP, SM_RCOMP#, SM_RCOMP_V_OH, SM_RCOMP_V_OL

Route as short as possible

P1.8V_AUX — R622 1K 1%, R607 3.01K 1%, R606 1K 1%; C656 100nF 10V, C655 2200nF-X5R 10V, C636 100nF 10V, C637 2200nF-X5R 10V (nostuff)

SYSTEM MEMORY A

SYSTEM MEMORY B

U3-3
EB88CTPM
3 OF 5

0904-002376

SM_REXT, SM_VREF → MEM1_VREF

SM_DRAMRST#, SM_PWROK → DDR 3 : Connect to VR. DDR 2 : Connect to GND

SB_CAS#, SB_RAS#, SB_WE# → MEM1_BCAS#, MEM1_BRAS#, MEM1_BWE#

SB_CS#_0, SB_CS#_1 → MEM1_CS2#, MEM1_CS3#

SB_ODT_0, SB_ODT_1 → MEM1_ODT2, MEM1_ODT3

SB_CKE_0, SB_CKE_1 → MEM1_CKE2, MEM1_CKE3

SB_CK_0, SB_CK#_0, SB_CK_1, SB_CK#_1 → CLK1_MCLK2, CLK1_MCLK2#, CLK1_MCLK3, CLK1_MCLK3#

SB_DM_0 … SB_DM_7 → MEM1_BDM(7:0)

SB_DQS#_0 … SB_DQS#_7 → MEM1_BDQS#(7:0)

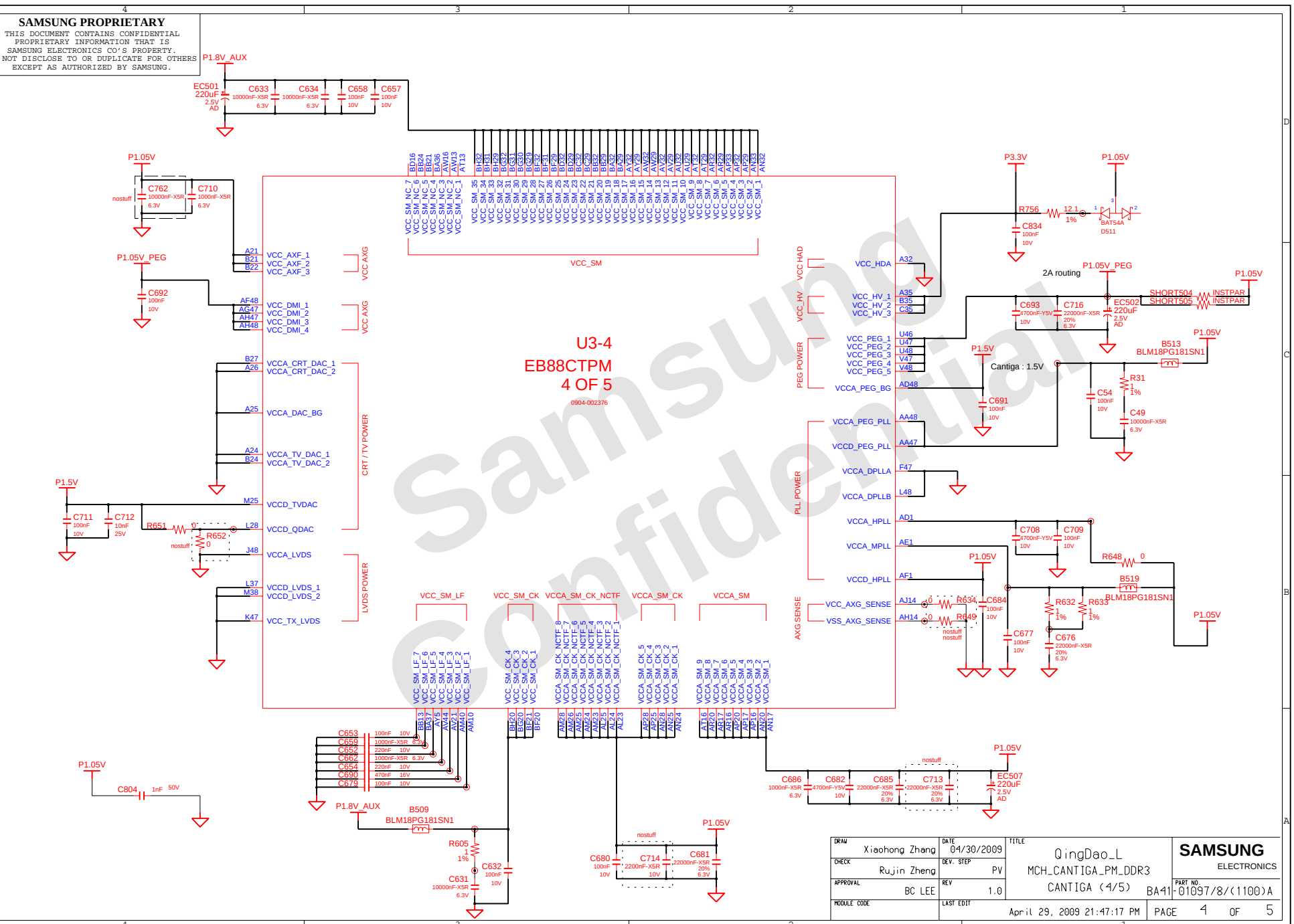
SB_DQS_0 … SB_DQS_7 → MEM1_BDQS(7:0)

SB_MA_0 … SB_MA_14 → MEM1_BMA(14:0)

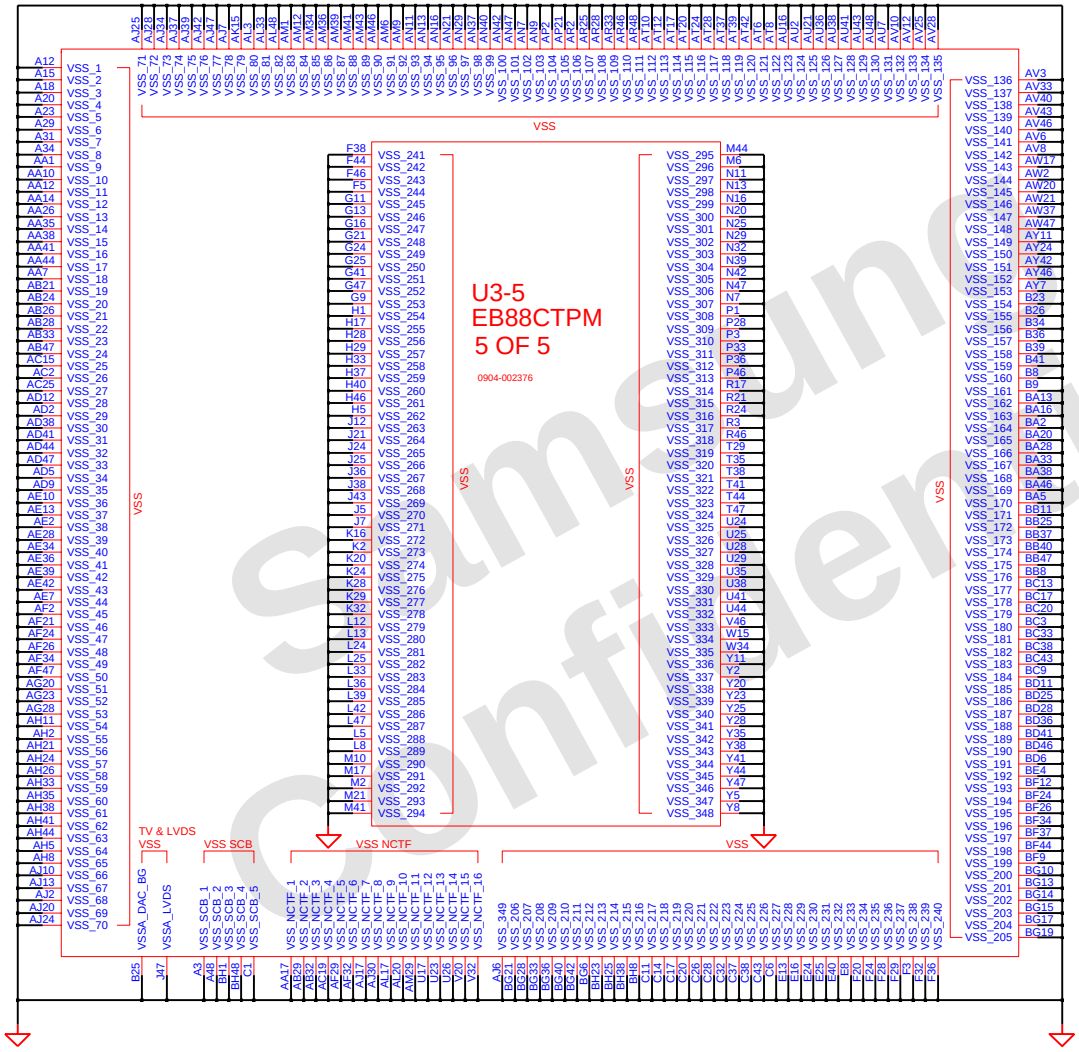
SB_BS_0, SB_BS_1, SB_BS_2 → MEM1_BBS(2:0)

SB_DQ_0 … SB_DQ_63 → MEM1_BDQ(63:0)

DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	MCH_CANTIGA_PM_DDR3	
APPROVAL: BC LEE	REV: 1.0	CANTIGA (3/5)	PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 3 OF 5	

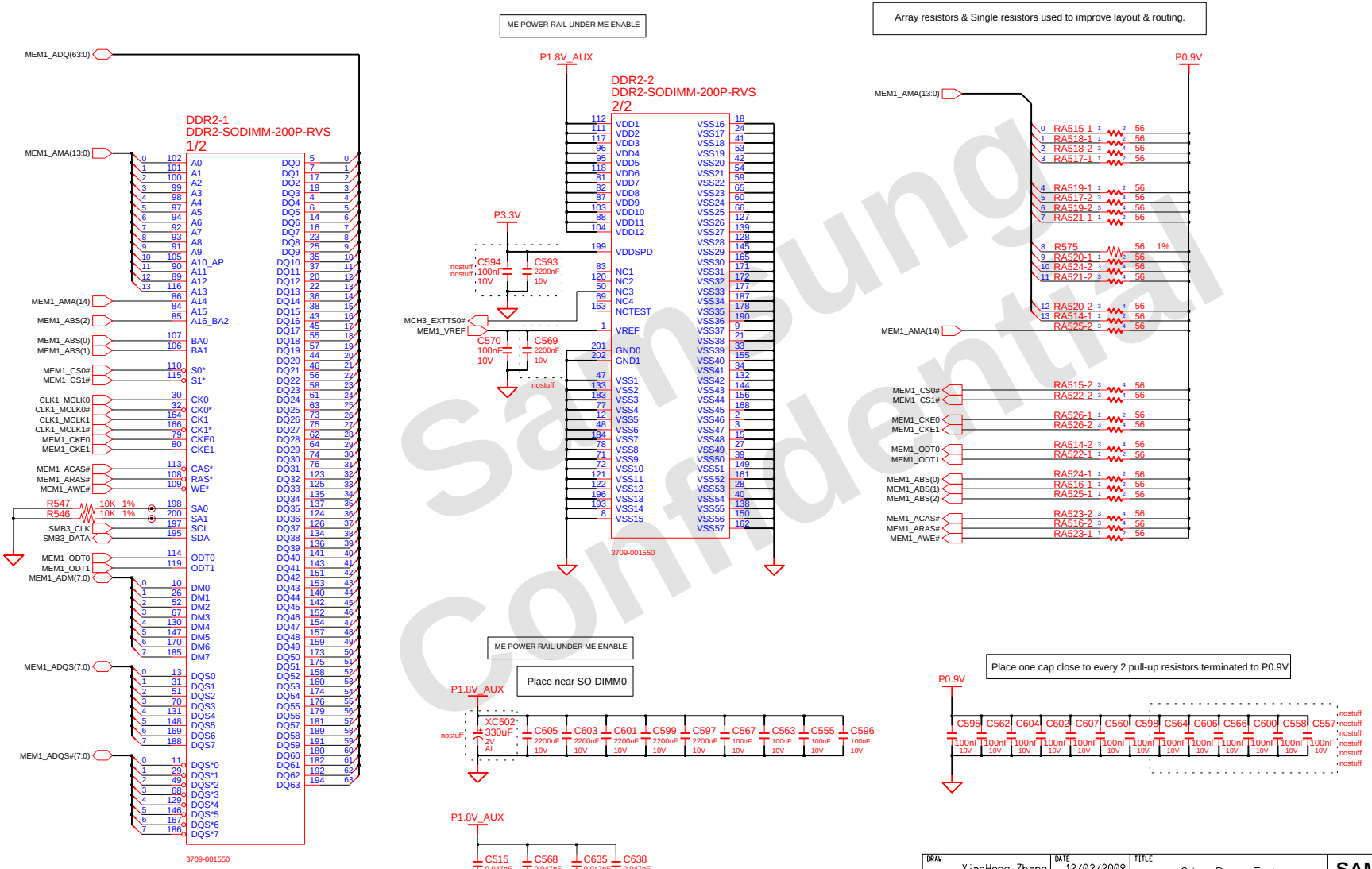


DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	MCH_CANTIGA_PM_DDR3	
APPROVAL: BC LEE	REV: 1.0	CANTIGA (4/5)	PART NO. BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 4 OF 5	



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MCH_CANTIGA_PM_DDR3 CANTIGA (5/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 5 OF 5

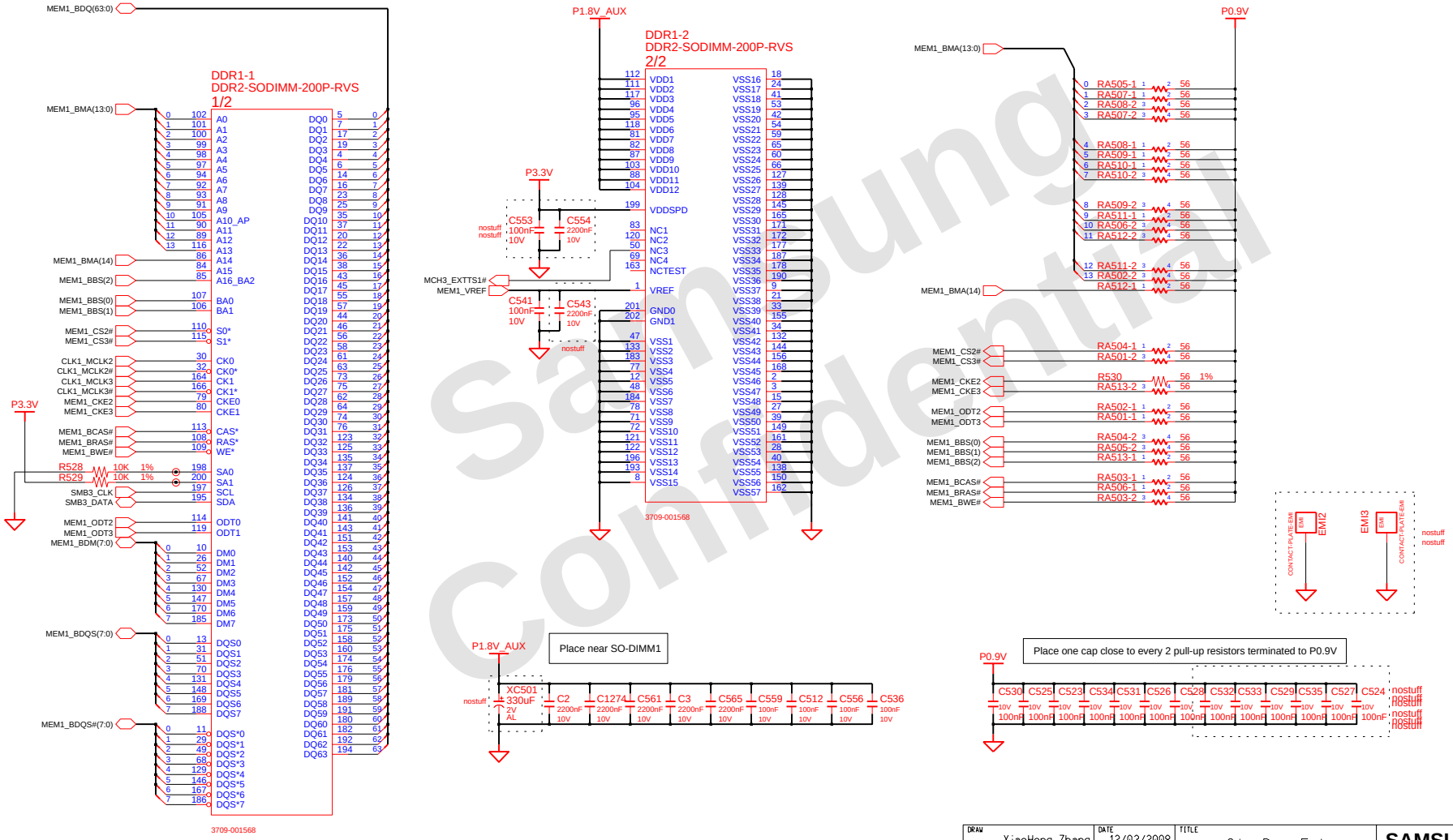
DDR SO-DIMM #0



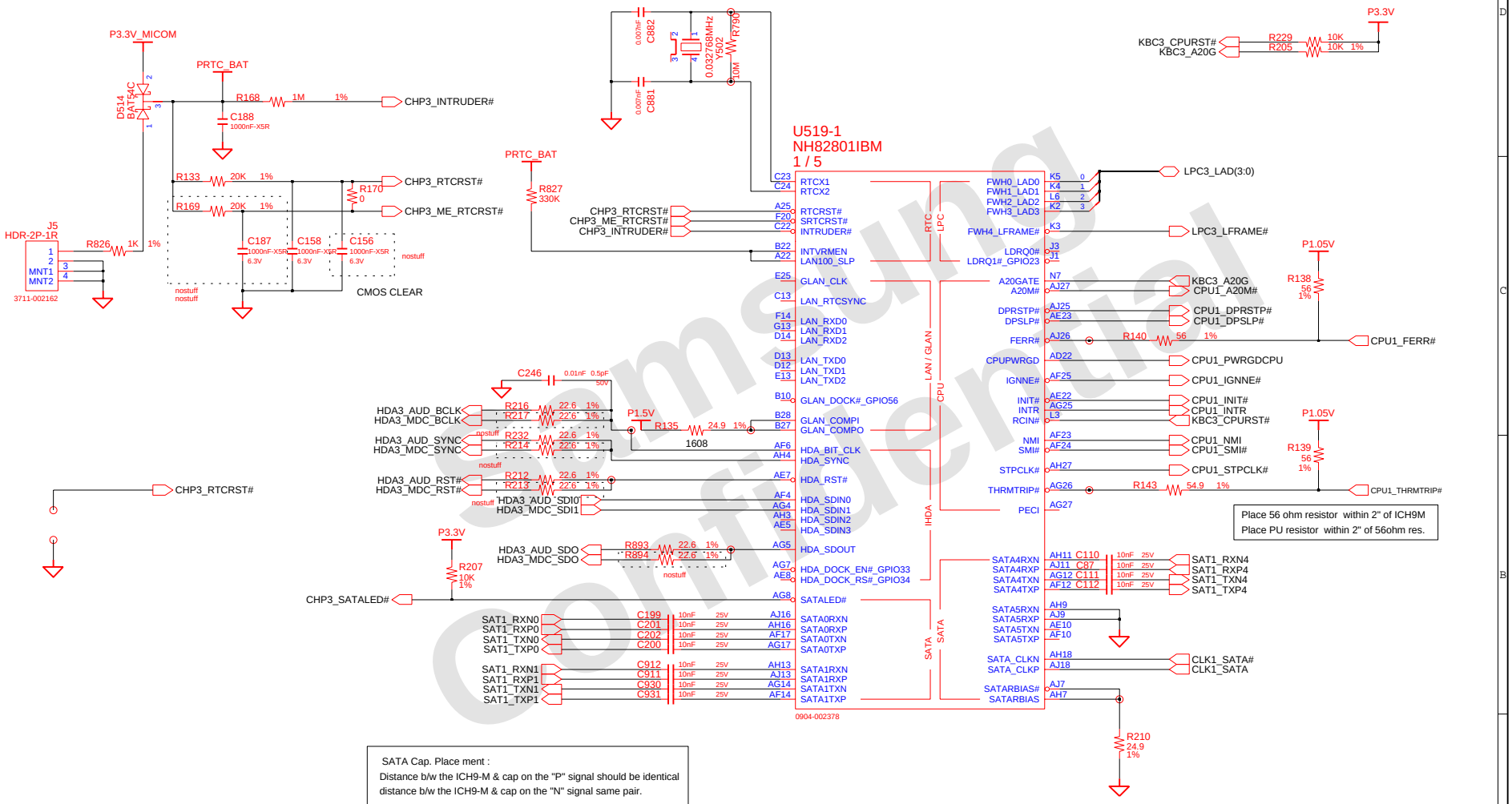
DRAW: XiaoHong Zhang	DATE: 12/03/2008	TITLE: QingDao_Ext SODIMM_DDR2 SODIMM_DDR2 #1	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: December 03, 2008 20:55:25 PM	PAGE 1 OF 2	

DDR SO-DIMM #1

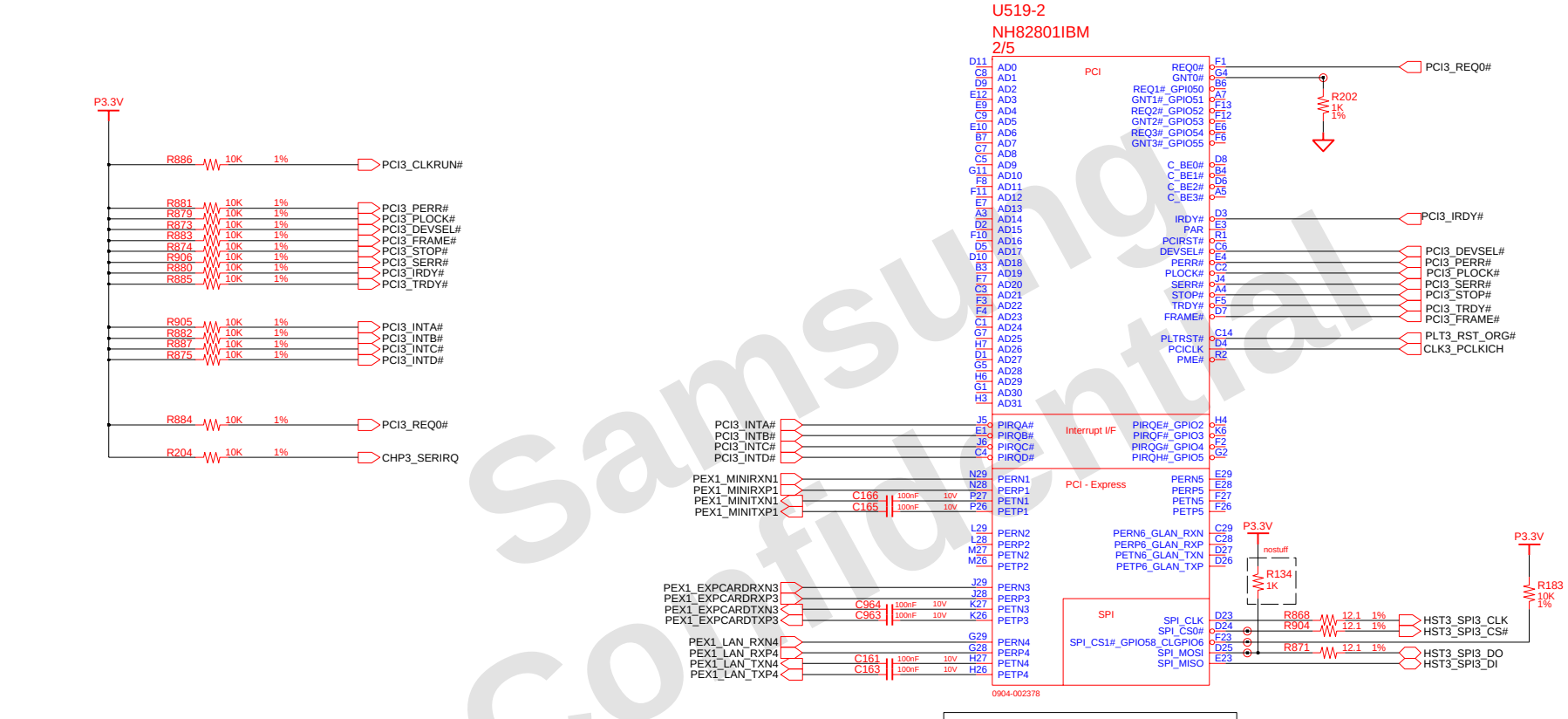
Array resistors & Single resistors used to improve layout & routing.



DRAW: XiaoHong Zhang	DATE: 12/03/2008	TITLE: QingDao_Ext SODIMM_DDR2 SODIMM_DDR2 #2	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1		PART NO.: BA41-xxxxxA
APPROVAL: BC LEE	REV: 1.0		
MODULE CODE	LAST EDIT: December 03, 2008 20:55:25 PM	PAGE 2 OF 2	

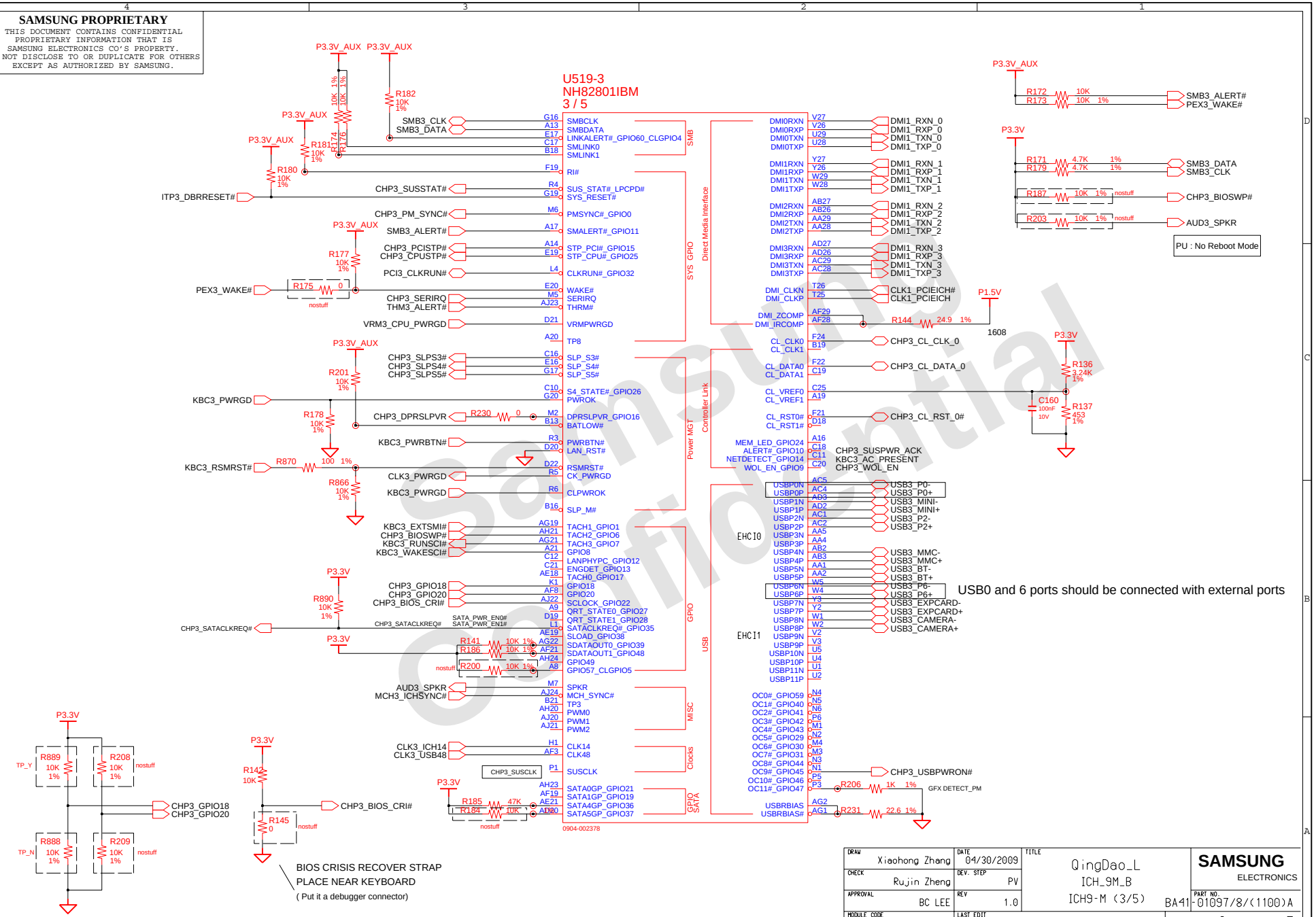


DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L ICH_9M_B ICH9-M (1/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 5	

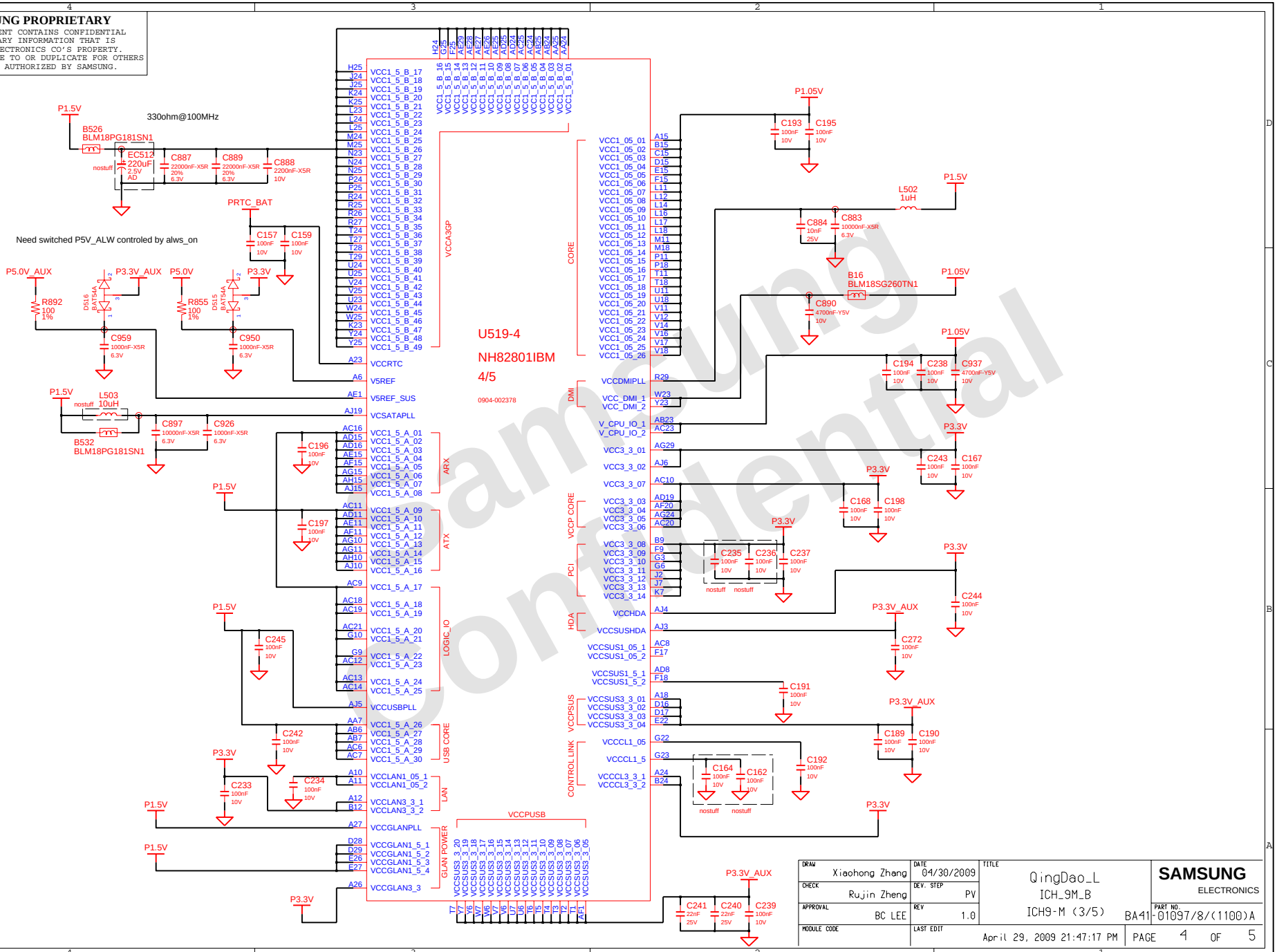


AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs

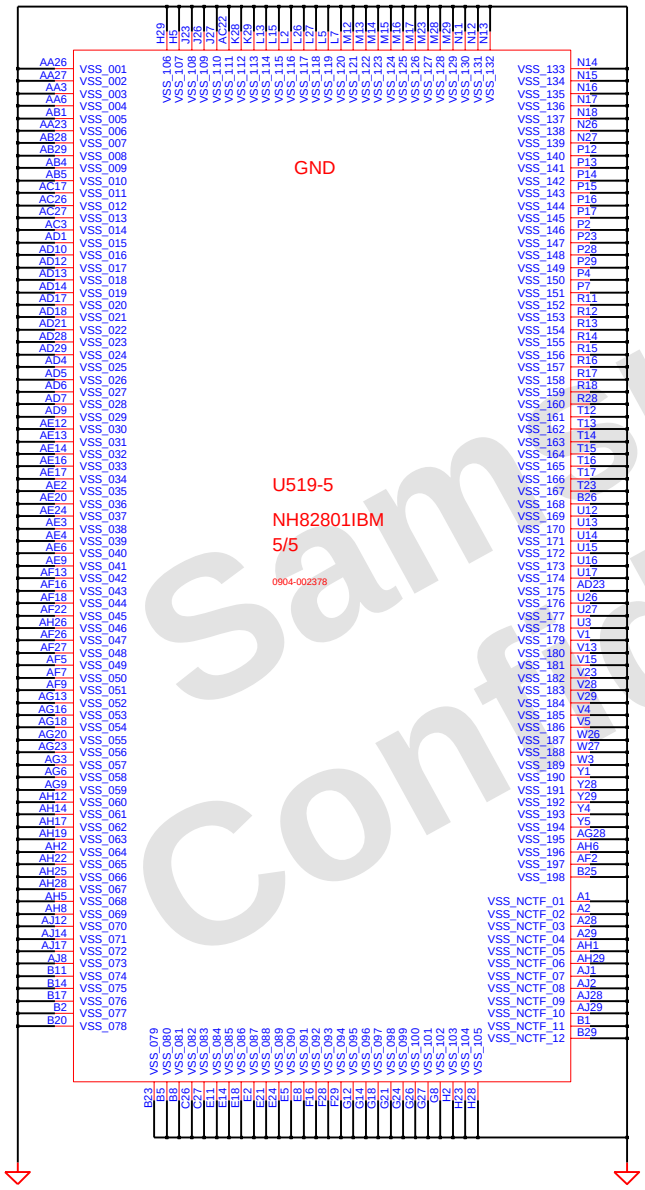
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 2 OF 5	



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 3 OF 5	

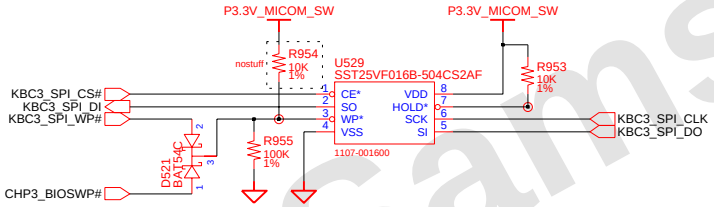


DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 4 OF 5	

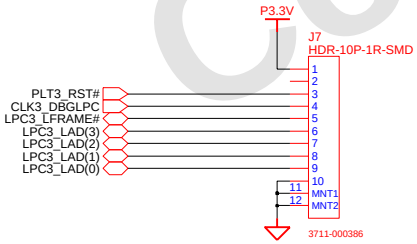


DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L / ICH_9M_B / ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 4 OF 5	

SPI_BIOS_ROM

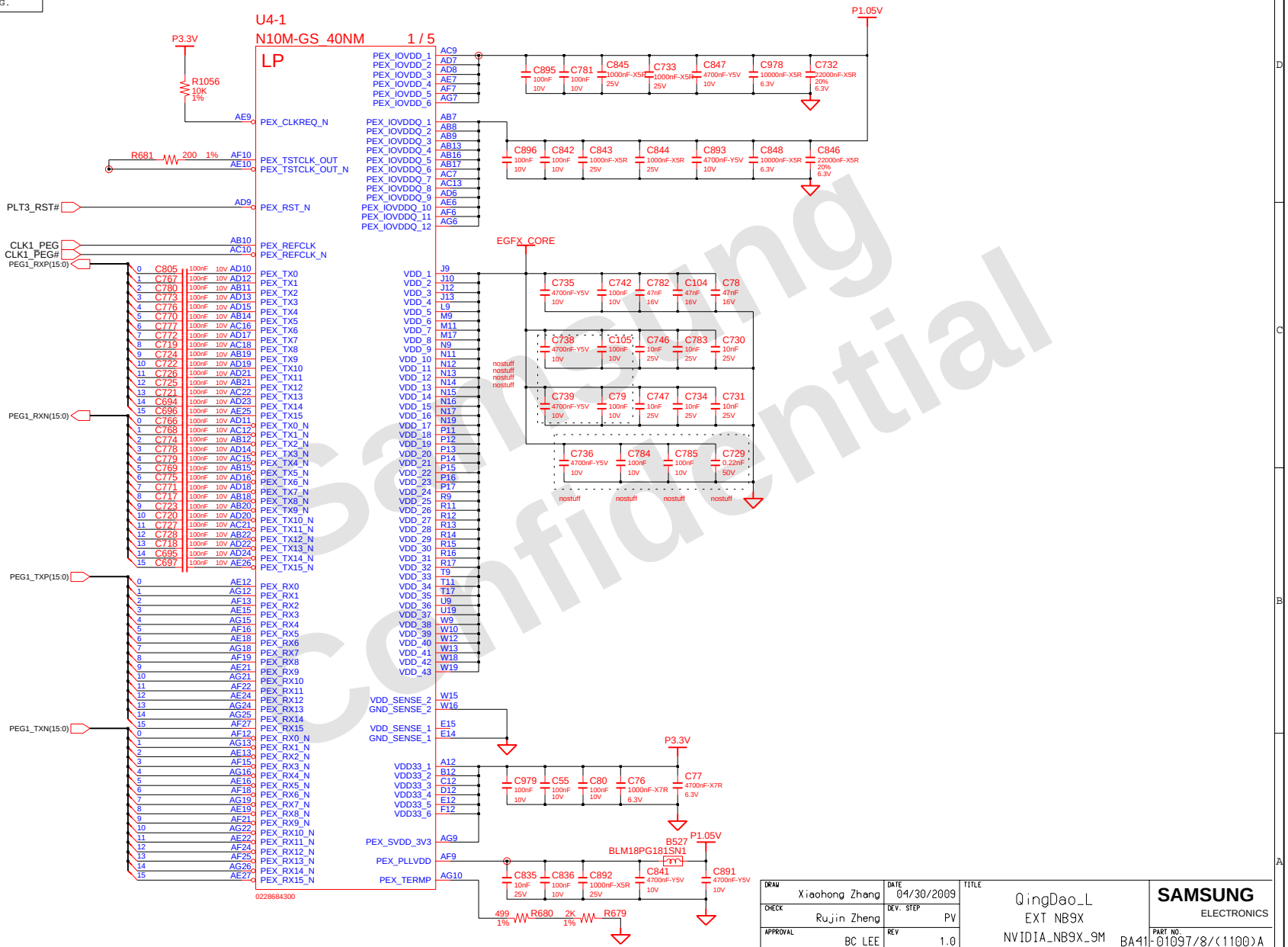


80H DECODER CONNECTOR

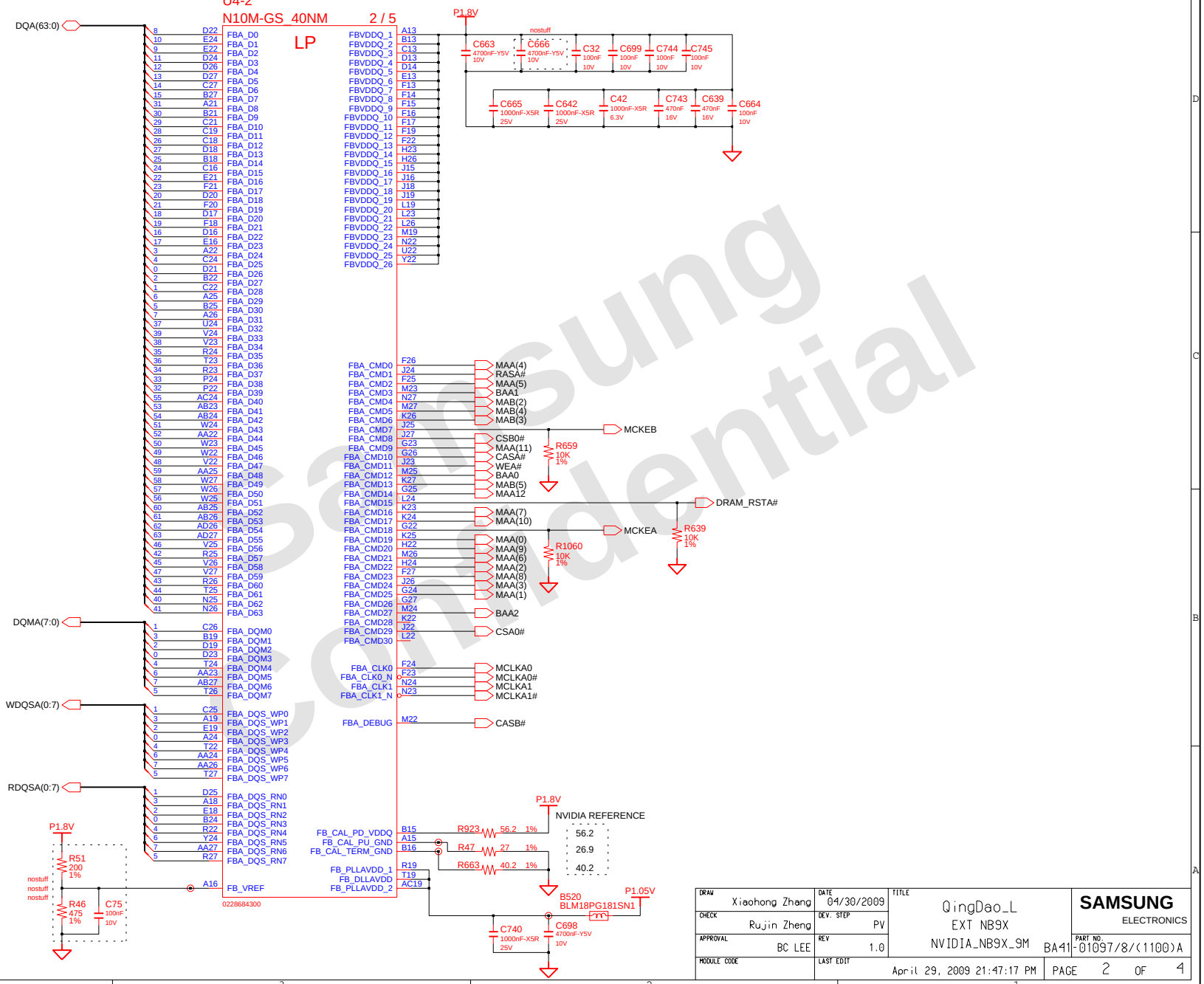


02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET	86 RE-INIT. ON-BOARD I/O PORT
WITH INITIAL POST VALUE	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

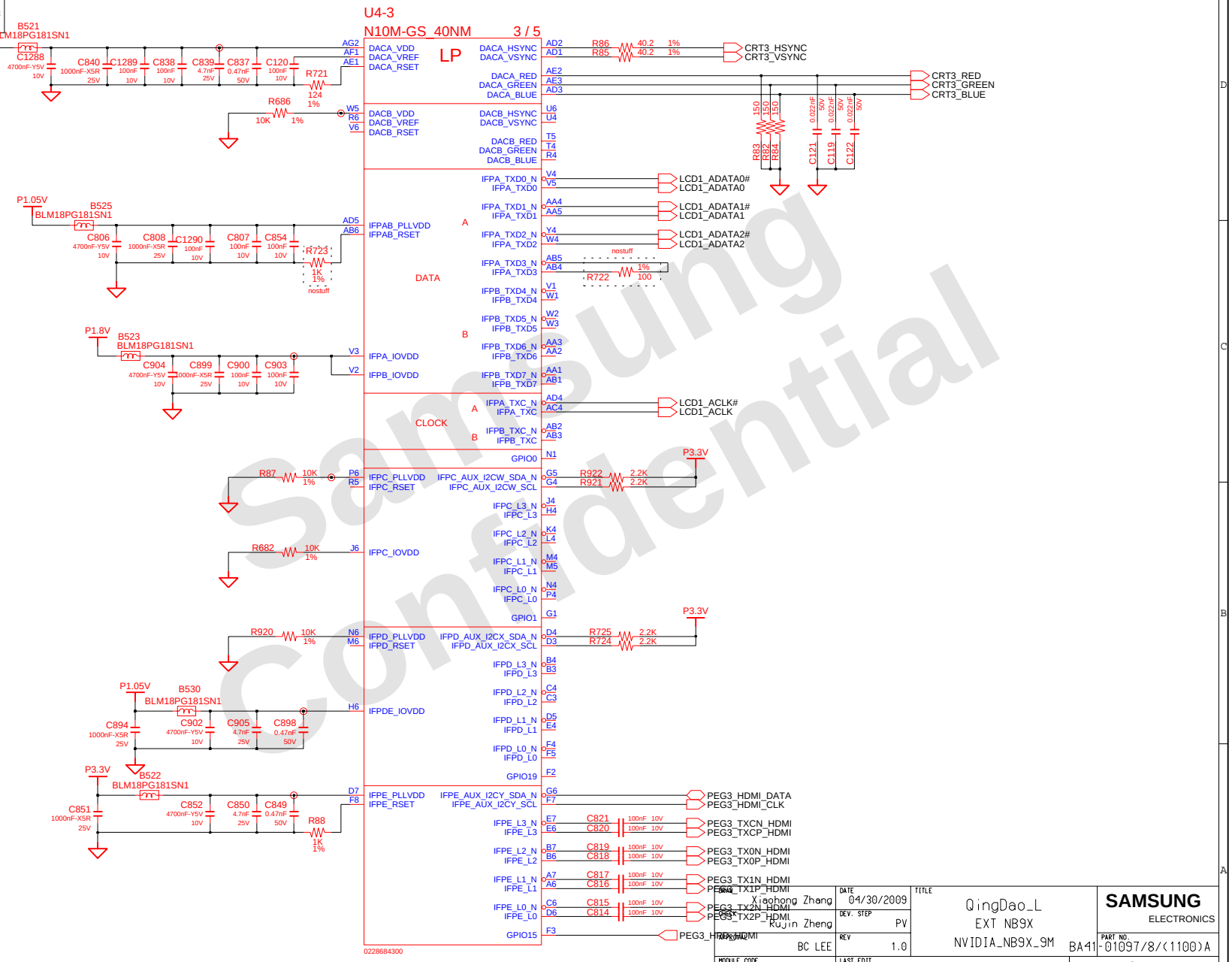
DRAW: XiaoHong Zhang	DATE: 12/03/2008	TITLE: QingDao_Ext SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1	SPI_BIOS_ROM	PART NO.: BA41-xxxxxA
APPROVAL: BC LEE	REV: 1.0		
MODULE CODE	LAST EDIT: December 03, 2008 20:56:20 PM	PAGE 1 OF 1	



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L EXT NB9X NVIDIA_NB9X_9M	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 4	



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	EXT NB9X	
APPROVAL: BC LEE	REV: 1.0	NVIDIA_NB9X_9M	PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 2 OF 4	



DRAWN	Xiaohong Zhang	DATE	04/30/2009
CHECK	Kujin Zheng	DEV. STEP	PV
APPROVED	BC LEE	REV	1.0
MODULE CODE		LAST EDIT	April 29, 2009 21:47:17 PM

TITLE: QingDao_L EXT NB9X NVIDIA_NB9X_9M

SAMSUNG ELECTRONICS

PART NO. BA41-01097/8/(1100)A

D:/users/ecadll/qingdao_ulcpc/mfg/pv/Qingdao_E_ULCPC_MAIN/design_blocks/Gfx_External_Nvidia_NB9x_9M

Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V
GPIO(6)	GPU VID1	10 0.85V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0 27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0110 for NB	
25K ohm	1100	0100	N10M-GS:0x0A74	
30K ohm	1101	0101	N10M-GE:0x0A68	
35K ohm	1110	0110	N10M-LP:0x0A69	
45K ohm	1111	0111	N10M-NS:0x0A6C	
			N10M-NE:0x0A6A	
			N10M-GLM:0x0A7C	

	Bit3	Bit2	Bit1	Bit0		
ROMSO	0	0	0	1	27M	
SCLK	0	0	1	0	GFX TPYE	
SI	0	1	1	1	1Gb	
Strap2	1	0	0	1	N10M-LP	DEVICE ID
Strap1	0	1	1	0	For NB	
Strap0	1	1	1	1	EDID_EN	

U4-4
N10M-GS_40NM
4 / 5
LP

U4-5
N10M-GS_40NM
LP
5 / 5

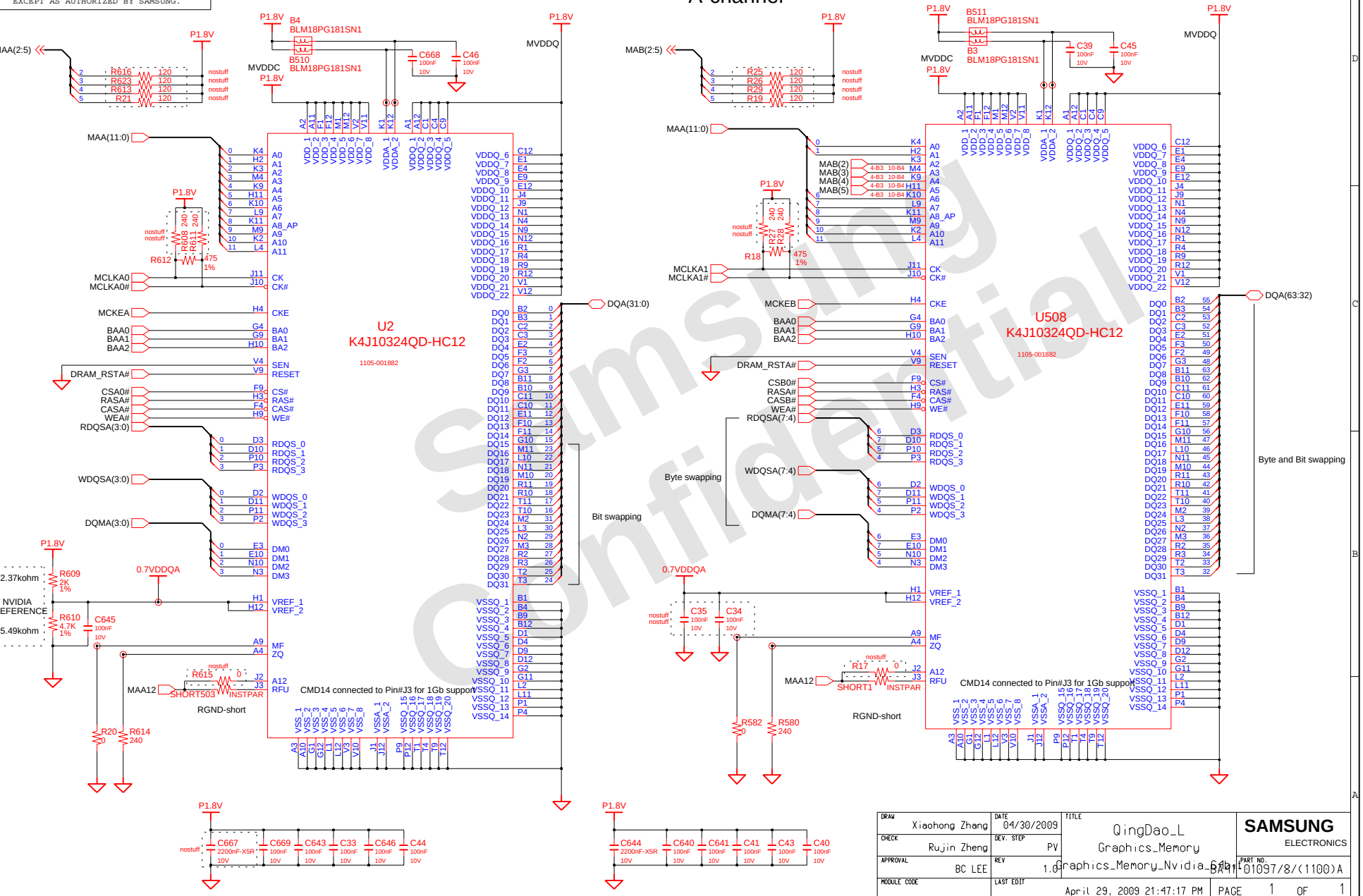
PU is for I2C ROM (AT24C16B, A0~A2 = 000)
PD is for Crypto ROM

HDCP

DRAW Xiaohong Zhang	DATE 04/30/2009	TITLE QingDao_L EXT NB9X NVIDIA_NB9X_9M	SAMSUNG ELECTRONICS
CHECK Rujin Zheng	DEV. STEP PV		
APPROVAL BC LEE	REV 1.0		PART NO. BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT April 29, 2009 21:47:17 PM		PAGE 4 OF 4

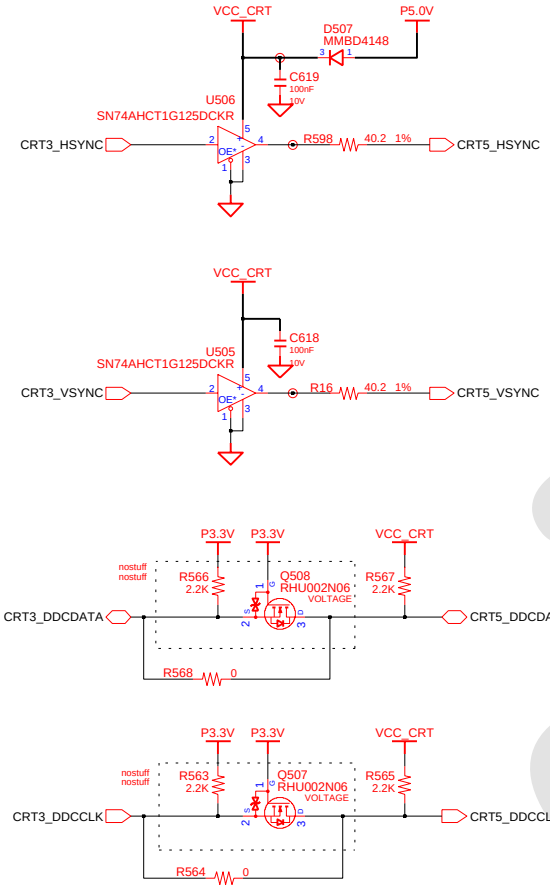
nVidia can support 700MHz, but for N10M_GE, there only debug 800MHz about VBIOS

A-channel

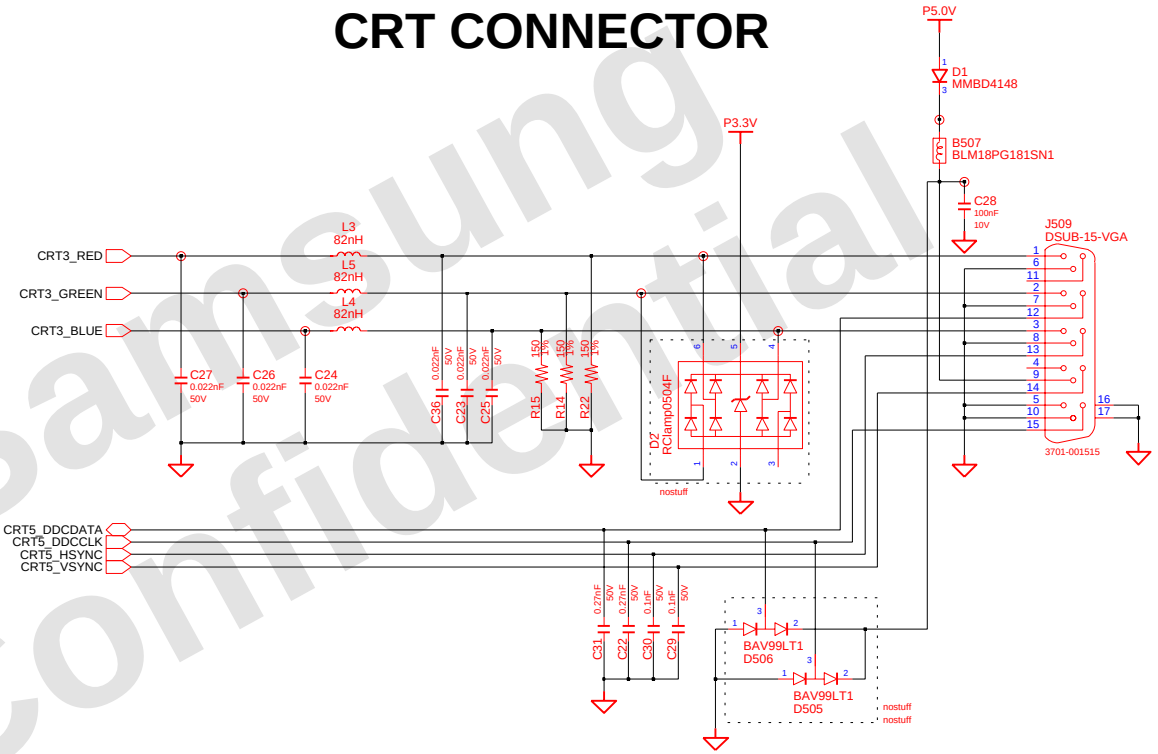


DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L Graphics_Memory	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0	Graphics_Memory_Nvidia_64bit	PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

CRT



CRT CONNECTOR



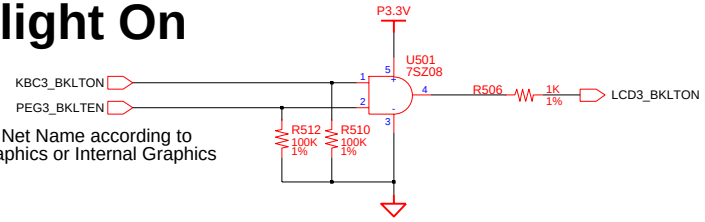
Check "CRT3_DDCCLK/DATA" Voltage Level

2N06 Can be replaced with SM6K2

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L GRAPHICS_IF CRT	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: 1 of undefined	

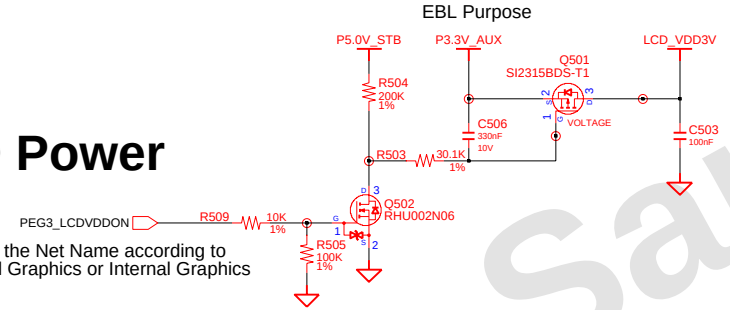
LVDS

Backlight On



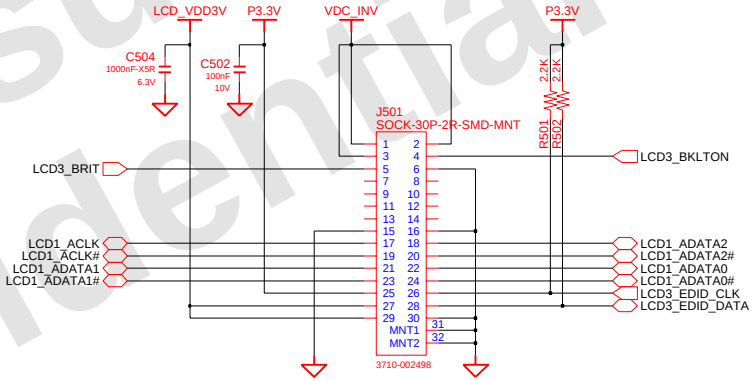
Change the Net Name according to External Graphics or Internal Graphics

LCD Power

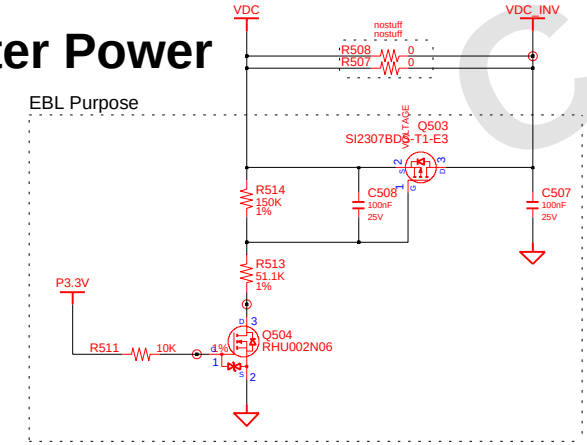


Change the Net Name according to External Graphics or Internal Graphics

1Ch. LCD Connector

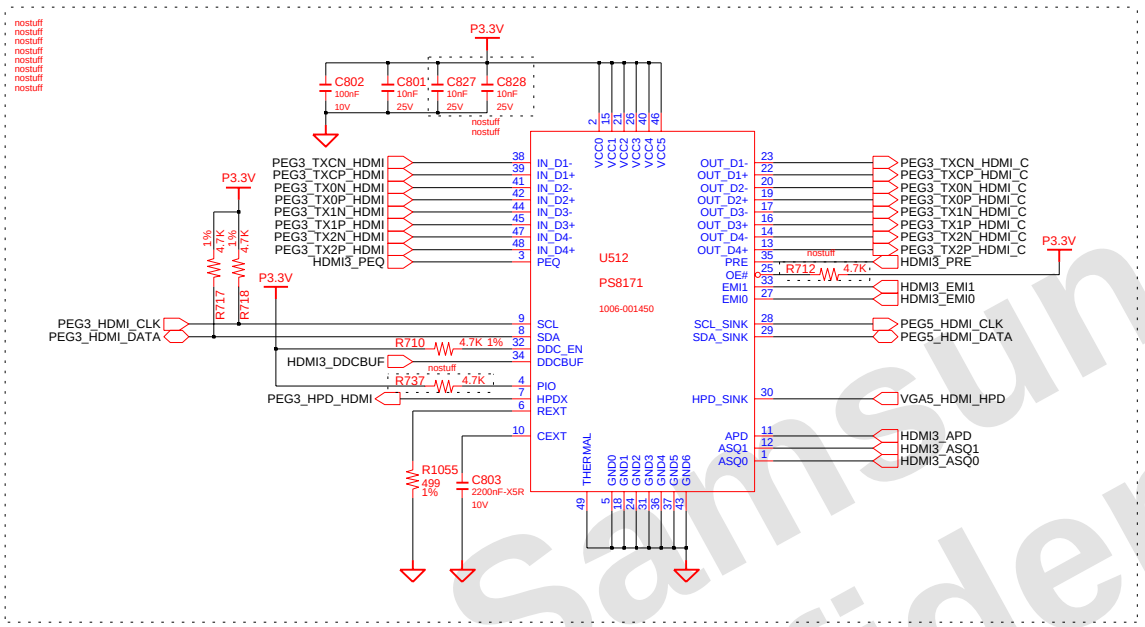


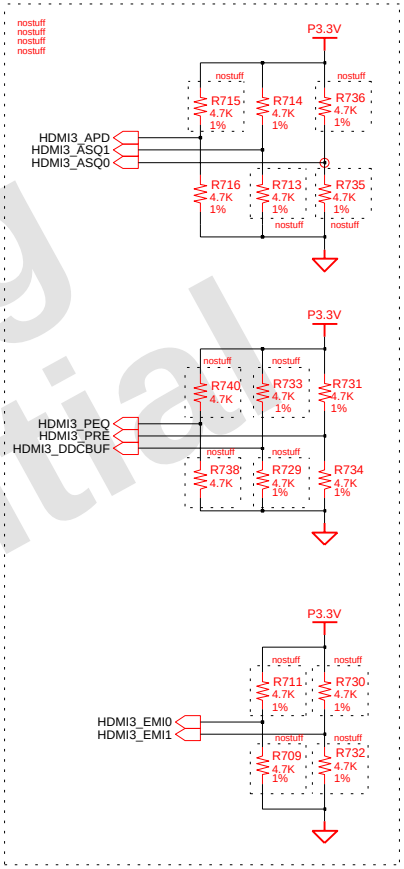
Inverter Power

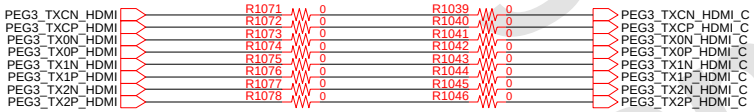


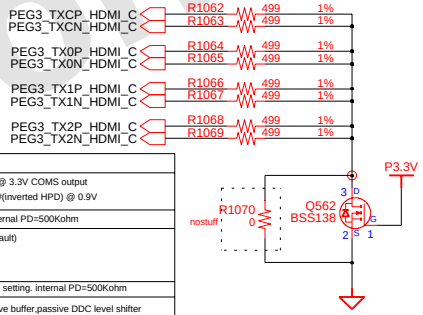
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L GRAPHICS_IF LCD	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: 2 under of ined	

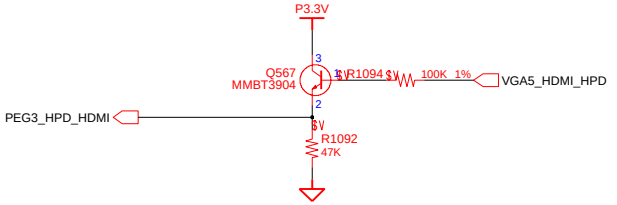
HDMI Level Shifter(Pre-emp)











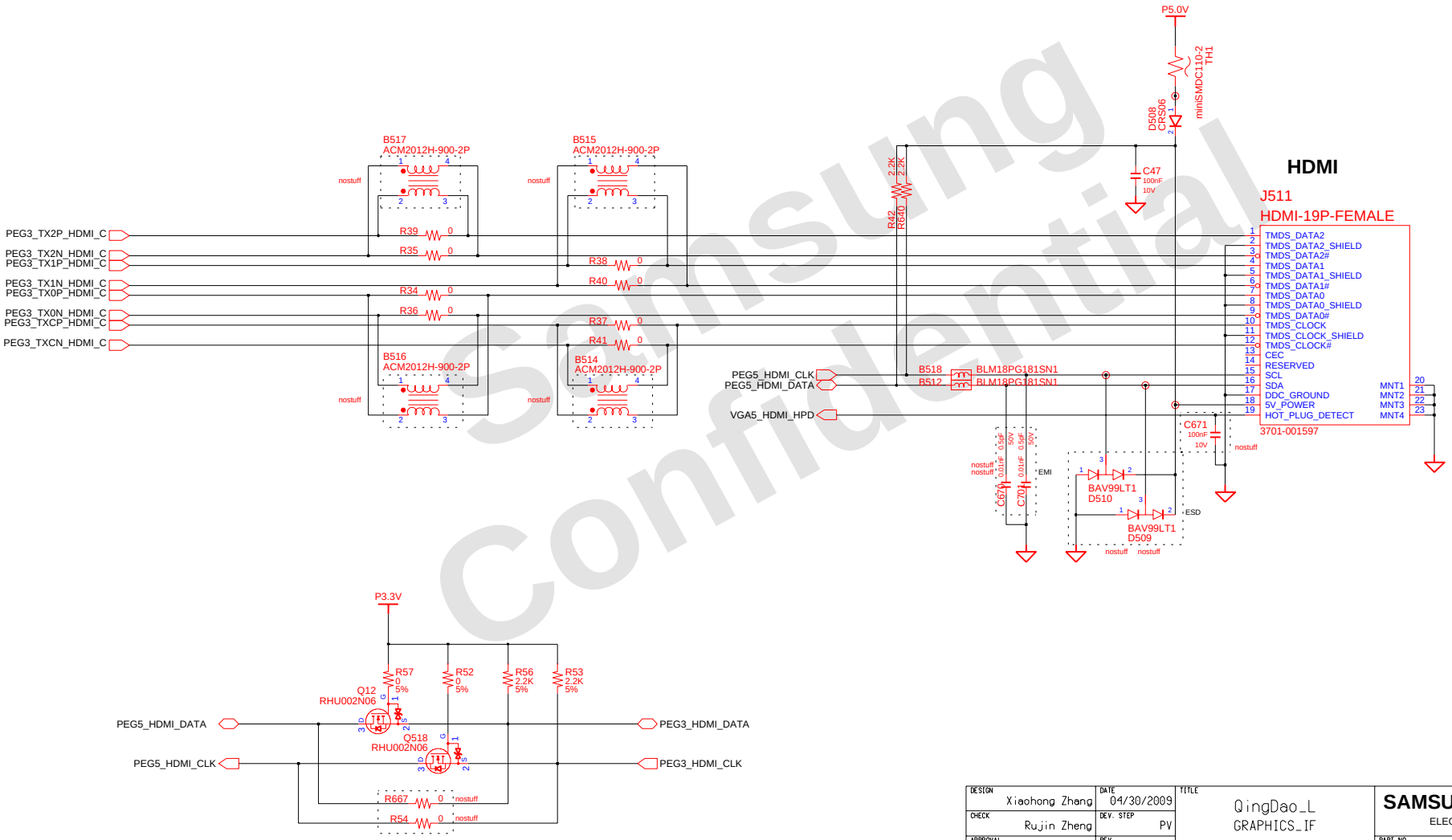
APD ASQ0.ASQ1	Same setting as PS8101. Debug in PV stage, then confirm value.

APD	Automatic power down management internal PU: R=500Kohm APD=LOW: Automatic power down disable APD=High: Automatic power down enable APD=MID: Reserved
EMI0/EMI1	EMI reduction and filter setting EMI1:internal PU: R=500Kohm EMI0:internal PD: R=500Kohm [EMI1,EMI0]=HL: no EMI reduction EMI0=High: Reduced rise/fall time MID: Reduced rise/fall time 2nd EMI1=LOW: EMI filter setting 1 MID: Reserved
ASQ0.ASQ1	Automatic squelch function internal PD: R=500Kohm [ASQ1,ASQ0]= HL: No automatic squelch LL: Automatic squelch enable, Level=120mVpp, default timer LH: Automatic squelch enable, Level=100mVpp, default timer HH: Automatic squelch enable, Level=80mVpp, default timer ML: Automatic squelch enable, Level=120mVpp, extended timer MH: Automatic squelch enable, Level=100mVpp, extended timer LM: Automatic squelch enable, Level=80mVpp, extended timer HM: Reserved MM: Reserved

HPDX	Define by PIO PIO=Low: HPD=HPD_SINK @ 3.3V COMS output PIO=High: HPD=HPD_SINK#(inverted HPD) @ 0.9V
PEQ	TMDS inputs equalization, internal PD=500Kohm PEQ=LOW: Mid level EQ (default) PEQ=High: High level EQ PEQ=MID: Low level EQ
DDCBUF	DDC Active Buffer enable and setting. internal PD=500Kohm DDCBUF=LOW: No DDC active buffer,passive DDC level shifter DDCBUF=High: Active DDC buffer enable, setting 1 DDCBUF=MID: Active DDC buffer enable, setting 2
PRE	TMDS output driver pre-emphasis level setting PRE=LOW: No pre-emphasis PRE=High: Low level pre-emphasis is added PRE=MID: High level pre-emphasis is added

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L GRAPHICS_IF HDMI LEVEL SHIFTER	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		PART NO.: BA41-01097/8/(1100)A
APPROVAL: BC LEE	REV: 1.0		
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: 4 of 4	

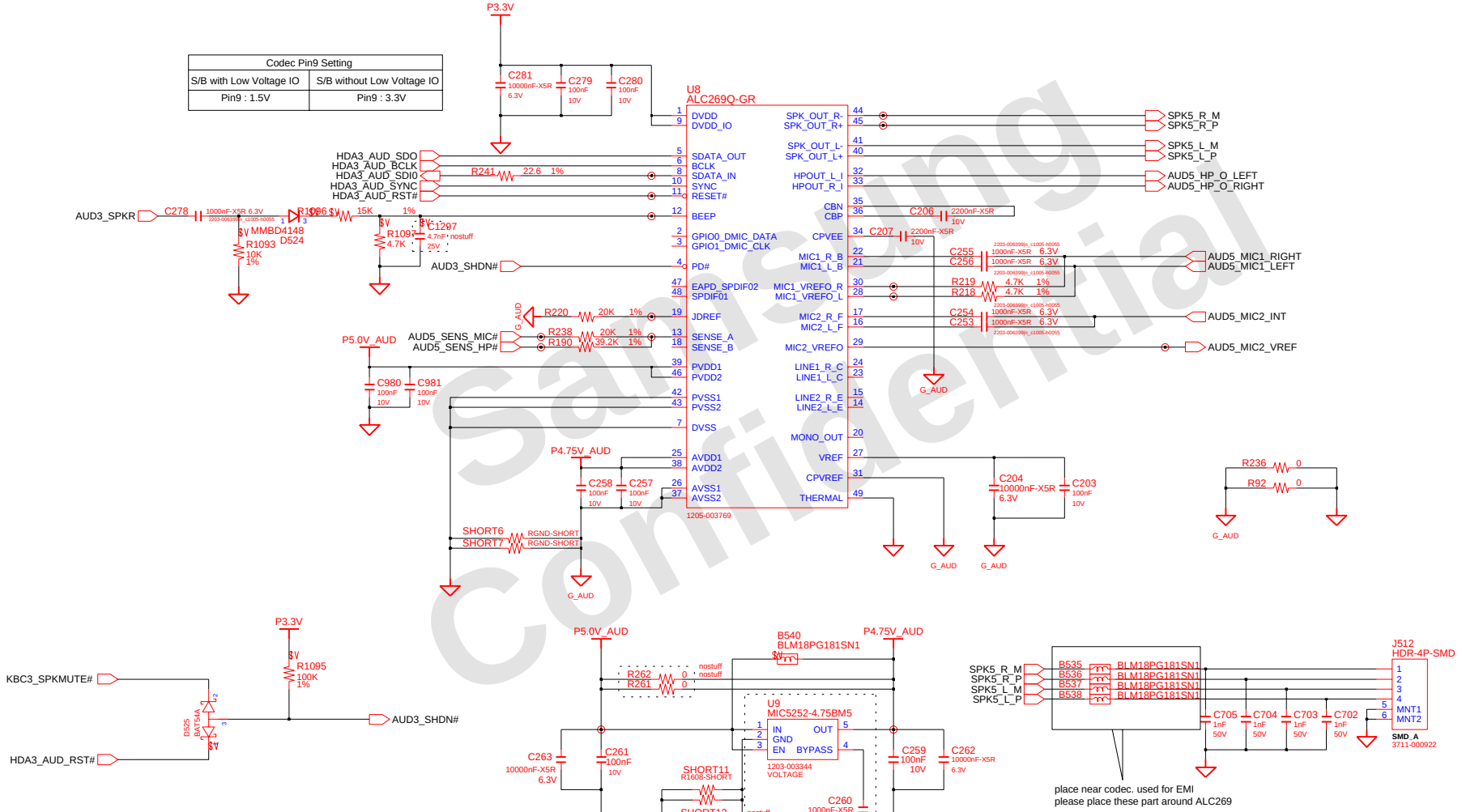
HDMI



DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: 3 undefined	

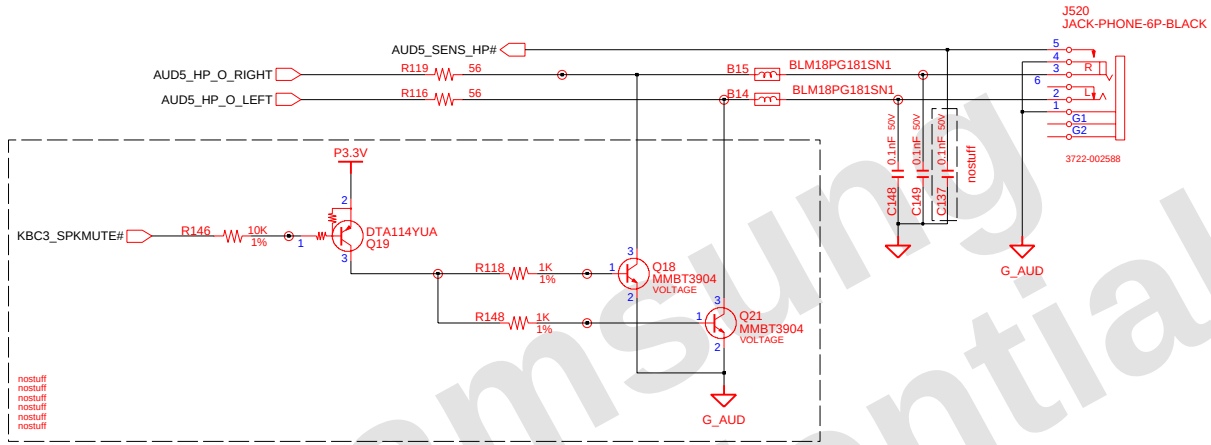
AUDIO

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

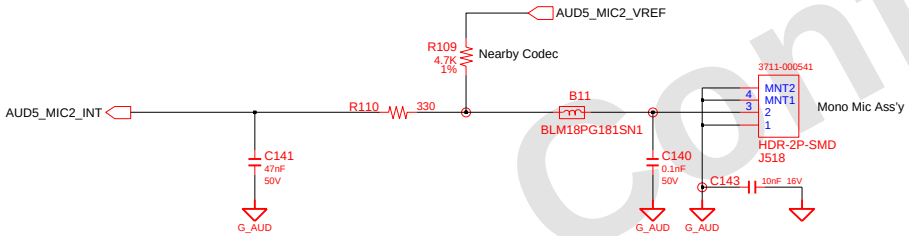


DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L HDA_CODEC_ALC272 AUDIO CODEC ALC272	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO. BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 5	

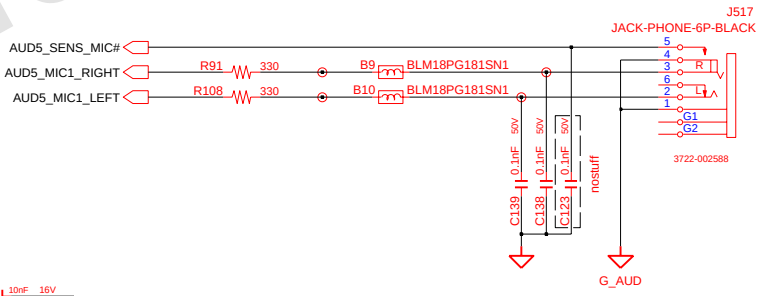
HEADPHONE

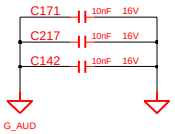


Analog MIC



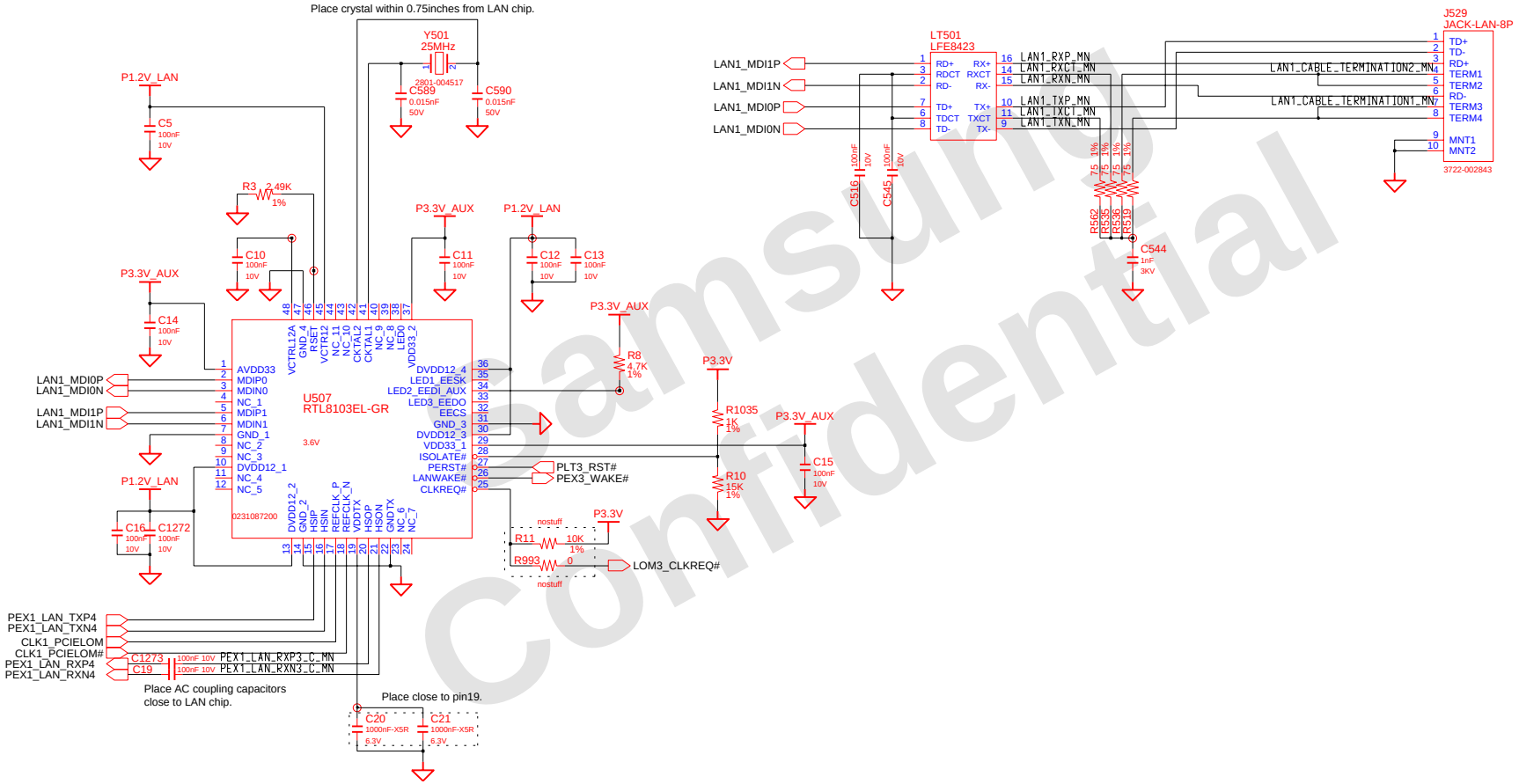
MIC JACK





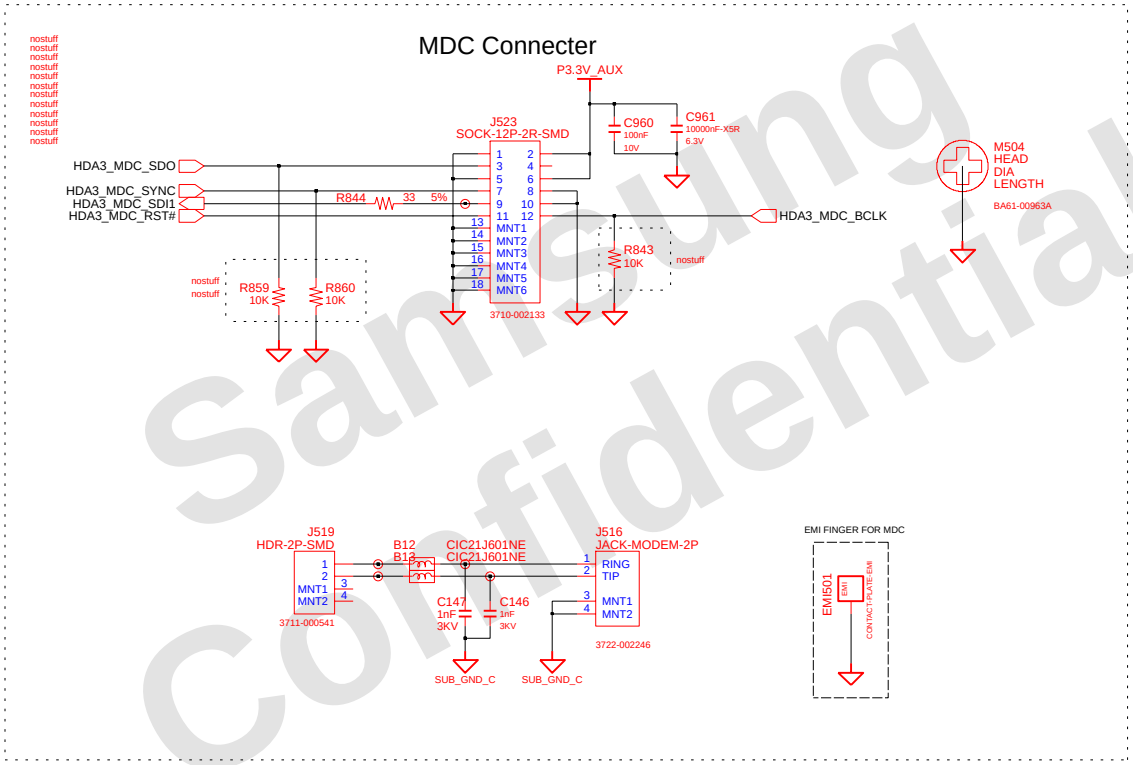
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	HDA_CODEC_ALC272	
APPROVAL: BC LEE	REV: 1.0	SPK AMP TPA6017	PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 2 OF 5	

LAN



DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L LAN_MARVELL_8055 LAN	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: undefined	

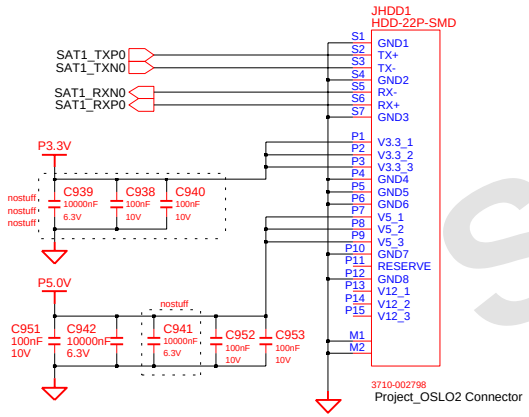
MDC



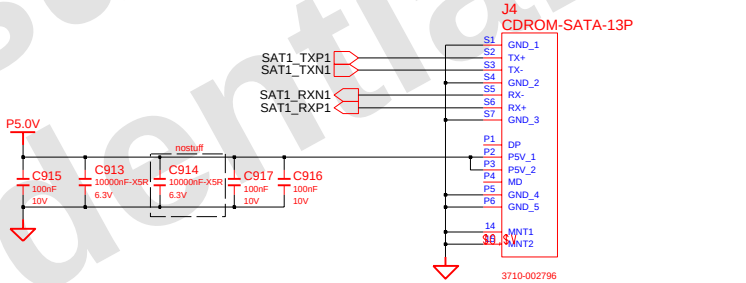
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L HDA_Modem HDA_Modem	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 1 OF 1

SATA I/F CONN

SATA HDD CONN

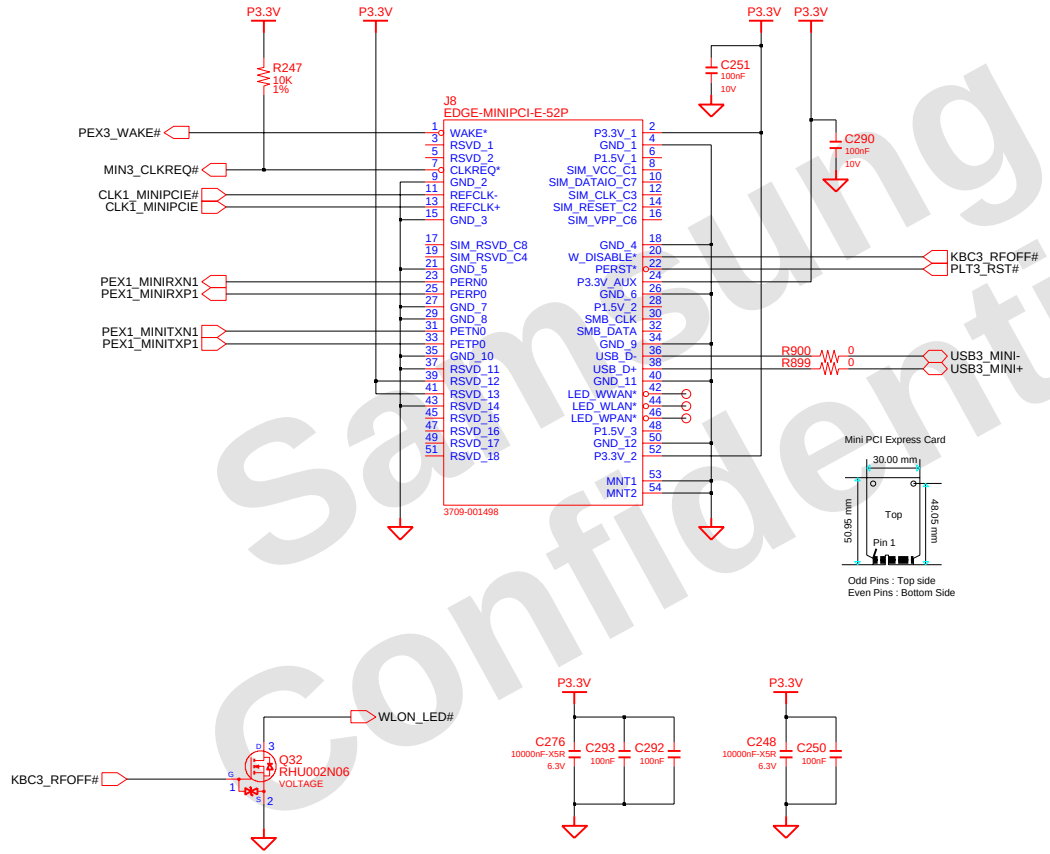


SATA ODD CONN



DESIGN: XiaoHong Zhang	DATE: 12/3/2008	TITLE: QingDao_Ext SATA_DEVICES HDD ODD	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE: undefined	LAST EDIT: December, 3, 2008 12:06:51 PM	PAGE 1 OF	

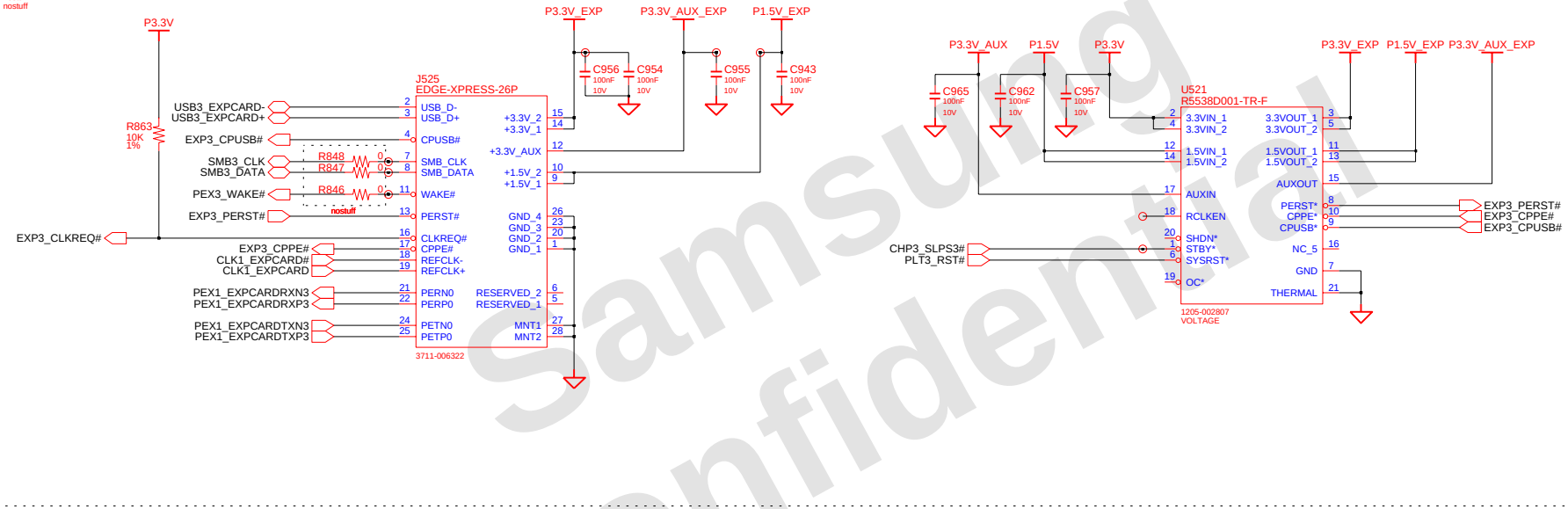
WLAN 7mm



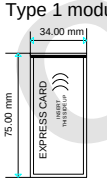
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MINI_PCIE_CONN WLAN	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF	

Express Card

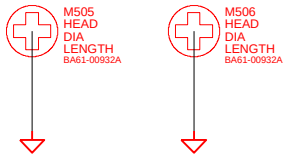
Express Card Power Switch



Type 1 module



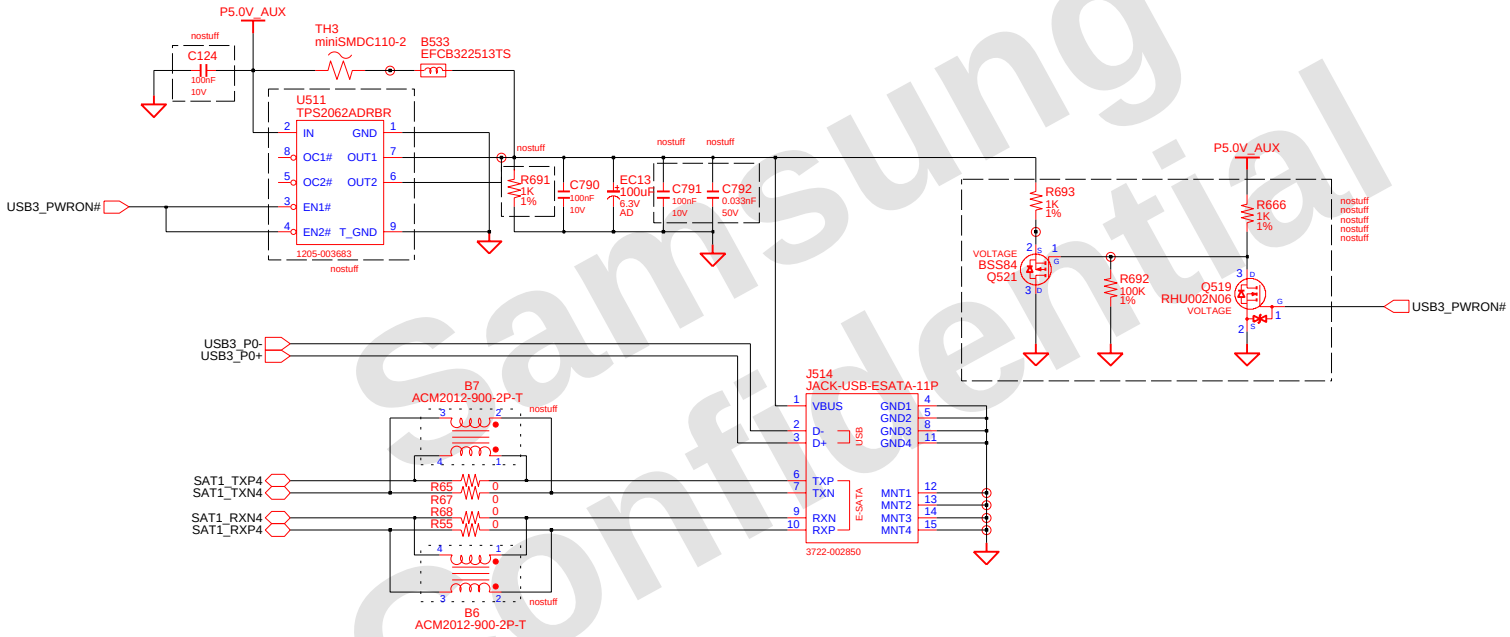
34.00 mm W
X
75.00 mm L
X
5.00 mm H



DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM		PAGE 1 OF

nostuff

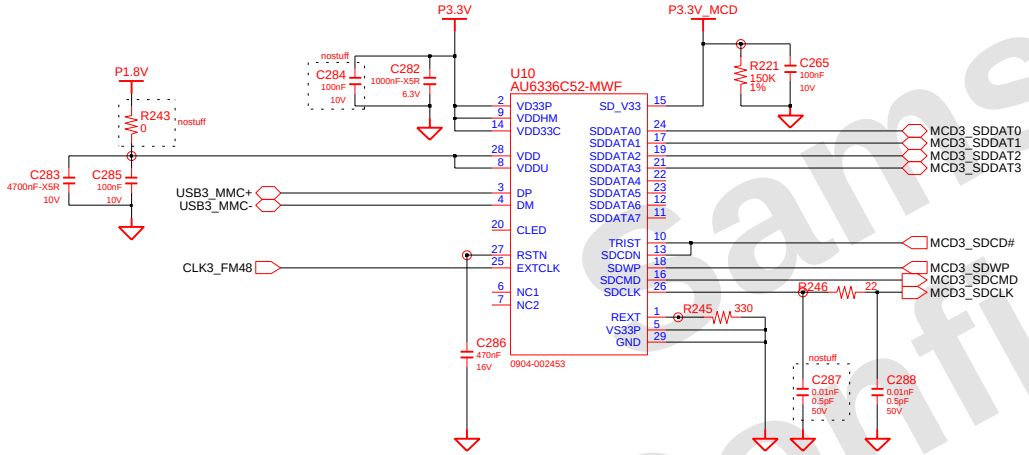
eSATA

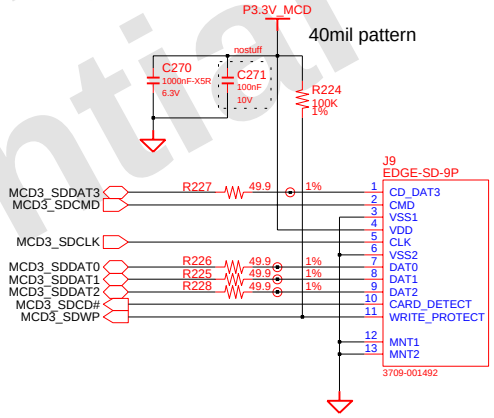


DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L / MAIN / eSATA	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 10 OF 15	

3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches





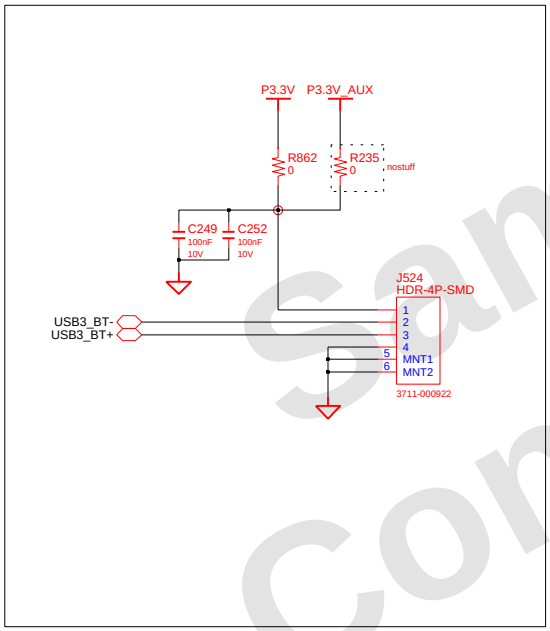
40 mil trace for medica card socket ground

MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

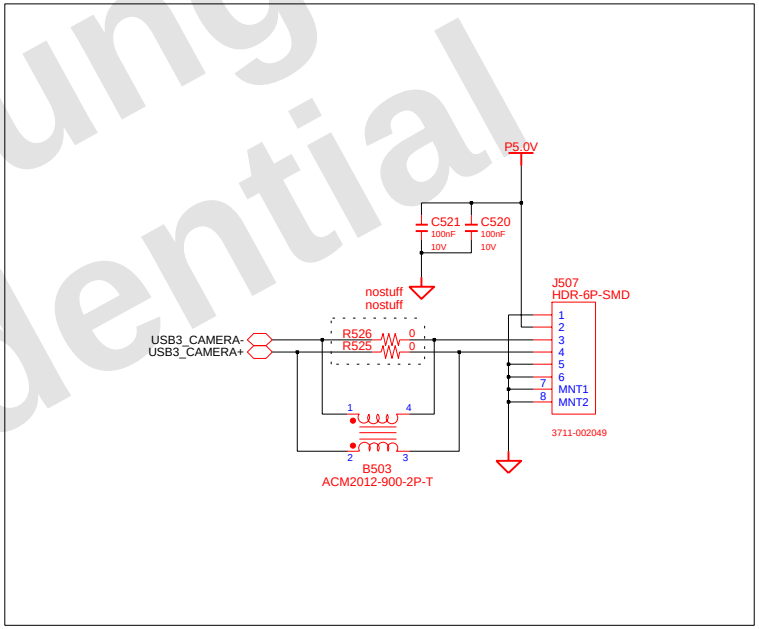
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L AU6336	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undef ined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF	

USB I/F Devices

Bluetooth Interface



CAMERA



DESIGN: XiaoHong Zhang	DATE: 12/3/2008	TITLE: QingDao_Ext USB_DEVICES BT CAMERA	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE:	LAST EDIT: December, 3, 2008 12:12:55 PM	PAGE: 1 of undefined	

USB SUB

UP

MAIN BOARD

CHP3_USBPWRON# — R534 0 (nostuff) — USB3_PWRON#
KBC3_USBPWRON# — R5 0 — USB3_PWRON#

VDC — C910 1nF 50V — P5.0V

MAIN BOARD

P5.0V_AUX — TH4 miniSMDC110-2 — B534 EFCB322513TS

C18 100nF 10V (nostuff)

U1 TPS2062ADRBR
IN, GND, OC1#, OUT1, OC2#, OUT2, EN1#, EN2#, T_GND
1205-003683 (nostuff)

Need 4A Routing

R6 1K 1% (nostuff) — C17 100nF 10V — EC3 100uF 16V AS — C1271 100nF 10V — C1277 0.033nF 50V (nostuff)

P5.0V_AUX_A

VOLTAGE BSS84 Q7 — R1036 1K 1% — R7 100K 1%

P5.0V_AUX

Q8 RHU002N06 — R1034 1K 1% (nostuff)

USB3_PWRON#

MAIN BOARD

P5.0V_AUX_A — C1275 1nF 50V — J508 HDR-6P-SMD
USB3_P6-
USB3_P6+
MNT1 MNT2
3711-002049

SUB BOARD

SUB_P5.0V_AUX_A — J510 JACK-USB-4P
SUB_USB3_P6-
SUB_USB3_P6+
PWR D- D+ GND MNT1 MNT2 MNT3 MNT4
3722-002577
SUB_GND_A

SUB BOARD

SUB_P5.0V_AUX_A — C81 1nF 50V — SUB_GND_A — J2 HDR-6P-SMD
SUB_USB3_P6-
SUB_USB3_P6+
MNT1 MNT2
3711-002049
SUB_GND_A

DOWN

MAIN BOARD

P5.0V_ALW — TH5 miniSMDC110-2 — B20 EFCB322513TS

C297 100nF 10V (nostuff)

U523 TPS2062ADRBR
IN, GND, OC1#, OUT1, OC2#, OUT2, EN1#, EN2#, T_GND
1205-003683 (nostuff)

Need 4A Routing

R912 1K 1% (nostuff) — C289 100nF 10V — EC514 100uF 16V AS — C969 100nF 10V — C970 0.033nF 50V (nostuff)

P5.0V_AUX_C

VOLTAGE BSS84 Q547 — R919 1K 1% — R914 100K 1%

P5.0V_AUX

Q548 RHU002N06 — R913 1K 1% (nostuff)

USB3_PWRON#

P5.0V_STB — R259 200K 1%
KBC5_P5ALWON# — KBC5_P5ALWON#
KBC3_USBCHG — Q31 RHU002N06

MAIN BOARD

P5.0V_AUX_C — C291 1nF 50V — J527 HDR-6P-SMD
USB3_P2-
USB3_P2+
MNT1 MNT2
3711-002049

SUB BOARD

SUB_P5.0V_AUX_C — J522 JACK-USB-4P
SUB_USB3_P2-
SUB_USB3_P2+
R810 0 — R809 0 (nostuff)
B531 ACM2012-900-2P-T
PWR D- D+ GND MNT1 MNT2 MNT3 MNT4
3722-002577
SUB_GND_C

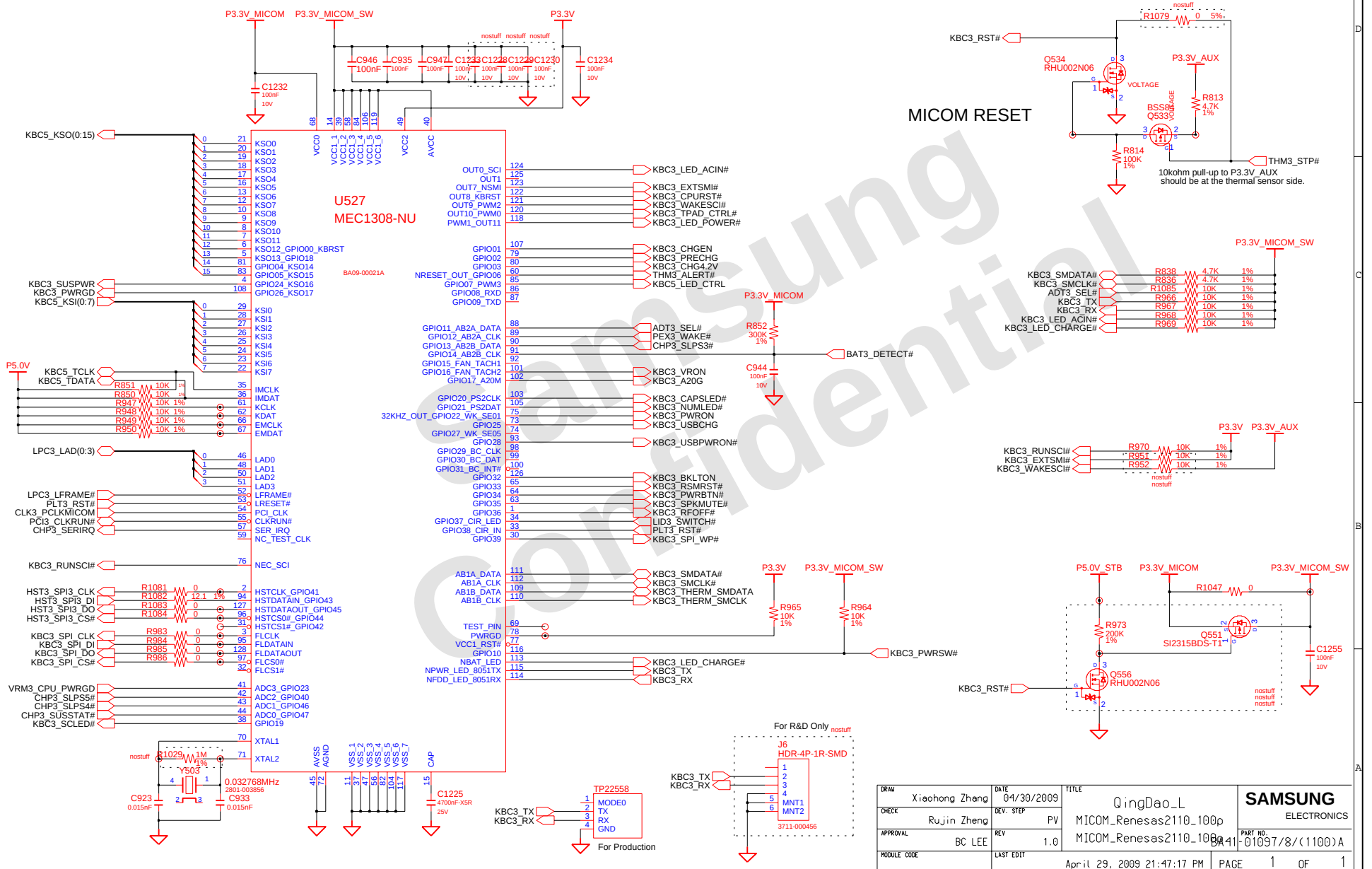
SUB BOARD

SUB_P5.0V_AUX_C — C932 1nF 50V — SUB_GND_C — J521 HDR-6P-SMD
SUB_USB3_P2-
SUB_USB3_P2+
MNT1 MNT2
3711-002049
SUB_GND_C

To RJ11 cable. (Connect with BA39-00593A)

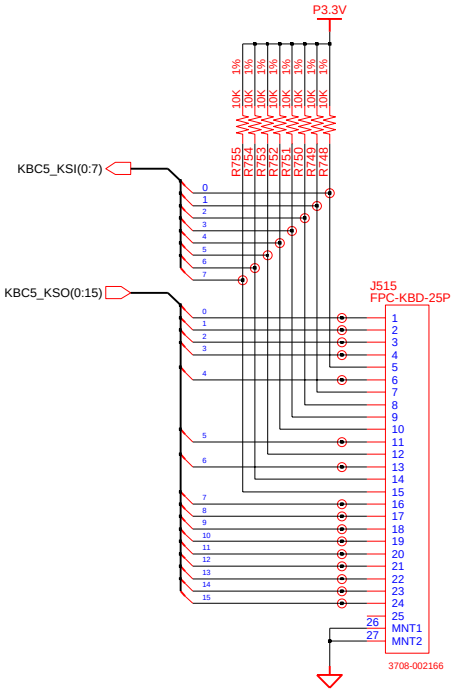
DESIGN: XiaoHong Zhang	DATE: 12/3/2008	TITLE: QingDao_Ext USB_CONN USB SUB	SAMSUNG ELECTRONICS
CHECK: RuJin Zheng	DEV. STEP: ADV1		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-xxxxxA
MODULE CODE: undef ined	LAST EDIT: December, 3, 2008 12:12:18 PM	PAGE 1 OF	

MICOM

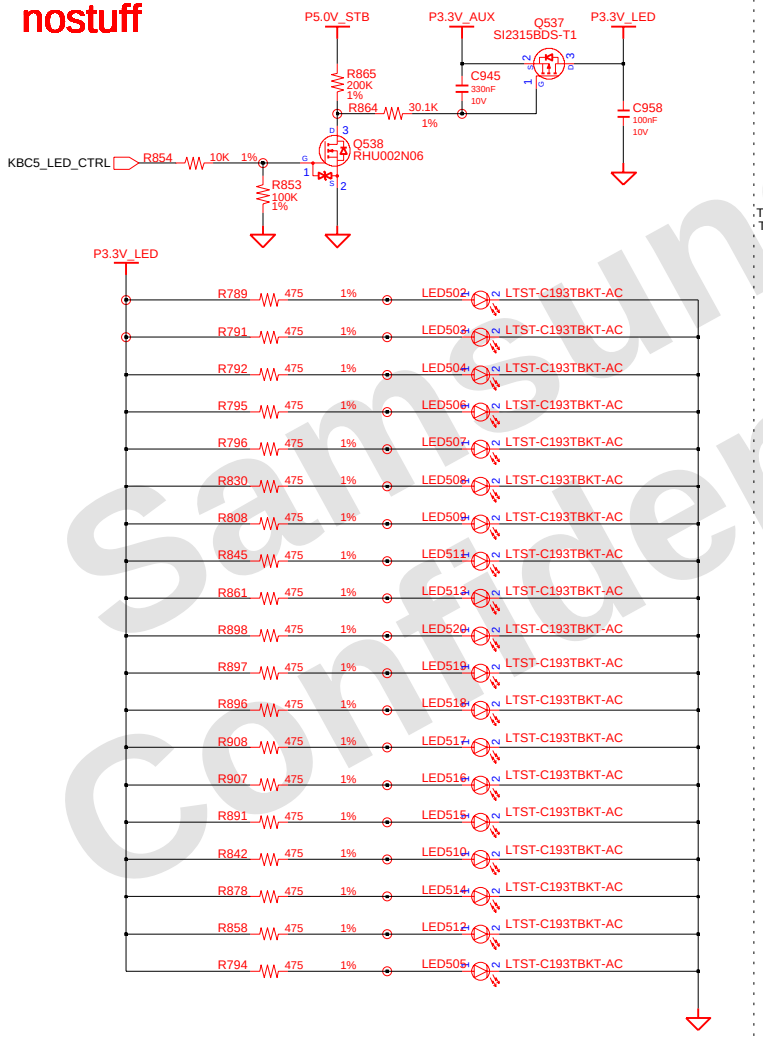


Micom Glue Logic

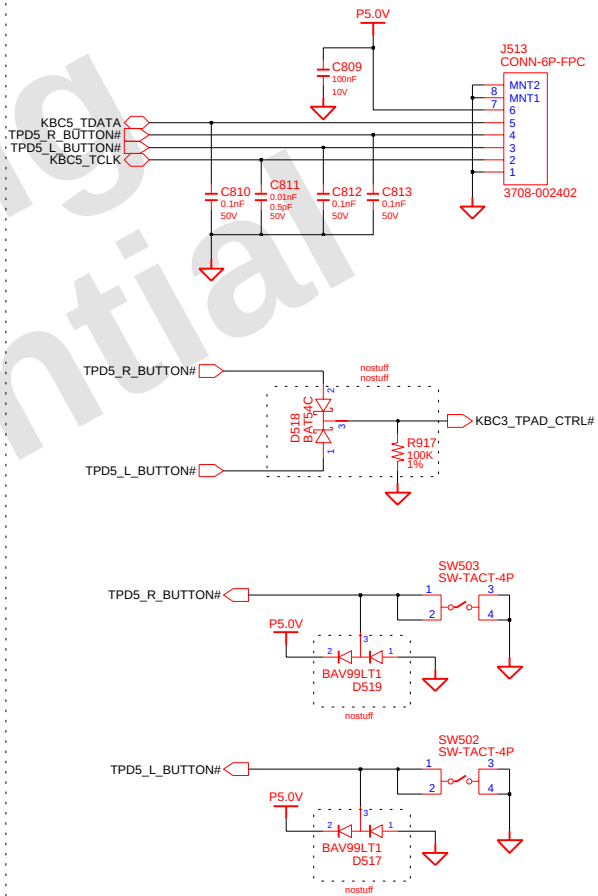
KEYBOARD



nostuff



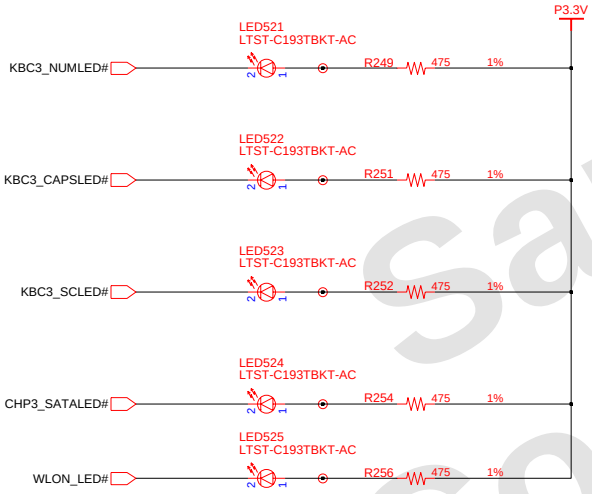
TOUCHPAD



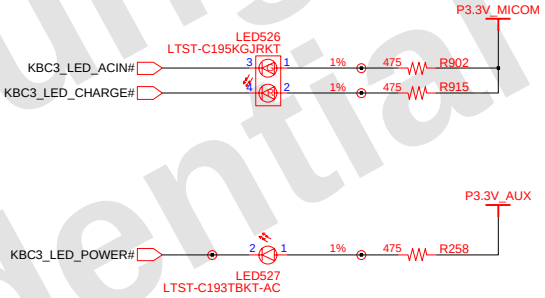
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MICOM_GLUE_LOGIC KBD TP	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE: 1 of undefined	

LED SWITCH LOGIC

Function Key LEDS



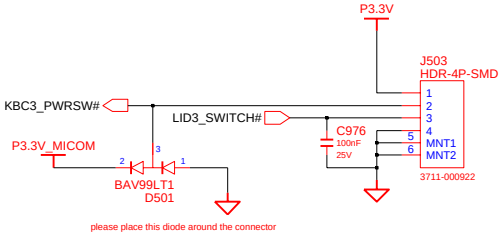
ADAPTERIN/CHARGING LED



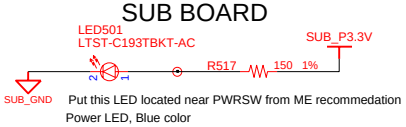
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

SUB Board

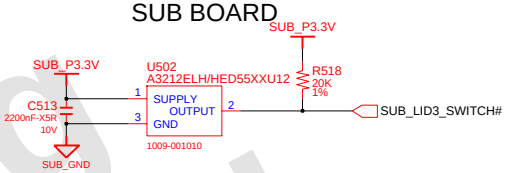
MAIN BOARD



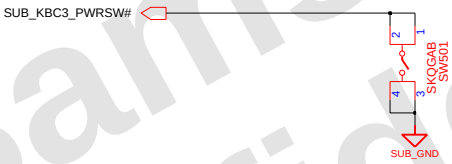
Power LED
SUB BOARD



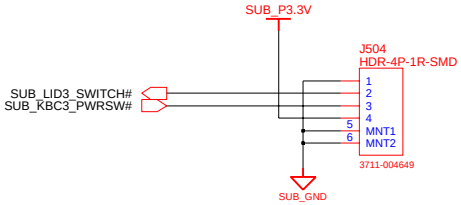
LID_SWITCH
SUB BOARD

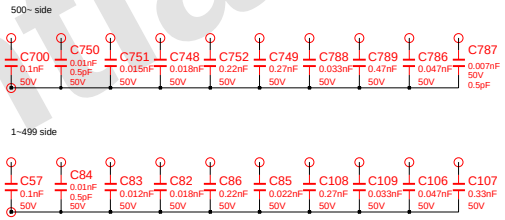


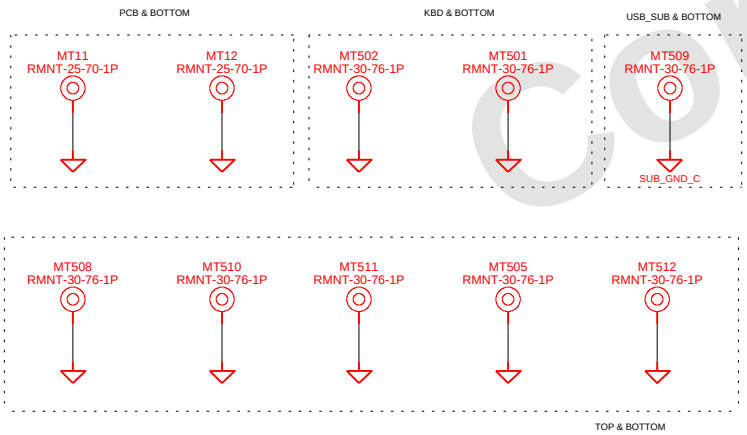
Power Switch
SUB BOARD

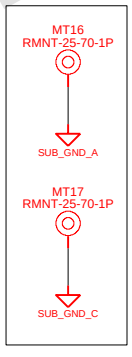


SUB BOARD

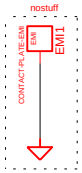








USB S/B MT

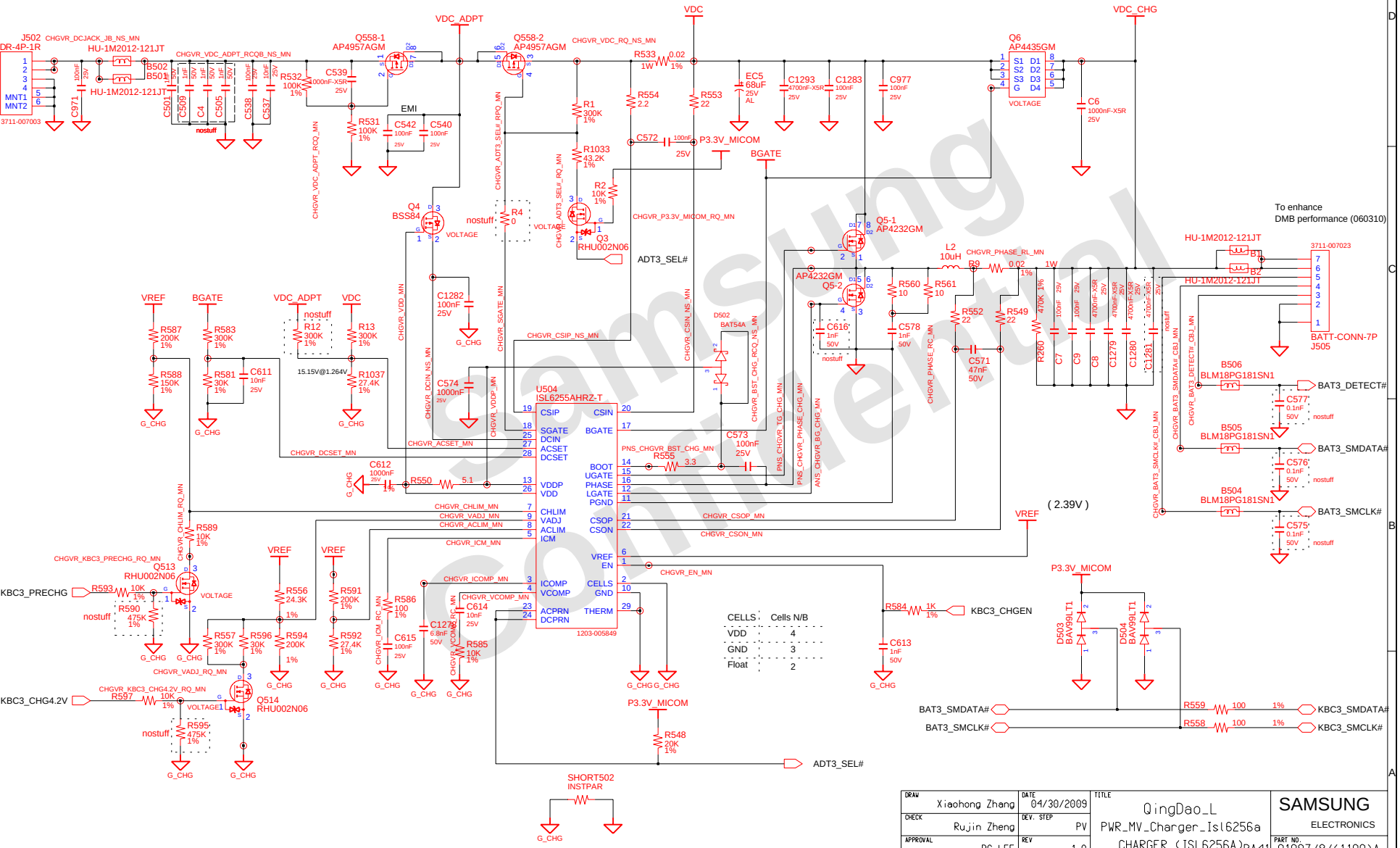


REV1

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

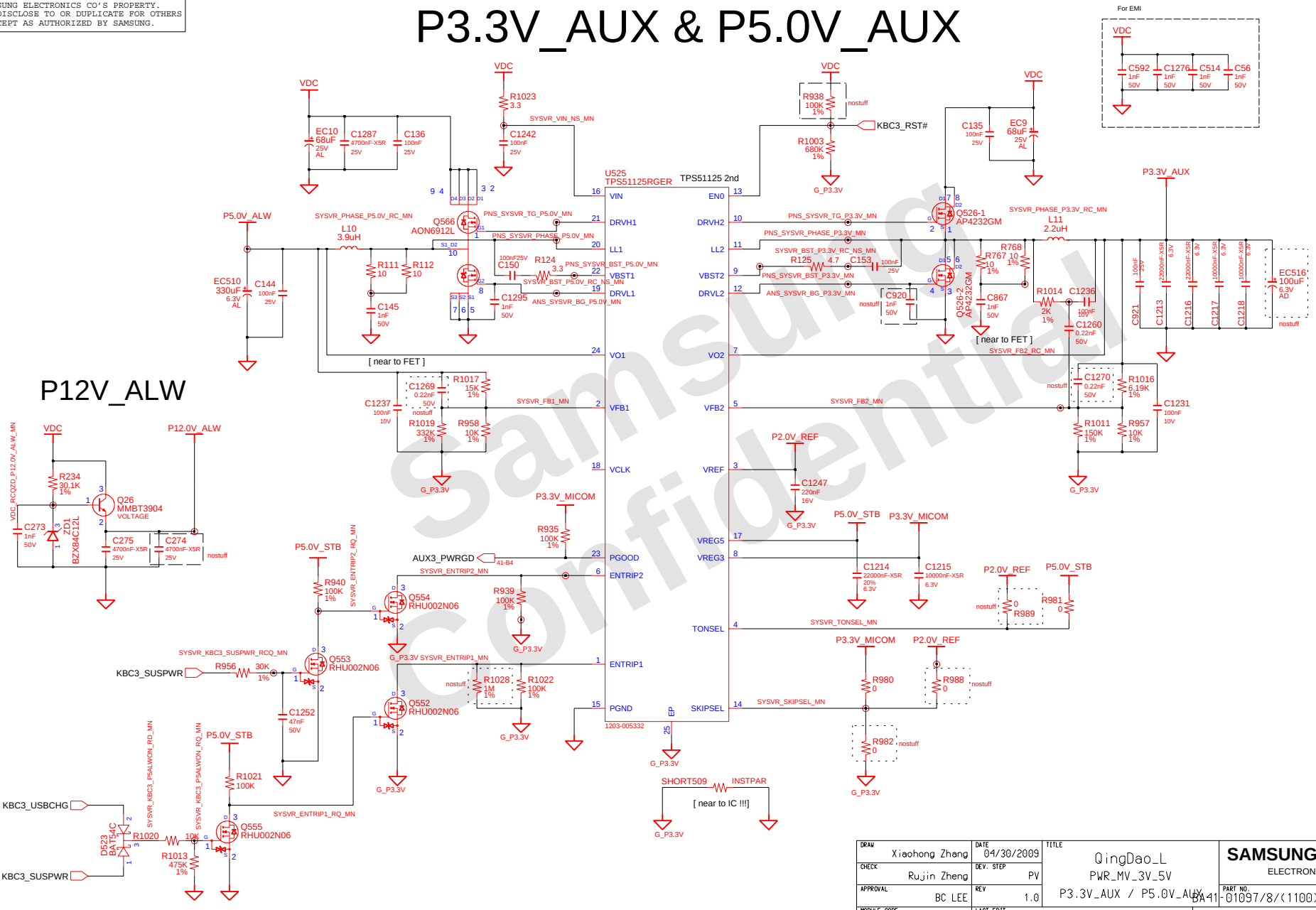
DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN PWR SW SUB	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 11 OF 15	

CHARGER & POWER MANAGEMENT



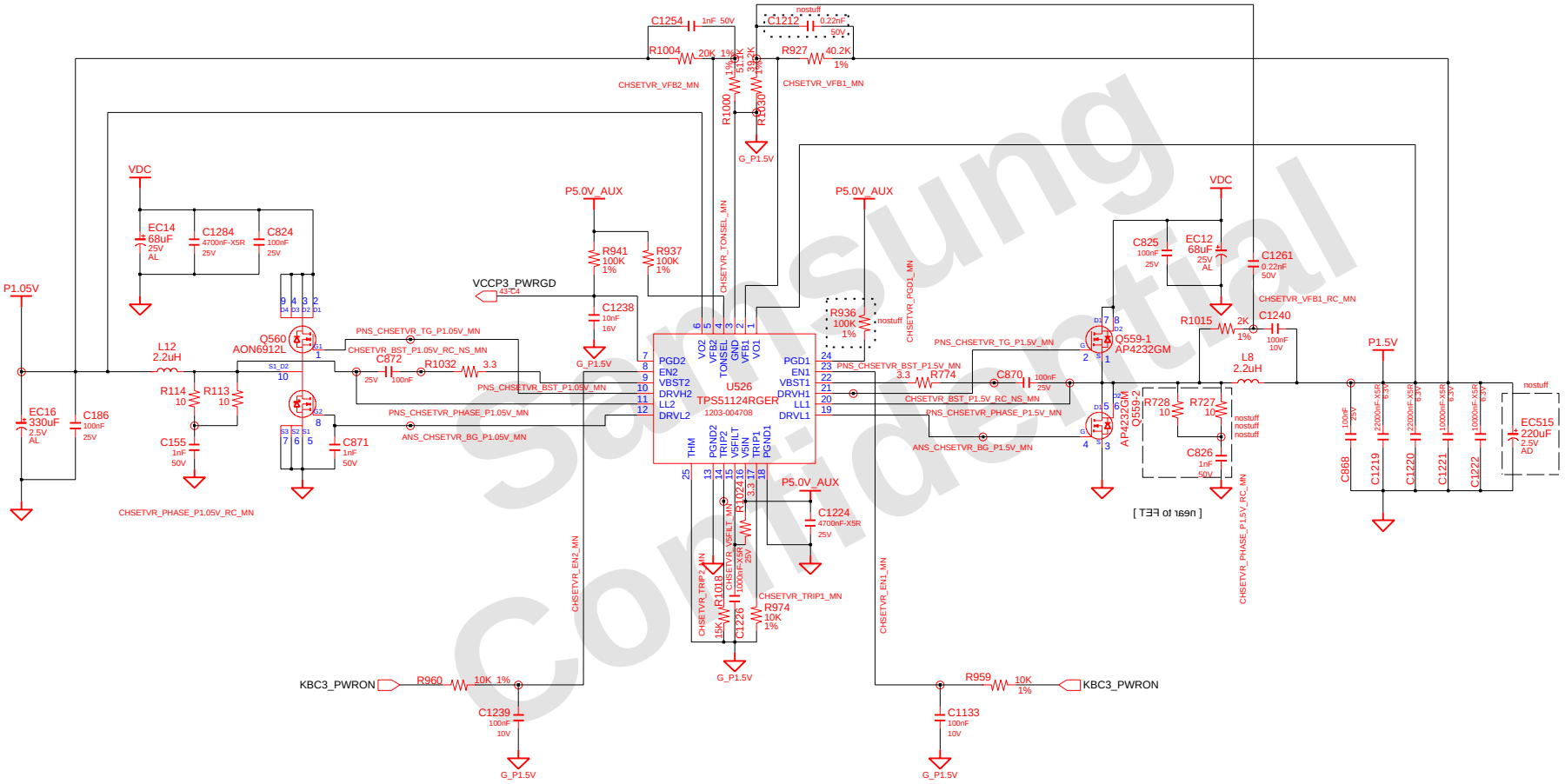
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_Charger_Isl6256a	
APPROVAL: BC LEE	REV: 1.0	CHARGER (ISL6256A) BA41-01097/8/(1100)A	PART NO.
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

P3.3V_AUX & P5.0V_AUX



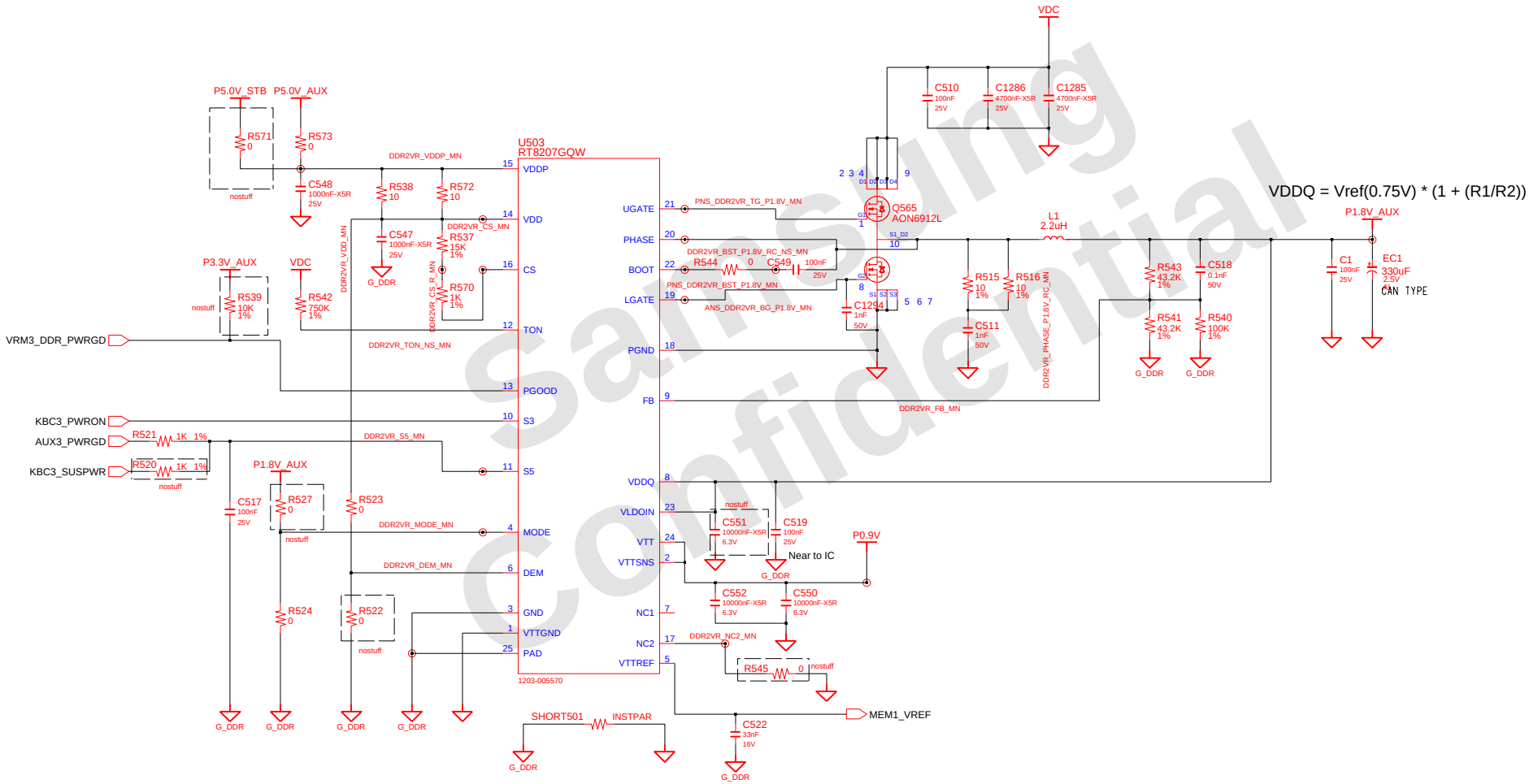
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_3V_5V	
APPROVAL: BC LEE	REV: 1.0	P3.3V_AUX / P5.0V_AUX	PART NO. BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

1.05V & P1.5V



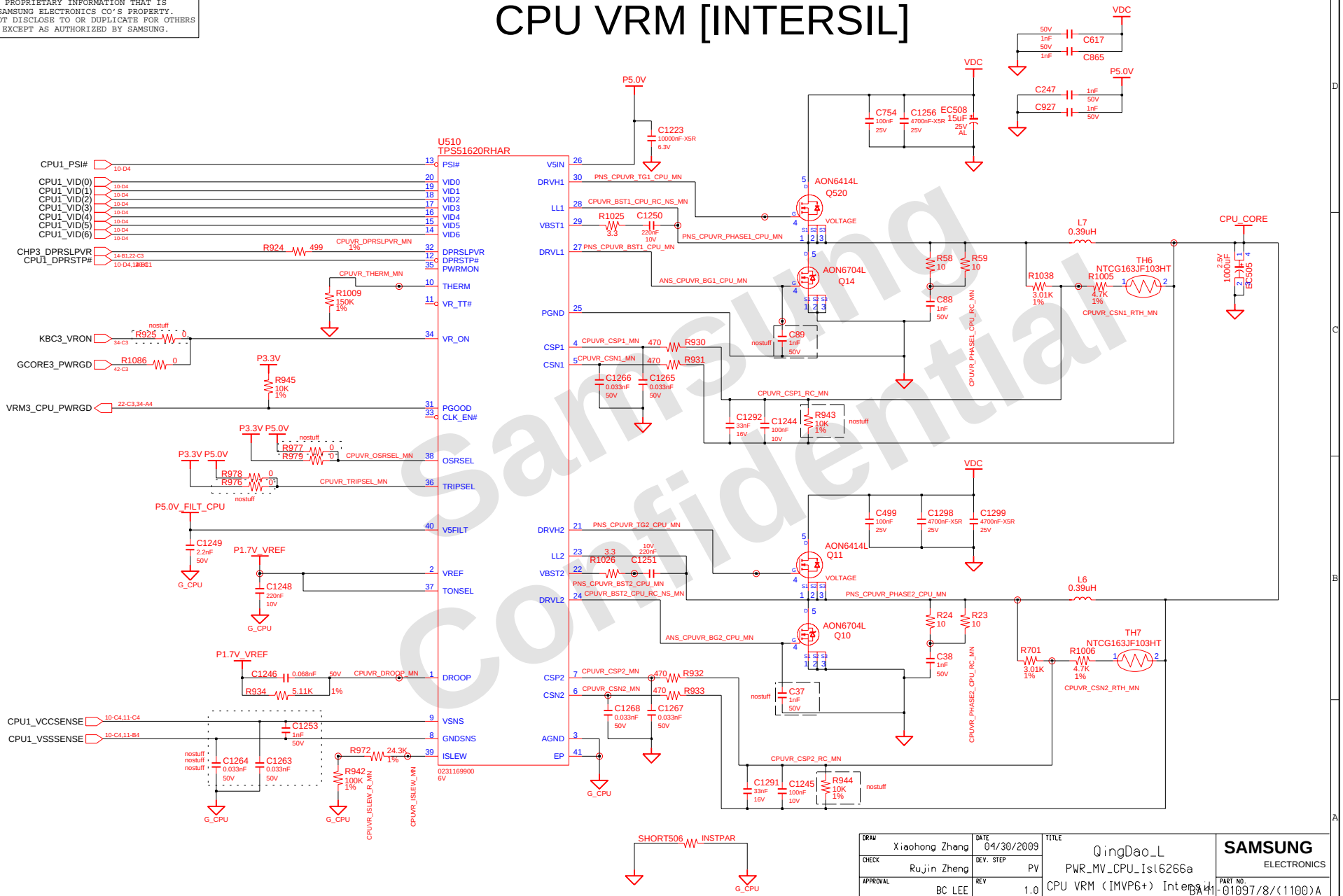
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L PWR_MV_Cantiga Chipset Power	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

DDR2 Power



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L PWR_MV_MeMory DDR3 POWER (P1.5V_AUX)	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

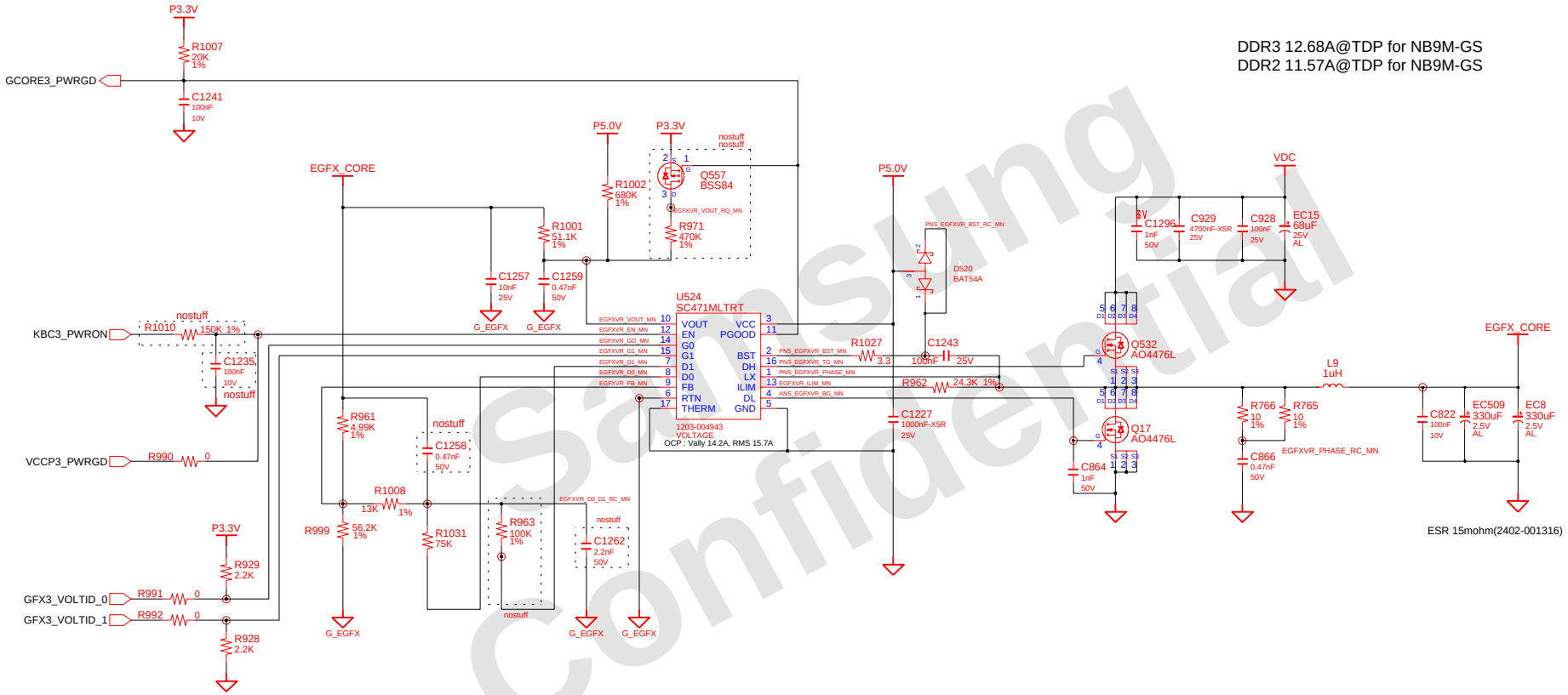
CPU VRM [INTERSIL]



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_MV_CPU_Isl6266a	
APPROVAL: BC LEE	REV: 1.0	CPU VRM (IMVP6+) Intersil	PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

Graphic Core Power

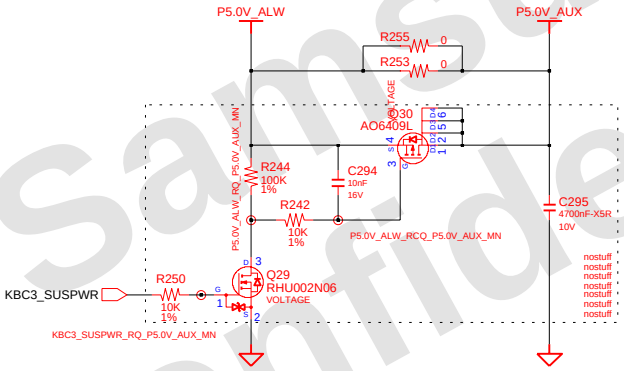
DDR3 12.68A@TDP for NB9M-GS
DDR2 11.57A@TDP for NB9M-GS



GFX3_VOLTID		
G0	G1	
0	0	0.8V(0.8166V)
1	0	0.85V(0.8591V)
0	1	RESERVE
1	1	RESERVE

DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV	PWR_Gfx_MV_Ext	
APPROVAL: BC LEE	REV: 1.0	Ext Gfx Memory(SC486)	PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

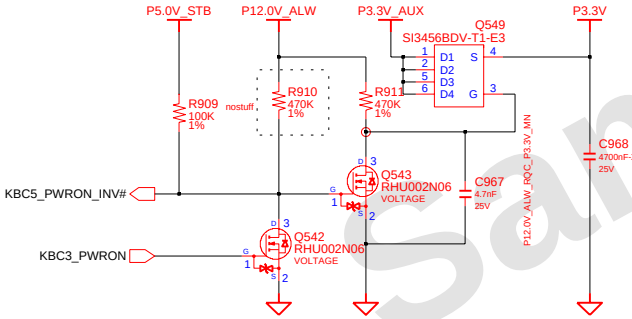
Switched Power



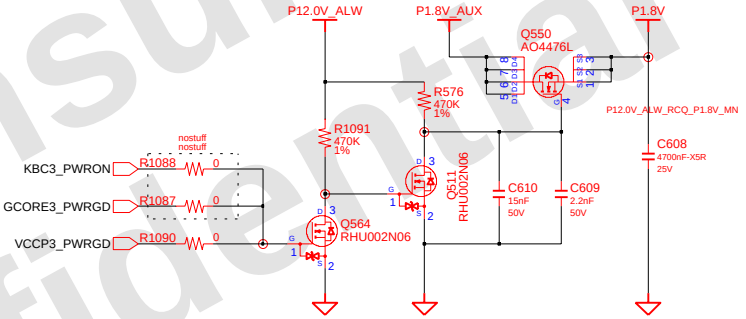
DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L PWR_MV_Switched SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE:	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 2	

Switched Power

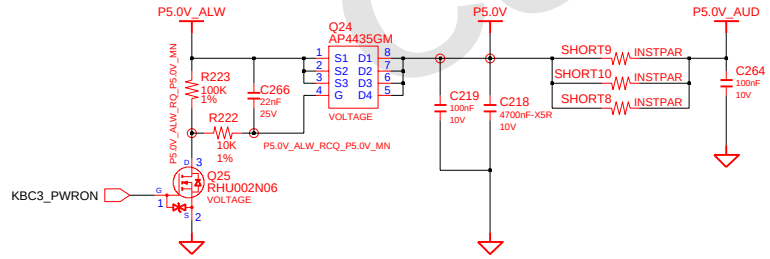
Switched Power On (P3.3V)



Switched Power On (P1.8V)

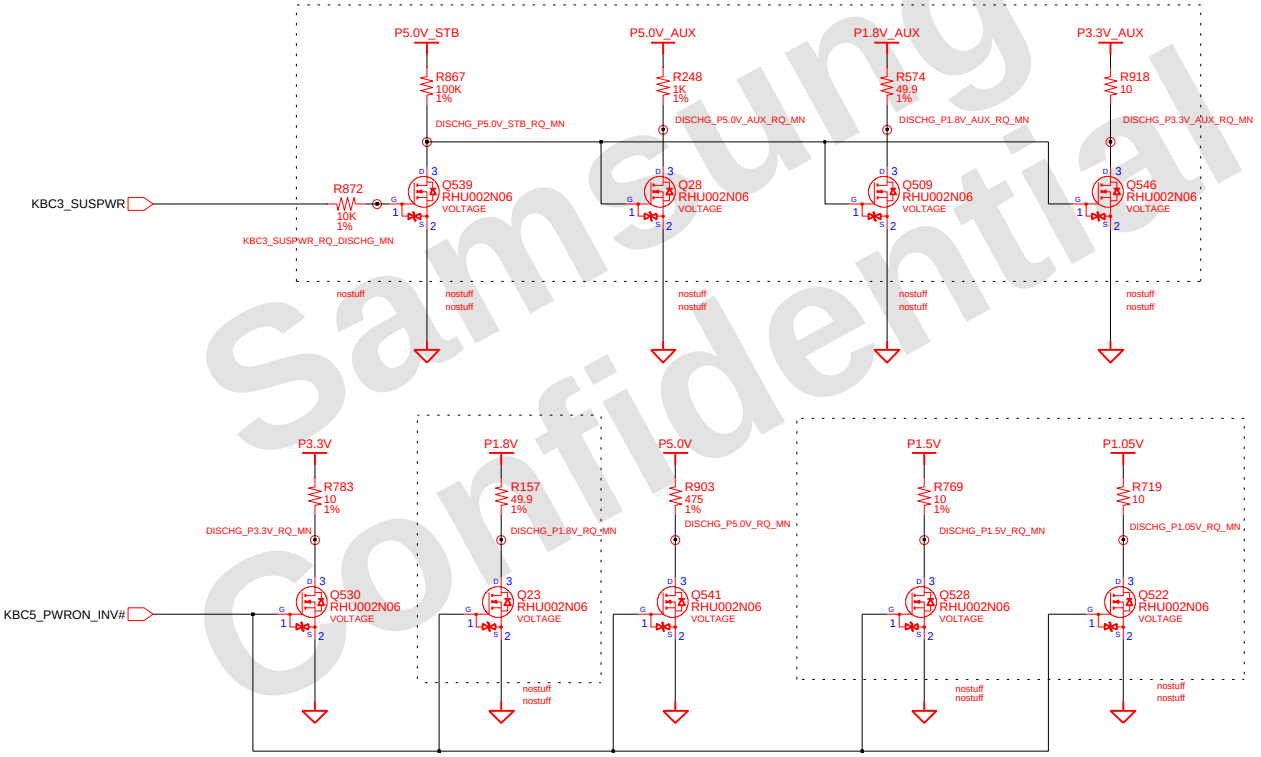


Switched Power On (P5.0V)



DESIGN: XIAOHONG, ZHANG	DATE: 12/3/2008	TITLE: QingDao_Ext PWR_MV_SWITCHED Switched Power	SAMSUNG ELECTRONICS
CHECK: RUJIN, ZHENG	DEV. STEP: ADV1		PART NO.: BA41-xxxxxA
APPROVAL: BC, LEE	REV: 1.0		
MODULE CODE	LAST EDIT: December, 3, 2008 3:39:16 PM	PAGE 2 OF	

POWER DISCHARGER



DRAW: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L PWR_MV_DisCharger DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE: undefined	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 1 OF 1	

- CPU1_NMI
- CPU1_TCK
- CPU1_TDI
- CPU1_TMS
- FAN5_VDD
- SMB3_CLK

- ADT3_SEL#
- CLK3_FM48
- CPU1_ADS#
- CPU1_BNR#
- CPU1_HIT#
- CPU1_INTR
- CPU1_PSI#

- CPU1_SMI#
- GFX3_HCLK
- KBC3_A20G

- KBC3_VRON
- KBC5_TCLK
- LCD3_BRIT
- MCD3_SDWP
- MEM1_VREF
- PLT3_RST#
- SMB3_DATA

- THM3_STP#
- WLON_LED#
- AUX3_PWRGD
- CLK3_ICH14
- CLK3_PWRGD
- CLK3_USB48
- CPU1_A20M#
- CPU1_BPRI#
- CPU1_BREQ#
- CPU1_DBSY#
- CPU1_DPWR#
- CPU1_DRDY#
- CPU1_FERR#

- CPU1_INIT#
- CPU1_LOCK#
- CPU1_TRDY#
- CPU1_TRST#
- CRT3_HSYNC
- CRT3_VSYNC
- CRT5_HSYNC
- CRT5_VSYNC
- DRAM_RST#
- EXP3_CPPE#
- GFX3_HDATA
- GFX3_ROMSI
- GFX3_ROMSO
- KBC3_CHGEN
- KBC3_PWRGD
- KBC3_PWRON
- KBC5_TDATA

- MCD3_SDCD#
- MCD3_SDCLK
- MCD3_SDCMD
- MCH1_HVREF
- PCI3_INTA#
- PCI3_INTB#
- PCI3_INTC#
- PCI3_INTD#
- PCI3_IRDY#
- PCI3_PERR#

- PCI3_SERR#
- PCI3_STOP#
- PCI3_TRDY#
- PEX3_WAKE#
- BAT3_SMCLK#
- CHP3_GPIO18
- CHP3_GPIO20
- CHP3_SERIRQ
- CHP3_SLPS4#
- CHP3_SLPS5#

- CLK3_DBGLPC

- CPU1_DPSLP#
- CPU1_IGNNE#
- CPU1_VID(0)
- CPU1_VID(1)
- CPU1_VID(2)
- CPU1_VID(3)
- CPU1_VID(4)
- CPU1_VID(5)
- CPU1_VID(6)
- CRT3_DDCCLK
- CRT5_DDCCLK
- EXP3_CPUSB#
- EXP3_PERST#

- GFX3_STRAP2

- KBC3_BKLTON
- KBC3_PRECHG
- KBC3_PWRSW#
- KBC3_RFOFF#
- KBC3_SCLED#
- KBC3_SMCLK#
- KBC3_SUSPWR
- LCD3_BKLTON
- LPC3_LAD(0)
- LPC3_LAD(1)
- LPC3_LAD(2)
- LPC3_LAD(3)
- MCD3_SDDAT0
- MCD3_SDDAT1
- MCD3_SDDAT2
- MCD3_SDDAT3

- PCI3_FRAME#
- PCI3_PLOCK#
- PEG3_BKLTEN
- SMB3_ALERT#
- THM3_ALERT#
- USB3_PWRON#
- VCCP3_PWRGD
- BAT3_DETECT#
- BAT3_SMDATA#
- CHP3_BIOSWP#
- CHP3_CPUSTP#
- CHP3_PCISTP#
- CLK3_GFX_27M
- CLK3_PCLKICH
- CPU1_DPRSTP#
- CPU1_DSTBN0#

- CPU2_THERMDA
- CPU2_THERMDC
- CRT3_DDCDATA
- CRT5_DDCDATA
- EXP3_CLKREQ#
- FAN3_FDBACK#
- GCORE3_PWRGD

- GFX3_ROMSCLK
- GFX3_THERMDN
- GFX3_THERMDP
- HDA3_MDC_SDO
- KBC3_CHG4.2V
- KBC3_CPURST#
- KBC3_EXTSMI#
- KBC3_NUMLED#

- KBC3_PWRBTN#
- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
- KBC3_SPKMUTE#
- LID3_SWITCH#
- LOM3_CLKREQ#
- LPC3_LFRAME#
- MCH1_HXSWING
- MCH3_CLKREQ#
- MCH3_EXTTS0#
- MCH3_EXTTS1#
- MIN3_CLKREQ#
- PCI3_CLKRUN#
- PCI3_DEVSEL#
- CHP3_CL_CLK_0
- CHP3_DPRSLPVR
- CHP3_PM_SYNC#
- CHP3_SATALED#
- CHP3_SUSSTAT#
- CPU1_PWRGDCPU
- CPU1_VCCSENSE
- CPU1_VSSSENSE

- GFX3_VOLTID_0
- GFX3_VOLTID_1

- HDA3_MDC_BCLK
- HDA3_MDC_RST#
- HDA3_MDC_SDI1
- HDA3_MDC_SYNC
- KBC3_CAPSLED#
- KBC5_LED_CTRL
- KBC3_WAKESCI#
- KBC5_PSALWON#
- LCD3_EDID_CLK
- MCH3_ICHSYNC#
- PEG3_HDMI_CLK
- PEG3_HPD_HDMI
- PEG3_LCDVDDON
- PEG5_HDMI_CLK

- CHP3_BIOS_CRI#
- CHP3_CL_DATA_0
- CHP3_CL_RST_0#
- CHP3_INTRUDER#
- CHP3_USBPWRON#
- CLK3_PCLKMICOM
- CPU1_THRMTRIP#
- CPU3_THRMTRIP#

- ITP3_DBRRESET#

- KBC3_LED_ACIN#
- KBC3_USBPWRON#
- LCD3_EDID_DATA
- PEG3_HDMI_DATA
- PEG5_HDMI_DATA
- TPD5_L_BUTTON#
- TPD5_R_BUTTON#
- VRM3_CPU_PWRGD
- VRM3_DDR_PWRGD
- CHP3_ME_RTCRST#
- CLK3_GFX_27M_SS

- KBC5_PWRON_INV#

- CHP3_SATACLKREQ#
- KBC3_LED_CHARGE#
- KBC3_THERM_SMCLK
- SUB_LID3_SWITCH#

- KBC3_THERM_SMDATA

- P3.3V_MICOM

- SUB_GND

- SUB_GND_A

- SUB_GND_C

- SUB_P3.3V

- P5.0V_AUX

DESIGN: Xiaohong Zhang	DATE: 04/30/2009	TITLE: QingDao_L MAIN TP	SAMSUNG ELECTRONICS
CHECK: Rujin Zheng	DEV. STEP: PV		
APPROVAL: BC LEE	REV: 1.0		PART NO.: BA41-01097/8/(1100)A
MODULE CODE	LAST EDIT: April 29, 2009 21:47:17 PM	PAGE 12 OF 15	

- HDMI3_APD
- HDMI3_PEQ
- HDMI3_PRE
- AUD5_MIC2_INT
- HDA3_AUD_SDO
- CPU1_BSEL0
- CPU1_BSEL1
- CPU1_BSEL2
- CPU1_HITM#

- HDMI3_ASQ1
- HDMI3_EMI0
- HDMI3_EMI1

- GFX3_THERM#
- KBC3_SPI_DI
- KBC3_SPI_DO
- KBC3_USBCHG
- CPU1_STPCLK#
- HDMI3_DDCBUF
- HST3_SPI3_DI
- HST3_SPI3_DO
- KBC3_SPI_CLK
- KBC3_SPI_CS#
- KBC3_SPI_WP#

- HDA3_AUD_BCLK
- HDA3_AUD_SDI0
- HDA3_AUD_SYNC
- HST3_SPI3_CLK
- HST3_SPI3_CS#
- VGA5_HDMI_HPD
- AUD5_HP_O_LEFT
- AUD5_MIC1_LEFT
- AUD5_HP_O_RIGHT
- AUD5_MIC1_RIGHT
- KBC3_TPAD_CTRL#