

# PRAHA (SRI)

CPU : Intel Merom (800MHz)  
 Chip Set : RS600ME & SB600  
 Remarks : Mobility Platform

Model Name : PRAHA  
 PBA Name : MAIN  
 PCB Code : TPT : BA41-00791A  
                   GCE : BA41-00792A  
                   NAN : BA41-00811A  
 Dev. Step : MP1.0 (8-Layer)  
 Revision : 1.0  
 T.R. Date : 2007.07.02

DRAW	CHECK	APPROVAL

■ Owner : SEC Mobile R & D      Signature :      X

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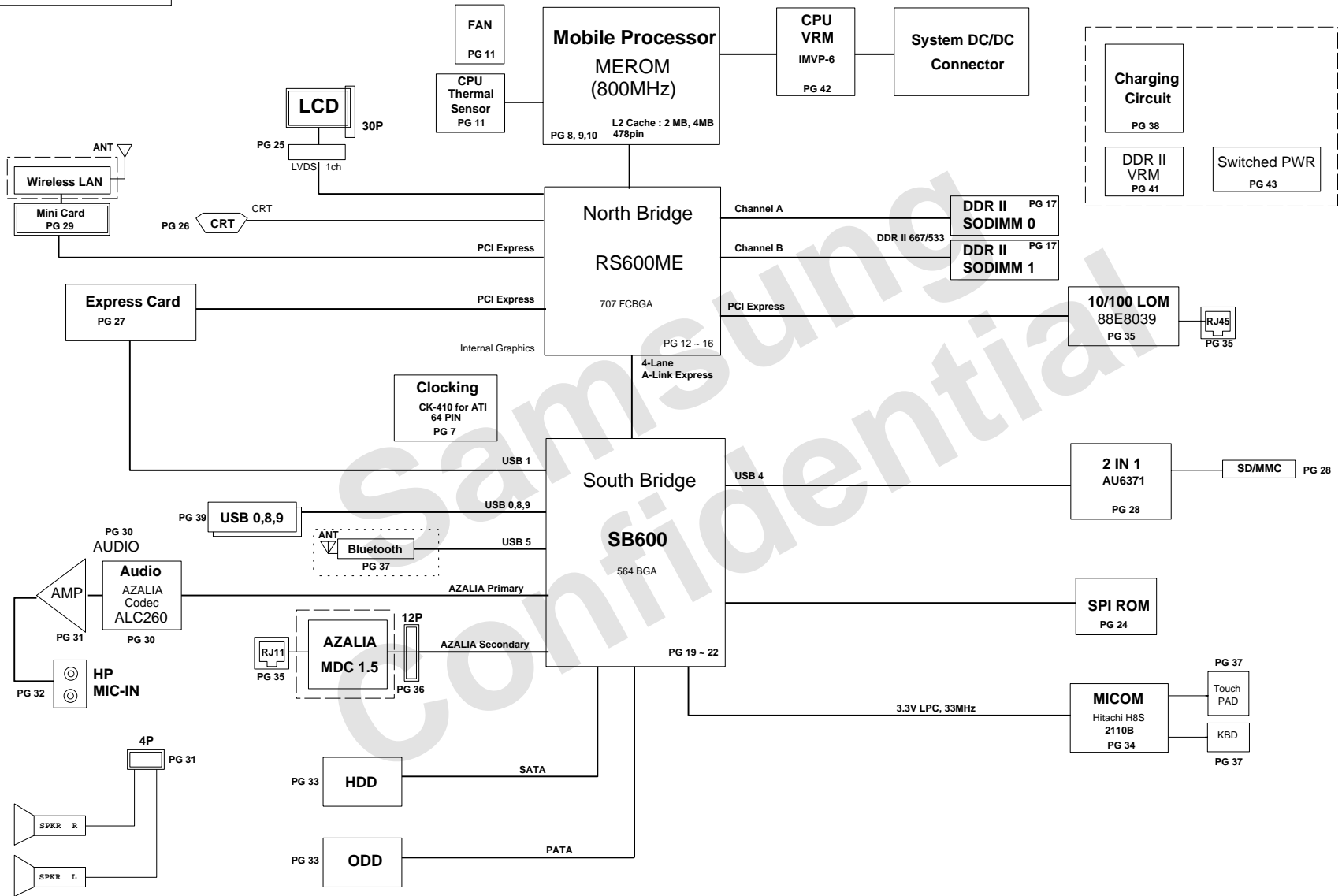
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**USE ICT PORT**

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	COVER	PART NO.	
APPROVAL	SJ PARK	REV	1.0		BA41-00791A	
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	1 OF 47	

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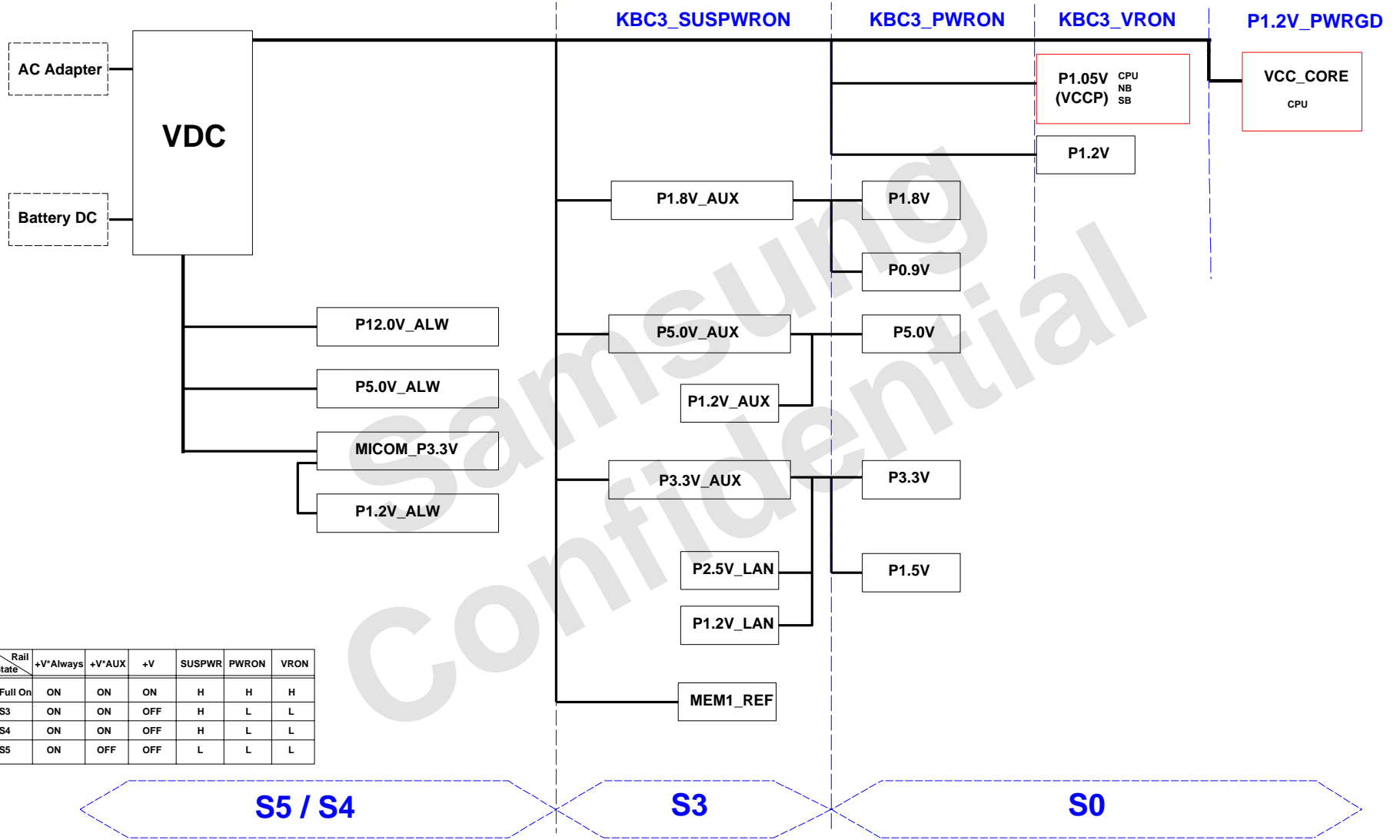
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CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	OPERATION BLOCK DIAGRAM	PART NO.	BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	2	OF 47

# Power Diagram

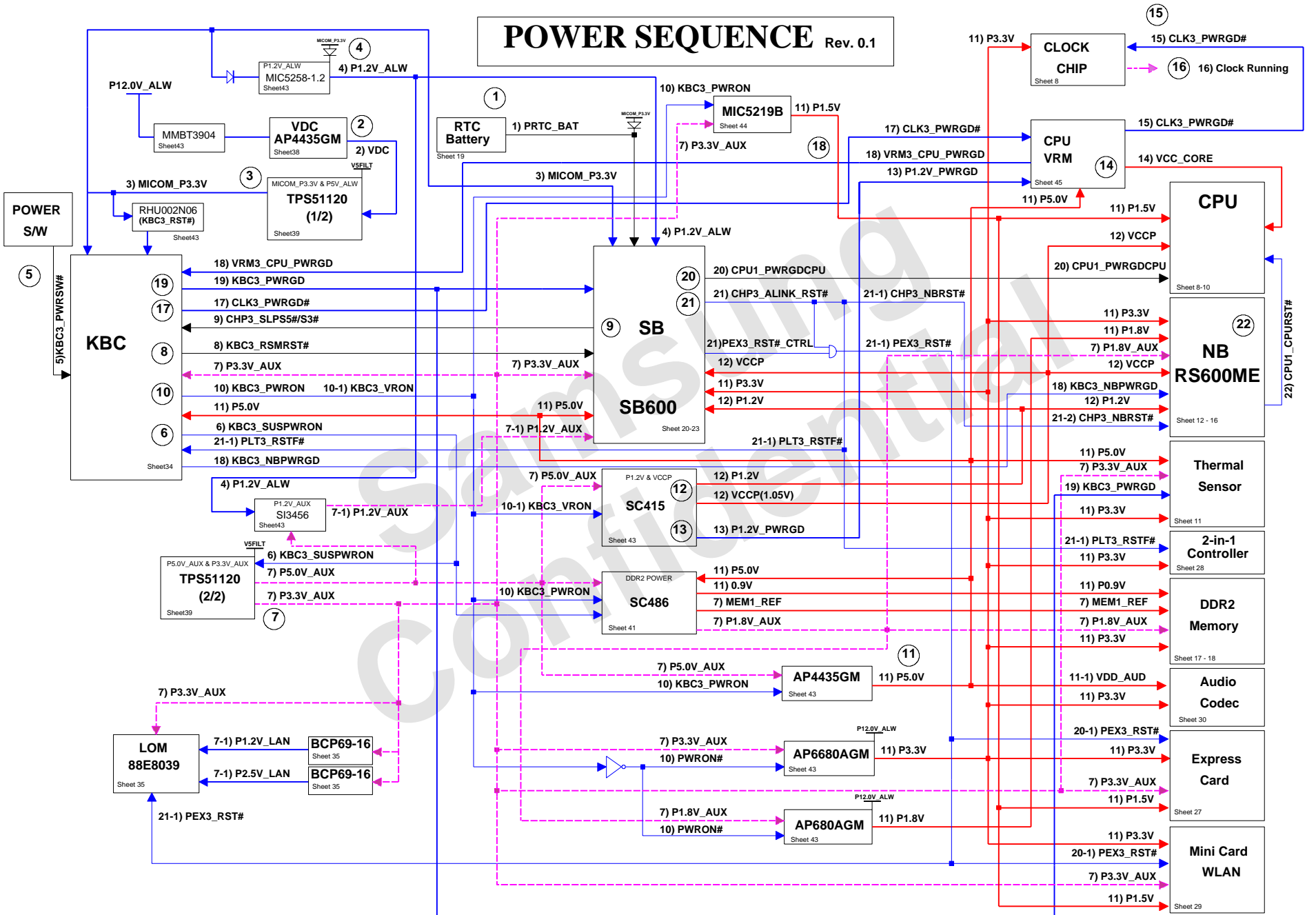
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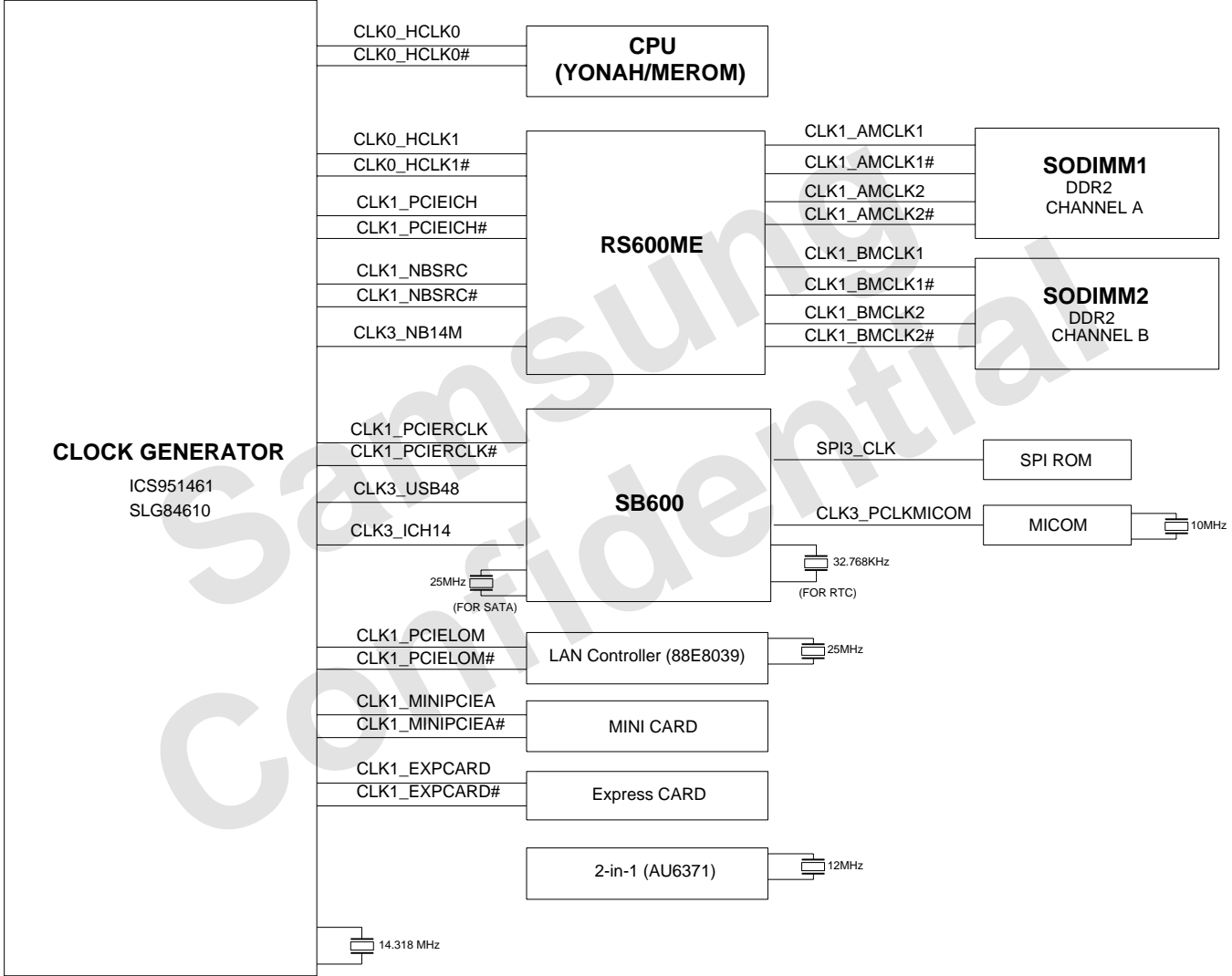
Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN	BA41-00791A	
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# POWER SEQUENCE Rev. 0.1



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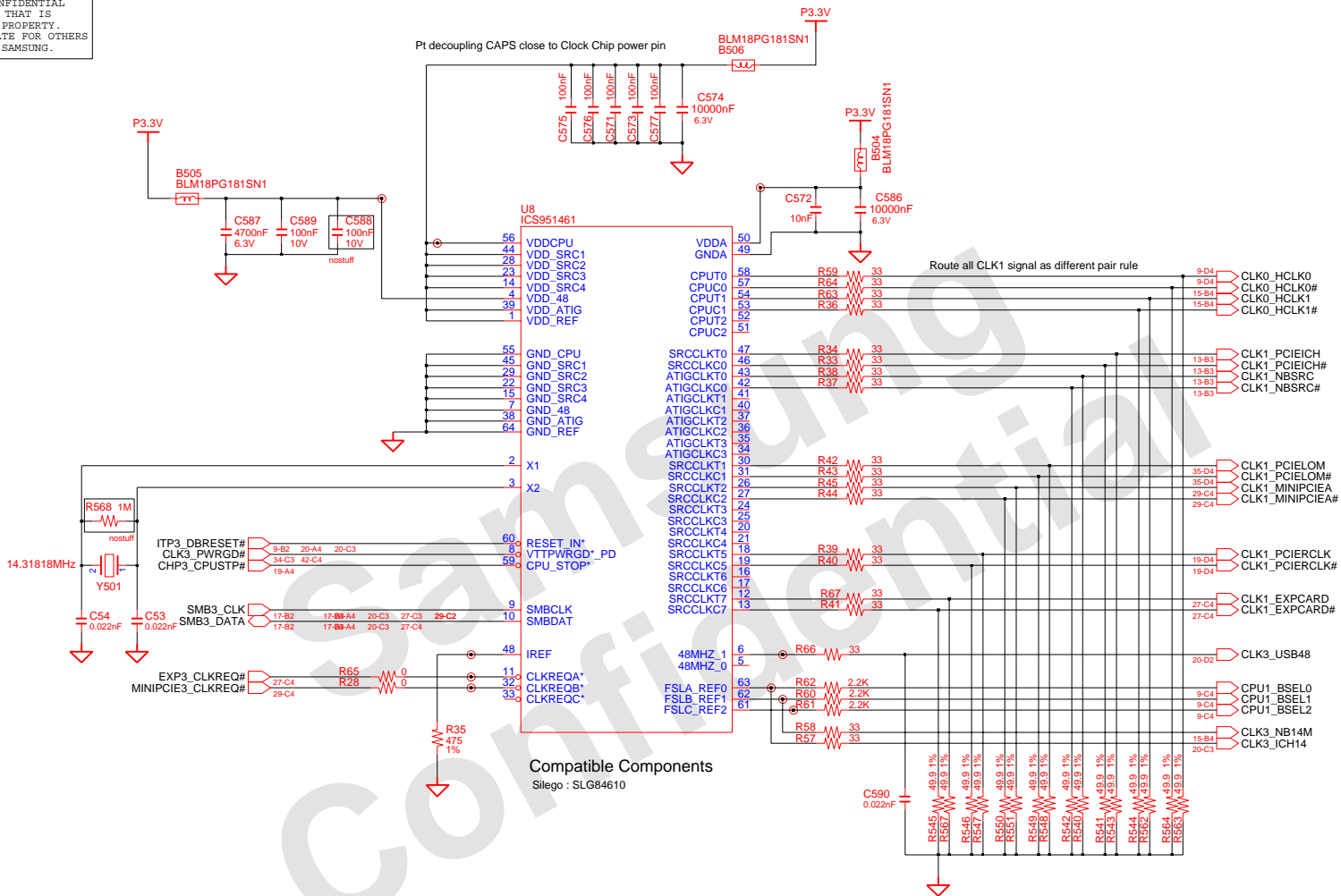


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APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	5	OF 47



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**Compatible Components**  
Silago : SLG84610

Place all the series termination resistor as close as Clock Chip as possible

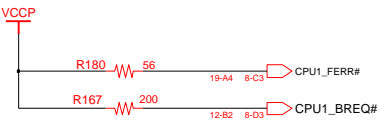
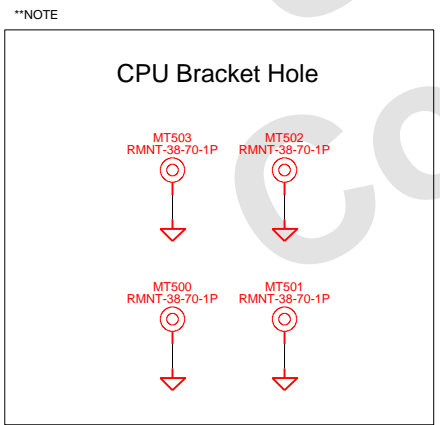
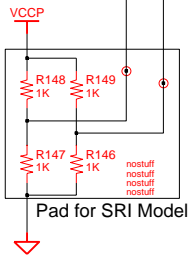
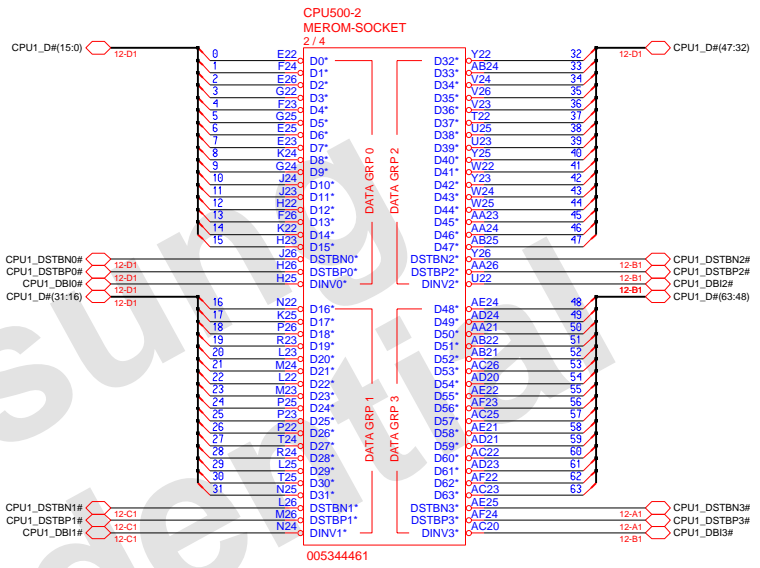
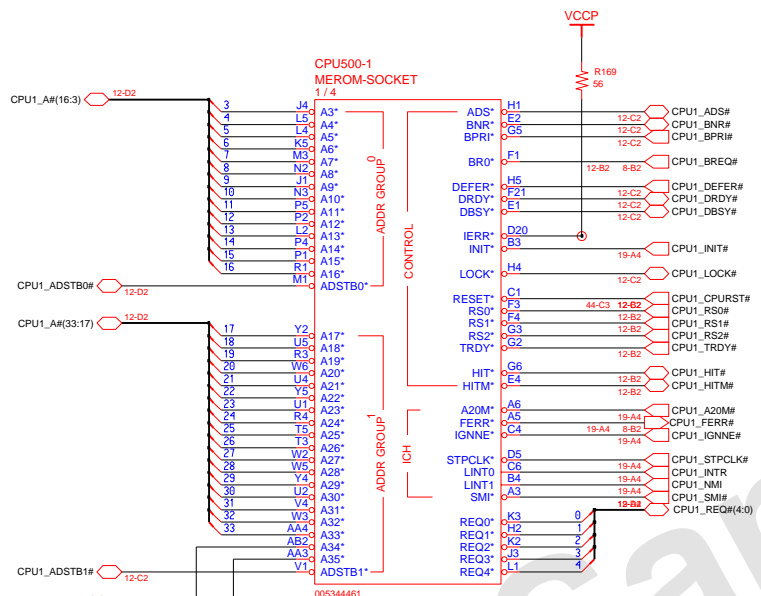
FSA, FSB, FSC of Clock chip are low threshold inputs  
 $V_{ih\_fs\_min} = 0.7V$   
 $V_{il\_fs\_max} = 0.35V$

CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Merom 800MHz  
 Celeron 533MHz  
 Merom 667MHz

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CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		CLOCK GENERATOR	PART NO. BA41-00791A
MODULE CODE		LAST EDIT				

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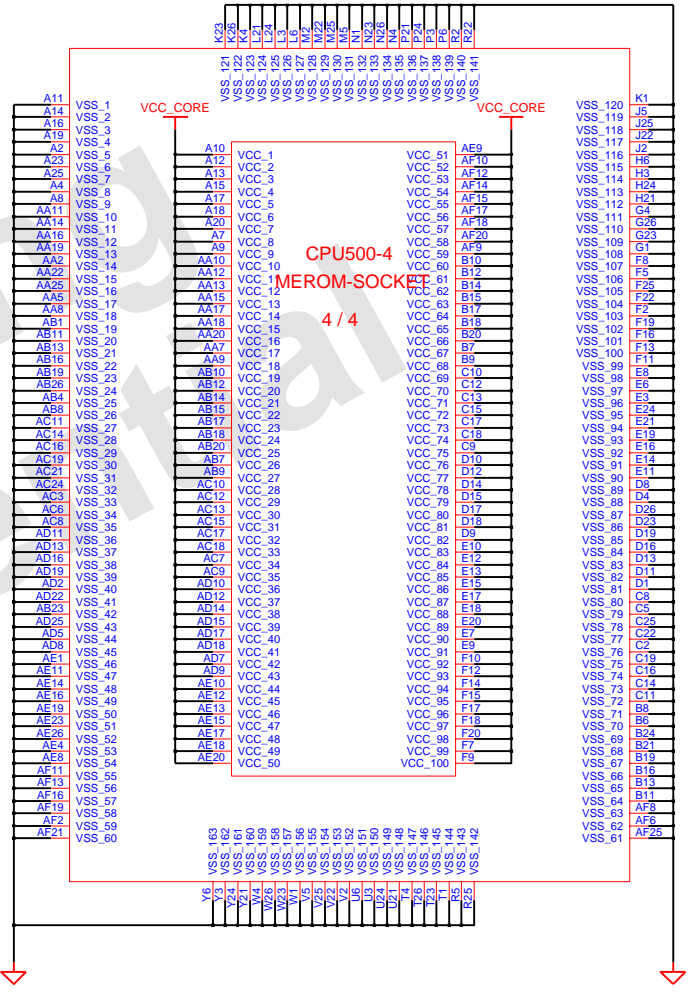
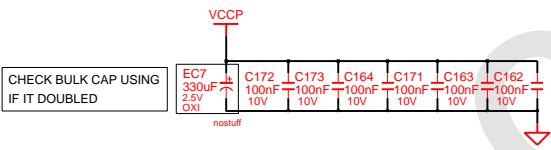
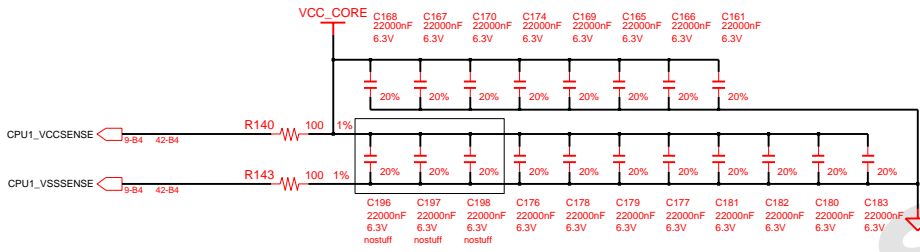
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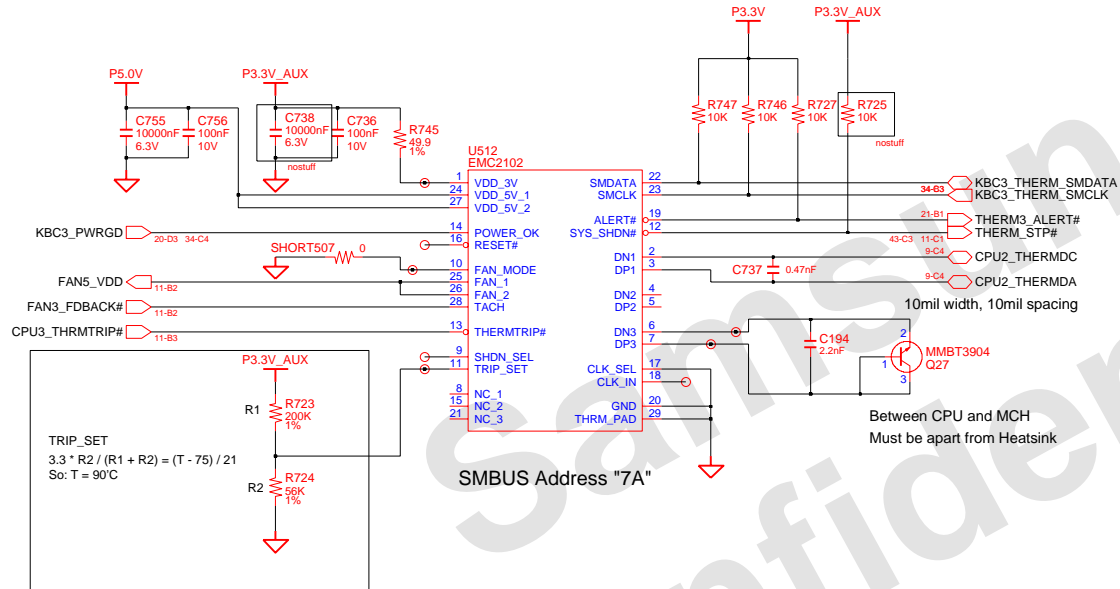
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Deleted 13 De-cap (Only use 19pcs out of 32)



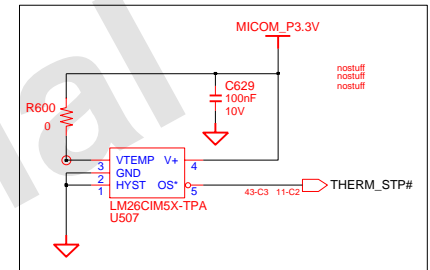
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APPROVAL	SJ PARK	REV	1.0		MEROM CPU(3/3)	PART NO.
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	10	OF 47
						BA41-00791A

# Thermal Monitor

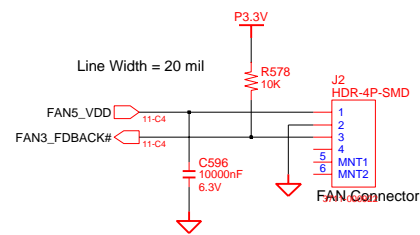
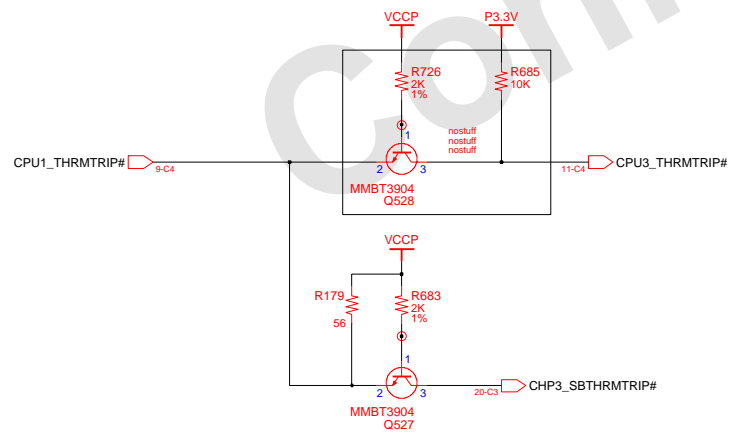


- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
  - Keep traces away from high voltage (+12V bus)
  - Keep traces away from fast data buses and CRT signal.
  - Use recommended trace widths and spacings (10mil)
  - Place a ground plane under the traces.
  - Use guard traces flanking DXP and DXN and connecting to GND

## OTP (NOSTUFF)

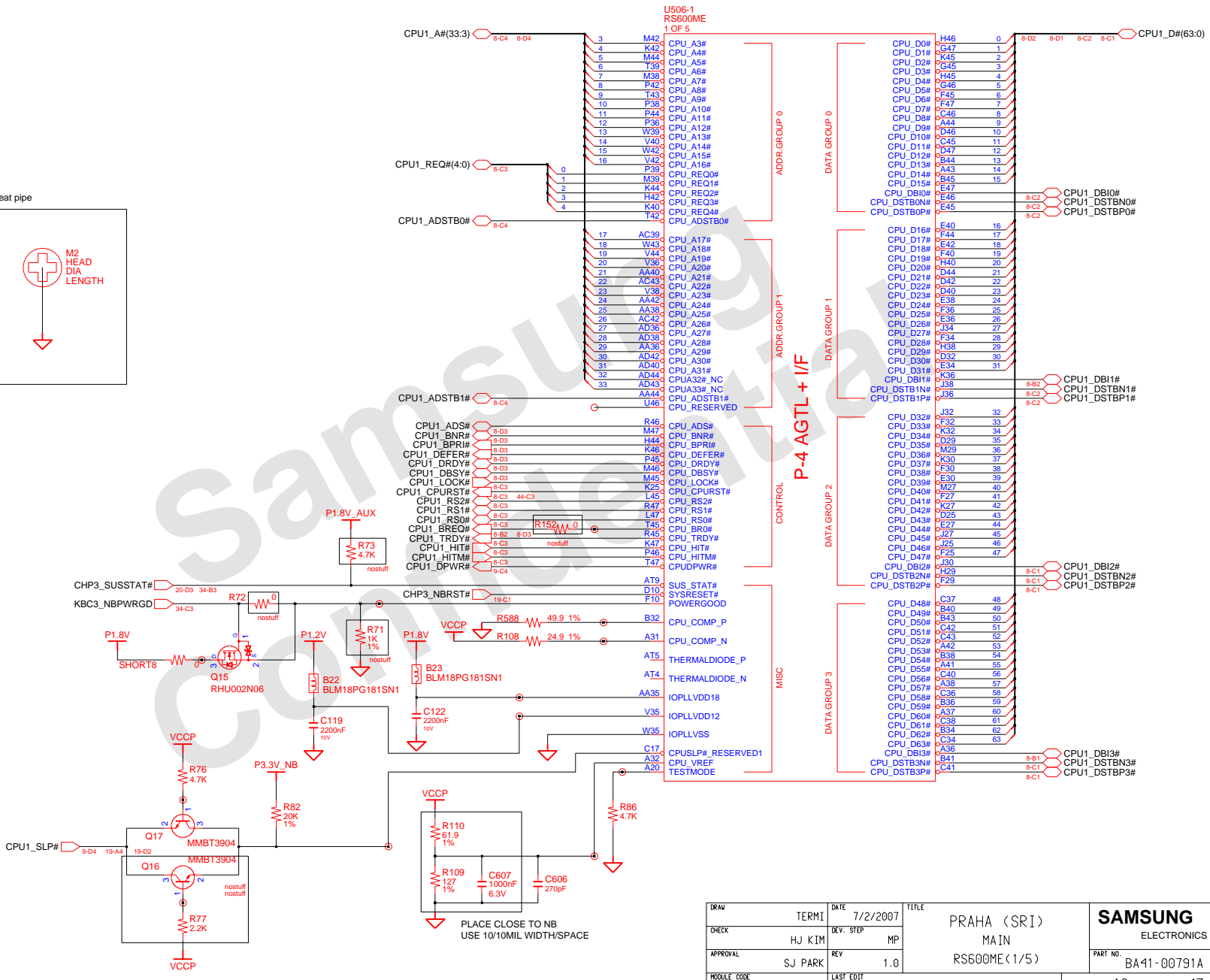
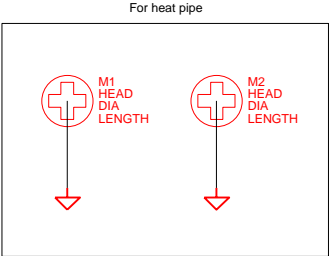


## FAN Control



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CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	THERMAL SENSOR/FAN CNTRL	PART NO.	BA41-00791A
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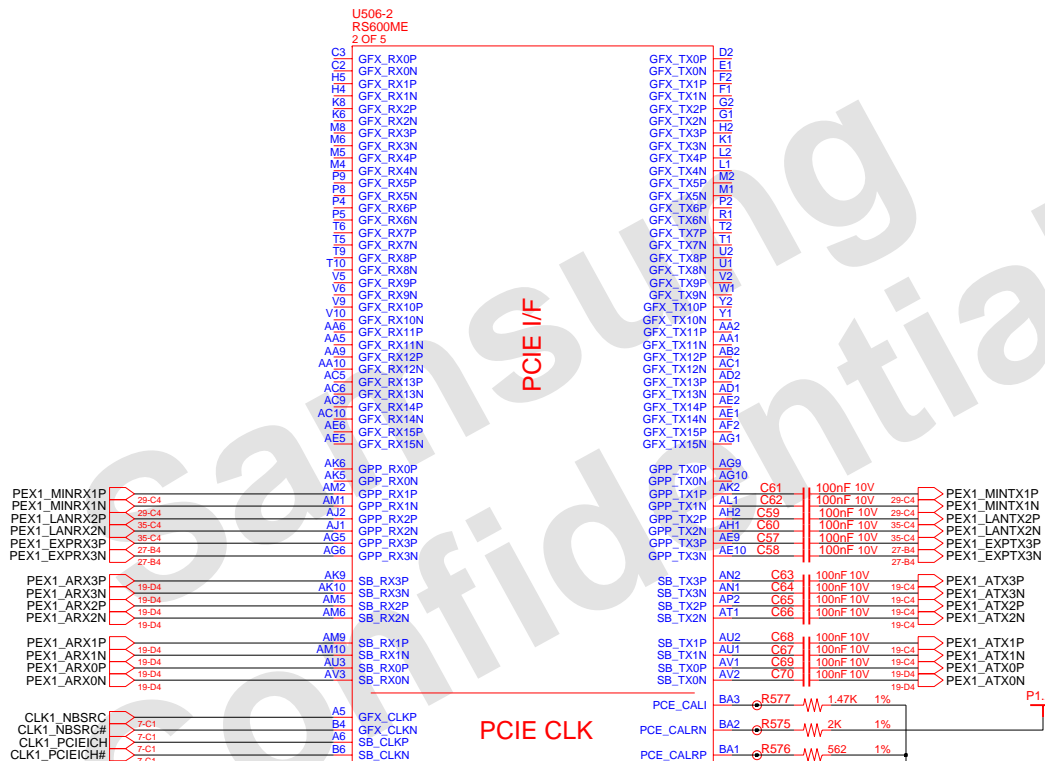
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CHECK	HJ KIM	7/2/2007	7/2/2007		
APPROVAL	SJ PARK	REV	1.0	RS600ME(1/5)	PART NO. BA41-00791A
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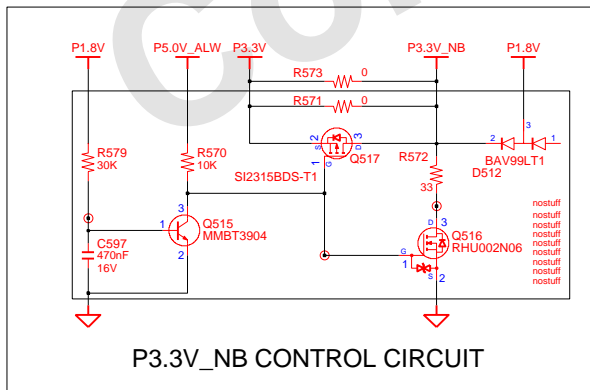
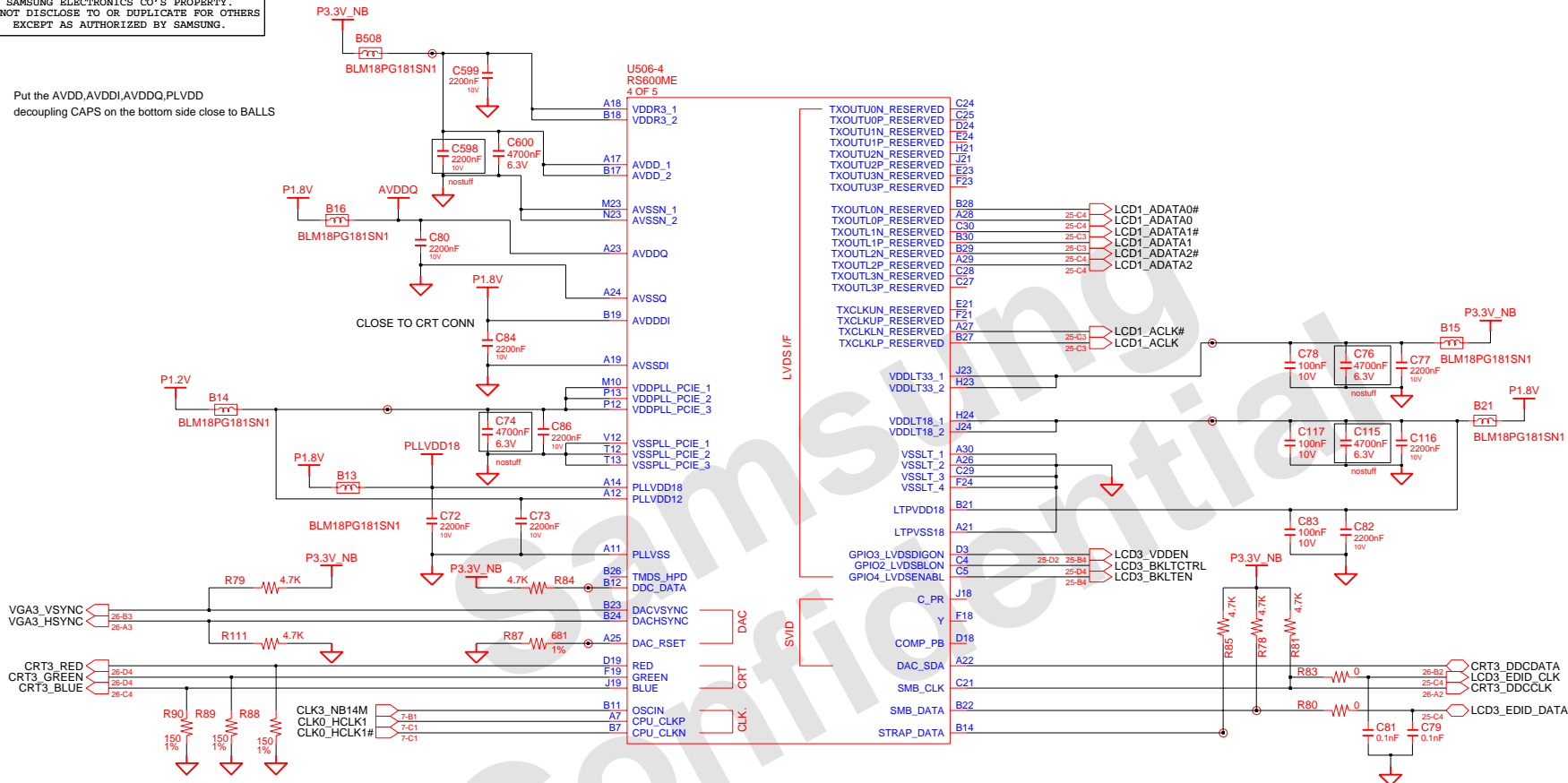
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Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS

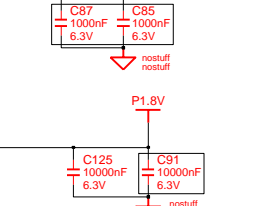
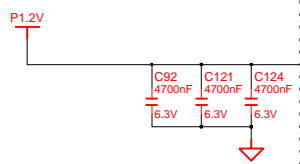
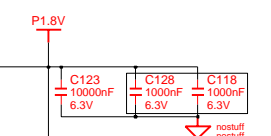
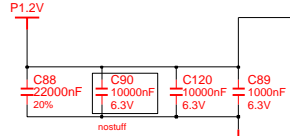
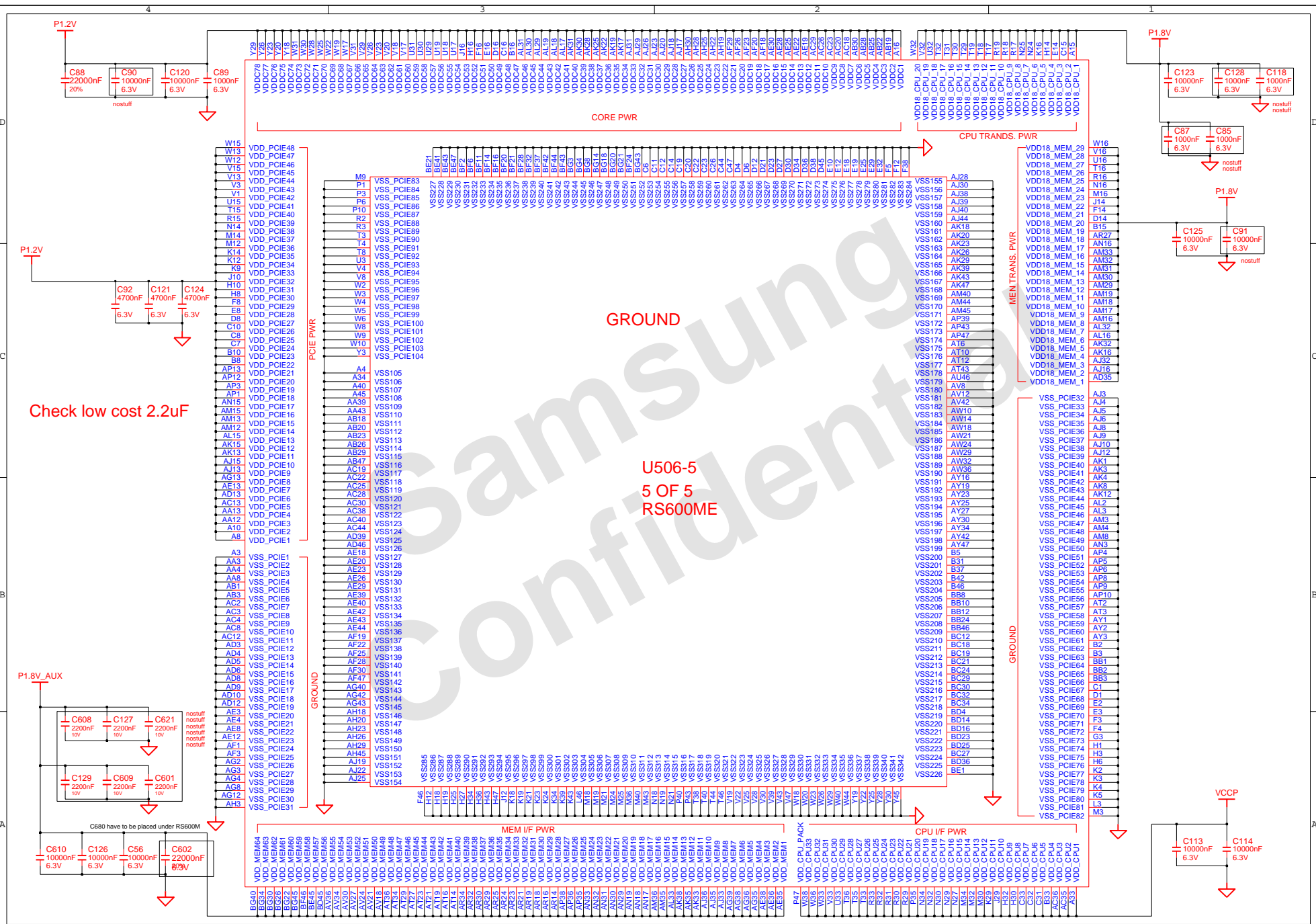


**P3.3V\_NB CONTROL CIRCUIT**

STRAP DEFINITIONS FOR THE RS6000	
STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS6000
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

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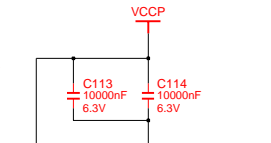
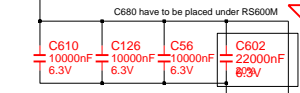
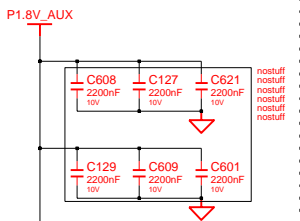




Check low cost 2.2uF

GROUND

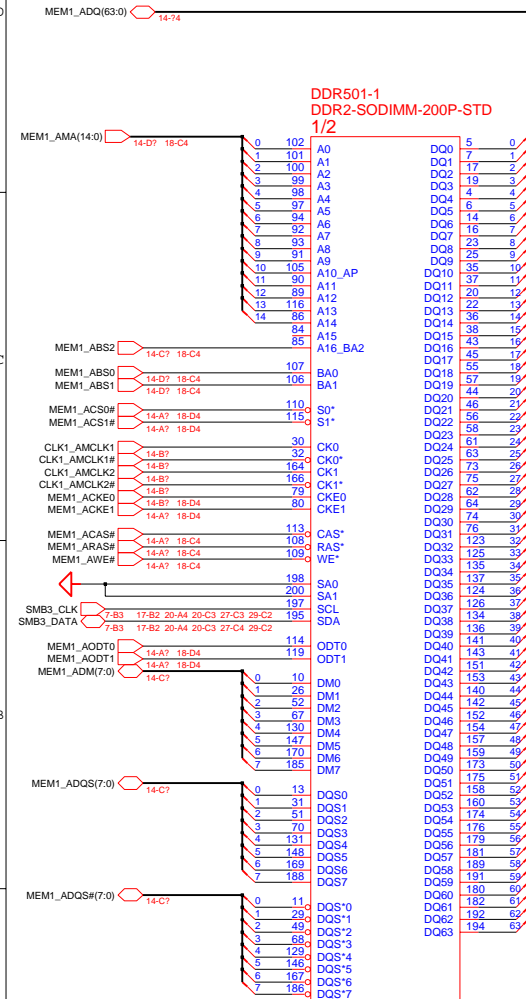
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5 OF 5  
RS600E



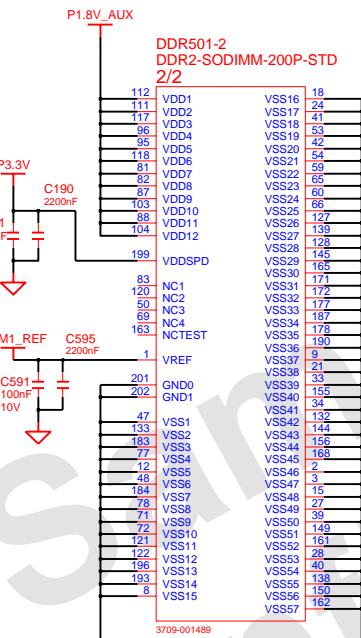


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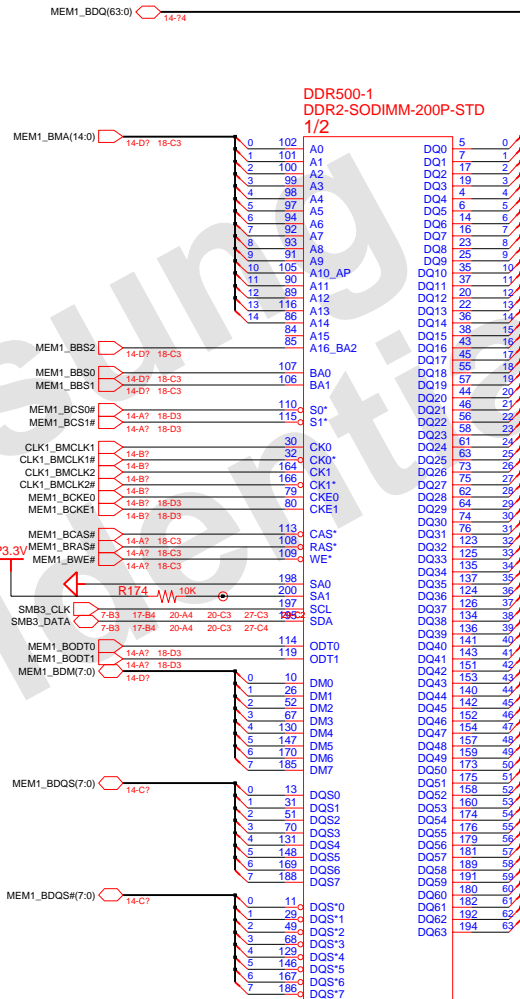


DDR501-1  
DDR2-SODIMM-200P-STD  
1/2

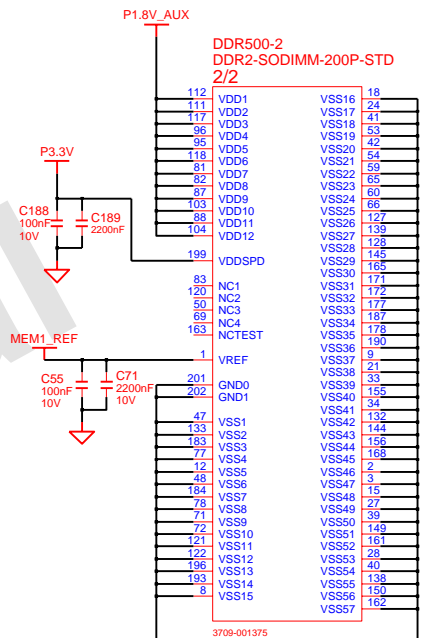


DDR501-2  
DDR2-SODIMM-200P-STD  
2/2

J4 Height : 9.2mm



DDR500-1  
DDR2-SODIMM-200P-STD  
1/2



DDR500-2  
DDR2-SODIMM-200P-STD  
2/2

DDR1 Height : 5.2mm

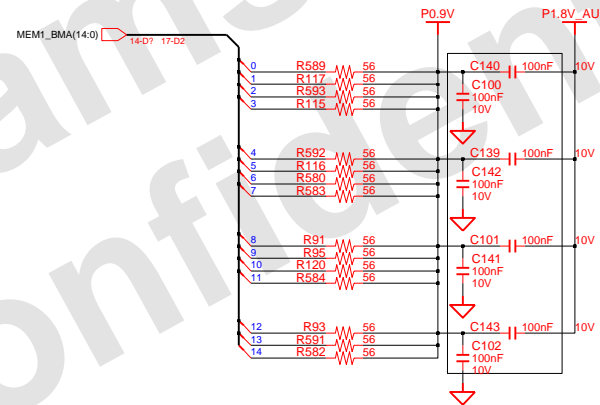
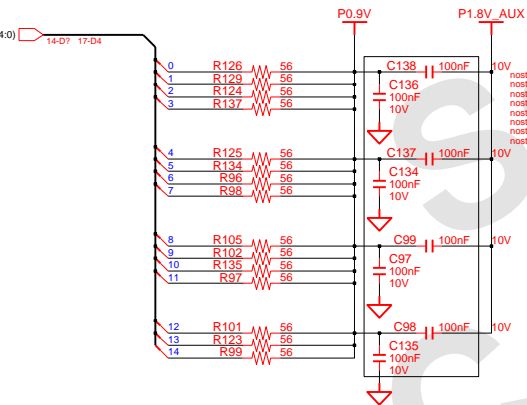
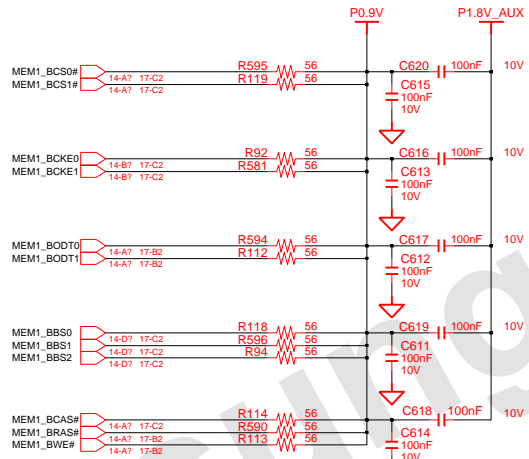
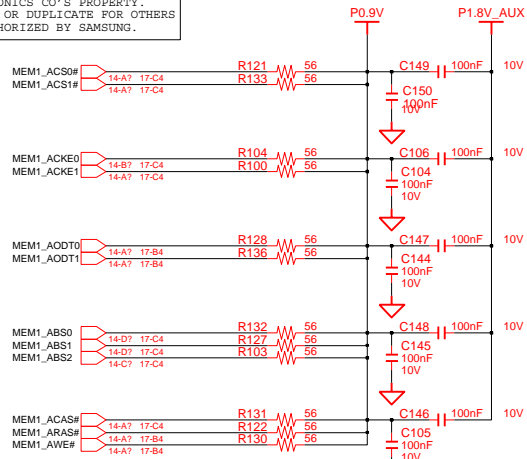
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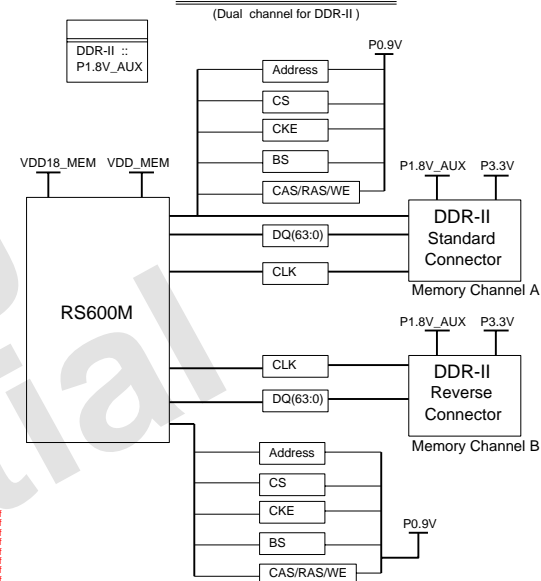
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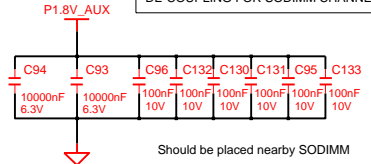
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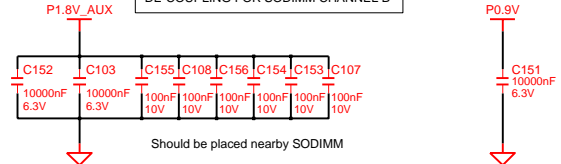
**Memory Topology**



**DE-COUPLING FOR SODIMM CHANNEL A**

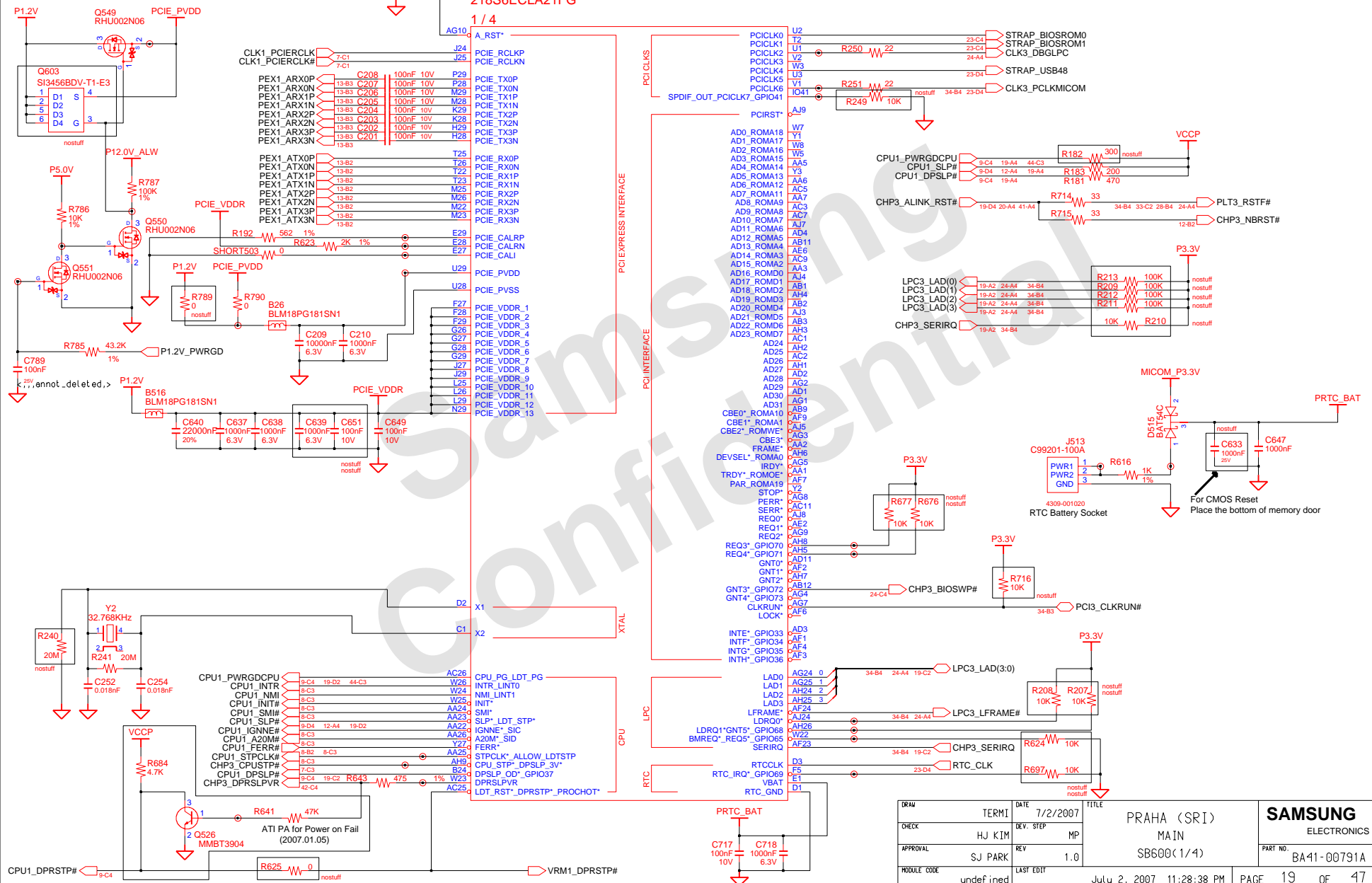


**DE-COUPLING FOR SODIMM CHANNEL B**



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	DDR2 - TERMINATION		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	18	OF 47

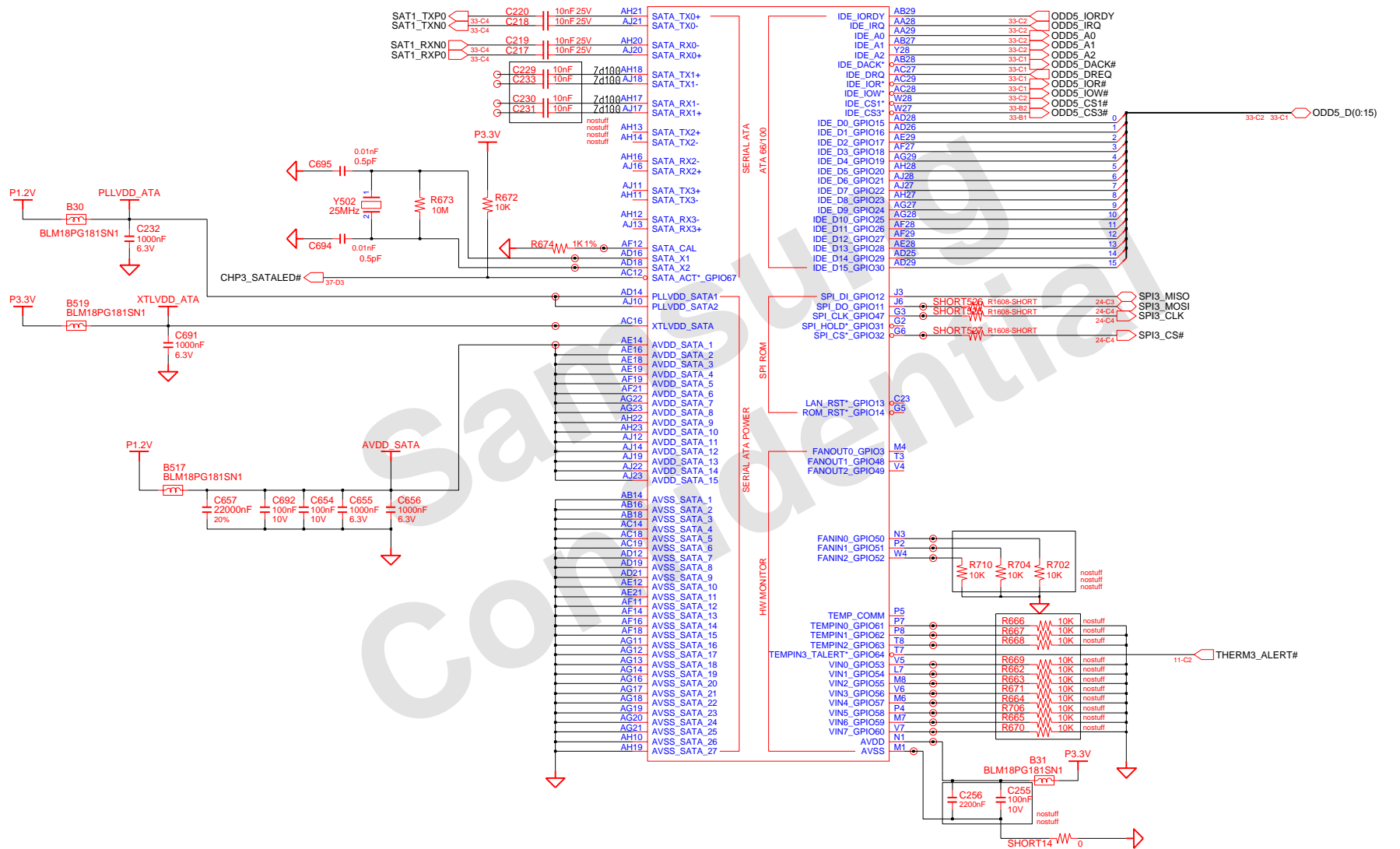
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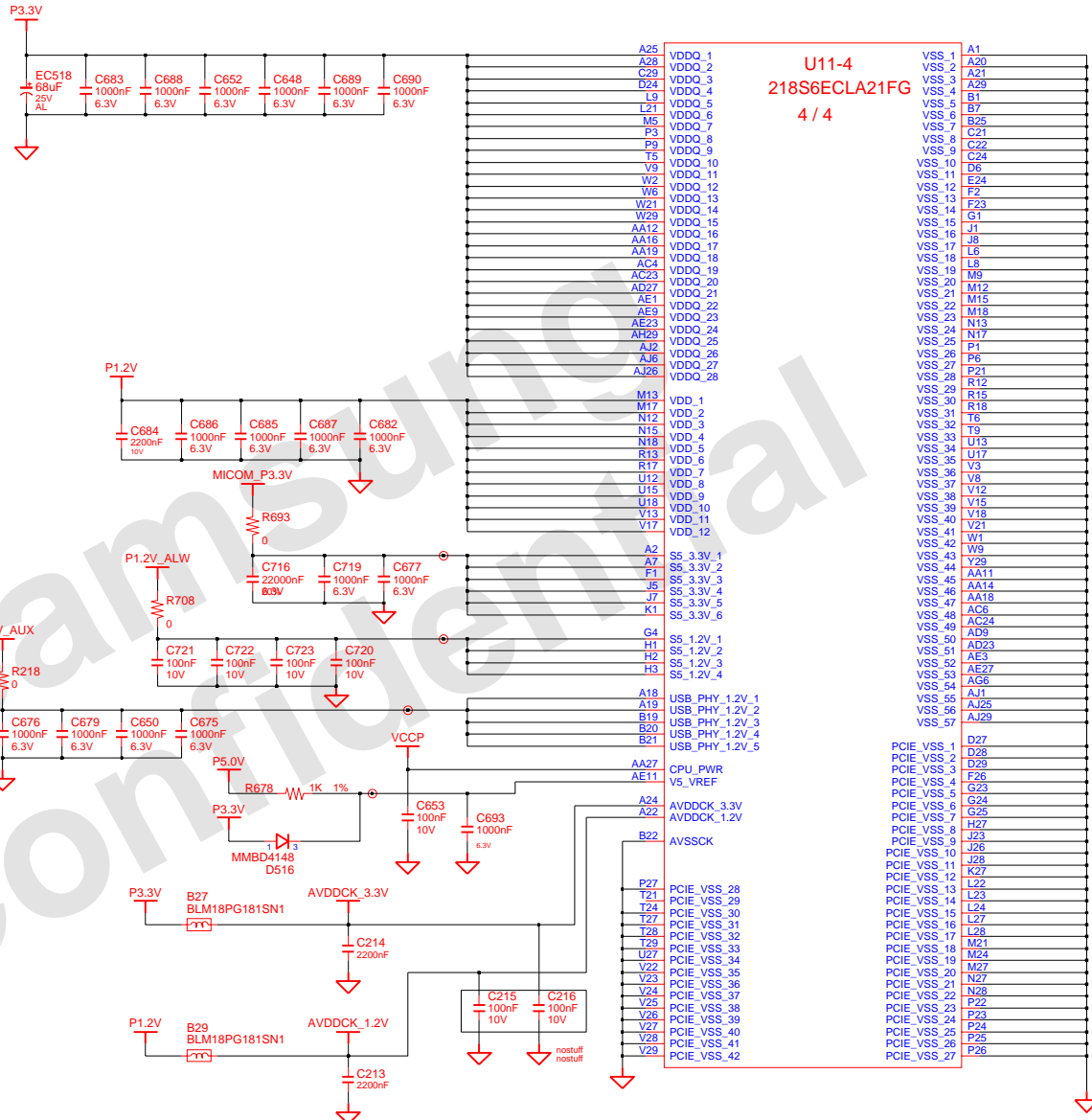
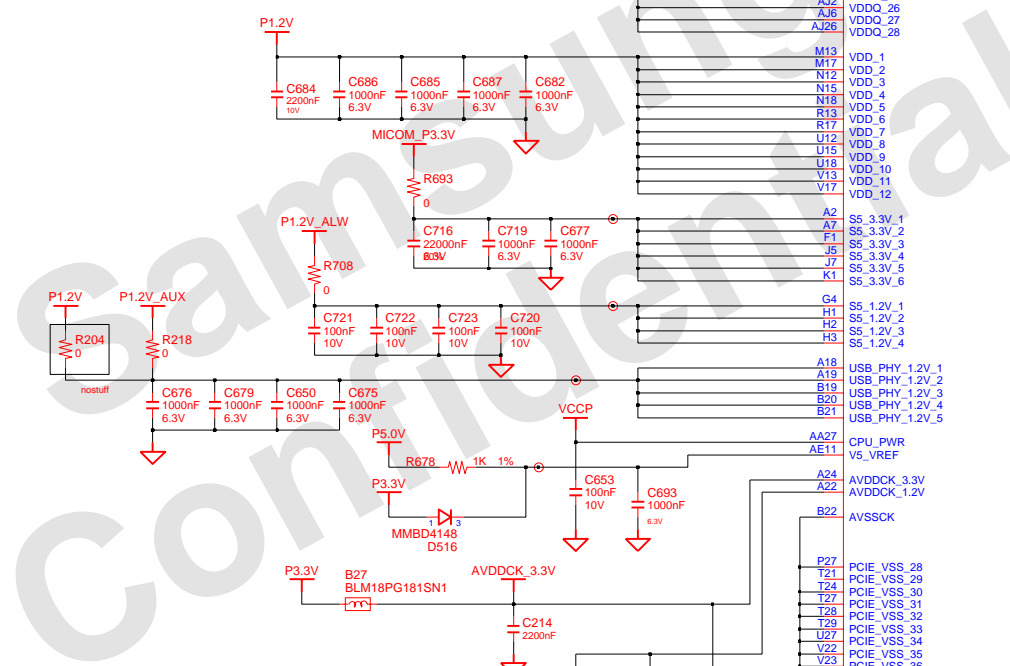
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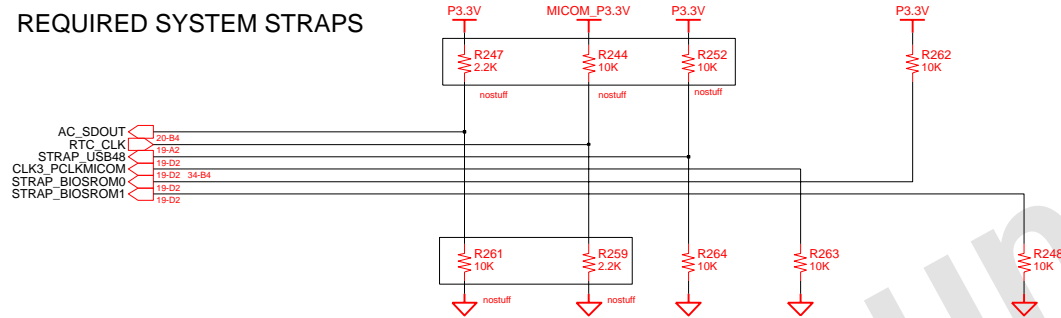


U11-4  
218S6ECLA21FG  
4 / 4

DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN SB600(4/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00791A
CHECK	HJ KIM	DEV. STEP	MP		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM		
PAGE 22 OF 47					

SB600 HAS AN INTERNAL PD FOR AC\_SDOUT  
 SB600 HAS AN INTERNAL PU FOR RTC\_CLK

**REQUIRED SYSTEM STRAPS**



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	L, H = LPC ROM L, L = FWH ROM	

**DEBUG STRAPS**

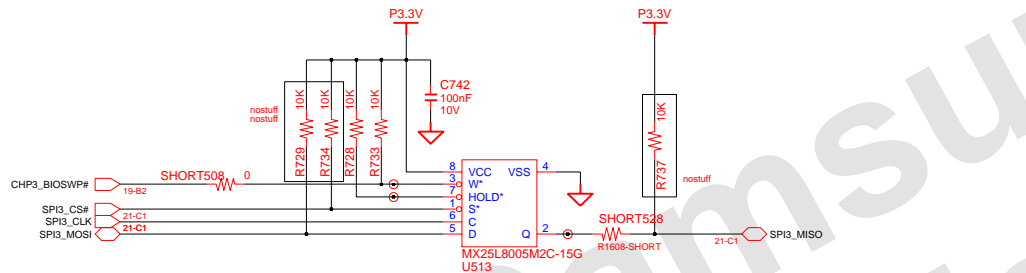
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		STRAPS	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	23	OF 47



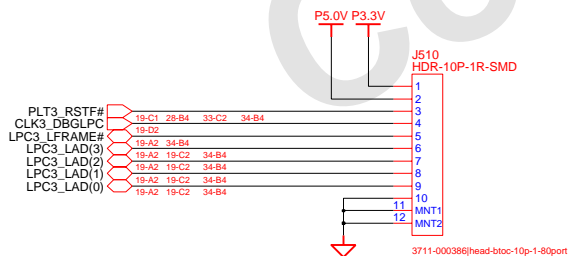
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SPI3\_CS#  
SB600 prior to A21 : Pulled up to P3.3V\_ALW with 1Kohm resistor.  
SB600 A21 and newer : No external pull-up resistor required.

**DEBUG CARD CONN**



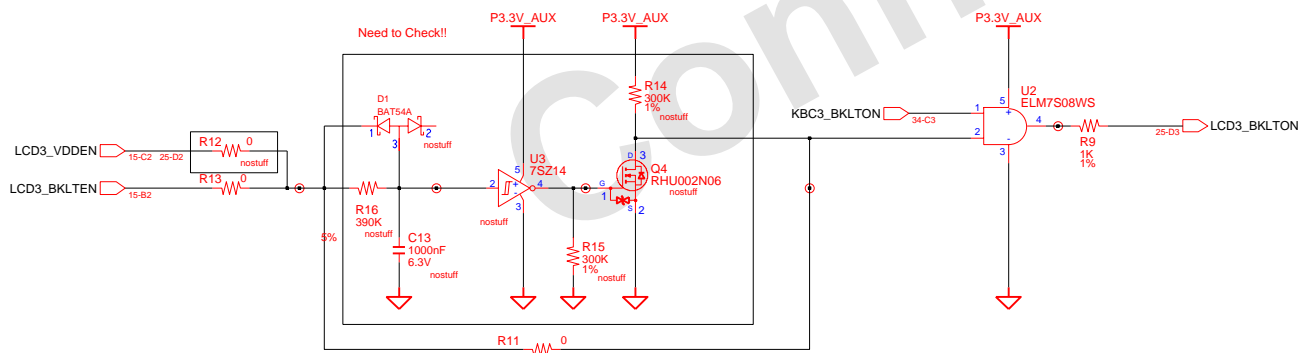
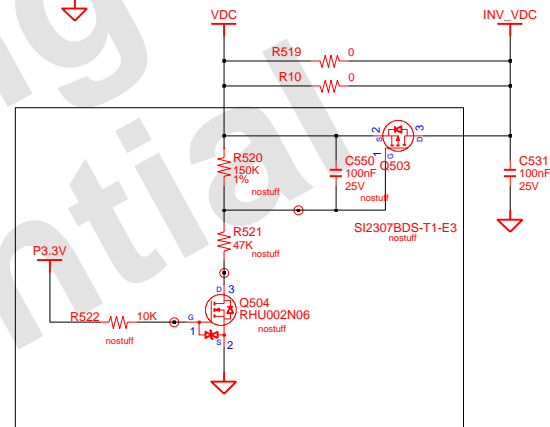
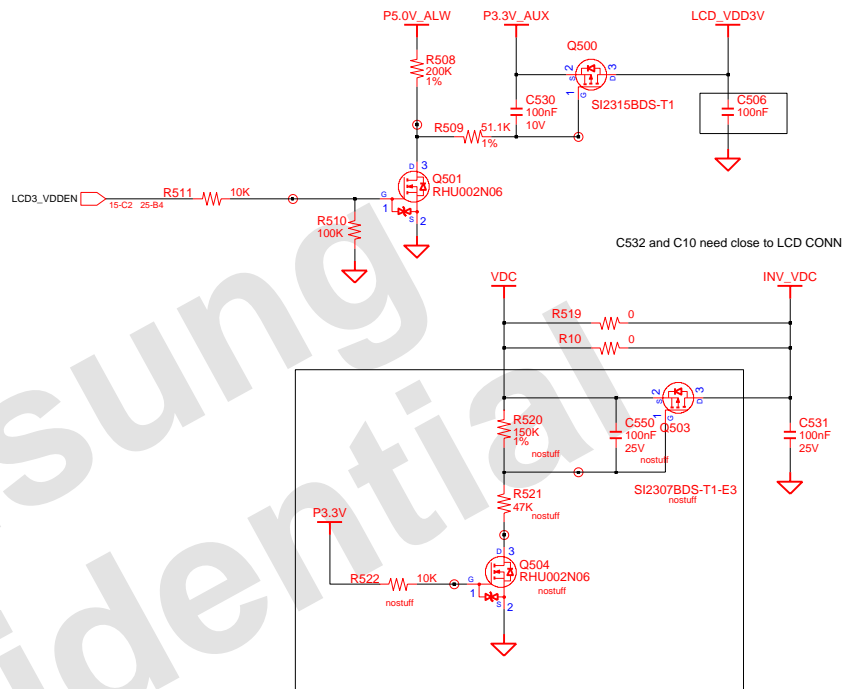
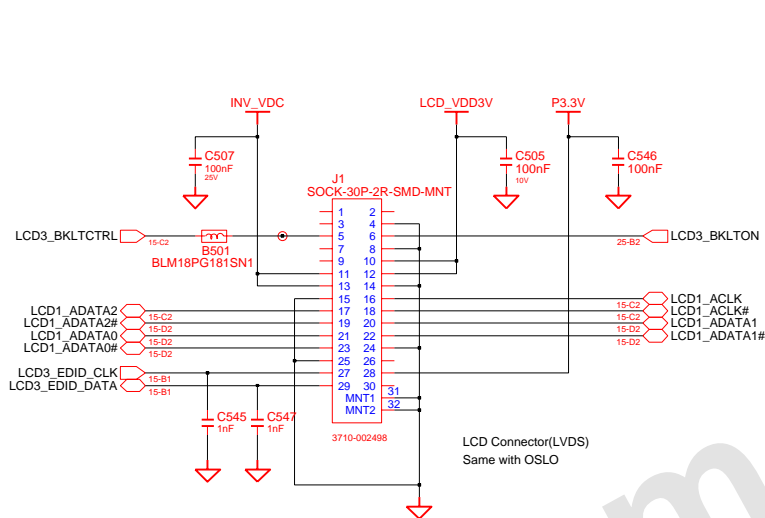
- |   |                                    |
|---|------------------------------------|
| 02 VERIFY REAL MODE                             | 66 CONFIGURE ADVANCE CACHE REG.    |
| 03 DISABLE NMI                                  | 6A DISPLAY EXTERNAL CACHE SIZE     |
| 04 GET CPU TYPE                                 | 6C DISPLAY SHADOW MESSAGE          |
| 06 INIT. SYSTEM H/W                             | 6E DISPLAY NON-DISPOSABLE SEGMENT  |
| 08 INIT. CHIPSET REG.                           | 70 DISPLAY ERROR MESSAGE           |
| 09 SET IN POST FLAG                             | 72 CHECK FOR CONFIGURATION ERROR   |
| 0A INIT CPU.REG                                 | 74 TEST REAL-TIME CLOCK            |
| 0B CPU CACHE ON                                 | 76 CHECK FOR KEYBOARD EERROR       |
| 0C INIT.CACHE TO POST                           | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE                              | 7E TEST COPROCESSER IF PRESENT     |
| 0F ENABLE THE L-BUS IDE                         | 80 DISABLE ON-BOARD I/O PORT       |
| 10 INIT. POWER MANAGER                          | 82 DETECT AND INSTALL EXT.RS232C   |
| 11 LOAD ALTERNATE REG.                          | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT      |
| 14 INIT. KEYBOARD CONTROLLER                    | 88 INIT. BIOS DATA ROM             |
| 16 CHECK CHECKSUM                               | 8A INIT.EXTENDED BIOS DATA AREA    |
| 18 8254 TIMER INIT.                             | 8C INIT. FDD CONTROLLER            |
| 1A 8237 DMA CONTROLLER INIT.                    | 9A SHADOW OPTION ROMS              |
| 1C RESET INTERRUPT CONTROLLER                   | 9C SETUP POWER MANAGEMENT          |
| 20 TEST DRAM REFRESH                            | 9E ENABLE H/W INTERRUPT            |
| 22 TEST 842 KEYBOARD CONTROLLER                 | A0 SET TIME OF DAY                 |
| 24 SET ES SEGMENT REG. TO 4GB                   | A4 INIT. TYPOMATIC RATE            |
| 26 ENABLE A20                                   | A8 ERASE F2 PROMPT                 |
| 28 AUTO SIZING DRAM                             | AA SCAN FOR F2 KEY STROKE          |
| 32 COMPUTE THE CPU SPEED                        | AC ENTER SETUP                     |
| 34 TESET CMOS RAM                               | AE CLEAR IN POST FLAG              |
| 38 SHADOW SYSTEM BIOS ROM                       | B0 CHECK FOR ERRORS                |
| 3A AUTO SIZING CACHE                            | B2 POST DONE-PREPARE TO BOOT O/S   |
| 3C CONFIGURE ADVANCED CHIPSET REG.              | B4 ONE BEEP                        |
| 3D LOAD ALTER REG. WITH CMOS VALUE              | B6 CHECK PASSWORD (OPTION)         |
| 42 INIT. INTERRUPT VECTOR                       | B7 ACPI INIT                       |
| 44 INIT. BIOS INTERRUPT                         | BA DMI INIT                        |
| 46 CHECK ROM COPYRIGHT NOTICE                   | BE CLEAR SCREEN                    |
| 47 INIT. I20 SUPPORT IF INSTALLED               | C0 TRY BOOT WITH INT19             |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS           | D0 INTERRUPT HANDLER ERROR         |
| 49 INIT. PCI BUS AND DEVICE                     | D2 UNKNOWN INTERRUPT ERROR         |
| 4A INIT. ALL VIDEO BIOS ROM                     | D4 PENDING INTERRUPT ERROR         |
| 4C SHADOW VIDEO BIOS ROM                        | D6 SHUTDOWN 5                      |
| 50 DISPLAY CPU TYPE AND SPEED                   | D8 SHUTDOWN ERROR                  |
| 52 TEST KEYBOARD                                | DA EXTENDED BLOCK MOVE             |
| 54 SET KEYCLICK IF ENABLED                      | DC SHUTDOWN 10                     |
| 56 ENABLE KEYBOARD                              | 89 ENABLE NMI                      |
| 58 TEST FOR UNEXPECTED INTERRUPTS               | 90 INIT. HDD CONTROLLER            |
| 5A DISPLAY " PRESS ..... SETUP"                 | 91 INIT. LOCAL BUS HDD CONTROLLER  |
| 5C TEST RAM BETWEEN 512K AND 640K               | 92 JUMP TO USER PATCH 2            |
| 60 TEST EXTENDED MEMORY                         | 94 DISABLE A20 ADDRESS LINE        |
| 62 TEST EXTENDED MEMORY ADDRESS LINE            | 96 CLEAR HUGE ES SEGMENT REG.      |
| 64 JUMP TO USER PATCH 1                         | 98 SEARCH FOR OPTION ROMS          |

DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	7/2/2007	DEV. STEP		
APPROVAL	SJ PARK	REV	1.0	SPI ROM & DEBUG PORT	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	24 OF 47



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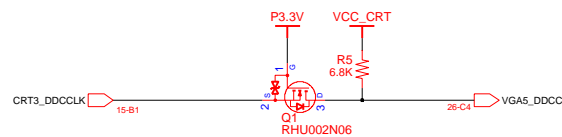
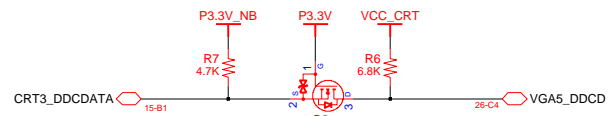
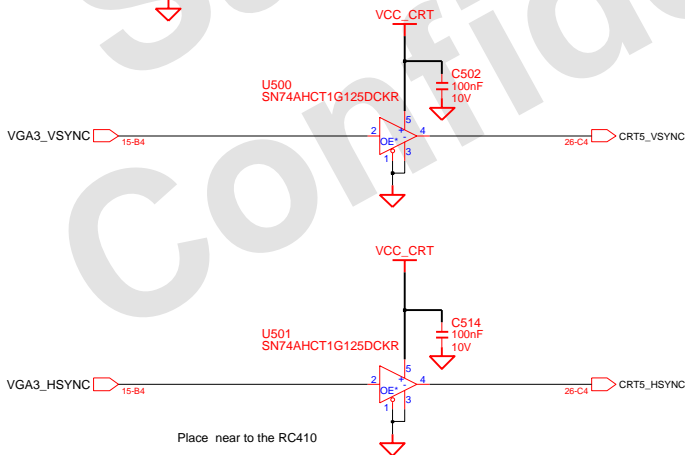
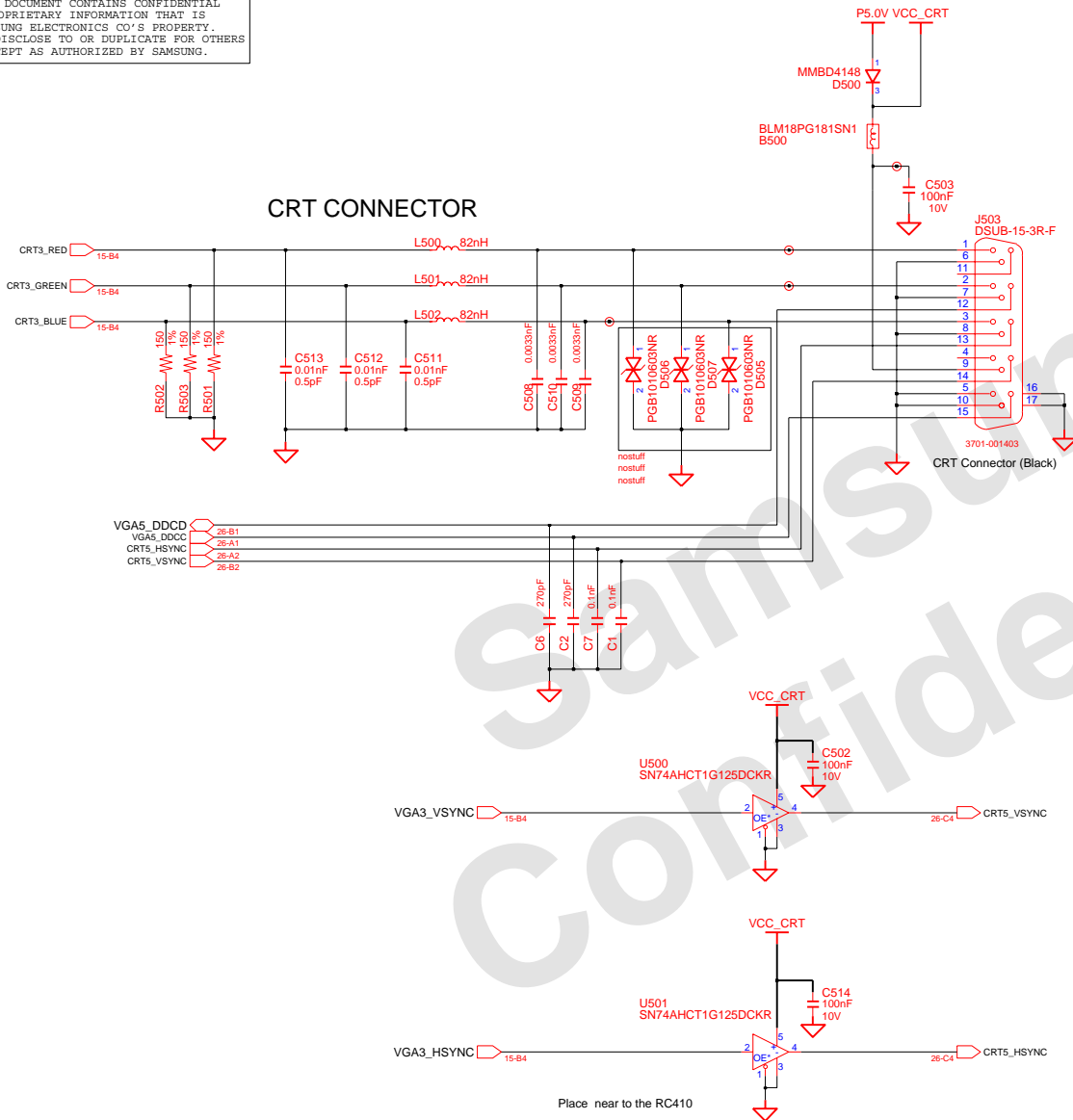


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) LCD Connector & SPREAD SPECTRUM	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	25	OF 47

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**CRT CONNECTOR**

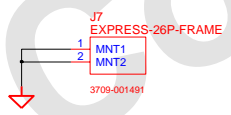
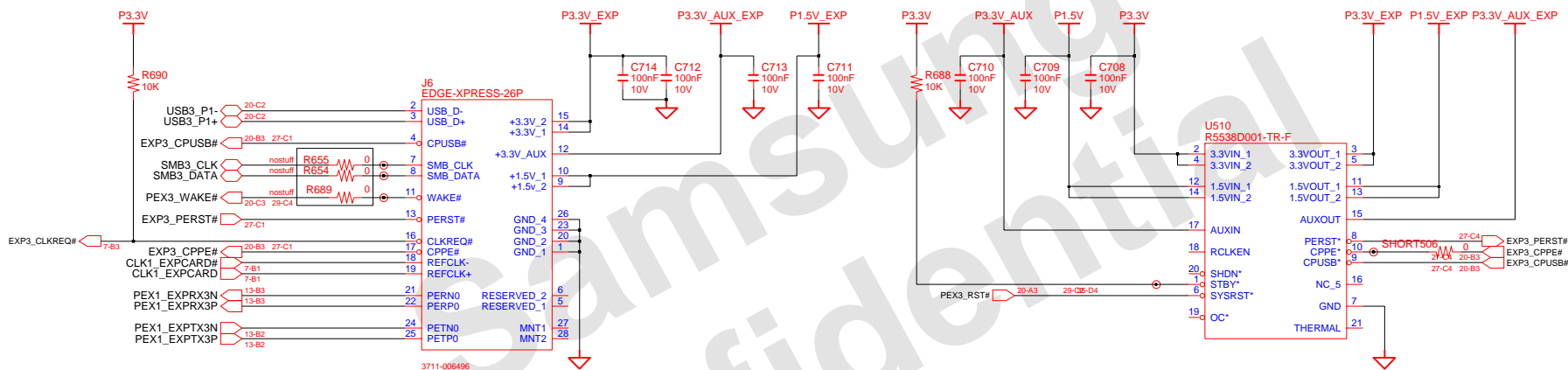


Place near to the RC410

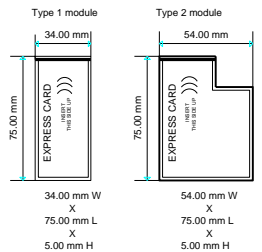
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CHECK	HJ KIM	DEV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0		CRT	PART NO.	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			BA41-00791A	
						PAGE	26 OF 47

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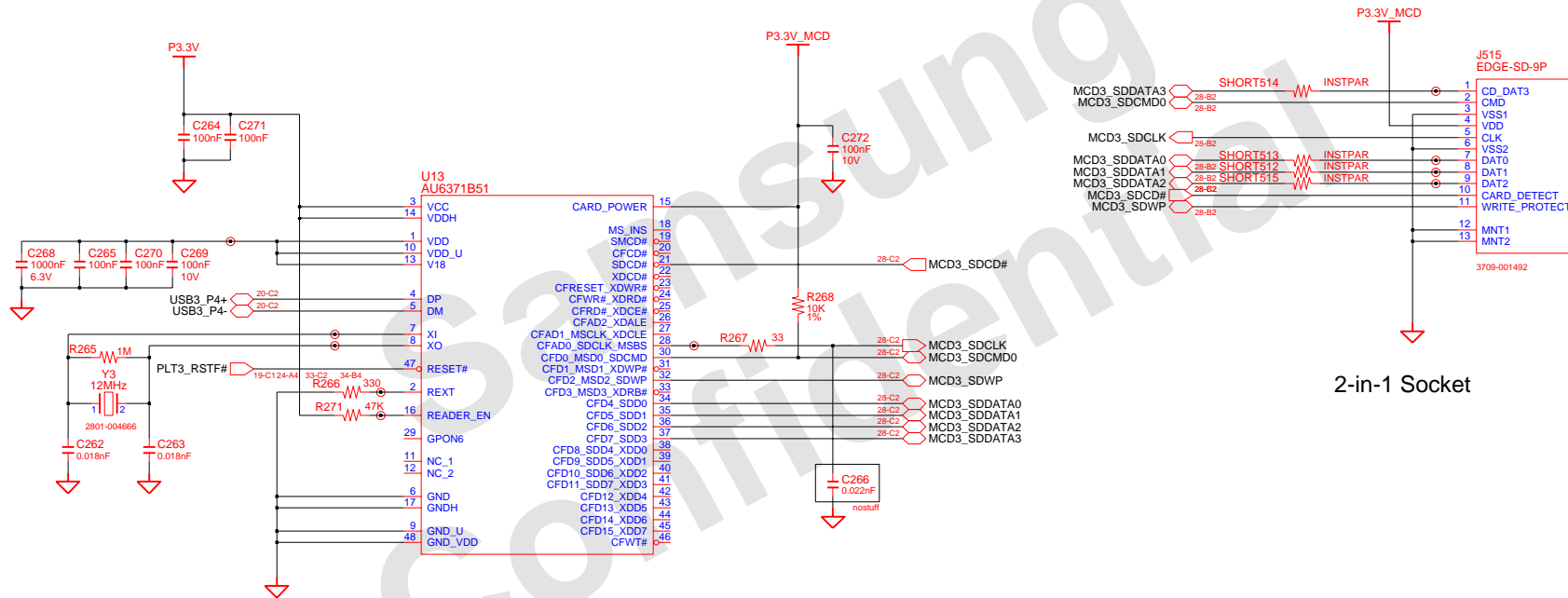


**EXPRESS CARD**



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		EXPRESS CARD	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	27	OF 47

2 IN 1 CARD

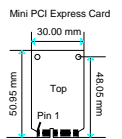
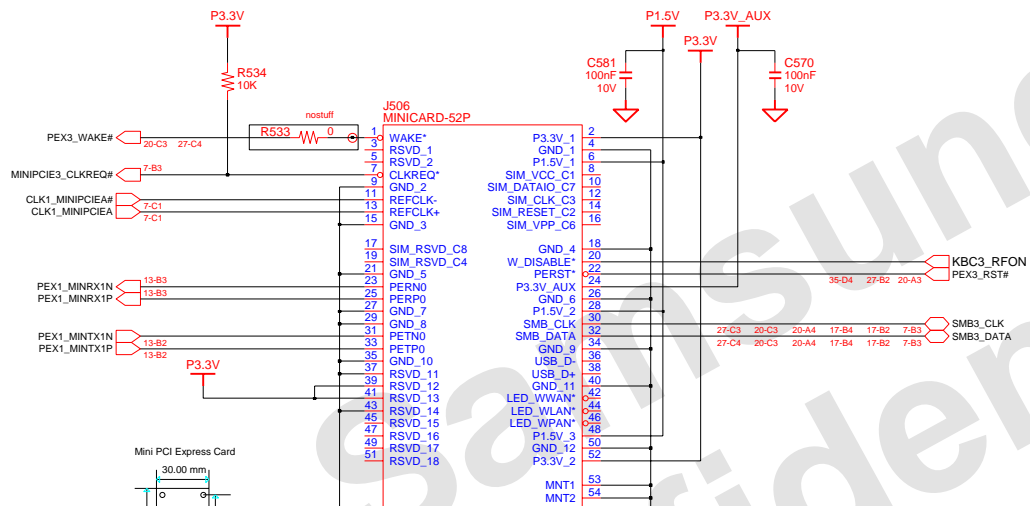


2-in-1 Socket

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	2 in 1 Socket		PART NO.
MODULE CODE	LAST EDIT		July 2, 2007 11:28:38 PM		PAGE	28 OF 47

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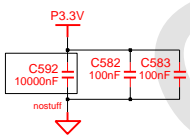
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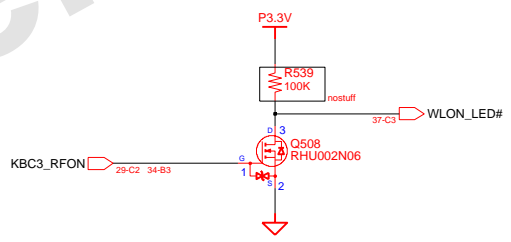
Odd Pins : Top side  
Even Pins : Bottom Side

**7mm Height  
Mini PCI Express**

PCI Express Mini Card ElectroMechanical Spec. 1.0



**4.5mm Height  
For MiniCard**

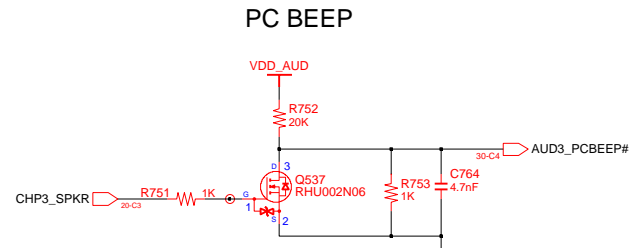
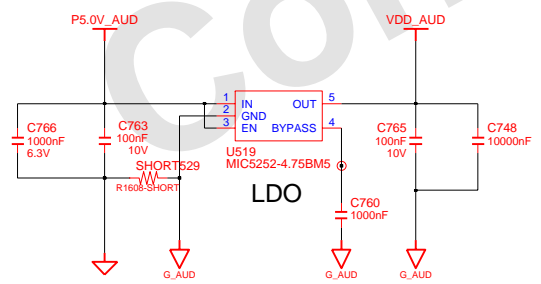
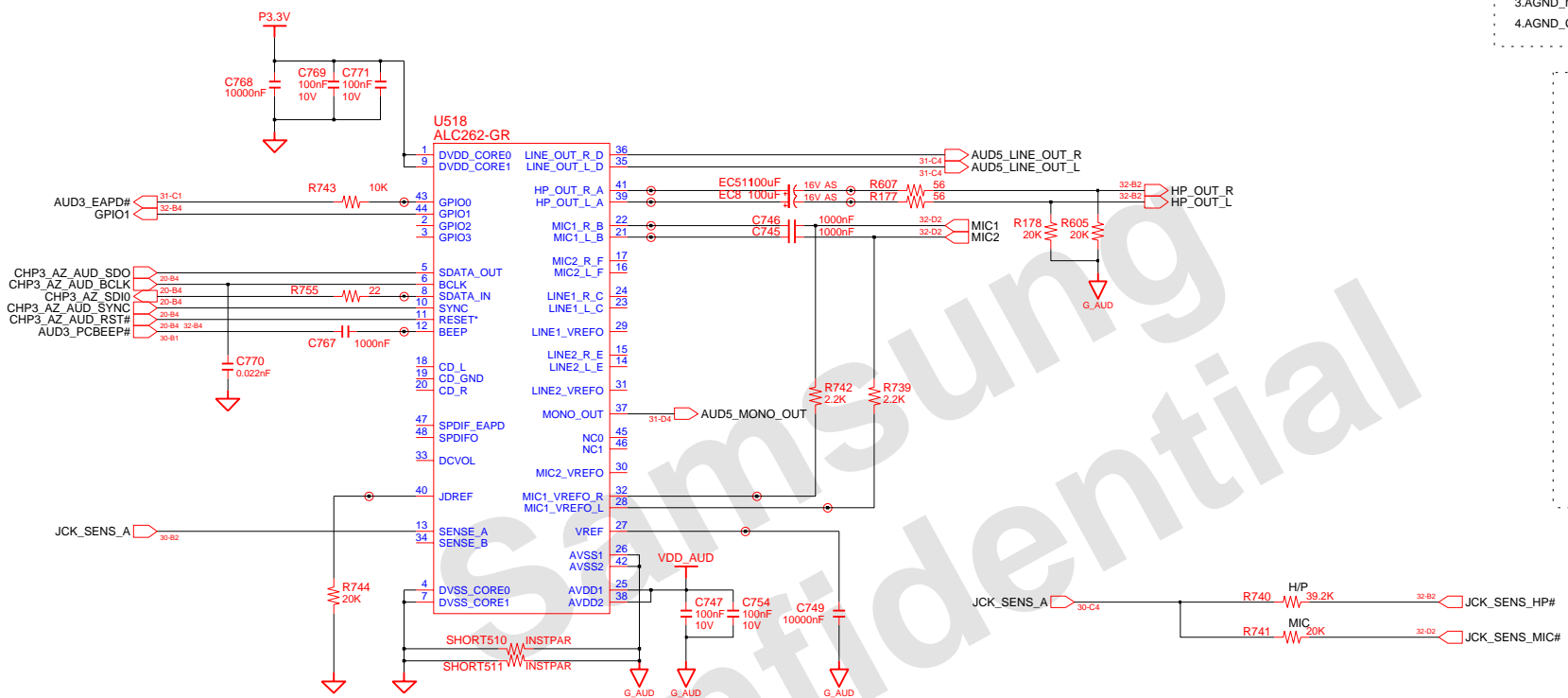
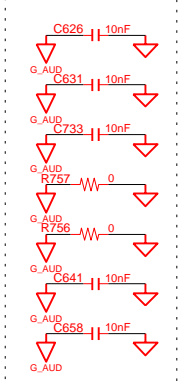


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MINI CARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 29 OF 47
MODULE CODE	undefined					

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- 1.AGND\_AUD IS AUDIO GROUND
- 2.GND IS DIGITAL GROUND
- 3.AGND\_MIC IS MIC GROUND
- 4.AGND\_CHS IS CHASS GROUND

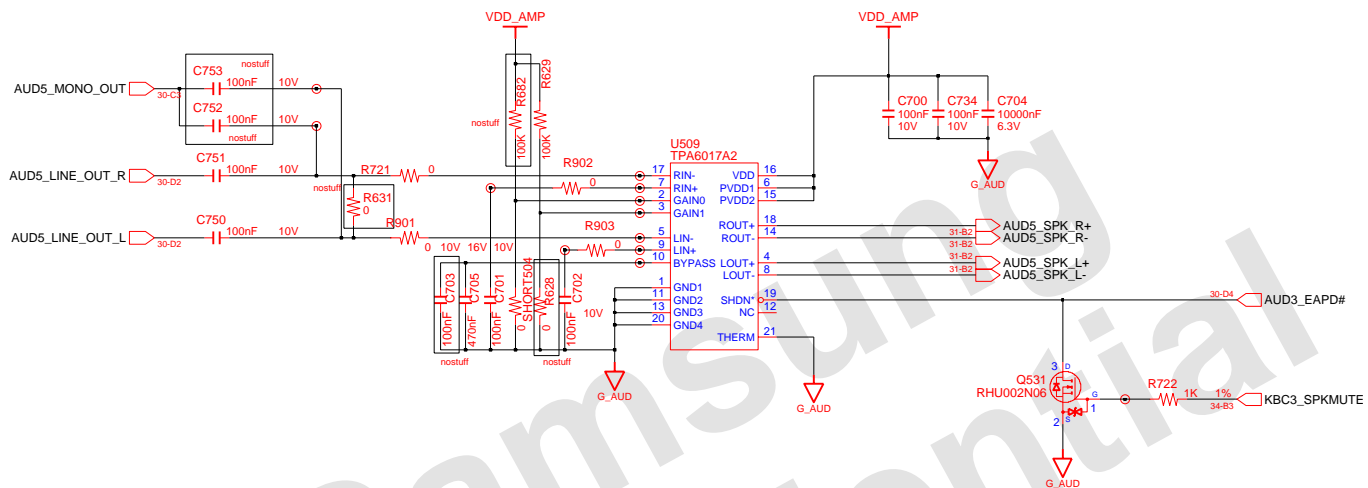
ALL TYPE IS 1608



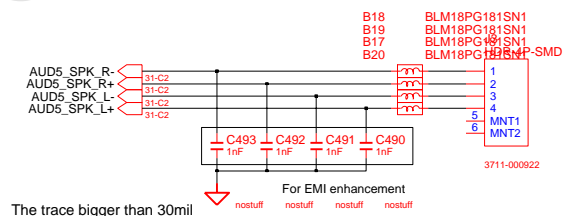
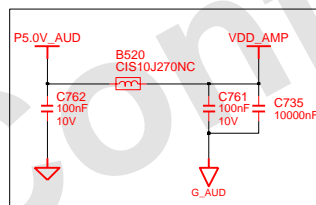
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CHECK	HJ KIM	7/2/2007	DEV. STEP		
APPROVAL	SJ PARK	REV	1.0		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 30	OF 47

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**AMP\_VDD INTERNAL STEREO SPEAKERS**

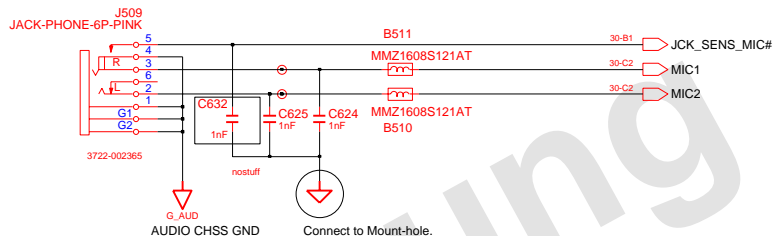


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN LIMITER & AMP	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 31 OF 47		
					PART NO.	BA41-00791A

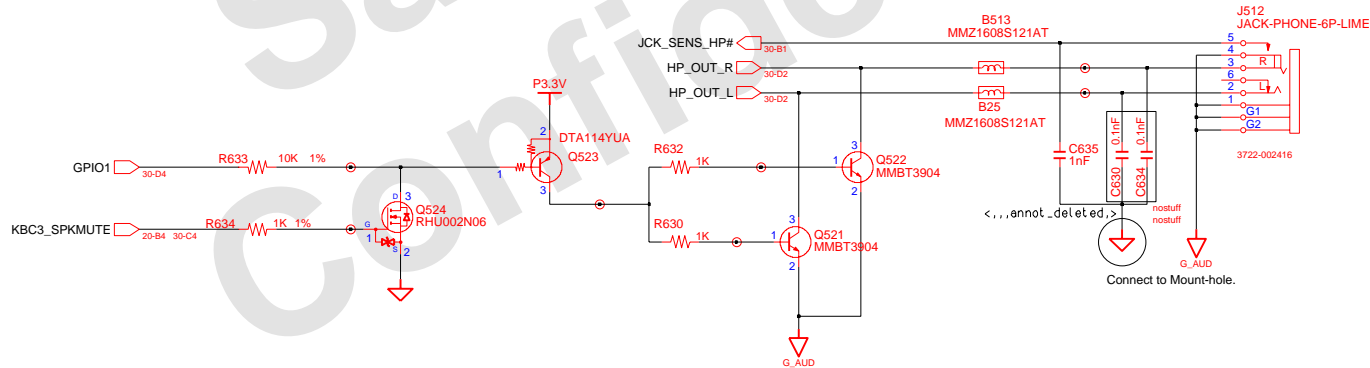
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**MIC JACK**



**HEADPHONE**



The traces led to Audio Jacks have the width over 10mil

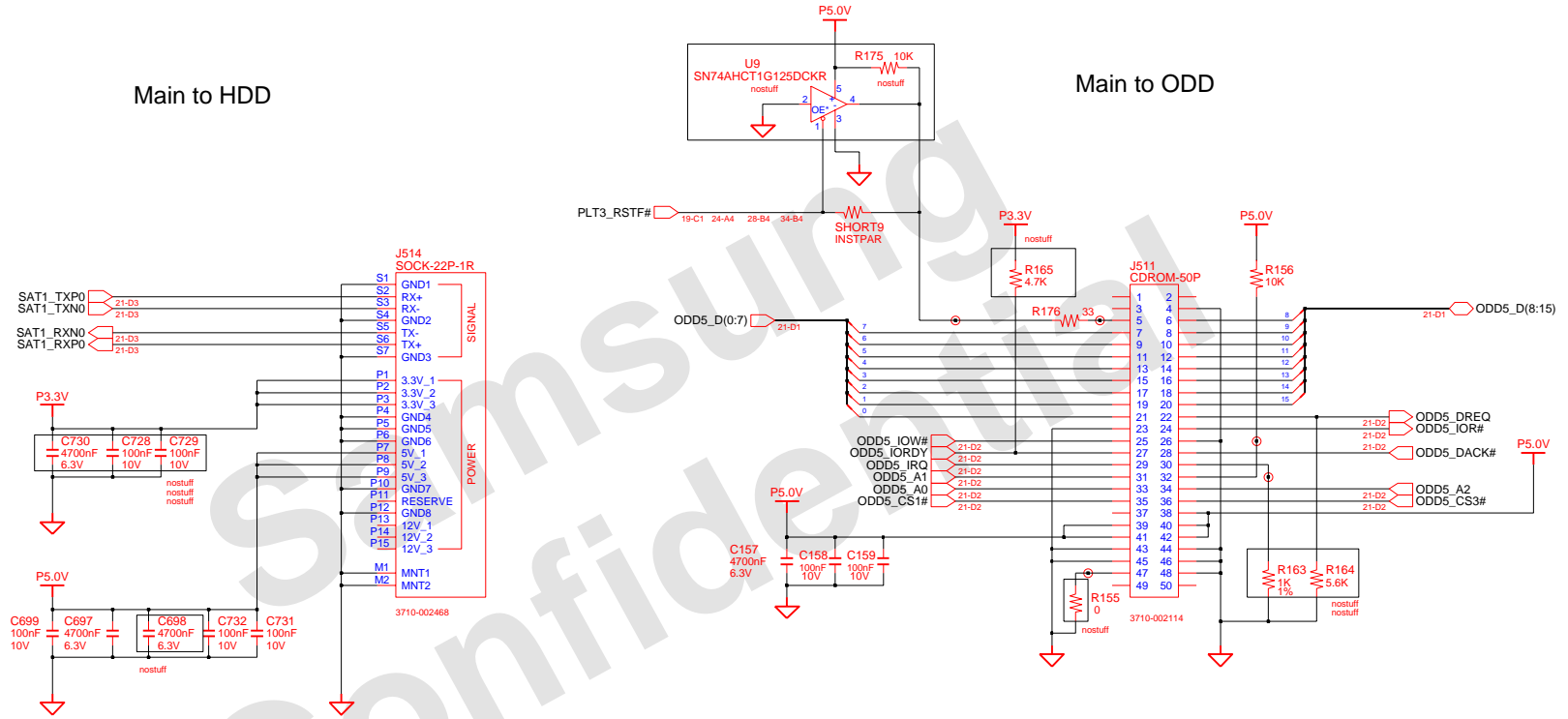
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MIC & HEADPHONE	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	32	OF 47



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Main to HDD

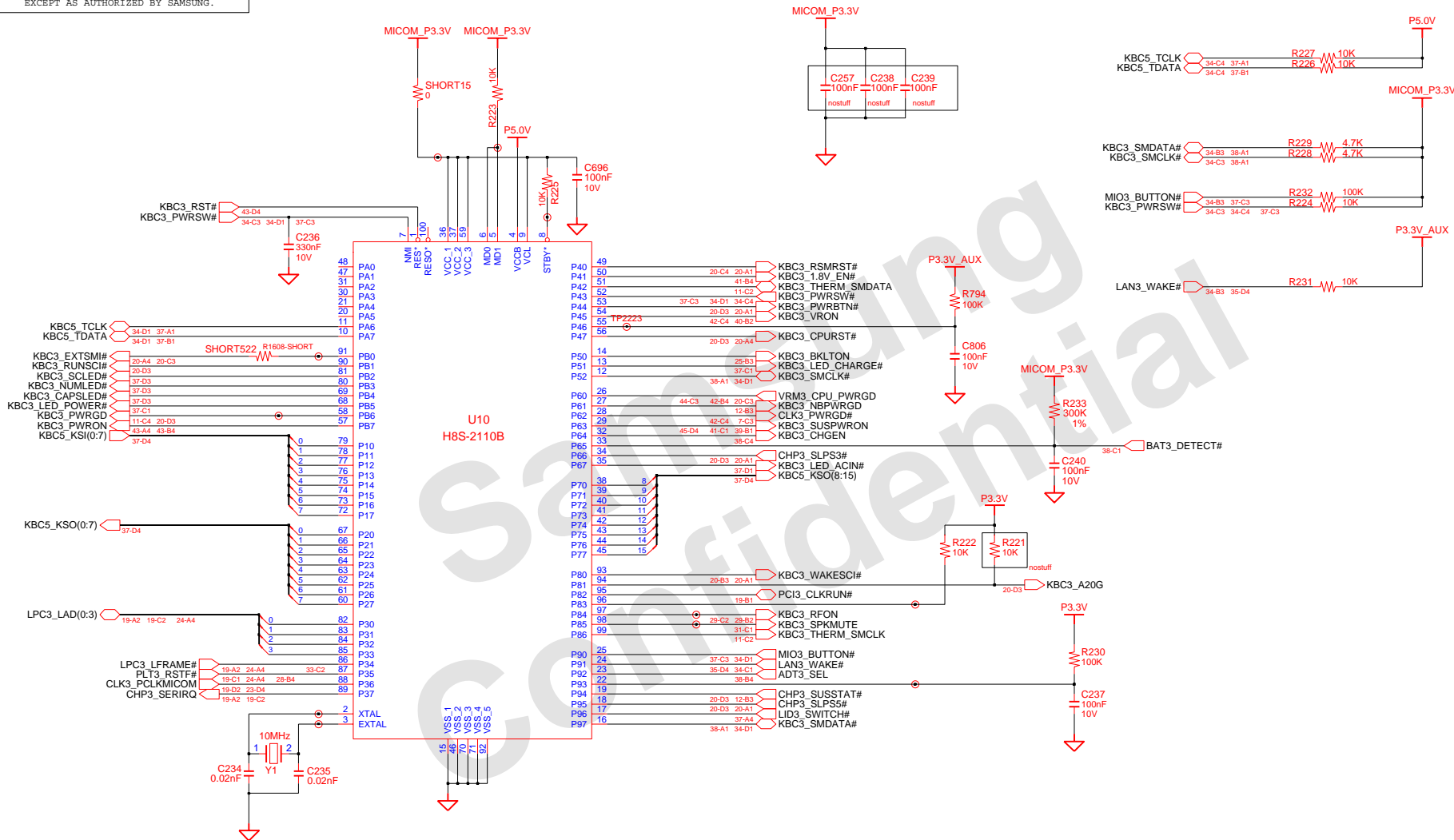
Main to ODD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER HDD & ODD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	33	OF 47

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**MICOM Crisis Update**  
 Condition: P90=P91=P92=High(MICOM\_P3V)  
 MD0=MD1=Low(0V)  
 Serial Port: P84 & P85

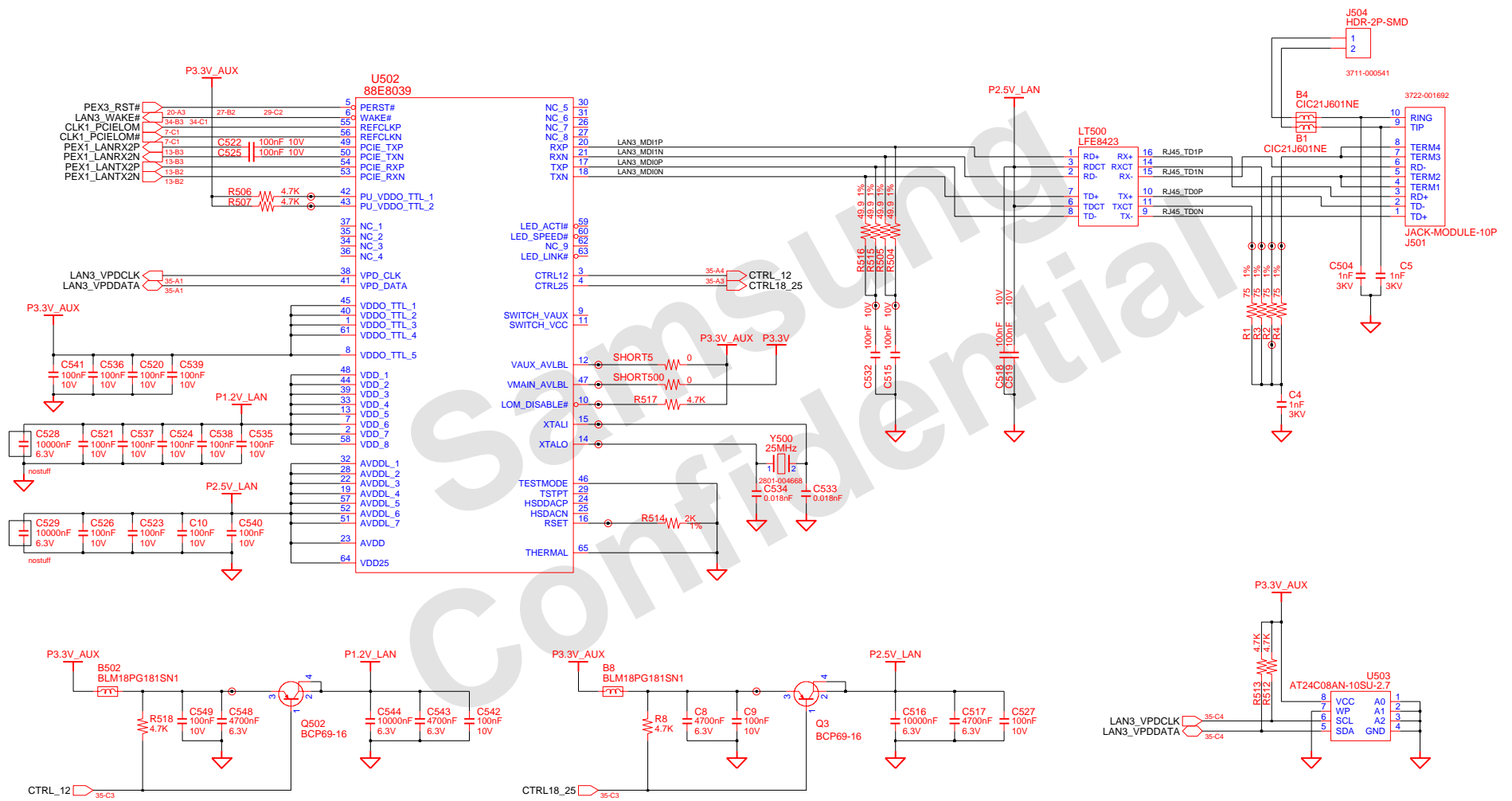
The removed signal compared from 144pin

- KBC5\_CAL\_THRM\*
- THRM\_ALERT\*
- LCD3\_BKLTEN
- FAN3\_FDBACK\*
- THERM\_STP\*

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		POWER	
APPROVAL	SJ PARK	REV	1.0		MICOM	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	34	OF 47

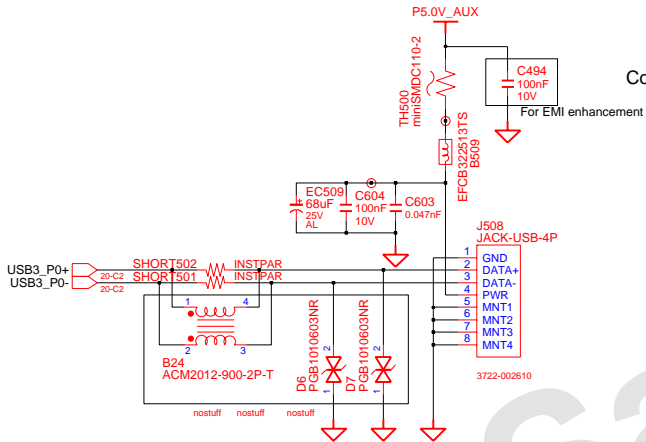
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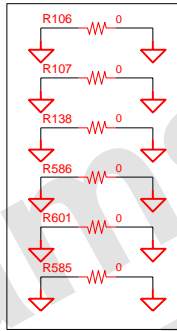
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CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	35	OF 47

## Side USB Connector



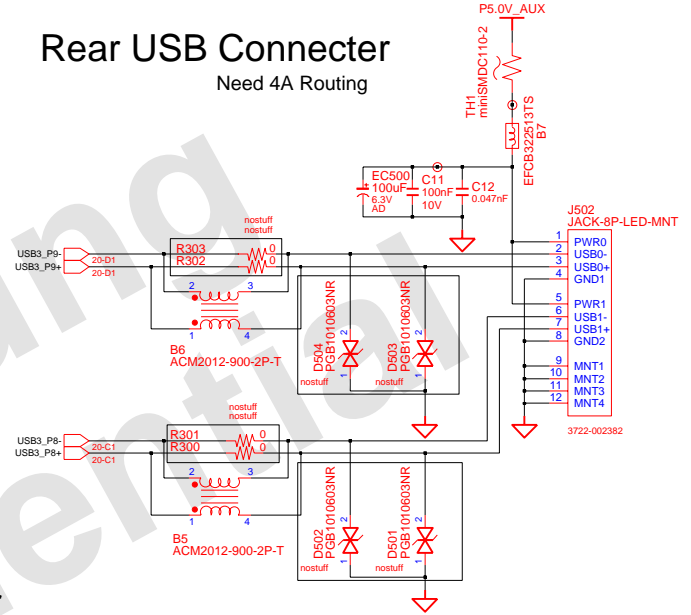
Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA

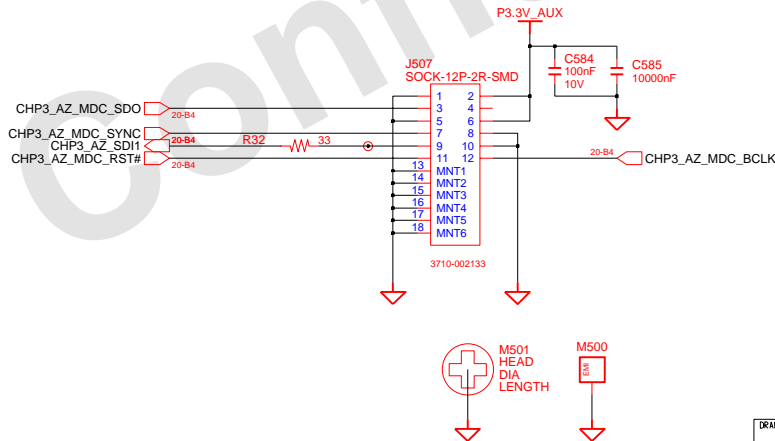


## Rear USB Connector

Need 4A Routing



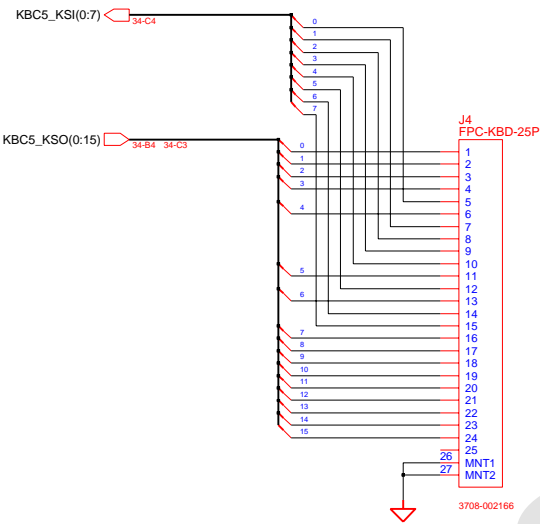
## MDC Connector



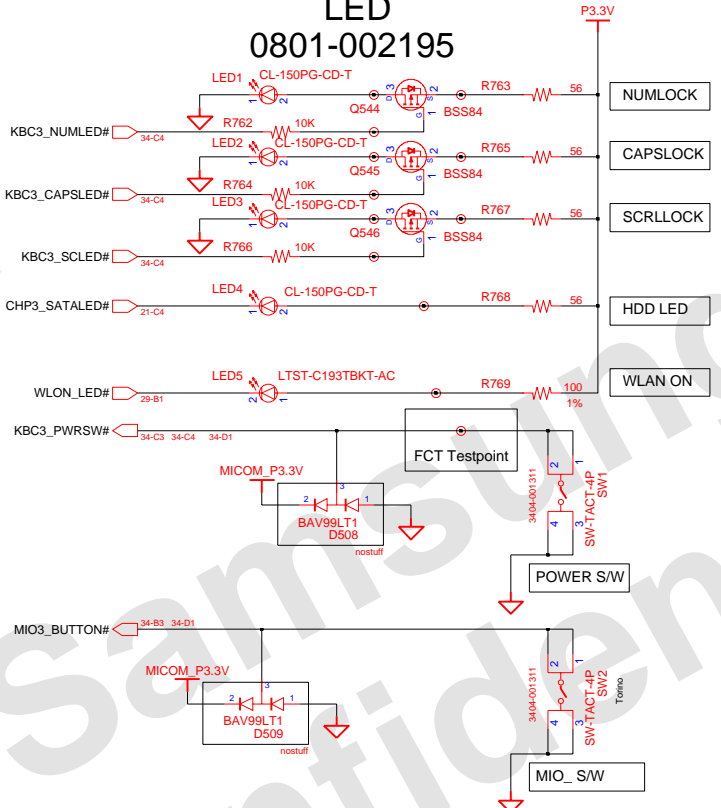
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	USB PORT & MDC Conn.		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA1A-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	36	OF 47

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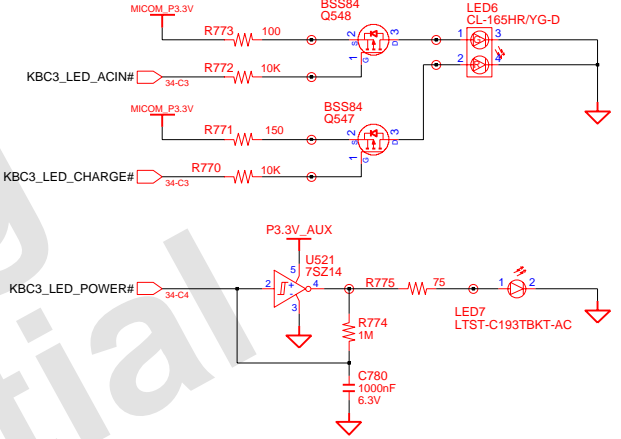
**KEYBOARD**



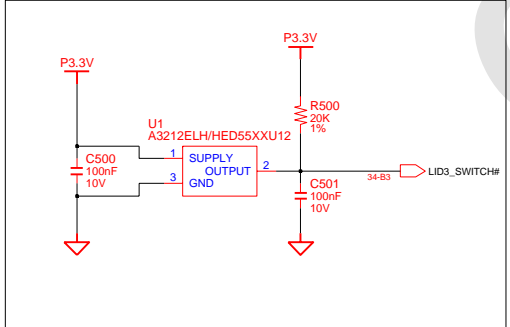
**LED 0801-002195**



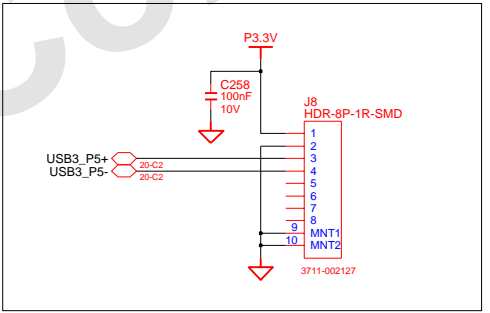
**ADAPTERIN/CHARGING LED**



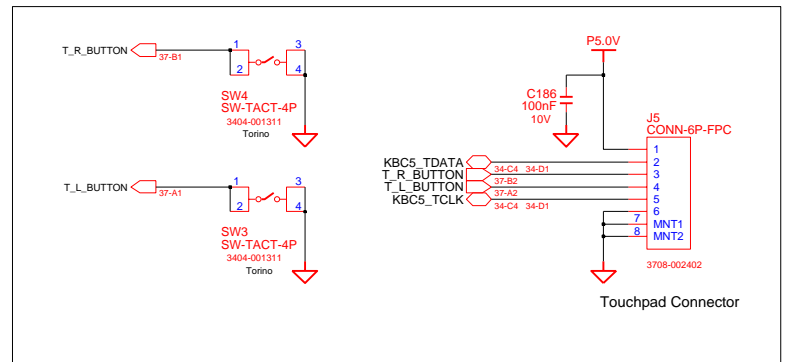
**LID SWITCH**



**Bluetooth Interface  
Factory Option**



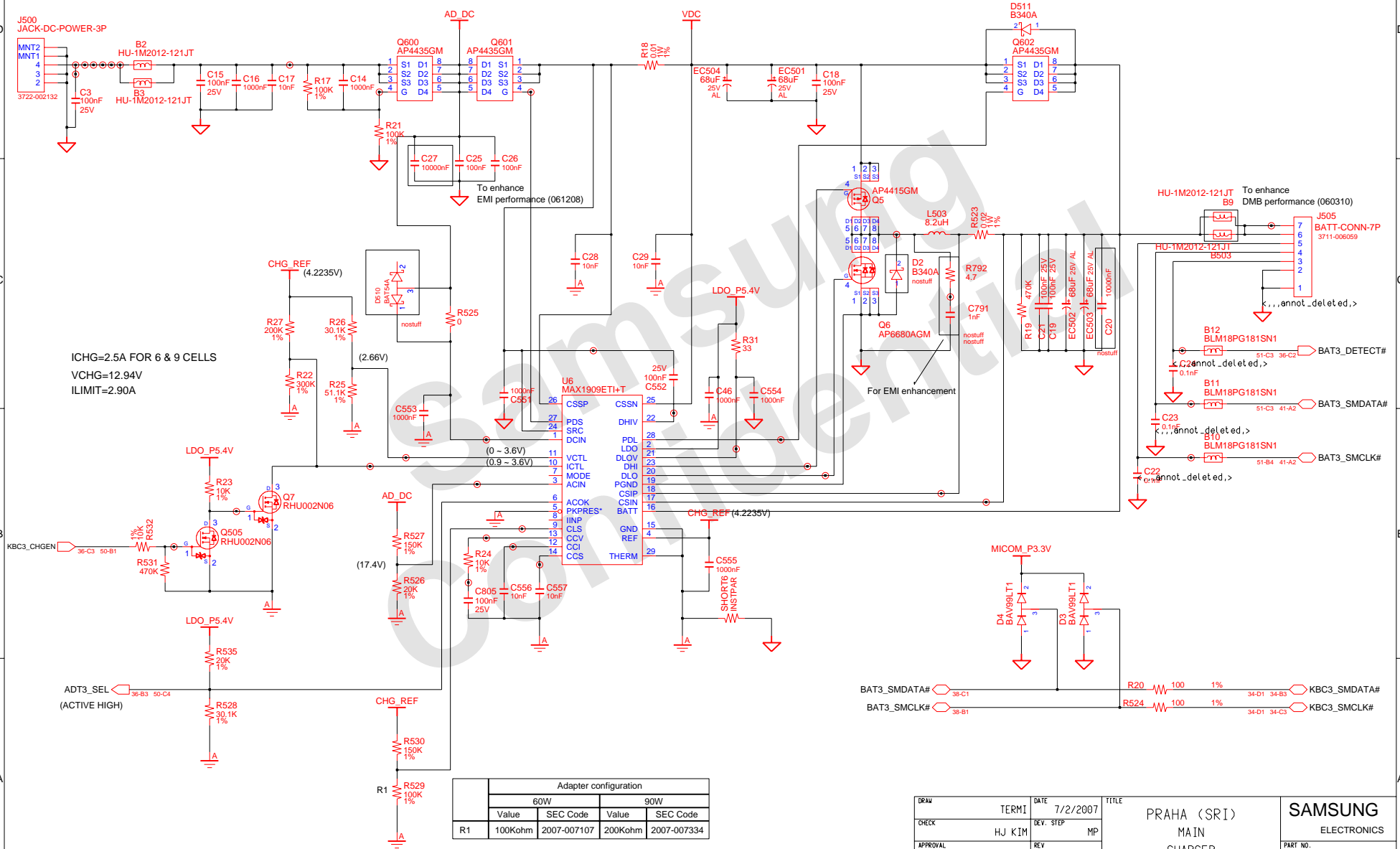
**TOUCHPAD**



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	LED & BLUETOOTH		
APPROVAL	SJ PARK	REV	1.0	TOUCHPAD & KBD & LID S/W		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	37	OF 47

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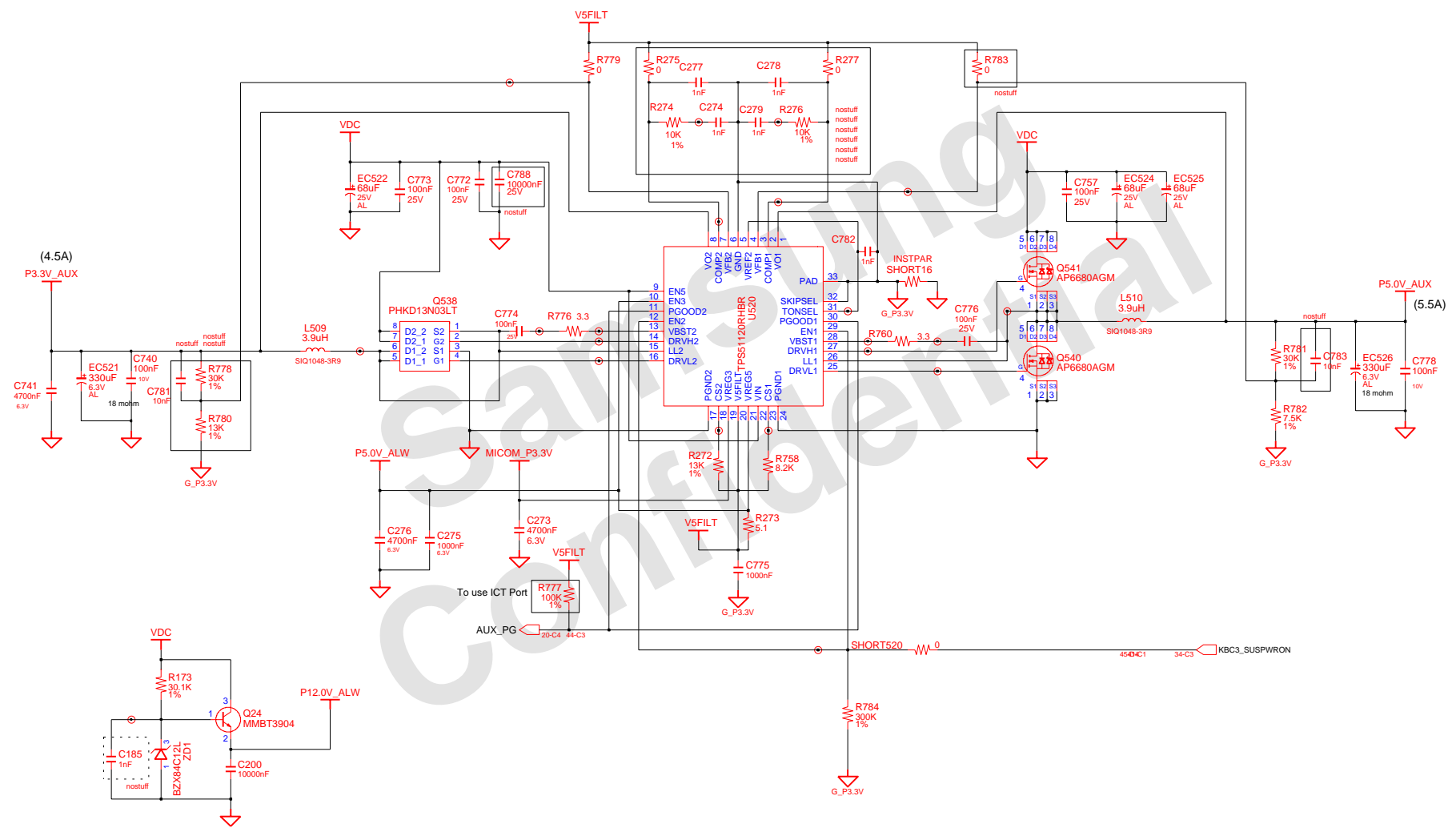
# CHARGER & POWER MANAGEMENT



GRW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		CHARGER	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	38	

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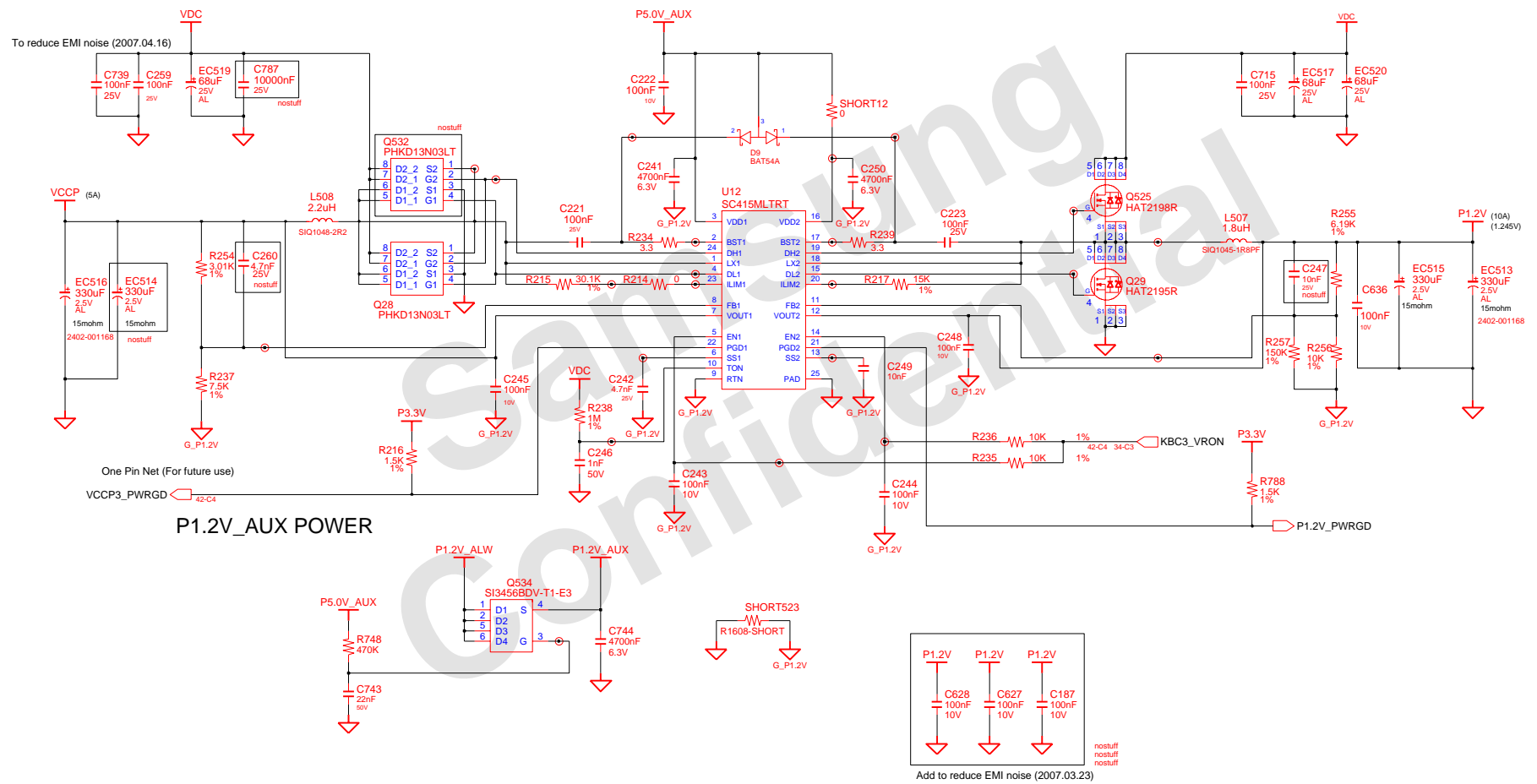
# P3.3V\_AUX & P5V\_AUX



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 39 OF 47
MODULE CODE	undefined					

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# P1.2V & VCCP\_CORE(1.05V)

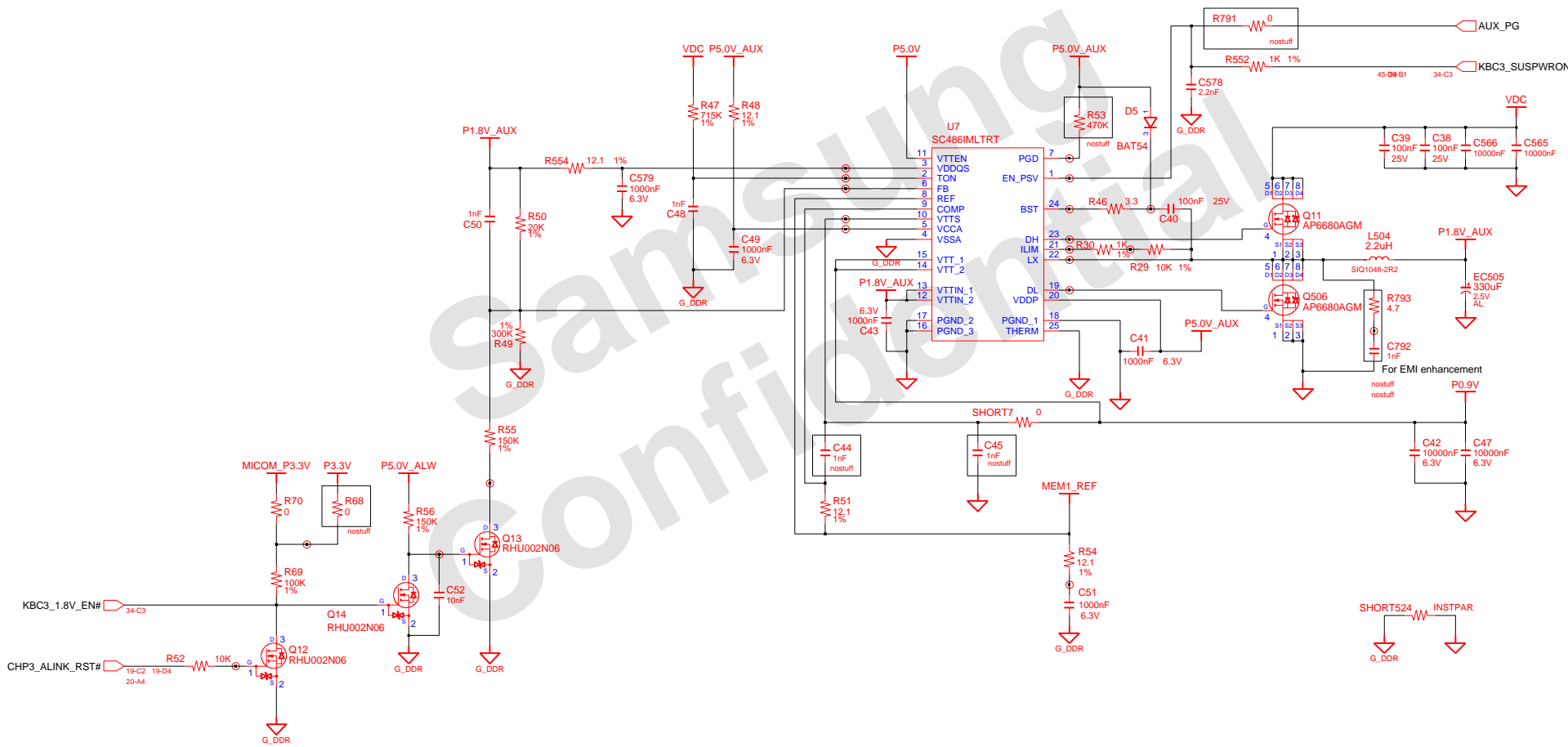


## P1.2V\_AUX POWER

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER	SAMSUNG ELECTRONICS
CHECK	HJ KIM	REV. STEP	MP	REV.		
APPROVAL	SJ PARK	REV	1.0	P1.2V & P1.2V_AUX & VCCP		PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	40	OF 17



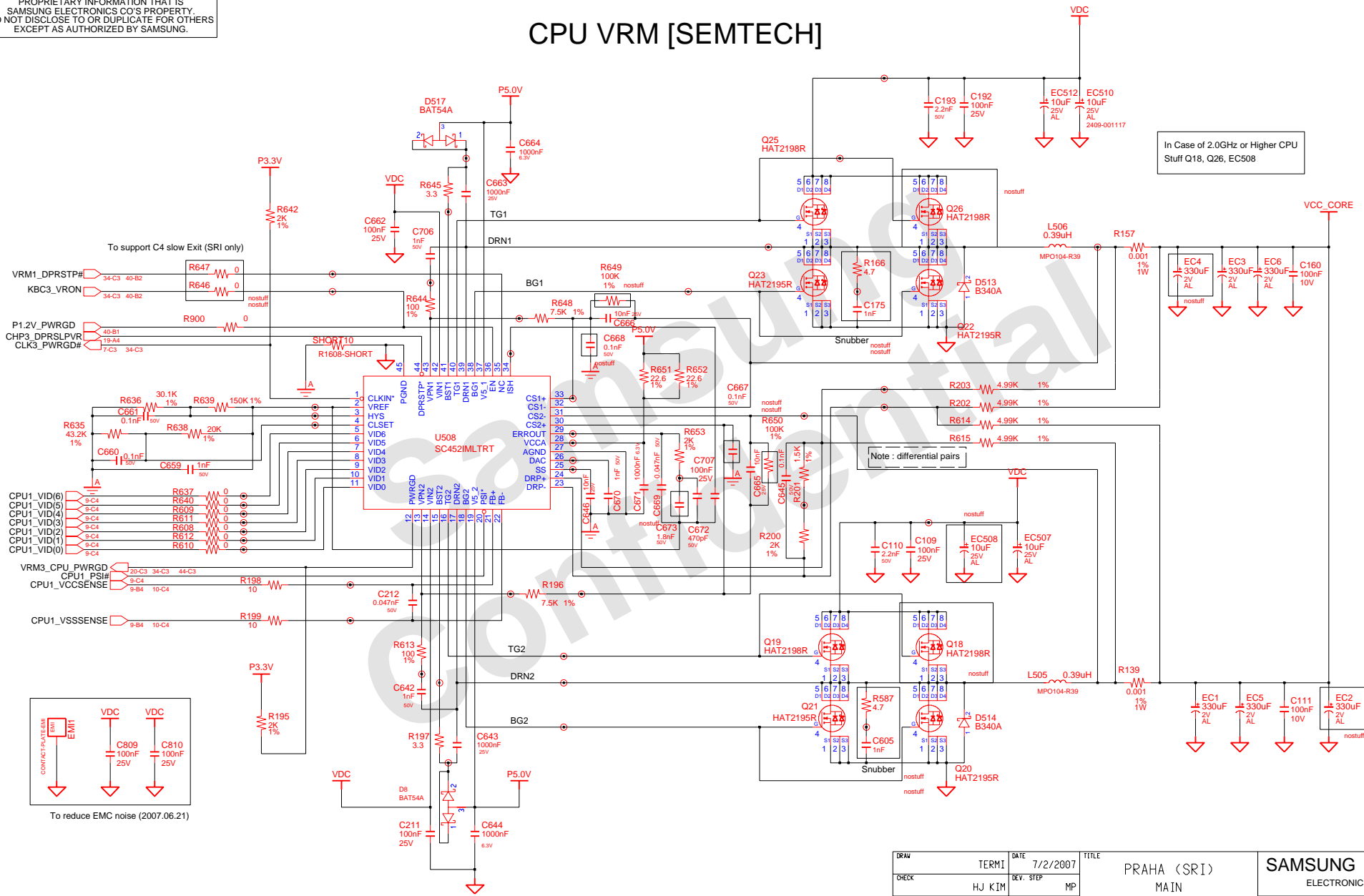
# DDR2 Power



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		DDR2 POWER	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	41	OF 47

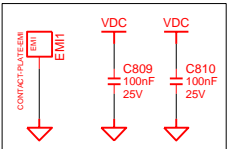
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# CPU VRM [SEMTECH]



In Case of 2.0GHz or Higher CPU  
 Stuff Q18, Q26, EC508

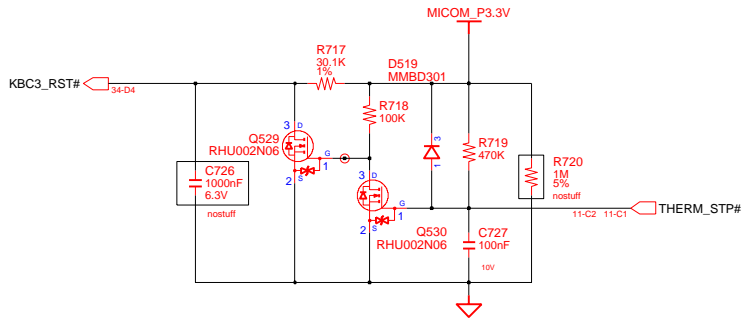
Note : differential pairs



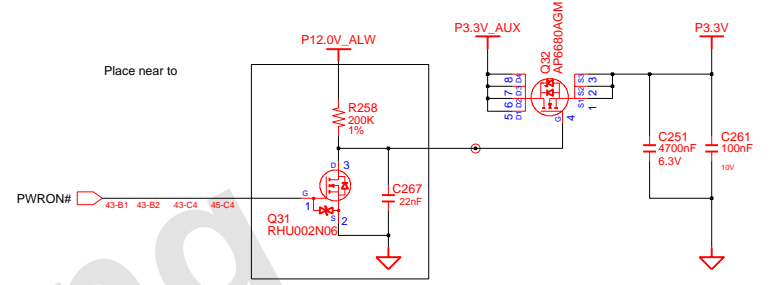
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	CPU VRM		PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	42	OF 17

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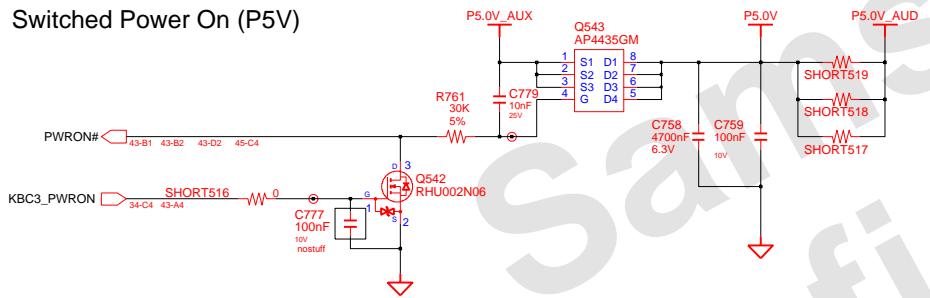
### MICOM RESET



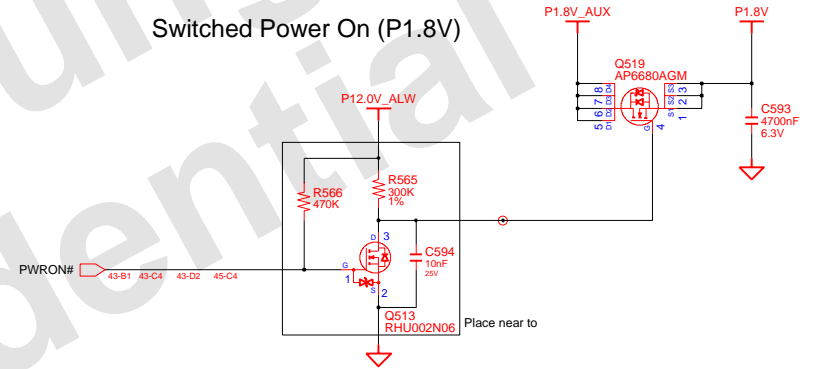
### Switched Power On (P3.3V)



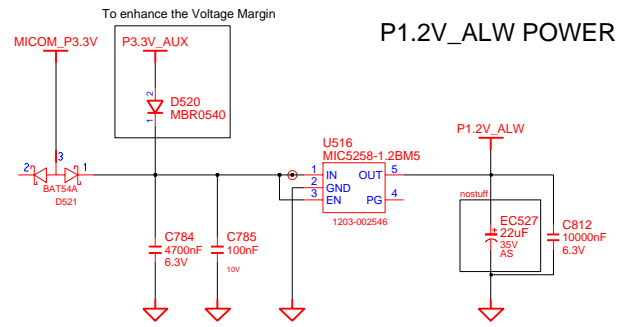
### Switched Power On (P5V)



### Switched Power On (P1.8V)



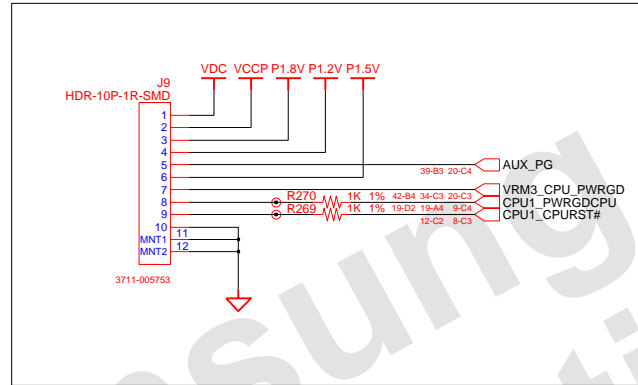
### P1.2V\_ALW POWER



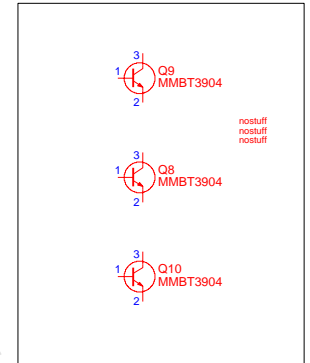
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MICOM & SWITCHED POWER		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	43	OF 47

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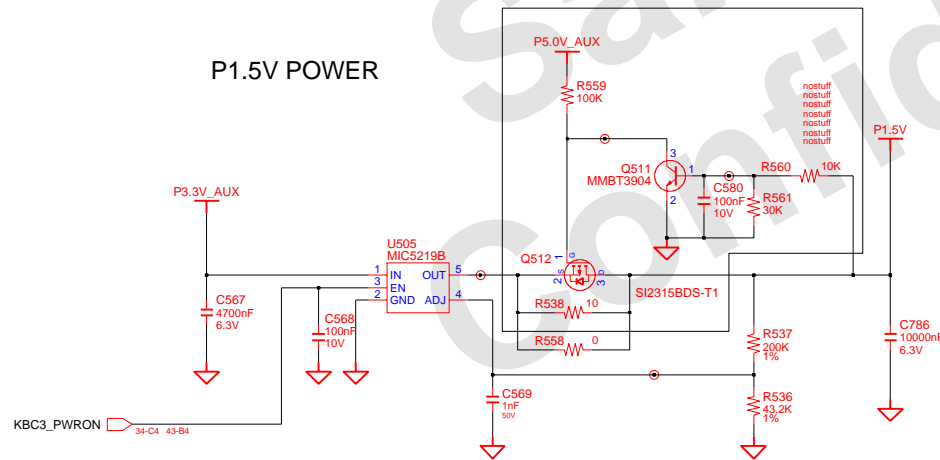
### ICT PORT



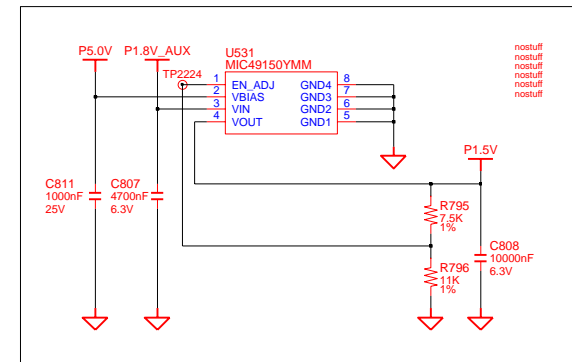
### For Debugging



### P1.5V POWER



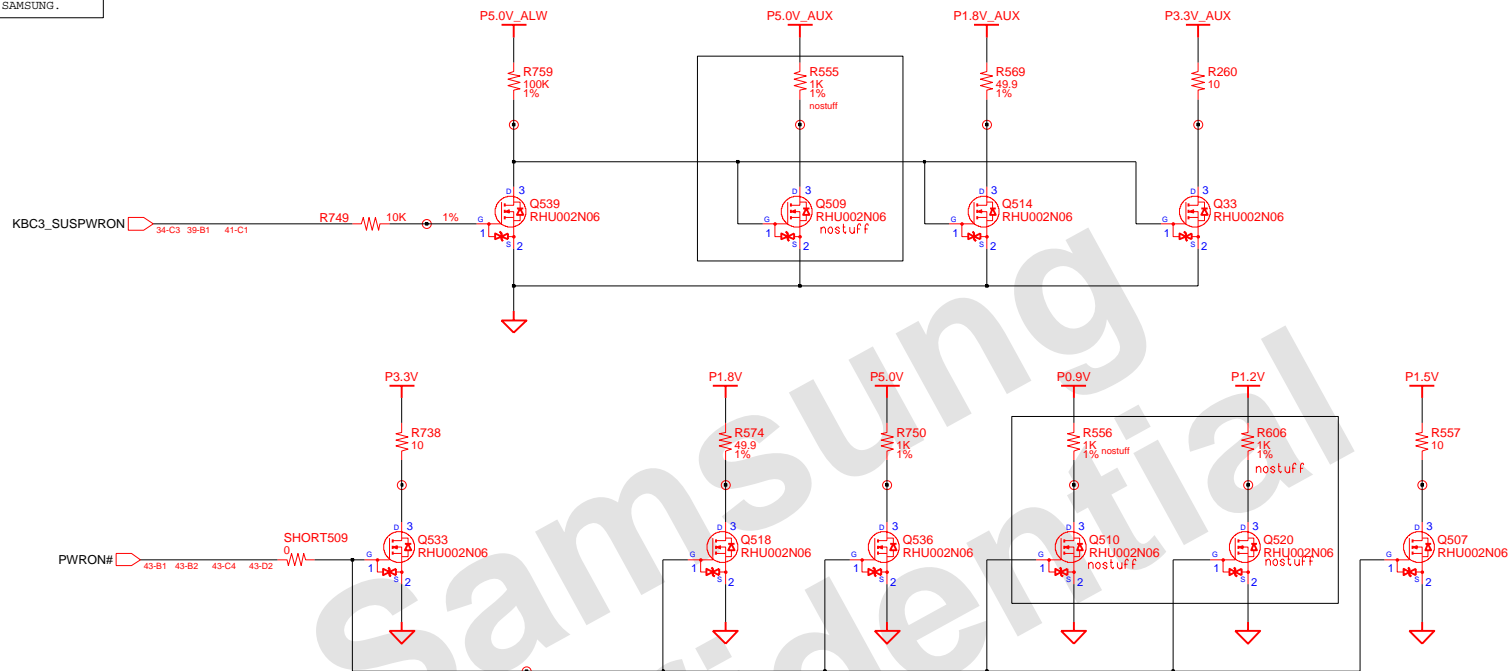
### To make up PCI Express 1.5V rail current margin (nostuff)



GRAM	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		ICT PORT	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			PAGE 44 OF 47

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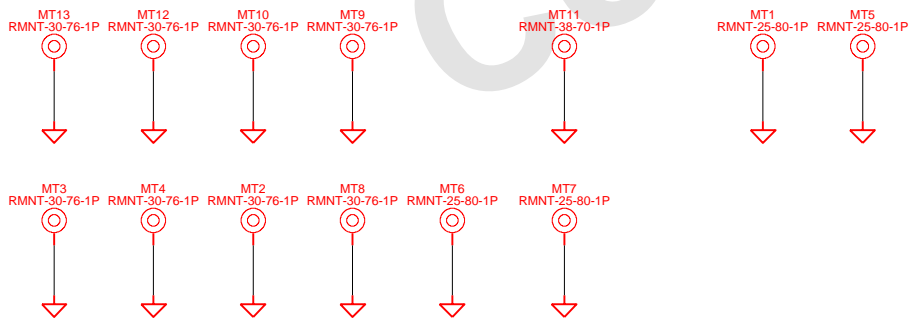
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**System**

**Board**

Located in lower left corner of PCB



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAINBD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	POWER DRAW & MNT HOLE		
APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A		PAGE 45 OF 47
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			

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REV1  
 1 O  
 2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		TP	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	46	OF 47

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○AC\_SDOUT  
 ○AUD3\_SEL  
 ○AUD3\_EAPD#  
 ○AUD3\_PCBEPP#  
 ○AUD5\_LINE\_OUT\_L  
 ○AUD5\_LINE\_OUT\_R  
 ○AUD5\_MONO\_OUT  
 ○AUD5\_SPK\_L+  
 ○AUD5\_SPK\_L-  
 ○AUD5\_SPK\_R+  
 ○AUD5\_SPK\_R-  
 ○AUX\_PG  
 ○BAT3\_DETECT#  
 ○BAT3\_SMCLK#  
 ○BAT3\_SMDATA#  
 ○CHP3\_ALINK\_RST#  
 ○CHP3\_AZ\_AUD\_BCLK  
 ○CHP3\_AZ\_AUD\_RST#  
 ○CHP3\_AZ\_AUD\_SDO  
 ○CHP3\_AZ\_AUD\_SYNC  
 ○CHP3\_AZ\_MDC\_BCLK  
 ○CHP3\_AZ\_MDC\_RST#  
 ○CHP3\_AZ\_MDC\_SDO  
 ○CHP3\_AZ\_MDC\_SYNC  
 ○CHP3\_AZ\_SDIO  
 ○CHP3\_AZ\_SDIO1  
 ○CHP3\_BIOSWP#  
 ○CHP3\_DPRSPLPWR  
 ○CHP3\_NBRST#  
 ○CHP3\_SATALED#  
 ○CHP3\_SBPME#  
 ○CHP3\_SBTHERMTRIP#  
 ○CHP3\_SERIRO  
 ○CHP3\_SLPS3#  
 ○CHP3\_SLPS5#  
 ○CHP3\_SPKR  
 ○CHP3\_SUSSTAT#  
 ○CPU1\_A2OM#  
 ○CPU1\_ADS#  
  
 ○CPU1\_BNR#  
 ○CPU1\_BPRI#  
 ○CPU1\_BREQ#  
 ○CPU1\_BSEL0  
 ○CPU1\_BSEL1  
 ○CPU1\_BSEL2  
 ○CPU1\_CPURST#  
 ○CLK3\_DBGCLPC  
 ○CLK3\_IQH14  
 ○CLK3\_NB14M  
 ○CLK3\_PCLKMICOM  
 ○CLK3\_PWRGD#  
 ○CLK3\_USB48  
  
 ○CPU1\_DBSY#  
 ○CPU1\_DEFR#  
 ○CPU1\_DPRS1P#  
 ○CPU1\_DPSLP#  
 ○CPU1\_DPWR#  
 ○CPU1\_DRDY#

○CPU1\_FERR#  
 ○CPU1\_HIT#  
 ○CPU1\_HITM#  
 ○CPU1\_IGNNE#  
 ○CPU1\_INIT#  
 ○CPU1\_INTR#  
 ○CPU1\_LOCK#  
 ○CPU1\_NMI#  
 ○CPU1\_PSI#  
 ○CPU1\_PWRGDCCPU  
  
 ○CPU1\_RS0#  
 ○CPU1\_RS1#  
 ○CPU1\_RS2#  
 ○CPU1\_SLP#  
 ○CPU1\_SMI#  
 ○CPU1\_TCK  
 ○CPU1\_TDI  
 ○CPU1\_THERMTRIP#  
 ○CPU1\_TMS  
 ○CPU1\_TRDY#  
 ○CPU1\_TRST#  
 ○CPU1\_VCCSENSE  
 ○CPU1\_VID(0)  
 ○CPU1\_VID(1)  
 ○CPU1\_VID(2)  
 ○CPU1\_VID(3)  
 ○CPU1\_VID(4)  
 ○CPU1\_VID(5)  
 ○CPU1\_VID(6)  
 ○CPU1\_VSSSENSE  
 ○CPU2\_THERMADA  
 ○CPU2\_THERMDC  
 ○CPU3\_THERMTRIP#  
 ○CRT3\_BLUE  
 ○CRT3\_DDCCLK  
 ○CRT3\_DODDATA  
 ○CRT3\_GREEN  
 ○CRT3\_RED  
 ○CRT5\_HSYNC  
 ○CRT5\_VSYNC  
 ○CTRL18\_25  
 ○CTRL12  
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 ○EXP3\_CPPE#

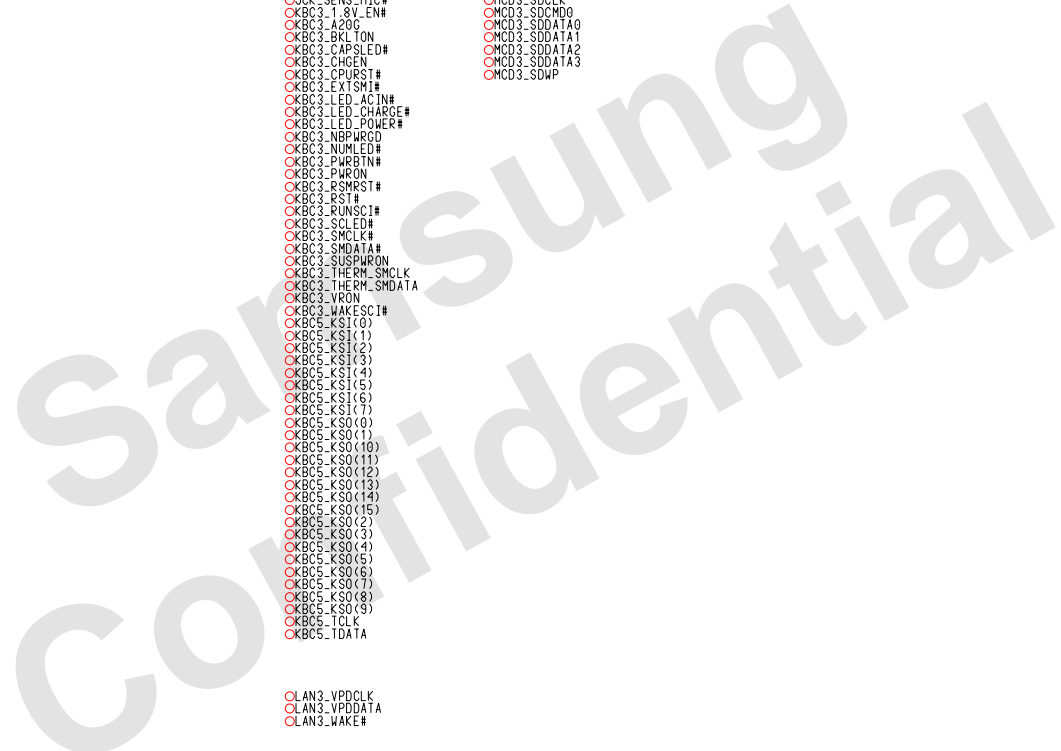
○EXP3\_CPUSB#  
 ○EXP3\_PERST#  
 ○FANS\_FBEEP#  
 ○FANS\_VDD  
 ○GPIO1  
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 ○HP\_OUT\_R  
 ○ITP3\_DBRESET#  
 ○ITP3\_SYSRST#  
 ○JCK\_SENS\_A  
 ○JCK\_SENS\_HP#  
 ○JCK\_SENS\_MIC#  
 ○KBC3\_18V\_EN#  
 ○KBC3\_A20G  
 ○KBC3\_BKLTON  
 ○KBC3\_CAPSLED#  
 ○KBC3\_CHGEN  
 ○KBC3\_CPURST#  
 ○KBC3\_EXTSMI#  
 ○KBC3\_LED\_ACIN#  
 ○KBC3\_LED\_CHARGE#  
 ○KBC3\_LED\_POWER#  
 ○KBC3\_NBPWRGD  
 ○KBC3\_NUMLED#  
 ○KBC3\_PWRBTN#  
 ○KBC3\_PWRON  
 ○KBC3\_SMRST#  
 ○KBC3\_RST#  
 ○KBC3\_RUNSCI#  
 ○KBC3\_SCLE#  
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 ○KBC3\_SUSPWRON  
 ○KBC3\_THERM\_SMCLK  
 ○KBC3\_THERM\_SMDATA  
 ○KBC3\_VIRON  
 ○KBC3\_WAKESC1#  
 ○KBC5\_KSI(0)  
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 ○KBC5\_KSO(7)  
 ○KBC5\_KSO(8)  
 ○KBC5\_KSO(9)  
 ○KBC5\_TCLK  
 ○KBC5\_TDATA

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 ○LAN3\_VPDDATA  
 ○LAN3\_WAKE#

○LCD3\_BKLTCTRL  
 ○LCD3\_BKLTEN

○LCD3\_BKLTON  
 ○LCD3\_EDID\_CLK  
 ○LCD3\_EDID\_DATA  
 ○CD3\_VDDEN  
 ○ID3\_SWITCH#  
 ○PC3\_LAD(0)  
 ○PC3\_LAD(1)  
 ○PC3\_LAD(2)  
 ○PC3\_LAD(3)  
 ○PC3\_LFRAME#  
 ○MCD3\_SDCD#  
 ○MCD3\_SDCLK  
 ○MCD3\_SDCMD0  
 ○MCD3\_SDDATA0  
 ○MCD3\_SDDATA1  
 ○MCD3\_SDDATA2  
 ○MCD3\_SDDATA3  
 ○MCD3\_SDWP

○MIC1  
 ○MIC2  
 ○MINIPCIE3\_CLKREQ#  
 ○MIO3\_BUTTON#



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	47	OF 47

