

Stanford_14/15

CPU : C-ULV
Chip Set : CANTIGA GS & ICH9M SFF
Remarks : INTEL MONTEVINA SFF

Model Name : Stanford_DDR3
**PCB Part No : BA41-01119A (GCE)
 BA41-01120A (NY)**
Dev. Step : PVR
Revision : 1.0
T.R. Date : 2009.07.06

DRAW	CHECK	APPROVAL

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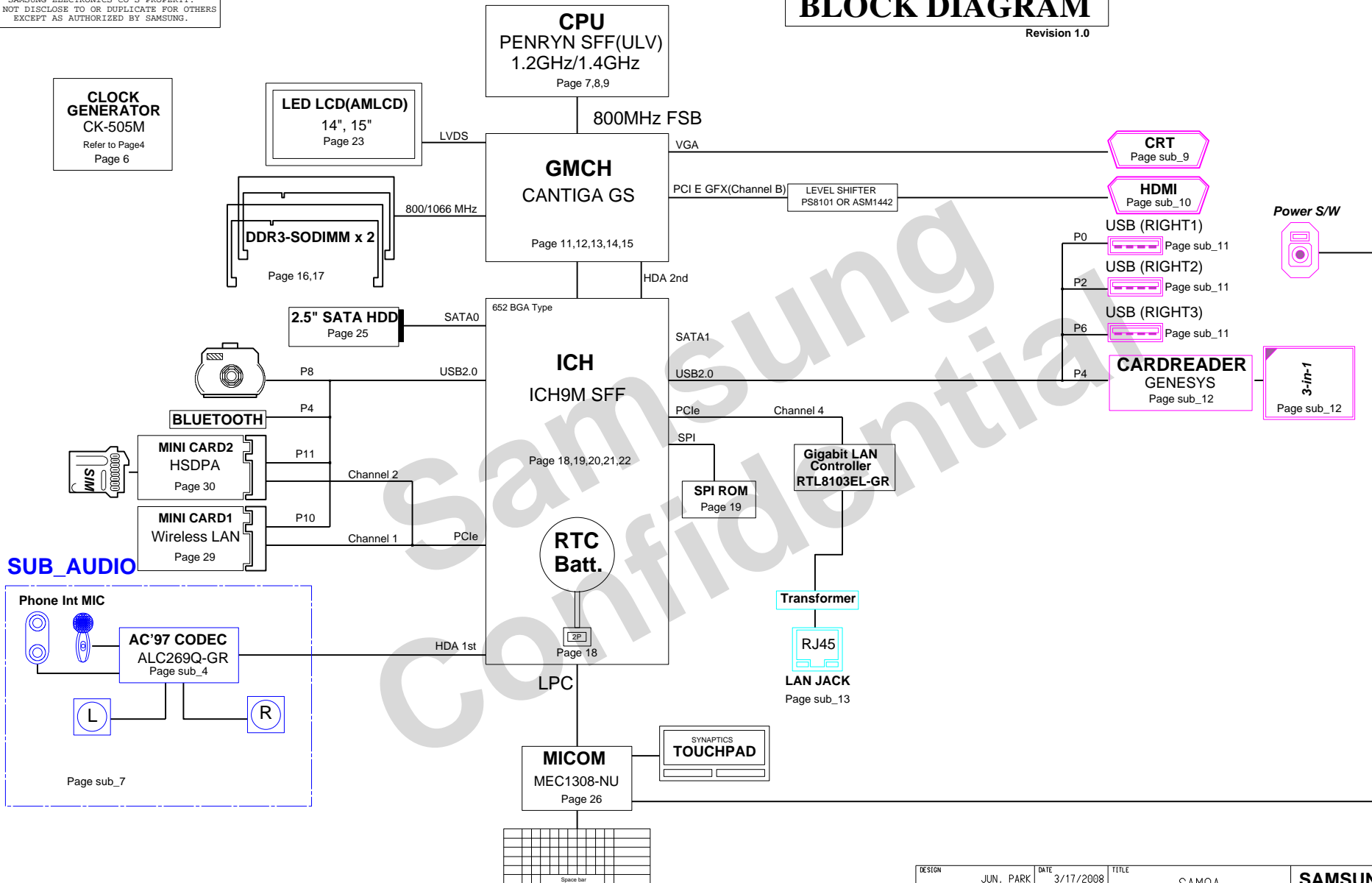
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CHECK HJ, KIM	DEV. STEP MP			
APPROVAL JS, EUH	REV 1.5			PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 1	OF 44

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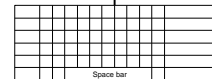
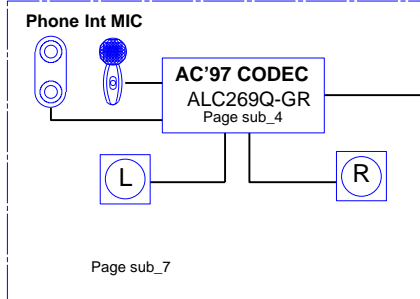
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BLOCK DIAGRAM

Revision 1.0



SUB_AUDIO



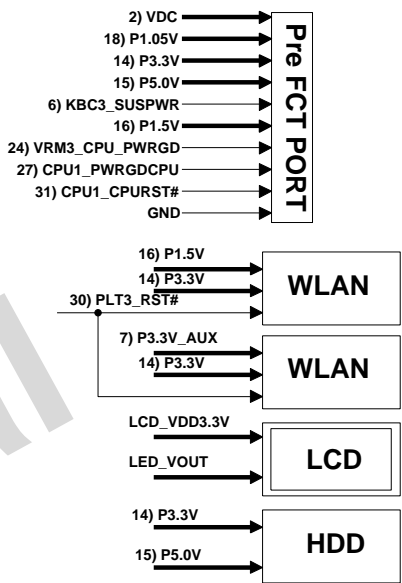
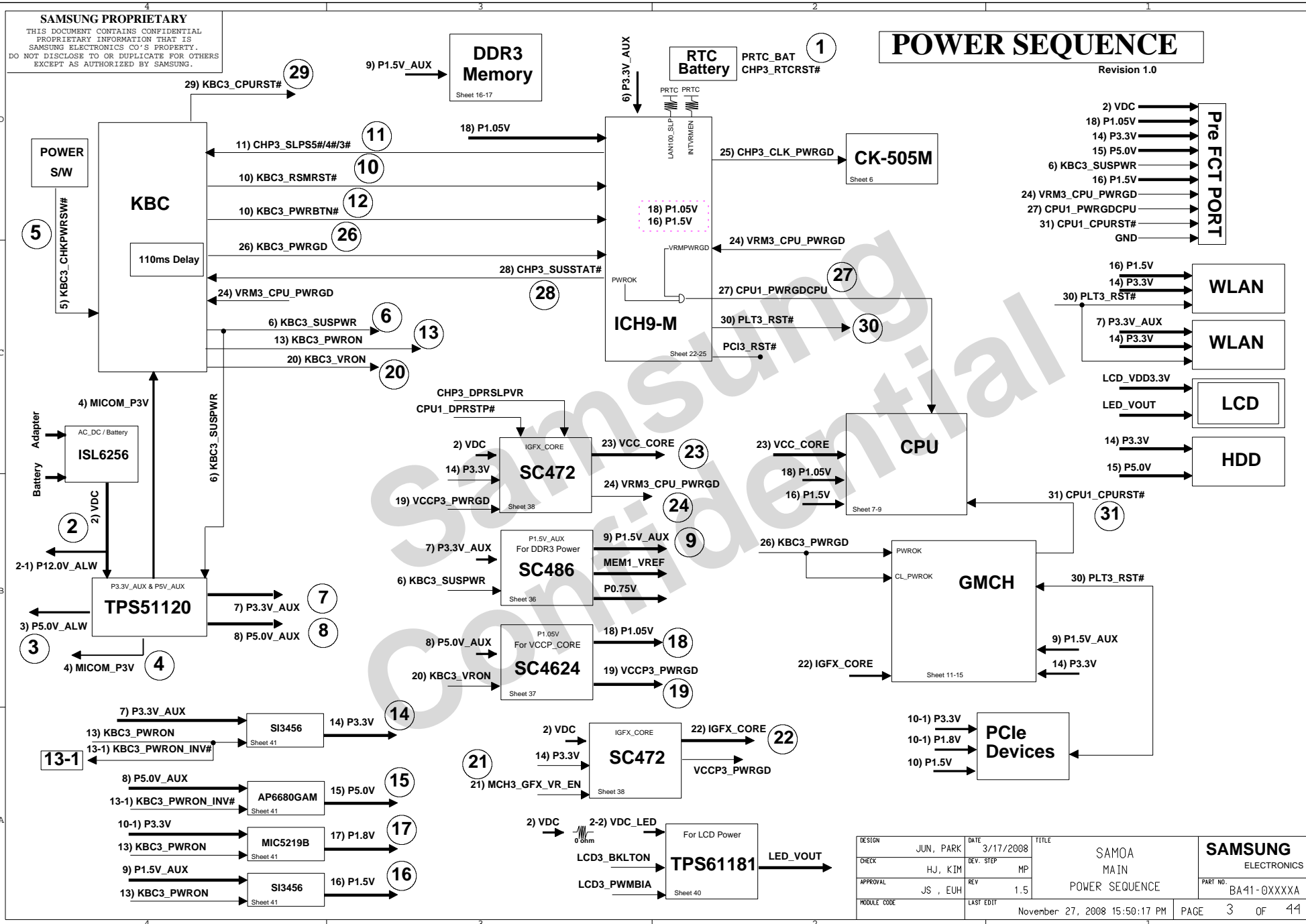
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POWER SEQUENCE

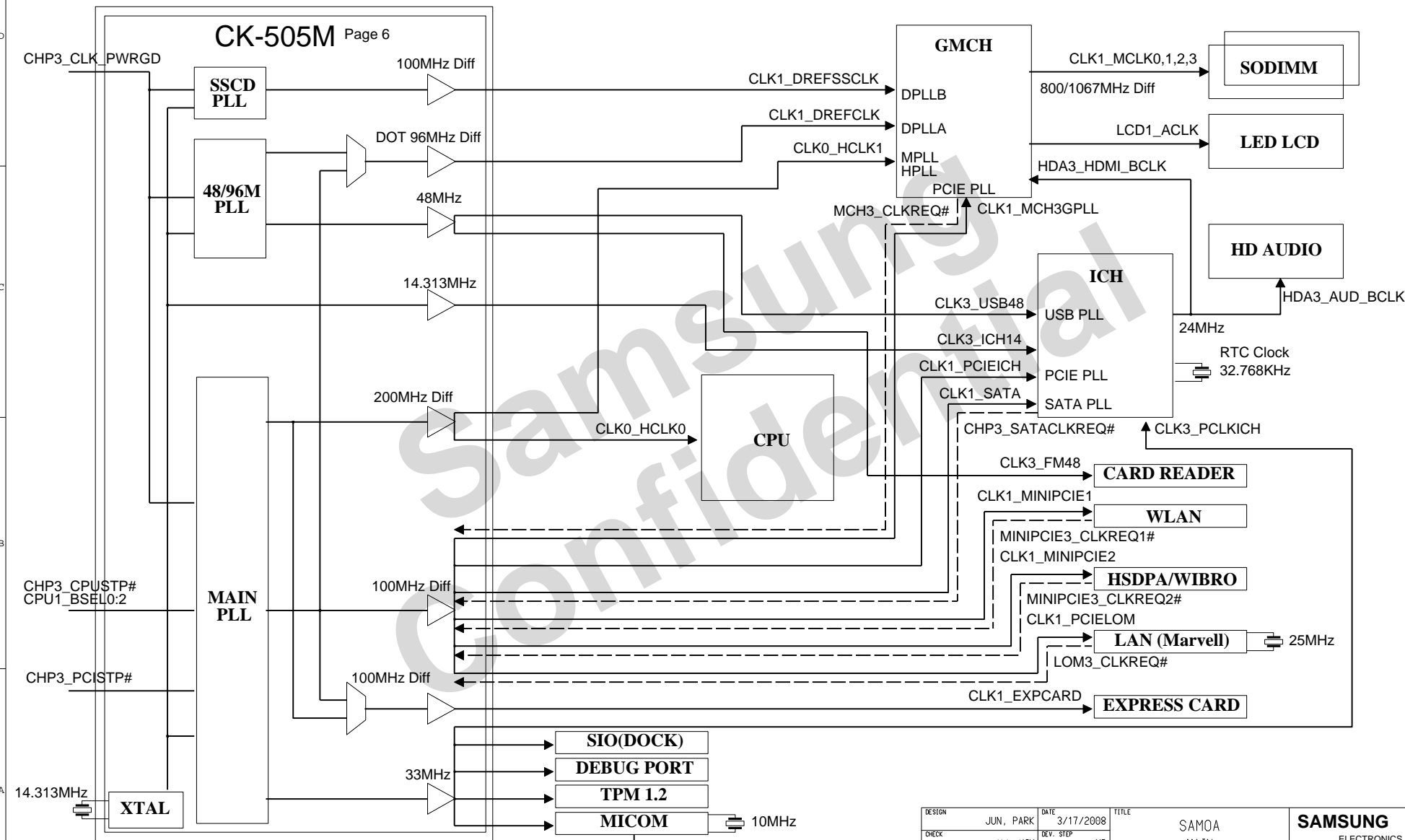
Revision 1.0



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CHECK	HJ, KIM	DEV. STEP	MP	REV		
APPROVAL	JS, EUH	REV	1.5	LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 3 OF 44
MODULE CODE						

CLOCK DISTRIBUTION

Revision 1.0



TOUCHPAD, THERMAL MONITOR, BATTERY, PS2_DOCK

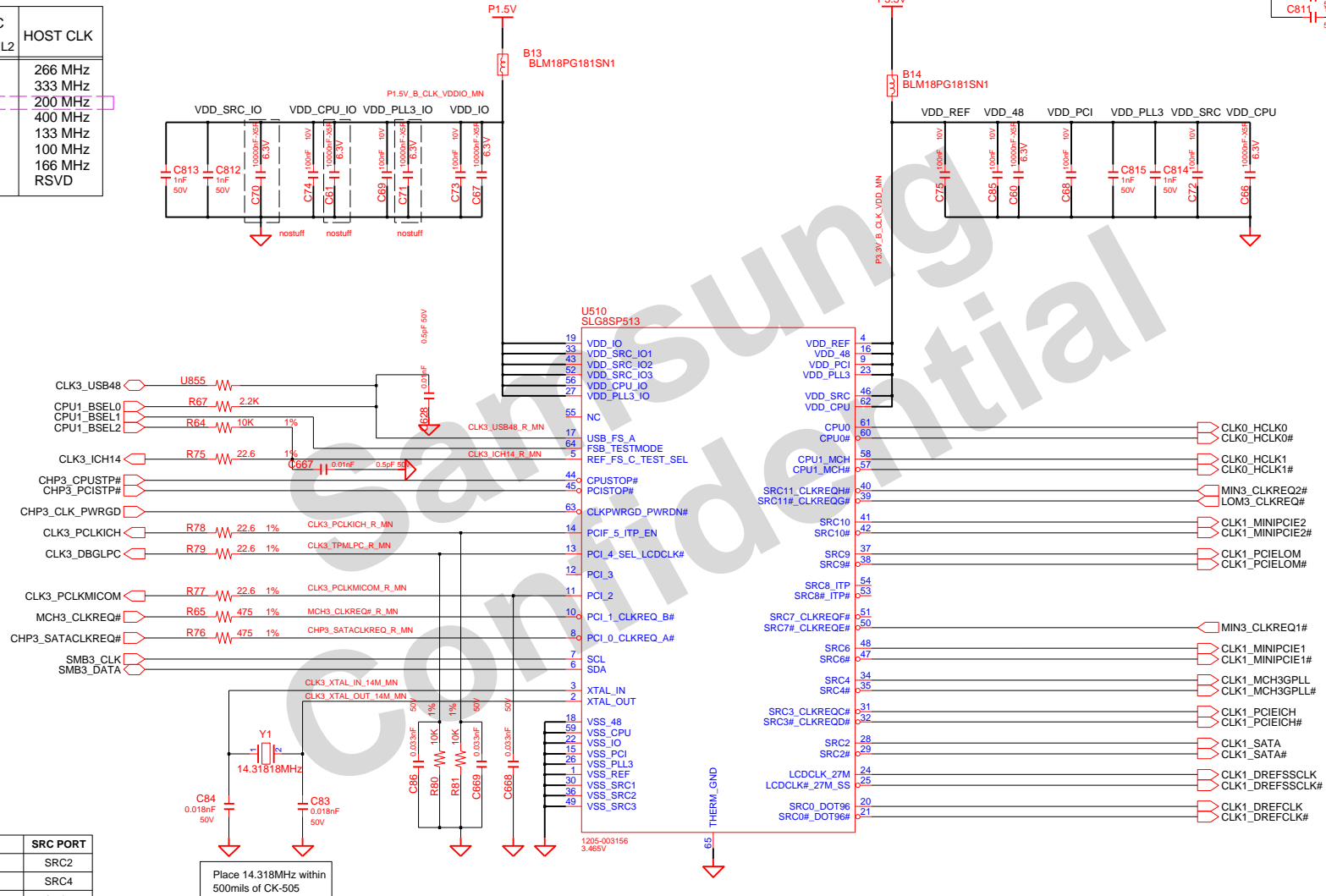
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APPROVAL	JS, EUH	REV	1.5			PART NO. BA41-0XXXXA
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CK505M

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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



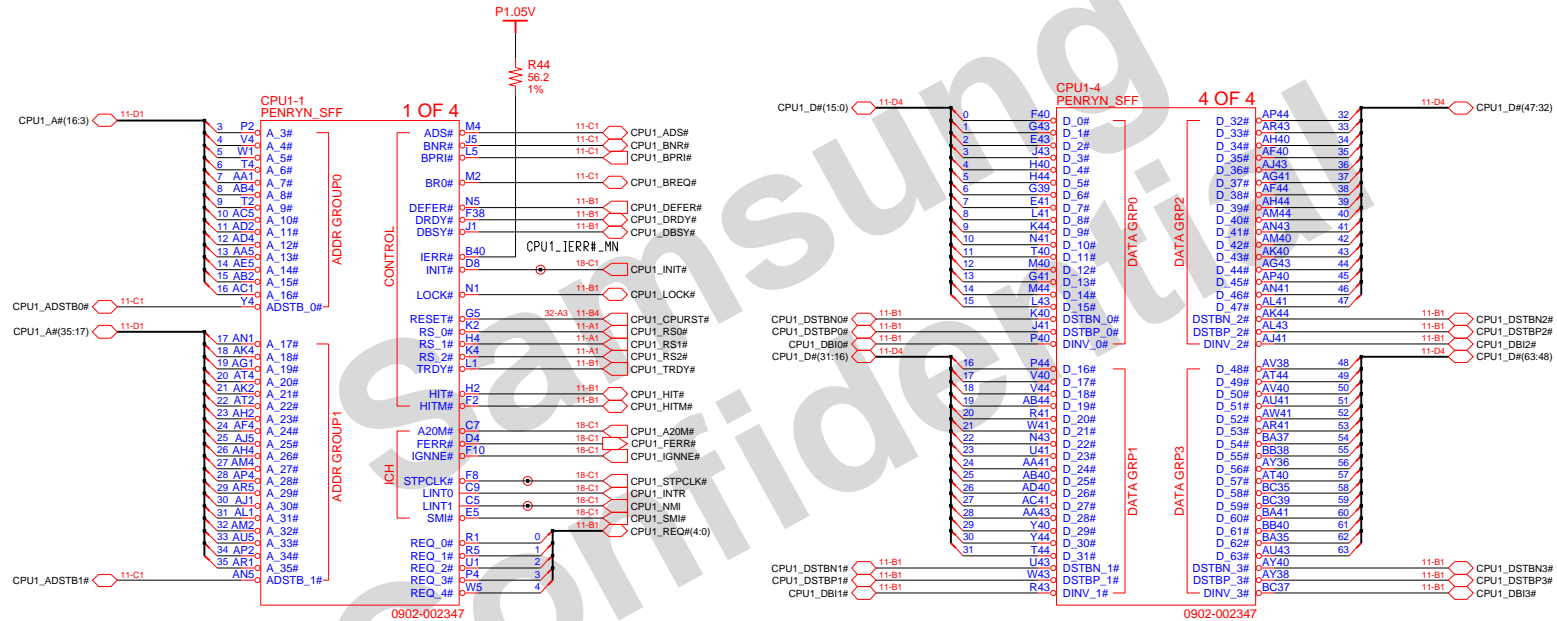
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

This part is 64pin QFN package.

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT				
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ULV CPU(Penryn SFF)



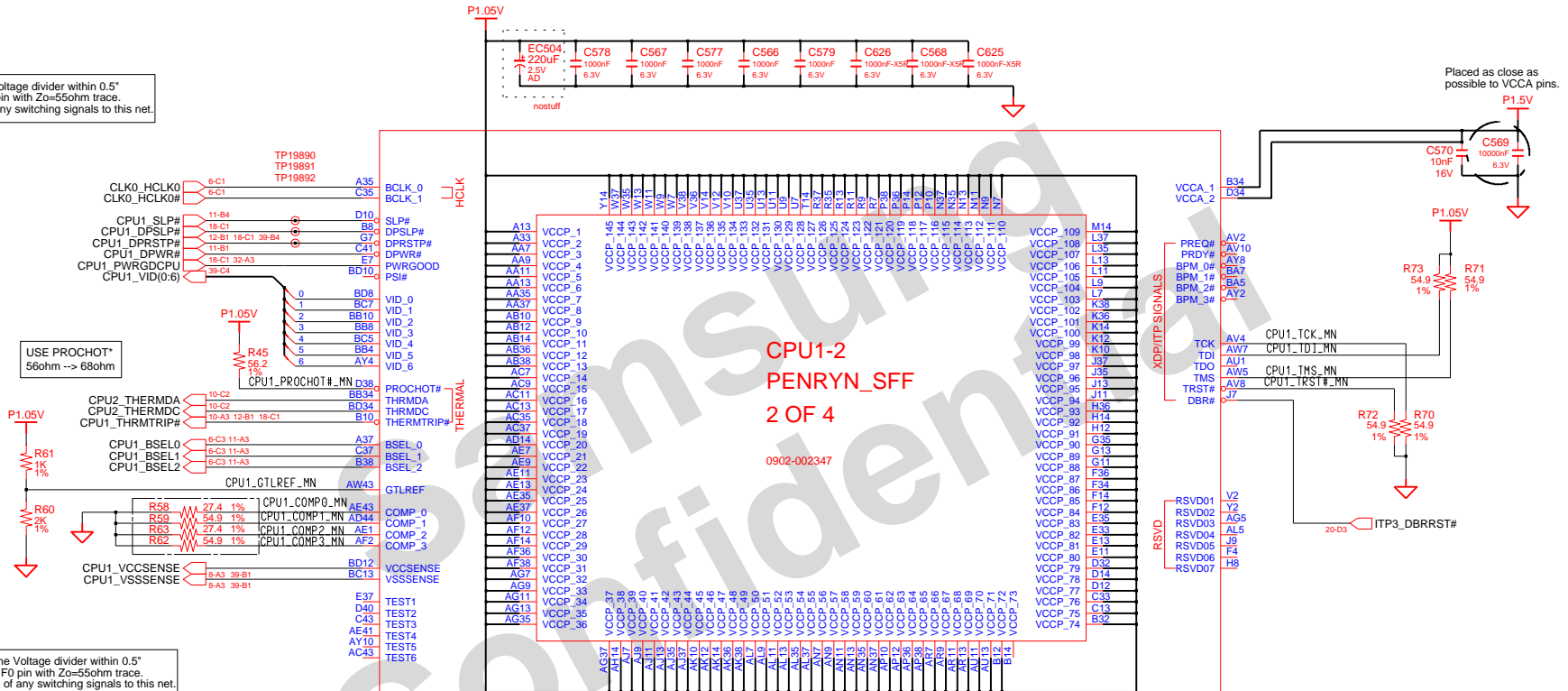
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN PENRYN ULV CPU(1/3)	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE	7	OF 44

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ULV CPU(Penryn SFF)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.



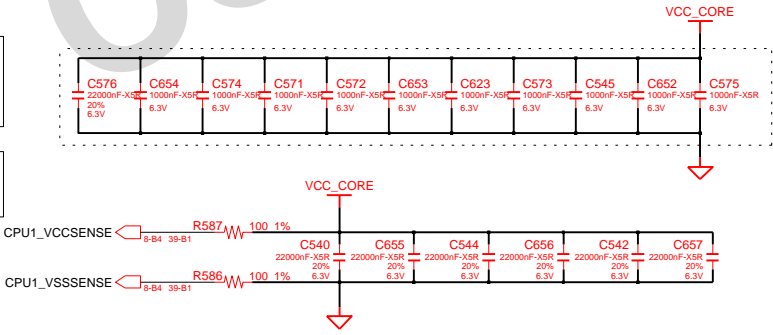
USE PROCHOT* 56ohm --> 68ohm

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Biasis socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

VCC/VSSsense lines between the Penryn CPU and the VR should have a trace width of 18mils on 7mil spacing with trace impedance of Zo=27.4ohm Place PU and PD within 1 inch of CPU



noستuff noستuff
noستuff noستuff
noستuff noستuff
noستuff noستuff
noستuff noستuff
noستuff noستuff
noستuff noستuff

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PENRYN ULV CPU(2/3)		
APPROVAL	JS, EUH	REV	1.5			PART NO. BA41-0XXXXA
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ULV CPU(Penryn SFF)

VCC_CORE

Table of pin connections for VCC_CORE, listing pin numbers and corresponding labels like AA33, AB16, AB20, etc.

CPU1-3
PENRYN_SFF
3 OF 4

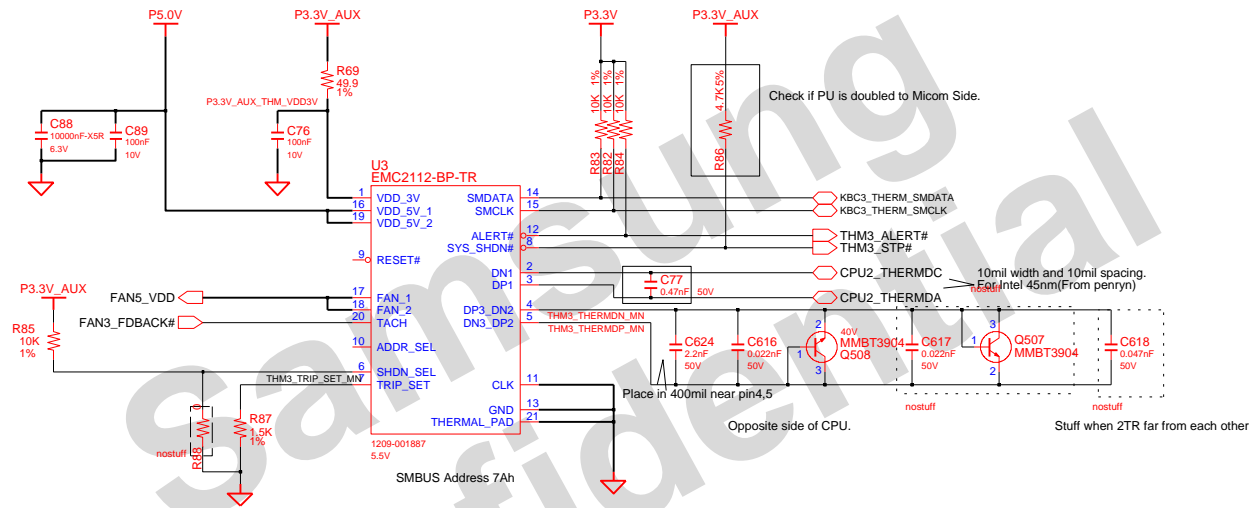
0902-002347

Table of pin connections for CPU1-3, listing pin numbers and corresponding labels like A5, A7, A9, etc.

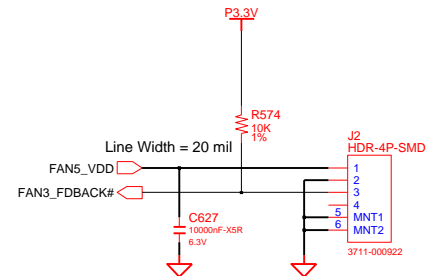
Table of pin connections for CPU1-3, listing pin numbers and corresponding labels like AR3, AR15, AR16, etc.

Table of pin connections for CPU1-3, listing pin numbers and corresponding labels like E19, E21, E22, etc.

THERMAL SENSOR & FAN CONTROL

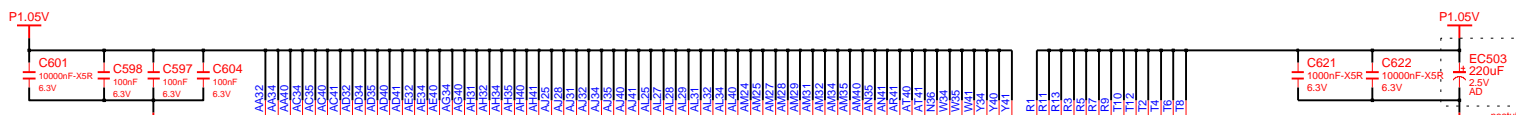


SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
✓ 1	EXT.DIODE2 (DIODE MODE)



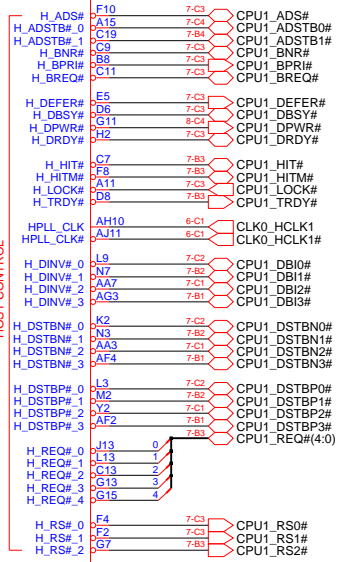
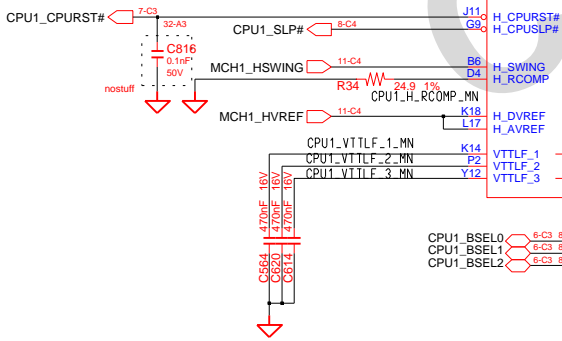
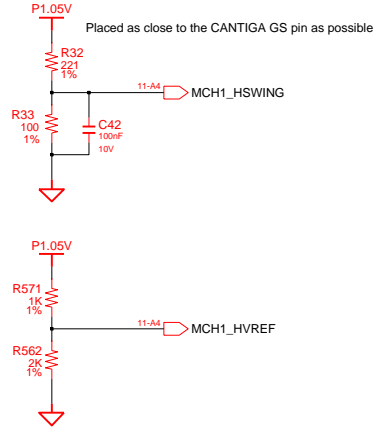
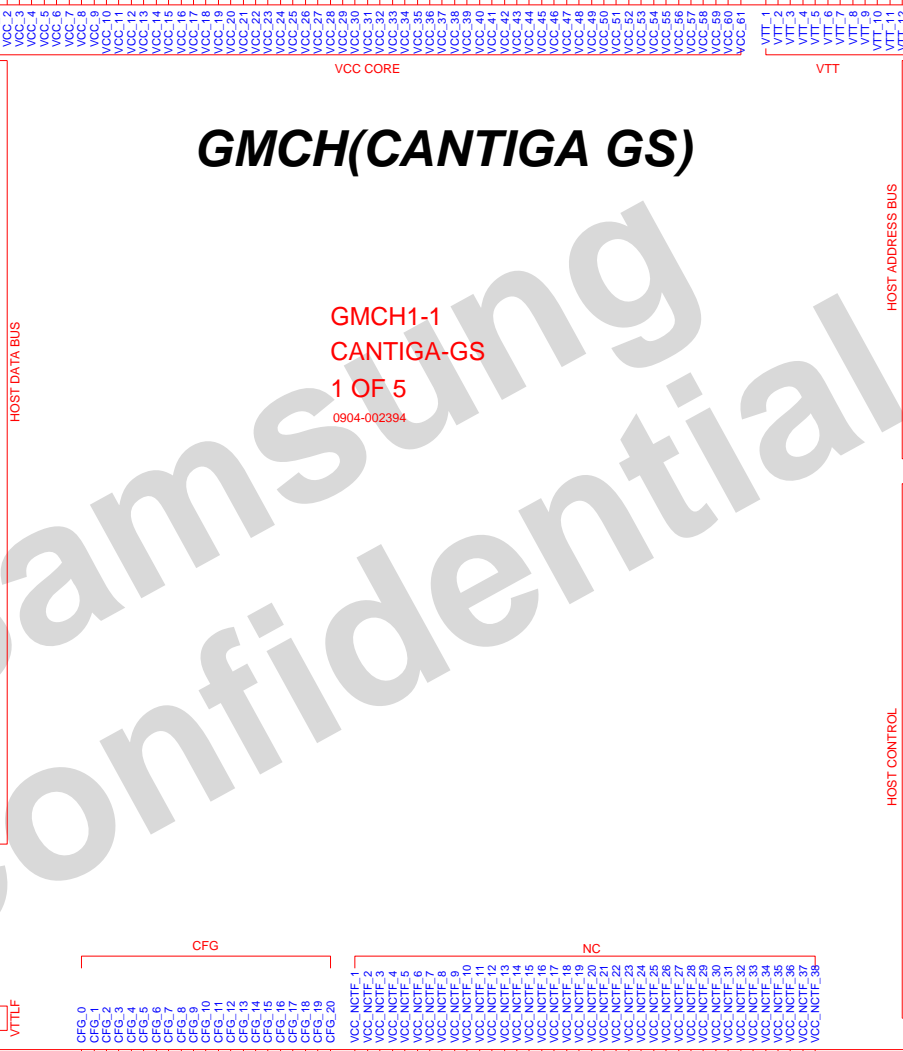
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GMCH(CANTIGA GS)

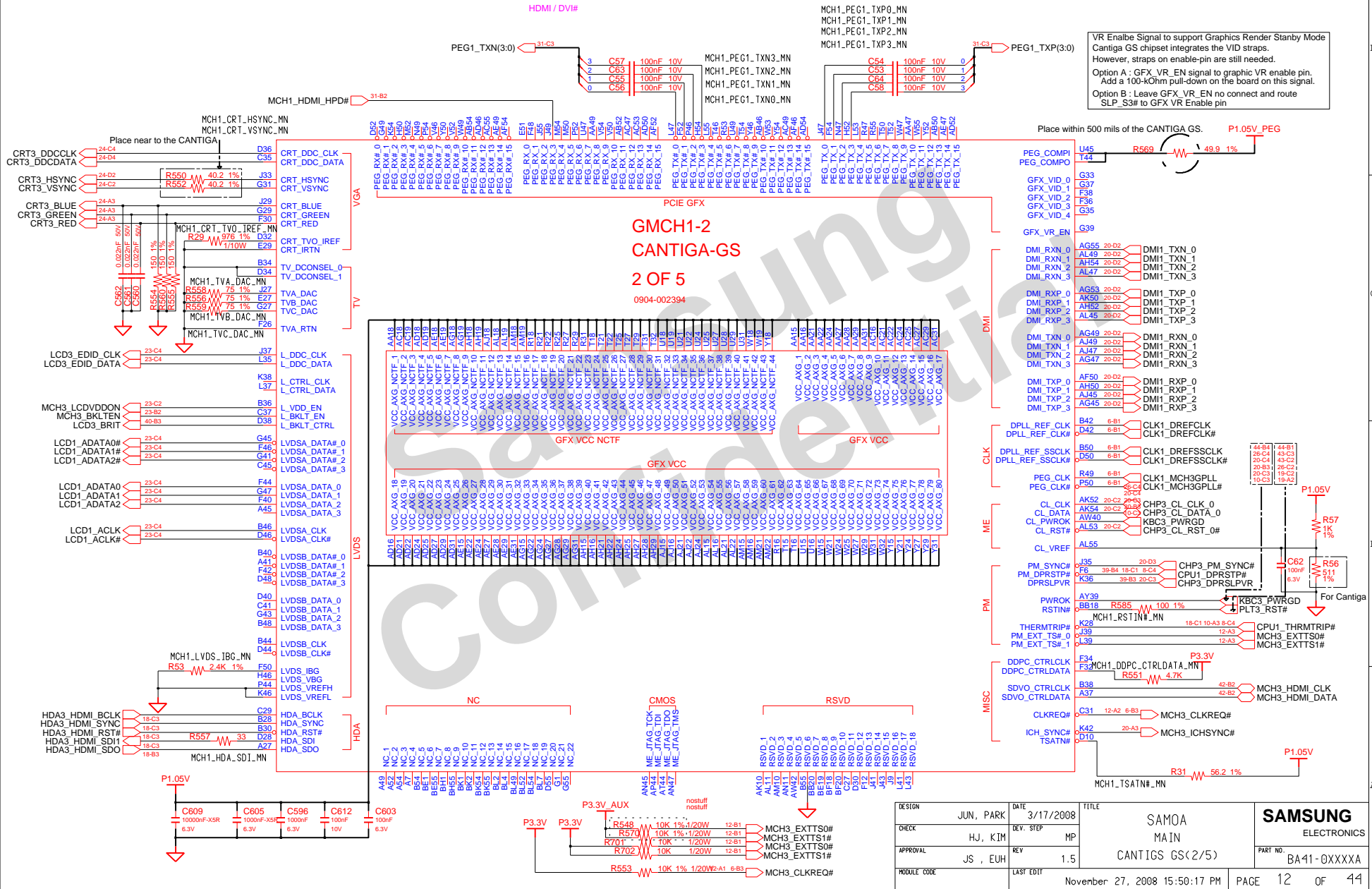
GMCH1-1
CANTIGA-GS
1 OF 5
0904-002394



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	REV	1.5	
APPROVAL	JS, EUH	LAST EDIT	November 27, 2008 15:50:17 PM	PAGE	11	OF 44
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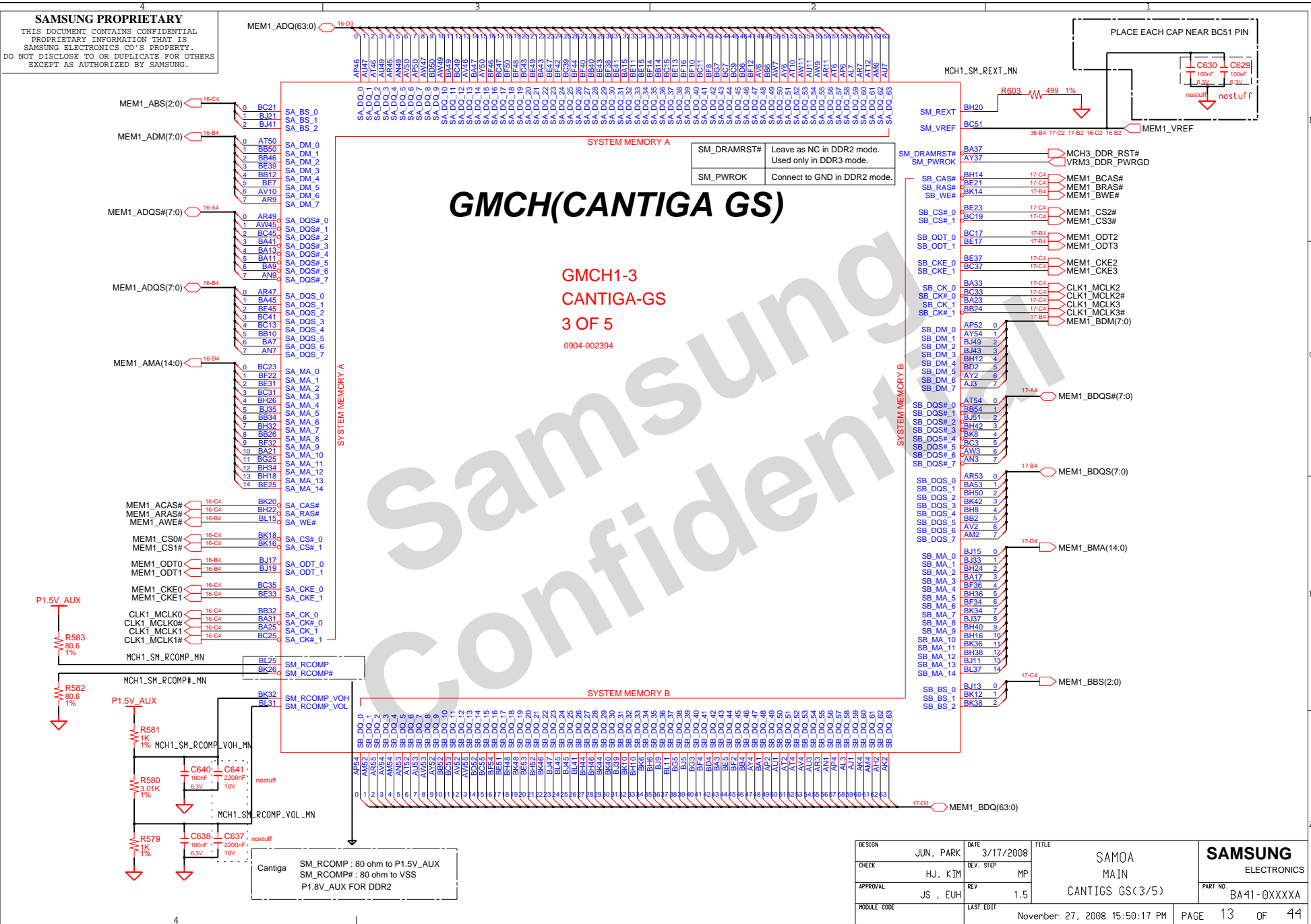
GMCH(CANTIGA GS)



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CANTIGS GS(2/5)		
APPROVAL	JS, EUH	REV	1.5	PART NO. BA41-0XXXXA		November 27, 2008 15:50:17 PM
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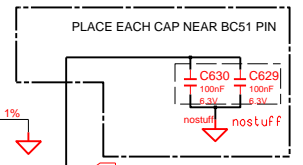
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GMCH(CANTIGA GS)

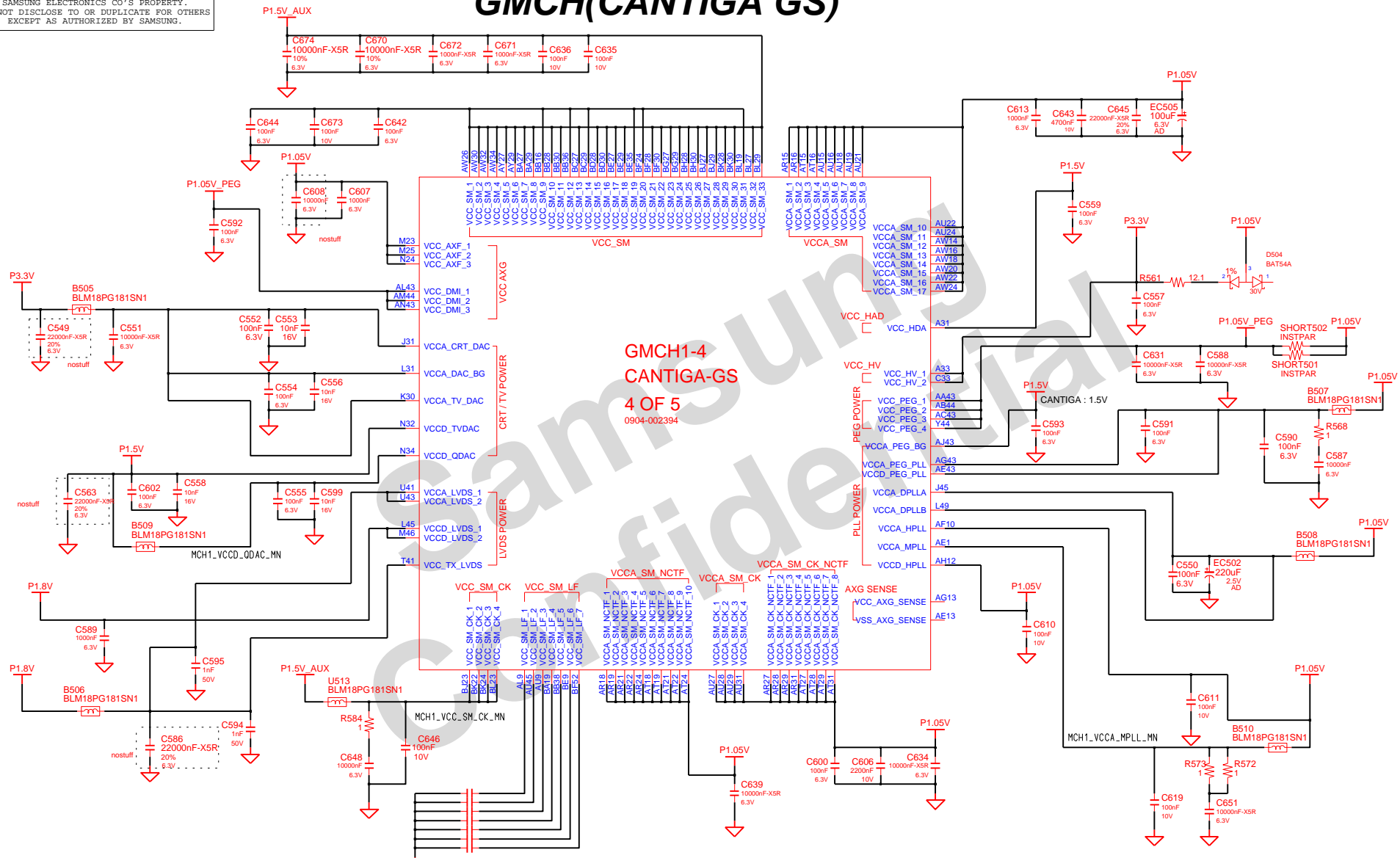
GMCH1-3
CANTIGA-GS
3 OF 5
0904-002394

SM_DRAMRST#	Leave as NC in DDR2 mode. Used only in DDR3 mode.
SM_PWROK	Connect to GND in DDR2 mode.



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	CANTIGS GS(3/5)		
APPROVAL	JS, EUH	REV	1.5	PART NO. BA41-0XXXXA		PAGE 13 OF 44
MODULE CODE	LAST EDIT		November 27, 2008 15:50:17 PM			

GMCH(CANTIGA GS)



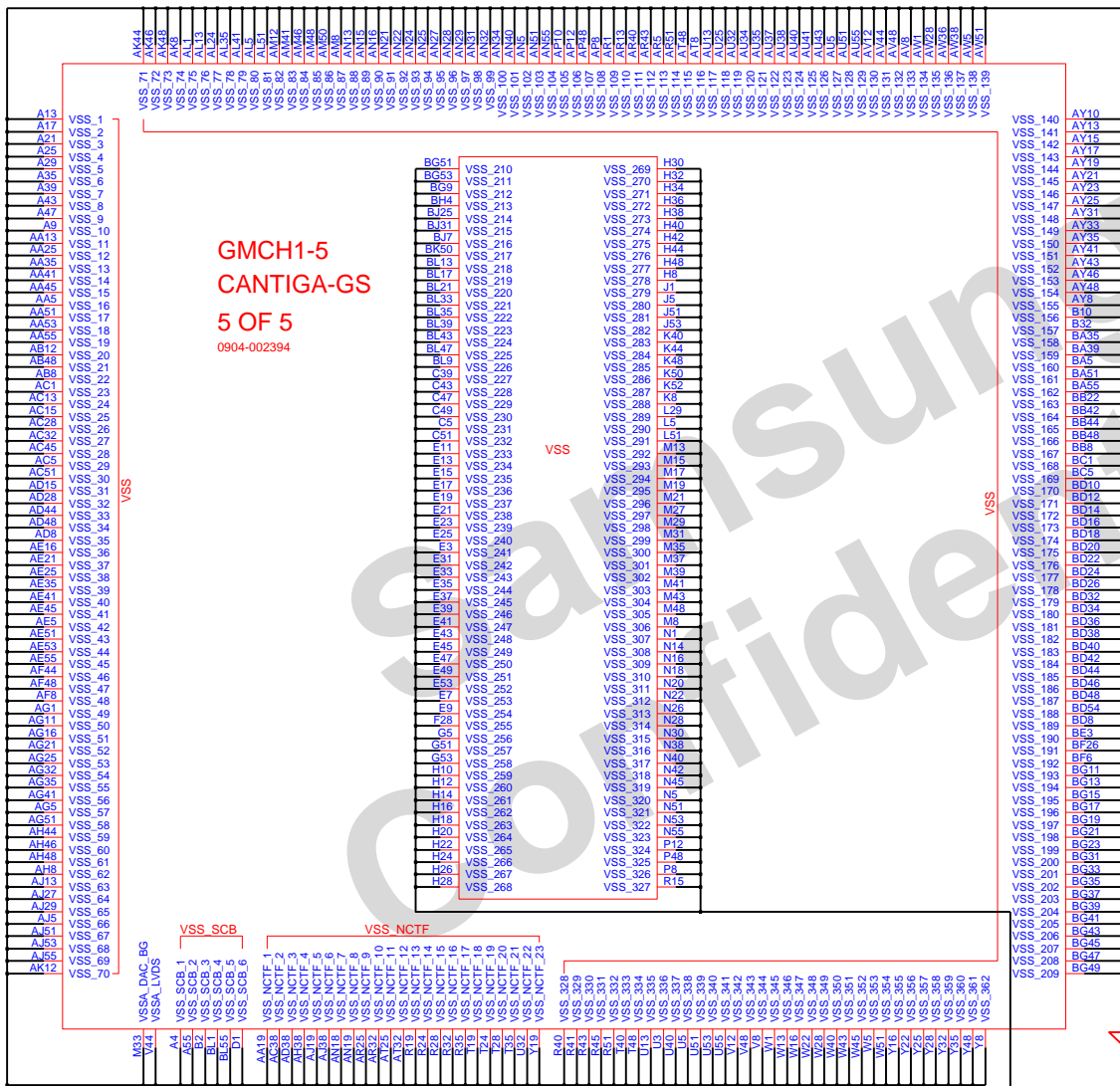
**GMCH1-4
CANTIGA-GS
4 OF 5
0904-002394**

C615	100nF	10V
C632	1000nF	6.3V
C649	100nF	10V
C647	220nF	10V
C633	470nF	16V
C650	220nF	10V
C87	1000nF	6.3V

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CANTIGA GS(4/5)	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
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GMCH(CANTIGA GS)

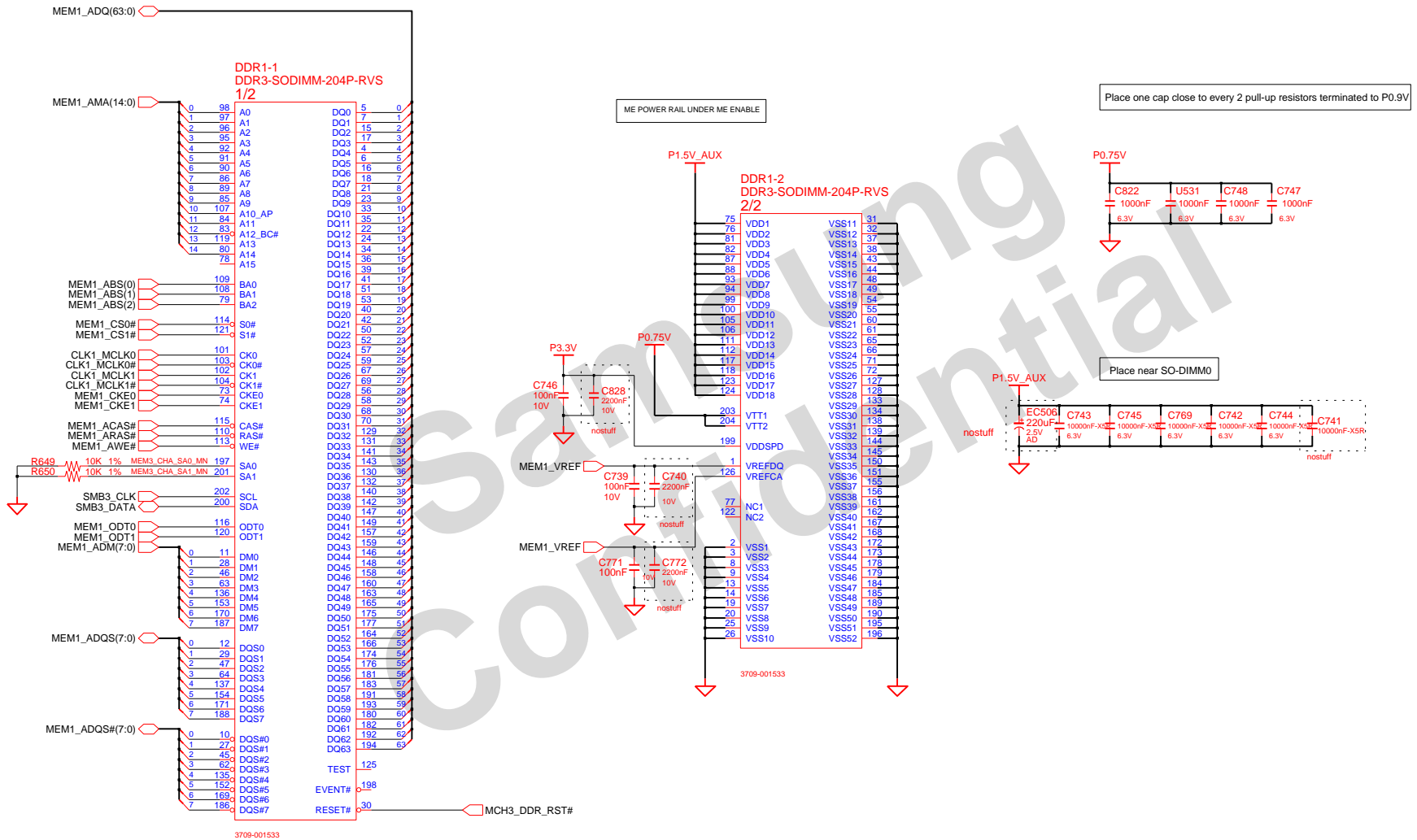


VSS 140	AY10
VSS 141	AY13
VSS 142	AY15
VSS 143	AY17
VSS 144	AY19
VSS 145	AY21
VSS 146	AY23
VSS 147	AY25
VSS 148	AY31
VSS 149	AY33
VSS 150	AY35
VSS 151	AY41
VSS 152	AY43
VSS 153	AY48
VSS 154	AY8
VSS 155	B10
VSS 156	B32
VSS 157	BA35
VSS 158	BA39
VSS 159	BA5
VSS 160	BA55
VSS 161	BA51
VSS 162	BB22
VSS 163	BB42
VSS 164	BB5
VSS 165	BB44
VSS 166	BB48
VSS 167	BC1
VSS 168	BC5
VSS 169	BD10
VSS 170	BD12
VSS 171	BD14
VSS 172	BD16
VSS 173	BD18
VSS 174	BD20
VSS 175	BD22
VSS 176	BD24
VSS 177	BD26
VSS 178	BD32
VSS 179	BD34
VSS 180	BD36
VSS 181	BD38
VSS 182	BD40
VSS 183	BD42
VSS 184	BD44
VSS 185	BD46
VSS 186	BD48
VSS 187	BD54
VSS 188	BD8
VSS 189	BE3
VSS 190	BF26
VSS 191	BF6
VSS 192	BG11
VSS 193	BG13
VSS 194	BG15
VSS 195	BG17
VSS 196	BG19
VSS 197	BG21
VSS 198	BG23
VSS 199	BG31
VSS 200	BG33
VSS 201	BG35
VSS 202	BG37
VSS 203	BG39
VSS 204	BG41
VSS 205	BG43
VSS 206	BG45
VSS 207	BG47
VSS 208	BG49
VSS 209	

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CANTIGS GS(5/5)	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS , EUH	REV	1.5		PART NO.	BA41-0XXXXA
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DDR SO-DIMM #0

Height : 5.2mm (Reverse)



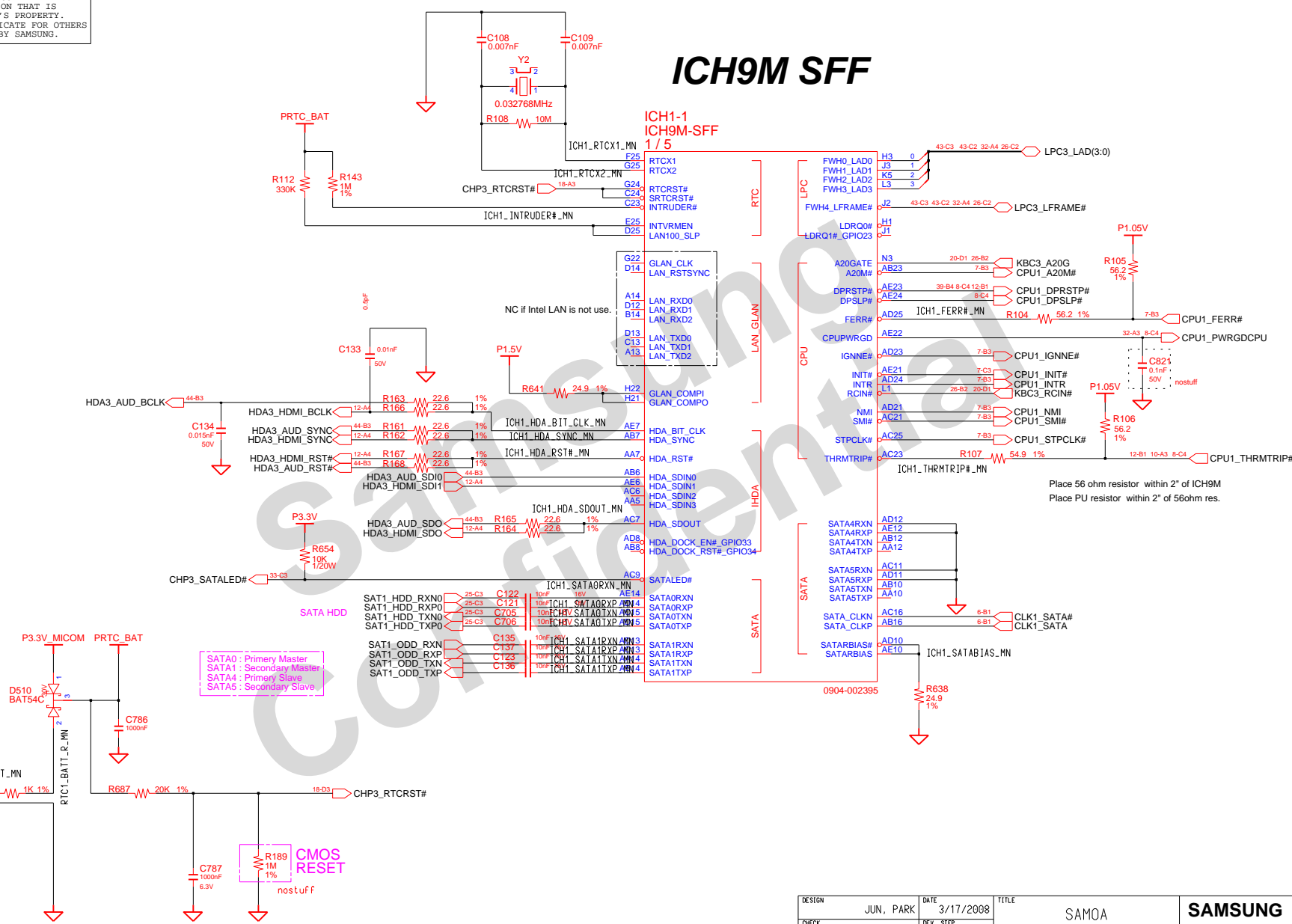
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APPROVAL	JS, EUH	REV	1.5		DDR3 SODIMM CH.0	PART NO. BA41-0XXXXA
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ICH9M SFF

ICH1-1
ICH9M-SFF
1/5

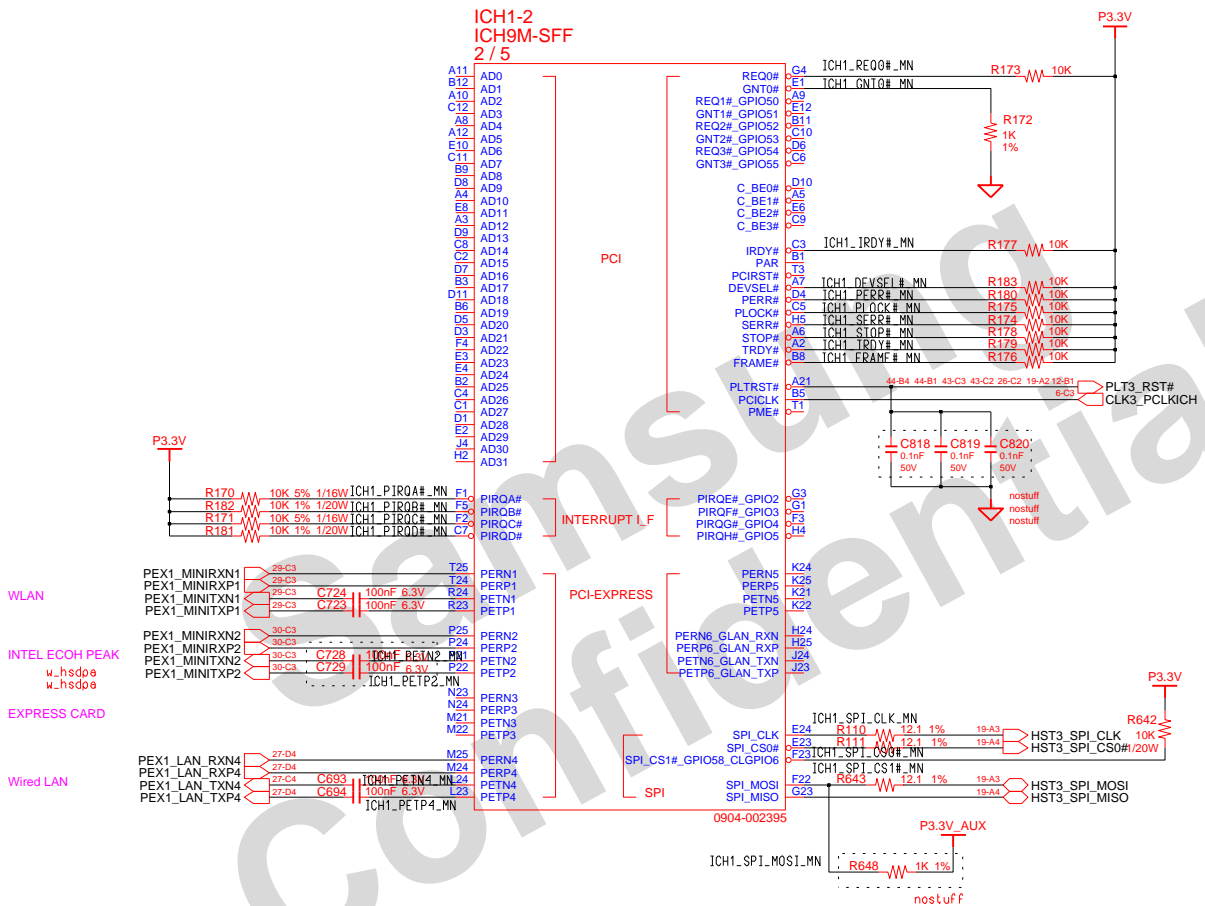


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ICH9M SFF

ICH1-2
ICH9M-SFF
2 / 5



WLAN
INTEL ECOH PEAK
EXPRESS CARD
Wired LAN

Boot BIOS Select

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
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APPROVAL	JS, EUH	REV	1.5	ICH9M SFF(2/5)		PAGE 19 OF 44
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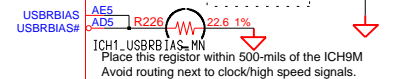
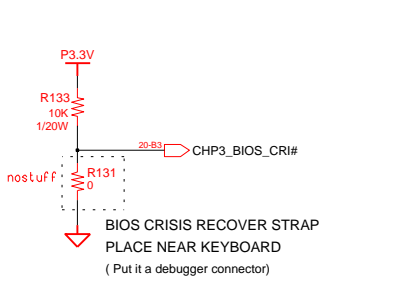
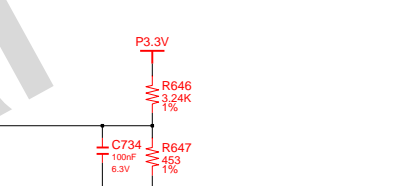
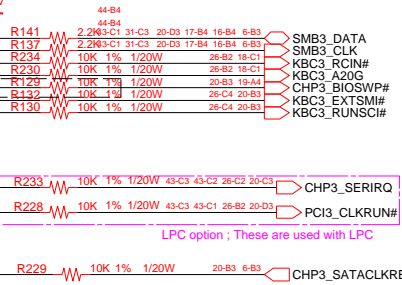
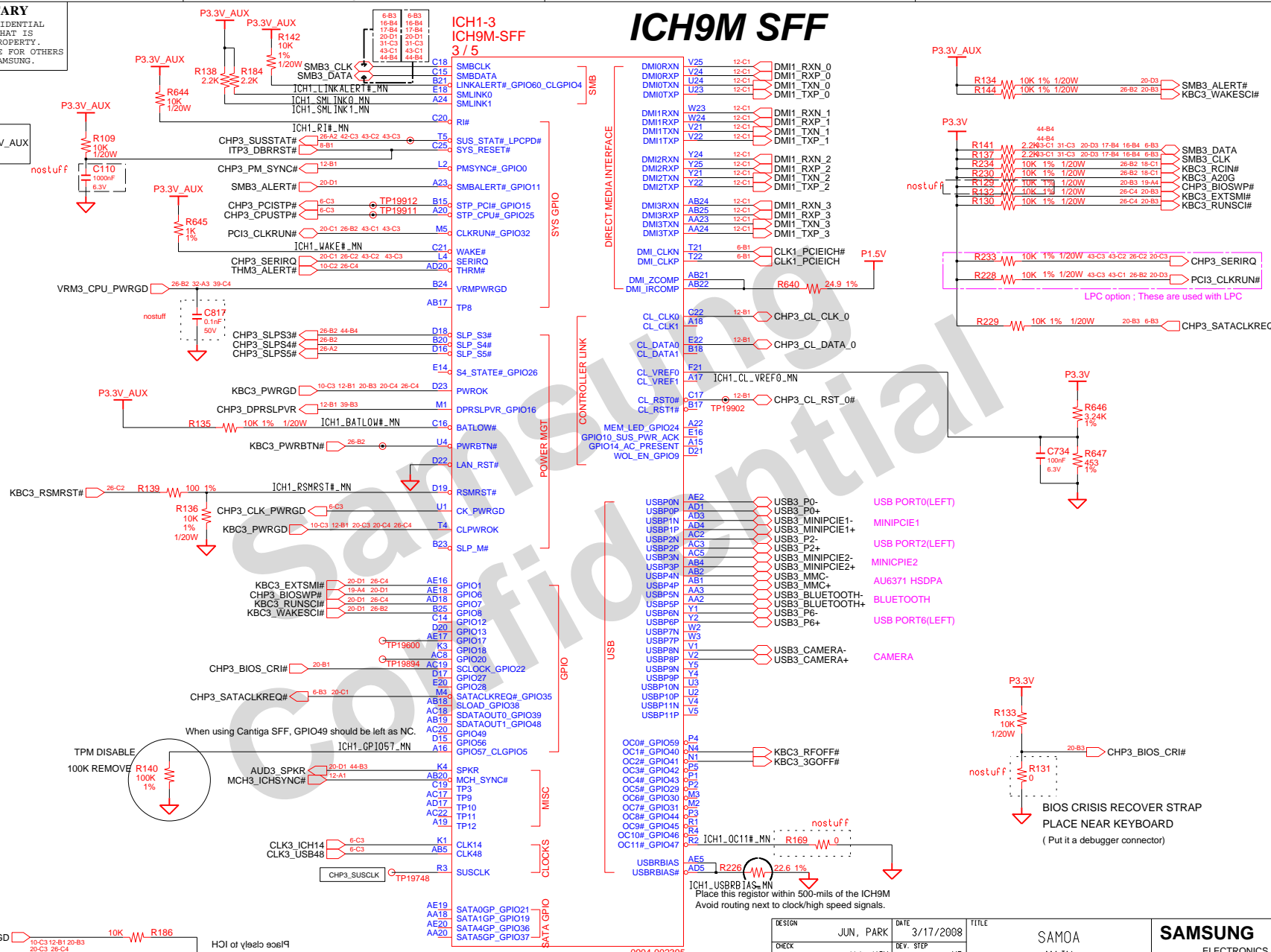
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SYS_RESET# is P3.3V tolerant and should be pulled up to P3.3V_AUX by the front panel header

ICH9M SFF

ICH1-3 ICH9M-SFF 3/5

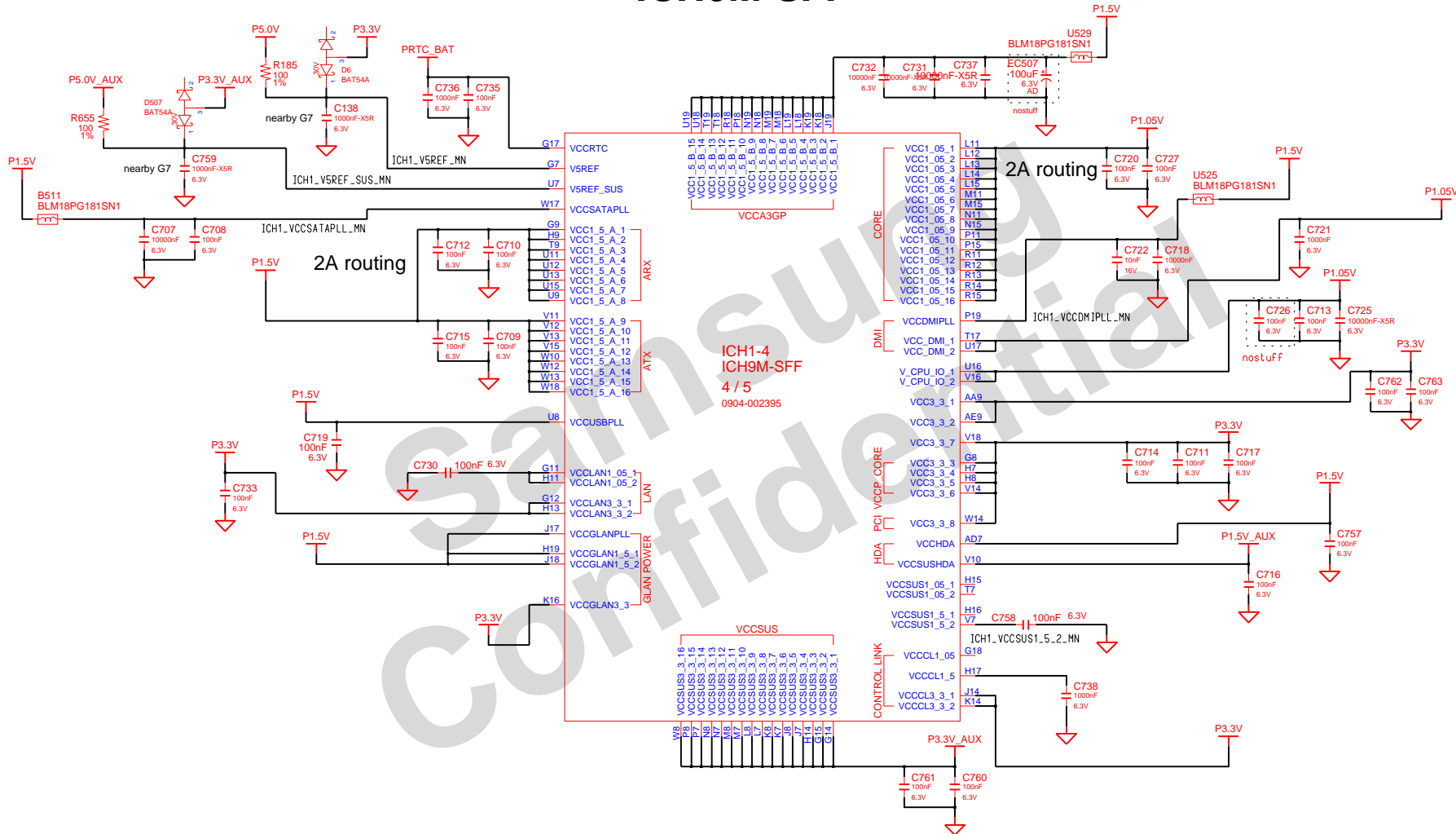


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PART NO. BA41-0XXXXA		
APPROVAL	JS, EUH	REV	1.5	ICH9M SFF(3/5)		PAGE 20 OF 44
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ICH9M SFF



ICH1-4 ICH9M-SFF 4/5 0904-002395

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5	ICH9M SFF(4/5)		PART NO. BA41-0XXXXA
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BIOS CODE

ICH9M SFF

02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT. BIOS DATA ROM
14	INIT. KEYBOARD CONTROLLER	8A	INIT.EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT. FDD CONTROLLER
18	8254 TIMER INIT.	9A	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT.	9C	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT. TYPOMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TESET CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	B2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG. WITH CMOS VALUE	B7	ACPI INIT
42	INIT. INTERRUPT VECTOR	BA	DMI INIT
44	INIT. BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT. I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	89	ENABLE NMI
56	ENABLE KEYBOARD	90	INIT. HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	91	INIT. LOCAL BUS HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	92	JUMP TO USER PATCH 2
5C	TEST RAM BETWEEN 512K AND 640K	94	DISABLE A20 ADDRESS LINE
60	TEST EXTENDED MEMORY	96	CLEAR HUGE ES SEGMENT REG.
62	TEST EXTENDED MEMORY ADDRESS LINE	98	SEARCH FOR OPTION ROMS
64	JUMP TO USER PATCH 1		

N14	AA1	VSS_1	VSS_133	R9
N19	AA11	VSS_2	VSS_134	T10
N17	AA13	VSS_3	VSS_134	T11
N21	AA15	VSS_4	VSS_135	T12
N21	AA16	VSS_5	VSS_136	T13
N22	AA17	VSS_6	VSS_137	T14
N22	AA19	VSS_7	VSS_138	T15
N22	AA21	VSS_8	VSS_139	T16
N22	AA22	VSS_9	VSS_140	T2
N22	AA25	VSS_10	VSS_141	T23
N22	AA4	VSS_11	VSS_142	T23
N22	AAE	VSS_12	VSS_143	U10
N22	AA8	VSS_13	VSS_144	U14
N22	AB11	VSS_14	VSS_145	U21
N22	AB13	VSS_15	VSS_146	U22
N22	AB5	VSS_16	VSS_147	U25
N22	AB9	VSS_17	VSS_148	U5
N22	AC1	VSS_18	VSS_149	V17
N22	AC10	VSS_19	VSS_150	V19
N22	AC12	VSS_20	VSS_151	V23
N22	AC14	VSS_21	VSS_152	V3
N22	AC24	VSS_22	VSS_153	V8
N22	AC4	VSS_23	VSS_154	V9
N22	AD16	VSS_24	VSS_155	V11
N22	AD19	VSS_25	VSS_156	W1
N22	AD2	VSS_26	VSS_157	W11
N22	AD22	VSS_27	VSS_158	W16
N22	AD5	VSS_28	VSS_159	W19
N22	AD9	VSS_29	VSS_160	W22
N22	AE11	VSS_30	VSS_161	W21
N22	AE13	VSS_31	VSS_162	W25
N22	AE15	VSS_32	VSS_163	W4
N22	AE3	VSS_33	VSS_164	W5
N22	AE4	VSS_34	VSS_166	W7
N22	AE8	VSS_35	VSS_167	Y23
N22	B10	VSS_36	VSS_168	Y3
N22	B13	VSS_37	VSS_169	
N22	B16	VSS_38		
N22	B19	VSS_39		
N22	B22	VSS_40		
N22	B4	VSS_41		
N22	B7	VSS_43		
N22	D2	VSS_44		
N22	E11	VSS_45		
N22	E13	VSS_46		
N22	E15	VSS_47		
N22	E17	VSS_48		
N22	E19	VSS_49		
N22	E21	VSS_50		
N22	E5	VSS_51		
N22	E7	VSS_52		
N22	E9	VSS_53		
N22	E24	VSS_54		
N22	G10	VSS_55		
N22	G13	VSS_56		
N22	G16	VSS_57		
N22	G19	VSS_58		
N22	G2	VSS_59		
N22	G21	VSS_60		
N22	G5	VSS_61		
N22	H10	VSS_62		
N22	H12	VSS_63		
N22	H18	VSS_64		
N22	H23	VSS_65		
N22	J10	VSS_66		
N22	J11	VSS_67		
N22	J12	VSS_68		
N22	J13	VSS_69		
N22	J15	VSS_70		
N22	J16	VSS_71		
N22	J21	VSS_72		
N22	J22	VSS_73		
N22	J25	VSS_74		
N22	J5	VSS_75		
N22	J8	VSS_76		
N22	J9	VSS_77		
N22	K10	VSS_78		
K11	VSS_79			
K12	VSS_80			
K13	VSS_81			
K17	VSS_82			
K2	VSS_84			
K3	VSS_85			
K9	VSS_86			
L10	VSS_89			
L16	VSS_90			
L17	VSS_91			
L22	VSS_92			
L23	VSS_93			
L5	VSS_94			
M10	VSS_95			
M12	VSS_97			
M13	VSS_98			
M14	VSS_99			
M17	VSS_100			
M21	VSS_102			
M9	VSS_103			
M10	VSS_104			
M13	VSS_105			
N13	VSS_106			
N14	VSS_107			
N19	VSS_108			
N17	VSS_109			
N21	VSS_110			
N21	VSS_111			
N22	VSS_112			
N22	VSS_113			
N22	VSS_114			
N22	VSS_115			
N22	VSS_116			
N22	VSS_117			
N22	VSS_118			
N22	VSS_119			
N22	VSS_120			
N22	VSS_121			
N22	VSS_122			
N22	VSS_123			
N22	VSS_124			
N22	VSS_125			
N22	VSS_126			
N22	VSS_127			
N22	VSS_128			
N22	VSS_129			
N22	VSS_130			
N22	VSS_131			
N22	VSS_132			

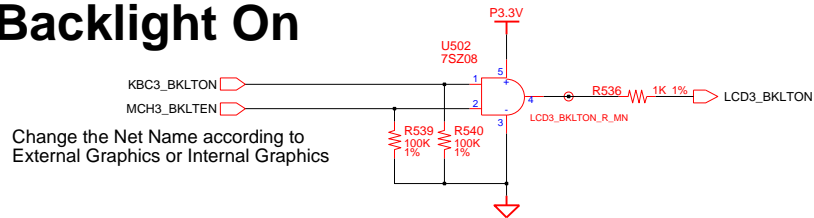
ICH1-5
ICH9M-SFF
5 / 5
GND
904-002395

VSS_NCTF_1 A1
VSS_NCTF_2 A25
VSS_NCTF_3 AE1
VSS_NCTF_4 AE25

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP		MAIN	
APPROVAL	JS, EUH	REV	1.5		ICH9M SFF(5/5)	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM			PAGE 22 OF 44

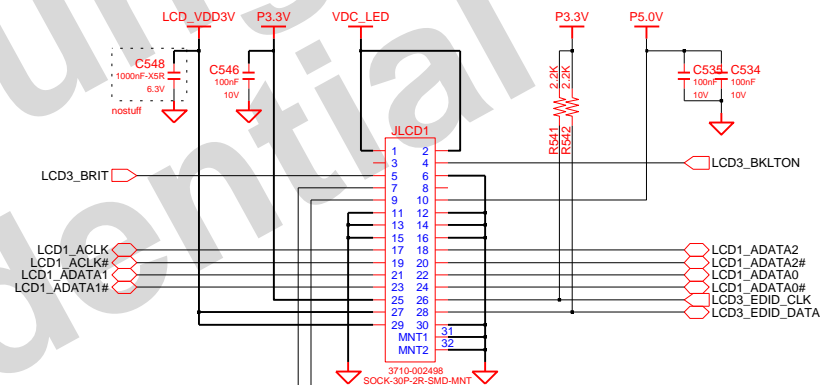
LVDS

Backlight On

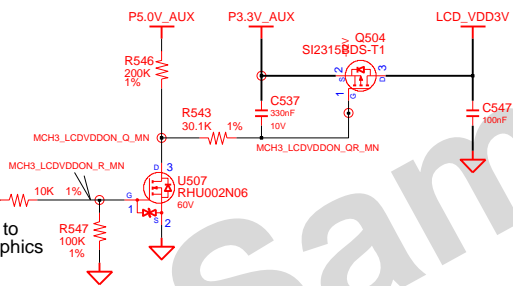


Change the Net Name according to External Graphics or Internal Graphics

1Ch. LCD Connector + CAMERA



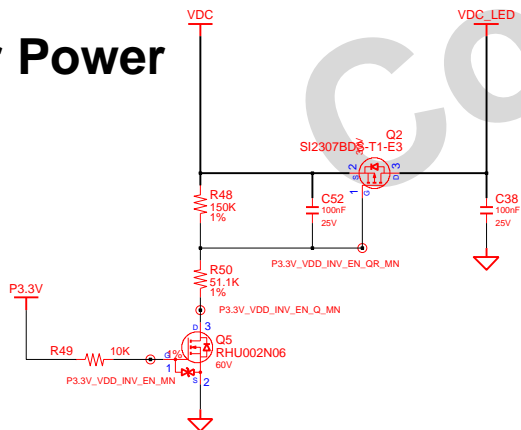
EBL Purpose



LCD Power

Change the Net Name according to External Graphics or Internal Graphics

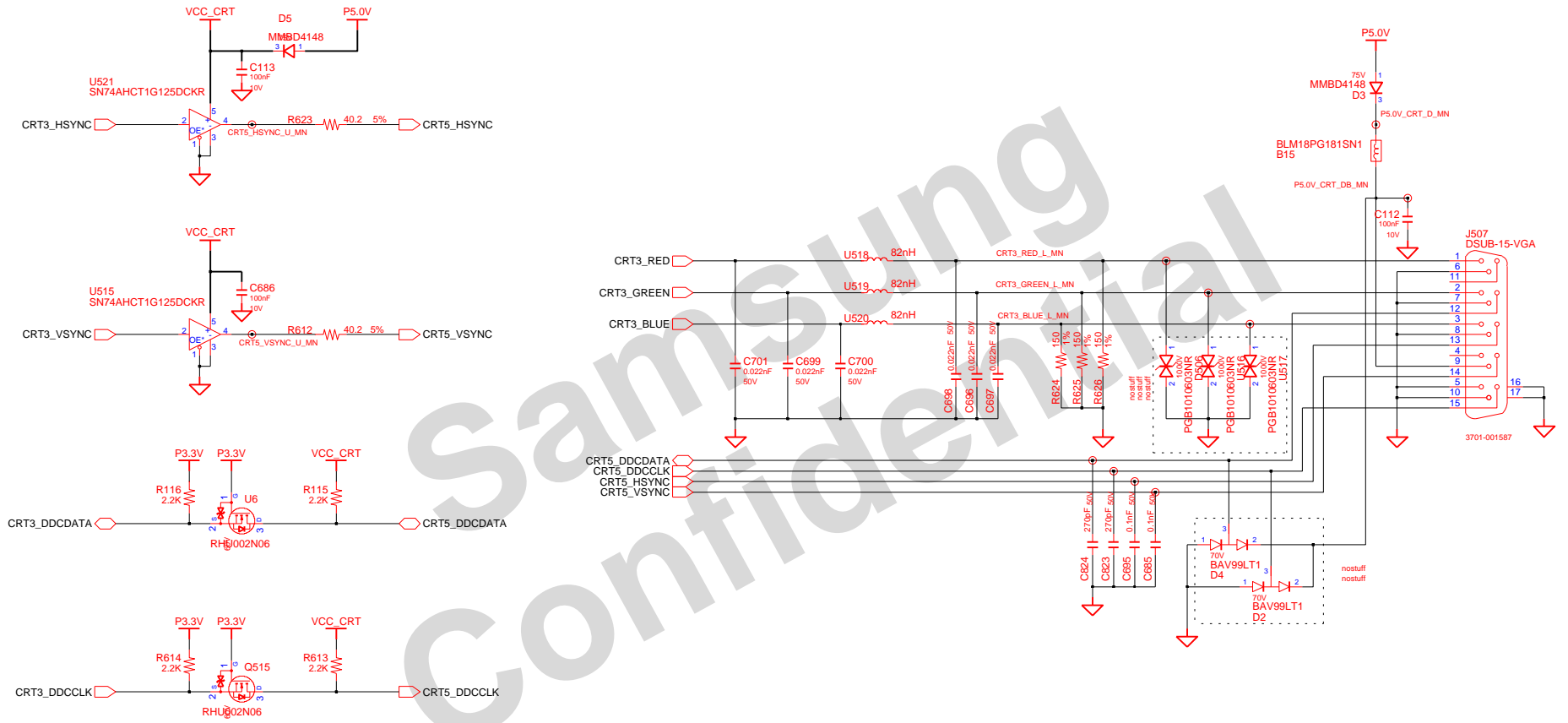
Inverter Power



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LED LCD I/F	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 23 OF 44		

CRT

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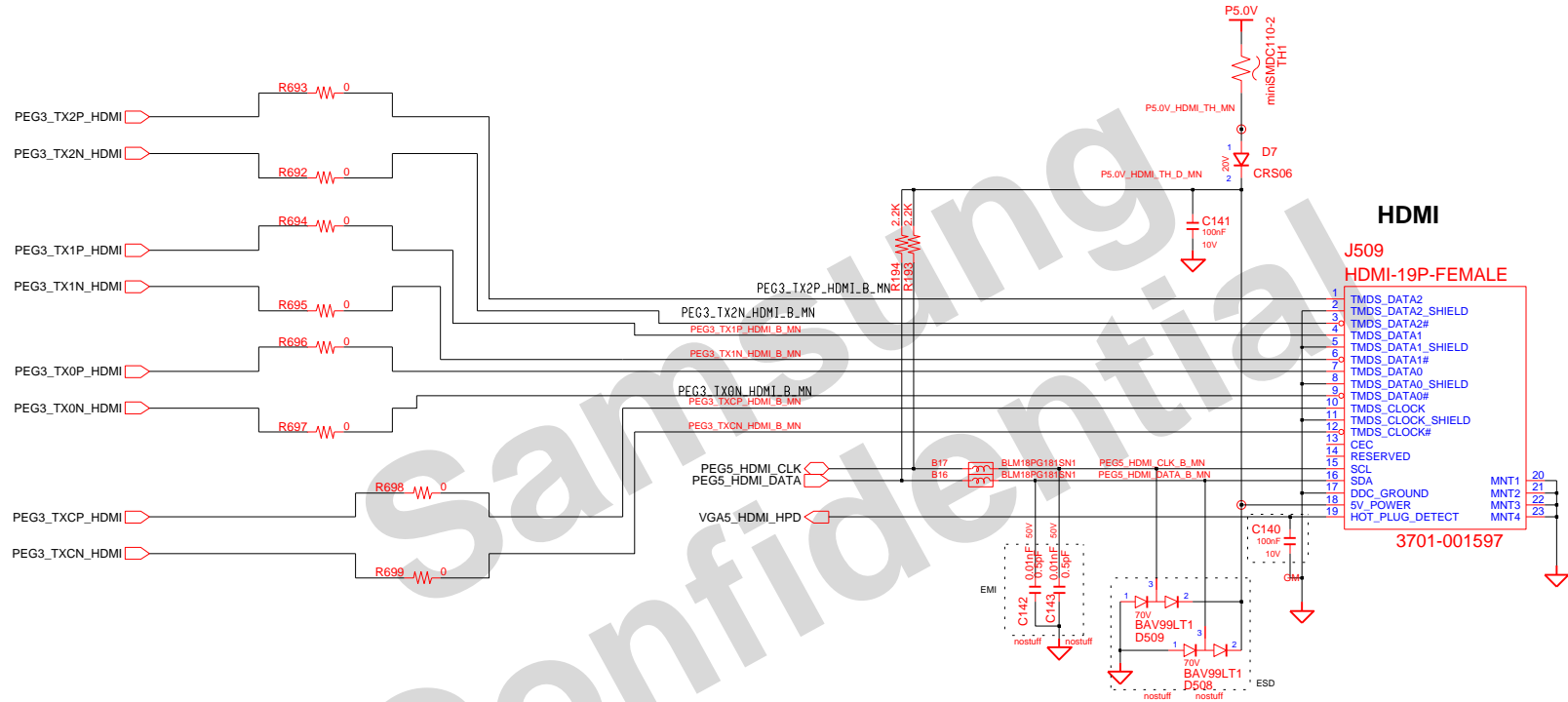
Check "CRT3_DDCCLK/DATA" Voltage Level
 2N06 Can be replaced with SM6K2

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CRT DOCK I/F	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 24 OF 44		

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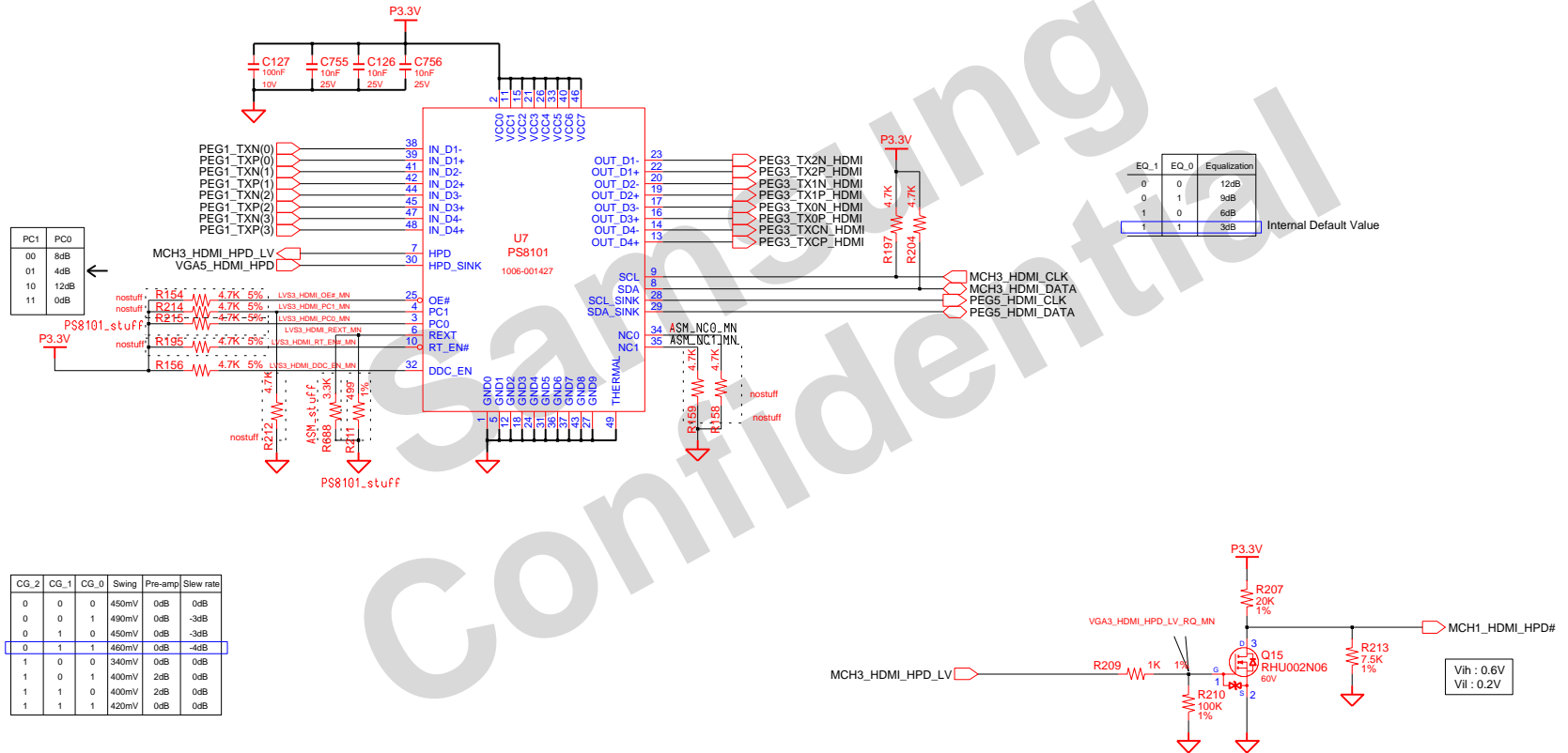
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HDMI



DESIGN	PARK, JUN	DATE	3/16/2009	TITLE	VERONA MAIN HDMI I/F	
CHECK	HJ, KIM	DEV. STEP	ADV			
APPROVAL	JS, EUH	REV	1.6			
MODULE CODE		LAST EDIT				
				March, 16, 2009 4:37:31 PM	PAGE 25	of 100

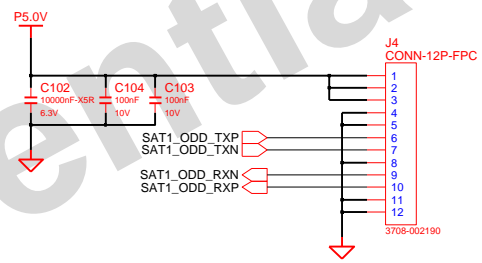
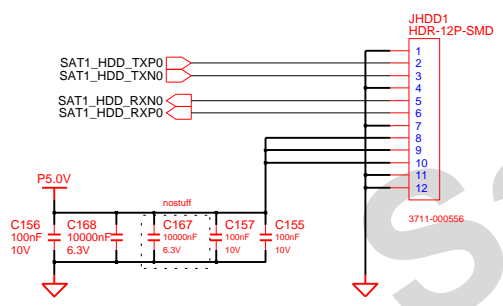
HDMI Level Shifter for Int. Graphic only



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SATA HDD I/F

SATA ODD I/F

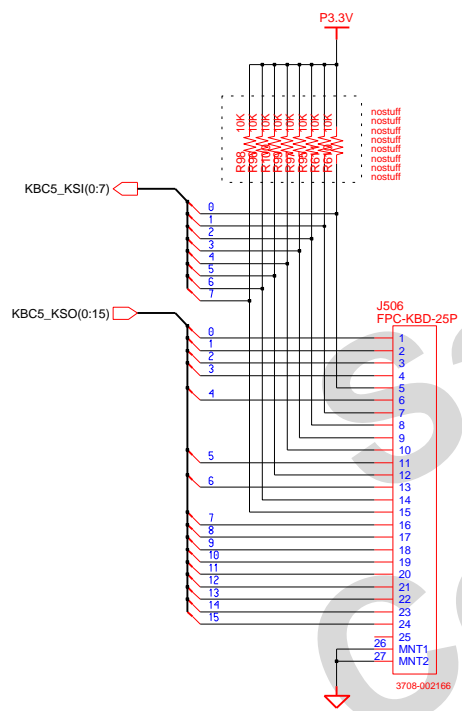


Samsung Confidential

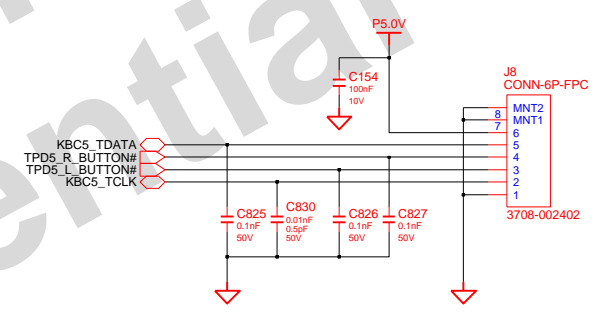
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN 1.8inch SATA HDD I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE	25	OF 44

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KEYBOARD

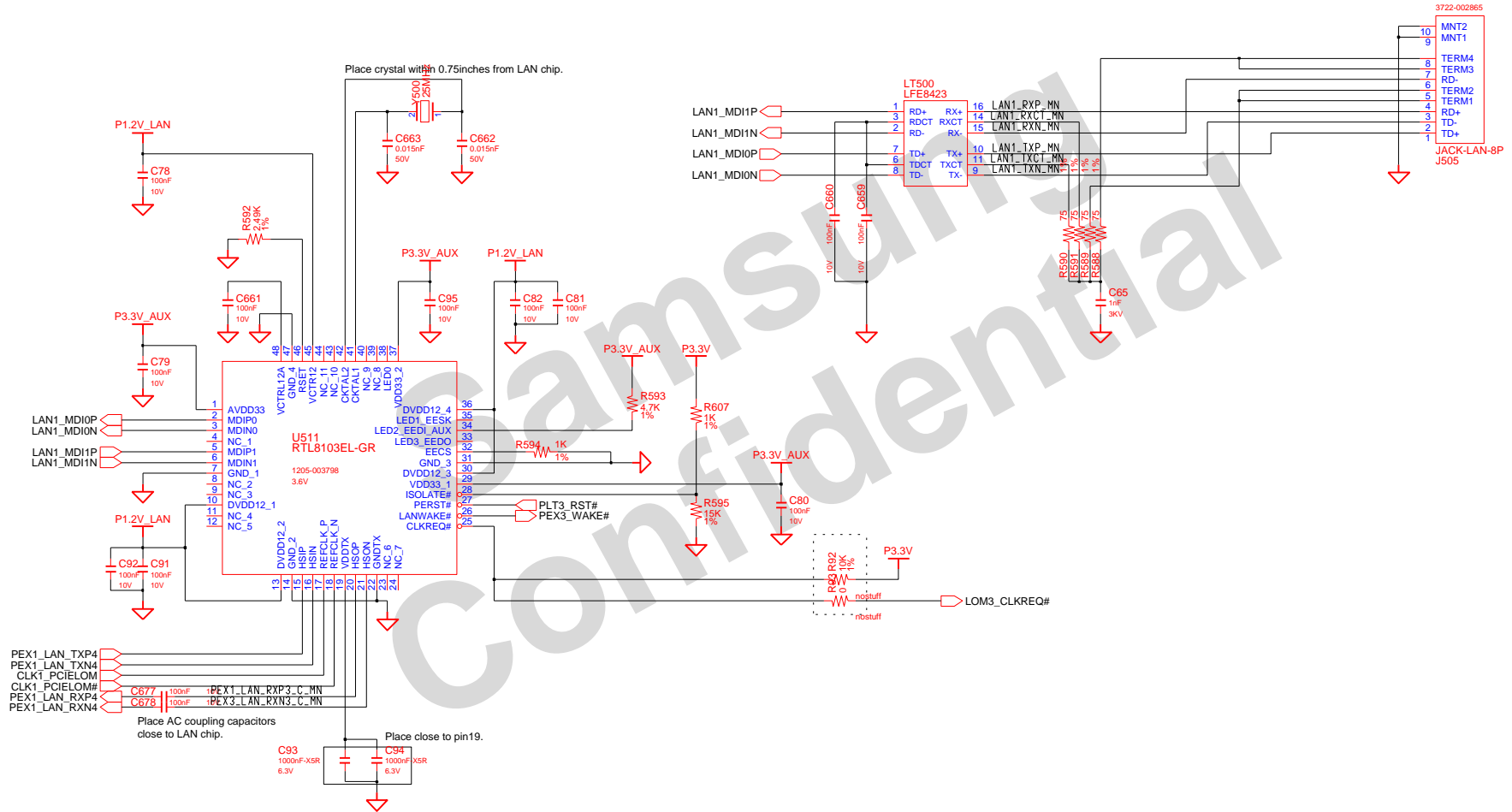


TOUCHPAD



DESIGN	PARK, JUN	DATE	3/16/2009	TITLE	VERONA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	ADV			
APPROVAL	JS, EUH	REV	1.6		MICOM GLUE LOGIC	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT		March, 16, 2009 5:22:09 PM	PAGE 2	of 1 defined

LAN CONTROLLER

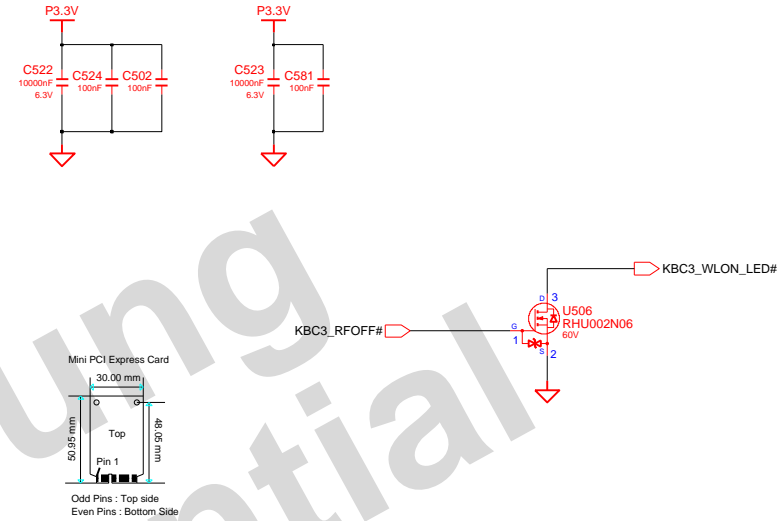
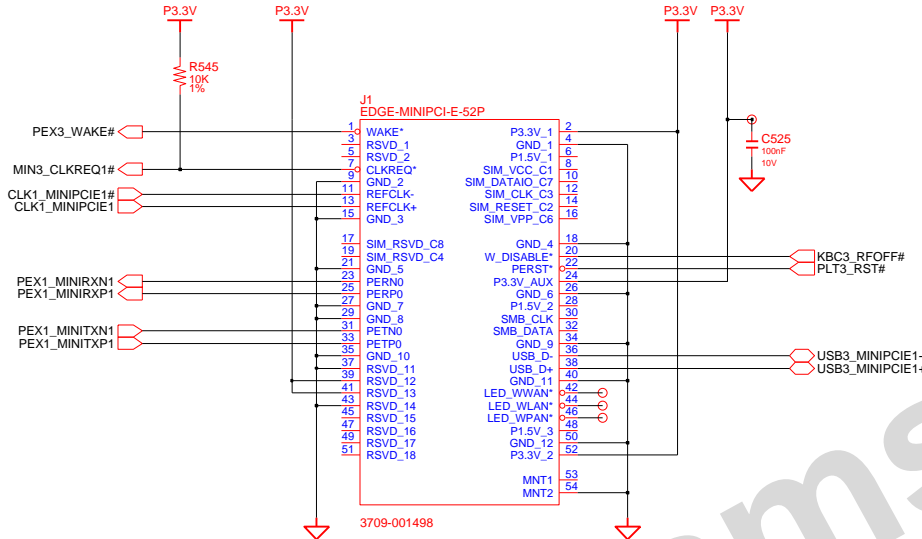


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN LAN CONTROLLER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5		PART NO.	BA41-0XXXXA
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE	27	OF 44

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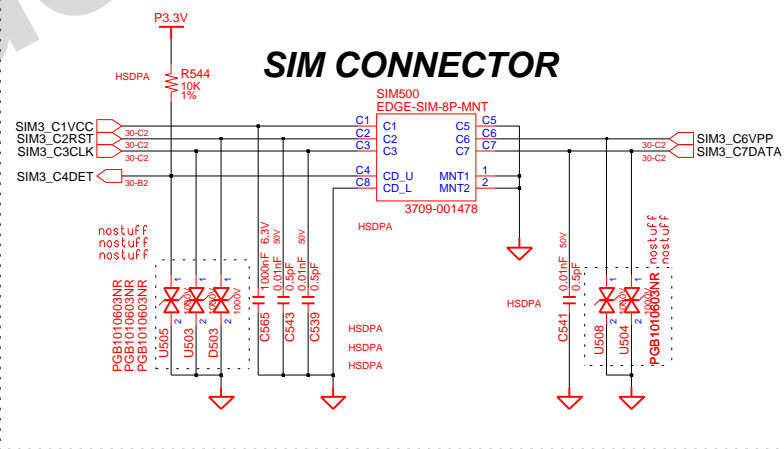
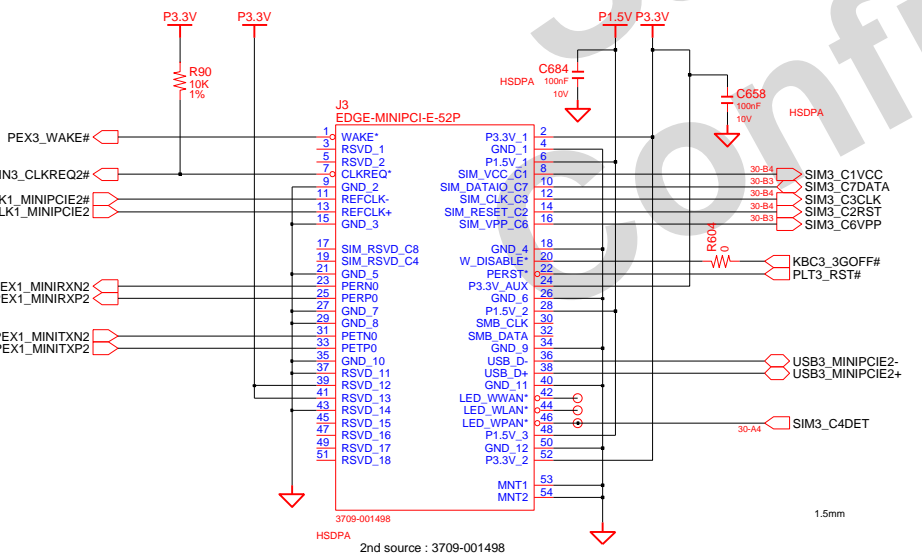
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WLAN, 7mm



HSDPA, 4mm

To fix Shirley Peak EMI issue
Place it at the old rubber area

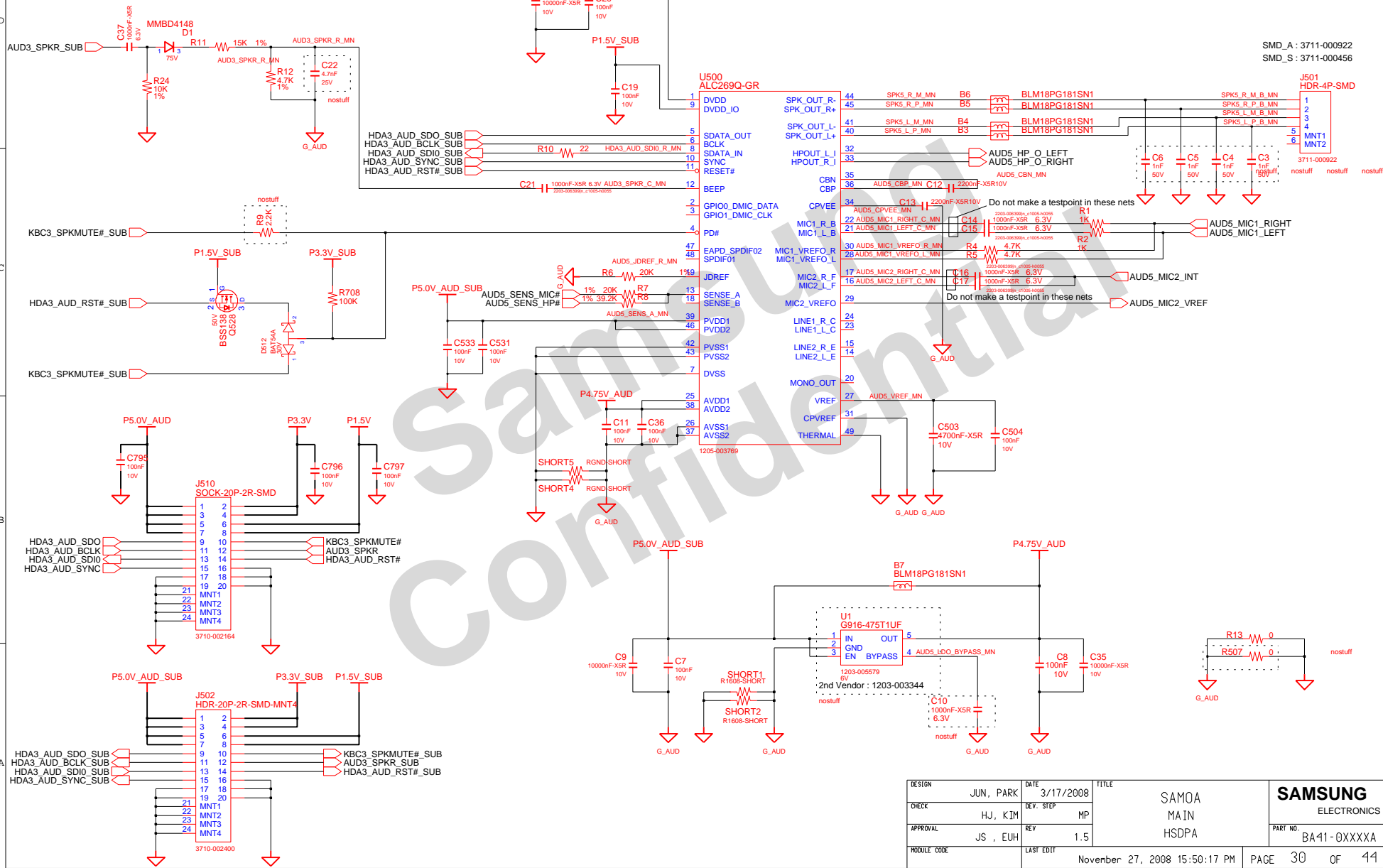


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN WIRELESS LAN	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM			
PAGE 29 OF 44						

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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



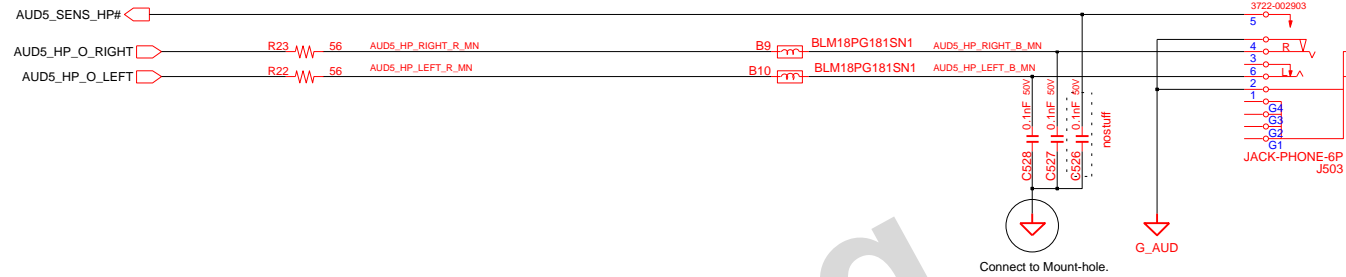
SMD_A : 3711-000922
SMD_S : 3711-000456

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN HSDPA	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT				
				November 27, 2008 15:50:17 PM	PAGE	30 OF 44

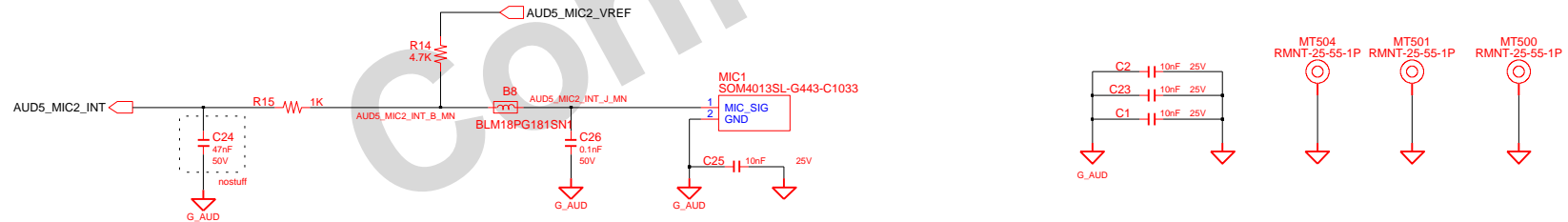
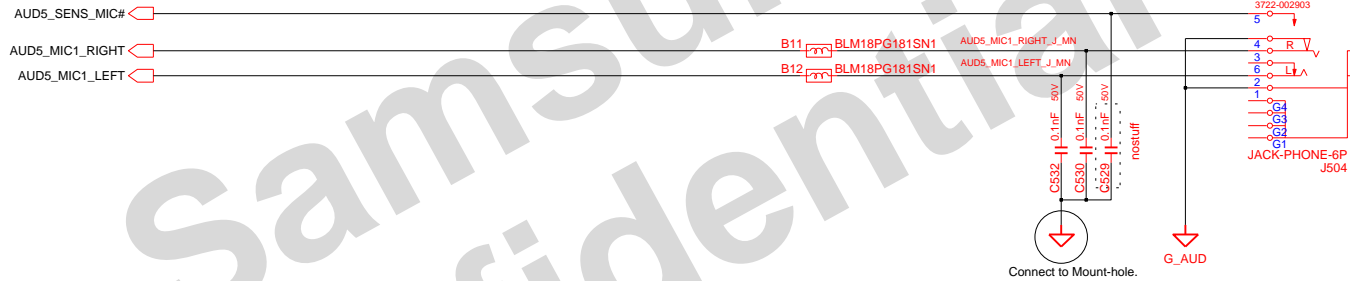
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HEADPHONE



MIC JACK



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN HDMI & DVI I/F	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PART NO.		
APPROVAL	JS, EUH	REV	1.5	November 27, 2008 15:50:17 PM		PAGE 31 OF 44
MODULE CODE	LAST EDIT					

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MAIN TO LED SUB

DEBUG PORT



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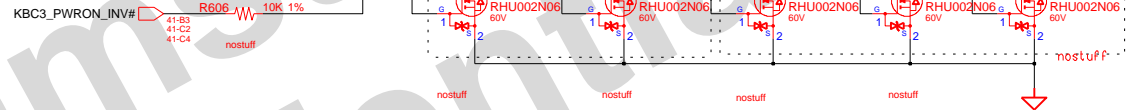
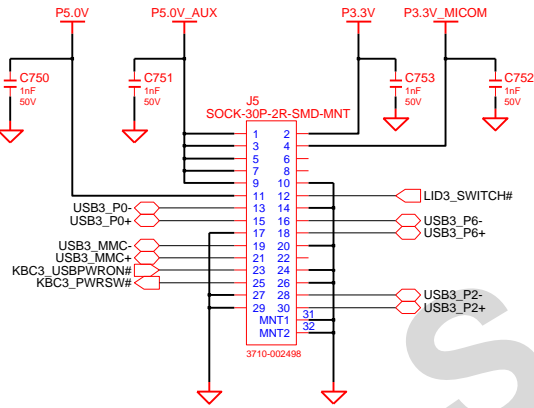
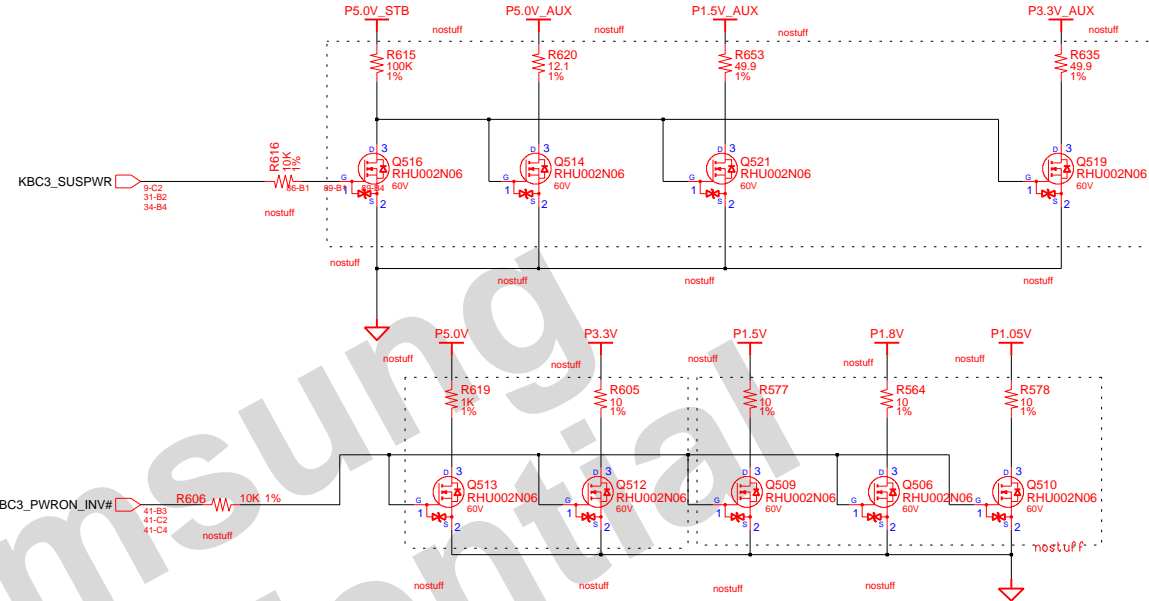
DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5	KBD/LED/DEBUG/SUB CONN.		
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM		PAGE	32 OF 44

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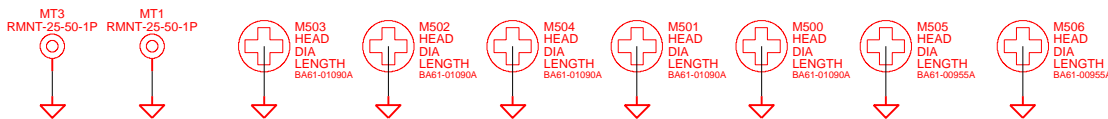
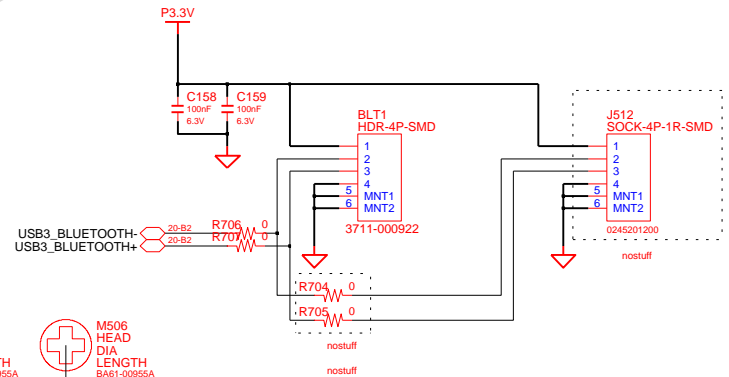
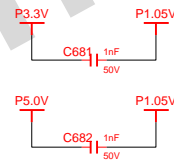
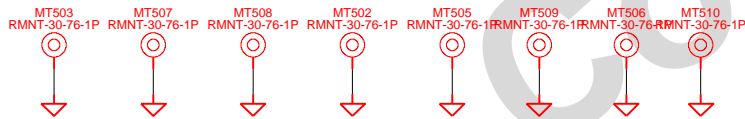
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DISCHARGE

MAIN TO SUB USB



BLUETOOTH

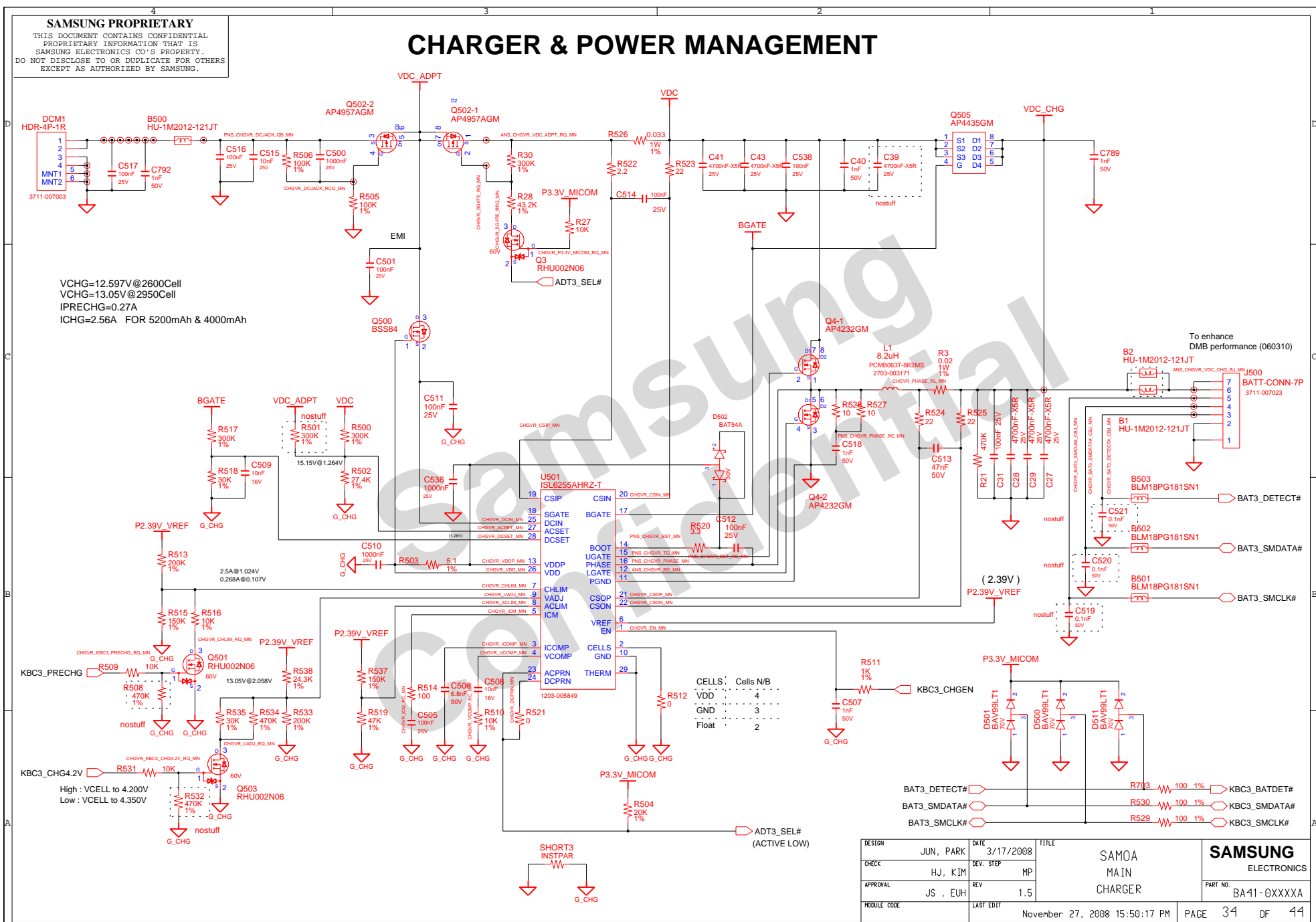


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5	CAMERA, BLUETOOTH & LED		PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT		November 27, 2008 15:50:17 PM		PAGE 33 OF 44

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CHARGER & POWER MANAGEMENT



VCHG=12.597V@2600Cell
 VCHG=13.05V@2950Cell
 IPRECHG=0.27A
 ICHG=2.56A FOR 5200mAh & 4000mAh

To enhance DMB performance (060310)

U501 ISL6255AHRZ-T

19	CSIP	CSIN
18	SGATE	BGATE
17	DCIN	ACSET
27	DCSET	DCSET
28	BOOT	UGATE
14	VDDP	VDD
15	PHS_CHEVR_TIE_MN	PHS_CHEVR_DET_REL_MN
16	ANS_CHEVR_PHS_MN	ANS_CHEVR_PHS_MN
12	ANS_CHEVR_RQ_MN	ANS_CHEVR_RQ_MN
11	PGND	PGND
21	CHLIM	CSOP
9	VADJ	CSON
8	ACLIM	VREF
5	ICM	EN
3	ICOMP	CELLS
4	VCOMP	GND
23	ACPRN	29
24	DCPRN	THERM
0		

CELLS: Cells N/B

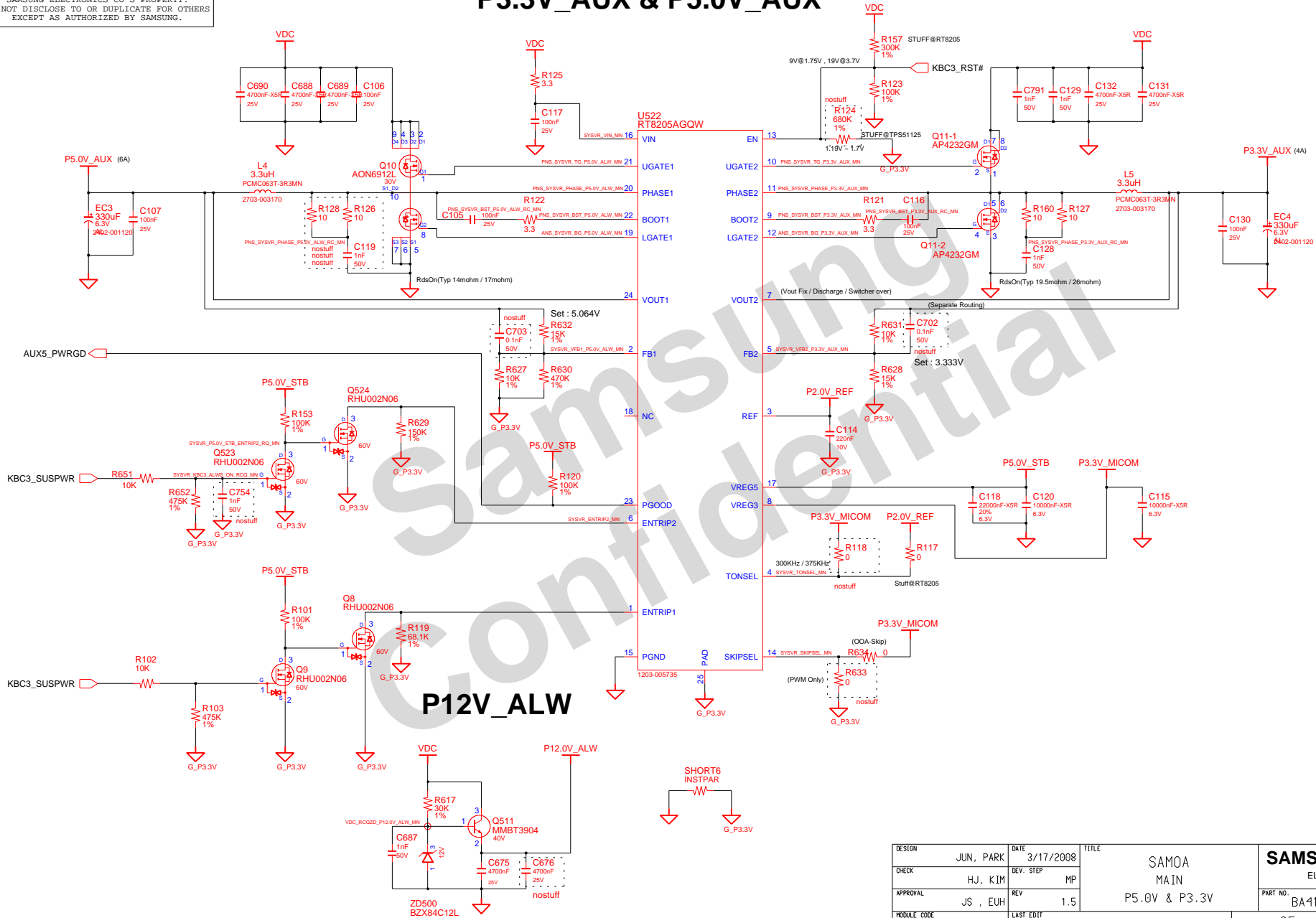
VDD	4
GND	3
Float	2

DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 34 OF 44		

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P3.3V_AUX & P5.0V_AUX

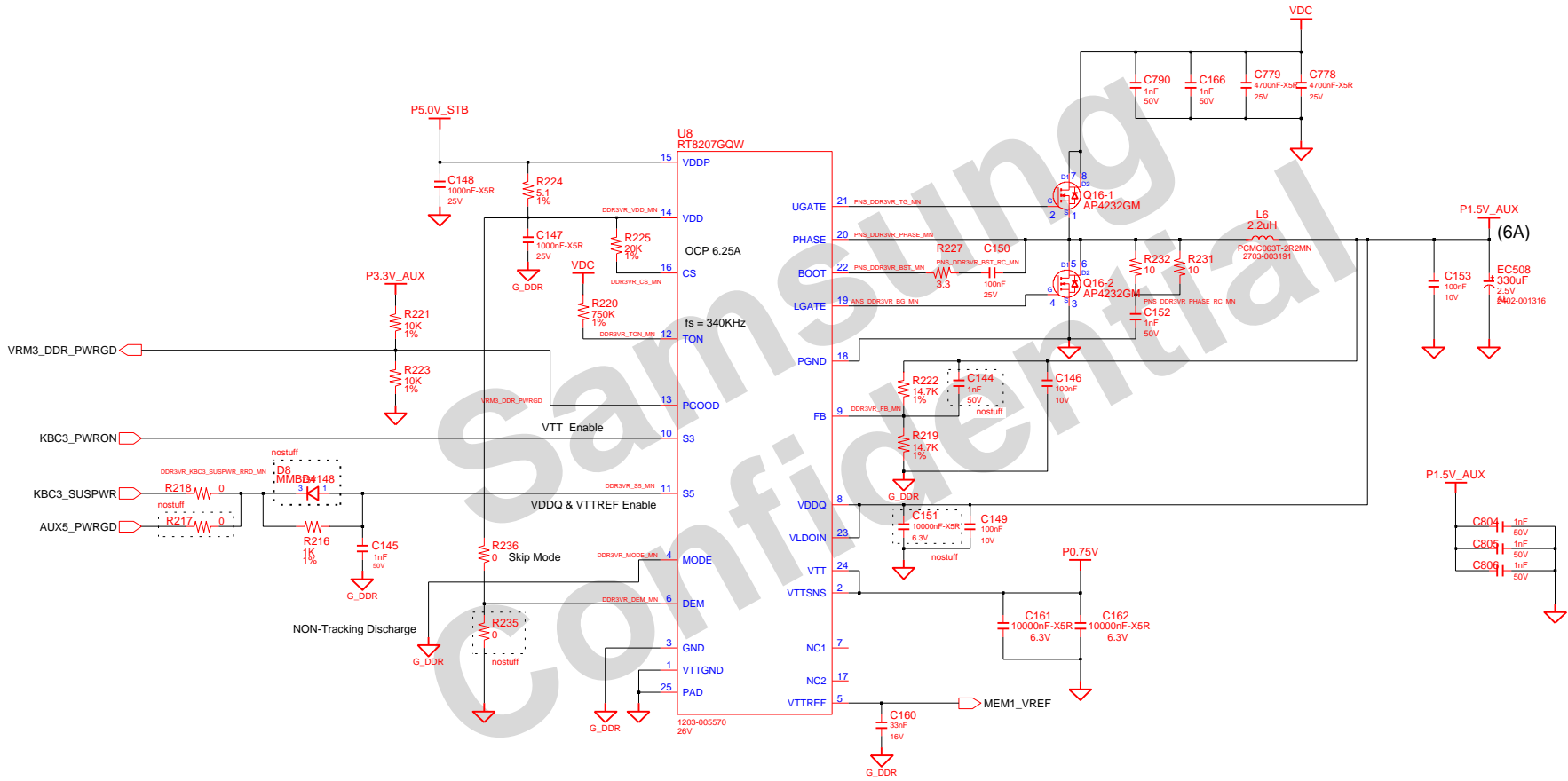


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN P5.0V & P3.3V	SAMSUNG ELECTRONICS	
CHECK	HJ, KIM	DEV. STEP	MP	PART NO.			BA41-0XXXXA
APPROVAL	JS, EUH	REV	1.5				
MODULE CODE	LAST EDIT		November 27, 2008 15:50:17 PM				PAGE 35 OF 44

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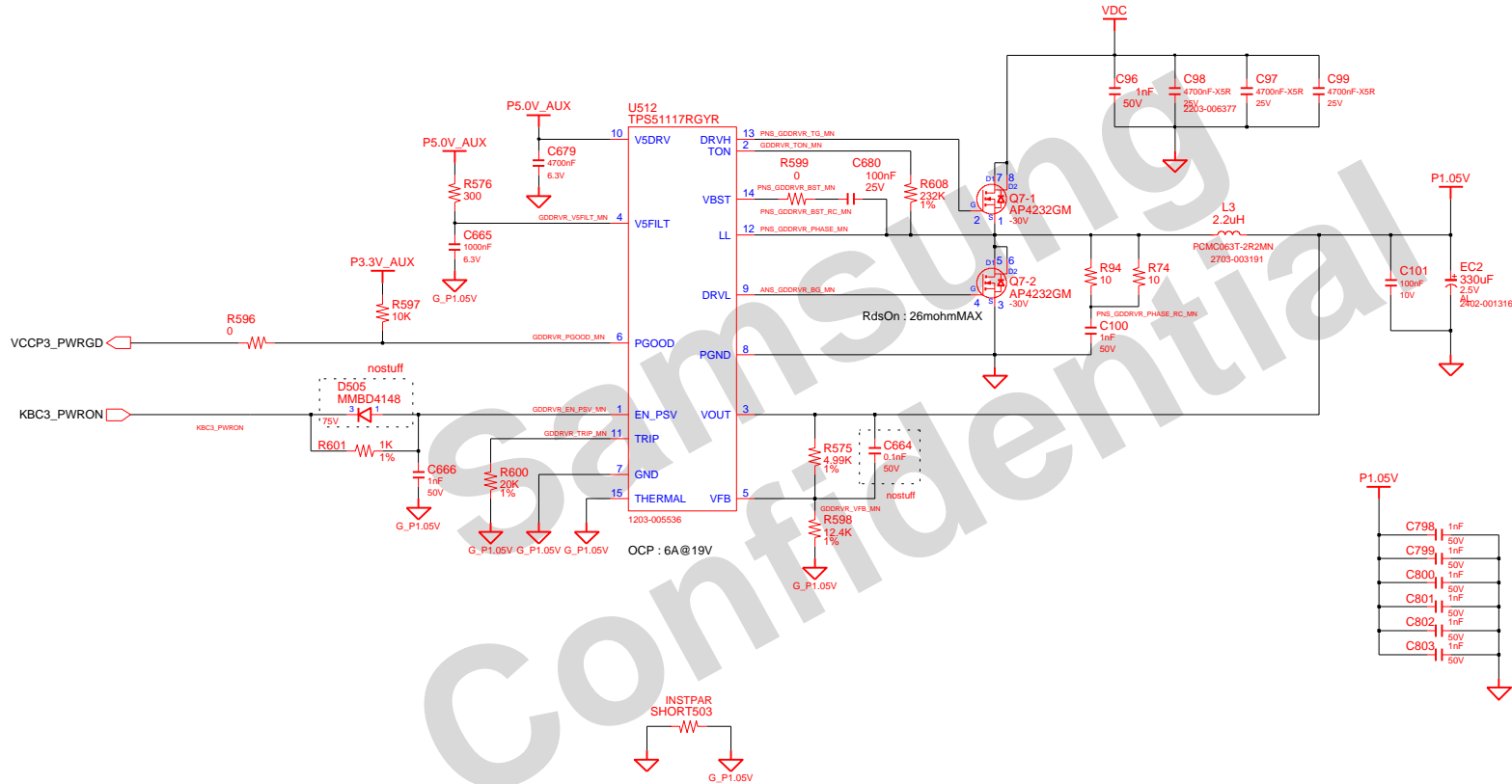
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DDR3 Power



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN DDR3 POWER	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP			
APPROVAL	JS, EUH	REV	1.5			
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 36 OF 44		

CHIPSET POWER(P1.05V)

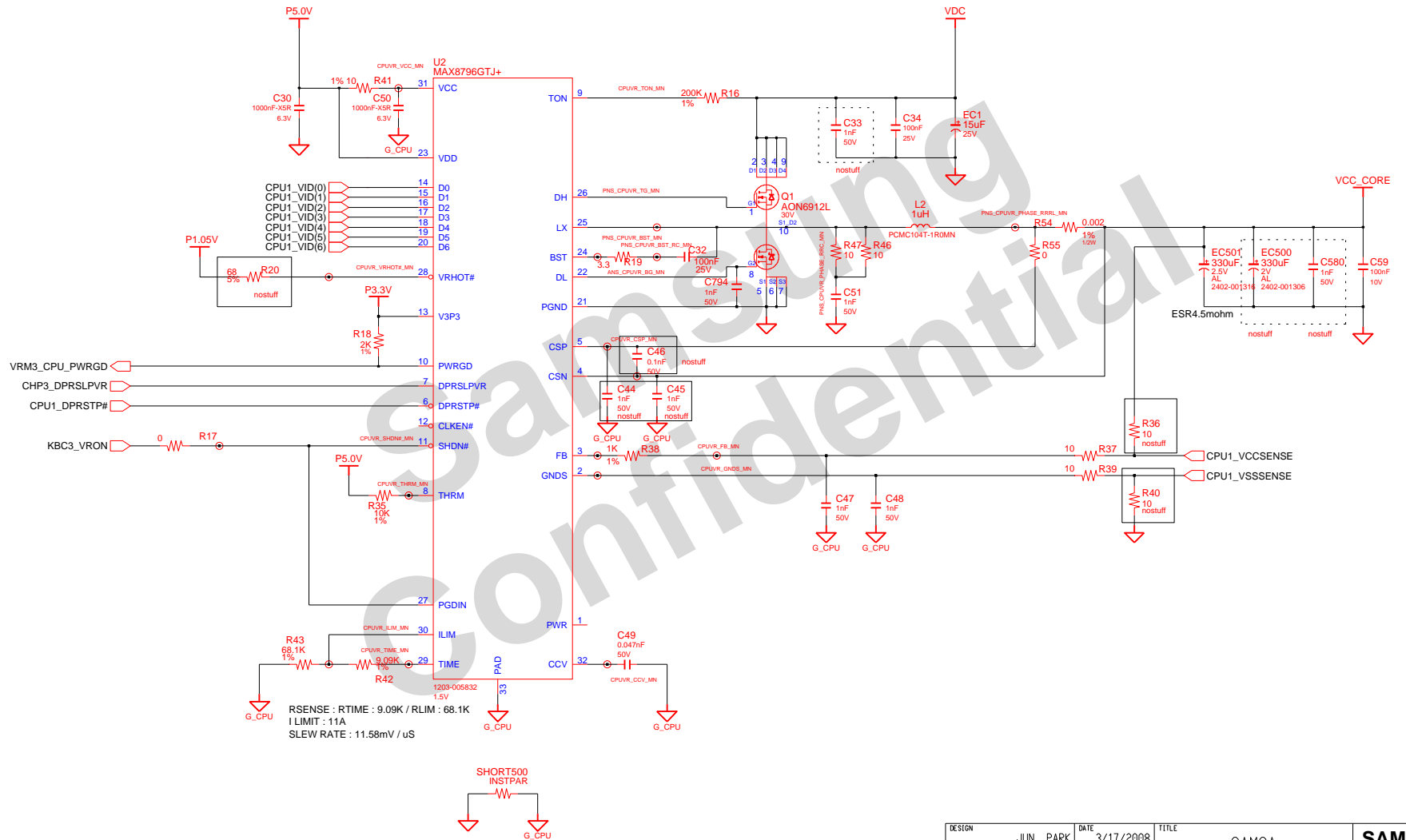


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN P1.05V	SAMSUNG ELECTRONICS	
CHECK	HJ, KIM	DEV. STEP	MP	PART NO.			BA41-0XXXXA
APPROVAL	JS, EUH	REV	1.5				
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE			37 OF 44

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CPU VRM POWER

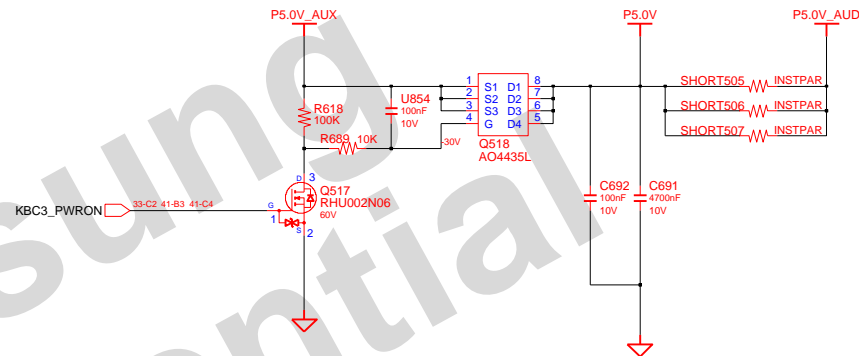
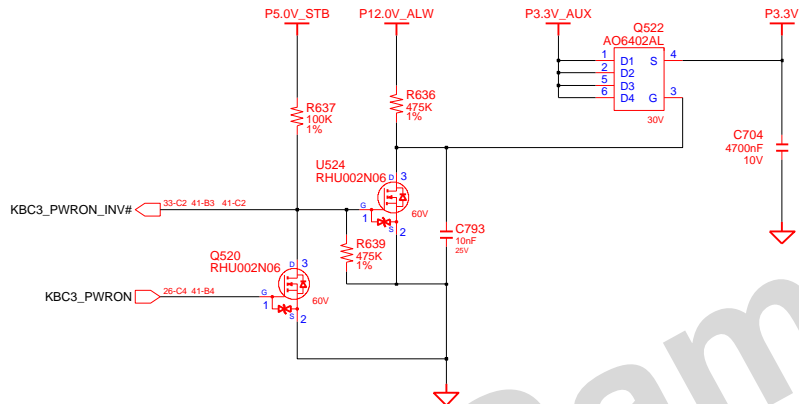


DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-0XXXXA
CHECK	HJ, KIM	DEV. STEP	MP	SAMOA MAIN CPU VRM POWER	
APPROVAL	JS, EUH	REV	1.5		
MODULE CODE		LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 39 OF 44	

SWITCHED POWER

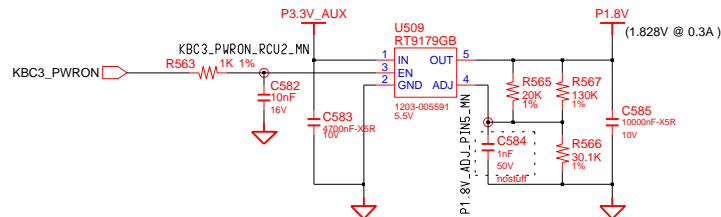
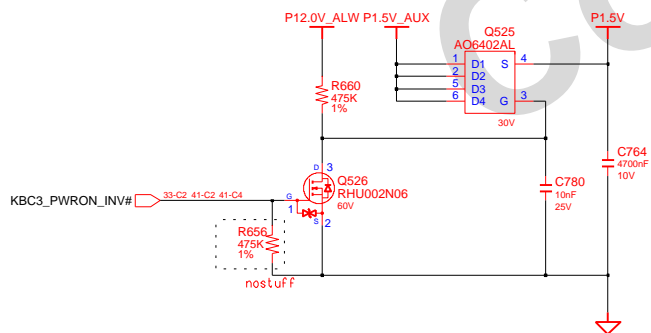
Switched Power On (P3.3V)

Switched Power On (P5V)



Switched Power On (P1.5V)

P1.8V



DESIGN	JUN, PARK	DATE	3/17/2008	TITLE	SAMOA MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	HJ, KIM	DEV. STEP	MP	PART NO.		
APPROVAL	JS, EUH	REV	1.5	LAST EDIT	November 27, 2008 15:50:17 PM	PAGE 41 OF 44
MODULE CODE						