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# MONACO-R

CPU : MEROM  
Chip Set : ATI RS600ME & SB600  
Remarks : DESKNOTE

Model Name : MONACO-R  
PBA Name : MAIN  
PCB Code : BA41-00720A  
Dev. Step : PR  
Revision : 1.1  
T.R. Date : 2007.01.03

DRAW	CHECK	APPROVAL
SON, C.W	LEE, S.P	LIM, J.G

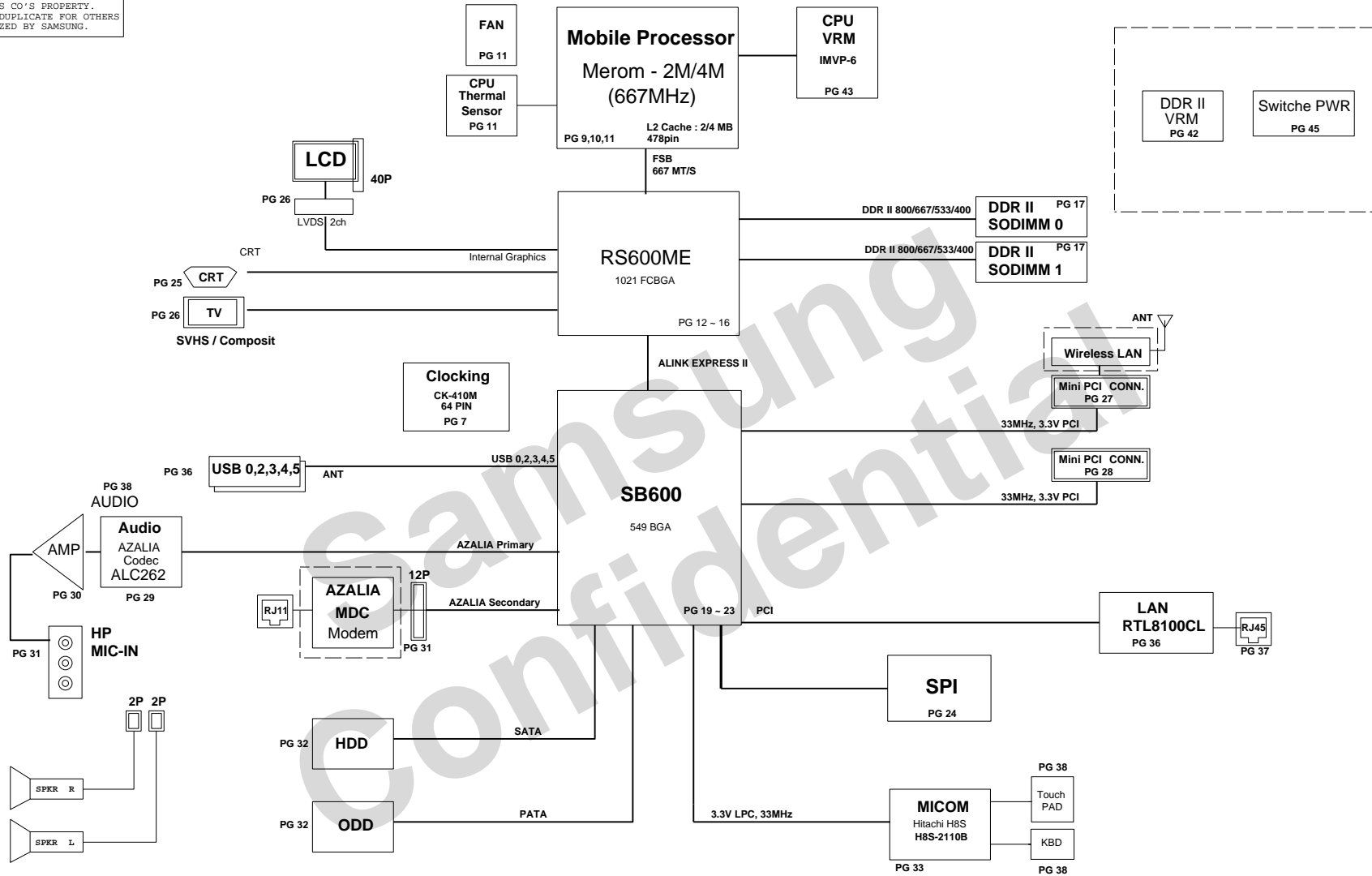
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DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN COVER	<b>SAMSUNG</b> ELECTRONICS	
CHECK	LEE, S.P	DEV. STEP	PR	PART NO.			BA41-00720A
APPROVAL	LIM, J.G	REV	1.1				
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE			1 OF 47

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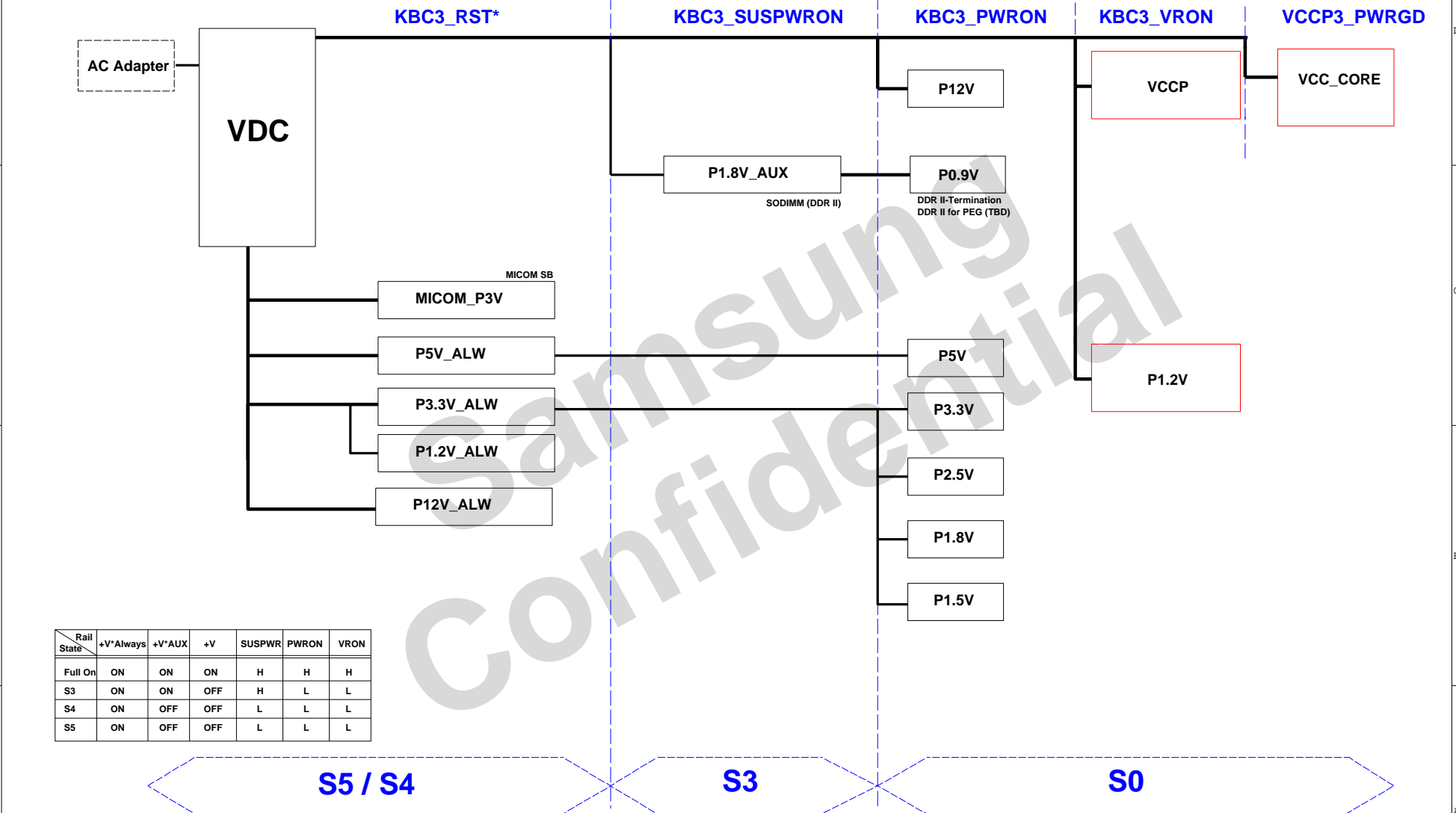


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APPROVAL	LIM, J.G	REV	1.1			
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# Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	L	L	L
S5	ON	OFF	OFF	L	L	L

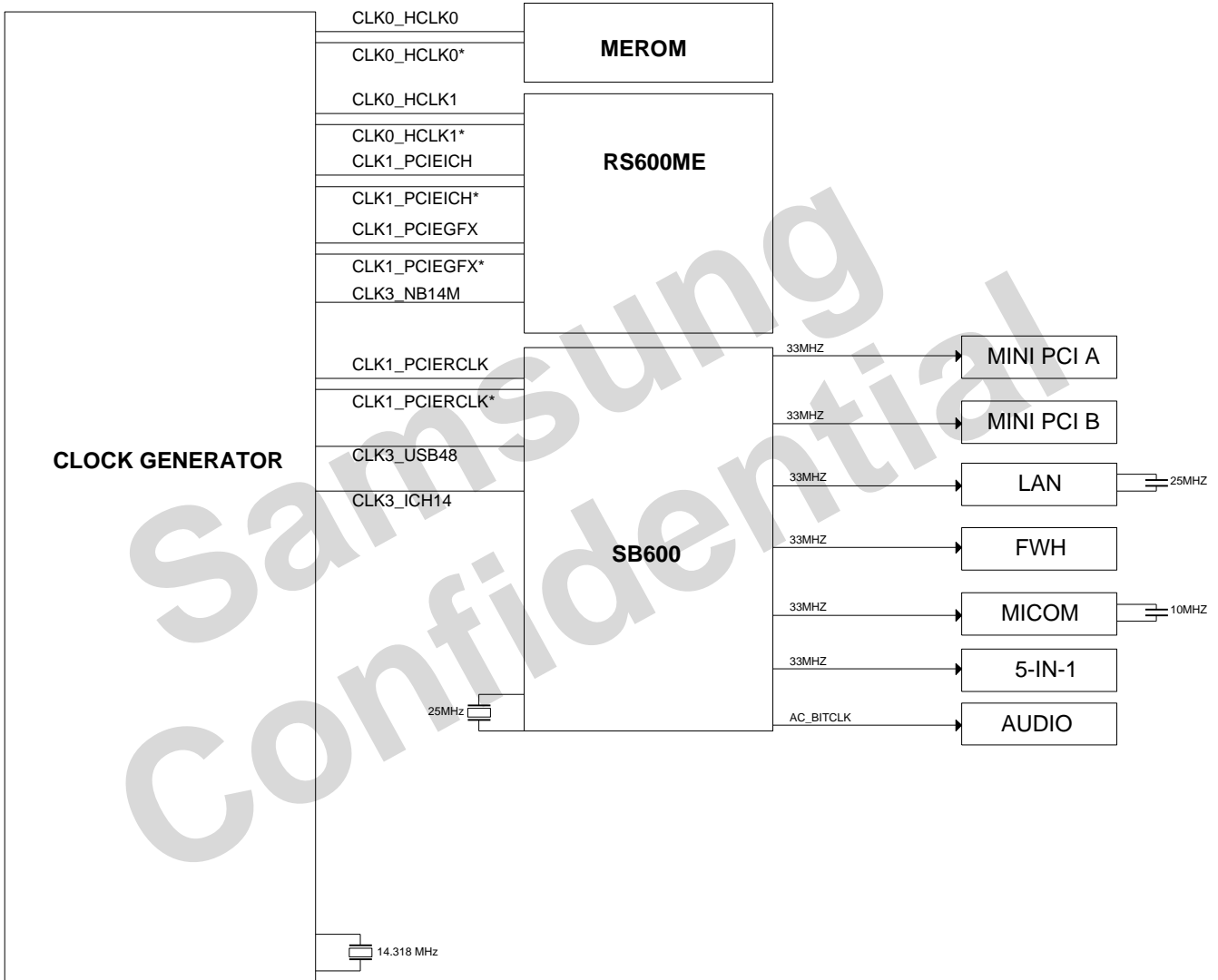
**S5 / S4**

**S3**

**S0**

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN POWER DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 3 OF 47		

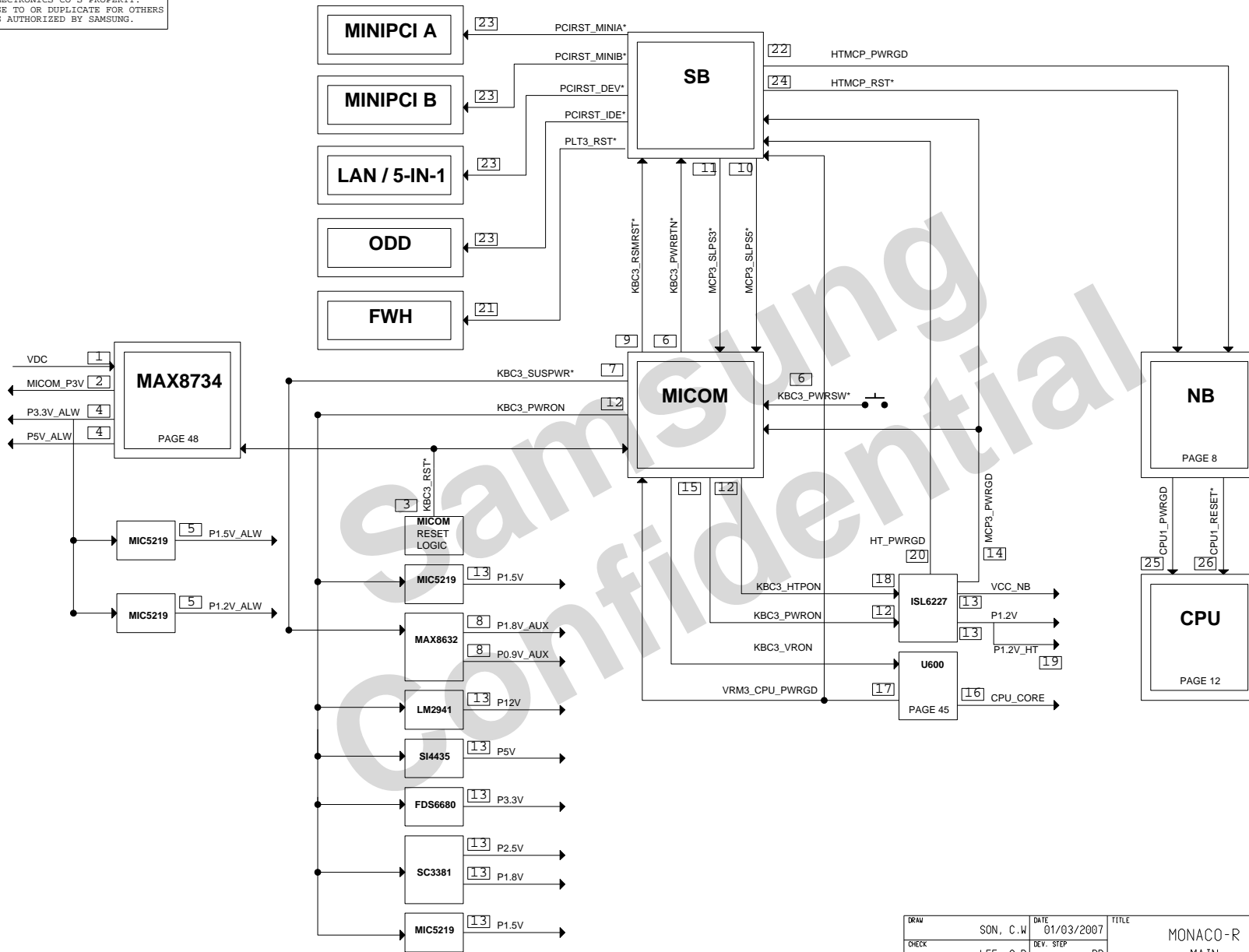
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DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN CLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS	
CHECK	LEE, S.P	DEV. STEP	PR	PART NO.			BA41-00720A
APPROVAL	LIM, J.G	REV	1.1				
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CHECK	LEE, S.P	DEV. STEP	PR	REV	1.1	
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MODULE CODE	undefined					

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## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
MINIPCI A	AD21	0	A,B
MINIPCI B	AD22	1	C,D
LAN	AD23	2	D
5-IN-1	AD24	3	B
USB	AD30(internal)		
Hub to PCI	AD31(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD31(internal)		

### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	25MHz	MCP51	MCP51 REF CLOCK
Crystal	32.768KHz	MCP51	Real Time Clock
Crystal	10MHz	MICOM	H8S-2110B
Crystal	27MHz	CSTMV	TV OUT
Crystal	25MHz	LAN	RTL8110CL

### Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU CORE	Core voltage for AMD SEMPRON (1.308-1.068V)
VCC_NB	SEMPRON Processor Hyper Transport (1.2V) North Bridge Core Voltage
P0.9V_AUX	0.9V switched power rail (off in S4-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWS	5V power rail (Always On)
P3.3V_ALWS	3.3V power rail (Always On)
P1.5V_ALWS	1.5V power rail (Always On)

### CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.5500 V	1 0 0 0 0 0	0.7625 V
0 0 0 0 0 1	1.5250 V	1 0 0 0 0 1	0.7500 V
0 0 0 0 1 0	1.5000 V	1 0 0 0 1 0	0.7375 V
0 0 0 0 1 1	1.4750 V	1 0 0 0 1 1	0.7250 V
0 0 0 1 0 0	1.4500 V	1 0 0 1 0 0	0.7125 V
0 0 0 1 0 1	1.4250 V	1 0 0 1 0 1	0.7000 V
0 0 0 1 1 0	1.4000 V	1 0 0 1 1 0	0.6875 V
0 0 0 1 1 1	1.3750 V	1 0 0 1 1 1	0.6750 V
0 0 1 0 0 0	1.3500 V	1 0 1 0 0 0	0.6625 V
0 0 1 0 0 1	1.3250 V	1 0 1 0 0 1	0.6500 V
0 0 1 0 1 0	1.3000 V	1 0 1 0 1 0	0.6375 V
0 0 1 0 1 1	1.2750 V	1 0 1 0 1 1	0.6250 V
0 0 1 1 0 0	1.2500 V	1 0 1 1 0 0	0.6125 V
0 0 1 1 0 1	1.2250 V	1 0 1 1 0 1	0.6000 V
0 0 1 1 1 0	1.2000 V	1 0 1 1 1 0	0.5875 V
0 0 1 1 1 1	1.1750 V	1 0 1 1 1 1	0.5750 V
0 1 0 0 0 0	1.1500 V	1 1 0 0 0 0	0.5625 V
0 1 0 0 0 1	1.1250 V	1 1 0 0 0 1	0.5500 V
0 1 0 0 1 0	1.1000 V	1 1 0 0 1 0	0.5375 V
0 1 0 0 1 1	1.0750 V	1 1 0 0 1 1	0.5250 V
0 1 0 1 0 0	1.0500 V	1 1 0 1 0 0	0.5125 V
0 1 0 1 0 1	1.0250 V	1 1 0 1 0 1	0.5000 V
0 1 0 1 1 0	1.0000 V	1 1 0 1 1 0	0.4875 V
0 1 0 1 1 1	0.9750 V	1 1 0 1 1 1	0.4750 V
0 1 1 0 0 0	0.9500 V	1 1 1 0 0 0	0.4625 V
0 1 1 0 0 1	0.9250 V	1 1 1 0 0 1	0.4500 V
0 1 1 0 1 0	0.9000 V	1 1 1 0 1 0	0.4375 V
0 1 1 0 1 1	0.8750 V	1 1 1 0 1 1	0.4250 V
0 1 1 1 0 0	0.8500 V	1 1 1 1 0 0	0.4125 V
0 1 1 1 0 1	0.8250 V	1 1 1 1 0 1	0.4000 V
0 1 1 1 1 0	0.8000 V	1 1 1 1 1 0	0.3875 V
0 1 1 1 1 1	0.7750 V	1 1 1 1 1 1	0.3750 V

### I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
W83L786NG(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor

### USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2, 3	SYSTEM PORT B
4, 5	SYSTEM PORT C
6	DMB

### System Power States

CHP3\_SLPS1\* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3\_SLPS3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3\_SLPS4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

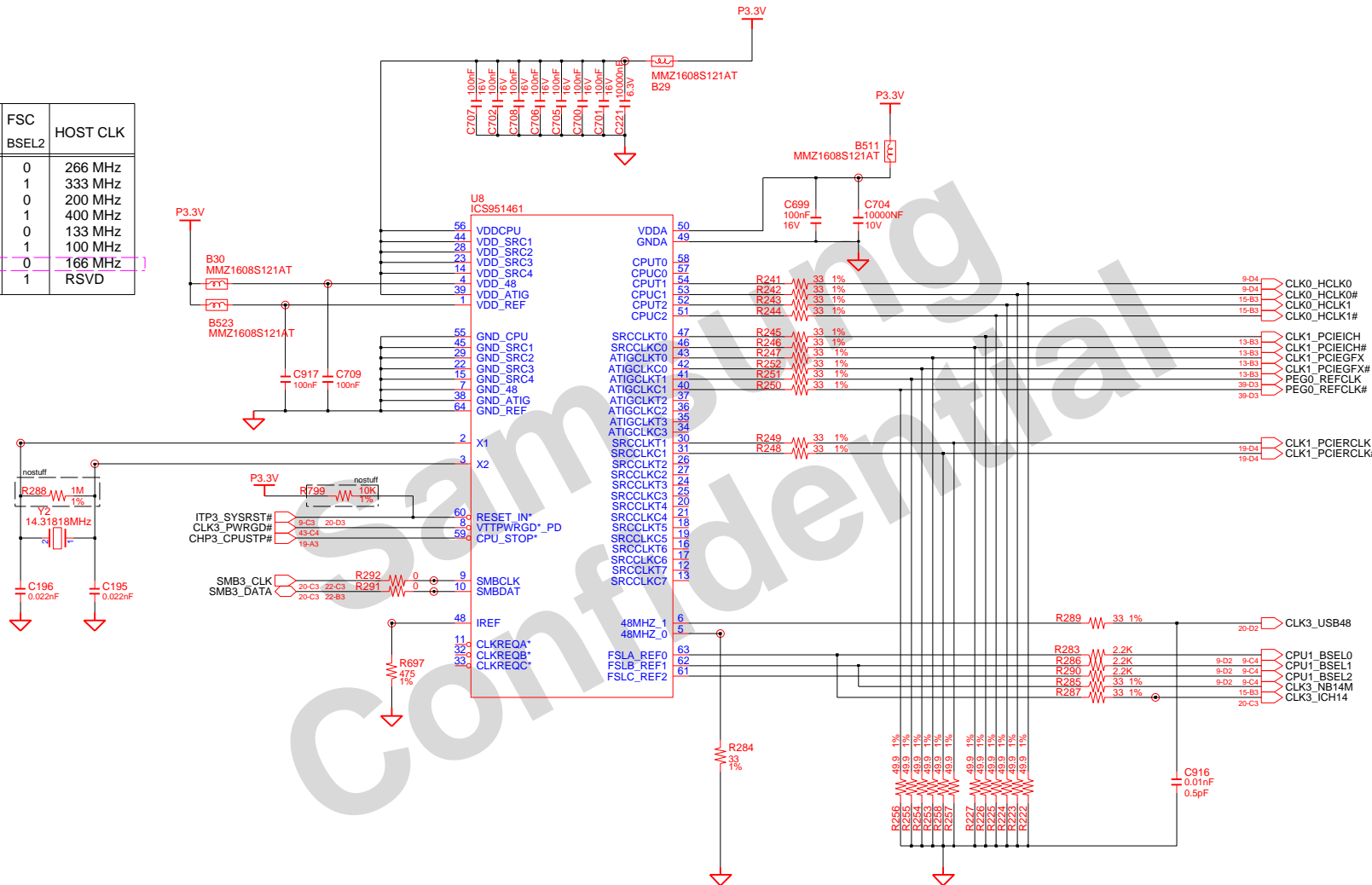
CHP3\_SLPS5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 6 OF 47		

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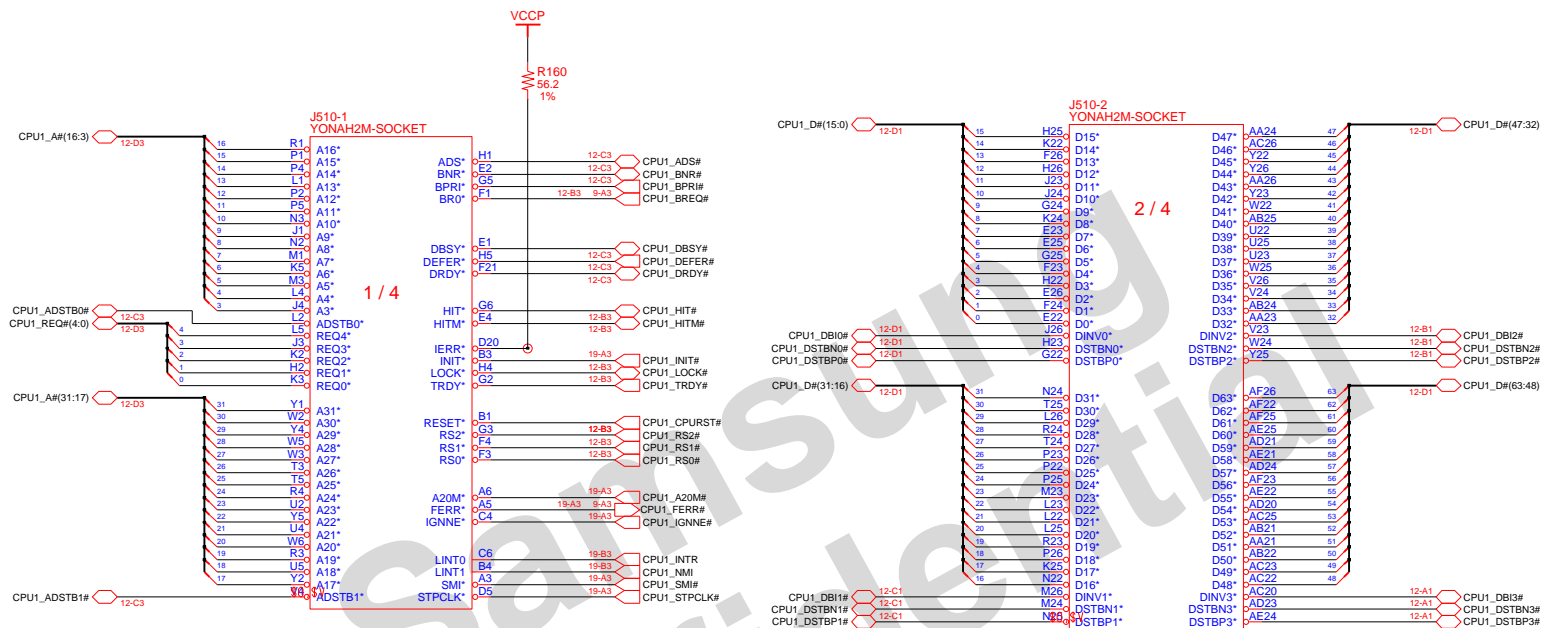
CPU			
FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN CLOCK GENERATOR	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR	REV	1.1	
APPROVAL	LIM, J.G	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	7 OF 47	

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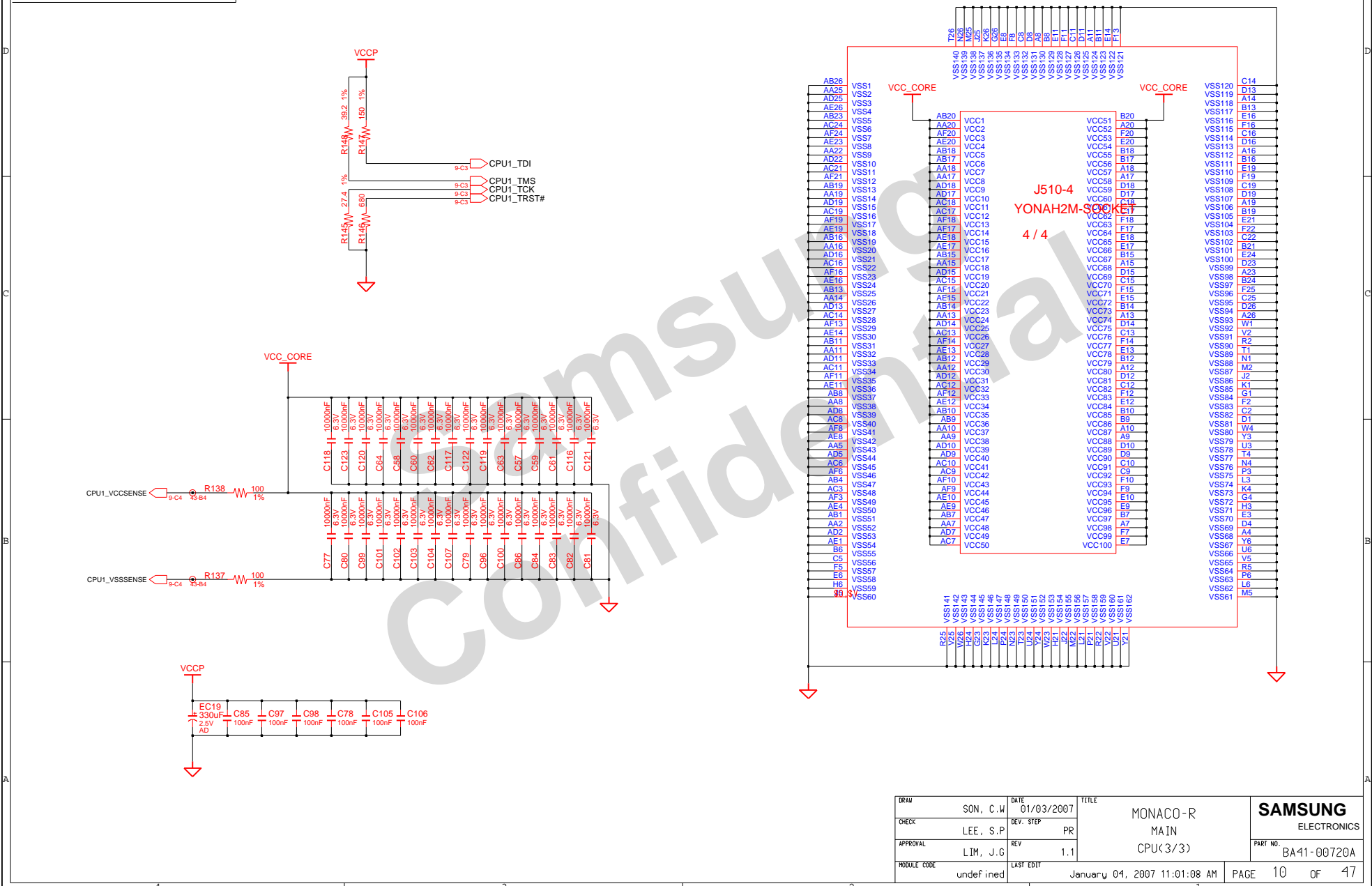
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CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
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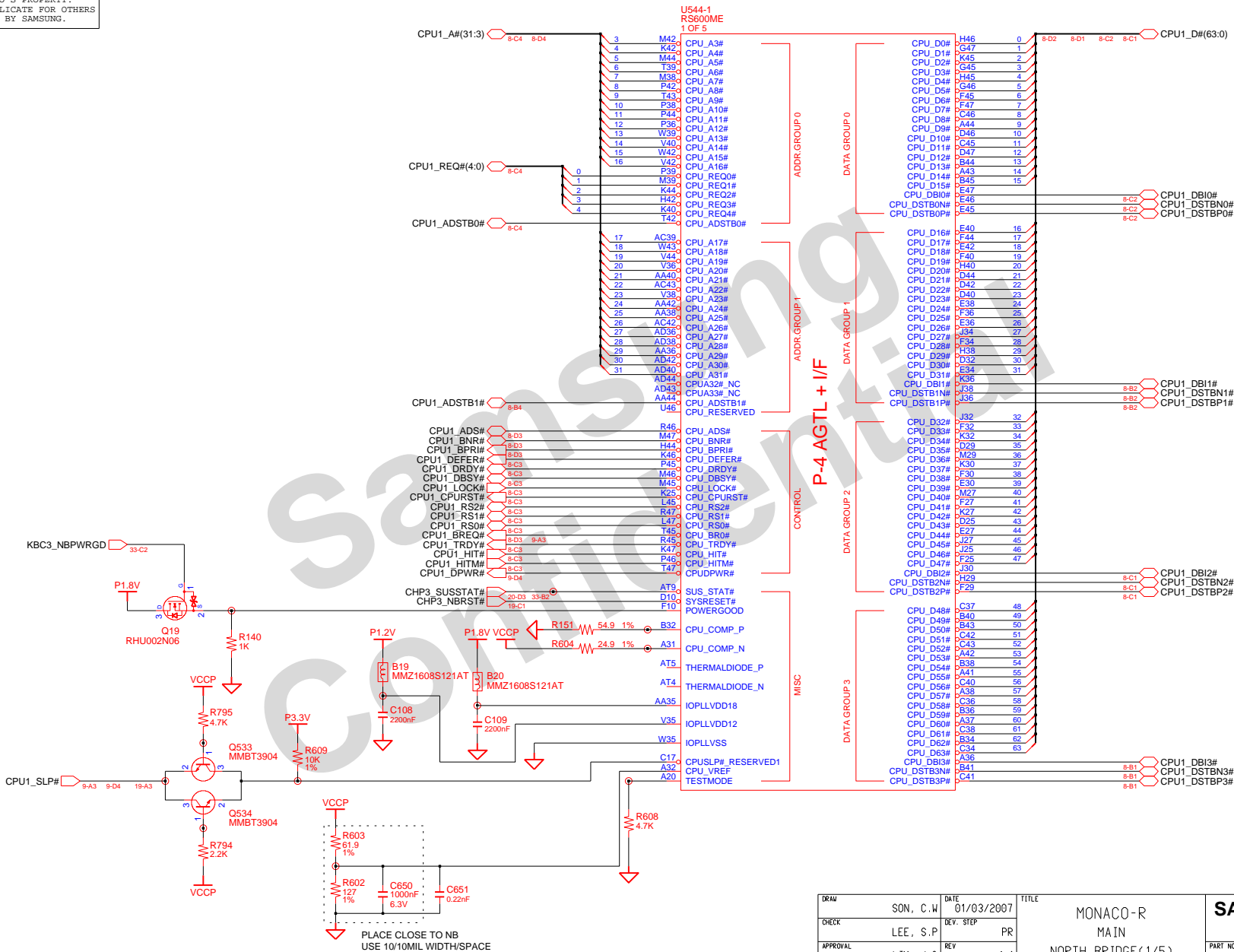


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CHECK	LEE, S.P	DEV. STEP	PR				
APPROVAL	LIM, J.G	REV	1.1				
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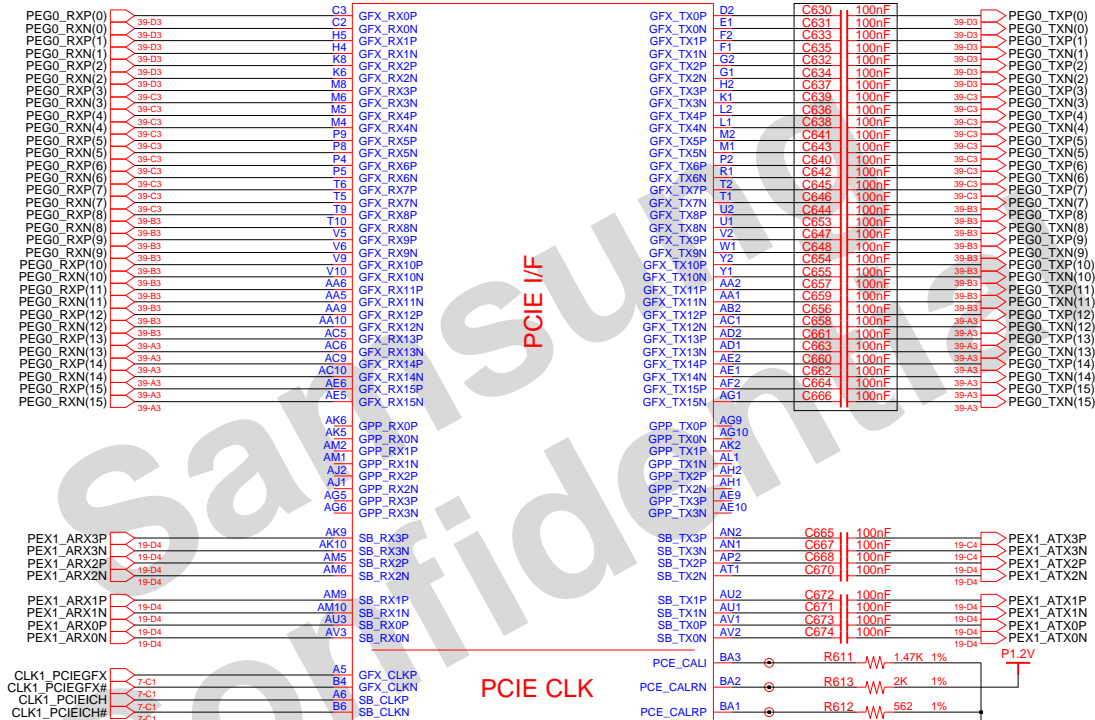
PLACE CLOSE TO NB  
USE 10/10ML WIDTH/SPACE

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.1	NORTH BRIDGE(1/5)	PART NO.	BA41-00720A
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	12	OF 47

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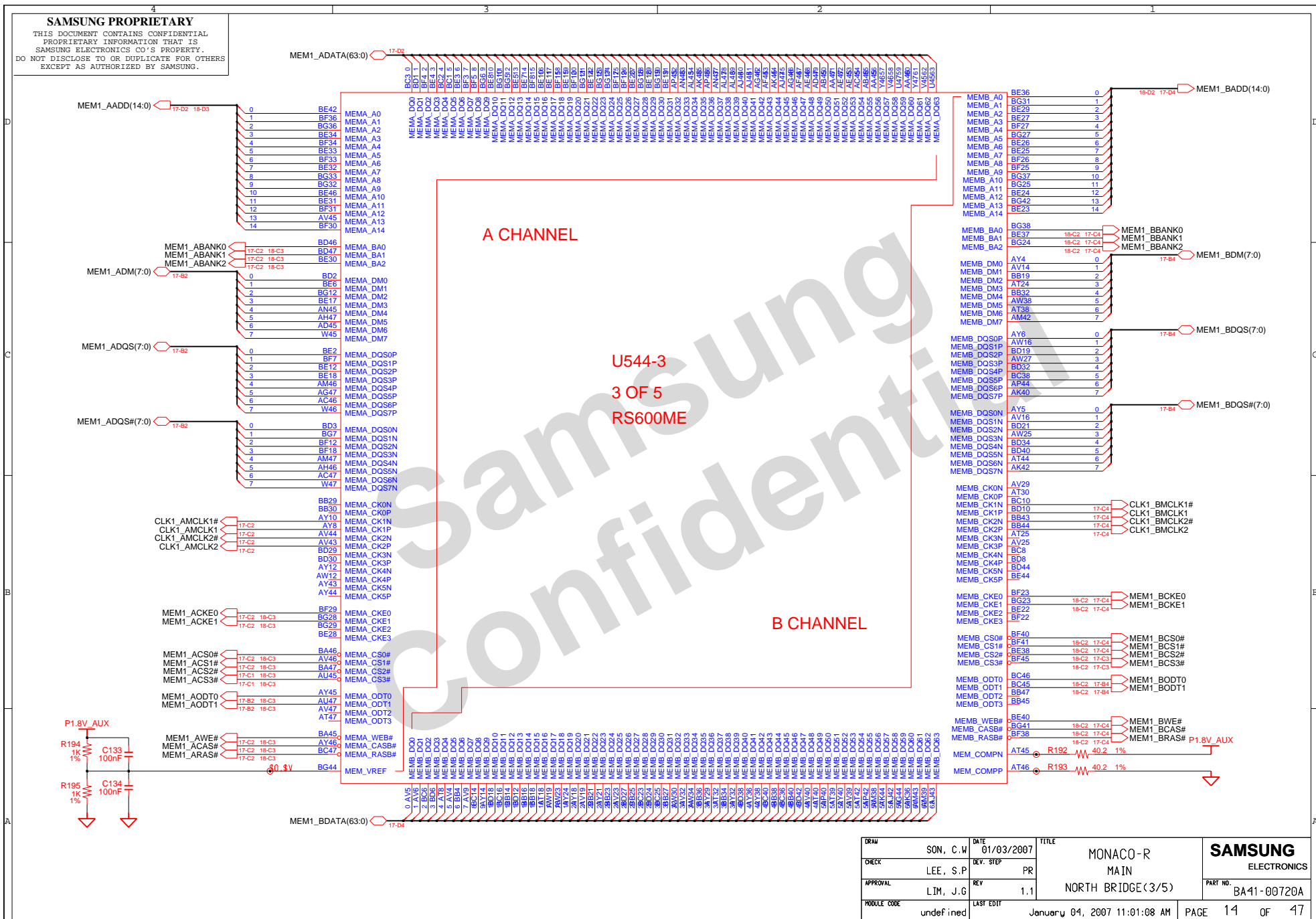
U544-2  
RS600ME  
2 OF 5



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APPROVAL	LIM, J.G	REV	1.1	NORTH BRIDGE(2/5)	PART NO.	BA41-00720A
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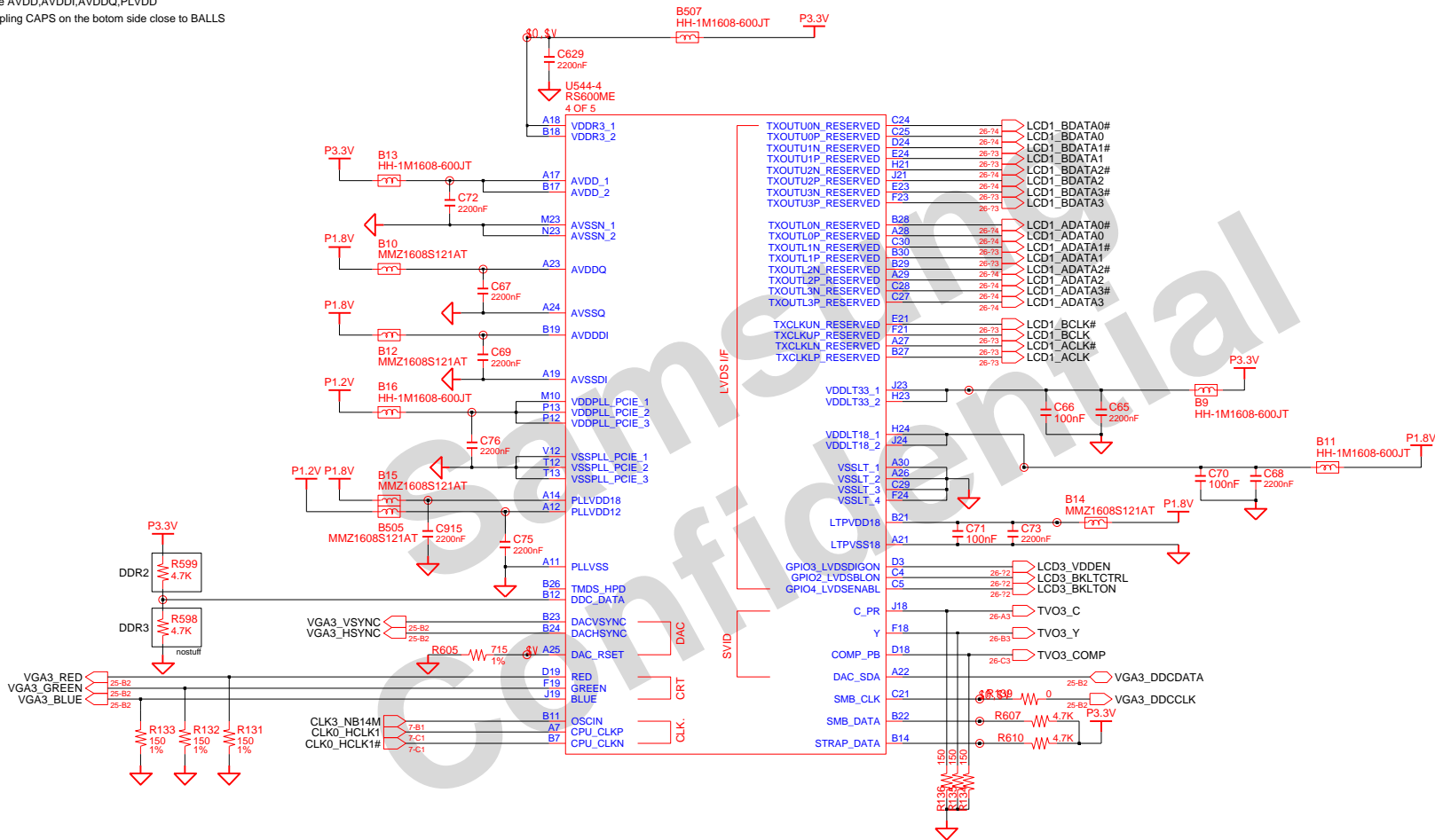


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CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
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Put the AVDD,AVDDI,AVDDQ,PLVDD decoupling CAPS on the botom side close to BALLS



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CHECK	LEE, S.P	DEV. STEP	PR	NORTH BRIDGE(4/5)		
APPROVAL	LIM, J.G	REV	1.1	PART NO.		BA41-00720A
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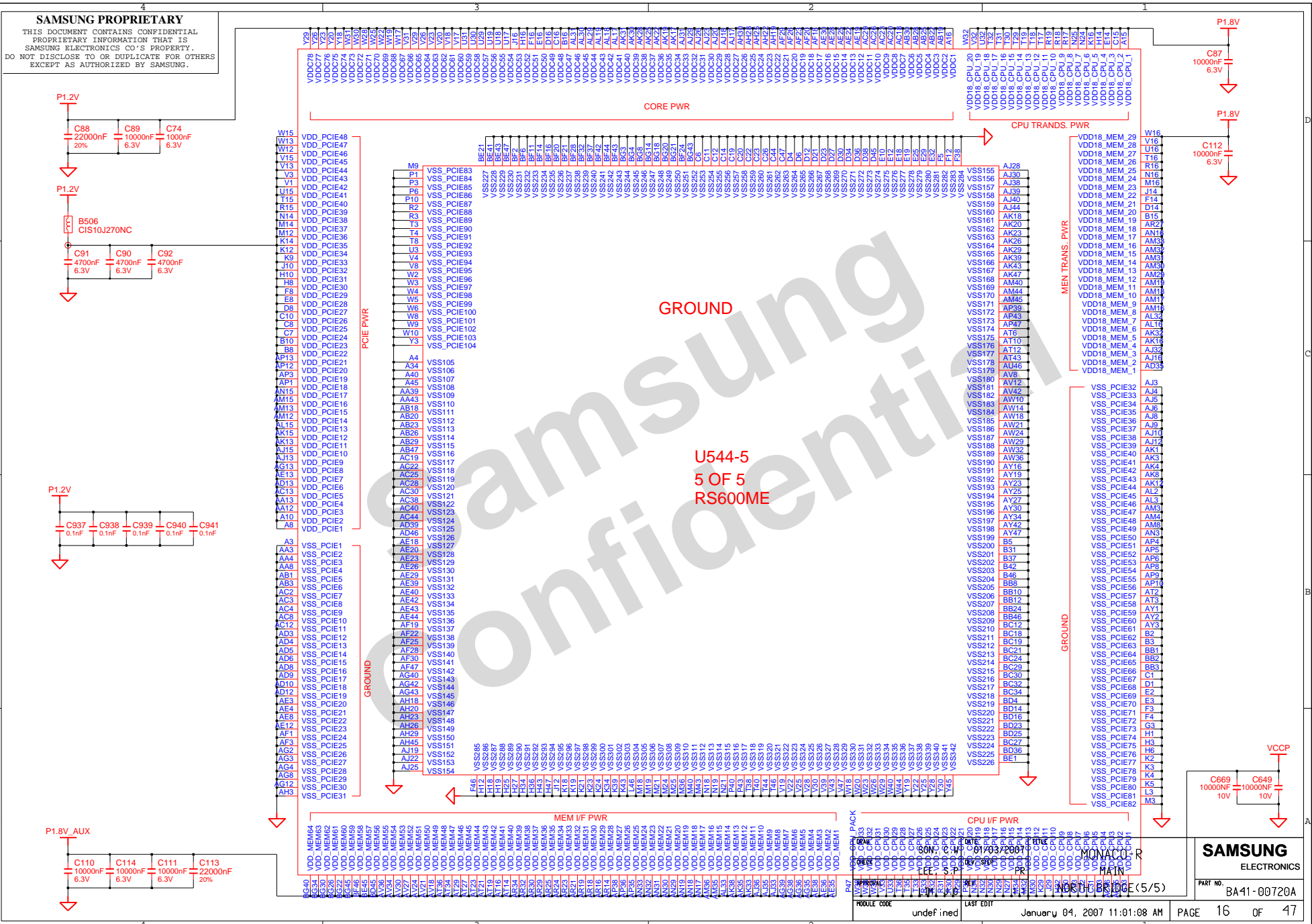


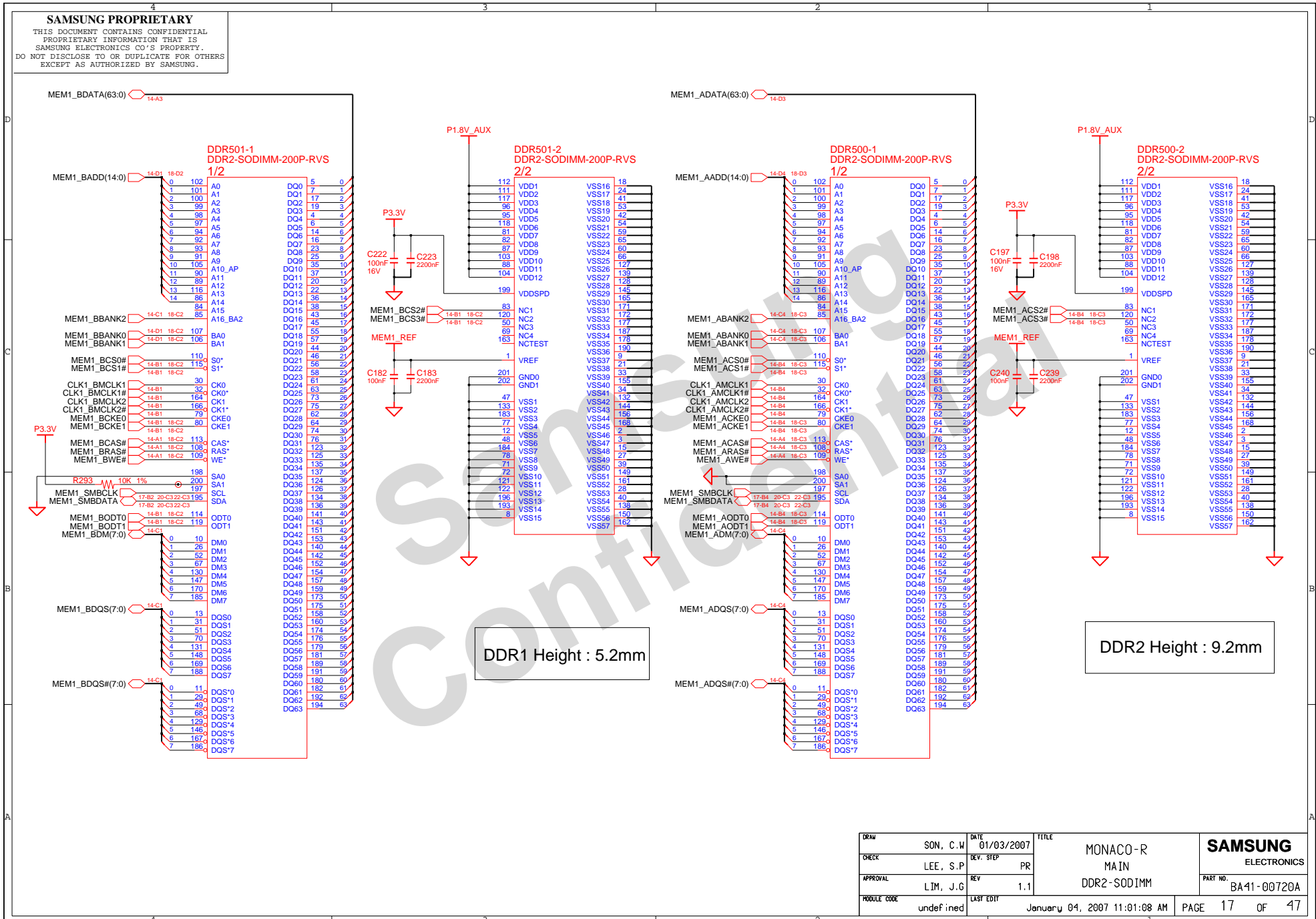
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SAMSUNG ELECTRONICS logo and part number 'BA41-00720A'. Includes a revision indicator '(5/5)'.



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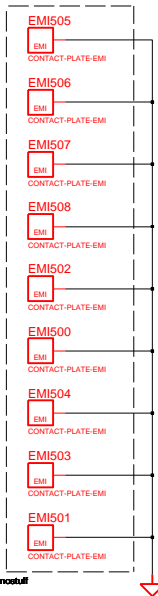
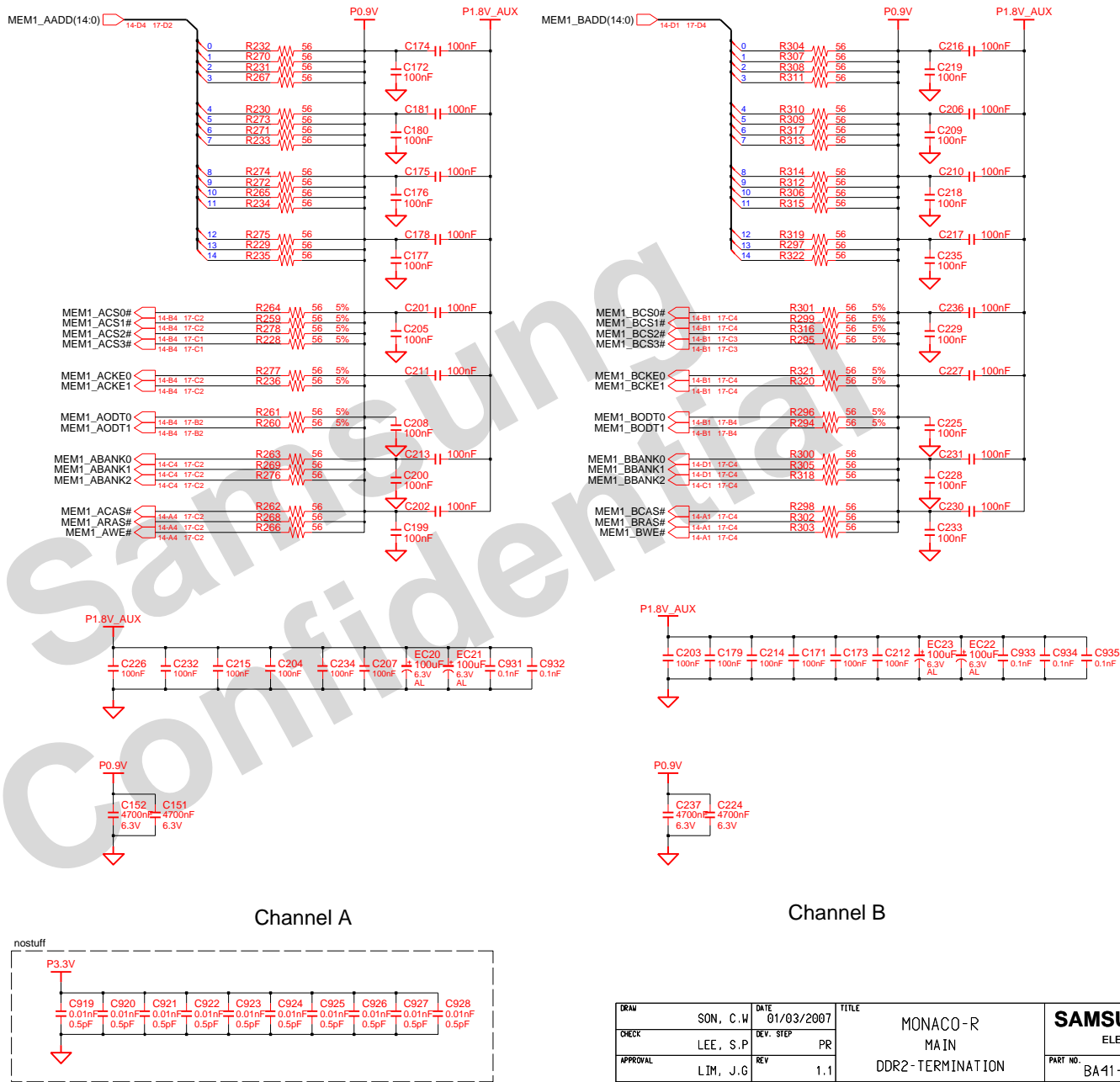
DDR1 Height : 5.2mm

DDR2 Height : 9.2mm

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.1	DDR2-SODIMM	PART NO.	BA41-00720A
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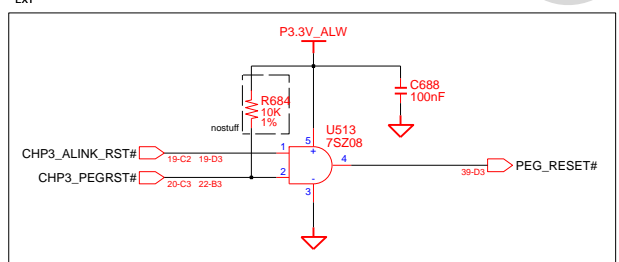
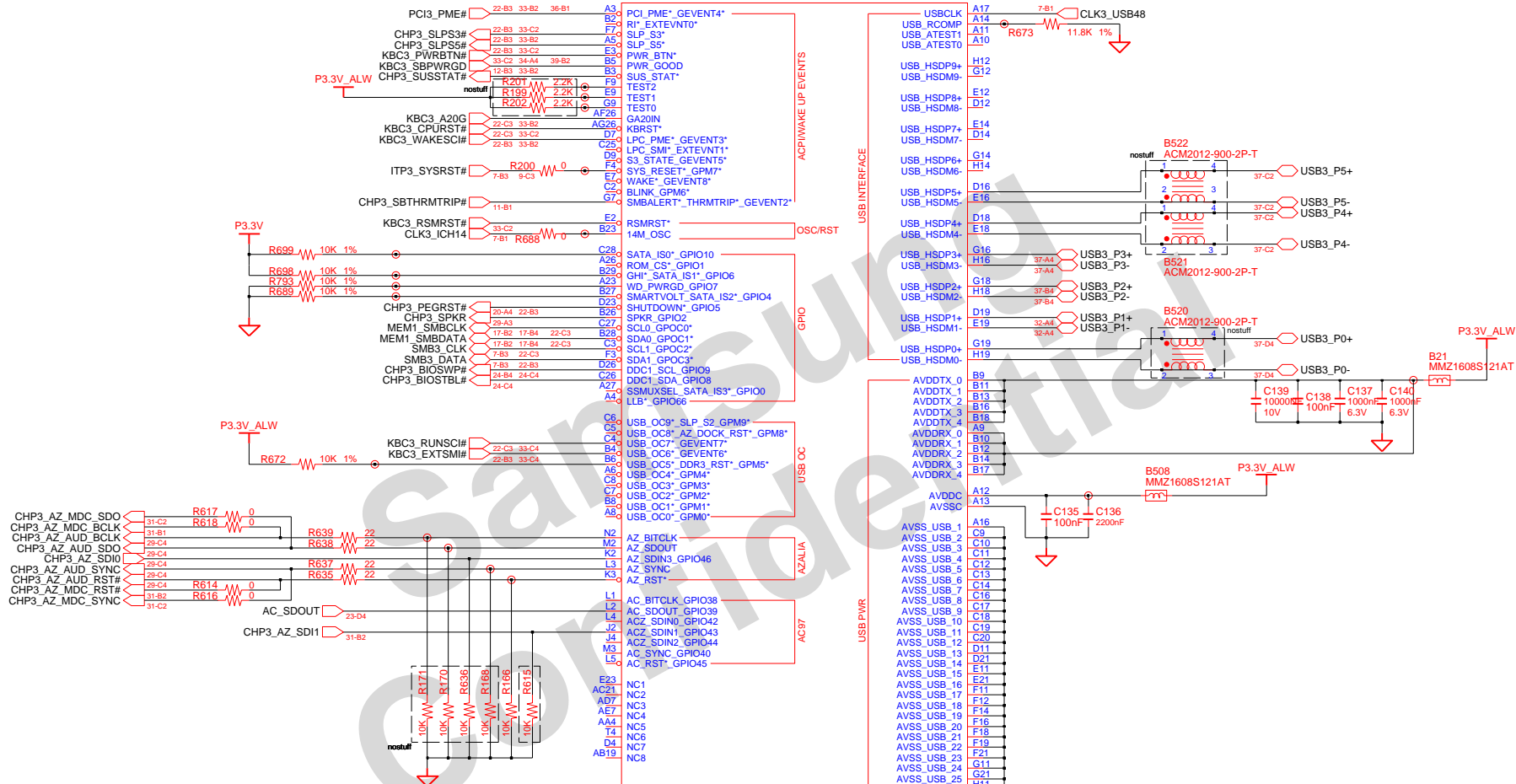
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CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
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**U510-2  
218S6ECLA21FG  
2 / 4**



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN SOUTH BRIDGE(2/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
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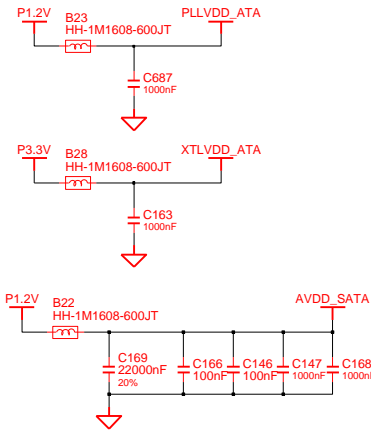
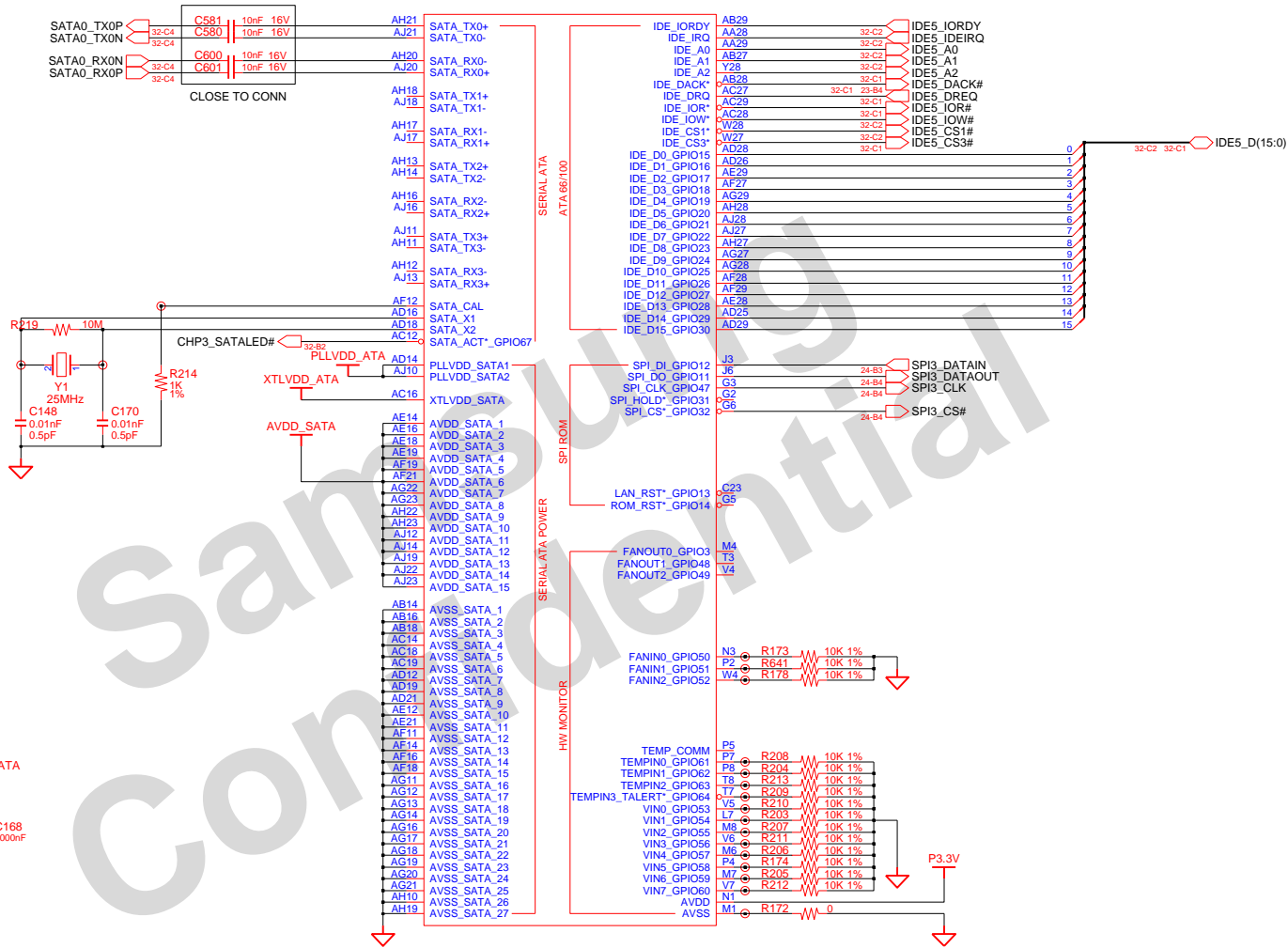
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**U510-3  
218S6ECLA21FG**

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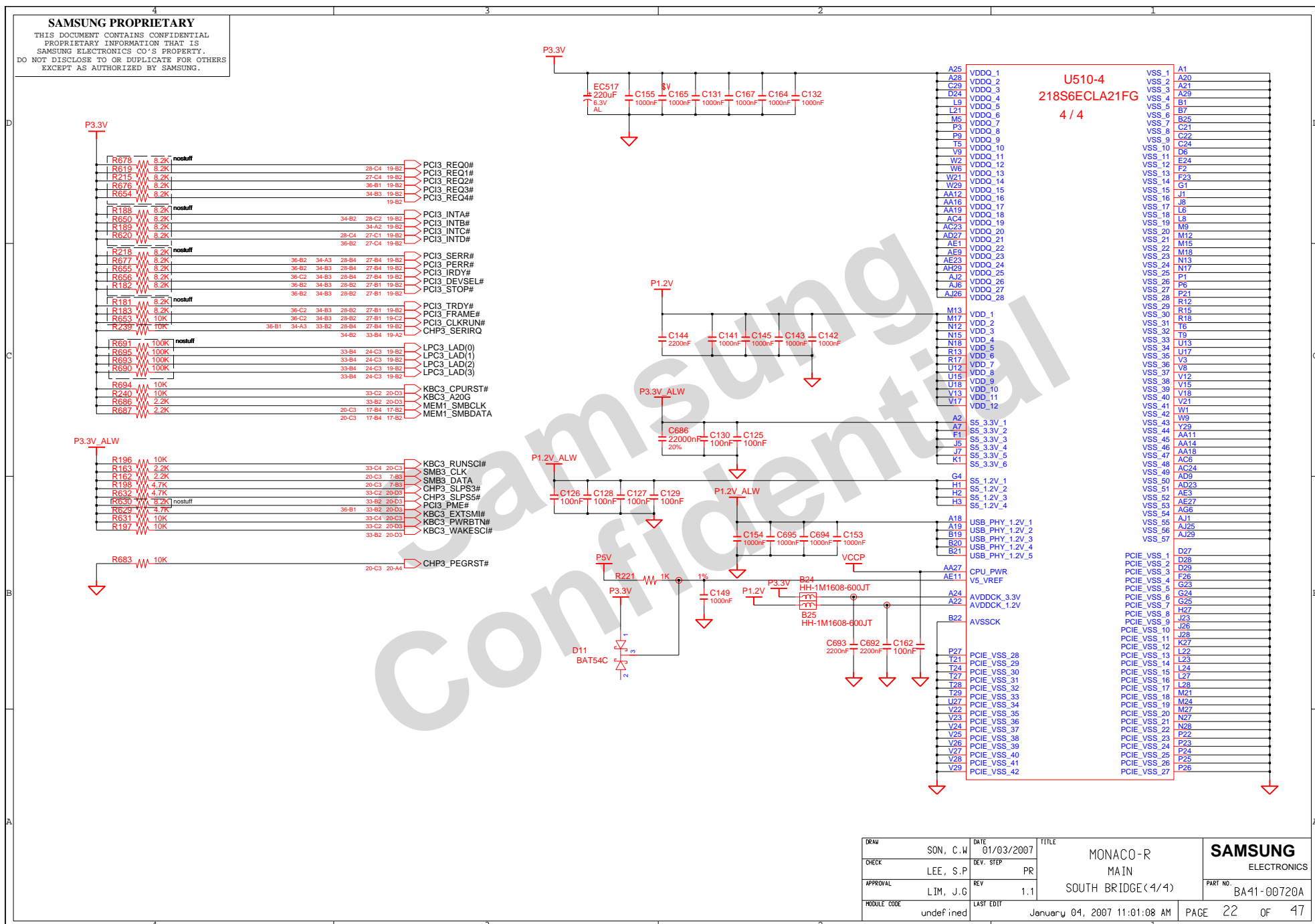
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DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	SOUTH BRIDGE(3/4)		
APPROVAL	LIM, J.G	REV	1.1			PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	21	OF 47

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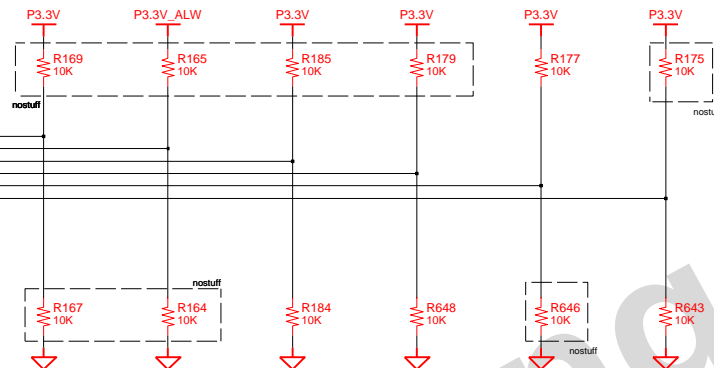
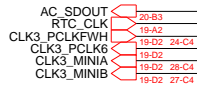
A25	VDD0_1	VSS_1	A1
A28	VDD0_2	VSS_2	A20
C29	VDD0_3	VSS_3	A21
D24	VDD0_4	VSS_4	A29
L3	VDD0_5	VSS_5	B1
L21	VDD0_6	VSS_6	B7
M5	VDD0_7	VSS_7	B5
P3	VDD0_8	VSS_8	C21
P8	VDD0_9	VSS_9	C22
T5	VDD0_10	VSS_10	D6
W2	VDD0_11	VSS_11	E24
W6	VDD0_12	VSS_12	F2
W21	VDD0_13	VSS_13	F23
W23	VDD0_14	VSS_14	G1
AA12	VDD0_15	VSS_15	J1
AA16	VDD0_16	VSS_16	J8
AA19	VDD0_17	VSS_17	L8
AC4	VDD0_18	VSS_18	L8
AC23	VDD0_19	VSS_19	M9
AD27	VDD0_20	VSS_20	M12
AE1	VDD0_21	VSS_21	M15
AE9	VDD0_22	VSS_22	M15
AE23	VDD0_23	VSS_23	M18
AH29	VDD0_24	VSS_24	N17
AJ2	VDD0_25	VSS_25	N17
AJ6	VDD0_26	VSS_26	P1
AJ26	VDD0_27	VSS_27	P6
	VDD0_28	VSS_28	R12
	VDD_1	VSS_29	R15
M13	VDD_2	VSS_30	R18
M17	VDD_3	VSS_31	T6
N12	VDD_4	VSS_32	T9
N15	VDD_5	VSS_33	U13
N18	VDD_6	VSS_34	U17
R13	VDD_7	VSS_35	V3
R17	VDD_8	VSS_36	V8
U12	VDD_9	VSS_37	V12
U15	VDD_10	VSS_38	V15
U18	VDD_11	VSS_39	V18
U19	VDD_12	VSS_40	V21
V17	VSS_41	VSS_42	W1
	VSS_43	VSS_44	W9
A2	SS_3.3V_1	VSS_45	Y29
A7	SS_3.3V_2	VSS_46	AA11
F1	SS_3.3V_3	VSS_47	AA14
J5	SS_3.3V_4	VSS_48	AA18
K1	SS_3.3V_5	VSS_49	AC6
	SS_3.3V_6	VSS_50	AC24
G4	SS_1.2V_1	VSS_51	AD9
H1	SS_1.2V_2	VSS_52	AD23
H2	SS_1.2V_3	VSS_53	AE3
H3	SS_1.2V_4	VSS_54	AE7
		VSS_55	AG6
A18	USB_PHY_1.2V_1	VSS_56	A1
A19	USB_PHY_1.2V_2	VSS_57	A25
B19	USB_PHY_1.2V_3		A29
B20	USB_PHY_1.2V_4		D27
B21	USB_PHY_1.2V_5		D28
AA27	CPU_PWR		D29
AE11	VS_VREF		F26
A24	AVDDCK_3.3V		G23
A22	AVDDCK_1.2V		G24
			G25
B22	AVSSCK		H27
			J23
			J26
			K27
			L22
P27	PCIE_VSS_28		L23
T21	PCIE_VSS_29		L24
T24	PCIE_VSS_30		L27
T27	PCIE_VSS_31		L28
T29	PCIE_VSS_32		M21
T28	PCIE_VSS_33		M24
U27	PCIE_VSS_34		M27
V22	PCIE_VSS_35		N27
V23	PCIE_VSS_36		N28
V24	PCIE_VSS_37		P22
V25	PCIE_VSS_38		P23
V26	PCIE_VSS_39		P24
V27	PCIE_VSS_40		P25
V28	PCIE_VSS_41		P26
V29	PCIE_VSS_42		

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.1		SOUTH BRIDGE(4/4)	PART NO. BA41-00720A
MODULE CODE	undef:ined	LAST EDIT	January 04, 2007 11:01:08 AM			PAGE 22 OF 47

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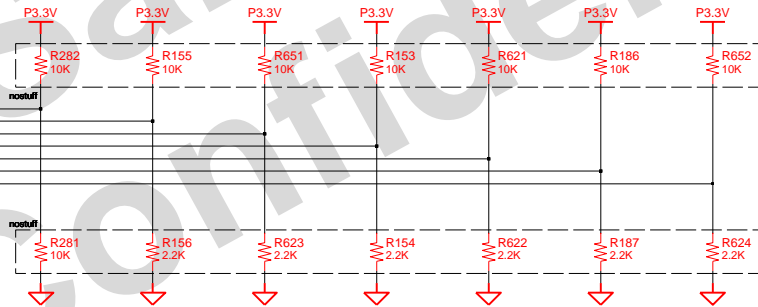
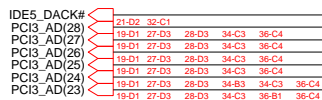
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**REQUIRED SYSTE STRAPS**



PULL HIGH	AC_SDOUT USE DEBUG STRAPS	RTC_CLK INTERNAL RTC DEFAULT	PCI_CLK4 USE INT. PLL48	PCI_CLK6 CPU IF = K8	PCI_CLK0 ROM TYPE: H,H = PCI ROM H,H = SPI ROM L,H = LPC ROM L,L = FWH ROM	PCI_CLK1 DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXT.RTC	USE EXT. 48MHz DEFAULT	CPU IF = P4		

**DEBUS STRAPS**



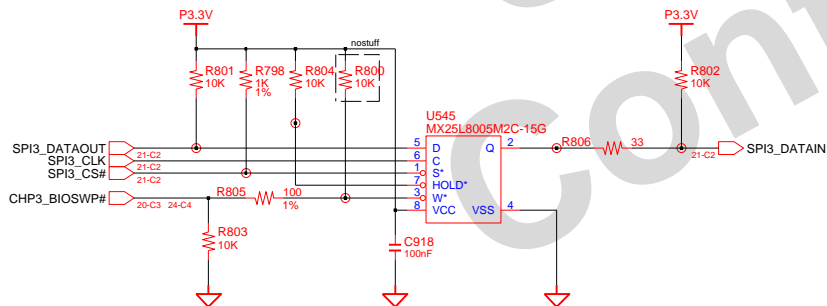
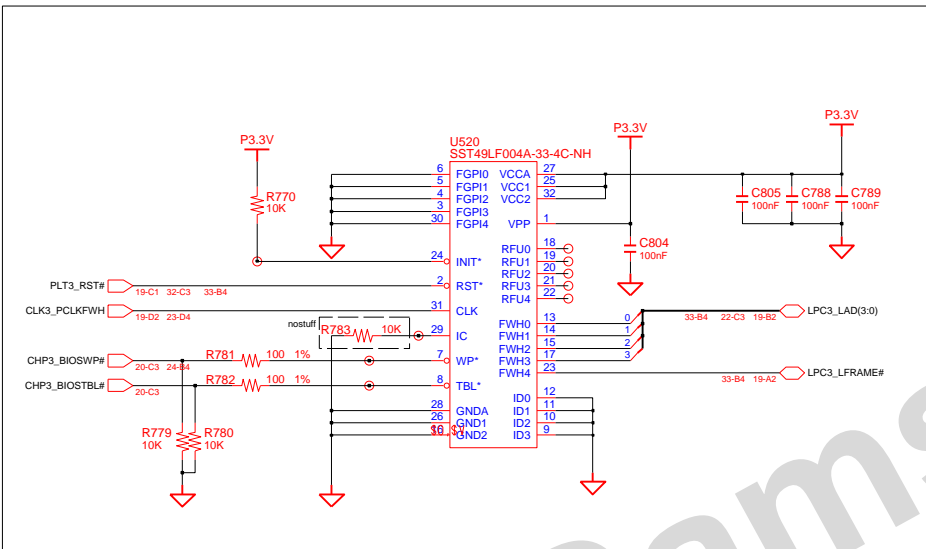
STRAP HIGH	IDE5_DACK* USE LONG RESET DEFAULT	PCI3_AD(28) USE LONG RESET DEFAULT	PCI3_AD(27) USE PCI PLL DEFAULT	PCI3_AD(26) USE ACPI BCLK DEFAULT	PCI3_AD(25) USE IDE PLL DEFAULT	PCI3_AD(24) USE DEFAULT PCIE STRAPS DEFAULT	PCI3_AD(23) BOOTFAIL TIMER DISABLED DEFAULT
STRAP LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN STRAPS OPTION	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE		

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nostuff



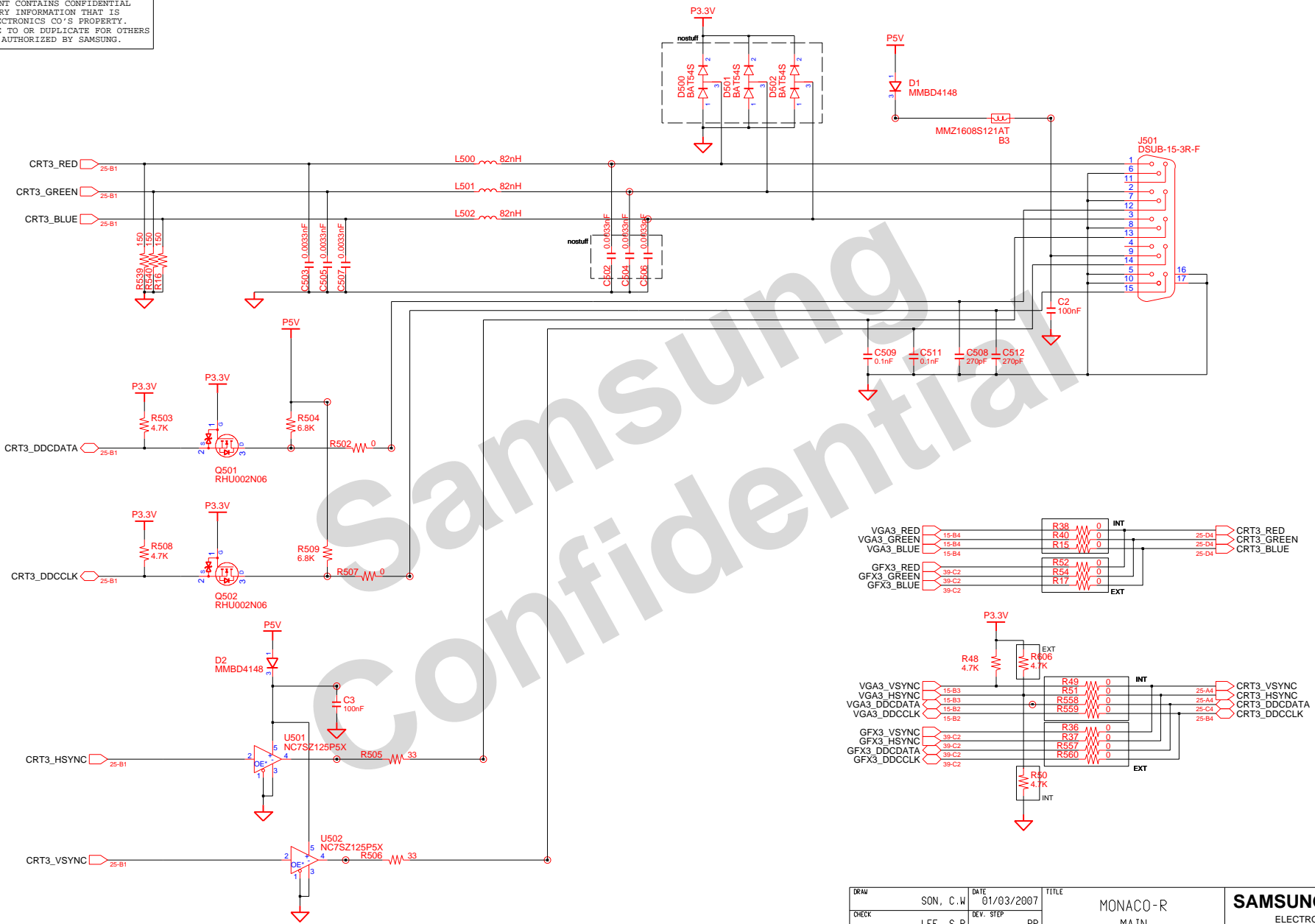
- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INITIALIZE SYSTEM H/W
- 08 INITIALIZE CHIPSET REGISTERS
- 09 SET IN POST FLAG
- 0A INIT CPU REGISTERS
- 0B CPU CACHE ON
- 0C INITIALIZE CACHE TO POST
- 0E INITIALIZE I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INITIALIZE POWER MANAGER
- 11 LOAD ALTERNATE REGISTERS
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INITIALIZE KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 INITIALIZE 8254 TIMER
- 1A INITIALIZE 8237 DMA CONTROLLER
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REGISTERS TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TEST CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REGISTERS
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INITIALIZE INTERRUPT VECTOR
- 44 INITIALIZE BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INITIALIZE I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INITIALIZE PCI BUS AND DEVICE
- 4A INITIALIZE ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY "PRESS ..... SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1
- 66 CONFIGURE ADVANCE CACHE REGISTERS
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD EERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT. RS232C
- 84 DETECT AND INSTALL EXT. PARALLEL
- 86 RE-INITIALIZE ON-BOARD I/O PORT
- 88 INITIALIZE BIOS DATA ROM
- 8A INITIALIZE EXTENDED BIOS DATA AREA
- 8C INITIALIZE FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INITIALIZE TYPOMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT O/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INITIALIZE HDD CONTROLLER
- 91 INITIALIZE LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.1		FWH	PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	24	OF 47



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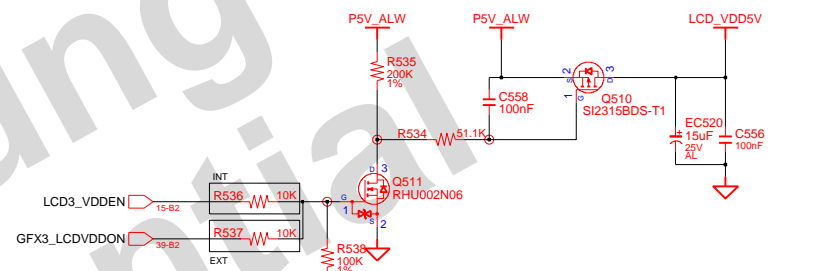
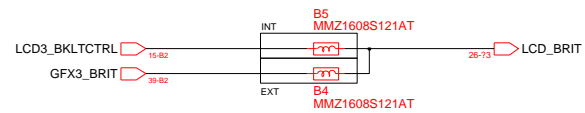
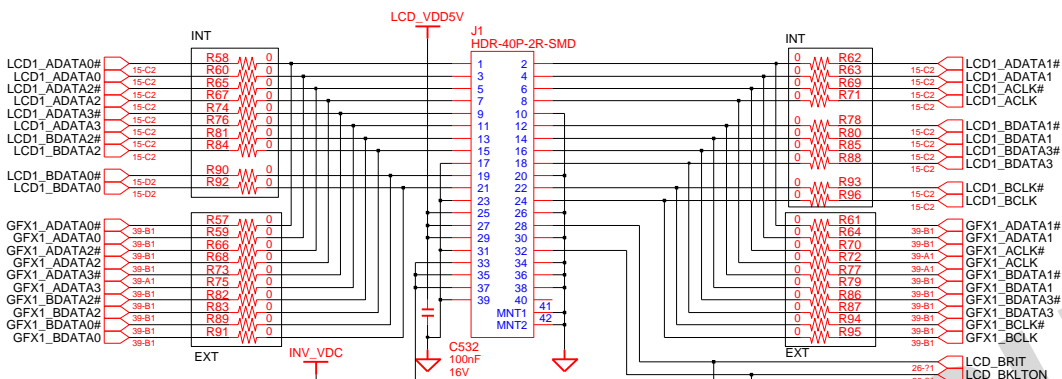


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN CRT PORT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	25 OF 47	

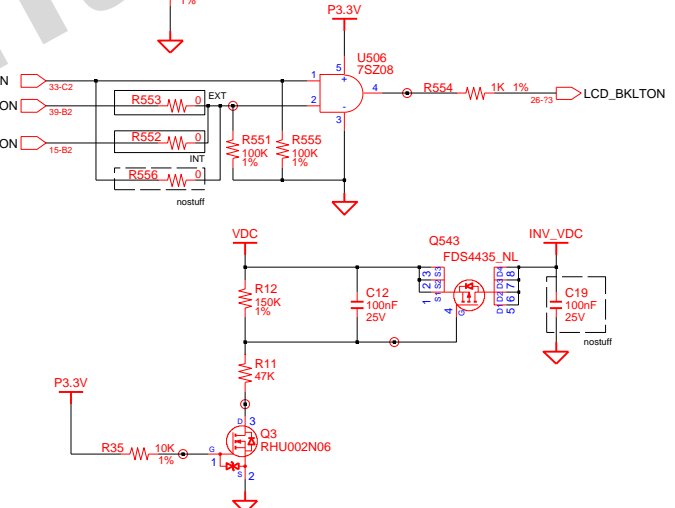
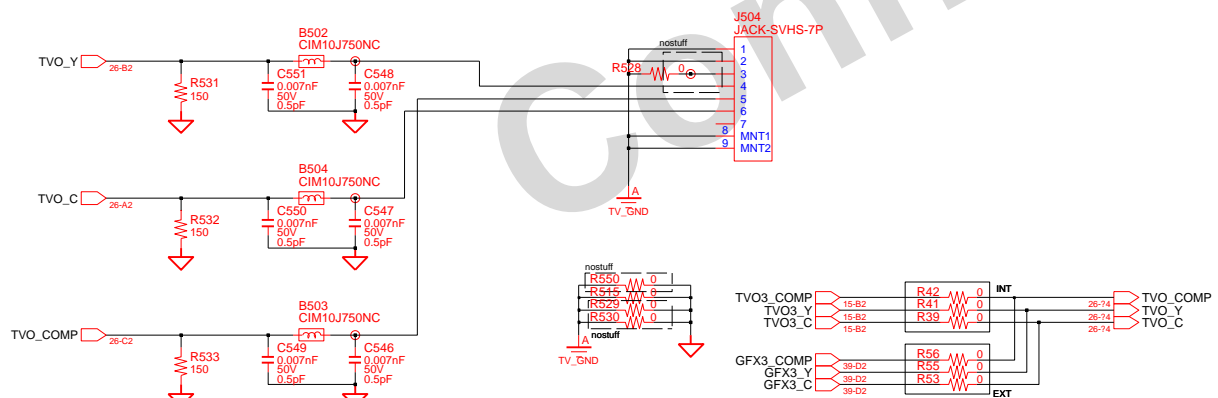
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**LCD CONNECTOR**



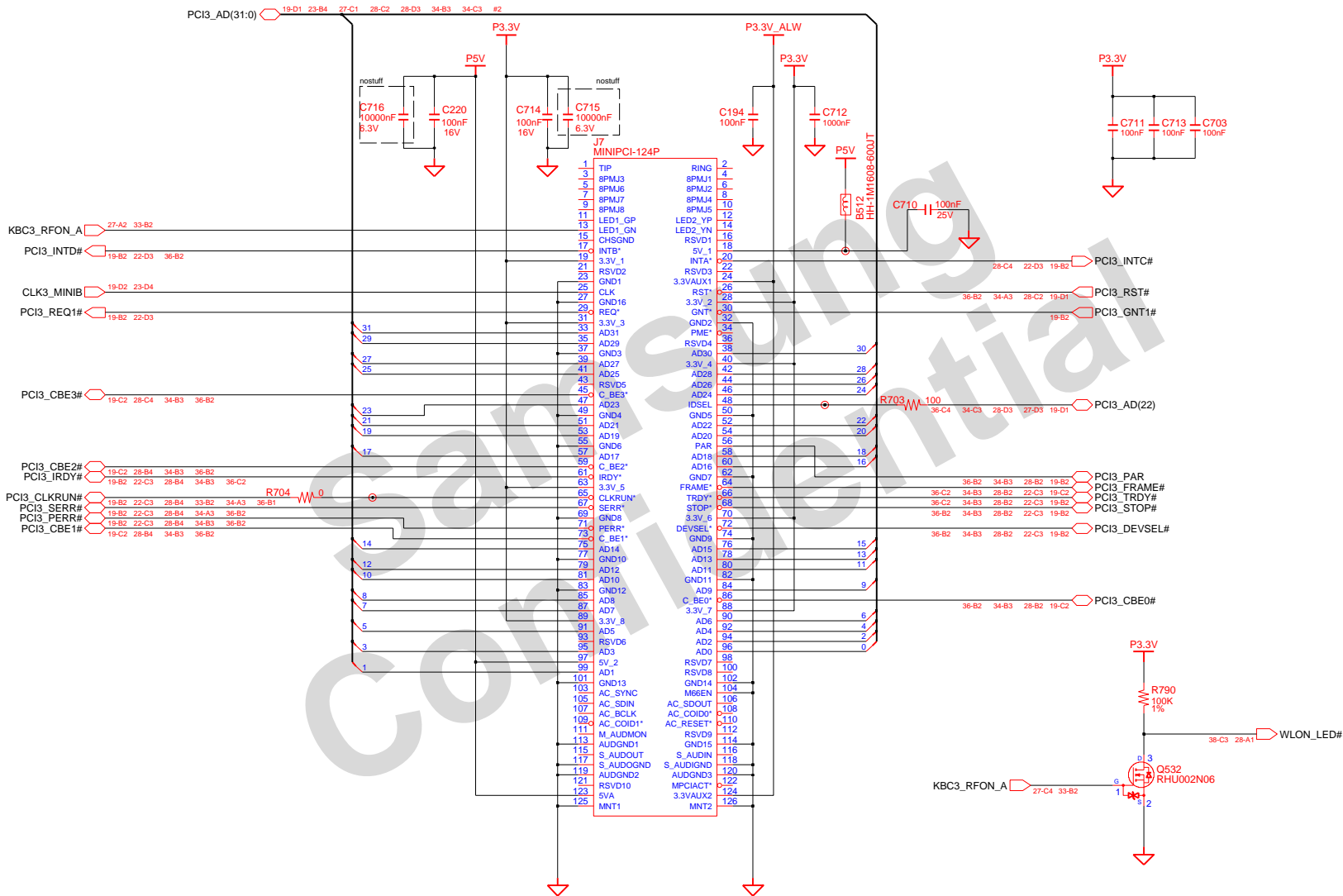
**TV-OUT**



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# FOR WIRELESS LAN

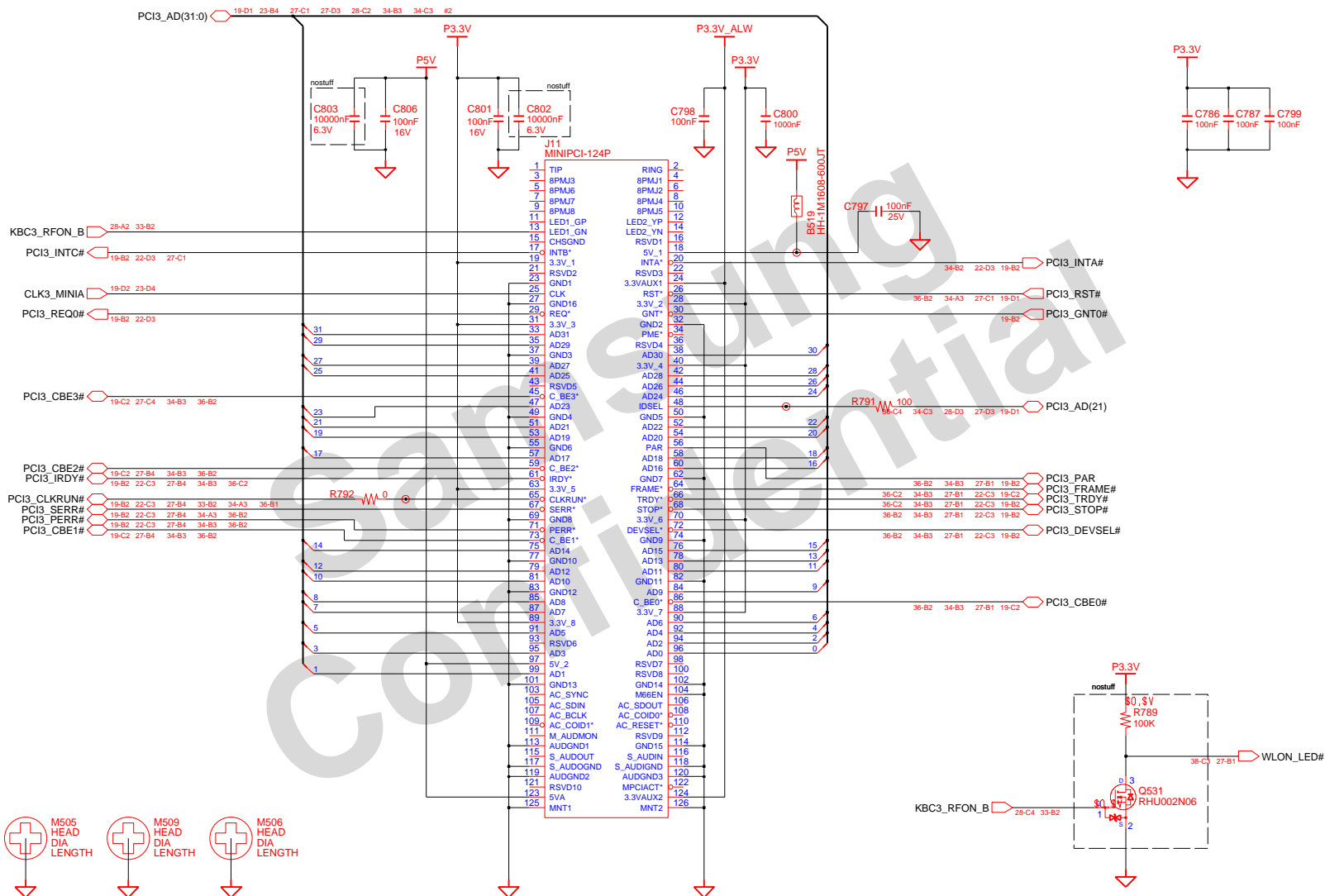


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN MINI PCI A	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	27	OF 47

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# FOR TV CARD(OPTION)

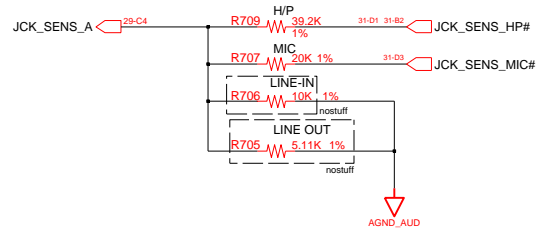
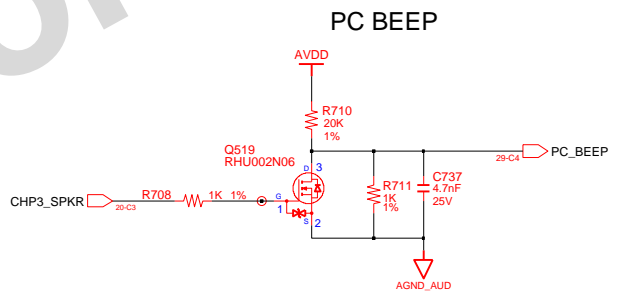
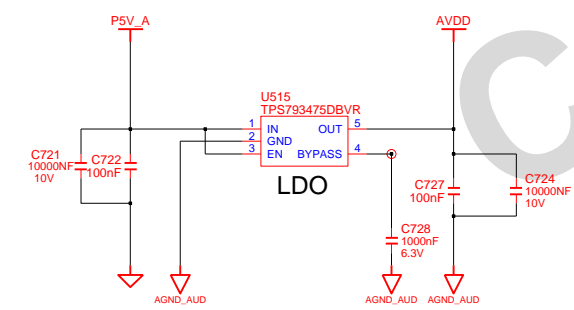
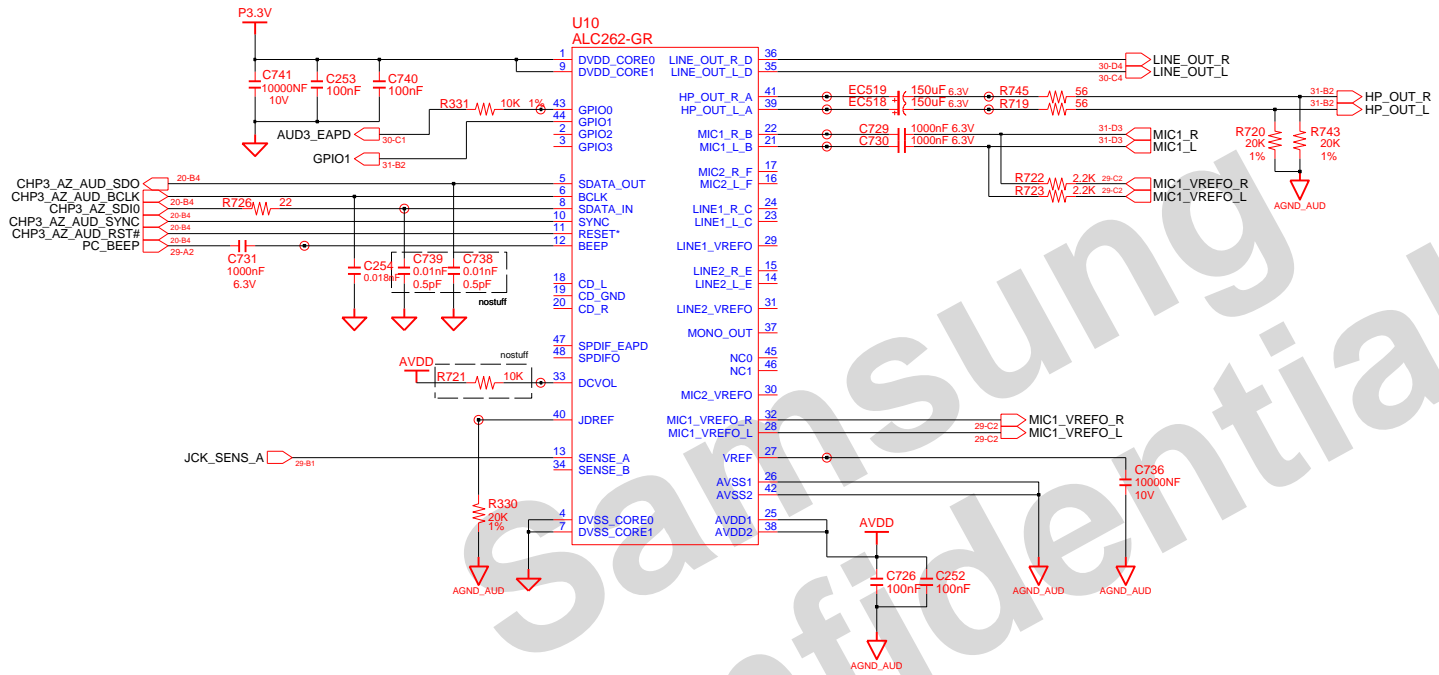
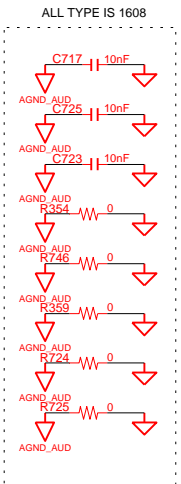


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN MINI PCI B	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	28	OF 47

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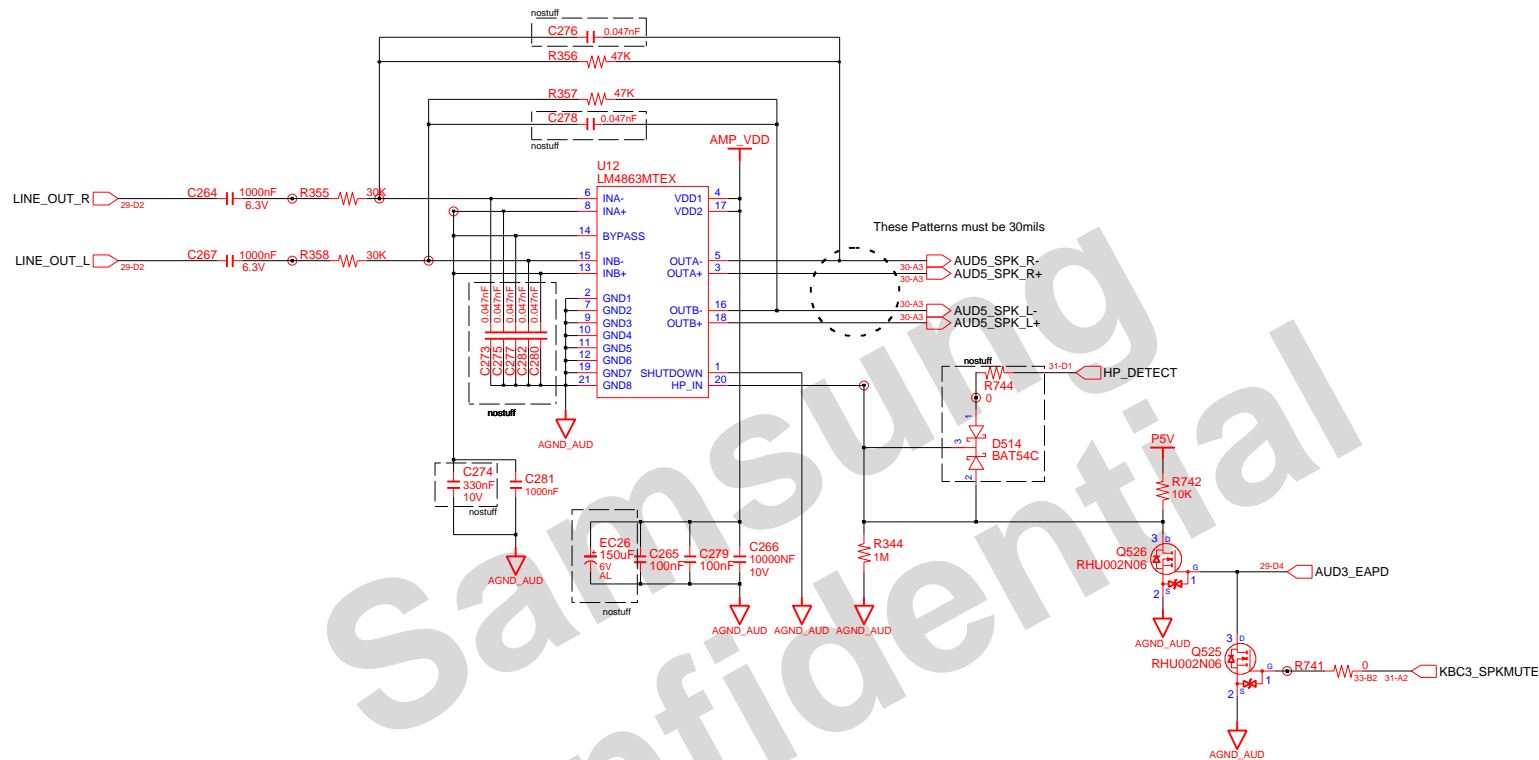
- 1. AGND\_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3. AGND\_MIC IS MIC GROUND
- 4. AGND\_CHS IS CHASSIS GROUND



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN AUDIO CODEC	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 29 OF 47		

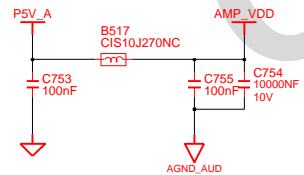
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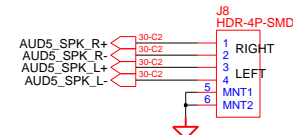


These Patterns must be 30mils

**AMP\_VDD**



**INTERNAL STEREO SPEAKERS**



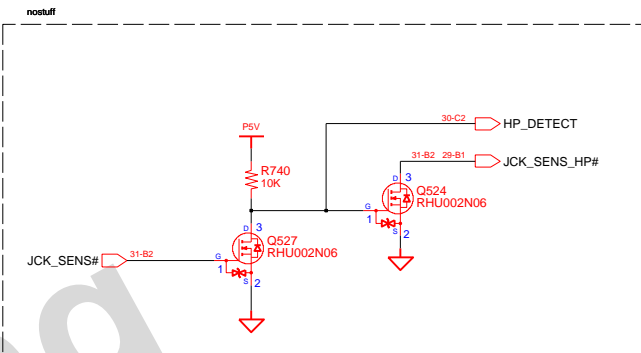
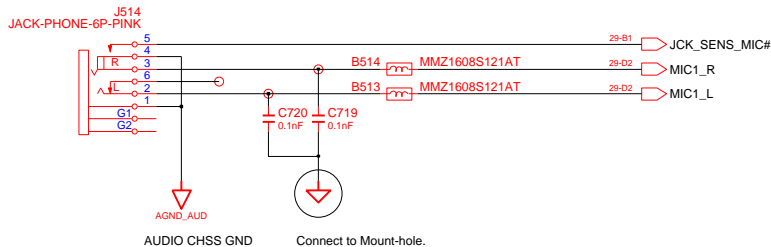
Should be written sign "L", "R" on the PCB

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN AUDIO AMP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	30 OF 47	

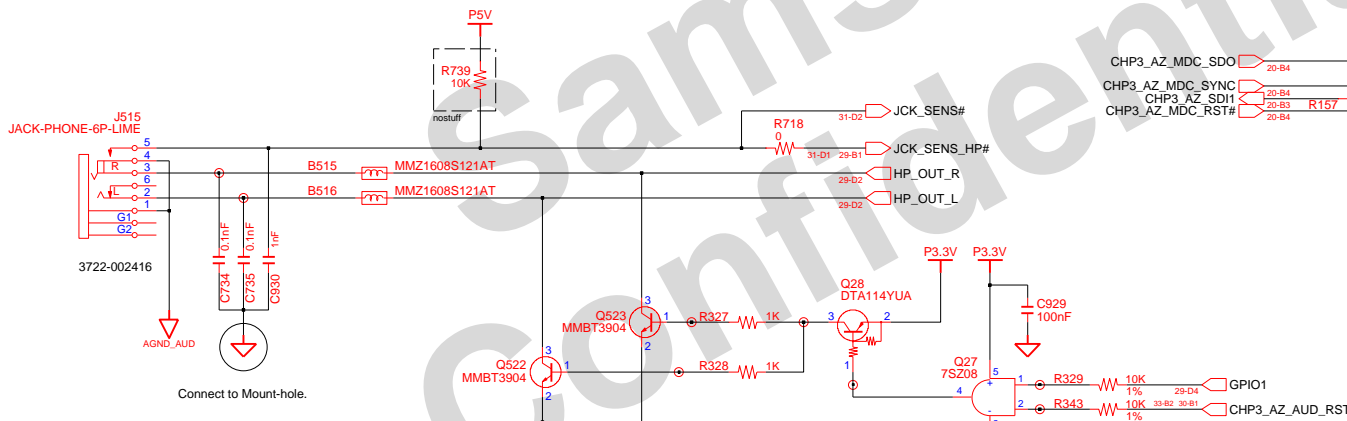
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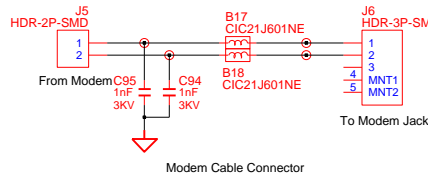
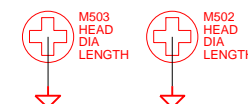
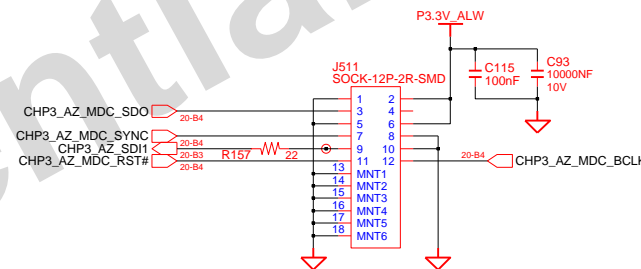
**MIC JACK**



**HEADPHONE**



**MDC Connector**



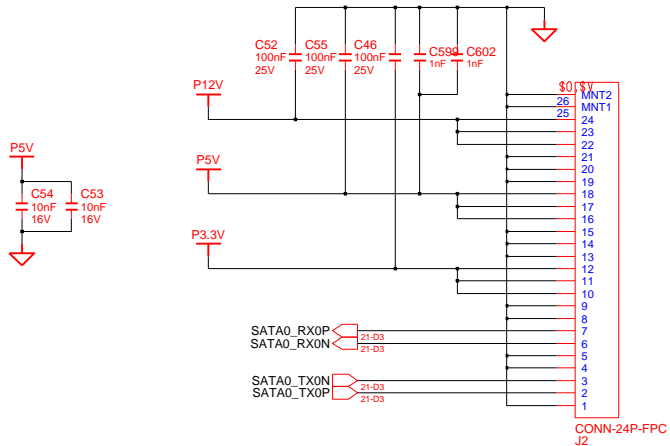
The traces led to Audio Jacks have the width over 10mil

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN AUDIO / MDC CONN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	31 OF 47	

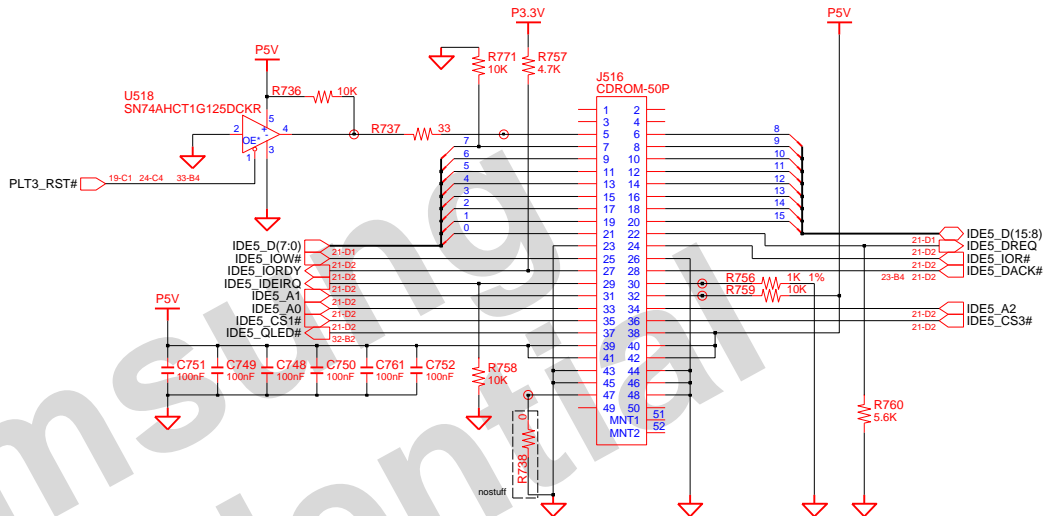
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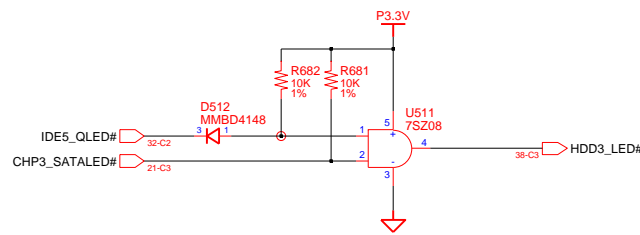
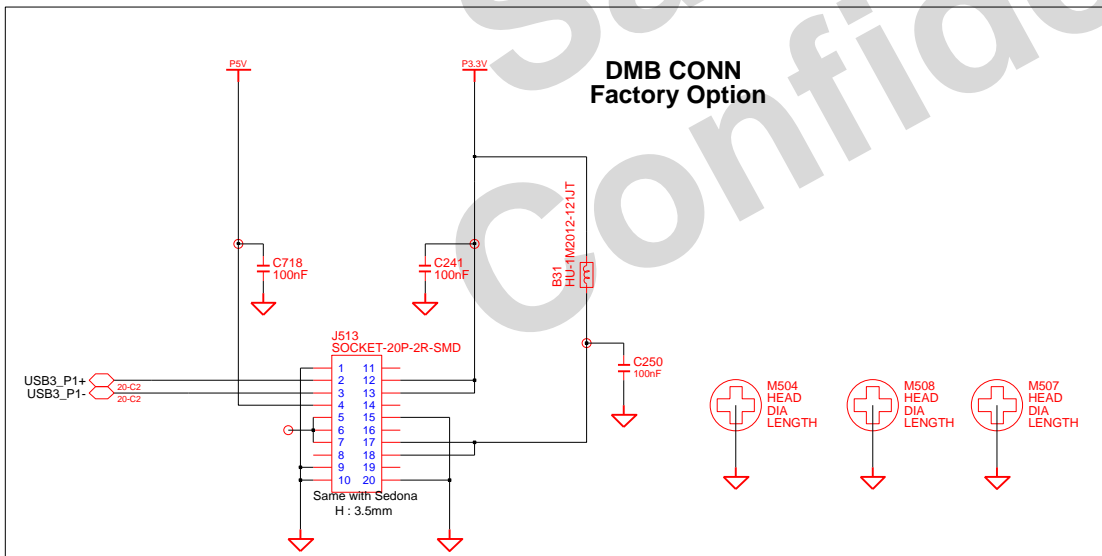
**HDD CONN**



**CD CONN**



**DMB CONN  
Factory Option**

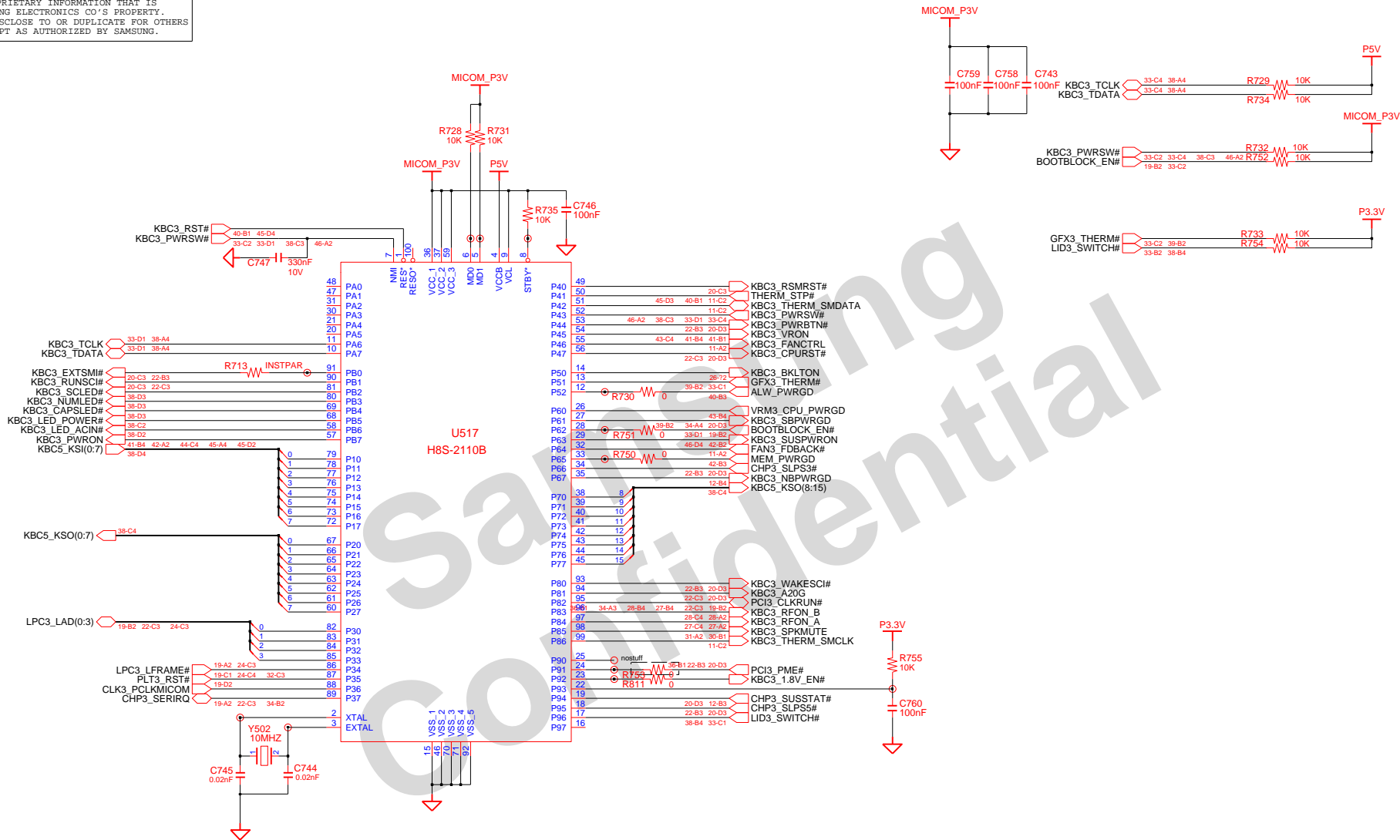


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN HDD/ODD/DMB	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			PART NO. BA41-00720A
MODULE CODE	undef:ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	32	OF 47



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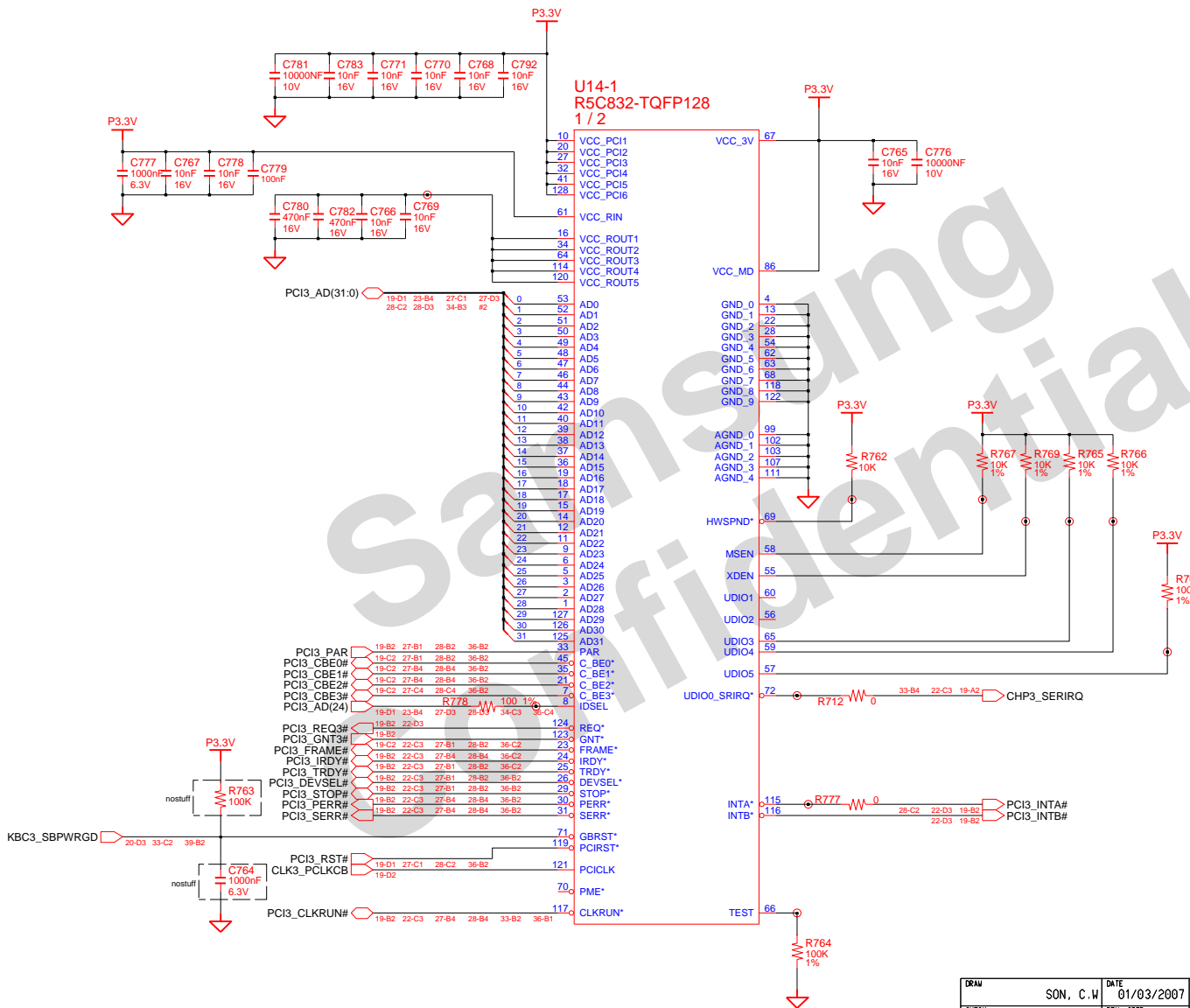
**MICOM Crisis Update**  
 Condition: P90=P91=P92=High(MICOM\_P3V)  
 MD0=MD1=Low(0V)  
 Serial Port: P84 & P85

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.1		MICOM	
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	33 OF 47	

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**OPTION**



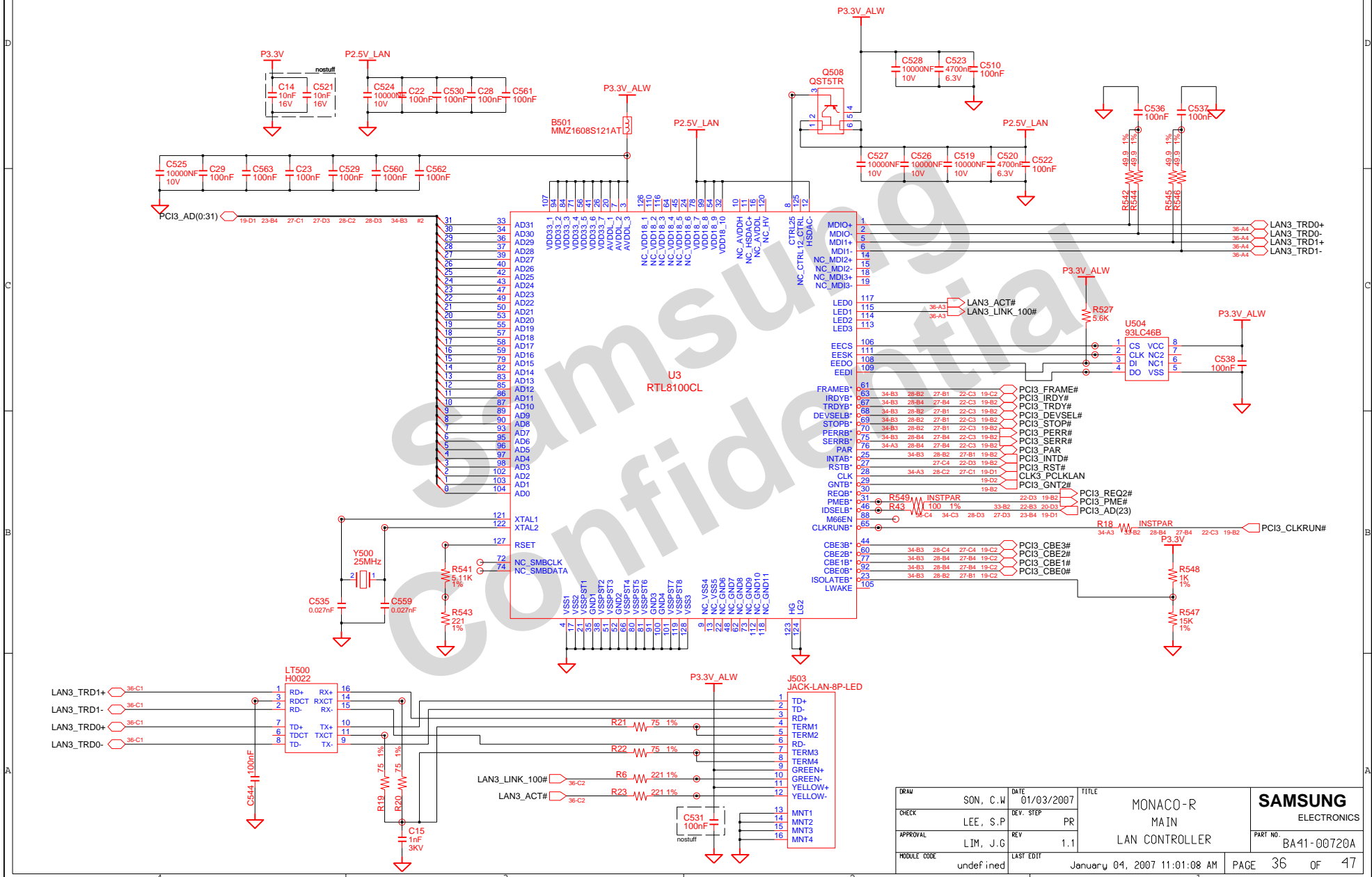
DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	5-IN-1 CONTROLLER(1/2)	PART NO.	
APPROVAL	LIM, J.G	REV	1.1	January 04, 2007 11:01:08 AM	BA41-00720A	PAGE 34 OF 47
MODULE CODE	undef:ined	LAST EDIT				



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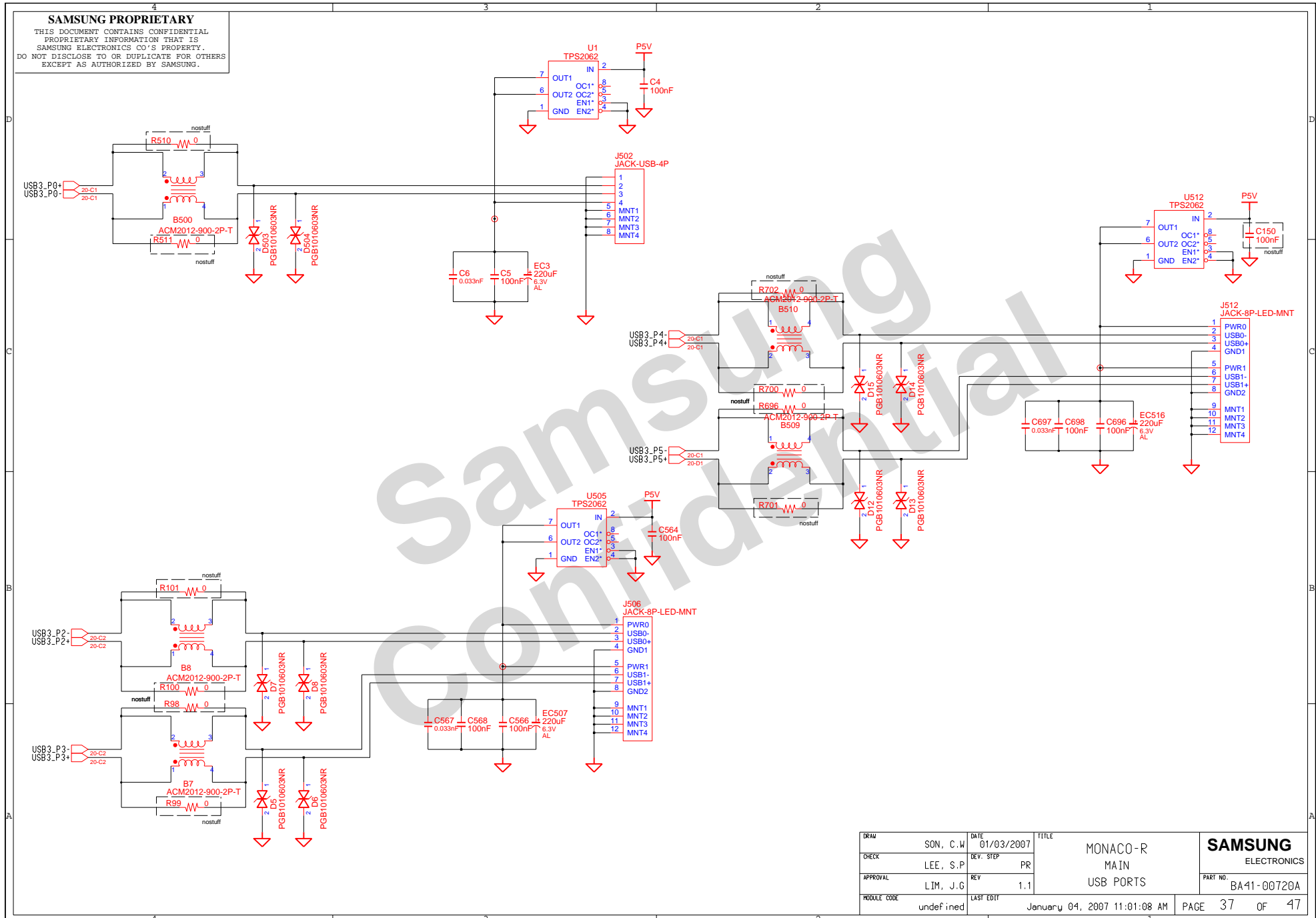
# LAN Controller (Only 10/100M)



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN LAN CONTROLLER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR	REV	1.1	
APPROVAL	LIM, J.G	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	36	OF 47
MODULE CODE	undefined					

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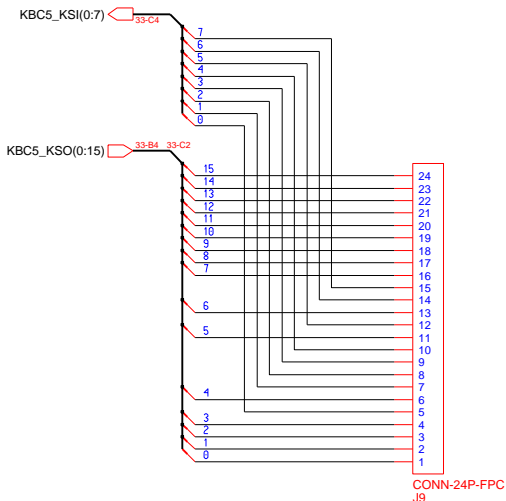


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN USB PORTS	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 37 OF 47		

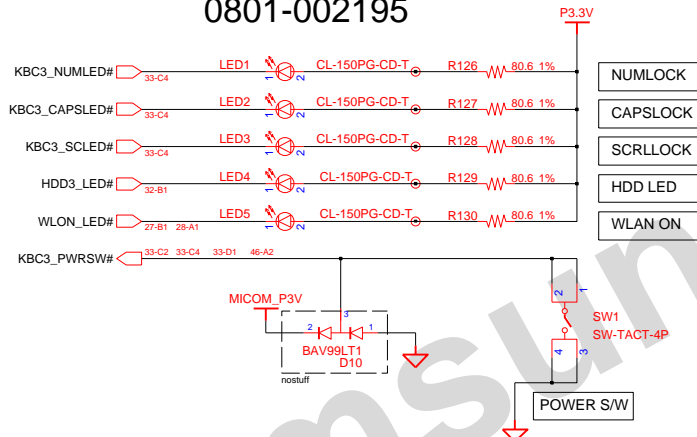
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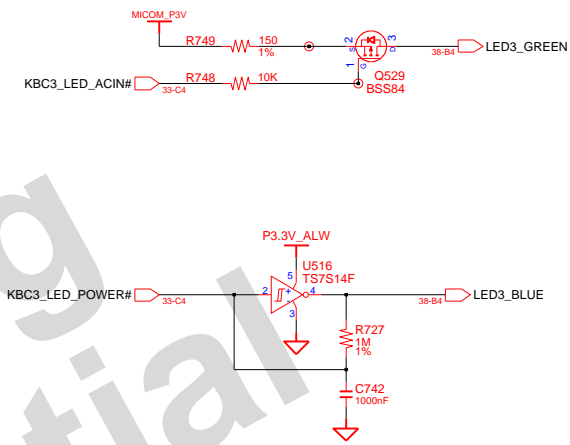
**KEYBOARD**



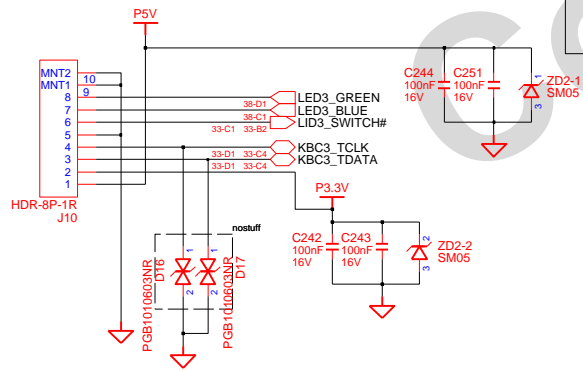
**LED  
0801-002195**



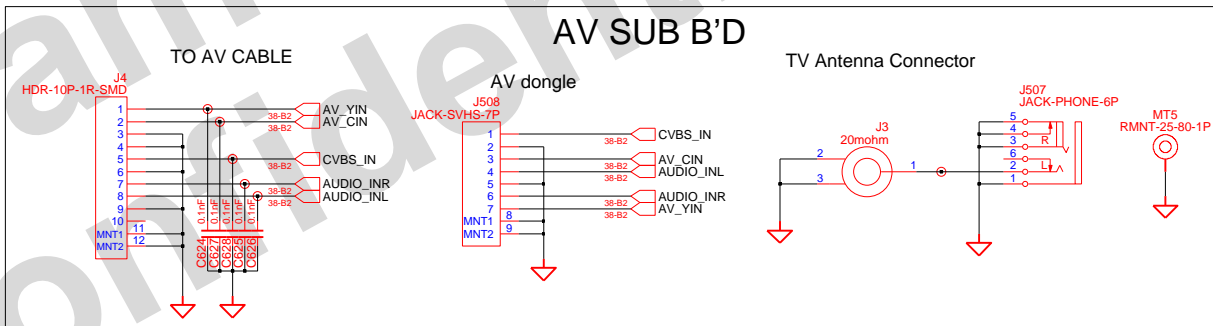
**ADAPTERIN/CHARGING LED**



**TOUCH PAD**



**AV SUB B'D**

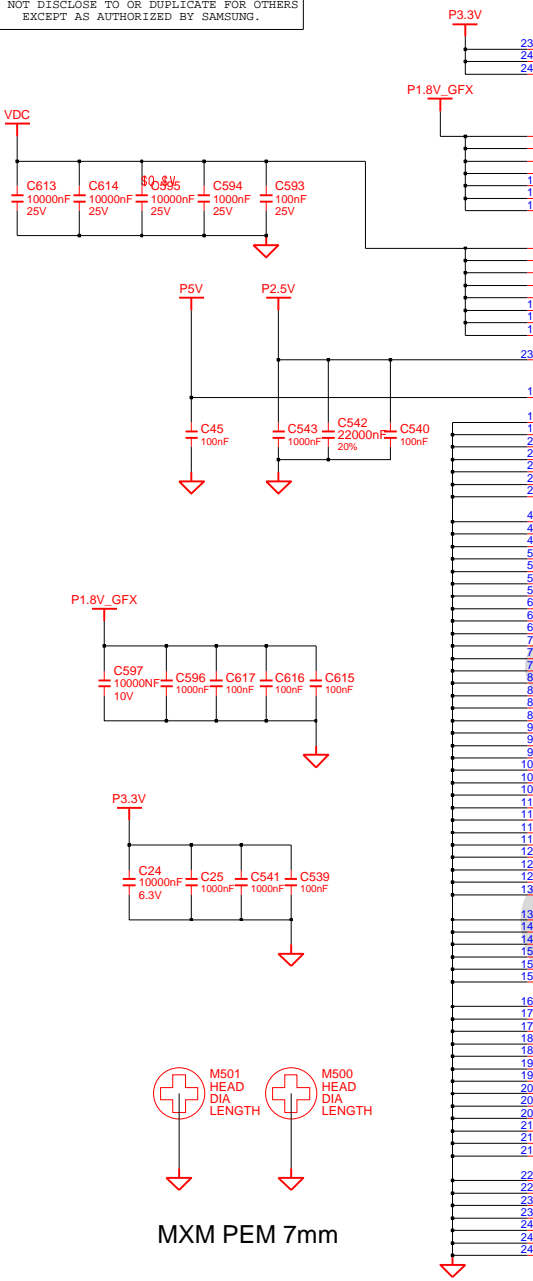


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	MAIN		
APPROVAL	LIM, J.G	REV	1.1	KBD/TPAD/LED/SW		PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	38	OF 47

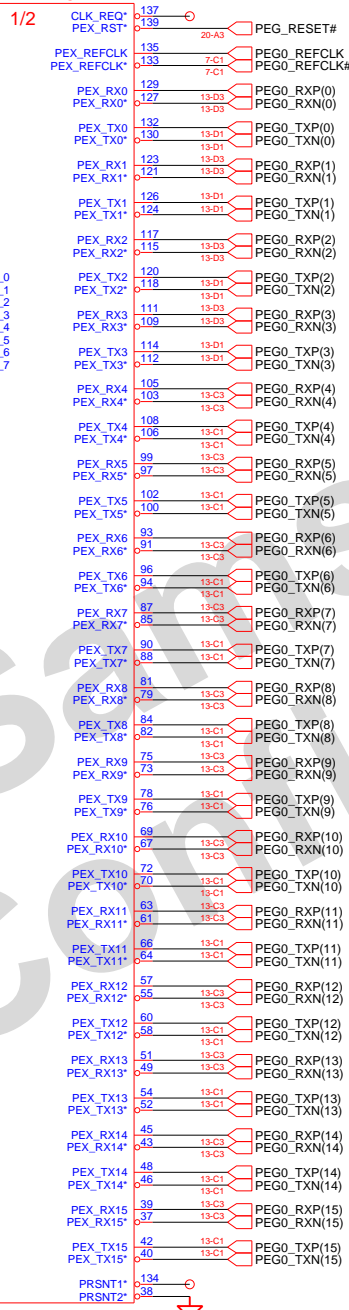
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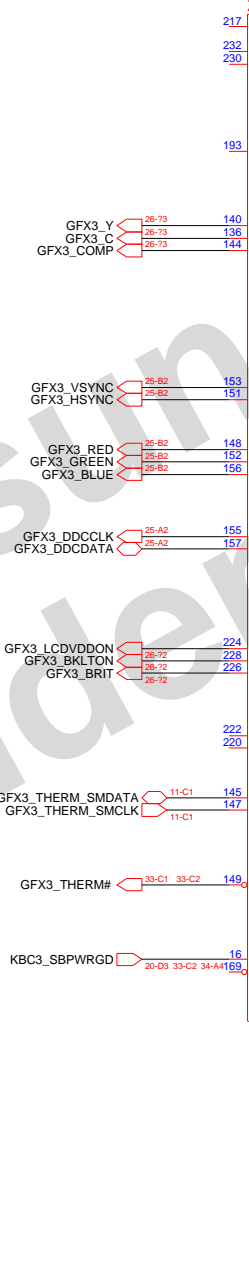
**J505-1 SOCKET-242P-2R-SMD**



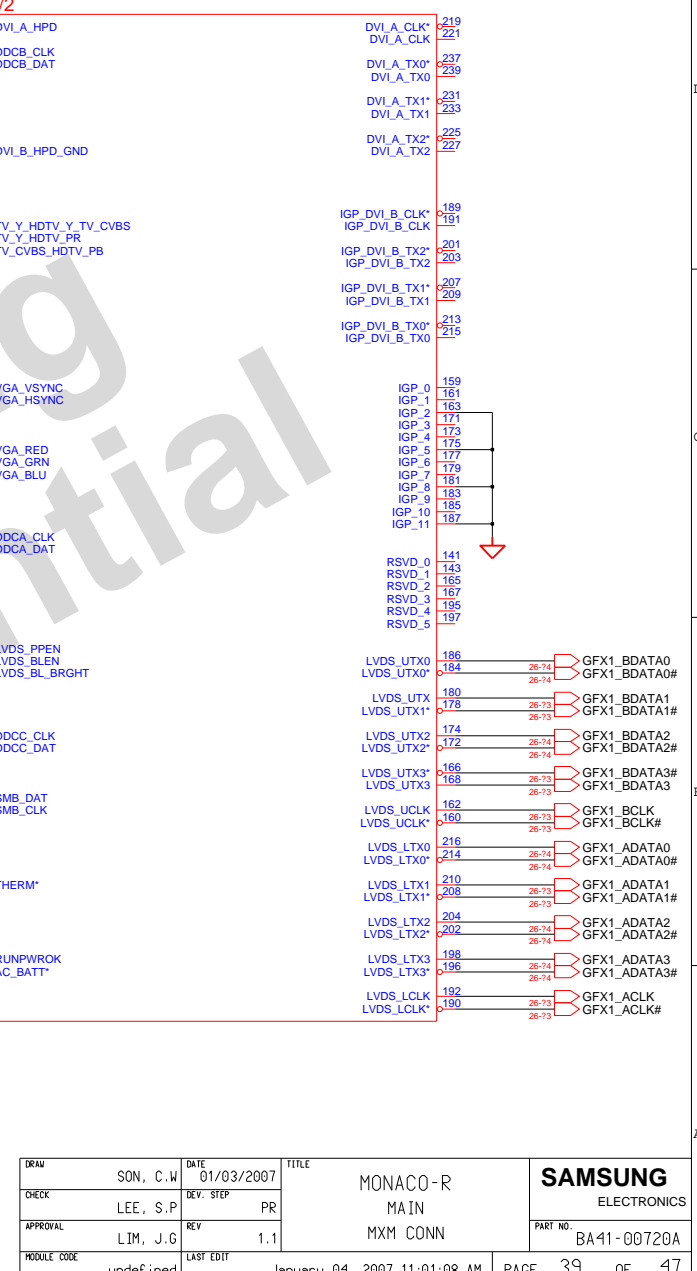
MXM PEM 7mm



**J505-2 SOCKET-242P-2R-SMD 2/2**



**EXT GFX ONLY**

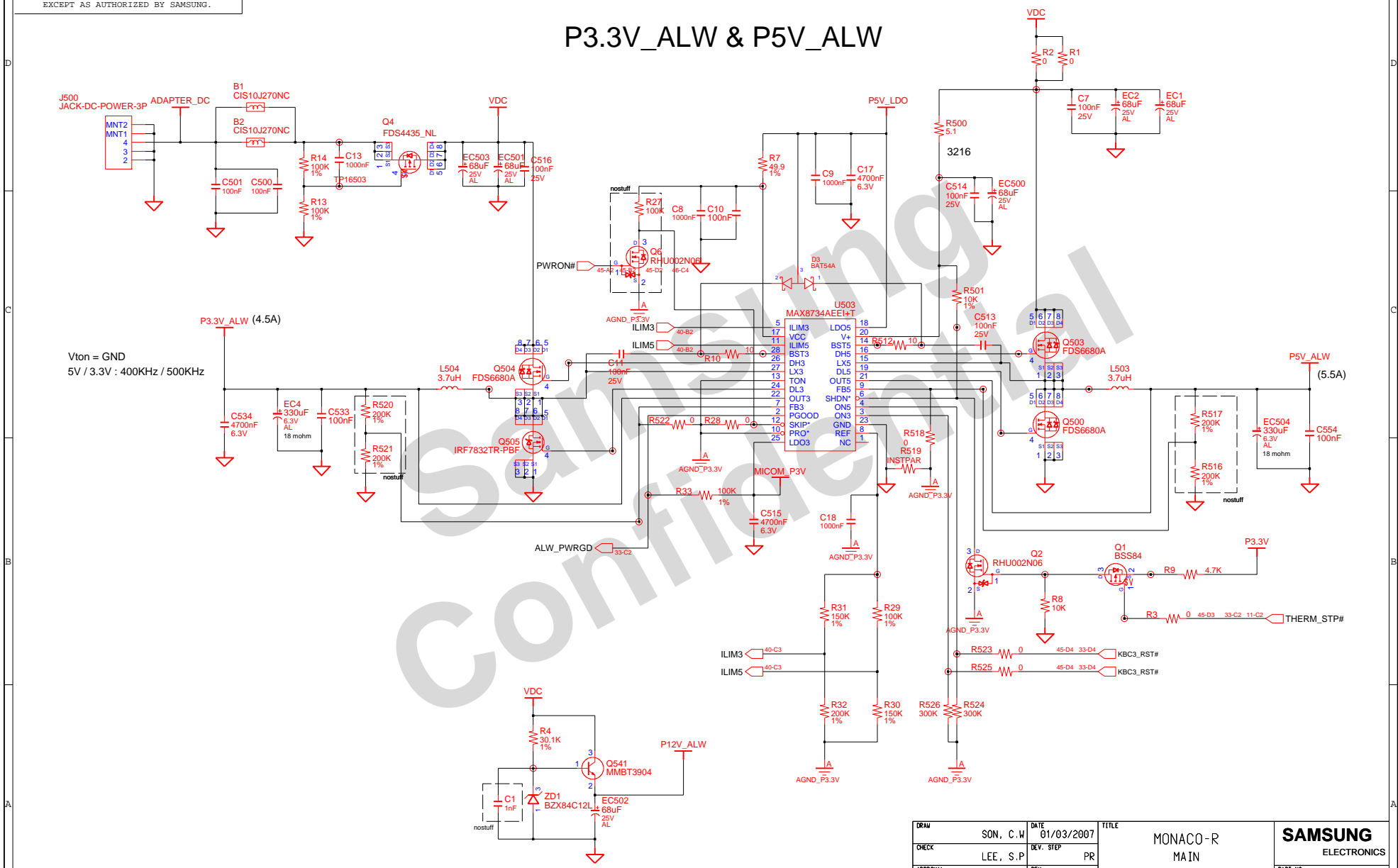


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A	
CHECK	LEE, S.P	DEV. STEP	PR	MAIN			
APPROVAL	LIM, J.G	REV	1.1	MXM CONN			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM				
						PAGE	39 OF 47

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# P3.3V\_ALW & P5V\_ALW



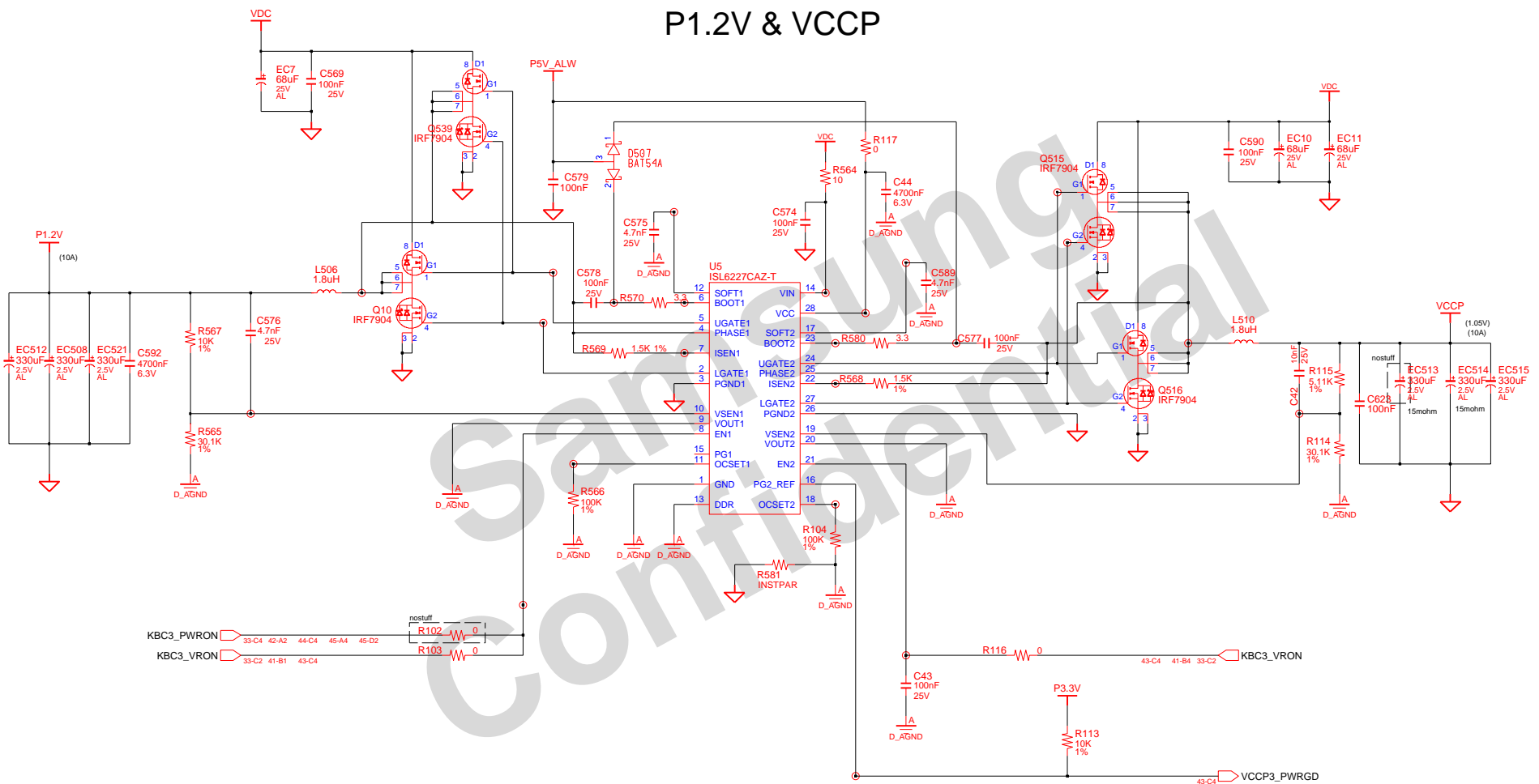
DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR		MAIN	
APPROVAL	LIM, J.G	REV	1.1		3.3V_ALW/5V_ALW POWER	PART NO. BA41-00720A
MODULE CODE	undef:ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	40	OF 47



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# P1.2V & VCCP

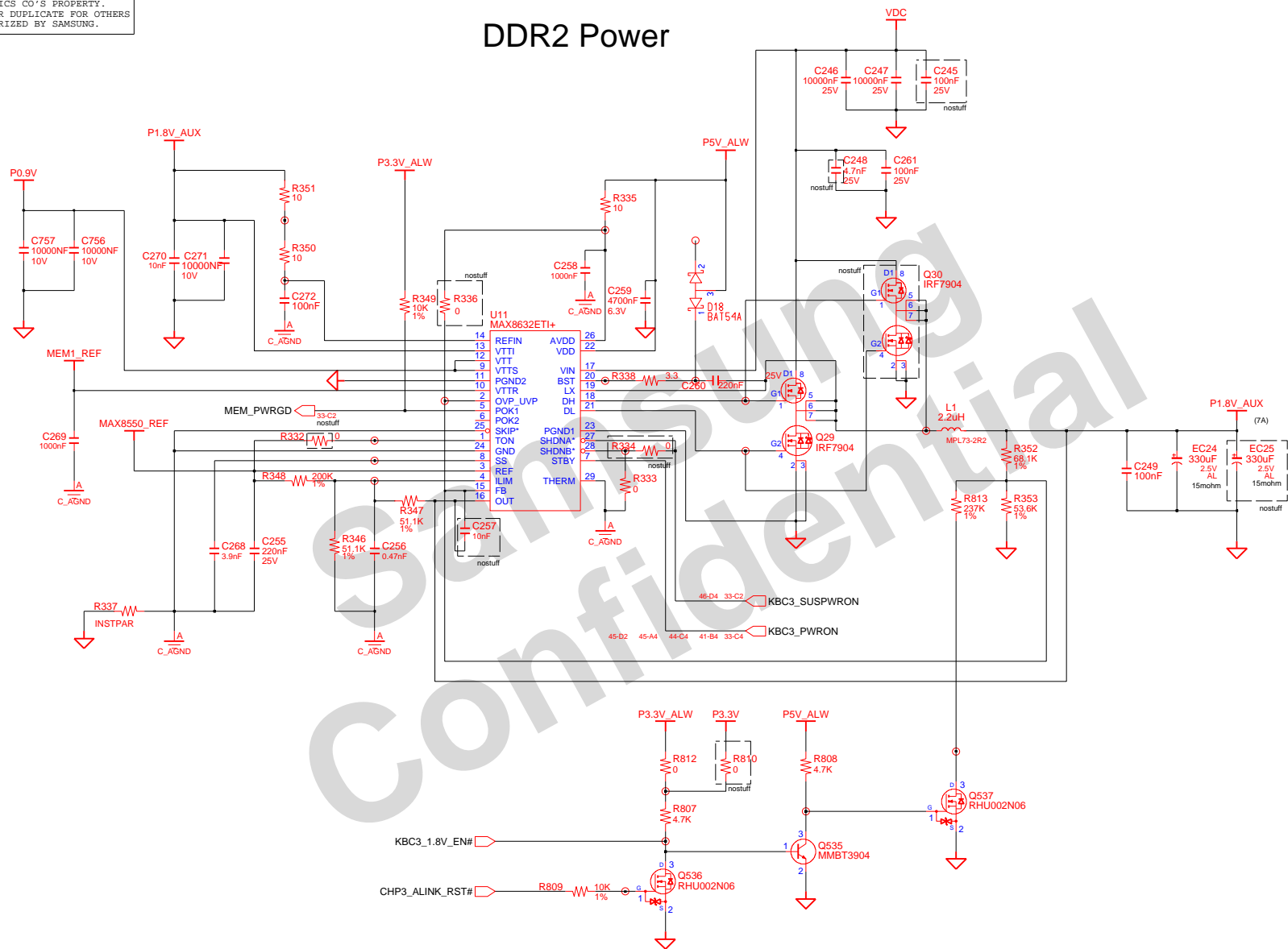


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN	SAMSUNG ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	1.2V/VCCP POWER		
APPROVAL	LIM, J.G	REV	1.1			PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	41	OF 47

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# DDR2 Power

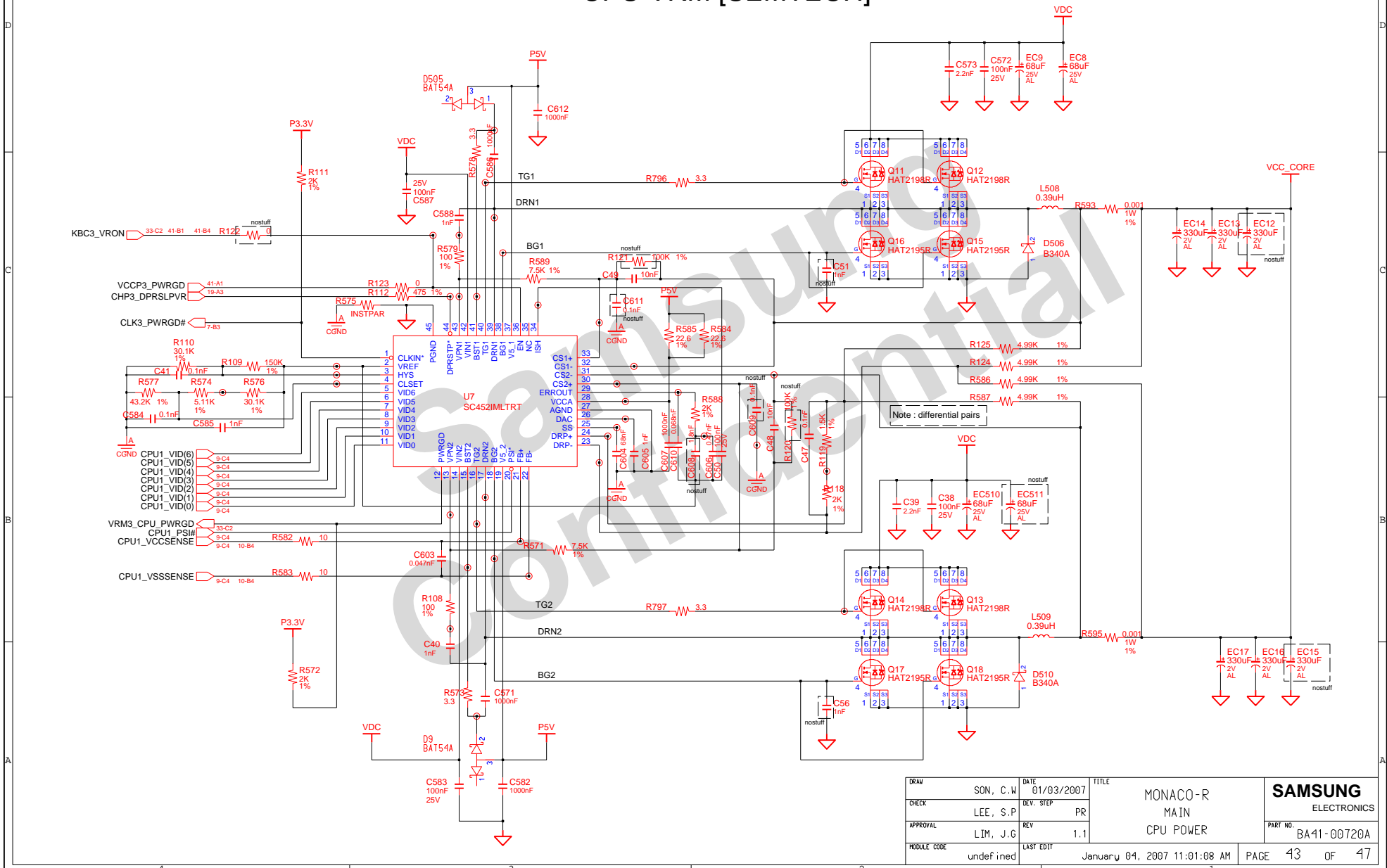


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN DDR2 POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 42 OF 47		

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# CPU VRM [SEMTECH]



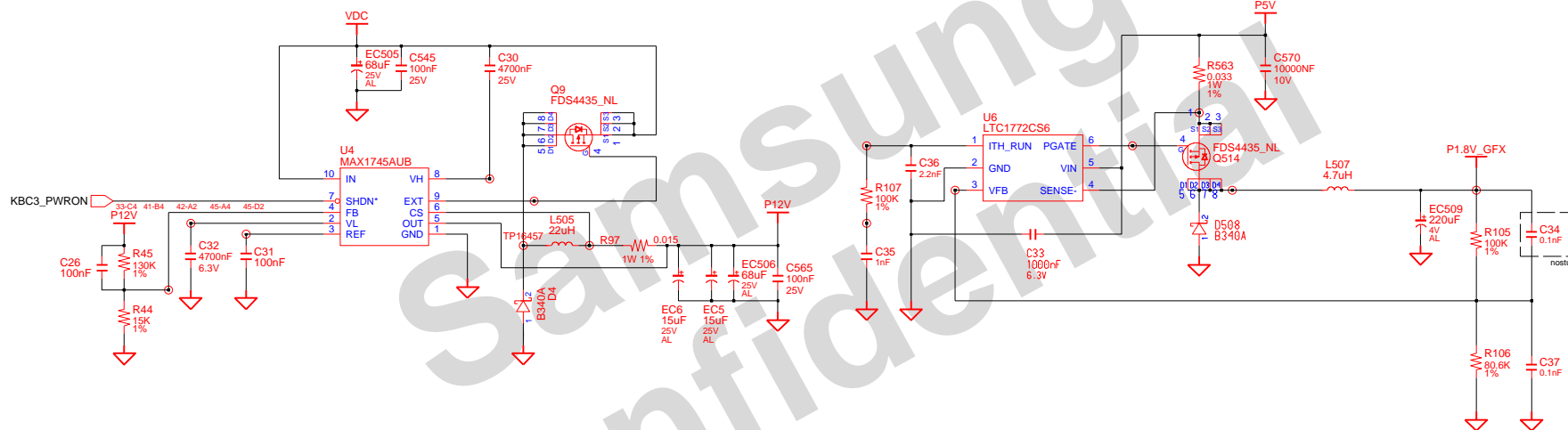
DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN CPU POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	43 OF 47	

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**P12V POWER**

**P1.8V POWER FOR MXM CARD**

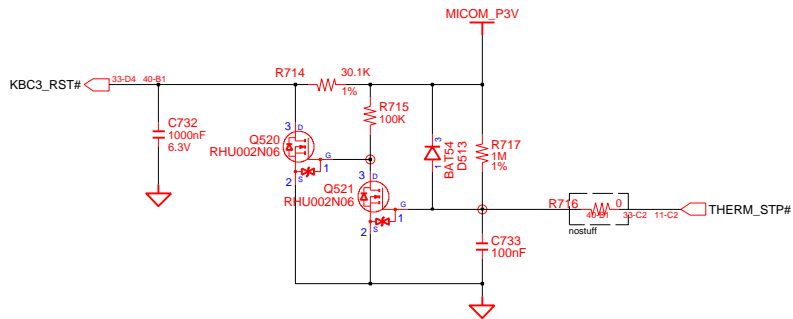


DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1		P12V / MXM 1.8V POWER	PART NO. BA41-00720A
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE	44	OF 47

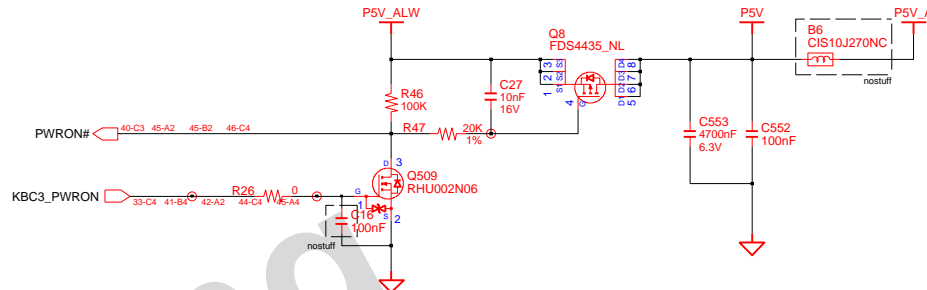
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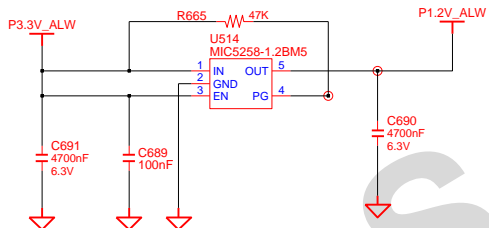
**MICOM RESET**



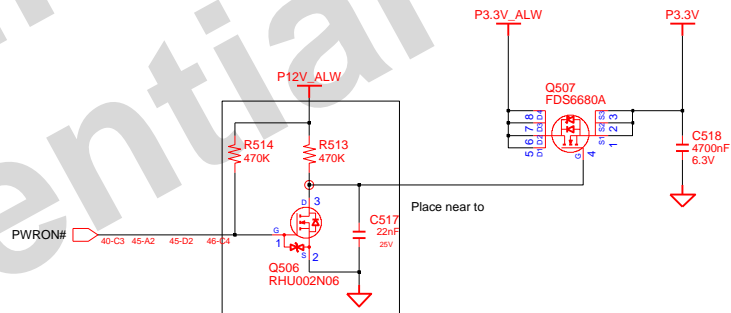
**Switched Power On (P5V)**



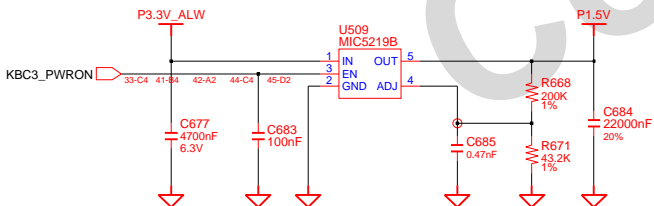
**P1.2V\_ALW**



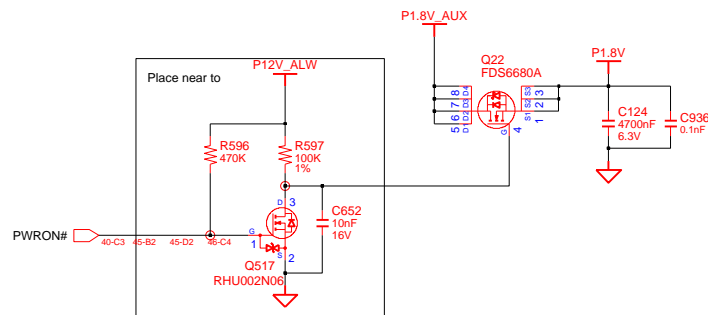
**Switched Power On (P3.3V)**



**P1.5V POWER**



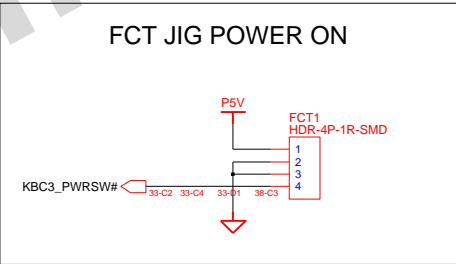
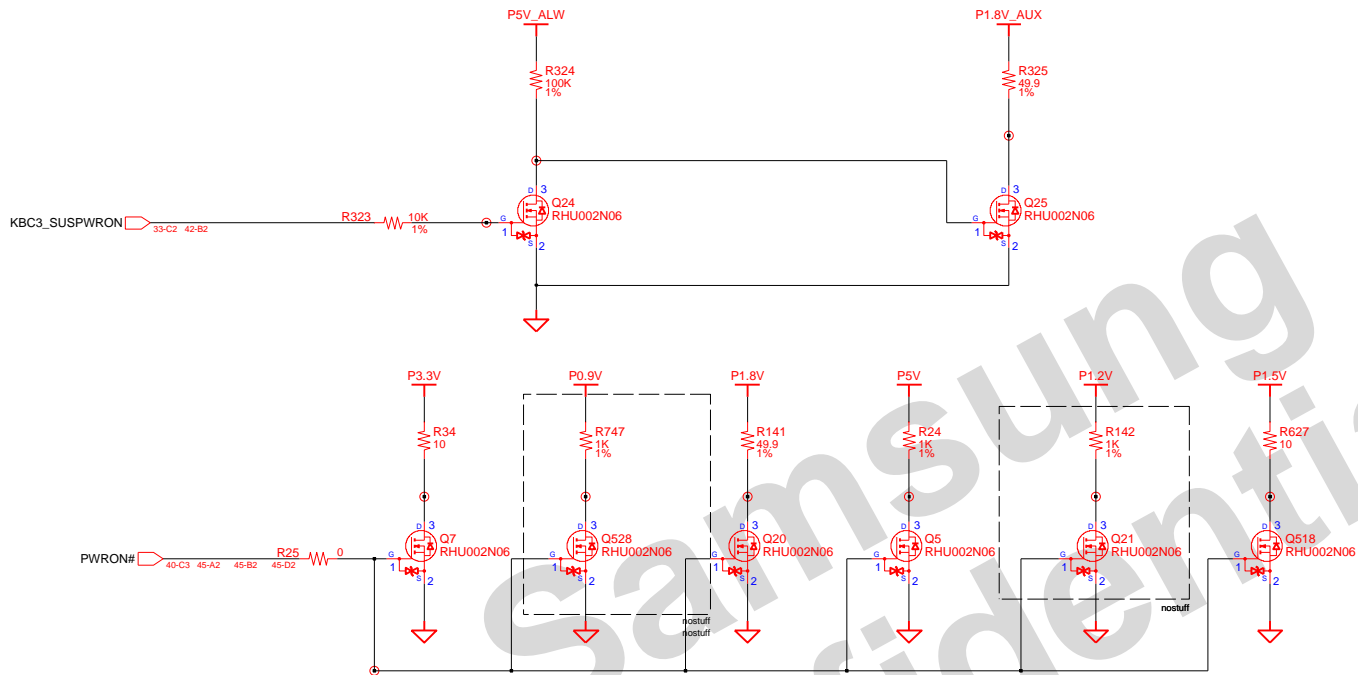
**Switched Power On (P1.8V)**



DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN SWITCHED POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-00720A
CHECK	LEE, S.P	DEV. STEP	PR			
APPROVAL	LIM, J.G	REV	1.1			
MODULE CODE	undef ined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 45 OF 47		

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- C795 || 0.0033nF
- C286 || 0.0033nF
- C784 || 0.015nF
- C287 || 0.015nF
- C796 || 0.033nF
- C292 || 0.033nF
- C785 || 0.047nF
- C294 || 0.047nF
- C794 || 0.1nF
- C293 || 0.1nF
- C793 || 0.01nF
- C295 || 0.01nF

These are for ICT using.

- MT6 RMNT-30-76-1P
- MT4 RMNT-30-76-1P
- MT500 RMNT-30-76-1P
- MT7 RMNT-30-76-1P
- MT13 RMNT-25-80-1P
- MT10 RMNT-25-80-1P
- MT2 RMNT-30-76-1P
- MT3 RMNT-30-76-1P
- MT1 RMNT-30-76-1P

DRAW	SON, C.W	DATE	01/03/2007	TITLE	MONACO-R MAIN POWER STRAPS	<b>SAMSUNG</b> ELECTRONICS
CHECK	LEE, S.P	DEV. STEP	PR	PART NO.		
APPROVAL	LIM, J.G	REV	1.1	BA41-00720A		
MODULE CODE	undefined	LAST EDIT	January 04, 2007 11:01:08 AM	PAGE 46 OF 47		

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 TP16747OCFX3\_RED  
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