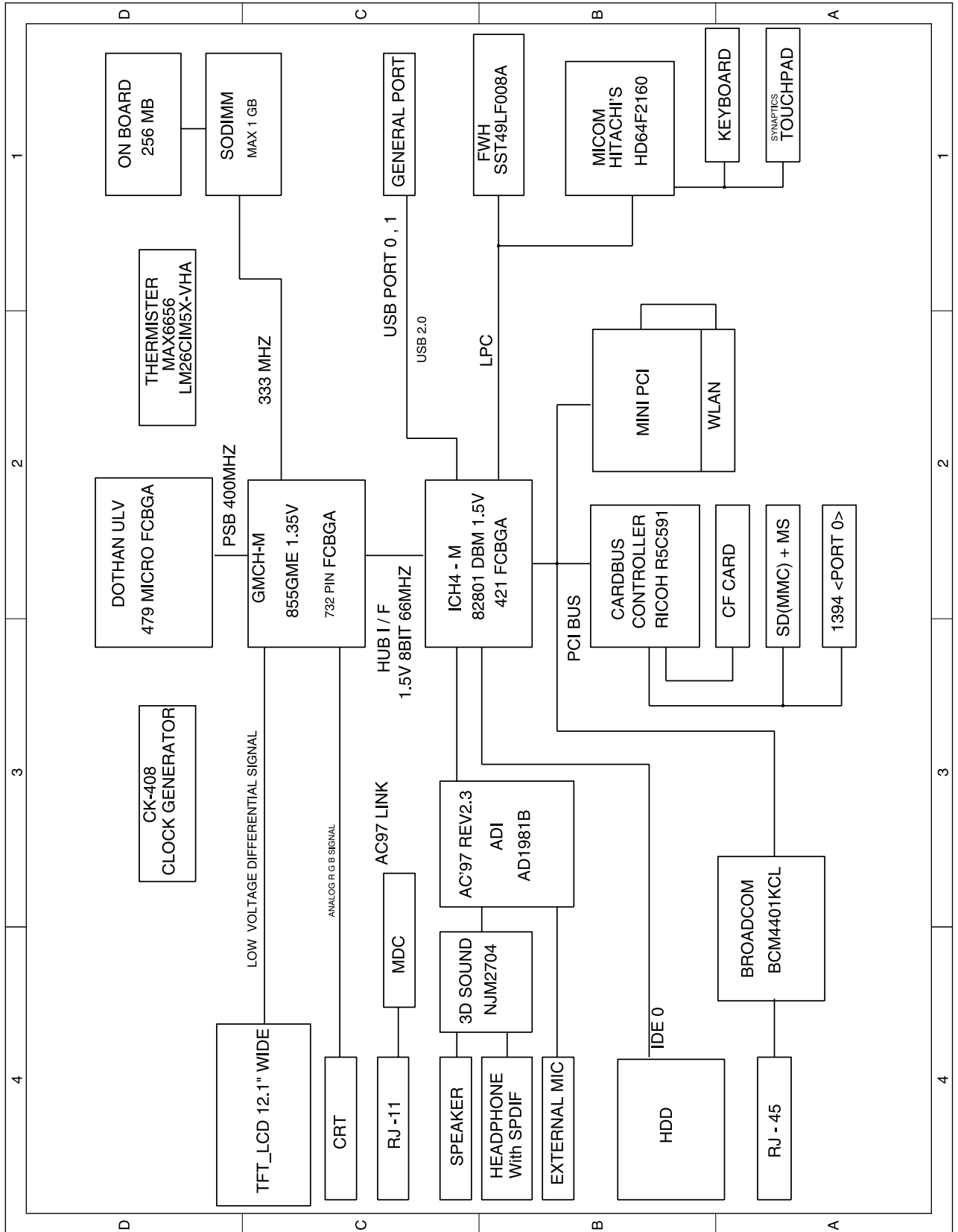


3 System Schematic Diagram

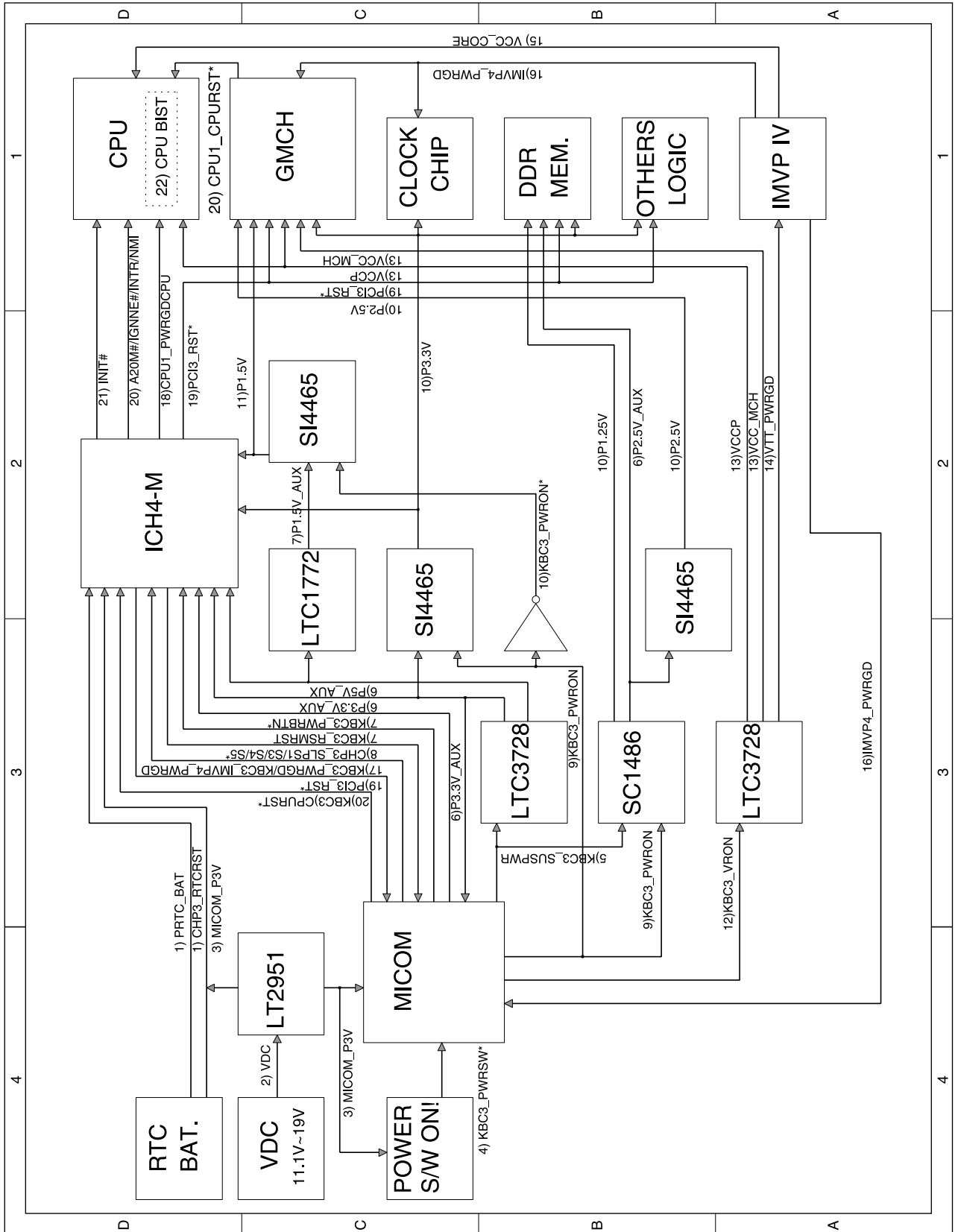
3-1 System Main Board Schematic Diagram

4	3	2	1	D	C	B	A									
<h1>NEON</h1>				Table of Contents												
<p>CPU : Dothan ULV Chip Set : 855GME Remarks :</p>				<ol style="list-style-type: none"> 1. COVER --(SHEET1) 2. BLOCK DIAGRAM --(SHEET2) 3. POWER SEQUENCE --(SHEET3) 4. CLOCK DISTRIBUTION --(SHEET4) 5. BOARD INFORMATION --(SHEET5) 6. CLOCK GENERATOR --(SHEET6) 7. DOTHAN CPU --(SHEET7,8) 8. THERMAL SENSOR & FAN --(SHEET9) 9. MONTARA-GM+ --(SHEET10,11,12,13) 10. DDR ON BOARD --(SHEET14) 11. DDR SODIMM --(SHEET15) 12. DDR TERMINATION --(SHEET16,17) 13. ICH4-M --(SHEET18,19,20) 14. FWH --(SHEET21) 15. CRT CONNECTOR --(SHEET22) 16. LCD CONNECTOR --(SHEET23) 17. HDD CONNECTOR --(SHEET24) 18. MICOM --(SHEET25) 19. BROADCOM LAN --(SHEET26) 20. USB & MDC --(SHEET27) 21. MINIPCI --(SHEET28) 22. CARDBUS CONTROLLER --(SHEET29,30) 23. CF SOCKET --(SHEET31) 24. AC'97 --(SHEET32) 25. AUDIO AMP --(SHEET33) 26. IEEE1394 (6PIN) PORT, DMB Conn. --(SHEET34) 27. KEYBOARD CONNECTOR --(SHEET35) 28. DC/DC POWER --(SHEET36) 29. CHARGER --(SHEET37) 30. DDR POWER --(SHEET38) 31. IMVP IV --(SHEET39) 32. GMCH POWER --(SHEET40) 33. SWITCHED POWER --(SHEET41) 34. MICOM POWER & POWER S/W --(SHEET42) 35. ALWAYS POWER --(SHEET43) 36. MOUNT HOLE --(SHEET44) 37. SUBBOARD CONNECTOR --(SHEET45) 38. TP --(SHEET46, 47) 												
<p>Model Name : Neon Main PCB Code : BA41-00449A Dev. Step : MP Revision : 1.0 T.R. Date : 2004.09.01</p>				<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">DRAW</th> <th style="width: 25%;">CHECK</th> <th style="width: 25%;">APPROVAL</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">YM AN</td> <td style="text-align: center;">HJ KIM</td> <td style="text-align: center;">YH JUNG</td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table>				DRAW	CHECK	APPROVAL	YM AN	HJ KIM	YH JUNG			
DRAW	CHECK	APPROVAL														
YM AN	HJ KIM	YH JUNG														
D	C	B	A	D	C	B	A									
4	3	2	1	D	C	B	A									

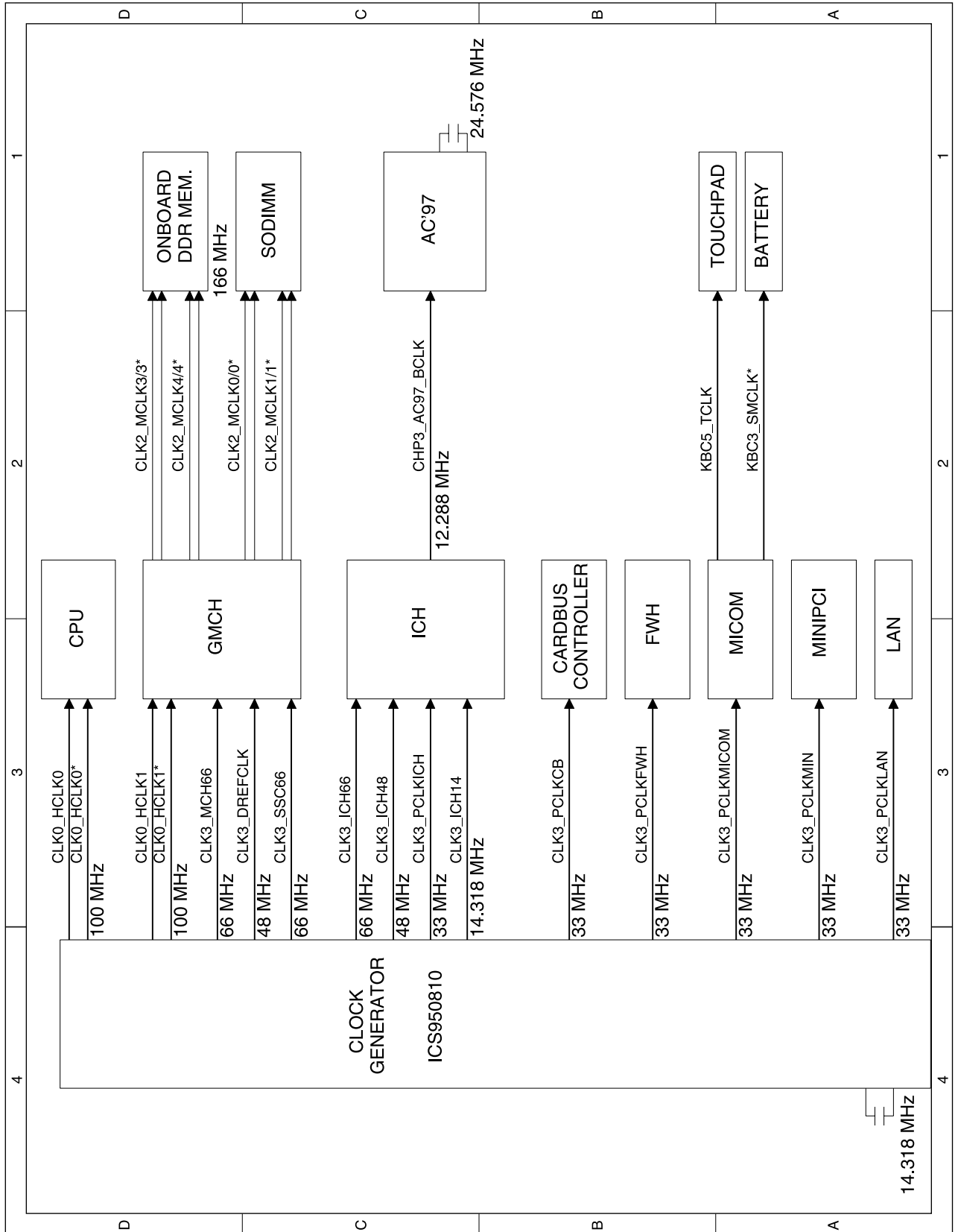
3-1-1(a) Main Board Schematic Sheet 2 of 47(Block Diagram)



3-1-1(b) Main Board Schematic Sheet 3 of 47(Power Sequence)



3-1-1(c) Main Board Schematic Sheet 4 of 47(Clock Distribution)



3-1-1(d) Main Board Schematic Sheet 5 of 47(Board Information)

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/INT#	Interrupts
Carbide	AD19	1	A
OTT1	AD21	3	G
BRCADCOM LAN	AD21	3	G
Internal MMC	AD22(internal)	-	E
USB	AD22(internal)	-	E
Hub to PCI	AD30(internal)	-	USB2.0 #0: A
LPC bridge/IDE/SMBUS	AD31(internal)	-	USB2.0 #1: D
			USB2.0 #2: C
			B

I²C / SMB Address

Devices	Address	Hex	Bus
ICH4	Master	1	SMBUS Master
ICH4	Slave	2h	Thermal Sensor
SODIMM0	1010 0000	40h	DRAM
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
2	DAB INTERFACE
OPTION	

System Power States

CHP3_SLPES3* S3, Suspend-To-RAM (STR): The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLPAS* S4, Suspend-To-Disk (STD): The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

CHP3_SLPSP* S5, Soft Off (S5OFF): System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Voltage Rails

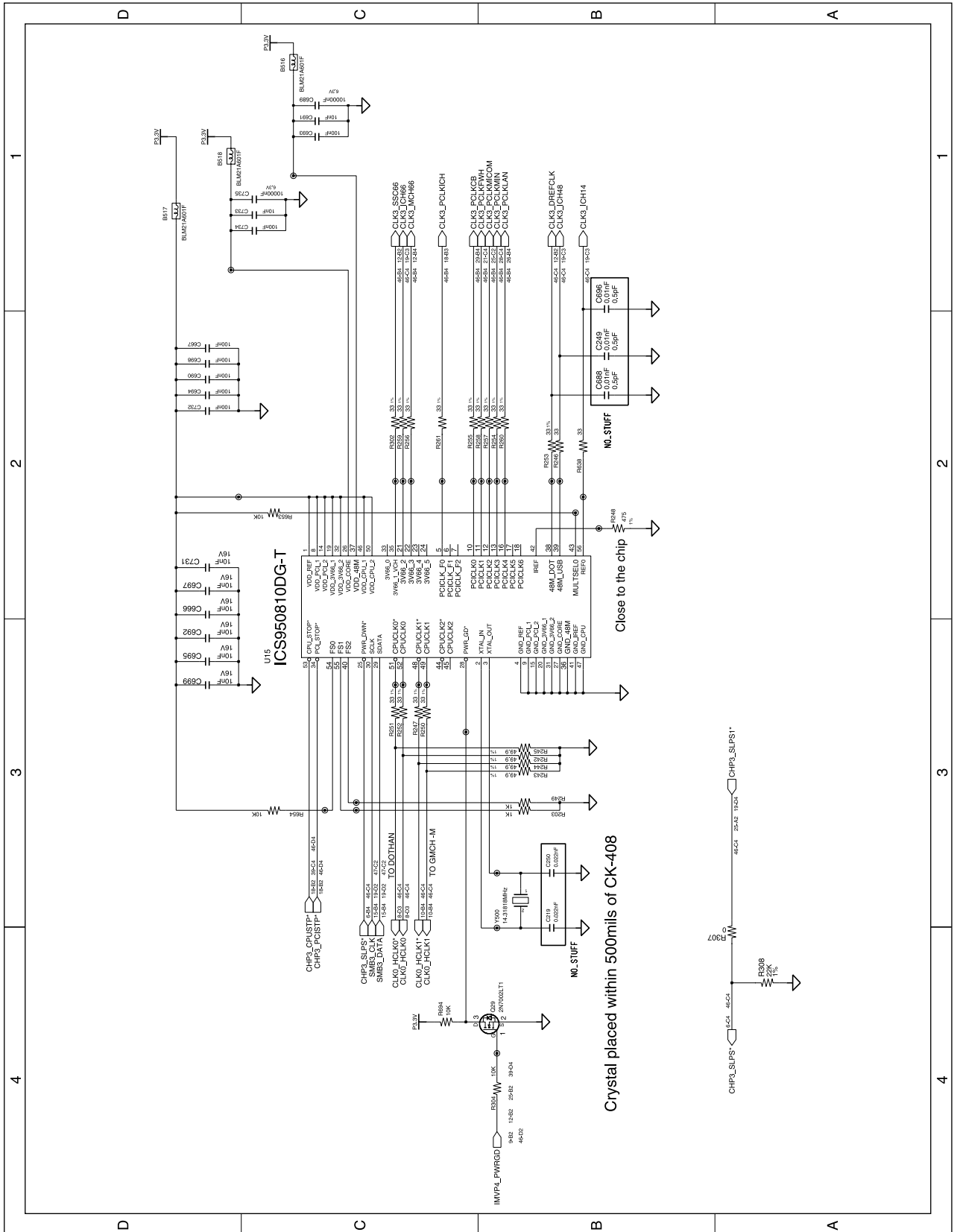
VDC	Primary DC system power supply (11.1 to 19V)
VCC-CORE	Core voltage for DOTHAN CPU (0.862 - 0.844V)
VCC-IO	Core voltage for DOTHAN CPU (0.862 - 0.844V)
VCC-MCH	Core voltage for System Bus (PSB) Termination (1.05V)
MCH-AC VAL	1.35V
P1.5V_AUX	1.5V switched power rail (off in S3-S5)
P2.5V_AUX	2.5V switched power rail (off in S3-S5)
P2.5V_AUX	2.5V power rail (off in S4-S5)
P3.3V_AUX	3.3V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V_AUX	3.3V switched power rail (off in S3-S5)
P5V_AUX	5.0V switched power rail (off in S3-S5)
P5V_AUX	5V power rail (off in S4-S5)

CPU Core Voltage Table

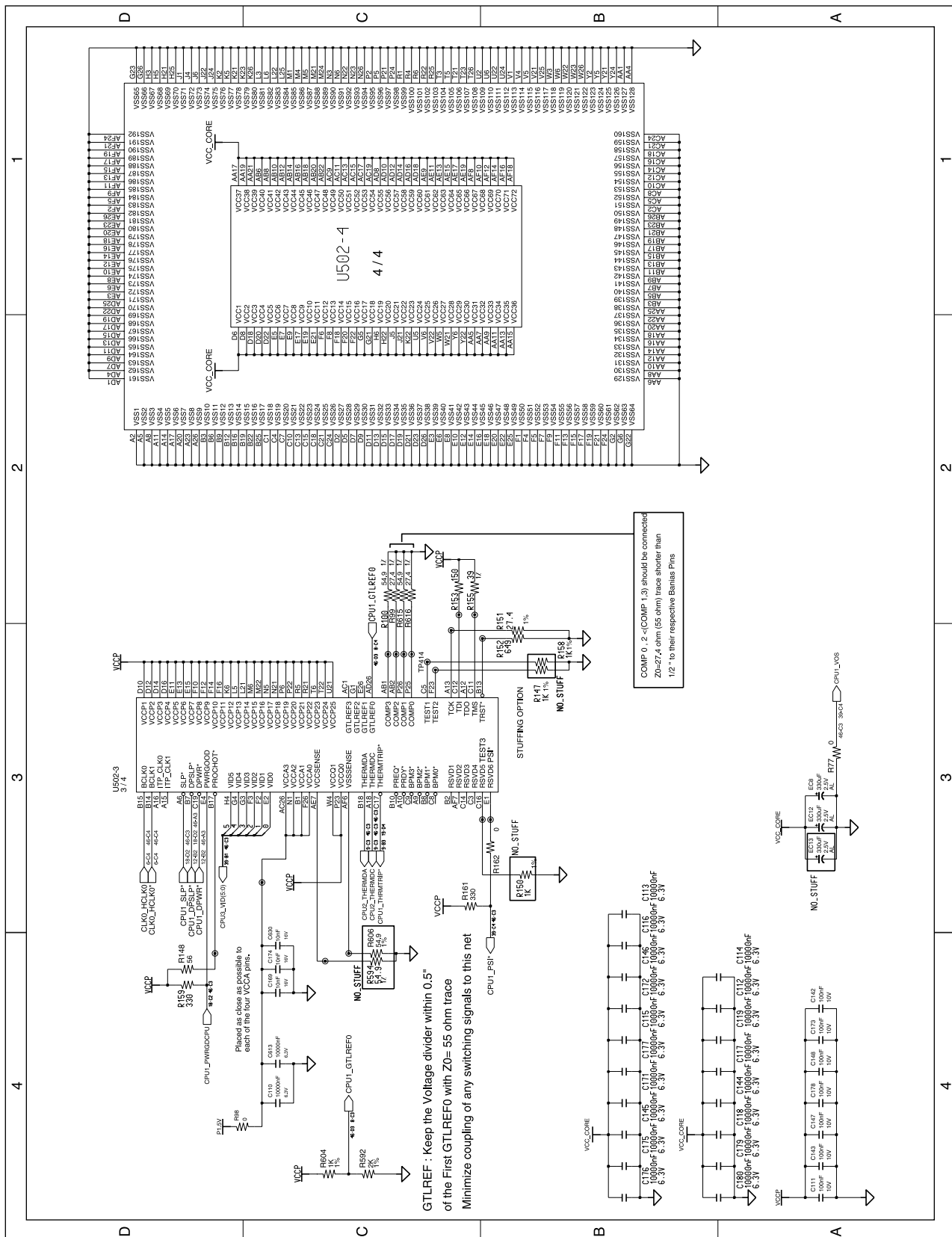
VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.750 V
0	0	0	0	0	0	1.680 V
0	0	0	0	0	0	1.676 V
0	0	0	0	0	0	1.664 V
0	0	0	0	0	0	1.644 V
0	0	0	0	0	0	1.628 V
0	0	0	0	0	0	1.616 V
0	0	0	0	0	0	1.596 V
0	0	0	0	0	0	1.584 V
0	0	0	0	0	0	1.560 V
0	0	0	0	0	0	1.552 V
0	0	0	0	0	0	1.548 V
0	0	0	0	0	0	1.500 V
0	0	0	0	0	0	1.484 V
0	0	0	0	0	0	1.456 V
0	0	0	0	0	0	1.436 V
0	0	0	0	0	0	1.420 V
0	0	0	0	0	0	1.404 V
0	0	0	0	0	0	1.376 V
0	0	0	0	0	0	1.360 V
0	0	0	0	0	0	1.356 V
0	0	0	0	0	0	1.324 V
0	0	0	0	0	0	1.308 V
0	0	0	0	0	0	1.292 V
0	0	0	0	0	0	1.276 V
0	0	0	0	0	0	1.276 V
0	0	0	0	0	0	1.260 V
0	0	0	0	0	0	1.260 V
0	0	0	0	0	0	1.228 V
0	0	0	0	0	0	1.212 V
0	0	0	0	0	0	1.212 V

DOTHAN ULV
HIGH FREQUENCY MODE
LOW FREQUENCY MODE

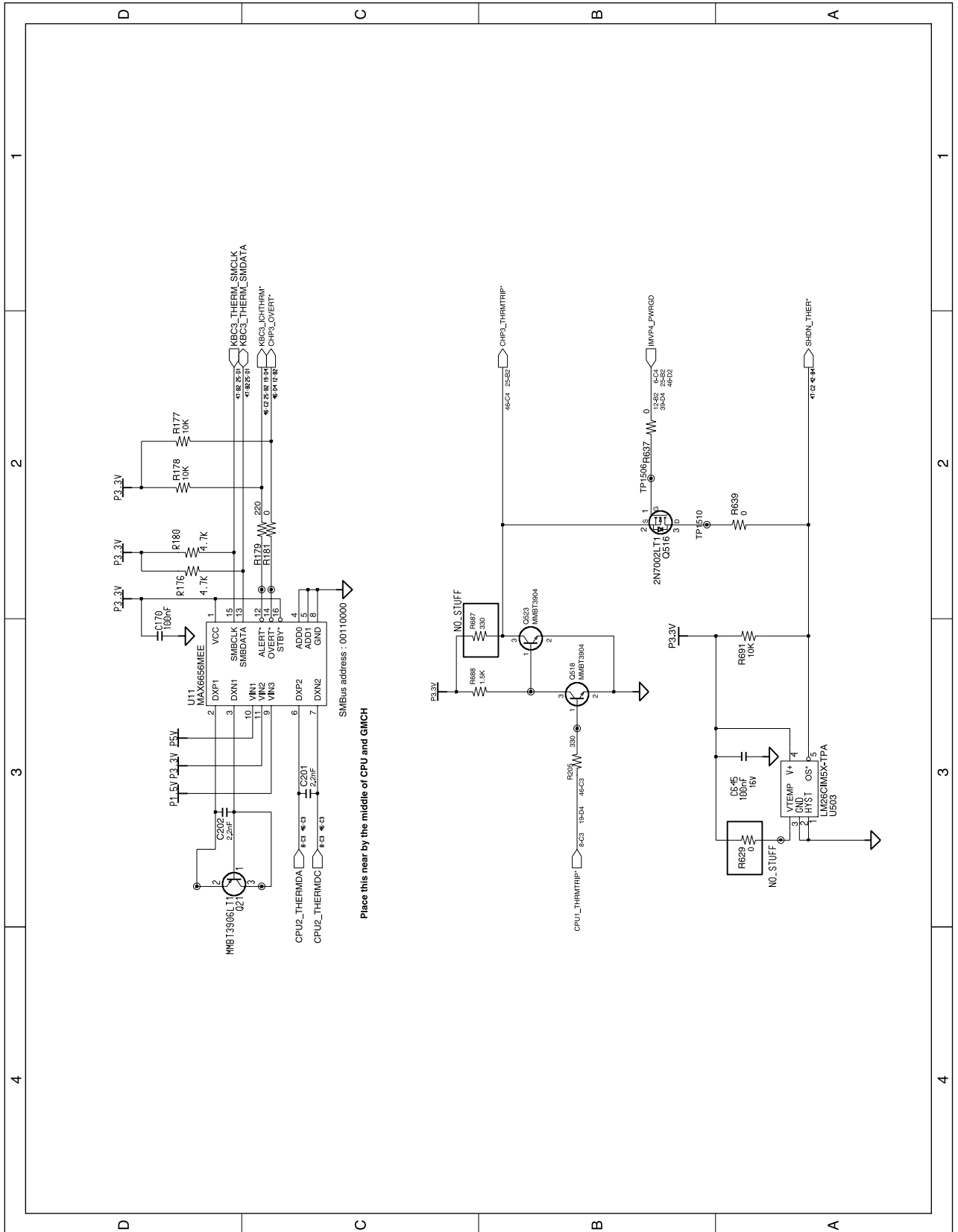
3-1-1(e) Main Board Schematic Sheet 6 of 47(Clock Generator)



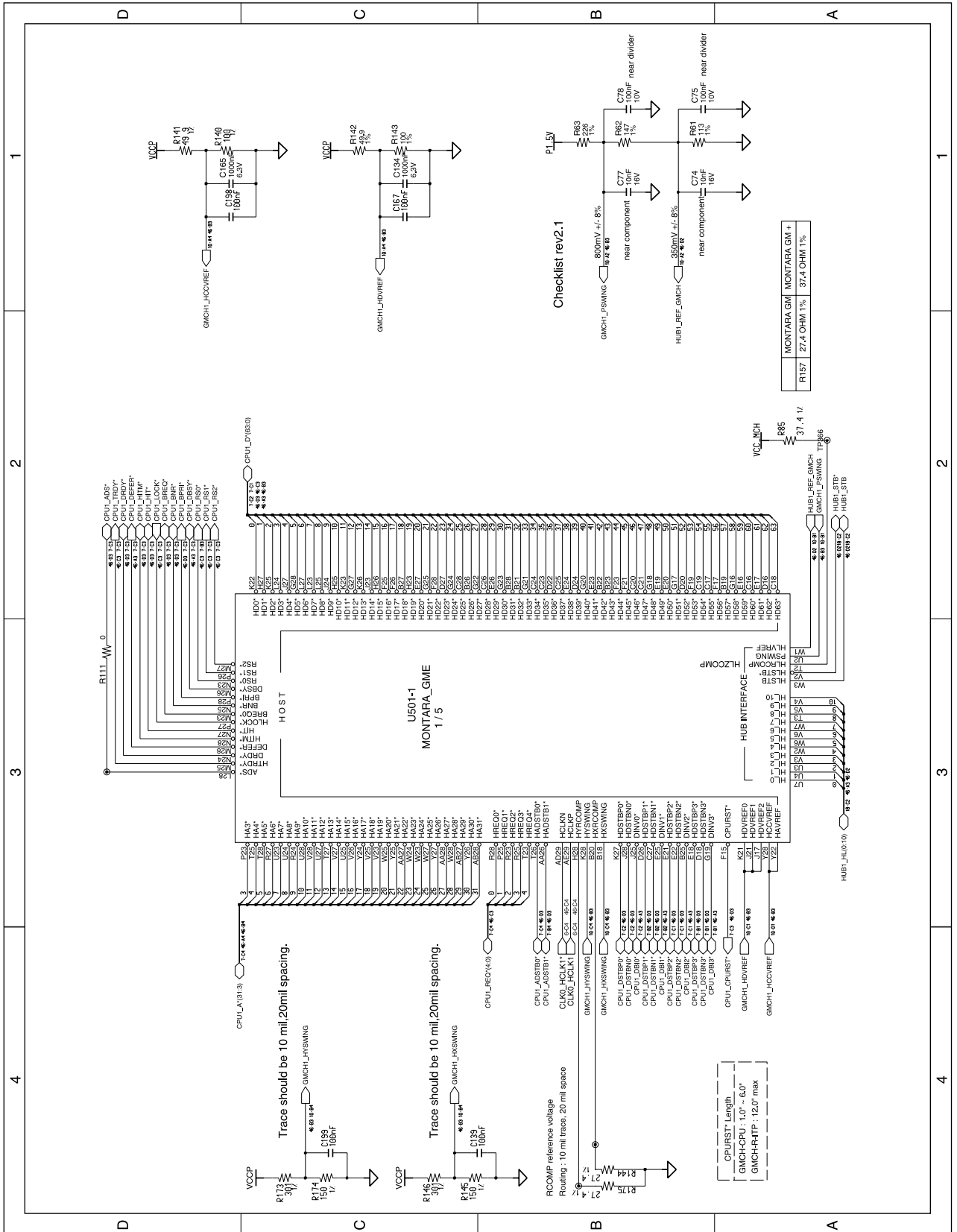
3-1-1(g) Main Board Schematic Sheet 8 of 47(Dothan CPU)



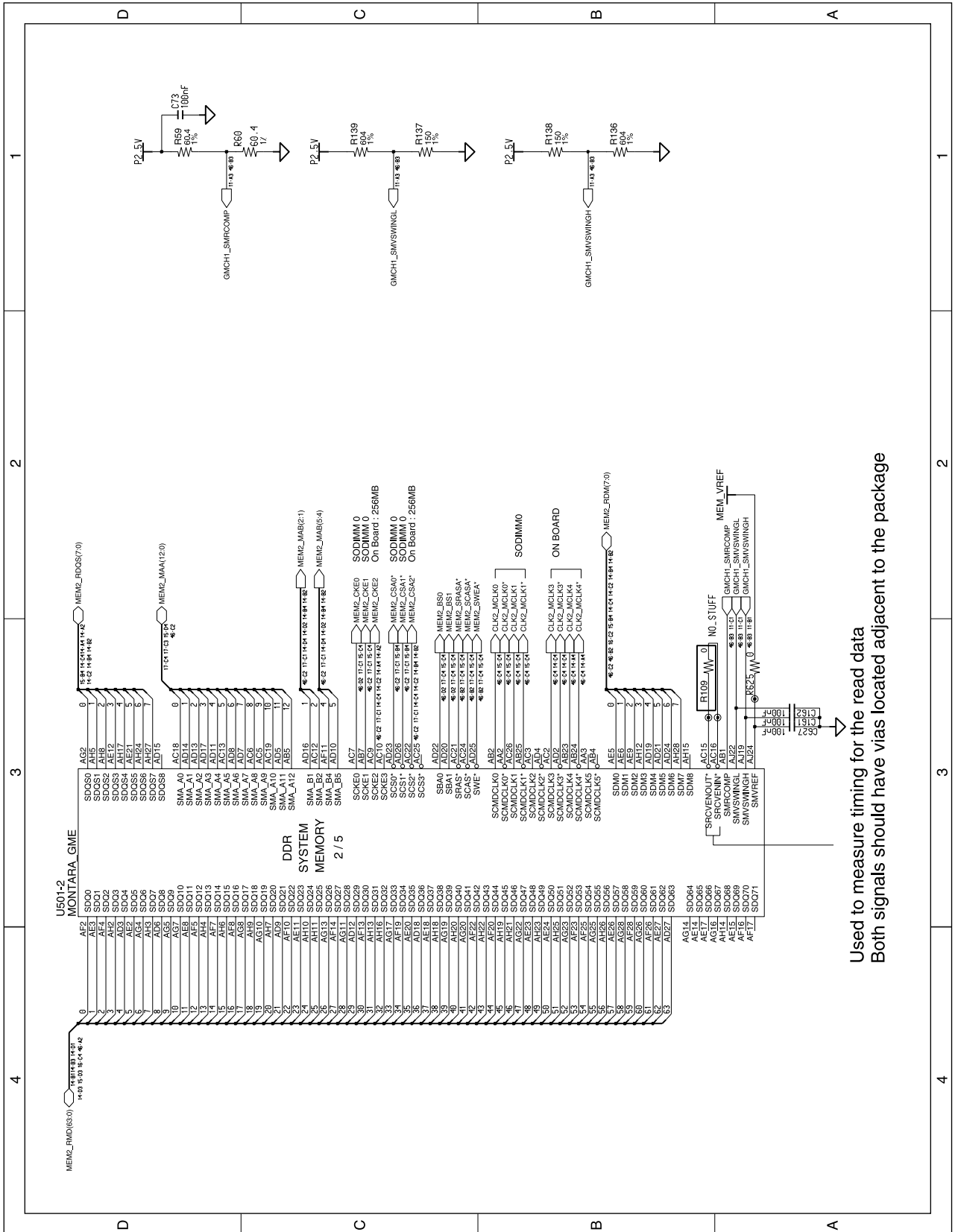
3-1-1(h) Main Board Schematic Sheet 9 of 47(Thermal Sensor)



3-1-1(i) Main Board Schematic Sheet 10 of 47(Montara-GM+)

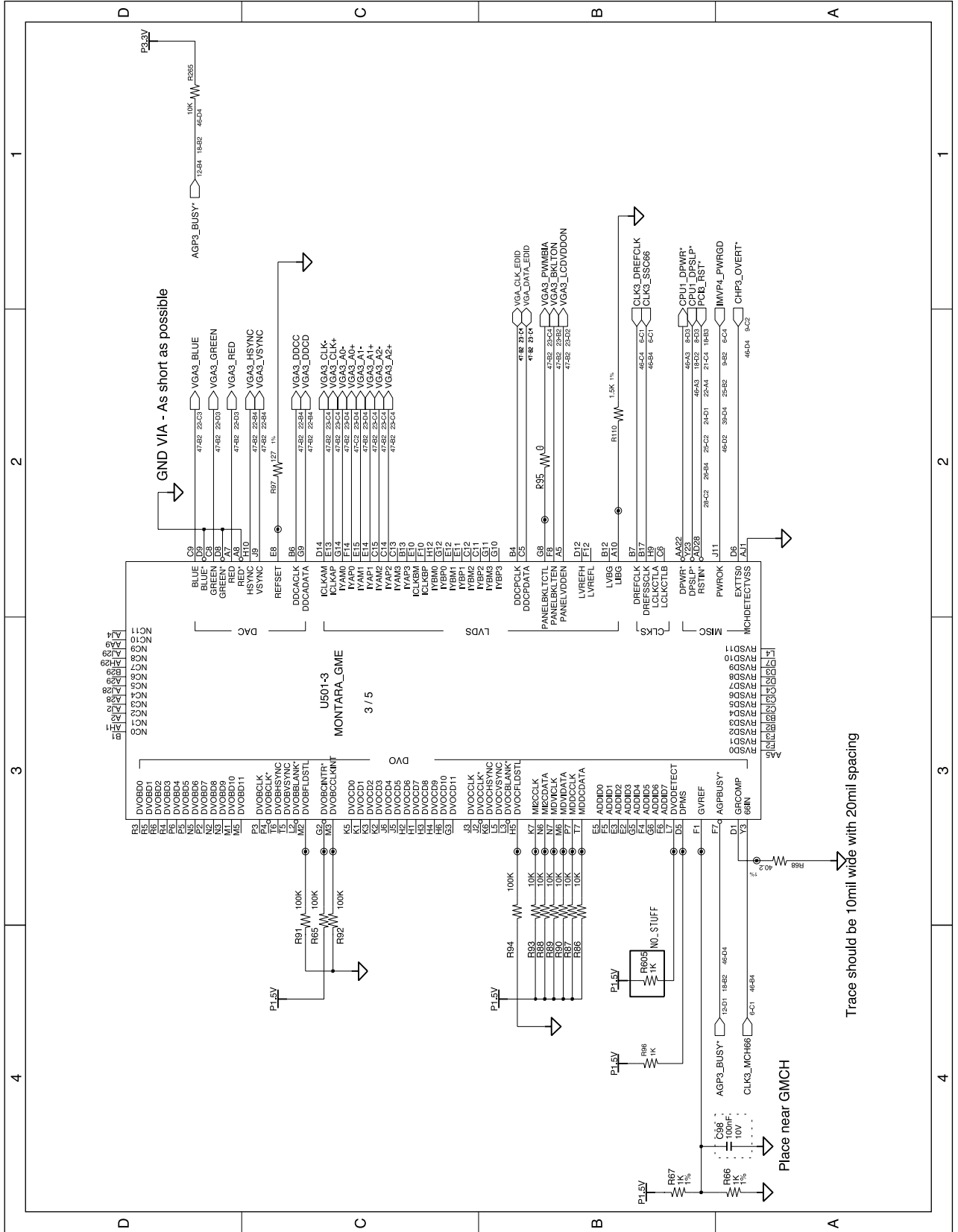


3-1-1(j) Main Board Schematic Sheet 11 of 47(Montara-GM+)

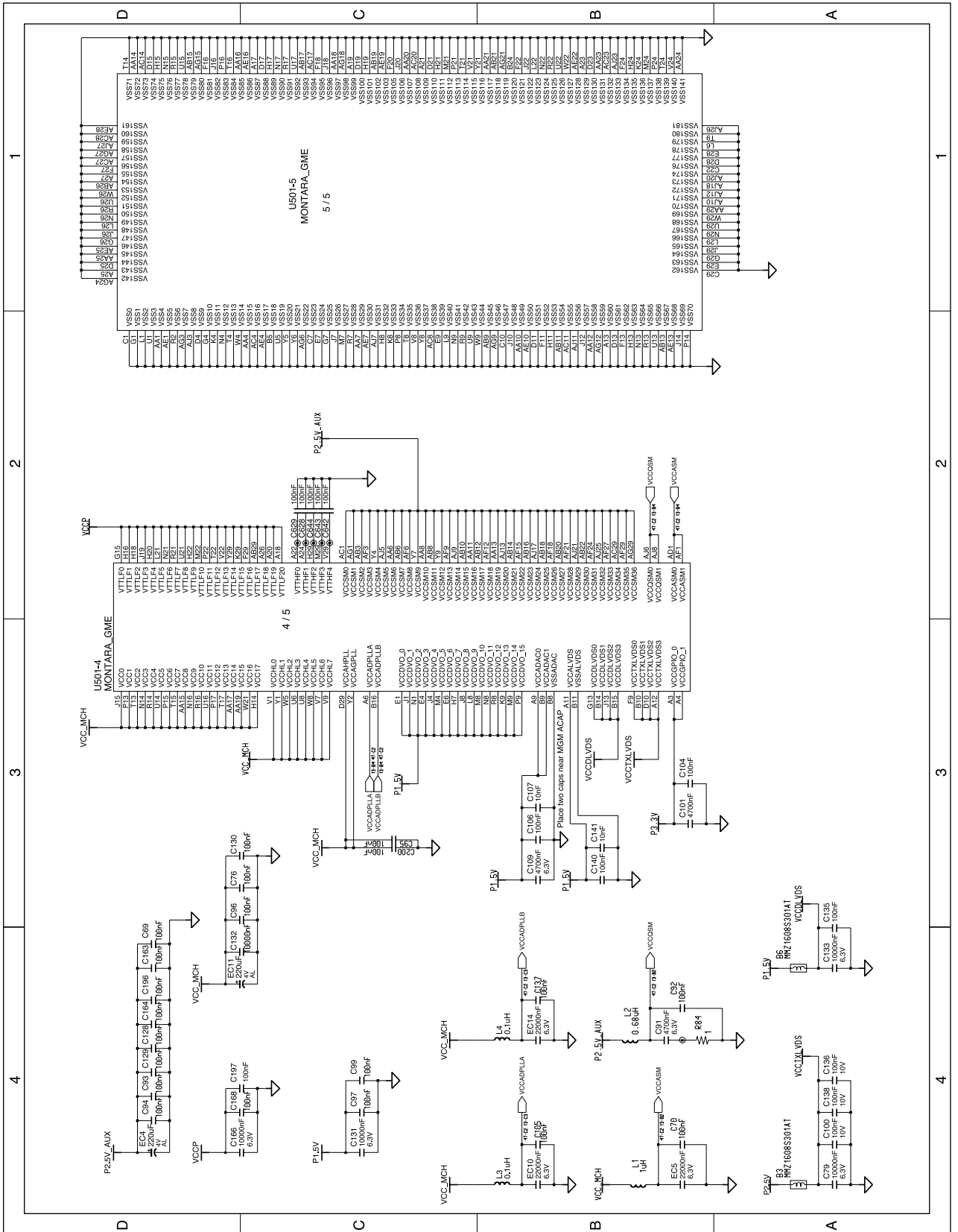


Used to measure timing for the read data
Both signals should have vias located adjacent to the package

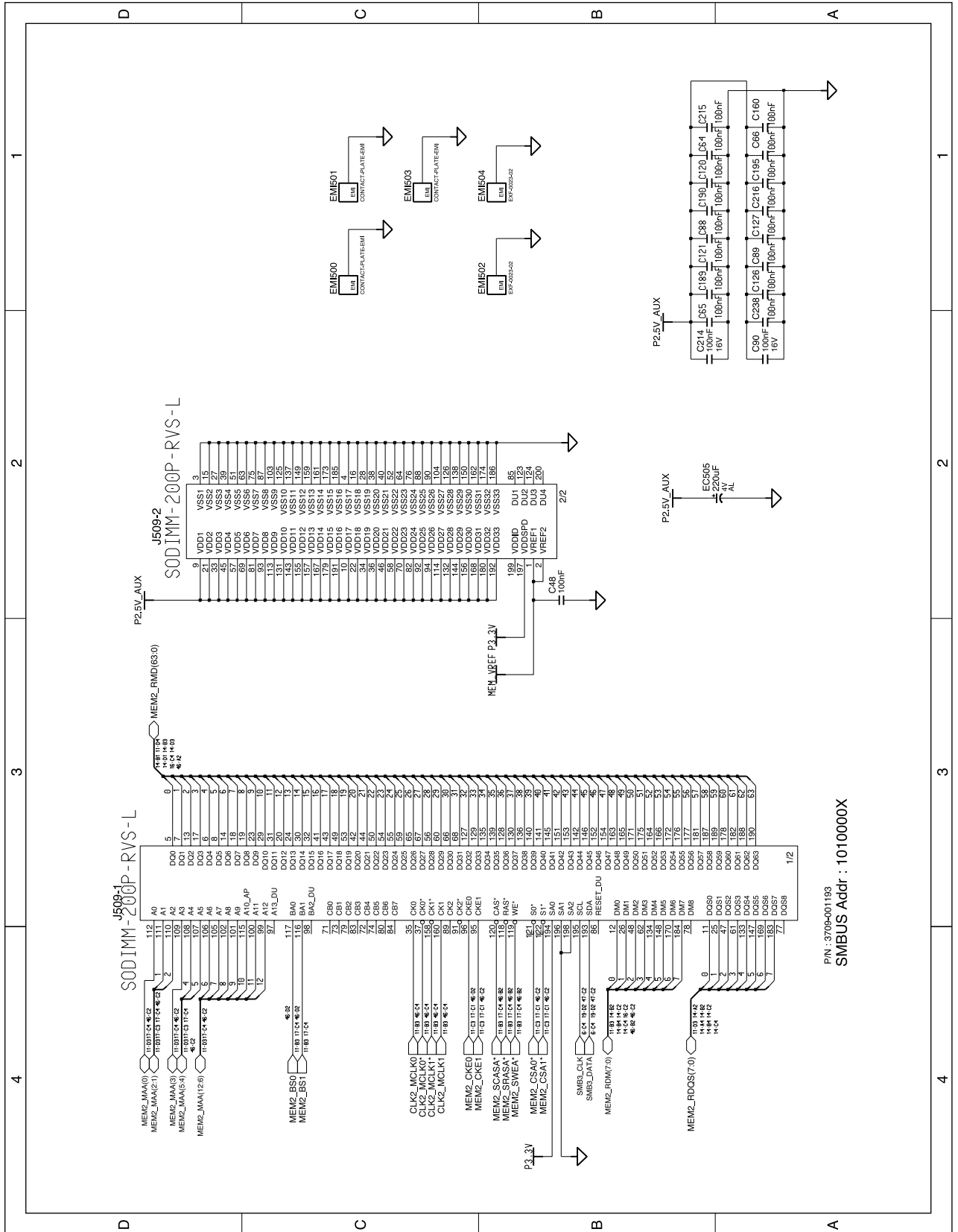
3-1-1(k) Main Board Schematic Sheet 12 of 47(Montara-GM+)



3-1-1(I) Main Board Schematic Sheet 13 of 47(Montara-GM+)

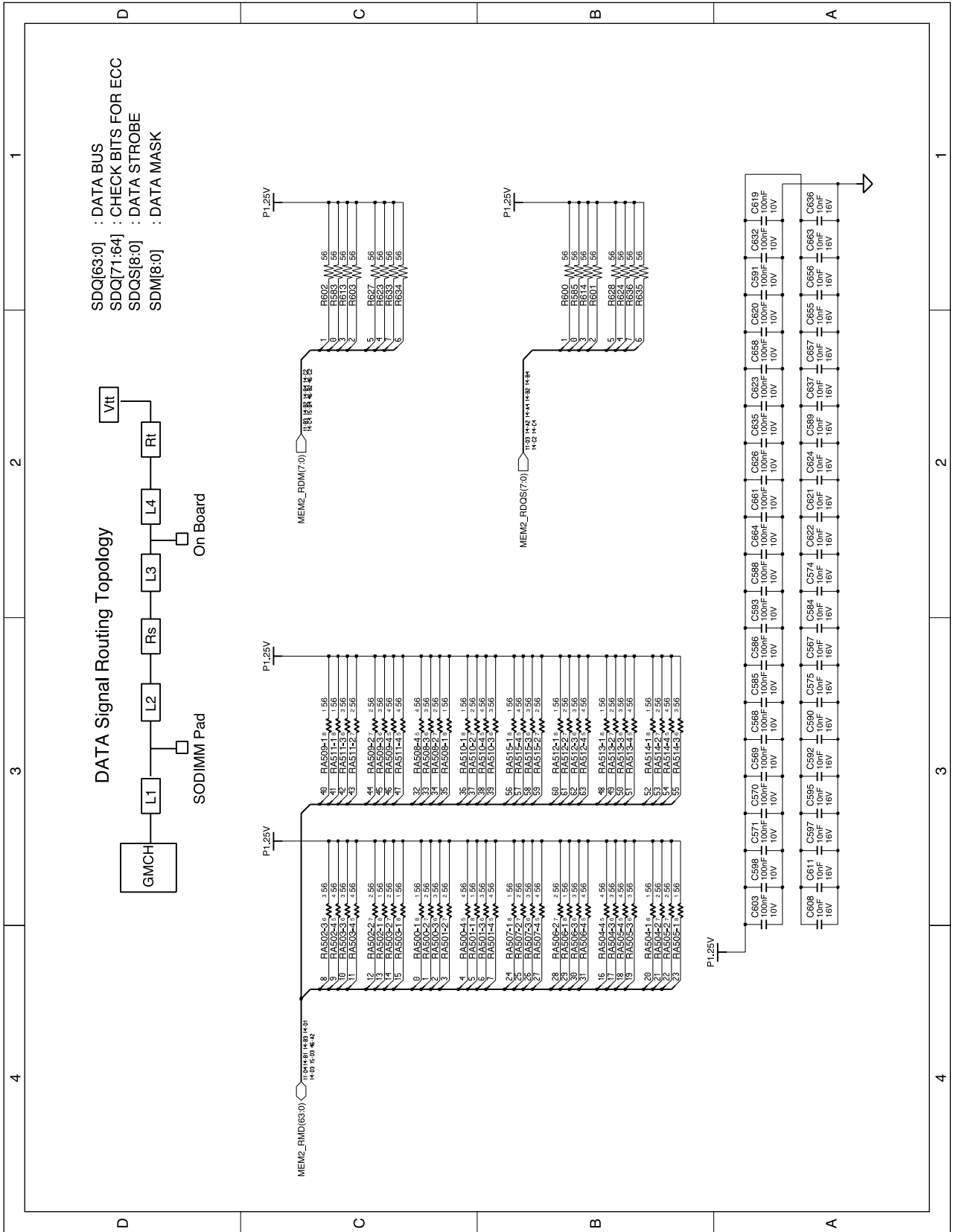


3-1-1(n) Main Board Schematic Sheet 15 of 47(DDR SODIMM)

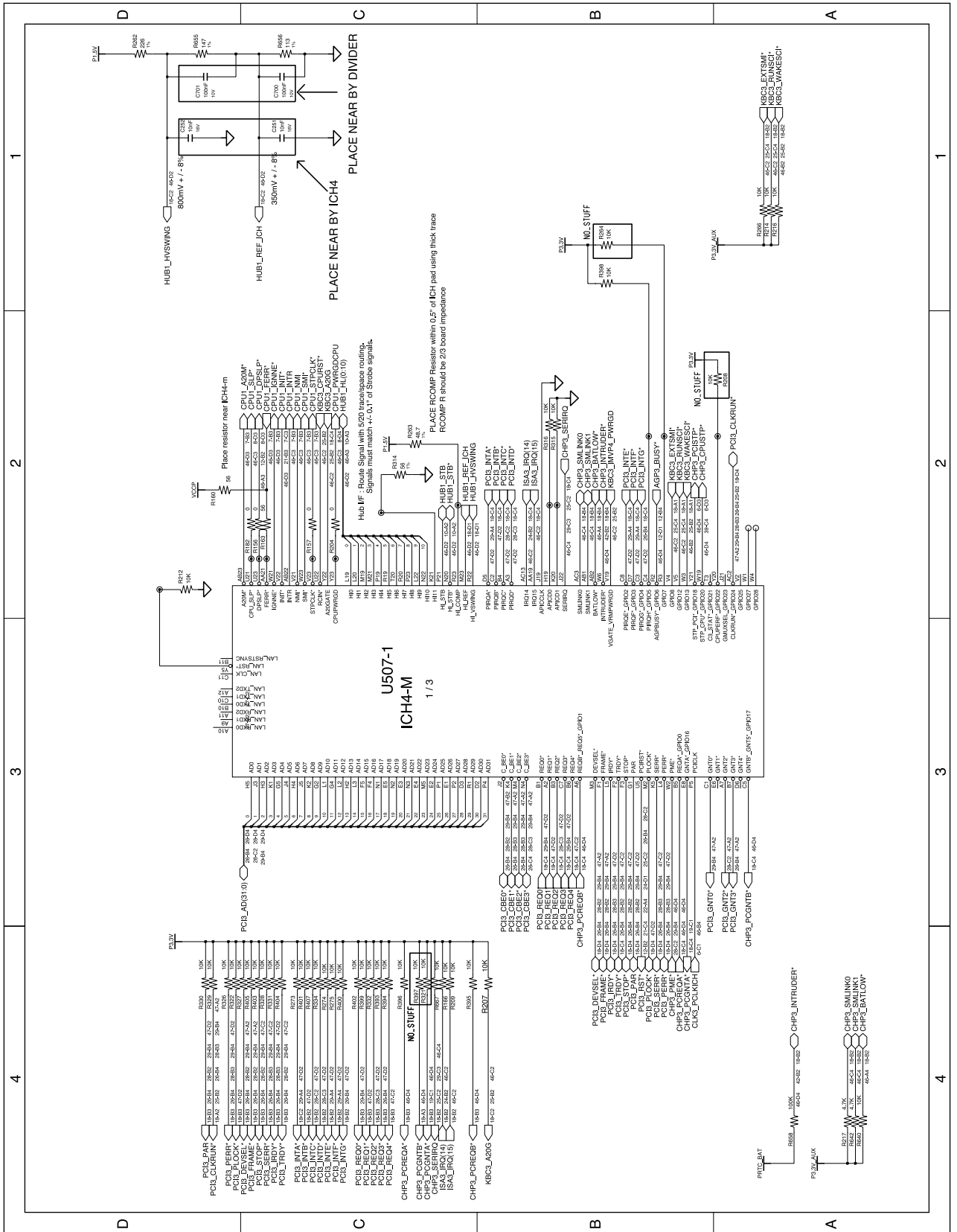


PIN : 3709-001193
SMBUS Addr : 1010000X

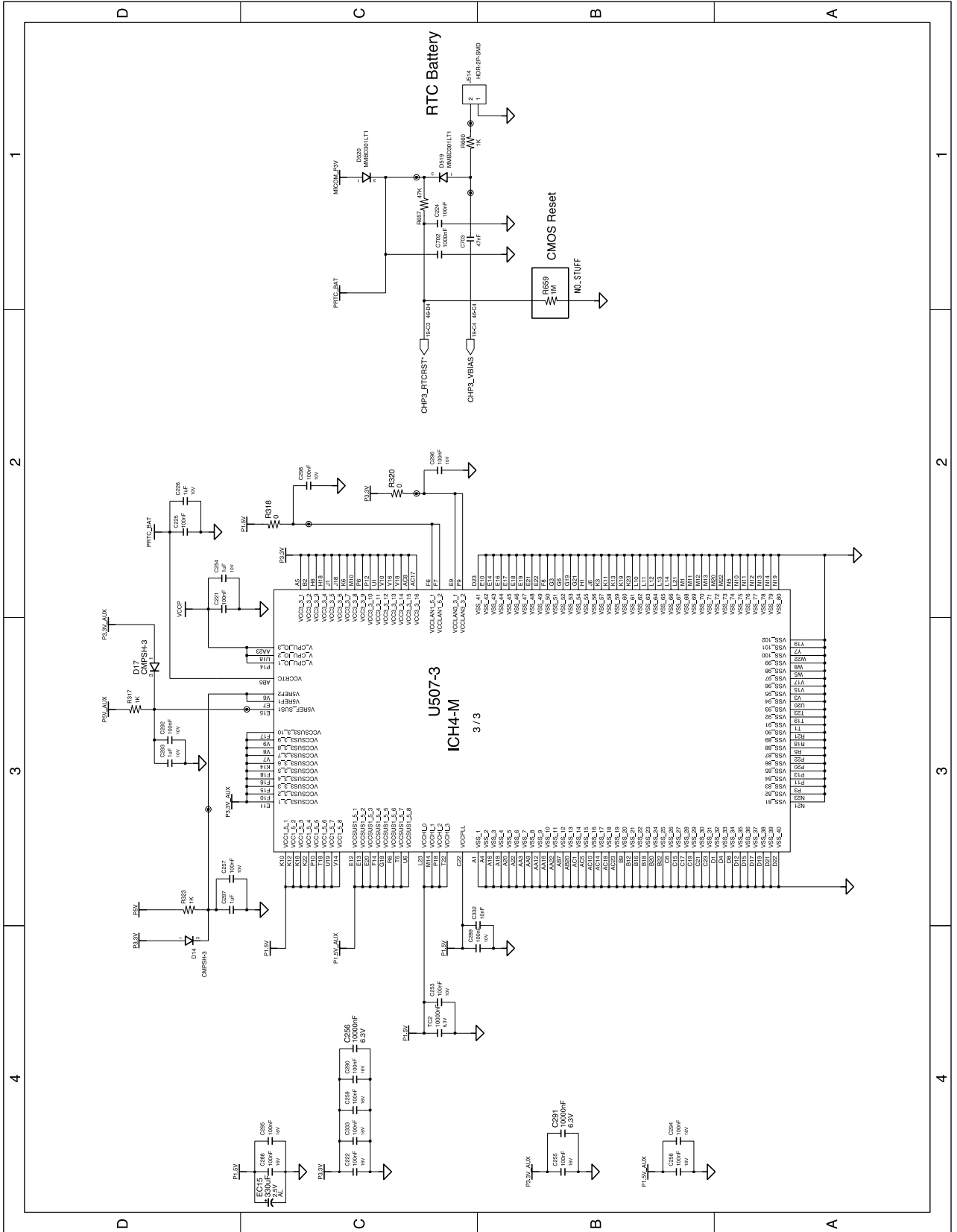
3-1-1(o) Main Board Schematic Sheet 16 of 47(DDR Termination)



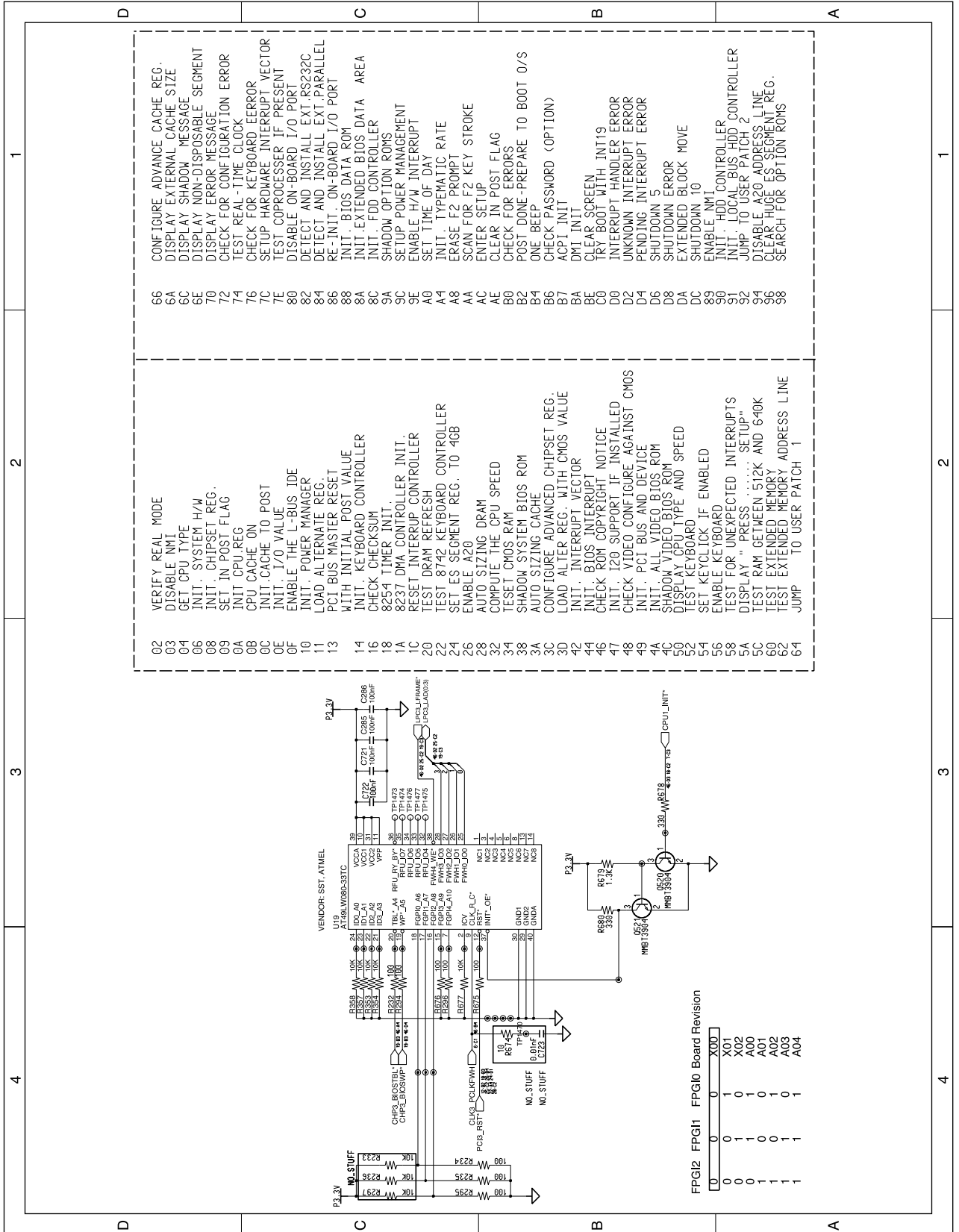
3-1-1(q) Main Board Schematic Sheet 18 of 47(ICH4-M)



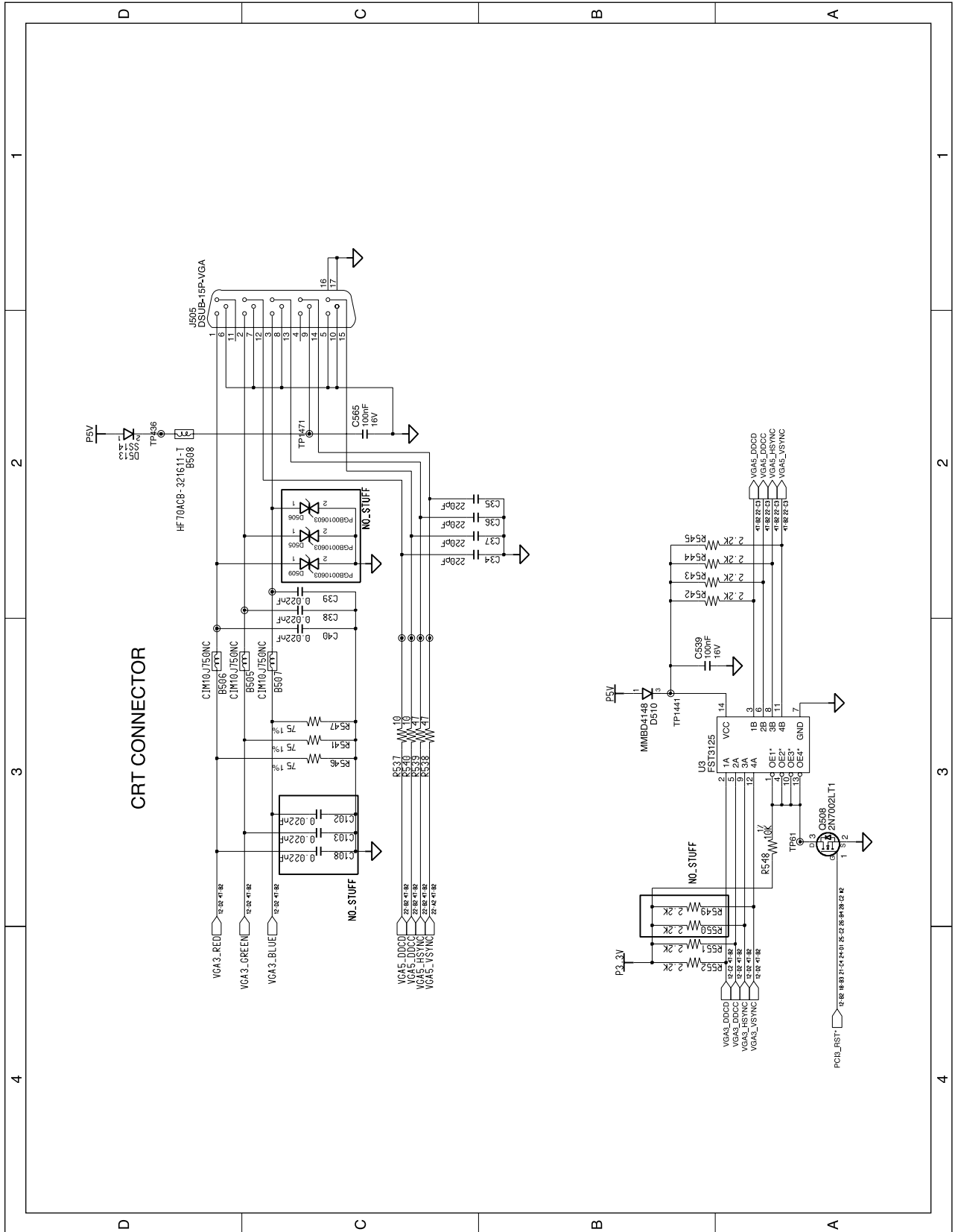
3-1-1(s) Main Board Schematic Sheet 20 of 47(ICH4-M)



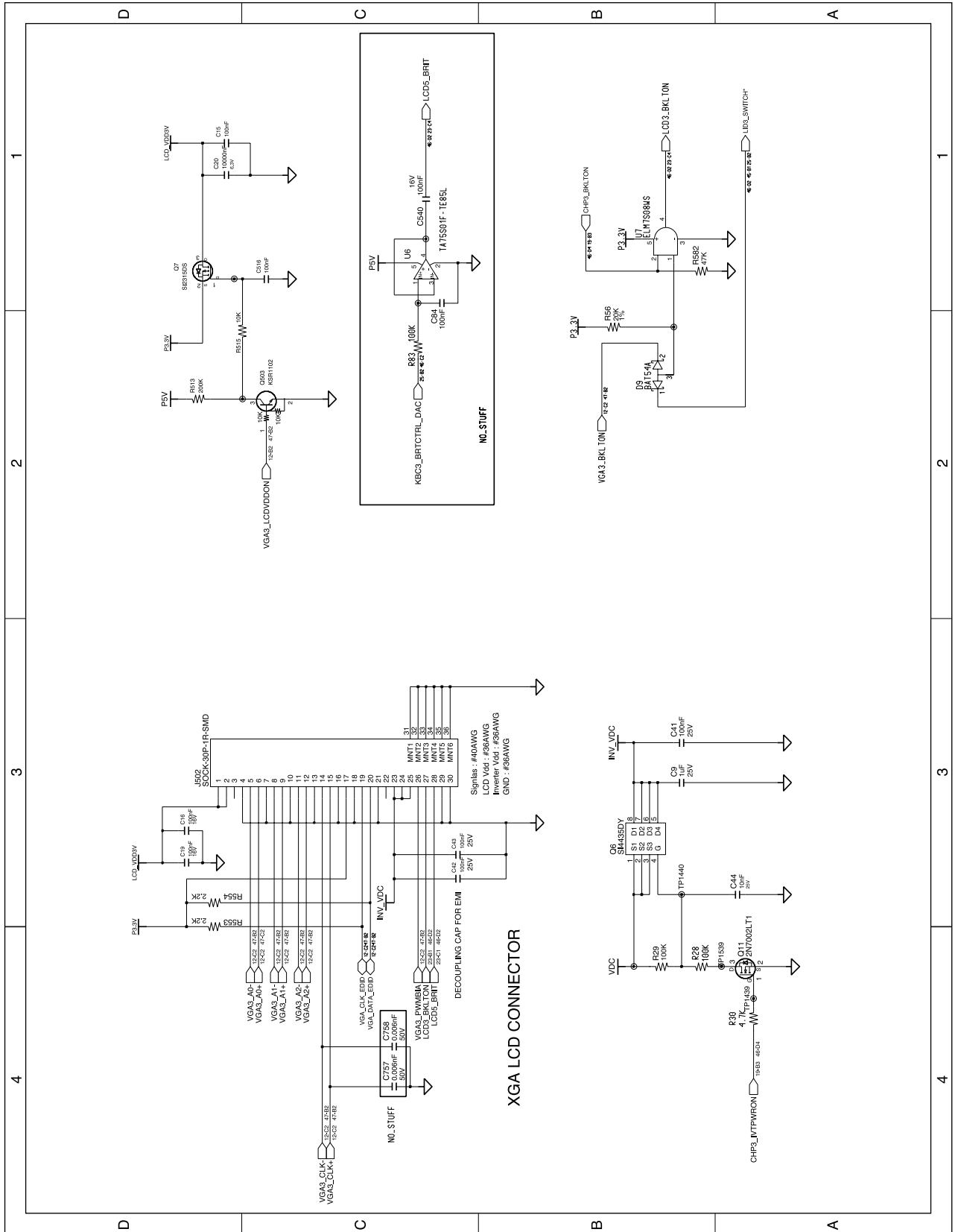
3-1-1(t) Main Board Schematic Sheet 21 of 47(FWH)



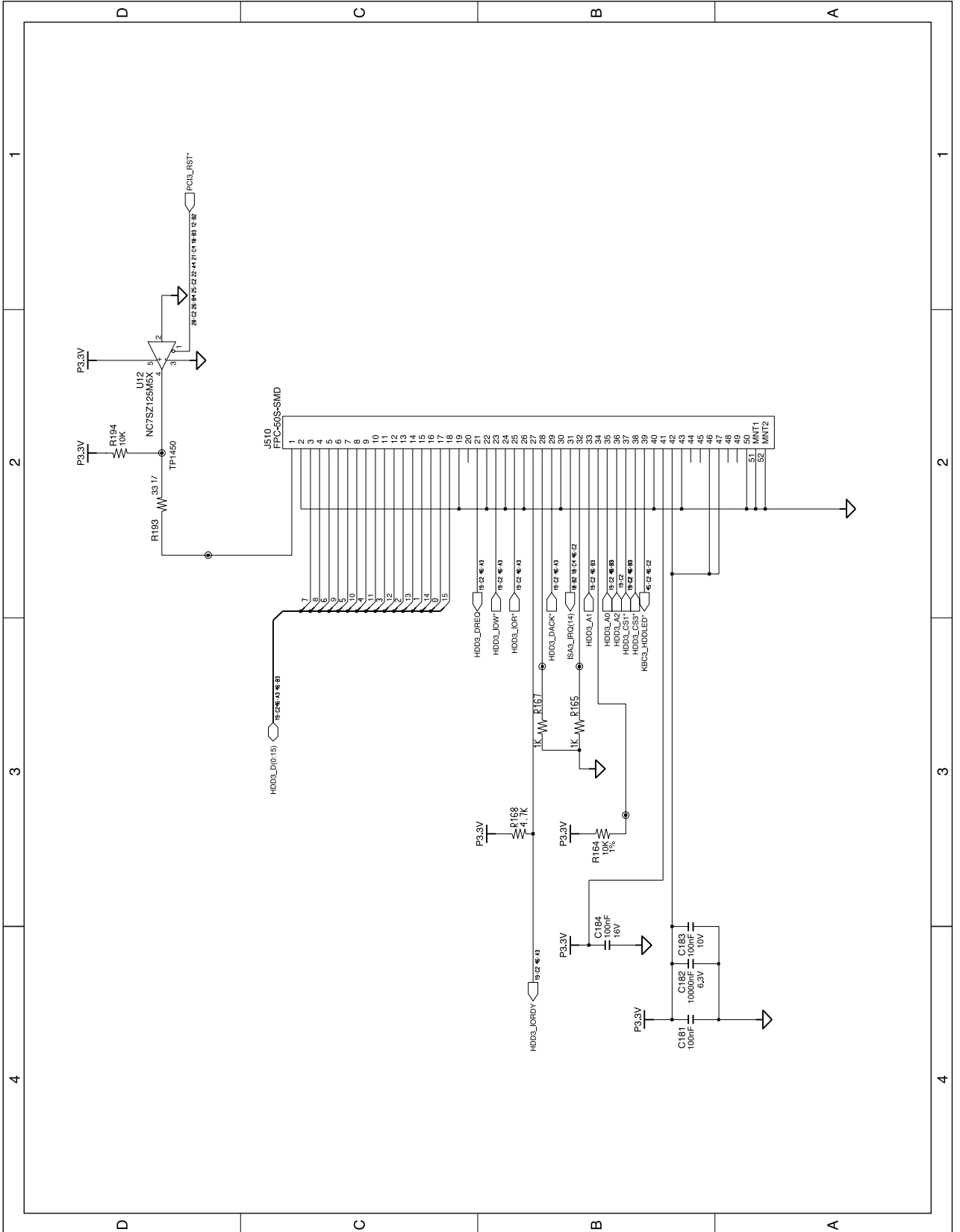
3-1-1(u) Main Board Schematic Sheet 22 of 47(CRT Connector)



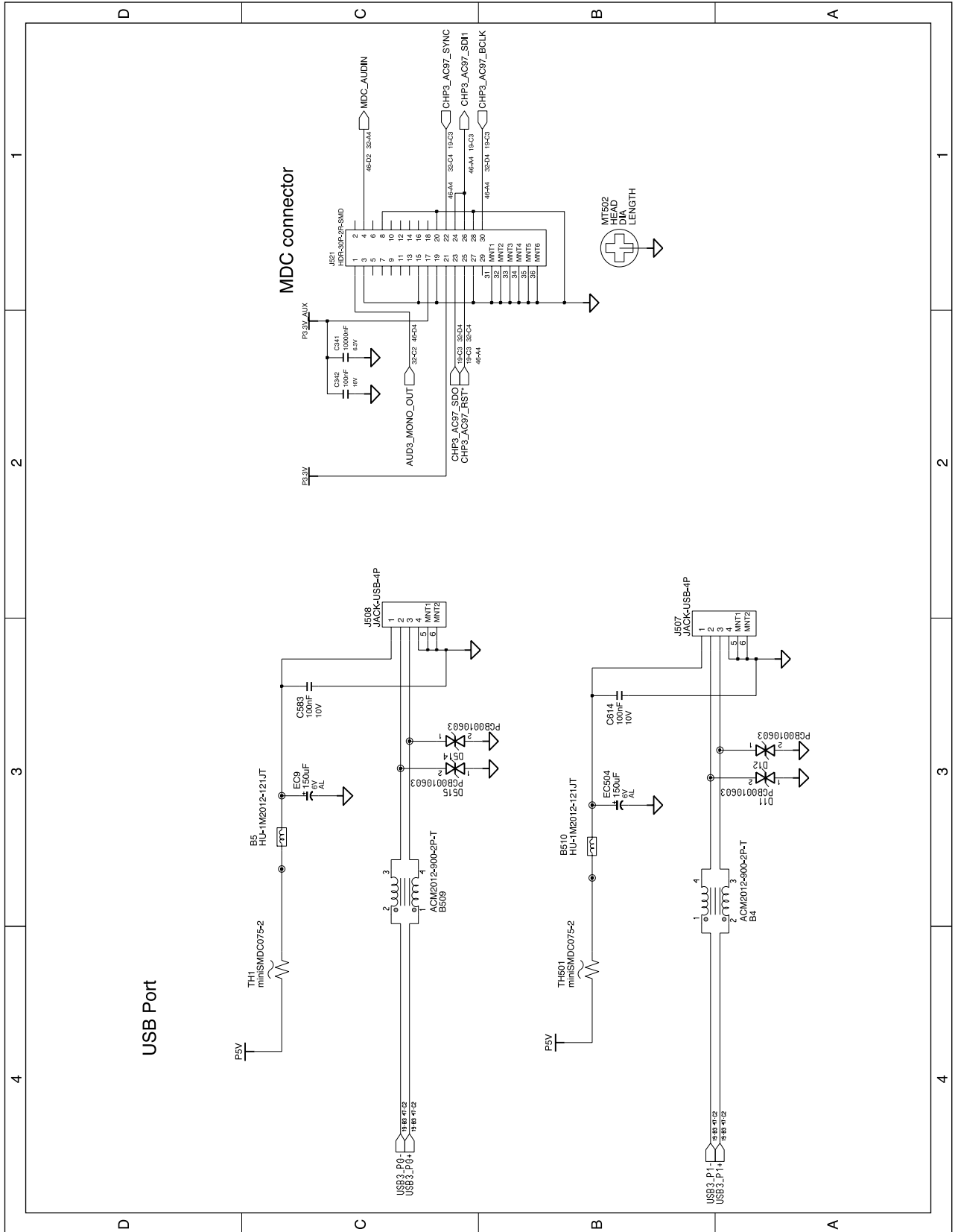
3-1-1(v) Main Board Schematic Sheet 23 of 47(LCD Connector)



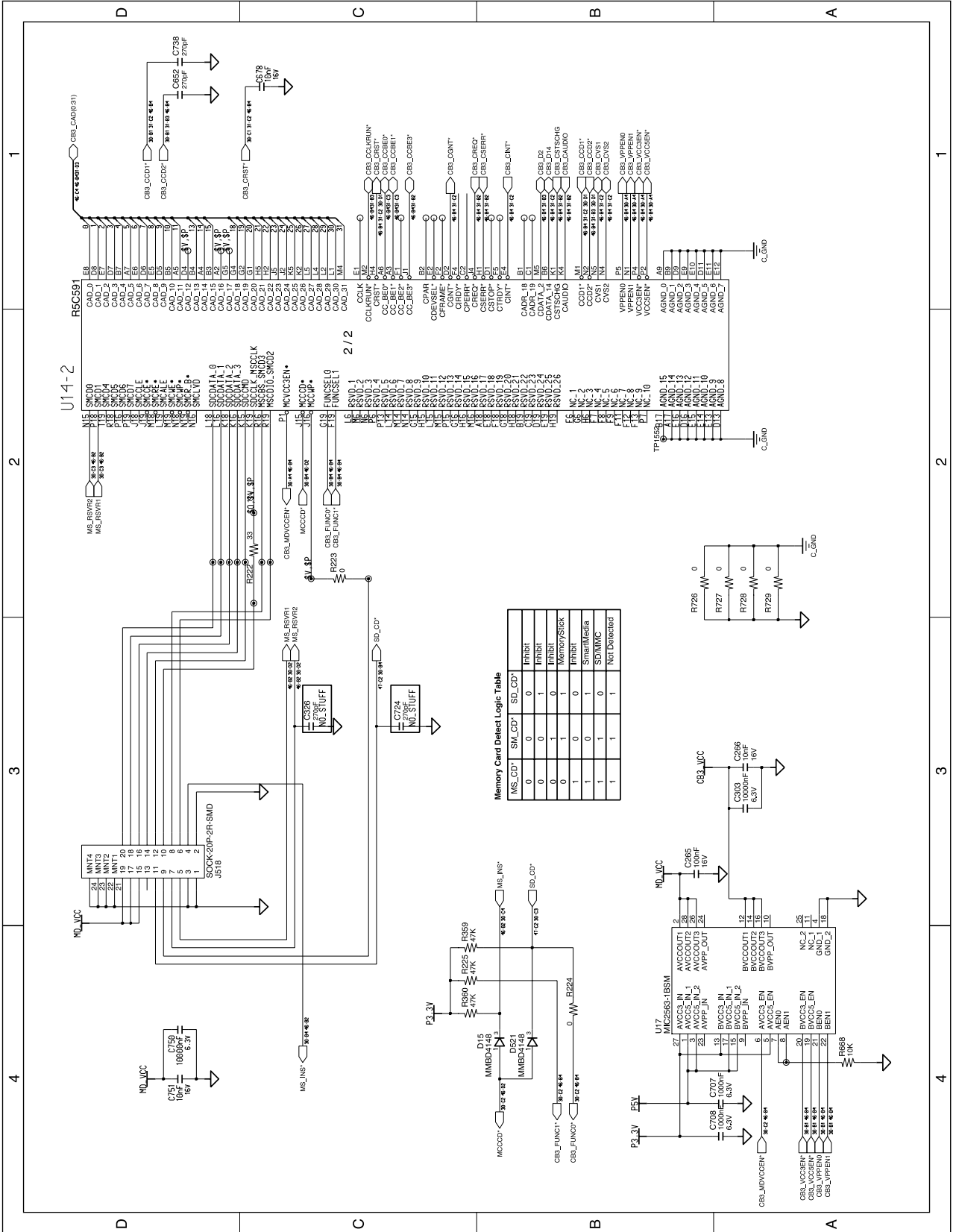
3-1-1(w) Main Board Schematic Sheet 24 of 47(HDD Connector)



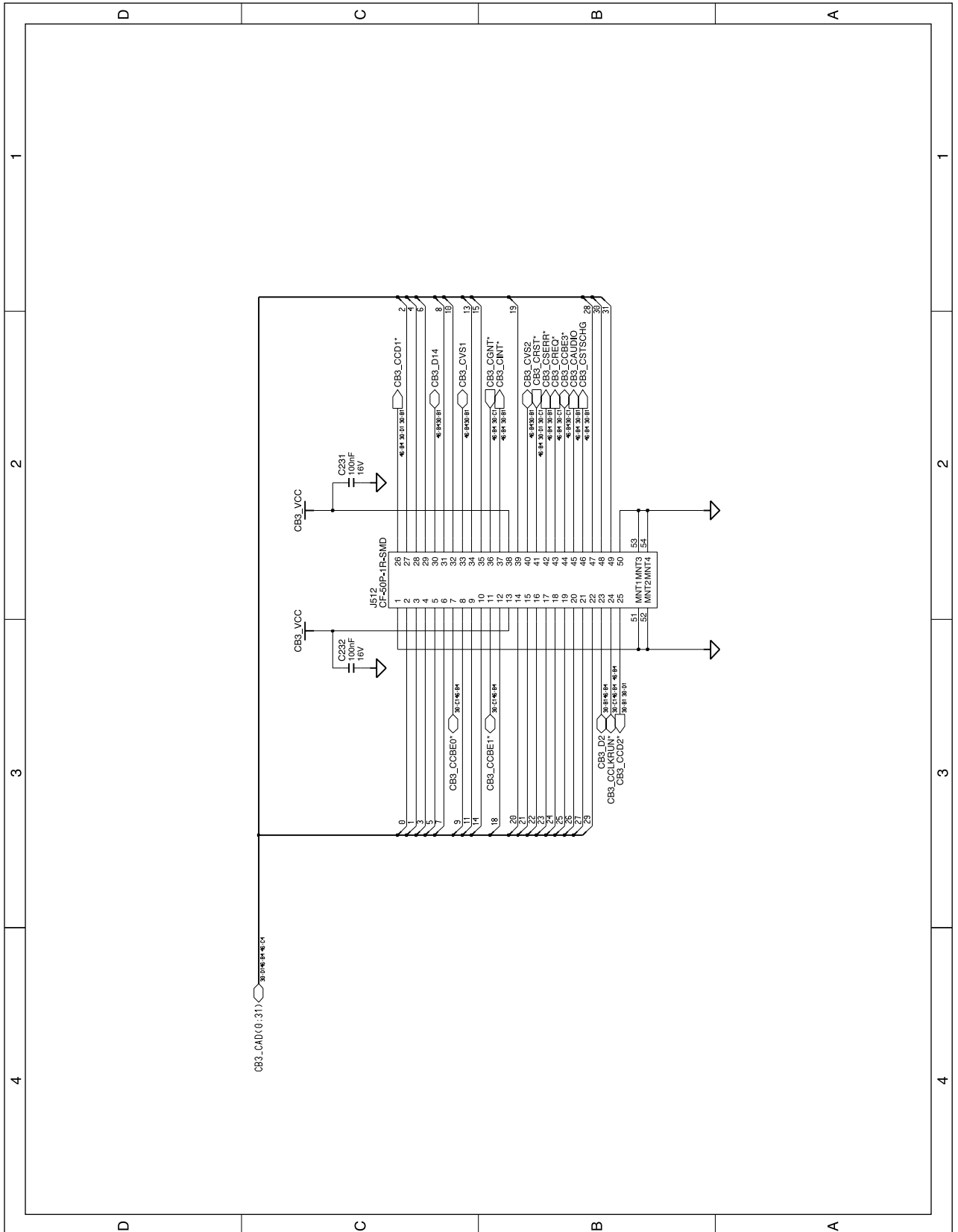
3-1-1(z) Main Board Schematic Sheet 27 of 47(USB & MDC Connector)



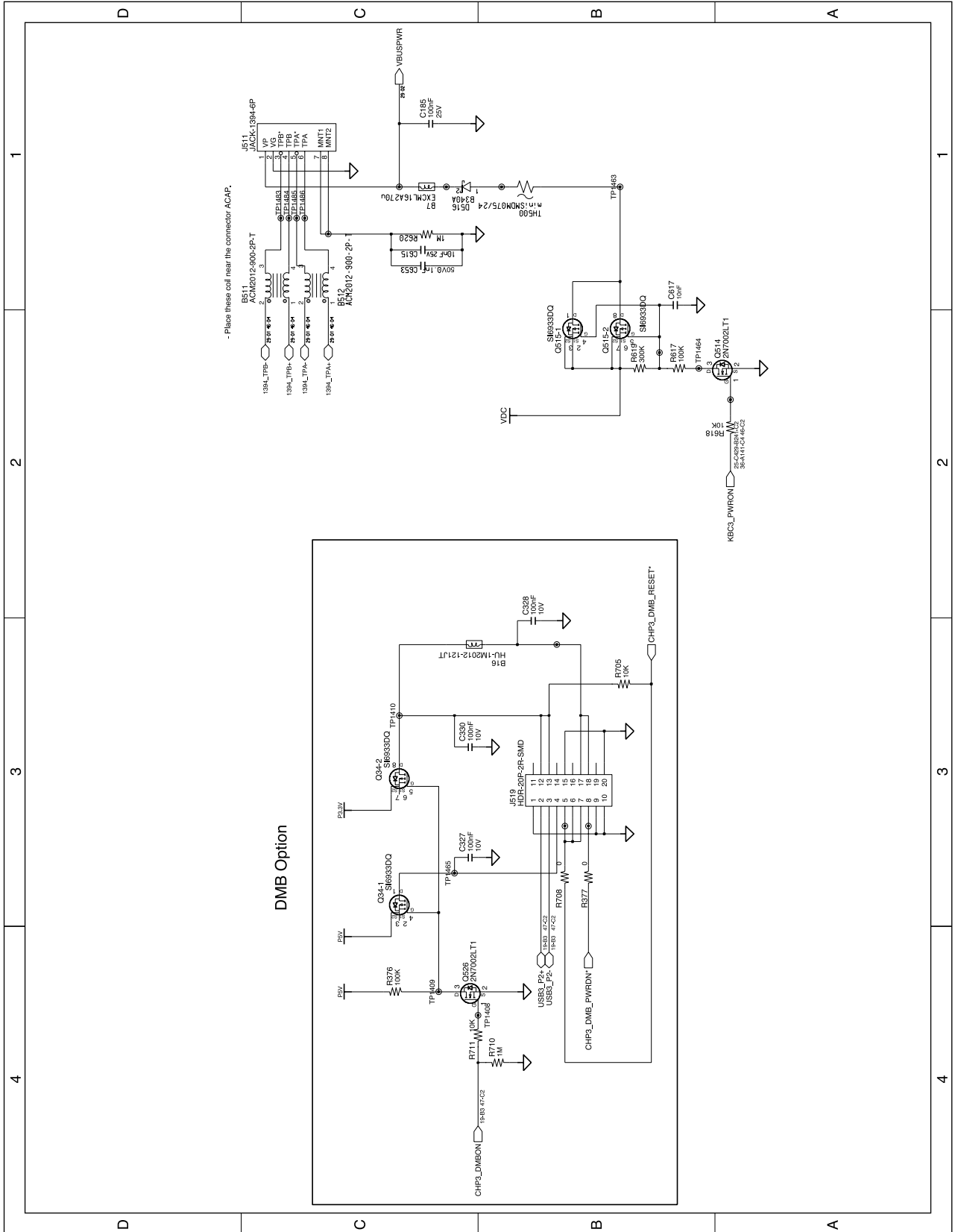
3-1-1(cc) Main Board Schematic Sheet 30 of 47(Cardbus Controller)



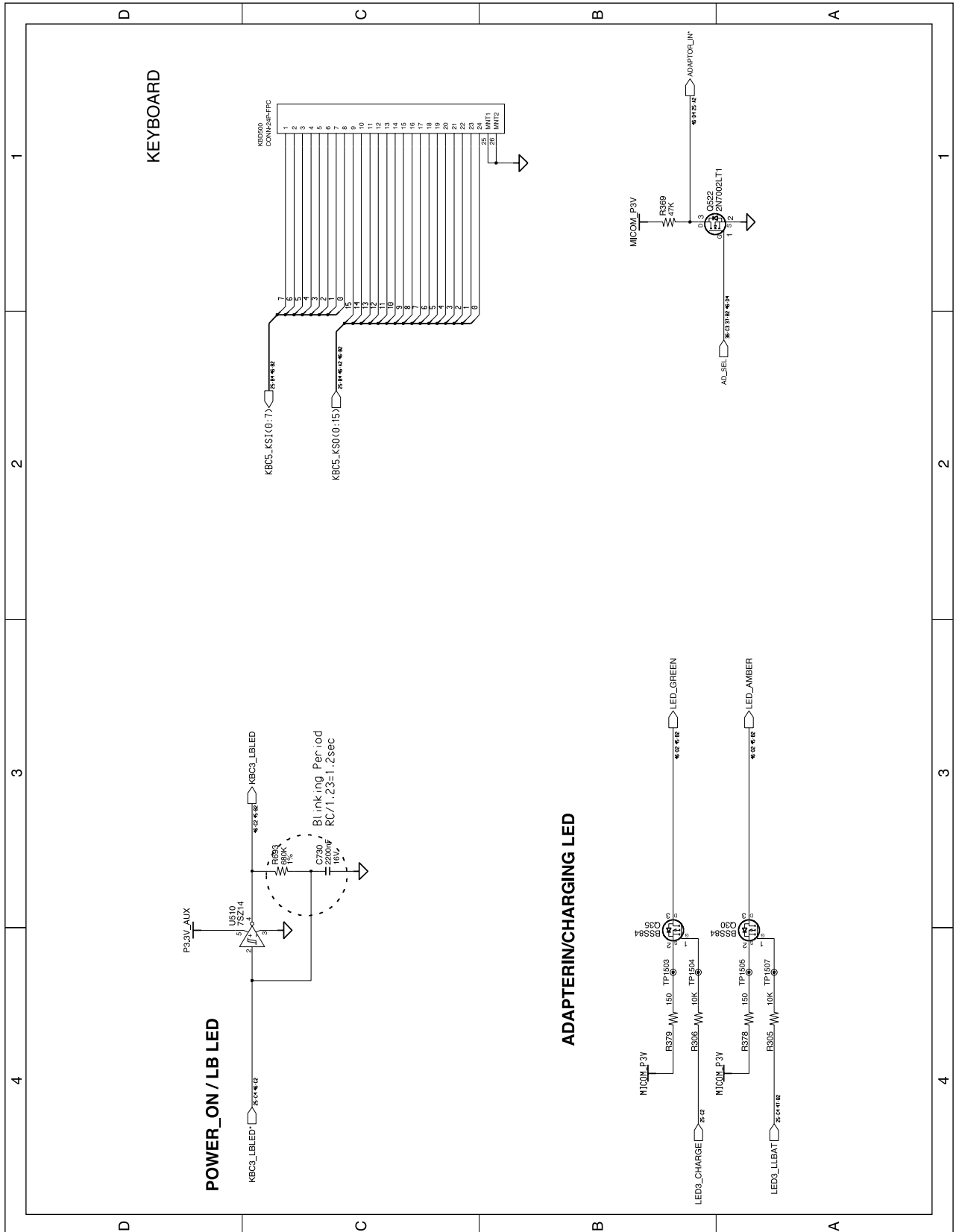
3-1-1(dd) Main Board Schematic Sheet 31 of 47(CF Socket)



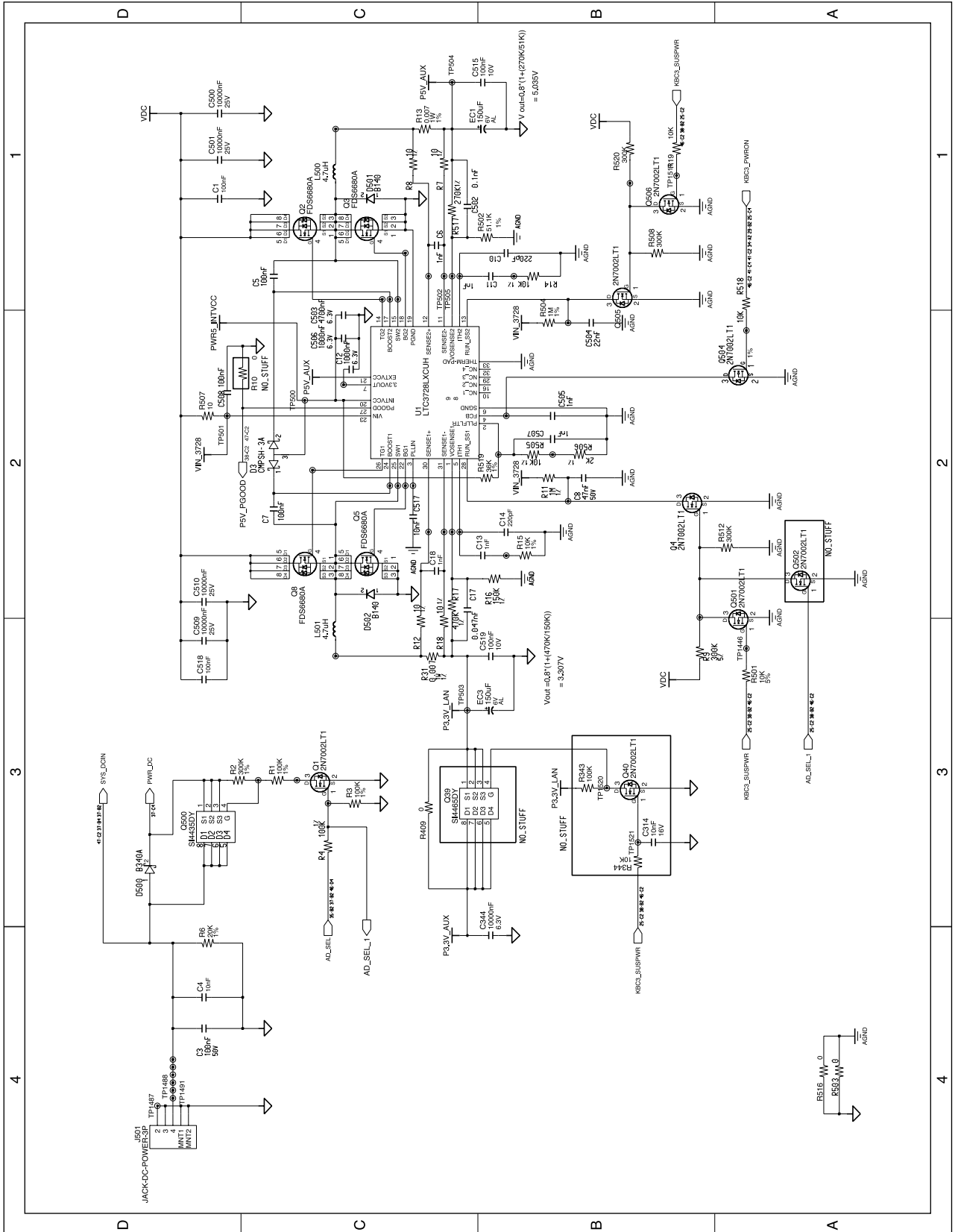
3-1-1(gg) Main Board Schematic Sheet 34 of 47(DMB & 1394 Port)



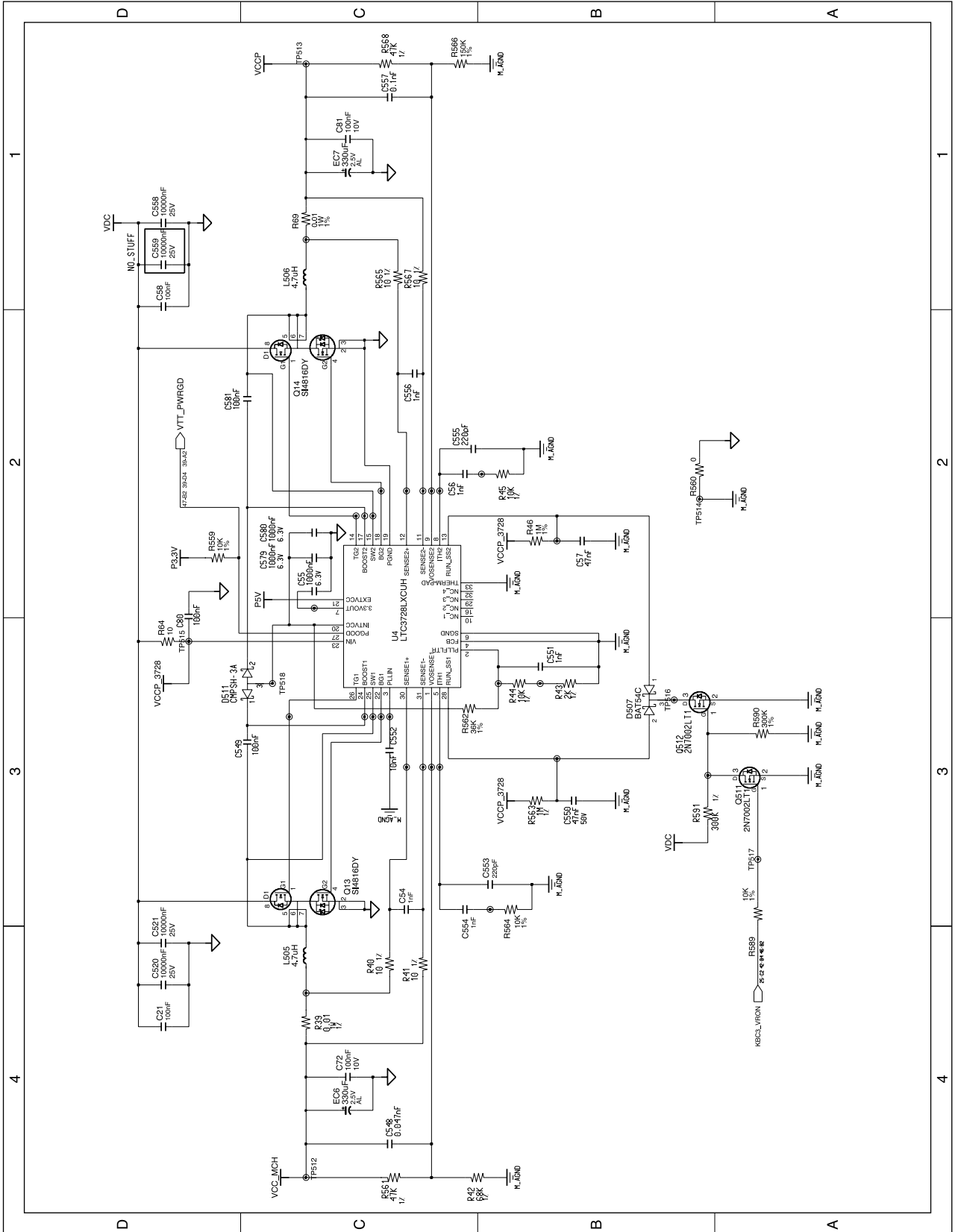
3-1-1(hh) Main Board Schematic Sheet 35 of 47(Keyboard Connector)



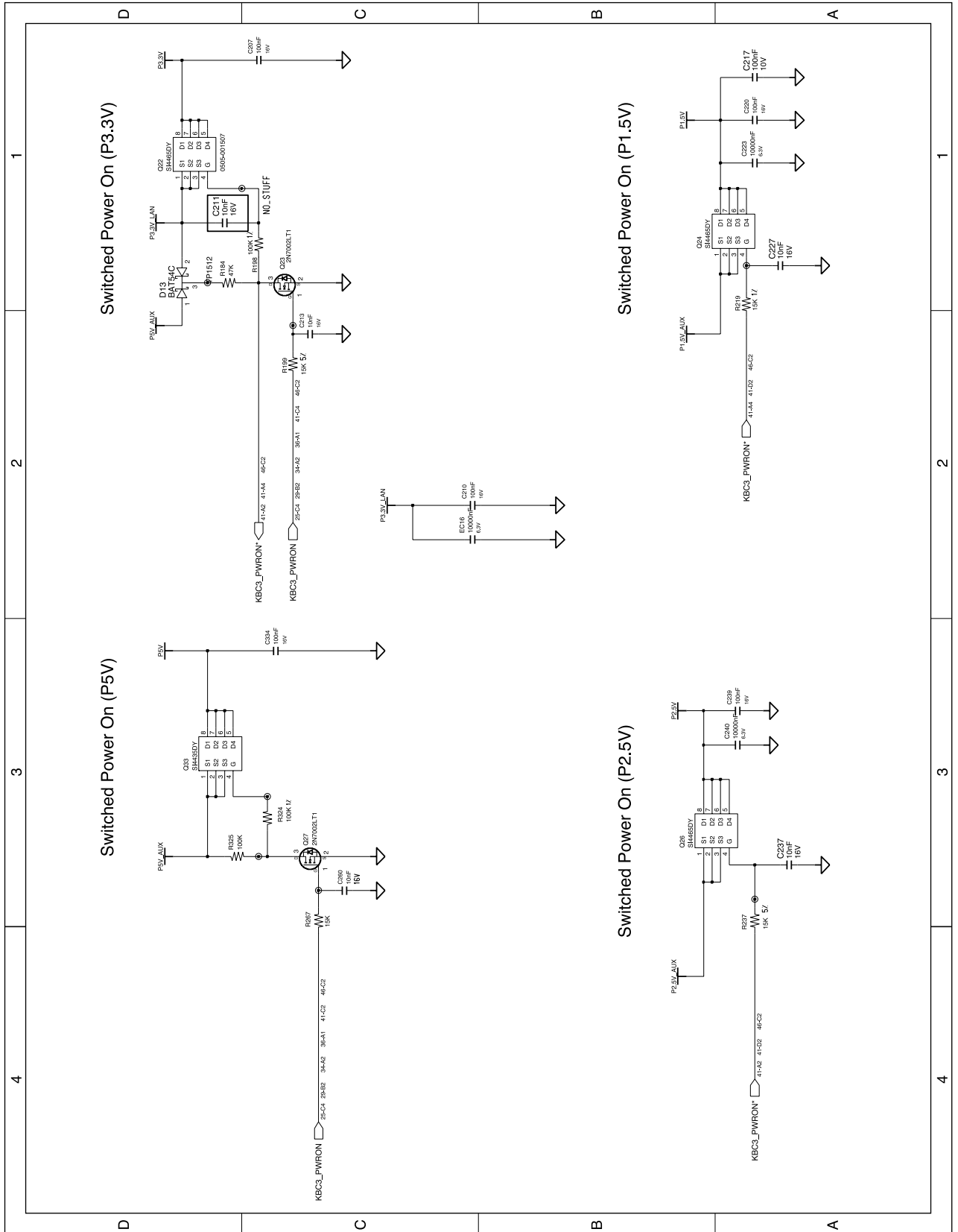
3-1-1(ii) Main Board Schematic Sheet 36 of 47(DC/DC Power)



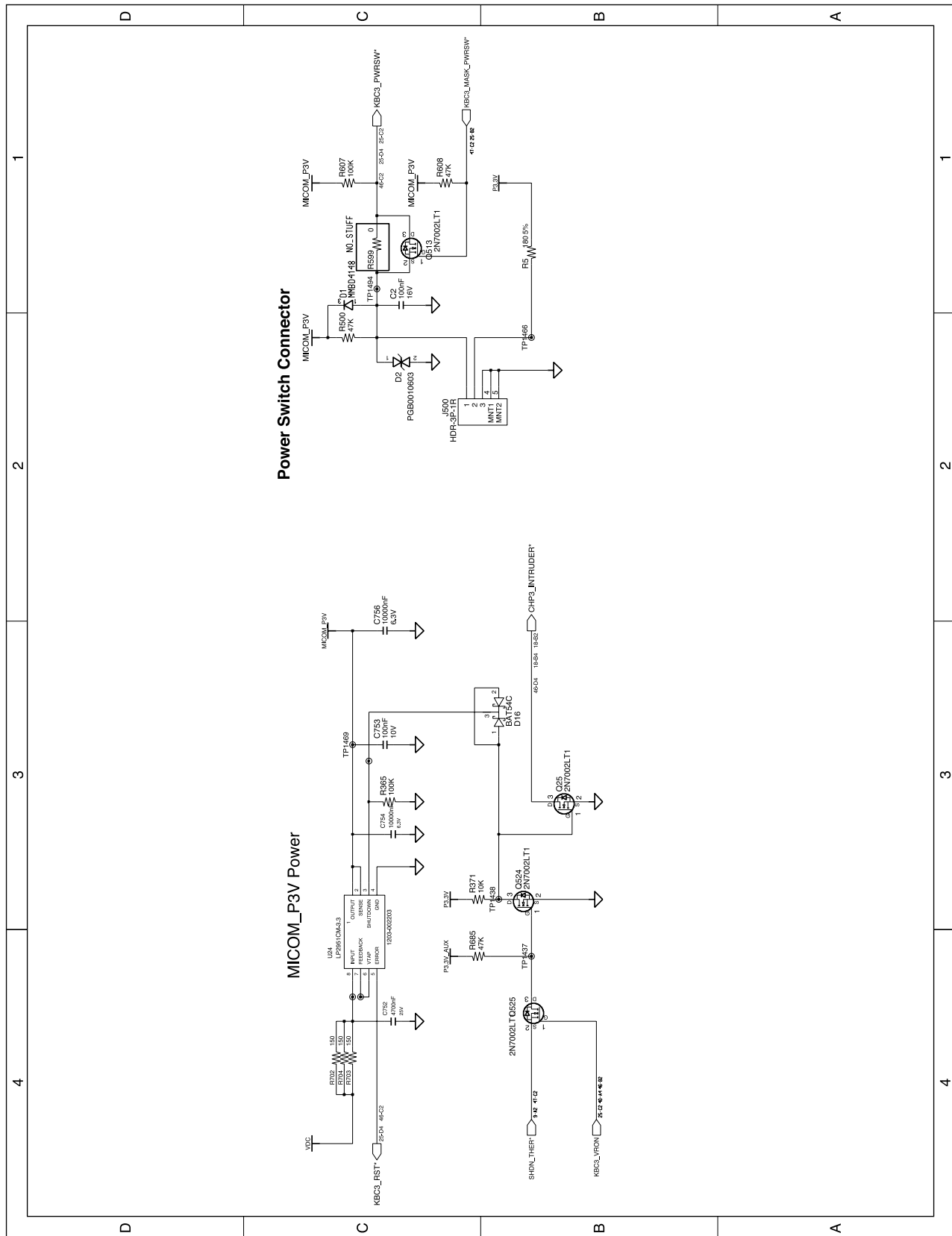
3-1-1(mm) Main Board Schematic Sheet 40 of 47(VCCP & GMCH Power)



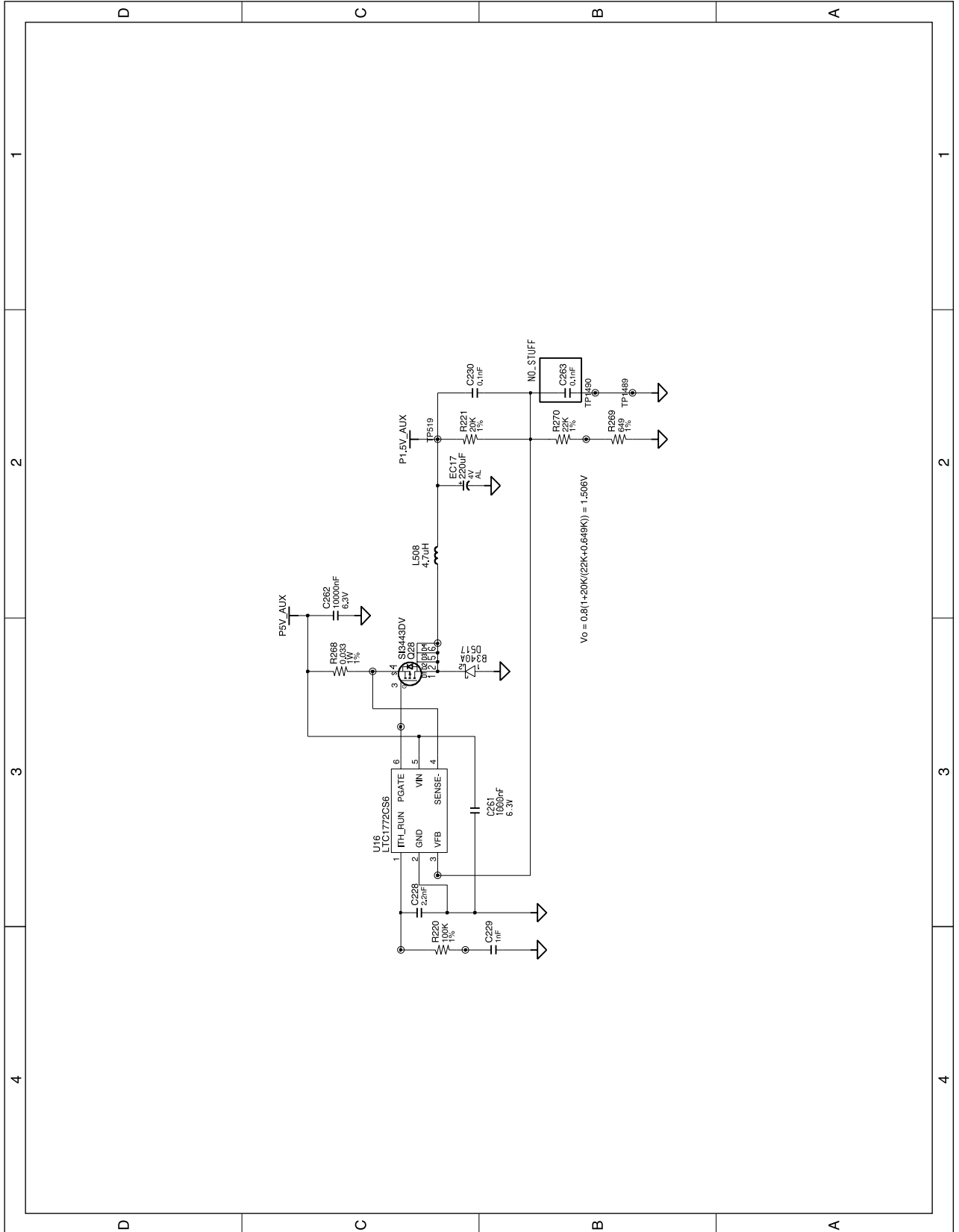
3-1-1(nn) Main Board Schematic Sheet 41 of 47(Switched Power)



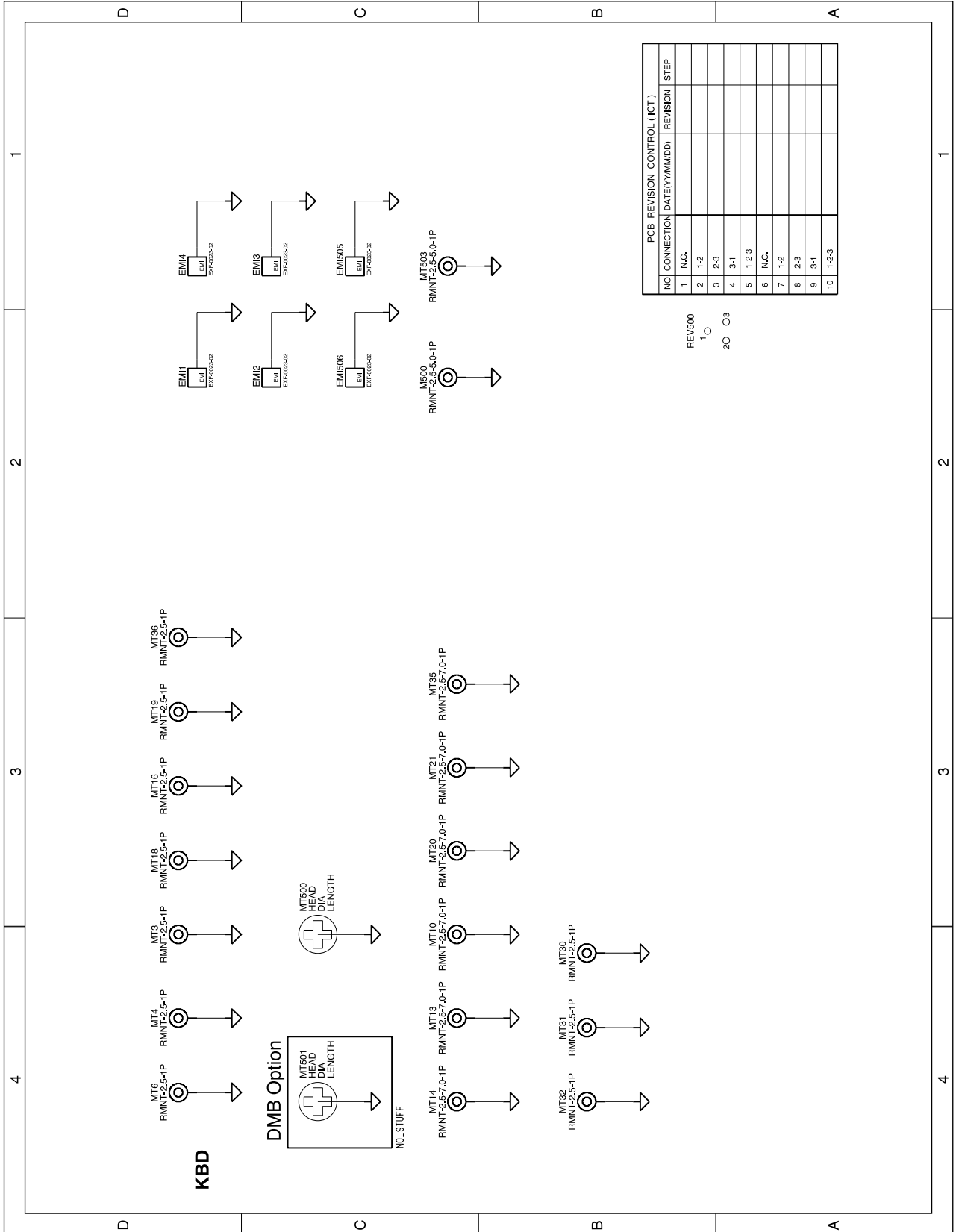
3-1-1(o) Main Board Schematic Sheet 42 of 47(MICOM Power & Power SW)



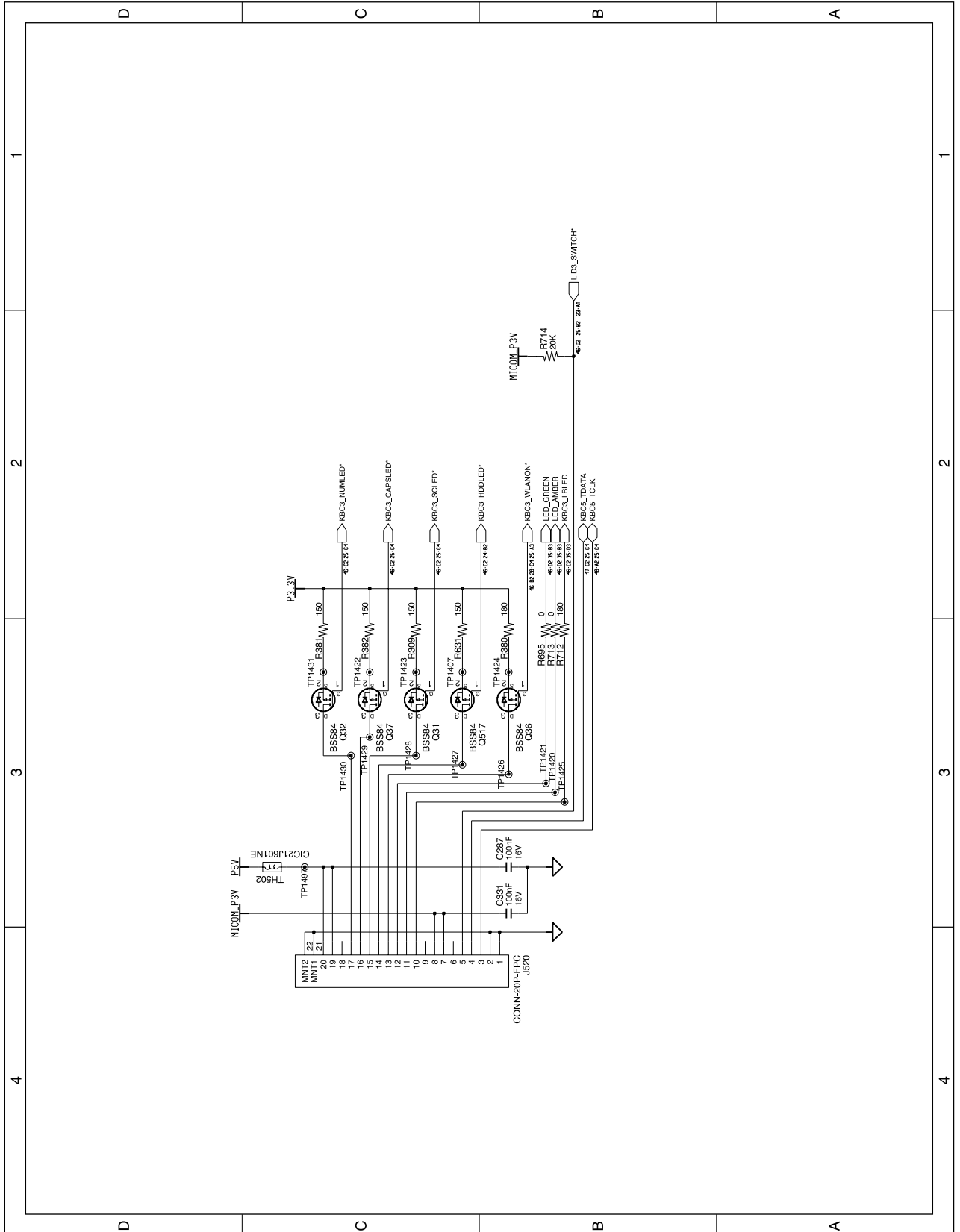
3-1-1(pp) Main Board Schematic Sheet 43 of 47(Always Power)



3-1-1(qq) Main Board Schematic Sheet 44 of 47(Mount Hole)



3-1-1(rr) Main Board Schematic Sheet 45 of 47(Sub-Board Connector)



3-1-1(ss) Main Board Schematic Sheet 46 of 47(TP)

D	C	B	A
1	2	3	4
2	3	4	1
3	4	1	2
4	1	2	3
D	C	B	A
1	2	3	4

3-1-1(tt) Main Board Schematic Sheet 47 of 47(TP)

