FIRENZE II

CPU : Intel Yonah (533/667MHz)
Chip Set : RC410MD & SB450
Remarks : Mobility Platform

Model Name : FIRENZE II
PBA Name : MAIN
PCB Code : GCE : BA41-00659A
TPT : BA41-00671A
Dev. Step : PRR
Revision : X03
T.R. Date : 2006.03.30

DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

■ ***Owner : SEC Mobile R & D*** ***Signature :*** ***X***

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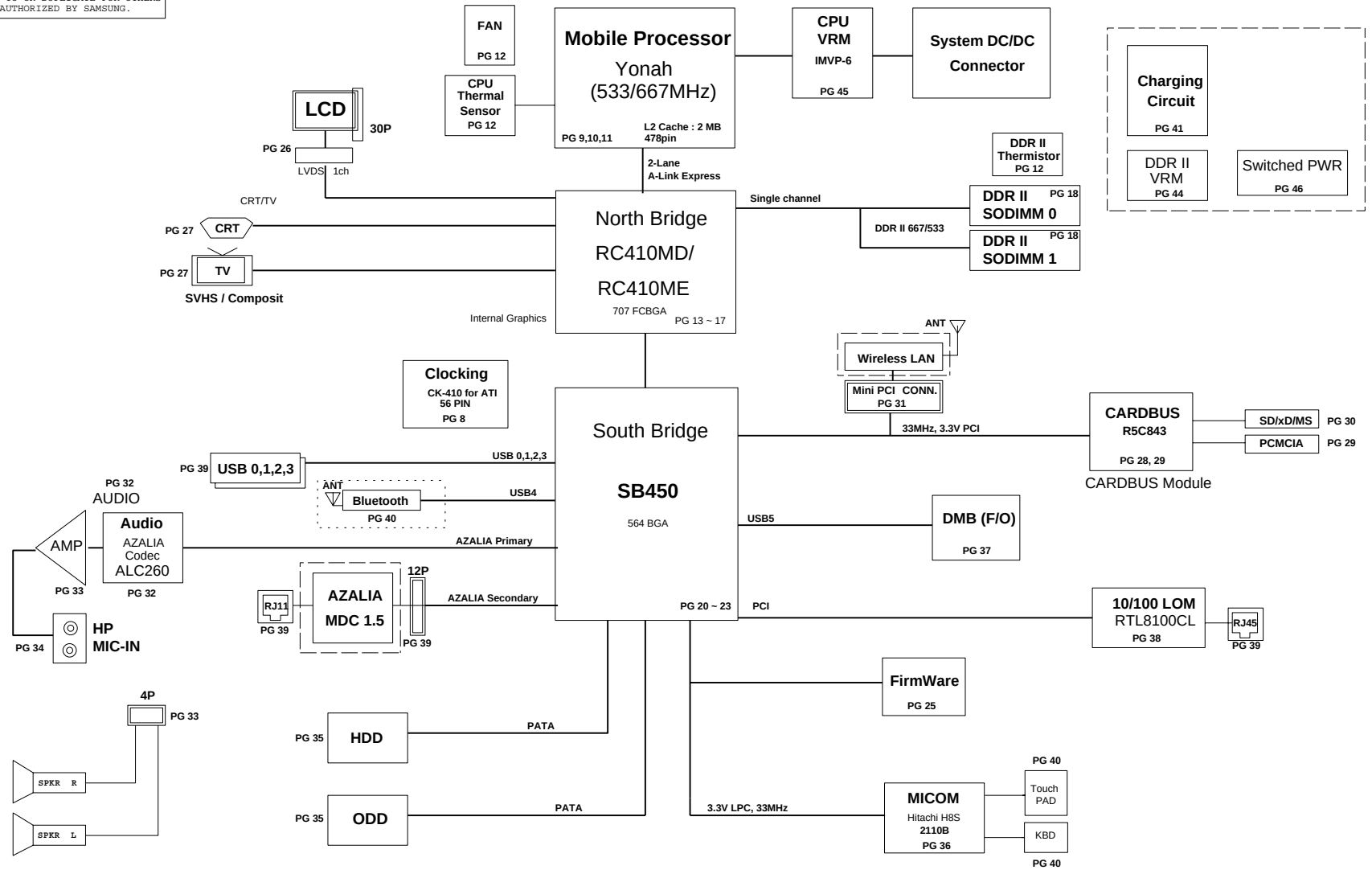
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II COVER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 1 OF 52	



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
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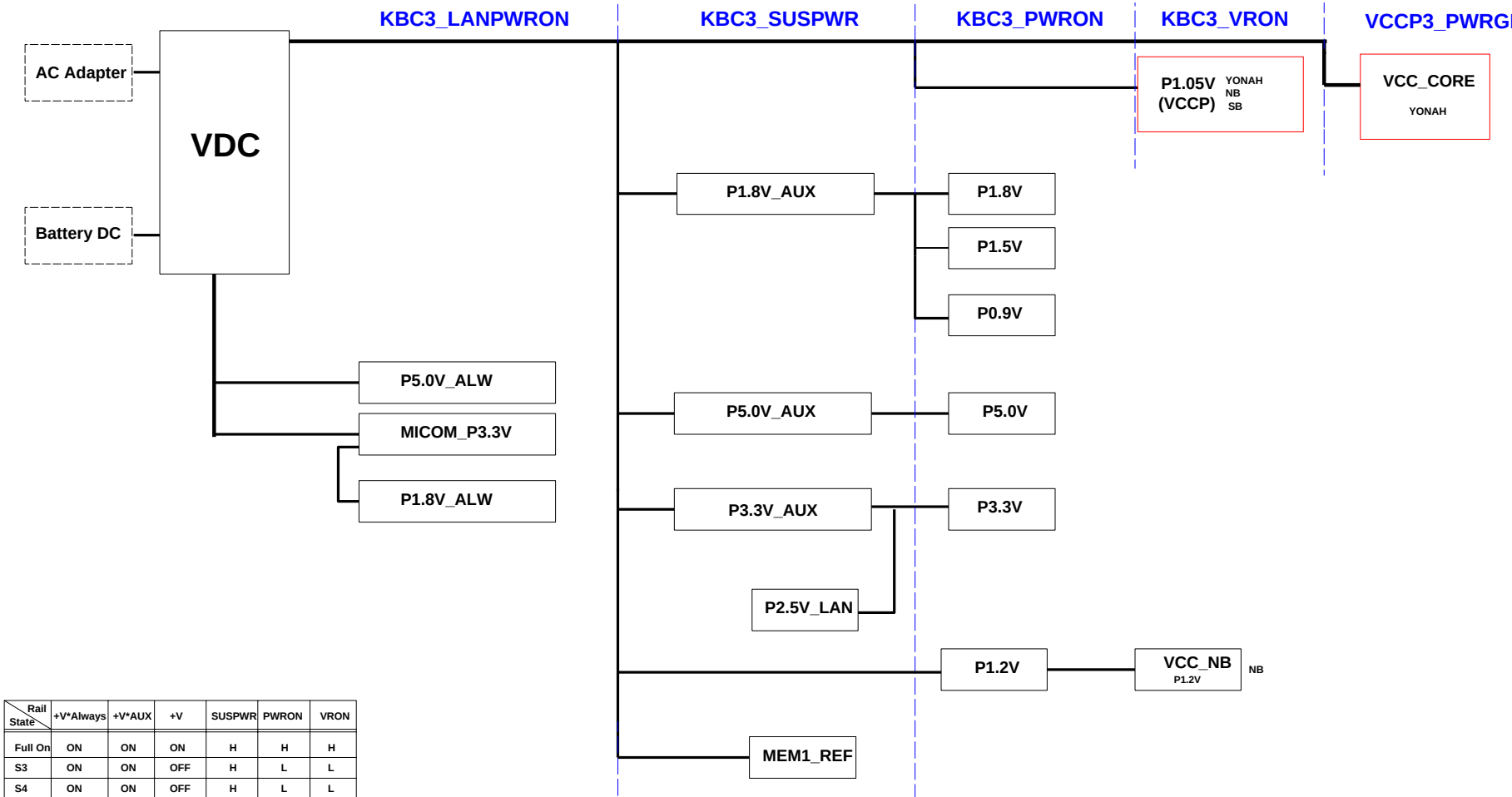
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
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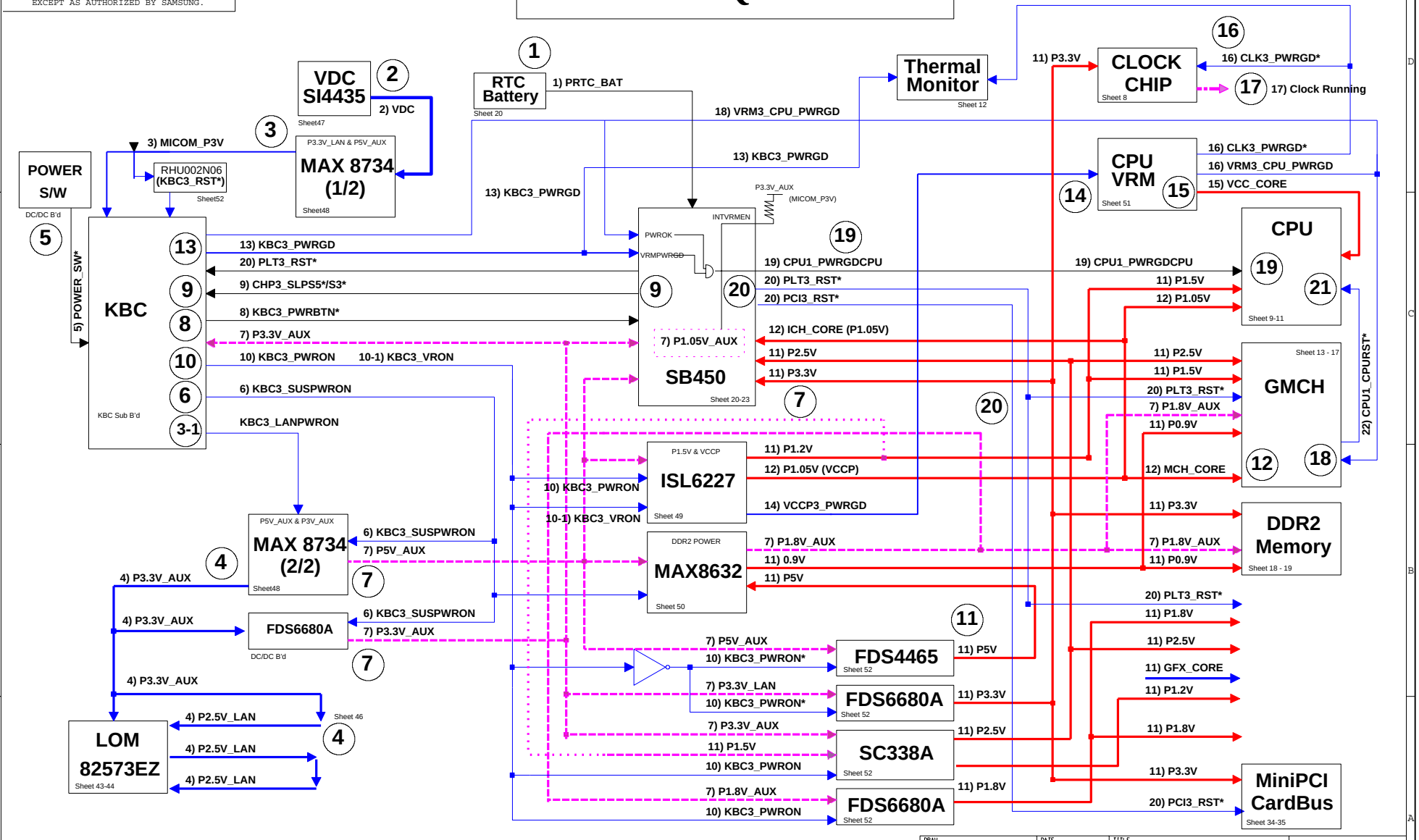
POWER SEQUENCE Rev. 0.8



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CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0	POWER SEQUENCE	PART NO.: BA41-00659A
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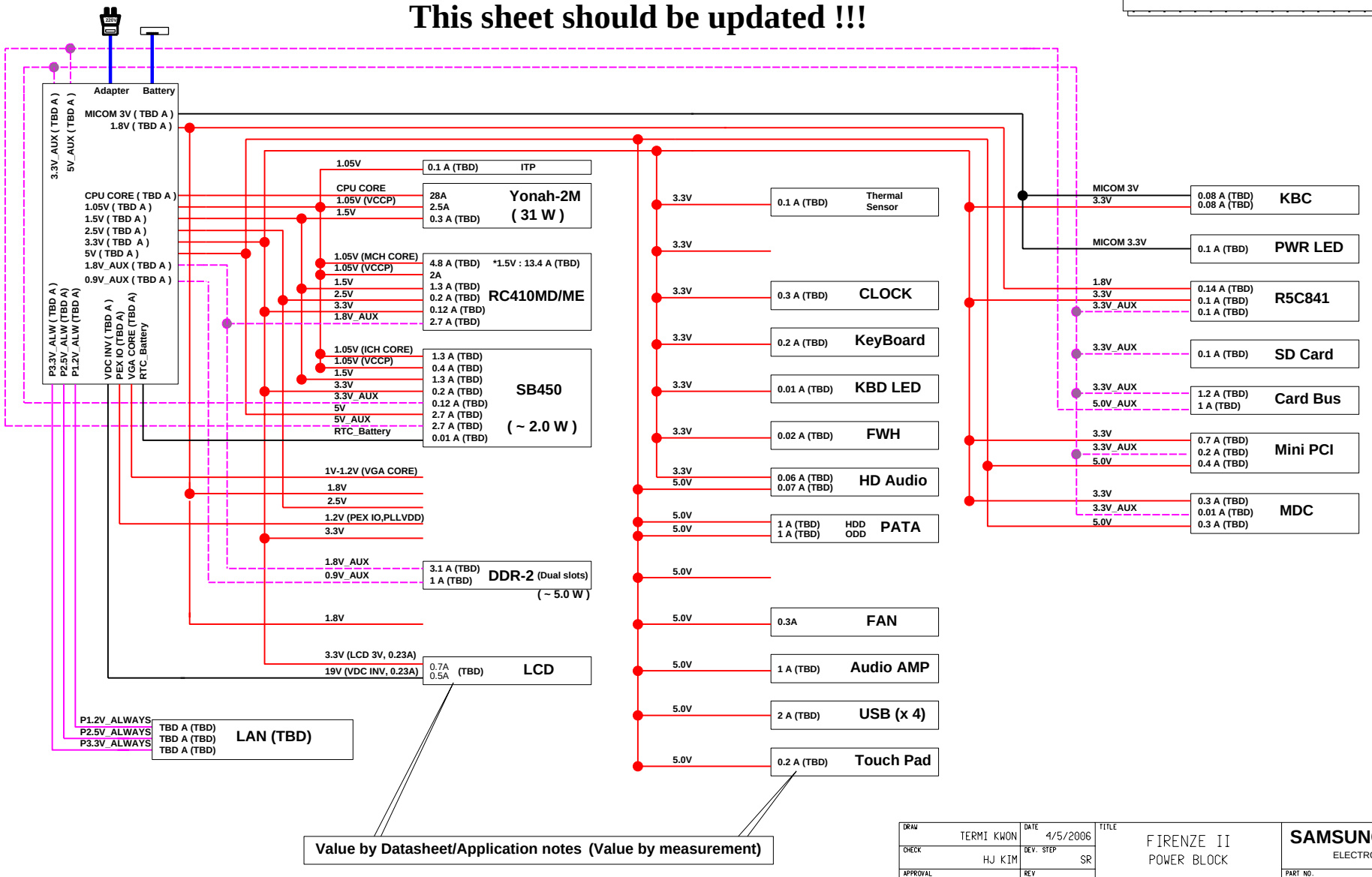
POWER RAILS ANALYSIS Rev. 0.8

S0 - S5
S0 - S3
OFF IN S3 - S5

This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II POWER BLOCK	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
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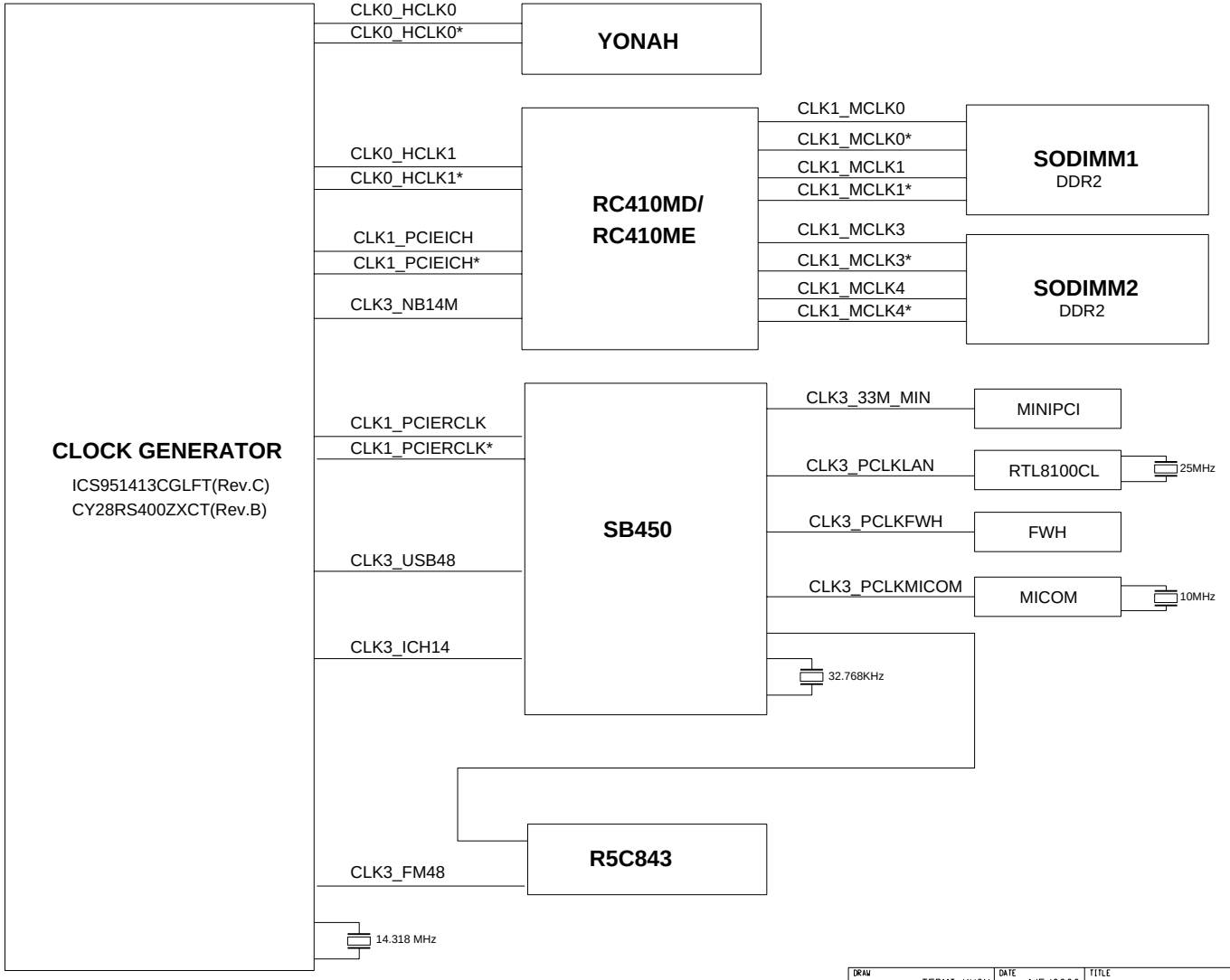

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	C
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
			-
			-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V)
	MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

2

I C / SMB Address

Devices	Address	Hex	Bus
SB450	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB450	Real Time Clock
Crystal	10MHz	MICOM	H8S-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 **1** **1**	1.596 V	**1** 0 0 **1** **1** 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V Lowest Freq.
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 **1** 0 1 **1** **1**	1.340 V	**1** **1** 0 **1** **1** 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

HFM Voltage
770:1.26V->1.372V
730,740,750,760:1.26->1.356V

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
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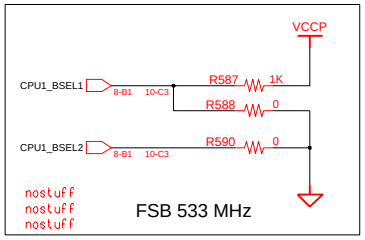
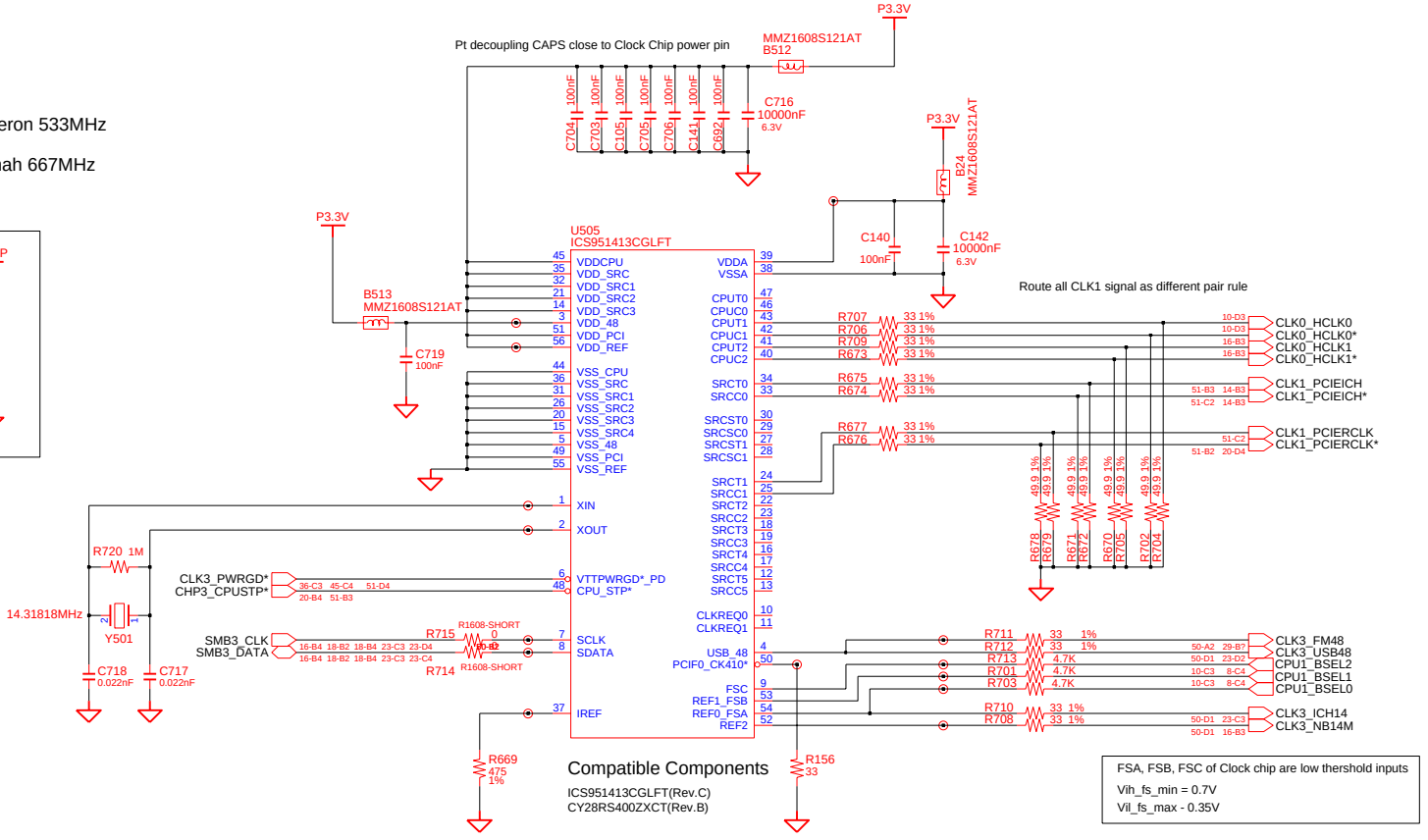
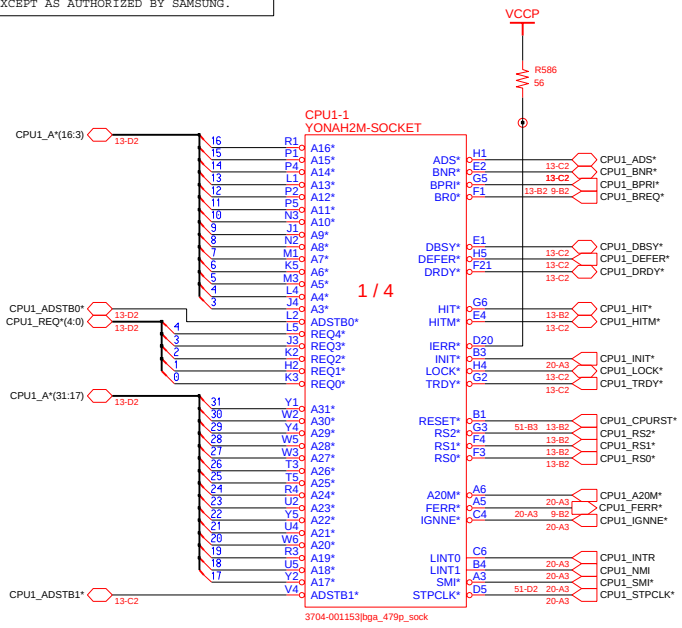
CPU FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK	
0	0	0	266 MHz	
0	0	1	333 MHz	
0	1	0	200 MHz	
0	1	1	400 MHz	
1	0	0	133 MHz	Celeron 533MHz
1	0	1	100 MHz	
1	1	0	166 MHz	Yonah 667MHz
1	1	1	RSVD	

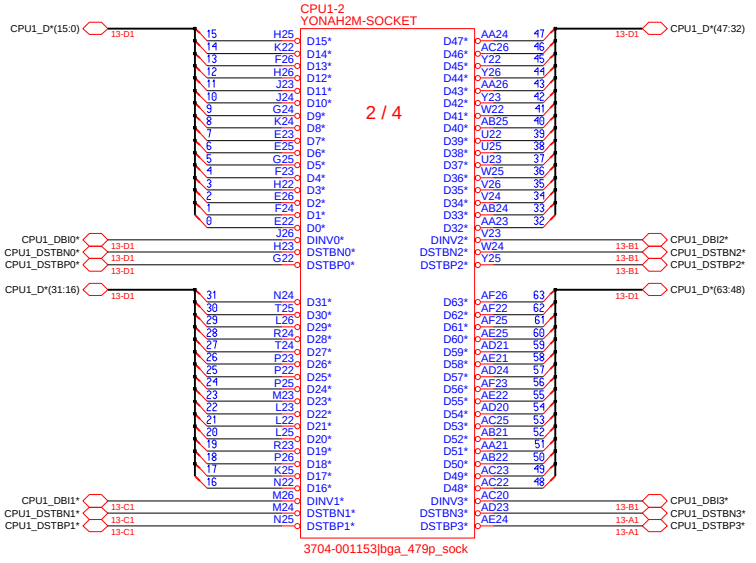




Place all te serias termination resistor as close as Clock Chip as possible

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 8 OF 52	





**NOTE

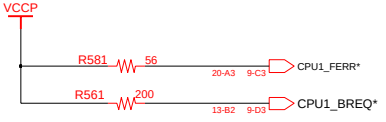
RHE SUPPORTER

MT504 RMNT-38-70-1P

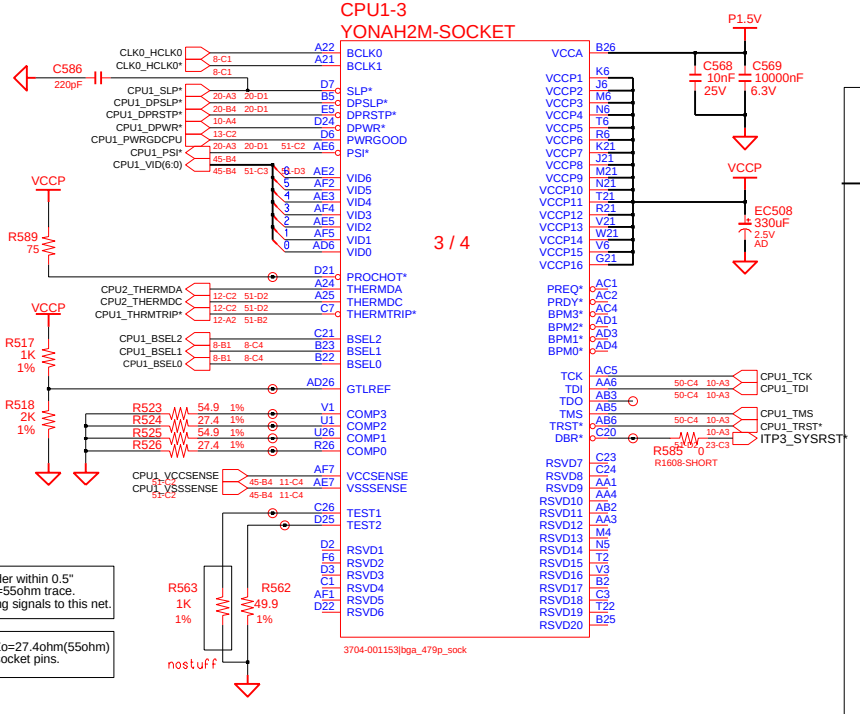
MT508 RMNT-38-70-1P

MT505 RMNT-38-70-1P

MT507 RMNT-38-70-1P



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 9 OF 52	



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table

IMVP-6

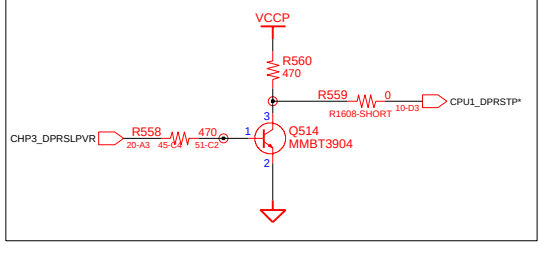
Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

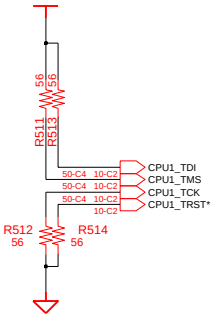
*"1111111" : 0V power good asserted.

Active		Deeper Slp	
DPRSLPVR	0	DPRSLPVR	1
DPRSTP*	1	DPRSTP*	0
PSI2*	0 or 1	PSI2*	0 or 1

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

Check CPU Power Page (P46)& SB450(P20)



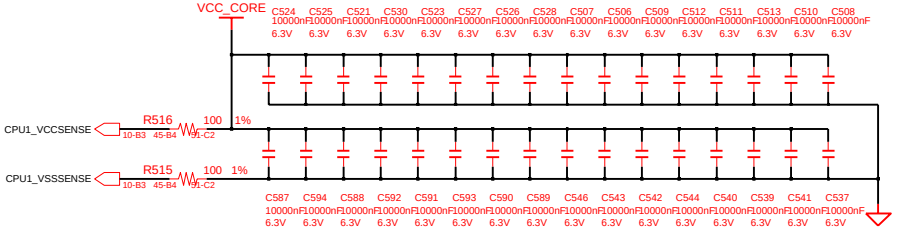


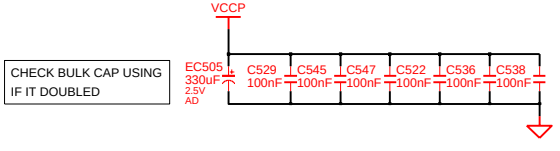
DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN YONAH CPU(2/3)
CHECK	HJ KIM	DEV. STEP	SR		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE		LAST EDIT	April 5, 2006 8:18:08 PM		

SAMSUNG ELECTRONICS

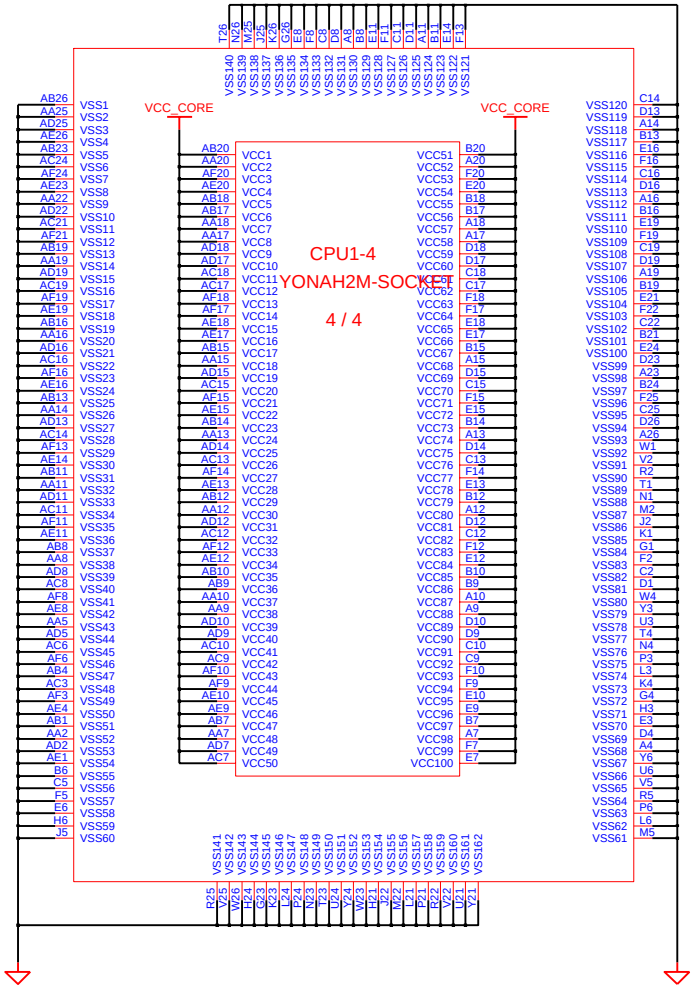
PART NO. BA41-00659A

D:/users/mobile62/mentor/firenze2/firenze2_SR1.0_0405





CHECK BULK CAP USING IF IT DOUBLED

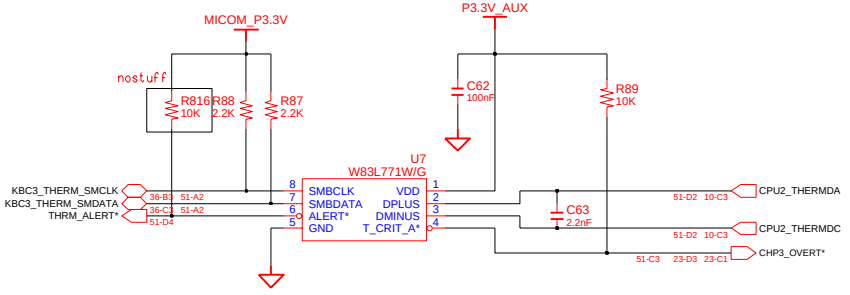


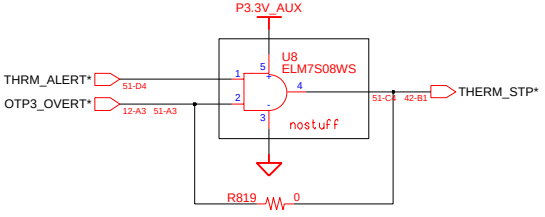
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN YONAH CPU(3/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 11 OF 52	

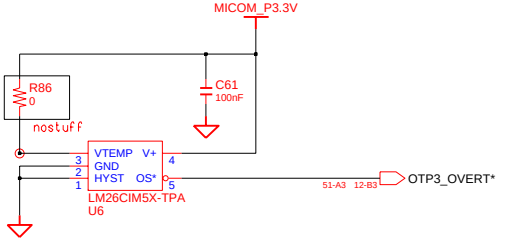
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

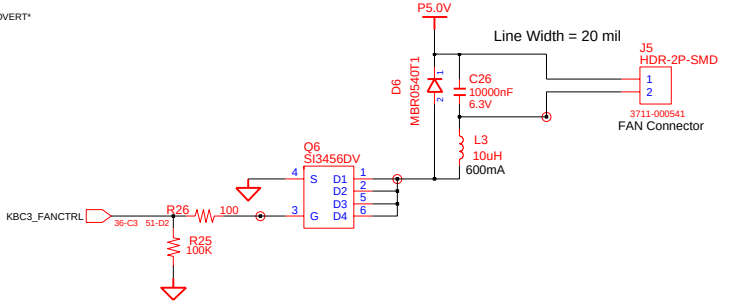
CPU Thermal Sensor

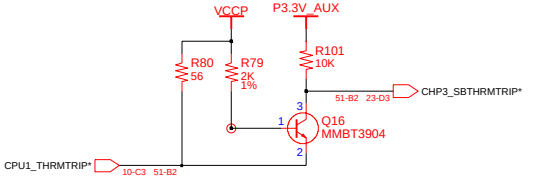






FAN Control Logic





DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN THERMAL SENSOR/FAN CONTRL	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 12 OF 52	

DUCT + FAN SUPPORTER

M1 HEAD DIA LENGTH

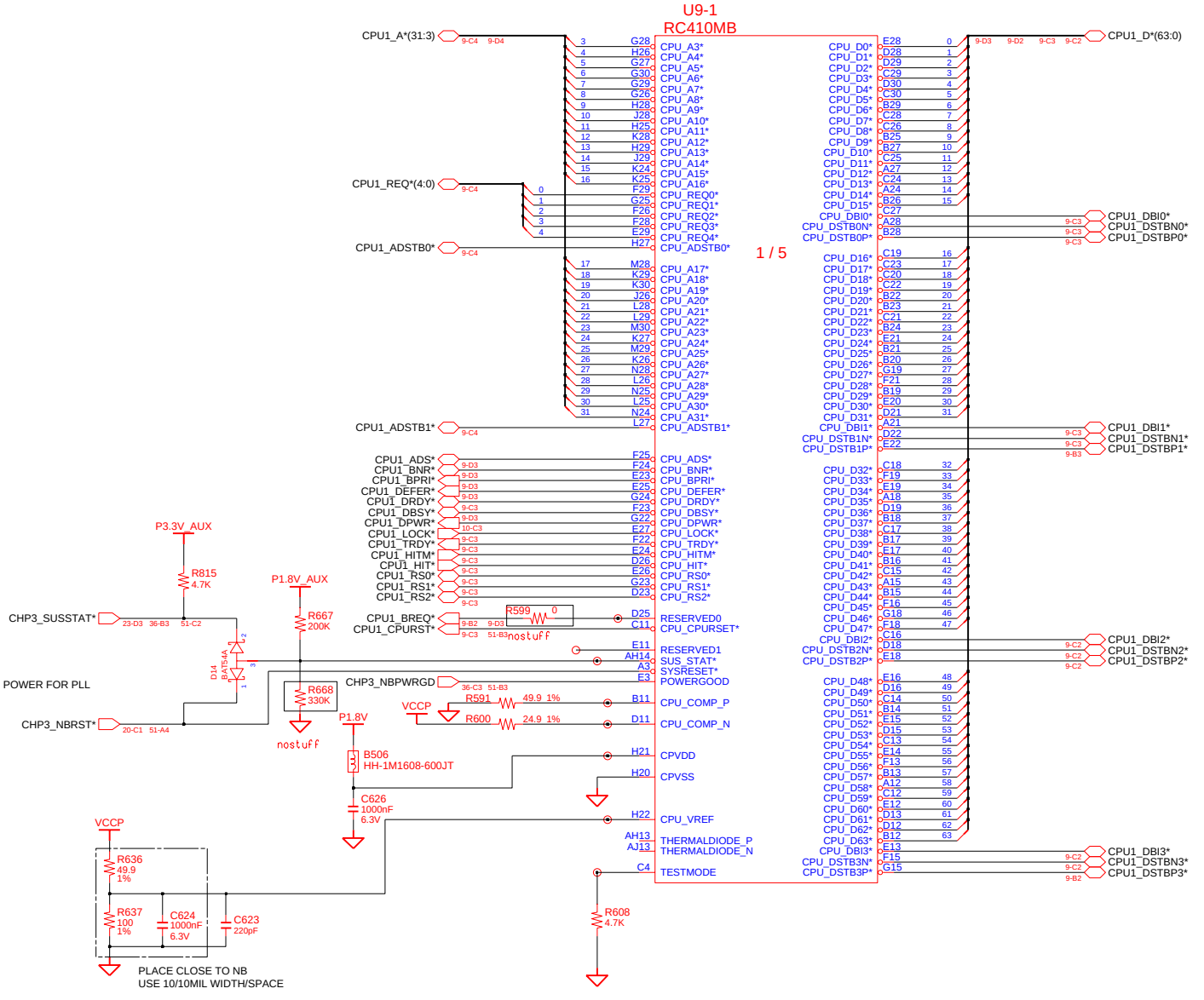
M503 HEAD DIA LENGTH

M500 HEAD DIA LENGTH

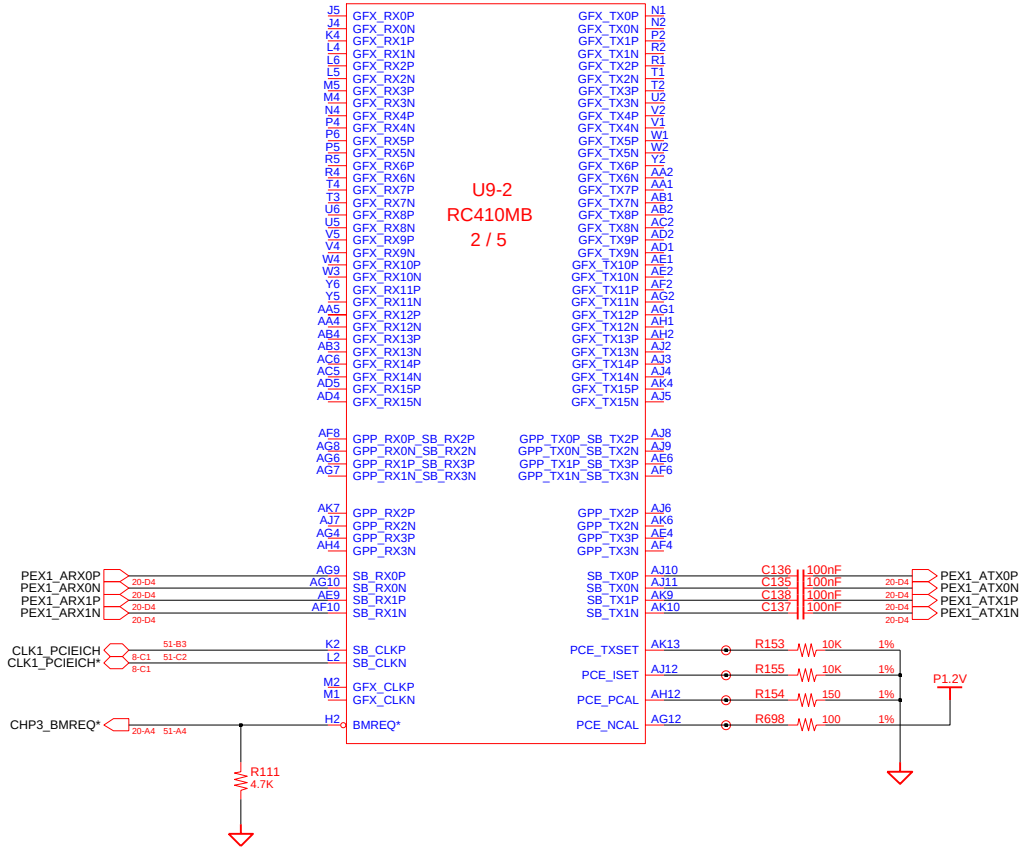
M4 HEAD DIA LENGTH

M3 HEAD DIA LENGTH

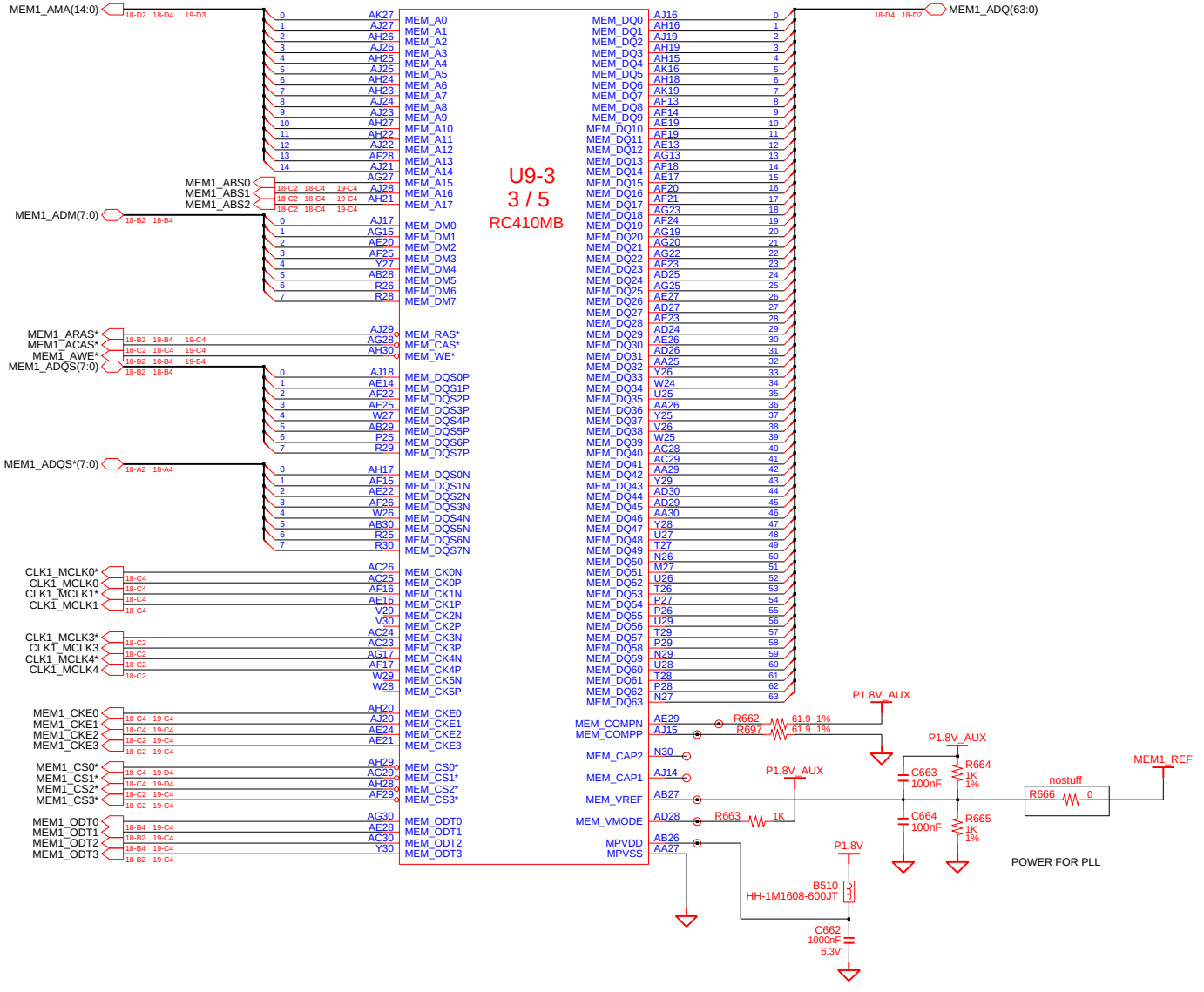
M502 HEAD DIA LENGTH



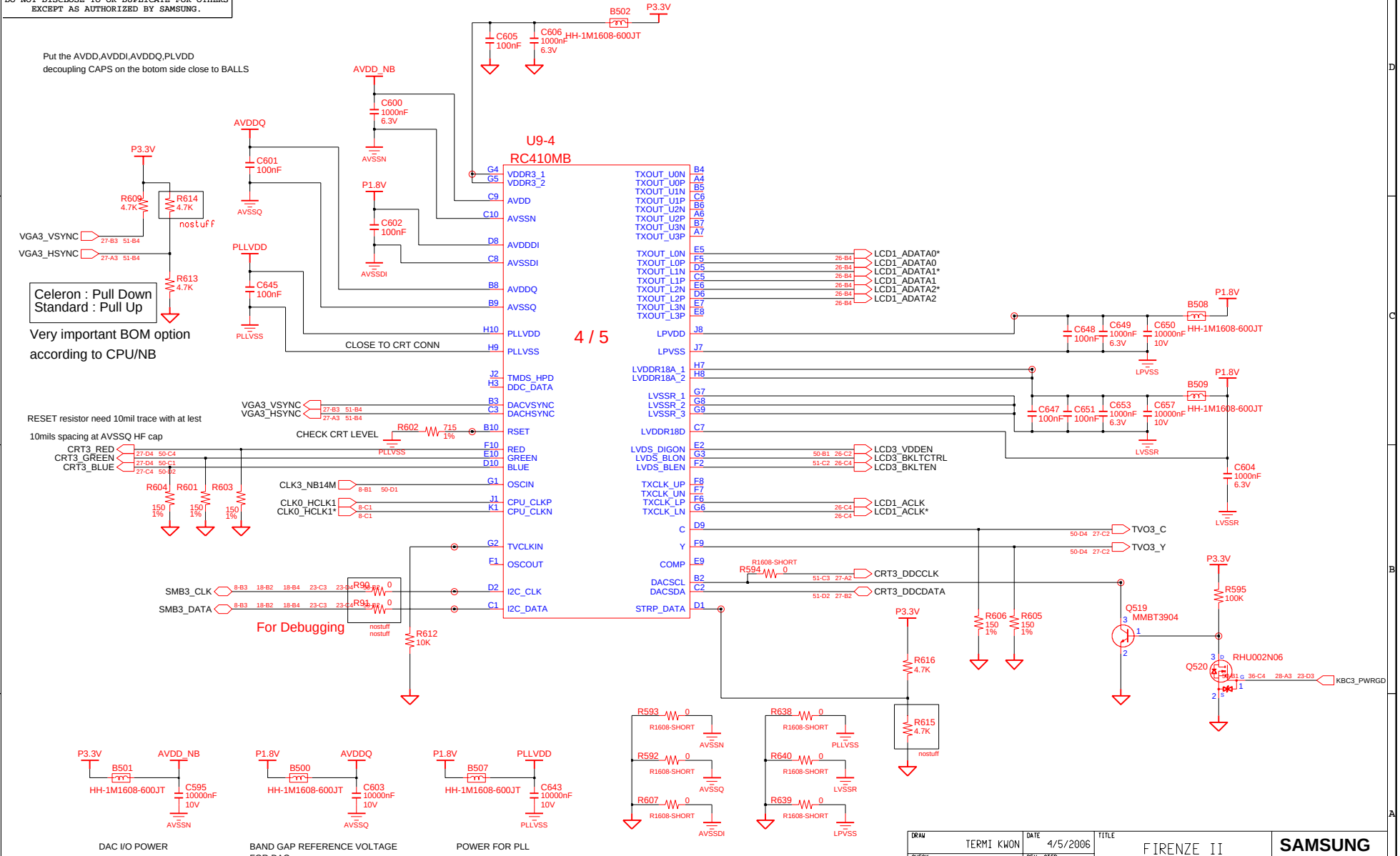
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN RC410MD(1/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 13 OF 52	



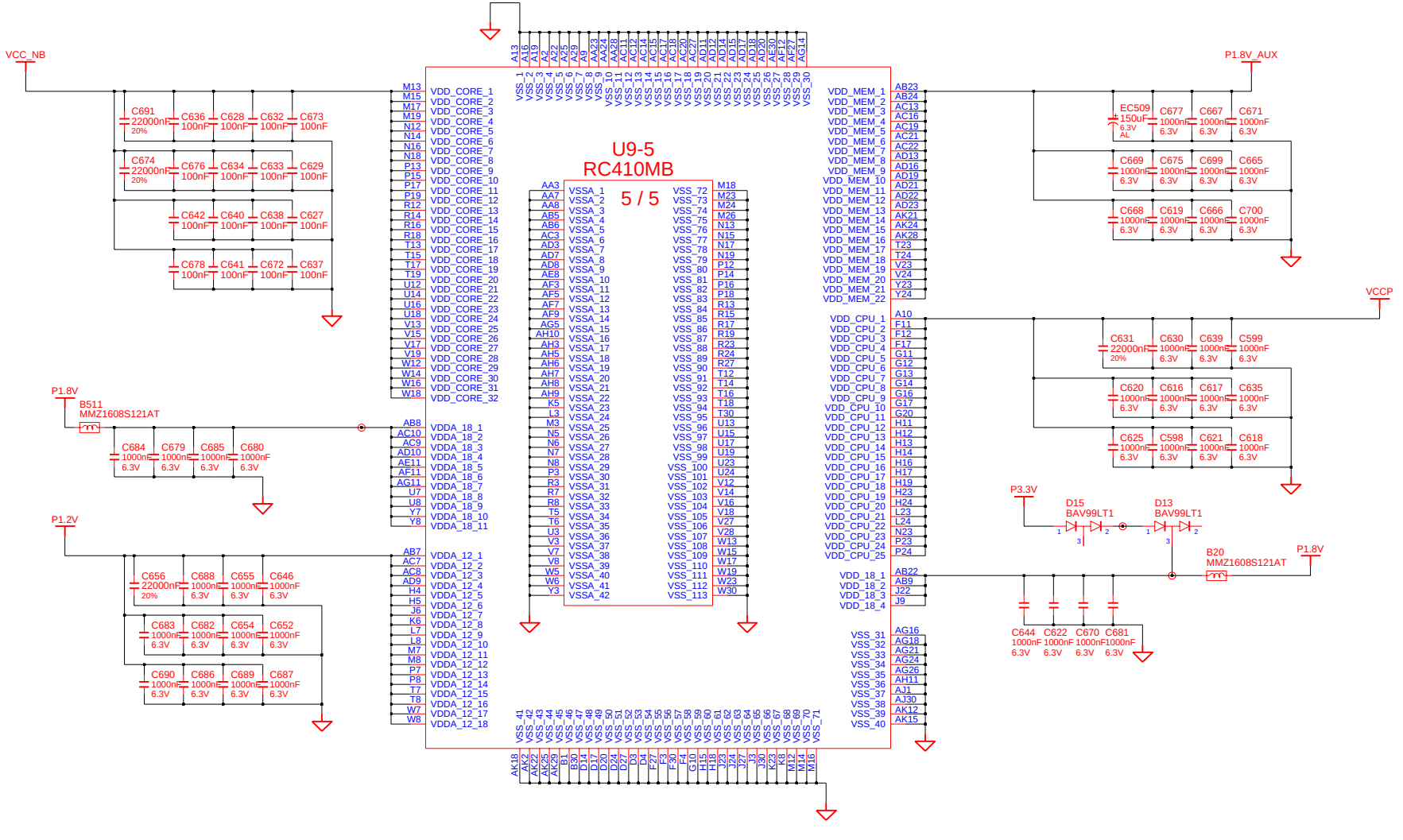
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN RC410MD(2/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 14 OF 52	



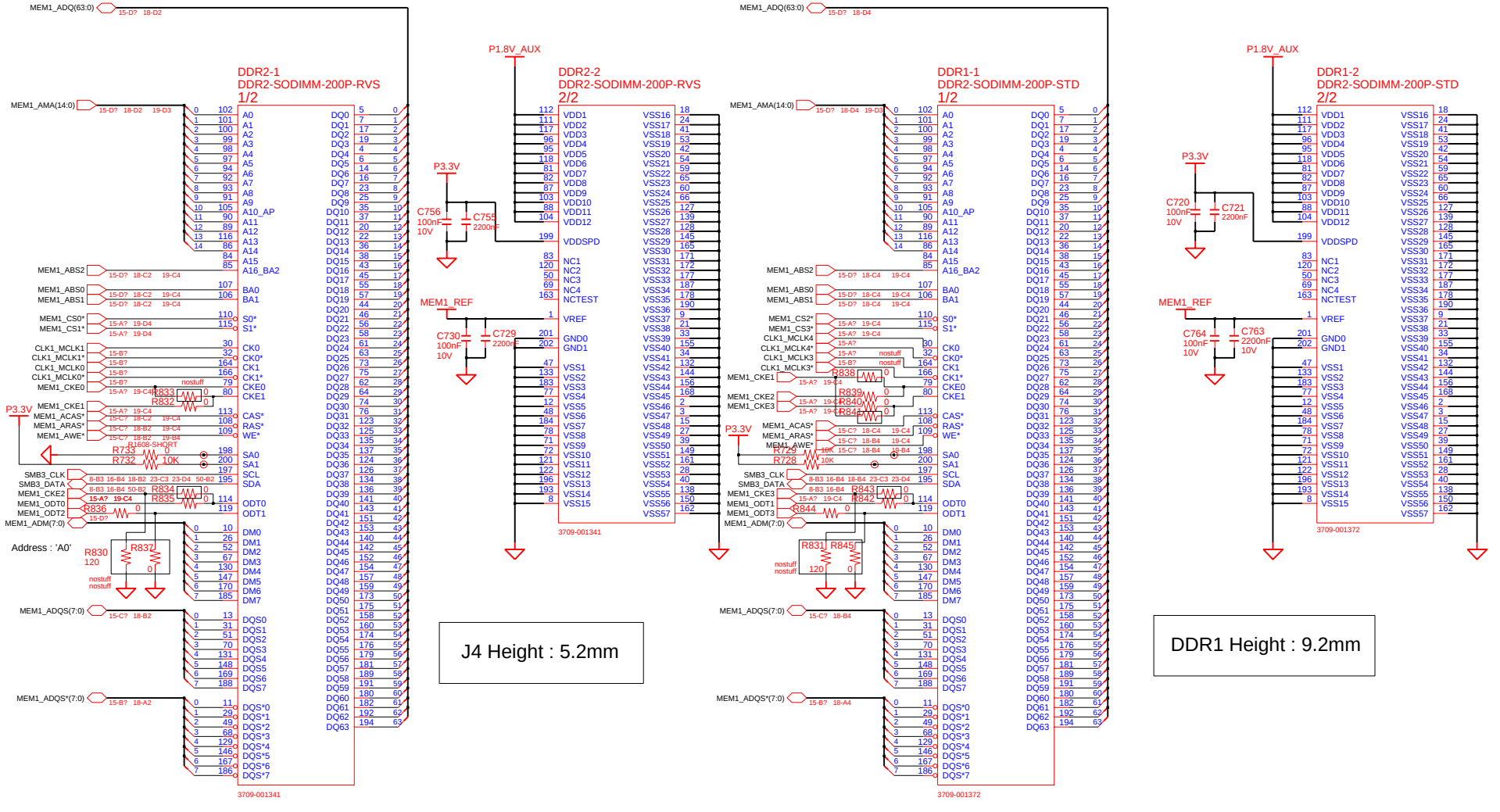
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN RC410MD(3/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 15 OF 52	



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN RC410MD(4/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 16 OF 52	



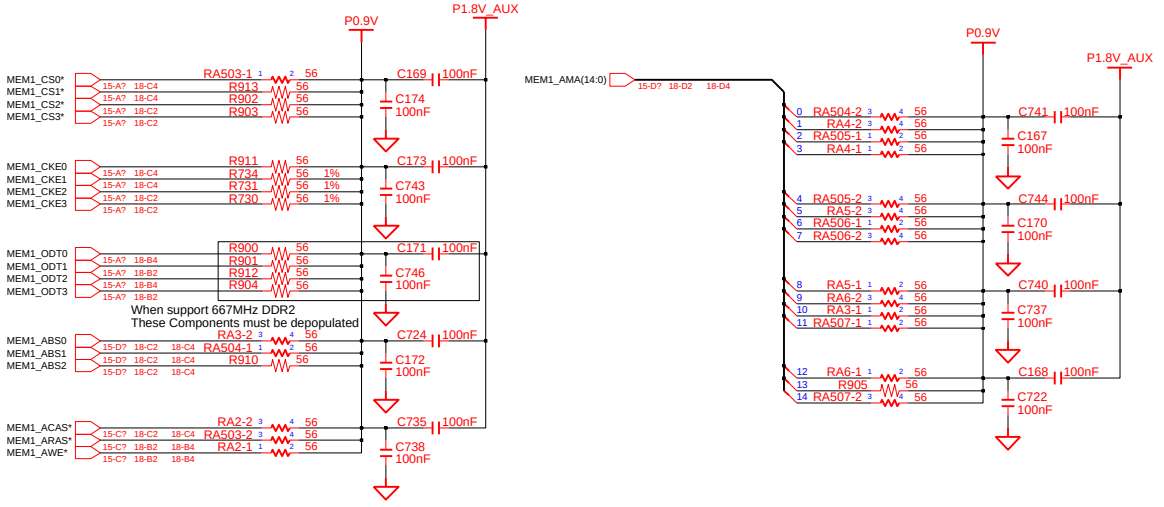
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN RC410MD(5/5)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 17 OF 52	



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II MAIN DDR2 - SODIMM
CHECK	HJ KIM	DEV. STEP	SR		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE		LAST EDIT	April 5, 2006 8:18:08 PM		

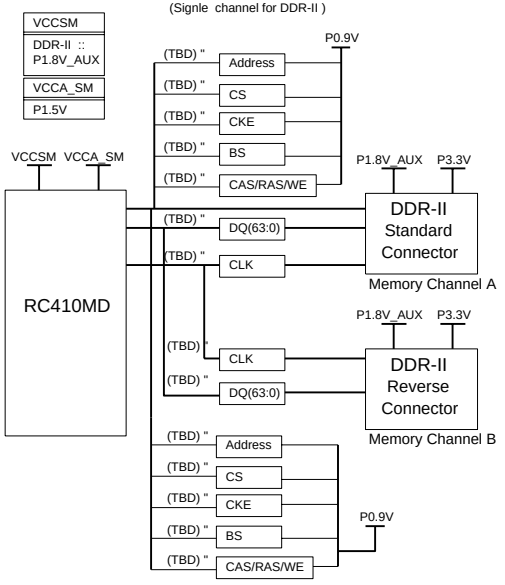
SAMSUNG ELECTRONICS

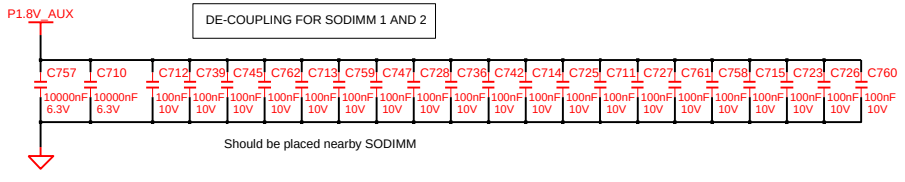
PART NO. BA41-00659A

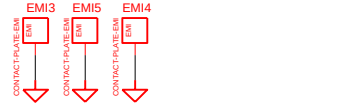


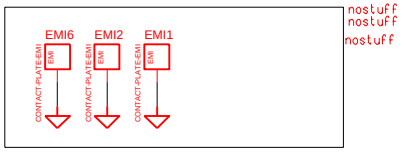
Memory Topology

(Signle channel for DDR-II)

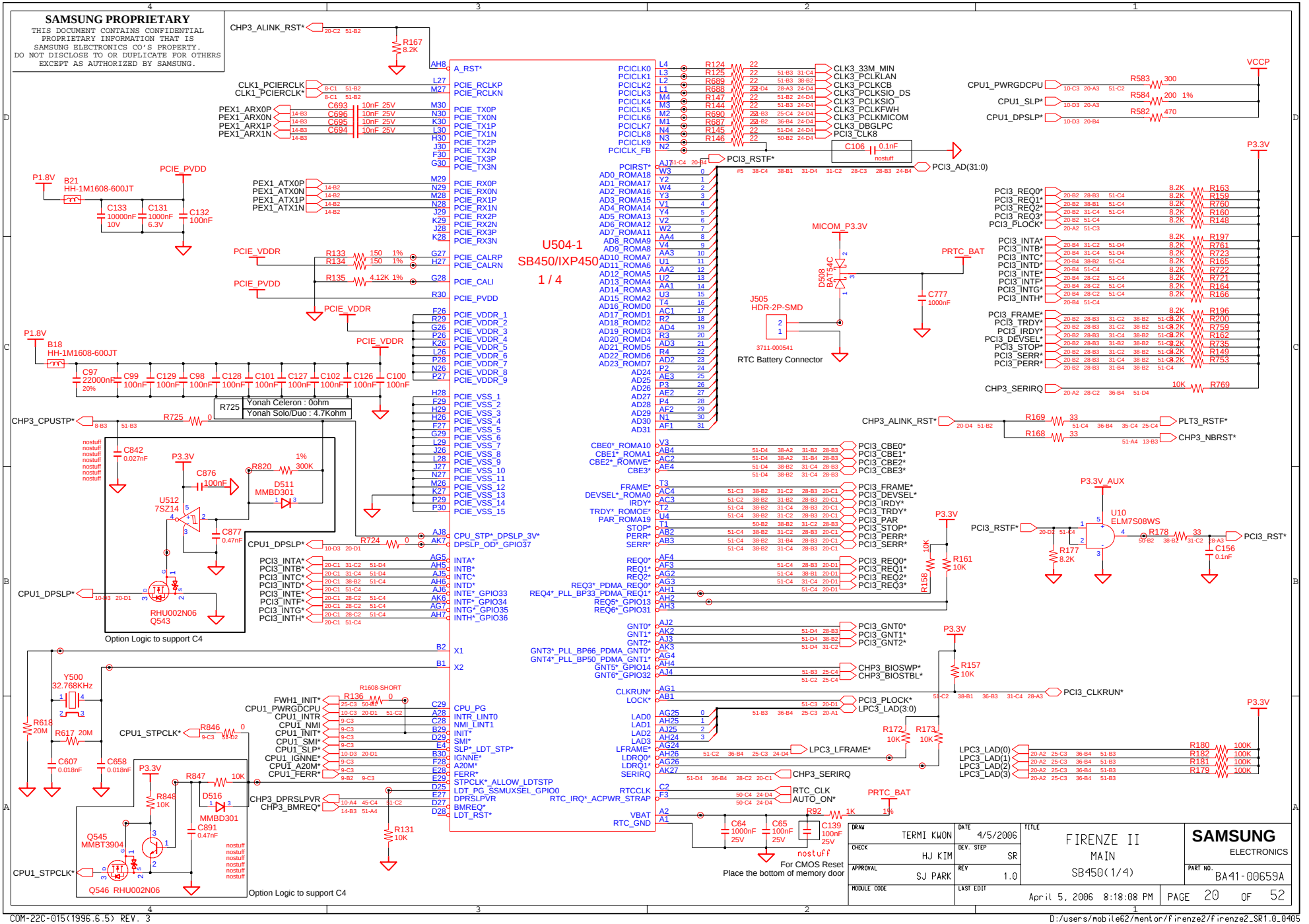








DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN DDR2 - TERMINATION	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 19 OF 52	



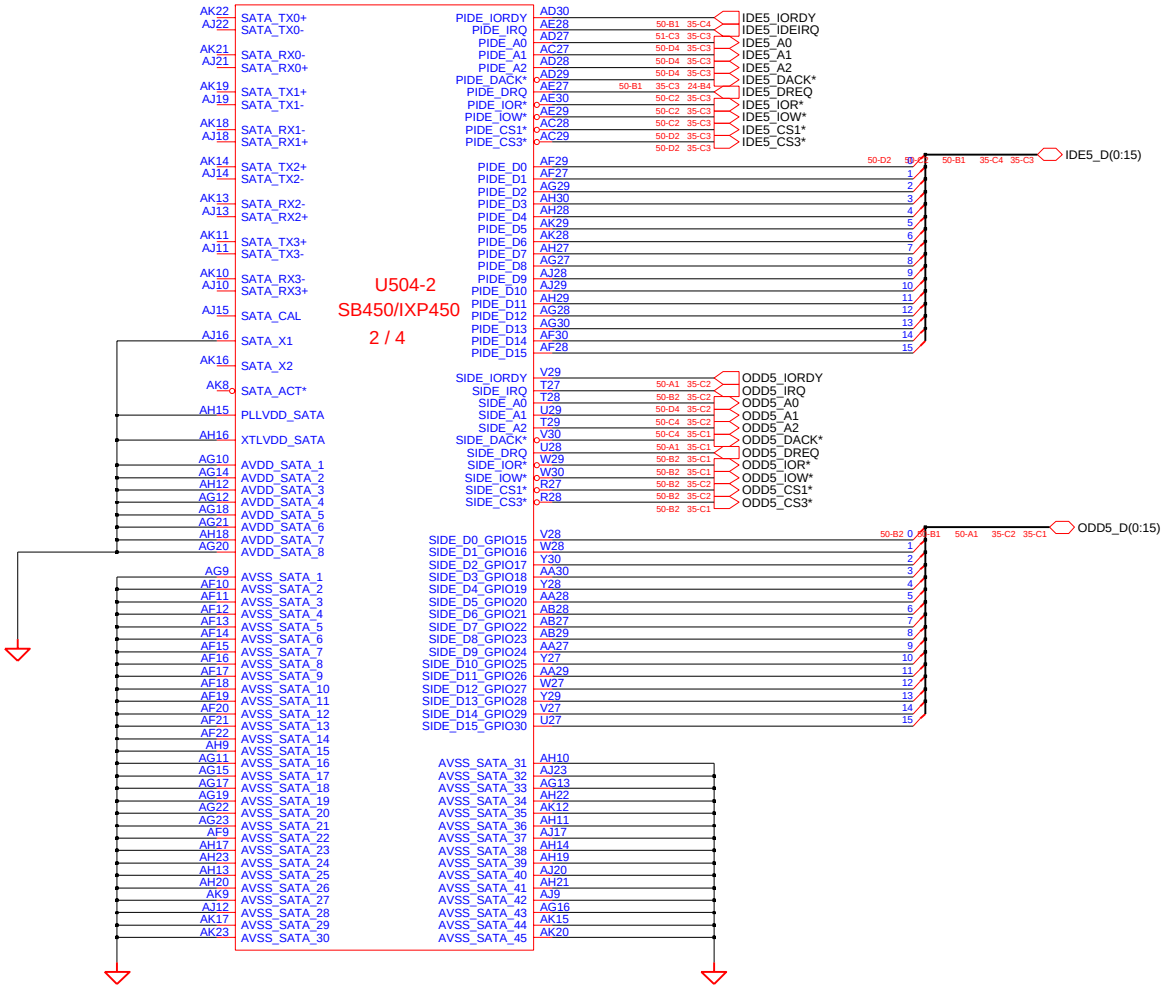
DRAW	TERMI KWON	DATE	4/5/2006
CHECK	HJ KIM	DEV. STEP	SR
APPROVAL	SJ PARK	REV	1.0
MODULE CODE		LAST EDIT	April 5, 2006 8:18:08 PM

TITLE: FIRENZE II MAIN SB450(1/4)

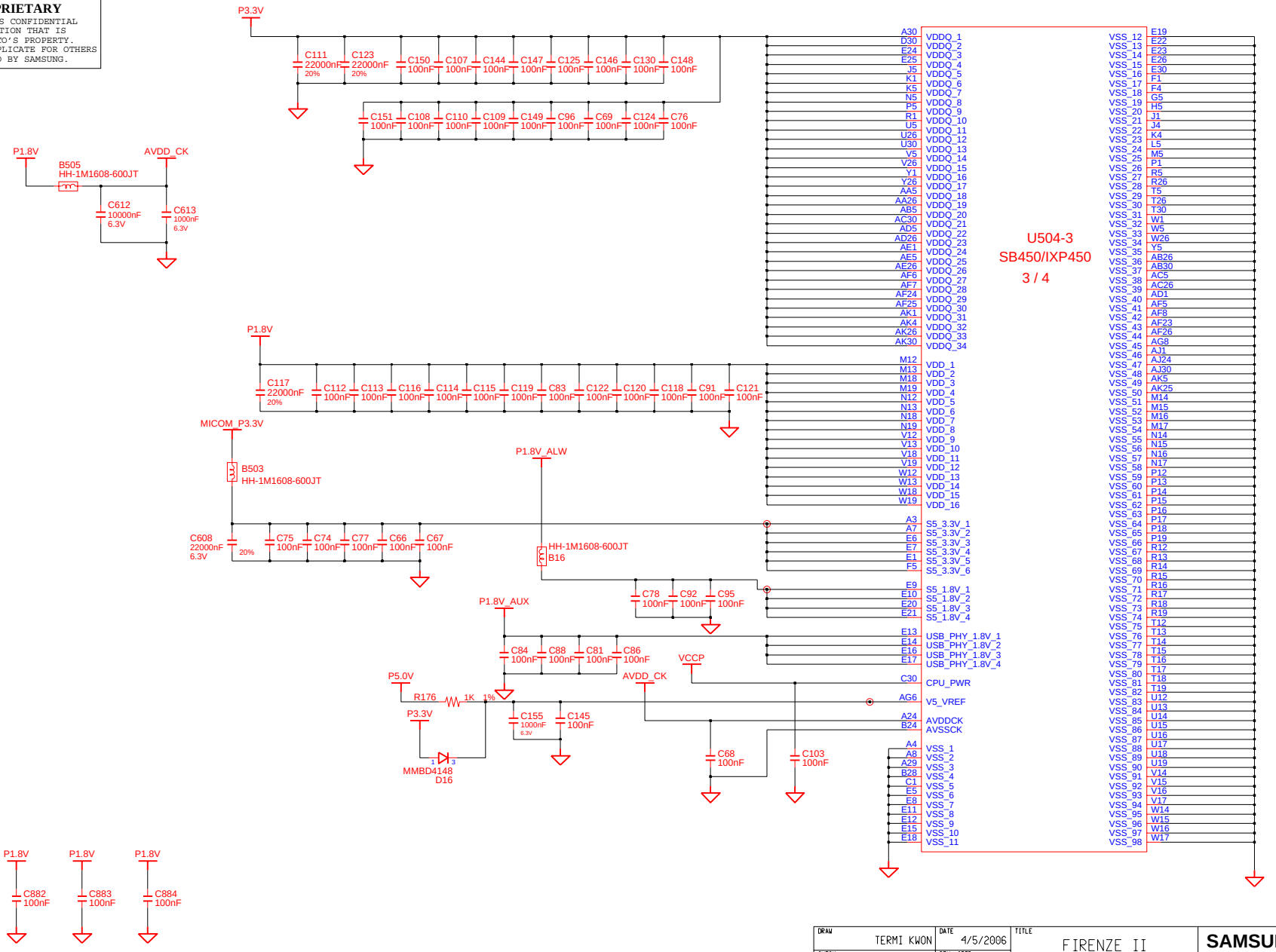
SAMSUNG ELECTRONICS

PART NO. BA41-00659A

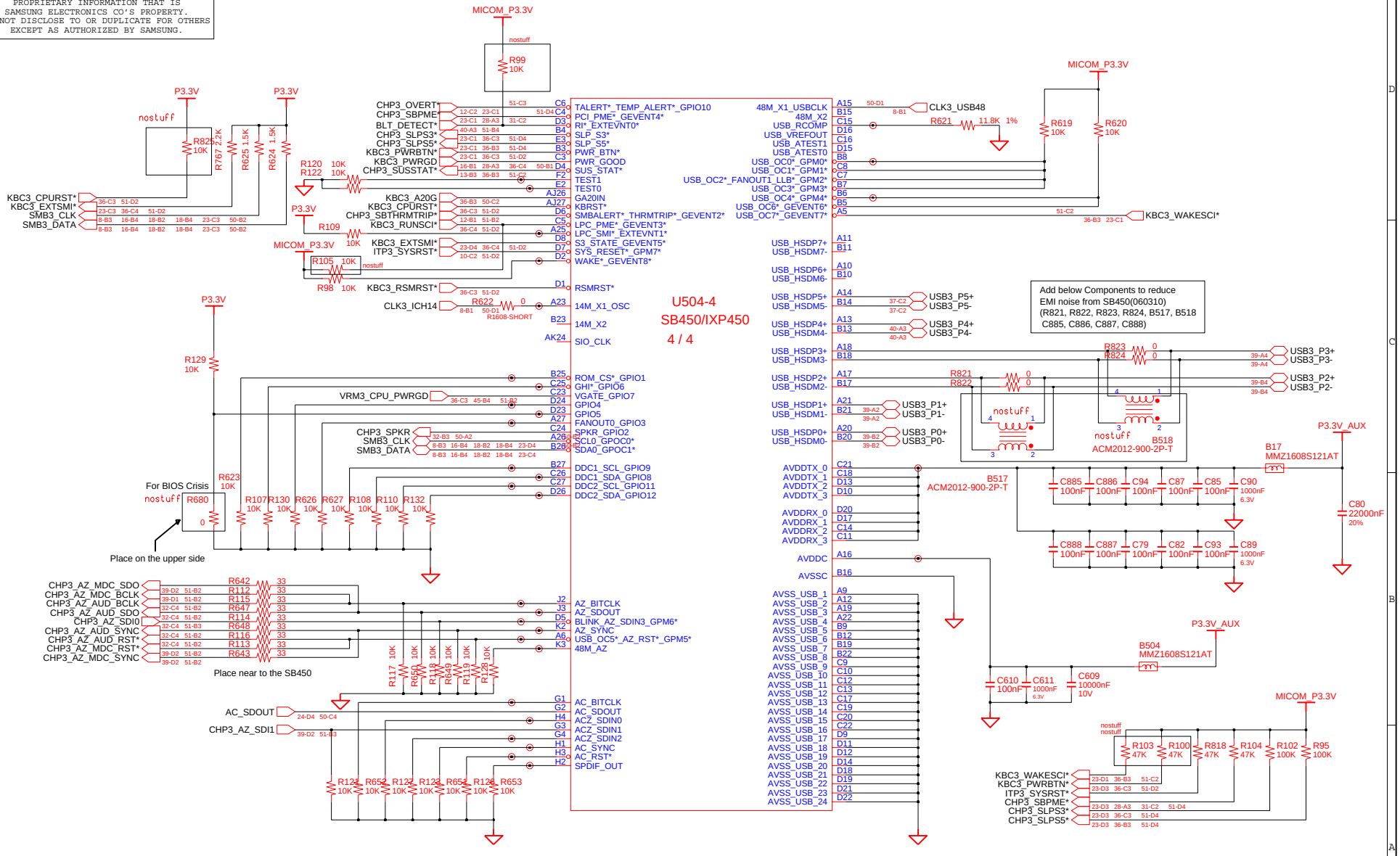
D:/users/mobile62/mentor/firenze2/firenze2_SR1.0_0405



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II POWER SB450(2/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 21 OF 52	

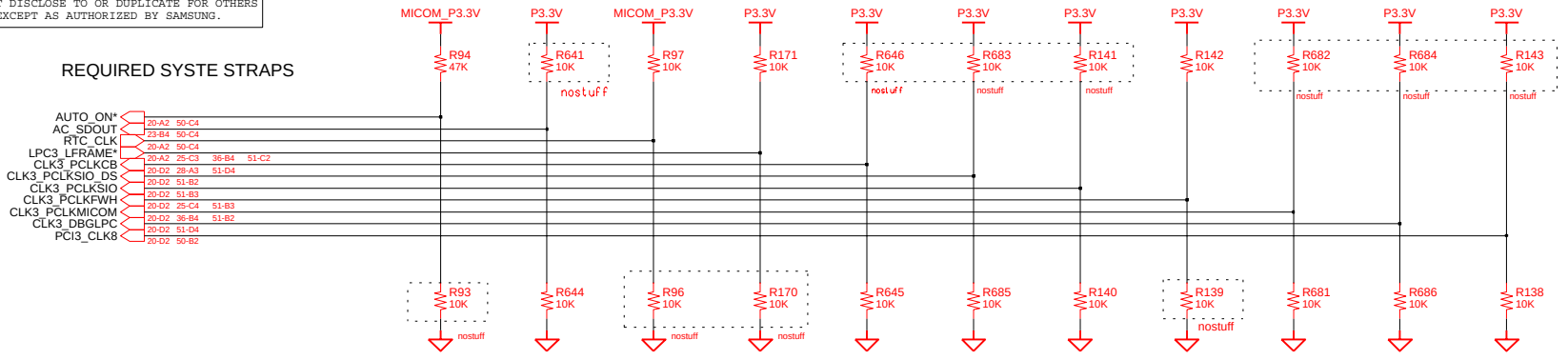


DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN SB450(3/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 22 OF 52	



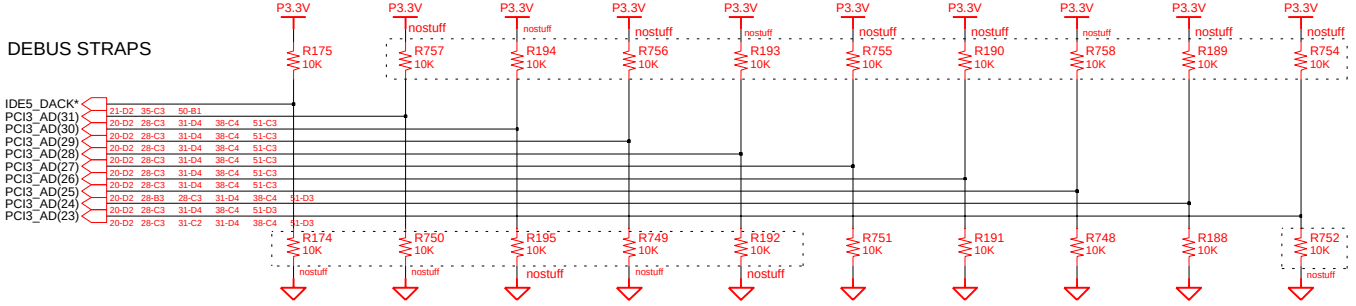
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN SB450(4/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 23 OF 52	

REQUIRED SYSTE STRAPS



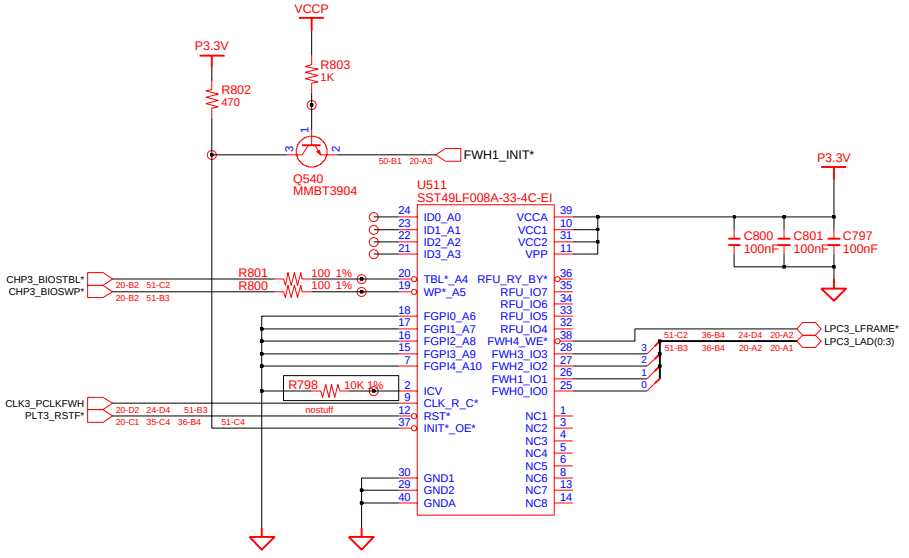
	AUTO_ON	AC_SDOUT	RTC_CLK	LPC3_FRAME	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	PCI3_CLK6	PCI3_CLK7,PCI3_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	Enable thermtrip* on power up	48MHZ XTAL MODE	USB PHY PWRDOWN DISABLE	USE USB PLL	PCI-E lane auto detect	CPU I/F = KB	ROM TYPE H.H = PCI ROM H,L = LPCROM I LPC ADDRESS MAPPED
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXRERNAL RTC	Disable thermtrip* on power up	48MHZ OSC MODE	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	Force PCI-E to lane2	CPU I/F = P4	BELOW 1 M LPC ADDRESS MAPPED TO TOP 4G L,H = LPC ROM II L,L = FWH ROM

DEBUS STRAPS



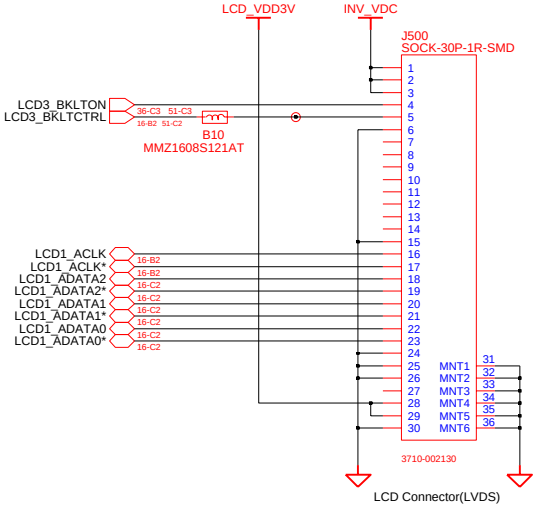
	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

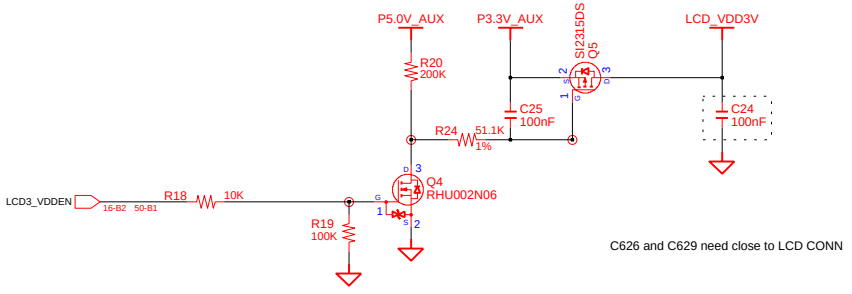
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0	STRAPS	PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 24 OF 52	

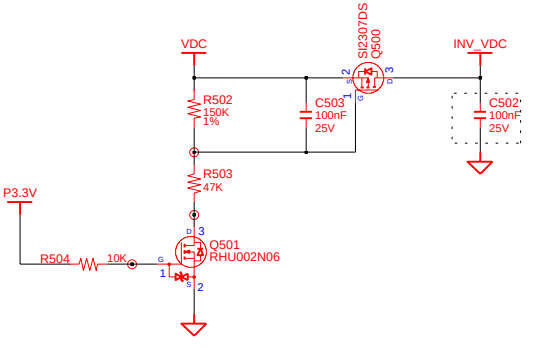


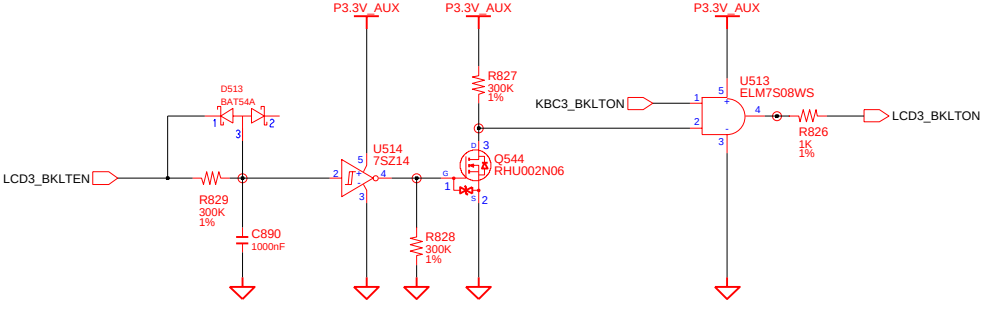
02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM		PAGE 25 OF 52

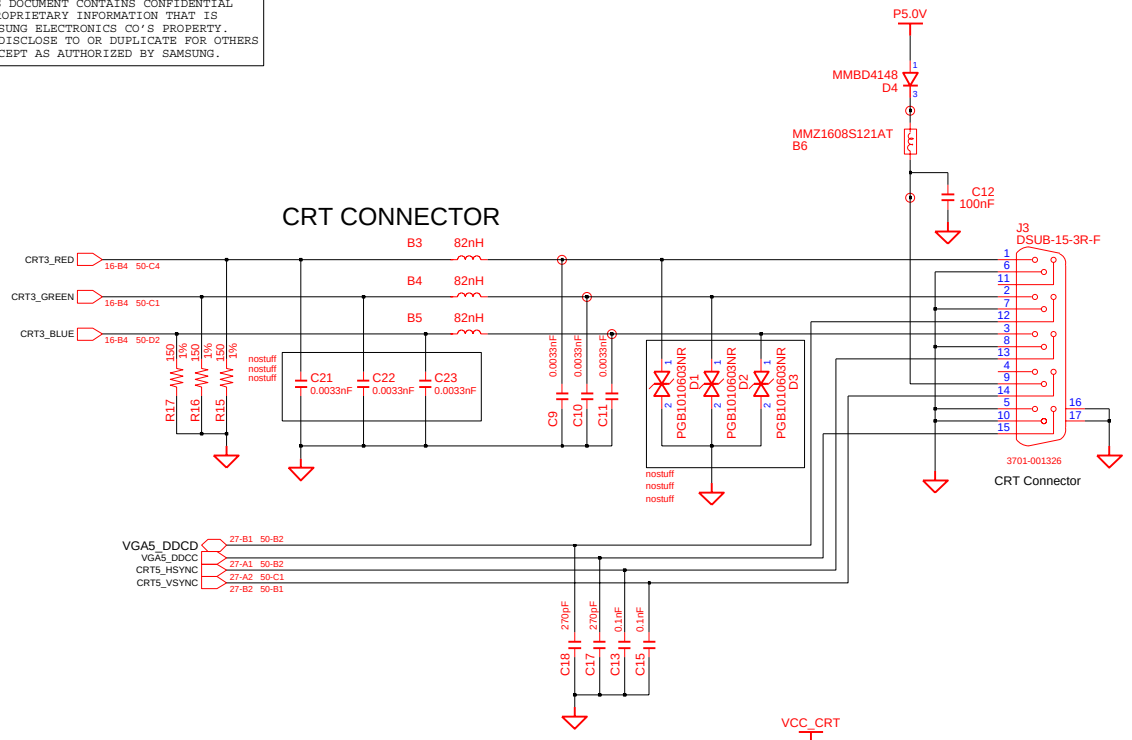


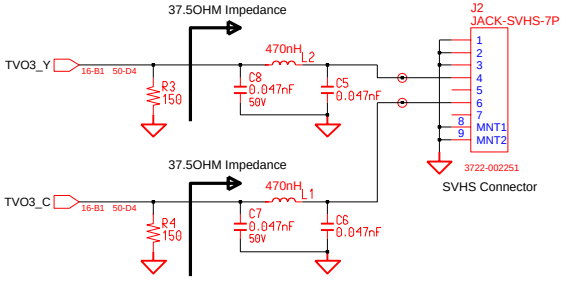




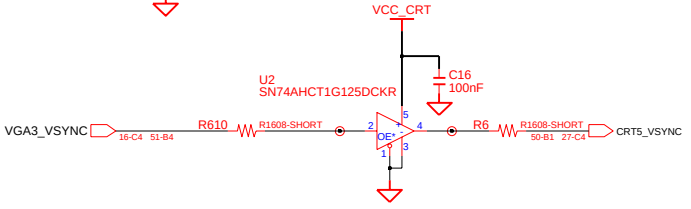


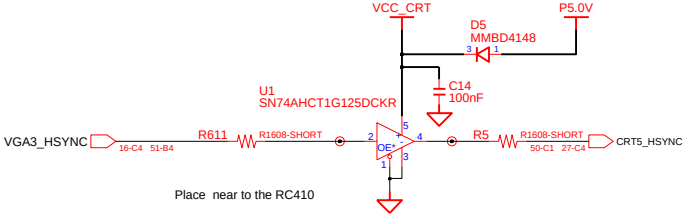
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 26 OF 52	

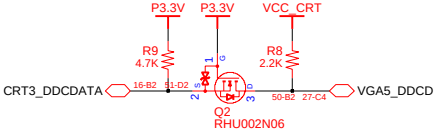


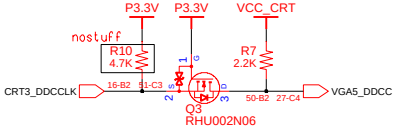


TV-OUT(S-VHS,COMPOSIT)

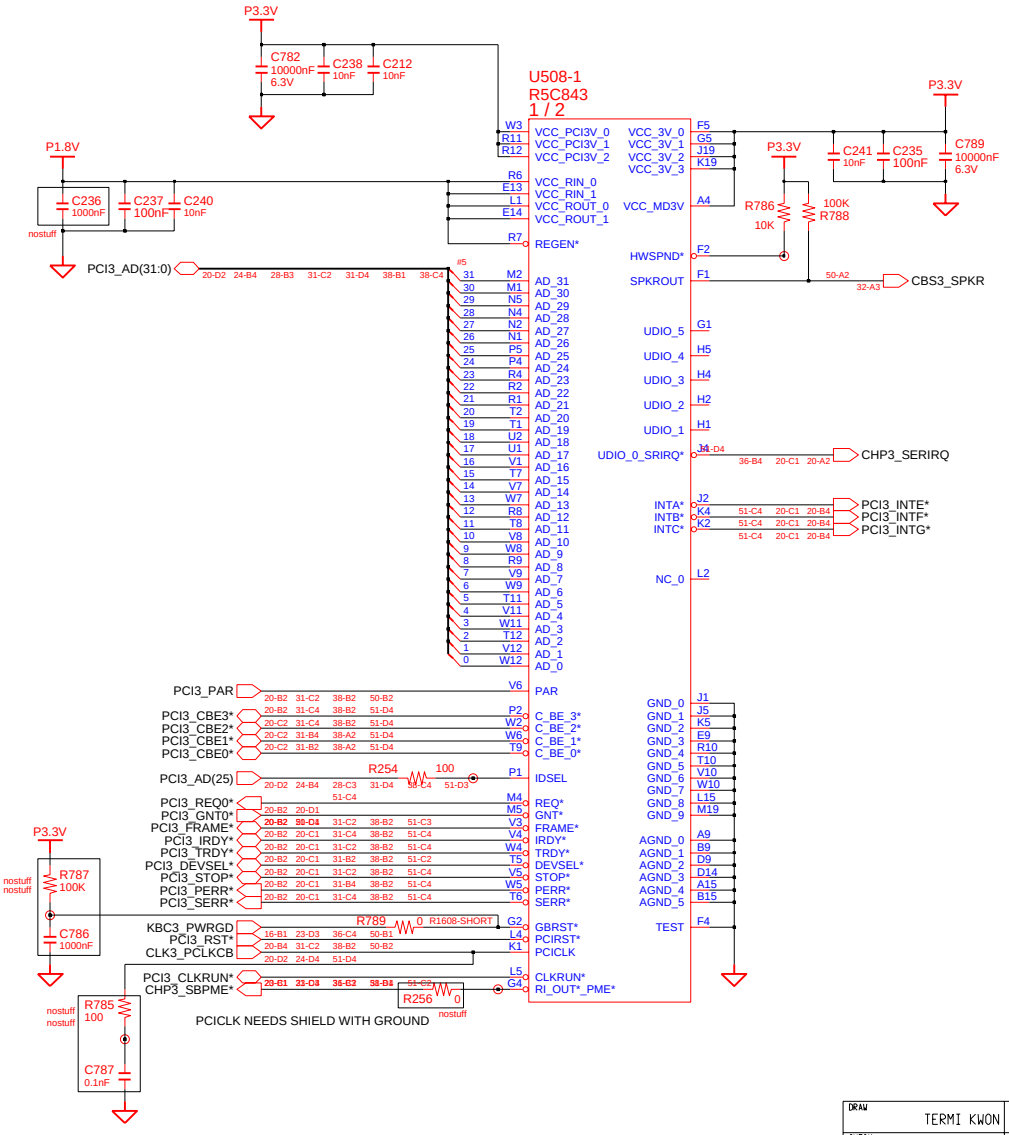




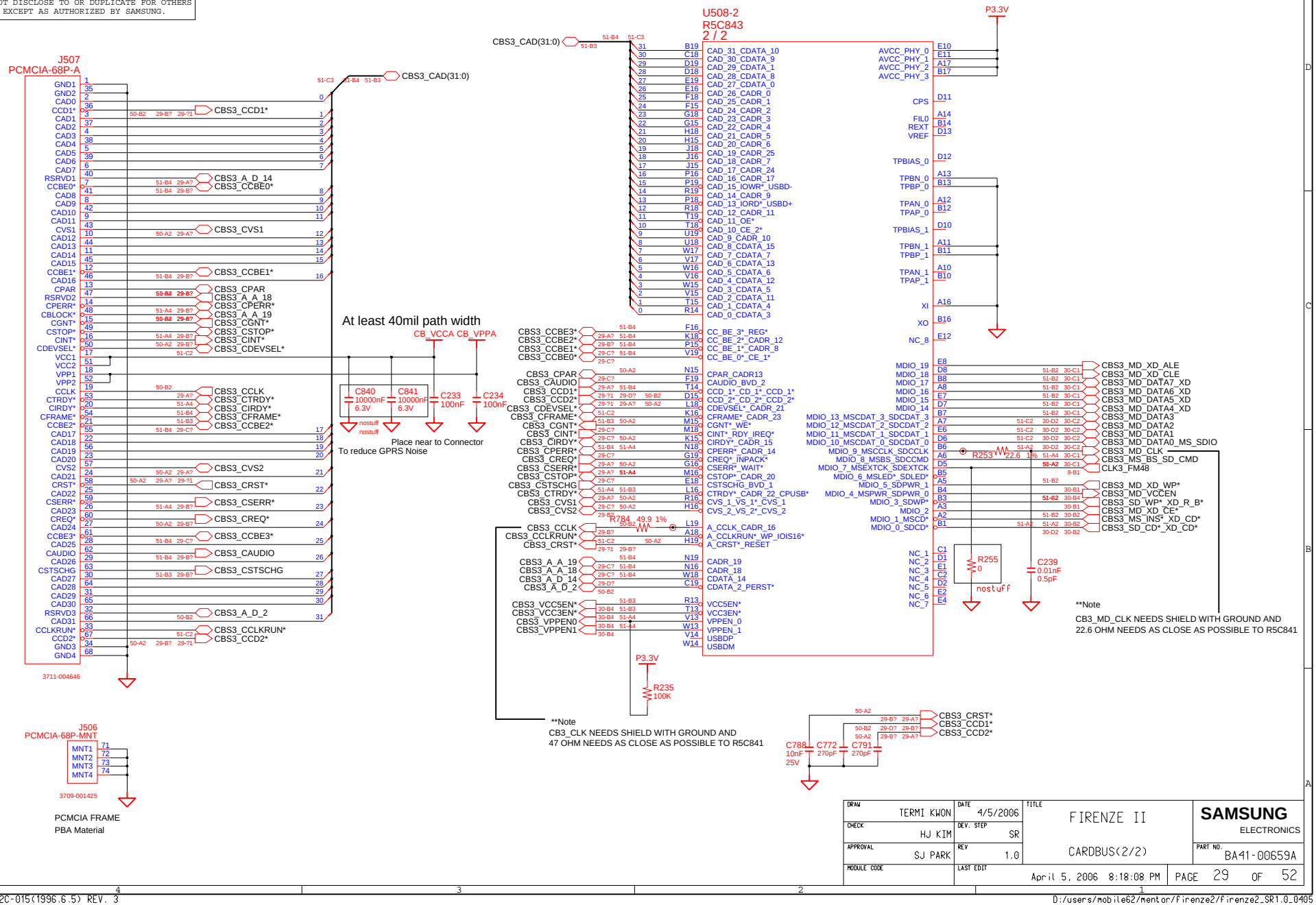




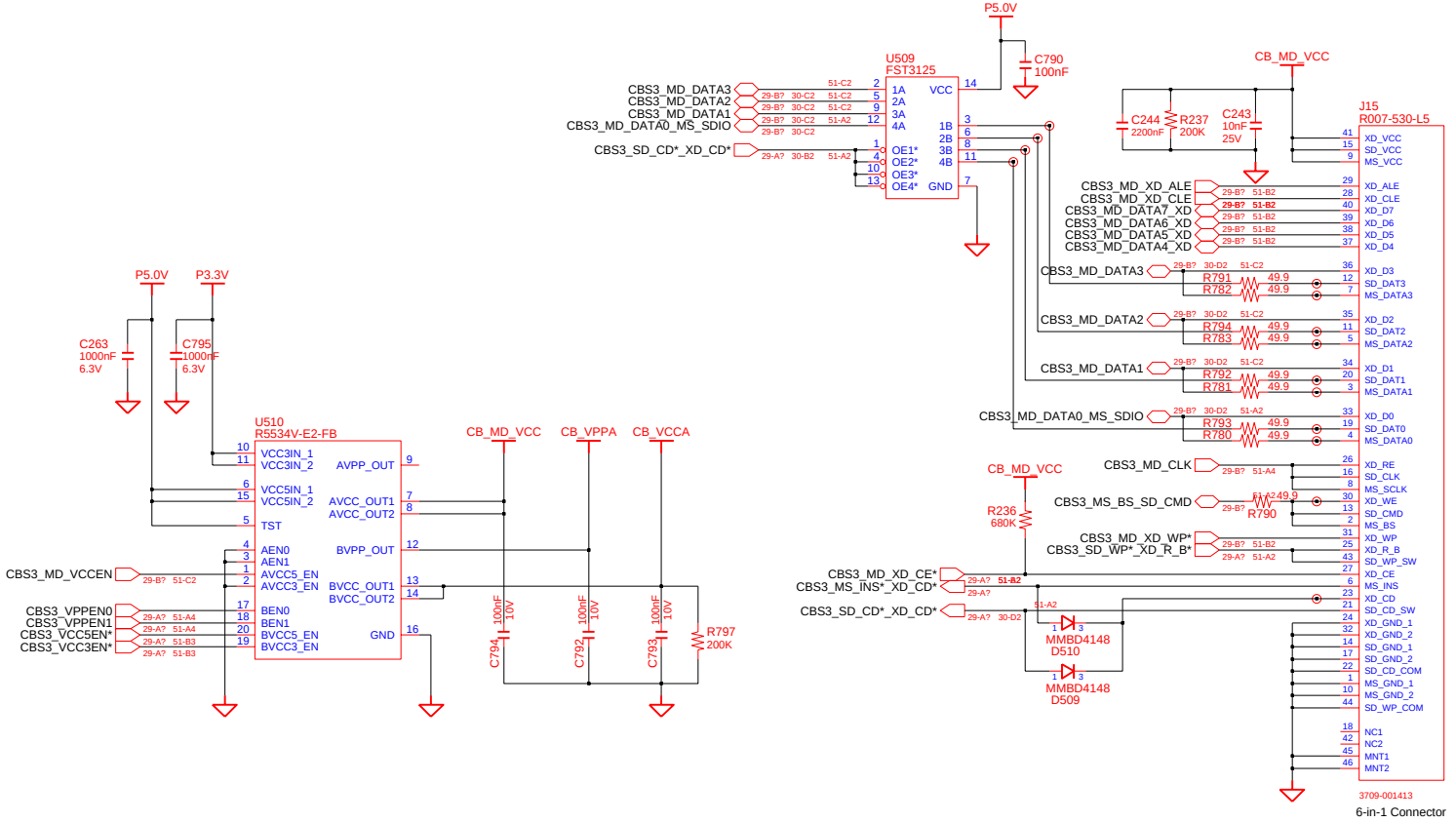
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR	CRT AND TV-OUT	PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 27 OF 52	



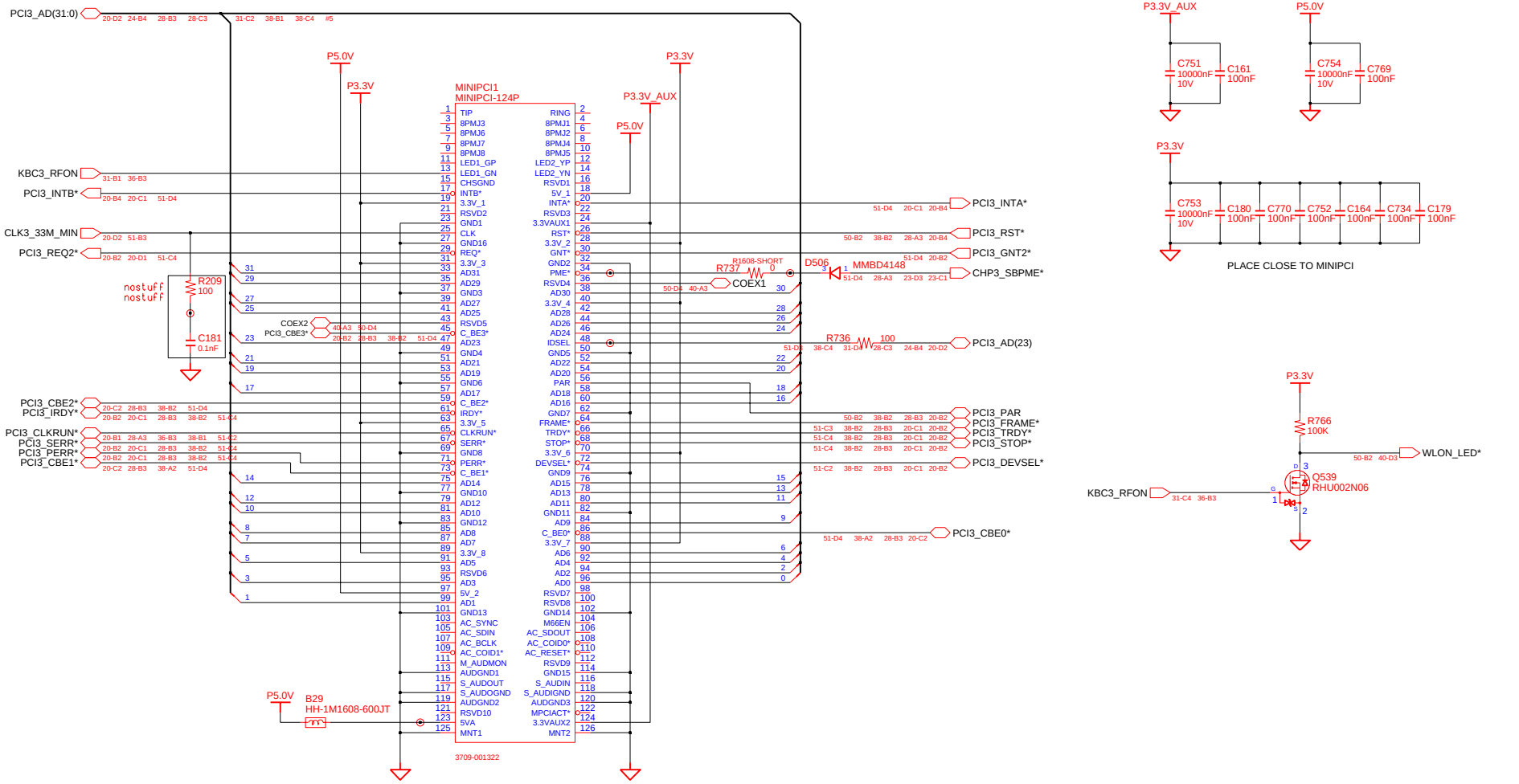
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR	CARDBUS(1/2)	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 28 OF 52	



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR	CARDBUS(2/2)	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 29 OF 52	



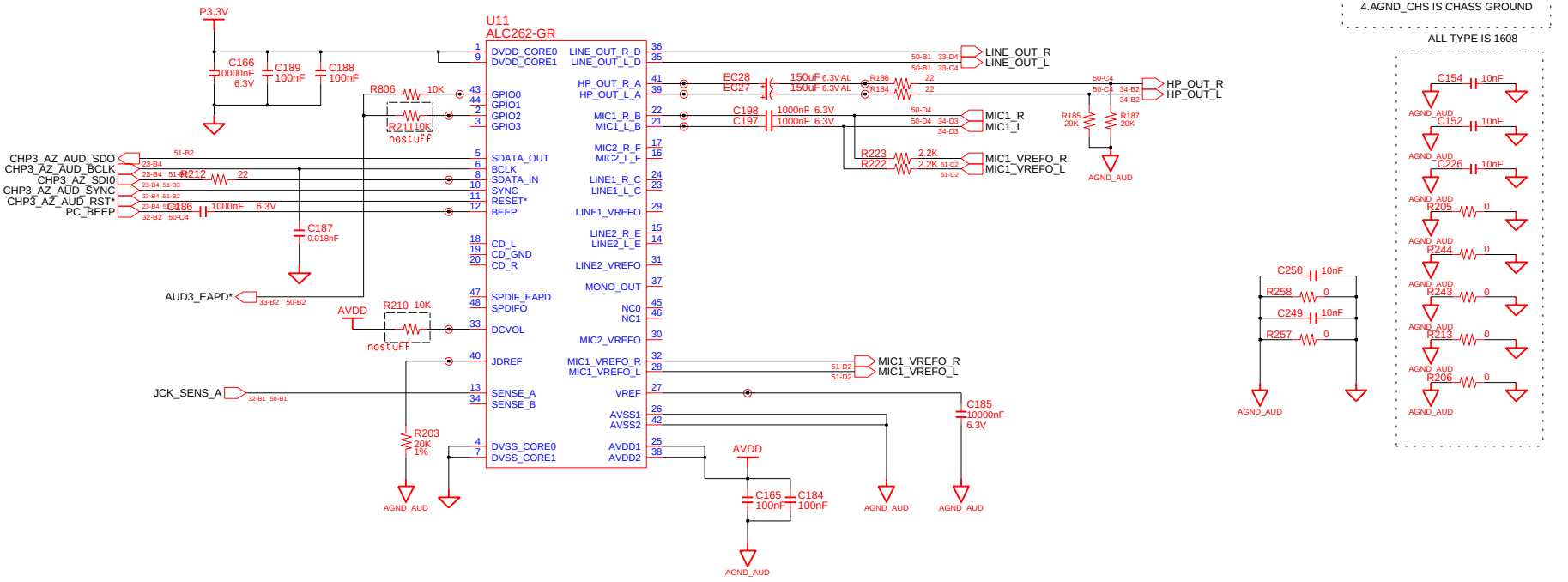
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR	5 in 1 Socket	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE	LAST EDIT: April 5, 2006 8:18:08 PM		PAGE 30 OF 52

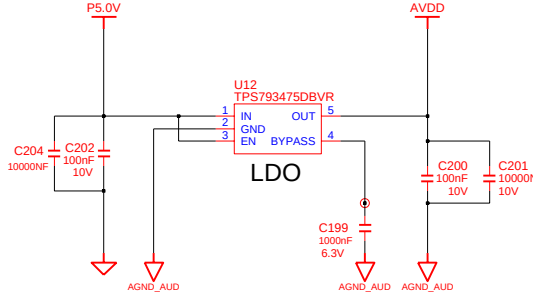


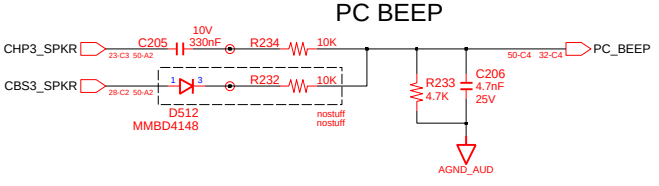
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 31 OF 52	

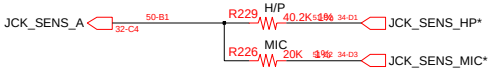
1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3.AGND_MIC IS MIC GROUND
4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608

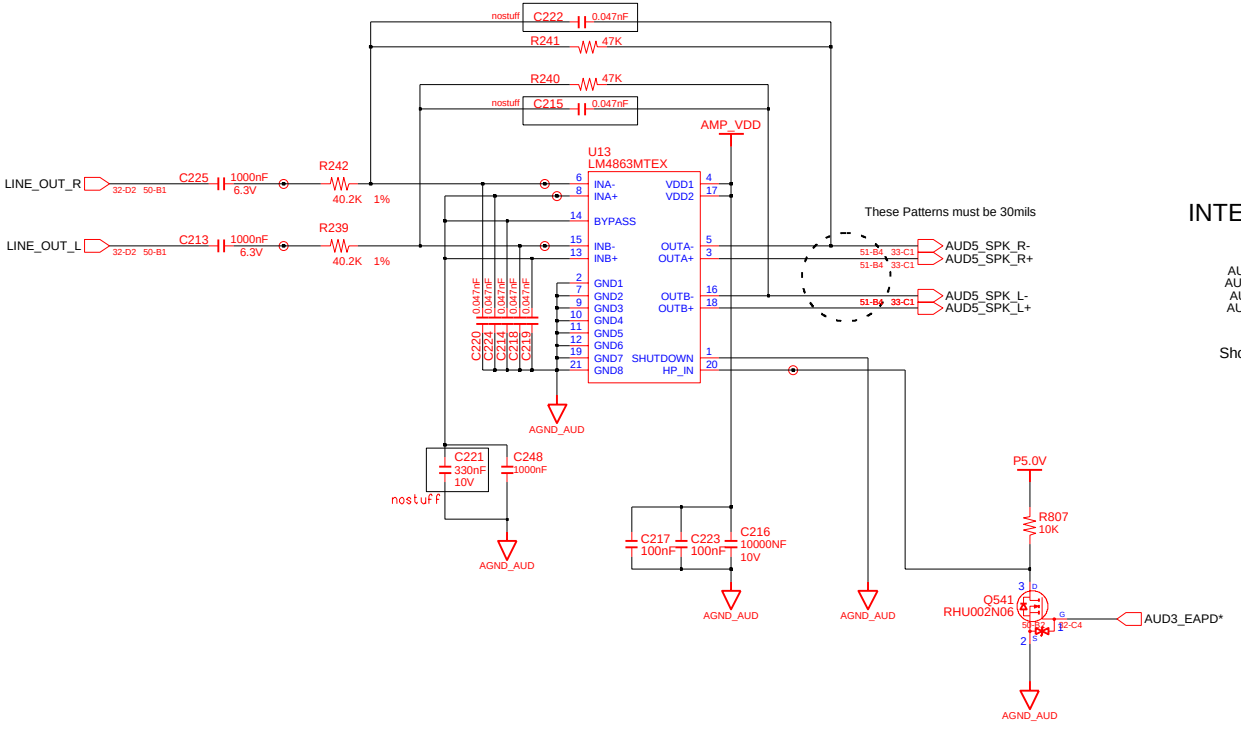




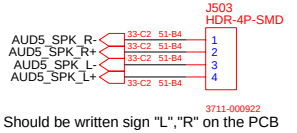




DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 32 OF 52	

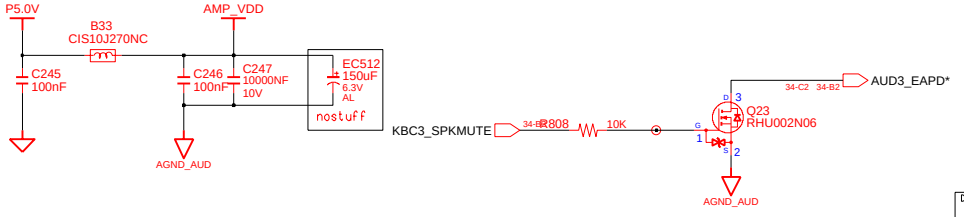


INTERNAL STEREO SPEAKERS



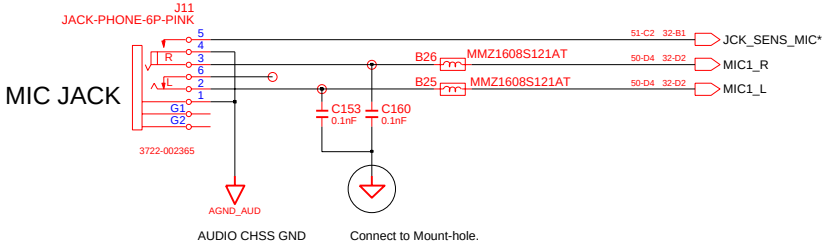
Should be written sign "L","R" on the PCB

AMP_VDD

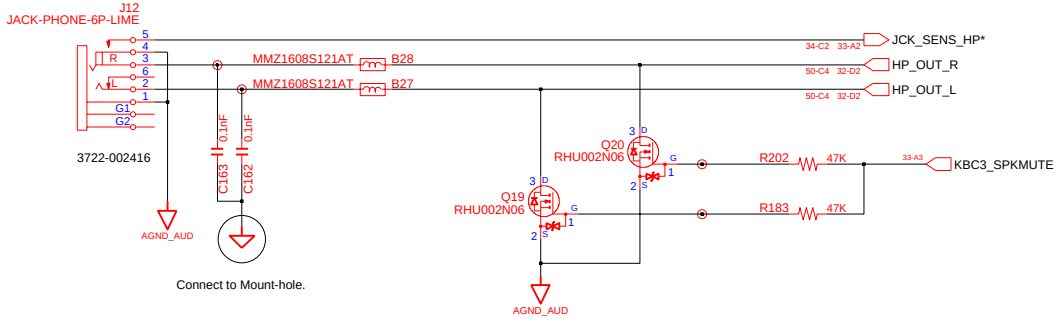


DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 33 OF 52	

MIC JACK



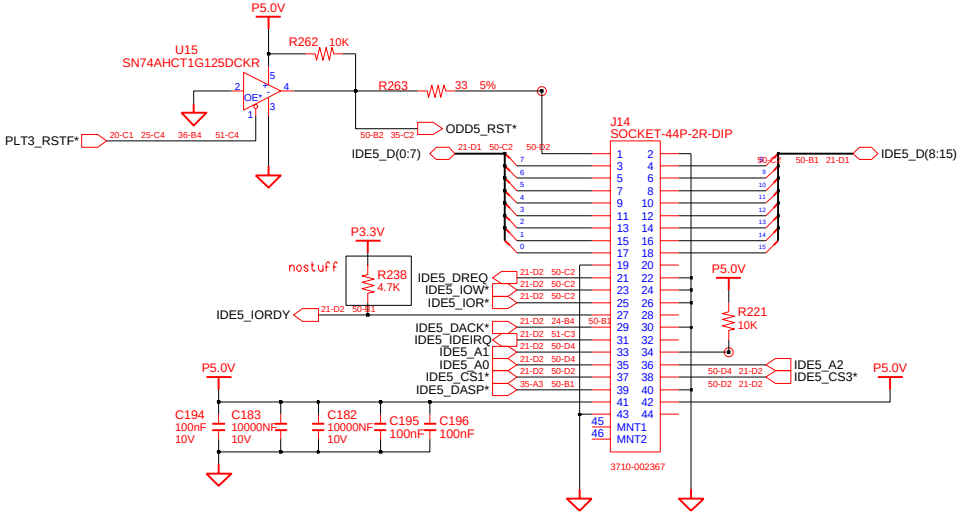
HEADPHONE



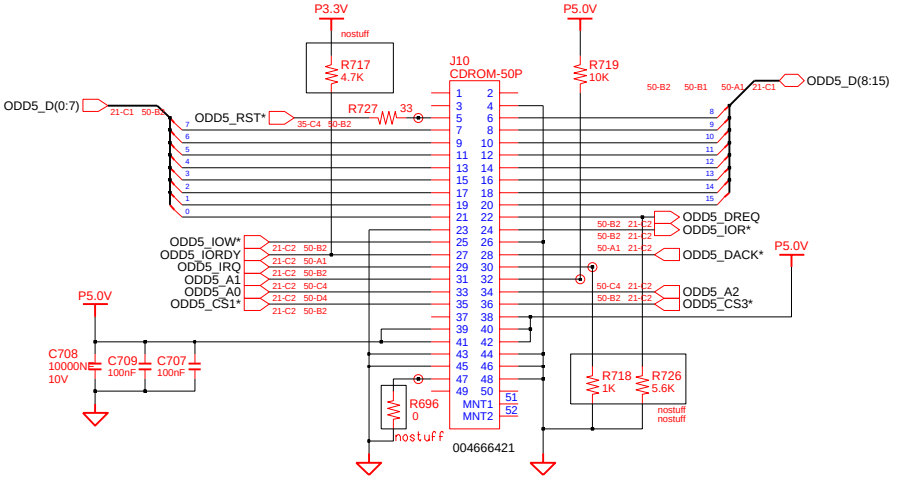
The traces led to Audio Jacks have the width over 10mil

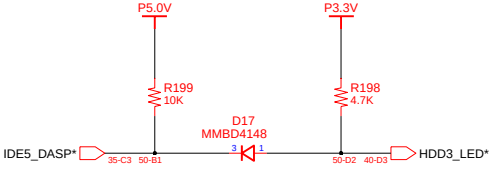
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 34 OF 52	

Main to HDD

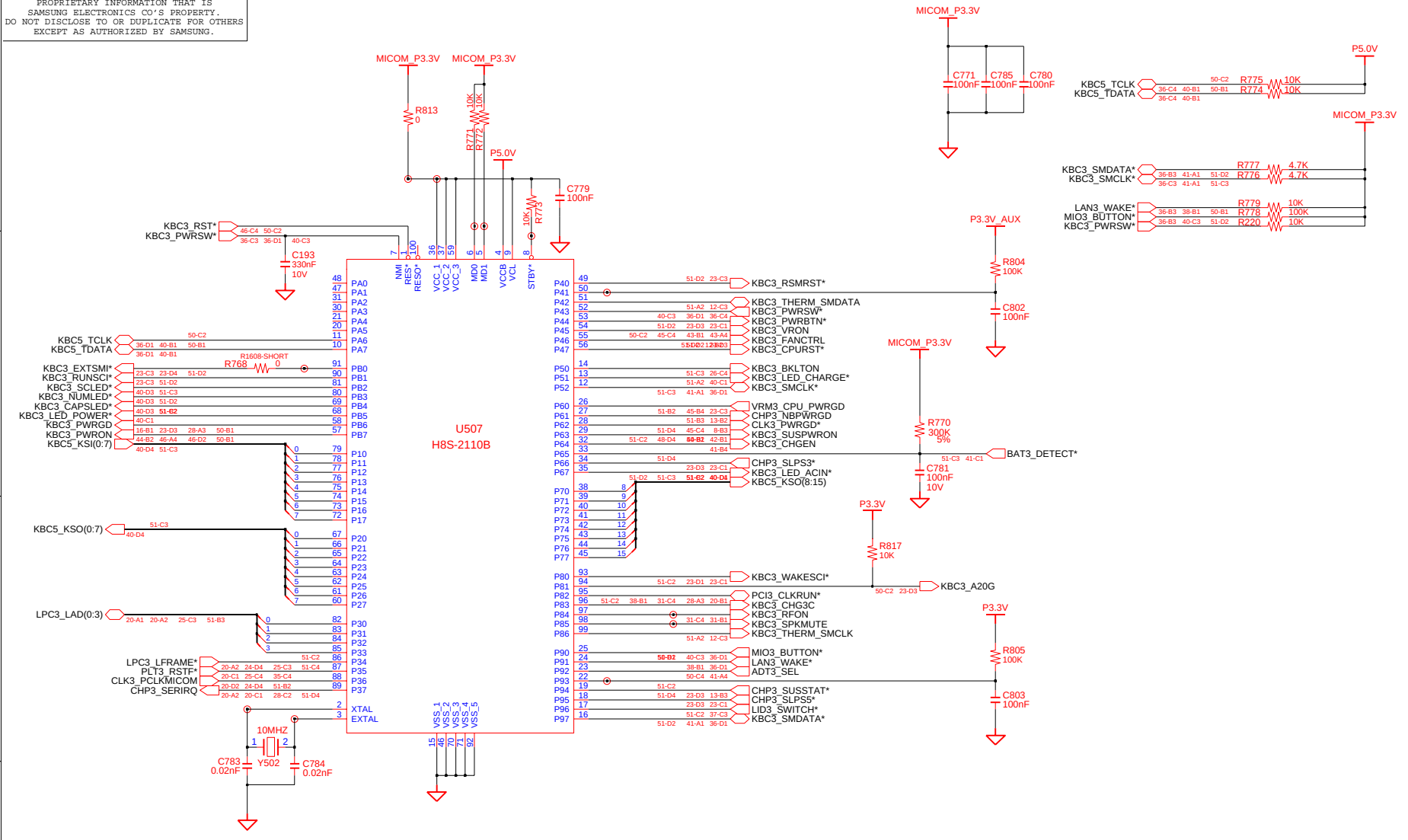


Main to ODD





DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 35 OF 52	



MICOM Crisis Update

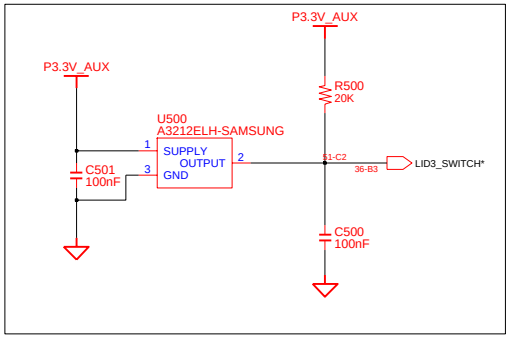
Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

The removed signal compaired from 144pin

- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

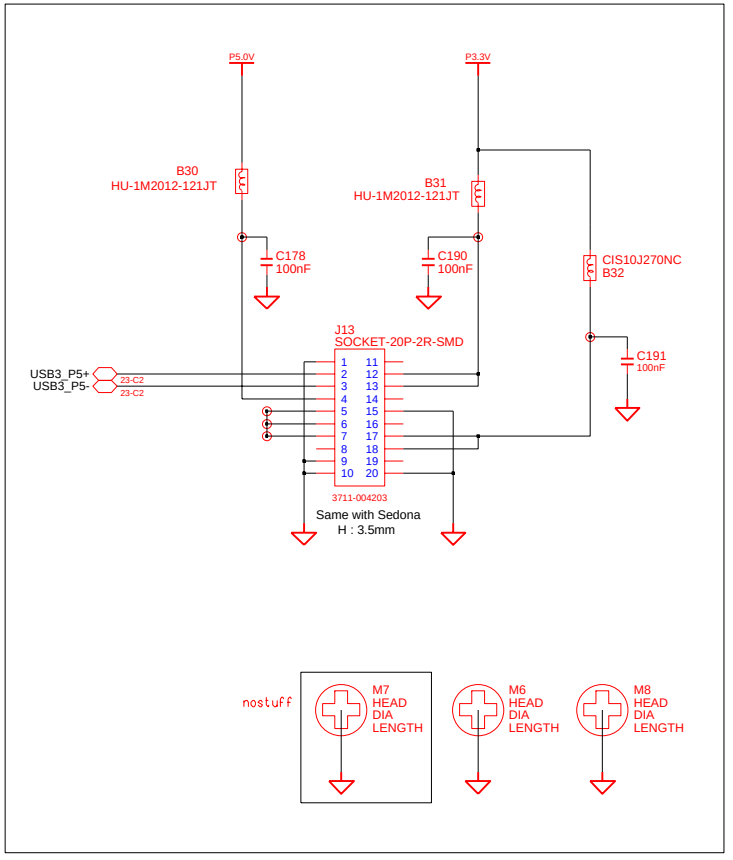
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II POWER MICOM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 36 OF 52	

LID SWITCH



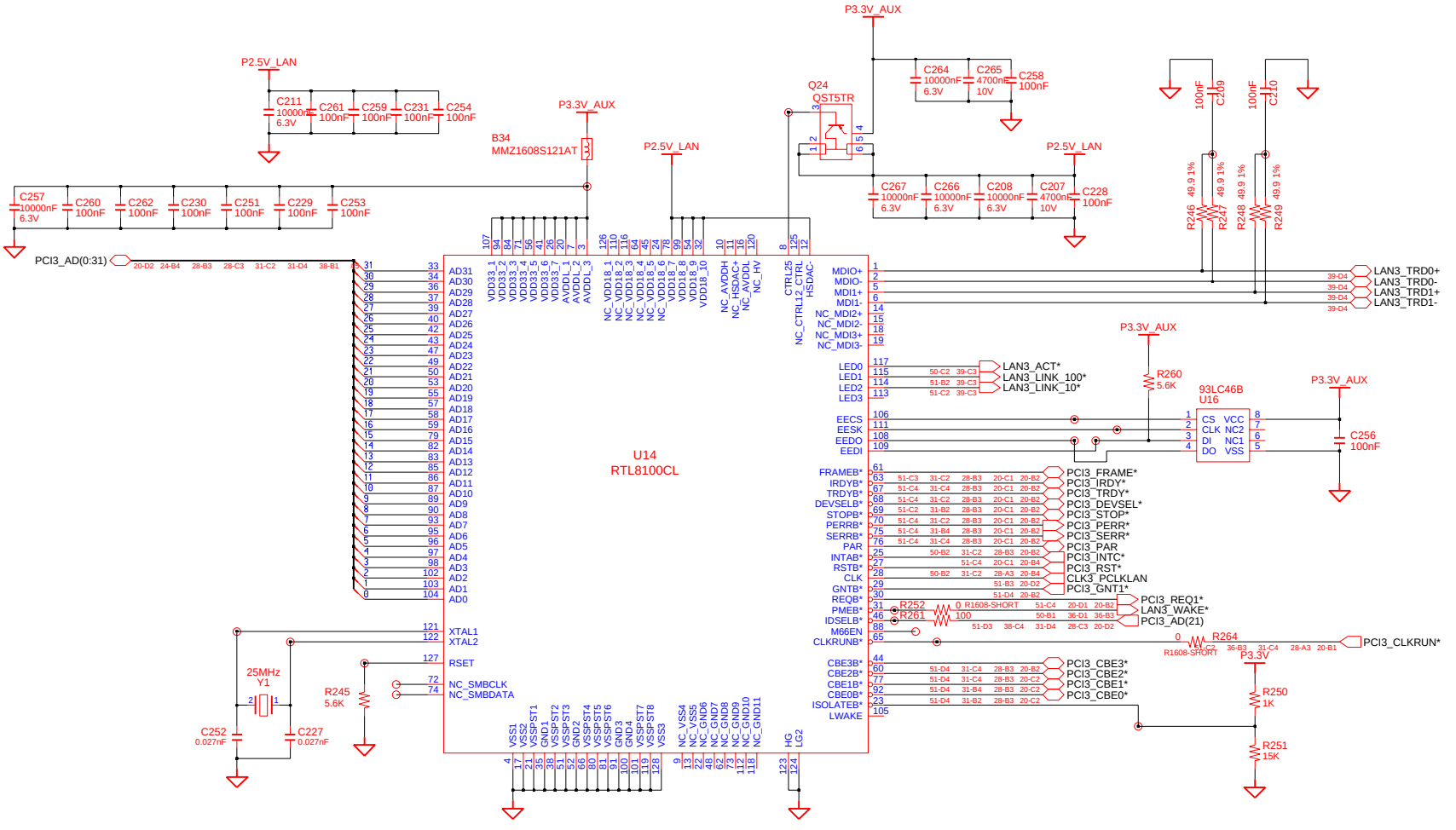
DMB

Factory Option



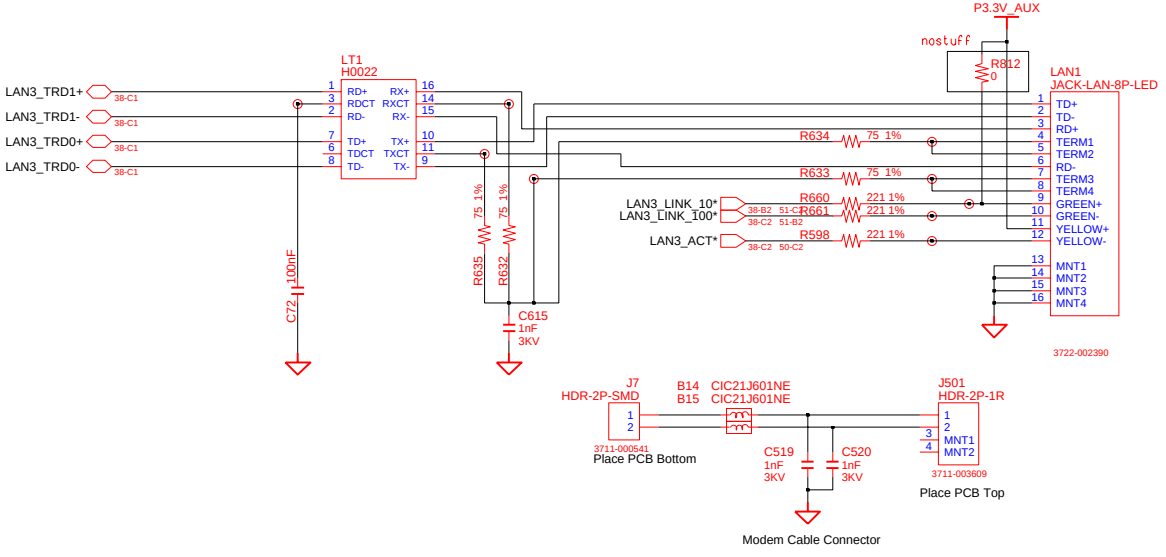
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN LPC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 37 OF 52	

LAN Controller (Only 10/100M)

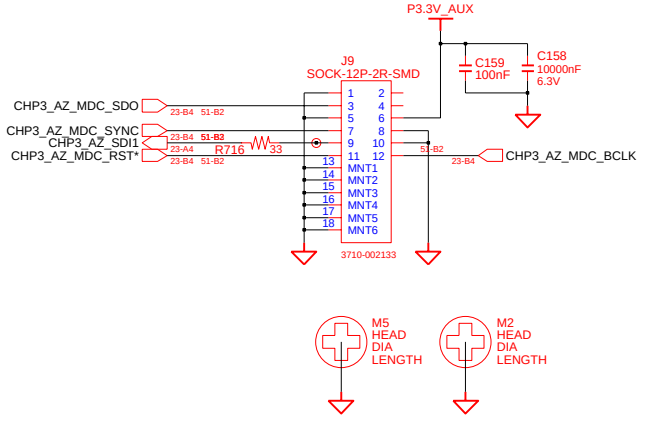


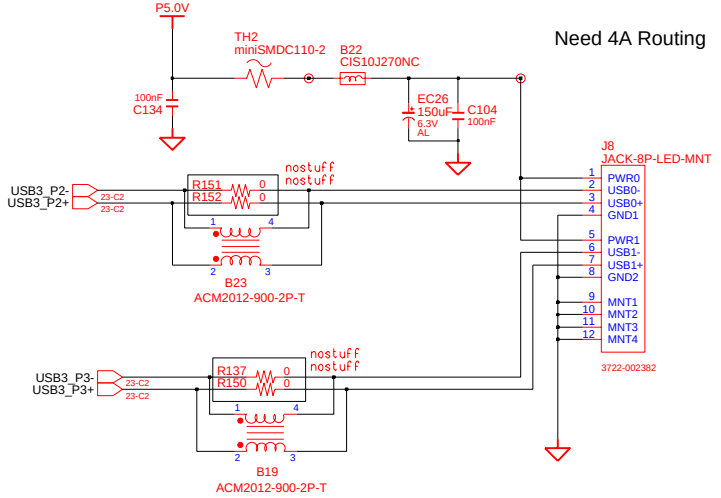
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN LAN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 38 OF 52	

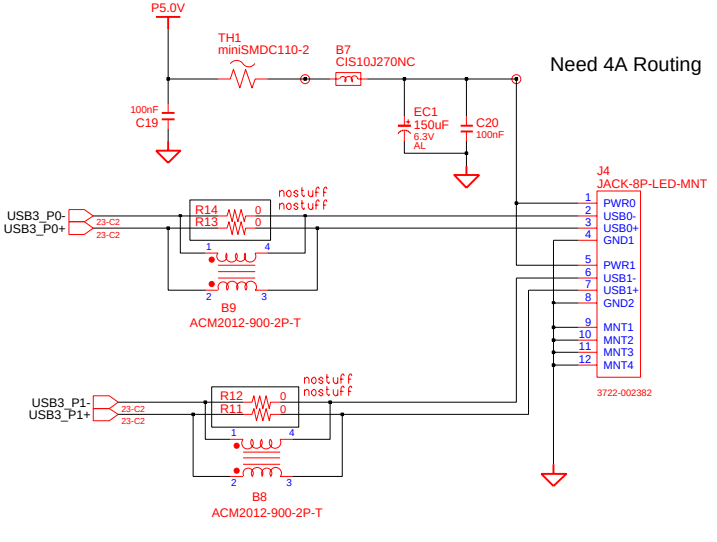
LAN Connector



MDC Connecter



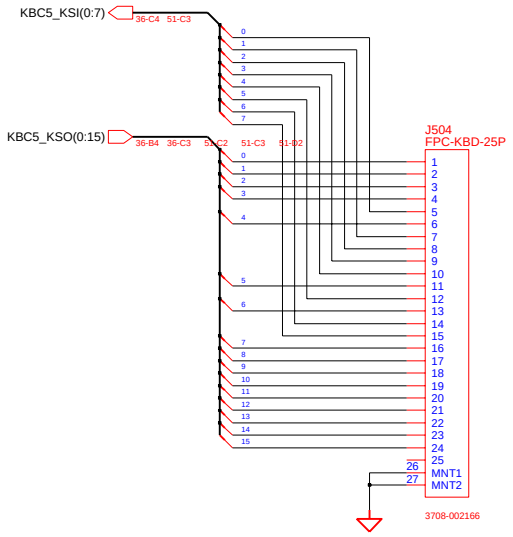


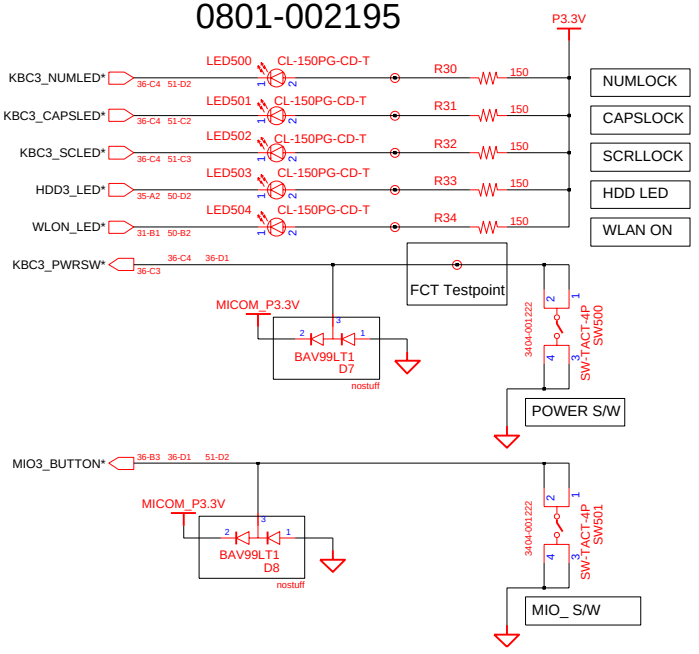


DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN LAN & USB0 & MODEM Conn.	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 39 OF 52	

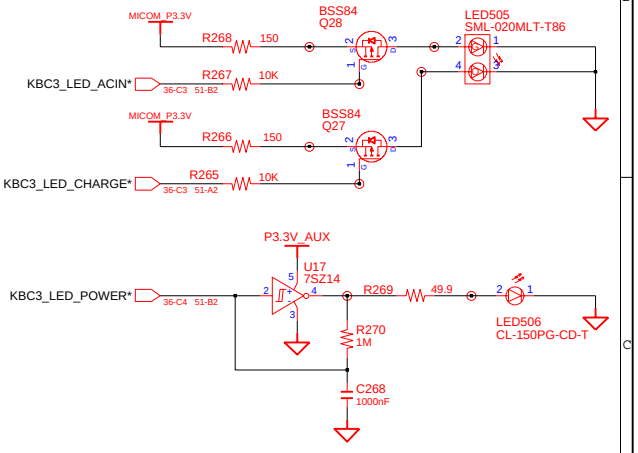
LED
0801-002195

KEYBOARD
Same connector with Sedona

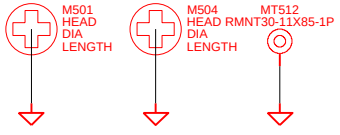


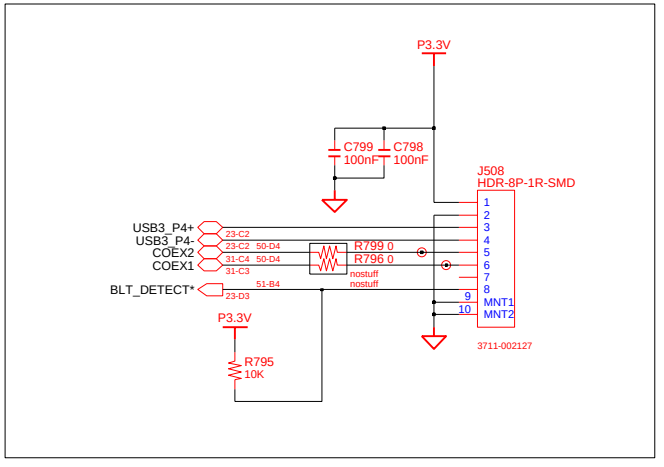


ADAPTERIN/CHARGING LED

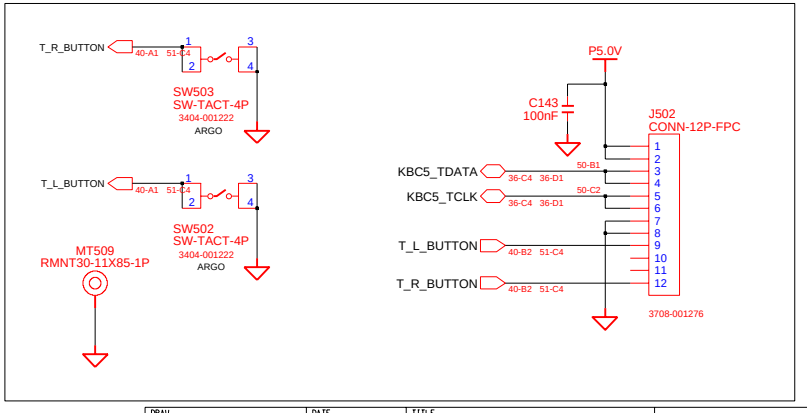


Bluetooth Interface
Factory Option



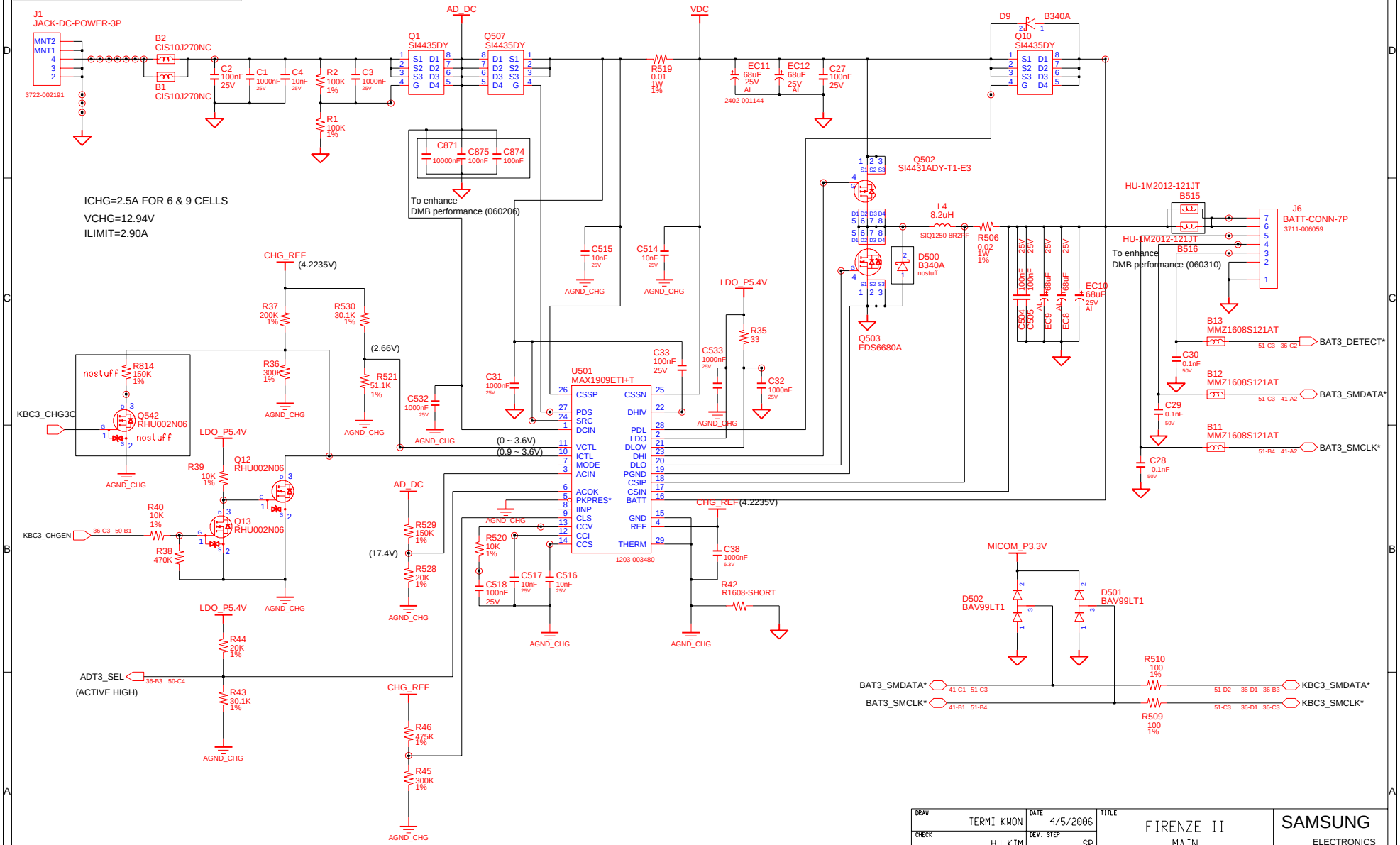


TOUCHPAD



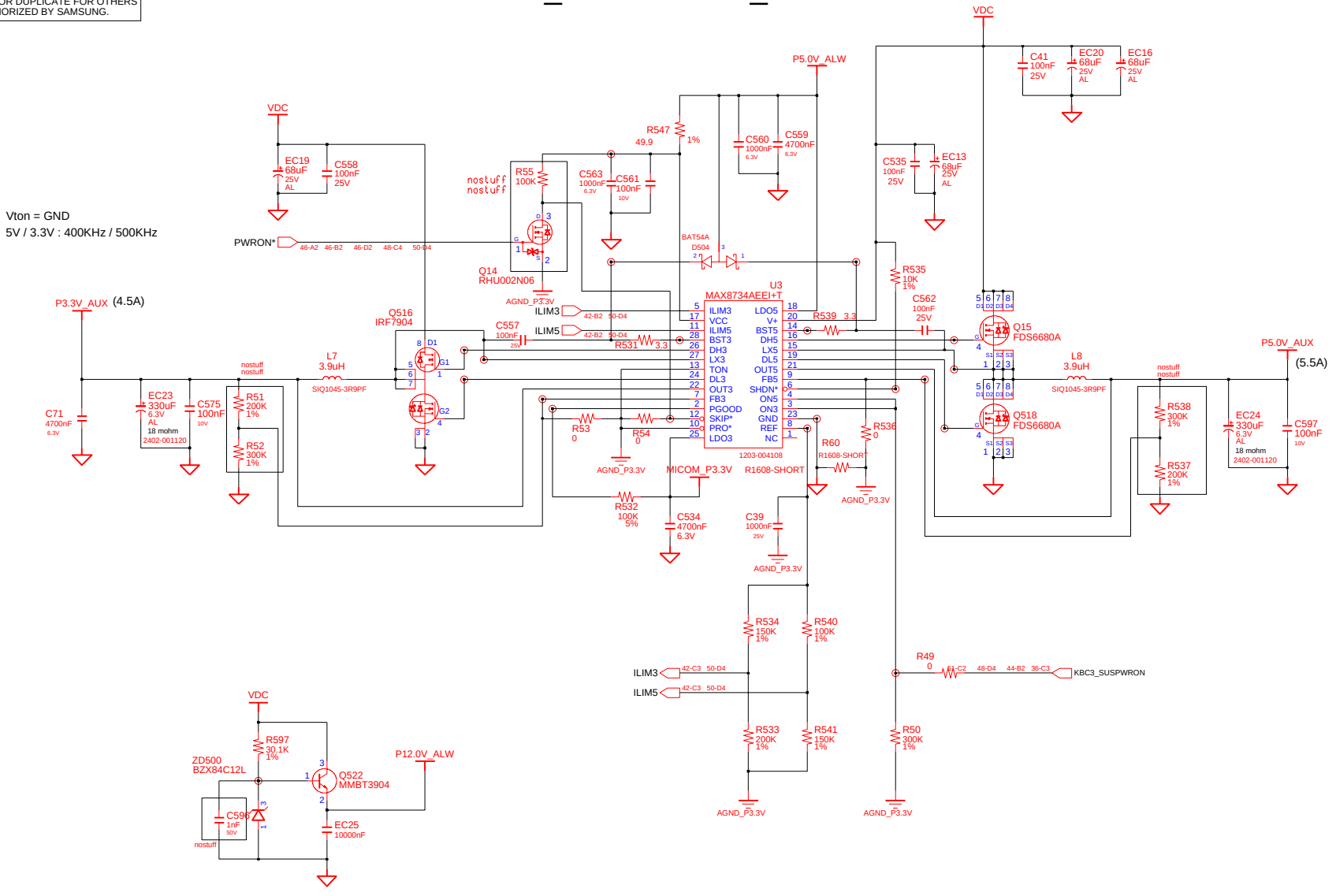
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 40 OF 52	

CHARGER & POWER MANAGEMENT



DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 41 OF 52	

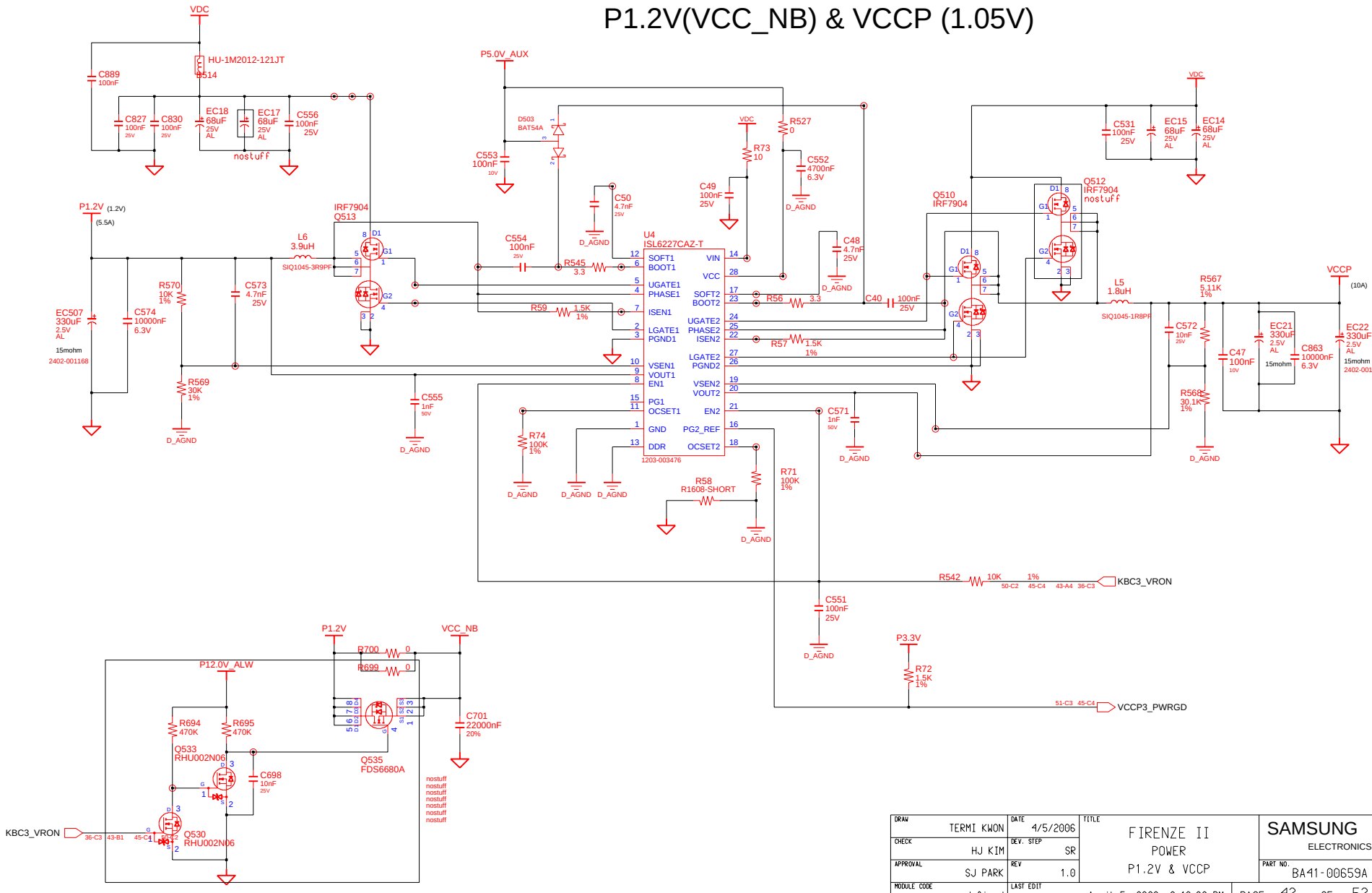
P3.3V_AUX & P5.0V_AUX



DRAW	TERMI KWON	DATE	4/5/2006	TITLE	FIRENZE II POWER P3.3V ALWAYS & P5V_AUX
CHECK	HJ KIM	DEV. STEP	SR		
APPROVAL	SJ PARK	REV	1.0		
MODULE CODE	undefined	LAST EDIT	April 5, 2006 8:18:08 PM	PAGE	42 OF 52

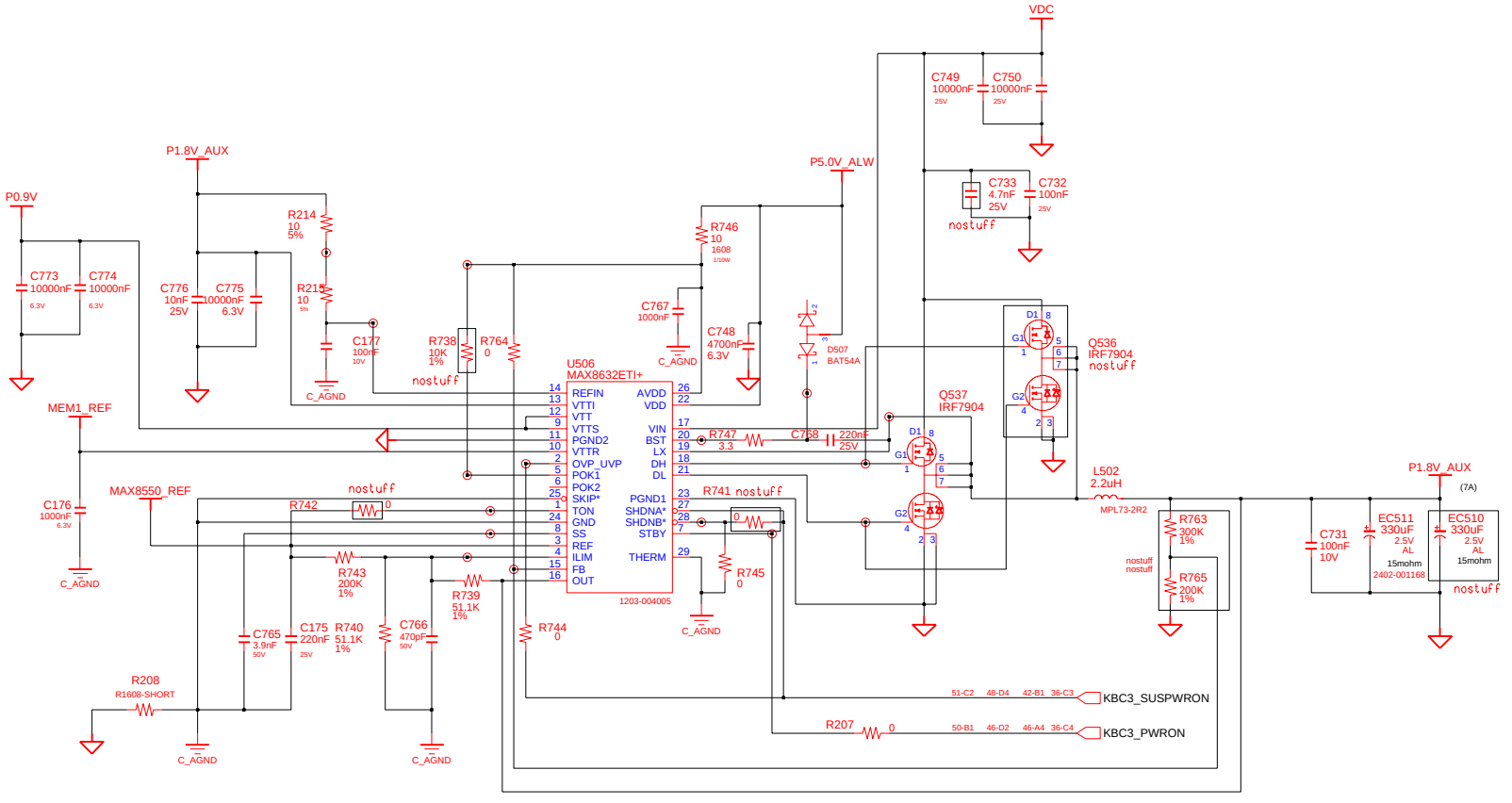
SAMSUNG ELECTRONICS
PART NO. BA41-00659A

P1.2V(VCC_NB) & VCCP (1.05V)



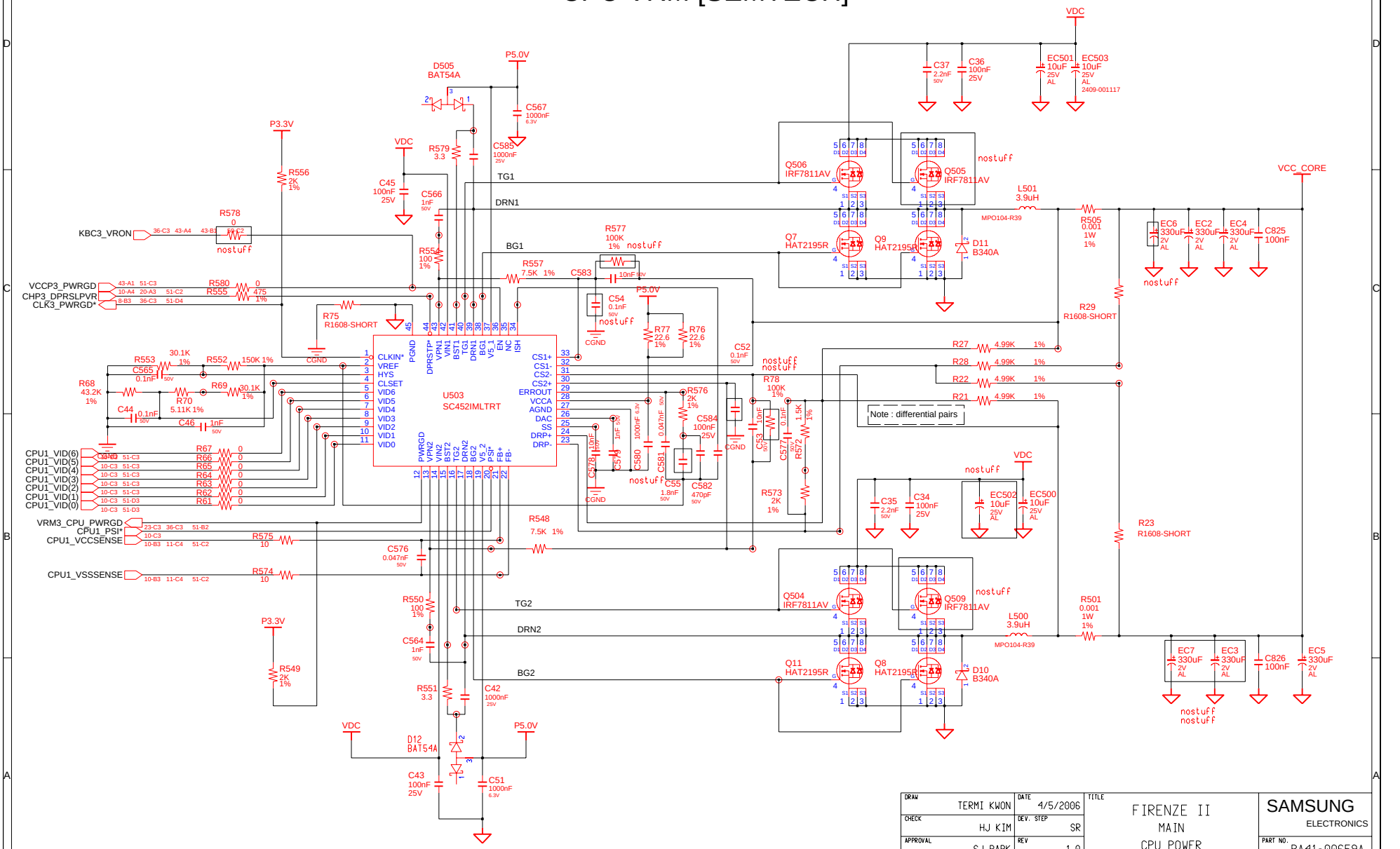
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II POWER P1.2V & VCCP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 43 OF 52	

DDR2 Power



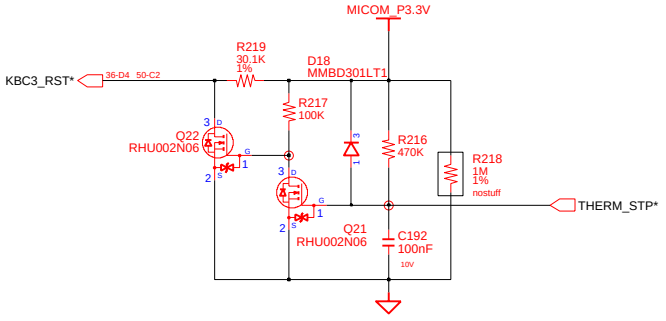
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 44 OF 52	

CPU VRM [SEMTECH]

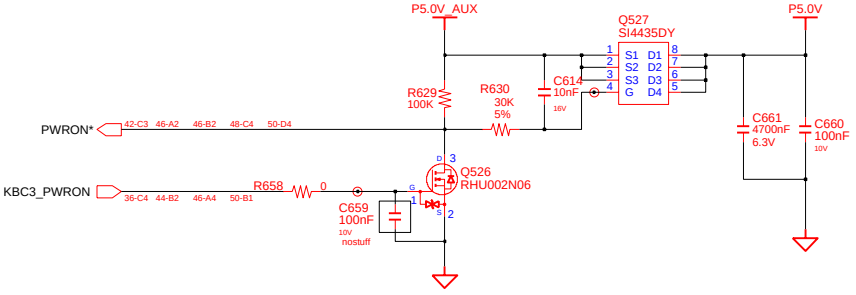


DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN CPU POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 45 OF 52	

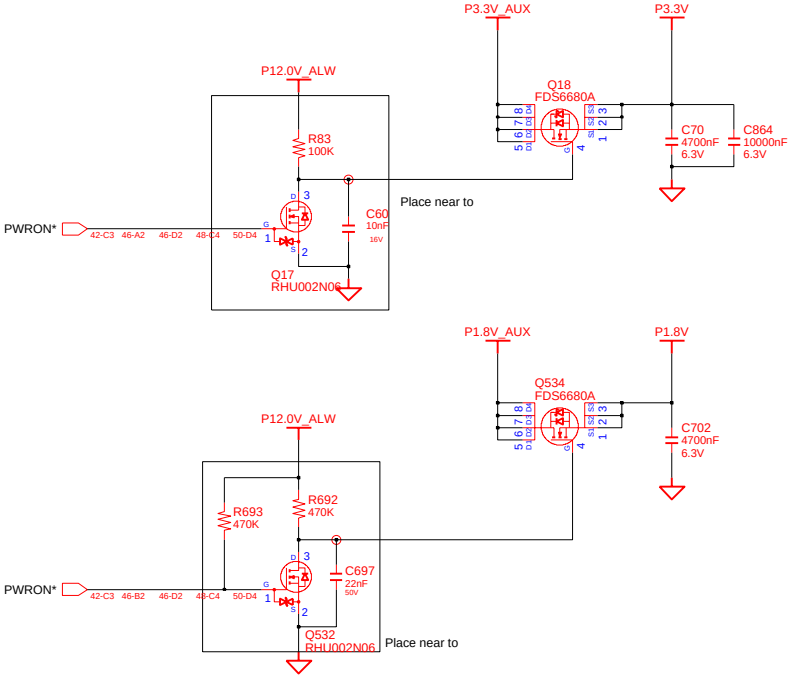
MICOM RESET



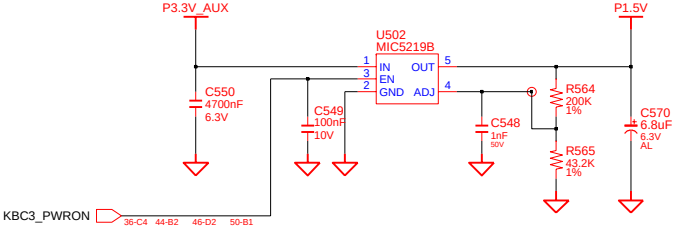
Switched Power On (P5V)



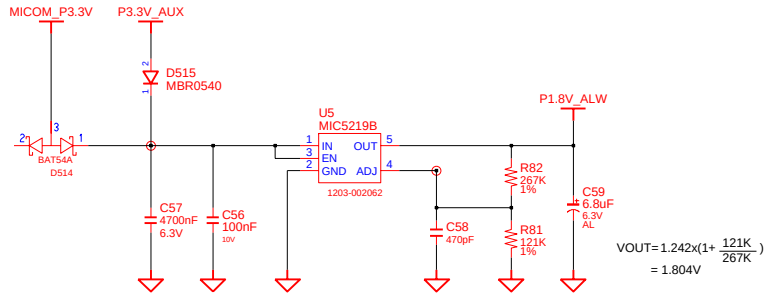
Switched Power On (P3.3V & 1.8V)

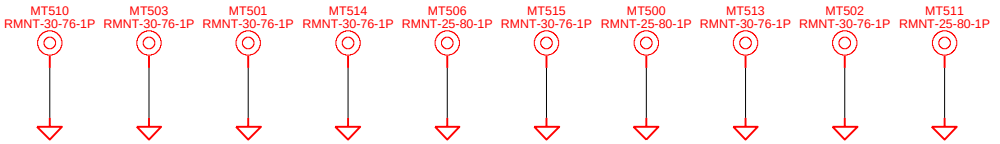


P1.5V POWER

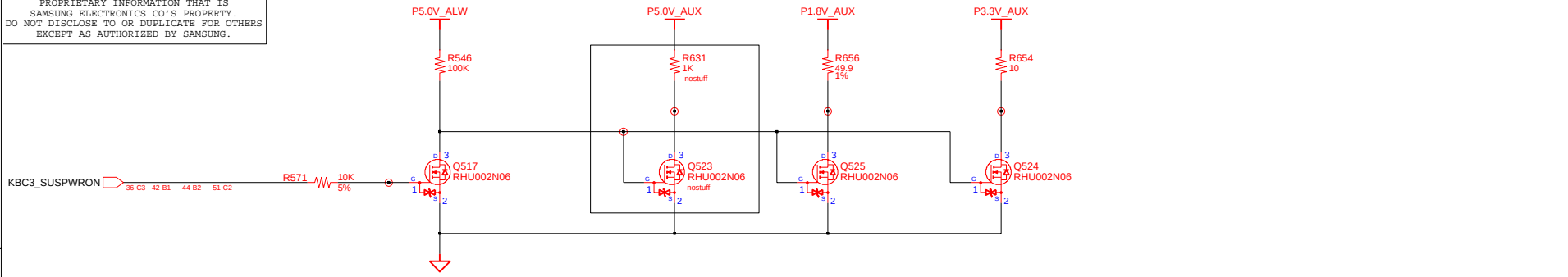


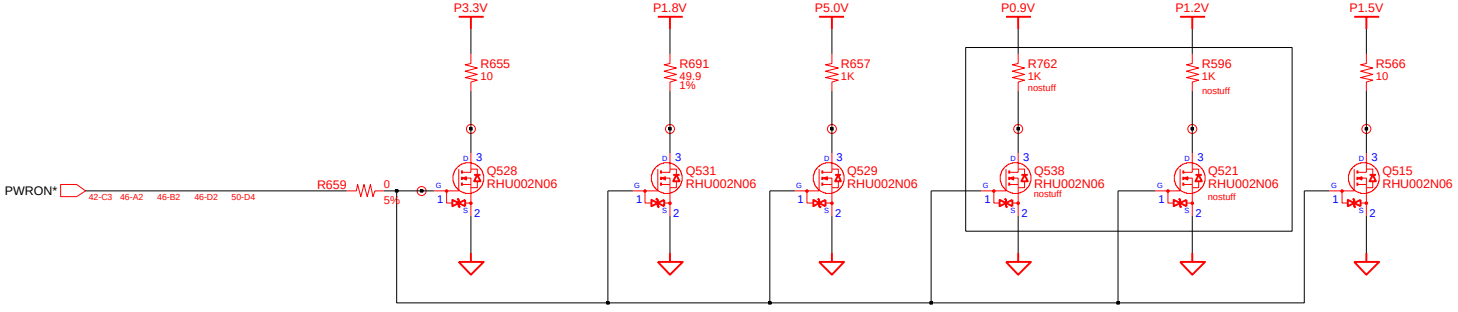
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 46 OF 52	

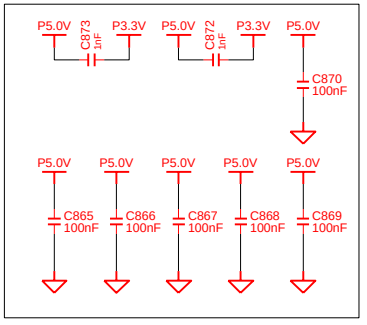




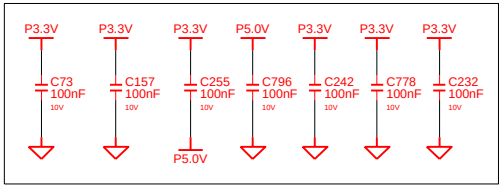
DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR	P1.2V & P2.5V AUX POWER	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00659A
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 47 OF 52	



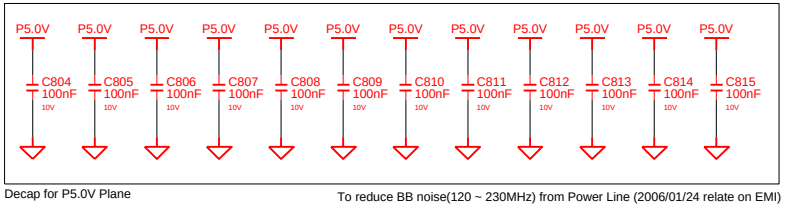




To enhance DMB performance(060206)

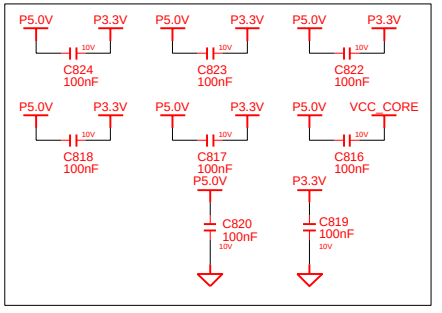


STICHING CAP



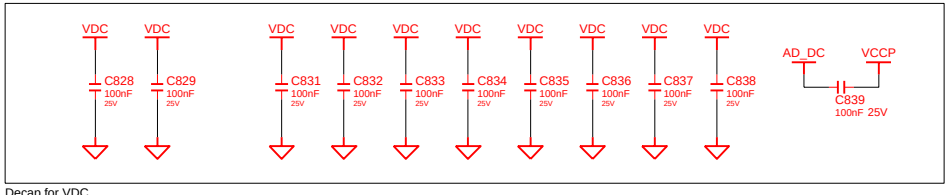
Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stiching Cap for Power partition

To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II MAINBD POWER ADAPT	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		PART NO.: BA41-00659A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 48 OF 52	

REV500

PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0	TP	PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 49 OF 52	

COEX1
COEX2
ILIM3
ILIM5
MIC1_L
MIC1_R
PWRON*
TV03_C
TV03_Y
IDE5_A0
IDE5_A1
IDE5_A2
ODD5_A0
ODD5_A1
ODD5_A2
PC_BEEP
RTC_CLK
AC_SDOUT
ADT3_SEL
AUTO_ON*

CPU1_TCK
CPU1_TDI
CPU1_TMS
CRT3_RED

HP_OUT_L
HP_OUT_R

CLK3_ICH14
CLK3_NB14M
CLK3_USB48

CRT3_BLUE
HDD3_LED*
IDE5_CS1*
IDE5_CS3*
IDE5_D(0)
IDE5_D(1)
IDE5_D(2)
IDE5_D(3)
IDE5_D(4)
IDE5_D(5)
IDE5_D(6)
IDE5_D(7)
IDE5_D(8)
IDE5_D(9)
IDE5_DREQ
IDE5_IOR*
IDE5_IOW*
KBC3_A20G
KBC3_RST*
KBC3_VRON
KBC5_TCLK
LAN3_ACT*

CRT3_GREEN
CRT5_HSYNC
CRT5_VSYNC
FWH1_INIT*
IDE5_D(10)
IDE5_D(11)
IDE5_D(12)
IDE5_D(13)
IDE5_D(14)
IDE5_D(15)
IDE5_DACK*
IDE5_DASP*
IDE5_IORDY
JCK_SENS_A
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC5_TDATA

ODD5_CS1*
ODD5_CS3*
ODD5_D(0)
ODD5_D(1)
ODD5_D(2)
ODD5_D(3)
ODD5_D(4)
ODD5_D(5)
ODD5_D(6)
ODD5_D(7)
ODD5_D(8)
ODD5_D(9)
ODD5_DREQ
ODD5_IOR*
ODD5_IOW*
ODD5_RST*
PCI3_CLK8
PCI3_RST*
SMB3_DATA
VGA5_DDCC
VGA5_DDCD
WLON_LED*
AUD3_EAPD*
CBS3_A_D_2
CBS3_CCD1*
CBS3_CCD2*
CBS3_CONT*
CBS3_CINT*
CBS3_CREQ*
CBS3_CRST*

LAN3_WAKE*

LCD3_VDDEN
LINE_OUT_L
LINE_OUT_R

ODD5_IRQ
PCI3_PAR
SMB3_CLK

CBS3_CCLK
CBS3_CPAR
CBS3_CVS1
CBS3_CVS2
CBS3_SPKR
CHP3_SPKR
CLK3_FM48

ODD5_D(10)
ODD5_D(11)
ODD5_D(12)
ODD5_D(13)
ODD5_D(14)
ODD5_D(15)
ODD5_DACK*
ODD5_IORDY
PCI3_AD(0)
PCI3_AD(1)
PCI3_AD(2)
PCI3_AD(3)

DRAW: TERMI KWON	DATE: 4/5/2006	TITLE: FIRENZE II	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: SR		
APPROVAL: SJ PARK	REV: 1.0	TP	PART NO.: BA41-00659A
MODULE CODE:	LAST EDIT: April 5, 2006 8:18:08 PM	PAGE 50 OF 52	

PCI3_AD(4)
PCI3_AD(5)
PCI3_AD(6)
PCI3_AD(7)
PCI3_AD(8)
PCI3_AD(9)
PCI3_CBE0*
PCI3_CBE1*
PCI3_CBE2*
PCI3_CBE3*
PCI3_GNT0*
PCI3_GNT1*
PCI3_GNT2*
PCI3_INTA*
PCI3_INTB*
PCI3_INTC*
PCI3_INTD*
PCI3_INTE*
PCI3_INTF*
PCI3_INTG*
PCI3_INTH*
PCI3_IRDY*
PCI3_PERR*
PCI3_REQ0*
PCI3_REQ1*
PCI3_REQ2*
PCI3_REQ3*
PCI3_RSTF*
PCI3_SERR*
PCI3_STOP*
PCI3_TRDY*

PLT3_RSTF*
THERM_STP*
T_L_BUTTON
T_R_BUTTON
VGA3_HSYNC
VGA3_VSYNC

AUD5_SPK_L+
AUD5_SPK_L-
AUD5_SPK_R+
AUD5_SPK_R-
BAT3_SMCLK*
BLT_DETECT*
CBS3_A_A_18
CBS3_A_A_19
CBS3_A_D_14
CBS3_CAD(0)
CBS3_CAD(1)
CBS3_CAD(2)
CBS3_CAD(3)
CBS3_CAD(4)
CBS3_CAD(5)
CBS3_CAD(6)
CBS3_CAD(7)
CBS3_CAD(8)
CBS3_CAD(9)
CBS3_CAUDIO
CBS3_CCBE0*
CBS3_CCBE1*
CBS3_CCBE2*
CBS3_CCBE3*
CBS3_CIRDY*
CBS3_CPERR*
CBS3_CSERR*
CBS3_CSTOP*
CBS3_CTRDY*
CBS3_MD_CLK
CBS3_VPPEN0
CBS3_VPPEN1
CHP3_BMREQ*
CHP3_NBRST*

CHP3_OVERT*
CHP3_SBPME*
CHP3_SERIRQ
CHP3_SLPS3*
CHP3_SLPS5*

CLK3_DBGLPC
CLK3_PCLKCB
CLK3_PWRGD*

CPU1_VID(0)
CPU1_VID(1)
CPU1_VID(2)
CPU1_VID(3)
CPU1_VID(4)
CPU1_VID(5)
CPU1_VID(6)
CRT3_DDCCLK
IDE5_IDEIRQ
KBC3_BKLTON
KBC3_SCLED*
KBC3_SMCLK*
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)

LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)

OTP3_OVERT*
PCI3_AD(10)

PCI3_AD(11)
PCI3_AD(12)
PCI3_AD(13)
PCI3_AD(14)
PCI3_AD(15)
PCI3_AD(16)
PCI3_AD(17)
PCI3_AD(18)
PCI3_AD(19)
PCI3_AD(20)
PCI3_AD(21)
PCI3_AD(22)
PCI3_AD(23)
PCI3_AD(24)
PCI3_AD(25)
PCI3_AD(26)
PCI3_AD(27)
PCI3_AD(28)
PCI3_AD(29)
PCI3_AD(30)
PCI3_AD(31)
PCI3_FRAME*
PCI3_PLOCK*
THRM_ALERT*
VCCP3_PWRGD
BAT3_DETECT*
BAT3_SMDATA*
CBS3_CAD(10)
CBS3_CAD(11)
CBS3_CAD(12)
CBS3_CAD(13)
CBS3_CAD(14)
CBS3_CAD(15)
CBS3_CAD(16)
CBS3_CAD(17)
CBS3_CAD(18)
CBS3_CAD(19)
CBS3_CAD(20)
CBS3_CAD(21)
CBS3_CAD(22)
CBS3_CAD(23)
CBS3_CAD(24)
CBS3_CAD(25)
CBS3_CAD(26)
CBS3_CAD(27)
CBS3_CAD(28)
CBS3_CAD(29)
CBS3_CAD(30)
CBS3_CAD(31)
CBS3_CFRAME*
CBS3_CSTSCHG
CBS3_VCC3EN*
CBS3_VCC5EN*
CHP3_AZ_SDI0
CHP3_AZ_SDI1
CHP3_BIOSWP*
CHP3_CPUSTP*
CHP3_NBPWRGD

CLK3_33M_MIN
CLK3_PCLKFWH
CLK3_PCLKLAN
CLK3_PCLKSIO

CPU1_CPURST*

CPU1_STPCLK*
CPU2_THERMDA
CPU2_THERMDC
CRT3_DDCDATA
ITP3_SYSRST*
JCK_SENS_HP*

KBC3_CHG3C

KBC3_CPURST*
KBC3_EXTSMI*
KBC3_FANCTRL
KBC3_NUMLED*
KBC3_PWRBTN*
KBC3_RSMRST*
KBC3_RUNSCI*
KBC3_SMDATA*
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)

LID3_SWITCH*
LPC3_LFRAME*

MIC1_VREFO_L
MIC1_VREFO_R
MIO3_BUTTON*
PCI3_CLKRUN*
PCI3_DEVSEL*
CBS3_CCLKRUN*
CBS3_CDEVSEL*
CBS3_MD_DATA1
CBS3_MD_DATA2
CBS3_MD_DATA3
CBS3_MD_VCCEN
CHP3_BIOSTBL*
CHP3_DPRSLPVR
CHP3_SUSSTAT*

CPU1_PWRGDCPU
CPU1_VCCSENSE
CPU1_VSSSENSE
JCK_SENS_MIC*
KBC3_CAPSLED*
KBC3_SUSPWRON
KBC3_WAKESCI*
LAN3_LINK_10*
LCD3_BKLTCTRL
LCD3_BKLTEN
LCD3_BKLTON

CBS3_MD_XD_ALE
CBS3_MD_XD_CE*
CBS3_MD_XD_CLE
CBS3_MD_XD_WP*

CLK3_PCLKMICOM
CPU1_THRMTRIP*
KBC3_LED_ACIN*
LAN3_LINK_100*
VRM3_CPU_PWRGD
CHP3_ALINK_RST*
CHP3_AZ_AUD_SDO
CHP3_AZ_MDC_SDO
CLK3_PCLKSIO_DS
KBC3_LED_POWER*
CBS3_MD_DATA4_XD
CBS3_MD_DATA5_XD
CBS3_MD_DATA6_XD
CBS3_MD_DATA7_XD
CHP3_AZ_AUD_BCLK
CHP3_AZ_AUD_RST*
CHP3_AZ_AUD_SYNC
CHP3_AZ_MDC_BCLK
CHP3_AZ_MDC_RST*
CHP3_AZ_MDC_SYNC
CHP3_SBTHRMTRIP*
KBC3_LED_CHARGE*
KBC3_THERM_SMCLK
CBS3_MS_BS_SD_CMD
KBC3_THERM_SMDATA
CBS3_SD_CD*_XD_CD*
CBS3_MS_INS*_XD_CD*
CBS3_SD_WP*_XD_R_B*
CBS3_MD_DATA0_MS_SDIO

AVDD
AVDD

AD_DC
AD_DC
AD_DC
AD_DC
AD_DC
AVDDQ

AVSSN

AVSSQ

AVSSDI

AMP_VDD
AMP_VDD

AVDD_CK

AVDD_NB

AGND_AUD
AGND_AUD
AGND_AUD
AGND_AUD
AGND_AUD
AGND_CHG

AGND_P3.3V

CGND

C_AGND

CB_VCCA

CB_VPPA

CHG_REF

CB_MD_VCC

D_AGND

GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND

INV_VDC
INV_VDC
LPVSS
LVSSR

LCD_VDD3V
LCD_VDD3V

LDO_P5.4V

MEM1_REF

MAX8550_REF

MICOM_P3.3V
MICOM_P3.3V

P0.9V
P0.9V
P0.9V
P0.9V
P0.9V
P1.2V
P1.2V
P1.2V
P1.2V
P1.5V
P1.5V

P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P3.3V

P3.3V
P3.3V
P3.3V
P3.3V
P5.0V
P5.0V
P5.0V
P5.0V
P5.0V
PLLVDD

PLLVSS

PRTC_BAT

P1.8V_ALW

P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P1.8V_AUX
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P2.5V_LAN
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P3.3V_AUX
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_ALW
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
PCIE_PVDD

PCIE_VDDR

P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
P12.0V_ALW
VDC
VDC
VDC
VDC
VDC
VCCP
VCCP
VCCP
VCCP
VCCP
VCC_NB

VCC_NB
VCC_NB
VCC_NB
VCC_NB

VCC_CRT

VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE